

# ***AM263x Register Addendum***

## ***Technical Reference Manual***

---



Literature Number: SPRUJ42G  
MARCH 2022 – REVISED SEPTEMBER 2026





# Table of Contents



|                                                            |      |
|------------------------------------------------------------|------|
| <b>Read This First</b>                                     | 7    |
| About This Register Addendum                               | 7    |
| Note on Register Names                                     | 7    |
| Glossary                                                   | 7    |
| Export Control Notice                                      | 7    |
| Related Documentation From Texas Instruments               | 8    |
| Support Resources                                          | 8    |
| Release History (Register Addendum)                        | 9    |
| <b>1 Memory Map</b>                                        | 12   |
| 1.1 Device Memory Map                                      | 13   |
| 1.2 R5FSS Memory Map                                       | 20   |
| 1.3 PRU-ICSS Memory Map                                    | 21   |
| <b>2 Control Module (CTRLMMR) Registers</b>                | 23   |
| 2.1 MMR Write Protection                                   | 24   |
| 2.2 MSS_CTRL                                               | 26   |
| 2.2.1 MSS_CTRL Summaries                                   | 26   |
| 2.2.2 MSS_CTRL Registers                                   | 40   |
| 2.3 TOP_CTRL                                               | 709  |
| 2.3.1 TOP_CTRL Summaries                                   | 709  |
| 2.3.2 TOP_CTRL Registers                                   | 710  |
| 2.4 MSS_IOMUX                                              | 790  |
| 2.4.1 MSS_IOMUX Summaries                                  | 790  |
| 2.4.2 MSS_IOMUX Registers                                  | 793  |
| 2.5 MSS_TOPRCM                                             | 1109 |
| 2.5.1 MSS_TOPRCM Summaries                                 | 1109 |
| 2.5.2 MSS_TOPRCM Registers                                 | 1111 |
| 2.6 MSS_RCM                                                | 1212 |
| 2.6.1 MSS_RCM Summaries                                    | 1212 |
| 2.6.2 MSS_RCM Registers                                    | 1218 |
| 2.7 CONTROLSS_GLOBAL_CTRL                                  | 1490 |
| 2.7.1 CONTROLSS_GLOBAL_CTRL Summaries                      | 1490 |
| 2.7.2 CONTROLSS_GLOBAL_CTRL Registers                      | 1496 |
| <b>3 Real-time Control Subsystem (CONTROLSS) Registers</b> | 1760 |
| 3.1 CONTROLSS 16-bit Register Access Note                  | 1760 |
| 3.2 ADC                                                    | 1761 |
| 3.2.1 ADC Summaries                                        | 1761 |
| 3.2.2 ADC Registers                                        | 1769 |
| 3.3 CMPSSA                                                 | 2018 |
| 3.3.1 CMPSSA Summaries                                     | 2018 |
| 3.3.2 CMPSSA Registers                                     | 2020 |
| 3.4 CMPSSB                                                 | 2049 |
| 3.4.1 CMPSSB Summaries                                     | 2049 |
| 3.4.2 CMPSSB Registers                                     | 2051 |
| 3.5 DAC                                                    | 2080 |
| 3.5.1 DAC Summaries                                        | 2080 |
| 3.5.2 DAC Registers                                        | 2080 |
| 3.6 ECAP                                                   | 2088 |
| 3.6.1 ECAP Summaries                                       | 2088 |
| 3.6.2 ECAP Registers                                       | 2091 |

|                                                   |             |
|---------------------------------------------------|-------------|
| 3.7 EPWM.....                                     | 2134        |
| 3.7.1 EPWM Summaries.....                         | 2134        |
| 3.7.2 EPWM Registers.....                         | 2306        |
| 3.8 EQEP.....                                     | 3031        |
| 3.8.1 EQEP Summaries.....                         | 3031        |
| 3.8.2 EQEP Registers.....                         | 3031        |
| 3.9 FSI_RX.....                                   | 3068        |
| 3.9.1 FSI_RX Summaries.....                       | 3068        |
| 3.9.2 FSI_RX Registers.....                       | 3070        |
| 3.10 FSI_TX.....                                  | 3118        |
| 3.10.1 FSI_TX Summaries.....                      | 3118        |
| 3.10.2 FSI_TX Registers.....                      | 3119        |
| 3.11 OTTOCAL.....                                 | 3148        |
| 3.11.1 OTTOCAL Summaries.....                     | 3148        |
| 3.11.2 OTTOCAL Registers.....                     | 3148        |
| 3.12 SDFM.....                                    | 3151        |
| 3.12.1 SDFM Summaries.....                        | 3151        |
| 3.12.2 SDFM Registers.....                        | 3153        |
| 3.13 CONTROLSS_DMAXBAR.....                       | 3246        |
| 3.13.1 CONTROLSS_DMAXBAR Summaries.....           | 3246        |
| 3.13.2 CONTROLSS_DMAXBAR Registers.....           | 3248        |
| 3.14 CONTROLSS_ICLXBAR.....                       | 3377        |
| 3.14.1 CONTROLSS_ICLXBAR Summaries.....           | 3377        |
| 3.14.2 CONTROLSS_ICLXBAR Registers.....           | 3378        |
| 3.15 CONTROLSS_INPUTXBAR.....                     | 3427        |
| 3.15.1 CONTROLSS_INPUTXBAR Summaries.....         | 3427        |
| 3.15.2 CONTROLSS_INPUTXBAR Registers.....         | 3429        |
| 3.16 CONTROLSS_INTXBAR.....                       | 3526        |
| 3.16.1 CONTROLSS_INTXBAR Summaries.....           | 3526        |
| 3.16.2 CONTROLSS_INTXBAR Registers.....           | 3531        |
| 3.17 CONTROLSS_MDLXBAR.....                       | 3788        |
| 3.17.1 CONTROLSS_MDLXBAR Summaries.....           | 3788        |
| 3.17.2 CONTROLSS_MDLXBAR Registers.....           | 3789        |
| 3.18 CONTROLSS_OUTPUTXBAR.....                    | 3838        |
| 3.18.1 CONTROLSS_OUTPUTXBAR Summaries.....        | 3838        |
| 3.18.2 CONTROLSS_OUTPUTXBAR Registers.....        | 3842        |
| 3.19 CONTROLSS_PWMSYNCOUXTBAR.....                | 4046        |
| 3.19.1 CONTROLSS_PWMSYNCOUXTBAR Summaries.....    | 4046        |
| 3.19.2 CONTROLSS_PWMSYNCOUXTBAR Registers.....    | 4046        |
| 3.20 CONTROLSS_PWMXBAR.....                       | 4051        |
| 3.20.1 CONTROLSS_PWMXBAR Summaries.....           | 4051        |
| 3.20.2 CONTROLSS_PWMXBAR Registers.....           | 4057        |
| 3.21 SoC_TIMESYNC_XBAR0.....                      | 4364        |
| 3.21.1 SoC_TIMESYNC_XBAR0 Summaries.....          | 4364        |
| 3.21.2 SoC_TIMESYNC_XBAR0 Registers.....          | 4364        |
| 3.22 SoC_TIMESYNC_XBAR1.....                      | 4367        |
| 3.22.1 SoC_TIMESYNC_XBAR1 Summaries.....          | 4367        |
| 3.22.2 SoC_TIMESYNC_XBAR1 Registers.....          | 4367        |
| <b>4 Processor and Accelerator Registers.....</b> | <b>4370</b> |
| 4.1 R5SS.....                                     | 4371        |
| 4.1.1 R5SS Summaries.....                         | 4371        |
| 4.1.2 R5SS Registers.....                         | 4377        |
| 4.2 ICSSM.....                                    | 4588        |
| 4.2.1 ICSSM Summaries.....                        | 4588        |
| 4.2.2 ICSSM Registers.....                        | 4602        |
| 4.3 ICSSM_XBAR_INTR.....                          | 5116        |
| 4.3.1 ICSSM_XBAR_INTR Summaries.....              | 5116        |
| 4.3.2 ICSSM_XBAR_INTR Registers.....              | 5116        |
| 4.4 EDMA.....                                     | 5119        |
| 4.4.1 EDMA Summaries.....                         | 5119        |
| 4.4.2 EDMA Registers.....                         | 5122        |

|                                              |             |
|----------------------------------------------|-------------|
| 4.5 EDMA_TRIGXBAR_INTR.....                  | 5365        |
| 4.5.1 EDMA_TRIGXBAR_INTR Summaries.....      | 5365        |
| 4.5.2 EDMA_TRIGXBAR_INTR Registers.....      | 5365        |
| <b>5 System-on-chip (SoC) Registers.....</b> | <b>5368</b> |
| 5.1 CPSW.....                                | 5369        |
| 5.1.1 CPSW Summaries.....                    | 5369        |
| 5.1.2 CPSW Registers.....                    | 5379        |
| 5.2 DCC.....                                 | 5846        |
| 5.2.1 DCC Summaries.....                     | 5846        |
| 5.2.2 DCC Registers.....                     | 5846        |
| 5.3 ECC_AGGR.....                            | 5867        |
| 5.3.1 ECC_AGGR Summaries.....                | 5867        |
| 5.3.2 ECC_AGGR Registers.....                | 5867        |
| 5.4 ELM.....                                 | 5891        |
| 5.4.1 ELM Summaries.....                     | 5891        |
| 5.4.2 ELM Registers.....                     | 5891        |
| 5.5 ESM.....                                 | 5922        |
| 5.5.1 ESM Summaries.....                     | 5922        |
| 5.5.2 ESM Registers.....                     | 5922        |
| 5.6 EXT_FLASH.....                           | 5952        |
| 5.6.1 EXT_FLASH Summaries.....               | 5952        |
| 5.6.2 EXT_FLASH Registers.....               | 5952        |
| 5.7 GPIO.....                                | 5955        |
| 5.7.1 GPIO Summaries.....                    | 5955        |
| 5.7.2 GPIO Registers.....                    | 5957        |
| 5.8 GPIO_XBAR_INTR.....                      | 6011        |
| 5.8.1 GPIO_XBAR_INTR Summaries.....          | 6011        |
| 5.8.2 GPIO_XBAR_INTR Registers.....          | 6011        |
| 5.9 GPMC.....                                | 6014        |
| 5.9.1 GPMC Summaries.....                    | 6014        |
| 5.9.2 GPMC Registers.....                    | 6015        |
| 5.10 I2C.....                                | 6064        |
| 5.10.1 I2C Summaries.....                    | 6064        |
| 5.10.2 I2C Registers.....                    | 6065        |
| 5.11 LIN.....                                | 6095        |
| 5.11.1 LIN Summaries.....                    | 6095        |
| 5.11.2 LIN Registers.....                    | 6097        |
| 5.12 MCAN.....                               | 6167        |
| 5.12.1 MCAN Summaries.....                   | 6167        |
| 5.12.2 MCAN Registers.....                   | 6171        |
| 5.13 MCRC.....                               | 6269        |
| 5.13.1 MCRC Summaries.....                   | 6269        |
| 5.13.2 MCRC Registers.....                   | 6270        |
| 5.14 MCSPI.....                              | 6343        |
| 5.14.1 MCSPI Summaries.....                  | 6343        |
| 5.14.2 MCSPI Registers.....                  | 6344        |
| 5.15 MMCSD.....                              | 6403        |
| 5.15.1 MMCSD Summaries.....                  | 6403        |
| 5.15.2 MMCSD Registers.....                  | 6404        |
| 5.16 MPU_8.....                              | 6489        |
| 5.16.1 MPU_8 Summaries.....                  | 6489        |
| 5.16.2 MPU_8 Registers.....                  | 6494        |
| 5.17 MPU_16.....                             | 6537        |
| 5.17.1 MPU_16 Summaries.....                 | 6537        |
| 5.17.2 MPU_16 Registers.....                 | 6538        |
| 5.18 MSRAM.....                              | 6611        |
| 5.18.1 MSRAM Summaries.....                  | 6611        |
| 5.18.2 MSRAM Registers.....                  | 6611        |
| 5.19 MSS_MBOX.....                           | 6614        |
| 5.19.1 MSS_MBOX Summaries.....               | 6614        |
| 5.19.2 MSS_MBOX Registers.....               | 6614        |

|                                |      |
|--------------------------------|------|
| 5.20 PBIST.....                | 6617 |
| 5.20.1 PBIST Summaries.....    | 6617 |
| 5.20.2 PBIST Registers.....    | 6617 |
| 5.21 QSPI.....                 | 6630 |
| 5.21.1 QSPI Summaries.....     | 6630 |
| 5.21.2 QSPI Registers.....     | 6630 |
| 5.22 RTI.....                  | 6661 |
| 5.22.1 RTI Summaries.....      | 6661 |
| 5.22.2 RTI Registers.....      | 6663 |
| 5.23 SPINLOCK.....             | 6716 |
| 5.23.1 SPINLOCK Summaries..... | 6716 |
| 5.23.2 SPINLOCK Registers..... | 6716 |
| 5.24 UART.....                 | 6722 |
| 5.24.1 UART Summaries.....     | 6722 |
| 5.24.2 UART Registers.....     | 6725 |
| 5.25 WDT.....                  | 6814 |
| 5.25.1 WDT Summaries.....      | 6814 |
| 5.25.2 WDT Registers.....      | 6816 |



## About This Register Addendum

This Register Addendum (RA) provides detailed register references for each peripheral and subsystem in the device including:

- Register Address
- Register Name
- Register Types
- Register Reset Values
- Register Descriptions
- Bit-field Descriptions

---

### Note

This Register Addendum has been created in order to make the Technical Reference Manual a more effective and size-efficient collateral document. The AM263x Technical Reference Manual can be downloaded at <https://www.ti.com/lit/SPRUJ17>.

---

### Note on Register Names

Rev E now aligns register names with sub section headers and figure titles.

### Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

### Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

## **Related Documentation From Texas Instruments**

For a complete listing of related documentation and development-support tools for the device, visit the Texas Instruments website at [www.ti.com](http://www.ti.com).

## **AM263x Collateral Links**

### AM263x Documentation

- [AM263x Data sheet](#)
- [AM263x Errata](#)
- [AM263x Technical Reference Manual](#)
  - Technical Reference Manual contains programming guides at the end of select IPs' chapters
- [AM263x Register Addendum](#)
  - Register addendum contains device register information and associated content
- [AM263x Hardware Design Guidelines](#)

### AM263x Software

- [Sitara MCU+ Academy for AM263x](#)
  - Texas Instruments offers the MCU+ Academy as a resource for designing with the MCU+ software and tools on supported devices.
  - The MCU+ Academy features easy-to-use training modules that range from the basics of getting started to advanced development topics.
- [MCU-PLUS-SDK-AM263x](#)

### AM263x Product Folders

- [AM2634 Product Folder](#)
- [AM2632 Product Folder](#)
- [AM2631 Product Folder](#)

### AM263x Evaluation Modules

- [AM263x Control Card \(TMDSCNCD263\)](#)
- [AM263x LaunchPad \(LP-AM263\)](#)

## **Support Resources**

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

## Release History (Register Addendum)

The below table summarizes Register Addendum versions and changes.

| Version | Literature Number | Date           | Notes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|---------|-------------------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| *1      | SPRUJ42*1         | March 2022     | Initial Creation                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| -       | SPRUJ42           | April 2022     | Original Release<br>Added Read This First Content                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| A       | SPRUJ42A          | September 2022 | <p>Memory Map Updates:</p> <ul style="list-style-type: none"> <li>Core-specific Memory Maps added</li> </ul> <p>Updates included for the following CTRLMMR Registers:</p> <ul style="list-style-type: none"> <li>TOP_CTRL</li> <li>MSS_CTRL</li> <li>MSS_IOMUX</li> <li>MSS_TOPRCM</li> <li>MSS_RCM</li> </ul> <p>CONTROLSS_EPWM Register Descriptions Added</p> <p>Updates included for the following CONTROLSS Registers:</p> <ul style="list-style-type: none"> <li>CONTROLSS_ADC*</li> <li>CONTROLSS_CMPSS*</li> <li>CONTROLSS_DAC</li> <li>CONTROLSS_ECAP</li> <li>CONTROLSS_EQEP</li> <li>CONTROLSS_FSI*</li> <li>CONTROLSS_GLOBAL_CTRL</li> <li>CONTROLSS_*XBAR</li> </ul> <p>Updates included for the following SoC Registers</p> <ul style="list-style-type: none"> <li>MSS_GPIO</li> <li>MSS_LIN</li> <li>MSS_SPINLOCK</li> </ul> |
| B       | SPRUJ42B          | October 2022   | <p>Updates included for the following CTRLMMR Registers:</p> <ul style="list-style-type: none"> <li>TOP_CTRL</li> <li>MSS_CTRL</li> <li>MSS_IOMUX</li> <li>MSS_TOPRCM</li> <li>MSS_RCM</li> </ul> <p>Updates included for the following CONTROLSS Registers:</p> <ul style="list-style-type: none"> <li>CONTROLSS_CMPSS*</li> <li>CONTROLSS_ECAP</li> <li>CONTROLSS_EQEP</li> <li>CONTROLSS_GLOBAL_CTRL</li> <li>CONTROLSS_*XBAR</li> </ul> <p>Updates included for the following SoC Registers</p> <ul style="list-style-type: none"> <li>XBAR and INTR Registers</li> <li>MSS_*</li> </ul>                                                                                                                                                                                                                                                |

| Version | Literature Number | Date          | Notes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|---------|-------------------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| C       | SPRUJ42C          | December 2022 | <p>Updates in general register description layout applied across document.</p> <p>PRU-ICSS Registers Added</p> <p>CONTROLSS_EPWM Registers Added</p> <p>Updates included for the following CTRLMMR Registers:</p> <ul style="list-style-type: none"> <li>• TOP_CTRL</li> <li>• MSS_CTRL</li> <li>• MSS_IOMUX</li> <li>• MSS_TOPRCM</li> <li>• MSS_RCM</li> </ul> <p>Updates included for the following SoC Registers</p> <ul style="list-style-type: none"> <li>• XBAR and INTR Registers</li> <li>• MSS_*</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| D       | SPRUJ42D          | December 2023 | <ul style="list-style-type: none"> <li>• Aligned register reset values in tables and images</li> <li>• Update register names with nomenclature used in other register addendums <ul style="list-style-type: none"> <li>– Uncompressed instances and registers in EPWM.</li> <li>– Removed "n" variable from register nomenclature from CMPSSA, CMPSSB, ECAP, EQEP, FSI_RX, FSI_TX, OTTOCAL, R5SS, DCC, MCAN, MCRC, RTI, UART, and SDFM</li> </ul> </li> <li>• Adding missing figures. ESM, GPIO, I2C, and INPUTXBAR still need missing figures added</li> <li>• CPSW combined into one chapter</li> <li>• TCM, TCMA, TCMB, CCMR, and STC moved into R5SS_Core chapter</li> <li>• Combined TPTC and TPCC chapter into EDMA chapter</li> <li>• Removed chapter CTRLMMR_CONTROLSS_GLOBAL_CTRL which was one page linking to another chapter</li> <li>• MCAN chapters combined into one chapter</li> <li>• Changed AGG to AGGR</li> <li>• TSXBAR_INTR renamed to SoC_TIMESYNC_XBAR0</li> <li>• SOC_TSXBAR_INTR chapter renamed to SoC_TIMESYNC_XBAR1 and moved to 3.24</li> <li>• TOP PBIST renamed to PBIST with instance name of PBIST0</li> <li>• CMPSS instances renamed to CMPSS12B. Names to align with CMPSSA in future revision</li> <li>• Global Control Registers have register name changes from epwm to etpwm and cmpssb to cmpss*b0.</li> <li>• Added GPMC, ELM, and WDT chapters</li> </ul> |



| Version | Literature Number | Date           | Notes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|---------|-------------------|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| E       | SPRUJ42E          | October 2024   | <ul style="list-style-type: none"> <li>Added MPU_16 and MPU_8 chapters</li> <li>Added new section for Processor and Accelerator Registers</li> <li>Aligned CMPSSB register names with CMPSSA register names</li> <li>ADC_CFG and ADC_RESULT_REGS have been compacted into ADC</li> <li>Individual ADC registers have been compacted to reflect ADC0-4 with minimal duplicate registers</li> <li>Numerous CPSW registers compacted with offset formulas to reduce chapter size</li> <li>Appended TPCC and TPTC to EDMA register names to better differentiate the different IP blocks</li> <li>Top Level Register Name updates: <ul style="list-style-type: none"> <li>RFSS_CORE to R5SS</li> <li>PRU-ICSS to ICSSM</li> <li>PRU_ICSS_XBAR_INTR to ICSSM_XBAR_INTR</li> <li>EDMA_TRIGGER_XBAR_INTROUTER to EDMA_TRIGXBAR_INTR</li> <li>ECC_AGG_TOP to ECC_AGGR</li> <li>MSS_LIN to LIN</li> <li>TOP_ESM to ESM</li> </ul> </li> <li>Updated IP and instance names across large portions of the document</li> <li>Register name updates to align with software names applied across large portions of the document</li> <li>Organized SoC peripherals by alphabet like Control Subsystem</li> <li>Resolved document-wide issues with incorrect reset values and offsets</li> <li>Updated PBIST Registers Base Address from "0x5330 0200" to "0x5330 0000"</li> </ul> |
| F       | SPRUJ42F          | September 2026 | <ul style="list-style-type: none"> <li>Declassified MSS_CTRL_DEBUGSS_STM_NSGUAREN</li> <li>Added a PG_VER bitfield in EFUSE1_ROW15 register and added a EFUSE_MODE_CTRL bitfield in TOP_CTRL_HW_SPARE_RW0 register</li> <li>Updated bitfield dewscription of OE_OVERRIDE, OE_OVERRIDE_CTRL, IE_OVERRIDE and IE_OVERRIDE_CTRL in all *_CFG_REG registers. Updated bitfield description in IOMUX_PADGLBL_CFG_REG</li> <li>Updated the physical addresses of EPWM registers</li> <li>Updated description of bitfields, PWMXBARx_G0_SEL in CONTROLSS_PWMXBARx_G0 register and PWMXBARx_G1_SEL in CONTROLSS_PWMXBARx_G1 register</li> <li>Updated description of bitfield WWDSize in RTI_RTIWWDSizeCTRL Register.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| G       | SPRUJ42G          | September 2026 | Updated PG_VER bitfield description in EFUSE1_ROW15 register in TOP_CTRL.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |



This chapter summarizes the memory map address regions for the device.

|                                     |           |
|-------------------------------------|-----------|
| <b>1.1 Device Memory Map.....</b>   | <b>13</b> |
| <b>1.2 R5FSS Memory Map.....</b>    | <b>20</b> |
| <b>1.3 PRU-ICSS Memory Map.....</b> | <b>21</b> |

## 1.1 Device Memory Map

This section describes the device memory map.

### Note

The memory locations not shown are either unallocated or reserved and not used.

Accesses to these locations are not recommended and must be avoided.

**Table 1-1. AM263x Memory Map**

| Region Name                                      | Start Address | End Address | Size      |
|--------------------------------------------------|---------------|-------------|-----------|
| Core-specific Internal Memory Map <sup>(1)</sup> | 0x0000 0000   | 0x1FFF FFFF | 512MB     |
| MCRC0                                            | 0x3500 0000   | 0x3500 03FF | 1 KB      |
| MPU_L2OCRAM_BANK0                                | 0x4002 0000   | 0x4002 0FFF | 4 KB      |
| MPU_L2OCRAM_BANK1                                | 0x4004 0000   | 0x4004 0FFF | 4 KB      |
| MPU_L2OCRAM_BANK2                                | 0x4006 0000   | 0x4006 0FFF | 4 KB      |
| MPU_L2OCRAM_BANK3                                | 0x4008 0000   | 0x4008 0FFF | 4 KB      |
| MPU_R5FSS0_CORE0_AXIS                            | 0x400A 0000   | 0x400A 0FFF | 4 KB      |
| MPU_R5FSS0_CORE1_AXIS                            | 0x400C 0000   | 0x400C 0FFF | 4 KB      |
| MPU_R5FSS1_CORE0_AXIS                            | 0x400E 0000   | 0x400E 0FFF | 4 KB      |
| MPU_R5FSS1_CORE1_AXIS                            | 0x4010 0000   | 0x4010 0FFF | 4 KB      |
| MPU_MBOX_SRAM                                    | 0x4014 0000   | 0x4014 0FFF | 4 KB      |
| MPU_QSPI0                                        | 0x4016 0000   | 0x4016 0FFF | 4 KB      |
| MPU_SCRM2SCRPO                                   | 0x4018 0000   | 0x4018 0FFF | 4 KB      |
| MPU_SCRM2SCRPI                                   | 0x401A 0000   | 0x401A 0FFF | 4 KB      |
| MPU_R5FSS0_CORE0_AHB                             | 0x401C 0000   | 0x401C 0FFF | 4 KB      |
| MPU_R5FSS0_CORE1_AHB                             | 0x401E 0000   | 0x401E 0FFF | 4 KB      |
| MPU_R5FSS1_CORE0_AHB                             | 0x4020 0000   | 0x4020 0FFF | 4 KB      |
| MPU_R5FSS1_CORE1_AHB                             | 0x4022 0000   | 0x4022 0FFF | 4 KB      |
| ICSS0_INTERNAL <sup>(1)</sup>                    | 0x4800 0000   | 0x4803 FFFF | 256 KB    |
| ICSS0_ECC                                        | 0x4810 0000   | 0x4810 03FF | 1 KB      |
| QSPI0                                            | 0x4820 0000   | 0x4820 01FF | 512 Bytes |
| MMC0                                             | 0x4830 0000   | 0x4830 1FFF | 8 KB      |
| GPMC0_CFG                                        | 0x4840 0000   | 0x4840 03FF | 1 KB      |
| CONTROLSS_G0_EPWM0                               | 0x5000 0000   | 0x5000 0FFF | 4 KB      |
| CONTROLSS_G0_EPWM1                               | 0x5000 1000   | 0x5000 1FFF | 4 KB      |
| CONTROLSS_G0_EPWM2                               | 0x5000 2000   | 0x5000 2FFF | 4 KB      |
| CONTROLSS_G0_EPWM3                               | 0x5000 3000   | 0x5000 3FFF | 4 KB      |
| CONTROLSS_G0_EPWM4                               | 0x5000 4000   | 0x5000 4FFF | 4 KB      |
| CONTROLSS_G0_EPWM5                               | 0x5000 5000   | 0x5000 5FFF | 4 KB      |
| CONTROLSS_G0_EPWM6                               | 0x5000 6000   | 0x5000 6FFF | 4 KB      |
| CONTROLSS_G0_EPWM7                               | 0x5000 7000   | 0x5000 7FFF | 4 KB      |
| CONTROLSS_G0_EPWM8                               | 0x5000 8000   | 0x5000 8FFF | 4 KB      |
| CONTROLSS_G0_EPWM9                               | 0x5000 9000   | 0x5000 9FFF | 4 KB      |
| CONTROLSS_G0_EPWM10                              | 0x5000 A000   | 0x5000 AFFF | 4 KB      |
| CONTROLSS_G0_EPWM11                              | 0x5000 B000   | 0x5000 BFFF | 4 KB      |
| CONTROLSS_G0_EPWM12                              | 0x5000 C000   | 0x5000 CFFF | 4 KB      |
| CONTROLSS_G0_EPWM13                              | 0x5000 D000   | 0x5000 DFFF | 4 KB      |

**Table 1-1. AM263x Memory Map (continued)**

| Region Name         | Start Address | End Address | Size |
|---------------------|---------------|-------------|------|
| CONTROLSS_G0_EPWM14 | 0x5000 E000   | 0x5000 EFFF | 4 KB |
| CONTROLSS_G0_EPWM15 | 0x5000 F000   | 0x5000 FFFF | 4 KB |
| CONTROLSS_G0_EPWM16 | 0x5001 0000   | 0x5001 0FFF | 4 KB |
| CONTROLSS_G0_EPWM17 | 0x5001 1000   | 0x5001 1FFF | 4 KB |
| CONTROLSS_G0_EPWM18 | 0x5001 2000   | 0x5001 2FFF | 4 KB |
| CONTROLSS_G0_EPWM19 | 0x5001 3000   | 0x5001 3FFF | 4 KB |
| CONTROLSS_G0_EPWM20 | 0x5001 4000   | 0x5001 4FFF | 4 KB |
| CONTROLSS_G0_EPWM21 | 0x5001 5000   | 0x5001 5FFF | 4 KB |
| CONTROLSS_G0_EPWM22 | 0x5001 6000   | 0x5001 6FFF | 4 KB |
| CONTROLSS_G0_EPWM23 | 0x5001 7000   | 0x5001 7FFF | 4 KB |
| CONTROLSS_G0_EPWM24 | 0x5001 8000   | 0x5001 8FFF | 4 KB |
| CONTROLSS_G0_EPWM25 | 0x5001 9000   | 0x5001 9FFF | 4 KB |
| CONTROLSS_G0_EPWM26 | 0x5001 A000   | 0x5001 AFFF | 4 KB |
| CONTROLSS_G0_EPWM27 | 0x5001 B000   | 0x5001 BFFF | 4 KB |
| CONTROLSS_G0_EPWM28 | 0x5001 C000   | 0x5001 CFFF | 4 KB |
| CONTROLSS_G0_EPWM29 | 0x5001 D000   | 0x5001 DFFF | 4 KB |
| CONTROLSS_G0_EPWM30 | 0x5001 E000   | 0x5001 EFFF | 4 KB |
| CONTROLSS_G0_EPWM31 | 0x5001 F000   | 0x5001 FFFF | 4 KB |
| CONTROLSS_G1_EPWM0  | 0x5004 0000   | 0x5004 0FFF | 4 KB |
| CONTROLSS_G1_EPWM1  | 0x5004 1000   | 0x5004 1FFF | 4 KB |
| CONTROLSS_G1_EPWM2  | 0x5004 2000   | 0x5004 2FFF | 4 KB |
| CONTROLSS_G1_EPWM3  | 0x5004 3000   | 0x5004 3FFF | 4 KB |
| CONTROLSS_G1_EPWM4  | 0x5004 4000   | 0x5004 4FFF | 4 KB |
| CONTROLSS_G1_EPWM5  | 0x5004 5000   | 0x5004 5FFF | 4 KB |
| CONTROLSS_G1_EPWM6  | 0x5004 6000   | 0x5004 6FFF | 4 KB |
| CONTROLSS_G1_EPWM7  | 0x5004 7000   | 0x5004 7FFF | 4 KB |
| CONTROLSS_G1_EPWM8  | 0x5004 8000   | 0x5004 8FFF | 4 KB |
| CONTROLSS_G1_EPWM9  | 0x5004 9000   | 0x5004 9FFF | 4 KB |
| CONTROLSS_G1_EPWM10 | 0x5004 A000   | 0x5004 AFFF | 4 KB |
| CONTROLSS_G1_EPWM11 | 0x5004 B000   | 0x5004 BFFF | 4 KB |
| CONTROLSS_G1_EPWM12 | 0x5004 C000   | 0x5004 CFFF | 4 KB |
| CONTROLSS_G1_EPWM13 | 0x5004 D000   | 0x5004 DFFF | 4 KB |
| CONTROLSS_G1_EPWM14 | 0x5004 E000   | 0x5004 EFFF | 4 KB |
| CONTROLSS_G1_EPWM15 | 0x5004 F000   | 0x5004 FFFF | 4 KB |
| CONTROLSS_G1_EPWM16 | 0x5005 0000   | 0x5005 0FFF | 4 KB |
| CONTROLSS_G1_EPWM17 | 0x5005 1000   | 0x5005 1FFF | 4 KB |
| CONTROLSS_G1_EPWM18 | 0x5005 2000   | 0x5005 2FFF | 4 KB |
| CONTROLSS_G1_EPWM19 | 0x5005 3000   | 0x5005 3FFF | 4 KB |
| CONTROLSS_G1_EPWM20 | 0x5005 4000   | 0x5005 4FFF | 4 KB |
| CONTROLSS_G1_EPWM21 | 0x5005 5000   | 0x5005 5FFF | 4 KB |
| CONTROLSS_G1_EPWM22 | 0x5005 6000   | 0x5005 6FFF | 4 KB |
| CONTROLSS_G1_EPWM23 | 0x5005 7000   | 0x5005 7FFF | 4 KB |
| CONTROLSS_G1_EPWM24 | 0x5005 8000   | 0x5005 8FFF | 4 KB |
| CONTROLSS_G1_EPWM25 | 0x5005 9000   | 0x5005 9FFF | 4 KB |
| CONTROLSS_G1_EPWM26 | 0x5005 A000   | 0x5005 AFFF | 4 KB |

**Table 1-1. AM263x Memory Map (continued)**

| Region Name         | Start Address | End Address | Size |
|---------------------|---------------|-------------|------|
| CONTROLSS_G1_EPWM27 | 0x5005 B000   | 0x5005 BFFF | 4 KB |
| CONTROLSS_G1_EPWM28 | 0x5005 C000   | 0x5005 CFFF | 4 KB |
| CONTROLSS_G1_EPWM29 | 0x5005 D000   | 0x5005 DFFF | 4 KB |
| CONTROLSS_G1_EPWM30 | 0x5005 E000   | 0x5005 EFFF | 4 KB |
| CONTROLSS_G1_EPWM31 | 0x5005 F000   | 0x5005 FFFF | 4 KB |
| CONTROLSS_G2_EPWM0  | 0x5008 0000   | 0x5008 0FFF | 4 KB |
| CONTROLSS_G2_EPWM1  | 0x5008 1000   | 0x5008 1FFF | 4 KB |
| CONTROLSS_G2_EPWM2  | 0x5008 2000   | 0x5008 2FFF | 4 KB |
| CONTROLSS_G2_EPWM3  | 0x5008 3000   | 0x5008 3FFF | 4 KB |
| CONTROLSS_G2_EPWM4  | 0x5008 4000   | 0x5008 4FFF | 4 KB |
| CONTROLSS_G2_EPWM5  | 0x5008 5000   | 0x5008 5FFF | 4 KB |
| CONTROLSS_G2_EPWM6  | 0x5008 6000   | 0x5008 6FFF | 4 KB |
| CONTROLSS_G2_EPWM7  | 0x5008 7000   | 0x5008 7FFF | 4 KB |
| CONTROLSS_G2_EPWM8  | 0x5008 8000   | 0x5008 8FFF | 4 KB |
| CONTROLSS_G2_EPWM9  | 0x5008 9000   | 0x5008 9FFF | 4 KB |
| CONTROLSS_G2_EPWM10 | 0x5008 A000   | 0x5008 AFFF | 4 KB |
| CONTROLSS_G2_EPWM11 | 0x5008 B000   | 0x5008 BFFF | 4 KB |
| CONTROLSS_G2_EPWM12 | 0x5008 C000   | 0x5008 CFFF | 4 KB |
| CONTROLSS_G2_EPWM13 | 0x5008 D000   | 0x5008 DFFF | 4 KB |
| CONTROLSS_G2_EPWM14 | 0x5008 E000   | 0x5008 EFFF | 4 KB |
| CONTROLSS_G2_EPWM15 | 0x5008 F000   | 0x5008 FFFF | 4 KB |
| CONTROLSS_G2_EPWM16 | 0x5009 0000   | 0x5009 0FFF | 4 KB |
| CONTROLSS_G2_EPWM17 | 0x5009 1000   | 0x5009 1FFF | 4 KB |
| CONTROLSS_G2_EPWM18 | 0x5009 2000   | 0x5009 2FFF | 4 KB |
| CONTROLSS_G2_EPWM19 | 0x5009 3000   | 0x5009 3FFF | 4 KB |
| CONTROLSS_G2_EPWM20 | 0x5009 4000   | 0x5009 4FFF | 4 KB |
| CONTROLSS_G2_EPWM21 | 0x5009 5000   | 0x5009 5FFF | 4 KB |
| CONTROLSS_G2_EPWM22 | 0x5009 6000   | 0x5009 6FFF | 4 KB |
| CONTROLSS_G2_EPWM23 | 0x5009 7000   | 0x5009 7FFF | 4 KB |
| CONTROLSS_G2_EPWM24 | 0x5009 8000   | 0x5009 8FFF | 4 KB |
| CONTROLSS_G2_EPWM25 | 0x5009 9000   | 0x5009 9FFF | 4 KB |
| CONTROLSS_G2_EPWM26 | 0x5009 A000   | 0x5009 AFFF | 4 KB |
| CONTROLSS_G2_EPWM27 | 0x5009 B000   | 0x5009 BFFF | 4 KB |
| CONTROLSS_G2_EPWM28 | 0x5009 C000   | 0x5009 CFFF | 4 KB |
| CONTROLSS_G2_EPWM29 | 0x5009 D000   | 0x5009 DFFF | 4 KB |
| CONTROLSS_G2_EPWM30 | 0x5009 E000   | 0x5009 EFFF | 4 KB |
| CONTROLSS_G2_EPWM31 | 0x5009 F000   | 0x5009 FFFF | 4 KB |
| CONTROLSS_G3_EPWM0  | 0x500C 0000   | 0x500C 0FFF | 4 KB |
| CONTROLSS_G3_EPWM1  | 0x500C 1000   | 0x500C 1FFF | 4 KB |
| CONTROLSS_G3_EPWM2  | 0x500C 2000   | 0x500C 2FFF | 4 KB |
| CONTROLSS_G3_EPWM3  | 0x500C 3000   | 0x500C 3FFF | 4 KB |
| CONTROLSS_G3_EPWM4  | 0x500C 4000   | 0x500C 4FFF | 4 KB |
| CONTROLSS_G3_EPWM5  | 0x500C 5000   | 0x500C 5FFF | 4 KB |
| CONTROLSS_G3_EPWM6  | 0x500C 6000   | 0x500C 6FFF | 4 KB |
| CONTROLSS_G3_EPWM7  | 0x500C 7000   | 0x500C 7FFF | 4 KB |

**Table 1-1. AM263x Memory Map (continued)**

| Region Name           | Start Address | End Address | Size |
|-----------------------|---------------|-------------|------|
| CONTROLSS_G3_EPWM8    | 0x500C 8000   | 0x500C 8FFF | 4 KB |
| CONTROLSS_G3_EPWM9    | 0x500C 9000   | 0x500C 9FFF | 4 KB |
| CONTROLSS_G3_EPWM10   | 0x500C A000   | 0x500C AFFF | 4 KB |
| CONTROLSS_G3_EPWM11   | 0x500C B000   | 0x500C BFFF | 4 KB |
| CONTROLSS_G3_EPWM12   | 0x500C C000   | 0x500C CFFF | 4 KB |
| CONTROLSS_G3_EPWM13   | 0x500C D000   | 0x500C DFFF | 4 KB |
| CONTROLSS_G3_EPWM14   | 0x500C E000   | 0x500C EFFF | 4 KB |
| CONTROLSS_G3_EPWM15   | 0x500C F000   | 0x500C FFFF | 4 KB |
| CONTROLSS_G3_EPWM16   | 0x500D 0000   | 0x500D 0FFF | 4 KB |
| CONTROLSS_G3_EPWM17   | 0x500D 1000   | 0x500D 1FFF | 4 KB |
| CONTROLSS_G3_EPWM18   | 0x500D 2000   | 0x500D 2FFF | 4 KB |
| CONTROLSS_G3_EPWM19   | 0x500D 3000   | 0x500D 3FFF | 4 KB |
| CONTROLSS_G3_EPWM20   | 0x500D 4000   | 0x500D 4FFF | 4 KB |
| CONTROLSS_G3_EPWM21   | 0x500D 5000   | 0x500D 5FFF | 4 KB |
| CONTROLSS_G3_EPWM22   | 0x500D 6000   | 0x500D 6FFF | 4 KB |
| CONTROLSS_G3_EPWM23   | 0x500D 7000   | 0x500D 7FFF | 4 KB |
| CONTROLSS_G3_EPWM24   | 0x500D 8000   | 0x500D 8FFF | 4 KB |
| CONTROLSS_G3_EPWM25   | 0x500D 9000   | 0x500D 9FFF | 4 KB |
| CONTROLSS_G3_EPWM26   | 0x500D A000   | 0x500D AFFF | 4 KB |
| CONTROLSS_G3_EPWM27   | 0x500D B000   | 0x500D BFFF | 4 KB |
| CONTROLSS_G3_EPWM28   | 0x500D C000   | 0x500D CFFF | 4 KB |
| CONTROLSS_G3_EPWM29   | 0x500D D000   | 0x500D DFFF | 4 KB |
| CONTROLSS_G3_EPWM30   | 0x500D E000   | 0x500D EFFF | 4 KB |
| CONTROLSS_G3_EPWM31   | 0x500D F000   | 0x500D FFFF | 4 KB |
| CONTROLSS_ADC0_RESULT | 0x5010 0000   | 0x5010 0FFF | 4 KB |
| CONTROLSS_ADC1_RESULT | 0x5010 1000   | 0x5010 1FFF | 4 KB |
| CONTROLSS_ADC2_RESULT | 0x5010 2000   | 0x5010 2FFF | 4 KB |
| CONTROLSS_ADC3_RESULT | 0x5010 3000   | 0x5010 3FFF | 4 KB |
| CONTROLSS_ADC4_RESULT | 0x5010 4000   | 0x5010 4FFF | 4 KB |
| CONTROLSS_CMPSSA0     | 0x5020 0000   | 0x5020 0FFF | 4 KB |
| CONTROLSS_CMPSSA1     | 0x5020 1000   | 0x5020 1FFF | 4 KB |
| CONTROLSS_CMPSSA2     | 0x5020 2000   | 0x5020 2FFF | 4 KB |
| CONTROLSS_CMPSSA3     | 0x5020 3000   | 0x5020 3FFF | 4 KB |
| CONTROLSS_CMPSSA4     | 0x5020 4000   | 0x5020 4FFF | 4 KB |
| CONTROLSS_CMPSSA5     | 0x5020 5000   | 0x5020 5FFF | 4 KB |
| CONTROLSS_CMPSSA6     | 0x5020 6000   | 0x5020 6FFF | 4 KB |
| CONTROLSS_CMPSSA7     | 0x5020 7000   | 0x5020 7FFF | 4 KB |
| CONTROLSS_CMPSSA8     | 0x5020 8000   | 0x5020 8FFF | 4 KB |
| CONTROLSS_CMPSSA9     | 0x5020 9000   | 0x5020 9FFF | 4 KB |
| CONTROLSS_CMPSSB0     | 0x5022 0000   | 0x5022 0FFF | 4 KB |
| CONTROLSS_CMPSSB1     | 0x5022 1000   | 0x5022 1FFF | 4 KB |
| CONTROLSS_CMPSSB2     | 0x5022 2000   | 0x5022 2FFF | 4 KB |
| CONTROLSS_CMPSSB3     | 0x5022 3000   | 0x5022 3FFF | 4 KB |
| CONTROLSS_CMPSSB4     | 0x5022 4000   | 0x5022 4FFF | 4 KB |
| CONTROLSS_CMPSSB5     | 0x5022 5000   | 0x5022 5FFF | 4 KB |

**Table 1-1. AM263x Memory Map (continued)**

| Region Name              | Start Address | End Address | Size |
|--------------------------|---------------|-------------|------|
| CONTROLSS_CMPSSB6        | 0x5022 6000   | 0x5022 6FFF | 4 KB |
| CONTROLSS_CMPSSB7        | 0x5022 7000   | 0x5022 7FFF | 4 KB |
| CONTROLSS_CMPSSB8        | 0x5022 8000   | 0x5022 8FFF | 4 KB |
| CONTROLSS_CMPSSB9        | 0x5022 9000   | 0x5022 9FFF | 4 KB |
| CONTROLSS_ECAP0          | 0x5024 0000   | 0x5024 0FFF | 4 KB |
| CONTROLSS_ECAP1          | 0x5024 1000   | 0x5024 1FFF | 4 KB |
| CONTROLSS_ECAP2          | 0x5024 2000   | 0x5024 2FFF | 4 KB |
| CONTROLSS_ECAP3          | 0x5024 3000   | 0x5024 3FFF | 4 KB |
| CONTROLSS_ECAP4          | 0x5024 4000   | 0x5024 4FFF | 4 KB |
| CONTROLSS_ECAP5          | 0x5024 5000   | 0x5024 5FFF | 4 KB |
| CONTROLSS_ECAP6          | 0x5024 6000   | 0x5024 6FFF | 4 KB |
| CONTROLSS_ECAP7          | 0x5024 7000   | 0x5024 7FFF | 4 KB |
| CONTROLSS_ECAP8          | 0x5024 8000   | 0x5024 8FFF | 4 KB |
| CONTROLSS_ECAP9          | 0x5024 9000   | 0x5024 9FFF | 4 KB |
| CONTROLSS_DAC0           | 0x5026 0000   | 0x5026 0FFF | 4 KB |
| CONTROLSS_SDFM0          | 0x5026 8000   | 0x5026 8FFF | 4 KB |
| CONTROLSS_SDFM1          | 0x5026 9000   | 0x5026 9FFF | 4 KB |
| CONTROLSS_EQEP0          | 0x5027 0000   | 0x5027 0FFF | 4 KB |
| CONTROLSS_EQEP1          | 0x5027 1000   | 0x5027 1FFF | 4 KB |
| CONTROLSS_EQEP2          | 0x5027 2000   | 0x5027 2FFF | 4 KB |
| CONTROLSS_FSI0_TX0       | 0x5028 0000   | 0x5028 0FFF | 4 KB |
| CONTROLSS_FSI0_TX1       | 0x5028 1000   | 0x5028 1FFF | 4 KB |
| CONTROLSS_FSI0_RX0       | 0x5029 0000   | 0x5029 0FFF | 4 KB |
| CONTROLSS_FSI0_RX1       | 0x5029 1000   | 0x5029 1FFF | 4 KB |
| CONTROLSS_FSI1_TX2       | 0x502A 0000   | 0x502A 0FFF | 4 KB |
| CONTROLSS_FSI1_TX3       | 0x502A 1000   | 0x502A 1FFF | 4 KB |
| CONTROLSS_FSI1_RX2       | 0x502B 0000   | 0x502B 0FFF | 4 KB |
| CONTROLSS_FSI1_RX3       | 0x502B 1000   | 0x502B 1FFF | 4 KB |
| CONTROLSS_ADC0_CFG       | 0x502C 0000   | 0x502C 0FFF | 4 KB |
| CONTROLSS_ADC1_CFG       | 0x502C 1000   | 0x502C 1FFF | 4 KB |
| CONTROLSS_ADC2_CFG       | 0x502C 2000   | 0x502C 2FFF | 4 KB |
| CONTROLSS_ADC3_CFG       | 0x502C 3000   | 0x502C 3FFF | 4 KB |
| CONTROLSS_ADC4_CFG       | 0x502C 4000   | 0x502C 4FFF | 4 KB |
| CONTROLSS_INPUTXBAR      | 0x502D 0000   | 0x502D 0FFF | 4 KB |
| CONTROLSS_PWMXBAR        | 0x502D 1000   | 0x502D 1FFF | 4 KB |
| CONTROLSS_PWMSYNCOUXTBAR | 0x502D 2000   | 0x502D 2FFF | 4 KB |
| CONTROLSS_MDLXBAR        | 0x502D 3000   | 0x502D 3FFF | 4 KB |
| CONTROLSS_ICLXBAR        | 0x502D 4000   | 0x502D 4FFF | 4 KB |
| CONTROLSS_INTXBAR        | 0x502D 5000   | 0x502D 5FFF | 4 KB |
| CONTROLSS_DMAXBAR        | 0x502D 6000   | 0x502D 6FFF | 4 KB |
| CONTROLSS_OUTPUTXBAR     | 0x502D 8000   | 0x502D 8FFF | 4 KB |
| CONTROLSS_OTTOCAL0       | 0x502E 0000   | 0x502E 0FFF | 4 KB |
| CONTROLSS_OTTOCAL1       | 0x502E 1000   | 0x502E 1FFF | 4 KB |
| CONTROLSS_OTTOCAL2       | 0x502E 2000   | 0x502E 2FFF | 4 KB |
| CONTROLSS_OTTOCAL3       | 0x502E 3000   | 0x502E 3FFF | 4 KB |

**Table 1-1. AM263x Memory Map (continued)**

| Region Name          | Start Address | End Address | Size      |
|----------------------|---------------|-------------|-----------|
| CONTROLSS_CTRL       | 0x502F 0000   | 0x502F 7FFF | 32 KB     |
| DEBUGSS              | 0x5080 0000   | 0x508F FFFF | 1024 KB   |
| MSS_CTRL             | 0x50D0 0000   | 0x50D3 FFFF | 256 KB    |
| TOP_CTRL             | 0x50D8 0000   | 0x50D8 7FFF | 32 KB     |
| SPINLOCK0            | 0x50E0 0000   | 0x50E0 7FFF | 32 KB     |
| VIM                  | 0x50F0 0000   | 0x50F0 3FFF | 16 KB     |
| GPIO0 <sup>(6)</sup> | 0x5200 0000   | 0x5200 00FF | 256 Bytes |
| GPIO1 <sup>(6)</sup> | 0x5200 1000   | 0x5200 10FF | 256 Bytes |
| GPIO2 <sup>(6)</sup> | 0x5200 2000   | 0x5200 20FF | 256 Bytes |
| GPIO3 <sup>(6)</sup> | 0x5200 3000   | 0x5200 30FF | 256 Bytes |
| WDT0 <sup>(7)</sup>  | 0x5210 0000   | 0x5210 00FF | 256 Bytes |
| WDT1 <sup>(7)</sup>  | 0x5210 1000   | 0x5210 10FF | 256 Bytes |
| WDT2 <sup>(7)</sup>  | 0x5210 2000   | 0x5210 20FF | 256 Bytes |
| WDT3 <sup>(7)</sup>  | 0x5210 3000   | 0x5210 30FF | 256 Bytes |
| RTI0                 | 0x5218 0000   | 0x5218 03FF | 1 KB      |
| RTI1                 | 0x5218 1000   | 0x5218 13FF | 1 KB      |
| RTI2                 | 0x5218 2000   | 0x5218 23FF | 1 KB      |
| RTI3                 | 0x5218 3000   | 0x5218 33FF | 1 KB      |
| MCSPi0               | 0x5220 0000   | 0x5220 01FF | 512 Bytes |
| MCSPi1               | 0x5220 1000   | 0x5220 11FF | 512 Bytes |
| MCSPi2               | 0x5220 2000   | 0x5220 21FF | 512 Bytes |
| MCSPi3               | 0x5220 3000   | 0x5220 31FF | 512 Bytes |
| MCSPi4               | 0x5220 4000   | 0x5220 41FF | 512 Bytes |
| UART0                | 0x5230 0000   | 0x5230 01FF | 512 Bytes |
| UART1                | 0x5230 1000   | 0x5230 11FF | 512 Bytes |
| UART2                | 0x5230 2000   | 0x5230 21FF | 512 Bytes |
| UART3                | 0x5230 3000   | 0x5230 31FF | 512 Bytes |
| UART4                | 0x5230 4000   | 0x5230 41FF | 512 Bytes |
| UART5                | 0x5230 5000   | 0x5230 51FF | 512 Bytes |
| LIN0                 | 0x5240 0000   | 0x5240 00FF | 256 Bytes |
| LIN1                 | 0x5240 1000   | 0x5240 10FF | 256 Bytes |
| LIN2                 | 0x5240 2000   | 0x5240 20FF | 256 Bytes |
| LIN3                 | 0x5240 3000   | 0x5240 30FF | 256 Bytes |
| LIN4                 | 0x5240 4000   | 0x5240 40FF | 256 Bytes |
| I2C0                 | 0x5250 0000   | 0x5250 00FF | 256 Bytes |
| I2C1                 | 0x5250 1000   | 0x5250 10FF | 256 Bytes |
| I2C2                 | 0x5250 2000   | 0x5250 20FF | 256 Bytes |
| I2C3                 | 0x5250 3000   | 0x5250 30FF | 256 Bytes |
| MCAN0_MSG_RAM        | 0x5260 0000   | 0x5260 7FFF | 32 KB     |
| MCAN0_CFG            | 0x5260 8000   | 0x5260 83FF | 1 KB      |
| MCAN1_MSG_RAM        | 0x5261 0000   | 0x5261 7FFF | 32 KB     |
| MCAN1_CFG            | 0x5261 8000   | 0x5261 83FF | 1 KB      |
| MCAN2_MSG_RAM        | 0x5262 0000   | 0x5262 7FFF | 32 KB     |
| MCAN2_CFG            | 0x5262 8000   | 0x5262 83FF | 1 KB      |
| MCAN3_MSG_RAM        | 0x5263 0000   | 0x5263 7FFF | 32 KB     |



**Table 1-1. AM263x Memory Map (continued)**

| Region Name                           | Start Address | End Address | Size                        |
|---------------------------------------|---------------|-------------|-----------------------------|
| MCAN3_CFG                             | 0x5263 8000   | 0x5263 83FF | 1 KB                        |
| MCAN0_ECC                             | 0x5270 0000   | 0x5270 03FF | 1 KB                        |
| MCAN1_ECC                             | 0x5270 1000   | 0x5270 13FF | 1 KB                        |
| MCAN2_ECC                             | 0x5270 2000   | 0x5270 23FF | 1 KB                        |
| MCAN3_ECC                             | 0x5270 3000   | 0x5270 33FF | 1 KB                        |
| ELM0                                  | 0x527F 0000   | 0x527F 0FFF | 4 KB                        |
| CPSW0                                 | 0x5280 0000   | 0x529F FFFF | 2 MB                        |
| TPCC_A                                | 0x52A0 0000   | 0x52A0 7FFF | 32 KB                       |
| TPTC_A0                               | 0x52A4 0000   | 0x52A4 0FFF | 4 KB                        |
| TPTC_A1                               | 0x52A6 0000   | 0x52A6 0FFF | 4 KB                        |
| DCC0                                  | 0x52B0 0000   | 0x52B0 00FF | 256 Bytes                   |
| DCC1                                  | 0x52B0 1000   | 0x52B0 10FF | 256 Bytes                   |
| DCC2                                  | 0x52B0 2000   | 0x52B0 20FF | 256 Bytes                   |
| DCC3                                  | 0x52B0 3000   | 0x52B0 30FF | 256 Bytes                   |
| TOP_ESM                               | 0x52D0 0000   | 0x52D0 0FFF | 4 KB                        |
| SOC_TIMESYNC_XBAR0                    | 0x52E0 0000   | 0x52E0 00FF | 256 Bytes                   |
| EDMA_TRIG_XBAR                        | 0x52E0 1000   | 0x52E0 11FF | 512 Bytes                   |
| GPIO_INTR_XBAR                        | 0x52E0 2000   | 0x52E0 23FF | 1 KB                        |
| ICSS_INTR_XBAR                        | 0x52E0 3000   | 0x52E0 30FF | 256 Bytes                   |
| SOC_TIMESYNC_XBAR1                    | 0x52E0 4000   | 0x52E0 43FF | 1 KB                        |
| ECC_AGG_R5FSS0_CORE0                  | 0x5300 0000   | 0x5300 03FF | 1 KB                        |
| ECC_AGG_R5FSS0_CORE1                  | 0x5300 3000   | 0x5300 33FF | 1 KB                        |
| ECC_AGG_R5FSS1_CORE0                  | 0x5300 4000   | 0x5300 43FF | 1 KB                        |
| ECC_AGG_R5FSS1_CORE1                  | 0x5300 7000   | 0x5300 73FF | 1 KB                        |
| ECC_AGG_TOP                           | 0x5301 0000   | 0x5301 03FF | 1 KB                        |
| IOMUX                                 | 0x5310 0000   | 0x5310 0FFF | 4 KB                        |
| TOP_RCM                               | 0x5320 0000   | 0x5320 7FFF | 32 KB                       |
| MSS_RCM                               | 0x5320 8000   | 0x5320 FFFF | 32 KB                       |
| R5FSS0_CCMR                           | 0x5321 0000   | 0x5321 0FFF | 4 KB                        |
| R5FSS1_CCMR                           | 0x5321 1000   | 0x5321 1FFF | 4 KB                        |
| TOP_PBI                               | 0x5330 0000   | 0x5330 03FF | 1 KB                        |
| R5FSS0_STC                            | 0x5350 0000   | 0x5350 01FF | 512 Bytes                   |
| R5FSS1_STC                            | 0x5351 0000   | 0x5351 01FF | 512 Bytes                   |
| EXT_FLASH0                            | 0x6000 0000   | 0x61FF FFFF | 32 MB                       |
| EXT_FLASH1                            | 0x6200 0000   | 0x63FF FFFF | 32 MB                       |
| GPMC0_MEM                             | 0x6800 0000   | 0x6FFF FFFF | 128 MB                      |
| L2OCRAM                               | 0x7000 0000   | 0x701F FFFF | 2 MB                        |
| MBOX_SRAM                             | 0x7200 0000   | 0x7200 3FFF | 16 KB                       |
| R5FSS0_CORE0_ICACHE <sup>(4)</sup>    | 0x7400 0000   | 0x747F FFFF | 16 KB (8 MB) <sup>(5)</sup> |
| R5FSS0_CORE0_DCACHE <sup>(4)</sup>    | 0x7480 0000   | 0x74FF FFFF | 16 KB (8 MB) <sup>(5)</sup> |
| R5FSS0_CORE1_ICACHE <sup>(2)(4)</sup> | 0x7500 0000   | 0x757F FFFF | 16 KB (8 MB) <sup>(5)</sup> |
| R5FSS0_CORE1_DCACHE <sup>(2)(4)</sup> | 0x7580 0000   | 0x75FF FFFF | 16 KB (8 MB) <sup>(5)</sup> |
| R5FSS1_CORE0_ICACHE <sup>(4)</sup>    | 0x7600 0000   | 0x767F FFFF | 16 KB (8 MB) <sup>(5)</sup> |
| R5FSS1_CORE0_DCACHE <sup>(4)</sup>    | 0x7680 0000   | 0x76FF FFFF | 16 KB (8 MB) <sup>(5)</sup> |
| R5FSS1_CORE1_ICACHE <sup>(2)(4)</sup> | 0x7700 0000   | 0x777F FFFF | 16 KB (8 MB) <sup>(5)</sup> |

**Table 1-1. AM263x Memory Map (continued)**

| Region Name                           | Start Address | End Address                                       | Size                                  |
|---------------------------------------|---------------|---------------------------------------------------|---------------------------------------|
| R5FSS1_CORE1_DCACHE <sup>(2)(4)</sup> | 0x7780 0000   | 0x77FF FFFF                                       | 16 KB (8 MB) <sup>(5)</sup>           |
| R5FSS0_CORE0_TCMA <sup>(3)(4)</sup>   | 0x7800 0000   | 0x7800 FFFF (Lockstep)<br>0x7800 7FFF (Dual Core) | 64 KB (Lockstep)<br>32 KB (Dual Core) |
| R5FSS0_CORE0_TCMB <sup>(3)(4)</sup>   | 0x7810 0000   | 0x7810 FFFF (Lockstep)<br>0x7810 7FFF (Dual Core) | 64 KB (Lockstep)<br>32 KB (Dual Core) |
| R5FSS0_CORE1_TCMA <sup>(2)(4)</sup>   | 0x7820 0000   | 0x7820 7FFF                                       | 32 KB                                 |
| R5FSS0_CORE1_TCMB <sup>(2)(4)</sup>   | 0x7830 0000   | 0x7830 7FFF                                       | 32 KB                                 |
| R5FSS1_CORE0_TCMA <sup>(3)(4)</sup>   | 0x7840 0000   | 0x7840 FFFF (Lockstep)<br>0x7840 7FFF (Dual Core) | 64 KB (Lockstep)<br>32 KB (Dual Core) |
| R5FSS1_CORE0_TCMB <sup>(3)(4)</sup>   | 0x7850 0000   | 0x7850 FFFF (Lockstep)<br>0x7850 7FFF (Dual Core) | 64 KB (Lockstep)<br>32 KB (Dual Core) |
| R5FSS1_CORE1_TCMA <sup>(2)(4)</sup>   | 0x7860 0000   | 0x7860 7FFF                                       | 32 KB                                 |
| R5FSS1_CORE1_TCMB <sup>(2)(4)</sup>   | 0x7870 0000   | 0x7870 7FFF                                       | 32 KB                                 |

- (1) See core-specific tables for the internal memory map.
- (2) In Lockstep mode, the R5FSSx CORE1 memory region is not accessible.
- (3) The size of these memories changes based on Dual-Core vs Lockstep operation.  
For more information about Dual-Core and Lockstep modes, see the *R5FSS* chapter.  
For more information about ATCM and BTCM, see the *Tightly-Coupled Memories (TCM)* section within the *R5FSS* chapter.
- (4) This memory region is used by each CPU core to access the TCM/Cache memory space of other CPU cores.
- (5) Each R5FSS contains 16 KB i-cache and 16 KB d-cache. However, the system interconnect sees an 8 MB address range at ICACHE/DCACHE. Any core attempting to access more than 16 KB will wrap around and access the same cache multiple times.
- (6) GPIO0 can only be accessed by R5FSS0\_CORE0, GPIO1 can only be accessed by R5FSS0\_CORE1, GPIO2 can only be accessed by R5FSS1\_CORE0, GPIO3 can only be accessed by R5FSS1\_CORE1
- (7) WDT0 can only be accessed by R5FSS0\_CORE0, WDT1 can only be accessed by R5FSS0\_CORE1, WDT2 can only be accessed by R5FSS1\_CORE0, WDT3 can only be accessed by R5FSS1\_CORE1

## 1.2 R5FSS Memory Map

**Table 1-2. R5FSS0-0 Memory Map**

| Region Name             | Start Address | End Address                                       | Size                                  |
|-------------------------|---------------|---------------------------------------------------|---------------------------------------|
| R5SS0_CORE0_TCMA_ROM    | 0x0000 0000   | 0x0001 FFFF                                       | 128 KB                                |
| R5SS0_CORE0_TCMA_RAM    | 0x0002 0000   | 0x0002 FFFF (Lockstep)<br>0x0002 7FFF (Dual Core) | 64 KB (Lockstep)<br>32 KB (Dual Core) |
| R5SS0_CORE0_TCMB_RAM    | 0x0008 0000   | 0x0008 FFFF (Lockstep)<br>0x0008 7FFF (Dual Core) | 64 KB (Lockstep)<br>32 KB (Dual Core) |
| R5SS0_CORE0_VIM         | 0x50F0 0000   | 0x50F0 3FFF                                       | 16 KB                                 |
| R5SS0_CORE0_WWDT (WDT0) | 0x5210 0000   | 0x5210 00FF                                       | 256 Bytes                             |
| <b>ROM to RAM Swap</b>  |               |                                                   |                                       |
| R5SS0_CORE0_TCMA_ROM    | NA            | NA                                                | NA                                    |

**Table 1-2. R5FSS0-0 Memory Map (continued)**

| Region Name             | Start Address | End Address                                       | Size                                  |
|-------------------------|---------------|---------------------------------------------------|---------------------------------------|
| R5SS0_CORE0_TCMA_RAM    | 0x0000 0000   | 0x0000 FFFF (Lockstep)<br>0x0000 7FFF (Dual Core) | 64 KB (Lockstep)<br>32 KB (Dual Core) |
| R5SS0_CORE0_TCMB_RAM    | 0x0008 0000   | 0x0008 FFFF (Lockstep)<br>0x0008 7FFF (Dual Core) | 64 KB (Lockstep)<br>32 KB (Dual Core) |
| R5SS0_CORE0_VIM         | 0x50F0 0000   | 0x50F0 3FFF                                       | 16 KB                                 |
| R5SS0_CORE0_WWDT (WDT0) | 0x5210 0000   | 0x5210 00FF                                       | 256 Bytes                             |

**Table 1-3. R5FSS0-1 Memory Map**

| Region Name             | Start Address | End Address | Size      |
|-------------------------|---------------|-------------|-----------|
| R5SS0_CORE1_TCMA_RAM    | 0x0000 0000   | 0x0000 7FFF | 32 KB     |
| R5SS0_CORE1_TCMB_RAM    | 0x0008 0000   | 0x0008 7FFF | 32 KB     |
| R5SS0_CORE1_VIM         | 0x50F0 0000   | 0x50F0 3FFF | 16 KB     |
| R5SS0_CORE1_WWDT (WDT1) | 0x5210 1000   | 0x5210 10FF | 256 Bytes |

**Table 1-4. R5FSS1-0 Memory Map**

| Region Name             | Start Address | End Address                                       | Size                                  |
|-------------------------|---------------|---------------------------------------------------|---------------------------------------|
| R5SS1_CORE0_TCMA_RAM    | 0x0000 0000   | 0x0000 FFFF (Lockstep)<br>0x0000 7FFF (Dual Core) | 64 KB (Lockstep)<br>32 KB (Dual Core) |
| R5SS1_CORE0_TCMB_RAM    | 0x0008 0000   | 0x0008 FFFF (Lockstep)<br>0x0008 7FFF (Dual Core) | 64 KB (Lockstep)<br>32 KB (Dual Core) |
| R5SS1_CORE0_VIM         | 0x50F0 0000   | 0x50F0 3FFF                                       | 16 KB                                 |
| R5SS1_CORE0_WWDT (WDT2) | 0x5210 2000   | 0x5210 20FF                                       | 256 Bytes                             |

**Table 1-5. R5FSS1-1 Memory Map**

| Region Name             | Start Address | End Address | Size      |
|-------------------------|---------------|-------------|-----------|
| R5SS1_CORE1_TCMA_RAM    | 0x0000 0000   | 0x0000 7FFF | 32 KB     |
| R5SS1_CORE1_TCMB_RAM    | 0x0008 0000   | 0x0008 7FFF | 32 KB     |
| R5SS1_CORE1_VIM         | 0x50F0 0000   | 0x50F0 3FFF | 16 KB     |
| R5SS1_CORE1_WWDT (WDT3) | 0x5210 3000   | 0x5210 30FF | 256 Bytes |

### 1.3 PRU-ICSS Memory Map

| Region Name                       | Start Address | End Address | Size  |
|-----------------------------------|---------------|-------------|-------|
| PRU-ICSS Data RAM0 (DRAM0)        | 0x0000 0000   | 0x0000 1FFF | 8 KB  |
| PRU-ICSS Data RAM1 (DRAM1)        | 0x0000 2000   | 0x0000 3FFF | 8 KB  |
| PRU-ICSS Data RAM2 (Shared DRAM2) | 0x0001 0000   | 0x0001 FFFF | 64 KB |
| PRU-ICSS INTc                     | 0x0002 0000   | 0x0002 1FFF | 8 KB  |
| PRU-ICSS PRU0 Control             | 0x0002 2000   | 0x0002 23FF | 1 KB  |

| Region Name           | Start Address | End Address | Size  |
|-----------------------|---------------|-------------|-------|
| PRU-ICSS PRU0 Debug   | 0x0002 2400   | 0x0002 3FFF | 7 KB  |
| PRU-ICSS PRU1 Control | 0x0002 4000   | 0x0002 43FF | 1 KB  |
| PRU-ICSS PRU1 Debug   | 0x0002 4400   | 0x0002 5FFF | 7 KB  |
| PRU-ICSS CFG          | 0x0002 6000   | 0x0002 6FFF | 4 KB  |
| PRU-ICSS ECC_CFG      | 0x0002 7000   | 0x0002 7FFF | 4 KB  |
| PRU-ICSS UART0        | 0x0002 8000   | 0x0002 9FFF | 8 KB  |
| PRU-ICSS Reserved     | 0x0002 A000   | 0x0002 BFFF | 8 KB  |
| PRU-ICSS Reserved     | 0x0002 C000   | 0x0002 DFFF | 8 KB  |
| PRU-ICSS IEP          | 0x0002 E000   | 0x0002 EFFF | 8 KB  |
| PRU-ICSS ECAP0        | 0x0003 0000   | 0x0003 1FFF | 8 KB  |
| PRU-ICSS MII_RT_CFG   | 0x0003 2000   | 0x0003 23FF | 1 KB  |
| PRU-ICSS MII_MDIO     | 0x0003 2400   | 0x0003 3FFF | 7 KB  |
| PRU-ICSS PRU0 IRAM    | 0x0003 4000   | 0x0003 7FFF | 16 KB |
| PRU-ICSS PRU1 IRAM    | 0x0003 8000   | 0x0003 BFFF | 16 KB |

## Control Module (CTRLMMR) Registers

---



The control module is the main controller for top-level device behavior in various states. Module contains registers for configuration, bootstrap (SOP) signals, I/O terminal pad multiplexing, clock selection, and many others. There are various control or (CTRLMMR) modules define in this device, and those module's registers are described in the following sections.

## 2.1 MMR Write Protection

All Control Module MMR have a protection mechanism which prevents spurious writes from changing register values. LOCK0\_KICK0 and LOCK0\_KICK1 registers are used for this purpose. The sequence to unlock these MMR is as follows:

1. Write exact unlock value (Table 2-1) to <Control Module>LOCK0\_KICK0:KEY field
2. Write exact unlock value (Table 2-1) to <Control Module>LOCK0\_KICK1:KEY field

The sequence to lock the MMR is as follows:

1. Write zero (or anyother value other than the unlock value)Table 2-1) to <Control Module>LOCK0\_KICK1:KEY field
2. Write zero (or anyother value other than the unlock value)Table 2-1) to <Control Module>LOCK0\_KICK0:KEY field

### Note

If the above sequence for locking the IOMUX is not followed, an AHB\_WRITE\_ERROR interrupt will occur (if enabled).

For example, to unlock Control Module MSS\_CTRL the sequence is as below:

1. Write 0x01234567 to MSS\_CTRL.LOCK0\_KICK0:KEY
2. Write 0xFEDCBA8 to MSS\_CTRL.LOCK0\_KICK1:KEY

To lock the Control Module MSS\_CTRL the sequence is as below:

1. Write 0x0 to MSS\_CTRL.LOCK0\_KICK1:KEY
2. Write 0x0 to MSS\_CTRL.LOCK0\_KICK0:KEY

Any writes to locked memory region will result in assertion of the MMR\_ACCESS\_ERR\_WR event by the respective control modules. This assertion can be enabled or disabled by writing the appropriate value to <Control Module>.INTR\_ENABLE.KICK\_ERR\_EN field.

The table below shows the values that must be written to the LOCK0\_KICK0 and LOCK0\_KICK1 registers to unlock the various Control modules' MMR.

**Table 2-1. Kick Protection Register Unlock Values**

| Protected Register | LockKick Register | Unlock Value |
|--------------------|-------------------|--------------|
| TOP_CTRL           | LOCK0_KICK0       | 0x01234567   |
|                    | LOCK0_KICK1       | 0xFEDCBA8    |
| MSS_CTRL           | LOCK0_KICK0       | 0x01234567   |
|                    | LOCK0_KICK1       | 0xFEDCBA8    |
| CONTROLSS_CTRL     | LOCK0_KICK0       | 0x01234567   |
|                    | LOCK0_KICK1       | 0xFEDCBA8    |
| TOP_RCM            | LOCK0_KICK0       | 0x01234567   |
|                    | LOCK0_KICK1       | 0xFEDCBA8    |
| MSS_RCM            | LOCK0_KICK0       | 0x01234567   |
|                    | LOCK0_KICK1       | 0xFEDCBA8    |
| IOMUX              | LOCK0_KICK0       | 0x83E70B13   |
|                    | LOCK0_KICK1       | 0x95A4F1E0   |

**Note**

To maintain that all registers from a given partition are write protected, software must always re-lock the protection mechanism after completing the register writes.

---

The kick protection registers described in this section are an exception and are not write protected by the protection mechanism.

## 2.2 MSS\_CTRL

### MSS\_CTRL

#### 2.2.1 MSS\_CTRL Summaries

#### MSS\_CTRL Summaries

**Table 2-2. MSS\_CTRL Registers, Base Address=50D0 0000h, Length=131072**

| Offset | Length | Register Name                                      | MSS_CTRL Physical Address |
|--------|--------|----------------------------------------------------|---------------------------|
| 20h    | 32     | <a href="#">MSS_CTRL_R5SS0_CONTROL</a>             | 50D0 0020h                |
| 24h    | 32     | <a href="#">MSS_CTRL_R5SS0_CORE0_HALT</a>          | 50D0 0024h                |
| 28h    | 32     | <a href="#">MSS_CTRL_R5SS0_CORE1_HALT</a>          | 50D0 0028h                |
| 2Ch    | 32     | <a href="#">MSS_CTRL_R5SS0_STATUS_REG</a>          | 50D0 002Ch                |
| 30h    | 32     | <a href="#">MSS_CTRL_R5SS0_CORE0_STAT</a>          | 50D0 0030h                |
| 34h    | 32     | <a href="#">MSS_CTRL_R5SS0_CORE1_STAT</a>          | 50D0 0034h                |
| 38h    | 32     | <a href="#">MSS_CTRL_MSS_STC_CONTROL0</a>          | 50D0 0038h                |
| 40h    | 32     | <a href="#">MSS_CTRL_R5SS1_CONTROL</a>             | 50D0 0040h                |
| 44h    | 32     | <a href="#">MSS_CTRL_R5SS1_CORE0_HALT</a>          | 50D0 0044h                |
| 48h    | 32     | <a href="#">MSS_CTRL_R5SS1_CORE1_HALT</a>          | 50D0 0048h                |
| 4Ch    | 32     | <a href="#">MSS_CTRL_R5SS1_STATUS_REG</a>          | 50D0 004Ch                |
| 50h    | 32     | <a href="#">MSS_CTRL_R5SS1_CORE0_STAT</a>          | 50D0 0050h                |
| 54h    | 32     | <a href="#">MSS_CTRL_R5SS1_CORE1_STAT</a>          | 50D0 0054h                |
| 58h    | 32     | <a href="#">MSS_CTRL_MSS_STC_CONTROL1</a>          | 50D0 0058h                |
| 80h    | 32     | <a href="#">MSS_CTRL_R5SS0_ROM_ECLIPSE</a>         | 50D0 0080h                |
| 100h   | 32     | <a href="#">MSS_CTRL_MSS_BOOT_INFO_REG0</a>        | 50D0 0100h                |
| 104h   | 32     | <a href="#">MSS_CTRL_MSS_BOOT_INFO_REG1</a>        | 50D0 0104h                |
| 108h   | 32     | <a href="#">MSS_CTRL_MSS_BOOT_INFO_REG2</a>        | 50D0 0108h                |
| 10Ch   | 32     | <a href="#">MSS_CTRL_MSS_BOOT_INFO_REG3</a>        | 50D0 010Ch                |
| 110h   | 32     | <a href="#">MSS_CTRL_MSS_BOOT_INFO_REG4</a>        | 50D0 0110h                |
| 114h   | 32     | <a href="#">MSS_CTRL_MSS_BOOT_INFO_REG5</a>        | 50D0 0114h                |
| 118h   | 32     | <a href="#">MSS_CTRL_MSS_BOOT_INFO_REG6</a>        | 50D0 0118h                |
| 11Ch   | 32     | <a href="#">MSS_CTRL_MSS_BOOT_INFO_REG7</a>        | 50D0 011Ch                |
| 200h   | 32     | <a href="#">MSS_CTRL_MSS_ATCM0_MEM_INIT</a>        | 50D0 0200h                |
| 204h   | 32     | <a href="#">MSS_CTRL_MSS_ATCM0_MEM_INIT_DONE</a>   | 50D0 0204h                |
| 208h   | 32     | <a href="#">MSS_CTRL_MSS_ATCM0_MEM_INIT_STATUS</a> | 50D0 0208h                |
| 210h   | 32     | <a href="#">MSS_CTRL_MSS_BTCM0_MEM_INIT</a>        | 50D0 0210h                |
| 214h   | 32     | <a href="#">MSS_CTRL_MSS_BTCM0_MEM_INIT_DONE</a>   | 50D0 0214h                |
| 218h   | 32     | <a href="#">MSS_CTRL_MSS_BTCM0_MEM_INIT_STATUS</a> | 50D0 0218h                |
| 220h   | 32     | <a href="#">MSS_CTRL_MSS_ATCM1_MEM_INIT</a>        | 50D0 0220h                |
| 224h   | 32     | <a href="#">MSS_CTRL_MSS_ATCM1_MEM_INIT_DONE</a>   | 50D0 0224h                |
| 228h   | 32     | <a href="#">MSS_CTRL_MSS_ATCM1_MEM_INIT_STATUS</a> | 50D0 0228h                |
| 230h   | 32     | <a href="#">MSS_CTRL_MSS_BTCM1_MEM_INIT</a>        | 50D0 0230h                |
| 234h   | 32     | <a href="#">MSS_CTRL_MSS_BTCM1_MEM_INIT_DONE</a>   | 50D0 0234h                |
| 238h   | 32     | <a href="#">MSS_CTRL_MSS_BTCM1_MEM_INIT_STATUS</a> | 50D0 0238h                |
| 240h   | 32     | <a href="#">MSS_CTRL_MSS_L2_MEM_INIT</a>           | 50D0 0240h                |
| 244h   | 32     | <a href="#">MSS_CTRL_MSS_L2_MEM_INIT_DONE</a>      | 50D0 0244h                |
| 248h   | 32     | <a href="#">MSS_CTRL_MSS_L2_MEM_INIT_STATUS</a>    | 50D0 0248h                |



**Table 2-2. MSS\_CTRL Registers, Base Address=50D0 0000h, Length=131072 (continued)**

| Offset | Length | Register Name                                         | MSS_CTRL Physical Address |
|--------|--------|-------------------------------------------------------|---------------------------|
| 250h   | 32     | <a href="#">MSS_CTRL_MSS_MAILBOX_MEM_INIT</a>         | 50D0 0250h                |
| 254h   | 32     | <a href="#">MSS_CTRL_MSS_MAILBOX_MEM_INIT_DONE</a>    | 50D0 0254h                |
| 258h   | 32     | <a href="#">MSS_CTRL_MSS_MAILBOX_MEM_INIT_STATUS</a>  | 50D0 0258h                |
| 260h   | 32     | <a href="#">MSS_CTRL_MSS_TPCC_MEMINIT_START</a>       | 50D0 0260h                |
| 264h   | 32     | <a href="#">MSS_CTRL_MSS_TPCC_MEMINIT_DONE</a>        | 50D0 0264h                |
| 268h   | 32     | <a href="#">MSS_CTRL_MSS_TPCC_MEMINIT_STATUS</a>      | 50D0 0268h                |
| 300h   | 32     | <a href="#">MSS_CTRL_TOP_PBIIST_KEY_RST</a>           | 50D0 0300h                |
| 400h   | 32     | <a href="#">MSS_CTRL_MSS_R5SS0_CTI_TRIG_SEL</a>       | 50D0 0400h                |
| 404h   | 32     | <a href="#">MSS_CTRL_MSS_R5SS1_CTI_TRIG_SEL</a>       | 50D0 0404h                |
| 408h   | 32     | <a href="#">MSS_CTRL_MSS_DBGSS_CTI_TRIG_SEL</a>       | 50D0 0408h                |
| 410h   | 32     | <a href="#">MSS_CTRL_DEBUGSS_STM_NSGUAREN</a>         | 50D0 0410h                |
| 420h   | 32     | <a href="#">MSS_CTRL_MCAN0_HALTEN</a>                 | 50D0 0420h                |
| 424h   | 32     | <a href="#">MSS_CTRL_MCAN1_HALTEN</a>                 | 50D0 0424h                |
| 428h   | 32     | <a href="#">MSS_CTRL_MCAN2_HALTEN</a>                 | 50D0 0428h                |
| 42Ch   | 32     | <a href="#">MSS_CTRL_MCAN3_HALTEN</a>                 | 50D0 042Ch                |
| 430h   | 32     | <a href="#">MSS_CTRL_LIN0_HALTEN</a>                  | 50D0 0430h                |
| 434h   | 32     | <a href="#">MSS_CTRL_LIN1_HALTEN</a>                  | 50D0 0434h                |
| 438h   | 32     | <a href="#">MSS_CTRL_LIN2_HALTEN</a>                  | 50D0 0438h                |
| 43Ch   | 32     | <a href="#">MSS_CTRL_LIN3_HALTEN</a>                  | 50D0 043Ch                |
| 440h   | 32     | <a href="#">MSS_CTRL_LIN4_HALTEN</a>                  | 50D0 0440h                |
| 444h   | 32     | <a href="#">MSS_CTRL_I2C0_HALTEN</a>                  | 50D0 0444h                |
| 448h   | 32     | <a href="#">MSS_CTRL_I2C1_HALTEN</a>                  | 50D0 0448h                |
| 44Ch   | 32     | <a href="#">MSS_CTRL_I2C2_HALTEN</a>                  | 50D0 044Ch                |
| 450h   | 32     | <a href="#">MSS_CTRL_I2C3_HALTEN</a>                  | 50D0 0450h                |
| 454h   | 32     | <a href="#">MSS_CTRL_RTIO_HALTEN</a>                  | 50D0 0454h                |
| 458h   | 32     | <a href="#">MSS_CTRL_RTII_HALTEN</a>                  | 50D0 0458h                |
| 45Ch   | 32     | <a href="#">MSS_CTRL_RTII2_HALTEN</a>                 | 50D0 045Ch                |
| 460h   | 32     | <a href="#">MSS_CTRL_RTII3_HALTEN</a>                 | 50D0 0460h                |
| 474h   | 32     | <a href="#">MSS_CTRL_CPSW_HALTEN</a>                  | 50D0 0474h                |
| 478h   | 32     | <a href="#">MSS_CTRL_CRC_HALTEN</a>                   | 50D0 0478h                |
| 800h   | 32     | <a href="#">MSS_CTRL_TPTC_DBS_CONFIG</a>              | 50D0 0800h                |
| 804h   | 32     | <a href="#">MSS_CTRL_MSS_TPTC_BOUNDARY_CFG</a>        | 50D0 0804h                |
| 808h   | 32     | <a href="#">MSS_CTRL_MSS_TPTC_XID_REORDER_CFG</a>     | 50D0 0808h                |
| 810h   | 32     | <a href="#">MSS_CTRL_CPSW_CONTROL</a>                 | 50D0 0810h                |
| 818h   | 32     | <a href="#">MSS_CTRL_GLOBAL_CONTROLS</a>              | 50D0 0818h                |
| 81Ch   | 32     | <a href="#">MSS_CTRL_PRU_ICSS_PRU0_GPI_SEL</a>        | 50D0 081Ch                |
| 820h   | 32     | <a href="#">MSS_CTRL_PRU_ICSS_PRU1_GPI_SEL</a>        | 50D0 0820h                |
| 824h   | 32     | <a href="#">MSS_CTRL_PRU_ICSS_PRU0_GPIO_OUT_CTRL</a>  | 50D0 0824h                |
| 828h   | 32     | <a href="#">MSS_CTRL_PRU_ICSS_PRU1_GPIO_OUT_CTRL</a>  | 50D0 0828h                |
| 82Ch   | 32     | <a href="#">MSS_CTRL_GPMC_CONTROL</a>                 | 50D0 082Ch                |
| 830h   | 32     | <a href="#">MSS_CTRL_MSS_TPCC_A_INTAGG_MASK</a>       | 50D0 0830h                |
| 834h   | 32     | <a href="#">MSS_CTRL_MSS_TPCC_A_INTAGG_STATUS</a>     | 50D0 0834h                |
| 838h   | 32     | <a href="#">MSS_CTRL_MSS_TPCC_A_INTAGG_STATUS_RAW</a> | 50D0 0838h                |
| 1008h  | 32     | <a href="#">MSS_CTRL_LOCK0_KICK0</a>                  | 50D0 1008h                |
| 100Ch  | 32     | <a href="#">MSS_CTRL_LOCK0_KICK1</a>                  | 50D0 100Ch                |

**Table 2-2. MSS\_CTRL Registers, Base Address=50D0 0000h, Length=131072 (continued)**

| Offset | Length | Register Name                                | MSS_CTRL Physical Address |
|--------|--------|----------------------------------------------|---------------------------|
| 1010h  | 32     | MSS_CTRL_INTR_RAW_STATUS                     | 50D0 1010h                |
| 1014h  | 32     | MSS_CTRL_INTR_ENABLED_STATUS_CLEAR           | 50D0 1014h                |
| 1018h  | 32     | MSS_CTRL_INTR_ENABLE                         | 50D0 1018h                |
| 101Ch  | 32     | MSS_CTRL_INTR_ENABLE_CLEAR                   | 50D0 101Ch                |
| 1020h  | 32     | MSS_CTRL_EOI                                 | 50D0 1020h                |
| 1024h  | 32     | MSS_CTRL_FAULT_ADDRESS                       | 50D0 1024h                |
| 1028h  | 32     | MSS_CTRL_FAULT_TYPE_STATUS                   | 50D0 1028h                |
| 102Ch  | 32     | MSS_CTRL_FAULT_ATTR_STATUS                   | 50D0 102Ch                |
| 1030h  | 32     | MSS_CTRL_FAULT_CLEAR                         | 50D0 1030h                |
| 4000h  | 32     | MSS_CTRL_MSS_R5SS0_CORE0_MBOX_WRITE_DONE     | 50D0 4000h                |
| 4004h  | 32     | MSS_CTRL_MSS_R5SS0_CORE0_MBOX_READ_REQ       | 50D0 4004h                |
| 4008h  | 32     | MSS_CTRL_MSS_R5SS0_CORE0_MBOX_READ_DONE_ACK  | 50D0 4008h                |
| 400Ch  | 32     | MSS_CTRL_MSS_R5SS0_CORE0_MBOX_READ_DONE      | 50D0 400Ch                |
| 4010h  | 32     | MSS_CTRL_MSS_SW_INT_R5SS0_CORE0              | 50D0 4010h                |
| 4020h  | 32     | MSS_CTRL_MPU_ADDR_INTR_ERRAGG0_MASK          | 50D0 4020h                |
| 4024h  | 32     | MSS_CTRL_MPU_ADDR_INTR_ERRAGG0_STATUS        | 50D0 4024h                |
| 4028h  | 32     | MSS_CTRL_MPU_ADDR_INTR_ERRAGG0_STATUS_RAW    | 50D0 4028h                |
| 4030h  | 32     | MSS_CTRL_MPU_PROT_INTR_ERRAGG0_MASK          | 50D0 4030h                |
| 4034h  | 32     | MSS_CTRL_MPU_PROT_INTR_ERRAGG0_STATUS        | 50D0 4034h                |
| 4038h  | 32     | MSS_CTRL_MPU_PROT_INTR_ERRAGG0_STATUS_RAW    | 50D0 4038h                |
| 8000h  | 32     | MSS_CTRL_MSS_R5SS0_CORE1_MBOX_WRITE_DONE     | 50D0 8000h                |
| 8004h  | 32     | MSS_CTRL_MSS_R5SS0_CORE1_MBOX_READ_REQ       | 50D0 8004h                |
| 8008h  | 32     | MSS_CTRL_MSS_R5SS0_CORE1_MBOX_READ_DONE_ACK  | 50D0 8008h                |
| 800Ch  | 32     | MSS_CTRL_MSS_R5SS0_CORE1_MBOX_READ_DONE      | 50D0 800Ch                |
| 8010h  | 32     | MSS_CTRL_MSS_SW_INT_R5SS0_CORE1              | 50D0 8010h                |
| 8020h  | 32     | MSS_CTRL_MPU_ADDR_INTR_ERRAGG1_MASK          | 50D0 8020h                |
| 8024h  | 32     | MSS_CTRL_MPU_ADDR_INTR_ERRAGG1_STATUS        | 50D0 8024h                |
| 8028h  | 32     | MSS_CTRL_MPU_ADDR_INTR_ERRAGG1_STATUS_RAW    | 50D0 8028h                |
| 8030h  | 32     | MSS_CTRL_MPU_PROT_INTR_ERRAGG1_MASK          | 50D0 8030h                |
| 8034h  | 32     | MSS_CTRL_MPU_PROT_INTR_ERRAGG1_STATUS        | 50D0 8034h                |
| 8038h  | 32     | MSS_CTRL_MPU_PROT_INTR_ERRAGG1_STATUS_RAW    | 50D0 8038h                |
| C000h  | 32     | MSS_CTRL_MSS_R5FSS1_CORE0_MBOX_WRITE_DONE    | 50D0 C000h                |
| C004h  | 32     | MSS_CTRL_MSS_R5FSS1_CORE0_MBOX_READ_REQ      | 50D0 C004h                |
| C008h  | 32     | MSS_CTRL_MSS_R5FSS1_CORE0_MBOX_READ_DONE_ACK | 50D0 C008h                |
| C00Ch  | 32     | MSS_CTRL_MSS_R5FSS1_CORE0_MBOX_READ_DONE     | 50D0 C00Ch                |
| C010h  | 32     | MSS_CTRL_MSS_SW_INT_R5SS1_CORE0              | 50D0 C010h                |
| C020h  | 32     | MSS_CTRL_MPU_ADDR_INTR_ERRAGG2_MASK          | 50D0 C020h                |
| C024h  | 32     | MSS_CTRL_MPU_ADDR_INTR_ERRAGG2_STATUS        | 50D0 C024h                |

**Table 2-2. MSS\_CTRL Registers, Base Address=50D0 0000h, Length=131072 (continued)**

| Offset | Length | Register Name                                     | MSS_CTRL Physical Address |
|--------|--------|---------------------------------------------------|---------------------------|
| C028h  | 32     | MSS_CTRL_MPU_ADDR_INTR_ERRAGG2_STATUS_RAW         | 50D0 C028h                |
| C030h  | 32     | MSS_CTRL_MPU_PROT_INTR_ERRAGG2_MASK               | 50D0 C030h                |
| C034h  | 32     | MSS_CTRL_MPU_PROT_INTR_ERRAGG2_STATUS             | 50D0 C034h                |
| C038h  | 32     | MSS_CTRL_MPU_PROT_INTR_ERRAGG2_STATUS_RAW         | 50D0 C038h                |
| 10000h | 32     | MSS_CTRL_MSS_R5FSS1_CORE1_MBOX_WRITE_DONE         | 50D1 0000h                |
| 10004h | 32     | MSS_CTRL_MSS_R5FSS1_CORE1_MBOX_READ_REQ           | 50D1 0004h                |
| 10008h | 32     | MSS_CTRL_MSS_R5FSS1_CORE1_MBOX_READ_DONE_ACK      | 50D1 0008h                |
| 1000Ch | 32     | MSS_CTRL_MSS_R5FSS1_CORE1_MBOX_READ_DONE          | 50D1 000Ch                |
| 10010h | 32     | MSS_CTRL_MSS_SW_INT_R5SS1_CORE1                   | 50D1 0010h                |
| 10020h | 32     | MSS_CTRL_MPU_ADDR_INTR_ERRAGG3_MASK               | 50D1 0020h                |
| 10024h | 32     | MSS_CTRL_MPU_ADDR_INTR_ERRAGG3_STATUS             | 50D1 0024h                |
| 10028h | 32     | MSS_CTRL_MPU_ADDR_INTR_ERRAGG3_STATUS_RAW         | 50D1 0028h                |
| 10030h | 32     | MSS_CTRL_MPU_PROT_INTR_ERRAGG3_MASK               | 50D1 0030h                |
| 10034h | 32     | MSS_CTRL_MPU_PROT_INTR_ERRAGG3_STATUS             | 50D1 0034h                |
| 10038h | 32     | MSS_CTRL_MPU_PROT_INTR_ERRAGG3_STATUS_RAW         | 50D1 0038h                |
| 14000h | 32     | MSS_CTRL_PRU_ICSS_PRU0_MBOX_WRITE_DONE            | 50D1 4000h                |
| 14004h | 32     | MSS_CTRL_PRU_ICSS_PRU0_MBOX_READ_REQ              | 50D1 4004h                |
| 14008h | 32     | MSS_CTRL_PRU_ICSS_PRU0_MBOX_READ_DONE_ACK         | 50D1 4008h                |
| 1400Ch | 32     | MSS_CTRL_PRU_ICSS_PRU0_MBOX_READ_DONE             | 50D1 400Ch                |
| 14010h | 32     | MSS_CTRL_PRU_ICSS_PRU1_MBOX_WRITE_DONE            | 50D1 4010h                |
| 14014h | 32     | MSS_CTRL_PRU_ICSS_PRU1_MBOX_READ_REQ              | 50D1 4014h                |
| 14018h | 32     | MSS_CTRL_PRU_ICSS_PRU1_MBOX_READ_DONE_ACK         | 50D1 4018h                |
| 1401Ch | 32     | MSS_CTRL_PRU_ICSS_PRU1_MBOX_READ_DONE             | 50D1 401Ch                |
| 18000h | 32     | MSS_CTRL_MSS_TPCC_A_ERRAGG_MASK                   | 50D1 8000h                |
| 18004h | 32     | MSS_CTRL_MSS_TPCC_A_ERRAGG_STATUS                 | 50D1 8004h                |
| 18008h | 32     | MSS_CTRL_MSS_TPCC_A_ERRAGG_STATUS_RAW             | 50D1 8008h                |
| 18010h | 32     | MSS_CTRL_MSS_PERIPH_ERRAGG_MASK0                  | 50D1 8010h                |
| 18014h | 32     | MSS_CTRL_MSS_PERIPH_ERRAGG_STATUS0                | 50D1 8014h                |
| 18018h | 32     | MSS_CTRL_MSS_PERIPH_ERRAGG_STATUS_RAW0            | 50D1 8018h                |
| 18080h | 32     | MSS_CTRL_R5SS0_CORE0_ECC_CORR_ERRAGG_MASK         | 50D1 8080h                |
| 18084h | 32     | MSS_CTRL_R5SS0_CORE0_ECC_CORR_ERRAGG_STATUS       | 50D1 8084h                |
| 18088h | 32     | MSS_CTRL_R5SS0_CORE0_ECC_CORR_ERRAGG_STATUS_RAW   | 50D1 8088h                |
| 18090h | 32     | MSS_CTRL_R5SS0_CORE0_ECC_UNCORR_ERRAGG_MASK       | 50D1 8090h                |
| 18094h | 32     | MSS_CTRL_R5SS0_CORE0_ECC_UNCORR_ERRAGG_STATUS     | 50D1 8094h                |
| 18098h | 32     | MSS_CTRL_R5SS0_CORE0_ECC_UNCORR_ERRAGG_STATUS_RAW | 50D1 8098h                |

**Table 2-2. MSS\_CTRL Registers, Base Address=50D0 0000h, Length=131072 (continued)**

| Offset | Length | Register Name                                         | MSS_CTRL Physical Address |
|--------|--------|-------------------------------------------------------|---------------------------|
| 180A0h | 32     | MSS_CTRL_R5SS0_CORE1_ECC_CORR_ERRAGG_MASK             | 50D1 80A0h                |
| 180A4h | 32     | MSS_CTRL_R5SS0_CORE1_ECC_CORR_ERRAGG_STATUS           | 50D1 80A4h                |
| 180A8h | 32     | MSS_CTRL_R5SS0_CORE1_ECC_CORR_ERRAGG_STATUS_RAW       | 50D1 80A8h                |
| 180B0h | 32     | MSS_CTRL_R5SS0_CORE1_ECC_UNCORR_ERRAGG_MASK           | 50D1 80B0h                |
| 180B4h | 32     | MSS_CTRL_R5SS0_CORE1_ECC_UNCORR_ERRAGG_STATUS         | 50D1 80B4h                |
| 180B8h | 32     | MSS_CTRL_R5SS0_CORE1_ECC_UNCORR_ERRAGG_STATUS_RAW     | 50D1 80B8h                |
| 180C0h | 32     | MSS_CTRL_R5SS1_CORE0_ECC_CORR_ERRAGG_MASK             | 50D1 80C0h                |
| 180C4h | 32     | MSS_CTRL_R5SS1_CORE0_ECC_CORR_ERRAGG_STATUS           | 50D1 80C4h                |
| 180C8h | 32     | MSS_CTRL_R5SS1_CORE0_ECC_CORR_ERRAGG_STATUS_RAW       | 50D1 80C8h                |
| 180D0h | 32     | MSS_CTRL_R5SS1_CORE0_ECC_UNCORR_ERRAGG_MASK           | 50D1 80D0h                |
| 180D4h | 32     | MSS_CTRL_R5SS1_CORE0_ECC_UNCORR_ERRAGG_STATUS         | 50D1 80D4h                |
| 180D8h | 32     | MSS_CTRL_R5SS1_CORE0_ECC_UNCORR_ERRAGG_STATUS_RAW     | 50D1 80D8h                |
| 180E0h | 32     | MSS_CTRL_R5SS1_CORE1_ECC_CORR_ERRAGG_MASK             | 50D1 80E0h                |
| 180E4h | 32     | MSS_CTRL_R5SS1_CORE1_ECC_CORR_ERRAGG_STATUS           | 50D1 80E4h                |
| 180E8h | 32     | MSS_CTRL_R5SS1_CORE1_ECC_CORR_ERRAGG_STATUS_RAW       | 50D1 80E8h                |
| 180F0h | 32     | MSS_CTRL_R5SS1_CORE1_ECC_UNCORR_ERRAGG_MASK           | 50D1 80F0h                |
| 180F4h | 32     | MSS_CTRL_R5SS1_CORE1_ECC_UNCORR_ERRAGG_STATUS         | 50D1 80F4h                |
| 180F8h | 32     | MSS_CTRL_R5SS1_CORE1_ECC_UNCORR_ERRAGG_STATUS_RAW     | 50D1 80F8h                |
| 18100h | 32     | MSS_CTRL_R5SS0_CORE0_TCM_ADDRPARITY_ERRAGG_MASK       | 50D1 8100h                |
| 18104h | 32     | MSS_CTRL_R5SS0_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS     | 50D1 8104h                |
| 18108h | 32     | MSS_CTRL_R5SS0_CORE0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW | 50D1 8108h                |
| 18110h | 32     | MSS_CTRL_R5SS0_CORE1_TCM_ADDRPARITY_ERRAGG_MASK       | 50D1 8110h                |
| 18114h | 32     | MSS_CTRL_R5SS0_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS     | 50D1 8114h                |
| 18118h | 32     | MSS_CTRL_R5SS0_CORE1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW | 50D1 8118h                |
| 18120h | 32     | MSS_CTRL_TCM0_PARITY_CTRL                             | 50D1 8120h                |
| 18124h | 32     | MSS_CTRL_ERR_PARITY_ATCM0_R5SS0                       | 50D1 8124h                |
| 18128h | 32     | MSS_CTRL_ERR_PARITY_ATCM1_R5SS0                       | 50D1 8128h                |
| 1812Ch | 32     | MSS_CTRL_ERR_PARITY_B0TCM0_R5SS0                      | 50D1 812Ch                |

**Table 2-2. MSS\_CTRL Registers, Base Address=50D0 0000h, Length=131072 (continued)**

| Offset | Length | Register Name                                                 | MSS_CTRL Physical Address |
|--------|--------|---------------------------------------------------------------|---------------------------|
| 18130h | 32     | MSS_CTRL_ERR_PARITY_B0TCM1_R5SS0                              | 50D1 8130h                |
| 18134h | 32     | MSS_CTRL_ERR_PARITY_B1TCM0_R5SS0                              | 50D1 8134h                |
| 18138h | 32     | MSS_CTRL_ERR_PARITY_B1TCM1_R5SS0                              | 50D1 8138h                |
| 1813Ch | 32     | MSS_CTRL_TCM0_PARITY_ERRFRG                                   | 50D1 813Ch                |
| 18140h | 32     | MSS_CTRL_R5SS1_CORE0_TCM_ADDRPARITY_ERRA<br>GG_MASK           | 50D1 8140h                |
| 18144h | 32     | MSS_CTRL_R5SS1_CORE0_TCM_ADDRPARITY_ERRA<br>GG_STATUS         | 50D1 8144h                |
| 18148h | 32     | MSS_CTRL_R5SS1_CORE0_TCM_ADDRPARITY_ERRA<br>GG_STATUS_RAW     | 50D1 8148h                |
| 18150h | 32     | MSS_CTRL_R5SS1_CORE1_TCM_ADDRPARITY_ERRA<br>GG_MASK           | 50D1 8150h                |
| 18154h | 32     | MSS_CTRL_R5SS1_CORE1_TCM_ADDRPARITY_ERRA<br>GG_STATUS         | 50D1 8154h                |
| 18158h | 32     | MSS_CTRL_R5SS1_CORE1_TCM_ADDRPARITY_ERRA<br>GG_STATUS_RAW     | 50D1 8158h                |
| 18160h | 32     | MSS_CTRL_TCM1_PARITY_CTRL                                     | 50D1 8160h                |
| 18164h | 32     | MSS_CTRL_ERR_PARITY_ATCM0_R5SS1                               | 50D1 8164h                |
| 18168h | 32     | MSS_CTRL_ERR_PARITY_ATCM1_R5SS1                               | 50D1 8168h                |
| 1816Ch | 32     | MSS_CTRL_ERR_PARITY_B0TCM0_R5SS1                              | 50D1 816Ch                |
| 18170h | 32     | MSS_CTRL_ERR_PARITY_B0TCM1_R5SS1                              | 50D1 8170h                |
| 18174h | 32     | MSS_CTRL_ERR_PARITY_B1TCM0_R5SS1                              | 50D1 8174h                |
| 18178h | 32     | MSS_CTRL_ERR_PARITY_B1TCM1_R5SS1                              | 50D1 8178h                |
| 1817Ch | 32     | MSS_CTRL_TCM1_PARITY_ERRFRG                                   | 50D1 817Ch                |
| 18180h | 32     | MSS_CTRL_TPCC_PARITY_CTRL                                     | 50D1 8180h                |
| 18184h | 32     | MSS_CTRL_TPCC_PARITY_STATUS                                   | 50D1 8184h                |
| 18200h | 32     | MSS_CTRL_MSS_BUS_SAFETY_CTRL                                  | 50D1 8200h                |
| 18220h | 32     | MSS_CTRL_MSS_R5SS0_CORE0_AXI_RD_BUS_SAFET<br>Y_CTRL           | 50D1 8220h                |
| 18224h | 32     | MSS_CTRL_MSS_R5SS0_CORE0_AXI_RD_BUS_SAFET<br>Y_FI             | 50D1 8224h                |
| 18228h | 32     | MSS_CTRL_MSS_R5SS0_CORE0_AXI_RD_BUS_SAFET<br>Y_ERR            | 50D1 8228h                |
| 1822Ch | 32     | MSS_CTRL_MSS_R5SS0_CORE0_AXI_RD_BUS_SAFET<br>Y_ERR_STAT_DATA0 | 50D1 822Ch                |
| 18230h | 32     | MSS_CTRL_MSS_R5SS0_CORE0_AXI_RD_BUS_SAFET<br>Y_ERR_STAT_CMD   | 50D1 8230h                |
| 18234h | 32     | MSS_CTRL_MSS_R5SS0_CORE0_AXI_RD_BUS_SAFET<br>Y_ERR_STAT_READ  | 50D1 8234h                |
| 18240h | 32     | MSS_CTRL_MSS_R5SS0_CORE1_AXI_RD_BUS_SAFET<br>Y_CTRL           | 50D1 8240h                |
| 18244h | 32     | MSS_CTRL_MSS_R5SS0_CORE1_AXI_RD_BUS_SAFET<br>Y_FI             | 50D1 8244h                |
| 18248h | 32     | MSS_CTRL_MSS_R5SS0_CORE1_AXI_RD_BUS_SAFET<br>Y_ERR            | 50D1 8248h                |
| 1824Ch | 32     | MSS_CTRL_MSS_R5SS0_CORE1_AXI_RD_BUS_SAFET<br>Y_ERR_STAT_DATA0 | 50D1 824Ch                |
| 18250h | 32     | MSS_CTRL_MSS_R5SS0_CORE1_AXI_RD_BUS_SAFET<br>Y_ERR_STAT_CMD   | 50D1 8250h                |
| 18254h | 32     | MSS_CTRL_MSS_R5SS0_CORE1_AXI_RD_BUS_SAFET<br>Y_ERR_STAT_READ  | 50D1 8254h                |

**Table 2-2. MSS\_CTRL Registers, Base Address=50D0 0000h, Length=131072 (continued)**

| Offset | Length | Register Name                                                                      | MSS_CTRL Physical Address |
|--------|--------|------------------------------------------------------------------------------------|---------------------------|
| 18260h | 32     | <a href="#">MSS_CTRL_MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFE<br/>TY_CTRL</a>              | 50D1 8260h                |
| 18264h | 32     | <a href="#">MSS_CTRL_MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFE<br/>TY_FI</a>                | 50D1 8264h                |
| 18268h | 32     | <a href="#">MSS_CTRL_MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFE<br/>TY_ERR</a>               | 50D1 8268h                |
| 1826Ch | 32     | <a href="#">MSS_CTRL_MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFE<br/>TY_ERR_STAT_DATA0</a>    | 50D1 826Ch                |
| 18270h | 32     | <a href="#">MSS_CTRL_MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFE<br/>TY_ERR_STAT_CMD</a>      | 50D1 8270h                |
| 18274h | 32     | <a href="#">MSS_CTRL_MSS_R5FSS1_CORE0_AXI_RD_BUS_SAFE<br/>TY_ERR_STAT_READ</a>     | 50D1 8274h                |
| 18280h | 32     | <a href="#">MSS_CTRL_MSS_R5FSS1_CORE1_AXI_RD_BUS_SAFE<br/>TY_CTRL</a>              | 50D1 8280h                |
| 18284h | 32     | <a href="#">MSS_CTRL_MSS_R5FSS1_CORE1_AXI_RD_BUS_SAFE<br/>TY_FI</a>                | 50D1 8284h                |
| 18288h | 32     | <a href="#">MSS_CTRL_MSS_R5FSS1_CORE1_AXI_RD_BUS_SAFE<br/>TY_ERR</a>               | 50D1 8288h                |
| 1828Ch | 32     | <a href="#">MSS_CTRL_MSS_R5FSS1_CORE1_AXI_RD_BUS_SAFE<br/>TY_ERR_STAT_DATA0</a>    | 50D1 828Ch                |
| 18290h | 32     | <a href="#">MSS_CTRL_MSS_R5FSS1_CORE1_AXI_RD_BUS_SAFE<br/>TY_ERR_STAT_CMD</a>      | 50D1 8290h                |
| 18294h | 32     | <a href="#">MSS_CTRL_MSS_R5FSS1_CORE1_AXI_RD_BUS_SAFE<br/>TY_ERR_STAT_READ</a>     | 50D1 8294h                |
| 182A0h | 32     | <a href="#">MSS_CTRL_MSS_R5SS0_CORE0_AXI_WR_BUS_SAFET<br/>Y_CTRL</a>               | 50D1 82A0h                |
| 182A4h | 32     | <a href="#">MSS_CTRL_MSS_R5SS0_CORE0_AXI_WR_BUS_SAFET<br/>Y_FI</a>                 | 50D1 82A4h                |
| 182A8h | 32     | <a href="#">MSS_CTRL_MSS_R5SS0_CORE0_AXI_WR_BUS_SAFET<br/>Y_ERR</a>                | 50D1 82A8h                |
| 182ACh | 32     | <a href="#">MSS_CTRL_MSS_R5SS0_CORE0_AXI_WR_BUS_SAFET<br/>Y_ERR_STAT_DATA0</a>     | 50D1 82ACh                |
| 182B0h | 32     | <a href="#">MSS_CTRL_MSS_R5SS0_CORE0_AXI_WR_BUS_SAFET<br/>Y_ERR_STAT_CMD</a>       | 50D1 82B0h                |
| 182B4h | 32     | <a href="#">MSS_CTRL_MSS_R5SS0_CORE0_AXI_WR_BUS_SAFET<br/>Y_ERR_STAT_WRITE</a>     | 50D1 82B4h                |
| 182B8h | 32     | <a href="#">MSS_CTRL_MSS_R5SS0_CORE0_AXI_WR_BUS_SAFET<br/>Y_ERR_STAT_WRITERESP</a> | 50D1 82B8h                |
| 182C0h | 32     | <a href="#">MSS_CTRL_MSS_R5SS0_CORE1_AXI_WR_BUS_SAFET<br/>Y_CTRL</a>               | 50D1 82C0h                |
| 182C4h | 32     | <a href="#">MSS_CTRL_MSS_R5SS0_CORE1_AXI_WR_BUS_SAFET<br/>Y_FI</a>                 | 50D1 82C4h                |
| 182C8h | 32     | <a href="#">MSS_CTRL_MSS_R5SS0_CORE1_AXI_WR_BUS_SAFET<br/>Y_ERR</a>                | 50D1 82C8h                |
| 182CCh | 32     | <a href="#">MSS_CTRL_MSS_R5SS0_CORE1_AXI_WR_BUS_SAFET<br/>Y_ERR_STAT_DATA0</a>     | 50D1 82CCh                |
| 182D0h | 32     | <a href="#">MSS_CTRL_MSS_R5SS0_CORE1_AXI_WR_BUS_SAFET<br/>Y_ERR_STAT_CMD</a>       | 50D1 82D0h                |
| 182D4h | 32     | <a href="#">MSS_CTRL_MSS_R5SS0_CORE1_AXI_WR_BUS_SAFET<br/>Y_ERR_STAT_WRITE</a>     | 50D1 82D4h                |
| 182D8h | 32     | <a href="#">MSS_CTRL_MSS_R5SS0_CORE1_AXI_WR_BUS_SAFET<br/>Y_ERR_STAT_WRITERESP</a> | 50D1 82D8h                |

**Table 2-2. MSS\_CTRL Registers, Base Address=50D0 0000h, Length=131072 (continued)**

| Offset | Length | Register Name                                                      | MSS_CTRL Physical Address |
|--------|--------|--------------------------------------------------------------------|---------------------------|
| 182E0h | 32     | MSS_CTRL_MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFE<br>TY_CTRL               | 50D1 82E0h                |
| 182E4h | 32     | MSS_CTRL_MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFE<br>TY_FI                 | 50D1 82E4h                |
| 182E8h | 32     | MSS_CTRL_MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFE<br>TY_ERR                | 50D1 82E8h                |
| 182ECh | 32     | MSS_CTRL_MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFE<br>TY_ERR_STAT_DATA0     | 50D1 82ECh                |
| 182F0h | 32     | MSS_CTRL_MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFE<br>TY_ERR_STAT_CMD       | 50D1 82F0h                |
| 182F4h | 32     | MSS_CTRL_MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFE<br>TY_ERR_STAT_WRITE     | 50D1 82F4h                |
| 182F8h | 32     | MSS_CTRL_MSS_R5FSS1_CORE0_AXI_WR_BUS_SAFE<br>TY_ERR_STAT_WRITERESP | 50D1 82F8h                |
| 18300h | 32     | MSS_CTRL_MSS_R5FSS1_CORE1_AXI_WR_BUS_SAFE<br>TY_CTRL               | 50D1 8300h                |
| 18304h | 32     | MSS_CTRL_MSS_R5FSS1_CORE1_AXI_WR_BUS_SAFE<br>TY_FI                 | 50D1 8304h                |
| 18308h | 32     | MSS_CTRL_MSS_R5FSS1_CORE1_AXI_WR_BUS_SAFE<br>TY_ERR                | 50D1 8308h                |
| 1830Ch | 32     | MSS_CTRL_MSS_R5FSS1_CORE1_AXI_WR_BUS_SAFE<br>TY_ERR_STAT_DATA0     | 50D1 830Ch                |
| 18310h | 32     | MSS_CTRL_MSS_R5FSS1_CORE1_AXI_WR_BUS_SAFE<br>TY_ERR_STAT_CMD       | 50D1 8310h                |
| 18314h | 32     | MSS_CTRL_MSS_R5FSS1_CORE1_AXI_WR_BUS_SAFE<br>TY_ERR_STAT_WRITE     | 50D1 8314h                |
| 18318h | 32     | MSS_CTRL_MSS_R5FSS1_CORE1_AXI_WR_BUS_SAFE<br>TY_ERR_STAT_WRITERESP | 50D1 8318h                |
| 18320h | 32     | MSS_CTRL_MSS_R5SS0_CORE0_AXI_S_BUS_SAFETY<br>_CTRL                 | 50D1 8320h                |
| 18324h | 32     | MSS_CTRL_MSS_R5SS0_CORE0_AXI_S_BUS_SAFETY<br>_FI                   | 50D1 8324h                |
| 18328h | 32     | MSS_CTRL_MSS_R5SS0_CORE0_AXI_S_BUS_SAFETY<br>_ERR                  | 50D1 8328h                |
| 1832Ch | 32     | MSS_CTRL_MSS_R5SS0_CORE0_AXI_S_BUS_SAFETY<br>_ERR_STAT_DATA0       | 50D1 832Ch                |
| 18330h | 32     | MSS_CTRL_MSS_R5SS0_CORE0_AXI_S_BUS_SAFETY<br>_ERR_STAT_CMD         | 50D1 8330h                |
| 18334h | 32     | MSS_CTRL_MSS_R5SS0_CORE0_AXI_S_BUS_SAFETY<br>_ERR_STAT_WRITE       | 50D1 8334h                |
| 18338h | 32     | MSS_CTRL_MSS_R5SS0_CORE0_AXI_S_BUS_SAFETY<br>_ERR_STAT_READ        | 50D1 8338h                |
| 1833Ch | 32     | MSS_CTRL_MSS_R5SS0_CORE0_AXI_S_BUS_SAFETY<br>_ERR_STAT_WRITERESP   | 50D1 833Ch                |
| 18340h | 32     | MSS_CTRL_MSS_R5SS0_CORE1_AXI_S_BUS_SAFETY<br>_CTRL                 | 50D1 8340h                |
| 18344h | 32     | MSS_CTRL_MSS_R5SS0_CORE1_AXI_S_BUS_SAFETY<br>_FI                   | 50D1 8344h                |
| 18348h | 32     | MSS_CTRL_MSS_R5SS0_CORE1_AXI_S_BUS_SAFETY<br>_ERR                  | 50D1 8348h                |
| 1834Ch | 32     | MSS_CTRL_MSS_R5SS0_CORE1_AXI_S_BUS_SAFETY<br>_ERR_STAT_DATA0       | 50D1 834Ch                |

**Table 2-2. MSS\_CTRL Registers, Base Address=50D0 0000h, Length=131072 (continued)**

| Offset | Length | Register Name                                                 | MSS_CTRL Physical Address |
|--------|--------|---------------------------------------------------------------|---------------------------|
| 18350h | 32     | MSS_CTRL_MSS_R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_CMD        | 50D1 8350h                |
| 18354h | 32     | MSS_CTRL_MSS_R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE      | 50D1 8354h                |
| 18358h | 32     | MSS_CTRL_MSS_R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_READ       | 50D1 8358h                |
| 1835Ch | 32     | MSS_CTRL_MSS_R5SS0_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP  | 50D1 835Ch                |
| 18360h | 32     | MSS_CTRL_MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_CTRL               | 50D1 8360h                |
| 18364h | 32     | MSS_CTRL_MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_FI                 | 50D1 8364h                |
| 18368h | 32     | MSS_CTRL_MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR                | 50D1 8368h                |
| 1836Ch | 32     | MSS_CTRL_MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0     | 50D1 836Ch                |
| 18370h | 32     | MSS_CTRL_MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_CMD       | 50D1 8370h                |
| 18374h | 32     | MSS_CTRL_MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE     | 50D1 8374h                |
| 18378h | 32     | MSS_CTRL_MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_READ      | 50D1 8378h                |
| 1837Ch | 32     | MSS_CTRL_MSS_R5FSS1_CORE0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP | 50D1 837Ch                |
| 18380h | 32     | MSS_CTRL_MSS_R5FSS1_CORE1_AXI_S_BUS_SAFETY_CTRL               | 50D1 8380h                |
| 18384h | 32     | MSS_CTRL_MSS_R5FSS1_CORE1_AXI_S_BUS_SAFETY_FI                 | 50D1 8384h                |
| 18388h | 32     | MSS_CTRL_MSS_R5FSS1_CORE1_AXI_S_BUS_SAFETY_ERR                | 50D1 8388h                |
| 1838Ch | 32     | MSS_CTRL_MSS_R5FSS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_DATA0     | 50D1 838Ch                |
| 18390h | 32     | MSS_CTRL_MSS_R5FSS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_CMD       | 50D1 8390h                |
| 18394h | 32     | MSS_CTRL_MSS_R5FSS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE     | 50D1 8394h                |
| 18398h | 32     | MSS_CTRL_MSS_R5FSS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_READ      | 50D1 8398h                |
| 1839Ch | 32     | MSS_CTRL_MSS_R5FSS1_CORE1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP | 50D1 839Ch                |
| 183A0h | 32     | MSS_CTRL_MSS_TPTC_A0_RD_BUS_SAFETY_CTRL                       | 50D1 83A0h                |
| 183A4h | 32     | MSS_CTRL_MSS_TPTC_A0_RD_BUS_SAFETY_FI                         | 50D1 83A4h                |
| 183A8h | 32     | MSS_CTRL_MSS_TPTC_A0_RD_BUS_SAFETY_ERR                        | 50D1 83A8h                |
| 183ACh | 32     | MSS_CTRL_MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_DATA0             | 50D1 83ACh                |
| 183B0h | 32     | MSS_CTRL_MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_CMD               | 50D1 83B0h                |
| 183B4h | 32     | MSS_CTRL_MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_READ              | 50D1 83B4h                |
| 183C0h | 32     | MSS_CTRL_MSS_TPTC_A1_RD_BUS_SAFETY_CTRL                       | 50D1 83C0h                |
| 183C4h | 32     | MSS_CTRL_MSS_TPTC_A1_RD_BUS_SAFETY_FI                         | 50D1 83C4h                |
| 183C8h | 32     | MSS_CTRL_MSS_TPTC_A1_RD_BUS_SAFETY_ERR                        | 50D1 83C8h                |



**Table 2-2. MSS\_CTRL Registers, Base Address=50D0 0000h, Length=131072 (continued)**

| Offset | Length | Register Name                                             | MSS_CTRL Physical Address |
|--------|--------|-----------------------------------------------------------|---------------------------|
| 183CCh | 32     | MSS_CTRL_MSS_TPTC_A1_RD_BUS_SAFETY_ERR_ST<br>AT_DATA0     | 50D1 83CCh                |
| 183D0h | 32     | MSS_CTRL_MSS_TPTC_A1_RD_BUS_SAFETY_ERR_ST<br>AT_CMD       | 50D1 83D0h                |
| 183D4h | 32     | MSS_CTRL_MSS_TPTC_A1_RD_BUS_SAFETY_ERR_ST<br>AT_READ      | 50D1 83D4h                |
| 183E0h | 32     | MSS_CTRL_MSS_TPTC_A0_WR_BUS_SAFETY_CTRL                   | 50D1 83E0h                |
| 183E4h | 32     | MSS_CTRL_MSS_TPTC_A0_WR_BUS_SAFETY_FI                     | 50D1 83E4h                |
| 183E8h | 32     | MSS_CTRL_MSS_TPTC_A0_WR_BUS_SAFETY_ERR                    | 50D1 83E8h                |
| 183ECh | 32     | MSS_CTRL_MSS_TPTC_A0_WR_BUS_SAFETY_ERR_S<br>TAT_DATA0     | 50D1 83ECh                |
| 183F0h | 32     | MSS_CTRL_MSS_TPTC_A0_WR_BUS_SAFETY_ERR_S<br>TAT_CMD       | 50D1 83F0h                |
| 183F4h | 32     | MSS_CTRL_MSS_TPTC_A0_WR_BUS_SAFETY_ERR_S<br>TAT_WRITE     | 50D1 83F4h                |
| 183F8h | 32     | MSS_CTRL_MSS_TPTC_A0_WR_BUS_SAFETY_ERR_S<br>TAT_WRITERESP | 50D1 83F8h                |
| 18400h | 32     | MSS_CTRL_MSS_TPTC_A1_WR_BUS_SAFETY_CTRL                   | 50D1 8400h                |
| 18404h | 32     | MSS_CTRL_MSS_TPTC_A1_WR_BUS_SAFETY_FI                     | 50D1 8404h                |
| 18408h | 32     | MSS_CTRL_MSS_TPTC_A1_WR_BUS_SAFETY_ERR                    | 50D1 8408h                |
| 1840Ch | 32     | MSS_CTRL_MSS_TPTC_A1_WR_BUS_SAFETY_ERR_S<br>TAT_DATA0     | 50D1 840Ch                |
| 18410h | 32     | MSS_CTRL_MSS_TPTC_A1_WR_BUS_SAFETY_ERR_S<br>TAT_CMD       | 50D1 8410h                |
| 18414h | 32     | MSS_CTRL_MSS_TPTC_A1_WR_BUS_SAFETY_ERR_S<br>TAT_WRITE     | 50D1 8414h                |
| 18418h | 32     | MSS_CTRL_MSS_TPTC_A1_WR_BUS_SAFETY_ERR_S<br>TAT_WRITERESP | 50D1 8418h                |
| 18420h | 32     | MSS_CTRL_HSM_TPTC_A0_RD_BUS_SAFETY_CTRL                   | 50D1 8420h                |
| 18424h | 32     | MSS_CTRL_HSM_TPTC_A0_RD_BUS_SAFETY_FI                     | 50D1 8424h                |
| 18428h | 32     | MSS_CTRL_HSM_TPTC_A0_RD_BUS_SAFETY_ERR                    | 50D1 8428h                |
| 1842Ch | 32     | MSS_CTRL_HSM_TPTC_A0_RD_BUS_SAFETY_ERR_S<br>TAT_DATA0     | 50D1 842Ch                |
| 18430h | 32     | MSS_CTRL_HSM_TPTC_A0_RD_BUS_SAFETY_ERR_S<br>TAT_CMD       | 50D1 8430h                |
| 18434h | 32     | MSS_CTRL_HSM_TPTC_A0_RD_BUS_SAFETY_ERR_S<br>TAT_READ      | 50D1 8434h                |
| 18440h | 32     | MSS_CTRL_HSM_TPTC_A1_RD_BUS_SAFETY_CTRL                   | 50D1 8440h                |
| 18444h | 32     | MSS_CTRL_HSM_TPTC_A1_RD_BUS_SAFETY_FI                     | 50D1 8444h                |
| 18448h | 32     | MSS_CTRL_HSM_TPTC_A1_RD_BUS_SAFETY_ERR                    | 50D1 8448h                |
| 1844Ch | 32     | MSS_CTRL_HSM_TPTC_A1_RD_BUS_SAFETY_ERR_S<br>TAT_DATA0     | 50D1 844Ch                |
| 18450h | 32     | MSS_CTRL_HSM_TPTC_A1_RD_BUS_SAFETY_ERR_S<br>TAT_CMD       | 50D1 8450h                |
| 18454h | 32     | MSS_CTRL_HSM_TPTC_A1_RD_BUS_SAFETY_ERR_S<br>TAT_READ      | 50D1 8454h                |
| 18460h | 32     | MSS_CTRL_HSM_TPTC_A0_WR_BUS_SAFETY_CTRL                   | 50D1 8460h                |
| 18464h | 32     | MSS_CTRL_HSM_TPTC_A0_WR_BUS_SAFETY_FI                     | 50D1 8464h                |
| 18468h | 32     | MSS_CTRL_HSM_TPTC_A0_WR_BUS_SAFETY_ERR                    | 50D1 8468h                |
| 1846Ch | 32     | MSS_CTRL_HSM_TPTC_A0_WR_BUS_SAFETY_ERR_S<br>TAT_DATA0     | 50D1 846Ch                |

**Table 2-2. MSS\_CTRL Registers, Base Address=50D0 0000h, Length=131072 (continued)**

| Offset | Length | Register Name                                             | MSS_CTRL Physical Address |
|--------|--------|-----------------------------------------------------------|---------------------------|
| 18470h | 32     | MSS_CTRL_HSM_TPTC_A0_WR_BUS_SAFETY_ERR_S<br>TAT_CMD       | 50D1 8470h                |
| 18474h | 32     | MSS_CTRL_HSM_TPTC_A0_WR_BUS_SAFETY_ERR_S<br>TAT_WRITE     | 50D1 8474h                |
| 18478h | 32     | MSS_CTRL_HSM_TPTC_A0_WR_BUS_SAFETY_ERR_S<br>TAT_WRITERESP | 50D1 8478h                |
| 18480h | 32     | MSS_CTRL_HSM_TPTC_A1_WR_BUS_SAFETY_CTRL                   | 50D1 8480h                |
| 18484h | 32     | MSS_CTRL_HSM_TPTC_A1_WR_BUS_SAFETY_FI                     | 50D1 8484h                |
| 18488h | 32     | MSS_CTRL_HSM_TPTC_A1_WR_BUS_SAFETY_ERR                    | 50D1 8488h                |
| 1848Ch | 32     | MSS_CTRL_HSM_TPTC_A1_WR_BUS_SAFETY_ERR_S<br>TAT_DATA0     | 50D1 848Ch                |
| 18490h | 32     | MSS_CTRL_HSM_TPTC_A1_WR_BUS_SAFETY_ERR_S<br>TAT_CMD       | 50D1 8490h                |
| 18494h | 32     | MSS_CTRL_HSM_TPTC_A1_WR_BUS_SAFETY_ERR_S<br>TAT_WRITE     | 50D1 8494h                |
| 18498h | 32     | MSS_CTRL_HSM_TPTC_A1_WR_BUS_SAFETY_ERR_S<br>TAT_WRITERESP | 50D1 8498h                |
| 184A0h | 32     | MSS_CTRL_MSS_QSPI_BUS_SAFETY_CTRL                         | 50D1 84A0h                |
| 184A4h | 32     | MSS_CTRL_MSS_QSPI_BUS_SAFETY_FI                           | 50D1 84A4h                |
| 184A8h | 32     | MSS_CTRL_MSS_QSPI_BUS_SAFETY_ERR                          | 50D1 84A8h                |
| 184ACh | 32     | MSS_CTRL_MSS_QSPI_BUS_SAFETY_ERR_STAT_DAT<br>A0           | 50D1 84ACh                |
| 184B0h | 32     | MSS_CTRL_MSS_QSPI_BUS_SAFETY_ERR_STAT_CMD                 | 50D1 84B0h                |
| 184B4h | 32     | MSS_CTRL_MSS_QSPI_BUS_SAFETY_ERR_STAT_WRI<br>TE           | 50D1 84B4h                |
| 184B8h | 32     | MSS_CTRL_MSS_QSPI_BUS_SAFETY_ERR_STAT_REA<br>D            | 50D1 84B8h                |
| 184BCh | 32     | MSS_CTRL_MSS_QSPI_BUS_SAFETY_ERR_STAT_WRI<br>TERESP       | 50D1 84BCh                |
| 18540h | 32     | MSS_CTRL_MSS_MCRC_BUS_SAFETY_CTRL                         | 50D1 8540h                |
| 18544h | 32     | MSS_CTRL_MSS_MCRC_BUS_SAFETY_FI                           | 50D1 8544h                |
| 18548h | 32     | MSS_CTRL_MSS_MCRC_BUS_SAFETY_ERR                          | 50D1 8548h                |
| 1854Ch | 32     | MSS_CTRL_MSS_MCRC_BUS_SAFETY_ERR_STAT_DA<br>TA0           | 50D1 854Ch                |
| 18550h | 32     | MSS_CTRL_MSS_MCRC_BUS_SAFETY_ERR_STAT_CM<br>D             | 50D1 8550h                |
| 18554h | 32     | MSS_CTRL_MSS_MCRC_BUS_SAFETY_ERR_STAT_WRI<br>TE           | 50D1 8554h                |
| 18558h | 32     | MSS_CTRL_MSS_MCRC_BUS_SAFETY_ERR_STAT_RE<br>AD            | 50D1 8558h                |
| 1855Ch | 32     | MSS_CTRL_MSS_MCRC_BUS_SAFETY_ERR_STAT_WRI<br>TERESP       | 50D1 855Ch                |
| 185E0h | 32     | MSS_CTRL_PRU_ICSSSLAVE_BUS_SAFETY_CTRL                    | 50D1 85E0h                |
| 185E4h | 32     | MSS_CTRL_PRU_ICSSSLAVE_BUS_SAFETY_FI                      | 50D1 85E4h                |
| 185E8h | 32     | MSS_CTRL_PRU_ICSSSLAVE_BUS_SAFETY_ERR                     | 50D1 85E8h                |
| 185ECh | 32     | MSS_CTRL_PRU_ICSSSLAVE_BUS_SAFETY_ERR_STA<br>T_DATA0      | 50D1 85ECh                |
| 185F0h | 32     | MSS_CTRL_PRU_ICSSSLAVE_BUS_SAFETY_ERR_STA<br>T_CMD        | 50D1 85F0h                |
| 185F4h | 32     | MSS_CTRL_PRU_ICSSSLAVE_BUS_SAFETY_ERR_STA<br>T_WRITE      | 50D1 85F4h                |

**Table 2-2. MSS\_CTRL Registers, Base Address=50D0 0000h, Length=131072 (continued)**

| Offset | Length | Register Name                                            | MSS_CTRL Physical Address |
|--------|--------|----------------------------------------------------------|---------------------------|
| 185F8h | 32     | MSS_CTRL_PRU_ICSSSLAVE_BUS_SAFETY_ERR_STA<br>T_READ      | 50D1 85F8h                |
| 185FCh | 32     | MSS_CTRL_PRU_ICSSSLAVE_BUS_SAFETY_ERR_STA<br>T_WRITERESP | 50D1 85FCh                |
| 18620h | 32     | MSS_CTRL_MSS_L2_A_BUS_SAFETY_CTRL                        | 50D1 8620h                |
| 18624h | 32     | MSS_CTRL_MSS_L2_A_BUS_SAFETY_FI                          | 50D1 8624h                |
| 18628h | 32     | MSS_CTRL_MSS_L2_A_BUS_SAFETY_ERR                         | 50D1 8628h                |
| 1862Ch | 32     | MSS_CTRL_MSS_L2_A_BUS_SAFETY_ERR_STAT_DAT<br>A0          | 50D1 862Ch                |
| 18630h | 32     | MSS_CTRL_MSS_L2_A_BUS_SAFETY_ERR_STAT_CMD                | 50D1 8630h                |
| 18634h | 32     | MSS_CTRL_MSS_L2_A_BUS_SAFETY_ERR_STAT_WRI<br>TE          | 50D1 8634h                |
| 18638h | 32     | MSS_CTRL_MSS_L2_A_BUS_SAFETY_ERR_STAT_REA<br>D           | 50D1 8638h                |
| 1863Ch | 32     | MSS_CTRL_MSS_L2_A_BUS_SAFETY_ERR_STAT_WRI<br>TERESP      | 50D1 863Ch                |
| 18640h | 32     | MSS_CTRL_MSS_L2_B_BUS_SAFETY_CTRL                        | 50D1 8640h                |
| 18644h | 32     | MSS_CTRL_MSS_L2_B_BUS_SAFETY_FI                          | 50D1 8644h                |
| 18648h | 32     | MSS_CTRL_MSS_L2_B_BUS_SAFETY_ERR                         | 50D1 8648h                |
| 1864Ch | 32     | MSS_CTRL_MSS_L2_B_BUS_SAFETY_ERR_STAT_DAT<br>A0          | 50D1 864Ch                |
| 18650h | 32     | MSS_CTRL_MSS_L2_B_BUS_SAFETY_ERR_STAT_CMD                | 50D1 8650h                |
| 18654h | 32     | MSS_CTRL_MSS_L2_B_BUS_SAFETY_ERR_STAT_WRI<br>TE          | 50D1 8654h                |
| 18658h | 32     | MSS_CTRL_MSS_L2_B_BUS_SAFETY_ERR_STAT_REA<br>D           | 50D1 8658h                |
| 1865Ch | 32     | MSS_CTRL_MSS_L2_B_BUS_SAFETY_ERR_STAT_WRI<br>TERESP      | 50D1 865Ch                |
| 18660h | 32     | MSS_CTRL_MSS_L2_C_BUS_SAFETY_CTRL                        | 50D1 8660h                |
| 18664h | 32     | MSS_CTRL_MSS_L2_C_BUS_SAFETY_FI                          | 50D1 8664h                |
| 18668h | 32     | MSS_CTRL_MSS_L2_C_BUS_SAFETY_ERR                         | 50D1 8668h                |
| 1866Ch | 32     | MSS_CTRL_MSS_L2_C_BUS_SAFETY_ERR_STAT_DAT<br>A0          | 50D1 866Ch                |
| 18670h | 32     | MSS_CTRL_MSS_L2_C_BUS_SAFETY_ERR_STAT_CMD                | 50D1 8670h                |
| 18674h | 32     | MSS_CTRL_MSS_L2_C_BUS_SAFETY_ERR_STAT_WRI<br>TE          | 50D1 8674h                |
| 18678h | 32     | MSS_CTRL_MSS_L2_C_BUS_SAFETY_ERR_STAT_REA<br>D           | 50D1 8678h                |
| 1867Ch | 32     | MSS_CTRL_MSS_L2_C_BUS_SAFETY_ERR_STAT_WRI<br>TERESP      | 50D1 867Ch                |
| 18680h | 32     | MSS_CTRL_MSS_L2_D_BUS_SAFETY_CTRL                        | 50D1 8680h                |
| 18684h | 32     | MSS_CTRL_MSS_L2_D_BUS_SAFETY_FI                          | 50D1 8684h                |
| 18688h | 32     | MSS_CTRL_MSS_L2_D_BUS_SAFETY_ERR                         | 50D1 8688h                |
| 1868Ch | 32     | MSS_CTRL_MSS_L2_D_BUS_SAFETY_ERR_STAT_DAT<br>A0          | 50D1 868Ch                |
| 18690h | 32     | MSS_CTRL_MSS_L2_D_BUS_SAFETY_ERR_STAT_CMD                | 50D1 8690h                |
| 18694h | 32     | MSS_CTRL_MSS_L2_D_BUS_SAFETY_ERR_STAT_WRI<br>TE          | 50D1 8694h                |
| 18698h | 32     | MSS_CTRL_MSS_L2_D_BUS_SAFETY_ERR_STAT_REA<br>D           | 50D1 8698h                |

**Table 2-2. MSS\_CTRL Registers, Base Address=50D0 0000h, Length=131072 (continued)**

| Offset | Length | Register Name                                           | MSS_CTRL Physical Address |
|--------|--------|---------------------------------------------------------|---------------------------|
| 1869Ch | 32     | MSS_CTRL_MSS_L2_D_BUS_SAFETY_ERR_STAT_WRI<br>TERESP     | 50D1 869Ch                |
| 186A0h | 32     | MSS_CTRL_MSS_MBOX_BUS_SAFETY_CTRL                       | 50D1 86A0h                |
| 186A4h | 32     | MSS_CTRL_MSS_MBOX_BUS_SAFETY_FI                         | 50D1 86A4h                |
| 186A8h | 32     | MSS_CTRL_MSS_MBOX_BUS_SAFETY_ERR                        | 50D1 86A8h                |
| 186ACh | 32     | MSS_CTRL_MSS_MBOX_BUS_SAFETY_ERR_STAT_DA<br>TA0         | 50D1 86ACh                |
| 186B0h | 32     | MSS_CTRL_MSS_MBOX_BUS_SAFETY_ERR_STAT_CM<br>D           | 50D1 86B0h                |
| 186B4h | 32     | MSS_CTRL_MSS_MBOX_BUS_SAFETY_ERR_STAT_WR<br>ITE         | 50D1 86B4h                |
| 186B8h | 32     | MSS_CTRL_MSS_MBOX_BUS_SAFETY_ERR_STAT_RE<br>AD          | 50D1 86B8h                |
| 186BCh | 32     | MSS_CTRL_MSS_MBOX_BUS_SAFETY_ERR_STAT_WR<br>ITERESP     | 50D1 86BCh                |
| 186C0h | 32     | MSS_CTRL_MSS_STM_STIM_BUS_SAFETY_CTRL                   | 50D1 86C0h                |
| 186C4h | 32     | MSS_CTRL_MSS_STM_STIM_BUS_SAFETY_FI                     | 50D1 86C4h                |
| 186C8h | 32     | MSS_CTRL_MSS_STM_STIM_BUS_SAFETY_ERR                    | 50D1 86C8h                |
| 186CCh | 32     | MSS_CTRL_MSS_STM_STIM_BUS_SAFETY_ERR_STAT<br>_DATA0     | 50D1 86CCh                |
| 186D0h | 32     | MSS_CTRL_MSS_STM_STIM_BUS_SAFETY_ERR_STAT<br>_CMD       | 50D1 86D0h                |
| 186D4h | 32     | MSS_CTRL_MSS_STM_STIM_BUS_SAFETY_ERR_STAT<br>_WRITE     | 50D1 86D4h                |
| 186D8h | 32     | MSS_CTRL_MSS_STM_STIM_BUS_SAFETY_ERR_STAT<br>_READ      | 50D1 86D8h                |
| 186DCh | 32     | MSS_CTRL_MSS_STM_STIM_BUS_SAFETY_ERR_STAT<br>_WRITERESP | 50D1 86DCh                |
| 186E0h | 32     | MSS_CTRL_MSS_MMC_BUS_SAFETY_CTRL                        | 50D1 86E0h                |
| 186E4h | 32     | MSS_CTRL_MSS_MMC_BUS_SAFETY_FI                          | 50D1 86E4h                |
| 186E8h | 32     | MSS_CTRL_MSS_MMC_BUS_SAFETY_ERR                         | 50D1 86E8h                |
| 186ECh | 32     | MSS_CTRL_MSS_MMC_BUS_SAFETY_ERR_STAT_DAT<br>A0          | 50D1 86ECh                |
| 186F0h | 32     | MSS_CTRL_MSS_MMC_BUS_SAFETY_ERR_STAT_CMD                | 50D1 86F0h                |
| 186F4h | 32     | MSS_CTRL_MSS_MMC_BUS_SAFETY_ERR_STAT_WRI<br>TE          | 50D1 86F4h                |
| 186F8h | 32     | MSS_CTRL_MSS_MMC_BUS_SAFETY_ERR_STAT_REA<br>D           | 50D1 86F8h                |
| 186FCh | 32     | MSS_CTRL_MSS_MMC_BUS_SAFETY_ERR_STAT_WRI<br>TERESP      | 50D1 86FCh                |
| 18700h | 32     | MSS_CTRL_MSS_GPMC_BUS_SAFETY_CTRL                       | 50D1 8700h                |
| 18704h | 32     | MSS_CTRL_MSS_GPMC_BUS_SAFETY_FI                         | 50D1 8704h                |
| 18708h | 32     | MSS_CTRL_MSS_GPMC_BUS_SAFETY_ERR                        | 50D1 8708h                |
| 1870Ch | 32     | MSS_CTRL_MSS_GPMC_BUS_SAFETY_ERR_STAT_DA<br>TA0         | 50D1 870Ch                |
| 18710h | 32     | MSS_CTRL_MSS_GPMC_BUS_SAFETY_ERR_STAT_CM<br>D           | 50D1 8710h                |
| 18714h | 32     | MSS_CTRL_MSS_GPMC_BUS_SAFETY_ERR_STAT_WR<br>ITE         | 50D1 8714h                |
| 18718h | 32     | MSS_CTRL_MSS_GPMC_BUS_SAFETY_ERR_STAT_RE<br>AD          | 50D1 8718h                |

**Table 2-2. MSS\_CTRL Registers, Base Address=50D0 0000h, Length=131072 (continued)**

| Offset | Length | Register Name                                               | MSS_CTRL Physical Address |
|--------|--------|-------------------------------------------------------------|---------------------------|
| 1871Ch | 32     | MSS_CTRL_MSS_GPMC_BUS_SAFETY_ERR_STAT_WRITERESP             | 50D1 871Ch                |
| 18740h | 32     | MSS_CTRL_MSS_R5SS0_CORE0_AHB_BUS_SAFETY_CTRL                | 50D1 8740h                |
| 18744h | 32     | MSS_CTRL_MSS_R5SS0_CORE0_AHB_BUS_SAFETY_FI                  | 50D1 8744h                |
| 18748h | 32     | MSS_CTRL_MSS_R5SS0_CORE0_AHB_BUS_SAFETY_ERR                 | 50D1 8748h                |
| 1874Ch | 32     | MSS_CTRL_MSS_R5SS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_DATA0      | 50D1 874Ch                |
| 18750h | 32     | MSS_CTRL_MSS_R5SS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_CMD        | 50D1 8750h                |
| 18754h | 32     | MSS_CTRL_MSS_R5SS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITE      | 50D1 8754h                |
| 18758h | 32     | MSS_CTRL_MSS_R5SS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_READ       | 50D1 8758h                |
| 1875Ch | 32     | MSS_CTRL_MSS_R5SS0_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITERESP  | 50D1 875Ch                |
| 18760h | 32     | MSS_CTRL_MSS_R5SS0_CORE1_AHB_BUS_SAFETY_CTRL                | 50D1 8760h                |
| 18764h | 32     | MSS_CTRL_MSS_R5SS0_CORE1_AHB_BUS_SAFETY_FI                  | 50D1 8764h                |
| 18768h | 32     | MSS_CTRL_MSS_R5SS0_CORE1_AHB_BUS_SAFETY_ERR                 | 50D1 8768h                |
| 1876Ch | 32     | MSS_CTRL_MSS_R5SS0_CORE1_AHB_BUS_SAFETY_ERR_STAT_DATA0      | 50D1 876Ch                |
| 18770h | 32     | MSS_CTRL_MSS_R5SS0_CORE1_AHB_BUS_SAFETY_ERR_STAT_CMD        | 50D1 8770h                |
| 18774h | 32     | MSS_CTRL_MSS_R5SS0_CORE1_AHB_BUS_SAFETY_ERR_STAT_WRITE      | 50D1 8774h                |
| 18778h | 32     | MSS_CTRL_MSS_R5SS0_CORE1_AHB_BUS_SAFETY_ERR_STAT_READ       | 50D1 8778h                |
| 1877Ch | 32     | MSS_CTRL_MSS_R5SS0_CORE1_AHB_BUS_SAFETY_ERR_STAT_WRITERESP  | 50D1 877Ch                |
| 18780h | 32     | MSS_CTRL_MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_CTRL               | 50D1 8780h                |
| 18784h | 32     | MSS_CTRL_MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_FI                 | 50D1 8784h                |
| 18788h | 32     | MSS_CTRL_MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR                | 50D1 8788h                |
| 1878Ch | 32     | MSS_CTRL_MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_DATA0     | 50D1 878Ch                |
| 18790h | 32     | MSS_CTRL_MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_CMD       | 50D1 8790h                |
| 18794h | 32     | MSS_CTRL_MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITE     | 50D1 8794h                |
| 18798h | 32     | MSS_CTRL_MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_READ      | 50D1 8798h                |
| 1879Ch | 32     | MSS_CTRL_MSS_R5FSS1_CORE0_AHB_BUS_SAFETY_ERR_STAT_WRITERESP | 50D1 879Ch                |
| 187A0h | 32     | MSS_CTRL_MSS_R5FSS1_CORE1_AHB_BUS_SAFETY_CTRL               | 50D1 87A0h                |

**Table 2-2. MSS\_CTRL Registers, Base Address=50D0 0000h, Length=131072 (continued)**

| Offset | Length | Register Name                                                               | MSS_CTRL Physical Address |
|--------|--------|-----------------------------------------------------------------------------|---------------------------|
| 187A4h | 32     | <a href="#">MSS_CTRL_MSS_R5FSS1_CORE1_AHB_BUS_SAFETY_FI</a>                 | 50D1 87A4h                |
| 187A8h | 32     | <a href="#">MSS_CTRL_MSS_R5FSS1_CORE1_AHB_BUS_SAFETY_ERR</a>                | 50D1 87A8h                |
| 187ACh | 32     | <a href="#">MSS_CTRL_MSS_R5FSS1_CORE1_AHB_BUS_SAFETY_ERR_STAT_DATA0</a>     | 50D1 87ACh                |
| 187B0h | 32     | <a href="#">MSS_CTRL_MSS_R5FSS1_CORE1_AHB_BUS_SAFETY_ERR_STAT_CMD</a>       | 50D1 87B0h                |
| 187B4h | 32     | <a href="#">MSS_CTRL_MSS_R5FSS1_CORE1_AHB_BUS_SAFETY_ERR_STAT_WRITE</a>     | 50D1 87B4h                |
| 187B8h | 32     | <a href="#">MSS_CTRL_MSS_R5FSS1_CORE1_AHB_BUS_SAFETY_ERR_STAT_READ</a>      | 50D1 87B8h                |
| 187BCh | 32     | <a href="#">MSS_CTRL_MSS_R5FSS1_CORE1_AHB_BUS_SAFETY_ERR_STAT_WRITERESP</a> | 50D1 87BCh                |

## 2.2.2 MSS\_CTRL Registers

### MSS\_CTRL Registers

### 2.2.2.1 MSS\_CTRL\_R5SS0\_CONTROL Register

#### 1 MSS\_CTRL\_R5SS0\_CONTROL Register (Offset = 20h) [reset = 707h]

This register is used to configure R5SS0 in Lock step or Dual core mode. The mode change can be affected only once in a SOC power cycle.

Return to [Summary Table](#)

**Table 2-3. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0020h       |

**Figure 2-1. MSS\_CTRL\_R5SS0\_CONTROL Name Register**

| 31       | 30 | 29 | 28 | 27 | 26                                  | 25 | 24 |
|----------|----|----|----|----|-------------------------------------|----|----|
| RESERVED |    |    |    |    | R5SS0_CONTROL_ROM_WAIT_STATE        |    |    |
| NONE     |    |    |    |    | R/W                                 |    |    |
| 0h       |    |    |    |    | 0h                                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                                  | 17 | 16 |
| RESERVED |    |    |    |    | R5SS0_CONTROL_RESET_FSM_TRIGGER     |    |    |
| NONE     |    |    |    |    | R/W                                 |    |    |
| 0h       |    |    |    |    | 0h                                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                                  | 9  | 8  |
| RESERVED |    |    |    |    | R5SS0_CONTROL_LOCK_STEP_SWITCH_WAIT |    |    |
| NONE     |    |    |    |    | R/W                                 |    |    |
| 0h       |    |    |    |    | 7h                                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                                   | 1  | 0  |
| RESERVED |    |    |    |    | R5SS0_CONTROL_LOCK_STEP             |    |    |
| NONE     |    |    |    |    | R/W                                 |    |    |
| 0h       |    |    |    |    | 7h                                  |    |    |

**Table 2-5. MSS\_CTRL\_R5SS0\_CONTROL Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                                                                                                                                                                                      |
|-------|-------------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:27 | RESERVED                            | NONE | 0h    | Reserved                                                                                                                                                                                                                         |
| 26:24 | R5SS0_CONTROL_ROM_WAIT_STATE        | R/W  | 0h    | Writing 3'b111 enables a single cycle wait state with respect to CR5A_clk for rom access. This needs to be set when R5 clock is at 400MHZ and Interconnect-clk is at 200MHZ. [because it is a timing issue in this scenario]     |
| 23:19 | RESERVED                            | NONE | 0h    | Reserved                                                                                                                                                                                                                         |
| 18:16 | R5SS0_CONTROL_RESET_FSM_TRIGGER     | R/W  | 0h    | Write pulse bit field:<br>Writing 3'b111 will trigger the reset FSM.<br>Reset FSM ensures reset to R5SS and inturn ensures the latching of lock_step and also mem_swap bit                                                       |
| 15:11 | RESERVED                            | NONE | 0h    | Reserved                                                                                                                                                                                                                         |
| 10:8  | R5SS0_CONTROL_LOCK_STEP_SWITCH_WAIT | R/W  | 7h    | Writing 3'b111 ensures switch happens only after R5SS reset. Or else it will be a immediate switch.                                                                                                                              |
| 7:3   | RESERVED                            | NONE | 0h    | Reserved                                                                                                                                                                                                                         |
| 2:0   | R5SS0_CONTROL_LOCK_STEP             | R/W  | 7h    | Writing 3'b000 ensures R5 to be in Dual-Core mode.<br>Note: The change happens after the R5SS reset assertion if corresponding R5SS_CONTROL_LOCK_STEP_SWITCH_WAIT is set. Or else the switching to Dual-core happens on the fly. |

### 2.2.2.2 MSS\_CTRL\_R5SS0\_CORE0\_HALT Register

#### 1 MSS\_CTRL\_R5SS0\_CORE0\_HALT Register (Offset = 24h) [reset = 7h]

This register is used to Halt or Unhalt R5SS0 Core 0

Return to [Summary Table](#)

**Table 2-6. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0024h       |

**Figure 2-2. MSS\_CTRL\_R5SS0\_CORE0\_HALT Name Register**

|          |    |    |    |    |                       |    |    |
|----------|----|----|----|----|-----------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                    | 25 | 24 |
| RESERVED |    |    |    |    |                       |    |    |
| NONE     |    |    |    |    |                       |    |    |
| 0h       |    |    |    |    |                       |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                    | 17 | 16 |
| RESERVED |    |    |    |    |                       |    |    |
| NONE     |    |    |    |    |                       |    |    |
| 0h       |    |    |    |    |                       |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                    | 9  | 8  |
| RESERVED |    |    |    |    |                       |    |    |
| NONE     |    |    |    |    |                       |    |    |
| 0h       |    |    |    |    |                       |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                     | 1  | 0  |
| RESERVED |    |    |    |    | R5SS0_COREA_HALT_HALT |    |    |
| NONE     |    |    |    |    | R/W                   |    |    |
| 0h       |    |    |    |    | 7h                    |    |    |

**Table 2-8. MSS\_CTRL\_R5SS0\_CORE0\_HALT Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                                 |
|------|-----------------------|------|-------|-----------------------------------------------------------------------------|
| 31:3 | RESERVED              | NONE | 0h    | Reserved                                                                    |
| 2:0  | R5SS0_COREA_HALT_HALT | R/W  | 7h    | Writing 3'b000 will unhalt CR5A. This register should be written only once. |



### 2.2.2.3 MSS\_CTRL\_R5SS0\_CORE1\_HALT Register

#### 1 MSS\_CTRL\_R5SS0\_CORE1\_HALT Register (Offset = 28h) [reset = 7h]

This register is used to Halt or Unhalt R5SS0 Core 1

Return to [Summary Table](#)

**Table 2-9. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0028h       |

**Figure 2-3. MSS\_CTRL\_R5SS0\_CORE1\_HALT Name Register**

|          |    |    |    |    |                       |    |    |
|----------|----|----|----|----|-----------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                    | 25 | 24 |
| RESERVED |    |    |    |    |                       |    |    |
| NONE     |    |    |    |    |                       |    |    |
| 0h       |    |    |    |    |                       |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                    | 17 | 16 |
| RESERVED |    |    |    |    |                       |    |    |
| NONE     |    |    |    |    |                       |    |    |
| 0h       |    |    |    |    |                       |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                    | 9  | 8  |
| RESERVED |    |    |    |    |                       |    |    |
| NONE     |    |    |    |    |                       |    |    |
| 0h       |    |    |    |    |                       |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                     | 1  | 0  |
| RESERVED |    |    |    |    | R5SS0_COREB_HALT_HALT |    |    |
| NONE     |    |    |    |    | R/W                   |    |    |
| 0h       |    |    |    |    | 7h                    |    |    |

**Table 2-11. MSS\_CTRL\_R5SS0\_CORE1\_HALT Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                                     |
|------|-----------------------|------|-------|---------------------------------------------------------------------------------|
| 31:3 | RESERVED              | NONE | 0h    | Reserved                                                                        |
| 2:0  | R5SS0_COREB_HALT_HALT | R/W  | 7h    | Writing 3'b000 will unhalt for CR5B. This register should be written only once. |

### 2.2.2.4 MSS\_CTRL\_R5SS0\_STATUS\_REG Register

#### 1 MSS\_CTRL\_R5SS0\_STATUS\_REG Register (Offset = 2Ch) [reset = 0h]

This register shows whether R5SS0 is in Lock step or Dual core mode.

Return to [Summary Table](#)

**Table 2-12. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 002Ch       |

**Figure 2-4. MSS\_CTRL\_R5SS0\_STATUS\_REG Name Register**

|          |    |    |    |    |    |    |                                    |
|----------|----|----|----|----|----|----|------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                                 |
| RESERVED |    |    |    |    |    |    |                                    |
| NONE     |    |    |    |    |    |    |                                    |
| 0h       |    |    |    |    |    |    |                                    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                                 |
| RESERVED |    |    |    |    |    |    |                                    |
| NONE     |    |    |    |    |    |    |                                    |
| 0h       |    |    |    |    |    |    |                                    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                                  |
| RESERVED |    |    |    |    |    |    | R5SS0_STATU<br>S_REG_LOCK_<br>STEP |
| NONE     |    |    |    |    |    |    | R                                  |
| 0h       |    |    |    |    |    |    | 0h                                 |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                                  |
| RESERVED |    |    |    |    |    |    | R5SS0_STATU<br>S_REG_MEMS<br>WAP   |
| NONE     |    |    |    |    |    |    | R                                  |
| 0h       |    |    |    |    |    |    | 0h                                 |

**Table 2-14. MSS\_CTRL\_R5SS0\_STATUS\_REG Register Field Descriptions**

| Bit  | Field                          | Type | Reset | Description                                                                                         |
|------|--------------------------------|------|-------|-----------------------------------------------------------------------------------------------------|
| 31:9 | RESERVED                       | NONE | 0h    | Reserved                                                                                            |
| 8    | R5SS0_STATUS_REG_L<br>OCK_STEP | R    | 0h    | Reading<br>1:confirms R5SS is in lockstep mode.<br>Reading<br>0:confirms R5SS is in Dual-core mode. |
| 7:1  | RESERVED                       | NONE | 0h    | Reserved                                                                                            |
| 0    | R5SS0_STATUS_REG_M<br>EMSWAP   | R    | 0h    | Reading<br>1:confirms ROM is Eclipsed from with RAM for R5.                                         |

### 2.2.2.5 MSS\_CTRL\_R5SS0\_CORE0\_STAT Register

#### 1 MSS\_CTRL\_R5SS0\_CORE0\_STAT Register (Offset = 30h) [reset = 0h]

This register shows the WFI WFE status of R5SS0 Core 0

Return to [Summary Table](#)

**Table 2-15. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0030h       |

**Figure 2-5. MSS\_CTRL\_R5SS0\_CORE0\_STAT Name Register**

|          |    |    |                           |          |    |    |                           |
|----------|----|----|---------------------------|----------|----|----|---------------------------|
| 31       | 30 | 29 | 28                        | 27       | 26 | 25 | 24                        |
| RESERVED |    |    |                           |          |    |    |                           |
| NONE     |    |    |                           |          |    |    |                           |
| 0h       |    |    |                           |          |    |    |                           |
| 23       | 22 | 21 | 20                        | 19       | 18 | 17 | 16                        |
| RESERVED |    |    |                           |          |    |    |                           |
| NONE     |    |    |                           |          |    |    |                           |
| 0h       |    |    |                           |          |    |    |                           |
| 15       | 14 | 13 | 12                        | 11       | 10 | 9  | 8                         |
| RESERVED |    |    |                           |          |    |    |                           |
| NONE     |    |    |                           |          |    |    |                           |
| 0h       |    |    |                           |          |    |    |                           |
| 7        | 6  | 5  | 4                         | 3        | 2  | 1  | 0                         |
| RESERVED |    |    | R5SS0_CORE0_STAT_WFE_STAT | RESERVED |    |    | R5SS0_CORE0_STAT_WFI_STAT |
| NONE     |    |    | R                         | NONE     |    |    | R                         |
| 0h       |    |    | 0h                        | 0h       |    |    | 0h                        |

**Table 2-17. MSS\_CTRL\_R5SS0\_CORE0\_STAT Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description |
|------|---------------------------|------|-------|-------------|
| 31:5 | RESERVED                  | NONE | 0h    | Reserved    |
| 4    | R5SS0_CORE0_STAT_WFE_STAT | R    | 0h    | WFE Status  |
| 3:1  | RESERVED                  | NONE | 0h    | Reserved    |
| 0    | R5SS0_CORE0_STAT_WFI_STAT | R    | 0h    | WFI Status  |

### 2.2.2.6 MSS\_CTRL\_R5SS0\_CORE1\_STAT Register

#### 1 MSS\_CTRL\_R5SS0\_CORE1\_STAT Register (Offset = 34h) [reset = 0h]

This register shows the WFI WFE status of R5SS0 Core 1

Return to [Summary Table](#)

**Table 2-18. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0034h       |

**Figure 2-6. MSS\_CTRL\_R5SS0\_CORE1\_STAT Name Register**

|          |    |    |                           |          |    |    |                           |
|----------|----|----|---------------------------|----------|----|----|---------------------------|
| 31       | 30 | 29 | 28                        | 27       | 26 | 25 | 24                        |
| RESERVED |    |    |                           |          |    |    |                           |
| NONE     |    |    |                           |          |    |    |                           |
| 0h       |    |    |                           |          |    |    |                           |
| 23       | 22 | 21 | 20                        | 19       | 18 | 17 | 16                        |
| RESERVED |    |    |                           |          |    |    |                           |
| NONE     |    |    |                           |          |    |    |                           |
| 0h       |    |    |                           |          |    |    |                           |
| 15       | 14 | 13 | 12                        | 11       | 10 | 9  | 8                         |
| RESERVED |    |    |                           |          |    |    |                           |
| NONE     |    |    |                           |          |    |    |                           |
| 0h       |    |    |                           |          |    |    |                           |
| 7        | 6  | 5  | 4                         | 3        | 2  | 1  | 0                         |
| RESERVED |    |    | R5SS0_CORE1_STAT_WFE_STAT | RESERVED |    |    | R5SS0_CORE1_STAT_WFI_STAT |
| NONE     |    |    | R                         | NONE     |    |    | R                         |
| 0h       |    |    | 0h                        | 0h       |    |    | 0h                        |

**Table 2-20. MSS\_CTRL\_R5SS0\_CORE1\_STAT Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description |
|------|---------------------------|------|-------|-------------|
| 31:5 | RESERVED                  | NONE | 0h    | Reserved    |
| 4    | R5SS0_CORE1_STAT_WFE_STAT | R    | 0h    | WFE Status  |
| 3:1  | RESERVED                  | NONE | 0h    | Reserved    |
| 0    | R5SS0_CORE1_STAT_WFI_STAT | R    | 0h    | WFI Status  |

### 2.2.2.7 MSS\_CTRL\_MSS\_STC\_CONTROL0 Register

#### 1 MSS\_CTRL\_MSS\_STC\_CONTROL0 Register (Offset = 38h) [reset = 0h]

This register is used to override and force WFI from R5SS0 to RCM.

Return to [Summary Table](#)

**Table 2-21. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0038h       |

**Figure 2-7. MSS\_CTRL\_MSS\_STC\_CONTROL0 Name Register**

|          |    |    |    |    |                                   |    |    |
|----------|----|----|----|----|-----------------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                                | 25 | 24 |
| RESERVED |    |    |    |    |                                   |    |    |
| NONE     |    |    |    |    |                                   |    |    |
| 0h       |    |    |    |    |                                   |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                                | 17 | 16 |
| RESERVED |    |    |    |    |                                   |    |    |
| NONE     |    |    |    |    |                                   |    |    |
| 0h       |    |    |    |    |                                   |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                                | 9  | 8  |
| RESERVED |    |    |    |    |                                   |    |    |
| NONE     |    |    |    |    |                                   |    |    |
| 0h       |    |    |    |    |                                   |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                                 | 1  | 0  |
| RESERVED |    |    |    |    | MSS_STC_CONTROL0_CR5_WFI_OVERRIDE |    |    |
| NONE     |    |    |    |    | R/W                               |    |    |
| 0h       |    |    |    |    | 0h                                |    |    |

**Table 2-23. MSS\_CTRL\_MSS\_STC\_CONTROL0 Register Field Descriptions**

| Bit  | Field                             | Type | Reset | Description                                            |
|------|-----------------------------------|------|-------|--------------------------------------------------------|
| 31:3 | RESERVED                          | NONE | 0h    | Reserved                                               |
| 2:0  | MSS_STC_CONTROL0_CR5_WFI_OVERRIDE | R/W  | 0h    | Writing 3'b111 will force the wfi signals of R5SS to 1 |

### 2.2.2.8 MSS\_CTRL\_R5SS1\_CONTROL Register

#### 1 MSS\_CTRL\_R5SS1\_CONTROL Register (Offset = 40h) [reset = 707h]

This register is used to configure corresponding R5SS in Lock step or Dual core mode. The mode change can be affected only once in a SOC power cycle.

Return to [Summary Table](#)

**Table 2-24. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0040h       |

**Figure 2-8. MSS\_CTRL\_R5SS1\_CONTROL Name Register**

|          |    |    |    |                                     |    |    |    |
|----------|----|----|----|-------------------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                                  | 26 | 25 | 24 |
| RESERVED |    |    |    |                                     |    |    |    |
| NONE     |    |    |    |                                     |    |    |    |
| 0h       |    |    |    |                                     |    |    |    |
| 23       | 22 | 21 | 20 | 19                                  | 18 | 17 | 16 |
| RESERVED |    |    |    | R5SS1_CONTROL_RESET_FSM_TRIGGER     |    |    |    |
| NONE     |    |    |    | R/W                                 |    |    |    |
| 0h       |    |    |    | 0h                                  |    |    |    |
| 15       | 14 | 13 | 12 | 11                                  | 10 | 9  | 8  |
| RESERVED |    |    |    | R5SS1_CONTROL_LOCK_STEP_SWITCH_WAIT |    |    |    |
| NONE     |    |    |    | R/W                                 |    |    |    |
| 0h       |    |    |    | 7h                                  |    |    |    |
| 7        | 6  | 5  | 4  | 3                                   | 2  | 1  | 0  |
| RESERVED |    |    |    | R5SS1_CONTROL_LOCK_STEP             |    |    |    |
| NONE     |    |    |    | R/W                                 |    |    |    |
| 0h       |    |    |    | 7h                                  |    |    |    |

**Table 2-26. MSS\_CTRL\_R5SS1\_CONTROL Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                                                                                                                                                                                      |
|-------|-------------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:19 | RESERVED                            | NONE | 0h    | Reserved                                                                                                                                                                                                                         |
| 18:16 | R5SS1_CONTROL_RESET_FSM_TRIGGER     | R/W  | 0h    | Write pulse bit field:<br>Writing 3'b111 will trigger the reset FSM.<br>Reset FSM ensures reset to R5SS and in turn ensures the latching of lock_step and also mem_swap bit                                                      |
| 15:11 | RESERVED                            | NONE | 0h    | Reserved                                                                                                                                                                                                                         |
| 10:8  | R5SS1_CONTROL_LOCK_STEP_SWITCH_WAIT | R/W  | 7h    | Writing 3'b111 ensures switch happens only after R5SS reset. Or else it will be a immediate switch.                                                                                                                              |
| 7:3   | RESERVED                            | NONE | 0h    | Reserved                                                                                                                                                                                                                         |
| 2:0   | R5SS1_CONTROL_LOCK_STEP             | R/W  | 7h    | Writing 3'b000 ensures R5 to be in Dual-Core mode.<br>Note: The change happens after the R5SS reset assertion if corresponding R5SS_CONTROL_LOCK_STEP_SWITCH_WAIT is set. Or else the switching to Dual-core happens on the fly. |

### 2.2.2.9 MSS\_CTRL\_R5SS1\_CORE0\_HALT Register

#### 1 MSS\_CTRL\_R5SS1\_CORE0\_HALT Register (Offset = 44h) [reset = 7h]

This register is used to Halt or Unhalt R5SS1 Core 0

Return to [Summary Table](#)

**Table 2-27. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0044h       |

**Figure 2-9. MSS\_CTRL\_R5SS1\_CORE0\_HALT Name Register**

|          |    |    |    |    |                       |    |    |
|----------|----|----|----|----|-----------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                    | 25 | 24 |
| RESERVED |    |    |    |    |                       |    |    |
| NONE     |    |    |    |    |                       |    |    |
| 0h       |    |    |    |    |                       |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                    | 17 | 16 |
| RESERVED |    |    |    |    |                       |    |    |
| NONE     |    |    |    |    |                       |    |    |
| 0h       |    |    |    |    |                       |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                    | 9  | 8  |
| RESERVED |    |    |    |    |                       |    |    |
| NONE     |    |    |    |    |                       |    |    |
| 0h       |    |    |    |    |                       |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                     | 1  | 0  |
| RESERVED |    |    |    |    | R5SS1_COREA_HALT_HALT |    |    |
| NONE     |    |    |    |    | R/W                   |    |    |
| 0h       |    |    |    |    | 7h                    |    |    |

**Table 2-29. MSS\_CTRL\_R5SS1\_CORE0\_HALT Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                                 |
|------|-----------------------|------|-------|-----------------------------------------------------------------------------|
| 31:3 | RESERVED              | NONE | 0h    | Reserved                                                                    |
| 2:0  | R5SS1_COREA_HALT_HALT | R/W  | 7h    | Writing 3'b000 will unhalt CR5A. This register should be written only once. |

### 2.2.2.10 MSS\_CTRL\_R5SS1\_CORE1\_HALT Register

#### 1 MSS\_CTRL\_R5SS1\_CORE1\_HALT Register (Offset = 48h) [reset = 7h]

This register is used to Halt or Unhalt R5SS1 Core 1

Return to [Summary Table](#)

**Table 2-30. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0048h       |

**Figure 2-10. MSS\_CTRL\_R5SS1\_CORE1\_HALT Name Register**

|          |    |    |    |    |                       |    |    |
|----------|----|----|----|----|-----------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                    | 25 | 24 |
| RESERVED |    |    |    |    |                       |    |    |
| NONE     |    |    |    |    |                       |    |    |
| 0h       |    |    |    |    |                       |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                    | 17 | 16 |
| RESERVED |    |    |    |    |                       |    |    |
| NONE     |    |    |    |    |                       |    |    |
| 0h       |    |    |    |    |                       |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                    | 9  | 8  |
| RESERVED |    |    |    |    |                       |    |    |
| NONE     |    |    |    |    |                       |    |    |
| 0h       |    |    |    |    |                       |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                     | 1  | 0  |
| RESERVED |    |    |    |    | R5SS1_COREB_HALT_HALT |    |    |
| NONE     |    |    |    |    | R/W                   |    |    |
| 0h       |    |    |    |    | 7h                    |    |    |

**Table 2-32. MSS\_CTRL\_R5SS1\_CORE1\_HALT Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                                     |
|------|-----------------------|------|-------|---------------------------------------------------------------------------------|
| 31:3 | RESERVED              | NONE | 0h    | Reserved                                                                        |
| 2:0  | R5SS1_COREB_HALT_HALT | R/W  | 7h    | Writing 3'b000 will unhalt for CR5B. This register should be written only once. |



### 2.2.2.11 MSS\_CTRL\_R5SS1\_STATUS\_REG Register

#### 1 MSS\_CTRL\_R5SS1\_STATUS\_REG Register (Offset = 4Ch) [reset = 0h]

This register shows whether R5SS1 is in Lock step or Dual core mode.

Return to [Summary Table](#)

**Table 2-33. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 004Ch       |

**Figure 2-11. MSS\_CTRL\_R5SS1\_STATUS\_REG Name Register**

|          |    |    |    |    |    |    |                                    |
|----------|----|----|----|----|----|----|------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                                 |
| RESERVED |    |    |    |    |    |    |                                    |
| NONE     |    |    |    |    |    |    |                                    |
| 0h       |    |    |    |    |    |    |                                    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                                 |
| RESERVED |    |    |    |    |    |    |                                    |
| NONE     |    |    |    |    |    |    |                                    |
| 0h       |    |    |    |    |    |    |                                    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                                  |
| RESERVED |    |    |    |    |    |    | R5SS1_STATU<br>S_REG_LOCK_<br>STEP |
| NONE     |    |    |    |    |    |    | R                                  |
| 0h       |    |    |    |    |    |    | 0h                                 |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                                  |
| RESERVED |    |    |    |    |    |    |                                    |
| NONE     |    |    |    |    |    |    |                                    |
| 0h       |    |    |    |    |    |    |                                    |

**Table 2-35. MSS\_CTRL\_R5SS1\_STATUS\_REG Register Field Descriptions**

| Bit  | Field                          | Type | Reset | Description                                                                                         |
|------|--------------------------------|------|-------|-----------------------------------------------------------------------------------------------------|
| 31:9 | RESERVED                       | NONE | 0h    | Reserved                                                                                            |
| 8    | R5SS1_STATUS_REG_L<br>OCK_STEP | R    | 0h    | Reading<br>1:confirms R5SS is in lockstep mode.<br>Reading<br>0:confirms R5SS is in Dual-core mode. |
| 7:0  | RESERVED                       | NONE | 0h    | Reserved                                                                                            |

### 2.2.2.12 MSS\_CTRL\_R5SS1\_CORE0\_STAT Register

#### 1 MSS\_CTRL\_R5SS1\_CORE0\_STAT Register (Offset = 50h) [reset = 0h]

This register shows the WFI WFE status of R5SS1 Core 0

Return to [Summary Table](#)

**Table 2-36. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0050h       |

**Figure 2-12. MSS\_CTRL\_R5SS1\_CORE0\_STAT Name Register**

|          |    |    |                           |          |    |    |                           |
|----------|----|----|---------------------------|----------|----|----|---------------------------|
| 31       | 30 | 29 | 28                        | 27       | 26 | 25 | 24                        |
| RESERVED |    |    |                           |          |    |    |                           |
| NONE     |    |    |                           |          |    |    |                           |
| 0h       |    |    |                           |          |    |    |                           |
| 23       | 22 | 21 | 20                        | 19       | 18 | 17 | 16                        |
| RESERVED |    |    |                           |          |    |    |                           |
| NONE     |    |    |                           |          |    |    |                           |
| 0h       |    |    |                           |          |    |    |                           |
| 15       | 14 | 13 | 12                        | 11       | 10 | 9  | 8                         |
| RESERVED |    |    |                           |          |    |    |                           |
| NONE     |    |    |                           |          |    |    |                           |
| 0h       |    |    |                           |          |    |    |                           |
| 7        | 6  | 5  | 4                         | 3        | 2  | 1  | 0                         |
| RESERVED |    |    | R5SS1_CORE0_STAT_WFE_STAT | RESERVED |    |    | R5SS1_CORE0_STAT_WFI_STAT |
| NONE     |    |    | R                         | NONE     |    |    | R                         |
| 0h       |    |    | 0h                        | 0h       |    |    | 0h                        |

**Table 2-38. MSS\_CTRL\_R5SS1\_CORE0\_STAT Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description |
|------|---------------------------|------|-------|-------------|
| 31:5 | RESERVED                  | NONE | 0h    | Reserved    |
| 4    | R5SS1_CORE0_STAT_WFE_STAT | R    | 0h    | WFE Status  |
| 3:1  | RESERVED                  | NONE | 0h    | Reserved    |
| 0    | R5SS1_CORE0_STAT_WFI_STAT | R    | 0h    | WFI Status  |

### 2.2.2.13 MSS\_CTRL\_R5SS1\_CORE1\_STAT Register

#### 1 MSS\_CTRL\_R5SS1\_CORE1\_STAT Register (Offset = 54h) [reset = 0h]

This register shows the WFI WFE status of R5SS1 Core 1

Return to [Summary Table](#)

**Table 2-39. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0054h       |

**Figure 2-13. MSS\_CTRL\_R5SS1\_CORE1\_STAT Name Register**

|          |    |    |                           |          |    |    |                           |
|----------|----|----|---------------------------|----------|----|----|---------------------------|
| 31       | 30 | 29 | 28                        | 27       | 26 | 25 | 24                        |
| RESERVED |    |    |                           |          |    |    |                           |
| NONE     |    |    |                           |          |    |    |                           |
| 0h       |    |    |                           |          |    |    |                           |
| 23       | 22 | 21 | 20                        | 19       | 18 | 17 | 16                        |
| RESERVED |    |    |                           |          |    |    |                           |
| NONE     |    |    |                           |          |    |    |                           |
| 0h       |    |    |                           |          |    |    |                           |
| 15       | 14 | 13 | 12                        | 11       | 10 | 9  | 8                         |
| RESERVED |    |    |                           |          |    |    |                           |
| NONE     |    |    |                           |          |    |    |                           |
| 0h       |    |    |                           |          |    |    |                           |
| 7        | 6  | 5  | 4                         | 3        | 2  | 1  | 0                         |
| RESERVED |    |    | R5SS1_CORE1_STAT_WFE_STAT | RESERVED |    |    | R5SS1_CORE1_STAT_WFI_STAT |
| NONE     |    |    | R                         | NONE     |    |    | R                         |
| 0h       |    |    | 0h                        | 0h       |    |    | 0h                        |

**Table 2-41. MSS\_CTRL\_R5SS1\_CORE1\_STAT Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description |
|------|---------------------------|------|-------|-------------|
| 31:5 | RESERVED                  | NONE | 0h    | Reserved    |
| 4    | R5SS1_CORE1_STAT_WFE_STAT | R    | 0h    | WFE Status  |
| 3:1  | RESERVED                  | NONE | 0h    | Reserved    |
| 0    | R5SS1_CORE1_STAT_WFI_STAT | R    | 0h    | WFI Status  |

### 2.2.2.14 MSS\_CTRL\_MSS\_STC\_CONTROL1 Register

#### 1 MSS\_CTRL\_MSS\_STC\_CONTROL1 Register (Offset = 58h) [reset = 0h]

This register is used to override and force WFI from R5SS1 to RCM.

Return to [Summary Table](#)

**Table 2-42. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0058h       |

**Figure 2-14. MSS\_CTRL\_MSS\_STC\_CONTROL1 Name Register**

|          |    |    |    |    |                                   |    |    |
|----------|----|----|----|----|-----------------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                                | 25 | 24 |
| RESERVED |    |    |    |    |                                   |    |    |
| NONE     |    |    |    |    |                                   |    |    |
| 0h       |    |    |    |    |                                   |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                                | 17 | 16 |
| RESERVED |    |    |    |    |                                   |    |    |
| NONE     |    |    |    |    |                                   |    |    |
| 0h       |    |    |    |    |                                   |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                                | 9  | 8  |
| RESERVED |    |    |    |    |                                   |    |    |
| NONE     |    |    |    |    |                                   |    |    |
| 0h       |    |    |    |    |                                   |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                                 | 1  | 0  |
| RESERVED |    |    |    |    | MSS_STC_CONTROL1_CR5_WFI_OVERRIDE |    |    |
| NONE     |    |    |    |    | R/W                               |    |    |
| 0h       |    |    |    |    | 0h                                |    |    |

**Table 2-44. MSS\_CTRL\_MSS\_STC\_CONTROL1 Register Field Descriptions**

| Bit  | Field                             | Type | Reset | Description                                            |
|------|-----------------------------------|------|-------|--------------------------------------------------------|
| 31:3 | RESERVED                          | NONE | 0h    | Reserved                                               |
| 2:0  | MSS_STC_CONTROL1_CR5_WFI_OVERRIDE | R/W  | 0h    | Writing 3'b111 will force the wfi signals of R5SS to 1 |

### 2.2.2.15 MSS\_CTRL\_R5SS0\_ROM\_ECLIPSE Register

#### 1 MSS\_CTRL\_R5SS0\_ROM\_ECLIPSE Register (Offset = 80h) [reset = 700h]

R5\_ROM\_ECLIPSE.

Return to [Summary Table](#)
**Table 2-45. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0080h       |

**Figure 2-15. MSS\_CTRL\_R5SS0\_ROM\_ECLIPSE Name Register**

|          |    |    |    |    |                                |    |    |
|----------|----|----|----|----|--------------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                             | 25 | 24 |
| RESERVED |    |    |    |    |                                |    |    |
| NONE     |    |    |    |    |                                |    |    |
| 0h       |    |    |    |    |                                |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                             | 17 | 16 |
| RESERVED |    |    |    |    |                                |    |    |
| NONE     |    |    |    |    |                                |    |    |
| 0h       |    |    |    |    |                                |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                             | 9  | 8  |
| RESERVED |    |    |    |    | R5SS0_ROM_ECLIPSE_MEMSWAP_WAIT |    |    |
| NONE     |    |    |    |    | R/W                            |    |    |
| 0h       |    |    |    |    | 7h                             |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                              | 1  | 0  |
| RESERVED |    |    |    |    | R5SS0_ROM_ECLIPSE_MEMSWAP      |    |    |
| NONE     |    |    |    |    | R/W                            |    |    |
| 0h       |    |    |    |    | 0h                             |    |    |

**Table 2-47. MSS\_CTRL\_R5SS0\_ROM\_ECLIPSE Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                                                                                                  |
|-------|--------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:11 | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                     |
| 10:8  | R5SS0_ROM_ECLIPSE_MEMSWAP_WAIT | R/W  | 7h    | Writing 3'b111 ensures ROM-Eclipsing happens only after R5SS reset. Or else it will be a immediate change.                                                   |
| 7:3   | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                     |
| 2:0   | R5SS0_ROM_ECLIPSE_MEMSWAP      | R/W  | 0h    | Writing 3'b111 ensures eclipsing of CR5A_ROM immediately if memswap_wait is not set. If memswap_wait is set then ROM is eclipsed after R5SS reset assertion. |

### 2.2.2.16 MSS\_CTRL\_MSS\_BOOT\_INFO\_REG0 Register

#### 1 MSS\_CTRL\_MSS\_BOOT\_INFO\_REG0 Register (Offset = 100h) [reset = 0h]

MSS\_BOOT\_INFO\_REG0.

Return to [Summary Table](#)

**Table 2-48. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0100h       |

**Figure 2-16. MSS\_CTRL\_MSS\_BOOT\_INFO\_REG0 Name Register**

|                           |    |    |    |    |    |    |    |
|---------------------------|----|----|----|----|----|----|----|
| 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_BOOT_INFO_REG0_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 23                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_BOOT_INFO_REG0_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 15                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_BOOT_INFO_REG0_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 7                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_BOOT_INFO_REG0_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |

**Table 2-50. MSS\_CTRL\_MSS\_BOOT\_INFO\_REG0 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                       |
|------|---------------------------|------|-------|-----------------------------------------------------------------------------------|
| 31:0 | MSS_BOOT_INFO_REG0_CONFIG | R/W  | 0h    | Reserved Register for Software use<br>**Note: Bit is getting reseted only on PORz |

### 2.2.2.17 MSS\_CTRL\_MSS\_BOOT\_INFO\_REG1 Register

#### 1 MSS\_CTRL\_MSS\_BOOT\_INFO\_REG1 Register (Offset = 104h) [reset = 0h]

MSS\_BOOT\_INFO\_REG1.

Return to [Summary Table](#)

**Table 2-51. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0104h       |

**Figure 2-17. MSS\_CTRL\_MSS\_BOOT\_INFO\_REG1 Name Register**

|                           |    |    |    |    |    |    |    |
|---------------------------|----|----|----|----|----|----|----|
| 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_BOOT_INFO_REG1_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 23                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_BOOT_INFO_REG1_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 15                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_BOOT_INFO_REG1_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 7                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_BOOT_INFO_REG1_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |

**Table 2-53. MSS\_CTRL\_MSS\_BOOT\_INFO\_REG1 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                       |
|------|---------------------------|------|-------|-----------------------------------------------------------------------------------|
| 31:0 | MSS_BOOT_INFO_REG1_CONFIG | R/W  | 0h    | Reserved Register for Software use<br>**Note: Bit is getting reseted only on PORz |

### 2.2.2.18 MSS\_CTRL\_MSS\_BOOT\_INFO\_REG2 Register

#### 1 MSS\_CTRL\_MSS\_BOOT\_INFO\_REG2 Register (Offset = 108h) [reset = 0h]

MSS\_BOOT\_INFO\_REG2.

Return to [Summary Table](#)

**Table 2-54. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0108h       |

**Figure 2-18. MSS\_CTRL\_MSS\_BOOT\_INFO\_REG2 Name Register**

|                           |    |    |    |    |    |    |    |
|---------------------------|----|----|----|----|----|----|----|
| 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_BOOT_INFO_REG2_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 23                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_BOOT_INFO_REG2_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 15                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_BOOT_INFO_REG2_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 7                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_BOOT_INFO_REG2_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |

**Table 2-56. MSS\_CTRL\_MSS\_BOOT\_INFO\_REG2 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                       |
|------|---------------------------|------|-------|-----------------------------------------------------------------------------------|
| 31:0 | MSS_BOOT_INFO_REG2_CONFIG | R/W  | 0h    | Reserved Register for Software use<br>**Note: Bit is getting reseted only on PORz |



### 2.2.2.19 MSS\_CTRL\_MSS\_BOOT\_INFO\_REG3 Register

#### 1 MSS\_CTRL\_MSS\_BOOT\_INFO\_REG3 Register (Offset = 10Ch) [reset = 0h]

MSS\_BOOT\_INFO\_REG3.

Return to [Summary Table](#)

**Table 2-57. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 010Ch       |

**Figure 2-19. MSS\_CTRL\_MSS\_BOOT\_INFO\_REG3 Name Register**

|                           |    |    |    |    |    |    |    |
|---------------------------|----|----|----|----|----|----|----|
| 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_BOOT_INFO_REG3_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 23                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_BOOT_INFO_REG3_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 15                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_BOOT_INFO_REG3_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 7                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_BOOT_INFO_REG3_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |

**Table 2-59. MSS\_CTRL\_MSS\_BOOT\_INFO\_REG3 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                       |
|------|---------------------------|------|-------|-----------------------------------------------------------------------------------|
| 31:0 | MSS_BOOT_INFO_REG3_CONFIG | R/W  | 0h    | Reserved Register for Software use<br>**Note: Bit is getting reseted only on PORz |

### 2.2.2.20 MSS\_CTRL\_MSS\_BOOT\_INFO\_REG4 Register

#### 1 MSS\_CTRL\_MSS\_BOOT\_INFO\_REG4 Register (Offset = 110h) [reset = 0h]

MSS\_BOOT\_INFO\_REG4.

Return to [Summary Table](#)

**Table 2-60. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0110h       |

**Figure 2-20. MSS\_CTRL\_MSS\_BOOT\_INFO\_REG4 Name Register**

|                           |    |    |    |    |    |    |    |
|---------------------------|----|----|----|----|----|----|----|
| 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_BOOT_INFO_REG4_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 23                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_BOOT_INFO_REG4_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 15                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_BOOT_INFO_REG4_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 7                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_BOOT_INFO_REG4_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |

**Table 2-62. MSS\_CTRL\_MSS\_BOOT\_INFO\_REG4 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                       |
|------|---------------------------|------|-------|-----------------------------------------------------------------------------------|
| 31:0 | MSS_BOOT_INFO_REG4_CONFIG | R/W  | 0h    | Reserved Register for Software use<br>**Note: Bit is getting reseted only on PORz |

### 2.2.2.21 MSS\_CTRL\_MSS\_BOOT\_INFO\_REG5 Register

#### 1 MSS\_CTRL\_MSS\_BOOT\_INFO\_REG5 Register (Offset = 114h) [reset = 0h]

MSS\_BOOT\_INFO\_REG5.

Return to [Summary Table](#)

**Table 2-63. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0114h       |

**Figure 2-21. MSS\_CTRL\_MSS\_BOOT\_INFO\_REG5 Name Register**

|                           |    |    |    |    |    |    |    |
|---------------------------|----|----|----|----|----|----|----|
| 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_BOOT_INFO_REG5_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 23                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_BOOT_INFO_REG5_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 15                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_BOOT_INFO_REG5_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 7                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_BOOT_INFO_REG5_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |

**Table 2-65. MSS\_CTRL\_MSS\_BOOT\_INFO\_REG5 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                       |
|------|---------------------------|------|-------|-----------------------------------------------------------------------------------|
| 31:0 | MSS_BOOT_INFO_REG5_CONFIG | R/W  | 0h    | Reserved Register for Software use<br>**Note: Bit is getting reseted only on PORz |

### 2.2.2.22 MSS\_CTRL\_MSS\_BOOT\_INFO\_REG6 Register

#### 1 MSS\_CTRL\_MSS\_BOOT\_INFO\_REG6 Register (Offset = 118h) [reset = 0h]

MSS\_BOOT\_INFO\_REG6.

Return to [Summary Table](#)

**Table 2-66. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0118h       |

**Figure 2-22. MSS\_CTRL\_MSS\_BOOT\_INFO\_REG6 Name Register**

|                           |    |    |    |    |    |    |    |
|---------------------------|----|----|----|----|----|----|----|
| 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_BOOT_INFO_REG6_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 23                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_BOOT_INFO_REG6_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 15                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_BOOT_INFO_REG6_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 7                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_BOOT_INFO_REG6_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |

**Table 2-68. MSS\_CTRL\_MSS\_BOOT\_INFO\_REG6 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                       |
|------|---------------------------|------|-------|-----------------------------------------------------------------------------------|
| 31:0 | MSS_BOOT_INFO_REG6_CONFIG | R/W  | 0h    | Reserved Register for Software use<br>**Note: Bit is getting reseted only on PORz |

### 2.2.2.23 MSS\_CTRL\_MSS\_BOOT\_INFO\_REG7 Register

#### 1 MSS\_CTRL\_MSS\_BOOT\_INFO\_REG7 Register (Offset = 11Ch) [reset = 0h]

MSS\_BOOT\_INFO\_REG7.

Return to [Summary Table](#)

**Table 2-69. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 011Ch       |

**Figure 2-23. MSS\_CTRL\_MSS\_BOOT\_INFO\_REG7 Name Register**

|                           |    |    |    |    |    |    |    |
|---------------------------|----|----|----|----|----|----|----|
| 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_BOOT_INFO_REG7_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 23                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_BOOT_INFO_REG7_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 15                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_BOOT_INFO_REG7_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 7                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_BOOT_INFO_REG7_CONFIG |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |

**Table 2-71. MSS\_CTRL\_MSS\_BOOT\_INFO\_REG7 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                       |
|------|---------------------------|------|-------|-----------------------------------------------------------------------------------|
| 31:0 | MSS_BOOT_INFO_REG7_CONFIG | R/W  | 0h    | Reserved Register for Software use<br>**Note: Bit is getting reseted only on PORz |

### 2.2.2.24 MSS\_CTRL\_MSS\_ATCM0\_MEM\_INIT Register

#### 1 MSS\_CTRL\_MSS\_ATCM0\_MEM\_INIT Register (Offset = 200h) [reset = 0h]

This register is used to initialise the data and ECC of ATCM memory of R5SS0 .

Return to [Summary Table](#)

**Table 2-72. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0200h       |

**Figure 2-24. MSS\_CTRL\_MSS\_ATCM0\_MEM\_INIT Name Register**

|          |    |    |    |    |    |    |                                 |
|----------|----|----|----|----|----|----|---------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                              |
| RESERVED |    |    |    |    |    |    |                                 |
| NONE     |    |    |    |    |    |    |                                 |
| 0h       |    |    |    |    |    |    |                                 |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                              |
| RESERVED |    |    |    |    |    |    |                                 |
| NONE     |    |    |    |    |    |    |                                 |
| 0h       |    |    |    |    |    |    |                                 |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                               |
| RESERVED |    |    |    |    |    |    |                                 |
| NONE     |    |    |    |    |    |    |                                 |
| 0h       |    |    |    |    |    |    |                                 |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                               |
| RESERVED |    |    |    |    |    |    | MSS_ATCM0_MEM_INIT_ME<br>M_INIT |
| NONE     |    |    |    |    |    |    | R/W                             |
| 0h       |    |    |    |    |    |    | 0h                              |

**Table 2-74. MSS\_CTRL\_MSS\_ATCM0\_MEM\_INIT Register Field Descriptions**

| Bit  | Field                           | Type | Reset | Description                                                                                                                                    |
|------|---------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                       |
| 0    | MSS_ATCM0_MEM_INIT<br>_MEM_INIT | R/W  | 0h    | Write_pulse bit field:<br>Writing 1'b1 will start initializing the ATCM banks of CR5A/B. Value in<br>each row is initialized to 0x0C_0000_0000 |

### 2.2.2.25 MSS\_CTRL\_MSS\_ATCM0\_MEM\_INIT\_DONE Register

#### 1 MSS\_CTRL\_MSS\_ATCM0\_MEM\_INIT\_DONE Register (Offset = 204h) [reset = 0h]

This register is used to indicate the ATCM memory initialization completion for R5SS0.

Return to [Summary Table](#)

**Table 2-75. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0204h       |

**Figure 2-25. MSS\_CTRL\_MSS\_ATCM0\_MEM\_INIT\_DONE Name Register**

|          |    |    |    |    |    |    |                                       |
|----------|----|----|----|----|----|----|---------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                                    |
| RESERVED |    |    |    |    |    |    |                                       |
| NONE     |    |    |    |    |    |    |                                       |
| 0h       |    |    |    |    |    |    |                                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                                    |
| RESERVED |    |    |    |    |    |    |                                       |
| NONE     |    |    |    |    |    |    |                                       |
| 0h       |    |    |    |    |    |    |                                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                                     |
| RESERVED |    |    |    |    |    |    |                                       |
| NONE     |    |    |    |    |    |    |                                       |
| 0h       |    |    |    |    |    |    |                                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                                     |
| RESERVED |    |    |    |    |    |    | MSS_ATCM0_MEM_INIT_DONE_MEM_INIT_DONE |
| NONE     |    |    |    |    |    |    | R/W                                   |
| 0h       |    |    |    |    |    |    | 0h                                    |

**Table 2-77. MSS\_CTRL\_MSS\_ATCM0\_MEM\_INIT\_DONE Register Field Descriptions**

| Bit  | Field                                 | Type | Reset | Description                                                                                             |
|------|---------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED                              | NONE | 0h    | Reserved                                                                                                |
| 0    | MSS_ATCM0_MEM_INIT_DONE_MEM_INIT_DONE | R/W  | 0h    | This field will be high once initialization of ATCM banks is finished. Writing '1' would clear the bit. |

### 2.2.2.26 MSS\_CTRL\_MSS\_ATCM0\_MEM\_INIT\_STATUS Register

#### 1 MSS\_CTRL\_MSS\_ATCM0\_MEM\_INIT\_STATUS Register (Offset = 208h) [reset = 0h]

This register is used to indicate the status of ongoing memory initialization for ATCM memory of R5SS0.

Return to [Summary Table](#)

**Table 2-78. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0208h       |

**Figure 2-26. MSS\_CTRL\_MSS\_ATCM0\_MEM\_INIT\_STATUS Name Register**

|          |    |    |    |    |    |    |                                      |
|----------|----|----|----|----|----|----|--------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                                   |
| RESERVED |    |    |    |    |    |    |                                      |
| NONE     |    |    |    |    |    |    |                                      |
| 0h       |    |    |    |    |    |    |                                      |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                                   |
| RESERVED |    |    |    |    |    |    |                                      |
| NONE     |    |    |    |    |    |    |                                      |
| 0h       |    |    |    |    |    |    |                                      |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                                    |
| RESERVED |    |    |    |    |    |    |                                      |
| NONE     |    |    |    |    |    |    |                                      |
| 0h       |    |    |    |    |    |    |                                      |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                                    |
| RESERVED |    |    |    |    |    |    | MSS_ATCM0_MEM_INIT_STATUS_MEM_STATUS |
| NONE     |    |    |    |    |    |    | R                                    |
| 0h       |    |    |    |    |    |    | 0h                                   |

**Table 2-80. MSS\_CTRL\_MSS\_ATCM0\_MEM\_INIT\_STATUS Register Field Descriptions**

| Bit  | Field                                | Type | Reset | Description                                                                                                                   |
|------|--------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                      |
| 0    | MSS_ATCM0_MEM_INIT_STATUS_MEM_STATUS | R    | 0h    | 1'b0: No initialization is happening for ATCM banks of CR5A/B<br>1'b1: Initialization is in progress for ATCM banks of CR5A/B |



### 2.2.2.27 MSS\_CTRL\_MSS\_BTCM0\_MEM\_INIT Register

#### 1 MSS\_CTRL\_MSS\_BTCM0\_MEM\_INIT Register (Offset = 210h) [reset = 0h]

This register is used to initialise the data and ECC of BTCM memory of R5SS0 .

Return to [Summary Table](#)

**Table 2-81. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0210h       |

**Figure 2-27. MSS\_CTRL\_MSS\_BTCM0\_MEM\_INIT Name Register**

|          |    |    |    |    |    |    |                             |
|----------|----|----|----|----|----|----|-----------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                          |
| RESERVED |    |    |    |    |    |    |                             |
| NONE     |    |    |    |    |    |    |                             |
| 0h       |    |    |    |    |    |    |                             |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                          |
| RESERVED |    |    |    |    |    |    |                             |
| NONE     |    |    |    |    |    |    |                             |
| 0h       |    |    |    |    |    |    |                             |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                           |
| RESERVED |    |    |    |    |    |    |                             |
| NONE     |    |    |    |    |    |    |                             |
| 0h       |    |    |    |    |    |    |                             |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                           |
| RESERVED |    |    |    |    |    |    | MSS_BTCM0_MEM_INIT_MEM_INIT |
| NONE     |    |    |    |    |    |    | R/W                         |
| 0h       |    |    |    |    |    |    | 0h                          |

**Table 2-83. MSS\_CTRL\_MSS\_BTCM0\_MEM\_INIT Register Field Descriptions**

| Bit  | Field                       | Type | Reset | Description                                                                                |
|------|-----------------------------|------|-------|--------------------------------------------------------------------------------------------|
| 31:1 | RESERVED                    | NONE | 0h    | Reserved                                                                                   |
| 0    | MSS_BTCM0_MEM_INIT_MEM_INIT | R/W  | 0h    | Write_pulse bit field:<br>Writing 1'b1 will start initializing the B0/1TCM banks of CR5A/B |

### 2.2.2.28 MSS\_CTRL\_MSS\_BTCM0\_MEM\_INIT\_DONE Register

#### 1 MSS\_CTRL\_MSS\_BTCM0\_MEM\_INIT\_DONE Register (Offset = 214h) [reset = 0h]

This register is used to indicate the BTCM memory initialization completion for R5SS0.

Return to [Summary Table](#)

**Table 2-84. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0214h       |

**Figure 2-28. MSS\_CTRL\_MSS\_BTCM0\_MEM\_INIT\_DONE Name Register**

|          |    |    |    |    |    |    |                                       |
|----------|----|----|----|----|----|----|---------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                                    |
| RESERVED |    |    |    |    |    |    |                                       |
| NONE     |    |    |    |    |    |    |                                       |
| 0h       |    |    |    |    |    |    |                                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                                    |
| RESERVED |    |    |    |    |    |    |                                       |
| NONE     |    |    |    |    |    |    |                                       |
| 0h       |    |    |    |    |    |    |                                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                                     |
| RESERVED |    |    |    |    |    |    |                                       |
| NONE     |    |    |    |    |    |    |                                       |
| 0h       |    |    |    |    |    |    |                                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                                     |
| RESERVED |    |    |    |    |    |    | MSS_BTCM0_MEM_INIT_DONE_MEM_INIT_DONE |
| NONE     |    |    |    |    |    |    | R/W                                   |
| 0h       |    |    |    |    |    |    | 0h                                    |

**Table 2-86. MSS\_CTRL\_MSS\_BTCM0\_MEM\_INIT\_DONE Register Field Descriptions**

| Bit  | Field                                 | Type | Reset | Description                                                                                                |
|------|---------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED                              | NONE | 0h    | Reserved                                                                                                   |
| 0    | MSS_BTCM0_MEM_INIT_DONE_MEM_INIT_DONE | R/W  | 0h    | This field will be high once initialization of B0/1TCM banks is finished. Writing '1' would clear the bit. |

### 2.2.2.29 MSS\_CTRL\_MSS\_BTCM0\_MEM\_INIT\_STATUS Register

#### 1 MSS\_CTRL\_MSS\_BTCM0\_MEM\_INIT\_STATUS Register (Offset = 218h) [reset = 0h]

This register is used to indicate the status of ongoing memory initialization for BTCM memory of R5SS0.

Return to [Summary Table](#)

**Table 2-87. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0218h       |

**Figure 2-29. MSS\_CTRL\_MSS\_BTCM0\_MEM\_INIT\_STATUS Name Register**

|          |    |    |    |    |    |    |                                      |
|----------|----|----|----|----|----|----|--------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                                   |
| RESERVED |    |    |    |    |    |    |                                      |
| NONE     |    |    |    |    |    |    |                                      |
| 0h       |    |    |    |    |    |    |                                      |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                                   |
| RESERVED |    |    |    |    |    |    |                                      |
| NONE     |    |    |    |    |    |    |                                      |
| 0h       |    |    |    |    |    |    |                                      |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                                    |
| RESERVED |    |    |    |    |    |    |                                      |
| NONE     |    |    |    |    |    |    |                                      |
| 0h       |    |    |    |    |    |    |                                      |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                                    |
| RESERVED |    |    |    |    |    |    | MSS_BTCM0_MEM_INIT_STATUS_MEM_STATUS |
| NONE     |    |    |    |    |    |    | R                                    |
| 0h       |    |    |    |    |    |    | 0h                                   |

**Table 2-89. MSS\_CTRL\_MSS\_BTCM0\_MEM\_INIT\_STATUS Register Field Descriptions**

| Bit  | Field                                | Type | Reset | Description                                                                                                                         |
|------|--------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                            |
| 0    | MSS_BTCM0_MEM_INIT_STATUS_MEM_STATUS | R    | 0h    | 1'b0: No initialization is happening for B0/1TCM banks of CR5A/B<br>1'b1: Initialization is in progress for B0/1TCM banks of CR5A/B |

### 2.2.2.30 MSS\_CTRL\_MSS\_ATCM1\_MEM\_INIT Register

#### 1 MSS\_CTRL\_MSS\_ATCM1\_MEM\_INIT Register (Offset = 220h) [reset = 0h]

This register is used to initialise the data and ECC of ATCM memory of R5SS1.

Return to [Summary Table](#)

**Table 2-90. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0220h       |

**Figure 2-30. MSS\_CTRL\_MSS\_ATCM1\_MEM\_INIT Name Register**

|          |    |    |    |    |    |    |                                 |
|----------|----|----|----|----|----|----|---------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                              |
| RESERVED |    |    |    |    |    |    |                                 |
| NONE     |    |    |    |    |    |    |                                 |
| 0h       |    |    |    |    |    |    |                                 |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                              |
| RESERVED |    |    |    |    |    |    |                                 |
| NONE     |    |    |    |    |    |    |                                 |
| 0h       |    |    |    |    |    |    |                                 |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                               |
| RESERVED |    |    |    |    |    |    |                                 |
| NONE     |    |    |    |    |    |    |                                 |
| 0h       |    |    |    |    |    |    |                                 |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                               |
| RESERVED |    |    |    |    |    |    | MSS_ATCM1_MEM_INIT_ME<br>M_INIT |
| NONE     |    |    |    |    |    |    | R/W                             |
| 0h       |    |    |    |    |    |    | 0h                              |

**Table 2-92. MSS\_CTRL\_MSS\_ATCM1\_MEM\_INIT Register Field Descriptions**

| Bit  | Field                           | Type | Reset | Description                                                                                                                                    |
|------|---------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                       |
| 0    | MSS_ATCM1_MEM_INIT<br>_MEM_INIT | R/W  | 0h    | Write_pulse bit field:<br>Writing 1'b1 will start initializing the ATCM banks of CR5A/B. Value in<br>each row is initialized to 0x0C_0000_0000 |

### 2.2.2.31 MSS\_CTRL\_MSS\_ATCM1\_MEM\_INIT\_DONE Register

#### 1 MSS\_CTRL\_MSS\_ATCM1\_MEM\_INIT\_DONE Register (Offset = 224h) [reset = 0h]

This register is used to indicate the ATCM memory initialization completion for R5SS1.

Return to [Summary Table](#)

**Table 2-93. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0224h       |

**Figure 2-31. MSS\_CTRL\_MSS\_ATCM1\_MEM\_INIT\_DONE Name Register**

|          |    |    |    |    |    |    |                                       |
|----------|----|----|----|----|----|----|---------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                                    |
| RESERVED |    |    |    |    |    |    |                                       |
| NONE     |    |    |    |    |    |    |                                       |
| 0h       |    |    |    |    |    |    |                                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                                    |
| RESERVED |    |    |    |    |    |    |                                       |
| NONE     |    |    |    |    |    |    |                                       |
| 0h       |    |    |    |    |    |    |                                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                                     |
| RESERVED |    |    |    |    |    |    |                                       |
| NONE     |    |    |    |    |    |    |                                       |
| 0h       |    |    |    |    |    |    |                                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                                     |
| RESERVED |    |    |    |    |    |    | MSS_ATCM1_MEM_INIT_DONE_MEM_INIT_DONE |
| NONE     |    |    |    |    |    |    | R/W                                   |
| 0h       |    |    |    |    |    |    | 0h                                    |

**Table 2-95. MSS\_CTRL\_MSS\_ATCM1\_MEM\_INIT\_DONE Register Field Descriptions**

| Bit  | Field                                 | Type | Reset | Description                                                                                             |
|------|---------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED                              | NONE | 0h    | Reserved                                                                                                |
| 0    | MSS_ATCM1_MEM_INIT_DONE_MEM_INIT_DONE | R/W  | 0h    | This field will be high once initialization of ATCM banks is finished. Writing '1' would clear the bit. |

### 2.2.2.32 MSS\_CTRL\_MSS\_ATCM1\_MEM\_INIT\_STATUS Register

#### 1 MSS\_CTRL\_MSS\_ATCM1\_MEM\_INIT\_STATUS Register (Offset = 228h) [reset = 0h]

This register is used to indicate the status of ongoing memory initialization for ATCM memory of R5SS1.

Return to [Summary Table](#)

**Table 2-96. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0228h       |

**Figure 2-32. MSS\_CTRL\_MSS\_ATCM1\_MEM\_INIT\_STATUS Name Register**

|          |    |    |    |    |    |    |                                                  |
|----------|----|----|----|----|----|----|--------------------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                                               |
| RESERVED |    |    |    |    |    |    |                                                  |
| NONE     |    |    |    |    |    |    |                                                  |
| 0h       |    |    |    |    |    |    |                                                  |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                                               |
| RESERVED |    |    |    |    |    |    |                                                  |
| NONE     |    |    |    |    |    |    |                                                  |
| 0h       |    |    |    |    |    |    |                                                  |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                                                |
| RESERVED |    |    |    |    |    |    |                                                  |
| NONE     |    |    |    |    |    |    |                                                  |
| 0h       |    |    |    |    |    |    |                                                  |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                                                |
| RESERVED |    |    |    |    |    |    | MSS_ATCM1_<br>MEM_INIT_STA<br>TUS_MEM_ST<br>ATUS |
| NONE     |    |    |    |    |    |    | R                                                |
| 0h       |    |    |    |    |    |    | 0h                                               |

**Table 2-98. MSS\_CTRL\_MSS\_ATCM1\_MEM\_INIT\_STATUS Register Field Descriptions**

| Bit  | Field                                | Type | Reset | Description                                                                                                                   |
|------|--------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                      |
| 0    | MSS_ATCM1_MEM_INIT_STATUS_MEM_STATUS | R    | 0h    | 1'b0: No initialization is happening for ATCM banks of CR5A/B<br>1'b1: Initialization is in progress for ATCM banks of CR5A/B |

### 2.2.2.33 MSS\_CTRL\_MSS\_BTCM1\_MEM\_INIT Register

#### 1 MSS\_CTRL\_MSS\_BTCM1\_MEM\_INIT Register (Offset = 230h) [reset = 0h]

This register is used to initialise the data and ECC of BTCM memory of R5SS1.

Return to [Summary Table](#)

**Table 2-99. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0230h       |

**Figure 2-33. MSS\_CTRL\_MSS\_BTCM1\_MEM\_INIT Name Register**

|          |    |    |    |    |    |    |                             |
|----------|----|----|----|----|----|----|-----------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                          |
| RESERVED |    |    |    |    |    |    |                             |
| NONE     |    |    |    |    |    |    |                             |
| 0h       |    |    |    |    |    |    |                             |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                          |
| RESERVED |    |    |    |    |    |    |                             |
| NONE     |    |    |    |    |    |    |                             |
| 0h       |    |    |    |    |    |    |                             |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                           |
| RESERVED |    |    |    |    |    |    |                             |
| NONE     |    |    |    |    |    |    |                             |
| 0h       |    |    |    |    |    |    |                             |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                           |
| RESERVED |    |    |    |    |    |    | MSS_BTCM1_MEM_INIT_MEM_INIT |
| NONE     |    |    |    |    |    |    | R/W                         |
| 0h       |    |    |    |    |    |    | 0h                          |

**Table 2-101. MSS\_CTRL\_MSS\_BTCM1\_MEM\_INIT Register Field Descriptions**

| Bit  | Field                       | Type | Reset | Description                                                                                |
|------|-----------------------------|------|-------|--------------------------------------------------------------------------------------------|
| 31:1 | RESERVED                    | NONE | 0h    | Reserved                                                                                   |
| 0    | MSS_BTCM1_MEM_INIT_MEM_INIT | R/W  | 0h    | Write_pulse bit field:<br>Writing 1'b1 will start initializing the B0/1TCM banks of CR5A/B |

### 2.2.2.34 MSS\_CTRL\_MSS\_BTCM1\_MEM\_INIT\_DONE Register

#### 1 MSS\_CTRL\_MSS\_BTCM1\_MEM\_INIT\_DONE Register (Offset = 234h) [reset = 0h]

This register is used to indicate the BTCM memory initialization completion for R5SS1.

Return to [Summary Table](#)

**Table 2-102. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0234h       |

**Figure 2-34. MSS\_CTRL\_MSS\_BTCM1\_MEM\_INIT\_DONE Name Register**

|          |    |    |    |    |    |    |                                       |
|----------|----|----|----|----|----|----|---------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                                    |
| RESERVED |    |    |    |    |    |    |                                       |
| NONE     |    |    |    |    |    |    |                                       |
| 0h       |    |    |    |    |    |    |                                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                                    |
| RESERVED |    |    |    |    |    |    |                                       |
| NONE     |    |    |    |    |    |    |                                       |
| 0h       |    |    |    |    |    |    |                                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                                     |
| RESERVED |    |    |    |    |    |    |                                       |
| NONE     |    |    |    |    |    |    |                                       |
| 0h       |    |    |    |    |    |    |                                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                                     |
| RESERVED |    |    |    |    |    |    | MSS_BTCM1_MEM_INIT_DONE_MEM_INIT_DONE |
| NONE     |    |    |    |    |    |    | R/W                                   |
| 0h       |    |    |    |    |    |    | 0h                                    |

**Table 2-104. MSS\_CTRL\_MSS\_BTCM1\_MEM\_INIT\_DONE Register Field Descriptions**

| Bit  | Field                                 | Type | Reset | Description                                                                                                |
|------|---------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED                              | NONE | 0h    | Reserved                                                                                                   |
| 0    | MSS_BTCM1_MEM_INIT_DONE_MEM_INIT_DONE | R/W  | 0h    | This field will be high once initialization of B0/1TCM banks is finished. Writing '1' would clear the bit. |



### 2.2.2.35 MSS\_CTRL\_MSS\_BTCM1\_MEM\_INIT\_STATUS Register

#### 1 MSS\_CTRL\_MSS\_BTCM1\_MEM\_INIT\_STATUS Register (Offset = 238h) [reset = 0h]

This register is used to indicate the status of ongoing memory initialization for BTCM memory of R5SS1.

Return to [Summary Table](#)

**Table 2-105. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0238h       |

**Figure 2-35. MSS\_CTRL\_MSS\_BTCM1\_MEM\_INIT\_STATUS Name Register**

|          |    |    |    |    |    |    |                                                  |
|----------|----|----|----|----|----|----|--------------------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                                               |
| RESERVED |    |    |    |    |    |    |                                                  |
| NONE     |    |    |    |    |    |    |                                                  |
| 0h       |    |    |    |    |    |    |                                                  |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                                               |
| RESERVED |    |    |    |    |    |    |                                                  |
| NONE     |    |    |    |    |    |    |                                                  |
| 0h       |    |    |    |    |    |    |                                                  |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                                                |
| RESERVED |    |    |    |    |    |    |                                                  |
| NONE     |    |    |    |    |    |    |                                                  |
| 0h       |    |    |    |    |    |    |                                                  |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                                                |
| RESERVED |    |    |    |    |    |    | MSS_BTCM1_<br>MEM_INIT_STA<br>TUS_MEM_ST<br>ATUS |
| NONE     |    |    |    |    |    |    | R                                                |
| 0h       |    |    |    |    |    |    | 0h                                               |

**Table 2-107. MSS\_CTRL\_MSS\_BTCM1\_MEM\_INIT\_STATUS Register Field Descriptions**

| Bit  | Field                                | Type | Reset | Description                                                                                                                         |
|------|--------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                            |
| 0    | MSS_BTCM1_MEM_INIT_STATUS_MEM_STATUS | R    | 0h    | 1'b0: No initialization is happening for B0/1TCM banks of CR5A/B<br>1'b1: Initialization is in progress for B0/1TCM banks of CR5A/B |

### 2.2.2.36 MSS\_CTRL\_MSS\_L2\_MEM\_INIT Register

#### 1 MSS\_CTRL\_MSS\_L2\_MEM\_INIT Register (Offset = 240h) [reset = 0h]

This register is used to initialise the data and ECC of L2OCRAM.

Return to [Summary Table](#)

**Table 2-108. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0240h       |

**Figure 2-36. MSS\_CTRL\_MSS\_L2\_MEM\_INIT Name Register**

|          |    |    |    |                           |                           |                           |                           |
|----------|----|----|----|---------------------------|---------------------------|---------------------------|---------------------------|
| 31       | 30 | 29 | 28 | 27                        | 26                        | 25                        | 24                        |
| RESERVED |    |    |    |                           |                           |                           |                           |
| NONE     |    |    |    |                           |                           |                           |                           |
| 0h       |    |    |    |                           |                           |                           |                           |
| 23       | 22 | 21 | 20 | 19                        | 18                        | 17                        | 16                        |
| RESERVED |    |    |    |                           |                           |                           |                           |
| NONE     |    |    |    |                           |                           |                           |                           |
| 0h       |    |    |    |                           |                           |                           |                           |
| 15       | 14 | 13 | 12 | 11                        | 10                        | 9                         | 8                         |
| RESERVED |    |    |    |                           |                           |                           |                           |
| NONE     |    |    |    |                           |                           |                           |                           |
| 0h       |    |    |    |                           |                           |                           |                           |
| 7        | 6  | 5  | 4  | 3                         | 2                         | 1                         | 0                         |
| RESERVED |    |    |    | MSS_L2_MEM_INIT_PARTITON3 | MSS_L2_MEM_INIT_PARTITON2 | MSS_L2_MEM_INIT_PARTITON1 | MSS_L2_MEM_INIT_PARTITON0 |
| NONE     |    |    |    | R/W                       | R/W                       | R/W                       | R/W                       |
| 0h       |    |    |    | 0h                        | 0h                        | 0h                        | 0h                        |

**Table 2-110. MSS\_CTRL\_MSS\_L2\_MEM\_INIT Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                          |
|------|---------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                  | NONE | 0h    | Reserved                                                                                                             |
| 3    | MSS_L2_MEM_INIT_PARTITON3 | R/W  | 0h    | Write_pulse bit field:<br>Writing 1'b1 will start initializing the L2 Bank3. Value in each row is initialized to 0x0 |
| 2    | MSS_L2_MEM_INIT_PARTITON2 | R/W  | 0h    | Write_pulse bit field:<br>Writing 1'b1 will start initializing the L2 Bank2. Value in each row is initialized to 0x0 |
| 1    | MSS_L2_MEM_INIT_PARTITON1 | R/W  | 0h    | Write_pulse bit field:<br>Writing 1'b1 will start initializing the L2 Bank1. Value in each row is initialized to 0x0 |
| 0    | MSS_L2_MEM_INIT_PARTITON0 | R/W  | 0h    | Write_pulse bit field:<br>Writing 1'b1 will start initializing the L2 Bank0. Value in each row is initialized to 0x0 |

### 2.2.2.37 MSS\_CTRL\_MSS\_L2\_MEM\_INIT\_DONE Register

#### 1 MSS\_CTRL\_MSS\_L2\_MEM\_INIT\_DONE Register (Offset = 244h) [reset = 0h]

This register is used to indicate the L2OCRAM memory initialization completion .

Return to [Summary Table](#)

**Table 2-111. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0244h       |

**Figure 2-37. MSS\_CTRL\_MSS\_L2\_MEM\_INIT\_DONE Name Register**

|          |    |    |    |                                 |                                 |                                 |                                 |
|----------|----|----|----|---------------------------------|---------------------------------|---------------------------------|---------------------------------|
| 31       | 30 | 29 | 28 | 27                              | 26                              | 25                              | 24                              |
| RESERVED |    |    |    |                                 |                                 |                                 |                                 |
| NONE     |    |    |    |                                 |                                 |                                 |                                 |
| 0h       |    |    |    |                                 |                                 |                                 |                                 |
| 23       | 22 | 21 | 20 | 19                              | 18                              | 17                              | 16                              |
| RESERVED |    |    |    |                                 |                                 |                                 |                                 |
| NONE     |    |    |    |                                 |                                 |                                 |                                 |
| 0h       |    |    |    |                                 |                                 |                                 |                                 |
| 15       | 14 | 13 | 12 | 11                              | 10                              | 9                               | 8                               |
| RESERVED |    |    |    |                                 |                                 |                                 |                                 |
| NONE     |    |    |    |                                 |                                 |                                 |                                 |
| 0h       |    |    |    |                                 |                                 |                                 |                                 |
| 7        | 6  | 5  | 4  | 3                               | 2                               | 1                               | 0                               |
| RESERVED |    |    |    | MSS_L2_MEM_INIT_DONE_PARTITION3 | MSS_L2_MEM_INIT_DONE_PARTITION2 | MSS_L2_MEM_INIT_DONE_PARTITION1 | MSS_L2_MEM_INIT_DONE_PARTITION0 |
| NONE     |    |    |    | R/W                             | R/W                             | R/W                             | R/W                             |
| 0h       |    |    |    | 0h                              | 0h                              | 0h                              | 0h                              |

**Table 2-113. MSS\_CTRL\_MSS\_L2\_MEM\_INIT\_DONE Register Field Descriptions**

| Bit  | Field                           | Type | Reset | Description                                                                                          |
|------|---------------------------------|------|-------|------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                        | NONE | 0h    | Reserved                                                                                             |
| 3    | MSS_L2_MEM_INIT_DONE_PARTITION3 | R/W  | 0h    | This field will be high once initialization of L2 bank3 is finished. Writing '1' would clear the bit |
| 2    | MSS_L2_MEM_INIT_DONE_PARTITION2 | R/W  | 0h    | This field will be high once initialization of L2 bank2 is finished. Writing '1' would clear the bit |
| 1    | MSS_L2_MEM_INIT_DONE_PARTITION1 | R/W  | 0h    | This field will be high once initialization of L2 bank1 is finished. Writing '1' would clear the bit |
| 0    | MSS_L2_MEM_INIT_DONE_PARTITION0 | R/W  | 0h    | This field will be high once initialization of L2 bank0 is finished. Writing '1' would clear the bit |

### 2.2.2.38 MSS\_CTRL\_MSS\_L2\_MEM\_INIT\_STATUS Register

#### 1 MSS\_CTRL\_MSS\_L2\_MEM\_INIT\_STATUS Register (Offset = 248h) [reset = 0h]

This register is used to indicate the status of ongoing memory initialization for L2OCRAM.

Return to [Summary Table](#)

**Table 2-114. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0248h       |

**Figure 2-38. MSS\_CTRL\_MSS\_L2\_MEM\_INIT\_STATUS Name Register**

|          |    |    |    |                                   |                                   |                                   |                                   |
|----------|----|----|----|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|
| 31       | 30 | 29 | 28 | 27                                | 26                                | 25                                | 24                                |
| RESERVED |    |    |    |                                   |                                   |                                   |                                   |
| NONE     |    |    |    |                                   |                                   |                                   |                                   |
| 0h       |    |    |    |                                   |                                   |                                   |                                   |
| 23       | 22 | 21 | 20 | 19                                | 18                                | 17                                | 16                                |
| RESERVED |    |    |    |                                   |                                   |                                   |                                   |
| NONE     |    |    |    |                                   |                                   |                                   |                                   |
| 0h       |    |    |    |                                   |                                   |                                   |                                   |
| 15       | 14 | 13 | 12 | 11                                | 10                                | 9                                 | 8                                 |
| RESERVED |    |    |    |                                   |                                   |                                   |                                   |
| NONE     |    |    |    |                                   |                                   |                                   |                                   |
| 0h       |    |    |    |                                   |                                   |                                   |                                   |
| 7        | 6  | 5  | 4  | 3                                 | 2                                 | 1                                 | 0                                 |
| RESERVED |    |    |    | MSS_L2_MEM_INIT_STATUS_PARTITION3 | MSS_L2_MEM_INIT_STATUS_PARTITION2 | MSS_L2_MEM_INIT_STATUS_PARTITION1 | MSS_L2_MEM_INIT_STATUS_PARTITION0 |
| NONE     |    |    |    | R                                 | R                                 | R                                 | R                                 |
| 0h       |    |    |    | 0h                                | 0h                                | 0h                                | 0h                                |

**Table 2-116. MSS\_CTRL\_MSS\_L2\_MEM\_INIT\_STATUS Register Field Descriptions**

| Bit  | Field                             | Type | Reset | Description                                                                                           |
|------|-----------------------------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                          | NONE | 0h    | Reserved                                                                                              |
| 3    | MSS_L2_MEM_INIT_STATUS_PARTITION3 | R    | 0h    | 1'b0: No initialization is happening for L2 bank3<br>1'b1: Initialization is in progress for L2 bank3 |
| 2    | MSS_L2_MEM_INIT_STATUS_PARTITION2 | R    | 0h    | 1'b0: No initialization is happening for L2 bank2<br>1'b1: Initialization is in progress for L2 bank2 |
| 1    | MSS_L2_MEM_INIT_STATUS_PARTITION1 | R    | 0h    | 1'b0: No initialization is happening for L2 bank1<br>1'b1: Initialization is in progress for L2 bank1 |
| 0    | MSS_L2_MEM_INIT_STATUS_PARTITION0 | R    | 0h    | 1'b0: No initialization is happening for L2 bank0<br>1'b1: Initialization is in progress for L2 bank0 |

### 2.2.2.39 MSS\_CTRL\_MSS\_MAILBOX\_MEM\_INIT Register

#### 1 MSS\_CTRL\_MSS\_MAILBOX\_MEM\_INIT Register (Offset = 250h) [reset = 0h]

This register is used to initialise the data and ECC of MBOX\_SRAM.

Return to [Summary Table](#)

**Table 2-117. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0250h       |

**Figure 2-39. MSS\_CTRL\_MSS\_MAILBOX\_MEM\_INIT Name Register**

|          |    |    |    |    |    |    |                                        |
|----------|----|----|----|----|----|----|----------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                                     |
| RESERVED |    |    |    |    |    |    |                                        |
| NONE     |    |    |    |    |    |    |                                        |
| 0h       |    |    |    |    |    |    |                                        |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                                     |
| RESERVED |    |    |    |    |    |    |                                        |
| NONE     |    |    |    |    |    |    |                                        |
| 0h       |    |    |    |    |    |    |                                        |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                                      |
| RESERVED |    |    |    |    |    |    |                                        |
| NONE     |    |    |    |    |    |    |                                        |
| 0h       |    |    |    |    |    |    |                                        |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                                      |
| RESERVED |    |    |    |    |    |    | MSS_MAILBOX<br>_MEM_INIT_M<br>EM0_INIT |
| NONE     |    |    |    |    |    |    | R/W                                    |
| 0h       |    |    |    |    |    |    | 0h                                     |

**Table 2-119. MSS\_CTRL\_MSS\_MAILBOX\_MEM\_INIT Register Field Descriptions**

| Bit  | Field                          | Type | Reset | Description                                                                                                          |
|------|--------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED                       | NONE | 0h    | Reserved                                                                                                             |
| 0    | MSS_MAILBOX_MEM_INIT_MEM0_INIT | R/W  | 0h    | Write_pulse bit field:<br>Writing 1'b1 will start initializing the MSS_MBOX. Value in each row is initialized to 0x0 |

### 2.2.2.40 MSS\_CTRL\_MSS\_MAILBOX\_MEM\_INIT\_DONE Register

#### 1 MSS\_CTRL\_MSS\_MAILBOX\_MEM\_INIT\_DONE Register (Offset = 254h) [reset = 0h]

This register is used to indicate the MBOX\_SRAM memory initialization completion .

Return to [Summary Table](#)

**Table 2-120. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0254h       |

**Figure 2-40. MSS\_CTRL\_MSS\_MAILBOX\_MEM\_INIT\_DONE Name Register**

|          |    |    |    |    |    |    |                                                 |
|----------|----|----|----|----|----|----|-------------------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                                              |
| RESERVED |    |    |    |    |    |    |                                                 |
| NONE     |    |    |    |    |    |    |                                                 |
| 0h       |    |    |    |    |    |    |                                                 |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                                              |
| RESERVED |    |    |    |    |    |    |                                                 |
| NONE     |    |    |    |    |    |    |                                                 |
| 0h       |    |    |    |    |    |    |                                                 |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                                               |
| RESERVED |    |    |    |    |    |    |                                                 |
| NONE     |    |    |    |    |    |    |                                                 |
| 0h       |    |    |    |    |    |    |                                                 |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                                               |
| RESERVED |    |    |    |    |    |    | MSS_MAILBOX<br>_MEM_INIT_D<br>ONE_MEM0_D<br>ONE |
| NONE     |    |    |    |    |    |    | R/W                                             |
| 0h       |    |    |    |    |    |    | 0h                                              |

**Table 2-122. MSS\_CTRL\_MSS\_MAILBOX\_MEM\_INIT\_DONE Register Field Descriptions**

| Bit  | Field                               | Type | Reset | Description                                                                                          |
|------|-------------------------------------|------|-------|------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED                            | NONE | 0h    | Reserved                                                                                             |
| 0    | MSS_MAILBOX_MEM_INIT_DONE_MEM0_DONE | R/W  | 0h    | This field will be high once initialization of MSS_MBOX is finished. Writing '1' would clear the bit |

### 2.2.2.41 MSS\_CTRL\_MSS\_MAILBOX\_MEM\_INIT\_STATUS Register

#### 1 MSS\_CTRL\_MSS\_MAILBOX\_MEM\_INIT\_STATUS Register (Offset = 258h) [reset = 0h]

This register is used to indicate the status of ongoing memory initialization for MBOX\_SRAM.

Return to [Summary Table](#)

**Table 2-123. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0258h       |

**Figure 2-41. MSS\_CTRL\_MSS\_MAILBOX\_MEM\_INIT\_STATUS Name Register**

|          |    |    |    |    |    |    |                                                     |
|----------|----|----|----|----|----|----|-----------------------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                                                  |
| RESERVED |    |    |    |    |    |    |                                                     |
| NONE     |    |    |    |    |    |    |                                                     |
| 0h       |    |    |    |    |    |    |                                                     |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                                                  |
| RESERVED |    |    |    |    |    |    |                                                     |
| NONE     |    |    |    |    |    |    |                                                     |
| 0h       |    |    |    |    |    |    |                                                     |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                                                   |
| RESERVED |    |    |    |    |    |    |                                                     |
| NONE     |    |    |    |    |    |    |                                                     |
| 0h       |    |    |    |    |    |    |                                                     |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                                                   |
| RESERVED |    |    |    |    |    |    | MSS_MAILBOX<br>_MEM_INIT_ST<br>ATUS_MEM0_<br>STATUS |
| NONE     |    |    |    |    |    |    | R                                                   |
| 0h       |    |    |    |    |    |    | 0h                                                  |

**Table 2-125. MSS\_CTRL\_MSS\_MAILBOX\_MEM\_INIT\_STATUS Register Field Descriptions**

| Bit  | Field                                   | Type | Reset | Description                                                                                           |
|------|-----------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED                                | NONE | 0h    | Reserved                                                                                              |
| 0    | MSS_MAILBOX_MEM_INIT_STATUS_MEM0_STATUS | R    | 0h    | 1'b0: No initialization is happening for MSS_MBOX<br>1'b1: Initialization is in progress for MSS_MBOX |

### 2.2.2.42 MSS\_CTRL\_MSS\_TPCC\_MEMINIT\_START Register

#### 1 MSS\_CTRL\_MSS\_TPCC\_MEMINIT\_START Register (Offset = 260h) [reset = 0h]

This register is used to initialise the data and ECC of EDMA\_TPCC RAM.

Return to [Summary Table](#)

**Table 2-126. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0260h       |

**Figure 2-42. MSS\_CTRL\_MSS\_TPCC\_MEMINIT\_START Name Register**

|          |    |    |    |    |    |    |                                                         |
|----------|----|----|----|----|----|----|---------------------------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                                                      |
| RESERVED |    |    |    |    |    |    |                                                         |
| NONE     |    |    |    |    |    |    |                                                         |
| 0h       |    |    |    |    |    |    |                                                         |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                                                      |
| RESERVED |    |    |    |    |    |    |                                                         |
| NONE     |    |    |    |    |    |    |                                                         |
| 0h       |    |    |    |    |    |    |                                                         |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                                                       |
| RESERVED |    |    |    |    |    |    |                                                         |
| NONE     |    |    |    |    |    |    |                                                         |
| 0h       |    |    |    |    |    |    |                                                         |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                                                       |
| RESERVED |    |    |    |    |    |    | MSS_TPCC_M<br>EMINIT_START<br>_TPCC_A_ME<br>MINIT_START |
| NONE     |    |    |    |    |    |    | R/W                                                     |
| 0h       |    |    |    |    |    |    | 0h                                                      |

**Table 2-128. MSS\_CTRL\_MSS\_TPCC\_MEMINIT\_START Register Field Descriptions**

| Bit  | Field                                               | Type | Reset | Description                                                                  |
|------|-----------------------------------------------------|------|-------|------------------------------------------------------------------------------|
| 31:1 | RESERVED                                            | NONE | 0h    | Reserved                                                                     |
| 0    | MSS_TPCC_MEMINIT_S<br>TART_TPCC_A_MEMINIT<br>_START | R/W  | 0h    | Write_pulse bit field:<br>Writing 1'b1 will start initializing the MSS_TPCCA |



### 2.2.2.43 MSS\_CTRL\_MSS\_TPCC\_MEMINIT\_DONE Register

#### 1 MSS\_CTRL\_MSS\_TPCC\_MEMINIT\_DONE Register (Offset = 264h) [reset = 0h]

This register is used to indicate the EDMA\_TPCC memory initialization completion .

Return to [Summary Table](#)

**Table 2-129. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0264h       |

**Figure 2-43. MSS\_CTRL\_MSS\_TPCC\_MEMINIT\_DONE Name Register**

|          |    |    |    |    |    |    |                                                       |
|----------|----|----|----|----|----|----|-------------------------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                                                    |
| RESERVED |    |    |    |    |    |    |                                                       |
| NONE     |    |    |    |    |    |    |                                                       |
| 0h       |    |    |    |    |    |    |                                                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                                                    |
| RESERVED |    |    |    |    |    |    |                                                       |
| NONE     |    |    |    |    |    |    |                                                       |
| 0h       |    |    |    |    |    |    |                                                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                                                     |
| RESERVED |    |    |    |    |    |    |                                                       |
| NONE     |    |    |    |    |    |    |                                                       |
| 0h       |    |    |    |    |    |    |                                                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                                                     |
| RESERVED |    |    |    |    |    |    | MSS_TPCC_M<br>EMINIT_DONE<br>_TPCC_A_ME<br>MINIT_DONE |
| NONE     |    |    |    |    |    |    | R/W                                                   |
| 0h       |    |    |    |    |    |    | 0h                                                    |

**Table 2-131. MSS\_CTRL\_MSS\_TPCC\_MEMINIT\_DONE Register Field Descriptions**

| Bit  | Field                                             | Type | Reset | Description                                                                                             |
|------|---------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED                                          | NONE | 0h    | Reserved                                                                                                |
| 0    | MSS_TPCC_MEMINIT_D<br>ONE_TPCC_A_MEMINIT<br>_DONE | R/W  | 0h    | This field will be high once intialization of MSS_TPCCA is finished.<br>Writing '1' would clear the bit |

### 2.2.2.44 MSS\_CTRL\_MSS\_TPCC\_MEMINIT\_STATUS Register

#### 1 MSS\_CTRL\_MSS\_TPCC\_MEMINIT\_STATUS Register (Offset = 268h) [reset = 0h]

This register is used to indicate the status of ongoing memory initialization for EDMA\_TPCC RAM.

Return to [Summary Table](#)

**Table 2-132. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0268h       |

**Figure 2-44. MSS\_CTRL\_MSS\_TPCC\_MEMINIT\_STATUS Name Register**

|          |    |    |    |    |    |    |                                                           |
|----------|----|----|----|----|----|----|-----------------------------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                                                        |
| RESERVED |    |    |    |    |    |    |                                                           |
| NONE     |    |    |    |    |    |    |                                                           |
| 0h       |    |    |    |    |    |    |                                                           |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                                                        |
| RESERVED |    |    |    |    |    |    |                                                           |
| NONE     |    |    |    |    |    |    |                                                           |
| 0h       |    |    |    |    |    |    |                                                           |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                                                         |
| RESERVED |    |    |    |    |    |    |                                                           |
| NONE     |    |    |    |    |    |    |                                                           |
| 0h       |    |    |    |    |    |    |                                                           |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                                                         |
| RESERVED |    |    |    |    |    |    | MSS_TPCC_M<br>EMINIT_STATU<br>S_TPCC_A_ME<br>MINIT_STATUS |
| NONE     |    |    |    |    |    |    | R                                                         |
| 0h       |    |    |    |    |    |    | 0h                                                        |

**Table 2-134. MSS\_CTRL\_MSS\_TPCC\_MEMINIT\_STATUS Register Field Descriptions**

| Bit  | Field                                                 | Type | Reset | Description                                                                                             |
|------|-------------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED                                              | NONE | 0h    | Reserved                                                                                                |
| 0    | MSS_TPCC_MEMINIT_S<br>TATUS_TPCC_A_MEMINI<br>T_STATUS | R    | 0h    | 1'b0: No initialization is happening for MSS_TPCCA<br>1'b1: Initialization is in progress for MSS_TPCCB |

### 2.2.2.45 MSS\_CTRL\_TOP\_PBIST\_KEY\_RST Register

#### 1 MSS\_CTRL\_TOP\_PBIST\_KEY\_RST Register (Offset = 300h) [reset = 0h]

This register is used to enable Top Pbist module.

Return to [Summary Table](#)

**Table 2-135. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0300h       |

**Figure 2-45. MSS\_CTRL\_TOP\_PBIST\_KEY\_RST Name Register**

|                                |    |    |    |                                |    |    |    |
|--------------------------------|----|----|----|--------------------------------|----|----|----|
| 31                             | 30 | 29 | 28 | 27                             | 26 | 25 | 24 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 23                             | 22 | 21 | 20 | 19                             | 18 | 17 | 16 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 15                             | 14 | 13 | 12 | 11                             | 10 | 9  | 8  |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 7                              | 6  | 5  | 4  | 3                              | 2  | 1  | 0  |
| MSS_PBIST_KEY_RST_PBIST_ST_RST |    |    |    | MSS_PBIST_KEY_RST_PBIST_ST_KEY |    |    |    |
| R/W                            |    |    |    | R/W                            |    |    |    |
| 0h                             |    |    |    | 0h                             |    |    |    |

**Table 2-137. MSS\_CTRL\_TOP\_PBIST\_KEY\_RST Register Field Descriptions**

| Bit  | Field                          | Type | Reset | Description                                                         |
|------|--------------------------------|------|-------|---------------------------------------------------------------------|
| 31:8 | RESERVED                       | NONE | 0h    | Reserved                                                            |
| 7:4  | MSS_PBIST_KEY_RST_PBIST_ST_RST | R/W  | 0h    | MSS PBIST controller will be brought out of reset when value is 0xA |
| 3:0  | MSS_PBIST_KEY_RST_PBIST_ST_KEY | R/W  | 0h    | Top PBIST Selftest Key. Valid value is 0x5                          |

### 2.2.2.46 MSS\_CTRL\_MSS\_R5SS0\_CTI\_TRIG\_SEL Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CTI\_TRIG\_SEL Register (Offset = 400h) [reset = 0h]

This register is used to select the two CTI trigger sources for R5SS[x]

Return to [Summary Table](#)

**Table 2-138. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0400h       |

**Figure 2-46. MSS\_CTRL\_MSS\_R5SS0\_CTI\_TRIG\_SEL Name Register**

|                              |    |    |    |    |    |    |    |
|------------------------------|----|----|----|----|----|----|----|
| 31                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                     |    |    |    |    |    |    |    |
| NONE                         |    |    |    |    |    |    |    |
| 0h                           |    |    |    |    |    |    |    |
| 23                           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                     |    |    |    |    |    |    |    |
| NONE                         |    |    |    |    |    |    |    |
| 0h                           |    |    |    |    |    |    |    |
| 15                           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_R5SS0_CTI_TRIG_SEL_TRIG1 |    |    |    |    |    |    |    |
| R/W                          |    |    |    |    |    |    |    |
| 0h                           |    |    |    |    |    |    |    |
| 7                            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_R5SS0_CTI_TRIG_SEL_TRIG0 |    |    |    |    |    |    |    |
| R/W                          |    |    |    |    |    |    |    |
| 0h                           |    |    |    |    |    |    |    |

**Table 2-140. MSS\_CTRL\_MSS\_R5SS0\_CTI\_TRIG\_SEL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                       |
|-------|------------------------------|------|-------|-------------------------------------------------------------------|
| 31:16 | RESERVED                     | NONE | 0h    | Reserved                                                          |
| 15:8  | MSS_R5SS0_CTI_TRIG_SEL_TRIG1 | R/W  | 0h    | Used for selecting the trigger source for 1st trigger of MSS_R5SS |
| 7:0   | MSS_R5SS0_CTI_TRIG_SEL_TRIG0 | R/W  | 0h    | Used for selecting the trigger source for 0th trigger of MSS_R5SS |

### 2.2.2.47 MSS\_CTRL\_MSS\_R5SS1\_CTI\_TRIG\_SEL Register

#### 1 MSS\_CTRL\_MSS\_R5SS1\_CTI\_TRIG\_SEL Register (Offset = 404h) [reset = 0h]

This register is used to select the two CTI trigger sources for R5SS[x]

Return to [Summary Table](#)

**Table 2-141. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0404h       |

**Figure 2-47. MSS\_CTRL\_MSS\_R5SS1\_CTI\_TRIG\_SEL Name Register**

|                              |    |    |    |    |    |    |    |
|------------------------------|----|----|----|----|----|----|----|
| 31                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                     |    |    |    |    |    |    |    |
| NONE                         |    |    |    |    |    |    |    |
| 0h                           |    |    |    |    |    |    |    |
| 23                           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                     |    |    |    |    |    |    |    |
| NONE                         |    |    |    |    |    |    |    |
| 0h                           |    |    |    |    |    |    |    |
| 15                           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_R5SS1_CTI_TRIG_SEL_TRIG1 |    |    |    |    |    |    |    |
| R/W                          |    |    |    |    |    |    |    |
| 0h                           |    |    |    |    |    |    |    |
| 7                            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_R5SS1_CTI_TRIG_SEL_TRIG0 |    |    |    |    |    |    |    |
| R/W                          |    |    |    |    |    |    |    |
| 0h                           |    |    |    |    |    |    |    |

**Table 2-143. MSS\_CTRL\_MSS\_R5SS1\_CTI\_TRIG\_SEL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                       |
|-------|------------------------------|------|-------|-------------------------------------------------------------------|
| 31:16 | RESERVED                     | NONE | 0h    | Reserved                                                          |
| 15:8  | MSS_R5SS1_CTI_TRIG_SEL_TRIG1 | R/W  | 0h    | Used for selecting the trigger source for 1st trigger of MSS_R5SS |
| 7:0   | MSS_R5SS1_CTI_TRIG_SEL_TRIG0 | R/W  | 0h    | Used for selecting the trigger source for 0th trigger of MSS_R5SS |

### 2.2.2.48 MSS\_CTRL\_MSS\_DBGSS\_CTI\_TRIG\_SEL Register

#### 1 MSS\_CTRL\_MSS\_DBGSS\_CTI\_TRIG\_SEL Register (Offset = 408h) [reset = 0h]

This register is used to select the four CTI trigger sources for DEBUGSS.

Return to [Summary Table](#)

**Table 2-144. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0408h       |

**Figure 2-48. MSS\_CTRL\_MSS\_DBGSS\_CTI\_TRIG\_SEL Name Register**

|                              |    |    |    |    |    |    |    |
|------------------------------|----|----|----|----|----|----|----|
| 31                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_DBGSS_CTI_TRIG_SEL_TRIG3 |    |    |    |    |    |    |    |
| R/W                          |    |    |    |    |    |    |    |
| 0h                           |    |    |    |    |    |    |    |
| 23                           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_DBGSS_CTI_TRIG_SEL_TRIG2 |    |    |    |    |    |    |    |
| R/W                          |    |    |    |    |    |    |    |
| 0h                           |    |    |    |    |    |    |    |
| 15                           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_DBGSS_CTI_TRIG_SEL_TRIG1 |    |    |    |    |    |    |    |
| R/W                          |    |    |    |    |    |    |    |
| 0h                           |    |    |    |    |    |    |    |
| 7                            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_DBGSS_CTI_TRIG_SEL_TRIG0 |    |    |    |    |    |    |    |
| R/W                          |    |    |    |    |    |    |    |
| 0h                           |    |    |    |    |    |    |    |

**Table 2-146. MSS\_CTRL\_MSS\_DBGSS\_CTI\_TRIG\_SEL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                          |
|-------|------------------------------|------|-------|----------------------------------------------------------------------|
| 31:24 | MSS_DBGSS_CTI_TRIG_SEL_TRIG3 | R/W  | 0h    | Used for selecting the trigger source for 3rd trigger of ONE_MCU_CTI |
| 23:16 | MSS_DBGSS_CTI_TRIG_SEL_TRIG2 | R/W  | 0h    | Used for selecting the trigger source for 2nd trigger of ONE_MCU_CTI |
| 15:8  | MSS_DBGSS_CTI_TRIG_SEL_TRIG1 | R/W  | 0h    | Used for selecting the trigger source for 1st trigger of ONE_MCU_CTI |
| 7:0   | MSS_DBGSS_CTI_TRIG_SEL_TRIG0 | R/W  | 0h    | Used for selecting the trigger source for 0th trigger of ONE_MCU_CTI |

### 2.2.2.49 MSS\_CTRL\_DEBUGSS\_STM\_NSGUAREN Register

#### 1 MSS\_CTRL\_DEBUGSS\_STM\_NSGUAREN Register (Offset = 410h) [reset = 0h]

This register controls the behaviour of STM for Non secure guaranteed AXI access.

Return to [Summary Table](#)

**Table 2-147. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0410h       |

**Figure 2-49. MSS\_CTRL\_DEBUGSS\_STM\_NSGUAREN Name Register**

|          |    |    |    |    |                                     |          |    |
|----------|----|----|----|----|-------------------------------------|----------|----|
| 31       | 30 | 29 | 28 | 27 | 26                                  | 25       | 24 |
| RESERVED |    |    |    |    |                                     |          |    |
| NONE     |    |    |    |    |                                     |          |    |
| 0h       |    |    |    |    |                                     |          |    |
| 23       | 22 | 21 | 20 | 19 | 18                                  | 17       | 16 |
| RESERVED |    |    |    |    |                                     |          |    |
| NONE     |    |    |    |    |                                     |          |    |
| 0h       |    |    |    |    |                                     |          |    |
| 15       | 14 | 13 | 12 | 11 | 10                                  | 9        | 8  |
| RESERVED |    |    |    |    | DEBUGSS_ST<br>M_NSGUAREN<br>_ENABLE | RESERVED |    |
| NONE     |    |    |    |    | R/W                                 | NONE     |    |
| 0h       |    |    |    |    | 0h                                  | 0h       |    |
| 7        | 6  | 5  | 4  | 3  | 2                                   | 1        | 0  |
| RESERVED |    |    |    |    |                                     |          |    |
| NONE     |    |    |    |    |                                     |          |    |
| 0h       |    |    |    |    |                                     |          |    |

**Table 2-149. MSS\_CTRL\_DEBUGSS\_STM\_NSGUAREN Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                                                                   |
|-------|---------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:11 | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                      |
| 10    | DEBUGSS_STM_NSGUA<br>REN_ENABLE | R/W  | 0h    | Non secure guaranteed access control<br>1'b0: Access does not stall the CPU. Trace not guaranteed<br>1'b1: Access may stall. Trace guaranteed |
| 9:0   | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                      |

### 2.2.2.50 MSS\_CTRL\_MCAN0\_HALTEN Register

#### 1 MSS\_CTRL\_MCAN0\_HALTEN Register (Offset = 420h) [reset = 0h]

This register selects which R5 CPU when debug halted shall halt MCAN[x] Peripheral.

Return to [Summary Table](#)

**Table 2-150. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0420h       |

**Figure 2-50. MSS\_CTRL\_MCAN0\_HALTEN Name Register**

|          |    |    |    |                              |                              |                              |                              |
|----------|----|----|----|------------------------------|------------------------------|------------------------------|------------------------------|
| 31       | 30 | 29 | 28 | 27                           | 26                           | 25                           | 24                           |
| RESERVED |    |    |    |                              |                              |                              |                              |
| NONE     |    |    |    |                              |                              |                              |                              |
| 0h       |    |    |    |                              |                              |                              |                              |
| 23       | 22 | 21 | 20 | 19                           | 18                           | 17                           | 16                           |
| RESERVED |    |    |    |                              |                              |                              |                              |
| NONE     |    |    |    |                              |                              |                              |                              |
| 0h       |    |    |    |                              |                              |                              |                              |
| 15       | 14 | 13 | 12 | 11                           | 10                           | 9                            | 8                            |
| RESERVED |    |    |    |                              |                              |                              |                              |
| NONE     |    |    |    |                              |                              |                              |                              |
| 0h       |    |    |    |                              |                              |                              |                              |
| 7        | 6  | 5  | 4  | 3                            | 2                            | 1                            | 0                            |
| RESERVED |    |    |    | CAN0_HALTEN_CR5B1_HALT<br>EN | CAN0_HALTEN_CR5A1_HALT<br>EN | CAN0_HALTEN_CR5B0_HALT<br>EN | CAN0_HALTEN_CR5A0_HALT<br>EN |
| NONE     |    |    |    | R/W                          | R/W                          | R/W                          | R/W                          |
| 0h       |    |    |    | 0h                           | 0h                           | 0h                           | 0h                           |

**Table 2-152. MSS\_CTRL\_MCAN0\_HALTEN Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                             |
|------|--------------------------|------|-------|---------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                 | NONE | 0h    | Reserved                                                                                                |
| 3    | CAN0_HALTEN_CR5B1_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | CAN0_HALTEN_CR5A1_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | CAN0_HALTEN_CR5B0_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | CAN0_HALTEN_CR5A0_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |



### 2.2.2.51 MSS\_CTRL\_MCAN1\_HALTEN Register

#### 1 MSS\_CTRL\_MCAN1\_HALTEN Register (Offset = 424h) [reset = 0h]

This register selects which R5 CPU when debug halted shall halt MCAN[x] Peripheral.

Return to [Summary Table](#)

**Table 2-153. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0424h       |

**Figure 2-51. MSS\_CTRL\_MCAN1\_HALTEN Name Register**

|          |    |    |    |                              |                              |                              |                              |
|----------|----|----|----|------------------------------|------------------------------|------------------------------|------------------------------|
| 31       | 30 | 29 | 28 | 27                           | 26                           | 25                           | 24                           |
| RESERVED |    |    |    |                              |                              |                              |                              |
| NONE     |    |    |    |                              |                              |                              |                              |
| 0h       |    |    |    |                              |                              |                              |                              |
| 23       | 22 | 21 | 20 | 19                           | 18                           | 17                           | 16                           |
| RESERVED |    |    |    |                              |                              |                              |                              |
| NONE     |    |    |    |                              |                              |                              |                              |
| 0h       |    |    |    |                              |                              |                              |                              |
| 15       | 14 | 13 | 12 | 11                           | 10                           | 9                            | 8                            |
| RESERVED |    |    |    |                              |                              |                              |                              |
| NONE     |    |    |    |                              |                              |                              |                              |
| 0h       |    |    |    |                              |                              |                              |                              |
| 7        | 6  | 5  | 4  | 3                            | 2                            | 1                            | 0                            |
| RESERVED |    |    |    | CAN1_HALTEN_CR5B1_HALT<br>EN | CAN1_HALTEN_CR5A1_HALT<br>EN | CAN1_HALTEN_CR5B0_HALT<br>EN | CAN1_HALTEN_CR5A0_HALT<br>EN |
| NONE     |    |    |    | R/W                          | R/W                          | R/W                          | R/W                          |
| 0h       |    |    |    | 0h                           | 0h                           | 0h                           | 0h                           |

**Table 2-155. MSS\_CTRL\_MCAN1\_HALTEN Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                             |
|------|--------------------------|------|-------|---------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                 | NONE | 0h    | Reserved                                                                                                |
| 3    | CAN1_HALTEN_CR5B1_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | CAN1_HALTEN_CR5A1_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | CAN1_HALTEN_CR5B0_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | CAN1_HALTEN_CR5A0_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |

### 2.2.2.52 MSS\_CTRL\_MCAN2\_HALTEN Register

#### 1 MSS\_CTRL\_MCAN2\_HALTEN Register (Offset = 428h) [reset = 0h]

This register selects which R5 CPU when debug halted shall halt MCAN[x] Peripheral.

Return to [Summary Table](#)

**Table 2-156. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0428h       |

**Figure 2-52. MSS\_CTRL\_MCAN2\_HALTEN Name Register**

|          |    |    |    |                          |                          |                          |                          |
|----------|----|----|----|--------------------------|--------------------------|--------------------------|--------------------------|
| 31       | 30 | 29 | 28 | 27                       | 26                       | 25                       | 24                       |
| RESERVED |    |    |    |                          |                          |                          |                          |
| NONE     |    |    |    |                          |                          |                          |                          |
| 0h       |    |    |    |                          |                          |                          |                          |
| 23       | 22 | 21 | 20 | 19                       | 18                       | 17                       | 16                       |
| RESERVED |    |    |    |                          |                          |                          |                          |
| NONE     |    |    |    |                          |                          |                          |                          |
| 0h       |    |    |    |                          |                          |                          |                          |
| 15       | 14 | 13 | 12 | 11                       | 10                       | 9                        | 8                        |
| RESERVED |    |    |    |                          |                          |                          |                          |
| NONE     |    |    |    |                          |                          |                          |                          |
| 0h       |    |    |    |                          |                          |                          |                          |
| 7        | 6  | 5  | 4  | 3                        | 2                        | 1                        | 0                        |
| RESERVED |    |    |    | CAN2_HALTEN_CR5B1_HALTEN | CAN2_HALTEN_CR5A1_HALTEN | CAN2_HALTEN_CR5B0_HALTEN | CAN2_HALTEN_CR5A0_HALTEN |
| NONE     |    |    |    | R/W                      | R/W                      | R/W                      | R/W                      |
| 0h       |    |    |    | 0h                       | 0h                       | 0h                       | 0h                       |

**Table 2-158. MSS\_CTRL\_MCAN2\_HALTEN Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                             |
|------|--------------------------|------|-------|---------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                 | NONE | 0h    | Reserved                                                                                                |
| 3    | CAN2_HALTEN_CR5B1_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | CAN2_HALTEN_CR5A1_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | CAN2_HALTEN_CR5B0_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | CAN2_HALTEN_CR5A0_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |

### 2.2.2.53 MSS\_CTRL\_MCAN3\_HALTEN Register

#### 1 MSS\_CTRL\_MCAN3\_HALTEN Register (Offset = 42Ch) [reset = 0h]

This register selects which R5 CPU when debug halted shall halt MCAN[x] Peripheral.

Return to [Summary Table](#)

**Table 2-159. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 042Ch       |

**Figure 2-53. MSS\_CTRL\_MCAN3\_HALTEN Name Register**

|          |    |    |    |                          |                          |                          |                          |
|----------|----|----|----|--------------------------|--------------------------|--------------------------|--------------------------|
| 31       | 30 | 29 | 28 | 27                       | 26                       | 25                       | 24                       |
| RESERVED |    |    |    |                          |                          |                          |                          |
| NONE     |    |    |    |                          |                          |                          |                          |
| 0h       |    |    |    |                          |                          |                          |                          |
| 23       | 22 | 21 | 20 | 19                       | 18                       | 17                       | 16                       |
| RESERVED |    |    |    |                          |                          |                          |                          |
| NONE     |    |    |    |                          |                          |                          |                          |
| 0h       |    |    |    |                          |                          |                          |                          |
| 15       | 14 | 13 | 12 | 11                       | 10                       | 9                        | 8                        |
| RESERVED |    |    |    |                          |                          |                          |                          |
| NONE     |    |    |    |                          |                          |                          |                          |
| 0h       |    |    |    |                          |                          |                          |                          |
| 7        | 6  | 5  | 4  | 3                        | 2                        | 1                        | 0                        |
| RESERVED |    |    |    | CAN3_HALTEN_CR5B1_HALTEN | CAN3_HALTEN_CR5A1_HALTEN | CAN3_HALTEN_CR5B0_HALTEN | CAN3_HALTEN_CR5A0_HALTEN |
| NONE     |    |    |    | R/W                      | R/W                      | R/W                      | R/W                      |
| 0h       |    |    |    | 0h                       | 0h                       | 0h                       | 0h                       |

**Table 2-161. MSS\_CTRL\_MCAN3\_HALTEN Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                             |
|------|--------------------------|------|-------|---------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                 | NONE | 0h    | Reserved                                                                                                |
| 3    | CAN3_HALTEN_CR5B1_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | CAN3_HALTEN_CR5A1_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | CAN3_HALTEN_CR5B0_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | CAN3_HALTEN_CR5A0_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |

### 2.2.2.54 MSS\_CTRL\_LIN0 HALTEN Register

#### 1 MSS\_CTRL\_LIN0 HALTEN Register (Offset = 430h) [reset = 0h]

This register selects which R5 CPU when debug halted shall halt LIN[x] Peripheral.

Return to [Summary Table](#)

**Table 2-162. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0430h       |

**Figure 2-54. MSS\_CTRL\_LIN0 HALTEN Name Register**

|          |    |    |    |                           |                           |                           |                           |
|----------|----|----|----|---------------------------|---------------------------|---------------------------|---------------------------|
| 31       | 30 | 29 | 28 | 27                        | 26                        | 25                        | 24                        |
| RESERVED |    |    |    |                           |                           |                           |                           |
| NONE     |    |    |    |                           |                           |                           |                           |
| 0h       |    |    |    |                           |                           |                           |                           |
| 23       | 22 | 21 | 20 | 19                        | 18                        | 17                        | 16                        |
| RESERVED |    |    |    |                           |                           |                           |                           |
| NONE     |    |    |    |                           |                           |                           |                           |
| 0h       |    |    |    |                           |                           |                           |                           |
| 15       | 14 | 13 | 12 | 11                        | 10                        | 9                         | 8                         |
| RESERVED |    |    |    |                           |                           |                           |                           |
| NONE     |    |    |    |                           |                           |                           |                           |
| 0h       |    |    |    |                           |                           |                           |                           |
| 7        | 6  | 5  | 4  | 3                         | 2                         | 1                         | 0                         |
| RESERVED |    |    |    | LIN0_HALTEN_CR5B1_HALTE_N | LIN0_HALTEN_CR5A1_HALTE_N | LIN0_HALTEN_CR5B0_HALTE_N | LIN0_HALTEN_CR5A0_HALTE_N |
| NONE     |    |    |    | R/W                       | R/W                       | R/W                       | R/W                       |
| 0h       |    |    |    | 0h                        | 0h                        | 0h                        | 0h                        |

**Table 2-164. MSS\_CTRL\_LIN0 HALTEN Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                             |
|------|--------------------------|------|-------|---------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                 | NONE | 0h    | Reserved                                                                                                |
| 3    | LIN0_HALTEN_CR5B1_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | LIN0_HALTEN_CR5A1_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | LIN0_HALTEN_CR5B0_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | LIN0_HALTEN_CR5A0_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |

### 2.2.2.55 MSS\_CTRL\_LIN1 HALTEN Register

#### 1 MSS\_CTRL\_LIN1\_HALTEN Register (Offset = 434h) [reset = 0h]

This register selects which R5 CPU when debug halted shall halt LIN[x] Peripheral.

Return to [Summary Table](#)

**Table 2-165. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0434h       |

**Figure 2-55. MSS\_CTRL\_LIN1\_HALTEN Name Register**

|          |    |    |    |                           |                           |                           |                           |
|----------|----|----|----|---------------------------|---------------------------|---------------------------|---------------------------|
| 31       | 30 | 29 | 28 | 27                        | 26                        | 25                        | 24                        |
| RESERVED |    |    |    |                           |                           |                           |                           |
| NONE     |    |    |    |                           |                           |                           |                           |
| 0h       |    |    |    |                           |                           |                           |                           |
| 23       | 22 | 21 | 20 | 19                        | 18                        | 17                        | 16                        |
| RESERVED |    |    |    |                           |                           |                           |                           |
| NONE     |    |    |    |                           |                           |                           |                           |
| 0h       |    |    |    |                           |                           |                           |                           |
| 15       | 14 | 13 | 12 | 11                        | 10                        | 9                         | 8                         |
| RESERVED |    |    |    |                           |                           |                           |                           |
| NONE     |    |    |    |                           |                           |                           |                           |
| 0h       |    |    |    |                           |                           |                           |                           |
| 7        | 6  | 5  | 4  | 3                         | 2                         | 1                         | 0                         |
| RESERVED |    |    |    | LIN1_HALTEN_CR5B1_HALTE_N | LIN1_HALTEN_CR5A1_HALTE_N | LIN1_HALTEN_CR5B0_HALTE_N | LIN1_HALTEN_CR5A0_HALTE_N |
| NONE     |    |    |    | R/W                       | R/W                       | R/W                       | R/W                       |
| 0h       |    |    |    | 0h                        | 0h                        | 0h                        | 0h                        |

**Table 2-167. MSS\_CTRL\_LIN1\_HALTEN Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                             |
|------|--------------------------|------|-------|---------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                 | NONE | 0h    | Reserved                                                                                                |
| 3    | LIN1_HALTEN_CR5B1_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | LIN1_HALTEN_CR5A1_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | LIN1_HALTEN_CR5B0_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | LIN1_HALTEN_CR5A0_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |

### 2.2.2.56 MSS\_CTRL\_LIN2\_HALTEN Register

#### 1 MSS\_CTRL\_LIN2\_HALTEN Register (Offset = 438h) [reset = 0h]

This register selects which R5 CPU when debug halted shall halt LIN[x] Peripheral.

Return to [Summary Table](#)

**Table 2-168. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0438h       |

**Figure 2-56. MSS\_CTRL\_LIN2\_HALTEN Name Register**

|          |    |    |    |                           |                           |                           |                           |
|----------|----|----|----|---------------------------|---------------------------|---------------------------|---------------------------|
| 31       | 30 | 29 | 28 | 27                        | 26                        | 25                        | 24                        |
| RESERVED |    |    |    |                           |                           |                           |                           |
| NONE     |    |    |    |                           |                           |                           |                           |
| 0h       |    |    |    |                           |                           |                           |                           |
| 23       | 22 | 21 | 20 | 19                        | 18                        | 17                        | 16                        |
| RESERVED |    |    |    |                           |                           |                           |                           |
| NONE     |    |    |    |                           |                           |                           |                           |
| 0h       |    |    |    |                           |                           |                           |                           |
| 15       | 14 | 13 | 12 | 11                        | 10                        | 9                         | 8                         |
| RESERVED |    |    |    |                           |                           |                           |                           |
| NONE     |    |    |    |                           |                           |                           |                           |
| 0h       |    |    |    |                           |                           |                           |                           |
| 7        | 6  | 5  | 4  | 3                         | 2                         | 1                         | 0                         |
| RESERVED |    |    |    | LIN2_HALTEN_CR5B1_HALTE_N | LIN2_HALTEN_CR5A1_HALTE_N | LIN2_HALTEN_CR5B0_HALTE_N | LIN2_HALTEN_CR5A0_HALTE_N |
| NONE     |    |    |    | R/W                       | R/W                       | R/W                       | R/W                       |
| 0h       |    |    |    | 0h                        | 0h                        | 0h                        | 0h                        |

**Table 2-170. MSS\_CTRL\_LIN2\_HALTEN Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                             |
|------|---------------------------|------|-------|---------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                  | NONE | 0h    | Reserved                                                                                                |
| 3    | LIN2_HALTEN_CR5B1_HALTE_N | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | LIN2_HALTEN_CR5A1_HALTE_N | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | LIN2_HALTEN_CR5B0_HALTE_N | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | LIN2_HALTEN_CR5A0_HALTE_N | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |

### 2.2.2.57 MSS\_CTRL\_LIN3\_HALTEN Register

#### 1 MSS\_CTRL\_LIN3\_HALTEN Register (Offset = 43Ch) [reset = 0h]

This register selects which R5 CPU when debug halted shall halt LIN[x] Peripheral.

Return to [Summary Table](#)

**Table 2-171. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 043Ch       |

**Figure 2-57. MSS\_CTRL\_LIN3\_HALTEN Name Register**

|          |    |    |    |                           |                           |                           |                           |
|----------|----|----|----|---------------------------|---------------------------|---------------------------|---------------------------|
| 31       | 30 | 29 | 28 | 27                        | 26                        | 25                        | 24                        |
| RESERVED |    |    |    |                           |                           |                           |                           |
| NONE     |    |    |    |                           |                           |                           |                           |
| 0h       |    |    |    |                           |                           |                           |                           |
| 23       | 22 | 21 | 20 | 19                        | 18                        | 17                        | 16                        |
| RESERVED |    |    |    |                           |                           |                           |                           |
| NONE     |    |    |    |                           |                           |                           |                           |
| 0h       |    |    |    |                           |                           |                           |                           |
| 15       | 14 | 13 | 12 | 11                        | 10                        | 9                         | 8                         |
| RESERVED |    |    |    |                           |                           |                           |                           |
| NONE     |    |    |    |                           |                           |                           |                           |
| 0h       |    |    |    |                           |                           |                           |                           |
| 7        | 6  | 5  | 4  | 3                         | 2                         | 1                         | 0                         |
| RESERVED |    |    |    | LIN3_HALTEN_CR5B1_HALTE_N | LIN3_HALTEN_CR5A1_HALTE_N | LIN3_HALTEN_CR5B0_HALTE_N | LIN3_HALTEN_CR5A0_HALTE_N |
| NONE     |    |    |    | R/W                       | R/W                       | R/W                       | R/W                       |
| 0h       |    |    |    | 0h                        | 0h                        | 0h                        | 0h                        |

**Table 2-173. MSS\_CTRL\_LIN3\_HALTEN Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                             |
|------|---------------------------|------|-------|---------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                  | NONE | 0h    | Reserved                                                                                                |
| 3    | LIN3_HALTEN_CR5B1_HALTE_N | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | LIN3_HALTEN_CR5A1_HALTE_N | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | LIN3_HALTEN_CR5B0_HALTE_N | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | LIN3_HALTEN_CR5A0_HALTE_N | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |

### 2.2.2.58 MSS\_CTRL\_LIN4 HALTEN Register

#### 1 MSS\_CTRL\_LIN4 HALTEN Register (Offset = 440h) [reset = 0h]

This register selects which R5 CPU when debug halted shall halt LIN[x] Peripheral.

Return to [Summary Table](#)

**Table 2-174. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0440h       |

**Figure 2-58. MSS\_CTRL\_LIN4 HALTEN Name Register**

|          |    |    |    |                           |                           |                           |                           |
|----------|----|----|----|---------------------------|---------------------------|---------------------------|---------------------------|
| 31       | 30 | 29 | 28 | 27                        | 26                        | 25                        | 24                        |
| RESERVED |    |    |    |                           |                           |                           |                           |
| NONE     |    |    |    |                           |                           |                           |                           |
| 0h       |    |    |    |                           |                           |                           |                           |
| 23       | 22 | 21 | 20 | 19                        | 18                        | 17                        | 16                        |
| RESERVED |    |    |    |                           |                           |                           |                           |
| NONE     |    |    |    |                           |                           |                           |                           |
| 0h       |    |    |    |                           |                           |                           |                           |
| 15       | 14 | 13 | 12 | 11                        | 10                        | 9                         | 8                         |
| RESERVED |    |    |    |                           |                           |                           |                           |
| NONE     |    |    |    |                           |                           |                           |                           |
| 0h       |    |    |    |                           |                           |                           |                           |
| 7        | 6  | 5  | 4  | 3                         | 2                         | 1                         | 0                         |
| RESERVED |    |    |    | LIN4 HALTEN_CR5B1_HALTE_N | LIN4 HALTEN_CR5A1_HALTE_N | LIN4 HALTEN_CR5B0_HALTE_N | LIN4 HALTEN_CR5A0_HALTE_N |
| NONE     |    |    |    | R/W                       | R/W                       | R/W                       | R/W                       |
| 0h       |    |    |    | 0h                        | 0h                        | 0h                        | 0h                        |

**Table 2-176. MSS\_CTRL\_LIN4 HALTEN Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                             |
|------|--------------------------|------|-------|---------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                 | NONE | 0h    | Reserved                                                                                                |
| 3    | LIN4_HALTEN_CR5B1_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | LIN4_HALTEN_CR5A1_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | LIN4_HALTEN_CR5B0_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | LIN4_HALTEN_CR5A0_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |



### 2.2.2.59 MSS\_CTRL\_I2C0\_HALTEN Register

#### 1 MSS\_CTRL\_I2C0\_HALTEN Register (Offset = 444h) [reset = 0h]

This register selects which R5 CPU when debug halted shall halt I2C[x] Peripheral.

Return to [Summary Table](#)

**Table 2-177. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0444h       |

**Figure 2-59. MSS\_CTRL\_I2C0\_HALTEN Name Register**

|          |    |    |    |                              |                              |                              |                              |
|----------|----|----|----|------------------------------|------------------------------|------------------------------|------------------------------|
| 31       | 30 | 29 | 28 | 27                           | 26                           | 25                           | 24                           |
| RESERVED |    |    |    |                              |                              |                              |                              |
| NONE     |    |    |    |                              |                              |                              |                              |
| 0h       |    |    |    |                              |                              |                              |                              |
| 23       | 22 | 21 | 20 | 19                           | 18                           | 17                           | 16                           |
| RESERVED |    |    |    |                              |                              |                              |                              |
| NONE     |    |    |    |                              |                              |                              |                              |
| 0h       |    |    |    |                              |                              |                              |                              |
| 15       | 14 | 13 | 12 | 11                           | 10                           | 9                            | 8                            |
| RESERVED |    |    |    |                              |                              |                              |                              |
| NONE     |    |    |    |                              |                              |                              |                              |
| 0h       |    |    |    |                              |                              |                              |                              |
| 7        | 6  | 5  | 4  | 3                            | 2                            | 1                            | 0                            |
| RESERVED |    |    |    | I2C0_HALTEN_CR5B1_HALTE<br>N | I2C0_HALTEN_CR5A1_HALTE<br>N | I2C0_HALTEN_CR5B0_HALTE<br>N | I2C0_HALTEN_CR5A0_HALTE<br>N |
| NONE     |    |    |    | R/W                          | R/W                          | R/W                          | R/W                          |
| 0h       |    |    |    | 0h                           | 0h                           | 0h                           | 0h                           |

**Table 2-179. MSS\_CTRL\_I2C0\_HALTEN Register Field Descriptions**

| Bit  | Field                        | Type | Reset | Description                                                                                             |
|------|------------------------------|------|-------|---------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                     | NONE | 0h    | Reserved                                                                                                |
| 3    | I2C0_HALTEN_CR5B1_H<br>ALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | I2C0_HALTEN_CR5A1_H<br>ALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | I2C0_HALTEN_CR5B0_H<br>ALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | I2C0_HALTEN_CR5A0_H<br>ALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |

### 2.2.2.60 MSS\_CTRL\_I2C1\_HALTEN Register

#### 1 MSS\_CTRL\_I2C1\_HALTEN Register (Offset = 448h) [reset = 0h]

This register selects which R5 CPU when debug halted shall halt I2C[x] Peripheral.

Return to [Summary Table](#)

**Table 2-180. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0448h       |

**Figure 2-60. MSS\_CTRL\_I2C1\_HALTEN Name Register**

|          |    |    |    |                              |                              |                              |                              |
|----------|----|----|----|------------------------------|------------------------------|------------------------------|------------------------------|
| 31       | 30 | 29 | 28 | 27                           | 26                           | 25                           | 24                           |
| RESERVED |    |    |    |                              |                              |                              |                              |
| NONE     |    |    |    |                              |                              |                              |                              |
| 0h       |    |    |    |                              |                              |                              |                              |
| 23       | 22 | 21 | 20 | 19                           | 18                           | 17                           | 16                           |
| RESERVED |    |    |    |                              |                              |                              |                              |
| NONE     |    |    |    |                              |                              |                              |                              |
| 0h       |    |    |    |                              |                              |                              |                              |
| 15       | 14 | 13 | 12 | 11                           | 10                           | 9                            | 8                            |
| RESERVED |    |    |    |                              |                              |                              |                              |
| NONE     |    |    |    |                              |                              |                              |                              |
| 0h       |    |    |    |                              |                              |                              |                              |
| 7        | 6  | 5  | 4  | 3                            | 2                            | 1                            | 0                            |
| RESERVED |    |    |    | I2C1_HALTEN_CR5B1_HALTE<br>N | I2C1_HALTEN_CR5A1_HALTE<br>N | I2C1_HALTEN_CR5B0_HALTE<br>N | I2C1_HALTEN_CR5A0_HALTE<br>N |
| NONE     |    |    |    | R/W                          | R/W                          | R/W                          | R/W                          |
| 0h       |    |    |    | 0h                           | 0h                           | 0h                           | 0h                           |

**Table 2-182. MSS\_CTRL\_I2C1\_HALTEN Register Field Descriptions**

| Bit  | Field                        | Type | Reset | Description                                                                                             |
|------|------------------------------|------|-------|---------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                     | NONE | 0h    | Reserved                                                                                                |
| 3    | I2C1_HALTEN_CR5B1_H<br>ALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | I2C1_HALTEN_CR5A1_H<br>ALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | I2C1_HALTEN_CR5B0_H<br>ALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | I2C1_HALTEN_CR5A0_H<br>ALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |

### 2.2.2.61 MSS\_CTRL\_I2C2\_HALTEN Register

#### 1 MSS\_CTRL\_I2C2\_HALTEN Register (Offset = 44Ch) [reset = 0h]

This register selects which R5 CPU when debug halted shall halt I2C[x] Peripheral.

Return to [Summary Table](#)

**Table 2-183. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 044Ch       |

**Figure 2-61. MSS\_CTRL\_I2C2\_HALTEN Name Register**

|          |    |    |    |                           |                           |                           |                           |
|----------|----|----|----|---------------------------|---------------------------|---------------------------|---------------------------|
| 31       | 30 | 29 | 28 | 27                        | 26                        | 25                        | 24                        |
| RESERVED |    |    |    |                           |                           |                           |                           |
| NONE     |    |    |    |                           |                           |                           |                           |
| 0h       |    |    |    |                           |                           |                           |                           |
| 23       | 22 | 21 | 20 | 19                        | 18                        | 17                        | 16                        |
| RESERVED |    |    |    |                           |                           |                           |                           |
| NONE     |    |    |    |                           |                           |                           |                           |
| 0h       |    |    |    |                           |                           |                           |                           |
| 15       | 14 | 13 | 12 | 11                        | 10                        | 9                         | 8                         |
| RESERVED |    |    |    |                           |                           |                           |                           |
| NONE     |    |    |    |                           |                           |                           |                           |
| 0h       |    |    |    |                           |                           |                           |                           |
| 7        | 6  | 5  | 4  | 3                         | 2                         | 1                         | 0                         |
| RESERVED |    |    |    | I2C2_HALTEN_CR5B1_HALTE_N | I2C2_HALTEN_CR5A1_HALTE_N | I2C2_HALTEN_CR5B0_HALTE_N | I2C2_HALTEN_CR5A0_HALTE_N |
| NONE     |    |    |    | R/W                       | R/W                       | R/W                       | R/W                       |
| 0h       |    |    |    | 0h                        | 0h                        | 0h                        | 0h                        |

**Table 2-185. MSS\_CTRL\_I2C2\_HALTEN Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                             |
|------|--------------------------|------|-------|---------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                 | NONE | 0h    | Reserved                                                                                                |
| 3    | I2C2_HALTEN_CR5B1_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | I2C2_HALTEN_CR5A1_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | I2C2_HALTEN_CR5B0_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | I2C2_HALTEN_CR5A0_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |

### 2.2.2.62 MSS\_CTRL\_I2C3\_HALTEN Register

#### 1 MSS\_CTRL\_I2C3\_HALTEN Register (Offset = 450h) [reset = 0h]

This register selects which R5 CPU when debug halted shall halt I2C[x] Peripheral.

Return to [Summary Table](#)

**Table 2-186. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0450h       |

**Figure 2-62. MSS\_CTRL\_I2C3\_HALTEN Name Register**

|          |    |    |    |                           |                           |                           |                           |
|----------|----|----|----|---------------------------|---------------------------|---------------------------|---------------------------|
| 31       | 30 | 29 | 28 | 27                        | 26                        | 25                        | 24                        |
| RESERVED |    |    |    |                           |                           |                           |                           |
| NONE     |    |    |    |                           |                           |                           |                           |
| 0h       |    |    |    |                           |                           |                           |                           |
| 23       | 22 | 21 | 20 | 19                        | 18                        | 17                        | 16                        |
| RESERVED |    |    |    |                           |                           |                           |                           |
| NONE     |    |    |    |                           |                           |                           |                           |
| 0h       |    |    |    |                           |                           |                           |                           |
| 15       | 14 | 13 | 12 | 11                        | 10                        | 9                         | 8                         |
| RESERVED |    |    |    |                           |                           |                           |                           |
| NONE     |    |    |    |                           |                           |                           |                           |
| 0h       |    |    |    |                           |                           |                           |                           |
| 7        | 6  | 5  | 4  | 3                         | 2                         | 1                         | 0                         |
| RESERVED |    |    |    | I2C3_HALTEN_CR5B1_HALTE_N | I2C3_HALTEN_CR5A1_HALTE_N | I2C3_HALTEN_CR5B0_HALTE_N | I2C3_HALTEN_CR5A0_HALTE_N |
| NONE     |    |    |    | R/W                       | R/W                       | R/W                       | R/W                       |
| 0h       |    |    |    | 0h                        | 0h                        | 0h                        | 0h                        |

**Table 2-188. MSS\_CTRL\_I2C3\_HALTEN Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                             |
|------|--------------------------|------|-------|---------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                 | NONE | 0h    | Reserved                                                                                                |
| 3    | I2C3_HALTEN_CR5B1_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | I2C3_HALTEN_CR5A1_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | I2C3_HALTEN_CR5B0_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | I2C3_HALTEN_CR5A0_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |

### 2.2.2.63 MSS\_CTRL\_RTIO\_HALTEN Register

#### 1 MSS\_CTRL\_RTIO\_HALTEN Register (Offset = 454h) [reset = 0h]

This register selects which R5 CPU when debug halted shall halt RTI[x] Peripheral.

Return to [Summary Table](#)

**Table 2-189. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0454h       |

**Figure 2-63. MSS\_CTRL\_RTIO\_HALTEN Name Register**

|          |    |    |    |                              |                              |                              |                              |
|----------|----|----|----|------------------------------|------------------------------|------------------------------|------------------------------|
| 31       | 30 | 29 | 28 | 27                           | 26                           | 25                           | 24                           |
| RESERVED |    |    |    |                              |                              |                              |                              |
| NONE     |    |    |    |                              |                              |                              |                              |
| 0h       |    |    |    |                              |                              |                              |                              |
| 23       | 22 | 21 | 20 | 19                           | 18                           | 17                           | 16                           |
| RESERVED |    |    |    |                              |                              |                              |                              |
| NONE     |    |    |    |                              |                              |                              |                              |
| 0h       |    |    |    |                              |                              |                              |                              |
| 15       | 14 | 13 | 12 | 11                           | 10                           | 9                            | 8                            |
| RESERVED |    |    |    |                              |                              |                              |                              |
| NONE     |    |    |    |                              |                              |                              |                              |
| 0h       |    |    |    |                              |                              |                              |                              |
| 7        | 6  | 5  | 4  | 3                            | 2                            | 1                            | 0                            |
| RESERVED |    |    |    | RTIO_HALTEN_CR5B1_HALTE<br>N | RTIO_HALTEN_CR5A1_HALTE<br>N | RTIO_HALTEN_CR5B0_HALTE<br>N | RTIO_HALTEN_CR5A0_HALTE<br>N |
| NONE     |    |    |    | R/W                          | R/W                          | R/W                          | R/W                          |
| 0h       |    |    |    | 0h                           | 0h                           | 0h                           | 0h                           |

**Table 2-191. MSS\_CTRL\_RTIO\_HALTEN Register Field Descriptions**

| Bit  | Field                        | Type | Reset | Description                                                                                             |
|------|------------------------------|------|-------|---------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                     | NONE | 0h    | Reserved                                                                                                |
| 3    | RTIO_HALTEN_CR5B1_H<br>ALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | RTIO_HALTEN_CR5A1_H<br>ALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | RTIO_HALTEN_CR5B0_H<br>ALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | RTIO_HALTEN_CR5A0_H<br>ALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |

### 2.2.2.64 MSS\_CTRL\_RTI1\_HALTEN Register

#### 1 MSS\_CTRL\_RTI1\_HALTEN Register (Offset = 458h) [reset = 0h]

This register selects which R5 CPU when debug halted shall halt RTI[x] Peripheral.

Return to [Summary Table](#)

**Table 2-192. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0458h       |

**Figure 2-64. MSS\_CTRL\_RTI1\_HALTEN Name Register**

|          |    |    |    |                          |                          |                          |                          |
|----------|----|----|----|--------------------------|--------------------------|--------------------------|--------------------------|
| 31       | 30 | 29 | 28 | 27                       | 26                       | 25                       | 24                       |
| RESERVED |    |    |    |                          |                          |                          |                          |
| NONE     |    |    |    |                          |                          |                          |                          |
| 0h       |    |    |    |                          |                          |                          |                          |
| 23       | 22 | 21 | 20 | 19                       | 18                       | 17                       | 16                       |
| RESERVED |    |    |    |                          |                          |                          |                          |
| NONE     |    |    |    |                          |                          |                          |                          |
| 0h       |    |    |    |                          |                          |                          |                          |
| 15       | 14 | 13 | 12 | 11                       | 10                       | 9                        | 8                        |
| RESERVED |    |    |    |                          |                          |                          |                          |
| NONE     |    |    |    |                          |                          |                          |                          |
| 0h       |    |    |    |                          |                          |                          |                          |
| 7        | 6  | 5  | 4  | 3                        | 2                        | 1                        | 0                        |
| RESERVED |    |    |    | RTI1_HALTEN_CR5B1_HALTEN | RTI1_HALTEN_CR5A1_HALTEN | RTI1_HALTEN_CR5B0_HALTEN | RTI1_HALTEN_CR5A0_HALTEN |
| NONE     |    |    |    | R/W                      | R/W                      | R/W                      | R/W                      |
| 0h       |    |    |    | 0h                       | 0h                       | 0h                       | 0h                       |

**Table 2-194. MSS\_CTRL\_RTI1\_HALTEN Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                             |
|------|--------------------------|------|-------|---------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                 | NONE | 0h    | Reserved                                                                                                |
| 3    | RTI1_HALTEN_CR5B1_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | RTI1_HALTEN_CR5A1_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | RTI1_HALTEN_CR5B0_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | RTI1_HALTEN_CR5A0_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |

### 2.2.2.65 MSS\_CTRL\_RT12\_HALTEN Register

#### 1 MSS\_CTRL\_RT12\_HALTEN Register (Offset = 45Ch) [reset = 0h]

This register selects which R5 CPU when debug halted shall halt RTI[x] Peripheral.

Return to [Summary Table](#)

**Table 2-195. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 045Ch       |

**Figure 2-65. MSS\_CTRL\_RT12\_HALTEN Name Register**

|          |    |    |    |                              |                              |                              |                              |
|----------|----|----|----|------------------------------|------------------------------|------------------------------|------------------------------|
| 31       | 30 | 29 | 28 | 27                           | 26                           | 25                           | 24                           |
| RESERVED |    |    |    |                              |                              |                              |                              |
| NONE     |    |    |    |                              |                              |                              |                              |
| 0h       |    |    |    |                              |                              |                              |                              |
| 23       | 22 | 21 | 20 | 19                           | 18                           | 17                           | 16                           |
| RESERVED |    |    |    |                              |                              |                              |                              |
| NONE     |    |    |    |                              |                              |                              |                              |
| 0h       |    |    |    |                              |                              |                              |                              |
| 15       | 14 | 13 | 12 | 11                           | 10                           | 9                            | 8                            |
| RESERVED |    |    |    |                              |                              |                              |                              |
| NONE     |    |    |    |                              |                              |                              |                              |
| 0h       |    |    |    |                              |                              |                              |                              |
| 7        | 6  | 5  | 4  | 3                            | 2                            | 1                            | 0                            |
| RESERVED |    |    |    | RTI2_HALTEN_CR5B1_HALTE<br>N | RTI2_HALTEN_CR5A1_HALTE<br>N | RTI2_HALTEN_CR5B0_HALTE<br>N | RTI2_HALTEN_CR5A0_HALTE<br>N |
| NONE     |    |    |    | R/W                          | R/W                          | R/W                          | R/W                          |
| 0h       |    |    |    | 0h                           | 0h                           | 0h                           | 0h                           |

**Table 2-197. MSS\_CTRL\_RT12\_HALTEN Register Field Descriptions**

| Bit  | Field                        | Type | Reset | Description                                                                                             |
|------|------------------------------|------|-------|---------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                     | NONE | 0h    | Reserved                                                                                                |
| 3    | RTI2_HALTEN_CR5B1_H<br>ALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | RTI2_HALTEN_CR5A1_H<br>ALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | RTI2_HALTEN_CR5B0_H<br>ALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | RTI2_HALTEN_CR5A0_H<br>ALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |

### 2.2.2.66 MSS\_CTRL\_RTI3\_HALTEN Register

#### 1 MSS\_CTRL\_RTI3\_HALTEN Register (Offset = 460h) [reset = 0h]

This register selects which R5 CPU when debug halted shall halt RTI[x] Peripheral.

Return to [Summary Table](#)

**Table 2-198. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0460h       |

**Figure 2-66. MSS\_CTRL\_RTI3\_HALTEN Name Register**

|          |    |    |    |                           |                           |                           |                           |
|----------|----|----|----|---------------------------|---------------------------|---------------------------|---------------------------|
| 31       | 30 | 29 | 28 | 27                        | 26                        | 25                        | 24                        |
| RESERVED |    |    |    |                           |                           |                           |                           |
| NONE     |    |    |    |                           |                           |                           |                           |
| 0h       |    |    |    |                           |                           |                           |                           |
| 23       | 22 | 21 | 20 | 19                        | 18                        | 17                        | 16                        |
| RESERVED |    |    |    |                           |                           |                           |                           |
| NONE     |    |    |    |                           |                           |                           |                           |
| 0h       |    |    |    |                           |                           |                           |                           |
| 15       | 14 | 13 | 12 | 11                        | 10                        | 9                         | 8                         |
| RESERVED |    |    |    |                           |                           |                           |                           |
| NONE     |    |    |    |                           |                           |                           |                           |
| 0h       |    |    |    |                           |                           |                           |                           |
| 7        | 6  | 5  | 4  | 3                         | 2                         | 1                         | 0                         |
| RESERVED |    |    |    | RTI3_HALTEN_CR5B1_HALTE_N | RTI3_HALTEN_CR5A1_HALTE_N | RTI3_HALTEN_CR5B0_HALTE_N | RTI3_HALTEN_CR5A0_HALTE_N |
| NONE     |    |    |    | R/W                       | R/W                       | R/W                       | R/W                       |
| 0h       |    |    |    | 0h                        | 0h                        | 0h                        | 0h                        |

**Table 2-200. MSS\_CTRL\_RTI3\_HALTEN Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                             |
|------|--------------------------|------|-------|---------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                 | NONE | 0h    | Reserved                                                                                                |
| 3    | RTI3_HALTEN_CR5B1_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | RTI3_HALTEN_CR5A1_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | RTI3_HALTEN_CR5B0_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | RTI3_HALTEN_CR5A0_HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |



### 2.2.2.67 MSS\_CTRL\_CPSW\_HALTEN Register

#### 1 MSS\_CTRL\_CPSW\_HALTEN Register (Offset = 474h) [reset = 0h]

This register selects which R5 CPU when debug halted shall halt CPSW Peripheral.

Return to [Summary Table](#)

**Table 2-201. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0474h       |

**Figure 2-67. MSS\_CTRL\_CPSW\_HALTEN Name Register**

|          |    |    |    |                                  |                                  |                                  |                                  |
|----------|----|----|----|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| 31       | 30 | 29 | 28 | 27                               | 26                               | 25                               | 24                               |
| RESERVED |    |    |    |                                  |                                  |                                  |                                  |
| NONE     |    |    |    |                                  |                                  |                                  |                                  |
| 0h       |    |    |    |                                  |                                  |                                  |                                  |
| 23       | 22 | 21 | 20 | 19                               | 18                               | 17                               | 16                               |
| RESERVED |    |    |    |                                  |                                  |                                  |                                  |
| NONE     |    |    |    |                                  |                                  |                                  |                                  |
| 0h       |    |    |    |                                  |                                  |                                  |                                  |
| 15       | 14 | 13 | 12 | 11                               | 10                               | 9                                | 8                                |
| RESERVED |    |    |    |                                  |                                  |                                  |                                  |
| NONE     |    |    |    |                                  |                                  |                                  |                                  |
| 0h       |    |    |    |                                  |                                  |                                  |                                  |
| 7        | 6  | 5  | 4  | 3                                | 2                                | 1                                | 0                                |
| RESERVED |    |    |    | CPSW_HALTE<br>N_CR5B1_HAL<br>TEN | CPSW_HALTE<br>N_CR5A1_HAL<br>TEN | CPSW_HALTE<br>N_CR5B0_HAL<br>TEN | CPSW_HALTE<br>N_CR5A0_HAL<br>TEN |
| NONE     |    |    |    | R/W                              | R/W                              | R/W                              | R/W                              |
| 0h       |    |    |    | 0h                               | 0h                               | 0h                               | 0h                               |

**Table 2-203. MSS\_CTRL\_CPSW\_HALTEN Register Field Descriptions**

| Bit  | Field                        | Type | Reset | Description                                                                                             |
|------|------------------------------|------|-------|---------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                     | NONE | 0h    | Reserved                                                                                                |
| 3    | CPSW_HALTEN_CR5B1_<br>HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | CPSW_HALTEN_CR5A1_<br>HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | CPSW_HALTEN_CR5B0_<br>HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | CPSW_HALTEN_CR5A0_<br>HALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |

### 2.2.2.68 MSS\_CTRL\_CRC HALTEN Register

#### 1 MSS\_CTRL\_CRC HALTEN Register (Offset = 478h) [reset = 0h]

This register selects which R5 CPU when debug halted shall halt MCRC Peripheral.

Return to [Summary Table](#)

**Table 2-204. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0478h       |

**Figure 2-68. MSS\_CTRL\_CRC HALTEN Name Register**

|          |    |    |    |                             |                             |                             |                             |
|----------|----|----|----|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| 31       | 30 | 29 | 28 | 27                          | 26                          | 25                          | 24                          |
| RESERVED |    |    |    |                             |                             |                             |                             |
| NONE     |    |    |    |                             |                             |                             |                             |
| 0h       |    |    |    |                             |                             |                             |                             |
| 23       | 22 | 21 | 20 | 19                          | 18                          | 17                          | 16                          |
| RESERVED |    |    |    |                             |                             |                             |                             |
| NONE     |    |    |    |                             |                             |                             |                             |
| 0h       |    |    |    |                             |                             |                             |                             |
| 15       | 14 | 13 | 12 | 11                          | 10                          | 9                           | 8                           |
| RESERVED |    |    |    |                             |                             |                             |                             |
| NONE     |    |    |    |                             |                             |                             |                             |
| 0h       |    |    |    |                             |                             |                             |                             |
| 7        | 6  | 5  | 4  | 3                           | 2                           | 1                           | 0                           |
| RESERVED |    |    |    | CRC HALTEN_CR5B1_HALTE<br>N | CRC HALTEN_CR5A1_HALTE<br>N | CRC HALTEN_CR5B0_HALTE<br>N | CRC HALTEN_CR5A0_HALTE<br>N |
| NONE     |    |    |    | R/W                         | R/W                         | R/W                         | R/W                         |
| 0h       |    |    |    | 0h                          | 0h                          | 0h                          | 0h                          |

**Table 2-206. MSS\_CTRL\_CRC HALTEN Register Field Descriptions**

| Bit  | Field                       | Type | Reset | Description                                                                                             |
|------|-----------------------------|------|-------|---------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                    | NONE | 0h    | Reserved                                                                                                |
| 3    | CRC_HALTEN_CR5B1_H<br>ALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | CRC_HALTEN_CR5A1_H<br>ALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | CRC_HALTEN_CR5B0_H<br>ALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | CRC_HALTEN_CR5A0_H<br>ALTEN | R/W  | 0h    | 1'b0: IP Halt disabled with corresponding CPU halt<br>1'b1: IP Halt enabled with corresponding CPU halt |

## 2.2.2.69 MSS\_CTRL\_TPTC\_DBS\_CONFIG Register

### 1 MSS\_CTRL\_TPTC\_DBS\_CONFIG Register (Offset = 800h) [reset = 11h]

This register controls the default burst size of EDMA TPTC.

Return to [Summary Table](#)

**Table 2-207. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0800h       |

**Figure 2-69. MSS\_CTRL\_TPTC\_DBS\_CONFIG Name Register**

|          |    |                         |    |          |    |                         |    |
|----------|----|-------------------------|----|----------|----|-------------------------|----|
| 31       | 30 | 29                      | 28 | 27       | 26 | 25                      | 24 |
| RESERVED |    |                         |    |          |    |                         |    |
| NONE     |    |                         |    |          |    |                         |    |
| 0h       |    |                         |    |          |    |                         |    |
| 23       | 22 | 21                      | 20 | 19       | 18 | 17                      | 16 |
| RESERVED |    |                         |    |          |    |                         |    |
| NONE     |    |                         |    |          |    |                         |    |
| 0h       |    |                         |    |          |    |                         |    |
| 15       | 14 | 13                      | 12 | 11       | 10 | 9                       | 8  |
| RESERVED |    |                         |    |          |    |                         |    |
| NONE     |    |                         |    |          |    |                         |    |
| 0h       |    |                         |    |          |    |                         |    |
| 7        | 6  | 5                       | 4  | 3        | 2  | 1                       | 0  |
| RESERVED |    | TPTC_DBS_CONFIG_TPTC_A1 |    | RESERVED |    | TPTC_DBS_CONFIG_TPTC_A0 |    |
| NONE     |    | R/W                     |    | NONE     |    | R/W                     |    |
| 0h       |    | 0h                      |    | 0h       |    | 0h                      |    |

**Table 2-209. MSS\_CTRL\_TPTC\_DBS\_CONFIG Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------|-------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:6 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 5:4  | TPTC_DBS_CONFIG_TPTC_A1 | R/W  | 0h    | DBS [default burst size] tieoff value for TPTC A1. DBS tieoff defines optimally sized cmd.Both the read and write controller will always issue commands that are less than or equal to the DBS tieoff value. This will typically be on the order of 4 or 8 dataphases worth of data. DBS must always be tied off to no larger than half of the Channel FIFO size.<br>Set DBS to -<br>2'b00 = 16 byte<br>2'b01 = 32 byte<br>2'b10 = 64 byte<br>2'b11 = 128 byte |
| 3:2  | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 1:0  | TPTC_DBS_CONFIG_TPTC_A0 | R/W  | 0h    | DBS [default burst size] tieoff value for TPTC A0. DBS tieoff defines optimally sized cmd.Both the read and write controller will always issue commands that are less than or equal to the DBS tieoff value. This will typically be on the order of 4 or 8 dataphases worth of data. DBS must always be tied off to no larger than half of the Channel FIFO size.<br>Set DBS to -<br>2'b00 = 16 byte<br>2'b01 = 32 byte<br>2'b10 = 64 byte<br>2'b11 = 128 byte |

### 2.2.2.70 MSS\_CTRL\_MSS\_TPTC\_BOUNDARY\_CFG Register

#### 1 MSS\_CTRL\_MSS\_TPTC\_BOUNDARY\_CFG Register (Offset = 804h) [reset = 1313h]

The register is used to control TPTC boundary configuration.

Return to [Summary Table](#)

**Table 2-210. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0804h       |

**Figure 2-70. MSS\_CTRL\_MSS\_TPTC\_BOUNDARY\_CFG Name Register**

|          |    |                                    |    |    |    |    |    |
|----------|----|------------------------------------|----|----|----|----|----|
| 31       | 30 | 29                                 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |                                    |    |    |    |    |    |
| NONE     |    |                                    |    |    |    |    |    |
| 0h       |    |                                    |    |    |    |    |    |
| 23       | 22 | 21                                 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |                                    |    |    |    |    |    |
| NONE     |    |                                    |    |    |    |    |    |
| 0h       |    |                                    |    |    |    |    |    |
| 15       | 14 | 13                                 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    | MSS_TPTC_BOUNDARY_CFG_TPTC_A1_SIZE |    |    |    |    |    |
| NONE     |    | R/W                                |    |    |    |    |    |
| 0h       |    | 13h                                |    |    |    |    |    |
| 7        | 6  | 5                                  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    | MSS_TPTC_BOUNDARY_CFG_TPTC_A0_SIZE |    |    |    |    |    |
| NONE     |    | R/W                                |    |    |    |    |    |
| 0h       |    | 13h                                |    |    |    |    |    |

**Table 2-212. MSS\_CTRL\_MSS\_TPTC\_BOUNDARY\_CFG Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                                                                                           |
|-------|------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:14 | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                              |
| 13:8  | MSS_TPTC_BOUNDARY_CFG_TPTC_A1_SIZE | R/W  | 13h   | 6 bit signal used for deciding the boundary crossing size for CID-RID-SID reordering of MSS_TPTC_A1<br>Example: Writing 6'd19 decides boundary to be 2^19 i.e. 512 KB |
| 7:6   | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                              |
| 5:0   | MSS_TPTC_BOUNDARY_CFG_TPTC_A0_SIZE | R/W  | 13h   | 6 bit signal used for deciding the boundary crossing size for CID-RID-SID reordering of MSS_TPTC_A0<br>Example: Writing 6'd19 decides boundary to be 2^19 i.e. 512 KB |

### 2.2.2.71 MSS\_CTRL\_MSS\_TPTC\_XID\_REORDER\_CFG Register

#### 1 MSS\_CTRL\_MSS\_TPTC\_XID\_REORDER\_CFG Register (Offset = 808h) [reset = 0h]

The register is used to control TPTC XID reorder configuration.

Return to [Summary Table](#)

**Table 2-213. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0808h       |

**Figure 2-71. MSS\_CTRL\_MSS\_TPTC\_XID\_REORDER\_CFG Name Register**

|          |    |    |    |    |    |    |                                          |
|----------|----|----|----|----|----|----|------------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                                       |
| RESERVED |    |    |    |    |    |    |                                          |
| NONE     |    |    |    |    |    |    |                                          |
| 0h       |    |    |    |    |    |    |                                          |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                                       |
| RESERVED |    |    |    |    |    |    |                                          |
| NONE     |    |    |    |    |    |    |                                          |
| 0h       |    |    |    |    |    |    |                                          |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                                        |
| RESERVED |    |    |    |    |    |    | MSS_TPTC_XID_REORDER_CFG_TPTC_A1_DISABLE |
| NONE     |    |    |    |    |    |    | R/W                                      |
| 0h       |    |    |    |    |    |    | 0h                                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                                        |
| RESERVED |    |    |    |    |    |    | MSS_TPTC_XID_REORDER_CFG_TPTC_A0_DISABLE |
| NONE     |    |    |    |    |    |    | R/W                                      |
| 0h       |    |    |    |    |    |    | 0h                                       |

**Table 2-215. MSS\_CTRL\_MSS\_TPTC\_XID\_REORDER\_CFG Register Field Descriptions**

| Bit  | Field                                    | Type | Reset | Description                                                                  |
|------|------------------------------------------|------|-------|------------------------------------------------------------------------------|
| 31:9 | RESERVED                                 | NONE | 0h    | Reserved                                                                     |
| 8    | MSS_TPTC_XID_REORDER_CFG_TPTC_A1_DISABLE | R/W  | 0h    | Writing 1'b1 will disable the CID-RID-SID reordering feature for MSS_TPTC_A1 |
| 7:1  | RESERVED                                 | NONE | 0h    | Reserved                                                                     |
| 0    | MSS_TPTC_XID_REORDER_CFG_TPTC_A0_DISABLE | R/W  | 0h    | Writing 1'b1 will disable the CID-RID-SID reordering feature for MSS_TPTC_A0 |

### 2.2.2.72 MSS\_CTRL\_CPSW\_CONTROL Register

#### 1 MSS\_CTRL\_CPSW\_CONTROL Register (Offset = 810h) [reset = 1000100h]

The register is for the CPSW Ethernet modes and additional controls on the.

Return to [Summary Table](#)

**Table 2-216. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0810h       |

**Figure 2-72. MSS\_CTRL\_CPSW\_CONTROL Name Register**

| 31       | 30                                     | 29       | 28                                      | 27       | 26                          | 25 | 24                                  |
|----------|----------------------------------------|----------|-----------------------------------------|----------|-----------------------------|----|-------------------------------------|
| RESERVED |                                        |          |                                         |          |                             |    | CPSW_CONTR<br>OL_RGMII2_ID<br>_MODE |
| NONE     |                                        |          |                                         |          |                             |    | R/W                                 |
| 0h       |                                        |          |                                         |          |                             |    | 1h                                  |
| 23       | 22                                     | 21       | 20                                      | 19       | 18                          | 17 | 16                                  |
| RESERVED | CPSW_CONTR<br>OL_RMII2_REF<br>_CLK_SEL | RESERVED | CPSW_CONTR<br>OL_RMII2_REF<br>_CLK_OE_N | RESERVED | CPSW_CONTROL_PORT2_MODE_SEL |    |                                     |
| NONE     | R/W                                    | NONE     | R/W                                     | NONE     | R/W                         |    |                                     |
| 0h       | 0h                                     | 0h       | 0h                                      | 0h       | 0h                          |    |                                     |
| 15       | 14                                     | 13       | 12                                      | 11       | 10                          | 9  | 8                                   |
| RESERVED |                                        |          |                                         |          |                             |    | CPSW_CONTR<br>OL_RGMII1_ID<br>_MODE |
| NONE     |                                        |          |                                         |          |                             |    | R/W                                 |
| 0h       |                                        |          |                                         |          |                             |    | 1h                                  |
| 7        | 6                                      | 5        | 4                                       | 3        | 2                           | 1  | 0                                   |
| RESERVED | CPSW_CONTR<br>OL_RMII1_REF<br>_CLK_SEL | RESERVED | CPSW_CONTR<br>OL_RMII1_REF<br>_CLK_OE_N | RESERVED | CPSW_CONTROL_PORT1_MODE_SEL |    |                                     |
| NONE     | R/W                                    | NONE     | R/W                                     | NONE     | R/W                         |    |                                     |
| 0h       | 0h                                     | 0h       | 0h                                      | 0h       | 0h                          |    |                                     |

**Table 2-218. MSS\_CTRL\_CPSW\_CONTROL Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                                                                                                                      |
|-------|---------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:25 | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                                                                         |
| 24    | CPSW_CONTROL_RGMII2_ID_MODE     | R/W  | 1h    | Internal delay mode for port 2. Only for TX<br>1'b0 ID mode is disabled<br>1'b1 ID mode is enabled                                                                                               |
| 23    | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                                                                         |
| 22    | CPSW_CONTROL_RMII2_REF_CLK_SEL  | R/W  | 0h    | To select the rmii_ref_clk loopback mux output either from PAD or from MSS_RCM.<br>Write 1'b0 to get clock will be from IO pad[pad loopback].<br>Write 1'b1 to get clock from internal loopback. |
| 21    | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                                                                         |
| 20    | CPSW_CONTROL_RMII2_REF_CLK_OE_N | R/W  | 0h    | RMII_REF_CLK IO Output enable control<br>1'b0: Output enable<br>1'b1: Output Disable                                                                                                             |
| 19    | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                                                                         |

**Table 2-218. MSS\_CTRL\_CPSW\_CONTROL Register Field Descriptions (continued)**

| Bit   | Field                           | Type | Reset | Description                                                                                                                                                                                   |
|-------|---------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 18:16 | CPSW_CONTROL_PORT_2_MODE_SEL    | R/W  | 0h    | Port 2 Interface<br>3'b000 = MII<br>3'b001 = RMII<br>3'b010 = RGMII<br>011 - 111 = Not Supported                                                                                              |
| 15:9  | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                                                                      |
| 8     | CPSW_CONTROL_RGMII_1_ID_MODE    | R/W  | 1h    | Internal delay mode for port 1. Only for TX<br>1'b0 ID mode is disabled<br>1'b1 ID mode is enabled                                                                                            |
| 7     | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                                                                      |
| 6     | CPSW_CONTROL_RMII1_REF_CLK_SEL  | R/W  | 0h    | To select the rmii_ref_clk loopback mux output either from PAD or from MSS_RCM.<br>Write 1'b0 to get clock will be from IO pad[pad loopback].<br>Write 1'b1 to get clock from internal source |
| 5     | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                                                                      |
| 4     | CPSW_CONTROL_RMII1_REF_CLK_OE_N | R/W  | 0h    | RMII_REF_CLK IO Output enable control<br>1'b0: Output enable<br>1'b1: Output Disable                                                                                                          |
| 3     | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                                                                      |
| 2:0   | CPSW_CONTROL_PORT_1_MODE_SEL    | R/W  | 0h    | Port 1 Interface<br>3'b000 = MII<br>3'b001 = RMII<br>3'b010 = RGMII<br>011 - 111 = Not Supported                                                                                              |

### 2.2.2.73 MSS\_CTRL\_GLOBAL\_CONTROLS Register

#### 1 MSS\_CTRL\_GLOBAL\_CONTROLS Register (Offset = 818h) [reset = 1h]

Internal Only.

Return to [Summary Table](#)

**Table 2-219. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0818h       |

**Figure 2-73. MSS\_CTRL\_GLOBAL\_CONTROLS Name Register**

|          |    |    |    |    |    |    |                                |
|----------|----|----|----|----|----|----|--------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                             |
| RESERVED |    |    |    |    |    |    |                                |
| NONE     |    |    |    |    |    |    |                                |
| 0h       |    |    |    |    |    |    |                                |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                             |
| RESERVED |    |    |    |    |    |    |                                |
| NONE     |    |    |    |    |    |    |                                |
| 0h       |    |    |    |    |    |    |                                |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                              |
| RESERVED |    |    |    |    |    |    |                                |
| NONE     |    |    |    |    |    |    |                                |
| 0h       |    |    |    |    |    |    |                                |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                              |
| RESERVED |    |    |    |    |    |    | GLOBAL_CON<br>TROLS_NOGA<br>TE |
| NONE     |    |    |    |    |    |    | R/W                            |
| 0h       |    |    |    |    |    |    | 1h                             |

**Table 2-221. MSS\_CTRL\_GLOBAL\_CONTROLS Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                                                                                                                                   |
|------|------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED               | NONE | 0h    | Reserved                                                                                                                                                                      |
| 0    | GLOBAL_CONTROLS_NOGATE | R/W  | 1h    | Writing 1'b0 will enable local auto-clock gating [lower power] at IP level with increase in access/functional latency. Following IPs are controlled with this signal<br>ICSSM |



### 2.2.2.74 MSS\_CTRL\_PRU\_ICSS\_PRU0\_GPI\_SEL Register

#### 1 MSS\_CTRL\_PRU\_ICSS\_PRU0\_GPI\_SEL Register (Offset = 81Ch) [reset = 0h]

Selects Chip input or Control peripheral for ICSSM PRU0 GPI source.

Return to [Summary Table](#)

**Table 2-222. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 081Ch       |

**Figure 2-74. MSS\_CTRL\_PRU\_ICSS\_PRU0\_GPI\_SEL Name Register**

|                           |    |                           |    |    |    |    |    |
|---------------------------|----|---------------------------|----|----|----|----|----|
| 31                        | 30 | 29                        | 28 | 27 | 26 | 25 | 24 |
| RESERVED                  |    | PRU_ICSS_PRU0_GPI_SEL_SEL |    |    |    |    |    |
| NONE                      |    | R/W                       |    |    |    |    |    |
| 0h                        |    | 0h                        |    |    |    |    |    |
| 23                        | 22 | 21                        | 20 | 19 | 18 | 17 | 16 |
| PRU_ICSS_PRU0_GPI_SEL_SEL |    |                           |    |    |    |    |    |
| R/W                       |    |                           |    |    |    |    |    |
| 0h                        |    |                           |    |    |    |    |    |
| 15                        | 14 | 13                        | 12 | 11 | 10 | 9  | 8  |
| PRU_ICSS_PRU0_GPI_SEL_SEL |    |                           |    |    |    |    |    |
| R/W                       |    |                           |    |    |    |    |    |
| 0h                        |    |                           |    |    |    |    |    |
| 7                         | 6  | 5                         | 4  | 3  | 2  | 1  | 0  |
| PRU_ICSS_PRU0_GPI_SEL_SEL |    |                           |    |    |    |    |    |
| R/W                       |    |                           |    |    |    |    |    |
| 0h                        |    |                           |    |    |    |    |    |

**Table 2-224. MSS\_CTRL\_PRU\_ICSS\_PRU0\_GPI\_SEL Register Field Descriptions**

| Bit   | Field                     | Type | Reset | Description                                                       |
|-------|---------------------------|------|-------|-------------------------------------------------------------------|
| 31:30 | RESERVED                  | NONE | 0h    | Reserved                                                          |
| 29:0  | PRU_ICSS_PRU0_GPI_SEL_SEL | R/W  | 0h    | GPI or PWMXBAR select for ICSSM Port0<br>1'b0 GPI<br>1'b1 PWMXBAR |

### 2.2.2.75 MSS\_CTRL\_PRU\_ICSS\_PRU1\_GPI\_SEL Register

#### 1 MSS\_CTRL\_PRU\_ICSS\_PRU1\_GPI\_SEL Register (Offset = 820h) [reset = 0h]

Selects Chip input or Control peripheral for ICSSM PRU1 GPI source.

Return to [Summary Table](#)

**Table 2-225. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0820h       |

**Figure 2-75. MSS\_CTRL\_PRU\_ICSS\_PRU1\_GPI\_SEL Name Register**

|                           |    |                           |    |    |    |    |    |
|---------------------------|----|---------------------------|----|----|----|----|----|
| 31                        | 30 | 29                        | 28 | 27 | 26 | 25 | 24 |
| RESERVED                  |    | PRU_ICSS_PRU1_GPI_SEL_SEL |    |    |    |    |    |
| NONE                      |    | R/W                       |    |    |    |    |    |
| 0h                        |    | 0h                        |    |    |    |    |    |
| 23                        | 22 | 21                        | 20 | 19 | 18 | 17 | 16 |
| PRU_ICSS_PRU1_GPI_SEL_SEL |    |                           |    |    |    |    |    |
| R/W                       |    |                           |    |    |    |    |    |
| 0h                        |    |                           |    |    |    |    |    |
| 15                        | 14 | 13                        | 12 | 11 | 10 | 9  | 8  |
| PRU_ICSS_PRU1_GPI_SEL_SEL |    |                           |    |    |    |    |    |
| R/W                       |    |                           |    |    |    |    |    |
| 0h                        |    |                           |    |    |    |    |    |
| 7                         | 6  | 5                         | 4  | 3  | 2  | 1  | 0  |
| PRU_ICSS_PRU1_GPI_SEL_SEL |    |                           |    |    |    |    |    |
| R/W                       |    |                           |    |    |    |    |    |
| 0h                        |    |                           |    |    |    |    |    |

**Table 2-227. MSS\_CTRL\_PRU\_ICSS\_PRU1\_GPI\_SEL Register Field Descriptions**

| Bit   | Field                     | Type | Reset | Description                                                       |
|-------|---------------------------|------|-------|-------------------------------------------------------------------|
| 31:30 | RESERVED                  | NONE | 0h    | Reserved                                                          |
| 29:0  | PRU_ICSS_PRU1_GPI_SEL_SEL | R/W  | 0h    | GPI or PWMXBAR select for ICSSM Port0<br>1'b0 GPI<br>1'b1 PWMXBAR |

### 2.2.2.76 MSS\_CTRL\_PRU\_ICSS\_PRU0\_GPIO\_OUT\_CTRL Register

#### 1 MSS\_CTRL\_PRU\_ICSS\_PRU0\_GPIO\_OUT\_CTRL Register (Offset = 824h) [reset = 0h]

Controls the Output enable of the ICSSM PRU0 GPIO pins.

Return to [Summary Table](#)

**Table 2-228. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0824h       |

**Figure 2-76. MSS\_CTRL\_PRU\_ICSS\_PRU0\_GPIO\_OUT\_CTRL Name Register**

|                                        |    |                                        |    |    |    |    |    |
|----------------------------------------|----|----------------------------------------|----|----|----|----|----|
| 31                                     | 30 | 29                                     | 28 | 27 | 26 | 25 | 24 |
| RESERVED                               |    | PRU_ICSS_PRU0_GPIO_OUT_CTRL_OUTDISABLE |    |    |    |    |    |
| NONE                                   |    | R/W                                    |    |    |    |    |    |
| 0h                                     |    | 0h                                     |    |    |    |    |    |
| 23                                     | 22 | 21                                     | 20 | 19 | 18 | 17 | 16 |
| PRU_ICSS_PRU0_GPIO_OUT_CTRL_OUTDISABLE |    |                                        |    |    |    |    |    |
| R/W                                    |    |                                        |    |    |    |    |    |
| 0h                                     |    |                                        |    |    |    |    |    |
| 15                                     | 14 | 13                                     | 12 | 11 | 10 | 9  | 8  |
| PRU_ICSS_PRU0_GPIO_OUT_CTRL_OUTDISABLE |    |                                        |    |    |    |    |    |
| R/W                                    |    |                                        |    |    |    |    |    |
| 0h                                     |    |                                        |    |    |    |    |    |
| 7                                      | 6  | 5                                      | 4  | 3  | 2  | 1  | 0  |
| PRU_ICSS_PRU0_GPIO_OUT_CTRL_OUTDISABLE |    |                                        |    |    |    |    |    |
| R/W                                    |    |                                        |    |    |    |    |    |
| 0h                                     |    |                                        |    |    |    |    |    |

**Table 2-230. MSS\_CTRL\_PRU\_ICSS\_PRU0\_GPIO\_OUT\_CTRL Register Field Descriptions**

| Bit   | Field                                             | Type | Reset | Description                                                                                                                                                                         |
|-------|---------------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | RESERVED                                          | NONE | 0h    | Reserved                                                                                                                                                                            |
| 29:0  | PRU_ICSS_PRU0_GPIO_OUT_CTRL_OUTDISAB <sub>E</sub> | R/W  | 0h    | GPO output disable for ICSSM Port 0 IO. Disable output for using the pin as input.<br>Each Bit maps to the corresponding bit in the IO<br>1'b0 Output Enable<br>1'b1 Output Disable |

### 2.2.2.77 MSS\_CTRL\_PRU\_ICSS\_PRU1\_GPIO\_OUT\_CTRL Register

#### 1 MSS\_CTRL\_PRU\_ICSS\_PRU1\_GPIO\_OUT\_CTRL Register (Offset = 828h) [reset = 0h]

Controls the Output enable of the ICSSM PRU1 GPIO pins.

Return to [Summary Table](#)

**Table 2-231. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0828h       |

**Figure 2-77. MSS\_CTRL\_PRU\_ICSS\_PRU1\_GPIO\_OUT\_CTRL Name Register**

|                                        |    |                                        |    |    |    |    |    |
|----------------------------------------|----|----------------------------------------|----|----|----|----|----|
| 31                                     | 30 | 29                                     | 28 | 27 | 26 | 25 | 24 |
| RESERVED                               |    | PRU_ICSS_PRU1_GPIO_OUT_CTRL_OUTDISABLE |    |    |    |    |    |
| NONE                                   |    | R/W                                    |    |    |    |    |    |
| 0h                                     |    | 0h                                     |    |    |    |    |    |
| 23                                     | 22 | 21                                     | 20 | 19 | 18 | 17 | 16 |
| PRU_ICSS_PRU1_GPIO_OUT_CTRL_OUTDISABLE |    |                                        |    |    |    |    |    |
| R/W                                    |    |                                        |    |    |    |    |    |
| 0h                                     |    |                                        |    |    |    |    |    |
| 15                                     | 14 | 13                                     | 12 | 11 | 10 | 9  | 8  |
| PRU_ICSS_PRU1_GPIO_OUT_CTRL_OUTDISABLE |    |                                        |    |    |    |    |    |
| R/W                                    |    |                                        |    |    |    |    |    |
| 0h                                     |    |                                        |    |    |    |    |    |
| 7                                      | 6  | 5                                      | 4  | 3  | 2  | 1  | 0  |
| PRU_ICSS_PRU1_GPIO_OUT_CTRL_OUTDISABLE |    |                                        |    |    |    |    |    |
| R/W                                    |    |                                        |    |    |    |    |    |
| 0h                                     |    |                                        |    |    |    |    |    |

**Table 2-233. MSS\_CTRL\_PRU\_ICSS\_PRU1\_GPIO\_OUT\_CTRL Register Field Descriptions**

| Bit   | Field                                             | Type | Reset | Description                                                                                                                                                                         |
|-------|---------------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | RESERVED                                          | NONE | 0h    | Reserved                                                                                                                                                                            |
| 29:0  | PRU_ICSS_PRU1_GPIO_OUT_CTRL_OUTDISAB <sub>E</sub> | R/W  | 0h    | GPO output disable for ICSSM Port 1 IO. Disable output for using the pin as input.<br>Each Bit maps to the corresponding bit in the IO<br>1'b0 Output Enable<br>1'b1 Output Disable |

### 2.2.2.78 MSS\_CTRL\_GPMC\_CONTROL Register

#### 1 MSS\_CTRL\_GPMC\_CONTROL Register (Offset = 82Ch) [reset = 100h]

This register is used to configure the GPMC Clock source and Loop Back clock Source.

Return to [Summary Table](#)

**Table 2-234. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 082Ch       |

**Figure 2-78. MSS\_CTRL\_GPMC\_CONTROL Name Register**

|          |    |    |                                  |          |    |    |                                 |
|----------|----|----|----------------------------------|----------|----|----|---------------------------------|
| 31       | 30 | 29 | 28                               | 27       | 26 | 25 | 24                              |
| RESERVED |    |    |                                  |          |    |    |                                 |
| NONE     |    |    |                                  |          |    |    |                                 |
| 0h       |    |    |                                  |          |    |    |                                 |
| 23       | 22 | 21 | 20                               | 19       | 18 | 17 | 16                              |
| RESERVED |    |    |                                  |          |    |    |                                 |
| NONE     |    |    |                                  |          |    |    |                                 |
| 0h       |    |    |                                  |          |    |    |                                 |
| 15       | 14 | 13 | 12                               | 11       | 10 | 9  | 8                               |
| RESERVED |    |    | GPMC_CONTR<br>OL_CLK_LB_O<br>E_N | RESERVED |    |    | GPMC_CONTR<br>OL_CLK_OE_N       |
| NONE     |    |    | R/W                              | NONE     |    |    | R/W                             |
| 0h       |    |    | 0h                               | 0h       |    |    | 1h                              |
| 7        | 6  | 5  | 4                                | 3        | 2  | 1  | 0                               |
| RESERVED |    |    | GPMC_CONTR<br>OL_CLK_LB_S<br>EL  | RESERVED |    |    | GPMC_CONTR<br>OL_CLKOUT_S<br>EL |
| NONE     |    |    | R/W                              | NONE     |    |    | R/W                             |
| 0h       |    |    | 0h                               | 0h       |    |    | 0h                              |

**Table 2-236. MSS\_CTRL\_GPMC\_CONTROL Register Field Descriptions**

| Bit   | Field                    | Type | Reset | Description                                                                                                            |
|-------|--------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------|
| 31:13 | RESERVED                 | NONE | 0h    | Reserved                                                                                                               |
| 12    | GPMC_CONTROL_CLK_LB_OE_N | R/W  | 0h    | GPMC_CLK_LB oe_n<br>1'b1 GPMC_dev_clk is driven to pad<br>1'b0 GPMC_dev_clk is not driven to pad                       |
| 11:9  | RESERVED                 | NONE | 0h    | Reserved                                                                                                               |
| 8     | GPMC_CONTROL_CLK_OE_N    | R/W  | 1h    | GPMC_CLKOUT oe_n<br>1'b1 GPMC_dev_clk mux output is driven to pad<br>1'b0 GPMC_dev_clk mux output is not driven to pad |
| 7:5   | RESERVED                 | NONE | 0h    | Reserved                                                                                                               |
| 4     | GPMC_CONTROL_CLK_LB_SEL  | R/W  | 0h    | GPMC_CLK_LB sel<br>1'b0 GPMC_CLK_LB pad clock<br>1'b1 GPMC_CLK pad clock                                               |
| 3:1   | RESERVED                 | NONE | 0h    | Reserved                                                                                                               |
| 0     | GPMC_CONTROL_CLKOUT_SEL  | R/W  | 0h    | GPMC_CLKOUT sel<br>1'b0 GPMC_func_clock<br>1'b1 GPMC_dev clock                                                         |

### 2.2.2.79 MSS\_CTRL\_MSS\_TPCC\_A\_INTAGG\_MASK Register

#### 1 MSS\_CTRL\_MSS\_TPCC\_A\_INTAGG\_MASK Register (Offset = 830h) [reset = 0h]

This register Masks selected interrupt sources from the Aggregated TPCC0 interrupt.

Return to [Summary Table](#)

**Table 2-237. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0830h       |

**Figure 2-79. MSS\_CTRL\_MSS\_TPCC\_A\_INTAGG\_MASK Name Register**

|                                    |                                    |                                    |                                    |                                    |                                    |                                    |                                    |
|------------------------------------|------------------------------------|------------------------------------|------------------------------------|------------------------------------|------------------------------------|------------------------------------|------------------------------------|
| 31                                 | 30                                 | 29                                 | 28                                 | 27                                 | 26                                 | 25                                 | 24                                 |
| RESERVED                           |                                    |                                    |                                    |                                    |                                    |                                    |                                    |
| NONE                               |                                    |                                    |                                    |                                    |                                    |                                    |                                    |
| 0h                                 |                                    |                                    |                                    |                                    |                                    |                                    |                                    |
| 23                                 | 22                                 | 21                                 | 20                                 | 19                                 | 18                                 | 17                                 | 16                                 |
| RESERVED                           |                                    |                                    |                                    |                                    |                                    | MSS_TPCC_A_INTAGG_MASK_TPTC_A1     | MSS_TPCC_A_INTAGG_MASK_TPTC_A0     |
| NONE                               |                                    |                                    |                                    |                                    |                                    | R/W                                | R/W                                |
| 0h                                 |                                    |                                    |                                    |                                    |                                    | 0h                                 | 0h                                 |
| 15                                 | 14                                 | 13                                 | 12                                 | 11                                 | 10                                 | 9                                  | 8                                  |
| RESERVED                           |                                    |                                    |                                    |                                    |                                    |                                    | MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT7 |
| NONE                               |                                    |                                    |                                    |                                    |                                    |                                    | R/W                                |
| 0h                                 |                                    |                                    |                                    |                                    |                                    |                                    | 0h                                 |
| 7                                  | 6                                  | 5                                  | 4                                  | 3                                  | 2                                  | 1                                  | 0                                  |
| MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT6 | MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT5 | MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT4 | MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT3 | MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT2 | MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT1 | MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT0 | MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT0 |
| R/W                                | R/W                                | R/W                                | R/W                                | R/W                                | R/W                                | R/W                                | R/W                                |
| 0h                                 | 0h                                 | 0h                                 | 0h                                 | 0h                                 | 0h                                 | 0h                                 | 0h                                 |

**Table 2-239. MSS\_CTRL\_MSS\_TPCC\_A\_INTAGG\_MASK Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                                                               |
|-------|------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                  |
| 17    | MSS_TPCC_A_INTAGG_MASK_TPTC_A1     | R/W  | 0h    | Mask Interrupt from TPTC A1 to aggregated Interrupt<br>MSS_TPCC_A_INTAGG<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked    |
| 16    | MSS_TPCC_A_INTAGG_MASK_TPTC_A0     | R/W  | 0h    | Mask Interrupt from TPTC A0 to aggregated Interrupt<br>MSS_TPCC_A_INTAGG<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked    |
| 15:9  | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                  |
| 8     | MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT7 | R/W  | 0h    | Mask Interrupt from MSS_TPCC_A to aggregated Interrupt<br>MSS_TPCC_A_INTAGG<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |

**Table 2-239. MSS\_CTRL\_MSS\_TPCC\_A\_INTAGG\_MASK Register Field Descriptions (continued)**

| Bit | Field                              | Type | Reset | Description                                                                                                                            |
|-----|------------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| 7   | MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT6 | R/W  | 0h    | Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 6   | MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT5 | R/W  | 0h    | Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 5   | MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT4 | R/W  | 0h    | Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 4   | MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT3 | R/W  | 0h    | Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 3   | MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT2 | R/W  | 0h    | Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 2   | MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT1 | R/W  | 0h    | Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 1   | MSS_TPCC_A_INTAGG_MASK_TPCC_A_INT0 | R/W  | 0h    | Mask Interrupt from TPCC A to aggregated Interrupt MSS_TPCC_A_INTAGG<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked     |
| 0   | MSS_TPCC_A_INTAGG_MASK_TPCC_A_INTG | R/W  | 0h    | Mask Interrupt from MSS_TPCC_A to aggregated Interrupt MSS_TPCC_A_INTAGG<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |

### 2.2.2.80 MSS\_CTRL\_MSS\_TPCC\_A\_INTAGG\_STATUS Register

#### 1 MSS\_CTRL\_MSS\_TPCC\_A\_INTAGG\_STATUS Register (Offset = 834h) [reset = 0h]

This register shows the Status of Unmasked Interrupts from TPCC0.

Return to [Summary Table](#)

**Table 2-240. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0834h       |

**Figure 2-80. MSS\_CTRL\_MSS\_TPCC\_A\_INTAGG\_STATUS Name Register**

|                                       |                                       |                                       |                                       |                                       |                                       |                                       |                                       |
|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|
| 31                                    | 30                                    | 29                                    | 28                                    | 27                                    | 26                                    | 25                                    | 24                                    |
| RESERVED                              |                                       |                                       |                                       |                                       |                                       |                                       |                                       |
| NONE                                  |                                       |                                       |                                       |                                       |                                       |                                       |                                       |
| 0h                                    |                                       |                                       |                                       |                                       |                                       |                                       |                                       |
| 23                                    | 22                                    | 21                                    | 20                                    | 19                                    | 18                                    | 17                                    | 16                                    |
| RESERVED                              |                                       |                                       |                                       |                                       |                                       | MSS_TPCC_A_INTAGG_STAT_US_TPTC_A1     | MSS_TPCC_A_INTAGG_STAT_US_TPTC_A0     |
| NONE                                  |                                       |                                       |                                       |                                       |                                       | R/W                                   | R/W                                   |
| 0h                                    |                                       |                                       |                                       |                                       |                                       | 0h                                    | 0h                                    |
| 15                                    | 14                                    | 13                                    | 12                                    | 11                                    | 10                                    | 9                                     | 8                                     |
| RESERVED                              |                                       |                                       |                                       |                                       |                                       |                                       | MSS_TPCC_A_INTAGG_STAT_US_TPCC_A_INT7 |
| NONE                                  |                                       |                                       |                                       |                                       |                                       |                                       | R/W                                   |
| 0h                                    |                                       |                                       |                                       |                                       |                                       |                                       | 0h                                    |
| 7                                     | 6                                     | 5                                     | 4                                     | 3                                     | 2                                     | 1                                     | 0                                     |
| MSS_TPCC_A_INTAGG_STAT_US_TPCC_A_INT6 | MSS_TPCC_A_INTAGG_STAT_US_TPCC_A_INT5 | MSS_TPCC_A_INTAGG_STAT_US_TPCC_A_INT4 | MSS_TPCC_A_INTAGG_STAT_US_TPCC_A_INT3 | MSS_TPCC_A_INTAGG_STAT_US_TPCC_A_INT2 | MSS_TPCC_A_INTAGG_STAT_US_TPCC_A_INT1 | MSS_TPCC_A_INTAGG_STAT_US_TPCC_A_INT0 | MSS_TPCC_A_INTAGG_STAT_US_TPCC_A_INTG |
| R/W                                   | R/W                                   | R/W                                   | R/W                                   | R/W                                   | R/W                                   | R/W                                   | R/W                                   |
| 0h                                    | 0h                                    | 0h                                    | 0h                                    | 0h                                    | 0h                                    | 0h                                    | 0h                                    |

**Table 2-242. MSS\_CTRL\_MSS\_TPCC\_A\_INTAGG\_STATUS Register Field Descriptions**

| Bit   | Field                                | Type | Reset | Description                                                                                                                               |
|-------|--------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                                  |
| 17    | MSS_TPCC_A_INTAGG_STATUS_TPTC_A1     | R/W  | 0h    | Status of Interrupt from TPTC A1.<br>Set only if Interrupt is unmasked in MSS_TPCC_A_INTAGG_MASK<br>Write 0x1 to clear this interrupt.    |
| 16    | MSS_TPCC_A_INTAGG_STATUS_TPTC_A0     | R/W  | 0h    | Status of Interrupt from TPTC A0.<br>Set only if Interrupt is unmasked in MSS_TPCC_A_INTAGG_MASK<br>Write 0x1 to clear this interrupt.    |
| 15:9  | RESERVED                             | NONE | 0h    | Reserved                                                                                                                                  |
| 8     | MSS_TPCC_A_INTAGG_STATUS_TPCC_A_INT7 | R/W  | 0h    | Status of Interrupt from MSS_TPCC_A.<br>Set only if Interrupt is unmasked in MSS_TPCC_A_INTAGG_MASK<br>Write 0x1 to clear this interrupt. |
| 7     | MSS_TPCC_A_INTAGG_STATUS_TPCC_A_INT6 | R/W  | 0h    | Status of Interrupt from MSS_TPCC_A.<br>Set only if Interrupt is unmasked in MSS_TPCC_A_INTAGG_MASK<br>Write 0x1 to clear this interrupt. |



**Table 2-242. MSS\_CTRL\_MSS\_TPCC\_A\_INTAGG\_STATUS Register Field Descriptions (continued)**

| Bit | Field                                | Type | Reset | Description                                                                                                                             |
|-----|--------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 6   | MSS_TPCC_A_INTAGG_STATUS_TPCC_A_INT5 | R/W  | 0h    | Status of Interrupt from MSS_TPCC_A.<br>Set only if Interupt is unmasked in MSS_TPCC_A_INTAGG_MASK<br>Wrie 0x1 to clear this interrupt. |
| 5   | MSS_TPCC_A_INTAGG_STATUS_TPCC_A_INT4 | R/W  | 0h    | Status of Interrupt from MSS_TPCC_A.<br>Set only if Interupt is unmasked in MSS_TPCC_A_INTAGG_MASK<br>Wrie 0x1 to clear this interrupt. |
| 4   | MSS_TPCC_A_INTAGG_STATUS_TPCC_A_INT3 | R/W  | 0h    | Status of Interrupt from MSS_TPCC_A.<br>Set only if Interupt is unmasked in MSS_TPCC_A_INTAGG_MASK<br>Wrie 0x1 to clear this interrupt. |
| 3   | MSS_TPCC_A_INTAGG_STATUS_TPCC_A_INT2 | R/W  | 0h    | Status of Interrupt from MSS_TPCC_A.<br>Set only if Interupt is unmasked in MSS_TPCC_A_INTAGG_MASK<br>Wrie 0x1 to clear this interrupt. |
| 2   | MSS_TPCC_A_INTAGG_STATUS_TPCC_A_INT1 | R/W  | 0h    | Status of Interrupt from MSS_TPCC_A.<br>Set only if Interupt is unmasked in MSS_TPCC_A_INTAGG_MASK<br>Wrie 0x1 to clear this interrupt. |
| 1   | MSS_TPCC_A_INTAGG_STATUS_TPCC_A_INT0 | R/W  | 0h    | Status of Interrupt from TPCC A<br>Set only if Interupt is unmasked in MSS_TPCC_A_INTAGG_MASK<br>Wrie 0x1 to clear this interrupt.      |
| 0   | MSS_TPCC_A_INTAGG_STATUS_TPCC_A_INTG | R/W  | 0h    | Status of Interrupt from MSS_TPCC_A.<br>Set only if Interupt is unmasked in MSS_TPCC_A_INTAGG_MASK<br>Wrie 0x1 to clear this interrupt. |

### 2.2.2.81 MSS\_CTRL\_MSS\_TPCC\_A\_INTAGG\_STATUS\_RAW Register

#### 1 MSS\_CTRL\_MSS\_TPCC\_A\_INTAGG\_STATUS\_RAW Register (Offset = 838h) [reset = 0h]

This register shows the Status of all Interrupts from TPCC0.

Return to [Summary Table](#)

**Table 2-243. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 0838h       |

**Figure 2-81. MSS\_CTRL\_MSS\_TPCC\_A\_INTAGG\_STATUS\_RAW Name Register**

|                                           |                                           |                                           |                                           |                                           |                                           |                                           |                                           |
|-------------------------------------------|-------------------------------------------|-------------------------------------------|-------------------------------------------|-------------------------------------------|-------------------------------------------|-------------------------------------------|-------------------------------------------|
| 31                                        | 30                                        | 29                                        | 28                                        | 27                                        | 26                                        | 25                                        | 24                                        |
| RESERVED                                  |                                           |                                           |                                           |                                           |                                           |                                           |                                           |
| NONE                                      |                                           |                                           |                                           |                                           |                                           |                                           |                                           |
| 0h                                        |                                           |                                           |                                           |                                           |                                           |                                           |                                           |
| 23                                        | 22                                        | 21                                        | 20                                        | 19                                        | 18                                        | 17                                        | 16                                        |
| RESERVED                                  |                                           |                                           |                                           |                                           |                                           | MSS_TPCC_A_INTAGG_STAT_US_RAW_TPTC_A1     | MSS_TPCC_A_INTAGG_STAT_US_RAW_TPTC_A0     |
| NONE                                      |                                           |                                           |                                           |                                           |                                           | R/W                                       | R/W                                       |
| 0h                                        |                                           |                                           |                                           |                                           |                                           | 0h                                        | 0h                                        |
| 15                                        | 14                                        | 13                                        | 12                                        | 11                                        | 10                                        | 9                                         | 8                                         |
| RESERVED                                  |                                           |                                           |                                           |                                           |                                           |                                           | MSS_TPCC_A_INTAGG_STAT_US_RAW_TPTC_A_INT7 |
| NONE                                      |                                           |                                           |                                           |                                           |                                           |                                           | R/W                                       |
| 0h                                        |                                           |                                           |                                           |                                           |                                           |                                           | 0h                                        |
| 7                                         | 6                                         | 5                                         | 4                                         | 3                                         | 2                                         | 1                                         | 0                                         |
| MSS_TPCC_A_INTAGG_STAT_US_RAW_TPTC_A_INT6 | MSS_TPCC_A_INTAGG_STAT_US_RAW_TPTC_A_INT5 | MSS_TPCC_A_INTAGG_STAT_US_RAW_TPTC_A_INT4 | MSS_TPCC_A_INTAGG_STAT_US_RAW_TPTC_A_INT3 | MSS_TPCC_A_INTAGG_STAT_US_RAW_TPTC_A_INT2 | MSS_TPCC_A_INTAGG_STAT_US_RAW_TPTC_A_INT1 | MSS_TPCC_A_INTAGG_STAT_US_RAW_TPTC_A_INT0 | MSS_TPCC_A_INTAGG_STAT_US_RAW_TPTC_A_INTG |
| R/W                                       | R/W                                       | R/W                                       | R/W                                       | R/W                                       | R/W                                       | R/W                                       | R/W                                       |
| 0h                                        | 0h                                        | 0h                                        | 0h                                        | 0h                                        | 0h                                        | 0h                                        | 0h                                        |

**Table 2-245. MSS\_CTRL\_MSS\_TPCC\_A\_INTAGG\_STATUS\_RAW Register Field Descriptions**

| Bit   | Field                                    | Type | Reset | Description                                                                                                                   |
|-------|------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                                 | NONE | 0h    | Reserved                                                                                                                      |
| 17    | MSS_TPCC_A_INTAGG_STATUS_RAW_TPTC_A1     | R/W  | 0h    | Raw Status of Interrupt from TPTC A1.<br>Set irrespective if the Interrupt is masked or unmasked in MSS_TPCC_A_INTAGG_MASK    |
| 16    | MSS_TPCC_A_INTAGG_STATUS_RAW_TPTC_A0     | R/W  | 0h    | Raw Status of Interrupt from TPTC A0.<br>Set irrespective if the Interrupt is masked or unmasked in MSS_TPCC_A_INTAGG_MASK    |
| 15:9  | RESERVED                                 | NONE | 0h    | Reserved                                                                                                                      |
| 8     | MSS_TPCC_A_INTAGG_STATUS_RAW_TPTC_A_INT7 | R/W  | 0h    | Raw Status of Interrupt from MSS_TPCC_A.<br>Set irrespective if the Interrupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK |
| 7     | MSS_TPCC_A_INTAGG_STATUS_RAW_TPTC_A_INT6 | R/W  | 0h    | Raw Status of Interrupt from MSS_TPCC_A.<br>Set irrespective if the Interrupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK |

**Table 2-245. MSS\_CTRL\_MSS\_TPCC\_A\_INTAGG\_STATUS\_RAW Register Field Descriptions (continued)**

| Bit | Field                                    | Type | Reset | Description                                                                                                                |
|-----|------------------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------|
| 6   | MSS_TPCC_A_INTAGG_STATUS_RAW_TPCC_A_INT5 | R/W  | 0h    | Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interrupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK |
| 5   | MSS_TPCC_A_INTAGG_STATUS_RAW_TPCC_A_INT4 | R/W  | 0h    | Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interrupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK |
| 4   | MSS_TPCC_A_INTAGG_STATUS_RAW_TPCC_A_INT3 | R/W  | 0h    | Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interrupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK |
| 3   | MSS_TPCC_A_INTAGG_STATUS_RAW_TPCC_A_INT2 | R/W  | 0h    | Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interrupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK |
| 2   | MSS_TPCC_A_INTAGG_STATUS_RAW_TPCC_A_INT1 | R/W  | 0h    | Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interrupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK |
| 1   | MSS_TPCC_A_INTAGG_STATUS_RAW_TPCC_A_INT0 | R/W  | 0h    | Raw Status of Interrupt from TPCC A. Set irrespective if the Interrupt is masked or unmasked in MSS_TPCC_A_INTAGG_MASK     |
| 0   | MSS_TPCC_A_INTAGG_STATUS_RAW_TPCC_A_INTG | R/W  | 0h    | Raw Status of Interrupt from MSS_TPCC_A. Set irrespective if the Interrupt is masked or unmasked in MSS_TPCC_C_INTAGG_MASK |

### 2.2.2.82 MSS\_CTRL\_LOCK0\_KICK0 Register

#### 1 MSS\_CTRL\_LOCK0\_KICK0 Register (Offset = 1008h) [reset = 0h]

- KICK0 component.

Return to [Summary Table](#)

**Table 2-246. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 1008h       |

**Figure 2-82. MSS\_CTRL\_LOCK0\_KICK0 Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| LOCK0_KICK0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LOCK0_KICK0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| LOCK0_KICK0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LOCK0_KICK0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 2-248. MSS\_CTRL\_LOCK0\_KICK0 Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description       |
|------|-------------|------|-------|-------------------|
| 31:0 | LOCK0_KICK0 | R/W  | 0h    | - KICK0 component |

### 2.2.2.83 MSS\_CTRL\_LOCK0\_KICK1 Register

#### 1 MSS\_CTRL\_LOCK0\_KICK1 Register (Offset = 100Ch) [reset = 0h]

- KICK1 component.

Return to [Summary Table](#)

**Table 2-249. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 100Ch       |

**Figure 2-83. MSS\_CTRL\_LOCK0\_KICK1 Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| LOCK0_KICK1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LOCK0_KICK1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| LOCK0_KICK1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LOCK0_KICK1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 2-251. MSS\_CTRL\_LOCK0\_KICK1 Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description       |
|------|-------------|------|-------|-------------------|
| 31:0 | LOCK0_KICK1 | R/W  | 0h    | - KICK1 component |

### 2.2.2.84 MSS\_CTRL\_INTR\_RAW\_STATUS Register

#### 1 MSS\_CTRL\_INTR\_RAW\_STATUS Register (Offset = 1010h) [reset = 0h]

Interrupt Raw Status/Set Register.

Return to [Summary Table](#)

**Table 2-252. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 1010h       |

**Figure 2-84. MSS\_CTRL\_INTR\_RAW\_STATUS Name Register**

|          |    |    |    |           |          |          |          |
|----------|----|----|----|-----------|----------|----------|----------|
| 31       | 30 | 29 | 28 | 27        | 26       | 25       | 24       |
| RESERVED |    |    |    |           |          |          |          |
| NONE     |    |    |    |           |          |          |          |
| 0h       |    |    |    |           |          |          |          |
| 23       | 22 | 21 | 20 | 19        | 18       | 17       | 16       |
| RESERVED |    |    |    |           |          |          |          |
| NONE     |    |    |    |           |          |          |          |
| 0h       |    |    |    |           |          |          |          |
| 15       | 14 | 13 | 12 | 11        | 10       | 9        | 8        |
| RESERVED |    |    |    |           |          |          |          |
| NONE     |    |    |    |           |          |          |          |
| 0h       |    |    |    |           |          |          |          |
| 7        | 6  | 5  | 4  | 3         | 2        | 1        | 0        |
| RESERVED |    |    |    | PROXY_ERR | KICK_ERR | ADDR_ERR | PROT_ERR |
| NONE     |    |    |    | R/W1TS    | R/W1TS   | R/W1TS   | R/W1TS   |
| 0h       |    |    |    | 0h        | 0h       | 0h       | 0h       |

**Table 2-254. MSS\_CTRL\_INTR\_RAW\_STATUS Register Field Descriptions**

| Bit  | Field     | Type   | Reset | Description                                                                                                |
|------|-----------|--------|-------|------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED  | NONE   | 0h    | Reserved                                                                                                   |
| 3    | PROXY_ERR | R/W1TS | 0h    | Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. |
| 2    | KICK_ERR  | R/W1TS | 0h    | Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.   |
| 1    | ADDR_ERR  | R/W1TS | 0h    | Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.    |
| 0    | PROT_ERR  | R/W1TS | 0h    | Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.    |

### 2.2.2.85 MSS\_CTRL\_INTR\_ENABLED\_STATUS\_CLEAR Register

#### 1 MSS\_CTRL\_INTR\_ENABLED\_STATUS\_CLEAR Register (Offset = 1014h) [reset = 0h]

Interrupt Enabled Status/Clear register.

Return to [Summary Table](#)

**Table 2-255. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 1014h       |

**Figure 2-85. MSS\_CTRL\_INTR\_ENABLED\_STATUS\_CLEAR Name Register**

|          |    |    |    |                   |                  |                  |                  |
|----------|----|----|----|-------------------|------------------|------------------|------------------|
| 31       | 30 | 29 | 28 | 27                | 26               | 25               | 24               |
| RESERVED |    |    |    |                   |                  |                  |                  |
| NONE     |    |    |    |                   |                  |                  |                  |
| 0h       |    |    |    |                   |                  |                  |                  |
| 23       | 22 | 21 | 20 | 19                | 18               | 17               | 16               |
| RESERVED |    |    |    |                   |                  |                  |                  |
| NONE     |    |    |    |                   |                  |                  |                  |
| 0h       |    |    |    |                   |                  |                  |                  |
| 15       | 14 | 13 | 12 | 11                | 10               | 9                | 8                |
| RESERVED |    |    |    |                   |                  |                  |                  |
| NONE     |    |    |    |                   |                  |                  |                  |
| 0h       |    |    |    |                   |                  |                  |                  |
| 7        | 6  | 5  | 4  | 3                 | 2                | 1                | 0                |
| RESERVED |    |    |    | ENABLED_PROXY_ERR | ENABLED_KICK_ERR | ENABLED_ADDR_ERR | ENABLED_PROT_ERR |
| NONE     |    |    |    | R/W1TC            | R/W1TC           | R/W1TC           | R/W1TC           |
| 0h       |    |    |    | 0h                | 0h               | 0h               | 0h               |

**Table 2-257. MSS\_CTRL\_INTR\_ENABLED\_STATUS\_CLEAR Register Field Descriptions**

| Bit  | Field             | Type   | Reset | Description                                                                                                      |
|------|-------------------|--------|-------|------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED          | NONE   | 0h    | Reserved                                                                                                         |
| 3    | ENABLED_PROXY_ERR | R/W1TC | 0h    | Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. |
| 2    | ENABLED_KICK_ERR  | R/W1TC | 0h    | Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.   |
| 1    | ENABLED_ADDR_ERR  | R/W1TC | 0h    | Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.    |
| 0    | ENABLED_PROT_ERR  | R/W1TC | 0h    | Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.    |

### 2.2.2.86 MSS\_CTRL\_INTR\_ENABLE Register

#### 1 MSS\_CTRL\_INTR\_ENABLE Register (Offset = 1018h) [reset = 0h]

Interrupt Enable register.

Return to [Summary Table](#)

**Table 2-258. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 1018h       |

**Figure 2-86. MSS\_CTRL\_INTR\_ENABLE Name Register**

|          |    |    |    |              |             |             |             |
|----------|----|----|----|--------------|-------------|-------------|-------------|
| 31       | 30 | 29 | 28 | 27           | 26          | 25          | 24          |
| RESERVED |    |    |    |              |             |             |             |
| NONE     |    |    |    |              |             |             |             |
| 0h       |    |    |    |              |             |             |             |
| 23       | 22 | 21 | 20 | 19           | 18          | 17          | 16          |
| RESERVED |    |    |    |              |             |             |             |
| NONE     |    |    |    |              |             |             |             |
| 0h       |    |    |    |              |             |             |             |
| 15       | 14 | 13 | 12 | 11           | 10          | 9           | 8           |
| RESERVED |    |    |    |              |             |             |             |
| NONE     |    |    |    |              |             |             |             |
| 0h       |    |    |    |              |             |             |             |
| 7        | 6  | 5  | 4  | 3            | 2           | 1           | 0           |
| RESERVED |    |    |    | PROXY_ERR_EN | KICK_ERR_EN | ADDR_ERR_EN | PROT_ERR_EN |
| NONE     |    |    |    | R/W1TS       | R/W1TS      | R/W1TS      | R/W1TS      |
| 0h       |    |    |    | 0h           | 0h          | 0h          | 0h          |

**Table 2-260. MSS\_CTRL\_INTR\_ENABLE Register Field Descriptions**

| Bit  | Field        | Type   | Reset | Description                                                                                   |
|------|--------------|--------|-------|-----------------------------------------------------------------------------------------------|
| 31:4 | RESERVED     | NONE   | 0h    | Reserved                                                                                      |
| 3    | PROXY_ERR_EN | R/W1TS | 0h    | Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. |
| 2    | KICK_ERR_EN  | R/W1TS | 0h    | Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.   |
| 1    | ADDR_ERR_EN  | R/W1TS | 0h    | Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.    |
| 0    | PROT_ERR_EN  | R/W1TS | 0h    | Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.    |



### 2.2.2.87 MSS\_CTRL\_INTR\_ENABLE\_CLEAR Register

#### 1 MSS\_CTRL\_INTR\_ENABLE\_CLEAR Register (Offset = 101Ch) [reset = 0h]

Interrupt Enable Clear register.

Return to [Summary Table](#)

**Table 2-261. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 101Ch       |

**Figure 2-87. MSS\_CTRL\_INTR\_ENABLE\_CLEAR Name Register**

|          |    |    |    |                  |                 |                 |                 |
|----------|----|----|----|------------------|-----------------|-----------------|-----------------|
| 31       | 30 | 29 | 28 | 27               | 26              | 25              | 24              |
| RESERVED |    |    |    |                  |                 |                 |                 |
| NONE     |    |    |    |                  |                 |                 |                 |
| 0h       |    |    |    |                  |                 |                 |                 |
| 23       | 22 | 21 | 20 | 19               | 18              | 17              | 16              |
| RESERVED |    |    |    |                  |                 |                 |                 |
| NONE     |    |    |    |                  |                 |                 |                 |
| 0h       |    |    |    |                  |                 |                 |                 |
| 15       | 14 | 13 | 12 | 11               | 10              | 9               | 8               |
| RESERVED |    |    |    |                  |                 |                 |                 |
| NONE     |    |    |    |                  |                 |                 |                 |
| 0h       |    |    |    |                  |                 |                 |                 |
| 7        | 6  | 5  | 4  | 3                | 2               | 1               | 0               |
| RESERVED |    |    |    | PROXY_ERR_EN_CLR | KICK_ERR_EN_CLR | ADDR_ERR_EN_CLR | PROT_ERR_EN_CLR |
| NONE     |    |    |    | R/W1TC           | R/W1TC          | R/W1TC          | R/W1TC          |
| 0h       |    |    |    | 0h               | 0h              | 0h              | 0h              |

**Table 2-263. MSS\_CTRL\_INTR\_ENABLE\_CLEAR Register Field Descriptions**

| Bit  | Field            | Type   | Reset | Description                                                                                           |
|------|------------------|--------|-------|-------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED         | NONE   | 0h    | Reserved                                                                                              |
| 3    | PROXY_ERR_EN_CLR | R/W1TC | 0h    | Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. |
| 2    | KICK_ERR_EN_CLR  | R/W1TC | 0h    | Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.   |
| 1    | ADDR_ERR_EN_CLR  | R/W1TC | 0h    | Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.    |
| 0    | PROT_ERR_EN_CLR  | R/W1TC | 0h    | Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.    |

### 2.2.2.88 MSS\_CTRL\_EOI Register

#### 1 MSS\_CTRL\_EOI Register (Offset = 1020h) [reset = 0h]

EOI register.

Return to [Summary Table](#)

**Table 2-264. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 1020h       |

**Figure 2-88. MSS\_CTRL\_EOI Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| EOI_VECTOR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 2-266. MSS\_CTRL\_EOI Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                 |
|------|------------|------|-------|-----------------------------------------------------------------------------|
| 31:8 | RESERVED   | NONE | 0h    | Reserved                                                                    |
| 7:0  | EOI_VECTOR | R/W  | 0h    | EOI vector value. Write this with interrupt distribution value in the chip. |

### 2.2.2.89 MSS\_CTRL\_FAULT\_ADDRESS Register

#### 1 MSS\_CTRL\_FAULT\_ADDRESS Register (Offset = 1024h) [reset = 0h]

Fault Address register.

Return to [Summary Table](#)

**Table 2-267. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 1024h       |

**Figure 2-89. MSS\_CTRL\_FAULT\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 2-269. MSS\_CTRL\_FAULT\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description    |
|------|------------|------|-------|----------------|
| 31:0 | FAULT_ADDR | R    | 0h    | Fault Address. |

### 2.2.2.90 MSS\_CTRL\_FAULT\_TYPE\_STATUS Register

#### 1 MSS\_CTRL\_FAULT\_TYPE\_STATUS Register (Offset = 1028h) [reset = 0h]

Fault Type Status register.

Return to [Summary Table](#)

**Table 2-270. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 1028h       |

**Figure 2-90. MSS\_CTRL\_FAULT\_TYPE\_STATUS Name Register**

|          |          |            |    |    |    |    |    |
|----------|----------|------------|----|----|----|----|----|
| 31       | 30       | 29         | 28 | 27 | 26 | 25 | 24 |
| RESERVED |          |            |    |    |    |    |    |
| NONE     |          |            |    |    |    |    |    |
| 0h       |          |            |    |    |    |    |    |
| 23       | 22       | 21         | 20 | 19 | 18 | 17 | 16 |
| RESERVED |          |            |    |    |    |    |    |
| NONE     |          |            |    |    |    |    |    |
| 0h       |          |            |    |    |    |    |    |
| 15       | 14       | 13         | 12 | 11 | 10 | 9  | 8  |
| RESERVED |          |            |    |    |    |    |    |
| NONE     |          |            |    |    |    |    |    |
| 0h       |          |            |    |    |    |    |    |
| 7        | 6        | 5          | 4  | 3  | 2  | 1  | 0  |
| RESERVED | FAULT_NS | FAULT_TYPE |    |    |    |    |    |
| NONE     | R        | R          |    |    |    |    |    |
| 0h       | 0h       | 0h         |    |    |    |    |    |

**Table 2-272. MSS\_CTRL\_FAULT\_TYPE\_STATUS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                         |
|------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                            |
| 6    | FAULT_NS   | R    | 0h    | Non-secure access.                                                                                                                                                                                                                                                                                                                                                                                  |
| 5:0  | FAULT_TYPE | R    | 0h    | Fault Type<br>10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1<br>01_0000 = Supervisor write fault - priv = 1 dir = 0<br>00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1<br>00_0100 = User read fault - priv = 0 dir = 1 dtype = 1<br>00_0010 = User write fault - priv = 0 dir = 0<br>00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1<br>00_0000 = No fault |

### 2.2.2.91 MSS\_CTRL\_FAULT\_ATTR\_STATUS Register

#### 1 MSS\_CTRL\_FAULT\_ATTR\_STATUS Register (Offset = 102Ch) [reset = 0h]

Fault Attribute Status register.

Return to [Summary Table](#)

**Table 2-273. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 102Ch       |

**Figure 2-91. MSS\_CTRL\_FAULT\_ATTR\_STATUS Name Register**

|               |    |    |    |               |    |    |    |
|---------------|----|----|----|---------------|----|----|----|
| 31            | 30 | 29 | 28 | 27            | 26 | 25 | 24 |
| FAULT_XID     |    |    |    |               |    |    |    |
| R             |    |    |    |               |    |    |    |
| 0h            |    |    |    |               |    |    |    |
| 23            | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
| FAULT_XID     |    |    |    | FAULT_ROUTEID |    |    |    |
| R             |    |    |    | R             |    |    |    |
| 0h            |    |    |    | 0h            |    |    |    |
| 15            | 14 | 13 | 12 | 11            | 10 | 9  | 8  |
| FAULT_ROUTEID |    |    |    |               |    |    |    |
| R             |    |    |    |               |    |    |    |
| 0h            |    |    |    |               |    |    |    |
| 7             | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| FAULT_PRIVID  |    |    |    |               |    |    |    |
| R             |    |    |    |               |    |    |    |
| 0h            |    |    |    |               |    |    |    |

**Table 2-275. MSS\_CTRL\_FAULT\_ATTR\_STATUS Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description   |
|-------|---------------|------|-------|---------------|
| 31:20 | FAULT_XID     | R    | 0h    | XID.          |
| 19:8  | FAULT_ROUTEID | R    | 0h    | Route ID.     |
| 7:0   | FAULT_PRIVID  | R    | 0h    | Privilege ID. |

### 2.2.2.92 MSS\_CTRL\_FAULT\_CLEAR Register

#### 1 MSS\_CTRL\_FAULT\_CLEAR Register (Offset = 1030h) [reset = 0h]

Fault Clear register.

Return to [Summary Table](#)

**Table 2-276. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 1030h       |

**Figure 2-92. MSS\_CTRL\_FAULT\_CLEAR Name Register**

|          |    |    |    |    |    |    |           |
|----------|----|----|----|----|----|----|-----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24        |
| RESERVED |    |    |    |    |    |    |           |
| NONE     |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16        |
| RESERVED |    |    |    |    |    |    |           |
| NONE     |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8         |
| RESERVED |    |    |    |    |    |    |           |
| NONE     |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0         |
| RESERVED |    |    |    |    |    |    | FAULT_CLR |
| NONE     |    |    |    |    |    |    | W         |
| 0h       |    |    |    |    |    |    | 0h        |

**Table 2-278. MSS\_CTRL\_FAULT\_CLEAR Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                   |
|------|-----------|------|-------|-------------------------------------------------------------------------------|
| 31:1 | RESERVED  | NONE | 0h    | Reserved                                                                      |
| 0    | FAULT_CLR | W    | 0h    | Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. |

### 2.2.2.93 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_MBOX\_WRITE\_DONE Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_MBOX\_WRITE\_DONE Register (Offset = 4000h) [reset = 0h]

This register is used by R5SS0 Core 0 to generate Mailbox interrupt to Recipient CPU.

Return to [Summary Table](#)

**Table 2-279. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 4000h       |

**Figure 2-93. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_MBOX\_WRITE\_DONE Name Register**

| 31       | 30 | 29 | 28                               | 27       | 26 | 25 | 24                               |
|----------|----|----|----------------------------------|----------|----|----|----------------------------------|
| RESERVED |    |    | MSS_CR5A0_MBOX_WRITE_DONE_PROC_7 | RESERVED |    |    | MSS_CR5A0_MBOX_WRITE_DONE_PROC_6 |
| NONE     |    |    | R/W                              | NONE     |    |    | R/W                              |
| 0h       |    |    | 0h                               | 0h       |    |    | 0h                               |
| 23       | 22 | 21 | 20                               | 19       | 18 | 17 | 16                               |
| RESERVED |    |    | MSS_CR5A0_MBOX_WRITE_DONE_PROC_5 | RESERVED |    |    | MSS_CR5A0_MBOX_WRITE_DONE_PROC_4 |
| NONE     |    |    | R/W                              | NONE     |    |    | R/W                              |
| 0h       |    |    | 0h                               | 0h       |    |    | 0h                               |
| 15       | 14 | 13 | 12                               | 11       | 10 | 9  | 8                                |
| RESERVED |    |    | MSS_CR5A0_MBOX_WRITE_DONE_PROC_3 | RESERVED |    |    | MSS_CR5A0_MBOX_WRITE_DONE_PROC_2 |
| NONE     |    |    | R/W                              | NONE     |    |    | R/W                              |
| 0h       |    |    | 0h                               | 0h       |    |    | 0h                               |
| 7        | 6  | 5  | 4                                | 3        | 2  | 1  | 0                                |
| RESERVED |    |    | MSS_CR5A0_MBOX_WRITE_DONE_PROC_1 | RESERVED |    |    | MSS_CR5A0_MBOX_WRITE_DONE_PROC_0 |
| NONE     |    |    | R/W                              | NONE     |    |    | R/W                              |
| 0h       |    |    | 0h                               | 0h       |    |    | 0h                               |

**Table 2-281. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_MBOX\_WRITE\_DONE Register Field Descriptions**

| Bit   | Field                            | Type | Reset | Description                                                                                                             |
|-------|----------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 28    | MSS_CR5A0_MBOX_WRITE_DONE_PROC_7 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 7 |
| 27:25 | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 24    | MSS_CR5A0_MBOX_WRITE_DONE_PROC_6 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 6 |
| 23:21 | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 20    | MSS_CR5A0_MBOX_WRITE_DONE_PROC_5 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 5 |

**Table 2-281. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_MBOX\_WRITE\_DONE Register Field Descriptions  
(continued)**

| Bit   | Field                            | Type | Reset | Description                                                                                                             |
|-------|----------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------|
| 19:17 | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 16    | MSS_CR5A0_MBOX_WRITE_DONE_PROC_4 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 4 |
| 15:13 | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 12    | MSS_CR5A0_MBOX_WRITE_DONE_PROC_3 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 3 |
| 11:9  | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 8     | MSS_CR5A0_MBOX_WRITE_DONE_PROC_2 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 2 |
| 7:5   | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 4     | MSS_CR5A0_MBOX_WRITE_DONE_PROC_1 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 1 |
| 3:1   | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 0     | MSS_CR5A0_MBOX_WRITE_DONE_PROC_0 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 0 |



### 2.2.2.94 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_MBOX\_READ\_REQ Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_MBOX\_READ\_REQ Register (Offset = 4004h) [reset = 0h]

This register is used by R5SS0 Core 0 to know the Sender of Mailbox Interrupt as well as clear it.

Return to [Summary Table](#)

**Table 2-282. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 4004h       |

**Figure 2-94. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_MBOX\_READ\_REQ Name Register**

| 31       | 30 | 29 | 28                             | 27       | 26 | 25 | 24                             |
|----------|----|----|--------------------------------|----------|----|----|--------------------------------|
| RESERVED |    |    | MSS_CR5A0_MBOX_READ_REQ_PROC_7 | RESERVED |    |    | MSS_CR5A0_MBOX_READ_REQ_PROC_6 |
| NONE     |    |    | R/W                            | NONE     |    |    | R/W                            |
| 0h       |    |    | 0h                             | 0h       |    |    | 0h                             |
| 23       | 22 | 21 | 20                             | 19       | 18 | 17 | 16                             |
| RESERVED |    |    | MSS_CR5A0_MBOX_READ_REQ_PROC_5 | RESERVED |    |    | MSS_CR5A0_MBOX_READ_REQ_PROC_4 |
| NONE     |    |    | R/W                            | NONE     |    |    | R/W                            |
| 0h       |    |    | 0h                             | 0h       |    |    | 0h                             |
| 15       | 14 | 13 | 12                             | 11       | 10 | 9  | 8                              |
| RESERVED |    |    | MSS_CR5A0_MBOX_READ_REQ_PROC_3 | RESERVED |    |    | MSS_CR5A0_MBOX_READ_REQ_PROC_2 |
| NONE     |    |    | R/W                            | NONE     |    |    | R/W                            |
| 0h       |    |    | 0h                             | 0h       |    |    | 0h                             |
| 7        | 6  | 5  | 4                              | 3        | 2  | 1  | 0                              |
| RESERVED |    |    | MSS_CR5A0_MBOX_READ_REQ_PROC_1 | RESERVED |    |    | MSS_CR5A0_MBOX_READ_REQ_PROC_0 |
| NONE     |    |    | R/W                            | NONE     |    |    | R/W                            |
| 0h       |    |    | 0h                             | 0h       |    |    | 0h                             |

**Table 2-284. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_MBOX\_READ\_REQ Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                       |
|-------|--------------------------------|------|-------|-----------------------------------------------------------------------------------|
| 31:29 | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 28    | MSS_CR5A0_MBOX_READ_REQ_PROC_7 | R/W  | 0h    | This is request from processor 7 to mss_cr5a. Requesting it to read from mailbox. |
| 27:25 | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 24    | MSS_CR5A0_MBOX_READ_REQ_PROC_6 | R/W  | 0h    | This is request from processor 6 to mss_cr5a. Requesting it to read from mailbox. |
| 23:21 | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 20    | MSS_CR5A0_MBOX_READ_REQ_PROC_5 | R/W  | 0h    | This is request from processor 5 to mss_cr5a. Requesting it to read from mailbox. |
| 19:17 | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 16    | MSS_CR5A0_MBOX_READ_REQ_PROC_4 | R/W  | 0h    | This is request from processor 4 to mss_cr5a. Requesting it to read from mailbox. |
| 15:13 | RESERVED                       | NONE | 0h    | Reserved                                                                          |

**Table 2-284. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_MBOX\_READ\_REQ Register Field Descriptions  
(continued)**

| Bit  | Field                          | Type | Reset | Description                                                                       |
|------|--------------------------------|------|-------|-----------------------------------------------------------------------------------|
| 12   | MSS_CR5A0_MBOX_READ_REQ_PROC_3 | R/W  | 0h    | This is request from processor 3 to mss_cr5a. Requesting it to read from mailbox. |
| 11:9 | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 8    | MSS_CR5A0_MBOX_READ_REQ_PROC_2 | R/W  | 0h    | This is request from processor 2 to mss_cr5a. Requesting it to read from mailbox. |
| 7:5  | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 4    | MSS_CR5A0_MBOX_READ_REQ_PROC_1 | R/W  | 0h    | This is request from processor 1 to mss_cr5a. Requesting it to read from mailbox. |
| 3:1  | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 0    | MSS_CR5A0_MBOX_READ_REQ_PROC_0 | R/W  | 0h    | This is request from processor 0 to mss_cr5a. Requesting it to read from mailbox. |

### 2.2.2.95 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_MBOX\_READ\_DONE\_ACK Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_MBOX\_READ\_DONE\_ACK Register (Offset = 4008h) [reset = 0h]

This register is used by R5SS0 Core 0 to generate Mailbox Read acknowledgement to the Sender CPU.

Return to [Summary Table](#)

**Table 2-285. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 4008h       |

**Figure 2-95. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_MBOX\_READ\_DONE\_ACK Name Register**

|                                   |    |    |    |    |    |    |    |
|-----------------------------------|----|----|----|----|----|----|----|
| 31                                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                          |    |    |    |    |    |    |    |
| NONE                              |    |    |    |    |    |    |    |
| 0h                                |    |    |    |    |    |    |    |
| 23                                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                          |    |    |    |    |    |    |    |
| NONE                              |    |    |    |    |    |    |    |
| 0h                                |    |    |    |    |    |    |    |
| 15                                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED                          |    |    |    |    |    |    |    |
| NONE                              |    |    |    |    |    |    |    |
| 0h                                |    |    |    |    |    |    |    |
| 7                                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A0_MBOX_READ_DONE_ACK_PROC |    |    |    |    |    |    |    |
| R/W                               |    |    |    |    |    |    |    |
| 0h                                |    |    |    |    |    |    |    |

**Table 2-287. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_MBOX\_READ\_DONE\_ACK Register Field Descriptions**

| Bit  | Field                             | Type | Reset | Description                                                                                                            |
|------|-----------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED                          | NONE | 0h    | Reserved                                                                                                               |
| 7:0  | MSS_CR5A0_MBOX_READ_DONE_ACK_PROC | R/W  | 0h    | Write pulse bit field:<br>For bits 0 to 7: Writing 1'b1 : Generates pulse interrupt to corresponding proc from MSS_CR5 |

### 2.2.2.96 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_MBOX\_READ\_DONE Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_MBOX\_READ\_DONE Register (Offset = 400Ch) [reset = 0h]

This register is used by R5SS0 Core 0 to know that the Receiver CPU has read the Mailbox and Acked. It is also used to clear the Read Done Interrupt.

Return to [Summary Table](#)

**Table 2-288. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 400Ch       |

**Figure 2-96. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_MBOX\_READ\_DONE Name Register**

| 31       | 30 | 29 | 28                              | 27       | 26 | 25 | 24                              |
|----------|----|----|---------------------------------|----------|----|----|---------------------------------|
| RESERVED |    |    | MSS_CR5A0_MBOX_READ_DONE_PROC_7 | RESERVED |    |    | MSS_CR5A0_MBOX_READ_DONE_PROC_6 |
| NONE     |    |    | R/W                             | NONE     |    |    | R/W                             |
| 0h       |    |    | 0h                              | 0h       |    |    | 0h                              |
| 23       | 22 | 21 | 20                              | 19       | 18 | 17 | 16                              |
| RESERVED |    |    | MSS_CR5A0_MBOX_READ_DONE_PROC_5 | RESERVED |    |    | MSS_CR5A0_MBOX_READ_DONE_PROC_4 |
| NONE     |    |    | R/W                             | NONE     |    |    | R/W                             |
| 0h       |    |    | 0h                              | 0h       |    |    | 0h                              |
| 15       | 14 | 13 | 12                              | 11       | 10 | 9  | 8                               |
| RESERVED |    |    | MSS_CR5A0_MBOX_READ_DONE_PROC_3 | RESERVED |    |    | MSS_CR5A0_MBOX_READ_DONE_PROC_2 |
| NONE     |    |    | R/W                             | NONE     |    |    | R/W                             |
| 0h       |    |    | 0h                              | 0h       |    |    | 0h                              |
| 7        | 6  | 5  | 4                               | 3        | 2  | 1  | 0                               |
| RESERVED |    |    | MSS_CR5A0_MBOX_READ_DONE_PROC_1 | RESERVED |    |    | MSS_CR5A0_MBOX_READ_DONE_PROC_0 |
| NONE     |    |    | R/W                             | NONE     |    |    | R/W                             |
| 0h       |    |    | 0h                              | 0h       |    |    | 0h                              |

**Table 2-290. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_MBOX\_READ\_DONE Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                 |
|-------|---------------------------------|------|-------|---------------------------------------------------------------------------------------------|
| 31:29 | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 28    | MSS_CR5A0_MBOX_READ_DONE_PROC_7 | R/W  | 0h    | This register should be written once finishing Reading from proc7's mailbox written by CR5A |
| 27:25 | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 24    | MSS_CR5A0_MBOX_READ_DONE_PROC_6 | R/W  | 0h    | This register should be written once finishing Reading from proc6's mailbox written by CR5A |
| 23:21 | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 20    | MSS_CR5A0_MBOX_READ_DONE_PROC_5 | R/W  | 0h    | This register should be written once finishing Reading from proc5's mailbox written by CR5A |
| 19:17 | RESERVED                        | NONE | 0h    | Reserved                                                                                    |

**Table 2-290. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_MBOX\_READ\_DONE Register Field Descriptions  
(continued)**

| Bit   | Field                           | Type | Reset | Description                                                                                 |
|-------|---------------------------------|------|-------|---------------------------------------------------------------------------------------------|
| 16    | MSS_CR5A0_MBOX_READ_DONE_PROC_4 | R/W  | 0h    | This register should be written once finishing Reading from proc4's mailbox written by CR5A |
| 15:13 | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 12    | MSS_CR5A0_MBOX_READ_DONE_PROC_3 | R/W  | 0h    | This register should be written once finishing Reading from proc3's mailbox written by CR5A |
| 11:9  | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 8     | MSS_CR5A0_MBOX_READ_DONE_PROC_2 | R/W  | 0h    | This register should be written once finishing Reading from proc2's mailbox written by CR5A |
| 7:5   | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 4     | MSS_CR5A0_MBOX_READ_DONE_PROC_1 | R/W  | 0h    | This register should be written once finishing Reading from proc1's mailbox written by CR5A |
| 3:1   | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 0     | MSS_CR5A0_MBOX_READ_DONE_PROC_0 | R/W  | 0h    | This register should be written once finishing Reading from proc0's mailbox written by CR5A |

### 2.2.2.97 MSS\_CTRL\_MSS\_SW\_INT\_R5SS0\_CORE0 Register

#### 1 MSS\_CTRL\_MSS\_SW\_INT\_R5SS0\_CORE0 Register (Offset = 4010h) [reset = 0h]

This Register is used to generate a S/W Triggered Interrupt to R5SS0 Core0.

Return to [Summary Table](#)

**Table 2-291. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 4010h       |

**Figure 2-97. MSS\_CTRL\_MSS\_SW\_INT\_R5SS0\_CORE0 Name Register**

|          |    |    |    |    |    |    |                              |
|----------|----|----|----|----|----|----|------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                           |
| RESERVED |    |    |    |    |    |    |                              |
| NONE     |    |    |    |    |    |    |                              |
| 0h       |    |    |    |    |    |    |                              |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                           |
| RESERVED |    |    |    |    |    |    |                              |
| NONE     |    |    |    |    |    |    |                              |
| 0h       |    |    |    |    |    |    |                              |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                            |
| RESERVED |    |    |    |    |    |    |                              |
| NONE     |    |    |    |    |    |    |                              |
| 0h       |    |    |    |    |    |    |                              |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                            |
| RESERVED |    |    |    |    |    |    | MSS_SW_INT_R5SS0_CORE0_PULSE |
| NONE     |    |    |    |    |    |    | R/W                          |
| 0h       |    |    |    |    |    |    | 0h                           |

**Table 2-293. MSS\_CTRL\_MSS\_SW\_INT\_R5SS0\_CORE0 Register Field Descriptions**

| Bit  | Field                        | Type | Reset | Description                                                                                                        |
|------|------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED                     | NONE | 0h    | Reserved                                                                                                           |
| 0    | MSS_SW_INT_R5SS0_CORE0_PULSE | R/W  | 0h    | Write_pulse bit field:<br>Writing 1'b1 to each bit will trigger MSS_SW_INT respectively to corresponding R5SS core |

### 2.2.2.98 MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG0\_MASK Register

#### 1 MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG0\_MASK Register (Offset = 4020h) [reset = 0h]

This register Masks selected interrupt sources from generating MPU Address Error Interrupt to R5SS0 CORE0 .

Return to [Summary Table](#)

**Table 2-294. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 4020h       |

**Figure 2-98. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG0\_MASK Name Register**

| 31                                                  | 30                                                  | 29                                                  | 28                                                   | 27                                                   | 26                                                 | 25                                                 | 24                                                 |
|-----------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|------------------------------------------------------|------------------------------------------------------|----------------------------------------------------|----------------------------------------------------|----------------------------------------------------|
| RESERVED                                            |                                                     |                                                     |                                                      |                                                      |                                                    |                                                    |                                                    |
| NONE                                                |                                                     |                                                     |                                                      |                                                      |                                                    |                                                    |                                                    |
| 0h                                                  |                                                     |                                                     |                                                      |                                                      |                                                    |                                                    |                                                    |
| 23                                                  | 22                                                  | 21                                                  | 20                                                   | 19                                                   | 18                                                 | 17                                                 | 16                                                 |
| RESERVED                                            |                                                     |                                                     |                                                      |                                                      |                                                    | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_HSM_ADDR_ERR0       | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_CR5B1_AHB_ADDR_ERR0 |
| NONE                                                |                                                     |                                                     |                                                      |                                                      |                                                    | R/W                                                | R/W                                                |
| 0h                                                  |                                                     |                                                     |                                                      |                                                      |                                                    | 0h                                                 | 0h                                                 |
| 15                                                  | 14                                                  | 13                                                  | 12                                                   | 11                                                   | 10                                                 | 9                                                  | 8                                                  |
| MPU_ADDR_INTR_ERRAGG0_MASK_MPU_CR5A1_AHB_ADDR_ERR0  | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_CR5B0_AHB_ADDR_ERR0  | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_CR5A0_AHB_ADDR_ERR0  | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_SCRM2SCRIP1_ADDR_ERR0 | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_SCRM2SCRIP0_ADDR_ERR0 | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_QSPI_ADDR_ERR0      | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_MBOX_ADDR_ERR0      | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_DTHE_A_ADDR_ERR0    |
| R/W                                                 | R/W                                                 | R/W                                                 | R/W                                                  | R/W                                                  | R/W                                                | R/W                                                | R/W                                                |
| 0h                                                  | 0h                                                  | 0h                                                  | 0h                                                   | 0h                                                   | 0h                                                 | 0h                                                 | 0h                                                 |
| 7                                                   | 6                                                   | 5                                                   | 4                                                    | 3                                                    | 2                                                  | 1                                                  | 0                                                  |
| MPU_ADDR_INTR_ERRAGG0_MASK_MPU_CR5B1_AXIS_ADDR_ERR0 | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_CR5A1_AXIS_ADDR_ERR0 | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_CR5B0_AXIS_ADDR_ERR0 | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_CR5A0_AXIS_ADDR_ERR0  | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_L2_BANK_D_ADDR_ERR0   | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_L2_BANK_C_ADDR_ERR0 | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_L2_BANK_B_ADDR_ERR0 | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_L2_BANK_A_ADDR_ERR0 |
| R/W                                                 | R/W                                                 | R/W                                                 | R/W                                                  | R/W                                                  | R/W                                                | R/W                                                | R/W                                                |
| 0h                                                  | 0h                                                  | 0h                                                  | 0h                                                   | 0h                                                   | 0h                                                 | 0h                                                 | 0h                                                 |

**Table 2-296. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG0\_MASK Register Field Descriptions**

| Bit   | Field                                              | Type | Reset | Description                                                                                                                  |
|-------|----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                                           | NONE | 0h    | Reserved                                                                                                                     |
| 17    | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_HSM_ADDR_ERR0       | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 16    | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_CR5B1_AHB_ADDR_ERR0 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 15    | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_CR5A1_AHB_ADDR_ERR0 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |

**Table 2-296. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG0\_MASK Register Field Descriptions (continued)**

| Bit | Field                                               | Type | Reset | Description                                                                                                                  |
|-----|-----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 14  | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_CR5B0_AHB_ADDR_ERR0  | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 13  | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_CR5A0_AHB_ADDR_ERR0  | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 12  | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_SCRM2SCR1_ADDR_ERR0  | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 11  | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_SCRM2SCR0_ADDR_ERR0  | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 10  | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_QSPI_ADDR_ERR0       | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 9   | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_MBOX_ADDR_ERR0       | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 8   | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_DTHEA_ADDR_ERR0      | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 7   | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_CR5B1_AXIS_ADDR_ERR0 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 6   | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_CR5A1_AXIS_ADDR_ERR0 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 5   | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_CR5B0_AXIS_ADDR_ERR0 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 4   | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_CR5A0_AXIS_ADDR_ERR0 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 3   | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_L2_BA NK_D_ADDR_ERR0 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 2   | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_L2_BA NK_C_ADDR_ERR0 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 1   | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_L2_BA NK_B_ADDR_ERR0 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |



**Table 2-296. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG0\_MASK Register Field Descriptions (continued)**

| Bit | Field                                              | Type | Reset | Description                                                                                                                  |
|-----|----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 0   | MPU_ADDR_INTR_ERRAGG0_MASK_MPU_L2_BANK_A_ADDR_ERR0 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |

### 2.2.2.99 MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG0\_STATUS Register

#### 1 MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG0\_STATUS Register (Offset = 4024h) [reset = 0h]

This register shows the Status of Unmasked MPU Address Errors to R5SS0 Core0 .

Return to [Summary Table](#)

**Table 2-297. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 4024h       |

**Figure 2-99. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG0\_STATUS Name Register**

|                                                       |                                                       |                                                       |                                                        |                                                        |                                                      |                                                      |                                                      |
|-------------------------------------------------------|-------------------------------------------------------|-------------------------------------------------------|--------------------------------------------------------|--------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|
| 31                                                    | 30                                                    | 29                                                    | 28                                                     | 27                                                     | 26                                                   | 25                                                   | 24                                                   |
| RESERVED                                              |                                                       |                                                       |                                                        |                                                        |                                                      |                                                      |                                                      |
| NONE                                                  |                                                       |                                                       |                                                        |                                                        |                                                      |                                                      |                                                      |
| 0h                                                    |                                                       |                                                       |                                                        |                                                        |                                                      |                                                      |                                                      |
| 23                                                    | 22                                                    | 21                                                    | 20                                                     | 19                                                     | 18                                                   | 17                                                   | 16                                                   |
| RESERVED                                              |                                                       |                                                       |                                                        |                                                        |                                                      | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_HSM_ADDR_ERR0       | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_CR5B1_AHB_ADDR_ERR0 |
| NONE                                                  |                                                       |                                                       |                                                        |                                                        |                                                      | R/W                                                  | R/W                                                  |
| 0h                                                    |                                                       |                                                       |                                                        |                                                        |                                                      | 0h                                                   | 0h                                                   |
| 15                                                    | 14                                                    | 13                                                    | 12                                                     | 11                                                     | 10                                                   | 9                                                    | 8                                                    |
| MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_CR5A1_AHB_ADDR_ERR0  | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_CR5B0_AHB_ADDR_ERR0  | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_CR5A0_AHB_ADDR_ERR0  | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_SCRM2SCRIP1_ADDR_ERR0 | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_SCRM2SCRIP0_ADDR_ERR0 | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_QSPI_ADDR_ERR0      | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_MBOX_ADDR_ERR0      | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_DTHE_A_ADDR_ERR0    |
| R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                    | R/W                                                    | R/W                                                  | R/W                                                  | R/W                                                  |
| 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                     | 0h                                                     | 0h                                                   | 0h                                                   | 0h                                                   |
| 7                                                     | 6                                                     | 5                                                     | 4                                                      | 3                                                      | 2                                                    | 1                                                    | 0                                                    |
| MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_CR5B1_AXIS_ADDR_ERR0 | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_CR5A1_AXIS_ADDR_ERR0 | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_CR5B0_AXIS_ADDR_ERR0 | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_CR5A0_AXIS_ADDR_ERR0  | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_L2_BANK_D_ADDR_ERR0   | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_L2_BANK_C_ADDR_ERR0 | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_L2_BANK_B_ADDR_ERR0 | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_L2_BANK_A_ADDR_ERR0 |
| R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                    | R/W                                                    | R/W                                                  | R/W                                                  | R/W                                                  |
| 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                     | 0h                                                     | 0h                                                   | 0h                                                   | 0h                                                   |

**Table 2-299. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG0\_STATUS Register Field Descriptions**

| Bit   | Field                                                | Type | Reset | Description                                                                                                                        |
|-------|------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                                             | NONE | 0h    | Reserved                                                                                                                           |
| 17    | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_HSM_ADDR_ERR0       | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 16    | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_CR5B1_AHB_ADDR_ERR0 | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 15    | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_CR5A1_AHB_ADDR_ERR0 | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |

**Table 2-299. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG0\_STATUS Register Field Descriptions (continued)**

| Bit | Field                                                 | Type | Reset | Description                                                                                                                        |
|-----|-------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 14  | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_CR5B0_AHB_ADDR_ERR0  | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 13  | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_CR5A0_AHB_ADDR_ERR0  | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 12  | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_SCRM2SCR1_ADDR_ERR0  | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 11  | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_SCRM2SCR0_ADDR_ERR0  | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 10  | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_QSPI_ADDR_ERR0       | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 9   | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_MBOX_ADDR_ERR0       | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 8   | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_DTHE_A_ADDR_ERR0     | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 7   | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_CR5B1_AXIS_ADDR_ERR0 | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 6   | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_CR5A1_AXIS_ADDR_ERR0 | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 5   | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_CR5B0_AXIS_ADDR_ERR0 | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 4   | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_CR5A0_AXIS_ADDR_ERR0 | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 3   | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_L2BANK_D_ADDR_ERR0   | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 2   | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_L2BANK_C_ADDR_ERR0   | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 1   | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_L2BANK_B_ADDR_ERR0   | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |

**Table 2-299. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG0\_STATUS Register Field Descriptions (continued)**

| Bit | Field                                                | Type | Reset | Description                                                                                                                             |
|-----|------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 0   | MPU_ADDR_INTR_ERRAGG0_STATUS_MPU_L2_BANK_A_ADDR_ERR0 | R/W  | 0h    | Status of Error from MPU_ADDR_INTR.<br>Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK<br>Write 0x1 to clear this Error. |

### 2.2.2.100 MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG0\_STATUS\_RAW Register

#### 1 MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG0\_STATUS\_RAW Register (Offset = 4028h) [reset = 0h]

This register shows the Status of all MPU Address Errors.

Return to [Summary Table](#)

**Table 2-300. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 4028h       |

**Figure 2-100. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG0\_STATUS\_RAW Name Register**

|                                                           |                                                           |                                                           |                                                            |                                                            |                                                          |                                                          |                                                          |
|-----------------------------------------------------------|-----------------------------------------------------------|-----------------------------------------------------------|------------------------------------------------------------|------------------------------------------------------------|----------------------------------------------------------|----------------------------------------------------------|----------------------------------------------------------|
| 31                                                        | 30                                                        | 29                                                        | 28                                                         | 27                                                         | 26                                                       | 25                                                       | 24                                                       |
| RESERVED                                                  |                                                           |                                                           |                                                            |                                                            |                                                          |                                                          |                                                          |
| NONE                                                      |                                                           |                                                           |                                                            |                                                            |                                                          |                                                          |                                                          |
| 0h                                                        |                                                           |                                                           |                                                            |                                                            |                                                          |                                                          |                                                          |
| 23                                                        | 22                                                        | 21                                                        | 20                                                         | 19                                                         | 18                                                       | 17                                                       | 16                                                       |
| RESERVED                                                  |                                                           |                                                           |                                                            |                                                            |                                                          | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_HSM_A_DDR_ERR0      | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_CR5B1_AHB_ADDR_ERR0 |
| NONE                                                      |                                                           |                                                           |                                                            |                                                            |                                                          | R/W                                                      | R/W                                                      |
| 0h                                                        |                                                           |                                                           |                                                            |                                                            |                                                          | 0h                                                       | 0h                                                       |
| 15                                                        | 14                                                        | 13                                                        | 12                                                         | 11                                                         | 10                                                       | 9                                                        | 8                                                        |
| MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_CR5A1_AHB_ADDR_ERR0  | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_CR5B0_AHB_ADDR_ERR0  | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_CR5A0_AHB_ADDR_ERR0  | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_SCRM2_SCRP1_ADDR_ERR0 | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_SCRM2_SCRP0_ADDR_ERR0 | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_QSPI_A_DDR_ERR0     | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_MBOX_ADDR_ERR0      | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_DTHE_A_ADDR_ERR0    |
| R/W                                                       | R/W                                                       | R/W                                                       | R/W                                                        | R/W                                                        | R/W                                                      | R/W                                                      | R/W                                                      |
| 0h                                                        | 0h                                                        | 0h                                                        | 0h                                                         | 0h                                                         | 0h                                                       | 0h                                                       | 0h                                                       |
| 7                                                         | 6                                                         | 5                                                         | 4                                                          | 3                                                          | 2                                                        | 1                                                        | 0                                                        |
| MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_CR5B1_AXIS_ADDR_ERR0 | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_CR5A1_AXIS_ADDR_ERR0 | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_CR5B0_AXIS_ADDR_ERR0 | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_CR5A0_AXIS_ADDR_ERR0  | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_L2_BANK_D_ADDR_ERR0   | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_L2_BANK_C_ADDR_ERR0 | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_L2_BANK_B_ADDR_ERR0 | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_L2_BANK_A_ADDR_ERR0 |
| R/W                                                       | R/W                                                       | R/W                                                       | R/W                                                        | R/W                                                        | R/W                                                      | R/W                                                      | R/W                                                      |
| 0h                                                        | 0h                                                        | 0h                                                        | 0h                                                         | 0h                                                         | 0h                                                       | 0h                                                       | 0h                                                       |

**Table 2-302. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG0\_STATUS\_RAW Register Field Descriptions**

| Bit   | Field                                                    | Type | Reset | Description                                                                                                                  |
|-------|----------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                                                 | NONE | 0h    | Reserved                                                                                                                     |
| 17    | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_HSM_A_DDR_ERR0      | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 16    | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW_MPU_CR5B1_AHB_ADDR_ERR0 | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |

**Table 2-302. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG0\_STATUS\_RAW Register Field Descriptions  
(continued)**

| Bit | Field                                                      | Type | Reset | Description                                                                                                                  |
|-----|------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 15  | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW MPU_CR5A1_AHB_ADDR_ERR0   | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 14  | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW MPU_CR5B0_AHB_ADDR_ERR0   | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 13  | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW MPU_CR5A0_AHB_ADDR_ERR0   | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 12  | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW MPU_SCRM2SCRIP1_ADDR_ERR0 | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 11  | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW MPU_SCRM2SCRIP0_ADDR_ERR0 | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 10  | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW MPU_QSPI_ADDR_ERR0        | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 9   | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW MPU_MBOX_ADDR_ERR0        | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 8   | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW MPU_DTHE_A_ADDR_ERR0      | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 7   | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW MPU_CR5B1_AXIS_ADDR_ERR0  | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 6   | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW MPU_CR5A1_AXIS_ADDR_ERR0  | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 5   | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW MPU_CR5B0_AXIS_ADDR_ERR0  | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 4   | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW MPU_CR5A0_AXIS_ADDR_ERR0  | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 3   | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW MPU_L2_BANK_D_ADDR_ERR0   | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 2   | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW MPU_L2_BANK_C_ADDR_ERR0   | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 1   | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW MPU_L2_BANK_B_ADDR_ERR0   | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |

**Table 2-302. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG0\_STATUS\_RAW Register Field Descriptions  
(continued)**

| Bit | Field                                                      | Type | Reset | Description                                                                                                                  |
|-----|------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 0   | MPU_ADDR_INTR_ERRAGG0_STATUS_RAW MPU_L2_BANK_A_ADDR_ERROR0 | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |

### 2.2.2.101 MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG0\_MASK Register

#### 1 MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG0\_MASK Register (Offset = 4030h) [reset = 0h]

This register Masks selected interrupt sources from generating MPU Protection Error Interrupt to R5SS0 CORE0 .

Return to [Summary Table](#)

**Table 2-303. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 4030h       |

**Figure 2-101. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG0\_MASK Name Register**

| 31                                                  | 30                                                  | 29                                                  | 28                                                   | 27                                                   | 26                                                 | 25                                                 | 24                                                 |
|-----------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|------------------------------------------------------|------------------------------------------------------|----------------------------------------------------|----------------------------------------------------|----------------------------------------------------|
| RESERVED                                            |                                                     |                                                     |                                                      |                                                      |                                                    |                                                    |                                                    |
| NONE                                                |                                                     |                                                     |                                                      |                                                      |                                                    |                                                    |                                                    |
| 0h                                                  |                                                     |                                                     |                                                      |                                                      |                                                    |                                                    |                                                    |
| 23                                                  | 22                                                  | 21                                                  | 20                                                   | 19                                                   | 18                                                 | 17                                                 | 16                                                 |
| RESERVED                                            |                                                     |                                                     |                                                      |                                                      |                                                    | MPU_PROT_INTR_ERRAGG0_MASK_MPU_HSM_PROT_ERR0       | MPU_PROT_INTR_ERRAGG0_MASK_MPU_CR5B1_AHB_PROT_ERR0 |
| NONE                                                |                                                     |                                                     |                                                      |                                                      |                                                    | R/W                                                | R/W                                                |
| 0h                                                  |                                                     |                                                     |                                                      |                                                      |                                                    | 0h                                                 | 0h                                                 |
| 15                                                  | 14                                                  | 13                                                  | 12                                                   | 11                                                   | 10                                                 | 9                                                  | 8                                                  |
| MPU_PROT_INTR_ERRAGG0_MASK_MPU_CR5A1_AHB_PROT_ERR0  | MPU_PROT_INTR_ERRAGG0_MASK_MPU_CR5B0_AHB_PROT_ERR0  | MPU_PROT_INTR_ERRAGG0_MASK_MPU_CR5A0_AHB_PROT_ERR0  | MPU_PROT_INTR_ERRAGG0_MASK_MPU_SCRM2SCRIP1_PROT_ERR0 | MPU_PROT_INTR_ERRAGG0_MASK_MPU_SCRM2SCRIP0_PROT_ERR0 | MPU_PROT_INTR_ERRAGG0_MASK_MPU_QSPI_PROT_ERR0      | MPU_PROT_INTR_ERRAGG0_MASK_MPU_MBOX_PROT_ERR0      | MPU_PROT_INTR_ERRAGG0_MASK_MPU_DTHE_A_PROT_ERR0    |
| R/W                                                 | R/W                                                 | R/W                                                 | R/W                                                  | R/W                                                  | R/W                                                | R/W                                                | R/W                                                |
| 0h                                                  | 0h                                                  | 0h                                                  | 0h                                                   | 0h                                                   | 0h                                                 | 0h                                                 | 0h                                                 |
| 7                                                   | 6                                                   | 5                                                   | 4                                                    | 3                                                    | 2                                                  | 1                                                  | 0                                                  |
| MPU_PROT_INTR_ERRAGG0_MASK_MPU_CR5B1_AXIS_PROT_ERR0 | MPU_PROT_INTR_ERRAGG0_MASK_MPU_CR5A1_AXIS_PROT_ERR0 | MPU_PROT_INTR_ERRAGG0_MASK_MPU_CR5B0_AXIS_PROT_ERR0 | MPU_PROT_INTR_ERRAGG0_MASK_MPU_CR5A0_AXIS_PROT_ERR0  | MPU_PROT_INTR_ERRAGG0_MASK_MPU_L2_BANK_D_PROT_ERR0   | MPU_PROT_INTR_ERRAGG0_MASK_MPU_L2_BANK_C_PROT_ERR0 | MPU_PROT_INTR_ERRAGG0_MASK_MPU_L2_BANK_B_PROT_ERR0 | MPU_PROT_INTR_ERRAGG0_MASK_MPU_L2_BANK_A_PROT_ERR0 |
| R/W                                                 | R/W                                                 | R/W                                                 | R/W                                                  | R/W                                                  | R/W                                                | R/W                                                | R/W                                                |
| 0h                                                  | 0h                                                  | 0h                                                  | 0h                                                   | 0h                                                   | 0h                                                 | 0h                                                 | 0h                                                 |

**Table 2-305. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG0\_MASK Register Field Descriptions**

| Bit   | Field                                              | Type | Reset | Description                                                                                                                   |
|-------|----------------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                                           | NONE | 0h    | Reserved                                                                                                                      |
| 17    | MPU_PROT_INTR_ERRAGG0_MASK_MPU_HSM_PROT_ERR0       | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG0<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 16    | MPU_PROT_INTR_ERRAGG0_MASK_MPU_CR5B1_AHB_PROT_ERR0 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG0<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 15    | MPU_PROT_INTR_ERRAGG0_MASK_MPU_CR5A1_AHB_PROT_ERR0 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG0<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |



**Table 2-305. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG0\_MASK Register Field Descriptions (continued)**

| Bit | Field                                               | Type | Reset | Description                                                                                                                  |
|-----|-----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 14  | MPU_PROT_INTR_ERRAGG0_MASK_MPU_CR5B0_AHB_PROT_ERR0  | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 13  | MPU_PROT_INTR_ERRAGG0_MASK_MPU_CR5A0_AHB_PROT_ERR0  | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 12  | MPU_PROT_INTR_ERRAGG0_MASK_MPU_SCRM2SCR1_PROT_ERR0  | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 11  | MPU_PROT_INTR_ERRAGG0_MASK_MPU_SCRM2SCR0_PROT_ERR0  | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 10  | MPU_PROT_INTR_ERRAGG0_MASK_MPU_QSPI_PROT_ERR0       | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 9   | MPU_PROT_INTR_ERRAGG0_MASK_MPU_MBOX_PROT_ERR0       | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 8   | MPU_PROT_INTR_ERRAGG0_MASK_MPU_DTHEA_PROT_ERR0      | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 7   | MPU_PROT_INTR_ERRAGG0_MASK_MPU_CR5B1_AXIS_PROT_ERR0 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 6   | MPU_PROT_INTR_ERRAGG0_MASK_MPU_CR5A1_AXIS_PROT_ERR0 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 5   | MPU_PROT_INTR_ERRAGG0_MASK_MPU_CR5B0_AXIS_PROT_ERR0 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 4   | MPU_PROT_INTR_ERRAGG0_MASK_MPU_CR5A0_AXIS_PROT_ERR0 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 3   | MPU_PROT_INTR_ERRAGG0_MASK_MPU_L2_BA_NK_D_PROT_ERR0 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 2   | MPU_PROT_INTR_ERRAGG0_MASK_MPU_L2_BA_NK_C_PROT_ERR0 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 1   | MPU_PROT_INTR_ERRAGG0_MASK_MPU_L2_BA_NK_B_PROT_ERR0 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |

**Table 2-305. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG0\_MASK Register Field Descriptions (continued)**

| Bit | Field                                              | Type | Reset | Description                                                                                                                  |
|-----|----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 0   | MPU_PROT_INTR_ERRAGG0_MASK_MPU_L2_BANK_A_PROT_ERR0 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |

### 2.2.2.102 MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG0\_STATUS Register

#### 1 MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG0\_STATUS Register (Offset = 4034h) [reset = 0h]

This register shows the Status of Unmasked MPU Protection Errors to R5SS0 Core0 .

Return to [Summary Table](#)

**Table 2-306. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 4034h       |

**Figure 2-102. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG0\_STATUS Name Register**

|                                                       |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
|-------------------------------------------------------|-------------------------------------------------------|-------------------------------------------------------|-------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|
| 31                                                    | 30                                                    | 29                                                    | 28                                                    | 27                                                   | 26                                                   | 25                                                   | 24                                                   |
| RESERVED                                              |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
| NONE                                                  |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
| 0h                                                    |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
| 23                                                    | 22                                                    | 21                                                    | 20                                                    | 19                                                   | 18                                                   | 17                                                   | 16                                                   |
| RESERVED                                              |                                                       |                                                       |                                                       |                                                      |                                                      | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_HSM_PROT_ERR0       | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_CR5B1_AHB_PROT_ERR0 |
| NONE                                                  |                                                       |                                                       |                                                       |                                                      |                                                      | R/W                                                  | R/W                                                  |
| 0h                                                    |                                                       |                                                       |                                                       |                                                      |                                                      | 0h                                                   | 0h                                                   |
| 15                                                    | 14                                                    | 13                                                    | 12                                                    | 11                                                   | 10                                                   | 9                                                    | 8                                                    |
| MPU_PROT_INTR_ERRAGG0_STATUS_MPU_CR5A1_AHB_PROT_ERR0  | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_CR5B0_AHB_PROT_ERR0  | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_CR5A0_AHB_PROT_ERR0  | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_SCRM2SCR1_PROT_ERR0  | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_SCRM2SCR0_PROT_ERR0 | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_QSPI_PROT_ERR0      | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_MBOX_PROT_ERR0      | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_DTHE_A_PROT_ERR0    |
| R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                  | R/W                                                  | R/W                                                  | R/W                                                  |
| 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                   | 0h                                                   | 0h                                                   | 0h                                                   |
| 7                                                     | 6                                                     | 5                                                     | 4                                                     | 3                                                    | 2                                                    | 1                                                    | 0                                                    |
| MPU_PROT_INTR_ERRAGG0_STATUS_MPU_CR5B1_AXIS_PROT_ERR0 | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_CR5A1_AXIS_PROT_ERR0 | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_CR5B0_AXIS_PROT_ERR0 | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_CR5A0_AXIS_PROT_ERR0 | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_L2_BANK_D_PROT_ERR0 | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_L2_BANK_C_PROT_ERR0 | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_L2_BANK_B_PROT_ERR0 | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_L2_BANK_A_PROT_ERR0 |
| R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                  | R/W                                                  | R/W                                                  | R/W                                                  |
| 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                   | 0h                                                   | 0h                                                   | 0h                                                   |

**Table 2-308. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG0\_STATUS Register Field Descriptions**

| Bit   | Field                                                | Type | Reset | Description                                                                                                                        |
|-------|------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                                             | NONE | 0h    | Reserved                                                                                                                           |
| 17    | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_HSM_PROT_ERR0       | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 16    | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_CR5B1_AHB_PROT_ERR0 | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 15    | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_CR5A1_AHB_PROT_ERR0 | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |

**Table 2-308. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG0\_STATUS Register Field Descriptions (continued)**

| Bit | Field                                                  | Type | Reset | Description                                                                                                                        |
|-----|--------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 14  | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_CR5B0_AHB_PROT_ERR0   | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 13  | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_CR5A0_AHB_PROT_ERR0   | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 12  | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_SCRM2SCRIP1_PROT_ERR0 | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 11  | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_SCRM2SCRIP0_PROT_ERR0 | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 10  | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_QSPI_PROT_ERR0        | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 9   | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_MBOX_PROT_ERR0        | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 8   | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_DTHE_A_PROT_ERR0      | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 7   | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_CR5B1_AXIS_PROT_ERR0  | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 6   | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_CR5A1_AXIS_PROT_ERR0  | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 5   | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_CR5B0_AXIS_PROT_ERR0  | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 4   | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_CR5A0_AXIS_PROT_ERR0  | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 3   | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_L2_BANK_D_PROT_ERR0   | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 2   | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_L2_BANK_C_PROT_ERR0   | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 1   | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_L2_BANK_B_PROT_ERR0   | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |

**Table 2-308. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG0\_STATUS Register Field Descriptions (continued)**

| Bit | Field                                                | Type | Reset | Description                                                                                                                             |
|-----|------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 0   | MPU_PROT_INTR_ERRAGG0_STATUS_MPU_L2_BANK_A_PROT_ERR0 | R/W  | 0h    | Status of Error from MPU_PROT_INTR.<br>Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK<br>Write 0x1 to clear this Error. |

### 2.2.2.103 MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG0\_STATUS\_RAW Register

#### 1 MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG0\_STATUS\_RAW Register (Offset = 4038h) [reset = 0h]

This register shows the Status of all MPU Protection Errors.

Return to [Summary Table](#)

**Table 2-309. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 4038h       |

**Figure 2-103. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG0\_STATUS\_RAW Name Register**

| 31                                                                           | 30                                                                           | 29                                                                           | 28                                                                             | 27                                                                             | 26                                                                          | 25                                                                          | 24                                                                          |
|------------------------------------------------------------------------------|------------------------------------------------------------------------------|------------------------------------------------------------------------------|--------------------------------------------------------------------------------|--------------------------------------------------------------------------------|-----------------------------------------------------------------------------|-----------------------------------------------------------------------------|-----------------------------------------------------------------------------|
| RESERVED                                                                     |                                                                              |                                                                              |                                                                                |                                                                                |                                                                             |                                                                             |                                                                             |
| NONE                                                                         |                                                                              |                                                                              |                                                                                |                                                                                |                                                                             |                                                                             |                                                                             |
| 0h                                                                           |                                                                              |                                                                              |                                                                                |                                                                                |                                                                             |                                                                             |                                                                             |
| 23                                                                           | 22                                                                           | 21                                                                           | 20                                                                             | 19                                                                             | 18                                                                          | 17                                                                          | 16                                                                          |
| RESERVED                                                                     |                                                                              |                                                                              |                                                                                |                                                                                |                                                                             | MPU_PROT_IN<br>TR_ERRAGG0<br>STATUS_RAW<br>_MPU_HSM_P<br>ROT_ERR0           | MPU_PROT_IN<br>TR_ERRAGG0<br>STATUS_RAW<br>_MPU_CR5B1_<br>AHB_PROT_E<br>RR0 |
| NONE                                                                         |                                                                              |                                                                              |                                                                                |                                                                                |                                                                             | R/W                                                                         | R/W                                                                         |
| 0h                                                                           |                                                                              |                                                                              |                                                                                |                                                                                |                                                                             | 0h                                                                          | 0h                                                                          |
| 15                                                                           | 14                                                                           | 13                                                                           | 12                                                                             | 11                                                                             | 10                                                                          | 9                                                                           | 8                                                                           |
| MPU_PROT_IN<br>TR_ERRAGG0<br>STATUS_RAW<br>_MPU_CR5A1_<br>AHB_PROT_E<br>RR0  | MPU_PROT_IN<br>TR_ERRAGG0<br>STATUS_RAW<br>_MPU_CR5B0_<br>AHB_PROT_E<br>RR0  | MPU_PROT_IN<br>TR_ERRAGG0<br>STATUS_RAW<br>_MPU_CR5A0_<br>AHB_PROT_E<br>RR0  | MPU_PROT_IN<br>TR_ERRAGG0<br>STATUS_RAW<br>_MPU_SCRM2_<br>SCRIP1_PROT_<br>ERR0 | MPU_PROT_IN<br>TR_ERRAGG0<br>STATUS_RAW<br>_MPU_SCRM2_<br>SCRIP0_PROT_<br>ERR0 | MPU_PROT_IN<br>TR_ERRAGG0<br>STATUS_RAW<br>_MPU_QSPI_P<br>ROT_ERR0          | MPU_PROT_IN<br>TR_ERRAGG0<br>STATUS_RAW<br>_MPU_MBOX_<br>PROT_ERR0          | MPU_PROT_IN<br>TR_ERRAGG0<br>STATUS_RAW<br>_MPU_DTHE_<br>A_PROT_ERR0        |
| R/W                                                                          | R/W                                                                          | R/W                                                                          | R/W                                                                            | R/W                                                                            | R/W                                                                         | R/W                                                                         | R/W                                                                         |
| 0h                                                                           | 0h                                                                           | 0h                                                                           | 0h                                                                             | 0h                                                                             | 0h                                                                          | 0h                                                                          | 0h                                                                          |
| 7                                                                            | 6                                                                            | 5                                                                            | 4                                                                              | 3                                                                              | 2                                                                           | 1                                                                           | 0                                                                           |
| MPU_PROT_IN<br>TR_ERRAGG0<br>STATUS_RAW<br>_MPU_CR5B1_<br>AXIS_PROT_E<br>RR0 | MPU_PROT_IN<br>TR_ERRAGG0<br>STATUS_RAW<br>_MPU_CR5A1_<br>AXIS_PROT_E<br>RR0 | MPU_PROT_IN<br>TR_ERRAGG0<br>STATUS_RAW<br>_MPU_CR5B0_<br>AXIS_PROT_E<br>RR0 | MPU_PROT_IN<br>TR_ERRAGG0<br>STATUS_RAW<br>_MPU_CR5A0_<br>AXIS_PROT_E<br>RR0   | MPU_PROT_IN<br>TR_ERRAGG0<br>STATUS_RAW<br>_MPU_L2_BAN<br>K_D_PROT_ER<br>R0    | MPU_PROT_IN<br>TR_ERRAGG0<br>STATUS_RAW<br>_MPU_L2_BAN<br>K_C_PROT_ER<br>R0 | MPU_PROT_IN<br>TR_ERRAGG0<br>STATUS_RAW<br>_MPU_L2_BAN<br>K_B_PROT_ER<br>R0 | MPU_PROT_IN<br>TR_ERRAGG0<br>STATUS_RAW<br>_MPU_L2_BAN<br>K_A_PROT_ER<br>R0 |
| R/W                                                                          | R/W                                                                          | R/W                                                                          | R/W                                                                            | R/W                                                                            | R/W                                                                         | R/W                                                                         | R/W                                                                         |
| 0h                                                                           | 0h                                                                           | 0h                                                                           | 0h                                                                             | 0h                                                                             | 0h                                                                          | 0h                                                                          | 0h                                                                          |

**Table 2-311. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG0\_STATUS\_RAW Register Field Descriptions**

| Bit   | Field                                                    | Type | Reset | Description                                                                                                                  |
|-------|----------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                                                 | NONE | 0h    | Reserved                                                                                                                     |
| 17    | MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_HSM_PROT_ERR0       | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 16    | MPU_PROT_INTR_ERRAGG0_STATUS_RAW_MPU_CR5B1_AHB_PROT_ERR0 | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |

**Table 2-311. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG0\_STATUS\_RAW Register Field Descriptions  
(continued)**

| Bit | Field                                                      | Type | Reset | Description                                                                                                                  |
|-----|------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 15  | MPU_PROT_INTR_ERRAGG0_STATUS_RAW MPU_CR5A1_AHB_PROT_ERR0   | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 14  | MPU_PROT_INTR_ERRAGG0_STATUS_RAW MPU_CR5B0_AHB_PROT_ERR0   | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 13  | MPU_PROT_INTR_ERRAGG0_STATUS_RAW MPU_CR5A0_AHB_PROT_ERR0   | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 12  | MPU_PROT_INTR_ERRAGG0_STATUS_RAW MPU_SCRM2SCRIP1_PROT_ERR0 | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 11  | MPU_PROT_INTR_ERRAGG0_STATUS_RAW MPU_SCRM2SCRIP0_PROT_ERR0 | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 10  | MPU_PROT_INTR_ERRAGG0_STATUS_RAW MPU_QSPI_PROT_ERR0        | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 9   | MPU_PROT_INTR_ERRAGG0_STATUS_RAW MPU_MBOX_PROT_ERR0        | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 8   | MPU_PROT_INTR_ERRAGG0_STATUS_RAW MPU_DTHE_A_PROT_ERR0      | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 7   | MPU_PROT_INTR_ERRAGG0_STATUS_RAW MPU_CR5B1_AXIS_PROT_ERR0  | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 6   | MPU_PROT_INTR_ERRAGG0_STATUS_RAW MPU_CR5A1_AXIS_PROT_ERR0  | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 5   | MPU_PROT_INTR_ERRAGG0_STATUS_RAW MPU_CR5B0_AXIS_PROT_ERR0  | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 4   | MPU_PROT_INTR_ERRAGG0_STATUS_RAW MPU_CR5A0_AXIS_PROT_ERR0  | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 3   | MPU_PROT_INTR_ERRAGG0_STATUS_RAW MPU_L2_BANK_D_PROT_ERR0   | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 2   | MPU_PROT_INTR_ERRAGG0_STATUS_RAW MPU_L2_BANK_C_PROT_ERR0   | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 1   | MPU_PROT_INTR_ERRAGG0_STATUS_RAW MPU_L2_BANK_B_PROT_ERR0   | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |

**Table 2-311. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG0\_STATUS\_RAW Register Field Descriptions  
(continued)**

| Bit | Field                                                      | Type | Reset | Description                                                                                                                  |
|-----|------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 0   | MPU_PROT_INTR_ERRAGG0_STATUS_RAW MPU_L2_BANK_A_PROT_ERROR0 | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |



### 2.2.2.104 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_MBOX\_WRITE\_DONE Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_MBOX\_WRITE\_DONE Register (Offset = 8000h) [reset = 0h]

This register is used by R5SS0 Core 1 to generate Mailbox interrupt to Recipient CPU.

Return to [Summary Table](#)

**Table 2-312. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 8000h       |

**Figure 2-104. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_MBOX\_WRITE\_DONE Name Register**

| 31       | 30 | 29 | 28                               | 27       | 26 | 25 | 24                               |
|----------|----|----|----------------------------------|----------|----|----|----------------------------------|
| RESERVED |    |    | MSS_CR5B0_MBOX_WRITE_DONE_PROC_7 | RESERVED |    |    | MSS_CR5B0_MBOX_WRITE_DONE_PROC_6 |
| NONE     |    |    | R/W                              | NONE     |    |    | R/W                              |
| 0h       |    |    | 0h                               | 0h       |    |    | 0h                               |
| 23       | 22 | 21 | 20                               | 19       | 18 | 17 | 16                               |
| RESERVED |    |    | MSS_CR5B0_MBOX_WRITE_DONE_PROC_5 | RESERVED |    |    | MSS_CR5B0_MBOX_WRITE_DONE_PROC_4 |
| NONE     |    |    | R/W                              | NONE     |    |    | R/W                              |
| 0h       |    |    | 0h                               | 0h       |    |    | 0h                               |
| 15       | 14 | 13 | 12                               | 11       | 10 | 9  | 8                                |
| RESERVED |    |    | MSS_CR5B0_MBOX_WRITE_DONE_PROC_3 | RESERVED |    |    | MSS_CR5B0_MBOX_WRITE_DONE_PROC_2 |
| NONE     |    |    | R/W                              | NONE     |    |    | R/W                              |
| 0h       |    |    | 0h                               | 0h       |    |    | 0h                               |
| 7        | 6  | 5  | 4                                | 3        | 2  | 1  | 0                                |
| RESERVED |    |    | MSS_CR5B0_MBOX_WRITE_DONE_PROC_1 | RESERVED |    |    | MSS_CR5B0_MBOX_WRITE_DONE_PROC_0 |
| NONE     |    |    | R/W                              | NONE     |    |    | R/W                              |
| 0h       |    |    | 0h                               | 0h       |    |    | 0h                               |

**Table 2-314. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_MBOX\_WRITE\_DONE Register Field Descriptions**

| Bit   | Field                            | Type | Reset | Description                                                                                                             |
|-------|----------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 28    | MSS_CR5B0_MBOX_WRITE_DONE_PROC_7 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 7 |
| 27:25 | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 24    | MSS_CR5B0_MBOX_WRITE_DONE_PROC_6 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 6 |
| 23:21 | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 20    | MSS_CR5B0_MBOX_WRITE_DONE_PROC_5 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 5 |

**Table 2-314. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_MBOX\_WRITE\_DONE Register Field Descriptions  
(continued)**

| Bit   | Field                            | Type | Reset | Description                                                                                                             |
|-------|----------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------|
| 19:17 | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 16    | MSS_CR5B0_MBOX_WRITE_DONE_PROC_4 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 4 |
| 15:13 | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 12    | MSS_CR5B0_MBOX_WRITE_DONE_PROC_3 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 3 |
| 11:9  | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 8     | MSS_CR5B0_MBOX_WRITE_DONE_PROC_2 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 2 |
| 7:5   | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 4     | MSS_CR5B0_MBOX_WRITE_DONE_PROC_1 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 1 |
| 3:1   | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 0     | MSS_CR5B0_MBOX_WRITE_DONE_PROC_0 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 0 |

### 2.2.2.105 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_MBOX\_READ\_REQ Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_MBOX\_READ\_REQ Register (Offset = 8004h) [reset = 0h]

This register is used by R5SS0 Core 1 to know the Sender of Mailbox Interrupt as well as clear it.

Return to [Summary Table](#)

**Table 2-315. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 8004h       |

**Figure 2-105. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_MBOX\_READ\_REQ Name Register**

| 31       | 30 | 29 | 28                             | 27       | 26 | 25 | 24                             |
|----------|----|----|--------------------------------|----------|----|----|--------------------------------|
| RESERVED |    |    | MSS_CR5B0_MBOX_READ_REQ_PROC_7 | RESERVED |    |    | MSS_CR5B0_MBOX_READ_REQ_PROC_6 |
| NONE     |    |    | R/W                            | NONE     |    |    | R/W                            |
| 0h       |    |    | 0h                             | 0h       |    |    | 0h                             |
| 23       | 22 | 21 | 20                             | 19       | 18 | 17 | 16                             |
| RESERVED |    |    | MSS_CR5B0_MBOX_READ_REQ_PROC_5 | RESERVED |    |    | MSS_CR5B0_MBOX_READ_REQ_PROC_4 |
| NONE     |    |    | R/W                            | NONE     |    |    | R/W                            |
| 0h       |    |    | 0h                             | 0h       |    |    | 0h                             |
| 15       | 14 | 13 | 12                             | 11       | 10 | 9  | 8                              |
| RESERVED |    |    | MSS_CR5B0_MBOX_READ_REQ_PROC_3 | RESERVED |    |    | MSS_CR5B0_MBOX_READ_REQ_PROC_2 |
| NONE     |    |    | R/W                            | NONE     |    |    | R/W                            |
| 0h       |    |    | 0h                             | 0h       |    |    | 0h                             |
| 7        | 6  | 5  | 4                              | 3        | 2  | 1  | 0                              |
| RESERVED |    |    | MSS_CR5B0_MBOX_READ_REQ_PROC_1 | RESERVED |    |    | MSS_CR5B0_MBOX_READ_REQ_PROC_0 |
| NONE     |    |    | R/W                            | NONE     |    |    | R/W                            |
| 0h       |    |    | 0h                             | 0h       |    |    | 0h                             |

**Table 2-317. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_MBOX\_READ\_REQ Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                       |
|-------|--------------------------------|------|-------|-----------------------------------------------------------------------------------|
| 31:29 | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 28    | MSS_CR5B0_MBOX_READ_REQ_PROC_7 | R/W  | 0h    | This is request from processor 7 to mss_CR5B. Requesting it to read from mailbox. |
| 27:25 | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 24    | MSS_CR5B0_MBOX_READ_REQ_PROC_6 | R/W  | 0h    | This is request from processor 6 to mss_CR5B. Requesting it to read from mailbox. |
| 23:21 | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 20    | MSS_CR5B0_MBOX_READ_REQ_PROC_5 | R/W  | 0h    | This is request from processor 5 to mss_CR5B. Requesting it to read from mailbox. |
| 19:17 | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 16    | MSS_CR5B0_MBOX_READ_REQ_PROC_4 | R/W  | 0h    | This is request from processor 4 to mss_CR5B. Requesting it to read from mailbox. |
| 15:13 | RESERVED                       | NONE | 0h    | Reserved                                                                          |

**Table 2-317. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_MBOX\_READ\_REQ Register Field Descriptions  
(continued)**

| Bit  | Field                          | Type | Reset | Description                                                                       |
|------|--------------------------------|------|-------|-----------------------------------------------------------------------------------|
| 12   | MSS_CR5B0_MBOX_READ_REQ_PROC_3 | R/W  | 0h    | This is request from processor 3 to mss_CR5B. Requesting it to read from mailbox. |
| 11:9 | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 8    | MSS_CR5B0_MBOX_READ_REQ_PROC_2 | R/W  | 0h    | This is request from processor 2 to mss_CR5B. Requesting it to read from mailbox. |
| 7:5  | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 4    | MSS_CR5B0_MBOX_READ_REQ_PROC_1 | R/W  | 0h    | This is request from processor 1 to mss_CR5B. Requesting it to read from mailbox. |
| 3:1  | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 0    | MSS_CR5B0_MBOX_READ_REQ_PROC_0 | R/W  | 0h    | This is request from processor 0 to mss_CR5B. Requesting it to read from mailbox. |

### 2.2.2.106 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_MBOX\_READ\_DONE\_ACK Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_MBOX\_READ\_DONE\_ACK Register (Offset = 8008h) [reset = 0h]

This register is used by R5SS0 Core 1 to generate Mailbox Read acknowledgement to the Sender CPU.

Return to [Summary Table](#)

**Table 2-318. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 8008h       |

**Figure 2-106. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_MBOX\_READ\_DONE\_ACK Name Register**

|                                   |    |    |    |    |    |    |    |
|-----------------------------------|----|----|----|----|----|----|----|
| 31                                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                          |    |    |    |    |    |    |    |
| NONE                              |    |    |    |    |    |    |    |
| 0h                                |    |    |    |    |    |    |    |
| 23                                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                          |    |    |    |    |    |    |    |
| NONE                              |    |    |    |    |    |    |    |
| 0h                                |    |    |    |    |    |    |    |
| 15                                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED                          |    |    |    |    |    |    |    |
| NONE                              |    |    |    |    |    |    |    |
| 0h                                |    |    |    |    |    |    |    |
| 7                                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B0_MBOX_READ_DONE_ACK_PROC |    |    |    |    |    |    |    |
| R/W                               |    |    |    |    |    |    |    |
| 0h                                |    |    |    |    |    |    |    |

**Table 2-320. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_MBOX\_READ\_DONE\_ACK Register Field Descriptions**

| Bit  | Field                             | Type | Reset | Description                                                                                                            |
|------|-----------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED                          | NONE | 0h    | Reserved                                                                                                               |
| 7:0  | MSS_CR5B0_MBOX_READ_DONE_ACK_PROC | R/W  | 0h    | Write pulse bit field:<br>For bits 0 to 7: Writing 1'b1 : Generates pulse interrupt to corresponding proc from MSS_CR5 |

### 2.2.2.107 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_MBOX\_READ\_DONE Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_MBOX\_READ\_DONE Register (Offset = 800Ch) [reset = 0h]

This register is used by R5SS0 Core 1 to know that the Receiver CPU has read the Mailbox and Acked. It is also used to clear the Read Done Interrupt.

Return to [Summary Table](#)

**Table 2-321. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 800Ch       |

**Figure 2-107. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_MBOX\_READ\_DONE Name Register**

| 31       | 30 | 29 | 28                              | 27       | 26 | 25 | 24                              |
|----------|----|----|---------------------------------|----------|----|----|---------------------------------|
| RESERVED |    |    | MSS_CR5B0_MBOX_READ_DONE_PROC_7 | RESERVED |    |    | MSS_CR5B0_MBOX_READ_DONE_PROC_6 |
| NONE     |    |    | R/W                             | NONE     |    |    | R/W                             |
| 0h       |    |    | 0h                              | 0h       |    |    | 0h                              |
| 23       | 22 | 21 | 20                              | 19       | 18 | 17 | 16                              |
| RESERVED |    |    | MSS_CR5B0_MBOX_READ_DONE_PROC_5 | RESERVED |    |    | MSS_CR5B0_MBOX_READ_DONE_PROC_4 |
| NONE     |    |    | R/W                             | NONE     |    |    | R/W                             |
| 0h       |    |    | 0h                              | 0h       |    |    | 0h                              |
| 15       | 14 | 13 | 12                              | 11       | 10 | 9  | 8                               |
| RESERVED |    |    | MSS_CR5B0_MBOX_READ_DONE_PROC_3 | RESERVED |    |    | MSS_CR5B0_MBOX_READ_DONE_PROC_2 |
| NONE     |    |    | R/W                             | NONE     |    |    | R/W                             |
| 0h       |    |    | 0h                              | 0h       |    |    | 0h                              |
| 7        | 6  | 5  | 4                               | 3        | 2  | 1  | 0                               |
| RESERVED |    |    | MSS_CR5B0_MBOX_READ_DONE_PROC_1 | RESERVED |    |    | MSS_CR5B0_MBOX_READ_DONE_PROC_0 |
| NONE     |    |    | R/W                             | NONE     |    |    | R/W                             |
| 0h       |    |    | 0h                              | 0h       |    |    | 0h                              |

**Table 2-323. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_MBOX\_READ\_DONE Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                 |
|-------|---------------------------------|------|-------|---------------------------------------------------------------------------------------------|
| 31:29 | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 28    | MSS_CR5B0_MBOX_READ_DONE_PROC_7 | R/W  | 0h    | This register should be written once finishing Reading from proc7's mailbox written by CR5B |
| 27:25 | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 24    | MSS_CR5B0_MBOX_READ_DONE_PROC_6 | R/W  | 0h    | This register should be written once finishing Reading from proc6's mailbox written by CR5B |
| 23:21 | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 20    | MSS_CR5B0_MBOX_READ_DONE_PROC_5 | R/W  | 0h    | This register should be written once finishing Reading from proc5's mailbox written by CR5B |
| 19:17 | RESERVED                        | NONE | 0h    | Reserved                                                                                    |

**Table 2-323. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_MBOX\_READ\_DONE Register Field Descriptions  
(continued)**

| Bit   | Field                           | Type | Reset | Description                                                                                 |
|-------|---------------------------------|------|-------|---------------------------------------------------------------------------------------------|
| 16    | MSS_CR5B0_MBOX_READ_DONE_PROC_4 | R/W  | 0h    | This register should be written once finishing Reading from proc4's mailbox written by CR5B |
| 15:13 | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 12    | MSS_CR5B0_MBOX_READ_DONE_PROC_3 | R/W  | 0h    | This register should be written once finishing Reading from proc3's mailbox written by CR5B |
| 11:9  | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 8     | MSS_CR5B0_MBOX_READ_DONE_PROC_2 | R/W  | 0h    | This register should be written once finishing Reading from proc2's mailbox written by CR5B |
| 7:5   | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 4     | MSS_CR5B0_MBOX_READ_DONE_PROC_1 | R/W  | 0h    | This register should be written once finishing Reading from proc1's mailbox written by CR5B |
| 3:1   | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 0     | MSS_CR5B0_MBOX_READ_DONE_PROC_0 | R/W  | 0h    | This register should be written once finishing Reading from proc0's mailbox written by CR5B |

### 2.2.2.108 MSS\_CTRL\_MSS\_SW\_INT\_R5SS0\_CORE1 Register

#### 1 MSS\_CTRL\_MSS\_SW\_INT\_R5SS0\_CORE1 Register (Offset = 8010h) [reset = 0h]

This Register is used to generate a S/W Triggered Interrupt to R5SS0 Core1.

Return to [Summary Table](#)

**Table 2-324. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 8010h       |

**Figure 2-108. MSS\_CTRL\_MSS\_SW\_INT\_R5SS0\_CORE1 Name Register**

|          |    |    |    |    |    |    |                              |
|----------|----|----|----|----|----|----|------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                           |
| RESERVED |    |    |    |    |    |    |                              |
| NONE     |    |    |    |    |    |    |                              |
| 0h       |    |    |    |    |    |    |                              |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                           |
| RESERVED |    |    |    |    |    |    |                              |
| NONE     |    |    |    |    |    |    |                              |
| 0h       |    |    |    |    |    |    |                              |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                            |
| RESERVED |    |    |    |    |    |    |                              |
| NONE     |    |    |    |    |    |    |                              |
| 0h       |    |    |    |    |    |    |                              |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                            |
| RESERVED |    |    |    |    |    |    | MSS_SW_INT_R5SS0_CORE1_PULSE |
| NONE     |    |    |    |    |    |    | R/W                          |
| 0h       |    |    |    |    |    |    | 0h                           |

**Table 2-326. MSS\_CTRL\_MSS\_SW\_INT\_R5SS0\_CORE1 Register Field Descriptions**

| Bit  | Field                        | Type | Reset | Description                                                                                        |
|------|------------------------------|------|-------|----------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED                     | NONE | 0h    | Reserved                                                                                           |
| 0    | MSS_SW_INT_R5SS0_CORE1_PULSE | R/W  | 0h    | Write_pulse bit field:<br>Writing 1'b1 to each bit will trigger MSS_SW_INT respectively to CR5A/B. |



### 2.2.2.109 MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG1\_MASK Register

#### 1 MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG1\_MASK Register (Offset = 8020h) [reset = 0h]

This register Masks selected interrupt sources from generating MPU Address Error Interrupt to R5SS0 CORE1 .

Return to [Summary Table](#)

**Table 2-327. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 8020h       |

**Figure 2-109. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG1\_MASK Name Register**

|                                                     |                                                     |                                                     |                                                      |                                                      |                                                    |                                                    |                                                    |
|-----------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|------------------------------------------------------|------------------------------------------------------|----------------------------------------------------|----------------------------------------------------|----------------------------------------------------|
| 31                                                  | 30                                                  | 29                                                  | 28                                                   | 27                                                   | 26                                                 | 25                                                 | 24                                                 |
| RESERVED                                            |                                                     |                                                     |                                                      |                                                      |                                                    |                                                    |                                                    |
| NONE                                                |                                                     |                                                     |                                                      |                                                      |                                                    |                                                    |                                                    |
| 0h                                                  |                                                     |                                                     |                                                      |                                                      |                                                    |                                                    |                                                    |
| 23                                                  | 22                                                  | 21                                                  | 20                                                   | 19                                                   | 18                                                 | 17                                                 | 16                                                 |
| RESERVED                                            |                                                     |                                                     |                                                      |                                                      |                                                    | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_HSM_ADDR_ERR1       | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_CR5B1_AHB_ADDR_ERR1 |
| NONE                                                |                                                     |                                                     |                                                      |                                                      |                                                    | R/W                                                | R/W                                                |
| 0h                                                  |                                                     |                                                     |                                                      |                                                      |                                                    | 0h                                                 | 0h                                                 |
| 15                                                  | 14                                                  | 13                                                  | 12                                                   | 11                                                   | 10                                                 | 9                                                  | 8                                                  |
| MPU_ADDR_INTR_ERRAGG1_MASK_MPU_CR5A1_AHB_ADDR_ERR1  | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_CR5B0_AHB_ADDR_ERR1  | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_CR5A0_AHB_ADDR_ERR1  | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_SCRM2SCRIP1_ADDR_ERR1 | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_SCRM2SCRIP0_ADDR_ERR1 | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_QSPI_ADDR_ERR1      | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_MBOX_ADDR_ERR1      | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_DTHE_A_ADDR_ERR1    |
| R/W                                                 | R/W                                                 | R/W                                                 | R/W                                                  | R/W                                                  | R/W                                                | R/W                                                | R/W                                                |
| 0h                                                  | 0h                                                  | 0h                                                  | 0h                                                   | 0h                                                   | 0h                                                 | 0h                                                 | 0h                                                 |
| 7                                                   | 6                                                   | 5                                                   | 4                                                    | 3                                                    | 2                                                  | 1                                                  | 0                                                  |
| MPU_ADDR_INTR_ERRAGG1_MASK_MPU_CR5B1_AXIS_ADDR_ERR1 | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_CR5A1_AXIS_ADDR_ERR1 | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_CR5B0_AXIS_ADDR_ERR1 | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_CR5A0_AXIS_ADDR_ERR1  | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_L2_BANK_D_ADDR_ERR1   | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_L2_BANK_C_ADDR_ERR1 | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_L2_BANK_B_ADDR_ERR1 | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_L2_BANK_A_ADDR_ERR1 |
| R/W                                                 | R/W                                                 | R/W                                                 | R/W                                                  | R/W                                                  | R/W                                                | R/W                                                | R/W                                                |
| 0h                                                  | 0h                                                  | 0h                                                  | 0h                                                   | 0h                                                   | 0h                                                 | 0h                                                 | 0h                                                 |

**Table 2-329. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG1\_MASK Register Field Descriptions**

| Bit   | Field                                              | Type | Reset | Description                                                                                                                   |
|-------|----------------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                                           | NONE | 0h    | Reserved                                                                                                                      |
| 17    | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_HSM_ADDR_ERR1       | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG1<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 16    | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_CR5B1_AHB_ADDR_ERR1 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG1<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 15    | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_CR5A1_AHB_ADDR_ERR1 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG1<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |

**Table 2-329. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG1\_MASK Register Field Descriptions (continued)**

| Bit | Field                                                | Type | Reset | Description                                                                                                                  |
|-----|------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 14  | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_CR5B0_AHB_ADDR_ERR1   | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 13  | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_CR5A0_AHB_ADDR_ERR1   | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 12  | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_SCRM2SCR1P1_ADDR_ERR1 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 11  | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_SCRM2SCR0_ADDR_ERR1   | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 10  | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_QSPI_ADDR_ERR1        | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 9   | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_MBOX_ADDR_ERR1        | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 8   | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_DTHEA_ADDR_ERR1       | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 7   | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_CR5B1_AXIS_ADDR_ERR1  | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 6   | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_CR5A1_AXIS_ADDR_ERR1  | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 5   | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_CR5B0_AXIS_ADDR_ERR1  | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 4   | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_CR5A0_AXIS_ADDR_ERR1  | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 3   | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_L2_BA NK_D_ADDR_ERR1  | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 2   | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_L2_BA NK_C_ADDR_ERR1  | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 1   | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_L2_BA NK_B_ADDR_ERR1  | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |

**Table 2-329. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG1\_MASK Register Field Descriptions (continued)**

| Bit | Field                                              | Type | Reset | Description                                                                                                                  |
|-----|----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 0   | MPU_ADDR_INTR_ERRAGG1_MASK_MPU_L2_BANK_A_ADDR_ERR1 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |

### 2.2.2.110 MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG1\_STATUS Register

#### 1 MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG1\_STATUS Register (Offset = 8024h) [reset = 0h]

This register shows the Status of Unmasked MPU Address Errors to R5SS0 CORE1 .

Return to [Summary Table](#)

**Table 2-330. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 8024h       |

**Figure 2-110. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG1\_STATUS Name Register**

|                                                       |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
|-------------------------------------------------------|-------------------------------------------------------|-------------------------------------------------------|-------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|
| 31                                                    | 30                                                    | 29                                                    | 28                                                    | 27                                                   | 26                                                   | 25                                                   | 24                                                   |
| RESERVED                                              |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
| NONE                                                  |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
| 0h                                                    |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
| 23                                                    | 22                                                    | 21                                                    | 20                                                    | 19                                                   | 18                                                   | 17                                                   | 16                                                   |
| RESERVED                                              |                                                       |                                                       |                                                       |                                                      |                                                      | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_HSM_ADDR_ERR1       | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_CR5B1_AHB_ADDR_ERR1 |
| NONE                                                  |                                                       |                                                       |                                                       |                                                      |                                                      | R/W                                                  | R/W                                                  |
| 0h                                                    |                                                       |                                                       |                                                       |                                                      |                                                      | 0h                                                   | 0h                                                   |
| 15                                                    | 14                                                    | 13                                                    | 12                                                    | 11                                                   | 10                                                   | 9                                                    | 8                                                    |
| MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_CR5A1_AHB_ADDR_ERR1  | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_CR5B0_AHB_ADDR_ERR1  | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_CR5A0_AHB_ADDR_ERR1  | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_SCRM2SCR1_ADDR_ERR1  | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_SCRM2SCR0_ADDR_ERR1 | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_QSPI_ADDR_ERR1      | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_MBOX_ADDR_ERR1      | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_DTHE_A_ADDR_ERR1    |
| R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                  | R/W                                                  | R/W                                                  | R/W                                                  |
| 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                   | 0h                                                   | 0h                                                   | 0h                                                   |
| 7                                                     | 6                                                     | 5                                                     | 4                                                     | 3                                                    | 2                                                    | 1                                                    | 0                                                    |
| MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_CR5B1_AXIS_ADDR_ERR1 | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_CR5A1_AXIS_ADDR_ERR1 | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_CR5B0_AXIS_ADDR_ERR1 | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_CR5A0_AXIS_ADDR_ERR1 | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_L2_BANK_D_ADDR_ERR1 | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_L2_BANK_C_ADDR_ERR1 | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_L2_BANK_B_ADDR_ERR1 | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_L2_BANK_A_ADDR_ERR1 |
| R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                  | R/W                                                  | R/W                                                  | R/W                                                  |
| 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                   | 0h                                                   | 0h                                                   | 0h                                                   |

**Table 2-332. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG1\_STATUS Register Field Descriptions**

| Bit   | Field                                                | Type | Reset | Description                                                                                                                        |
|-------|------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                                             | NONE | 0h    | Reserved                                                                                                                           |
| 17    | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_HSM_ADDR_ERR1       | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 16    | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_CR5B1_AHB_ADDR_ERR1 | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 15    | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_CR5A1_AHB_ADDR_ERR1 | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |

**Table 2-332. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG1\_STATUS Register Field Descriptions (continued)**

| Bit | Field                                                   | Type | Reset | Description                                                                                                                        |
|-----|---------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 14  | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_CR5_B0_AHB_ADDR_ERR1   | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 13  | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_CR5_A0_AHB_ADDR_ERR1   | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 12  | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_SCR_M2SCR_P1_ADDR_ERR1 | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 11  | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_SCR_M2SCR_P0_ADDR_ERR1 | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 10  | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_QSPI_ADDR_ERR1         | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 9   | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_MBOX_ADDR_ERR1         | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 8   | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_DTHE_A_ADDR_ERR1       | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 7   | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_CR5_B1_AXIS_ADDR_ERR1  | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 6   | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_CR5_A1_AXIS_ADDR_ERR1  | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 5   | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_CR5_B0_AXIS_ADDR_ERR1  | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 4   | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_CR5_A0_AXIS_ADDR_ERR1  | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 3   | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_L2_BANK_D_ADDR_ERR1    | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 2   | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_L2_BANK_C_ADDR_ERR1    | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 1   | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_L2_BANK_B_ADDR_ERR1    | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |

**Table 2-332. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG1\_STATUS Register Field Descriptions (continued)**

| Bit | Field                                                | Type | Reset | Description                                                                                                                             |
|-----|------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 0   | MPU_ADDR_INTR_ERRAGG1_STATUS_MPU_L2_BANK_A_ADDR_ERR1 | R/W  | 0h    | Status of Error from MPU_ADDR_INTR.<br>Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK<br>Write 0x1 to clear this Error. |

### 2.2.2.111 MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG1\_STATUS\_RAW Register

#### 1 MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG1\_STATUS\_RAW Register (Offset = 8028h) [reset = 0h]

This register shows the Status of all MPU Address Errors.

Return to [Summary Table](#)

**Table 2-333. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 8028h       |

**Figure 2-111. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG1\_STATUS\_RAW Name Register**

|                                                           |                                                           |                                                           |                                                            |                                                            |                                                          |                                                          |                                                          |
|-----------------------------------------------------------|-----------------------------------------------------------|-----------------------------------------------------------|------------------------------------------------------------|------------------------------------------------------------|----------------------------------------------------------|----------------------------------------------------------|----------------------------------------------------------|
| 31                                                        | 30                                                        | 29                                                        | 28                                                         | 27                                                         | 26                                                       | 25                                                       | 24                                                       |
| RESERVED                                                  |                                                           |                                                           |                                                            |                                                            |                                                          |                                                          |                                                          |
| NONE                                                      |                                                           |                                                           |                                                            |                                                            |                                                          |                                                          |                                                          |
| 0h                                                        |                                                           |                                                           |                                                            |                                                            |                                                          |                                                          |                                                          |
| 23                                                        | 22                                                        | 21                                                        | 20                                                         | 19                                                         | 18                                                       | 17                                                       | 16                                                       |
| RESERVED                                                  |                                                           |                                                           |                                                            |                                                            |                                                          | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_HSM_A_DDR_ERR1      | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_CR5B1_AHB_ADDR_ERR1 |
| NONE                                                      |                                                           |                                                           |                                                            |                                                            |                                                          | R/W                                                      | R/W                                                      |
| 0h                                                        |                                                           |                                                           |                                                            |                                                            |                                                          | 0h                                                       | 0h                                                       |
| 15                                                        | 14                                                        | 13                                                        | 12                                                         | 11                                                         | 10                                                       | 9                                                        | 8                                                        |
| MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_CR5A1_AHB_ADDR_ERR1  | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_CR5B0_AHB_ADDR_ERR1  | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_CR5A0_AHB_ADDR_ERR1  | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_SCRM2_SCRP1_ADDR_ERR1 | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_SCRM2_SCRP0_ADDR_ERR1 | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_QSPI_A_DDR_ERR1     | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_MBOX_ADDR_ERR1      | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_DTHE_A_ADDR_ERR1    |
| R/W                                                       | R/W                                                       | R/W                                                       | R/W                                                        | R/W                                                        | R/W                                                      | R/W                                                      | R/W                                                      |
| 0h                                                        | 0h                                                        | 0h                                                        | 0h                                                         | 0h                                                         | 0h                                                       | 0h                                                       | 0h                                                       |
| 7                                                         | 6                                                         | 5                                                         | 4                                                          | 3                                                          | 2                                                        | 1                                                        | 0                                                        |
| MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_CR5B1_AXIS_ADDR_ERR1 | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_CR5A1_AXIS_ADDR_ERR1 | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_CR5B0_AXIS_ADDR_ERR1 | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_CR5A0_AXIS_ADDR_ERR1  | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_L2_BANK_D_ADDR_ERR1   | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_L2_BANK_C_ADDR_ERR1 | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_L2_BANK_B_ADDR_ERR1 | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_L2_BANK_A_ADDR_ERR1 |
| R/W                                                       | R/W                                                       | R/W                                                       | R/W                                                        | R/W                                                        | R/W                                                      | R/W                                                      | R/W                                                      |
| 0h                                                        | 0h                                                        | 0h                                                        | 0h                                                         | 0h                                                         | 0h                                                       | 0h                                                       | 0h                                                       |

**Table 2-335. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG1\_STATUS\_RAW Register Field Descriptions**

| Bit   | Field                                                    | Type | Reset | Description                                                                                                                  |
|-------|----------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                                                 | NONE | 0h    | Reserved                                                                                                                     |
| 17    | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_HSM_A_DDR_ERR1      | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 16    | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW_MPU_CR5B1_AHB_ADDR_ERR1 | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |

**Table 2-335. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG1\_STATUS\_RAW Register Field Descriptions  
(continued)**

| Bit | Field                                                      | Type | Reset | Description                                                                                                                  |
|-----|------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 15  | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW MPU_CR5A1_AHB_ADDR_ERR1   | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 14  | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW MPU_CR5B0_AHB_ADDR_ERR1   | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 13  | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW MPU_CR5A0_AHB_ADDR_ERR1   | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 12  | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW MPU_SCRM2SCRIP1_ADDR_ERR1 | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 11  | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW MPU_SCRM2SCRIP0_ADDR_ERR1 | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 10  | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW MPU_QSPI_ADDR_ERR1        | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 9   | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW MPU_MBOX_ADDR_ERR1        | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 8   | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW MPU_DTHE_A_ADDR_ERR1      | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 7   | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW MPU_CR5B1_AXIS_ADDR_ERR1  | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 6   | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW MPU_CR5A1_AXIS_ADDR_ERR1  | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 5   | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW MPU_CR5B0_AXIS_ADDR_ERR1  | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 4   | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW MPU_CR5A0_AXIS_ADDR_ERR1  | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 3   | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW MPU_L2_BANK_D_ADDR_ERR1   | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 2   | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW MPU_L2_BANK_C_ADDR_ERR1   | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 1   | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW MPU_L2_BANK_B_ADDR_ERR1   | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |



**Table 2-335. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG1\_STATUS\_RAW Register Field Descriptions  
(continued)**

| Bit | Field                                                    | Type | Reset | Description                                                                                                                  |
|-----|----------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 0   | MPU_ADDR_INTR_ERRAGG1_STATUS_RAW MPU_L2_BANK_A_ADDR_ERR1 | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |

### 2.2.2.112 MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG1\_MASK Register

#### 1 MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG1\_MASK Register (Offset = 8030h) [reset = 0h]

This register Masks selected interrupt sources from generating MPU Protection Error Interrupt to R5SS0 CORE1 .

Return to [Summary Table](#)

**Table 2-336. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 8030h       |

**Figure 2-112. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG1\_MASK Name Register**

| 31                                                  | 30                                                  | 29                                                  | 28                                                   | 27                                                   | 26                                                  | 25                                                  | 24                                                  |
|-----------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|------------------------------------------------------|------------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|
| RESERVED                                            |                                                     |                                                     |                                                      |                                                      |                                                     |                                                     |                                                     |
| NONE                                                |                                                     |                                                     |                                                      |                                                      |                                                     |                                                     |                                                     |
| 0h                                                  |                                                     |                                                     |                                                      |                                                      |                                                     |                                                     |                                                     |
| 23                                                  | 22                                                  | 21                                                  | 20                                                   | 19                                                   | 18                                                  | 17                                                  | 16                                                  |
| RESERVED                                            |                                                     |                                                     |                                                      |                                                      |                                                     | MPU_PROT_INTR_ERRAGG1_MASK_MPU_HSM_PROT_ERR1        | MPU_PROT_INTR_ERRAGG1_MASK_MPU_CR5B1_AHB_PROT_ERR1  |
| NONE                                                |                                                     |                                                     |                                                      |                                                      |                                                     | R/W                                                 | R/W                                                 |
| 0h                                                  |                                                     |                                                     |                                                      |                                                      |                                                     | 0h                                                  | 0h                                                  |
| 15                                                  | 14                                                  | 13                                                  | 12                                                   | 11                                                   | 10                                                  | 9                                                   | 8                                                   |
| MPU_PROT_INTR_ERRAGG1_MASK_MPU_CR5A1_AHB_PROT_ERR1  | MPU_PROT_INTR_ERRAGG1_MASK_MPU_CR5B0_AHB_PROT_ERR1  | MPU_PROT_INTR_ERRAGG1_MASK_MPU_CR5A0_AHB_PROT_ERR1  | MPU_PROT_INTR_ERRAGG1_MASK_MPU_SCRM2SCRIP1_PROT_ERR1 | MPU_PROT_INTR_ERRAGG1_MASK_MPU_SCRM2SCRIP0_PROT_ERR1 | MPU_PROT_INTR_ERRAGG1_MASK_MPU_QSPI_PROT_ERR1       | MPU_PROT_INTR_ERRAGG1_MASK_MPU_MBOX_PROT_ERR1       | MPU_PROT_INTR_ERRAGG1_MASK_MPU_DTHE_A_PROT_ERR1     |
| R/W                                                 | R/W                                                 | R/W                                                 | R/W                                                  | R/W                                                  | R/W                                                 | R/W                                                 | R/W                                                 |
| 0h                                                  | 0h                                                  | 0h                                                  | 0h                                                   | 0h                                                   | 0h                                                  | 0h                                                  | 0h                                                  |
| 7                                                   | 6                                                   | 5                                                   | 4                                                    | 3                                                    | 2                                                   | 1                                                   | 0                                                   |
| MPU_PROT_INTR_ERRAGG1_MASK_MPU_CR5B1_AXIS_PROT_ERR1 | MPU_PROT_INTR_ERRAGG1_MASK_MPU_CR5A1_AXIS_PROT_ERR1 | MPU_PROT_INTR_ERRAGG1_MASK_MPU_CR5B0_AXIS_PROT_ERR1 | MPU_PROT_INTR_ERRAGG1_MASK_MPU_CR5A0_AXIS_PROT_ERR1  | MPU_PROT_INTR_ERRAGG1_MASK_MPU_L2_BANK_D_P_ROT_ERR1  | MPU_PROT_INTR_ERRAGG1_MASK_MPU_L2_BANK_C_P_ROT_ERR1 | MPU_PROT_INTR_ERRAGG1_MASK_MPU_L2_BANK_B_P_ROT_ERR1 | MPU_PROT_INTR_ERRAGG1_MASK_MPU_L2_BANK_A_P_ROT_ERR1 |
| R/W                                                 | R/W                                                 | R/W                                                 | R/W                                                  | R/W                                                  | R/W                                                 | R/W                                                 | R/W                                                 |
| 0h                                                  | 0h                                                  | 0h                                                  | 0h                                                   | 0h                                                   | 0h                                                  | 0h                                                  | 0h                                                  |

**Table 2-338. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG1\_MASK Register Field Descriptions**

| Bit   | Field                                              | Type | Reset | Description                                                                                                                   |
|-------|----------------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                                           | NONE | 0h    | Reserved                                                                                                                      |
| 17    | MPU_PROT_INTR_ERRAGG1_MASK_MPU_HSM_PROT_ERR1       | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG1<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 16    | MPU_PROT_INTR_ERRAGG1_MASK_MPU_CR5B1_AHB_PROT_ERR1 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG1<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 15    | MPU_PROT_INTR_ERRAGG1_MASK_MPU_CR5A1_AHB_PROT_ERR1 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG1<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |

**Table 2-338. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG1\_MASK Register Field Descriptions (continued)**

| Bit | Field                                               | Type | Reset | Description                                                                                                                  |
|-----|-----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 14  | MPU_PROT_INTR_ERRAGG1_MASK_MPU_CR5B0_AHB_PROT_ERR1  | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 13  | MPU_PROT_INTR_ERRAGG1_MASK_MPU_CR5A0_AHB_PROT_ERR1  | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 12  | MPU_PROT_INTR_ERRAGG1_MASK_MPU_SCRM2SCR1_PROT_ERR1  | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 11  | MPU_PROT_INTR_ERRAGG1_MASK_MPU_SCRM2SCR0_PROT_ERR1  | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 10  | MPU_PROT_INTR_ERRAGG1_MASK_MPU_QSPI_PROT_ERR1       | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 9   | MPU_PROT_INTR_ERRAGG1_MASK_MPU_MBOX_PROT_ERR1       | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 8   | MPU_PROT_INTR_ERRAGG1_MASK_MPU_DTHE_A_PROT_ERR1     | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 7   | MPU_PROT_INTR_ERRAGG1_MASK_MPU_CR5B1_AXIS_PROT_ERR1 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 6   | MPU_PROT_INTR_ERRAGG1_MASK_MPU_CR5A1_AXIS_PROT_ERR1 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 5   | MPU_PROT_INTR_ERRAGG1_MASK_MPU_CR5B0_AXIS_PROT_ERR1 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 4   | MPU_PROT_INTR_ERRAGG1_MASK_MPU_CR5A0_AXIS_PROT_ERR1 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 3   | MPU_PROT_INTR_ERRAGG1_MASK_MPU_L2_BA_NK_D_PROT_ERR1 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 2   | MPU_PROT_INTR_ERRAGG1_MASK_MPU_L2_BA_NK_C_PROT_ERR1 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 1   | MPU_PROT_INTR_ERRAGG1_MASK_MPU_L2_BA_NK_B_PROT_ERR1 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |

**Table 2-338. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG1\_MASK Register Field Descriptions (continued)**

| Bit | Field                                              | Type | Reset | Description                                                                                                                  |
|-----|----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 0   | MPU_PROT_INTR_ERRAGG1_MASK_MPU_L2_BANK_A_PROT_ERR1 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |

### 2.2.2.113 MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG1\_STATUS Register

#### 1 MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG1\_STATUS Register (Offset = 8034h) [reset = 0h]

This register shows the Status of Unmasked MPU Protection Errors to R5SS0 CORE1 .

Return to [Summary Table](#)

**Table 2-339. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 8034h       |

**Figure 2-113. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG1\_STATUS Name Register**

|                                                       |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
|-------------------------------------------------------|-------------------------------------------------------|-------------------------------------------------------|-------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|
| 31                                                    | 30                                                    | 29                                                    | 28                                                    | 27                                                   | 26                                                   | 25                                                   | 24                                                   |
| RESERVED                                              |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
| NONE                                                  |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
| 0h                                                    |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
| 23                                                    | 22                                                    | 21                                                    | 20                                                    | 19                                                   | 18                                                   | 17                                                   | 16                                                   |
| RESERVED                                              |                                                       |                                                       |                                                       |                                                      |                                                      | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_HSM_PROT_ERR1       | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_CR5B1_AHB_PROT_ERR1 |
| NONE                                                  |                                                       |                                                       |                                                       |                                                      |                                                      | R/W                                                  | R/W                                                  |
| 0h                                                    |                                                       |                                                       |                                                       |                                                      |                                                      | 0h                                                   | 0h                                                   |
| 15                                                    | 14                                                    | 13                                                    | 12                                                    | 11                                                   | 10                                                   | 9                                                    | 8                                                    |
| MPU_PROT_INTR_ERRAGG1_STATUS_MPU_CR5A1_AHB_PROT_ERR1  | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_CR5B0_AHB_PROT_ERR1  | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_CR5A0_AHB_PROT_ERR1  | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_SCRM2SCR1_PROT_ERR1  | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_SCRM2SCR0_PROT_ERR1 | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_QSPI_PROT_ERR1      | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_MBOX_PROT_ERR1      | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_DTHE_A_PROT_ERR1    |
| R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                  | R/W                                                  | R/W                                                  | R/W                                                  |
| 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                   | 0h                                                   | 0h                                                   | 0h                                                   |
| 7                                                     | 6                                                     | 5                                                     | 4                                                     | 3                                                    | 2                                                    | 1                                                    | 0                                                    |
| MPU_PROT_INTR_ERRAGG1_STATUS_MPU_CR5B1_AXIS_PROT_ERR1 | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_CR5A1_AXIS_PROT_ERR1 | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_CR5B0_AXIS_PROT_ERR1 | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_CR5A0_AXIS_PROT_ERR1 | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_L2_BANK_D_PROT_ERR1 | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_L2_BANK_C_PROT_ERR1 | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_L2_BANK_B_PROT_ERR1 | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_L2_BANK_A_PROT_ERR1 |
| R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                  | R/W                                                  | R/W                                                  | R/W                                                  |
| 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                   | 0h                                                   | 0h                                                   | 0h                                                   |

**Table 2-341. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG1\_STATUS Register Field Descriptions**

| Bit   | Field                                                | Type | Reset | Description                                                                                                                        |
|-------|------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                                             | NONE | 0h    | Reserved                                                                                                                           |
| 17    | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_HSM_PROT_ERR1       | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 16    | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_CR5B1_AHB_PROT_ERR1 | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 15    | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_CR5A1_AHB_PROT_ERR1 | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |

**Table 2-341. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG1\_STATUS Register Field Descriptions (continued)**

| Bit | Field                                                   | Type | Reset | Description                                                                                                                        |
|-----|---------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 14  | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_CR5_B0_AHB_PROT_ERR1   | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 13  | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_CR5_A0_AHB_PROT_ERR1   | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 12  | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_SCR_M2SCR_P1_PROT_ERR1 | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 11  | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_SCR_M2SCR_P0_PROT_ERR1 | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 10  | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_QSPI_PROT_ERR1         | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 9   | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_MBOX_PROT_ERR1         | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 8   | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_DTHE_A_PROT_ERR1       | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 7   | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_CR5_B1_AXIS_PROT_ERR1  | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 6   | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_CR5_A1_AXIS_PROT_ERR1  | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 5   | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_CR5_B0_AXIS_PROT_ERR1  | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 4   | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_CR5_A0_AXIS_PROT_ERR1  | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 3   | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_L2_BANK_D_PROT_ERR1    | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 2   | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_L2_BANK_C_PROT_ERR1    | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 1   | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_L2_BANK_B_PROT_ERR1    | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |

**Table 2-341. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG1\_STATUS Register Field Descriptions (continued)**

| Bit | Field                                                | Type | Reset | Description                                                                                                                             |
|-----|------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 0   | MPU_PROT_INTR_ERRAGG1_STATUS_MPU_L2_BANK_A_PROT_ERR1 | R/W  | 0h    | Status of Error from MPU_PROT_INTR.<br>Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK<br>Write 0x1 to clear this Error. |

### 2.2.2.114 MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG1\_STATUS\_RAW Register

#### 1 MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG1\_STATUS\_RAW Register (Offset = 8038h) [reset = 0h]

This register shows the Status of all MPU Protection Errors.

Return to [Summary Table](#)

**Table 2-342. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 8038h       |

**Figure 2-114. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG1\_STATUS\_RAW Name Register**

| 31                                                                           | 30                                                                           | 29                                                                           | 28                                                                             | 27                                                                             | 26                                                                          | 25                                                                          | 24                                                                          |
|------------------------------------------------------------------------------|------------------------------------------------------------------------------|------------------------------------------------------------------------------|--------------------------------------------------------------------------------|--------------------------------------------------------------------------------|-----------------------------------------------------------------------------|-----------------------------------------------------------------------------|-----------------------------------------------------------------------------|
| RESERVED                                                                     |                                                                              |                                                                              |                                                                                |                                                                                |                                                                             |                                                                             |                                                                             |
| NONE                                                                         |                                                                              |                                                                              |                                                                                |                                                                                |                                                                             |                                                                             |                                                                             |
| 0h                                                                           |                                                                              |                                                                              |                                                                                |                                                                                |                                                                             |                                                                             |                                                                             |
| 23                                                                           | 22                                                                           | 21                                                                           | 20                                                                             | 19                                                                             | 18                                                                          | 17                                                                          | 16                                                                          |
| RESERVED                                                                     |                                                                              |                                                                              |                                                                                |                                                                                |                                                                             | MPU_PROT_IN<br>TR_ERRAGG1<br>STATUS_RAW<br>_MPU_HSM_P<br>ROT_ERR1           | MPU_PROT_IN<br>TR_ERRAGG1<br>STATUS_RAW<br>_MPU_CR5B1_<br>AHB_PROT_E<br>RR1 |
| NONE                                                                         |                                                                              |                                                                              |                                                                                |                                                                                |                                                                             | R/W                                                                         | R/W                                                                         |
| 0h                                                                           |                                                                              |                                                                              |                                                                                |                                                                                |                                                                             | 0h                                                                          | 0h                                                                          |
| 15                                                                           | 14                                                                           | 13                                                                           | 12                                                                             | 11                                                                             | 10                                                                          | 9                                                                           | 8                                                                           |
| MPU_PROT_IN<br>TR_ERRAGG1<br>STATUS_RAW<br>_MPU_CR5A1_<br>AHB_PROT_E<br>RR1  | MPU_PROT_IN<br>TR_ERRAGG1<br>STATUS_RAW<br>_MPU_CR5B0_<br>AHB_PROT_E<br>RR1  | MPU_PROT_IN<br>TR_ERRAGG1<br>STATUS_RAW<br>_MPU_CR5A0_<br>AHB_PROT_E<br>RR1  | MPU_PROT_IN<br>TR_ERRAGG1<br>STATUS_RAW<br>_MPU_SCRM2_<br>SCRIP1_PROT_<br>ERR1 | MPU_PROT_IN<br>TR_ERRAGG1<br>STATUS_RAW<br>_MPU_SCRM2_<br>SCRIP0_PROT_<br>ERR1 | MPU_PROT_IN<br>TR_ERRAGG1<br>STATUS_RAW<br>_MPU_QSPI_P<br>ROT_ERR1          | MPU_PROT_IN<br>TR_ERRAGG1<br>STATUS_RAW<br>_MPU_MBOX_<br>PROT_ERR1          | MPU_PROT_IN<br>TR_ERRAGG1<br>STATUS_RAW<br>_MPU_DTHE_<br>A_PROT_ERR1        |
| R/W                                                                          | R/W                                                                          | R/W                                                                          | R/W                                                                            | R/W                                                                            | R/W                                                                         | R/W                                                                         | R/W                                                                         |
| 0h                                                                           | 0h                                                                           | 0h                                                                           | 0h                                                                             | 0h                                                                             | 0h                                                                          | 0h                                                                          | 0h                                                                          |
| 7                                                                            | 6                                                                            | 5                                                                            | 4                                                                              | 3                                                                              | 2                                                                           | 1                                                                           | 0                                                                           |
| MPU_PROT_IN<br>TR_ERRAGG1<br>STATUS_RAW<br>_MPU_CR5B1_<br>AXIS_PROT_E<br>RR1 | MPU_PROT_IN<br>TR_ERRAGG1<br>STATUS_RAW<br>_MPU_CR5A1_<br>AXIS_PROT_E<br>RR1 | MPU_PROT_IN<br>TR_ERRAGG1<br>STATUS_RAW<br>_MPU_CR5B0_<br>AXIS_PROT_E<br>RR1 | MPU_PROT_IN<br>TR_ERRAGG1<br>STATUS_RAW<br>_MPU_CR5A0_<br>AXIS_PROT_E<br>RR1   | MPU_PROT_IN<br>TR_ERRAGG1<br>STATUS_RAW<br>_MPU_L2_BAN<br>K_D_PROT_ER<br>R1    | MPU_PROT_IN<br>TR_ERRAGG1<br>STATUS_RAW<br>_MPU_L2_BAN<br>K_C_PROT_ER<br>R1 | MPU_PROT_IN<br>TR_ERRAGG1<br>STATUS_RAW<br>_MPU_L2_BAN<br>K_B_PROT_ER<br>R1 | MPU_PROT_IN<br>TR_ERRAGG1<br>STATUS_RAW<br>_MPU_L2_BAN<br>K_A_PROT_ER<br>R1 |
| R/W                                                                          | R/W                                                                          | R/W                                                                          | R/W                                                                            | R/W                                                                            | R/W                                                                         | R/W                                                                         | R/W                                                                         |
| 0h                                                                           | 0h                                                                           | 0h                                                                           | 0h                                                                             | 0h                                                                             | 0h                                                                          | 0h                                                                          | 0h                                                                          |

**Table 2-344. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG1\_STATUS\_RAW Register Field Descriptions**

| Bit   | Field                                                    | Type | Reset | Description                                                                                                                  |
|-------|----------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                                                 | NONE | 0h    | Reserved                                                                                                                     |
| 17    | MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_HSM_PROT_ERR1       | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 16    | MPU_PROT_INTR_ERRAGG1_STATUS_RAW_MPU_CR5B1_AHB_PROT_ERR1 | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |



**Table 2-344. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG1\_STATUS\_RAW Register Field Descriptions  
(continued)**

| Bit | Field                                                      | Type | Reset | Description                                                                                                                  |
|-----|------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 15  | MPU_PROT_INTR_ERRAGG1_STATUS_RAW MPU_CR5A1_AHB_PROT_ERR1   | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 14  | MPU_PROT_INTR_ERRAGG1_STATUS_RAW MPU_CR5B0_AHB_PROT_ERR1   | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 13  | MPU_PROT_INTR_ERRAGG1_STATUS_RAW MPU_CR5A0_AHB_PROT_ERR1   | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 12  | MPU_PROT_INTR_ERRAGG1_STATUS_RAW MPU_SCRM2SCRIP1_PROT_ERR1 | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 11  | MPU_PROT_INTR_ERRAGG1_STATUS_RAW MPU_SCRM2SCRIP0_PROT_ERR1 | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 10  | MPU_PROT_INTR_ERRAGG1_STATUS_RAW MPU_QSPI_PROT_ERR1        | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 9   | MPU_PROT_INTR_ERRAGG1_STATUS_RAW MPU_MBOX_PROT_ERR1        | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 8   | MPU_PROT_INTR_ERRAGG1_STATUS_RAW MPU_DTHE_A_PROT_ERR1      | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 7   | MPU_PROT_INTR_ERRAGG1_STATUS_RAW MPU_CR5B1_AXIS_PROT_ERR1  | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 6   | MPU_PROT_INTR_ERRAGG1_STATUS_RAW MPU_CR5A1_AXIS_PROT_ERR1  | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 5   | MPU_PROT_INTR_ERRAGG1_STATUS_RAW MPU_CR5B0_AXIS_PROT_ERR1  | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 4   | MPU_PROT_INTR_ERRAGG1_STATUS_RAW MPU_CR5A0_AXIS_PROT_ERR1  | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 3   | MPU_PROT_INTR_ERRAGG1_STATUS_RAW MPU_L2_BANK_D_PROT_ERR1   | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 2   | MPU_PROT_INTR_ERRAGG1_STATUS_RAW MPU_L2_BANK_C_PROT_ERR1   | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 1   | MPU_PROT_INTR_ERRAGG1_STATUS_RAW MPU_L2_BANK_B_PROT_ERR1   | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |

**Table 2-344. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG1\_STATUS\_RAW Register Field Descriptions  
(continued)**

| Bit | Field                                                    | Type | Reset | Description                                                                                                                  |
|-----|----------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 0   | MPU_PROT_INTR_ERRAGG1_STATUS_RAW MPU_L2_BANK_A_PROT_ERR1 | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |

### 2.2.2.115 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_MBOX\_WRITE\_DONE Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_MBOX\_WRITE\_DONE Register (Offset = C000h) [reset = 0h]

This register is used by R5SS1 Core 0 to generate Mailbox interrupt to Recipient CPU.

Return to [Summary Table](#)

**Table 2-345. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 C000h       |

**Figure 2-115. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_MBOX\_WRITE\_DONE Name Register**

| 31       | 30 | 29 | 28                               | 27       | 26 | 25 | 24                               |
|----------|----|----|----------------------------------|----------|----|----|----------------------------------|
| RESERVED |    |    | MSS_CR5A1_MBOX_WRITE_DONE_PROC_7 | RESERVED |    |    | MSS_CR5A1_MBOX_WRITE_DONE_PROC_6 |
| NONE     |    |    | R/W                              | NONE     |    |    | R/W                              |
| 0h       |    |    | 0h                               | 0h       |    |    | 0h                               |
| 23       | 22 | 21 | 20                               | 19       | 18 | 17 | 16                               |
| RESERVED |    |    | MSS_CR5A1_MBOX_WRITE_DONE_PROC_5 | RESERVED |    |    | MSS_CR5A1_MBOX_WRITE_DONE_PROC_4 |
| NONE     |    |    | R/W                              | NONE     |    |    | R/W                              |
| 0h       |    |    | 0h                               | 0h       |    |    | 0h                               |
| 15       | 14 | 13 | 12                               | 11       | 10 | 9  | 8                                |
| RESERVED |    |    | MSS_CR5A1_MBOX_WRITE_DONE_PROC_3 | RESERVED |    |    | MSS_CR5A1_MBOX_WRITE_DONE_PROC_2 |
| NONE     |    |    | R/W                              | NONE     |    |    | R/W                              |
| 0h       |    |    | 0h                               | 0h       |    |    | 0h                               |
| 7        | 6  | 5  | 4                                | 3        | 2  | 1  | 0                                |
| RESERVED |    |    | MSS_CR5A1_MBOX_WRITE_DONE_PROC_1 | RESERVED |    |    | MSS_CR5A1_MBOX_WRITE_DONE_PROC_0 |
| NONE     |    |    | R/W                              | NONE     |    |    | R/W                              |
| 0h       |    |    | 0h                               | 0h       |    |    | 0h                               |

**Table 2-347. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_MBOX\_WRITE\_DONE Register Field Descriptions**

| Bit   | Field                            | Type | Reset | Description                                                                                                             |
|-------|----------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 28    | MSS_CR5A1_MBOX_WRITE_DONE_PROC_7 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 7 |
| 27:25 | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 24    | MSS_CR5A1_MBOX_WRITE_DONE_PROC_6 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 6 |
| 23:21 | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 20    | MSS_CR5A1_MBOX_WRITE_DONE_PROC_5 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 5 |

**Table 2-347. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_MBOX\_WRITE\_DONE Register Field Descriptions  
(continued)**

| Bit   | Field                            | Type | Reset | Description                                                                                                             |
|-------|----------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------|
| 19:17 | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 16    | MSS_CR5A1_MBOX_WRITE_DONE_PROC_4 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 4 |
| 15:13 | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 12    | MSS_CR5A1_MBOX_WRITE_DONE_PROC_3 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 3 |
| 11:9  | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 8     | MSS_CR5A1_MBOX_WRITE_DONE_PROC_2 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 2 |
| 7:5   | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 4     | MSS_CR5A1_MBOX_WRITE_DONE_PROC_1 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 1 |
| 3:1   | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 0     | MSS_CR5A1_MBOX_WRITE_DONE_PROC_0 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 0 |

### 2.2.2.116 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_MBOX\_READ\_REQ Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_MBOX\_READ\_REQ Register (Offset = C004h) [reset = 0h]

This register is used by R5SS1 Core 0 to know the Sender of Mailbox Interrupt as well as clear it.

Return to [Summary Table](#)

**Table 2-348. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 C004h       |

**Figure 2-116. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_MBOX\_READ\_REQ Name Register**

| 31       | 30 | 29 | 28                             | 27       | 26 | 25 | 24                             |
|----------|----|----|--------------------------------|----------|----|----|--------------------------------|
| RESERVED |    |    | MSS_CR5A1_MBOX_READ_REQ_PROC_7 | RESERVED |    |    | MSS_CR5A1_MBOX_READ_REQ_PROC_6 |
| NONE     |    |    | R/W                            | NONE     |    |    | R/W                            |
| 0h       |    |    | 0h                             | 0h       |    |    | 0h                             |
| 23       | 22 | 21 | 20                             | 19       | 18 | 17 | 16                             |
| RESERVED |    |    | MSS_CR5A1_MBOX_READ_REQ_PROC_5 | RESERVED |    |    | MSS_CR5A1_MBOX_READ_REQ_PROC_4 |
| NONE     |    |    | R/W                            | NONE     |    |    | R/W                            |
| 0h       |    |    | 0h                             | 0h       |    |    | 0h                             |
| 15       | 14 | 13 | 12                             | 11       | 10 | 9  | 8                              |
| RESERVED |    |    | MSS_CR5A1_MBOX_READ_REQ_PROC_3 | RESERVED |    |    | MSS_CR5A1_MBOX_READ_REQ_PROC_2 |
| NONE     |    |    | R/W                            | NONE     |    |    | R/W                            |
| 0h       |    |    | 0h                             | 0h       |    |    | 0h                             |
| 7        | 6  | 5  | 4                              | 3        | 2  | 1  | 0                              |
| RESERVED |    |    | MSS_CR5A1_MBOX_READ_REQ_PROC_1 | RESERVED |    |    | MSS_CR5A1_MBOX_READ_REQ_PROC_0 |
| NONE     |    |    | R/W                            | NONE     |    |    | R/W                            |
| 0h       |    |    | 0h                             | 0h       |    |    | 0h                             |

**Table 2-350. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_MBOX\_READ\_REQ Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                       |
|-------|--------------------------------|------|-------|-----------------------------------------------------------------------------------|
| 31:29 | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 28    | MSS_CR5A1_MBOX_READ_REQ_PROC_7 | R/W  | 0h    | This is request from processor 7 to mss_cr5a. Requesting it to read from mailbox. |
| 27:25 | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 24    | MSS_CR5A1_MBOX_READ_REQ_PROC_6 | R/W  | 0h    | This is request from processor 6 to mss_cr5a. Requesting it to read from mailbox. |
| 23:21 | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 20    | MSS_CR5A1_MBOX_READ_REQ_PROC_5 | R/W  | 0h    | This is request from processor 5 to mss_cr5a. Requesting it to read from mailbox. |
| 19:17 | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 16    | MSS_CR5A1_MBOX_READ_REQ_PROC_4 | R/W  | 0h    | This is request from processor 4 to mss_cr5a. Requesting it to read from mailbox. |
| 15:13 | RESERVED                       | NONE | 0h    | Reserved                                                                          |

**Table 2-350. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_MBOX\_READ\_REQ Register Field Descriptions  
(continued)**

| Bit  | Field                          | Type | Reset | Description                                                                       |
|------|--------------------------------|------|-------|-----------------------------------------------------------------------------------|
| 12   | MSS_CR5A1_MBOX_READ_REQ_PROC_3 | R/W  | 0h    | This is request from processor 3 to mss_cr5a. Requesting it to read from mailbox. |
| 11:9 | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 8    | MSS_CR5A1_MBOX_READ_REQ_PROC_2 | R/W  | 0h    | This is request from processor 2 to mss_cr5a. Requesting it to read from mailbox. |
| 7:5  | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 4    | MSS_CR5A1_MBOX_READ_REQ_PROC_1 | R/W  | 0h    | This is request from processor 1 to mss_cr5a. Requesting it to read from mailbox. |
| 3:1  | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 0    | MSS_CR5A1_MBOX_READ_REQ_PROC_0 | R/W  | 0h    | This is request from processor 0 to mss_cr5a. Requesting it to read from mailbox. |

### 2.2.2.117 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_MBOX\_READ\_DONE\_ACK Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_MBOX\_READ\_DONE\_ACK Register (Offset = C008h) [reset = 0h]

This register is used by R5SS1 Core 0 to generate Mailbox Read acknowledgement to the Sender CPU.

Return to [Summary Table](#)

**Table 2-351. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 C008h       |

**Figure 2-117. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_MBOX\_READ\_DONE\_ACK Name Register**

|                                   |    |    |    |    |    |    |    |
|-----------------------------------|----|----|----|----|----|----|----|
| 31                                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                          |    |    |    |    |    |    |    |
| NONE                              |    |    |    |    |    |    |    |
| 0h                                |    |    |    |    |    |    |    |
| 23                                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                          |    |    |    |    |    |    |    |
| NONE                              |    |    |    |    |    |    |    |
| 0h                                |    |    |    |    |    |    |    |
| 15                                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED                          |    |    |    |    |    |    |    |
| NONE                              |    |    |    |    |    |    |    |
| 0h                                |    |    |    |    |    |    |    |
| 7                                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A1_MBOX_READ_DONE_ACK_PROC |    |    |    |    |    |    |    |
| R/W                               |    |    |    |    |    |    |    |
| 0h                                |    |    |    |    |    |    |    |

**Table 2-353. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_MBOX\_READ\_DONE\_ACK Register Field Descriptions**

| Bit  | Field                             | Type | Reset | Description                                                                                                            |
|------|-----------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED                          | NONE | 0h    | Reserved                                                                                                               |
| 7:0  | MSS_CR5A1_MBOX_READ_DONE_ACK_PROC | R/W  | 0h    | Write pulse bit field:<br>For bits 0 to 7: Writing 1'b1 : Generates pulse interrupt to corresponding proc from MSS_CR5 |

### 2.2.2.118 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_MBOX\_READ\_DONE Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_MBOX\_READ\_DONE Register (Offset = C00Ch) [reset = 0h]

This register is used by R5SS1 Core 0 to know that the Receiver CPU has read the Mailbox and Acked. It is also used to clear the Read Done Interrupt.

Return to [Summary Table](#)

**Table 2-354. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 C00Ch       |

**Figure 2-118. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_MBOX\_READ\_DONE Name Register**

| 31       | 30 | 29 | 28                              | 27       | 26 | 25 | 24                              |
|----------|----|----|---------------------------------|----------|----|----|---------------------------------|
| RESERVED |    |    | MSS_CR5A1_MBOX_READ_DONE_PROC_7 | RESERVED |    |    | MSS_CR5A1_MBOX_READ_DONE_PROC_6 |
| NONE     |    |    | R/W                             | NONE     |    |    | R/W                             |
| 0h       |    |    | 0h                              | 0h       |    |    | 0h                              |
| 23       | 22 | 21 | 20                              | 19       | 18 | 17 | 16                              |
| RESERVED |    |    | MSS_CR5A1_MBOX_READ_DONE_PROC_5 | RESERVED |    |    | MSS_CR5A1_MBOX_READ_DONE_PROC_4 |
| NONE     |    |    | R/W                             | NONE     |    |    | R/W                             |
| 0h       |    |    | 0h                              | 0h       |    |    | 0h                              |
| 15       | 14 | 13 | 12                              | 11       | 10 | 9  | 8                               |
| RESERVED |    |    | MSS_CR5A1_MBOX_READ_DONE_PROC_3 | RESERVED |    |    | MSS_CR5A1_MBOX_READ_DONE_PROC_2 |
| NONE     |    |    | R/W                             | NONE     |    |    | R/W                             |
| 0h       |    |    | 0h                              | 0h       |    |    | 0h                              |
| 7        | 6  | 5  | 4                               | 3        | 2  | 1  | 0                               |
| RESERVED |    |    | MSS_CR5A1_MBOX_READ_DONE_PROC_1 | RESERVED |    |    | MSS_CR5A1_MBOX_READ_DONE_PROC_0 |
| NONE     |    |    | R/W                             | NONE     |    |    | R/W                             |
| 0h       |    |    | 0h                              | 0h       |    |    | 0h                              |

**Table 2-356. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_MBOX\_READ\_DONE Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                 |
|-------|---------------------------------|------|-------|---------------------------------------------------------------------------------------------|
| 31:29 | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 28    | MSS_CR5A1_MBOX_READ_DONE_PROC_7 | R/W  | 0h    | This register should be written once finishing Reading from proc7's mailbox written by CR5A |
| 27:25 | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 24    | MSS_CR5A1_MBOX_READ_DONE_PROC_6 | R/W  | 0h    | This register should be written once finishing Reading from proc6's mailbox written by CR5A |
| 23:21 | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 20    | MSS_CR5A1_MBOX_READ_DONE_PROC_5 | R/W  | 0h    | This register should be written once finishing Reading from proc5's mailbox written by CR5A |
| 19:17 | RESERVED                        | NONE | 0h    | Reserved                                                                                    |



**Table 2-356. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_MBOX\_READ\_DONE Register Field Descriptions  
(continued)**

| Bit   | Field                           | Type | Reset | Description                                                                                 |
|-------|---------------------------------|------|-------|---------------------------------------------------------------------------------------------|
| 16    | MSS_CR5A1_MBOX_READ_DONE_PROC_4 | R/W  | 0h    | This register should be written once finishing Reading from proc4's mailbox written by CR5A |
| 15:13 | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 12    | MSS_CR5A1_MBOX_READ_DONE_PROC_3 | R/W  | 0h    | This register should be written once finishing Reading from proc3's mailbox written by CR5A |
| 11:9  | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 8     | MSS_CR5A1_MBOX_READ_DONE_PROC_2 | R/W  | 0h    | This register should be written once finishing Reading from proc2's mailbox written by CR5A |
| 7:5   | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 4     | MSS_CR5A1_MBOX_READ_DONE_PROC_1 | R/W  | 0h    | This register should be written once finishing Reading from proc1's mailbox written by CR5A |
| 3:1   | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 0     | MSS_CR5A1_MBOX_READ_DONE_PROC_0 | R/W  | 0h    | This register should be written once finishing Reading from proc0's mailbox written by CR5A |

### 2.2.2.119 MSS\_CTRL\_MSS\_SW\_INT\_R5SS1\_CORE0 Register

#### 1 MSS\_CTRL\_MSS\_SW\_INT\_R5SS1\_CORE0 Register (Offset = C010h) [reset = 0h]

This Register is used to generate a S/W Triggered Interrupt to R5SS1 Core0.

Return to [Summary Table](#)

**Table 2-357. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 C010h       |

**Figure 2-119. MSS\_CTRL\_MSS\_SW\_INT\_R5SS1\_CORE0 Name Register**

|          |    |    |    |    |    |    |                              |
|----------|----|----|----|----|----|----|------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                           |
| RESERVED |    |    |    |    |    |    |                              |
| NONE     |    |    |    |    |    |    |                              |
| 0h       |    |    |    |    |    |    |                              |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                           |
| RESERVED |    |    |    |    |    |    |                              |
| NONE     |    |    |    |    |    |    |                              |
| 0h       |    |    |    |    |    |    |                              |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                            |
| RESERVED |    |    |    |    |    |    |                              |
| NONE     |    |    |    |    |    |    |                              |
| 0h       |    |    |    |    |    |    |                              |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                            |
| RESERVED |    |    |    |    |    |    | MSS_SW_INT_R5SS1_CORE0_PULSE |
| NONE     |    |    |    |    |    |    | R/W                          |
| 0h       |    |    |    |    |    |    | 0h                           |

**Table 2-359. MSS\_CTRL\_MSS\_SW\_INT\_R5SS1\_CORE0 Register Field Descriptions**

| Bit  | Field                        | Type | Reset | Description                                                                                        |
|------|------------------------------|------|-------|----------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED                     | NONE | 0h    | Reserved                                                                                           |
| 0    | MSS_SW_INT_R5SS1_CORE0_PULSE | R/W  | 0h    | Write_pulse bit field:<br>Writing 1'b1 to each bit will trigger MSS_SW_INT respectively to CR5A/B. |

### 2.2.2.120 MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG2\_MASK Register

#### 1 MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG2\_MASK Register (Offset = C020h) [reset = 0h]

This register Masks selected interrupt sources from generating MPU Address Error Interrupt to R5SS1 CORE0 .

Return to [Summary Table](#)

**Table 2-360. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 C020h       |

**Figure 2-120. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG2\_MASK Name Register**

|                                                     |                                                     |                                                     |                                                      |                                                      |                                                    |                                                    |                                                    |
|-----------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|------------------------------------------------------|------------------------------------------------------|----------------------------------------------------|----------------------------------------------------|----------------------------------------------------|
| 31                                                  | 30                                                  | 29                                                  | 28                                                   | 27                                                   | 26                                                 | 25                                                 | 24                                                 |
| RESERVED                                            |                                                     |                                                     |                                                      |                                                      |                                                    |                                                    |                                                    |
| NONE                                                |                                                     |                                                     |                                                      |                                                      |                                                    |                                                    |                                                    |
| 0h                                                  |                                                     |                                                     |                                                      |                                                      |                                                    |                                                    |                                                    |
| 23                                                  | 22                                                  | 21                                                  | 20                                                   | 19                                                   | 18                                                 | 17                                                 | 16                                                 |
| RESERVED                                            |                                                     |                                                     |                                                      |                                                      |                                                    | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_HSM_ADDR_ERR2       | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_CR5B1_AHB_ADDR_ERR2 |
| NONE                                                |                                                     |                                                     |                                                      |                                                      |                                                    | R/W                                                | R/W                                                |
| 0h                                                  |                                                     |                                                     |                                                      |                                                      |                                                    | 0h                                                 | 0h                                                 |
| 15                                                  | 14                                                  | 13                                                  | 12                                                   | 11                                                   | 10                                                 | 9                                                  | 8                                                  |
| MPU_ADDR_INTR_ERRAGG2_MASK_MPU_CR5A1_AHB_ADDR_ERR2  | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_CR5B0_AHB_ADDR_ERR2  | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_CR5A0_AHB_ADDR_ERR2  | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_SCRM2SCRIP1_ADDR_ERR2 | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_SCRM2SCRIP0_ADDR_ERR2 | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_QSPI_ADDR_ERR2      | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_MBOX_ADDR_ERR2      | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_DTHE_A_ADDR_ERR2    |
| R/W                                                 | R/W                                                 | R/W                                                 | R/W                                                  | R/W                                                  | R/W                                                | R/W                                                | R/W                                                |
| 0h                                                  | 0h                                                  | 0h                                                  | 0h                                                   | 0h                                                   | 0h                                                 | 0h                                                 | 0h                                                 |
| 7                                                   | 6                                                   | 5                                                   | 4                                                    | 3                                                    | 2                                                  | 1                                                  | 0                                                  |
| MPU_ADDR_INTR_ERRAGG2_MASK_MPU_CR5B1_AXIS_ADDR_ERR2 | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_CR5A1_AXIS_ADDR_ERR2 | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_CR5B0_AXIS_ADDR_ERR2 | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_CR5A0_AXIS_ADDR_ERR2  | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_L2_BANK_D_ADDR_ERR2   | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_L2_BANK_C_ADDR_ERR2 | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_L2_BANK_B_ADDR_ERR2 | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_L2_BANK_A_ADDR_ERR2 |
| R/W                                                 | R/W                                                 | R/W                                                 | R/W                                                  | R/W                                                  | R/W                                                | R/W                                                | R/W                                                |
| 0h                                                  | 0h                                                  | 0h                                                  | 0h                                                   | 0h                                                   | 0h                                                 | 0h                                                 | 0h                                                 |

**Table 2-362. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG2\_MASK Register Field Descriptions**

| Bit   | Field                                              | Type | Reset | Description                                                                                                                  |
|-------|----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                                           | NONE | 0h    | Reserved                                                                                                                     |
| 17    | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_HSM_ADDR_ERR2       | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 16    | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_CR5B1_AHB_ADDR_ERR2 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 15    | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_CR5A1_AHB_ADDR_ERR2 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |

**Table 2-362. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG2\_MASK Register Field Descriptions (continued)**

| Bit | Field                                               | Type | Reset | Description                                                                                                                  |
|-----|-----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 14  | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_CR5B0_AHB_ADDR_ERR2  | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 13  | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_CR5A0_AHB_ADDR_ERR2  | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 12  | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_SCRM2SCR1_ADDR_ERR2  | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 11  | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_SCRM2SCR0_ADDR_ERR2  | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 10  | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_QSPI_ADDR_ERR2       | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 9   | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_MBOX_ADDR_ERR2       | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 8   | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_DTHEA_ADDR_ERR2      | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 7   | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_CR5B1_AXIS_ADDR_ERR2 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 6   | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_CR5A1_AXIS_ADDR_ERR2 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 5   | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_CR5B0_AXIS_ADDR_ERR2 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 4   | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_CR5A0_AXIS_ADDR_ERR2 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 3   | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_L2_BA_NK_D_ADDR_ERR2 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 2   | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_L2_BA_NK_C_ADDR_ERR2 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 1   | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_L2_BA_NK_B_ADDR_ERR2 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |

**Table 2-362. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG2\_MASK Register Field Descriptions (continued)**

| Bit | Field                                              | Type | Reset | Description                                                                                                                  |
|-----|----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 0   | MPU_ADDR_INTR_ERRAGG2_MASK_MPU_L2_BANK_A_ADDR_ERR2 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |

### 2.2.2.121 MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG2\_STATUS Register

#### 1 MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG2\_STATUS Register (Offset = C024h) [reset = 0h]

This register shows the Status of Unmasked MPU Address Errors to R5SS1 Core0 .

Return to [Summary Table](#)

**Table 2-363. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 C024h       |

**Figure 2-121. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG2\_STATUS Name Register**

|                                                       |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
|-------------------------------------------------------|-------------------------------------------------------|-------------------------------------------------------|-------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|
| 31                                                    | 30                                                    | 29                                                    | 28                                                    | 27                                                   | 26                                                   | 25                                                   | 24                                                   |
| RESERVED                                              |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
| NONE                                                  |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
| 0h                                                    |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
| 23                                                    | 22                                                    | 21                                                    | 20                                                    | 19                                                   | 18                                                   | 17                                                   | 16                                                   |
| RESERVED                                              |                                                       |                                                       |                                                       |                                                      |                                                      | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_HSM_ADDR_ERR2       | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_CR5B1_AHB_ADDR_ERR2 |
| NONE                                                  |                                                       |                                                       |                                                       |                                                      |                                                      | R/W                                                  | R/W                                                  |
| 0h                                                    |                                                       |                                                       |                                                       |                                                      |                                                      | 0h                                                   | 0h                                                   |
| 15                                                    | 14                                                    | 13                                                    | 12                                                    | 11                                                   | 10                                                   | 9                                                    | 8                                                    |
| MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_CR5A1_AHB_ADDR_ERR2  | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_CR5B0_AHB_ADDR_ERR2  | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_CR5A0_AHB_ADDR_ERR2  | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_SCRM2SCR1_ADDR_ERR2  | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_SCRM2SCR0_ADDR_ERR2 | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_QSPI_ADDR_ERR2      | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_MBOX_ADDR_ERR2      | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_DTHE_A_ADDR_ERR2    |
| R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                  | R/W                                                  | R/W                                                  | R/W                                                  |
| 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                   | 0h                                                   | 0h                                                   | 0h                                                   |
| 7                                                     | 6                                                     | 5                                                     | 4                                                     | 3                                                    | 2                                                    | 1                                                    | 0                                                    |
| MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_CR5B1_AXIS_ADDR_ERR2 | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_CR5A1_AXIS_ADDR_ERR2 | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_CR5B0_AXIS_ADDR_ERR2 | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_CR5A0_AXIS_ADDR_ERR2 | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_L2_BANK_D_ADDR_ERR2 | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_L2_BANK_C_ADDR_ERR2 | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_L2_BANK_B_ADDR_ERR2 | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_L2_BANK_A_ADDR_ERR2 |
| R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                  | R/W                                                  | R/W                                                  | R/W                                                  |
| 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                   | 0h                                                   | 0h                                                   | 0h                                                   |

**Table 2-365. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG2\_STATUS Register Field Descriptions**

| Bit   | Field                                                | Type | Reset | Description                                                                                                                        |
|-------|------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                                             | NONE | 0h    | Reserved                                                                                                                           |
| 17    | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_HSM_ADDR_ERR2       | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 16    | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_CR5B1_AHB_ADDR_ERR2 | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 15    | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_CR5A1_AHB_ADDR_ERR2 | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |

**Table 2-365. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG2\_STATUS Register Field Descriptions (continued)**

| Bit | Field                                                   | Type | Reset | Description                                                                                                                        |
|-----|---------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 14  | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_CR5_B0_AHB_ADDR_ERR2   | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 13  | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_CR5_A0_AHB_ADDR_ERR2   | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 12  | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_SCR_M2SCR_P1_ADDR_ERR2 | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 11  | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_SCR_M2SCR_P0_ADDR_ERR2 | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 10  | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_QSPI_ADDR_ERR2         | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 9   | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_MBOX_ADDR_ERR2         | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 8   | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_DTHE_A_ADDR_ERR2       | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 7   | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_CR5_B1_AXIS_ADDR_ERR2  | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 6   | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_CR5_A1_AXIS_ADDR_ERR2  | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 5   | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_CR5_B0_AXIS_ADDR_ERR2  | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 4   | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_CR5_A0_AXIS_ADDR_ERR2  | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 3   | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_L2_BANK_D_ADDR_ERR2    | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 2   | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_L2_BANK_C_ADDR_ERR2    | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 1   | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_L2_BANK_B_ADDR_ERR2    | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |

**Table 2-365. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG2\_STATUS Register Field Descriptions (continued)**

| Bit | Field                                                | Type | Reset | Description                                                                                                                             |
|-----|------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 0   | MPU_ADDR_INTR_ERRAGG2_STATUS_MPU_L2_BANK_A_ADDR_ERR2 | R/W  | 0h    | Status of Error from MPU_ADDR_INTR.<br>Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK<br>Write 0x1 to clear this Error. |



### 2.2.2.122 MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG2\_STATUS\_RAW Register

#### 1 MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG2\_STATUS\_RAW Register (Offset = C028h) [reset = 0h]

This register shows the Status of all MPU Address Errors.

Return to [Summary Table](#)

**Table 2-366. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 C028h       |

**Figure 2-122. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG2\_STATUS\_RAW Name Register**

|                                                           |                                                           |                                                           |                                                            |                                                            |                                                          |                                                          |                                                          |
|-----------------------------------------------------------|-----------------------------------------------------------|-----------------------------------------------------------|------------------------------------------------------------|------------------------------------------------------------|----------------------------------------------------------|----------------------------------------------------------|----------------------------------------------------------|
| 31                                                        | 30                                                        | 29                                                        | 28                                                         | 27                                                         | 26                                                       | 25                                                       | 24                                                       |
| RESERVED                                                  |                                                           |                                                           |                                                            |                                                            |                                                          |                                                          |                                                          |
| NONE                                                      |                                                           |                                                           |                                                            |                                                            |                                                          |                                                          |                                                          |
| 0h                                                        |                                                           |                                                           |                                                            |                                                            |                                                          |                                                          |                                                          |
| 23                                                        | 22                                                        | 21                                                        | 20                                                         | 19                                                         | 18                                                       | 17                                                       | 16                                                       |
| RESERVED                                                  |                                                           |                                                           |                                                            |                                                            |                                                          | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_HSM_A_DDR_ERR2      | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_CR5B1_AHB_ADDR_ERR2 |
| NONE                                                      |                                                           |                                                           |                                                            |                                                            |                                                          | R/W                                                      | R/W                                                      |
| 0h                                                        |                                                           |                                                           |                                                            |                                                            |                                                          | 0h                                                       | 0h                                                       |
| 15                                                        | 14                                                        | 13                                                        | 12                                                         | 11                                                         | 10                                                       | 9                                                        | 8                                                        |
| MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_CR5A1_AHB_ADDR_ERR2  | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_CR5B0_AHB_ADDR_ERR2  | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_CR5A0_AHB_ADDR_ERR2  | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_SCRM2_SCRP1_ADDR_ERR2 | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_SCRM2_SCRP0_ADDR_ERR2 | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_QSPI_A_DDR_ERR2     | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_MBOX_ADDR_ERR2      | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_DTHE_A_ADDR_ERR2    |
| R/W                                                       | R/W                                                       | R/W                                                       | R/W                                                        | R/W                                                        | R/W                                                      | R/W                                                      | R/W                                                      |
| 0h                                                        | 0h                                                        | 0h                                                        | 0h                                                         | 0h                                                         | 0h                                                       | 0h                                                       | 0h                                                       |
| 7                                                         | 6                                                         | 5                                                         | 4                                                          | 3                                                          | 2                                                        | 1                                                        | 0                                                        |
| MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_CR5B1_AXIS_ADDR_ERR2 | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_CR5A1_AXIS_ADDR_ERR2 | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_CR5B0_AXIS_ADDR_ERR2 | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_CR5A0_AXIS_ADDR_ERR2  | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_L2_BANK_D_ADDR_ERR2   | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_L2_BANK_C_ADDR_ERR2 | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_L2_BANK_B_ADDR_ERR2 | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_L2_BANK_A_ADDR_ERR2 |
| R/W                                                       | R/W                                                       | R/W                                                       | R/W                                                        | R/W                                                        | R/W                                                      | R/W                                                      | R/W                                                      |
| 0h                                                        | 0h                                                        | 0h                                                        | 0h                                                         | 0h                                                         | 0h                                                       | 0h                                                       | 0h                                                       |

**Table 2-368. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG2\_STATUS\_RAW Register Field Descriptions**

| Bit   | Field                                                    | Type | Reset | Description                                                                                                                  |
|-------|----------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                                                 | NONE | 0h    | Reserved                                                                                                                     |
| 17    | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_HSM_A_DDR_ERR2      | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 16    | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW_MPU_CR5B1_AHB_ADDR_ERR2 | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |

**Table 2-368. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG2\_STATUS\_RAW Register Field Descriptions  
(continued)**

| Bit | Field                                                      | Type | Reset | Description                                                                                                                  |
|-----|------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 15  | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW MPU_CR5A1_AHB_ADDR_ERR2   | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 14  | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW MPU_CR5B0_AHB_ADDR_ERR2   | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 13  | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW MPU_CR5A0_AHB_ADDR_ERR2   | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 12  | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW MPU_SCRM2SCRIP1_ADDR_ERR2 | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 11  | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW MPU_SCRM2SCRIP0_ADDR_ERR2 | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 10  | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW MPU_QSPI_ADDR_ERR2        | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 9   | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW MPU_MBOX_ADDR_ERR2        | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 8   | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW MPU_DTHE_A_ADDR_ERR2      | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 7   | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW MPU_CR5B1_AXIS_ADDR_ERR2  | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 6   | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW MPU_CR5A1_AXIS_ADDR_ERR2  | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 5   | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW MPU_CR5B0_AXIS_ADDR_ERR2  | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 4   | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW MPU_CR5A0_AXIS_ADDR_ERR2  | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 3   | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW MPU_L2_BANK_D_ADDR_ERR2   | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 2   | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW MPU_L2_BANK_C_ADDR_ERR2   | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 1   | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW MPU_L2_BANK_B_ADDR_ERR2   | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |

**Table 2-368. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG2\_STATUS\_RAW Register Field Descriptions  
(continued)**

| Bit | Field                                                    | Type | Reset | Description                                                                                                                  |
|-----|----------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 0   | MPU_ADDR_INTR_ERRAGG2_STATUS_RAW MPU_L2_BANK_A_ADDR_ERR2 | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |

### 2.2.2.123 MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG2\_MASK Register

#### 1 MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG2\_MASK Register (Offset = C030h) [reset = 0h]

This register Masks selected interrupt sources from generating MPU Protection Error Interrupt to R5SS1 CORE0 .

Return to [Summary Table](#)

**Table 2-369. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 C030h       |

**Figure 2-123. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG2\_MASK Name Register**

| 31                                                  | 30                                                  | 29                                                  | 28                                                  | 27                                                  | 26                                                  | 25                                                  | 24                                                  |
|-----------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|
| RESERVED                                            |                                                     |                                                     |                                                     |                                                     |                                                     |                                                     |                                                     |
| NONE                                                |                                                     |                                                     |                                                     |                                                     |                                                     |                                                     |                                                     |
| 0h                                                  |                                                     |                                                     |                                                     |                                                     |                                                     |                                                     |                                                     |
| 23                                                  | 22                                                  | 21                                                  | 20                                                  | 19                                                  | 18                                                  | 17                                                  | 16                                                  |
| RESERVED                                            |                                                     |                                                     |                                                     |                                                     |                                                     | MPU_PROT_INTR_ERRAGG2_MASK_MPU_HSM_PROT_ERR2        | MPU_PROT_INTR_ERRAGG2_MASK_MPU_CR5B1_AHB_PROT_ERR2  |
| NONE                                                |                                                     |                                                     |                                                     |                                                     |                                                     | R/W                                                 | R/W                                                 |
| 0h                                                  |                                                     |                                                     |                                                     |                                                     |                                                     | 0h                                                  | 0h                                                  |
| 15                                                  | 14                                                  | 13                                                  | 12                                                  | 11                                                  | 10                                                  | 9                                                   | 8                                                   |
| MPU_PROT_INTR_ERRAGG2_MASK_MPU_CR5A1_AHB_PROT_ERR2  | MPU_PROT_INTR_ERRAGG2_MASK_MPU_CR5B0_AHB_PROT_ERR2  | MPU_PROT_INTR_ERRAGG2_MASK_MPU_CR5A0_AHB_PROT_ERR2  | MPU_PROT_INTR_ERRAGG2_MASK_MPU_SCRM2SCR1_PROT_ERR2  | MPU_PROT_INTR_ERRAGG2_MASK_MPU_SCRM2SCR0_PROT_ERR2  | MPU_PROT_INTR_ERRAGG2_MASK_MPU_QSPI_PROT_ERR2       | MPU_PROT_INTR_ERRAGG2_MASK_MPU_MBOX_PROT_ERR2       | MPU_PROT_INTR_ERRAGG2_MASK_MPU_DTHE_A_PROT_ERR2     |
| R/W                                                 | R/W                                                 | R/W                                                 | R/W                                                 | R/W                                                 | R/W                                                 | R/W                                                 | R/W                                                 |
| 0h                                                  | 0h                                                  | 0h                                                  | 0h                                                  | 0h                                                  | 0h                                                  | 0h                                                  | 0h                                                  |
| 7                                                   | 6                                                   | 5                                                   | 4                                                   | 3                                                   | 2                                                   | 1                                                   | 0                                                   |
| MPU_PROT_INTR_ERRAGG2_MASK_MPU_CR5B1_AXIS_PROT_ERR2 | MPU_PROT_INTR_ERRAGG2_MASK_MPU_CR5A1_AXIS_PROT_ERR2 | MPU_PROT_INTR_ERRAGG2_MASK_MPU_CR5B0_AXIS_PROT_ERR2 | MPU_PROT_INTR_ERRAGG2_MASK_MPU_CR5A0_AXIS_PROT_ERR2 | MPU_PROT_INTR_ERRAGG2_MASK_MPU_L2_BANK_D_P_ROT_ERR2 | MPU_PROT_INTR_ERRAGG2_MASK_MPU_L2_BANK_C_P_ROT_ERR2 | MPU_PROT_INTR_ERRAGG2_MASK_MPU_L2_BANK_B_P_ROT_ERR2 | MPU_PROT_INTR_ERRAGG2_MASK_MPU_L2_BANK_A_P_ROT_ERR2 |
| R/W                                                 | R/W                                                 | R/W                                                 | R/W                                                 | R/W                                                 | R/W                                                 | R/W                                                 | R/W                                                 |
| 0h                                                  | 0h                                                  | 0h                                                  | 0h                                                  | 0h                                                  | 0h                                                  | 0h                                                  | 0h                                                  |

**Table 2-371. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG2\_MASK Register Field Descriptions**

| Bit   | Field                                              | Type | Reset | Description                                                                                                                  |
|-------|----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                                           | NONE | 0h    | Reserved                                                                                                                     |
| 17    | MPU_PROT_INTR_ERRAGG2_MASK_MPU_HSM_PROT_ERR2       | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 16    | MPU_PROT_INTR_ERRAGG2_MASK_MPU_CR5B1_AHB_PROT_ERR2 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 15    | MPU_PROT_INTR_ERRAGG2_MASK_MPU_CR5A1_AHB_PROT_ERR2 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |

**Table 2-371. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG2\_MASK Register Field Descriptions (continued)**

| Bit | Field                                               | Type | Reset | Description                                                                                                                  |
|-----|-----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 14  | MPU_PROT_INTR_ERRAGG2_MASK_MPU_CR5B0_AHB_PROT_ERR2  | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 13  | MPU_PROT_INTR_ERRAGG2_MASK_MPU_CR5A0_AHB_PROT_ERR2  | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 12  | MPU_PROT_INTR_ERRAGG2_MASK_MPU_SCRM2SCR1_PROT_ERR2  | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 11  | MPU_PROT_INTR_ERRAGG2_MASK_MPU_SCRM2SCR0_PROT_ERR2  | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 10  | MPU_PROT_INTR_ERRAGG2_MASK_MPU_QSPI_PROT_ERR2       | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 9   | MPU_PROT_INTR_ERRAGG2_MASK_MPU_MBOX_PROT_ERR2       | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 8   | MPU_PROT_INTR_ERRAGG2_MASK_MPU_DTHEA_PROT_ERR2      | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 7   | MPU_PROT_INTR_ERRAGG2_MASK_MPU_CR5B1_AXIS_PROT_ERR2 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 6   | MPU_PROT_INTR_ERRAGG2_MASK_MPU_CR5A1_AXIS_PROT_ERR2 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 5   | MPU_PROT_INTR_ERRAGG2_MASK_MPU_CR5B0_AXIS_PROT_ERR2 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 4   | MPU_PROT_INTR_ERRAGG2_MASK_MPU_CR5A0_AXIS_PROT_ERR2 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 3   | MPU_PROT_INTR_ERRAGG2_MASK_MPU_L2_BA_NK_D_PROT_ERR2 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 2   | MPU_PROT_INTR_ERRAGG2_MASK_MPU_L2_BA_NK_C_PROT_ERR2 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 1   | MPU_PROT_INTR_ERRAGG2_MASK_MPU_L2_BA_NK_B_PROT_ERR2 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |

**Table 2-371. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG2\_MASK Register Field Descriptions (continued)**

| Bit | Field                                              | Type | Reset | Description                                                                                                                  |
|-----|----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 0   | MPU_PROT_INTR_ERRAGG2_MASK_MPU_L2_BANK_A_PROT_ERR2 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |

### 2.2.2.124 MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG2\_STATUS Register

#### 1 MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG2\_STATUS Register (Offset = C034h) [reset = 0h]

This register shows the Status of Unmasked MPU Protection Errors to R5SS1 Core0 .

Return to [Summary Table](#)

**Table 2-372. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 C034h       |

**Figure 2-124. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG2\_STATUS Name Register**

|                                                       |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
|-------------------------------------------------------|-------------------------------------------------------|-------------------------------------------------------|-------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|
| 31                                                    | 30                                                    | 29                                                    | 28                                                    | 27                                                   | 26                                                   | 25                                                   | 24                                                   |
| RESERVED                                              |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
| NONE                                                  |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
| 0h                                                    |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
| 23                                                    | 22                                                    | 21                                                    | 20                                                    | 19                                                   | 18                                                   | 17                                                   | 16                                                   |
| RESERVED                                              |                                                       |                                                       |                                                       |                                                      |                                                      | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_HSM_PROT_ERR2       | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_CR5B1_AHB_PROT_ERR2 |
| NONE                                                  |                                                       |                                                       |                                                       |                                                      |                                                      | R/W                                                  | R/W                                                  |
| 0h                                                    |                                                       |                                                       |                                                       |                                                      |                                                      | 0h                                                   | 0h                                                   |
| 15                                                    | 14                                                    | 13                                                    | 12                                                    | 11                                                   | 10                                                   | 9                                                    | 8                                                    |
| MPU_PROT_INTR_ERRAGG2_STATUS_MPU_CR5A1_AHB_PROT_ERR2  | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_CR5B0_AHB_PROT_ERR2  | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_CR5A0_AHB_PROT_ERR2  | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_SCRM2SCR1_PROT_ERR2  | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_SCRM2SCR0_PROT_ERR2 | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_QSPI_PROT_ERR2      | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_MBOX_PROT_ERR2      | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_DTHE_A_PROT_ERR2    |
| R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                  | R/W                                                  | R/W                                                  | R/W                                                  |
| 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                   | 0h                                                   | 0h                                                   | 0h                                                   |
| 7                                                     | 6                                                     | 5                                                     | 4                                                     | 3                                                    | 2                                                    | 1                                                    | 0                                                    |
| MPU_PROT_INTR_ERRAGG2_STATUS_MPU_CR5B1_AXIS_PROT_ERR2 | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_CR5A1_AXIS_PROT_ERR2 | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_CR5B0_AXIS_PROT_ERR2 | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_CR5A0_AXIS_PROT_ERR2 | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_L2_BANK_D_PROT_ERR2 | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_L2_BANK_C_PROT_ERR2 | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_L2_BANK_B_PROT_ERR2 | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_L2_BANK_A_PROT_ERR2 |
| R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                  | R/W                                                  | R/W                                                  | R/W                                                  |
| 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                   | 0h                                                   | 0h                                                   | 0h                                                   |

**Table 2-374. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG2\_STATUS Register Field Descriptions**

| Bit   | Field                                                | Type | Reset | Description                                                                                                                        |
|-------|------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                                             | NONE | 0h    | Reserved                                                                                                                           |
| 17    | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_HSM_PROT_ERR2       | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 16    | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_CR5B1_AHB_PROT_ERR2 | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 15    | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_CR5A1_AHB_PROT_ERR2 | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |

**Table 2-374. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG2\_STATUS Register Field Descriptions (continued)**

| Bit | Field                                                   | Type | Reset | Description                                                                                                                        |
|-----|---------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 14  | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_CR5_B0_AHB_PROT_ERR2   | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 13  | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_CR5_A0_AHB_PROT_ERR2   | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 12  | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_SCR_M2SCR_P1_PROT_ERR2 | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 11  | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_SCR_M2SCR_P0_PROT_ERR2 | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 10  | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_QSPI_PROT_ERR2         | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 9   | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_MBOX_PROT_ERR2         | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 8   | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_DTHE_A_PROT_ERR2       | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 7   | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_CR5_B1_AXIS_PROT_ERR2  | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 6   | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_CR5_A1_AXIS_PROT_ERR2  | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 5   | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_CR5_B0_AXIS_PROT_ERR2  | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 4   | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_CR5_A0_AXIS_PROT_ERR2  | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 3   | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_L2_BANK_D_PROT_ERR2    | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 2   | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_L2_BANK_C_PROT_ERR2    | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 1   | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_L2_BANK_B_PROT_ERR2    | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |



**Table 2-374. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG2\_STATUS Register Field Descriptions (continued)**

| Bit | Field                                                | Type | Reset | Description                                                                                                                             |
|-----|------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 0   | MPU_PROT_INTR_ERRAGG2_STATUS_MPU_L2_BANK_A_PROT_ERR2 | R/W  | 0h    | Status of Error from MPU_PROT_INTR.<br>Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK<br>Write 0x1 to clear this Error. |

### 2.2.2.125 MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG2\_STATUS\_RAW Register

#### 1 MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG2\_STATUS\_RAW Register (Offset = C038h) [reset = 0h]

This register shows the Status of all MPU Protection Errors.

Return to [Summary Table](#)

**Table 2-375. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D0 C038h       |

**Figure 2-125. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG2\_STATUS\_RAW Name Register**

| 31                                                        | 30                                                        | 29                                                        | 28                                                         | 27                                                         | 26                                                       | 25                                                       | 24                                                       |
|-----------------------------------------------------------|-----------------------------------------------------------|-----------------------------------------------------------|------------------------------------------------------------|------------------------------------------------------------|----------------------------------------------------------|----------------------------------------------------------|----------------------------------------------------------|
| RESERVED                                                  |                                                           |                                                           |                                                            |                                                            |                                                          |                                                          |                                                          |
| NONE                                                      |                                                           |                                                           |                                                            |                                                            |                                                          |                                                          |                                                          |
| 0h                                                        |                                                           |                                                           |                                                            |                                                            |                                                          |                                                          |                                                          |
| 23                                                        | 22                                                        | 21                                                        | 20                                                         | 19                                                         | 18                                                       | 17                                                       | 16                                                       |
| RESERVED                                                  |                                                           |                                                           |                                                            |                                                            |                                                          | MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_HSM_PROT_ERR2       | MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_CR5B1_AHB_PROT_ERR2 |
| NONE                                                      |                                                           |                                                           |                                                            |                                                            |                                                          | R/W                                                      | R/W                                                      |
| 0h                                                        |                                                           |                                                           |                                                            |                                                            |                                                          | 0h                                                       | 0h                                                       |
| 15                                                        | 14                                                        | 13                                                        | 12                                                         | 11                                                         | 10                                                       | 9                                                        | 8                                                        |
| MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_CR5A1_AHB_PROT_ERR2  | MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_CR5B0_AHB_PROT_ERR2  | MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_CR5A0_AHB_PROT_ERR2  | MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_SCRM2_SCRP1_PROT_ERR2 | MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_SCRM2_SCRP0_PROT_ERR2 | MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_QSPI_PROT_ERR2      | MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_MBOX_PROT_ERR2      | MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_DTHEA_PROT_ERR2     |
| R/W                                                       | R/W                                                       | R/W                                                       | R/W                                                        | R/W                                                        | R/W                                                      | R/W                                                      | R/W                                                      |
| 0h                                                        | 0h                                                        | 0h                                                        | 0h                                                         | 0h                                                         | 0h                                                       | 0h                                                       | 0h                                                       |
| 7                                                         | 6                                                         | 5                                                         | 4                                                          | 3                                                          | 2                                                        | 1                                                        | 0                                                        |
| MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_CR5B1_AXIS_PROT_ERR2 | MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_CR5A1_AXIS_PROT_ERR2 | MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_CR5B0_AXIS_PROT_ERR2 | MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_CR5A0_AXIS_PROT_ERR2  | MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_L2_BANK_D_PROT_ERR2   | MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_L2_BANK_C_PROT_ERR2 | MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_L2_BANK_B_PROT_ERR2 | MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_L2_BANK_A_PROT_ERR2 |
| R/W                                                       | R/W                                                       | R/W                                                       | R/W                                                        | R/W                                                        | R/W                                                      | R/W                                                      | R/W                                                      |
| 0h                                                        | 0h                                                        | 0h                                                        | 0h                                                         | 0h                                                         | 0h                                                       | 0h                                                       | 0h                                                       |

**Table 2-377. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG2\_STATUS\_RAW Register Field Descriptions**

| Bit   | Field                                                    | Type | Reset | Description                                                                                                                  |
|-------|----------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                                                 | NONE | 0h    | Reserved                                                                                                                     |
| 17    | MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_HSM_PROT_ERR2       | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 16    | MPU_PROT_INTR_ERRAGG2_STATUS_RAW_MPU_CR5B1_AHB_PROT_ERR2 | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |

**Table 2-377. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG2\_STATUS\_RAW Register Field Descriptions  
(continued)**

| Bit | Field                                                      | Type | Reset | Description                                                                                                                  |
|-----|------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 15  | MPU_PROT_INTR_ERRAGG2_STATUS_RAW MPU_CR5A1_AHB_PROT_ERR2   | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 14  | MPU_PROT_INTR_ERRAGG2_STATUS_RAW MPU_CR5B0_AHB_PROT_ERR2   | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 13  | MPU_PROT_INTR_ERRAGG2_STATUS_RAW MPU_CR5A0_AHB_PROT_ERR2   | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 12  | MPU_PROT_INTR_ERRAGG2_STATUS_RAW MPU_SCRM2SCRIP1_PROT_ERR2 | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 11  | MPU_PROT_INTR_ERRAGG2_STATUS_RAW MPU_SCRM2SCRIP0_PROT_ERR2 | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 10  | MPU_PROT_INTR_ERRAGG2_STATUS_RAW MPU_QSPI_PROT_ERR2        | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 9   | MPU_PROT_INTR_ERRAGG2_STATUS_RAW MPU_MBOX_PROT_ERR2        | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 8   | MPU_PROT_INTR_ERRAGG2_STATUS_RAW MPU_DTHE_A_PROT_ERR2      | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 7   | MPU_PROT_INTR_ERRAGG2_STATUS_RAW MPU_CR5B1_AXIS_PROT_ERR2  | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 6   | MPU_PROT_INTR_ERRAGG2_STATUS_RAW MPU_CR5A1_AXIS_PROT_ERR2  | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 5   | MPU_PROT_INTR_ERRAGG2_STATUS_RAW MPU_CR5B0_AXIS_PROT_ERR2  | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 4   | MPU_PROT_INTR_ERRAGG2_STATUS_RAW MPU_CR5A0_AXIS_PROT_ERR2  | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 3   | MPU_PROT_INTR_ERRAGG2_STATUS_RAW MPU_L2_BANK_D_PROT_ERR2   | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 2   | MPU_PROT_INTR_ERRAGG2_STATUS_RAW MPU_L2_BANK_C_PROT_ERR2   | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 1   | MPU_PROT_INTR_ERRAGG2_STATUS_RAW MPU_L2_BANK_B_PROT_ERR2   | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |

**Table 2-377. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG2\_STATUS\_RAW Register Field Descriptions  
(continued)**

| Bit | Field                                                    | Type | Reset | Description                                                                                                                  |
|-----|----------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 0   | MPU_PROT_INTR_ERRAGG2_STATUS_RAW MPU_L2_BANK_A_PROT_ERR2 | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |

### 2.2.2.126 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_MBOX\_WRITE\_DONE Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_MBOX\_WRITE\_DONE Register (Offset = 10000h) [reset = 0h]

This register is used by R5SS1 Core 1 to generate Mailbox interrupt to Recipient CPU.

Return to [Summary Table](#)

**Table 2-378. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 0000h       |

**Figure 2-126. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_MBOX\_WRITE\_DONE Name Register**

| 31       | 30 | 29 | 28                               | 27       | 26 | 25 | 24                               |
|----------|----|----|----------------------------------|----------|----|----|----------------------------------|
| RESERVED |    |    | MSS_CR5B1_MBOX_WRITE_DONE_PROC_7 | RESERVED |    |    | MSS_CR5B1_MBOX_WRITE_DONE_PROC_6 |
| NONE     |    |    | R/W                              | NONE     |    |    | R/W                              |
| 0h       |    |    | 0h                               | 0h       |    |    | 0h                               |
| 23       | 22 | 21 | 20                               | 19       | 18 | 17 | 16                               |
| RESERVED |    |    | MSS_CR5B1_MBOX_WRITE_DONE_PROC_5 | RESERVED |    |    | MSS_CR5B1_MBOX_WRITE_DONE_PROC_4 |
| NONE     |    |    | R/W                              | NONE     |    |    | R/W                              |
| 0h       |    |    | 0h                               | 0h       |    |    | 0h                               |
| 15       | 14 | 13 | 12                               | 11       | 10 | 9  | 8                                |
| RESERVED |    |    | MSS_CR5B1_MBOX_WRITE_DONE_PROC_3 | RESERVED |    |    | MSS_CR5B1_MBOX_WRITE_DONE_PROC_2 |
| NONE     |    |    | R/W                              | NONE     |    |    | R/W                              |
| 0h       |    |    | 0h                               | 0h       |    |    | 0h                               |
| 7        | 6  | 5  | 4                                | 3        | 2  | 1  | 0                                |
| RESERVED |    |    | MSS_CR5B1_MBOX_WRITE_DONE_PROC_1 | RESERVED |    |    | MSS_CR5B1_MBOX_WRITE_DONE_PROC_0 |
| NONE     |    |    | R/W                              | NONE     |    |    | R/W                              |
| 0h       |    |    | 0h                               | 0h       |    |    | 0h                               |

**Table 2-380. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_MBOX\_WRITE\_DONE Register Field Descriptions**

| Bit   | Field                            | Type | Reset | Description                                                                                                             |
|-------|----------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 28    | MSS_CR5B1_MBOX_WRITE_DONE_PROC_7 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 7 |
| 27:25 | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 24    | MSS_CR5B1_MBOX_WRITE_DONE_PROC_6 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 6 |
| 23:21 | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 20    | MSS_CR5B1_MBOX_WRITE_DONE_PROC_5 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 5 |

**Table 2-380. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_MBOX\_WRITE\_DONE Register Field Descriptions  
(continued)**

| Bit   | Field                            | Type | Reset | Description                                                                                                             |
|-------|----------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------|
| 19:17 | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 16    | MSS_CR5B1_MBOX_WRITE_DONE_PROC_4 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 4 |
| 15:13 | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 12    | MSS_CR5B1_MBOX_WRITE_DONE_PROC_3 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 3 |
| 11:9  | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 8     | MSS_CR5B1_MBOX_WRITE_DONE_PROC_2 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 2 |
| 7:5   | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 4     | MSS_CR5B1_MBOX_WRITE_DONE_PROC_1 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 1 |
| 3:1   | RESERVED                         | NONE | 0h    | Reserved                                                                                                                |
| 0     | MSS_CR5B1_MBOX_WRITE_DONE_PROC_0 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 0 |

### 2.2.2.127 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_MBOX\_READ\_REQ Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_MBOX\_READ\_REQ Register (Offset = 10004h) [reset = 0h]

This register is used by R5SS1 Core 1 to know the Sender of Mailbox Interrupt as well as clear it.

Return to [Summary Table](#)

**Table 2-381. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 0004h       |

**Figure 2-127. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_MBOX\_READ\_REQ Name Register**

| 31       | 30 | 29 | 28                             | 27       | 26 | 25 | 24                             |
|----------|----|----|--------------------------------|----------|----|----|--------------------------------|
| RESERVED |    |    | MSS_CR5B1_MBOX_READ_REQ_PROC_7 | RESERVED |    |    | MSS_CR5B1_MBOX_READ_REQ_PROC_6 |
| NONE     |    |    | R/W                            | NONE     |    |    | R/W                            |
| 0h       |    |    | 0h                             | 0h       |    |    | 0h                             |
| 23       | 22 | 21 | 20                             | 19       | 18 | 17 | 16                             |
| RESERVED |    |    | MSS_CR5B1_MBOX_READ_REQ_PROC_5 | RESERVED |    |    | MSS_CR5B1_MBOX_READ_REQ_PROC_4 |
| NONE     |    |    | R/W                            | NONE     |    |    | R/W                            |
| 0h       |    |    | 0h                             | 0h       |    |    | 0h                             |
| 15       | 14 | 13 | 12                             | 11       | 10 | 9  | 8                              |
| RESERVED |    |    | MSS_CR5B1_MBOX_READ_REQ_PROC_3 | RESERVED |    |    | MSS_CR5B1_MBOX_READ_REQ_PROC_2 |
| NONE     |    |    | R/W                            | NONE     |    |    | R/W                            |
| 0h       |    |    | 0h                             | 0h       |    |    | 0h                             |
| 7        | 6  | 5  | 4                              | 3        | 2  | 1  | 0                              |
| RESERVED |    |    | MSS_CR5B1_MBOX_READ_REQ_PROC_1 | RESERVED |    |    | MSS_CR5B1_MBOX_READ_REQ_PROC_0 |
| NONE     |    |    | R/W                            | NONE     |    |    | R/W                            |
| 0h       |    |    | 0h                             | 0h       |    |    | 0h                             |

**Table 2-383. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_MBOX\_READ\_REQ Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                       |
|-------|--------------------------------|------|-------|-----------------------------------------------------------------------------------|
| 31:29 | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 28    | MSS_CR5B1_MBOX_READ_REQ_PROC_7 | R/W  | 0h    | This is request from processor 7 to mss_CR5B. Requesting it to read from mailbox. |
| 27:25 | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 24    | MSS_CR5B1_MBOX_READ_REQ_PROC_6 | R/W  | 0h    | This is request from processor 6 to mss_CR5B. Requesting it to read from mailbox. |
| 23:21 | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 20    | MSS_CR5B1_MBOX_READ_REQ_PROC_5 | R/W  | 0h    | This is request from processor 5 to mss_CR5B. Requesting it to read from mailbox. |
| 19:17 | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 16    | MSS_CR5B1_MBOX_READ_REQ_PROC_4 | R/W  | 0h    | This is request from processor 4 to mss_CR5B. Requesting it to read from mailbox. |
| 15:13 | RESERVED                       | NONE | 0h    | Reserved                                                                          |

**Table 2-383. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_MBOX\_READ\_REQ Register Field Descriptions  
(continued)**

| Bit  | Field                          | Type | Reset | Description                                                                       |
|------|--------------------------------|------|-------|-----------------------------------------------------------------------------------|
| 12   | MSS_CR5B1_MBOX_READ_REQ_PROC_3 | R/W  | 0h    | This is request from processor 3 to mss_CR5B. Requesting it to read from mailbox. |
| 11:9 | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 8    | MSS_CR5B1_MBOX_READ_REQ_PROC_2 | R/W  | 0h    | This is request from processor 2 to mss_CR5B. Requesting it to read from mailbox. |
| 7:5  | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 4    | MSS_CR5B1_MBOX_READ_REQ_PROC_1 | R/W  | 0h    | This is request from processor 1 to mss_CR5B. Requesting it to read from mailbox. |
| 3:1  | RESERVED                       | NONE | 0h    | Reserved                                                                          |
| 0    | MSS_CR5B1_MBOX_READ_REQ_PROC_0 | R/W  | 0h    | This is request from processor 0 to mss_CR5B. Requesting it to read from mailbox. |



### 2.2.2.128 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_MBOX\_READ\_DONE\_ACK Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_MBOX\_READ\_DONE\_ACK Register (Offset = 10008h) [reset = 0h]

This register is used by R5SS1 Core 1 to generate Mailbox Read acknowledgement to the Sender CPU.

Return to [Summary Table](#)

**Table 2-384. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 0008h       |

**Figure 2-128. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_MBOX\_READ\_DONE\_ACK Name Register**

|                                   |    |    |    |    |    |    |    |
|-----------------------------------|----|----|----|----|----|----|----|
| 31                                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                          |    |    |    |    |    |    |    |
| NONE                              |    |    |    |    |    |    |    |
| 0h                                |    |    |    |    |    |    |    |
| 23                                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                          |    |    |    |    |    |    |    |
| NONE                              |    |    |    |    |    |    |    |
| 0h                                |    |    |    |    |    |    |    |
| 15                                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED                          |    |    |    |    |    |    |    |
| NONE                              |    |    |    |    |    |    |    |
| 0h                                |    |    |    |    |    |    |    |
| 7                                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B1_MBOX_READ_DONE_ACK_PROC |    |    |    |    |    |    |    |
| R/W                               |    |    |    |    |    |    |    |
| 0h                                |    |    |    |    |    |    |    |

**Table 2-386. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_MBOX\_READ\_DONE\_ACK Register Field Descriptions**

| Bit  | Field                             | Type | Reset | Description                                                                                                            |
|------|-----------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED                          | NONE | 0h    | Reserved                                                                                                               |
| 7:0  | MSS_CR5B1_MBOX_READ_DONE_ACK_PROC | R/W  | 0h    | Write pulse bit field:<br>For bits 0 to 7: Writing 1'b1 : Generates pulse interrupt to corresponding proc from MSS_CR5 |

### 2.2.2.129 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_MBOX\_READ\_DONE Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_MBOX\_READ\_DONE Register (Offset = 1000Ch) [reset = 0h]

This register is used by R5SS1 Core 1 to know that the Receiver CPU has read the Mailbox and Acked. It is also used to clear the Read Done Interrupt.

Return to [Summary Table](#)

**Table 2-387. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 000Ch       |

**Figure 2-129. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_MBOX\_READ\_DONE Name Register**

| 31       | 30 | 29 | 28                              | 27       | 26 | 25 | 24                              |
|----------|----|----|---------------------------------|----------|----|----|---------------------------------|
| RESERVED |    |    | MSS_CR5B1_MBOX_READ_DONE_PROC_7 | RESERVED |    |    | MSS_CR5B1_MBOX_READ_DONE_PROC_6 |
| NONE     |    |    | R/W                             | NONE     |    |    | R/W                             |
| 0h       |    |    | 0h                              | 0h       |    |    | 0h                              |
| 23       | 22 | 21 | 20                              | 19       | 18 | 17 | 16                              |
| RESERVED |    |    | MSS_CR5B1_MBOX_READ_DONE_PROC_5 | RESERVED |    |    | MSS_CR5B1_MBOX_READ_DONE_PROC_4 |
| NONE     |    |    | R/W                             | NONE     |    |    | R/W                             |
| 0h       |    |    | 0h                              | 0h       |    |    | 0h                              |
| 15       | 14 | 13 | 12                              | 11       | 10 | 9  | 8                               |
| RESERVED |    |    | MSS_CR5B1_MBOX_READ_DONE_PROC_3 | RESERVED |    |    | MSS_CR5B1_MBOX_READ_DONE_PROC_2 |
| NONE     |    |    | R/W                             | NONE     |    |    | R/W                             |
| 0h       |    |    | 0h                              | 0h       |    |    | 0h                              |
| 7        | 6  | 5  | 4                               | 3        | 2  | 1  | 0                               |
| RESERVED |    |    | MSS_CR5B1_MBOX_READ_DONE_PROC_1 | RESERVED |    |    | MSS_CR5B1_MBOX_READ_DONE_PROC_0 |
| NONE     |    |    | R/W                             | NONE     |    |    | R/W                             |
| 0h       |    |    | 0h                              | 0h       |    |    | 0h                              |

**Table 2-389. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_MBOX\_READ\_DONE Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                 |
|-------|---------------------------------|------|-------|---------------------------------------------------------------------------------------------|
| 31:29 | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 28    | MSS_CR5B1_MBOX_READ_DONE_PROC_7 | R/W  | 0h    | This register should be written once finishing Reading from proc7's mailbox written by CR5B |
| 27:25 | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 24    | MSS_CR5B1_MBOX_READ_DONE_PROC_6 | R/W  | 0h    | This register should be written once finishing Reading from proc6's mailbox written by CR5B |
| 23:21 | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 20    | MSS_CR5B1_MBOX_READ_DONE_PROC_5 | R/W  | 0h    | This register should be written once finishing Reading from proc5's mailbox written by CR5B |
| 19:17 | RESERVED                        | NONE | 0h    | Reserved                                                                                    |

**Table 2-389. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_MBOX\_READ\_DONE Register Field Descriptions  
(continued)**

| Bit   | Field                           | Type | Reset | Description                                                                                 |
|-------|---------------------------------|------|-------|---------------------------------------------------------------------------------------------|
| 16    | MSS_CR5B1_MBOX_READ_DONE_PROC_4 | R/W  | 0h    | This register should be written once finishing Reading from proc4's mailbox written by CR5B |
| 15:13 | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 12    | MSS_CR5B1_MBOX_READ_DONE_PROC_3 | R/W  | 0h    | This register should be written once finishing Reading from proc3's mailbox written by CR5B |
| 11:9  | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 8     | MSS_CR5B1_MBOX_READ_DONE_PROC_2 | R/W  | 0h    | This register should be written once finishing Reading from proc2's mailbox written by CR5B |
| 7:5   | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 4     | MSS_CR5B1_MBOX_READ_DONE_PROC_1 | R/W  | 0h    | This register should be written once finishing Reading from proc1's mailbox written by CR5B |
| 3:1   | RESERVED                        | NONE | 0h    | Reserved                                                                                    |
| 0     | MSS_CR5B1_MBOX_READ_DONE_PROC_0 | R/W  | 0h    | This register should be written once finishing Reading from proc0's mailbox written by CR5B |

### 2.2.2.130 MSS\_CTRL\_MSS\_SW\_INT\_R5SS1\_CORE1 Register

#### 1 MSS\_CTRL\_MSS\_SW\_INT\_R5SS1\_CORE1 Register (Offset = 10010h) [reset = 0h]

This Register is used to generate a S/W Triggered Interrupt to R5SS1 Core1.

Return to [Summary Table](#)

**Table 2-390. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 0010h       |

**Figure 2-130. MSS\_CTRL\_MSS\_SW\_INT\_R5SS1\_CORE1 Name Register**

|          |    |    |    |    |    |    |                              |
|----------|----|----|----|----|----|----|------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                           |
| RESERVED |    |    |    |    |    |    |                              |
| NONE     |    |    |    |    |    |    |                              |
| 0h       |    |    |    |    |    |    |                              |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                           |
| RESERVED |    |    |    |    |    |    |                              |
| NONE     |    |    |    |    |    |    |                              |
| 0h       |    |    |    |    |    |    |                              |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                            |
| RESERVED |    |    |    |    |    |    |                              |
| NONE     |    |    |    |    |    |    |                              |
| 0h       |    |    |    |    |    |    |                              |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                            |
| RESERVED |    |    |    |    |    |    | MSS_SW_INT_R5SS1_CORE1_PULSE |
| NONE     |    |    |    |    |    |    | R/W                          |
| 0h       |    |    |    |    |    |    | 0h                           |

**Table 2-392. MSS\_CTRL\_MSS\_SW\_INT\_R5SS1\_CORE1 Register Field Descriptions**

| Bit  | Field                        | Type | Reset | Description                                                                                        |
|------|------------------------------|------|-------|----------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED                     | NONE | 0h    | Reserved                                                                                           |
| 0    | MSS_SW_INT_R5SS1_CORE1_PULSE | R/W  | 0h    | Write_pulse bit field:<br>Writing 1'b1 to each bit will trigger MSS_SW_INT respectively to CR5A/B. |

### 2.2.2.131 MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG3\_MASK Register

#### 1 MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG3\_MASK Register (Offset = 10020h) [reset = 0h]

This register Masks selected interrupt sources from generating MPU Address Error Interrupt to R5SS1 CORE1 .

Return to [Summary Table](#)

**Table 2-393. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 0020h       |

**Figure 2-131. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG3\_MASK Name Register**

|                                                     |                                                     |                                                     |                                                      |                                                      |                                                    |                                                    |                                                    |
|-----------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|------------------------------------------------------|------------------------------------------------------|----------------------------------------------------|----------------------------------------------------|----------------------------------------------------|
| 31                                                  | 30                                                  | 29                                                  | 28                                                   | 27                                                   | 26                                                 | 25                                                 | 24                                                 |
| RESERVED                                            |                                                     |                                                     |                                                      |                                                      |                                                    |                                                    |                                                    |
| NONE                                                |                                                     |                                                     |                                                      |                                                      |                                                    |                                                    |                                                    |
| 0h                                                  |                                                     |                                                     |                                                      |                                                      |                                                    |                                                    |                                                    |
| 23                                                  | 22                                                  | 21                                                  | 20                                                   | 19                                                   | 18                                                 | 17                                                 | 16                                                 |
| RESERVED                                            |                                                     |                                                     |                                                      |                                                      |                                                    | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_HSM_ADDR_ERR3       | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_CR5B1_AHB_ADDR_ERR3 |
| NONE                                                |                                                     |                                                     |                                                      |                                                      |                                                    | R/W                                                | R/W                                                |
| 0h                                                  |                                                     |                                                     |                                                      |                                                      |                                                    | 0h                                                 | 0h                                                 |
| 15                                                  | 14                                                  | 13                                                  | 12                                                   | 11                                                   | 10                                                 | 9                                                  | 8                                                  |
| MPU_ADDR_INTR_ERRAGG3_MASK_MPU_CR5A1_AHB_ADDR_ERR3  | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_CR5B0_AHB_ADDR_ERR3  | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_CR5A0_AHB_ADDR_ERR3  | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_SCRM2SCRIP1_ADDR_ERR3 | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_SCRM2SCRIP0_ADDR_ERR3 | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_QSPI_ADDR_ERR3      | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_MBOX_ADDR_ERR3      | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_DTHE_A_ADDR_ERR3    |
| R/W                                                 | R/W                                                 | R/W                                                 | R/W                                                  | R/W                                                  | R/W                                                | R/W                                                | R/W                                                |
| 0h                                                  | 0h                                                  | 0h                                                  | 0h                                                   | 0h                                                   | 0h                                                 | 0h                                                 | 0h                                                 |
| 7                                                   | 6                                                   | 5                                                   | 4                                                    | 3                                                    | 2                                                  | 1                                                  | 0                                                  |
| MPU_ADDR_INTR_ERRAGG3_MASK_MPU_CR5B1_AXIS_ADDR_ERR3 | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_CR5A1_AXIS_ADDR_ERR3 | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_CR5B0_AXIS_ADDR_ERR3 | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_CR5A0_AXIS_ADDR_ERR3  | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_L2_BANK_D_ADDR_ERR3   | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_L2_BANK_C_ADDR_ERR3 | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_L2_BANK_B_ADDR_ERR3 | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_L2_BANK_A_ADDR_ERR3 |
| R/W                                                 | R/W                                                 | R/W                                                 | R/W                                                  | R/W                                                  | R/W                                                | R/W                                                | R/W                                                |
| 0h                                                  | 0h                                                  | 0h                                                  | 0h                                                   | 0h                                                   | 0h                                                 | 0h                                                 | 0h                                                 |

**Table 2-395. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG3\_MASK Register Field Descriptions**

| Bit   | Field                                              | Type | Reset | Description                                                                                                                   |
|-------|----------------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                                           | NONE | 0h    | Reserved                                                                                                                      |
| 17    | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_HSM_ADDR_ERR3       | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG3<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 16    | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_CR5B1_AHB_ADDR_ERR3 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG3<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 15    | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_CR5A1_AHB_ADDR_ERR3 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG3<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |

**Table 2-395. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG3\_MASK Register Field Descriptions (continued)**

| Bit | Field                                               | Type | Reset | Description                                                                                                                  |
|-----|-----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 14  | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_CR5B0_AHB_ADDR_ERR3  | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 13  | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_CR5A0_AHB_ADDR_ERR3  | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 12  | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_SCRM2SCR1_ADDR_ERR3  | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 11  | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_SCRM2SCR0_ADDR_ERR3  | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 10  | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_QSPI_ADDR_ERR3       | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 9   | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_MBOX_ADDR_ERR3       | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 8   | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_DTHEA_ADDR_ERR3      | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 7   | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_CR5B1_AXIS_ADDR_ERR3 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 6   | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_CR5A1_AXIS_ADDR_ERR3 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 5   | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_CR5B0_AXIS_ADDR_ERR3 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 4   | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_CR5A0_AXIS_ADDR_ERR3 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 3   | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_L2_BA_NK_D_ADDR_ERR3 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 2   | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_L2_BA_NK_C_ADDR_ERR3 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 1   | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_L2_BA_NK_B_ADDR_ERR3 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |

**Table 2-395. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG3\_MASK Register Field Descriptions (continued)**

| Bit | Field                                              | Type | Reset | Description                                                                                                                  |
|-----|----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 0   | MPU_ADDR_INTR_ERRAGG3_MASK_MPU_L2_BANK_A_ADDR_ERR3 | R/W  | 0h    | Mask Error from MPU_ADDR_INTR to aggregated Error MPU_ADDR_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |

### 2.2.2.132 MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG3\_STATUS Register

#### 1 MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG3\_STATUS Register (Offset = 10024h) [reset = 0h]

This register shows the Status of Unmasked MPU Address Errors to R5SS1 CORE1 .

Return to [Summary Table](#)

**Table 2-396. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 0024h       |

**Figure 2-132. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG3\_STATUS Name Register**

|                                                       |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
|-------------------------------------------------------|-------------------------------------------------------|-------------------------------------------------------|-------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|
| 31                                                    | 30                                                    | 29                                                    | 28                                                    | 27                                                   | 26                                                   | 25                                                   | 24                                                   |
| RESERVED                                              |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
| NONE                                                  |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
| 0h                                                    |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
| 23                                                    | 22                                                    | 21                                                    | 20                                                    | 19                                                   | 18                                                   | 17                                                   | 16                                                   |
| RESERVED                                              |                                                       |                                                       |                                                       |                                                      |                                                      | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_HSM_ADDR_ERR3       | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_CR5B1_AHB_ADDR_ERR3 |
| NONE                                                  |                                                       |                                                       |                                                       |                                                      |                                                      | R/W                                                  | R/W                                                  |
| 0h                                                    |                                                       |                                                       |                                                       |                                                      |                                                      | 0h                                                   | 0h                                                   |
| 15                                                    | 14                                                    | 13                                                    | 12                                                    | 11                                                   | 10                                                   | 9                                                    | 8                                                    |
| MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_CR5A1_AHB_ADDR_ERR3  | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_CR5B0_AHB_ADDR_ERR3  | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_CR5A0_AHB_ADDR_ERR3  | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_SCRM2SCR1_ADDR_ERR3  | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_SCRM2SCR0_ADDR_ERR3 | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_QSPI_ADDR_ERR3      | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_MBOX_ADDR_ERR3      | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_DTHE_A_ADDR_ERR3    |
| R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                  | R/W                                                  | R/W                                                  | R/W                                                  |
| 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                   | 0h                                                   | 0h                                                   | 0h                                                   |
| 7                                                     | 6                                                     | 5                                                     | 4                                                     | 3                                                    | 2                                                    | 1                                                    | 0                                                    |
| MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_CR5B1_AXIS_ADDR_ERR3 | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_CR5A1_AXIS_ADDR_ERR3 | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_CR5B0_AXIS_ADDR_ERR3 | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_CR5A0_AXIS_ADDR_ERR3 | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_L2_BANK_D_ADDR_ERR3 | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_L2_BANK_C_ADDR_ERR3 | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_L2_BANK_B_ADDR_ERR3 | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_L2_BANK_A_ADDR_ERR3 |
| R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                  | R/W                                                  | R/W                                                  | R/W                                                  |
| 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                   | 0h                                                   | 0h                                                   | 0h                                                   |

**Table 2-398. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG3\_STATUS Register Field Descriptions**

| Bit   | Field                                                | Type | Reset | Description                                                                                                                        |
|-------|------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                                             | NONE | 0h    | Reserved                                                                                                                           |
| 17    | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_HSM_ADDR_ERR3       | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 16    | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_CR5B1_AHB_ADDR_ERR3 | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 15    | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_CR5A1_AHB_ADDR_ERR3 | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |



**Table 2-398. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG3\_STATUS Register Field Descriptions (continued)**

| Bit | Field                                                  | Type | Reset | Description                                                                                                                        |
|-----|--------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 14  | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_CR5_B0_AHB_ADDR_ERR3  | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 13  | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_CR5_A0_AHB_ADDR_ERR3  | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 12  | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_SCR_M2SCR1_ADDR_ERR3  | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 11  | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_SCR_M2SCR0_ADDR_ERR3  | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 10  | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_QSPI_ADDR_ERR3        | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 9   | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_MBOX_ADDR_ERR3        | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 8   | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_DTHE_A_ADDR_ERR3      | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 7   | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_CR5_B1_AXIS_ADDR_ERR3 | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 6   | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_CR5_A1_AXIS_ADDR_ERR3 | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 5   | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_CR5_B0_AXIS_ADDR_ERR3 | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 4   | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_CR5_A0_AXIS_ADDR_ERR3 | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 3   | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_L2_BANK_D_ADDR_ERR3   | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 2   | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_L2_BANK_C_ADDR_ERR3   | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 1   | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_L2_BANK_B_ADDR_ERR3   | R/W  | 0h    | Status of Error from MPU_ADDR_INTR. Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |

**Table 2-398. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG3\_STATUS Register Field Descriptions (continued)**

| Bit | Field                                                | Type | Reset | Description                                                                                                                             |
|-----|------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 0   | MPU_ADDR_INTR_ERRAGG3_STATUS_MPU_L2_BANK_A_ADDR_ERR3 | R/W  | 0h    | Status of Error from MPU_ADDR_INTR.<br>Set only if Interrupt is unmasked in MPU_ADDR_INTR_ERRAGG_MASK<br>Write 0x1 to clear this Error. |

### 2.2.2.133 MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG3\_STATUS\_RAW Register

#### 1 MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG3\_STATUS\_RAW Register (Offset = 10028h) [reset = 0h]

This register shows the Status of all MPU Address Errors.

Return to [Summary Table](#)

**Table 2-399. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 0028h       |

**Figure 2-133. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG3\_STATUS\_RAW Name Register**

| 31                                                        | 30                                                        | 29                                                        | 28                                                         | 27                                                         | 26                                                       | 25                                                       | 24                                                       |
|-----------------------------------------------------------|-----------------------------------------------------------|-----------------------------------------------------------|------------------------------------------------------------|------------------------------------------------------------|----------------------------------------------------------|----------------------------------------------------------|----------------------------------------------------------|
| RESERVED                                                  |                                                           |                                                           |                                                            |                                                            |                                                          |                                                          |                                                          |
| NONE                                                      |                                                           |                                                           |                                                            |                                                            |                                                          |                                                          |                                                          |
| 0h                                                        |                                                           |                                                           |                                                            |                                                            |                                                          |                                                          |                                                          |
| 23                                                        | 22                                                        | 21                                                        | 20                                                         | 19                                                         | 18                                                       | 17                                                       | 16                                                       |
| RESERVED                                                  |                                                           |                                                           |                                                            |                                                            |                                                          | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_HSM_A_DDR_ERR3      | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_CR5B1_AHB_ADDR_ERR3 |
| NONE                                                      |                                                           |                                                           |                                                            |                                                            |                                                          | R/W                                                      | R/W                                                      |
| 0h                                                        |                                                           |                                                           |                                                            |                                                            |                                                          | 0h                                                       | 0h                                                       |
| 15                                                        | 14                                                        | 13                                                        | 12                                                         | 11                                                         | 10                                                       | 9                                                        | 8                                                        |
| MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_CR5A1_AHB_ADDR_ERR3  | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_CR5B0_AHB_ADDR_ERR3  | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_CR5A0_AHB_ADDR_ERR3  | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_SCRM2_SCRP1_ADDR_ERR3 | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_SCRM2_SCRP0_ADDR_ERR3 | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_QSPI_A_DDR_ERR3     | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_MBOX_ADDR_ERR3      | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_DTHE_A_ADDR_ERR3    |
| R/W                                                       | R/W                                                       | R/W                                                       | R/W                                                        | R/W                                                        | R/W                                                      | R/W                                                      | R/W                                                      |
| 0h                                                        | 0h                                                        | 0h                                                        | 0h                                                         | 0h                                                         | 0h                                                       | 0h                                                       | 0h                                                       |
| 7                                                         | 6                                                         | 5                                                         | 4                                                          | 3                                                          | 2                                                        | 1                                                        | 0                                                        |
| MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_CR5B1_AXIS_ADDR_ERR3 | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_CR5A1_AXIS_ADDR_ERR3 | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_CR5B0_AXIS_ADDR_ERR3 | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_CR5A0_AXIS_ADDR_ERR3  | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_L2_BANK_D_ADDR_ERR3   | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_L2_BANK_C_ADDR_ERR3 | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_L2_BANK_B_ADDR_ERR3 | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_L2_BANK_A_ADDR_ERR3 |
| R/W                                                       | R/W                                                       | R/W                                                       | R/W                                                        | R/W                                                        | R/W                                                      | R/W                                                      | R/W                                                      |
| 0h                                                        | 0h                                                        | 0h                                                        | 0h                                                         | 0h                                                         | 0h                                                       | 0h                                                       | 0h                                                       |

**Table 2-401. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG3\_STATUS\_RAW Register Field Descriptions**

| Bit   | Field                                                    | Type | Reset | Description                                                                                                                  |
|-------|----------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                                                 | NONE | 0h    | Reserved                                                                                                                     |
| 17    | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_HSM_A_DDR_ERR3      | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 16    | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW_MPU_CR5B1_AHB_ADDR_ERR3 | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |

**Table 2-401. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG3\_STATUS\_RAW Register Field Descriptions  
(continued)**

| Bit | Field                                                      | Type | Reset | Description                                                                                                                  |
|-----|------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 15  | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW MPU_CR5A1_AHB_ADDR_ERR3   | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 14  | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW MPU_CR5B0_AHB_ADDR_ERR3   | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 13  | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW MPU_CR5A0_AHB_ADDR_ERR3   | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 12  | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW MPU_SCRM2SCRIP1_ADDR_ERR3 | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 11  | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW MPU_SCRM2SCRIP0_ADDR_ERR3 | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 10  | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW MPU_QSPI_ADDR_ERR3        | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 9   | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW MPU_MBOX_ADDR_ERR3        | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 8   | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW MPU_DTHE_A_ADDR_ERR3      | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 7   | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW MPU_CR5B1_AXIS_ADDR_ERR3  | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 6   | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW MPU_CR5A1_AXIS_ADDR_ERR3  | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 5   | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW MPU_CR5B0_AXIS_ADDR_ERR3  | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 4   | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW MPU_CR5A0_AXIS_ADDR_ERR3  | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 3   | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW MPU_L2_BANK_D_ADDR_ERR3   | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 2   | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW MPU_L2_BANK_C_ADDR_ERR3   | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |
| 1   | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW MPU_L2_BANK_B_ADDR_ERR3   | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |

**Table 2-401. MSS\_CTRL\_MPU\_ADDR\_INTR\_ERRAGG3\_STATUS\_RAW Register Field Descriptions  
(continued)**

| Bit | Field                                                    | Type | Reset | Description                                                                                                                  |
|-----|----------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 0   | MPU_ADDR_INTR_ERRAGG3_STATUS_RAW MPU_L2_BANK_A_ADDR_ERR3 | R/W  | 0h    | Raw Status of Error from MPU_ADDR_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_ADDR_INTR_ERRAGG_MASK |

### 2.2.2.134 MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG3\_MASK Register

#### 1 MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG3\_MASK Register (Offset = 10030h) [reset = 0h]

This register Masks selected interrupt sources from generating MPU Protection Error Interrupt to R5SS1 CORE1 .

Return to [Summary Table](#)

**Table 2-402. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 0030h       |

**Figure 2-134. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG3\_MASK Name Register**

|                                                     |                                                     |                                                     |                                                      |                                                      |                                                     |                                                     |                                                     |
|-----------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|------------------------------------------------------|------------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|
| 31                                                  | 30                                                  | 29                                                  | 28                                                   | 27                                                   | 26                                                  | 25                                                  | 24                                                  |
| RESERVED                                            |                                                     |                                                     |                                                      |                                                      |                                                     |                                                     |                                                     |
| NONE                                                |                                                     |                                                     |                                                      |                                                      |                                                     |                                                     |                                                     |
| 0h                                                  |                                                     |                                                     |                                                      |                                                      |                                                     |                                                     |                                                     |
| 23                                                  | 22                                                  | 21                                                  | 20                                                   | 19                                                   | 18                                                  | 17                                                  | 16                                                  |
| RESERVED                                            |                                                     |                                                     |                                                      |                                                      |                                                     | MPU_PROT_INTR_ERRAGG3_MASK_MPU_HSM_PROT_ERR3        | MPU_PROT_INTR_ERRAGG3_MASK_MPU_CR5B1_AHB_PROT_ERR3  |
| NONE                                                |                                                     |                                                     |                                                      |                                                      |                                                     | R/W                                                 | R/W                                                 |
| 0h                                                  |                                                     |                                                     |                                                      |                                                      |                                                     | 0h                                                  | 0h                                                  |
| 15                                                  | 14                                                  | 13                                                  | 12                                                   | 11                                                   | 10                                                  | 9                                                   | 8                                                   |
| MPU_PROT_INTR_ERRAGG3_MASK_MPU_CR5A1_AHB_PROT_ERR3  | MPU_PROT_INTR_ERRAGG3_MASK_MPU_CR5B0_AHB_PROT_ERR3  | MPU_PROT_INTR_ERRAGG3_MASK_MPU_CR5A0_AHB_PROT_ERR3  | MPU_PROT_INTR_ERRAGG3_MASK_MPU_SCRM2SCRIP1_PROT_ERR3 | MPU_PROT_INTR_ERRAGG3_MASK_MPU_SCRM2SCRIP0_PROT_ERR3 | MPU_PROT_INTR_ERRAGG3_MASK_MPU_QSPI_PROT_ERR3       | MPU_PROT_INTR_ERRAGG3_MASK_MPU_MBOX_PROT_ERR3       | MPU_PROT_INTR_ERRAGG3_MASK_MPU_DTHE_A_PROT_ERR3     |
| R/W                                                 | R/W                                                 | R/W                                                 | R/W                                                  | R/W                                                  | R/W                                                 | R/W                                                 | R/W                                                 |
| 0h                                                  | 0h                                                  | 0h                                                  | 0h                                                   | 0h                                                   | 0h                                                  | 0h                                                  | 0h                                                  |
| 7                                                   | 6                                                   | 5                                                   | 4                                                    | 3                                                    | 2                                                   | 1                                                   | 0                                                   |
| MPU_PROT_INTR_ERRAGG3_MASK_MPU_CR5B1_AXIS_PROT_ERR3 | MPU_PROT_INTR_ERRAGG3_MASK_MPU_CR5A1_AXIS_PROT_ERR3 | MPU_PROT_INTR_ERRAGG3_MASK_MPU_CR5B0_AXIS_PROT_ERR3 | MPU_PROT_INTR_ERRAGG3_MASK_MPU_CR5A0_AXIS_PROT_ERR3  | MPU_PROT_INTR_ERRAGG3_MASK_MPU_L2_BANK_D_P_ROT_ERR3  | MPU_PROT_INTR_ERRAGG3_MASK_MPU_L2_BANK_C_P_ROT_ERR3 | MPU_PROT_INTR_ERRAGG3_MASK_MPU_L2_BANK_B_P_ROT_ERR3 | MPU_PROT_INTR_ERRAGG3_MASK_MPU_L2_BANK_A_P_ROT_ERR3 |
| R/W                                                 | R/W                                                 | R/W                                                 | R/W                                                  | R/W                                                  | R/W                                                 | R/W                                                 | R/W                                                 |
| 0h                                                  | 0h                                                  | 0h                                                  | 0h                                                   | 0h                                                   | 0h                                                  | 0h                                                  | 0h                                                  |

**Table 2-404. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG3\_MASK Register Field Descriptions**

| Bit   | Field                                              | Type | Reset | Description                                                                                                                   |
|-------|----------------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                                           | NONE | 0h    | Reserved                                                                                                                      |
| 17    | MPU_PROT_INTR_ERRAGG3_MASK_MPU_HSM_PROT_ERR3       | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG3<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 16    | MPU_PROT_INTR_ERRAGG3_MASK_MPU_CR5B1_AHB_PROT_ERR3 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG3<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 15    | MPU_PROT_INTR_ERRAGG3_MASK_MPU_CR5A1_AHB_PROT_ERR3 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG3<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |

**Table 2-404. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG3\_MASK Register Field Descriptions (continued)**

| Bit | Field                                               | Type | Reset | Description                                                                                                                  |
|-----|-----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 14  | MPU_PROT_INTR_ERRAGG3_MASK_MPU_CR5B0_AHB_PROT_ERR3  | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 13  | MPU_PROT_INTR_ERRAGG3_MASK_MPU_CR5A0_AHB_PROT_ERR3  | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 12  | MPU_PROT_INTR_ERRAGG3_MASK_MPU_SCRM2SCR1_PROT_ERR3  | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 11  | MPU_PROT_INTR_ERRAGG3_MASK_MPU_SCRM2SCR0_PROT_ERR3  | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 10  | MPU_PROT_INTR_ERRAGG3_MASK_MPU_QSPI_PROT_ERR3       | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 9   | MPU_PROT_INTR_ERRAGG3_MASK_MPU_MBOX_PROT_ERR3       | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 8   | MPU_PROT_INTR_ERRAGG3_MASK_MPU_DTHEA_PROT_ERR3      | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 7   | MPU_PROT_INTR_ERRAGG3_MASK_MPU_CR5B1_AXIS_PROT_ERR3 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 6   | MPU_PROT_INTR_ERRAGG3_MASK_MPU_CR5A1_AXIS_PROT_ERR3 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 5   | MPU_PROT_INTR_ERRAGG3_MASK_MPU_CR5B0_AXIS_PROT_ERR3 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 4   | MPU_PROT_INTR_ERRAGG3_MASK_MPU_CR5A0_AXIS_PROT_ERR3 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 3   | MPU_PROT_INTR_ERRAGG3_MASK_MPU_L2_BA_NK_D_PROT_ERR3 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 2   | MPU_PROT_INTR_ERRAGG3_MASK_MPU_L2_BA_NK_C_PROT_ERR3 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 1   | MPU_PROT_INTR_ERRAGG3_MASK_MPU_L2_BA_NK_B_PROT_ERR3 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |

**Table 2-404. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG3\_MASK Register Field Descriptions (continued)**

| Bit | Field                                              | Type | Reset | Description                                                                                                                  |
|-----|----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 0   | MPU_PROT_INTR_ERRAGG3_MASK_MPU_L2_BANK_A_PROT_ERR3 | R/W  | 0h    | Mask Error from MPU_PROT_INTR to aggregated Error MPU_PROT_INTR_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |



### 2.2.2.135 MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG3\_STATUS Register

#### 1 MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG3\_STATUS Register (Offset = 10034h) [reset = 0h]

This register shows the Status of Unmasked MPU Protection Errors to R5SS1 CORE1 .

Return to [Summary Table](#)

**Table 2-405. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 0034h       |

**Figure 2-135. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG3\_STATUS Name Register**

|                                                       |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
|-------------------------------------------------------|-------------------------------------------------------|-------------------------------------------------------|-------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|------------------------------------------------------|
| 31                                                    | 30                                                    | 29                                                    | 28                                                    | 27                                                   | 26                                                   | 25                                                   | 24                                                   |
| RESERVED                                              |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
| NONE                                                  |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
| 0h                                                    |                                                       |                                                       |                                                       |                                                      |                                                      |                                                      |                                                      |
| 23                                                    | 22                                                    | 21                                                    | 20                                                    | 19                                                   | 18                                                   | 17                                                   | 16                                                   |
| RESERVED                                              |                                                       |                                                       |                                                       |                                                      |                                                      | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_HSM_PROT_ERR3       | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_CR5B1_AHB_PROT_ERR3 |
| NONE                                                  |                                                       |                                                       |                                                       |                                                      |                                                      | R/W                                                  | R/W                                                  |
| 0h                                                    |                                                       |                                                       |                                                       |                                                      |                                                      | 0h                                                   | 0h                                                   |
| 15                                                    | 14                                                    | 13                                                    | 12                                                    | 11                                                   | 10                                                   | 9                                                    | 8                                                    |
| MPU_PROT_INTR_ERRAGG3_STATUS_MPU_CR5A1_AHB_PROT_ERR3  | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_CR5B0_AHB_PROT_ERR3  | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_CR5A0_AHB_PROT_ERR3  | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_SCRM2SCR1_PROT_ERR3  | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_SCRM2SCR0_PROT_ERR3 | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_QSPI_PROT_ERR3      | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_MBOX_PROT_ERR3      | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_DTHE_A_PROT_ERR3    |
| R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                  | R/W                                                  | R/W                                                  | R/W                                                  |
| 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                   | 0h                                                   | 0h                                                   | 0h                                                   |
| 7                                                     | 6                                                     | 5                                                     | 4                                                     | 3                                                    | 2                                                    | 1                                                    | 0                                                    |
| MPU_PROT_INTR_ERRAGG3_STATUS_MPU_CR5B1_AXIS_PROT_ERR3 | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_CR5A1_AXIS_PROT_ERR3 | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_CR5B0_AXIS_PROT_ERR3 | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_CR5A0_AXIS_PROT_ERR3 | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_L2_BANK_D_PROT_ERR3 | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_L2_BANK_C_PROT_ERR3 | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_L2_BANK_B_PROT_ERR3 | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_L2_BANK_A_PROT_ERR3 |
| R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                   | R/W                                                  | R/W                                                  | R/W                                                  | R/W                                                  |
| 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                    | 0h                                                   | 0h                                                   | 0h                                                   | 0h                                                   |

**Table 2-407. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG3\_STATUS Register Field Descriptions**

| Bit   | Field                                                | Type | Reset | Description                                                                                                                        |
|-------|------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                                             | NONE | 0h    | Reserved                                                                                                                           |
| 17    | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_HSM_PROT_ERR3       | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 16    | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_CR5B1_AHB_PROT_ERR3 | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 15    | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_CR5A1_AHB_PROT_ERR3 | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |

**Table 2-407. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG3\_STATUS Register Field Descriptions (continued)**

| Bit | Field                                                   | Type | Reset | Description                                                                                                                        |
|-----|---------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 14  | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_CR5_B0_AHB_PROT_ERR3   | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 13  | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_CR5_A0_AHB_PROT_ERR3   | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 12  | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_SCR_M2SCR_P1_PROT_ERR3 | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 11  | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_SCR_M2SCR_P0_PROT_ERR3 | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 10  | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_QSPI_PROT_ERR3         | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 9   | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_MBOX_PROT_ERR3         | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 8   | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_DTHE_A_PROT_ERR3       | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 7   | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_CR5_B1_AXIS_PROT_ERR3  | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 6   | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_CR5_A1_AXIS_PROT_ERR3  | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 5   | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_CR5_B0_AXIS_PROT_ERR3  | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 4   | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_CR5_A0_AXIS_PROT_ERR3  | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 3   | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_L2_BANK_D_PROT_ERR3    | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 2   | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_L2_BANK_C_PROT_ERR3    | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |
| 1   | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_L2_BANK_B_PROT_ERR3    | R/W  | 0h    | Status of Error from MPU_PROT_INTR. Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK. Write 0x1 to clear this Error. |

**Table 2-407. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG3\_STATUS Register Field Descriptions (continued)**

| Bit | Field                                                | Type | Reset | Description                                                                                                                             |
|-----|------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 0   | MPU_PROT_INTR_ERRAGG3_STATUS_MPU_L2_BANK_A_PROT_ERR3 | R/W  | 0h    | Status of Error from MPU_PROT_INTR.<br>Set only if Interrupt is unmasked in MPU_PROT_INTR_ERRAGG_MASK<br>Write 0x1 to clear this Error. |

### 2.2.2.136 MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG3\_STATUS\_RAW Register

#### 1 MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG3\_STATUS\_RAW Register (Offset = 10038h) [reset = 0h]

This register shows the Status of all MPU Protection Errors.

Return to [Summary Table](#)

**Table 2-408. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 0038h       |

**Figure 2-136. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG3\_STATUS\_RAW Name Register**

| 31                                                                           | 30                                                                           | 29                                                                           | 28                                                                             | 27                                                                             | 26                                                                          | 25                                                                          | 24                                                                          |
|------------------------------------------------------------------------------|------------------------------------------------------------------------------|------------------------------------------------------------------------------|--------------------------------------------------------------------------------|--------------------------------------------------------------------------------|-----------------------------------------------------------------------------|-----------------------------------------------------------------------------|-----------------------------------------------------------------------------|
| RESERVED                                                                     |                                                                              |                                                                              |                                                                                |                                                                                |                                                                             |                                                                             |                                                                             |
| NONE                                                                         |                                                                              |                                                                              |                                                                                |                                                                                |                                                                             |                                                                             |                                                                             |
| 0h                                                                           |                                                                              |                                                                              |                                                                                |                                                                                |                                                                             |                                                                             |                                                                             |
| 23                                                                           | 22                                                                           | 21                                                                           | 20                                                                             | 19                                                                             | 18                                                                          | 17                                                                          | 16                                                                          |
| RESERVED                                                                     |                                                                              |                                                                              |                                                                                |                                                                                |                                                                             | MPU_PROT_IN<br>TR_ERRAGG3<br>STATUS_RAW<br>_MPU_HSM_P<br>ROT_ERR3           | MPU_PROT_IN<br>TR_ERRAGG3<br>STATUS_RAW<br>_MPU_CR5B1_<br>AHB_PROT_E<br>RR3 |
| NONE                                                                         |                                                                              |                                                                              |                                                                                |                                                                                |                                                                             | R/W                                                                         | R/W                                                                         |
| 0h                                                                           |                                                                              |                                                                              |                                                                                |                                                                                |                                                                             | 0h                                                                          | 0h                                                                          |
| 15                                                                           | 14                                                                           | 13                                                                           | 12                                                                             | 11                                                                             | 10                                                                          | 9                                                                           | 8                                                                           |
| MPU_PROT_IN<br>TR_ERRAGG3<br>STATUS_RAW<br>_MPU_CR5A1_<br>AHB_PROT_E<br>RR3  | MPU_PROT_IN<br>TR_ERRAGG3<br>STATUS_RAW<br>_MPU_CR5B0_<br>AHB_PROT_E<br>RR3  | MPU_PROT_IN<br>TR_ERRAGG3<br>STATUS_RAW<br>_MPU_CR5A0_<br>AHB_PROT_E<br>RR3  | MPU_PROT_IN<br>TR_ERRAGG3<br>STATUS_RAW<br>_MPU_SCRM2_<br>SCRIP1_PROT_<br>ERR3 | MPU_PROT_IN<br>TR_ERRAGG3<br>STATUS_RAW<br>_MPU_SCRM2_<br>SCRIP0_PROT_<br>ERR3 | MPU_PROT_IN<br>TR_ERRAGG3<br>STATUS_RAW<br>_MPU_QSPI_P<br>ROT_ERR3          | MPU_PROT_IN<br>TR_ERRAGG3<br>STATUS_RAW<br>_MPU_MBOX_<br>PROT_ERR3          | MPU_PROT_IN<br>TR_ERRAGG3<br>STATUS_RAW<br>_MPU_DTHE_<br>A_PROT_ERR3        |
| R/W                                                                          | R/W                                                                          | R/W                                                                          | R/W                                                                            | R/W                                                                            | R/W                                                                         | R/W                                                                         | R/W                                                                         |
| 0h                                                                           | 0h                                                                           | 0h                                                                           | 0h                                                                             | 0h                                                                             | 0h                                                                          | 0h                                                                          | 0h                                                                          |
| 7                                                                            | 6                                                                            | 5                                                                            | 4                                                                              | 3                                                                              | 2                                                                           | 1                                                                           | 0                                                                           |
| MPU_PROT_IN<br>TR_ERRAGG3<br>STATUS_RAW<br>_MPU_CR5B1_<br>AXIS_PROT_E<br>RR3 | MPU_PROT_IN<br>TR_ERRAGG3<br>STATUS_RAW<br>_MPU_CR5A1_<br>AXIS_PROT_E<br>RR3 | MPU_PROT_IN<br>TR_ERRAGG3<br>STATUS_RAW<br>_MPU_CR5B0_<br>AXIS_PROT_E<br>RR3 | MPU_PROT_IN<br>TR_ERRAGG3<br>STATUS_RAW<br>_MPU_CR5A0_<br>AXIS_PROT_E<br>RR3   | MPU_PROT_IN<br>TR_ERRAGG3<br>STATUS_RAW<br>_MPU_L2_BAN<br>K_D_PROT_ER<br>R3    | MPU_PROT_IN<br>TR_ERRAGG3<br>STATUS_RAW<br>_MPU_L2_BAN<br>K_C_PROT_ER<br>R3 | MPU_PROT_IN<br>TR_ERRAGG3<br>STATUS_RAW<br>_MPU_L2_BAN<br>K_B_PROT_ER<br>R3 | MPU_PROT_IN<br>TR_ERRAGG3<br>STATUS_RAW<br>_MPU_L2_BAN<br>K_A_PROT_ER<br>R3 |
| R/W                                                                          | R/W                                                                          | R/W                                                                          | R/W                                                                            | R/W                                                                            | R/W                                                                         | R/W                                                                         | R/W                                                                         |
| 0h                                                                           | 0h                                                                           | 0h                                                                           | 0h                                                                             | 0h                                                                             | 0h                                                                          | 0h                                                                          | 0h                                                                          |

**Table 2-410. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG3\_STATUS\_RAW Register Field Descriptions**

| Bit   | Field                                                    | Type | Reset | Description                                                                                                                  |
|-------|----------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                                                 | NONE | 0h    | Reserved                                                                                                                     |
| 17    | MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_HSM_PROT_ERR3       | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 16    | MPU_PROT_INTR_ERRAGG3_STATUS_RAW_MPU_CR5B1_AHB_PROT_ERR3 | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |

**Table 2-410. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG3\_STATUS\_RAW Register Field Descriptions  
(continued)**

| Bit | Field                                                      | Type | Reset | Description                                                                                                                  |
|-----|------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 15  | MPU_PROT_INTR_ERRAGG3_STATUS_RAW MPU_CR5A1_AHB_PROT_ERR3   | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 14  | MPU_PROT_INTR_ERRAGG3_STATUS_RAW MPU_CR5B0_AHB_PROT_ERR3   | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 13  | MPU_PROT_INTR_ERRAGG3_STATUS_RAW MPU_CR5A0_AHB_PROT_ERR3   | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 12  | MPU_PROT_INTR_ERRAGG3_STATUS_RAW MPU_SCRM2SCRIP1_PROT_ERR3 | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 11  | MPU_PROT_INTR_ERRAGG3_STATUS_RAW MPU_SCRM2SCRIP0_PROT_ERR3 | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 10  | MPU_PROT_INTR_ERRAGG3_STATUS_RAW MPU_QSPI_PROT_ERR3        | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 9   | MPU_PROT_INTR_ERRAGG3_STATUS_RAW MPU_MBOX_PROT_ERR3        | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 8   | MPU_PROT_INTR_ERRAGG3_STATUS_RAW MPU_DTHE_A_PROT_ERR3      | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 7   | MPU_PROT_INTR_ERRAGG3_STATUS_RAW MPU_CR5B1_AXIS_PROT_ERR3  | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 6   | MPU_PROT_INTR_ERRAGG3_STATUS_RAW MPU_CR5A1_AXIS_PROT_ERR3  | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 5   | MPU_PROT_INTR_ERRAGG3_STATUS_RAW MPU_CR5B0_AXIS_PROT_ERR3  | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 4   | MPU_PROT_INTR_ERRAGG3_STATUS_RAW MPU_CR5A0_AXIS_PROT_ERR3  | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 3   | MPU_PROT_INTR_ERRAGG3_STATUS_RAW MPU_L2_BANK_D_PROT_ERR3   | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 2   | MPU_PROT_INTR_ERRAGG3_STATUS_RAW MPU_L2_BANK_C_PROT_ERR3   | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |
| 1   | MPU_PROT_INTR_ERRAGG3_STATUS_RAW MPU_L2_BANK_B_PROT_ERR3   | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |

**Table 2-410. MSS\_CTRL\_MPU\_PROT\_INTR\_ERRAGG3\_STATUS\_RAW Register Field Descriptions  
(continued)**

| Bit | Field                                                     | Type | Reset | Description                                                                                                                  |
|-----|-----------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 0   | MPU_PROT_INTR_ERRAGG3_STATUS_RAW MPU_L2_BANK_A_PROT_ERRR3 | R/W  | 0h    | Raw Status of Error from MPU_PROT_INTR. Set irrespective if the Interrupt is masked or unmasked in MPU_PROT_INTR_ERRAGG_MASK |

### 2.2.2.137 MSS\_CTRL\_PRU\_ICSS\_PRU0\_MBOX\_WRITE\_DONE Register

#### 1 MSS\_CTRL\_PRU\_ICSS\_PRU0\_MBOX\_WRITE\_DONE Register (Offset = 14000h) [reset = 0h]

This register is used by ICSSM PRU0 to generate Mailbox interrupt to Recipient CPU.

Return to [Summary Table](#)

**Table 2-411. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 4000h       |

**Figure 2-137. MSS\_CTRL\_PRU\_ICSS\_PRU0\_MBOX\_WRITE\_DONE Name Register**

| 31       | 30 | 29 | 28                                               | 27       | 26 | 25 | 24                                               |
|----------|----|----|--------------------------------------------------|----------|----|----|--------------------------------------------------|
| RESERVED |    |    | PRU_ICSS_PR<br>U0_MBOX_WR<br>ITE_DONE_PR<br>OC_7 | RESERVED |    |    | PRU_ICSS_PR<br>U0_MBOX_WR<br>ITE_DONE_PR<br>OC_6 |
| NONE     |    |    | R/W                                              | NONE     |    |    | R/W                                              |
| 0h       |    |    | 0h                                               | 0h       |    |    | 0h                                               |
| 23       | 22 | 21 | 20                                               | 19       | 18 | 17 | 16                                               |
| RESERVED |    |    | PRU_ICSS_PR<br>U0_MBOX_WR<br>ITE_DONE_PR<br>OC_5 | RESERVED |    |    | PRU_ICSS_PR<br>U0_MBOX_WR<br>ITE_DONE_PR<br>OC_4 |
| NONE     |    |    | R/W                                              | NONE     |    |    | R/W                                              |
| 0h       |    |    | 0h                                               | 0h       |    |    | 0h                                               |
| 15       | 14 | 13 | 12                                               | 11       | 10 | 9  | 8                                                |
| RESERVED |    |    | PRU_ICSS_PR<br>U0_MBOX_WR<br>ITE_DONE_PR<br>OC_3 | RESERVED |    |    | PRU_ICSS_PR<br>U0_MBOX_WR<br>ITE_DONE_PR<br>OC_2 |
| NONE     |    |    | R/W                                              | NONE     |    |    | R/W                                              |
| 0h       |    |    | 0h                                               | 0h       |    |    | 0h                                               |
| 7        | 6  | 5  | 4                                                | 3        | 2  | 1  | 0                                                |
| RESERVED |    |    | PRU_ICSS_PR<br>U0_MBOX_WR<br>ITE_DONE_PR<br>OC_1 | RESERVED |    |    | PRU_ICSS_PR<br>U0_MBOX_WR<br>ITE_DONE_PR<br>OC_0 |
| NONE     |    |    | R/W                                              | NONE     |    |    | R/W                                              |
| 0h       |    |    | 0h                                               | 0h       |    |    | 0h                                               |

**Table 2-413. MSS\_CTRL\_PRU\_ICSS\_PRU0\_MBOX\_WRITE\_DONE Register Field Descriptions**

| Bit   | Field                                | Type | Reset | Description                                                                                                             |
|-------|--------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                |
| 28    | PRU_ICSS_PRU0_MBOX_WRITE_DONE_PROC_7 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 7 |
| 27:25 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                |
| 24    | PRU_ICSS_PRU0_MBOX_WRITE_DONE_PROC_6 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 6 |
| 23:21 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                |
| 20    | PRU_ICSS_PRU0_MBOX_WRITE_DONE_PROC_5 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 5 |

**Table 2-413. MSS\_CTRL\_PRU\_ICSS\_PRU0\_MBOX\_WRITE\_DONE Register Field Descriptions (continued)**

| Bit   | Field                                | Type | Reset | Description                                                                                                             |
|-------|--------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------|
| 19:17 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                |
| 16    | PRU_ICSS_PRU0_MBOX_WRITE_DONE_PROC_4 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 4 |
| 15:13 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                |
| 12    | PRU_ICSS_PRU0_MBOX_WRITE_DONE_PROC_3 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 3 |
| 11:9  | RESERVED                             | NONE | 0h    | Reserved                                                                                                                |
| 8     | PRU_ICSS_PRU0_MBOX_WRITE_DONE_PROC_2 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 2 |
| 7:5   | RESERVED                             | NONE | 0h    | Reserved                                                                                                                |
| 4     | PRU_ICSS_PRU0_MBOX_WRITE_DONE_PROC_1 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 1 |
| 3:1   | RESERVED                             | NONE | 0h    | Reserved                                                                                                                |
| 0     | PRU_ICSS_PRU0_MBOX_WRITE_DONE_PROC_0 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 0 |



### 2.2.2.138 MSS\_CTRL\_PRU\_ICSS\_PRU0\_MBOX\_READ\_REQ Register

#### 1 MSS\_CTRL\_PRU\_ICSS\_PRU0\_MBOX\_READ\_REQ Register (Offset = 14004h) [reset = 0h]

This register is used by ICSSM PRU0 to know the Sender of Mailbox Interrupt as well as clear it.

Return to [Summary Table](#)

**Table 2-414. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 4004h       |

**Figure 2-138. MSS\_CTRL\_PRU\_ICSS\_PRU0\_MBOX\_READ\_REQ Name Register**

| 31       | 30 | 29 | 28                                             | 27       | 26 | 25 | 24                                             |
|----------|----|----|------------------------------------------------|----------|----|----|------------------------------------------------|
| RESERVED |    |    | PRU_ICSS_PR<br>U0_MBOX_RE<br>AD_REQ_PRO<br>C_7 | RESERVED |    |    | PRU_ICSS_PR<br>U0_MBOX_RE<br>AD_REQ_PRO<br>C_6 |
| NONE     |    |    | R/W                                            | NONE     |    |    | R/W                                            |
| 0h       |    |    | 0h                                             | 0h       |    |    | 0h                                             |
| 23       | 22 | 21 | 20                                             | 19       | 18 | 17 | 16                                             |
| RESERVED |    |    | PRU_ICSS_PR<br>U0_MBOX_RE<br>AD_REQ_PRO<br>C_5 | RESERVED |    |    | PRU_ICSS_PR<br>U0_MBOX_RE<br>AD_REQ_PRO<br>C_4 |
| NONE     |    |    | R/W                                            | NONE     |    |    | R/W                                            |
| 0h       |    |    | 0h                                             | 0h       |    |    | 0h                                             |
| 15       | 14 | 13 | 12                                             | 11       | 10 | 9  | 8                                              |
| RESERVED |    |    | PRU_ICSS_PR<br>U0_MBOX_RE<br>AD_REQ_PRO<br>C_3 | RESERVED |    |    | PRU_ICSS_PR<br>U0_MBOX_RE<br>AD_REQ_PRO<br>C_2 |
| NONE     |    |    | R/W                                            | NONE     |    |    | R/W                                            |
| 0h       |    |    | 0h                                             | 0h       |    |    | 0h                                             |
| 7        | 6  | 5  | 4                                              | 3        | 2  | 1  | 0                                              |
| RESERVED |    |    | PRU_ICSS_PR<br>U0_MBOX_RE<br>AD_REQ_PRO<br>C_1 | RESERVED |    |    | PRU_ICSS_PR<br>U0_MBOX_RE<br>AD_REQ_PRO<br>C_0 |
| NONE     |    |    | R/W                                            | NONE     |    |    | R/W                                            |
| 0h       |    |    | 0h                                             | 0h       |    |    | 0h                                             |

**Table 2-416. MSS\_CTRL\_PRU\_ICSS\_PRU0\_MBOX\_READ\_REQ Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                      |
|-------|------------------------------------|------|-------|--------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED                           | NONE | 0h    | Reserved                                                                                         |
| 28    | PRU_ICSS_PRU0_MBOX_READ_REQ_PROC_7 | R/W  | 0h    | This is request from processor 7 to corresponding ICSSM_PRU. Requesting it to read from mailbox. |
| 27:25 | RESERVED                           | NONE | 0h    | Reserved                                                                                         |
| 24    | PRU_ICSS_PRU0_MBOX_READ_REQ_PROC_6 | R/W  | 0h    | This is request from processor 6 to corresponding ICSSM_PRU. Requesting it to read from mailbox. |
| 23:21 | RESERVED                           | NONE | 0h    | Reserved                                                                                         |
| 20    | PRU_ICSS_PRU0_MBOX_READ_REQ_PROC_5 | R/W  | 0h    | This is request from processor 5 to corresponding ICSSM_PRU. Requesting it to read from mailbox. |
| 19:17 | RESERVED                           | NONE | 0h    | Reserved                                                                                         |

**Table 2-416. MSS\_CTRL\_PRU\_ICSS\_PRU0\_MBOX\_READ\_REQ Register Field Descriptions (continued)**

| Bit   | Field                              | Type | Reset | Description                                                                                      |
|-------|------------------------------------|------|-------|--------------------------------------------------------------------------------------------------|
| 16    | PRU_ICSS_PRU0_MBOX_READ_REQ_PROC_4 | R/W  | 0h    | This is request from processor 4 to corresponding ICSSM_PRU. Requesting it to read from mailbox. |
| 15:13 | RESERVED                           | NONE | 0h    | Reserved                                                                                         |
| 12    | PRU_ICSS_PRU0_MBOX_READ_REQ_PROC_3 | R/W  | 0h    | This is request from processor 3 to corresponding ICSSM_PRU. Requesting it to read from mailbox. |
| 11:9  | RESERVED                           | NONE | 0h    | Reserved                                                                                         |
| 8     | PRU_ICSS_PRU0_MBOX_READ_REQ_PROC_2 | R/W  | 0h    | This is request from processor 2 to corresponding ICSSM_PRU. Requesting it to read from mailbox. |
| 7:5   | RESERVED                           | NONE | 0h    | Reserved                                                                                         |
| 4     | PRU_ICSS_PRU0_MBOX_READ_REQ_PROC_1 | R/W  | 0h    | This is request from processor 1 to corresponding ICSSM_PRU. Requesting it to read from mailbox. |
| 3:1   | RESERVED                           | NONE | 0h    | Reserved                                                                                         |
| 0     | PRU_ICSS_PRU0_MBOX_READ_REQ_PROC_0 | R/W  | 0h    | This is request from processor 0 to corresponding ICSSM_PRU. Requesting it to read from mailbox. |

### 2.2.2.139 MSS\_CTRL\_PRU\_ICSS\_PRU0\_MBOX\_READ\_DONE\_ACK Register

#### 1 MSS\_CTRL\_PRU\_ICSS\_PRU0\_MBOX\_READ\_DONE\_ACK Register (Offset = 14008h) [reset = 0h]

This register is used by ICSSM PRU0 to generate Mailbox Read acknowledgement to the Sender CPU.

Return to [Summary Table](#)

**Table 2-417. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 4008h       |

**Figure 2-139. MSS\_CTRL\_PRU\_ICSS\_PRU0\_MBOX\_READ\_DONE\_ACK Name Register**

|                                       |    |    |    |    |    |    |    |
|---------------------------------------|----|----|----|----|----|----|----|
| 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 23                                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 15                                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 7                                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PRU_ICSS_PRU0_MBOX_READ_DONE_ACK_PROC |    |    |    |    |    |    |    |
| R/W                                   |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |

**Table 2-419. MSS\_CTRL\_PRU\_ICSS\_PRU0\_MBOX\_READ\_DONE\_ACK Register Field Descriptions**

| Bit  | Field                                 | Type | Reset | Description                                                                                                                                                                                                                         |
|------|---------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED                              | NONE | 0h    | Reserved                                                                                                                                                                                                                            |
| 7:0  | PRU_ICSS_PRU0_MBOX_READ_DONE_ACK_PROC | R/W  | 0h    | Write pulse bit field:<br>For bits 0 to 7: Wrting<br>1'b1 : Generates pulse interrupt to corresponding proc from ICSSM_PRU0.<br>For bits 8 to 15: Wrting<br>1'b1 : Generates pulse interrupt to corresponding proc from ICSSM_PRU1. |

### 2.2.2.140 MSS\_CTRL\_PRU\_ICSS\_PRU0\_MBOX\_READ\_DONE Register

#### 1 MSS\_CTRL\_PRU\_ICSS\_PRU0\_MBOX\_READ\_DONE Register (Offset = 1400Ch) [reset = 0h]

This register is used by ICSSM PRU0 to know that the Receiver CPU has read the Mailbox and Acked. It is also used to clear the Read Done Interrupt.

Return to [Summary Table](#)

**Table 2-420. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 400Ch       |

**Figure 2-140. MSS\_CTRL\_PRU\_ICSS\_PRU0\_MBOX\_READ\_DONE Name Register**

| 31       | 30 | 29 | 28                                              | 27       | 26 | 25 | 24                                              |
|----------|----|----|-------------------------------------------------|----------|----|----|-------------------------------------------------|
| RESERVED |    |    | PRU_ICSS_PR<br>U0_MBOX_RE<br>AD_DONE_PR<br>OC_7 | RESERVED |    |    | PRU_ICSS_PR<br>U0_MBOX_RE<br>AD_DONE_PR<br>OC_6 |
| NONE     |    |    | R/W                                             | NONE     |    |    | R/W                                             |
| 0h       |    |    | 0h                                              | 0h       |    |    | 0h                                              |
| 23       | 22 | 21 | 20                                              | 19       | 18 | 17 | 16                                              |
| RESERVED |    |    | PRU_ICSS_PR<br>U0_MBOX_RE<br>AD_DONE_PR<br>OC_5 | RESERVED |    |    | PRU_ICSS_PR<br>U0_MBOX_RE<br>AD_DONE_PR<br>OC_4 |
| NONE     |    |    | R/W                                             | NONE     |    |    | R/W                                             |
| 0h       |    |    | 0h                                              | 0h       |    |    | 0h                                              |
| 15       | 14 | 13 | 12                                              | 11       | 10 | 9  | 8                                               |
| RESERVED |    |    | PRU_ICSS_PR<br>U0_MBOX_RE<br>AD_DONE_PR<br>OC_3 | RESERVED |    |    | PRU_ICSS_PR<br>U0_MBOX_RE<br>AD_DONE_PR<br>OC_2 |
| NONE     |    |    | R/W                                             | NONE     |    |    | R/W                                             |
| 0h       |    |    | 0h                                              | 0h       |    |    | 0h                                              |
| 7        | 6  | 5  | 4                                               | 3        | 2  | 1  | 0                                               |
| RESERVED |    |    | PRU_ICSS_PR<br>U0_MBOX_RE<br>AD_DONE_PR<br>OC_1 | RESERVED |    |    | PRU_ICSS_PR<br>U0_MBOX_RE<br>AD_DONE_PR<br>OC_0 |
| NONE     |    |    | R/W                                             | NONE     |    |    | R/W                                             |
| 0h       |    |    | 0h                                              | 0h       |    |    | 0h                                              |

**Table 2-422. MSS\_CTRL\_PRU\_ICSS\_PRU0\_MBOX\_READ\_DONE Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                                                                    |
|-------|-------------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED                            | NONE | 0h    | Reserved                                                                                                       |
| 28    | PRU_ICSS_PRU0_MBOX_READ_DONE_PROC_7 | R/W  | 0h    | This register should be written once finishing Reading from corresponding proc7's mailbox written by ICSSM_PRU |
| 27:25 | RESERVED                            | NONE | 0h    | Reserved                                                                                                       |
| 24    | PRU_ICSS_PRU0_MBOX_READ_DONE_PROC_6 | R/W  | 0h    | This register should be written once finishing Reading from corresponding proc6's mailbox written by ICSSM_PRU |
| 23:21 | RESERVED                            | NONE | 0h    | Reserved                                                                                                       |
| 20    | PRU_ICSS_PRU0_MBOX_READ_DONE_PROC_5 | R/W  | 0h    | This register should be written once finishing Reading from corresponding proc5's mailbox written by ICSSM_PRU |
| 19:17 | RESERVED                            | NONE | 0h    | Reserved                                                                                                       |

**Table 2-422. MSS\_CTRL\_PRU\_ICSS\_PRU0\_MBOX\_READ\_DONE Register Field Descriptions (continued)**

| Bit   | Field                               | Type | Reset | Description                                                                                                    |
|-------|-------------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------|
| 16    | PRU_ICSS_PRU0_MBOX_READ_DONE_PROC_4 | R/W  | 0h    | This register should be written once finishing Reading from corresponding proc4's mailbox written by ICSSM_PRU |
| 15:13 | RESERVED                            | NONE | 0h    | Reserved                                                                                                       |
| 12    | PRU_ICSS_PRU0_MBOX_READ_DONE_PROC_3 | R/W  | 0h    | This register should be written once finishing Reading from corresponding proc3's mailbox written by ICSSM_PRU |
| 11:9  | RESERVED                            | NONE | 0h    | Reserved                                                                                                       |
| 8     | PRU_ICSS_PRU0_MBOX_READ_DONE_PROC_2 | R/W  | 0h    | This register should be written once finishing Reading from corresponding proc2's mailbox written by ICSSM_PRU |
| 7:5   | RESERVED                            | NONE | 0h    | Reserved                                                                                                       |
| 4     | PRU_ICSS_PRU0_MBOX_READ_DONE_PROC_1 | R/W  | 0h    | This register should be written once finishing Reading from corresponding proc1's mailbox written by ICSSM_PRU |
| 3:1   | RESERVED                            | NONE | 0h    | Reserved                                                                                                       |
| 0     | PRU_ICSS_PRU0_MBOX_READ_DONE_PROC_0 | R/W  | 0h    | This register should be written once finishing Reading from corresponding proc0's mailbox written by ICSSM_PRU |

### 2.2.2.141 MSS\_CTRL\_PRU\_ICSS\_PRU1\_MBOX\_WRITE\_DONE Register

#### 1 MSS\_CTRL\_PRU\_ICSS\_PRU1\_MBOX\_WRITE\_DONE Register (Offset = 14010h) [reset = 0h]

This register is used by ICSSM PRU1 to generate Mailbox interrupt to Recipient CPU.

Return to [Summary Table](#)

**Table 2-423. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 4010h       |

**Figure 2-141. MSS\_CTRL\_PRU\_ICSS\_PRU1\_MBOX\_WRITE\_DONE Name Register**

| 31       | 30 | 29 | 28                                               | 27       | 26 | 25 | 24                                               |
|----------|----|----|--------------------------------------------------|----------|----|----|--------------------------------------------------|
| RESERVED |    |    | PRU_ICSS_PR<br>U1_MBOX_WR<br>ITE_DONE_PR<br>OC_7 | RESERVED |    |    | PRU_ICSS_PR<br>U1_MBOX_WR<br>ITE_DONE_PR<br>OC_6 |
| NONE     |    |    | R/W                                              | NONE     |    |    | R/W                                              |
| 0h       |    |    | 0h                                               | 0h       |    |    | 0h                                               |
| 23       | 22 | 21 | 20                                               | 19       | 18 | 17 | 16                                               |
| RESERVED |    |    | PRU_ICSS_PR<br>U1_MBOX_WR<br>ITE_DONE_PR<br>OC_5 | RESERVED |    |    | PRU_ICSS_PR<br>U1_MBOX_WR<br>ITE_DONE_PR<br>OC_4 |
| NONE     |    |    | R/W                                              | NONE     |    |    | R/W                                              |
| 0h       |    |    | 0h                                               | 0h       |    |    | 0h                                               |
| 15       | 14 | 13 | 12                                               | 11       | 10 | 9  | 8                                                |
| RESERVED |    |    | PRU_ICSS_PR<br>U1_MBOX_WR<br>ITE_DONE_PR<br>OC_3 | RESERVED |    |    | PRU_ICSS_PR<br>U1_MBOX_WR<br>ITE_DONE_PR<br>OC_2 |
| NONE     |    |    | R/W                                              | NONE     |    |    | R/W                                              |
| 0h       |    |    | 0h                                               | 0h       |    |    | 0h                                               |
| 7        | 6  | 5  | 4                                                | 3        | 2  | 1  | 0                                                |
| RESERVED |    |    | PRU_ICSS_PR<br>U1_MBOX_WR<br>ITE_DONE_PR<br>OC_1 | RESERVED |    |    | PRU_ICSS_PR<br>U1_MBOX_WR<br>ITE_DONE_PR<br>OC_0 |
| NONE     |    |    | R/W                                              | NONE     |    |    | R/W                                              |
| 0h       |    |    | 0h                                               | 0h       |    |    | 0h                                               |

**Table 2-425. MSS\_CTRL\_PRU\_ICSS\_PRU1\_MBOX\_WRITE\_DONE Register Field Descriptions**

| Bit   | Field                                | Type | Reset | Description                                                                                                             |
|-------|--------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                |
| 28    | PRU_ICSS_PRU1_MBOX_WRITE_DONE_PROC_7 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 7 |
| 27:25 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                |
| 24    | PRU_ICSS_PRU1_MBOX_WRITE_DONE_PROC_6 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 6 |
| 23:21 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                |
| 20    | PRU_ICSS_PRU1_MBOX_WRITE_DONE_PROC_5 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 5 |

**Table 2-425. MSS\_CTRL\_PRU\_ICSS\_PRU1\_MBOX\_WRITE\_DONE Register Field Descriptions (continued)**

| Bit   | Field                                | Type | Reset | Description                                                                                                             |
|-------|--------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------|
| 19:17 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                |
| 16    | PRU_ICSS_PRU1_MBOX_WRITE_DONE_PROC_4 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 4 |
| 15:13 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                |
| 12    | PRU_ICSS_PRU1_MBOX_WRITE_DONE_PROC_3 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 3 |
| 11:9  | RESERVED                             | NONE | 0h    | Reserved                                                                                                                |
| 8     | PRU_ICSS_PRU1_MBOX_WRITE_DONE_PROC_2 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 2 |
| 7:5   | RESERVED                             | NONE | 0h    | Reserved                                                                                                                |
| 4     | PRU_ICSS_PRU1_MBOX_WRITE_DONE_PROC_1 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 1 |
| 3:1   | RESERVED                             | NONE | 0h    | Reserved                                                                                                                |
| 0     | PRU_ICSS_PRU1_MBOX_WRITE_DONE_PROC_0 | R/W  | 0h    | Write pulse bit field:<br>This register should be written once finishing Writing into the mailbox memory of processor 0 |

### 2.2.2.142 MSS\_CTRL\_PRU\_ICSS\_PRU1\_MBOX\_READ\_REQ Register

#### 1 MSS\_CTRL\_PRU\_ICSS\_PRU1\_MBOX\_READ\_REQ Register (Offset = 14014h) [reset = 0h]

This register is used by ICSSM PRU1 to know the Sender of Mailbox Interrupt as well as clear it.

Return to [Summary Table](#)

**Table 2-426. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 4014h       |

**Figure 2-142. MSS\_CTRL\_PRU\_ICSS\_PRU1\_MBOX\_READ\_REQ Name Register**

| 31       | 30 | 29 | 28                                             | 27       | 26 | 25 | 24                                             |
|----------|----|----|------------------------------------------------|----------|----|----|------------------------------------------------|
| RESERVED |    |    | PRU_ICSS_PR<br>U1_MBOX_RE<br>AD_REQ_PRO<br>C_7 | RESERVED |    |    | PRU_ICSS_PR<br>U1_MBOX_RE<br>AD_REQ_PRO<br>C_6 |
| NONE     |    |    | R/W                                            | NONE     |    |    | R/W                                            |
| 0h       |    |    | 0h                                             | 0h       |    |    | 0h                                             |
| 23       | 22 | 21 | 20                                             | 19       | 18 | 17 | 16                                             |
| RESERVED |    |    | PRU_ICSS_PR<br>U1_MBOX_RE<br>AD_REQ_PRO<br>C_5 | RESERVED |    |    | PRU_ICSS_PR<br>U1_MBOX_RE<br>AD_REQ_PRO<br>C_4 |
| NONE     |    |    | R/W                                            | NONE     |    |    | R/W                                            |
| 0h       |    |    | 0h                                             | 0h       |    |    | 0h                                             |
| 15       | 14 | 13 | 12                                             | 11       | 10 | 9  | 8                                              |
| RESERVED |    |    | PRU_ICSS_PR<br>U1_MBOX_RE<br>AD_REQ_PRO<br>C_3 | RESERVED |    |    | PRU_ICSS_PR<br>U1_MBOX_RE<br>AD_REQ_PRO<br>C_2 |
| NONE     |    |    | R/W                                            | NONE     |    |    | R/W                                            |
| 0h       |    |    | 0h                                             | 0h       |    |    | 0h                                             |
| 7        | 6  | 5  | 4                                              | 3        | 2  | 1  | 0                                              |
| RESERVED |    |    | PRU_ICSS_PR<br>U1_MBOX_RE<br>AD_REQ_PRO<br>C_1 | RESERVED |    |    | PRU_ICSS_PR<br>U1_MBOX_RE<br>AD_REQ_PRO<br>C_0 |
| NONE     |    |    | R/W                                            | NONE     |    |    | R/W                                            |
| 0h       |    |    | 0h                                             | 0h       |    |    | 0h                                             |

**Table 2-428. MSS\_CTRL\_PRU\_ICSS\_PRU1\_MBOX\_READ\_REQ Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                      |
|-------|------------------------------------|------|-------|--------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED                           | NONE | 0h    | Reserved                                                                                         |
| 28    | PRU_ICSS_PRU1_MBOX_READ_REQ_PROC_7 | R/W  | 0h    | This is request from processor 7 to corresponding ICSSM_PRU. Requesting it to read from mailbox. |
| 27:25 | RESERVED                           | NONE | 0h    | Reserved                                                                                         |
| 24    | PRU_ICSS_PRU1_MBOX_READ_REQ_PROC_6 | R/W  | 0h    | This is request from processor 6 to corresponding ICSSM_PRU. Requesting it to read from mailbox. |
| 23:21 | RESERVED                           | NONE | 0h    | Reserved                                                                                         |
| 20    | PRU_ICSS_PRU1_MBOX_READ_REQ_PROC_5 | R/W  | 0h    | This is request from processor 5 to corresponding ICSSM_PRU. Requesting it to read from mailbox. |
| 19:17 | RESERVED                           | NONE | 0h    | Reserved                                                                                         |



**Table 2-428. MSS\_CTRL\_PRU\_ICSS\_PRU1\_MBOX\_READ\_REQ Register Field Descriptions (continued)**

| Bit   | Field                              | Type | Reset | Description                                                                                      |
|-------|------------------------------------|------|-------|--------------------------------------------------------------------------------------------------|
| 16    | PRU_ICSS_PRU1_MBOX_READ_REQ_PROC_4 | R/W  | 0h    | This is request from processor 4 to corresponding ICSSM_PRU. Requesting it to read from mailbox. |
| 15:13 | RESERVED                           | NONE | 0h    | Reserved                                                                                         |
| 12    | PRU_ICSS_PRU1_MBOX_READ_REQ_PROC_3 | R/W  | 0h    | This is request from processor 3 to corresponding ICSSM_PRU. Requesting it to read from mailbox. |
| 11:9  | RESERVED                           | NONE | 0h    | Reserved                                                                                         |
| 8     | PRU_ICSS_PRU1_MBOX_READ_REQ_PROC_2 | R/W  | 0h    | This is request from processor 2 to corresponding ICSSM_PRU. Requesting it to read from mailbox. |
| 7:5   | RESERVED                           | NONE | 0h    | Reserved                                                                                         |
| 4     | PRU_ICSS_PRU1_MBOX_READ_REQ_PROC_1 | R/W  | 0h    | This is request from processor 1 to corresponding ICSSM_PRU. Requesting it to read from mailbox. |
| 3:1   | RESERVED                           | NONE | 0h    | Reserved                                                                                         |
| 0     | PRU_ICSS_PRU1_MBOX_READ_REQ_PROC_0 | R/W  | 0h    | This is request from processor 0 to corresponding ICSSM_PRU. Requesting it to read from mailbox. |

### 2.2.2.143 MSS\_CTRL\_PRU\_ICSS\_PRU1\_MBOX\_READ\_DONE\_ACK Register

#### 1 MSS\_CTRL\_PRU\_ICSS\_PRU1\_MBOX\_READ\_DONE\_ACK Register (Offset = 14018h) [reset = 0h]

This register is used by ICSSM PRU1 to generate Mailbox Read acknowledgement to the Sender CPU.

Return to [Summary Table](#)

**Table 2-429. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 4018h       |

**Figure 2-143. MSS\_CTRL\_PRU\_ICSS\_PRU1\_MBOX\_READ\_DONE\_ACK Name Register**

|                                       |    |    |    |    |    |    |    |
|---------------------------------------|----|----|----|----|----|----|----|
| 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 23                                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 15                                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 7                                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PRU_ICSS_PRU1_MBOX_READ_DONE_ACK_PROC |    |    |    |    |    |    |    |
| R/W                                   |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |

**Table 2-431. MSS\_CTRL\_PRU\_ICSS\_PRU1\_MBOX\_READ\_DONE\_ACK Register Field Descriptions**

| Bit  | Field                                 | Type | Reset | Description                                                                                                                                                                                                                     |
|------|---------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED                              | NONE | 0h    | Reserved                                                                                                                                                                                                                        |
| 7:0  | PRU_ICSS_PRU1_MBOX_READ_DONE_ACK_PROC | R/W  | 0h    | Write pulse bit field:<br>For bits 0 to 7: Writing 1'b1 : Generates pulse interrupt to corresponding proc from ICSSM_PRU0.<br>For bits 8 to 15: Writing 1'b1 : Generates pulse interrupt to corresponding proc from ICSSM_PRU1. |

### 2.2.2.144 MSS\_CTRL\_PRU\_ICSS\_PRU1\_MBOX\_READ\_DONE Register

#### 1 MSS\_CTRL\_PRU\_ICSS\_PRU1\_MBOX\_READ\_DONE Register (Offset = 1401Ch) [reset = 0h]

This register is used by ICSSM PRU1 to know that the Receiver CPU has read the Mailbox and Acked. It is also used to clear the Read Done Interrupt.

Return to [Summary Table](#)

**Table 2-432. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 401Ch       |

**Figure 2-144. MSS\_CTRL\_PRU\_ICSS\_PRU1\_MBOX\_READ\_DONE Name Register**

| 31       | 30 | 29 | 28                                              | 27       | 26 | 25 | 24                                              |
|----------|----|----|-------------------------------------------------|----------|----|----|-------------------------------------------------|
| RESERVED |    |    | PRU_ICSS_PR<br>U1_MBOX_RE<br>AD_DONE_PR<br>OC_7 | RESERVED |    |    | PRU_ICSS_PR<br>U1_MBOX_RE<br>AD_DONE_PR<br>OC_6 |
| NONE     |    |    | R/W                                             | NONE     |    |    | R/W                                             |
| 0h       |    |    | 0h                                              | 0h       |    |    | 0h                                              |
| 23       | 22 | 21 | 20                                              | 19       | 18 | 17 | 16                                              |
| RESERVED |    |    | PRU_ICSS_PR<br>U1_MBOX_RE<br>AD_DONE_PR<br>OC_5 | RESERVED |    |    | PRU_ICSS_PR<br>U1_MBOX_RE<br>AD_DONE_PR<br>OC_4 |
| NONE     |    |    | R/W                                             | NONE     |    |    | R/W                                             |
| 0h       |    |    | 0h                                              | 0h       |    |    | 0h                                              |
| 15       | 14 | 13 | 12                                              | 11       | 10 | 9  | 8                                               |
| RESERVED |    |    | PRU_ICSS_PR<br>U1_MBOX_RE<br>AD_DONE_PR<br>OC_3 | RESERVED |    |    | PRU_ICSS_PR<br>U1_MBOX_RE<br>AD_DONE_PR<br>OC_2 |
| NONE     |    |    | R/W                                             | NONE     |    |    | R/W                                             |
| 0h       |    |    | 0h                                              | 0h       |    |    | 0h                                              |
| 7        | 6  | 5  | 4                                               | 3        | 2  | 1  | 0                                               |
| RESERVED |    |    | PRU_ICSS_PR<br>U1_MBOX_RE<br>AD_DONE_PR<br>OC_1 | RESERVED |    |    | PRU_ICSS_PR<br>U1_MBOX_RE<br>AD_DONE_PR<br>OC_0 |
| NONE     |    |    | R/W                                             | NONE     |    |    | R/W                                             |
| 0h       |    |    | 0h                                              | 0h       |    |    | 0h                                              |

**Table 2-434. MSS\_CTRL\_PRU\_ICSS\_PRU1\_MBOX\_READ\_DONE Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                                                                    |
|-------|-------------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED                            | NONE | 0h    | Reserved                                                                                                       |
| 28    | PRU_ICSS_PRU1_MBOX_READ_DONE_PROC_7 | R/W  | 0h    | This register should be written once finishing Reading from corresponding proc7's mailbox written by ICSSM_PRU |
| 27:25 | RESERVED                            | NONE | 0h    | Reserved                                                                                                       |
| 24    | PRU_ICSS_PRU1_MBOX_READ_DONE_PROC_6 | R/W  | 0h    | This register should be written once finishing Reading from corresponding proc6's mailbox written by ICSSM_PRU |
| 23:21 | RESERVED                            | NONE | 0h    | Reserved                                                                                                       |
| 20    | PRU_ICSS_PRU1_MBOX_READ_DONE_PROC_5 | R/W  | 0h    | This register should be written once finishing Reading from corresponding proc5's mailbox written by ICSSM_PRU |
| 19:17 | RESERVED                            | NONE | 0h    | Reserved                                                                                                       |

**Table 2-434. MSS\_CTRL\_PRU\_ICSS\_PRU1\_MBOX\_READ\_DONE Register Field Descriptions (continued)**

| Bit   | Field                               | Type | Reset | Description                                                                                                    |
|-------|-------------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------|
| 16    | PRU_ICSS_PRU1_MBOX_READ_DONE_PROC_4 | R/W  | 0h    | This register should be written once finishing Reading from corresponding proc4's mailbox written by ICSSM_PRU |
| 15:13 | RESERVED                            | NONE | 0h    | Reserved                                                                                                       |
| 12    | PRU_ICSS_PRU1_MBOX_READ_DONE_PROC_3 | R/W  | 0h    | This register should be written once finishing Reading from corresponding proc3's mailbox written by ICSSM_PRU |
| 11:9  | RESERVED                            | NONE | 0h    | Reserved                                                                                                       |
| 8     | PRU_ICSS_PRU1_MBOX_READ_DONE_PROC_2 | R/W  | 0h    | This register should be written once finishing Reading from corresponding proc2's mailbox written by ICSSM_PRU |
| 7:5   | RESERVED                            | NONE | 0h    | Reserved                                                                                                       |
| 4     | PRU_ICSS_PRU1_MBOX_READ_DONE_PROC_1 | R/W  | 0h    | This register should be written once finishing Reading from corresponding proc1's mailbox written by ICSSM_PRU |
| 3:1   | RESERVED                            | NONE | 0h    | Reserved                                                                                                       |
| 0     | PRU_ICSS_PRU1_MBOX_READ_DONE_PROC_0 | R/W  | 0h    | This register should be written once finishing Reading from corresponding proc0's mailbox written by ICSSM_PRU |

### 2.2.2.145 MSS\_CTRL\_MSS\_TPCC\_A\_ERRAGG\_MASK Register

#### 1 MSS\_CTRL\_MSS\_TPCC\_A\_ERRAGG\_MASK Register (Offset = 18000h) [reset = 0h]

This register Masks selected interrupt sources from generating the Aggregated TPCC0 Error Interrupt.

Return to [Summary Table](#)

**Table 2-435. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8000h       |

**Figure 2-145. MSS\_CTRL\_MSS\_TPCC\_A\_ERRAGG\_MASK Name Register**

| 31       | 30 | 29 | 28                                    | 27                                 | 26                                                | 25                                                | 24                                               |
|----------|----|----|---------------------------------------|------------------------------------|---------------------------------------------------|---------------------------------------------------|--------------------------------------------------|
| RESERVED |    |    |                                       |                                    | MSS_TPCC_A_ERRAGG_MASK_TPTC_A1_READ_ACCESS_ERROR  | MSS_TPCC_A_ERRAGG_MASK_TPTC_A0_READ_ACCESS_ERROR  | MSS_TPCC_A_ERRAGG_MASK_TPCC_A_READ_ACCESS_ERROR  |
| NONE     |    |    |                                       |                                    | R/W                                               | R/W                                               | R/W                                              |
| 0h       |    |    |                                       |                                    | 0h                                                | 0h                                                | 0h                                               |
| 23       | 22 | 21 | 20                                    | 19                                 | 18                                                | 17                                                | 16                                               |
| RESERVED |    |    |                                       |                                    | MSS_TPCC_A_ERRAGG_MASK_TPTC_A1_WRITE_ACCESS_ERROR | MSS_TPCC_A_ERRAGG_MASK_TPTC_A0_WRITE_ACCESS_ERROR | MSS_TPCC_A_ERRAGG_MASK_TPCC_A_WRITE_ACCESS_ERROR |
| NONE     |    |    |                                       |                                    | R/W                                               | R/W                                               | R/W                                              |
| 0h       |    |    |                                       |                                    | 0h                                                | 0h                                                | 0h                                               |
| 15       | 14 | 13 | 12                                    | 11                                 | 10                                                | 9                                                 | 8                                                |
| RESERVED |    |    |                                       |                                    |                                                   |                                                   |                                                  |
| NONE     |    |    |                                       |                                    |                                                   |                                                   |                                                  |
| 0h       |    |    |                                       |                                    |                                                   |                                                   |                                                  |
| 7        | 6  | 5  | 4                                     | 3                                  | 2                                                 | 1                                                 | 0                                                |
| RESERVED |    |    | MSS_TPCC_A_ERRAGG_MASK_TPCC_A_PAR_ERR | MSS_TPCC_A_ERRAGG_MASK_TPTC_A1_ERR | MSS_TPCC_A_ERRAGG_MASK_TPTC_A0_ERR                | MSS_TPCC_A_ERRAGG_MASK_TPCC_A_MP_INT              | MSS_TPCC_A_ERRAGG_MASK_TPCC_A_ERINT              |
| NONE     |    |    | R/W                                   | R/W                                | R/W                                               | R/W                                               | R/W                                              |
| 0h       |    |    | 0h                                    | 0h                                 | 0h                                                | 0h                                                | 0h                                               |

**Table 2-437. MSS\_CTRL\_MSS\_TPCC\_A\_ERRAGG\_MASK Register Field Descriptions**

| Bit   | Field                                            | Type | Reset | Description                                                                                                             |
|-------|--------------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------|
| 31:27 | RESERVED                                         | NONE | 0h    | Reserved                                                                                                                |
| 26    | MSS_TPCC_A_ERRAGG_MASK_TPTC_A1_READ_ACCESS_ERROR | R/W  | 0h    | Mask Error from MSS_TPTC_A1 to aggregated Error MSS_TPCC_A_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 25    | MSS_TPCC_A_ERRAGG_MASK_TPTC_A0_READ_ACCESS_ERROR | R/W  | 0h    | Mask Error from MSS_TPTC_A0 to aggregated Error MSS_TPCC_A_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 24    | MSS_TPCC_A_ERRAGG_MASK_TPCC_A_READ_ACCESS_ERROR  | R/W  | 0h    | Mask Error from MSS_TPCC_A to aggregated Error MSS_TPCC_A_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked  |

**Table 2-437. MSS\_CTRL\_MSS\_TPCC\_A\_ERRAGG\_MASK Register Field Descriptions (continued)**

| Bit   | Field                                             | Type | Reset | Description                                                                                                             |
|-------|---------------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------|
| 23:19 | RESERVED                                          | NONE | 0h    | Reserved                                                                                                                |
| 18    | MSS_TPCC_A_ERRAGG_MASK_TPTC_A1_WRITE_ACCESS_ERROR | R/W  | 0h    | Mask Error from MSS_TPTC_A1 to aggregated Error MSS_TPCC_A_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 17    | MSS_TPCC_A_ERRAGG_MASK_TPTC_A0_WRITE_ACCESS_ERROR | R/W  | 0h    | Mask Error from MSS_TPTC_A0 to aggregated Error MSS_TPCC_A_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 16    | MSS_TPCC_A_ERRAGG_MASK_TPCC_A_WRITE_ACCESS_ERROR  | R/W  | 0h    | Mask Error from MSS_TPCC_A to aggregated Error MSS_TPCC_A_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked  |
| 15:5  | RESERVED                                          | NONE | 0h    | Reserved                                                                                                                |
| 4     | MSS_TPCC_A_ERRAGG_MASK_TPCC_A_PAR_ERROR           | R/W  | 0h    | Mask Error from MSS_TPCC_A to aggregated Error MSS_TPCC_A_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked  |
| 3     | MSS_TPCC_A_ERRAGG_MASK_TPTC_A1_ERR                | R/W  | 0h    | Mask Error from MSS_TPTC_A1 to aggregated Error MSS_TPCC_A_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 2     | MSS_TPCC_A_ERRAGG_MASK_TPTC_A0_ERR                | R/W  | 0h    | Mask Error from MSS_TPTC_A0 to aggregated Error MSS_TPCC_A_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked |
| 1     | MSS_TPCC_A_ERRAGG_MASK_TPCC_A_MPINT               | R/W  | 0h    | Mask Error from MSS_TPCC_A to aggregated Error MSS_TPCC_A_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked  |
| 0     | MSS_TPCC_A_ERRAGG_MASK_TPCC_A_ERRINT              | R/W  | 0h    | Mask Error from MSS_TPCC_A to aggregated Error MSS_TPCC_A_ERRAGG<br>1'b1 : Error is Masked<br>1'b0 : Error is Unmasked  |

### 2.2.2.146 MSS\_CTRL\_MSS\_TPCC\_A\_ERRAGG\_STATUS Register

#### 1 MSS\_CTRL\_MSS\_TPCC\_A\_ERRAGG\_STATUS Register (Offset = 18004h) [reset = 0h]

This register shows the Status of Unmasked Errors from TPCC0.

Return to [Summary Table](#)

**Table 2-438. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8004h       |

**Figure 2-146. MSS\_CTRL\_MSS\_TPCC\_A\_ERRAGG\_STATUS Name Register**

| 31       | 30 | 29 | 28                                      | 27                                   | 26                                                  | 25                                                  | 24                                                 |
|----------|----|----|-----------------------------------------|--------------------------------------|-----------------------------------------------------|-----------------------------------------------------|----------------------------------------------------|
| RESERVED |    |    |                                         |                                      | MSS_TPCC_A_ERRAGG_STATUS_TPTC_A1_READ_ACCESS_ERROR  | MSS_TPCC_A_ERRAGG_STATUS_TPTC_A0_READ_ACCESS_ERROR  | MSS_TPCC_A_ERRAGG_STATUS_TPCC_A_READ_ACCESS_ERROR  |
| NONE     |    |    |                                         |                                      | R/W                                                 | R/W                                                 | R/W                                                |
| 0h       |    |    |                                         |                                      | 0h                                                  | 0h                                                  | 0h                                                 |
| 23       | 22 | 21 | 20                                      | 19                                   | 18                                                  | 17                                                  | 16                                                 |
| RESERVED |    |    |                                         |                                      | MSS_TPCC_A_ERRAGG_STATUS_TPTC_A1_WRITE_ACCESS_ERROR | MSS_TPCC_A_ERRAGG_STATUS_TPTC_A0_WRITE_ACCESS_ERROR | MSS_TPCC_A_ERRAGG_STATUS_TPCC_A_WRITE_ACCESS_ERROR |
| NONE     |    |    |                                         |                                      | R/W                                                 | R/W                                                 | R/W                                                |
| 0h       |    |    |                                         |                                      | 0h                                                  | 0h                                                  | 0h                                                 |
| 15       | 14 | 13 | 12                                      | 11                                   | 10                                                  | 9                                                   | 8                                                  |
| RESERVED |    |    |                                         |                                      |                                                     |                                                     |                                                    |
| NONE     |    |    |                                         |                                      |                                                     |                                                     |                                                    |
| 0h       |    |    |                                         |                                      |                                                     |                                                     |                                                    |
| 7        | 6  | 5  | 4                                       | 3                                    | 2                                                   | 1                                                   | 0                                                  |
| RESERVED |    |    | MSS_TPCC_A_ERRAGG_STATUS_TPCC_A_PAR_ERR | MSS_TPCC_A_ERRAGG_STATUS_TPTC_A1_ERR | MSS_TPCC_A_ERRAGG_STATUS_TPTC_A0_ERR                | MSS_TPCC_A_ERRAGG_STATUS_TPCC_A_MPINT               | MSS_TPCC_A_ERRAGG_STATUS_TPCC_A_ERRINT             |
| NONE     |    |    | R/W                                     | R/W                                  | R/W                                                 | R/W                                                 | R/W                                                |
| 0h       |    |    | 0h                                      | 0h                                   | 0h                                                  | 0h                                                  | 0h                                                 |

**Table 2-440. MSS\_CTRL\_MSS\_TPCC\_A\_ERRAGG\_STATUS Register Field Descriptions**

| Bit   | Field                                              | Type | Reset | Description                                                                                                                        |
|-------|----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 31:27 | RESERVED                                           | NONE | 0h    | Reserved                                                                                                                           |
| 26    | MSS_TPCC_A_ERRAGG_STATUS_TPTC_A1_READ_ACCESS_ERROR | R/W  | 0h    | Status of Error from MSS_TPTC_A1.<br>Set only if Interrupt is unmasked in MSS_TPCC_A_ERRAGG_MASK<br>Write 0x1 to clear this Error. |
| 25    | MSS_TPCC_A_ERRAGG_STATUS_TPTC_A0_READ_ACCESS_ERROR | R/W  | 0h    | Status of Error from MSS_TPTC_A0.<br>Set only if Interrupt is unmasked in MSS_TPCC_A_ERRAGG_MASK<br>Write 0x1 to clear this Error. |
| 24    | MSS_TPCC_A_ERRAGG_STATUS_TPCC_A_READ_ACCESS_ERROR  | R/W  | 0h    | Status of Error from MSS_TPCC_A.<br>Set only if Interrupt is unmasked in MSS_TPCC_A_ERRAGG_MASK<br>Write 0x1 to clear this Error.  |
| 23:19 | RESERVED                                           | NONE | 0h    | Reserved                                                                                                                           |

**Table 2-440. MSS\_CTRL\_MSS\_TPCC\_A\_ERRAGG\_STATUS Register Field Descriptions (continued)**

| Bit  | Field                                               | Type | Reset | Description                                                                                                                        |
|------|-----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 18   | MSS_TPCC_A_ERRAGG_STATUS_TPTC_A1_WRITE_ACCESS_ERROR | R/W  | 0h    | Status of Error from MSS_TPTC_A1.<br>Set only if Interrupt is unmasked in MSS_TPCC_A_ERRAGG_MASK<br>Write 0x1 to clear this Error. |
| 17   | MSS_TPCC_A_ERRAGG_STATUS_TPTC_A0_WRITE_ACCESS_ERROR | R/W  | 0h    | Status of Error from MSS_TPTC_A0.<br>Set only if Interrupt is unmasked in MSS_TPCC_A_ERRAGG_MASK<br>Write 0x1 to clear this Error. |
| 16   | MSS_TPCC_A_ERRAGG_STATUS_TPCC_A_WRITE_ACCESS_ERROR  | R/W  | 0h    | Status of Error from MSS_TPCC_A.<br>Set only if Interrupt is unmasked in MSS_TPCC_A_ERRAGG_MASK<br>Write 0x1 to clear this Error.  |
| 15:5 | RESERVED                                            | NONE | 0h    | Reserved                                                                                                                           |
| 4    | MSS_TPCC_A_ERRAGG_STATUS_TPCC_A_PAR_ERR             | R/W  | 0h    | Status of Error from MSS_TPCC_A.<br>Set only if Interrupt is unmasked in MSS_TPCC_A_ERRAGG_MASK<br>Write 0x1 to clear this Error.  |
| 3    | MSS_TPCC_A_ERRAGG_STATUS_TPTC_A1_ERR                | R/W  | 0h    | Status of Error from MSS_TPTC_A1.<br>Set only if Interrupt is unmasked in MSS_TPCC_A_ERRAGG_MASK<br>Write 0x1 to clear this Error. |
| 2    | MSS_TPCC_A_ERRAGG_STATUS_TPTC_A0_ERR                | R/W  | 0h    | Status of Error from MSS_TPTC_A0.<br>Set only if Interrupt is unmasked in MSS_TPCC_A_ERRAGG_MASK<br>Write 0x1 to clear this Error. |
| 1    | MSS_TPCC_A_ERRAGG_STATUS_TPCC_A_MPINT               | R/W  | 0h    | Status of Error from MSS_TPCC_A.<br>Set only if Interrupt is unmasked in MSS_TPCC_A_ERRAGG_MASK<br>Write 0x1 to clear this Error.  |
| 0    | MSS_TPCC_A_ERRAGG_STATUS_TPCC_A_ERRINT              | R/W  | 0h    | Status of Error from MSS_TPCC_A.<br>Set only if Interrupt is unmasked in MSS_TPCC_A_ERRAGG_MASK<br>Write 0x1 to clear this Error.  |



### 2.2.2.147 MSS\_CTRL\_MSS\_TPCC\_A\_ERRAGG\_STATUS\_RAW Register

#### 1 MSS\_CTRL\_MSS\_TPCC\_A\_ERRAGG\_STATUS\_RAW Register (Offset = 18008h) [reset = 0h]

This register shows the Status of all Errors from TPCC0.

Return to [Summary Table](#)

**Table 2-441. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8008h       |

**Figure 2-147. MSS\_CTRL\_MSS\_TPCC\_A\_ERRAGG\_STATUS\_RAW Name Register**

| 31       | 30 | 29 | 28                                                    | 27                                       | 26                                                      | 25                                                      | 24                                                     |
|----------|----|----|-------------------------------------------------------|------------------------------------------|---------------------------------------------------------|---------------------------------------------------------|--------------------------------------------------------|
| RESERVED |    |    |                                                       |                                          | MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A1_READ_ACCESS_ERROR  | MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A0_READ_ACCESS_ERROR  | MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A_READ_ACCESS_ERROR  |
| NONE     |    |    |                                                       |                                          | R/W                                                     | R/W                                                     | R/W                                                    |
| 0h       |    |    |                                                       |                                          | 0h                                                      | 0h                                                      | 0h                                                     |
| 23       | 22 | 21 | 20                                                    | 19                                       | 18                                                      | 17                                                      | 16                                                     |
| RESERVED |    |    |                                                       |                                          | MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A1_WRITE_ACCESS_ERROR | MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A0_WRITE_ACCESS_ERROR | MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A_WRITE_ACCESS_ERROR |
| NONE     |    |    |                                                       |                                          | R/W                                                     | R/W                                                     | R/W                                                    |
| 0h       |    |    |                                                       |                                          | 0h                                                      | 0h                                                      | 0h                                                     |
| 15       | 14 | 13 | 12                                                    | 11                                       | 10                                                      | 9                                                       | 8                                                      |
| RESERVED |    |    |                                                       |                                          |                                                         |                                                         |                                                        |
| NONE     |    |    |                                                       |                                          |                                                         |                                                         |                                                        |
| 0h       |    |    |                                                       |                                          |                                                         |                                                         |                                                        |
| 7        | 6  | 5  | 4                                                     | 3                                        | 2                                                       | 1                                                       | 0                                                      |
| RESERVED |    |    | MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A_READ_ACCESS_ERROR | MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A1_ERR | MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A0_ERR                | MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A_MPINT               | MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A_ERRINT             |
| NONE     |    |    | R/W                                                   | R/W                                      | R/W                                                     | R/W                                                     | R/W                                                    |
| 0h       |    |    | 0h                                                    | 0h                                       | 0h                                                      | 0h                                                      | 0h                                                     |

**Table 2-443. MSS\_CTRL\_MSS\_TPCC\_A\_ERRAGG\_STATUS\_RAW Register Field Descriptions**

| Bit   | Field                                                  | Type | Reset | Description                                                                                                             |
|-------|--------------------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------|
| 31:27 | RESERVED                                               | NONE | 0h    | Reserved                                                                                                                |
| 26    | MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A1_READ_ACCESS_ERROR | R/W  | 0h    | Raw Status of Error from MSS_TPTC_A1. Set irrespective if the Interrupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK |
| 25    | MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A0_READ_ACCESS_ERROR | R/W  | 0h    | Raw Status of Error from MSS_TPTC_A0. Set irrespective if the Interrupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK |

**Table 2-443. MSS\_CTRL\_MSS\_TPCC\_A\_ERRAGG\_STATUS\_RAW Register Field Descriptions (continued)**

| Bit   | Field                                                   | Type | Reset | Description                                                                                                             |
|-------|---------------------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------|
| 24    | MSS_TPCC_A_ERRAGG_STATUS_RAW_TPCC_A_READ_ACCESS_ERROR   | R/W  | 0h    | Raw Status of Error from MSS_TPCC_A. Set irrespective if the Interrupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK  |
| 23:19 | RESERVED                                                | NONE | 0h    | Reserved                                                                                                                |
| 18    | MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A1_WRITE_ACCESS_ERROR | R/W  | 0h    | Raw Status of Error from MSS_TPTC_A1. Set irrespective if the Interrupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK |
| 17    | MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A0_WRITE_ACCESS_ERROR | R/W  | 0h    | Raw Status of Error from MSS_TPTC_A0. Set irrespective if the Interrupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK |
| 16    | MSS_TPCC_A_ERRAGG_STATUS_RAW_TPCC_A_WRITE_ACCESS_ERROR  | R/W  | 0h    | Raw Status of Error from MSS_TPCC_A. Set irrespective if the Interrupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK  |
| 15:5  | RESERVED                                                | NONE | 0h    | Reserved                                                                                                                |
| 4     | MSS_TPCC_A_ERRAGG_STATUS_RAW_TPCC_A_PAR_ERR             | R/W  | 0h    | Raw Status of Error from MSS_TPCC_A. Set irrespective if the Interrupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK  |
| 3     | MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A1_ERR                | R/W  | 0h    | Raw Status of Error from MSS_TPTC_A1. Set irrespective if the Interrupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK |
| 2     | MSS_TPCC_A_ERRAGG_STATUS_RAW_TPTC_A0_ERR                | R/W  | 0h    | Raw Status of Error from MSS_TPTC_A0. Set irrespective if the Interrupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK |
| 1     | MSS_TPCC_A_ERRAGG_STATUS_RAW_TPCC_A_MPINT               | R/W  | 0h    | Raw Status of Error from MSS_TPCC_A. Set irrespective if the Interrupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK  |
| 0     | MSS_TPCC_A_ERRAGG_STATUS_RAW_TPCC_A_ERRINT              | R/W  | 0h    | Raw Status of Error from MSS_TPCC_A. Set irrespective if the Interrupt is masked or unmasked in MSS_TPCC_A_ERRAGG_MASK  |

### 2.2.2.148 MSS\_CTRL\_MSS\_PERIPH\_ERRAGG\_MASK0 Register

#### 1 MSS\_CTRL\_MSS\_PERIPH\_ERRAGG\_MASK0 Register (Offset = 18010h) [reset = 0h]

This register Masks selected interrupt sources from generating the Aggregated MMR Access Error Interrupt.

Return to [Summary Table](#)

**Table 2-444. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8010h       |

**Figure 2-148. MSS\_CTRL\_MSS\_PERIPH\_ERRAGG\_MASK0 Name Register**

|                                    |                                    |                                     |                                     |                                     |                                     |                                         |                                         |
|------------------------------------|------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|-----------------------------------------|-----------------------------------------|
| 31                                 | 30                                 | 29                                  | 28                                  | 27                                  | 26                                  | 25                                      | 24                                      |
| RESERVED                           |                                    |                                     |                                     |                                     |                                     |                                         |                                         |
| NONE                               |                                    |                                     |                                     |                                     |                                     |                                         |                                         |
| 0h                                 |                                    |                                     |                                     |                                     |                                     |                                         |                                         |
| 23                                 | 22                                 | 21                                  | 20                                  | 19                                  | 18                                  | 17                                      | 16                                      |
| RESERVED                           |                                    |                                     |                                     |                                     |                                     |                                         |                                         |
| NONE                               |                                    |                                     |                                     |                                     |                                     |                                         |                                         |
| 0h                                 |                                    |                                     |                                     |                                     |                                     |                                         |                                         |
| 15                                 | 14                                 | 13                                  | 12                                  | 11                                  | 10                                  | 9                                       | 8                                       |
| RESERVED                           |                                    |                                     |                                     | MSS_PERIPH_ERRAGG_MASK0_HSM_CTRL_WR | MSS_PERIPH_ERRAGG_MASK0_HSM_CTRL_RD | MSS_PERIPH_ERRAGG_MASK0_HSM_SOC_CTRL_WR | MSS_PERIPH_ERRAGG_MASK0_HSM_SOC_CTRL_RD |
| NONE                               |                                    |                                     |                                     | R/W                                 | R/W                                 | R/W                                     | R/W                                     |
| 0h                                 |                                    |                                     |                                     | 0h                                  | 0h                                  | 0h                                      | 0h                                      |
| 7                                  | 6                                  | 5                                   | 4                                   | 3                                   | 2                                   | 1                                       | 0                                       |
| MSS_PERIPH_ERRAGG_MASK0_TOP_RCM_WR | MSS_PERIPH_ERRAGG_MASK0_TOP_RCM_RD | MSS_PERIPH_ERRAGG_MASK0_TOP_CTRL_WR | MSS_PERIPH_ERRAGG_MASK0_TOP_CTRL_RD | MSS_PERIPH_ERRAGG_MASK0_MSS_RCM_WR  | MSS_PERIPH_ERRAGG_MASK0_MSS_RCM_RD  | MSS_PERIPH_ERRAGG_MASK0_MSS_CTRL_WR     | MSS_PERIPH_ERRAGG_MASK0_MSS_CTRL_RD     |
| R/W                                | R/W                                | R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                     | R/W                                     |
| 0h                                 | 0h                                 | 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                      | 0h                                      |

**Table 2-446. MSS\_CTRL\_MSS\_PERIPH\_ERRAGG\_MASK0 Register Field Descriptions**

| Bit   | Field                                   | Type | Reset | Description                                                                                                                                        |
|-------|-----------------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                                | NONE | 0h    | Reserved                                                                                                                                           |
| 11    | MSS_PERIPH_ERRAGG_MASK0_HSM_CTRL_WR     | R/W  | 0h    | Mask Interrupt from HSM_CTRL to aggregated Interrupt<br>MSS_PERIPH_ACCESS_ERRAGG<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked     |
| 10    | MSS_PERIPH_ERRAGG_MASK0_HSM_CTRL_RD     | R/W  | 0h    | Mask Interrupt from HSM_CTRL to aggregated Interrupt<br>MSS_PERIPH_ACCESS_ERRAGG<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked     |
| 9     | MSS_PERIPH_ERRAGG_MASK0_HSM_SOC_CTRL_WR | R/W  | 0h    | Mask Interrupt from HSM_SOC_CTRL to aggregated Interrupt<br>MSS_PERIPH_ACCESS_ERRAGG<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 8     | MSS_PERIPH_ERRAGG_MASK0_HSM_SOC_CTRL_RD | R/W  | 0h    | Mask Interrupt from HSM_SOC_CTRL to aggregated Interrupt<br>MSS_PERIPH_ACCESS_ERRAGG<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |

**Table 2-446. MSS\_CTRL\_MSS\_PERIPH\_ERRAGG\_MASK0 Register Field Descriptions (continued)**

| Bit | Field                               | Type | Reset | Description                                                                                                                                 |
|-----|-------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | MSS_PERIPH_ERRAGG_MASK0_TOP_RCM_WR  | R/W  | 0h    | Mask Interrupt from TOP_RCM to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked  |
| 6   | MSS_PERIPH_ERRAGG_MASK0_TOP_RCM_RD  | R/W  | 0h    | Mask Interrupt from TOP_RCM to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked  |
| 5   | MSS_PERIPH_ERRAGG_MASK0_TOP_CTRL_WR | R/W  | 0h    | Mask Interrupt from TOP_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 4   | MSS_PERIPH_ERRAGG_MASK0_TOP_CTRL_RD | R/W  | 0h    | Mask Interrupt from TOP_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 3   | MSS_PERIPH_ERRAGG_MASK0_MSS_RCM_WR  | R/W  | 0h    | Mask Interrupt from MSS_RCM to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked  |
| 2   | MSS_PERIPH_ERRAGG_MASK0_MSS_RCM_RD  | R/W  | 0h    | Mask Interrupt from MSS_RCM to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked  |
| 1   | MSS_PERIPH_ERRAGG_MASK0_MSS_CTRL_WR | R/W  | 0h    | Mask Interrupt from MSS_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 0   | MSS_PERIPH_ERRAGG_MASK0_MSS_CTRL_RD | R/W  | 0h    | Mask Interrupt from MSS_CTRL to aggregated Interrupt MSS_PERIPH_ACCESS_ERRAGG<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |

### 2.2.2.149 MSS\_CTRL\_MSS\_PERIPH\_ERRAGG\_STATUS0 Register

#### 1 MSS\_CTRL\_MSS\_PERIPH\_ERRAGG\_STATUS0 Register (Offset = 18014h) [reset = 0h]

This register shows the Status of Unmasked MMR Access Errors.

Return to [Summary Table](#)

**Table 2-447. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8014h       |

**Figure 2-149. MSS\_CTRL\_MSS\_PERIPH\_ERRAGG\_STATUS0 Name Register**

|                                     |                                     |                                      |                                      |                                      |                                      |                                          |                                          |
|-------------------------------------|-------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|------------------------------------------|------------------------------------------|
| 31                                  | 30                                  | 29                                   | 28                                   | 27                                   | 26                                   | 25                                       | 24                                       |
| RESERVED                            |                                     |                                      |                                      |                                      |                                      |                                          |                                          |
| NONE                                |                                     |                                      |                                      |                                      |                                      |                                          |                                          |
| 0h                                  |                                     |                                      |                                      |                                      |                                      |                                          |                                          |
| 23                                  | 22                                  | 21                                   | 20                                   | 19                                   | 18                                   | 17                                       | 16                                       |
| RESERVED                            |                                     |                                      |                                      |                                      |                                      |                                          |                                          |
| NONE                                |                                     |                                      |                                      |                                      |                                      |                                          |                                          |
| 0h                                  |                                     |                                      |                                      |                                      |                                      |                                          |                                          |
| 15                                  | 14                                  | 13                                   | 12                                   | 11                                   | 10                                   | 9                                        | 8                                        |
| RESERVED                            |                                     |                                      |                                      | MSS_PERIPH_ERRAGG_STATUS0_HSM_CTRL_W | MSS_PERIPH_ERRAGG_STATUS0_HSM_CTRL_R | MSS_PERIPH_ERRAGG_STATUS0_HSM_SOC_CTRL_W | MSS_PERIPH_ERRAGG_STATUS0_HSM_SOC_CTRL_R |
| NONE                                |                                     |                                      |                                      | R/W                                  | R/W                                  | R/W                                      | R/W                                      |
| 0h                                  |                                     |                                      |                                      | 0h                                   | 0h                                   | 0h                                       | 0h                                       |
| 7                                   | 6                                   | 5                                    | 4                                    | 3                                    | 2                                    | 1                                        | 0                                        |
| MSS_PERIPH_ERRAGG_STATUS0_TOP_RCM_W | MSS_PERIPH_ERRAGG_STATUS0_TOP_RCM_R | MSS_PERIPH_ERRAGG_STATUS0_TOP_CTRL_W | MSS_PERIPH_ERRAGG_STATUS0_TOP_CTRL_R | MSS_PERIPH_ERRAGG_STATUS0_MSS_RCM_W  | MSS_PERIPH_ERRAGG_STATUS0_MSS_RCM_R  | MSS_PERIPH_ERRAGG_STATUS0_MSS_CTRL_W     | MSS_PERIPH_ERRAGG_STATUS0_MSS_CTRL_R     |
| R/W                                 | R/W                                 | R/W                                  | R/W                                  | R/W                                  | R/W                                  | R/W                                      | R/W                                      |
| 0h                                  | 0h                                  | 0h                                   | 0h                                   | 0h                                   | 0h                                   | 0h                                       | 0h                                       |

**Table 2-449. MSS\_CTRL\_MSS\_PERIPH\_ERRAGG\_STATUS0 Register Field Descriptions**

| Bit   | Field                                    | Type | Reset | Description                                                                                                                                 |
|-------|------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                                 | NONE | 0h    | Reserved                                                                                                                                    |
| 11    | MSS_PERIPH_ERRAGG_STATUS0_HSM_CTRL_W     | R/W  | 0h    | Status of Interrupt from HSM_CTRL<br>Set only if Interrupt is unmasked in MSS_PERIPH_ERRAGG_MASK0<br>Write 0x1 to clear this interrupt.     |
| 10    | MSS_PERIPH_ERRAGG_STATUS0_HSM_CTRL_R     | R/W  | 0h    | Status of Interrupt from HSM_CTRL<br>Set only if Interrupt is unmasked in MSS_PERIPH_ERRAGG_MASK0<br>Write 0x1 to clear this interrupt.     |
| 9     | MSS_PERIPH_ERRAGG_STATUS0_HSM_SOC_CTRL_W | R/W  | 0h    | Status of Interrupt from HSM_SOC_CTRL<br>Set only if Interrupt is unmasked in MSS_PERIPH_ERRAGG_MASK0<br>Write 0x1 to clear this interrupt. |
| 8     | MSS_PERIPH_ERRAGG_STATUS0_HSM_SOC_CTRL_R | R/W  | 0h    | Status of Interrupt from HSM_SOC_CTRL<br>Set only if Interrupt is unmasked in MSS_PERIPH_ERRAGG_MASK0<br>Write 0x1 to clear this interrupt. |
| 7     | MSS_PERIPH_ERRAGG_STATUS0_TOP_RCM_W      | R/W  | 0h    | Status of Interrupt from TOP_RCM<br>Set only if Interrupt is unmasked in MSS_PERIPH_ERRAGG_MASK0<br>Write 0x1 to clear this interrupt.      |

**Table 2-449. MSS\_CTRL\_MSS\_PERIPH\_ERRAGG\_STATUS0 Register Field Descriptions (continued)**

| Bit | Field                                  | Type | Reset | Description                                                                                                                           |
|-----|----------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 6   | MSS_PERIPH_ERRAGG_STATUS0_TOP_RCM_RD   | R/W  | 0h    | Status of Interrupt from TOP_RCM<br>Set only if Interupt is unmasked in MSS_PERIPH_ERRAGG_MASK0<br>Wrie 0x1 to clear this interrupt.  |
| 5   | MSS_PERIPH_ERRAGG_STATUS0_TOP_CTRL_W R | R/W  | 0h    | Status of Interrupt from TOP_CTRL<br>Set only if Interupt is unmasked in MSS_PERIPH_ERRAGG_MASK0<br>Wrie 0x1 to clear this interrupt. |
| 4   | MSS_PERIPH_ERRAGG_STATUS0_TOP_CTRL_R D | R/W  | 0h    | Status of Interrupt from TOP_CTRL<br>Set only if Interupt is unmasked in MSS_PERIPH_ERRAGG_MASK0<br>Wrie 0x1 to clear this interrupt. |
| 3   | MSS_PERIPH_ERRAGG_STATUS0_MSS_RCM_W R  | R/W  | 0h    | Status of Interrupt from MSS_RCM<br>Set only if Interupt is unmasked in MSS_PERIPH_ERRAGG_MASK0<br>Wrie 0x1 to clear this interrupt.  |
| 2   | MSS_PERIPH_ERRAGG_STATUS0_MSS_RCM_RD   | R/W  | 0h    | Status of Interrupt from MSS_RCM<br>Set only if Interupt is unmasked in MSS_PERIPH_ERRAGG_MASK0<br>Wrie 0x1 to clear this interrupt.  |
| 1   | MSS_PERIPH_ERRAGG_STATUS0_MSS_CTRL_W R | R/W  | 0h    | Status of Interrupt from MSS_CTRL<br>Set only if Interupt is unmasked in MSS_PERIPH_ERRAGG_MASK0<br>Wrie 0x1 to clear this interrupt. |
| 0   | MSS_PERIPH_ERRAGG_STATUS0_MSS_CTRL_R D | R/W  | 0h    | Status of Interrupt from MSS_CTRL<br>Set only if Interupt is unmasked in MSS_PERIPH_ERRAGG_MASK0<br>Wrie 0x1 to clear this interrupt. |

### 2.2.2.150 MSS\_CTRL\_MSS\_PERIPH\_ERRAGG\_STATUS\_RAW0 Register

#### 1 MSS\_CTRL\_MSS\_PERIPH\_ERRAGG\_STATUS\_RAW0 Register (Offset = 18018h) [reset = 0h]

This register shows the Status of all MMR Access Errors.

Return to [Summary Table](#)

**Table 2-450. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8018h       |

**Figure 2-150. MSS\_CTRL\_MSS\_PERIPH\_ERRAGG\_STATUS\_RAW0 Name Register**

|                                          |                                          |                                          |                                          |                                           |                                           |                                               |                                               |
|------------------------------------------|------------------------------------------|------------------------------------------|------------------------------------------|-------------------------------------------|-------------------------------------------|-----------------------------------------------|-----------------------------------------------|
| 31                                       | 30                                       | 29                                       | 28                                       | 27                                        | 26                                        | 25                                            | 24                                            |
| RESERVED                                 |                                          |                                          |                                          |                                           |                                           |                                               |                                               |
| NONE                                     |                                          |                                          |                                          |                                           |                                           |                                               |                                               |
| 0h                                       |                                          |                                          |                                          |                                           |                                           |                                               |                                               |
| 23                                       | 22                                       | 21                                       | 20                                       | 19                                        | 18                                        | 17                                            | 16                                            |
| RESERVED                                 |                                          |                                          |                                          |                                           |                                           |                                               |                                               |
| NONE                                     |                                          |                                          |                                          |                                           |                                           |                                               |                                               |
| 0h                                       |                                          |                                          |                                          |                                           |                                           |                                               |                                               |
| 15                                       | 14                                       | 13                                       | 12                                       | 11                                        | 10                                        | 9                                             | 8                                             |
| RESERVED                                 |                                          |                                          |                                          | MSS_PERIPH_ERRAGG_STATUS_RAW0_HSM_CTRL_WR | MSS_PERIPH_ERRAGG_STATUS_RAW0_HSM_CTRL_RD | MSS_PERIPH_ERRAGG_STATUS_RAW0_HSM_SOC_CTRL_WR | MSS_PERIPH_ERRAGG_STATUS_RAW0_HSM_SOC_CTRL_RD |
| NONE                                     |                                          |                                          |                                          | R/W                                       | R/W                                       | R/W                                           | R/W                                           |
| 0h                                       |                                          |                                          |                                          | 0h                                        | 0h                                        | 0h                                            | 0h                                            |
| 7                                        | 6                                        | 5                                        | 4                                        | 3                                         | 2                                         | 1                                             | 0                                             |
| MSS_PERIPH_ERRAGG_STATUS_RAW0_TOP_RCM_WR | MSS_PERIPH_ERRAGG_STATUS_RAW0_TOP_RCM_RD | MSS_PERIPH_ERRAGG_STATUS_RAW0_OP_CTRL_WR | MSS_PERIPH_ERRAGG_STATUS_RAW0_OP_CTRL_RD | MSS_PERIPH_ERRAGG_STATUS_RAW0_SS_RCM_WR   | MSS_PERIPH_ERRAGG_STATUS_RAW0_SS_RCM_RD   | MSS_PERIPH_ERRAGG_STATUS_RAW0_SS_CTRL_WR      | MSS_PERIPH_ERRAGG_STATUS_RAW0_SS_CTRL_RD      |
| R/W                                      | R/W                                      | R/W                                      | R/W                                      | R/W                                       | R/W                                       | R/W                                           | R/W                                           |
| 0h                                       | 0h                                       | 0h                                       | 0h                                       | 0h                                        | 0h                                        | 0h                                            | 0h                                            |

**Table 2-452. MSS\_CTRL\_MSS\_PERIPH\_ERRAGG\_STATUS\_RAW0 Register Field Descriptions**

| Bit   | Field                                         | Type | Reset | Description                                                                                                                   |
|-------|-----------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                                      | NONE | 0h    | Reserved                                                                                                                      |
| 11    | MSS_PERIPH_ERRAGG_STATUS_RAW0_HSM_CTRL_WR     | R/W  | 0h    | Raw Status of Interrupt from HSM_CTRL. Set irrespective if the Interrupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0     |
| 10    | MSS_PERIPH_ERRAGG_STATUS_RAW0_HSM_CTRL_RD     | R/W  | 0h    | Raw Status of Interrupt from HSM_CTRL. Set irrespective if the Interrupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0     |
| 9     | MSS_PERIPH_ERRAGG_STATUS_RAW0_HSM_SOC_CTRL_WR | R/W  | 0h    | Raw Status of Interrupt from HSM_SOC_CTRL. Set irrespective if the Interrupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0 |
| 8     | MSS_PERIPH_ERRAGG_STATUS_RAW0_HSM_SOC_CTRL_RD | R/W  | 0h    | Raw Status of Interrupt from HSM_SOC_CTRL. Set irrespective if the Interrupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0 |
| 7     | MSS_PERIPH_ERRAGG_STATUS_RAW0_TOP_RCM_WR      | R/W  | 0h    | Raw Status of Interrupt from TOP_RCM. Set irrespective if the Interrupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0      |

**Table 2-452. MSS\_CTRL\_MSS\_PERIPH\_ERRAGG\_STATUS\_RAW0 Register Field Descriptions  
(continued)**

| Bit | Field                                     | Type | Reset | Description                                                                                                                  |
|-----|-------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 6   | MSS_PERIPH_ERRAGG_STATUS_RAW0_TOP_RCM_RD  | R/W  | 0h    | Raw Status of Interrupt from TOP_RCM.<br>Set irrespective if the Interrupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0  |
| 5   | MSS_PERIPH_ERRAGG_STATUS_RAW0_TOP_CTRL_WR | R/W  | 0h    | Raw Status of Interrupt from TOP_CTRL.<br>Set irrespective if the Interrupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0 |
| 4   | MSS_PERIPH_ERRAGG_STATUS_RAW0_TOP_CTRL_RD | R/W  | 0h    | Raw Status of Interrupt from TOP_CTRL.<br>Set irrespective if the Interrupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0 |
| 3   | MSS_PERIPH_ERRAGG_STATUS_RAW0_MSS_RCM_WR  | R/W  | 0h    | Raw Status of Interrupt from MSS_RCM.<br>Set irrespective if the Interrupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0  |
| 2   | MSS_PERIPH_ERRAGG_STATUS_RAW0_MSS_RCM_RD  | R/W  | 0h    | Raw Status of Interrupt from MSS_RCM.<br>Set irrespective if the Interrupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0  |
| 1   | MSS_PERIPH_ERRAGG_STATUS_RAW0_MSS_CTRL_WR | R/W  | 0h    | Raw Status of Interrupt from MSS_CTRL.<br>Set irrespective if the Interrupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0 |
| 0   | MSS_PERIPH_ERRAGG_STATUS_RAW0_MSS_CTRL_RD | R/W  | 0h    | Raw Status of Interrupt from MSS_CTRL.<br>Set irrespective if the Interrupt is masked or unmasked in MSS_PERIPH_ERRAGG_MASK0 |



### 2.2.2.151 MSS\_CTRL\_R5SS0\_CORE0\_ECC\_CORR\_ERRAGG\_MASK Register

#### 1 MSS\_CTRL\_R5SS0\_CORE0\_ECC\_CORR\_ERRAGG\_MASK Register (Offset = 18080h) [reset = 0h]

Register to Mask Correctable error from R5SS0 CORE0 Memories.

Return to [Summary Table](#)

**Table 2-453. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8080h       |

**Figure 2-151. MSS\_CTRL\_R5SS0\_CORE0\_ECC\_CORR\_ERRAGG\_MASK Name Register**

| 31       | 30                                                        | 29                                                       | 28                                                        | 27                                                       | 26                                                        | 25                                                        | 24                                                       |
|----------|-----------------------------------------------------------|----------------------------------------------------------|-----------------------------------------------------------|----------------------------------------------------------|-----------------------------------------------------------|-----------------------------------------------------------|----------------------------------------------------------|
| RESERVED |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| NONE     |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| 0h       |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| 23       | 22                                                        | 21                                                       | 20                                                        | 19                                                       | 18                                                        | 17                                                        | 16                                                       |
| RESERVED |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| NONE     |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| 0h       |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| 15       | 14                                                        | 13                                                       | 12                                                        | 11                                                       | 10                                                        | 9                                                         | 8                                                        |
| RESERVED |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| NONE     |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| 0h       |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| 7        | 6                                                         | 5                                                        | 4                                                         | 3                                                        | 2                                                         | 1                                                         | 0                                                        |
| RESERVED | R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_IDATA_CORR_ERR | R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_ITAG_CORR_ERR | R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_DDATA_CORR_ERR | R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_DTAG_CORR_ERR | R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_B0TCM_CORR_ERR | R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_B1TCM_CORR_ERR | R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_ATCM_CORR_ERR |
| NONE     | R/W                                                       | R/W                                                      | R/W                                                       | R/W                                                      | R/W                                                       | R/W                                                       | R/W                                                      |
| 0h       | 0h                                                        | 0h                                                       | 0h                                                        | 0h                                                       | 0h                                                        | 0h                                                        | 0h                                                       |

**Table 2-455. MSS\_CTRL\_R5SS0\_CORE0\_ECC\_CORR\_ERRAGG\_MASK Register Field Descriptions**

| Bit  | Field                                                     | Type | Reset | Description                                                                                                                                      |
|------|-----------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED                                                  | NONE | 0h    | Reserved                                                                                                                                         |
| 6    | R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_IDATA_CORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 5    | R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_ITAG_CORR_ERR  | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 4    | R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_DDATA_CORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 3    | R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_DTAG_CORR_ERR  | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |

**Table 2-455. MSS\_CTRL\_R5SS0\_CORE0\_ECC\_CORR\_ERRAGG\_MASK Register Field Descriptions  
(continued)**

| Bit | Field                                                     | Type | Reset | Description                                                                                                                                      |
|-----|-----------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_B0TCM_CORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 1   | R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_B1TCM_CORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 0   | R5SS0_CPU0_ECC_CORR_ERRAGG_MASK_R5SS0_CPU0_ATCM_CORR_ERR  | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |

### 2.2.2.152 MSS\_CTRL\_R5SS0\_CORE0\_ECC\_CORR\_ERRAGG\_STATUS Register

#### 1 MSS\_CTRL\_R5SS0\_CORE0\_ECC\_CORR\_ERRAGG\_STATUS Register (Offset = 18084h) [reset = 0h]

Status register based on mask for correctable error R5SS0 CORE0 Memories.

Return to [Summary Table](#)

**Table 2-456. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8084h       |

**Figure 2-152. MSS\_CTRL\_R5SS0\_CORE0\_ECC\_CORR\_ERRAGG\_STATUS Name Register**

| 31       | 30                                                          | 29                                                         | 28                                                          | 27                                                         | 26                                                          | 25                                                         | 24                                                         |
|----------|-------------------------------------------------------------|------------------------------------------------------------|-------------------------------------------------------------|------------------------------------------------------------|-------------------------------------------------------------|------------------------------------------------------------|------------------------------------------------------------|
| RESERVED |                                                             |                                                            |                                                             |                                                            |                                                             |                                                            |                                                            |
| NONE     |                                                             |                                                            |                                                             |                                                            |                                                             |                                                            |                                                            |
| 0h       |                                                             |                                                            |                                                             |                                                            |                                                             |                                                            |                                                            |
| 23       | 22                                                          | 21                                                         | 20                                                          | 19                                                         | 18                                                          | 17                                                         | 16                                                         |
| RESERVED |                                                             |                                                            |                                                             |                                                            |                                                             |                                                            |                                                            |
| NONE     |                                                             |                                                            |                                                             |                                                            |                                                             |                                                            |                                                            |
| 0h       |                                                             |                                                            |                                                             |                                                            |                                                             |                                                            |                                                            |
| 15       | 14                                                          | 13                                                         | 12                                                          | 11                                                         | 10                                                          | 9                                                          | 8                                                          |
| RESERVED |                                                             |                                                            |                                                             |                                                            |                                                             |                                                            |                                                            |
| NONE     |                                                             |                                                            |                                                             |                                                            |                                                             |                                                            |                                                            |
| 0h       |                                                             |                                                            |                                                             |                                                            |                                                             |                                                            |                                                            |
| 7        | 6                                                           | 5                                                          | 4                                                           | 3                                                          | 2                                                           | 1                                                          | 0                                                          |
| RESERVED | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_IDATA_CORR_ERR | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_ITAG_CORR_ERR | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_DDATA_CORR_ERR | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_DTAG_CORR_ERR | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_B1TCM_CORR_ERR | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_ATCM_CORR_ERR | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_ATCM_CORR_ERR |
| NONE     | R/W                                                         | R/W                                                        | R/W                                                         | R/W                                                        | R/W                                                         | R/W                                                        | R/W                                                        |
| 0h       | 0h                                                          | 0h                                                         | 0h                                                          | 0h                                                         | 0h                                                          | 0h                                                         | 0h                                                         |

**Table 2-458. MSS\_CTRL\_R5SS0\_CORE0\_ECC\_CORR\_ERRAGG\_STATUS Register Field Descriptions**

| Bit  | Field                                                       | Type | Reset | Description                                                                                                                                                                                          |
|------|-------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED                                                    | NONE | 0h    | Reserved                                                                                                                                                                                             |
| 6    | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_IDATA_CORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 5    | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_ITAG_CORR_ERR  | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 4    | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_DDATA_CORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 3    | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_DTAG_CORR_ERR  | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |

**Table 2-458. MSS\_CTRL\_R5SS0\_CORE0\_ECC\_CORR\_ERRAGG\_STATUS Register Field Descriptions  
(continued)**

| Bit | Field                                                       | Type | Reset | Description                                                                                                                                                                                          |
|-----|-------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_B0TCM_CORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 1   | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_B1TCM_CORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 0   | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU0_ATCM_CORR_ERR  | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |

### 2.2.2.153 MSS\_CTRL\_R5SS0\_CORE0\_ECC\_CORR\_ERRAGG\_STATUS\_RAW Register

**1 MSS\_CTRL\_R5SS0\_CORE0\_ECC\_CORR\_ERRAGG\_STATUS\_RAW Register (Offset = 18088h) [reset = 0h]**

Raw status for correctable error from R5SS0 CORE0 Memories.

Return to [Summary Table](#)

**Table 2-459. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8088h       |

**Figure 2-153. MSS\_CTRL\_R5SS0\_CORE0\_ECC\_CORR\_ERRAGG\_STATUS\_RAW Name Register**

| 31       | 30                                                              | 29                                                             | 28                                                              | 27                                                            | 26                                                               | 25                                                               | 24                                                              |
|----------|-----------------------------------------------------------------|----------------------------------------------------------------|-----------------------------------------------------------------|---------------------------------------------------------------|------------------------------------------------------------------|------------------------------------------------------------------|-----------------------------------------------------------------|
| RESERVED |                                                                 |                                                                |                                                                 |                                                               |                                                                  |                                                                  |                                                                 |
| NONE     |                                                                 |                                                                |                                                                 |                                                               |                                                                  |                                                                  |                                                                 |
| 0h       |                                                                 |                                                                |                                                                 |                                                               |                                                                  |                                                                  |                                                                 |
| 23       | 22                                                              | 21                                                             | 20                                                              | 19                                                            | 18                                                               | 17                                                               | 16                                                              |
| RESERVED |                                                                 |                                                                |                                                                 |                                                               |                                                                  |                                                                  |                                                                 |
| NONE     |                                                                 |                                                                |                                                                 |                                                               |                                                                  |                                                                  |                                                                 |
| 0h       |                                                                 |                                                                |                                                                 |                                                               |                                                                  |                                                                  |                                                                 |
| 15       | 14                                                              | 13                                                             | 12                                                              | 11                                                            | 10                                                               | 9                                                                | 8                                                               |
| RESERVED |                                                                 |                                                                |                                                                 |                                                               |                                                                  |                                                                  |                                                                 |
| NONE     |                                                                 |                                                                |                                                                 |                                                               |                                                                  |                                                                  |                                                                 |
| 0h       |                                                                 |                                                                |                                                                 |                                                               |                                                                  |                                                                  |                                                                 |
| 7        | 6                                                               | 5                                                              | 4                                                               | 3                                                             | 2                                                                | 1                                                                | 0                                                               |
| RESERVED | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_IDATA_CORR_ERR | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_ITAG_CORR_ERR | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_DDATA_CORR_ERR | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_DTA_CORR_ERR | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_B0T_CM_CORR_ERR | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_B1T_CM_CORR_ERR | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_ATC_M_CORR_ERR |
| NONE     | R/W                                                             | R/W                                                            | R/W                                                             | R/W                                                           | R/W                                                              | R/W                                                              | R/W                                                             |
| 0h       | 0h                                                              | 0h                                                             | 0h                                                              | 0h                                                            | 0h                                                               | 0h                                                               | 0h                                                              |

**Table 2-461. MSS\_CTRL\_R5SS0\_CORE0\_ECC\_CORR\_ERRAGG\_STATUS\_RAW Register Field Descriptions**

| Bit  | Field                                                           | Type | Reset | Description                                                                                                                                                                                        |
|------|-----------------------------------------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED                                                        | NONE | 0h    | Reserved                                                                                                                                                                                           |
| 6    | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_IDATA_CORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS* CPU* ECC_CORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |
| 5    | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_ITAG_CORR_ERR  | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS* CPU* ECC_CORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |
| 4    | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_DDATA_CORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS* CPU* ECC_CORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |

**Table 2-461. MSS\_CTRL\_R5SS0\_CORE0\_ECC\_CORR\_ERRAGG\_STATUS\_RAW Register Field Descriptions (continued)**

| Bit | Field                                                           | Type | Reset | Description                                                                                                                                                                                              |
|-----|-----------------------------------------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3   | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_DTAG_CORR_ERR  | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 2   | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_B0TCM_CORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 1   | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_B1TCM_CORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 0   | R5SS0_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_ATCM_CORR_ERR  | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |

### 2.2.2.154 MSS\_CTRL\_R5SS0\_CORE0\_ECC\_UNCORR\_ERRAGG\_MASK Register

#### 1 MSS\_CTRL\_R5SS0\_CORE0\_ECC\_UNCORR\_ERRAGG\_MASK Register (Offset = 18090h) [reset = 0h]

Register to Mask Uncorrectable error from R5SS0 CORE0 Memories.

Return to [Summary Table](#)

**Table 2-462. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8090h       |

**Figure 2-154. MSS\_CTRL\_R5SS0\_CORE0\_ECC\_UNCORR\_ERRAGG\_MASK Name Register**

|          |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
|----------|----|----|---------------------------------------------------------------|--------------------------------------------------------------|---------------------------------------------------------------|---------------------------------------------------------------|--------------------------------------------------------------|
| 31       | 30 | 29 | 28                                                            | 27                                                           | 26                                                            | 25                                                            | 24                                                           |
| RESERVED |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| NONE     |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| 0h       |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| 23       | 22 | 21 | 20                                                            | 19                                                           | 18                                                            | 17                                                            | 16                                                           |
| RESERVED |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| NONE     |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| 0h       |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| 15       | 14 | 13 | 12                                                            | 11                                                           | 10                                                            | 9                                                             | 8                                                            |
| RESERVED |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| NONE     |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| 0h       |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| 7        | 6  | 5  | 4                                                             | 3                                                            | 2                                                             | 1                                                             | 0                                                            |
| RESERVED |    |    | R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_DDATA_UNCORR_ERR | R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_DTAG_UNCORR_ERR | R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_B0TCM_UNCORR_ERR | R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_B1TCM_UNCORR_ERR | R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_ATCM_UNCORR_ERR |
| NONE     |    |    | R/W                                                           | R/W                                                          | R/W                                                           | R/W                                                           | R/W                                                          |
| 0h       |    |    | 0h                                                            | 0h                                                           | 0h                                                            | 0h                                                            | 0h                                                           |

**Table 2-464. MSS\_CTRL\_R5SS0\_CORE0\_ECC\_UNCORR\_ERRAGG\_MASK Register Field Descriptions**

| Bit  | Field                                                         | Type | Reset | Description                                                                                                                                      |
|------|---------------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:5 | RESERVED                                                      | NONE | 0h    | Reserved                                                                                                                                         |
| 4    | R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_DDATA_UNCORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 3    | R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_DTAG_UNCORR_ERR  | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 2    | R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_B0TCM_UNCORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 1    | R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_B1TCM_UNCORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |

**Table 2-464. MSS\_CTRL\_R5SS0\_CORE0\_ECC\_UNCORR\_ERRAGG\_MASK Register Field Descriptions  
(continued)**

| Bit | Field                                                        | Type | Reset | Description                                                                                                                                      |
|-----|--------------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | R5SS0_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU0_ATCM_UNCORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |



### 2.2.2.155 MSS\_CTRL\_R5SS0\_CORE0\_ECC\_UNCORR\_ERRAGG\_STATUS Register

#### 1 MSS\_CTRL\_R5SS0\_CORE0\_ECC\_UNCORR\_ERRAGG\_STATUS Register (Offset = 18094h) [reset = 0h]

Status register based on mask for uncorrectable error R5SS0 CORE0 Memories.

Return to [Summary Table](#)

**Table 2-465. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8094h       |

**Figure 2-155. MSS\_CTRL\_R5SS0\_CORE0\_ECC\_UNCORR\_ERRAGG\_STATUS Name Register**

|          |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
|----------|----|----|-----------------------------------------------------------------|----------------------------------------------------------------|-----------------------------------------------------------------|-----------------------------------------------------------------|----------------------------------------------------------------|
| 31       | 30 | 29 | 28                                                              | 27                                                             | 26                                                              | 25                                                              | 24                                                             |
| RESERVED |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| NONE     |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| 0h       |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| 23       | 22 | 21 | 20                                                              | 19                                                             | 18                                                              | 17                                                              | 16                                                             |
| RESERVED |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| NONE     |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| 0h       |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| 15       | 14 | 13 | 12                                                              | 11                                                             | 10                                                              | 9                                                               | 8                                                              |
| RESERVED |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| NONE     |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| 0h       |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| 7        | 6  | 5  | 4                                                               | 3                                                              | 2                                                               | 1                                                               | 0                                                              |
| RESERVED |    |    | R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_DDATA_UNCORR_ERR | R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_DTAG_UNCORR_ERR | R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_B0TCM_UNCORR_ERR | R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_B1TCM_UNCORR_ERR | R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_ATCM_UNCORR_ERR |
| NONE     |    |    | R/W                                                             | R/W                                                            | R/W                                                             | R/W                                                             | R/W                                                            |
| 0h       |    |    | 0h                                                              | 0h                                                             | 0h                                                              | 0h                                                              | 0h                                                             |

**Table 2-467. MSS\_CTRL\_R5SS0\_CORE0\_ECC\_UNCORR\_ERRAGG\_STATUS Register Field Descriptions**

| Bit  | Field                                                           | Type | Reset | Description                                                                                                                                                                                            |
|------|-----------------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:5 | RESERVED                                                        | NONE | 0h    | Reserved                                                                                                                                                                                               |
| 4    | R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_DDATA_UNCORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 3    | R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_DTAG_UNCORR_ERR  | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 2    | R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_B0TCM_UNCORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 1    | R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_B1TCM_UNCORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |

**Table 2-467. MSS\_CTRL\_R5SS0\_CORE0\_ECC\_UNCORR\_ERRAGG\_STATUS Register Field Descriptions  
(continued)**

| Bit | Field                                                          | Type | Reset | Description                                                                                                                                                                                            |
|-----|----------------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU0_ATCM_UNCORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |

### 2.2.2.156 MSS\_CTRL\_R5SS0\_CORE0\_ECC\_UNCORR\_ERRAGG\_STATUS\_RAW Register

**1 MSS\_CTRL\_R5SS0\_CORE0\_ECC\_UNCORR\_ERRAGG\_STATUS\_RAW Register (Offset = 18098h) [reset = 0h]**

Raw status for uncorrectable error from R5SS0 CORE0 Memories.

Return to [Summary Table](#)

**Table 2-468. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8098h       |

**Figure 2-156. MSS\_CTRL\_R5SS0\_CORE0\_ECC\_UNCORR\_ERRAGG\_STATUS\_RAW Name Register**

| 31       | 30 | 29 | 28                                                                 | 27                                                                | 26                                                                 | 25                                                                 | 24                                                                 |
|----------|----|----|--------------------------------------------------------------------|-------------------------------------------------------------------|--------------------------------------------------------------------|--------------------------------------------------------------------|--------------------------------------------------------------------|
| RESERVED |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                    |
| NONE     |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                    |
| 0h       |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                    |
| 23       | 22 | 21 | 20                                                                 | 19                                                                | 18                                                                 | 17                                                                 | 16                                                                 |
| RESERVED |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                    |
| NONE     |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                    |
| 0h       |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                    |
| 15       | 14 | 13 | 12                                                                 | 11                                                                | 10                                                                 | 9                                                                  | 8                                                                  |
| RESERVED |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                    |
| NONE     |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                    |
| 0h       |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                    |
| 7        | 6  | 5  | 4                                                                  | 3                                                                 | 2                                                                  | 1                                                                  | 0                                                                  |
| RESERVED |    |    | R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_DATA_UNCORR_ERR | R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_TAG_UNCORR_ERR | R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_0TCM_UNCORR_ERR | R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_1TCM_UNCORR_ERR | R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_ATCM_UNCORR_ERR |
| NONE     |    |    | R/W                                                                | R/W                                                               | R/W                                                                | R/W                                                                | R/W                                                                |
| 0h       |    |    | 0h                                                                 | 0h                                                                | 0h                                                                 | 0h                                                                 | 0h                                                                 |

**Table 2-470. MSS\_CTRL\_R5SS0\_CORE0\_ECC\_UNCORR\_ERRAGG\_STATUS\_RAW Register Field Descriptions**

| Bit  | Field                                                              | Type | Reset | Description                                                                                                                                                                                          |
|------|--------------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:5 | RESERVED                                                           | NONE | 0h    | Reserved                                                                                                                                                                                             |
| 4    | R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_DATA_UNCORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |
| 3    | R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_TAG_UNCORR_ERR  | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |
| 2    | R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_0TCM_UNCORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |

**Table 2-470. MSS\_CTRL\_R5SS0\_CORE0\_ECC\_UNCORR\_ERRAGG\_STATUS\_RAW Register Field Descriptions (continued)**

| Bit | Field                                                                | Type | Reset | Description                                                                                                                                                                                                |
|-----|----------------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_B1_TCM_UNCORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 0   | R5SS0_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU0_ATCM_UNCORR_ERR   | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |

### 2.2.2.157 MSS\_CTRL\_R5SS0\_CORE1\_ECC\_CORR\_ERRAGG\_MASK Register

#### 1 MSS\_CTRL\_R5SS0\_CORE1\_ECC\_CORR\_ERRAGG\_MASK Register (Offset = 180A0h) [reset = 0h]

Register to Mask Correctable error from R5SS0 CORE1 Memories.

Return to [Summary Table](#)

**Table 2-471. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 80A0h       |

**Figure 2-157. MSS\_CTRL\_R5SS0\_CORE1\_ECC\_CORR\_ERRAGG\_MASK Name Register**

| 31       | 30                                                        | 29                                                       | 28                                                        | 27                                                       | 26                                                        | 25                                                        | 24                                                       |
|----------|-----------------------------------------------------------|----------------------------------------------------------|-----------------------------------------------------------|----------------------------------------------------------|-----------------------------------------------------------|-----------------------------------------------------------|----------------------------------------------------------|
| RESERVED |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| NONE     |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| 0h       |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| 23       | 22                                                        | 21                                                       | 20                                                        | 19                                                       | 18                                                        | 17                                                        | 16                                                       |
| RESERVED |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| NONE     |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| 0h       |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| 15       | 14                                                        | 13                                                       | 12                                                        | 11                                                       | 10                                                        | 9                                                         | 8                                                        |
| RESERVED |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| NONE     |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| 0h       |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| 7        | 6                                                         | 5                                                        | 4                                                         | 3                                                        | 2                                                         | 1                                                         | 0                                                        |
| RESERVED | R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_IDATA_CORR_ERR | R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_ITAG_CORR_ERR | R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_DDATA_CORR_ERR | R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_DTAG_CORR_ERR | R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_B0TCM_CORR_ERR | R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_B1TCM_CORR_ERR | R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_ATCM_CORR_ERR |
| NONE     | R/W                                                       | R/W                                                      | R/W                                                       | R/W                                                      | R/W                                                       | R/W                                                       | R/W                                                      |
| 0h       | 0h                                                        | 0h                                                       | 0h                                                        | 0h                                                       | 0h                                                        | 0h                                                        | 0h                                                       |

**Table 2-473. MSS\_CTRL\_R5SS0\_CORE1\_ECC\_CORR\_ERRAGG\_MASK Register Field Descriptions**

| Bit  | Field                                                     | Type | Reset | Description                                                                                                                                      |
|------|-----------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED                                                  | NONE | 0h    | Reserved                                                                                                                                         |
| 6    | R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_IDATA_CORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 5    | R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_ITAG_CORR_ERR  | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 4    | R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_DDATA_CORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 3    | R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_DTAG_CORR_ERR  | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |

**Table 2-473. MSS\_CTRL\_R5SS0\_CORE1\_ECC\_CORR\_ERRAGG\_MASK Register Field Descriptions  
(continued)**

| Bit | Field                                                     | Type | Reset | Description                                                                                                                                      |
|-----|-----------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_B0TCM_CORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 1   | R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_B1TCM_CORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 0   | R5SS0_CPU1_ECC_CORR_ERRAGG_MASK_R5SS0_CPU1_ATCM_CORR_ERR  | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |

### 2.2.2.158 MSS\_CTRL\_R5SS0\_CORE1\_ECC\_CORR\_ERRAGG\_STATUS Register

#### 1 MSS\_CTRL\_R5SS0\_CORE1\_ECC\_CORR\_ERRAGG\_STATUS Register (Offset = 180A4h) [reset = 0h]

Status register based on mask for correctable error R5SS0 CORE1 Memories.

Return to [Summary Table](#)

**Table 2-474. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 80A4h       |

**Figure 2-158. MSS\_CTRL\_R5SS0\_CORE1\_ECC\_CORR\_ERRAGG\_STATUS Name Register**

| 31       | 30                                                          | 29                                                         | 28                                                          | 27                                                         | 26                                                          | 25                                                          | 24                                                         |
|----------|-------------------------------------------------------------|------------------------------------------------------------|-------------------------------------------------------------|------------------------------------------------------------|-------------------------------------------------------------|-------------------------------------------------------------|------------------------------------------------------------|
| RESERVED |                                                             |                                                            |                                                             |                                                            |                                                             |                                                             |                                                            |
| NONE     |                                                             |                                                            |                                                             |                                                            |                                                             |                                                             |                                                            |
| 0h       |                                                             |                                                            |                                                             |                                                            |                                                             |                                                             |                                                            |
| 23       | 22                                                          | 21                                                         | 20                                                          | 19                                                         | 18                                                          | 17                                                          | 16                                                         |
| RESERVED |                                                             |                                                            |                                                             |                                                            |                                                             |                                                             |                                                            |
| NONE     |                                                             |                                                            |                                                             |                                                            |                                                             |                                                             |                                                            |
| 0h       |                                                             |                                                            |                                                             |                                                            |                                                             |                                                             |                                                            |
| 15       | 14                                                          | 13                                                         | 12                                                          | 11                                                         | 10                                                          | 9                                                           | 8                                                          |
| RESERVED |                                                             |                                                            |                                                             |                                                            |                                                             |                                                             |                                                            |
| NONE     |                                                             |                                                            |                                                             |                                                            |                                                             |                                                             |                                                            |
| 0h       |                                                             |                                                            |                                                             |                                                            |                                                             |                                                             |                                                            |
| 7        | 6                                                           | 5                                                          | 4                                                           | 3                                                          | 2                                                           | 1                                                           | 0                                                          |
| RESERVED | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_IDATA_CORR_ERR | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_ITAG_CORR_ERR | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_DDATA_CORR_ERR | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_DTAG_CORR_ERR | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_B0TCM_CORR_ERR | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_B1TCM_CORR_ERR | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_ATCM_CORR_ERR |
| NONE     | R/W                                                         | R/W                                                        | R/W                                                         | R/W                                                        | R/W                                                         | R/W                                                         | R/W                                                        |
| 0h       | 0h                                                          | 0h                                                         | 0h                                                          | 0h                                                         | 0h                                                          | 0h                                                          | 0h                                                         |

**Table 2-476. MSS\_CTRL\_R5SS0\_CORE1\_ECC\_CORR\_ERRAGG\_STATUS Register Field Descriptions**

| Bit  | Field                                                       | Type | Reset | Description                                                                                                                                                                                          |
|------|-------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED                                                    | NONE | 0h    | Reserved                                                                                                                                                                                             |
| 6    | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_IDATA_CORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 5    | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_ITAG_CORR_ERR  | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 4    | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_DDATA_CORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 3    | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_DTAG_CORR_ERR  | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |

**Table 2-476. MSS\_CTRL\_R5SS0\_CORE1\_ECC\_CORR\_ERRAGG\_STATUS Register Field Descriptions  
(continued)**

| Bit | Field                                                       | Type | Reset | Description                                                                                                                                                                                          |
|-----|-------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_B0TCM_CORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 1   | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_B1TCM_CORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 0   | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS0_CPU1_ATCM_CORR_ERR  | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |



### 2.2.2.159 MSS\_CTRL\_R5SS0\_CORE1\_ECC\_CORR\_ERRAGG\_STATUS\_RAW Register

**1 MSS\_CTRL\_R5SS0\_CORE1\_ECC\_CORR\_ERRAGG\_STATUS\_RAW Register (Offset = 180A8h) [reset = 0h]**

Raw status for correctable error from R5SS0 CORE1 Memories.

Return to [Summary Table](#)

**Table 2-477. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 80A8h       |

**Figure 2-159. MSS\_CTRL\_R5SS0\_CORE1\_ECC\_CORR\_ERRAGG\_STATUS\_RAW Name Register**

| 31       | 30                                                              | 29                                                             | 28                                                              | 27                                                            | 26                                                               | 25                                                               | 24                                                              |
|----------|-----------------------------------------------------------------|----------------------------------------------------------------|-----------------------------------------------------------------|---------------------------------------------------------------|------------------------------------------------------------------|------------------------------------------------------------------|-----------------------------------------------------------------|
| RESERVED |                                                                 |                                                                |                                                                 |                                                               |                                                                  |                                                                  |                                                                 |
| NONE     |                                                                 |                                                                |                                                                 |                                                               |                                                                  |                                                                  |                                                                 |
| 0h       |                                                                 |                                                                |                                                                 |                                                               |                                                                  |                                                                  |                                                                 |
| 23       | 22                                                              | 21                                                             | 20                                                              | 19                                                            | 18                                                               | 17                                                               | 16                                                              |
| RESERVED |                                                                 |                                                                |                                                                 |                                                               |                                                                  |                                                                  |                                                                 |
| NONE     |                                                                 |                                                                |                                                                 |                                                               |                                                                  |                                                                  |                                                                 |
| 0h       |                                                                 |                                                                |                                                                 |                                                               |                                                                  |                                                                  |                                                                 |
| 15       | 14                                                              | 13                                                             | 12                                                              | 11                                                            | 10                                                               | 9                                                                | 8                                                               |
| RESERVED |                                                                 |                                                                |                                                                 |                                                               |                                                                  |                                                                  |                                                                 |
| NONE     |                                                                 |                                                                |                                                                 |                                                               |                                                                  |                                                                  |                                                                 |
| 0h       |                                                                 |                                                                |                                                                 |                                                               |                                                                  |                                                                  |                                                                 |
| 7        | 6                                                               | 5                                                              | 4                                                               | 3                                                             | 2                                                                | 1                                                                | 0                                                               |
| RESERVED | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_IDATA_CORR_ERR | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_ITAG_CORR_ERR | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_DDATA_CORR_ERR | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_DTA_CORR_ERR | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_B0T_CM_CORR_ERR | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_B1T_CM_CORR_ERR | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_ATC_M_CORR_ERR |
| NONE     | R/W                                                             | R/W                                                            | R/W                                                             | R/W                                                           | R/W                                                              | R/W                                                              | R/W                                                             |
| 0h       | 0h                                                              | 0h                                                             | 0h                                                              | 0h                                                            | 0h                                                               | 0h                                                               | 0h                                                              |

**Table 2-479. MSS\_CTRL\_R5SS0\_CORE1\_ECC\_CORR\_ERRAGG\_STATUS\_RAW Register Field Descriptions**

| Bit  | Field                                                           | Type | Reset | Description                                                                                                                                                                                        |
|------|-----------------------------------------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED                                                        | NONE | 0h    | Reserved                                                                                                                                                                                           |
| 6    | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_IDATA_CORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |
| 5    | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_ITAG_CORR_ERR  | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |
| 4    | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_DDATA_CORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |

**Table 2-479. MSS\_CTRL\_R5SS0\_CORE1\_ECC\_CORR\_ERRAGG\_STATUS\_RAW Register Field Descriptions (continued)**

| Bit | Field                                                           | Type | Reset | Description                                                                                                                                                                                              |
|-----|-----------------------------------------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3   | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_DTAG_CORR_ERR  | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 2   | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_B0TCM_CORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 1   | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_B1TCM_CORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 0   | R5SS0_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_ATCM_CORR_ERR  | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |

### 2.2.2.160 MSS\_CTRL\_R5SS0\_CORE1\_ECC\_UNCORR\_ERRAGG\_MASK Register

#### 1 MSS\_CTRL\_R5SS0\_CORE1\_ECC\_UNCORR\_ERRAGG\_MASK Register (Offset = 180B0h) [reset = 0h]

Register to Mask Uncorrectable error from R5SS0 CORE1 Memories.

Return to [Summary Table](#)

**Table 2-480. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 80B0h       |

**Figure 2-160. MSS\_CTRL\_R5SS0\_CORE1\_ECC\_UNCORR\_ERRAGG\_MASK Name Register**

|          |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
|----------|----|----|---------------------------------------------------------------|--------------------------------------------------------------|---------------------------------------------------------------|---------------------------------------------------------------|--------------------------------------------------------------|
| 31       | 30 | 29 | 28                                                            | 27                                                           | 26                                                            | 25                                                            | 24                                                           |
| RESERVED |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| NONE     |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| 0h       |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| 23       | 22 | 21 | 20                                                            | 19                                                           | 18                                                            | 17                                                            | 16                                                           |
| RESERVED |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| NONE     |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| 0h       |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| 15       | 14 | 13 | 12                                                            | 11                                                           | 10                                                            | 9                                                             | 8                                                            |
| RESERVED |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| NONE     |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| 0h       |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| 7        | 6  | 5  | 4                                                             | 3                                                            | 2                                                             | 1                                                             | 0                                                            |
| RESERVED |    |    | R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_DDATA_UNCORR_ERR | R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_DTAG_UNCORR_ERR | R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_B0TCM_UNCORR_ERR | R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_B1TCM_UNCORR_ERR | R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_ATCM_UNCORR_ERR |
| NONE     |    |    | R/W                                                           | R/W                                                          | R/W                                                           | R/W                                                           | R/W                                                          |
| 0h       |    |    | 0h                                                            | 0h                                                           | 0h                                                            | 0h                                                            | 0h                                                           |

**Table 2-482. MSS\_CTRL\_R5SS0\_CORE1\_ECC\_UNCORR\_ERRAGG\_MASK Register Field Descriptions**

| Bit  | Field                                                         | Type | Reset | Description                                                                                                                                      |
|------|---------------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:5 | RESERVED                                                      | NONE | 0h    | Reserved                                                                                                                                         |
| 4    | R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_DDATA_UNCORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 3    | R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_DTAG_UNCORR_ERR  | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 2    | R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_B0TCM_UNCORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 1    | R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_B1TCM_UNCORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |

**Table 2-482. MSS\_CTRL\_R5SS0\_CORE1\_ECC\_UNCORR\_ERRAGG\_MASK Register Field Descriptions  
(continued)**

| Bit | Field                                                        | Type | Reset | Description                                                                                                                                      |
|-----|--------------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | R5SS0_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS0_CPU1_ATCM_UNCORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |

### 2.2.2.161 MSS\_CTRL\_R5SS0\_CORE1\_ECC\_UNCORR\_ERRAGG\_STATUS Register

#### 1 MSS\_CTRL\_R5SS0\_CORE1\_ECC\_UNCORR\_ERRAGG\_STATUS Register (Offset = 180B4h) [reset = 0h]

Status register based on mask for uncorrectable error R5SS0 CORE1 Memories.

Return to [Summary Table](#)

**Table 2-483. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 80B4h       |

**Figure 2-161. MSS\_CTRL\_R5SS0\_CORE1\_ECC\_UNCORR\_ERRAGG\_STATUS Name Register**

|          |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
|----------|----|----|-----------------------------------------------------------------|----------------------------------------------------------------|-----------------------------------------------------------------|-----------------------------------------------------------------|----------------------------------------------------------------|
| 31       | 30 | 29 | 28                                                              | 27                                                             | 26                                                              | 25                                                              | 24                                                             |
| RESERVED |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| NONE     |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| 0h       |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| 23       | 22 | 21 | 20                                                              | 19                                                             | 18                                                              | 17                                                              | 16                                                             |
| RESERVED |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| NONE     |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| 0h       |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| 15       | 14 | 13 | 12                                                              | 11                                                             | 10                                                              | 9                                                               | 8                                                              |
| RESERVED |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| NONE     |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| 0h       |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| 7        | 6  | 5  | 4                                                               | 3                                                              | 2                                                               | 1                                                               | 0                                                              |
| RESERVED |    |    | R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_DDATA_UNCORR_ERR | R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_DTAG_UNCORR_ERR | R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_B0TCM_UNCORR_ERR | R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_B1TCM_UNCORR_ERR | R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_ATCM_UNCORR_ERR |
| NONE     |    |    | R/W                                                             | R/W                                                            | R/W                                                             | R/W                                                             | R/W                                                            |
| 0h       |    |    | 0h                                                              | 0h                                                             | 0h                                                              | 0h                                                              | 0h                                                             |

**Table 2-485. MSS\_CTRL\_R5SS0\_CORE1\_ECC\_UNCORR\_ERRAGG\_STATUS Register Field Descriptions**

| Bit  | Field                                                           | Type | Reset | Description                                                                                                                                                                                      |
|------|-----------------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:5 | RESERVED                                                        | NONE | 0h    | Reserved                                                                                                                                                                                         |
| 4    | R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_DDATA_UNCORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |
| 3    | R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_DTAG_UNCORR_ERR  | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |
| 2    | R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_B0TCM_UNCORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |
| 1    | R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_B1TCM_UNCORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |

**Table 2-485. MSS\_CTRL\_R5SS0\_CORE1\_ECC\_UNCORR\_ERRAGG\_STATUS Register Field Descriptions  
(continued)**

| Bit | Field                                                          | Type | Reset | Description                                                                                                                                                                                            |
|-----|----------------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS0_CPU1_ATCM_UNCORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |

### 2.2.2.162 MSS\_CTRL\_R5SS0\_CORE1\_ECC\_UNCORR\_ERRAGG\_STATUS\_RAW Register

**1 MSS\_CTRL\_R5SS0\_CORE1\_ECC\_UNCORR\_ERRAGG\_STATUS\_RAW Register (Offset = 180B8h) [reset = 0h]**

Raw status for uncorrectable error from R5SS0 CORE1 Memories.

Return to [Summary Table](#)

**Table 2-486. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 80B8h       |

**Figure 2-162. MSS\_CTRL\_R5SS0\_CORE1\_ECC\_UNCORR\_ERRAGG\_STATUS\_RAW Name Register**

| 31       | 30 | 29 | 28                                                                 | 27                                                                | 26                                                                 | 25                                                                 | 24                                                                  |
|----------|----|----|--------------------------------------------------------------------|-------------------------------------------------------------------|--------------------------------------------------------------------|--------------------------------------------------------------------|---------------------------------------------------------------------|
| RESERVED |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                     |
| NONE     |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                     |
| 0h       |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                     |
| 23       | 22 | 21 | 20                                                                 | 19                                                                | 18                                                                 | 17                                                                 | 16                                                                  |
| RESERVED |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                     |
| NONE     |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                     |
| 0h       |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                     |
| 15       | 14 | 13 | 12                                                                 | 11                                                                | 10                                                                 | 9                                                                  | 8                                                                   |
| RESERVED |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                     |
| NONE     |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                     |
| 0h       |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                     |
| 7        | 6  | 5  | 4                                                                  | 3                                                                 | 2                                                                  | 1                                                                  | 0                                                                   |
| RESERVED |    |    | R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_DATA_UNCORR_ERR | R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_TAG_UNCORR_ERR | R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_0TCM_UNCORR_ERR | R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_1TCM_UNCORR_ERR | R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_A_TCM_UNCORR_ERR |
| NONE     |    |    | R/W                                                                | R/W                                                               | R/W                                                                | R/W                                                                | R/W                                                                 |
| 0h       |    |    | 0h                                                                 | 0h                                                                | 0h                                                                 | 0h                                                                 | 0h                                                                  |

**Table 2-488. MSS\_CTRL\_R5SS0\_CORE1\_ECC\_UNCORR\_ERRAGG\_STATUS\_RAW Register Field Descriptions**

| Bit  | Field                                                              | Type | Reset | Description                                                                                                                                                                                          |
|------|--------------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:5 | RESERVED                                                           | NONE | 0h    | Reserved                                                                                                                                                                                             |
| 4    | R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_DATA_UNCORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |
| 3    | R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_TAG_UNCORR_ERR  | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |
| 2    | R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_0TCM_UNCORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |

**Table 2-488. MSS\_CTRL\_R5SS0\_CORE1\_ECC\_UNCORR\_ERRAGG\_STATUS\_RAW Register Field Descriptions (continued)**

| Bit | Field                                                                | Type | Reset | Description                                                                                                                                                                                                |
|-----|----------------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_B1_TCM_UNCORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 0   | R5SS0_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS0_CPU1_ATCM_UNCORR_ERR   | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |



### 2.2.2.163 MSS\_CTRL\_R5SS1\_CORE0\_ECC\_CORR\_ERRAGG\_MASK Register

#### 1 MSS\_CTRL\_R5SS1\_CORE0\_ECC\_CORR\_ERRAGG\_MASK Register (Offset = 180C0h) [reset = 0h]

Register to Mask Correctable error from R5SS1 CORE0 Memories.

Return to [Summary Table](#)

**Table 2-489. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 80C0h       |

**Figure 2-163. MSS\_CTRL\_R5SS1\_CORE0\_ECC\_CORR\_ERRAGG\_MASK Name Register**

| 31       | 30                                                        | 29                                                       | 28                                                        | 27                                                       | 26                                                        | 25                                                        | 24                                                       |
|----------|-----------------------------------------------------------|----------------------------------------------------------|-----------------------------------------------------------|----------------------------------------------------------|-----------------------------------------------------------|-----------------------------------------------------------|----------------------------------------------------------|
| RESERVED |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| NONE     |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| 0h       |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| 23       | 22                                                        | 21                                                       | 20                                                        | 19                                                       | 18                                                        | 17                                                        | 16                                                       |
| RESERVED |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| NONE     |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| 0h       |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| 15       | 14                                                        | 13                                                       | 12                                                        | 11                                                       | 10                                                        | 9                                                         | 8                                                        |
| RESERVED |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| NONE     |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| 0h       |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| 7        | 6                                                         | 5                                                        | 4                                                         | 3                                                        | 2                                                         | 1                                                         | 0                                                        |
| RESERVED | R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_IDATA_CORR_ERR | R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_ITAG_CORR_ERR | R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_DDATA_CORR_ERR | R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_DTAG_CORR_ERR | R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_B0TCM_CORR_ERR | R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_B1TCM_CORR_ERR | R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_ATCM_CORR_ERR |
| NONE     | R/W                                                       | R/W                                                      | R/W                                                       | R/W                                                      | R/W                                                       | R/W                                                       | R/W                                                      |
| 0h       | 0h                                                        | 0h                                                       | 0h                                                        | 0h                                                       | 0h                                                        | 0h                                                        | 0h                                                       |

**Table 2-491. MSS\_CTRL\_R5SS1\_CORE0\_ECC\_CORR\_ERRAGG\_MASK Register Field Descriptions**

| Bit  | Field                                                     | Type | Reset | Description                                                                                                                                      |
|------|-----------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED                                                  | NONE | 0h    | Reserved                                                                                                                                         |
| 6    | R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_IDATA_CORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 5    | R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_ITAG_CORR_ERR  | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 4    | R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_DDATA_CORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 3    | R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_DTAG_CORR_ERR  | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |

**Table 2-491. MSS\_CTRL\_R5SS1\_CORE0\_ECC\_CORR\_ERRAGG\_MASK Register Field Descriptions  
(continued)**

| Bit | Field                                                     | Type | Reset | Description                                                                                                                                      |
|-----|-----------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_B0TCM_CORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 1   | R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_B1TCM_CORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 0   | R5SS1_CPU0_ECC_CORR_ERRAGG_MASK_R5SS1_CPU0_ATCM_CORR_ERR  | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |

### 2.2.2.164 MSS\_CTRL\_R5SS1\_CORE0\_ECC\_CORR\_ERRAGG\_STATUS Register

#### 1 MSS\_CTRL\_R5SS1\_CORE0\_ECC\_CORR\_ERRAGG\_STATUS Register (Offset = 180C4h) [reset = 0h]

Status register based on mask for correctable error R5SS1 CORE0 Memories.

Return to [Summary Table](#)

**Table 2-492. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 80C4h       |

**Figure 2-164. MSS\_CTRL\_R5SS1\_CORE0\_ECC\_CORR\_ERRAGG\_STATUS Name Register**

| 31       | 30                                                          | 29                                                         | 28                                                          | 27                                                         | 26                                                          | 25                                                         | 24                                                         |
|----------|-------------------------------------------------------------|------------------------------------------------------------|-------------------------------------------------------------|------------------------------------------------------------|-------------------------------------------------------------|------------------------------------------------------------|------------------------------------------------------------|
| RESERVED |                                                             |                                                            |                                                             |                                                            |                                                             |                                                            |                                                            |
| NONE     |                                                             |                                                            |                                                             |                                                            |                                                             |                                                            |                                                            |
| 0h       |                                                             |                                                            |                                                             |                                                            |                                                             |                                                            |                                                            |
| 23       | 22                                                          | 21                                                         | 20                                                          | 19                                                         | 18                                                          | 17                                                         | 16                                                         |
| RESERVED |                                                             |                                                            |                                                             |                                                            |                                                             |                                                            |                                                            |
| NONE     |                                                             |                                                            |                                                             |                                                            |                                                             |                                                            |                                                            |
| 0h       |                                                             |                                                            |                                                             |                                                            |                                                             |                                                            |                                                            |
| 15       | 14                                                          | 13                                                         | 12                                                          | 11                                                         | 10                                                          | 9                                                          | 8                                                          |
| RESERVED |                                                             |                                                            |                                                             |                                                            |                                                             |                                                            |                                                            |
| NONE     |                                                             |                                                            |                                                             |                                                            |                                                             |                                                            |                                                            |
| 0h       |                                                             |                                                            |                                                             |                                                            |                                                             |                                                            |                                                            |
| 7        | 6                                                           | 5                                                          | 4                                                           | 3                                                          | 2                                                           | 1                                                          | 0                                                          |
| RESERVED | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_IDATA_CORR_ERR | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_ITAG_CORR_ERR | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_DDATA_CORR_ERR | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_DTAG_CORR_ERR | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_B1TCM_CORR_ERR | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_ATCM_CORR_ERR | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_ATCM_CORR_ERR |
| NONE     | R/W                                                         | R/W                                                        | R/W                                                         | R/W                                                        | R/W                                                         | R/W                                                        | R/W                                                        |
| 0h       | 0h                                                          | 0h                                                         | 0h                                                          | 0h                                                         | 0h                                                          | 0h                                                         | 0h                                                         |

**Table 2-494. MSS\_CTRL\_R5SS1\_CORE0\_ECC\_CORR\_ERRAGG\_STATUS Register Field Descriptions**

| Bit  | Field                                                       | Type | Reset | Description                                                                                                                                                                                          |
|------|-------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED                                                    | NONE | 0h    | Reserved                                                                                                                                                                                             |
| 6    | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_IDATA_CORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 5    | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_ITAG_CORR_ERR  | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 4    | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_DDATA_CORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 3    | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_DTAG_CORR_ERR  | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |

**Table 2-494. MSS\_CTRL\_R5SS1\_CORE0\_ECC\_CORR\_ERRAGG\_STATUS Register Field Descriptions  
(continued)**

| Bit | Field                                                       | Type | Reset | Description                                                                                                                                                                                          |
|-----|-------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_B0TCM_CORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 1   | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_B1TCM_CORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 0   | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU0_ATCM_CORR_ERR  | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |

### 2.2.2.165 MSS\_CTRL\_R5SS1\_CORE0\_ECC\_CORR\_ERRAGG\_STATUS\_RAW Register

**1 MSS\_CTRL\_R5SS1\_CORE0\_ECC\_CORR\_ERRAGG\_STATUS\_RAW Register (Offset = 180C8h) [reset = 0h]**

Raw status for correctable error from R5SS1 CORE0 Memories.

Return to [Summary Table](#)

**Table 2-495. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 80C8h       |

**Figure 2-165. MSS\_CTRL\_R5SS1\_CORE0\_ECC\_CORR\_ERRAGG\_STATUS\_RAW Name Register**

| 31       | 30                                                              | 29                                                             | 28                                                              | 27                                                              | 26                                                              | 25                                                              | 24                                                              |
|----------|-----------------------------------------------------------------|----------------------------------------------------------------|-----------------------------------------------------------------|-----------------------------------------------------------------|-----------------------------------------------------------------|-----------------------------------------------------------------|-----------------------------------------------------------------|
| RESERVED |                                                                 |                                                                |                                                                 |                                                                 |                                                                 |                                                                 |                                                                 |
| NONE     |                                                                 |                                                                |                                                                 |                                                                 |                                                                 |                                                                 |                                                                 |
| 0h       |                                                                 |                                                                |                                                                 |                                                                 |                                                                 |                                                                 |                                                                 |
| 23       | 22                                                              | 21                                                             | 20                                                              | 19                                                              | 18                                                              | 17                                                              | 16                                                              |
| RESERVED |                                                                 |                                                                |                                                                 |                                                                 |                                                                 |                                                                 |                                                                 |
| NONE     |                                                                 |                                                                |                                                                 |                                                                 |                                                                 |                                                                 |                                                                 |
| 0h       |                                                                 |                                                                |                                                                 |                                                                 |                                                                 |                                                                 |                                                                 |
| 15       | 14                                                              | 13                                                             | 12                                                              | 11                                                              | 10                                                              | 9                                                               | 8                                                               |
| RESERVED |                                                                 |                                                                |                                                                 |                                                                 |                                                                 |                                                                 |                                                                 |
| NONE     |                                                                 |                                                                |                                                                 |                                                                 |                                                                 |                                                                 |                                                                 |
| 0h       |                                                                 |                                                                |                                                                 |                                                                 |                                                                 |                                                                 |                                                                 |
| 7        | 6                                                               | 5                                                              | 4                                                               | 3                                                               | 2                                                               | 1                                                               | 0                                                               |
| RESERVED | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_IDATA_CORR_ERR | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_ITAG_CORR_ERR | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_DDATA_CORR_ERR | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_DDATA_CORR_ERR | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_DDATA_CORR_ERR | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_DDATA_CORR_ERR | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_DDATA_CORR_ERR |
| NONE     | R/W                                                             | R/W                                                            | R/W                                                             | R/W                                                             | R/W                                                             | R/W                                                             | R/W                                                             |
| 0h       | 0h                                                              | 0h                                                             | 0h                                                              | 0h                                                              | 0h                                                              | 0h                                                              | 0h                                                              |

**Table 2-497. MSS\_CTRL\_R5SS1\_CORE0\_ECC\_CORR\_ERRAGG\_STATUS\_RAW Register Field Descriptions**

| Bit  | Field                                                           | Type | Reset | Description                                                                                                                                                                                        |
|------|-----------------------------------------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED                                                        | NONE | 0h    | Reserved                                                                                                                                                                                           |
| 6    | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_IDATA_CORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |
| 5    | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_ITAG_CORR_ERR  | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |
| 4    | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_DDATA_CORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |

**Table 2-497. MSS\_CTRL\_R5SS1\_CORE0\_ECC\_CORR\_ERRAGG\_STATUS\_RAW Register Field Descriptions (continued)**

| Bit | Field                                                           | Type | Reset | Description                                                                                                                                                                                              |
|-----|-----------------------------------------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3   | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_DTAG_CORR_ERR  | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 2   | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_B0TCM_CORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 1   | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_B1TCM_CORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 0   | R5SS1_CPU0_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_ATCM_CORR_ERR  | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |

### 2.2.2.166 MSS\_CTRL\_R5SS1\_CORE0\_ECC\_UNCORR\_ERRAGG\_MASK Register

#### 1 MSS\_CTRL\_R5SS1\_CORE0\_ECC\_UNCORR\_ERRAGG\_MASK Register (Offset = 180D0h) [reset = 0h]

Register to Mask Uncorrectable error from R5SS1 CORE0 Memories.

Return to [Summary Table](#)

**Table 2-498. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 80D0h       |

**Figure 2-166. MSS\_CTRL\_R5SS1\_CORE0\_ECC\_UNCORR\_ERRAGG\_MASK Name Register**

|          |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
|----------|----|----|---------------------------------------------------------------|--------------------------------------------------------------|---------------------------------------------------------------|---------------------------------------------------------------|--------------------------------------------------------------|
| 31       | 30 | 29 | 28                                                            | 27                                                           | 26                                                            | 25                                                            | 24                                                           |
| RESERVED |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| NONE     |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| 0h       |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| 23       | 22 | 21 | 20                                                            | 19                                                           | 18                                                            | 17                                                            | 16                                                           |
| RESERVED |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| NONE     |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| 0h       |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| 15       | 14 | 13 | 12                                                            | 11                                                           | 10                                                            | 9                                                             | 8                                                            |
| RESERVED |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| NONE     |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| 0h       |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| 7        | 6  | 5  | 4                                                             | 3                                                            | 2                                                             | 1                                                             | 0                                                            |
| RESERVED |    |    | R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_DDATA_UNCORR_ERR | R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_DTAG_UNCORR_ERR | R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_B0TCM_UNCORR_ERR | R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_B1TCM_UNCORR_ERR | R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_ATCM_UNCORR_ERR |
| NONE     |    |    | R/W                                                           | R/W                                                          | R/W                                                           | R/W                                                           | R/W                                                          |
| 0h       |    |    | 0h                                                            | 0h                                                           | 0h                                                            | 0h                                                            | 0h                                                           |

**Table 2-500. MSS\_CTRL\_R5SS1\_CORE0\_ECC\_UNCORR\_ERRAGG\_MASK Register Field Descriptions**

| Bit  | Field                                                         | Type | Reset | Description                                                                                                                                      |
|------|---------------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:5 | RESERVED                                                      | NONE | 0h    | Reserved                                                                                                                                         |
| 4    | R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_DDATA_UNCORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 3    | R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_DTAG_UNCORR_ERR  | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 2    | R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_B0TCM_UNCORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 1    | R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_B1TCM_UNCORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |

**Table 2-500. MSS\_CTRL\_R5SS1\_CORE0\_ECC\_UNCORR\_ERRAGG\_MASK Register Field Descriptions  
(continued)**

| Bit | Field                                                        | Type | Reset | Description                                                                                                                                      |
|-----|--------------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | R5SS1_CPU0_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU0_ATCM_UNCORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |



### 2.2.2.167 MSS\_CTRL\_R5SS1\_CORE0\_ECC\_UNCORR\_ERRAGG\_STATUS Register

#### 1 MSS\_CTRL\_R5SS1\_CORE0\_ECC\_UNCORR\_ERRAGG\_STATUS Register (Offset = 180D4h) [reset = 0h]

Status register based on mask for uncorrectable error R5SS1 CORE0 Memories.

Return to [Summary Table](#)

**Table 2-501. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 80D4h       |

**Figure 2-167. MSS\_CTRL\_R5SS1\_CORE0\_ECC\_UNCORR\_ERRAGG\_STATUS Name Register**

|          |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
|----------|----|----|-----------------------------------------------------------------|----------------------------------------------------------------|-----------------------------------------------------------------|-----------------------------------------------------------------|----------------------------------------------------------------|
| 31       | 30 | 29 | 28                                                              | 27                                                             | 26                                                              | 25                                                              | 24                                                             |
| RESERVED |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| NONE     |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| 0h       |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| 23       | 22 | 21 | 20                                                              | 19                                                             | 18                                                              | 17                                                              | 16                                                             |
| RESERVED |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| NONE     |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| 0h       |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| 15       | 14 | 13 | 12                                                              | 11                                                             | 10                                                              | 9                                                               | 8                                                              |
| RESERVED |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| NONE     |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| 0h       |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| 7        | 6  | 5  | 4                                                               | 3                                                              | 2                                                               | 1                                                               | 0                                                              |
| RESERVED |    |    | R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_DDATA_UNCORR_ERR | R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_DTAG_UNCORR_ERR | R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_B0TCM_UNCORR_ERR | R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_B1TCM_UNCORR_ERR | R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_ATCM_UNCORR_ERR |
| NONE     |    |    | R/W                                                             | R/W                                                            | R/W                                                             | R/W                                                             | R/W                                                            |
| 0h       |    |    | 0h                                                              | 0h                                                             | 0h                                                              | 0h                                                              | 0h                                                             |

**Table 2-503. MSS\_CTRL\_R5SS1\_CORE0\_ECC\_UNCORR\_ERRAGG\_STATUS Register Field Descriptions**

| Bit  | Field                                                           | Type | Reset | Description                                                                                                                                                                                            |
|------|-----------------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:5 | RESERVED                                                        | NONE | 0h    | Reserved                                                                                                                                                                                               |
| 4    | R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_DDATA_UNCORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 3    | R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_DTAG_UNCORR_ERR  | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 2    | R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_B0TCM_UNCORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 1    | R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_B1TCM_UNCORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |

**Table 2-503. MSS\_CTRL\_R5SS1\_CORE0\_ECC\_UNCORR\_ERRAGG\_STATUS Register Field Descriptions  
(continued)**

| Bit | Field                                                          | Type | Reset | Description                                                                                                                                                                                            |
|-----|----------------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU0_ATCM_UNCORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |

### 2.2.2.168 MSS\_CTRL\_R5SS1\_CORE0\_ECC\_UNCORR\_ERRAGG\_STATUS\_RAW Register

**1 MSS\_CTRL\_R5SS1\_CORE0\_ECC\_UNCORR\_ERRAGG\_STATUS\_RAW Register (Offset = 180D8h) [reset = 0h]**

Raw status for uncorrectable error from R5SS1 CORE0 Memories.

Return to [Summary Table](#)

**Table 2-504. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 80D8h       |

**Figure 2-168. MSS\_CTRL\_R5SS1\_CORE0\_ECC\_UNCORR\_ERRAGG\_STATUS\_RAW Name Register**

| 31       | 30 | 29 | 28                                                                 | 27                                                                | 26                                                                 | 25                                                                 | 24                                                                  |
|----------|----|----|--------------------------------------------------------------------|-------------------------------------------------------------------|--------------------------------------------------------------------|--------------------------------------------------------------------|---------------------------------------------------------------------|
| RESERVED |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                     |
| NONE     |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                     |
| 0h       |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                     |
| 23       | 22 | 21 | 20                                                                 | 19                                                                | 18                                                                 | 17                                                                 | 16                                                                  |
| RESERVED |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                     |
| NONE     |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                     |
| 0h       |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                     |
| 15       | 14 | 13 | 12                                                                 | 11                                                                | 10                                                                 | 9                                                                  | 8                                                                   |
| RESERVED |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                     |
| NONE     |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                     |
| 0h       |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                     |
| 7        | 6  | 5  | 4                                                                  | 3                                                                 | 2                                                                  | 1                                                                  | 0                                                                   |
| RESERVED |    |    | R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_DATA_UNCORR_ERR | R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_TAG_UNCORR_ERR | R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_0TCM_UNCORR_ERR | R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_1TCM_UNCORR_ERR | R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_A_TCM_UNCORR_ERR |
| NONE     |    |    | R/W                                                                | R/W                                                               | R/W                                                                | R/W                                                                | R/W                                                                 |
| 0h       |    |    | 0h                                                                 | 0h                                                                | 0h                                                                 | 0h                                                                 | 0h                                                                  |

**Table 2-506. MSS\_CTRL\_R5SS1\_CORE0\_ECC\_UNCORR\_ERRAGG\_STATUS\_RAW Register Field Descriptions**

| Bit  | Field                                                              | Type | Reset | Description                                                                                                                                                                                          |
|------|--------------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:5 | RESERVED                                                           | NONE | 0h    | Reserved                                                                                                                                                                                             |
| 4    | R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_DATA_UNCORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |
| 3    | R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_TAG_UNCORR_ERR  | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |
| 2    | R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_0TCM_UNCORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |

**Table 2-506. MSS\_CTRL\_R5SS1\_CORE0\_ECC\_UNCORR\_ERRAGG\_STATUS\_RAW Register Field Descriptions (continued)**

| Bit | Field                                                                | Type | Reset | Description                                                                                                                                                                                                |
|-----|----------------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_B1_TCM_UNCORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 0   | R5SS1_CPU0_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU0_ATCM_UNCORR_ERR   | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |

### 2.2.2.169 MSS\_CTRL\_R5SS1\_CORE1\_ECC\_CORR\_ERRAGG\_MASK Register

#### 1 MSS\_CTRL\_R5SS1\_CORE1\_ECC\_CORR\_ERRAGG\_MASK Register (Offset = 180E0h) [reset = 0h]

Register to Mask Correctable error from R5SS1 CORE1 Memories.

Return to [Summary Table](#)

**Table 2-507. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 80E0h       |

**Figure 2-169. MSS\_CTRL\_R5SS1\_CORE1\_ECC\_CORR\_ERRAGG\_MASK Name Register**

| 31       | 30                                                        | 29                                                       | 28                                                        | 27                                                       | 26                                                        | 25                                                        | 24                                                       |
|----------|-----------------------------------------------------------|----------------------------------------------------------|-----------------------------------------------------------|----------------------------------------------------------|-----------------------------------------------------------|-----------------------------------------------------------|----------------------------------------------------------|
| RESERVED |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| NONE     |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| 0h       |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| 23       | 22                                                        | 21                                                       | 20                                                        | 19                                                       | 18                                                        | 17                                                        | 16                                                       |
| RESERVED |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| NONE     |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| 0h       |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| 15       | 14                                                        | 13                                                       | 12                                                        | 11                                                       | 10                                                        | 9                                                         | 8                                                        |
| RESERVED |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| NONE     |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| 0h       |                                                           |                                                          |                                                           |                                                          |                                                           |                                                           |                                                          |
| 7        | 6                                                         | 5                                                        | 4                                                         | 3                                                        | 2                                                         | 1                                                         | 0                                                        |
| RESERVED | R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_IDATA_CORR_ERR | R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_ITAG_CORR_ERR | R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_DDATA_CORR_ERR | R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_DTAG_CORR_ERR | R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_B0TCM_CORR_ERR | R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_B1TCM_CORR_ERR | R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_ATCM_CORR_ERR |
| NONE     | R/W                                                       | R/W                                                      | R/W                                                       | R/W                                                      | R/W                                                       | R/W                                                       | R/W                                                      |
| 0h       | 0h                                                        | 0h                                                       | 0h                                                        | 0h                                                       | 0h                                                        | 0h                                                        | 0h                                                       |

**Table 2-509. MSS\_CTRL\_R5SS1\_CORE1\_ECC\_CORR\_ERRAGG\_MASK Register Field Descriptions**

| Bit  | Field                                                     | Type | Reset | Description                                                                                                                                      |
|------|-----------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED                                                  | NONE | 0h    | Reserved                                                                                                                                         |
| 6    | R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_IDATA_CORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 5    | R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_ITAG_CORR_ERR  | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 4    | R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_DDATA_CORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 3    | R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_DTAG_CORR_ERR  | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |

**Table 2-509. MSS\_CTRL\_R5SS1\_CORE1\_ECC\_CORR\_ERRAGG\_MASK Register Field Descriptions  
(continued)**

| Bit | Field                                                     | Type | Reset | Description                                                                                                                                      |
|-----|-----------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_B0TCM_CORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 1   | R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_B1TCM_CORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 0   | R5SS1_CPU1_ECC_CORR_ERRAGG_MASK_R5SS1_CPU1_ATCM_CORR_ERR  | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |

### 2.2.2.170 MSS\_CTRL\_R5SS1\_CORE1\_ECC\_CORR\_ERRAGG\_STATUS Register

#### 1 MSS\_CTRL\_R5SS1\_CORE1\_ECC\_CORR\_ERRAGG\_STATUS Register (Offset = 180E4h) [reset = 0h]

Status register based on mask for correctable error R5SS1 CORE1 Memories.

Return to [Summary Table](#)

**Table 2-510. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 80E4h       |

**Figure 2-170. MSS\_CTRL\_R5SS1\_CORE1\_ECC\_CORR\_ERRAGG\_STATUS Name Register**

| 31       | 30                                                          | 29                                                         | 28                                                          | 27                                                         | 26                                                          | 25                                                         | 24                                                         |
|----------|-------------------------------------------------------------|------------------------------------------------------------|-------------------------------------------------------------|------------------------------------------------------------|-------------------------------------------------------------|------------------------------------------------------------|------------------------------------------------------------|
| RESERVED |                                                             |                                                            |                                                             |                                                            |                                                             |                                                            |                                                            |
| NONE     |                                                             |                                                            |                                                             |                                                            |                                                             |                                                            |                                                            |
| 0h       |                                                             |                                                            |                                                             |                                                            |                                                             |                                                            |                                                            |
| 23       | 22                                                          | 21                                                         | 20                                                          | 19                                                         | 18                                                          | 17                                                         | 16                                                         |
| RESERVED |                                                             |                                                            |                                                             |                                                            |                                                             |                                                            |                                                            |
| NONE     |                                                             |                                                            |                                                             |                                                            |                                                             |                                                            |                                                            |
| 0h       |                                                             |                                                            |                                                             |                                                            |                                                             |                                                            |                                                            |
| 15       | 14                                                          | 13                                                         | 12                                                          | 11                                                         | 10                                                          | 9                                                          | 8                                                          |
| RESERVED |                                                             |                                                            |                                                             |                                                            |                                                             |                                                            |                                                            |
| NONE     |                                                             |                                                            |                                                             |                                                            |                                                             |                                                            |                                                            |
| 0h       |                                                             |                                                            |                                                             |                                                            |                                                             |                                                            |                                                            |
| 7        | 6                                                           | 5                                                          | 4                                                           | 3                                                          | 2                                                           | 1                                                          | 0                                                          |
| RESERVED | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_IDATA_CORR_ERR | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_ITAG_CORR_ERR | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_DDATA_CORR_ERR | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_DTAG_CORR_ERR | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_B1TCM_CORR_ERR | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_ATCM_CORR_ERR | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_ATCM_CORR_ERR |
| NONE     | R/W                                                         | R/W                                                        | R/W                                                         | R/W                                                        | R/W                                                         | R/W                                                        | R/W                                                        |
| 0h       | 0h                                                          | 0h                                                         | 0h                                                          | 0h                                                         | 0h                                                          | 0h                                                         | 0h                                                         |

**Table 2-512. MSS\_CTRL\_R5SS1\_CORE1\_ECC\_CORR\_ERRAGG\_STATUS Register Field Descriptions**

| Bit  | Field                                                       | Type | Reset | Description                                                                                                                                                                                          |
|------|-------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED                                                    | NONE | 0h    | Reserved                                                                                                                                                                                             |
| 6    | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_IDATA_CORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 5    | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_ITAG_CORR_ERR  | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 4    | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_DDATA_CORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 3    | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_DTAG_CORR_ERR  | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |

**Table 2-512. MSS\_CTRL\_R5SS1\_CORE1\_ECC\_CORR\_ERRAGG\_STATUS Register Field Descriptions  
(continued)**

| Bit | Field                                                       | Type | Reset | Description                                                                                                                                                                                          |
|-----|-------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_B0TCM_CORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 1   | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_B1TCM_CORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 0   | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_R5SS1_CPU1_ATCM_CORR_ERR  | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |



### 2.2.2.171 MSS\_CTRL\_R5SS1\_CORE1\_ECC\_CORR\_ERRAGG\_STATUS\_RAW Register

**1 MSS\_CTRL\_R5SS1\_CORE1\_ECC\_CORR\_ERRAGG\_STATUS\_RAW Register (Offset = 180E8h) [reset = 0h]**

Raw status for correctable error from R5SS1 CORE1 Memories.

Return to [Summary Table](#)

**Table 2-513. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 80E8h       |

**Figure 2-171. MSS\_CTRL\_R5SS1\_CORE1\_ECC\_CORR\_ERRAGG\_STATUS\_RAW Name Register**

| 31       | 30                                                              | 29                                                             | 28                                                              | 27                                                              | 26                                                              | 25                                                              | 24                                                              |
|----------|-----------------------------------------------------------------|----------------------------------------------------------------|-----------------------------------------------------------------|-----------------------------------------------------------------|-----------------------------------------------------------------|-----------------------------------------------------------------|-----------------------------------------------------------------|
| RESERVED |                                                                 |                                                                |                                                                 |                                                                 |                                                                 |                                                                 |                                                                 |
| NONE     |                                                                 |                                                                |                                                                 |                                                                 |                                                                 |                                                                 |                                                                 |
| 0h       |                                                                 |                                                                |                                                                 |                                                                 |                                                                 |                                                                 |                                                                 |
| 23       | 22                                                              | 21                                                             | 20                                                              | 19                                                              | 18                                                              | 17                                                              | 16                                                              |
| RESERVED |                                                                 |                                                                |                                                                 |                                                                 |                                                                 |                                                                 |                                                                 |
| NONE     |                                                                 |                                                                |                                                                 |                                                                 |                                                                 |                                                                 |                                                                 |
| 0h       |                                                                 |                                                                |                                                                 |                                                                 |                                                                 |                                                                 |                                                                 |
| 15       | 14                                                              | 13                                                             | 12                                                              | 11                                                              | 10                                                              | 9                                                               | 8                                                               |
| RESERVED |                                                                 |                                                                |                                                                 |                                                                 |                                                                 |                                                                 |                                                                 |
| NONE     |                                                                 |                                                                |                                                                 |                                                                 |                                                                 |                                                                 |                                                                 |
| 0h       |                                                                 |                                                                |                                                                 |                                                                 |                                                                 |                                                                 |                                                                 |
| 7        | 6                                                               | 5                                                              | 4                                                               | 3                                                               | 2                                                               | 1                                                               | 0                                                               |
| RESERVED | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_IDATA_CORR_ERR | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_ITAG_CORR_ERR | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_DDATA_CORR_ERR | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_DDATA_CORR_ERR | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_DDATA_CORR_ERR | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_DDATA_CORR_ERR | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_DDATA_CORR_ERR |
| NONE     | R/W                                                             | R/W                                                            | R/W                                                             | R/W                                                             | R/W                                                             | R/W                                                             | R/W                                                             |
| 0h       | 0h                                                              | 0h                                                             | 0h                                                              | 0h                                                              | 0h                                                              | 0h                                                              | 0h                                                              |

**Table 2-515. MSS\_CTRL\_R5SS1\_CORE1\_ECC\_CORR\_ERRAGG\_STATUS\_RAW Register Field Descriptions**

| Bit  | Field                                                           | Type | Reset | Description                                                                                                                                                                                        |
|------|-----------------------------------------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED                                                        | NONE | 0h    | Reserved                                                                                                                                                                                           |
| 6    | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_IDATA_CORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |
| 5    | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_ITAG_CORR_ERR  | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |
| 4    | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_DDATA_CORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |

**Table 2-515. MSS\_CTRL\_R5SS1\_CORE1\_ECC\_CORR\_ERRAGG\_STATUS\_RAW Register Field Descriptions (continued)**

| Bit | Field                                                           | Type | Reset | Description                                                                                                                                                                                              |
|-----|-----------------------------------------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3   | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_DTAG_CORR_ERR  | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 2   | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_B0TCM_CORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 1   | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_B1TCM_CORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 0   | R5SS1_CPU1_ECC_CORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_ATCM_CORR_ERR  | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_CORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |

### 2.2.2.172 MSS\_CTRL\_R5SS1\_CORE1\_ECC\_UNCORR\_ERRAGG\_MASK Register

#### 1 MSS\_CTRL\_R5SS1\_CORE1\_ECC\_UNCORR\_ERRAGG\_MASK Register (Offset = 180F0h) [reset = 0h]

Register to Mask Uncorrectable error from R5SS1 CORE1 Memories.

Return to [Summary Table](#)

**Table 2-516. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 80F0h       |

**Figure 2-172. MSS\_CTRL\_R5SS1\_CORE1\_ECC\_UNCORR\_ERRAGG\_MASK Name Register**

|          |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
|----------|----|----|---------------------------------------------------------------|--------------------------------------------------------------|---------------------------------------------------------------|---------------------------------------------------------------|--------------------------------------------------------------|
| 31       | 30 | 29 | 28                                                            | 27                                                           | 26                                                            | 25                                                            | 24                                                           |
| RESERVED |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| NONE     |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| 0h       |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| 23       | 22 | 21 | 20                                                            | 19                                                           | 18                                                            | 17                                                            | 16                                                           |
| RESERVED |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| NONE     |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| 0h       |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| 15       | 14 | 13 | 12                                                            | 11                                                           | 10                                                            | 9                                                             | 8                                                            |
| RESERVED |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| NONE     |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| 0h       |    |    |                                                               |                                                              |                                                               |                                                               |                                                              |
| 7        | 6  | 5  | 4                                                             | 3                                                            | 2                                                             | 1                                                             | 0                                                            |
| RESERVED |    |    | R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_DDATA_UNCORR_ERR | R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_DTAG_UNCORR_ERR | R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_B0TCM_UNCORR_ERR | R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_B1TCM_UNCORR_ERR | R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_ATCM_UNCORR_ERR |
| NONE     |    |    | R/W                                                           | R/W                                                          | R/W                                                           | R/W                                                           | R/W                                                          |
| 0h       |    |    | 0h                                                            | 0h                                                           | 0h                                                            | 0h                                                            | 0h                                                           |

**Table 2-518. MSS\_CTRL\_R5SS1\_CORE1\_ECC\_UNCORR\_ERRAGG\_MASK Register Field Descriptions**

| Bit  | Field                                                         | Type | Reset | Description                                                                                                                                      |
|------|---------------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:5 | RESERVED                                                      | NONE | 0h    | Reserved                                                                                                                                         |
| 4    | R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_DDATA_UNCORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 3    | R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_DTAG_UNCORR_ERR  | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 2    | R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_B0TCM_UNCORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 1    | R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_B1TCM_UNCORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |

**Table 2-518. MSS\_CTRL\_R5SS1\_CORE1\_ECC\_UNCORR\_ERRAGG\_MASK Register Field Descriptions  
(continued)**

| Bit | Field                                                        | Type | Reset | Description                                                                                                                                      |
|-----|--------------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | R5SS1_CPU1_ECC_UNCORR_ERRAGG_MASK_R5SS1_CPU1_ATCM_UNCORR_ERR | R/W  | 0h    | Mask Interrupt for correctable errors to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |

### 2.2.2.173 MSS\_CTRL\_R5SS1\_CORE1\_ECC\_UNCORR\_ERRAGG\_STATUS Register

#### 1 MSS\_CTRL\_R5SS1\_CORE1\_ECC\_UNCORR\_ERRAGG\_STATUS Register (Offset = 180F4h) [reset = 0h]

Status register based on mask for uncorrectable error R5SS1 CORE1 Memories.

Return to [Summary Table](#)

**Table 2-519. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 80F4h       |

**Figure 2-173. MSS\_CTRL\_R5SS1\_CORE1\_ECC\_UNCORR\_ERRAGG\_STATUS Name Register**

| 31       | 30 | 29 | 28                                                              | 27                                                             | 26                                                              | 25                                                              | 24                                                             |
|----------|----|----|-----------------------------------------------------------------|----------------------------------------------------------------|-----------------------------------------------------------------|-----------------------------------------------------------------|----------------------------------------------------------------|
| RESERVED |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| NONE     |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| 0h       |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| 23       | 22 | 21 | 20                                                              | 19                                                             | 18                                                              | 17                                                              | 16                                                             |
| RESERVED |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| NONE     |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| 0h       |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| 15       | 14 | 13 | 12                                                              | 11                                                             | 10                                                              | 9                                                               | 8                                                              |
| RESERVED |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| NONE     |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| 0h       |    |    |                                                                 |                                                                |                                                                 |                                                                 |                                                                |
| 7        | 6  | 5  | 4                                                               | 3                                                              | 2                                                               | 1                                                               | 0                                                              |
| RESERVED |    |    | R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_DDATA_UNCORR_ERR | R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_DTAG_UNCORR_ERR | R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_B0TCM_UNCORR_ERR | R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_B1TCM_UNCORR_ERR | R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_ATCM_UNCORR_ERR |
| NONE     |    |    | R/W                                                             | R/W                                                            | R/W                                                             | R/W                                                             | R/W                                                            |
| 0h       |    |    | 0h                                                              | 0h                                                             | 0h                                                              | 0h                                                              | 0h                                                             |

**Table 2-521. MSS\_CTRL\_R5SS1\_CORE1\_ECC\_UNCORR\_ERRAGG\_STATUS Register Field Descriptions**

| Bit  | Field                                                           | Type | Reset | Description                                                                                                                                                                                            |
|------|-----------------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:5 | RESERVED                                                        | NONE | 0h    | Reserved                                                                                                                                                                                               |
| 4    | R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_DDATA_UNCORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 3    | R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_DTAG_UNCORR_ERR  | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 2    | R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_B0TCM_UNCORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 1    | R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_B1TCM_UNCORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |

**Table 2-521. MSS\_CTRL\_R5SS1\_CORE1\_ECC\_UNCORR\_ERRAGG\_STATUS Register Field Descriptions  
(continued)**

| Bit | Field                                                          | Type | Reset | Description                                                                                                                                                                                            |
|-----|----------------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_R5SS1_CPU1_ATCM_UNCORR_ERR | R/W  | 0h    | Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |

### 2.2.2.174 MSS\_CTRL\_R5SS1\_CORE1\_ECC\_UNCORR\_ERRAGG\_STATUS\_RAW Register

**1 MSS\_CTRL\_R5SS1\_CORE1\_ECC\_UNCORR\_ERRAGG\_STATUS\_RAW Register (Offset = 180F8h) [reset = 0h]**

Raw status for uncorrectable error from R5SS1 CORE1 Memories.

Return to [Summary Table](#)

**Table 2-522. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 80F8h       |

**Figure 2-174. MSS\_CTRL\_R5SS1\_CORE1\_ECC\_UNCORR\_ERRAGG\_STATUS\_RAW Name Register**

| 31       | 30 | 29 | 28                                                                 | 27                                                                | 26                                                                 | 25                                                                 | 24                                                                  |
|----------|----|----|--------------------------------------------------------------------|-------------------------------------------------------------------|--------------------------------------------------------------------|--------------------------------------------------------------------|---------------------------------------------------------------------|
| RESERVED |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                     |
| NONE     |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                     |
| 0h       |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                     |
| 23       | 22 | 21 | 20                                                                 | 19                                                                | 18                                                                 | 17                                                                 | 16                                                                  |
| RESERVED |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                     |
| NONE     |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                     |
| 0h       |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                     |
| 15       | 14 | 13 | 12                                                                 | 11                                                                | 10                                                                 | 9                                                                  | 8                                                                   |
| RESERVED |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                     |
| NONE     |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                     |
| 0h       |    |    |                                                                    |                                                                   |                                                                    |                                                                    |                                                                     |
| 7        | 6  | 5  | 4                                                                  | 3                                                                 | 2                                                                  | 1                                                                  | 0                                                                   |
| RESERVED |    |    | R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_DATA_UNCORR_ERR | R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_TAG_UNCORR_ERR | R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_0TCM_UNCORR_ERR | R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_1TCM_UNCORR_ERR | R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_A_TCM_UNCORR_ERR |
| NONE     |    |    | R/W                                                                | R/W                                                               | R/W                                                                | R/W                                                                | R/W                                                                 |
| 0h       |    |    | 0h                                                                 | 0h                                                                | 0h                                                                 | 0h                                                                 | 0h                                                                  |

**Table 2-524. MSS\_CTRL\_R5SS1\_CORE1\_ECC\_UNCORR\_ERRAGG\_STATUS\_RAW Register Field Descriptions**

| Bit  | Field                                                              | Type | Reset | Description                                                                                                                                                                                          |
|------|--------------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:5 | RESERVED                                                           | NONE | 0h    | Reserved                                                                                                                                                                                             |
| 4    | R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_DATA_UNCORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |
| 3    | R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_TAG_UNCORR_ERR  | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |
| 2    | R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_0TCM_UNCORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register Write 0x1 to clear this interrupt. |

**Table 2-524. MSS\_CTRL\_R5SS1\_CORE1\_ECC\_UNCORR\_ERRAGG\_STATUS\_RAW Register Field Descriptions (continued)**

| Bit | Field                                                                | Type | Reset | Description                                                                                                                                                                                                |
|-----|----------------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_B1_TCM_UNCORR_ERR | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 0   | R5SS1_CPU1_ECC_UNCORR_ERRAGG_STATUS_RAW_R5SS1_CPU1_ATCM_UNCORR_ERR   | R/W  | 0h    | Raw Status of Interrupt from correctable error of corresponding CPU<br>Set only if Interrupt is unmasked in corresponding R5SS*_CPU*_ECC_UNCORR_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |



### 2.2.2.175 MSS\_CTRL\_R5SS0\_CORE0\_TCM\_ADDRPARITY\_ERRAGG\_MASK Register

**1 MSS\_CTRL\_R5SS0\_CORE0\_TCM\_ADDRPARITY\_ERRAGG\_MASK Register (Offset = 18100h) [reset = 0h]**

Register to Mask TCM address parity errors from R5SS0 CORE0.

Return to [Summary Table](#)

**Table 2-525. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8100h       |

**Figure 2-175. MSS\_CTRL\_R5SS0\_CORE0\_TCM\_ADDRPARITY\_ERRAGG\_MASK Name Register**

|          |    |    |    |    |                                                                    |                                                                    |                                                                   |
|----------|----|----|----|----|--------------------------------------------------------------------|--------------------------------------------------------------------|-------------------------------------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26                                                                 | 25                                                                 | 24                                                                |
| RESERVED |    |    |    |    |                                                                    |                                                                    |                                                                   |
| NONE     |    |    |    |    |                                                                    |                                                                    |                                                                   |
| 0h       |    |    |    |    |                                                                    |                                                                    |                                                                   |
| 23       | 22 | 21 | 20 | 19 | 18                                                                 | 17                                                                 | 16                                                                |
| RESERVED |    |    |    |    |                                                                    |                                                                    |                                                                   |
| NONE     |    |    |    |    |                                                                    |                                                                    |                                                                   |
| 0h       |    |    |    |    |                                                                    |                                                                    |                                                                   |
| 15       | 14 | 13 | 12 | 11 | 10                                                                 | 9                                                                  | 8                                                                 |
| RESERVED |    |    |    |    |                                                                    |                                                                    |                                                                   |
| NONE     |    |    |    |    |                                                                    |                                                                    |                                                                   |
| 0h       |    |    |    |    |                                                                    |                                                                    |                                                                   |
| 7        | 6  | 5  | 4  | 3  | 2                                                                  | 1                                                                  | 0                                                                 |
| RESERVED |    |    |    |    | R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU0_B1TCM0_PARITY_ERR | R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU0_B0TCM0_PARITY_ERR | R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU0_ATCM0_PARITY_ERR |
| NONE     |    |    |    |    | R/W                                                                | R/W                                                                | R/W                                                               |
| 0h       |    |    |    |    | 0h                                                                 | 0h                                                                 | 0h                                                                |

**Table 2-527. MSS\_CTRL\_R5SS0\_CORE0\_TCM\_ADDRPARITY\_ERRAGG\_MASK Register Field Descriptions**

| Bit  | Field                                                              | Type | Reset | Description                                                                                                                                          |
|------|--------------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                                                           | NONE | 0h    | Reserved                                                                                                                                             |
| 2    | R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU0_B1TCM0_PARITY_ERR | R/W  | 0h    | Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 1    | R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU0_B0TCM0_PARITY_ERR | R/W  | 0h    | Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 0    | R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU0_ATCM0_PARITY_ERR  | R/W  | 0h    | Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |

### 2.2.2.176 MSS\_CTRL\_R5SS0\_CORE0\_TCM\_ADDRPARITY\_ERRAGG\_STATUS Register

**1 MSS\_CTRL\_R5SS0\_CORE0\_TCM\_ADDRPARITY\_ERRAGG\_STATUS Register (Offset = 18104h) [reset = 0h]**

Status register based on mask for TCM address parity errors from R5SS0 CORE0.

Return to [Summary Table](#)

**Table 2-528. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8104h       |

**Figure 2-176. MSS\_CTRL\_R5SS0\_CORE0\_TCM\_ADDRPARITY\_ERRAGG\_STATUS Name Register**

|          |    |    |    |    |                                                                       |                                                                       |                                                                      |
|----------|----|----|----|----|-----------------------------------------------------------------------|-----------------------------------------------------------------------|----------------------------------------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26                                                                    | 25                                                                    | 24                                                                   |
| RESERVED |    |    |    |    |                                                                       |                                                                       |                                                                      |
| NONE     |    |    |    |    |                                                                       |                                                                       |                                                                      |
| 0h       |    |    |    |    |                                                                       |                                                                       |                                                                      |
| 23       | 22 | 21 | 20 | 19 | 18                                                                    | 17                                                                    | 16                                                                   |
| RESERVED |    |    |    |    |                                                                       |                                                                       |                                                                      |
| NONE     |    |    |    |    |                                                                       |                                                                       |                                                                      |
| 0h       |    |    |    |    |                                                                       |                                                                       |                                                                      |
| 15       | 14 | 13 | 12 | 11 | 10                                                                    | 9                                                                     | 8                                                                    |
| RESERVED |    |    |    |    |                                                                       |                                                                       |                                                                      |
| NONE     |    |    |    |    |                                                                       |                                                                       |                                                                      |
| 0h       |    |    |    |    |                                                                       |                                                                       |                                                                      |
| 7        | 6  | 5  | 4  | 3  | 2                                                                     | 1                                                                     | 0                                                                    |
| RESERVED |    |    |    |    | R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU0_B1T_CM0_PARITY_ERR | R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU0_B0T_CM0_PARITY_ERR | R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU0_ATC_M0_PARITY_ERR |
| NONE     |    |    |    |    | R/W                                                                   | R/W                                                                   | R/W                                                                  |
| 0h       |    |    |    |    | 0h                                                                    | 0h                                                                    | 0h                                                                   |

**Table 2-530. MSS\_CTRL\_R5SS0\_CORE0\_TCM\_ADDRPARITY\_ERRAGG\_STATUS Register Field Descriptions**

| Bit  | Field                                                                 | Type | Reset | Description                                                                                                                                   |
|------|-----------------------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                                                              | NONE | 0h    | Reserved                                                                                                                                      |
| 2    | R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU0_B1T_CM0_PARITY_ERR | R/W  | 0h    | Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 1    | R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU0_B0T_CM0_PARITY_ERR | R/W  | 0h    | Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 0    | R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU0_ATC_M0_PARITY_ERR  | R/W  | 0h    | Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |

### 2.2.2.177 MSS\_CTRL\_R5SS0\_CORE0\_TCM\_ADDRPARITY\_ERRAGG\_STATUS\_RAW Register

#### 1 MSS\_CTRL\_R5SS0\_CORE0\_TCM\_ADDRPARITY\_ERRAGG\_STATUS\_RAW Register (Offset = 18108h) [reset = 0h]

Raw status for TCM address parity errors from R5SS0 CORE0.

Return to [Summary Table](#)

**Table 2-531. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8108h       |

**Figure 2-177. MSS\_CTRL\_R5SS0\_CORE0\_TCM\_ADDRPARITY\_ERRAGG\_STATUS\_RAW Name Register**

| 31       | 30 | 29 | 28 | 27 | 26                                                                       | 25                                                                       | 24                                                                      |
|----------|----|----|----|----|--------------------------------------------------------------------------|--------------------------------------------------------------------------|-------------------------------------------------------------------------|
| RESERVED |    |    |    |    |                                                                          |                                                                          |                                                                         |
| NONE     |    |    |    |    |                                                                          |                                                                          |                                                                         |
| 0h       |    |    |    |    |                                                                          |                                                                          |                                                                         |
| 23       | 22 | 21 | 20 | 19 | 18                                                                       | 17                                                                       | 16                                                                      |
| RESERVED |    |    |    |    |                                                                          |                                                                          |                                                                         |
| NONE     |    |    |    |    |                                                                          |                                                                          |                                                                         |
| 0h       |    |    |    |    |                                                                          |                                                                          |                                                                         |
| 15       | 14 | 13 | 12 | 11 | 10                                                                       | 9                                                                        | 8                                                                       |
| RESERVED |    |    |    |    |                                                                          |                                                                          |                                                                         |
| NONE     |    |    |    |    |                                                                          |                                                                          |                                                                         |
| 0h       |    |    |    |    |                                                                          |                                                                          |                                                                         |
| 7        | 6  | 5  | 4  | 3  | 2                                                                        | 1                                                                        | 0                                                                       |
| RESERVED |    |    |    |    | R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU0_B1TCM0_PARITY_ERR | R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU0_B0TCM0_PARITY_ERR | R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU0_ATCM0_PARITY_ERR |
| NONE     |    |    |    |    | R/W                                                                      | R/W                                                                      | R/W                                                                     |
| 0h       |    |    |    |    | 0h                                                                       | 0h                                                                       | 0h                                                                      |

**Table 2-533. MSS\_CTRL\_R5SS0\_CORE0\_TCM\_ADDRPARITY\_ERRAGG\_STATUS\_RAW Register Field Descriptions**

| Bit  | Field                                                                    | Type | Reset | Description                                                                                                                                       |
|------|--------------------------------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                                                                 | NONE | 0h    | Reserved                                                                                                                                          |
| 2    | R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU0_B1TCM0_PARITY_ERR | R/W  | 0h    | Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 1    | R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU0_B0TCM0_PARITY_ERR | R/W  | 0h    | Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 0    | R5SS0_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU0_ATCM0_PARITY_ERR  | R/W  | 0h    | Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |

### 2.2.2.178 MSS\_CTRL\_R5SS0\_CORE1\_TCM\_ADDRPARITY\_ERRAGG\_MASK Register

**1 MSS\_CTRL\_R5SS0\_CORE1\_TCM\_ADDRPARITY\_ERRAGG\_MASK Register (Offset = 18110h) [reset = 0h]**

Register to Mask TCM address parity errors from R5SS0 CORE1.

Return to [Summary Table](#)

**Table 2-534. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8110h       |

**Figure 2-178. MSS\_CTRL\_R5SS0\_CORE1\_TCM\_ADDRPARITY\_ERRAGG\_MASK Name Register**

| 31       | 30 | 29 | 28 | 27 | 26                                                                 | 25                                                                 | 24                                                                |
|----------|----|----|----|----|--------------------------------------------------------------------|--------------------------------------------------------------------|-------------------------------------------------------------------|
| RESERVED |    |    |    |    |                                                                    |                                                                    |                                                                   |
| NONE     |    |    |    |    |                                                                    |                                                                    |                                                                   |
| 0h       |    |    |    |    |                                                                    |                                                                    |                                                                   |
| 23       | 22 | 21 | 20 | 19 | 18                                                                 | 17                                                                 | 16                                                                |
| RESERVED |    |    |    |    |                                                                    |                                                                    |                                                                   |
| NONE     |    |    |    |    |                                                                    |                                                                    |                                                                   |
| 0h       |    |    |    |    |                                                                    |                                                                    |                                                                   |
| 15       | 14 | 13 | 12 | 11 | 10                                                                 | 9                                                                  | 8                                                                 |
| RESERVED |    |    |    |    |                                                                    |                                                                    |                                                                   |
| NONE     |    |    |    |    |                                                                    |                                                                    |                                                                   |
| 0h       |    |    |    |    |                                                                    |                                                                    |                                                                   |
| 7        | 6  | 5  | 4  | 3  | 2                                                                  | 1                                                                  | 0                                                                 |
| RESERVED |    |    |    |    | R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU1_B1TCM1_PARITY_ERR | R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU1_B1TCM0_PARITY_ERR | R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU1_ATCM1_PARITY_ERR |
| NONE     |    |    |    |    | R/W                                                                | R/W                                                                | R/W                                                               |
| 0h       |    |    |    |    | 0h                                                                 | 0h                                                                 | 0h                                                                |

**Table 2-536. MSS\_CTRL\_R5SS0\_CORE1\_TCM\_ADDRPARITY\_ERRAGG\_MASK Register Field Descriptions**

| Bit  | Field                                                              | Type | Reset | Description                                                                                                                                          |
|------|--------------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                                                           | NONE | 0h    | Reserved                                                                                                                                             |
| 2    | R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU1_B1TCM1_PARITY_ERR | R/W  | 0h    | Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 1    | R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU1_B1TCM0_PARITY_ERR | R/W  | 0h    | Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 0    | R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS0_CPU1_ATCM1_PARITY_ERR  | R/W  | 0h    | Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |

### 2.2.2.179 MSS\_CTRL\_R5SS0\_CORE1\_TCM\_ADDRPARITY\_ERRAGG\_STATUS Register

**1 MSS\_CTRL\_R5SS0\_CORE1\_TCM\_ADDRPARITY\_ERRAGG\_STATUS Register (Offset = 18114h) [reset = 0h]**

Status register based on mask for TCM address parity errors from R5SS0 CORE1.

Return to [Summary Table](#)

**Table 2-537. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8114h       |

**Figure 2-179. MSS\_CTRL\_R5SS0\_CORE1\_TCM\_ADDRPARITY\_ERRAGG\_STATUS Name Register**

|          |    |    |    |    |                                                                      |                                                                      |                                                                    |
|----------|----|----|----|----|----------------------------------------------------------------------|----------------------------------------------------------------------|--------------------------------------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26                                                                   | 25                                                                   | 24                                                                 |
| RESERVED |    |    |    |    |                                                                      |                                                                      |                                                                    |
| NONE     |    |    |    |    |                                                                      |                                                                      |                                                                    |
| 0h       |    |    |    |    |                                                                      |                                                                      |                                                                    |
| 23       | 22 | 21 | 20 | 19 | 18                                                                   | 17                                                                   | 16                                                                 |
| RESERVED |    |    |    |    |                                                                      |                                                                      |                                                                    |
| NONE     |    |    |    |    |                                                                      |                                                                      |                                                                    |
| 0h       |    |    |    |    |                                                                      |                                                                      |                                                                    |
| 15       | 14 | 13 | 12 | 11 | 10                                                                   | 9                                                                    | 8                                                                  |
| RESERVED |    |    |    |    |                                                                      |                                                                      |                                                                    |
| NONE     |    |    |    |    |                                                                      |                                                                      |                                                                    |
| 0h       |    |    |    |    |                                                                      |                                                                      |                                                                    |
| 7        | 6  | 5  | 4  | 3  | 2                                                                    | 1                                                                    | 0                                                                  |
| RESERVED |    |    |    |    | R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5S0_CPU1_B1T_CM1_PARITY_ERR | R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5S0_CPU1_B0T_CM1_PARITY_ERR | R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5S0_CPU1_ATCM1_PARITY_ERR |
| NONE     |    |    |    |    | R/W                                                                  | R/W                                                                  | R/W                                                                |
| 0h       |    |    |    |    | 0h                                                                   | 0h                                                                   | 0h                                                                 |

**Table 2-539. MSS\_CTRL\_R5SS0\_CORE1\_TCM\_ADDRPARITY\_ERRAGG\_STATUS Register Field Descriptions**

| Bit  | Field                                                                 | Type | Reset | Description                                                                                                                                   |
|------|-----------------------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                                                              | NONE | 0h    | Reserved                                                                                                                                      |
| 2    | R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU1_B1T_CM1_PARITY_ERR | R/W  | 0h    | Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 1    | R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU1_B0T_CM1_PARITY_ERR | R/W  | 0h    | Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 0    | R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS0_CPU1_ATCM1_PARITY_ERR   | R/W  | 0h    | Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |

### 2.2.2.180 MSS\_CTRL\_R5SS0\_CORE1\_TCM\_ADDRPARITY\_ERRAGG\_STATUS\_RAW Register

#### 1 MSS\_CTRL\_R5SS0\_CORE1\_TCM\_ADDRPARITY\_ERRAGG\_STATUS\_RAW Register (Offset = 18118h) [reset = 0h]

Raw status for TCM address parity errors from R5SS0 CORE1.

Return to [Summary Table](#)

**Table 2-540. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8118h       |

**Figure 2-180. MSS\_CTRL\_R5SS0\_CORE1\_TCM\_ADDRPARITY\_ERRAGG\_STATUS\_RAW Name Register**

| 31       | 30 | 29 | 28 | 27 | 26                                                                       | 25                                                                       | 24                                                                      |
|----------|----|----|----|----|--------------------------------------------------------------------------|--------------------------------------------------------------------------|-------------------------------------------------------------------------|
| RESERVED |    |    |    |    |                                                                          |                                                                          |                                                                         |
| NONE     |    |    |    |    |                                                                          |                                                                          |                                                                         |
| 0h       |    |    |    |    |                                                                          |                                                                          |                                                                         |
| 23       | 22 | 21 | 20 | 19 | 18                                                                       | 17                                                                       | 16                                                                      |
| RESERVED |    |    |    |    |                                                                          |                                                                          |                                                                         |
| NONE     |    |    |    |    |                                                                          |                                                                          |                                                                         |
| 0h       |    |    |    |    |                                                                          |                                                                          |                                                                         |
| 15       | 14 | 13 | 12 | 11 | 10                                                                       | 9                                                                        | 8                                                                       |
| RESERVED |    |    |    |    |                                                                          |                                                                          |                                                                         |
| NONE     |    |    |    |    |                                                                          |                                                                          |                                                                         |
| 0h       |    |    |    |    |                                                                          |                                                                          |                                                                         |
| 7        | 6  | 5  | 4  | 3  | 2                                                                        | 1                                                                        | 0                                                                       |
| RESERVED |    |    |    |    | R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU1_B1TCM1_PARITY_ERR | R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU1_B0TCM1_PARITY_ERR | R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU1_ATCM1_PARITY_ERR |
| NONE     |    |    |    |    | R/W                                                                      | R/W                                                                      | R/W                                                                     |
| 0h       |    |    |    |    | 0h                                                                       | 0h                                                                       | 0h                                                                      |

**Table 2-542. MSS\_CTRL\_R5SS0\_CORE1\_TCM\_ADDRPARITY\_ERRAGG\_STATUS\_RAW Register Field Descriptions**

| Bit  | Field                                                                    | Type | Reset | Description                                                                                                                                        |
|------|--------------------------------------------------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                                                                 | NONE | 0h    | Reserved                                                                                                                                           |
| 2    | R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU1_B1TCM1_PARITY_ERR | R/W  | 0h    | Raw Status of Interrupt from address parity error of corresponding CPU* _TCM_ADDRPARITY_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 1    | R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU1_B0TCM1_PARITY_ERR | R/W  | 0h    | Raw Status of Interrupt from address parity error of corresponding CPU* _TCM_ADDRPARITY_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 0    | R5SS0_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS0_CPU1_ATCM1_PARITY_ERR  | R/W  | 0h    | Raw Status of Interrupt from address parity error of corresponding CPU* _TCM_ADDRPARITY_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |

### 2.2.2.181 MSS\_CTRL\_TCM0\_PARITY\_CTRL Register

#### 1 MSS\_CTRL\_TCM0\_PARITY\_CTRL Register (Offset = 18120h) [reset = 0h]

This register clears the TCM Address Parity Errors of R5SS0.

Return to [Summary Table](#)

**Table 2-543. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8120h       |

**Figure 2-181. MSS\_CTRL\_TCM0\_PARITY\_CTRL Name Register**

|          |                                     |    |    |          |                                     |    |    |
|----------|-------------------------------------|----|----|----------|-------------------------------------|----|----|
| 31       | 30                                  | 29 | 28 | 27       | 26                                  | 25 | 24 |
| RESERVED |                                     |    |    |          |                                     |    |    |
| NONE     |                                     |    |    |          |                                     |    |    |
| 0h       |                                     |    |    |          |                                     |    |    |
| 23       | 22                                  | 21 | 20 | 19       | 18                                  | 17 | 16 |
| RESERVED | TCM0_PARITY_CTRL_B1TCM1_ERRADDR_CLR |    |    | RESERVED | TCM0_PARITY_CTRL_B1TCM0_ERRADDR_CLR |    |    |
| NONE     | R/W                                 |    |    | NONE     | R/W                                 |    |    |
| 0h       | 0h                                  |    |    | 0h       | 0h                                  |    |    |
| 15       | 14                                  | 13 | 12 | 11       | 10                                  | 9  | 8  |
| RESERVED | TCM0_PARITY_CTRL_B0CM1_ERRADDR_CLR  |    |    | RESERVED | TCM0_PARITY_CTRL_B0TCM0_ERRADDR_CLR |    |    |
| NONE     | R/W                                 |    |    | NONE     | R/W                                 |    |    |
| 0h       | 0h                                  |    |    | 0h       | 0h                                  |    |    |
| 7        | 6                                   | 5  | 4  | 3        | 2                                   | 1  | 0  |
| RESERVED | TCM0_PARITY_CTRL_ATCM1_ERRADDR_CLR  |    |    | RESERVED | TCM0_PARITY_CTRL_ATCM0_ERRADDR_CLR  |    |    |
| NONE     | R/W                                 |    |    | NONE     | R/W                                 |    |    |
| 0h       | 0h                                  |    |    | 0h       | 0h                                  |    |    |

**Table 2-545. MSS\_CTRL\_TCM0\_PARITY\_CTRL Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                                                           |
|-------|-------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:23 | RESERVED                            | NONE | 0h    | Reserved                                                                                              |
| 22:20 | TCM0_PARITY_CTRL_B1TCM1_ERRADDR_CLR | R/W  | 0h    | Write pulse bit field: Writing 3'b111 clears the Address latched after parity error for B1TCM of CR5B |
| 19    | RESERVED                            | NONE | 0h    | Reserved                                                                                              |
| 18:16 | TCM0_PARITY_CTRL_B1TCM0_ERRADDR_CLR | R/W  | 0h    | Write pulse bit field: Writing 3'b111 clears the Address latched after parity error for B1TCM of CR5A |
| 15    | RESERVED                            | NONE | 0h    | Reserved                                                                                              |
| 14:12 | TCM0_PARITY_CTRL_B0CM1_ERRADDR_CLR  | R/W  | 0h    | Write pulse bit field: Writing 3'b111 clears the Address latched after parity error for B0TCM of CR5B |
| 11    | RESERVED                            | NONE | 0h    | Reserved                                                                                              |
| 10:8  | TCM0_PARITY_CTRL_B0TCM0_ERRADDR_CLR | R/W  | 0h    | Write pulse bit field: Writing 3'b111 clears the Address latched after parity error for B0TCM of CR5A |
| 7     | RESERVED                            | NONE | 0h    | Reserved                                                                                              |
| 6:4   | TCM0_PARITY_CTRL_ATCM1_ERRADDR_CLR  | R/W  | 0h    | Write pulse bit field: Writing 3'b111 clears the Address latched after parity error for ATCM of CR5B  |
| 3     | RESERVED                            | NONE | 0h    | Reserved                                                                                              |

**Table 2-545. MSS\_CTRL\_TCM0\_PARITY\_CTRL Register Field Descriptions (continued)**

| Bit | Field                              | Type | Reset | Description                                                                                      |
|-----|------------------------------------|------|-------|--------------------------------------------------------------------------------------------------|
| 2:0 | TCM0_PARITY_CTRL_ATCM0_ERRADDR_CLR | R/W  | 0h    | Pulse bit-field<br>Writing 3'b111 clears the Address latched after parity error for ATCM of CR5A |



### 2.2.2.182 MSS\_CTRL\_ERR\_PARITY\_ATCM0\_R5SS0 Register

#### 1 MSS\_CTRL\_ERR\_PARITY\_ATCM0\_R5SS0 Register (Offset = 18124h) [reset = 0h]

This register latches the ATCM Address where the Address Parity Error occurred in R5SS0 CORE0.

Return to [Summary Table](#)

**Table 2-546. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8124h       |

**Figure 2-182. MSS\_CTRL\_ERR\_PARITY\_ATCM0\_R5SS0 Name Register**

|                             |    |    |    |                             |    |    |    |
|-----------------------------|----|----|----|-----------------------------|----|----|----|
| 31                          | 30 | 29 | 28 | 27                          | 26 | 25 | 24 |
| RESERVED                    |    |    |    |                             |    |    |    |
| NONE                        |    |    |    |                             |    |    |    |
| 0h                          |    |    |    |                             |    |    |    |
| 23                          | 22 | 21 | 20 | 19                          | 18 | 17 | 16 |
| RESERVED                    |    |    |    | ERR_PARITY_ATCM0_R5SS0_ADDR |    |    |    |
| NONE                        |    |    |    | R                           |    |    |    |
| 0h                          |    |    |    | 0h                          |    |    |    |
| 15                          | 14 | 13 | 12 | 11                          | 10 | 9  | 8  |
| ERR_PARITY_ATCM0_R5SS0_ADDR |    |    |    |                             |    |    |    |
| R                           |    |    |    |                             |    |    |    |
| 0h                          |    |    |    |                             |    |    |    |
| 7                           | 6  | 5  | 4  | 3                           | 2  | 1  | 0  |
| ERR_PARITY_ATCM0_R5SS0_ADDR |    |    |    |                             |    |    |    |
| R                           |    |    |    |                             |    |    |    |
| 0h                          |    |    |    |                             |    |    |    |

**Table 2-548. MSS\_CTRL\_ERR\_PARITY\_ATCM0\_R5SS0 Register Field Descriptions**

| Bit   | Field                       | Type | Reset | Description                                                    |
|-------|-----------------------------|------|-------|----------------------------------------------------------------|
| 31:20 | RESERVED                    | NONE | 0h    | Reserved                                                       |
| 19:0  | ERR_PARITY_ATCM0_R5SS0_ADDR | R    | 0h    | Address latched when parity error is occurred for ATCM of CR5A |

### 2.2.2.183 MSS\_CTRL\_ERR\_PARITY\_ATCM1\_R5SS0 Register

#### 1 MSS\_CTRL\_ERR\_PARITY\_ATCM1\_R5SS0 Register (Offset = 18128h) [reset = 0h]

This register latches the ATCM Address where the Address Parity Error occurred in R5SS0 CORE1.

Return to [Summary Table](#)

**Table 2-549. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8128h       |

**Figure 2-183. MSS\_CTRL\_ERR\_PARITY\_ATCM1\_R5SS0 Name Register**

|                             |    |    |    |                             |    |    |    |
|-----------------------------|----|----|----|-----------------------------|----|----|----|
| 31                          | 30 | 29 | 28 | 27                          | 26 | 25 | 24 |
| RESERVED                    |    |    |    |                             |    |    |    |
| NONE                        |    |    |    |                             |    |    |    |
| 0h                          |    |    |    |                             |    |    |    |
| 23                          | 22 | 21 | 20 | 19                          | 18 | 17 | 16 |
| RESERVED                    |    |    |    | ERR_PARITY_ATCM1_R5SS0_ADDR |    |    |    |
| NONE                        |    |    |    | R                           |    |    |    |
| 0h                          |    |    |    | 0h                          |    |    |    |
| 15                          | 14 | 13 | 12 | 11                          | 10 | 9  | 8  |
| ERR_PARITY_ATCM1_R5SS0_ADDR |    |    |    |                             |    |    |    |
| R                           |    |    |    |                             |    |    |    |
| 0h                          |    |    |    |                             |    |    |    |
| 7                           | 6  | 5  | 4  | 3                           | 2  | 1  | 0  |
| ERR_PARITY_ATCM1_R5SS0_ADDR |    |    |    |                             |    |    |    |
| R                           |    |    |    |                             |    |    |    |
| 0h                          |    |    |    |                             |    |    |    |

**Table 2-551. MSS\_CTRL\_ERR\_PARITY\_ATCM1\_R5SS0 Register Field Descriptions**

| Bit   | Field                       | Type | Reset | Description                                                    |
|-------|-----------------------------|------|-------|----------------------------------------------------------------|
| 31:20 | RESERVED                    | NONE | 0h    | Reserved                                                       |
| 19:0  | ERR_PARITY_ATCM1_R5SS0_ADDR | R    | 0h    | Address latched when parity error is occurred for ATCM of CR5B |

### 2.2.2.184 MSS\_CTRL\_ERR\_PARITY\_B0TCM0\_R5SS0 Register

#### 1 MSS\_CTRL\_ERR\_PARITY\_B0TCM0\_R5SS0 Register (Offset = 1812Ch) [reset = 0h]

This register latches the B0TCM Address where the Address Parity Error occurred in R5SS0 CORE0.

Return to [Summary Table](#)

**Table 2-552. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 812Ch       |

**Figure 2-184. MSS\_CTRL\_ERR\_PARITY\_B0TCM0\_R5SS0 Name Register**

|                              |    |    |    |                              |    |    |    |
|------------------------------|----|----|----|------------------------------|----|----|----|
| 31                           | 30 | 29 | 28 | 27                           | 26 | 25 | 24 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 23                           | 22 | 21 | 20 | 19                           | 18 | 17 | 16 |
| RESERVED                     |    |    |    | ERR_PARITY_B0TCM0_R5SS0_ADDR |    |    |    |
| NONE                         |    |    |    | R                            |    |    |    |
| 0h                           |    |    |    | 0h                           |    |    |    |
| 15                           | 14 | 13 | 12 | 11                           | 10 | 9  | 8  |
| ERR_PARITY_B0TCM0_R5SS0_ADDR |    |    |    |                              |    |    |    |
| R                            |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 7                            | 6  | 5  | 4  | 3                            | 2  | 1  | 0  |
| ERR_PARITY_B0TCM0_R5SS0_ADDR |    |    |    |                              |    |    |    |
| R                            |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |

**Table 2-554. MSS\_CTRL\_ERR\_PARITY\_B0TCM0\_R5SS0 Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                     |
|-------|------------------------------|------|-------|-----------------------------------------------------------------|
| 31:20 | RESERVED                     | NONE | 0h    | Reserved                                                        |
| 19:0  | ERR_PARITY_B0TCM0_R5SS0_ADDR | R    | 0h    | Address latched when parity error is occurred for B0TCM of CR5A |

### 2.2.2.185 MSS\_CTRL\_ERR\_PARITY\_B0TCM1\_R5SS0 Register

#### 1 MSS\_CTRL\_ERR\_PARITY\_B0TCM1\_R5SS0 Register (Offset = 18130h) [reset = 0h]

This register latches the B0TCM Address where the Address Parity Error occurred in R5SS0 CORE1.

Return to [Summary Table](#)

**Table 2-555. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8130h       |

**Figure 2-185. MSS\_CTRL\_ERR\_PARITY\_B0TCM1\_R5SS0 Name Register**

|                              |    |    |    |                              |    |    |    |
|------------------------------|----|----|----|------------------------------|----|----|----|
| 31                           | 30 | 29 | 28 | 27                           | 26 | 25 | 24 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 23                           | 22 | 21 | 20 | 19                           | 18 | 17 | 16 |
| RESERVED                     |    |    |    | ERR_PARITY_B0TCM1_R5SS0_ADDR |    |    |    |
| NONE                         |    |    |    | R                            |    |    |    |
| 0h                           |    |    |    | 0h                           |    |    |    |
| 15                           | 14 | 13 | 12 | 11                           | 10 | 9  | 8  |
| ERR_PARITY_B0TCM1_R5SS0_ADDR |    |    |    |                              |    |    |    |
| R                            |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 7                            | 6  | 5  | 4  | 3                            | 2  | 1  | 0  |
| ERR_PARITY_B0TCM1_R5SS0_ADDR |    |    |    |                              |    |    |    |
| R                            |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |

**Table 2-557. MSS\_CTRL\_ERR\_PARITY\_B0TCM1\_R5SS0 Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                     |
|-------|------------------------------|------|-------|-----------------------------------------------------------------|
| 31:20 | RESERVED                     | NONE | 0h    | Reserved                                                        |
| 19:0  | ERR_PARITY_B0TCM1_R5SS0_ADDR | R    | 0h    | Address latched when parity error is occurred for B0TCM of CR5B |

### 2.2.2.186 MSS\_CTRL\_ERR\_PARITY\_B1TCM0\_R5SS0 Register

#### 1 MSS\_CTRL\_ERR\_PARITY\_B1TCM0\_R5SS0 Register (Offset = 18134h) [reset = 0h]

This register latches the B1TCM Address where the Address Parity Error occurred in R5SS0 CORE0.

Return to [Summary Table](#)

**Table 2-558. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8134h       |

**Figure 2-186. MSS\_CTRL\_ERR\_PARITY\_B1TCM0\_R5SS0 Name Register**

|                              |    |    |    |                              |    |    |    |
|------------------------------|----|----|----|------------------------------|----|----|----|
| 31                           | 30 | 29 | 28 | 27                           | 26 | 25 | 24 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 23                           | 22 | 21 | 20 | 19                           | 18 | 17 | 16 |
| RESERVED                     |    |    |    | ERR_PARITY_B1TCM0_R5SS0_ADDR |    |    |    |
| NONE                         |    |    |    | R                            |    |    |    |
| 0h                           |    |    |    | 0h                           |    |    |    |
| 15                           | 14 | 13 | 12 | 11                           | 10 | 9  | 8  |
| ERR_PARITY_B1TCM0_R5SS0_ADDR |    |    |    |                              |    |    |    |
| R                            |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 7                            | 6  | 5  | 4  | 3                            | 2  | 1  | 0  |
| ERR_PARITY_B1TCM0_R5SS0_ADDR |    |    |    |                              |    |    |    |
| R                            |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |

**Table 2-560. MSS\_CTRL\_ERR\_PARITY\_B1TCM0\_R5SS0 Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                     |
|-------|------------------------------|------|-------|-----------------------------------------------------------------|
| 31:20 | RESERVED                     | NONE | 0h    | Reserved                                                        |
| 19:0  | ERR_PARITY_B1TCM0_R5SS0_ADDR | R    | 0h    | Address latched when parity error is occurred for B1TCM of CR5A |

### 2.2.2.187 MSS\_CTRL\_ERR\_PARITY\_B1TCM1\_R5SS0 Register

#### 1 MSS\_CTRL\_ERR\_PARITY\_B1TCM1\_R5SS0 Register (Offset = 18138h) [reset = 0h]

This register latches the B1TCM Address where the Address Parity Error occurred in R5SS0 CORE1.

Return to [Summary Table](#)

**Table 2-561. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8138h       |

**Figure 2-187. MSS\_CTRL\_ERR\_PARITY\_B1TCM1\_R5SS0 Name Register**

|                              |    |    |    |                              |    |    |    |
|------------------------------|----|----|----|------------------------------|----|----|----|
| 31                           | 30 | 29 | 28 | 27                           | 26 | 25 | 24 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 23                           | 22 | 21 | 20 | 19                           | 18 | 17 | 16 |
| RESERVED                     |    |    |    | ERR_PARITY_B1TCM1_R5SS0_ADDR |    |    |    |
| NONE                         |    |    |    | R                            |    |    |    |
| 0h                           |    |    |    | 0h                           |    |    |    |
| 15                           | 14 | 13 | 12 | 11                           | 10 | 9  | 8  |
| ERR_PARITY_B1TCM1_R5SS0_ADDR |    |    |    |                              |    |    |    |
| R                            |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 7                            | 6  | 5  | 4  | 3                            | 2  | 1  | 0  |
| ERR_PARITY_B1TCM1_R5SS0_ADDR |    |    |    |                              |    |    |    |
| R                            |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |

**Table 2-563. MSS\_CTRL\_ERR\_PARITY\_B1TCM1\_R5SS0 Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                     |
|-------|------------------------------|------|-------|-----------------------------------------------------------------|
| 31:20 | RESERVED                     | NONE | 0h    | Reserved                                                        |
| 19:0  | ERR_PARITY_B1TCM1_R5SS0_ADDR | R    | 0h    | Address latched when parity error is occurred for B1TCM of CR5B |

### 2.2.2.188 MSS\_CTRL\_TCM0\_PARITY\_ERRFRC Register

#### 1 MSS\_CTRL\_TCM0\_PARITY\_ERRFRC Register (Offset = 1813Ch) [reset = 0h]

This register is used to Inject fault in the TCM Address Parity Error detection logic of R5SS0 .

Return to [Summary Table](#)

**Table 2-564. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 813Ch       |

**Figure 2-188. MSS\_CTRL\_TCM0\_PARITY\_ERRFRC Name Register**

|          |                           |    |    |          |                           |    |    |
|----------|---------------------------|----|----|----------|---------------------------|----|----|
| 31       | 30                        | 29 | 28 | 27       | 26                        | 25 | 24 |
| RESERVED |                           |    |    |          |                           |    |    |
| NONE     |                           |    |    |          |                           |    |    |
| 0h       |                           |    |    |          |                           |    |    |
| 23       | 22                        | 21 | 20 | 19       | 18                        | 17 | 16 |
| RESERVED | TCM0_PARITY_ERRFRC_B1TCM1 |    |    | RESERVED | TCM0_PARITY_ERRFRC_B1TCM0 |    |    |
| NONE     | R/W                       |    |    | NONE     | R/W                       |    |    |
| 0h       | 0h                        |    |    | 0h       | 0h                        |    |    |
| 15       | 14                        | 13 | 12 | 11       | 10                        | 9  | 8  |
| RESERVED | TCM0_PARITY_ERRFRC_B0TCM1 |    |    | RESERVED | TCM0_PARITY_ERRFRC_B0TCM0 |    |    |
| NONE     | R/W                       |    |    | NONE     | R/W                       |    |    |
| 0h       | 0h                        |    |    | 0h       | 0h                        |    |    |
| 7        | 6                         | 5  | 4  | 3        | 2                         | 1  | 0  |
| RESERVED | TCM0_PARITY_ERRFRC_ATCM1  |    |    | RESERVED | TCM0_PARITY_ERRFRC_ATCM0  |    |    |
| NONE     | R/W                       |    |    | NONE     | R/W                       |    |    |
| 0h       | 0h                        |    |    | 0h       | 0h                        |    |    |

**Table 2-566. MSS\_CTRL\_TCM0\_PARITY\_ERRFRC Register Field Descriptions**

| Bit   | Field                     | Type | Reset | Description                                                                      |
|-------|---------------------------|------|-------|----------------------------------------------------------------------------------|
| 31:23 | RESERVED                  | NONE | 0h    | Reserved                                                                         |
| 22:20 | TCM0_PARITY_ERRFRC_B1TCM1 | R/W  | 0h    | Write pulse bit field:<br>Writing 3'b111 forces a parity error for B1TCM of CR5B |
| 19    | RESERVED                  | NONE | 0h    | Reserved                                                                         |
| 18:16 | TCM0_PARITY_ERRFRC_B1TCM0 | R/W  | 0h    | Write pulse bit field:<br>Writing 3'b111 forces a parity error for B1TCM of CR5A |
| 15    | RESERVED                  | NONE | 0h    | Reserved                                                                         |
| 14:12 | TCM0_PARITY_ERRFRC_B0TCM1 | R/W  | 0h    | Write pulse bit field:<br>Writing 3'b111 forces a parity error for B0TCM of CR5B |
| 11    | RESERVED                  | NONE | 0h    | Reserved                                                                         |
| 10:8  | TCM0_PARITY_ERRFRC_B0TCM0 | R/W  | 0h    | Write pulse bit field:<br>Writing 3'b111 forces a parity error for B0TCM of CR5A |
| 7     | RESERVED                  | NONE | 0h    | Reserved                                                                         |
| 6:4   | TCM0_PARITY_ERRFRC_ATCM1  | R/W  | 0h    | Write pulse bit field:<br>Writing 3'b111 forces a parity error for ATCM of CR5B  |
| 3     | RESERVED                  | NONE | 0h    | Reserved                                                                         |
| 2:0   | TCM0_PARITY_ERRFRC_ATCM0  | R/W  | 0h    | Write pulse bit field:<br>Writing 3'b111 forces a parity error for ATCM of CR5A  |

### 2.2.2.189 MSS\_CTRL\_R5SS1\_CORE0\_TCM\_ADDRPARITY\_ERRAGG\_MASK Register

**1 MSS\_CTRL\_R5SS1\_CORE0\_TCM\_ADDRPARITY\_ERRAGG\_MASK Register (Offset = 18140h) [reset = 0h]**

Register to Mask TCM address parity errors from R5SS1 CORE0.

Return to [Summary Table](#)

**Table 2-567. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8140h       |

**Figure 2-189. MSS\_CTRL\_R5SS1\_CORE0\_TCM\_ADDRPARITY\_ERRAGG\_MASK Name Register**

|          |    |    |    |    |                                                                    |                                                                    |                                                                   |
|----------|----|----|----|----|--------------------------------------------------------------------|--------------------------------------------------------------------|-------------------------------------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26                                                                 | 25                                                                 | 24                                                                |
| RESERVED |    |    |    |    |                                                                    |                                                                    |                                                                   |
| NONE     |    |    |    |    |                                                                    |                                                                    |                                                                   |
| 0h       |    |    |    |    |                                                                    |                                                                    |                                                                   |
| 23       | 22 | 21 | 20 | 19 | 18                                                                 | 17                                                                 | 16                                                                |
| RESERVED |    |    |    |    |                                                                    |                                                                    |                                                                   |
| NONE     |    |    |    |    |                                                                    |                                                                    |                                                                   |
| 0h       |    |    |    |    |                                                                    |                                                                    |                                                                   |
| 15       | 14 | 13 | 12 | 11 | 10                                                                 | 9                                                                  | 8                                                                 |
| RESERVED |    |    |    |    |                                                                    |                                                                    |                                                                   |
| NONE     |    |    |    |    |                                                                    |                                                                    |                                                                   |
| 0h       |    |    |    |    |                                                                    |                                                                    |                                                                   |
| 7        | 6  | 5  | 4  | 3  | 2                                                                  | 1                                                                  | 0                                                                 |
| RESERVED |    |    |    |    | R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU0_B1TCM0_PARITY_ERR | R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU0_B0TCM0_PARITY_ERR | R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU0_ATCM0_PARITY_ERR |
| NONE     |    |    |    |    | R/W                                                                | R/W                                                                | R/W                                                               |
| 0h       |    |    |    |    | 0h                                                                 | 0h                                                                 | 0h                                                                |

**Table 2-569. MSS\_CTRL\_R5SS1\_CORE0\_TCM\_ADDRPARITY\_ERRAGG\_MASK Register Field Descriptions**

| Bit  | Field                                                              | Type | Reset | Description                                                                                                                                          |
|------|--------------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                                                           | NONE | 0h    | Reserved                                                                                                                                             |
| 2    | R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU0_B1TCM0_PARITY_ERR | R/W  | 0h    | Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 1    | R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU0_B0TCM0_PARITY_ERR | R/W  | 0h    | Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 0    | R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU0_ATCM0_PARITY_ERR  | R/W  | 0h    | Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |



### 2.2.2.190 MSS\_CTRL\_R5SS1\_CORE0\_TCM\_ADDRPARITY\_ERRAGG\_STATUS Register

**1 MSS\_CTRL\_R5SS1\_CORE0\_TCM\_ADDRPARITY\_ERRAGG\_STATUS Register (Offset = 18144h) [reset = 0h]**

Status register based on mask for TCM address parity errors from R5SS1 CORE0.

Return to [Summary Table](#)

**Table 2-570. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8144h       |

**Figure 2-190. MSS\_CTRL\_R5SS1\_CORE0\_TCM\_ADDRPARITY\_ERRAGG\_STATUS Name Register**

|          |    |    |    |    |                                                                      |                                                                      |                                                                    |
|----------|----|----|----|----|----------------------------------------------------------------------|----------------------------------------------------------------------|--------------------------------------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26                                                                   | 25                                                                   | 24                                                                 |
| RESERVED |    |    |    |    |                                                                      |                                                                      |                                                                    |
| NONE     |    |    |    |    |                                                                      |                                                                      |                                                                    |
| 0h       |    |    |    |    |                                                                      |                                                                      |                                                                    |
| 23       | 22 | 21 | 20 | 19 | 18                                                                   | 17                                                                   | 16                                                                 |
| RESERVED |    |    |    |    |                                                                      |                                                                      |                                                                    |
| NONE     |    |    |    |    |                                                                      |                                                                      |                                                                    |
| 0h       |    |    |    |    |                                                                      |                                                                      |                                                                    |
| 15       | 14 | 13 | 12 | 11 | 10                                                                   | 9                                                                    | 8                                                                  |
| RESERVED |    |    |    |    |                                                                      |                                                                      |                                                                    |
| NONE     |    |    |    |    |                                                                      |                                                                      |                                                                    |
| 0h       |    |    |    |    |                                                                      |                                                                      |                                                                    |
| 7        | 6  | 5  | 4  | 3  | 2                                                                    | 1                                                                    | 0                                                                  |
| RESERVED |    |    |    |    | R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5S1_CPU0_B1T_CM0_PARITY_ERR | R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5S1_CPU0_B0T_CM0_PARITY_ERR | R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5S1_CPU0_ATCM0_PARITY_ERR |
| NONE     |    |    |    |    | R/W                                                                  | R/W                                                                  | R/W                                                                |
| 0h       |    |    |    |    | 0h                                                                   | 0h                                                                   | 0h                                                                 |

**Table 2-572. MSS\_CTRL\_R5SS1\_CORE0\_TCM\_ADDRPARITY\_ERRAGG\_STATUS Register Field Descriptions**

| Bit  | Field                                                                 | Type | Reset | Description                                                                                                                                   |
|------|-----------------------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                                                              | NONE | 0h    | Reserved                                                                                                                                      |
| 2    | R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU0_B1T_CM0_PARITY_ERR | R/W  | 0h    | Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 1    | R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU0_B0T_CM0_PARITY_ERR | R/W  | 0h    | Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 0    | R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU0_ATCM0_PARITY_ERR   | R/W  | 0h    | Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |

### 2.2.2.191 MSS\_CTRL\_R5SS1\_CORE0\_TCM\_ADDRPARITY\_ERRAGG\_STATUS\_RAW Register

#### 1 MSS\_CTRL\_R5SS1\_CORE0\_TCM\_ADDRPARITY\_ERRAGG\_STATUS\_RAW Register (Offset = 18148h) [reset = 0h]

Raw status for TCM address parity errors from R5SS1 CORE0.

Return to [Summary Table](#)

**Table 2-573. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8148h       |

**Figure 2-191. MSS\_CTRL\_R5SS1\_CORE0\_TCM\_ADDRPARITY\_ERRAGG\_STATUS\_RAW Name Register**

| 31       | 30 | 29 | 28 | 27 | 26                                                                       | 25                                                                       | 24                                                                      |
|----------|----|----|----|----|--------------------------------------------------------------------------|--------------------------------------------------------------------------|-------------------------------------------------------------------------|
| RESERVED |    |    |    |    |                                                                          |                                                                          |                                                                         |
| NONE     |    |    |    |    |                                                                          |                                                                          |                                                                         |
| 0h       |    |    |    |    |                                                                          |                                                                          |                                                                         |
| 23       | 22 | 21 | 20 | 19 | 18                                                                       | 17                                                                       | 16                                                                      |
| RESERVED |    |    |    |    |                                                                          |                                                                          |                                                                         |
| NONE     |    |    |    |    |                                                                          |                                                                          |                                                                         |
| 0h       |    |    |    |    |                                                                          |                                                                          |                                                                         |
| 15       | 14 | 13 | 12 | 11 | 10                                                                       | 9                                                                        | 8                                                                       |
| RESERVED |    |    |    |    |                                                                          |                                                                          |                                                                         |
| NONE     |    |    |    |    |                                                                          |                                                                          |                                                                         |
| 0h       |    |    |    |    |                                                                          |                                                                          |                                                                         |
| 7        | 6  | 5  | 4  | 3  | 2                                                                        | 1                                                                        | 0                                                                       |
| RESERVED |    |    |    |    | R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU0_B1TCM0_PARITY_ERR | R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU0_B0TCM0_PARITY_ERR | R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU0_ATCM0_PARITY_ERR |
| NONE     |    |    |    |    | R/W                                                                      | R/W                                                                      | R/W                                                                     |
| 0h       |    |    |    |    | 0h                                                                       | 0h                                                                       | 0h                                                                      |

**Table 2-575. MSS\_CTRL\_R5SS1\_CORE0\_TCM\_ADDRPARITY\_ERRAGG\_STATUS\_RAW Register Field Descriptions**

| Bit  | Field                                                                    | Type | Reset | Description                                                                                                                                       |
|------|--------------------------------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                                                                 | NONE | 0h    | Reserved                                                                                                                                          |
| 2    | R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU0_B1TCM0_PARITY_ERR | R/W  | 0h    | Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 1    | R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU0_B0TCM0_PARITY_ERR | R/W  | 0h    | Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 0    | R5SS1_CPU0_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU0_ATCM0_PARITY_ERR  | R/W  | 0h    | Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |

### 2.2.2.192 MSS\_CTRL\_R5SS1\_CORE1\_TCM\_ADDRPARITY\_ERRAGG\_MASK Register

**1 MSS\_CTRL\_R5SS1\_CORE1\_TCM\_ADDRPARITY\_ERRAGG\_MASK Register (Offset = 18150h) [reset = 0h]**

Register to Mask TCM address parity errors from R5SS1 CORE1.

Return to [Summary Table](#)

**Table 2-576. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8150h       |

**Figure 2-192. MSS\_CTRL\_R5SS1\_CORE1\_TCM\_ADDRPARITY\_ERRAGG\_MASK Name Register**

|          |    |    |    |    |                                                                    |                                                                    |                                                                   |
|----------|----|----|----|----|--------------------------------------------------------------------|--------------------------------------------------------------------|-------------------------------------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26                                                                 | 25                                                                 | 24                                                                |
| RESERVED |    |    |    |    |                                                                    |                                                                    |                                                                   |
| NONE     |    |    |    |    |                                                                    |                                                                    |                                                                   |
| 0h       |    |    |    |    |                                                                    |                                                                    |                                                                   |
| 23       | 22 | 21 | 20 | 19 | 18                                                                 | 17                                                                 | 16                                                                |
| RESERVED |    |    |    |    |                                                                    |                                                                    |                                                                   |
| NONE     |    |    |    |    |                                                                    |                                                                    |                                                                   |
| 0h       |    |    |    |    |                                                                    |                                                                    |                                                                   |
| 15       | 14 | 13 | 12 | 11 | 10                                                                 | 9                                                                  | 8                                                                 |
| RESERVED |    |    |    |    |                                                                    |                                                                    |                                                                   |
| NONE     |    |    |    |    |                                                                    |                                                                    |                                                                   |
| 0h       |    |    |    |    |                                                                    |                                                                    |                                                                   |
| 7        | 6  | 5  | 4  | 3  | 2                                                                  | 1                                                                  | 0                                                                 |
| RESERVED |    |    |    |    | R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU1_B1TCM1_PARITY_ERR | R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU1_B0TCM1_PARITY_ERR | R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU1_ATCM1_PARITY_ERR |
| NONE     |    |    |    |    | R/W                                                                | R/W                                                                | R/W                                                               |
| 0h       |    |    |    |    | 0h                                                                 | 0h                                                                 | 0h                                                                |

**Table 2-578. MSS\_CTRL\_R5SS1\_CORE1\_TCM\_ADDRPARITY\_ERRAGG\_MASK Register Field Descriptions**

| Bit  | Field                                                              | Type | Reset | Description                                                                                                                                          |
|------|--------------------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                                                           | NONE | 0h    | Reserved                                                                                                                                             |
| 2    | R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU1_B1TCM1_PARITY_ERR | R/W  | 0h    | Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 1    | R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU1_B0TCM1_PARITY_ERR | R/W  | 0h    | Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |
| 0    | R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_MASK_R5SS1_CPU1_ATCM1_PARITY_ERR  | R/W  | 0h    | Mask Interrupt for address parity error s to aggregated Interrupt of corresponding CPU<br>1'b1 : Interrupt is Masked<br>1'b0 : Interrupt is Unmasked |

### 2.2.2.193 MSS\_CTRL\_R5SS1\_CORE1\_TCM\_ADDRPARITY\_ERRAGG\_STATUS Register

#### 1 MSS\_CTRL\_R5SS1\_CORE1\_TCM\_ADDRPARITY\_ERRAGG\_STATUS Register (Offset = 18154h) [reset = 0h]

Status register based on mask for TCM address parity errors from R5SS1 CORE1.

Return to [Summary Table](#)

**Table 2-579. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8154h       |

**Figure 2-193. MSS\_CTRL\_R5SS1\_CORE1\_TCM\_ADDRPARITY\_ERRAGG\_STATUS Name Register**

|          |    |    |    |    |                                                                      |                                                                      |                                                                    |
|----------|----|----|----|----|----------------------------------------------------------------------|----------------------------------------------------------------------|--------------------------------------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26                                                                   | 25                                                                   | 24                                                                 |
| RESERVED |    |    |    |    |                                                                      |                                                                      |                                                                    |
| NONE     |    |    |    |    |                                                                      |                                                                      |                                                                    |
| 0h       |    |    |    |    |                                                                      |                                                                      |                                                                    |
| 23       | 22 | 21 | 20 | 19 | 18                                                                   | 17                                                                   | 16                                                                 |
| RESERVED |    |    |    |    |                                                                      |                                                                      |                                                                    |
| NONE     |    |    |    |    |                                                                      |                                                                      |                                                                    |
| 0h       |    |    |    |    |                                                                      |                                                                      |                                                                    |
| 15       | 14 | 13 | 12 | 11 | 10                                                                   | 9                                                                    | 8                                                                  |
| RESERVED |    |    |    |    |                                                                      |                                                                      |                                                                    |
| NONE     |    |    |    |    |                                                                      |                                                                      |                                                                    |
| 0h       |    |    |    |    |                                                                      |                                                                      |                                                                    |
| 7        | 6  | 5  | 4  | 3  | 2                                                                    | 1                                                                    | 0                                                                  |
| RESERVED |    |    |    |    | R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5S1_CPU1_B1T_CM1_PARITY_ERR | R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5S1_CPU1_B0T_CM1_PARITY_ERR | R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5S1_CPU1_ATCM1_PARITY_ERR |
| NONE     |    |    |    |    | R/W                                                                  | R/W                                                                  | R/W                                                                |
| 0h       |    |    |    |    | 0h                                                                   | 0h                                                                   | 0h                                                                 |

**Table 2-581. MSS\_CTRL\_R5SS1\_CORE1\_TCM\_ADDRPARITY\_ERRAGG\_STATUS Register Field Descriptions**

| Bit  | Field                                                                 | Type | Reset | Description                                                                                                                                   |
|------|-----------------------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                                                              | NONE | 0h    | Reserved                                                                                                                                      |
| 2    | R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU1_B1T_CM1_PARITY_ERR | R/W  | 0h    | Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 1    | R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU1_B0T_CM1_PARITY_ERR | R/W  | 0h    | Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 0    | R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_R5SS1_CPU1_ATCM1_PARITY_ERR   | R/W  | 0h    | Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |

### 2.2.2.194 MSS\_CTRL\_R5SS1\_CORE1\_TCM\_ADDRPARITY\_ERRAGG\_STATUS\_RAW Register

#### 1 MSS\_CTRL\_R5SS1\_CORE1\_TCM\_ADDRPARITY\_ERRAGG\_STATUS\_RAW Register (Offset = 18158h) [reset = 0h]

Raw status for TCM address parity errors from R5SS1 CORE1.

Return to [Summary Table](#)

**Table 2-582. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8158h       |

**Figure 2-194. MSS\_CTRL\_R5SS1\_CORE1\_TCM\_ADDRPARITY\_ERRAGG\_STATUS\_RAW Name Register**

| 31       | 30 | 29 | 28 | 27 | 26                                                                       | 25                                                                       | 24                                                                      |
|----------|----|----|----|----|--------------------------------------------------------------------------|--------------------------------------------------------------------------|-------------------------------------------------------------------------|
| RESERVED |    |    |    |    |                                                                          |                                                                          |                                                                         |
| NONE     |    |    |    |    |                                                                          |                                                                          |                                                                         |
| 0h       |    |    |    |    |                                                                          |                                                                          |                                                                         |
| 23       | 22 | 21 | 20 | 19 | 18                                                                       | 17                                                                       | 16                                                                      |
| RESERVED |    |    |    |    |                                                                          |                                                                          |                                                                         |
| NONE     |    |    |    |    |                                                                          |                                                                          |                                                                         |
| 0h       |    |    |    |    |                                                                          |                                                                          |                                                                         |
| 15       | 14 | 13 | 12 | 11 | 10                                                                       | 9                                                                        | 8                                                                       |
| RESERVED |    |    |    |    |                                                                          |                                                                          |                                                                         |
| NONE     |    |    |    |    |                                                                          |                                                                          |                                                                         |
| 0h       |    |    |    |    |                                                                          |                                                                          |                                                                         |
| 7        | 6  | 5  | 4  | 3  | 2                                                                        | 1                                                                        | 0                                                                       |
| RESERVED |    |    |    |    | R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU1_B1TCM1_PARITY_ERR | R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU1_B0TCM1_PARITY_ERR | R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU1_ATCM1_PARITY_ERR |
| NONE     |    |    |    |    | R/W                                                                      | R/W                                                                      | R/W                                                                     |
| 0h       |    |    |    |    | 0h                                                                       | 0h                                                                       | 0h                                                                      |

**Table 2-584. MSS\_CTRL\_R5SS1\_CORE1\_TCM\_ADDRPARITY\_ERRAGG\_STATUS\_RAW Register Field Descriptions**

| Bit  | Field                                                                    | Type | Reset | Description                                                                                                                                       |
|------|--------------------------------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                                                                 | NONE | 0h    | Reserved                                                                                                                                          |
| 2    | R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU1_B1TCM1_PARITY_ERR | R/W  | 0h    | Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 1    | R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU1_B0TCM1_PARITY_ERR | R/W  | 0h    | Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |
| 0    | R5SS1_CPU1_TCM_ADDRPARITY_ERRAGG_STATUS_RAW_R5SS1_CPU1_ATCM1_PARITY_ERR  | R/W  | 0h    | Raw Status of Interrupt from address parity error of corresponding CPU*_TCM_ADDRPARITY_ERRAGG_MASK register<br>Write 0x1 to clear this interrupt. |

### 2.2.2.195 MSS\_CTRL\_TCM1\_PARITY\_CTRL Register

#### 1 MSS\_CTRL\_TCM1\_PARITY\_CTRL Register (Offset = 18160h) [reset = 0h]

This register clears the TCM Address Parity Errors of R5SS1.

Return to [Summary Table](#)

**Table 2-585. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8160h       |

**Figure 2-195. MSS\_CTRL\_TCM1\_PARITY\_CTRL Name Register**

|          |                                     |    |    |          |                                     |    |    |
|----------|-------------------------------------|----|----|----------|-------------------------------------|----|----|
| 31       | 30                                  | 29 | 28 | 27       | 26                                  | 25 | 24 |
| RESERVED |                                     |    |    |          |                                     |    |    |
| NONE     |                                     |    |    |          |                                     |    |    |
| 0h       |                                     |    |    |          |                                     |    |    |
| 23       | 22                                  | 21 | 20 | 19       | 18                                  | 17 | 16 |
| RESERVED | TCM1_PARITY_CTRL_B1TCM1_ERRADDR_CLR |    |    | RESERVED | TCM1_PARITY_CTRL_B1TCM0_ERRADDR_CLR |    |    |
| NONE     | R/W                                 |    |    | NONE     | R/W                                 |    |    |
| 0h       | 0h                                  |    |    | 0h       | 0h                                  |    |    |
| 15       | 14                                  | 13 | 12 | 11       | 10                                  | 9  | 8  |
| RESERVED | TCM1_PARITY_CTRL_B0CM1_ERRADDR_CLR  |    |    | RESERVED | TCM1_PARITY_CTRL_B0TCM0_ERRADDR_CLR |    |    |
| NONE     | R/W                                 |    |    | NONE     | R/W                                 |    |    |
| 0h       | 0h                                  |    |    | 0h       | 0h                                  |    |    |
| 7        | 6                                   | 5  | 4  | 3        | 2                                   | 1  | 0  |
| RESERVED | TCM1_PARITY_CTRL_ATCM1_ERRADDR_CLR  |    |    | RESERVED | TCM1_PARITY_CTRL_ATCM0_ERRADDR_CLR  |    |    |
| NONE     | R/W                                 |    |    | NONE     | R/W                                 |    |    |
| 0h       | 0h                                  |    |    | 0h       | 0h                                  |    |    |

**Table 2-587. MSS\_CTRL\_TCM1\_PARITY\_CTRL Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                                                           |
|-------|-------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:23 | RESERVED                            | NONE | 0h    | Reserved                                                                                              |
| 22:20 | TCM1_PARITY_CTRL_B1TCM1_ERRADDR_CLR | R/W  | 0h    | Write pulse bit field: Writing 3'b111 clears the Address latched after parity error for B1TCM of CR5B |
| 19    | RESERVED                            | NONE | 0h    | Reserved                                                                                              |
| 18:16 | TCM1_PARITY_CTRL_B1TCM0_ERRADDR_CLR | R/W  | 0h    | Write pulse bit field: Writing 3'b111 clears the Address latched after parity error for B1TCM of CR5A |
| 15    | RESERVED                            | NONE | 0h    | Reserved                                                                                              |
| 14:12 | TCM1_PARITY_CTRL_B0CM1_ERRADDR_CLR  | R/W  | 0h    | Write pulse bit field: Writing 3'b111 clears the Address latched after parity error for B0TCM of CR5B |
| 11    | RESERVED                            | NONE | 0h    | Reserved                                                                                              |
| 10:8  | TCM1_PARITY_CTRL_B0TCM0_ERRADDR_CLR | R/W  | 0h    | Write pulse bit field: Writing 3'b111 clears the Address latched after parity error for B0TCM of CR5A |
| 7     | RESERVED                            | NONE | 0h    | Reserved                                                                                              |
| 6:4   | TCM1_PARITY_CTRL_ATCM1_ERRADDR_CLR  | R/W  | 0h    | Write pulse bit field: Writing 3'b111 clears the Address latched after parity error for ATCM of CR5B  |
| 3     | RESERVED                            | NONE | 0h    | Reserved                                                                                              |

**Table 2-587. MSS\_CTRL\_TCM1\_PARITY\_CTRL Register Field Descriptions (continued)**

| Bit | Field                                  | Type | Reset | Description                                                                                         |
|-----|----------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------|
| 2:0 | TCM1_PARITY_CTRL_AT<br>CM0_ERRADDR_CLR | R/W  | 0h    | Pulse bit-field<br>Writing 3'b111 clears the Address latched after parity error for ATCM<br>of CR5A |

### 2.2.2.196 MSS\_CTRL\_ERR\_PARITY\_ATCM0\_R5SS1 Register

#### 1 MSS\_CTRL\_ERR\_PARITY\_ATCM0\_R5SS1 Register (Offset = 18164h) [reset = 0h]

This register latches the ATCM Address where the Address Parity Error occurred in R5SS1 CORE0.

Return to [Summary Table](#)

**Table 2-588. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8164h       |

**Figure 2-196. MSS\_CTRL\_ERR\_PARITY\_ATCM0\_R5SS1 Name Register**

|                             |    |    |    |                             |    |    |    |
|-----------------------------|----|----|----|-----------------------------|----|----|----|
| 31                          | 30 | 29 | 28 | 27                          | 26 | 25 | 24 |
| RESERVED                    |    |    |    |                             |    |    |    |
| NONE                        |    |    |    |                             |    |    |    |
| 0h                          |    |    |    |                             |    |    |    |
| 23                          | 22 | 21 | 20 | 19                          | 18 | 17 | 16 |
| RESERVED                    |    |    |    | ERR_PARITY_ATCM0_R5SS1_ADDR |    |    |    |
| NONE                        |    |    |    | R                           |    |    |    |
| 0h                          |    |    |    | 0h                          |    |    |    |
| 15                          | 14 | 13 | 12 | 11                          | 10 | 9  | 8  |
| ERR_PARITY_ATCM0_R5SS1_ADDR |    |    |    |                             |    |    |    |
| R                           |    |    |    |                             |    |    |    |
| 0h                          |    |    |    |                             |    |    |    |
| 7                           | 6  | 5  | 4  | 3                           | 2  | 1  | 0  |
| ERR_PARITY_ATCM0_R5SS1_ADDR |    |    |    |                             |    |    |    |
| R                           |    |    |    |                             |    |    |    |
| 0h                          |    |    |    |                             |    |    |    |

**Table 2-590. MSS\_CTRL\_ERR\_PARITY\_ATCM0\_R5SS1 Register Field Descriptions**

| Bit   | Field                       | Type | Reset | Description                                                    |
|-------|-----------------------------|------|-------|----------------------------------------------------------------|
| 31:20 | RESERVED                    | NONE | 0h    | Reserved                                                       |
| 19:0  | ERR_PARITY_ATCM0_R5SS1_ADDR | R    | 0h    | Address latched when parity error is occurred for ATCM of CR5A |



### 2.2.2.197 MSS\_CTRL\_ERR\_PARITY\_ATCM1\_R5SS1 Register

#### 1 MSS\_CTRL\_ERR\_PARITY\_ATCM1\_R5SS1 Register (Offset = 18168h) [reset = 0h]

This register latches the ATCM Address where the Address Parity Error occurred in R5SS1 CORE1.

Return to [Summary Table](#)

**Table 2-591. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8168h       |

**Figure 2-197. MSS\_CTRL\_ERR\_PARITY\_ATCM1\_R5SS1 Name Register**

|                             |    |    |    |                             |    |    |    |
|-----------------------------|----|----|----|-----------------------------|----|----|----|
| 31                          | 30 | 29 | 28 | 27                          | 26 | 25 | 24 |
| RESERVED                    |    |    |    |                             |    |    |    |
| NONE                        |    |    |    |                             |    |    |    |
| 0h                          |    |    |    |                             |    |    |    |
| 23                          | 22 | 21 | 20 | 19                          | 18 | 17 | 16 |
| RESERVED                    |    |    |    | ERR_PARITY_ATCM1_R5SS1_ADDR |    |    |    |
| NONE                        |    |    |    | R                           |    |    |    |
| 0h                          |    |    |    | 0h                          |    |    |    |
| 15                          | 14 | 13 | 12 | 11                          | 10 | 9  | 8  |
| ERR_PARITY_ATCM1_R5SS1_ADDR |    |    |    |                             |    |    |    |
| R                           |    |    |    |                             |    |    |    |
| 0h                          |    |    |    |                             |    |    |    |
| 7                           | 6  | 5  | 4  | 3                           | 2  | 1  | 0  |
| ERR_PARITY_ATCM1_R5SS1_ADDR |    |    |    |                             |    |    |    |
| R                           |    |    |    |                             |    |    |    |
| 0h                          |    |    |    |                             |    |    |    |

**Table 2-593. MSS\_CTRL\_ERR\_PARITY\_ATCM1\_R5SS1 Register Field Descriptions**

| Bit   | Field                       | Type | Reset | Description                                                    |
|-------|-----------------------------|------|-------|----------------------------------------------------------------|
| 31:20 | RESERVED                    | NONE | 0h    | Reserved                                                       |
| 19:0  | ERR_PARITY_ATCM1_R5SS1_ADDR | R    | 0h    | Address latched when parity error is occurred for ATCM of CR5B |

### 2.2.2.198 MSS\_CTRL\_ERR\_PARITY\_B0TCM0\_R5SS1 Register

#### 1 MSS\_CTRL\_ERR\_PARITY\_B0TCM0\_R5SS1 Register (Offset = 1816Ch) [reset = 0h]

This register latches the B0TCM Address where the Address Parity Error occurred in R5SS1 CORE0.

Return to [Summary Table](#)

**Table 2-594. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 816Ch       |

**Figure 2-198. MSS\_CTRL\_ERR\_PARITY\_B0TCM0\_R5SS1 Name Register**

|                              |    |    |    |                              |    |    |    |
|------------------------------|----|----|----|------------------------------|----|----|----|
| 31                           | 30 | 29 | 28 | 27                           | 26 | 25 | 24 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 23                           | 22 | 21 | 20 | 19                           | 18 | 17 | 16 |
| RESERVED                     |    |    |    | ERR_PARITY_B0TCM0_R5SS1_ADDR |    |    |    |
| NONE                         |    |    |    | R                            |    |    |    |
| 0h                           |    |    |    | 0h                           |    |    |    |
| 15                           | 14 | 13 | 12 | 11                           | 10 | 9  | 8  |
| ERR_PARITY_B0TCM0_R5SS1_ADDR |    |    |    |                              |    |    |    |
| R                            |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 7                            | 6  | 5  | 4  | 3                            | 2  | 1  | 0  |
| ERR_PARITY_B0TCM0_R5SS1_ADDR |    |    |    |                              |    |    |    |
| R                            |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |

**Table 2-596. MSS\_CTRL\_ERR\_PARITY\_B0TCM0\_R5SS1 Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                     |
|-------|------------------------------|------|-------|-----------------------------------------------------------------|
| 31:20 | RESERVED                     | NONE | 0h    | Reserved                                                        |
| 19:0  | ERR_PARITY_B0TCM0_R5SS1_ADDR | R    | 0h    | Address latched when parity error is occurred for B0TCM of CR5A |

### 2.2.2.199 MSS\_CTRL\_ERR\_PARITY\_B0TCM1\_R5SS1 Register

#### 1 MSS\_CTRL\_ERR\_PARITY\_B0TCM1\_R5SS1 Register (Offset = 18170h) [reset = 0h]

This register latches the B0TCM Address where the Address Parity Error occurred in R5SS1 CORE1.

Return to [Summary Table](#)

**Table 2-597. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8170h       |

**Figure 2-199. MSS\_CTRL\_ERR\_PARITY\_B0TCM1\_R5SS1 Name Register**

|                              |    |    |    |                              |    |    |    |
|------------------------------|----|----|----|------------------------------|----|----|----|
| 31                           | 30 | 29 | 28 | 27                           | 26 | 25 | 24 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 23                           | 22 | 21 | 20 | 19                           | 18 | 17 | 16 |
| RESERVED                     |    |    |    | ERR_PARITY_B0TCM1_R5SS1_ADDR |    |    |    |
| NONE                         |    |    |    | R                            |    |    |    |
| 0h                           |    |    |    | 0h                           |    |    |    |
| 15                           | 14 | 13 | 12 | 11                           | 10 | 9  | 8  |
| ERR_PARITY_B0TCM1_R5SS1_ADDR |    |    |    |                              |    |    |    |
| R                            |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 7                            | 6  | 5  | 4  | 3                            | 2  | 1  | 0  |
| ERR_PARITY_B0TCM1_R5SS1_ADDR |    |    |    |                              |    |    |    |
| R                            |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |

**Table 2-599. MSS\_CTRL\_ERR\_PARITY\_B0TCM1\_R5SS1 Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                     |
|-------|------------------------------|------|-------|-----------------------------------------------------------------|
| 31:20 | RESERVED                     | NONE | 0h    | Reserved                                                        |
| 19:0  | ERR_PARITY_B0TCM1_R5SS1_ADDR | R    | 0h    | Address latched when parity error is occurred for B0TCM of CR5B |

### 2.2.2.200 MSS\_CTRL\_ERR\_PARITY\_B1TCM0\_R5SS1 Register

#### 1 MSS\_CTRL\_ERR\_PARITY\_B1TCM0\_R5SS1 Register (Offset = 18174h) [reset = 0h]

This register latches the B1TCM Address where the Address Parity Error occurred in R5SS1 CORE0.

Return to [Summary Table](#)

**Table 2-600. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8174h       |

**Figure 2-200. MSS\_CTRL\_ERR\_PARITY\_B1TCM0\_R5SS1 Name Register**

|                              |    |    |    |                              |    |    |    |
|------------------------------|----|----|----|------------------------------|----|----|----|
| 31                           | 30 | 29 | 28 | 27                           | 26 | 25 | 24 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 23                           | 22 | 21 | 20 | 19                           | 18 | 17 | 16 |
| RESERVED                     |    |    |    | ERR_PARITY_B1TCM0_R5SS1_ADDR |    |    |    |
| NONE                         |    |    |    | R                            |    |    |    |
| 0h                           |    |    |    | 0h                           |    |    |    |
| 15                           | 14 | 13 | 12 | 11                           | 10 | 9  | 8  |
| ERR_PARITY_B1TCM0_R5SS1_ADDR |    |    |    |                              |    |    |    |
| R                            |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 7                            | 6  | 5  | 4  | 3                            | 2  | 1  | 0  |
| ERR_PARITY_B1TCM0_R5SS1_ADDR |    |    |    |                              |    |    |    |
| R                            |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |

**Table 2-602. MSS\_CTRL\_ERR\_PARITY\_B1TCM0\_R5SS1 Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                     |
|-------|------------------------------|------|-------|-----------------------------------------------------------------|
| 31:20 | RESERVED                     | NONE | 0h    | Reserved                                                        |
| 19:0  | ERR_PARITY_B1TCM0_R5SS1_ADDR | R    | 0h    | Address latched when parity error is occurred for B1TCM of CR5A |

### 2.2.2.201 MSS\_CTRL\_ERR\_PARITY\_B1TCM1\_R5SS1 Register

#### 1 MSS\_CTRL\_ERR\_PARITY\_B1TCM1\_R5SS1 Register (Offset = 18178h) [reset = 0h]

This register latches the B1TCM Address where the Address Parity Error occurred in R5SS1 CORE1.

Return to [Summary Table](#)

**Table 2-603. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8178h       |

**Figure 2-201. MSS\_CTRL\_ERR\_PARITY\_B1TCM1\_R5SS1 Name Register**

|                              |    |    |    |                              |    |    |    |
|------------------------------|----|----|----|------------------------------|----|----|----|
| 31                           | 30 | 29 | 28 | 27                           | 26 | 25 | 24 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 23                           | 22 | 21 | 20 | 19                           | 18 | 17 | 16 |
| RESERVED                     |    |    |    | ERR_PARITY_B1TCM1_R5SS1_ADDR |    |    |    |
| NONE                         |    |    |    | R                            |    |    |    |
| 0h                           |    |    |    | 0h                           |    |    |    |
| 15                           | 14 | 13 | 12 | 11                           | 10 | 9  | 8  |
| ERR_PARITY_B1TCM1_R5SS1_ADDR |    |    |    |                              |    |    |    |
| R                            |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 7                            | 6  | 5  | 4  | 3                            | 2  | 1  | 0  |
| ERR_PARITY_B1TCM1_R5SS1_ADDR |    |    |    |                              |    |    |    |
| R                            |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |

**Table 2-605. MSS\_CTRL\_ERR\_PARITY\_B1TCM1\_R5SS1 Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                     |
|-------|------------------------------|------|-------|-----------------------------------------------------------------|
| 31:20 | RESERVED                     | NONE | 0h    | Reserved                                                        |
| 19:0  | ERR_PARITY_B1TCM1_R5SS1_ADDR | R    | 0h    | Address latched when parity error is occurred for B1TCM of CR5B |

### 2.2.2.202 MSS\_CTRL\_TCM1\_PARITY\_ERRFRC Register

#### 1 MSS\_CTRL\_TCM1\_PARITY\_ERRFRC Register (Offset = 1817Ch) [reset = 0h]

This register is used to Inject fault in the TCM Address Parity Error detection logic of R5SS1 .

Return to [Summary Table](#)

**Table 2-606. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 817Ch       |

**Figure 2-202. MSS\_CTRL\_TCM1\_PARITY\_ERRFRC Name Register**

|          |                           |    |    |          |                           |    |    |
|----------|---------------------------|----|----|----------|---------------------------|----|----|
| 31       | 30                        | 29 | 28 | 27       | 26                        | 25 | 24 |
| RESERVED |                           |    |    |          |                           |    |    |
| NONE     |                           |    |    |          |                           |    |    |
| 0h       |                           |    |    |          |                           |    |    |
| 23       | 22                        | 21 | 20 | 19       | 18                        | 17 | 16 |
| RESERVED | TCM1_PARITY_ERRFRC_B1TCM1 |    |    | RESERVED | TCM1_PARITY_ERRFRC_B1TCM0 |    |    |
| NONE     | R/W                       |    |    | NONE     | R/W                       |    |    |
| 0h       | 0h                        |    |    | 0h       | 0h                        |    |    |
| 15       | 14                        | 13 | 12 | 11       | 10                        | 9  | 8  |
| RESERVED | TCM1_PARITY_ERRFRC_B0TCM1 |    |    | RESERVED | TCM1_PARITY_ERRFRC_B0TCM0 |    |    |
| NONE     | R/W                       |    |    | NONE     | R/W                       |    |    |
| 0h       | 0h                        |    |    | 0h       | 0h                        |    |    |
| 7        | 6                         | 5  | 4  | 3        | 2                         | 1  | 0  |
| RESERVED | TCM1_PARITY_ERRFRC_ATCM1  |    |    | RESERVED | TCM1_PARITY_ERRFRC_ATCM0  |    |    |
| NONE     | R/W                       |    |    | NONE     | R/W                       |    |    |
| 0h       | 0h                        |    |    | 0h       | 0h                        |    |    |

**Table 2-608. MSS\_CTRL\_TCM1\_PARITY\_ERRFRC Register Field Descriptions**

| Bit   | Field                     | Type | Reset | Description                                                                      |
|-------|---------------------------|------|-------|----------------------------------------------------------------------------------|
| 31:23 | RESERVED                  | NONE | 0h    | Reserved                                                                         |
| 22:20 | TCM1_PARITY_ERRFRC_B1TCM1 | R/W  | 0h    | Write pulse bit field:<br>Writing 3'b111 forces a parity error for B1TCM of CR5B |
| 19    | RESERVED                  | NONE | 0h    | Reserved                                                                         |
| 18:16 | TCM1_PARITY_ERRFRC_B1TCM0 | R/W  | 0h    | Write pulse bit field:<br>Writing 3'b111 forces a parity error for B1TCM of CR5A |
| 15    | RESERVED                  | NONE | 0h    | Reserved                                                                         |
| 14:12 | TCM1_PARITY_ERRFRC_B0TCM1 | R/W  | 0h    | Write pulse bit field:<br>Writing 3'b111 forces a parity error for B0TCM of CR5B |
| 11    | RESERVED                  | NONE | 0h    | Reserved                                                                         |
| 10:8  | TCM1_PARITY_ERRFRC_B0TCM0 | R/W  | 0h    | Write pulse bit field:<br>Writing 3'b111 forces a parity error for B0TCM of CR5A |
| 7     | RESERVED                  | NONE | 0h    | Reserved                                                                         |
| 6:4   | TCM1_PARITY_ERRFRC_ATCM1  | R/W  | 0h    | Write pulse bit field:<br>Writing 3'b111 forces a parity error for ATCM of CR5B  |
| 3     | RESERVED                  | NONE | 0h    | Reserved                                                                         |
| 2:0   | TCM1_PARITY_ERRFRC_ATCM0  | R/W  | 0h    | Write pulse bit field:<br>Writing 3'b111 forces a parity error for ATCM of CR5A  |

### 2.2.2.203 MSS\_CTRL\_TPCC\_PARITY\_CTRL Register

#### 1 MSS\_CTRL\_TPCC\_PARITY\_CTRL Register (Offset = 18180h) [reset = 0h]

This register Controls the Parity Error detection logic of EDMA TPCC0 Memories.

Return to [Summary Table](#)

**Table 2-609. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8180h       |

**Figure 2-203. MSS\_CTRL\_TPCC\_PARITY\_CTRL Name Register**

|          |    |    |                                       |          |    |    |                                        |
|----------|----|----|---------------------------------------|----------|----|----|----------------------------------------|
| 31       | 30 | 29 | 28                                    | 27       | 26 | 25 | 24                                     |
| RESERVED |    |    |                                       |          |    |    |                                        |
| NONE     |    |    |                                       |          |    |    |                                        |
| 0h       |    |    |                                       |          |    |    |                                        |
| 23       | 22 | 21 | 20                                    | 19       | 18 | 17 | 16                                     |
| RESERVED |    |    |                                       |          |    |    | TPCC_PARITY_CTRL_TPCC_A_PARITY_ERR_CLR |
| NONE     |    |    |                                       |          |    |    | R/W                                    |
| 0h       |    |    |                                       |          |    |    | 0h                                     |
| 15       | 14 | 13 | 12                                    | 11       | 10 | 9  | 8                                      |
| RESERVED |    |    |                                       |          |    |    |                                        |
| NONE     |    |    |                                       |          |    |    |                                        |
| 0h       |    |    |                                       |          |    |    |                                        |
| 7        | 6  | 5  | 4                                     | 3        | 2  | 1  | 0                                      |
| RESERVED |    |    | TPCC_PARITY_CTRL_TPCC_A_PARITY_TESTEN | RESERVED |    |    | TPCC_PARITY_CTRL_TPCC_A_PARITY_EN      |
| NONE     |    |    | R/W                                   | NONE     |    |    | R/W                                    |
| 0h       |    |    | 0h                                    | 0h       |    |    | 0h                                     |

**Table 2-611. MSS\_CTRL\_TPCC\_PARITY\_CTRL Register Field Descriptions**

| Bit   | Field                                  | Type | Reset | Description                                                                             |
|-------|----------------------------------------|------|-------|-----------------------------------------------------------------------------------------|
| 31:17 | RESERVED                               | NONE | 0h    | Reserved                                                                                |
| 16    | TPCC_PARITY_CTRL_TPCC_A_PARITY_ERR_CLR | R/W  | 0h    | Write pulse bit field: parity clear bit. Writing 1'b1 will clear the tpcc_a_parity_addr |
| 15:5  | RESERVED                               | NONE | 0h    | Reserved                                                                                |
| 4     | TPCC_PARITY_CTRL_TPCC_A_PARITY_TESTEN  | R/W  | 0h    | parity test enable for tpcc a                                                           |
| 3:1   | RESERVED                               | NONE | 0h    | Reserved                                                                                |
| 0     | TPCC_PARITY_CTRL_TPCC_A_PARITY_EN      | R/W  | 0h    | Writing 1'b1 enables parity for TPCC_A                                                  |

### 2.2.2.204 MSS\_CTRL\_TPCC\_PARITY\_STATUS Register

#### 1 MSS\_CTRL\_TPCC\_PARITY\_STATUS Register (Offset = 18184h) [reset = 0h]

This register indicates the Address where the Parity Error occurred in TPCC0 Memory.

Return to [Summary Table](#)

**Table 2-612. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8184h       |

**Figure 2-204. MSS\_CTRL\_TPCC\_PARITY\_STATUS Name Register**

|                                       |    |    |    |    |    |    |                                           |
|---------------------------------------|----|----|----|----|----|----|-------------------------------------------|
| 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24                                        |
| RESERVED                              |    |    |    |    |    |    |                                           |
| NONE                                  |    |    |    |    |    |    |                                           |
| 0h                                    |    |    |    |    |    |    |                                           |
| 23                                    | 22 | 21 | 20 | 19 | 18 | 17 | 16                                        |
| RESERVED                              |    |    |    |    |    |    |                                           |
| NONE                                  |    |    |    |    |    |    |                                           |
| 0h                                    |    |    |    |    |    |    |                                           |
| 15                                    | 14 | 13 | 12 | 11 | 10 | 9  | 8                                         |
| RESERVED                              |    |    |    |    |    |    | TPCC_PARITY_STATUS_TPC<br>C_A_PARITY_ADDR |
| NONE                                  |    |    |    |    |    |    | R                                         |
| 0h                                    |    |    |    |    |    |    | 0h                                        |
| 7                                     | 6  | 5  | 4  | 3  | 2  | 1  | 0                                         |
| TPCC_PARITY_STATUS_TPCC_A_PARITY_ADDR |    |    |    |    |    |    |                                           |
| R                                     |    |    |    |    |    |    |                                           |
| 0h                                    |    |    |    |    |    |    |                                           |

**Table 2-614. MSS\_CTRL\_TPCC\_PARITY\_STATUS Register Field Descriptions**

| Bit  | Field                                 | Type | Reset | Description                                   |
|------|---------------------------------------|------|-------|-----------------------------------------------|
| 31:9 | RESERVED                              | NONE | 0h    | Reserved                                      |
| 8:0  | TPCC_PARITY_STATUS_TPCC_A_PARITY_ADDR | R    | 0h    | Address where parity error happened for tpcca |



### 2.2.2.205 MSS\_CTRL\_MSS\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_BUS\_SAFETY\_CTRL Register (Offset = 18200h) [reset = 0h]

This register is used to Globally enable Interconnect Safety.

Return to [Summary Table](#)

**Table 2-615. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8200h       |

**Figure 2-205. MSS\_CTRL\_MSS\_BUS\_SAFETY\_CTRL Name Register**

|          |    |    |    |    |                            |    |    |
|----------|----|----|----|----|----------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                         | 25 | 24 |
| RESERVED |    |    |    |    |                            |    |    |
| NONE     |    |    |    |    |                            |    |    |
| 0h       |    |    |    |    |                            |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                         | 17 | 16 |
| RESERVED |    |    |    |    |                            |    |    |
| NONE     |    |    |    |    |                            |    |    |
| 0h       |    |    |    |    |                            |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                         | 9  | 8  |
| RESERVED |    |    |    |    |                            |    |    |
| NONE     |    |    |    |    |                            |    |    |
| 0h       |    |    |    |    |                            |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                          | 1  | 0  |
| RESERVED |    |    |    |    | MSS_BUS_SAFETY_CTRL_ENABLE |    |    |
| NONE     |    |    |    |    | R/W                        |    |    |
| 0h       |    |    |    |    | 0h                         |    |    |

**Table 2-617. MSS\_CTRL\_MSS\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit  | Field                      | Type | Reset | Description                                                                                                                           |
|------|----------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                   | NONE | 0h    | Reserved                                                                                                                              |
| 2:0  | MSS_BUS_SAFETY_CTRL_ENABLE | R/W  | 0h    | Set this bit to 3'b111 to Globally enable Interconnect Safety.<br>Set this bit to 3'b000 to globally disable the Interconnect safety. |

### 2.2.2.206 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_RD\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_RD\_BUS\_SAFETY\_CTRL Register (Offset = 18220h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS0 CORE0 AXI RD Initiator Port.

Return to [Summary Table](#)

**Table 2-618. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8220h       |

**Figure 2-206. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_RD\_BUS\_SAFETY\_CTRL Name Register**

|                                       |    |    |    |    |                                         |    |                                            |
|---------------------------------------|----|----|----|----|-----------------------------------------|----|--------------------------------------------|
| 31                                    | 30 | 29 | 28 | 27 | 26                                      | 25 | 24                                         |
| RESERVED                              |    |    |    |    |                                         |    |                                            |
| NONE                                  |    |    |    |    |                                         |    |                                            |
| 0h                                    |    |    |    |    |                                         |    |                                            |
| 23                                    | 22 | 21 | 20 | 19 | 18                                      | 17 | 16                                         |
| MSS_CR5A0_AXI_RD_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                         |    |                                            |
| R                                     |    |    |    |    |                                         |    |                                            |
| 0h                                    |    |    |    |    |                                         |    |                                            |
| 15                                    | 14 | 13 | 12 | 11 | 10                                      | 9  | 8                                          |
| RESERVED                              |    |    |    |    |                                         |    | MSS_CR5A0_AXI_RD_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                                  |    |    |    |    |                                         |    | R/W                                        |
| 0h                                    |    |    |    |    |                                         |    | 0h                                         |
| 7                                     | 6  | 5  | 4  | 3  | 2                                       | 1  | 0                                          |
| RESERVED                              |    |    |    |    | MSS_CR5A0_AXI_RD_BUS_SAFETY_CTRL_ENABLE |    |                                            |
| NONE                                  |    |    |    |    | R/W                                     |    |                                            |
| 0h                                    |    |    |    |    | 7h                                      |    |                                            |

**Table 2-620. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_RD\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|--------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                                   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | MSS_CR5A0_AXI_RD_BUS_SAFETY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                                   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | MSS_CR5A0_AXI_RD_BUS_SAFETY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

**Table 2-620. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_RD\_BUS\_SAFETY\_CTRL Register Field Descriptions  
(continued)**

| Bit | Field                                           | Type | Reset | Description                                                                                                                                           |
|-----|-------------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:3 | RESERVED                                        | NONE | 0h    | Reserved                                                                                                                                              |
| 2:0 | MSS_CR5A0_AXI_RD_B<br>US_SAFETY_CTRL_ENA<br>BLE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.207 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_RD\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_RD\_BUS\_SAFETY\_FI Register (Offset = 18224h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of R5SS0 CORE0 AXI RD Initiator Port.

Return to [Summary Table](#)

**Table 2-621. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8224h       |

**Figure 2-207. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_RD\_BUS\_SAFETY\_FI Name Register**

| 31                                  | 30                                  | 29                                | 28                                | 27                                | 26                                | 25                                | 24                                |
|-------------------------------------|-------------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|
| MSS_CR5A0_AXI_RD_BUS_SAFETY_FI_SAFE |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| R/W                                 |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 0h                                  |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 23                                  | 22                                  | 21                                | 20                                | 19                                | 18                                | 17                                | 16                                |
| MSS_CR5A0_AXI_RD_BUS_SAFETY_FI_MAIN |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| R/W                                 |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 0h                                  |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 15                                  | 14                                  | 13                                | 12                                | 11                                | 10                                | 9                                 | 8                                 |
| MSS_CR5A0_AXI_RD_BUS_SAFETY_FI_DATA |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| R/W                                 |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 0h                                  |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 7                                   | 6                                   | 5                                 | 4                                 | 3                                 | 2                                 | 1                                 | 0                                 |
| RESERVED                            | MSS_CR5A0_AXI_RD_BUS_SAFETY_FI_DATA | MSS_CR5A0_AXI_RD_BUS_SAFETY_FI_SE | MSS_CR5A0_AXI_RD_BUS_SAFETY_FI_GL | MSS_CR5A0_AXI_RD_BUS_SAFETY_FI_GL | MSS_CR5A0_AXI_RD_BUS_SAFETY_FI_GL | MSS_CR5A0_AXI_RD_BUS_SAFETY_FI_GL | MSS_CR5A0_AXI_RD_BUS_SAFETY_FI_GL |
| NONE                                | R/W                                 | R/W                               | R/W                               | R/W                               | R/W                               | R/W                               | R/W                               |
| 0h                                  | 0h                                  | 0h                                | 0h                                | 0h                                | 0h                                | 0h                                | 0h                                |

**Table 2-623. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_RD\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5A0_AXI_RD_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_CR5A0_AXI_RD_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_CR5A0_AXI_RD_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |

**Table 2-623. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_RD\_BUS\_SAFETY\_FI Register Field Descriptions  
(continued)**

| Bit | Field                                                  | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|--------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | MSS_CR5A0_AXI_RD_B<br>US_SAFETY_FI_DED                 | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                             |
| 4   | MSS_CR5A0_AXI_RD_B<br>US_SAFETY_FI_SEC                 | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_CR5A0_AXI_RD_B<br>US_SAFETY_FI_GLOBAL<br>_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_CR5A0_AXI_RD_B<br>US_SAFETY_FI_GLOBAL<br>_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_CR5A0_AXI_RD_B<br>US_SAFETY_FI_GLOBAL<br>_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_CR5A0_AXI_RD_B<br>US_SAFETY_FI_GLOBAL<br>_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

### 2.2.2.208 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR Register (Offset = 18228h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of R5SS0 CORE0 AXI RD Initiator port.

Return to [Summary Table](#)

**Table 2-624. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8228h       |

**Figure 2-208. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR Name Register**

|                                            |    |    |    |    |    |    |    |
|--------------------------------------------|----|----|----|----|----|----|----|
| 31                                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A0_AXI_RD_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 23                                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A0_AXI_RD_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 15                                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A0_AXI_RD_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 7                                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A0_AXI_RD_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |

**Table 2-626. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                                              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5A0_AXI_RD_B<br>US_SAFETY_ERR_DED            | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_CR5A0_AXI_RD_B<br>US_SAFETY_ERR_SEC            | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_CR5A0_AXI_RD_B<br>US_SAFETY_ERR_COM<br>P_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-626. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR Register Field Descriptions (continued)**

| Bit | Field                                            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|--------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_CR5A0_AXI_RD_B<br>US_SAFETY_ERR_COM<br>P_ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.209 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 1822Ch) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS0 CORE0 AXI RD Initiator Port.

Return to [Summary Table](#)

**Table 2-627. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 822Ch       |

**Figure 2-209. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                               |    |    |    |    |    |    |    |
|-----------------------------------------------|----|----|----|----|----|----|----|
| 31                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                                      |    |    |    |    |    |    |    |
| NONE                                          |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 23                                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                                      |    |    |    |    |    |    |    |
| NONE                                          |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 15                                            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 7                                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |

**Table 2-629. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                                 | Type | Reset | Description                                                                                                                                                |
|-------|-------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                                              | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_CR5A0_AXI_RD_B<br>US_SAFETY_ERR_STAT<br>_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_CR5A0_AXI_RD_B<br>US_SAFETY_ERR_STAT<br>_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |



### 2.2.2.210 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 18230h) [reset = 0h]

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS0 CORE0 AXI RD Initiator Port.

Return to [Summary Table](#)

**Table 2-630. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8230h       |

**Figure 2-210. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                               |    |    |    |    |    |    |    |
|-----------------------------------------------|----|----|----|----|----|----|----|
| 31                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 23                                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 15                                            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 7                                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |

**Table 2-632. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                                 | Type | Reset | Description                                                                                                                       |
|------|-------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5A0_AXI_RD_B<br>US_SAFETY_ERR_STAT<br>_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.211 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Register (Offset = 18234h) [reset = 0h]

This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of R5SS0 CORE0 AXI RD Initiator Port.

Return to [Summary Table](#)

**Table 2-633. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8234h       |

**Figure 2-211. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Name Register**

|                                                |    |    |    |    |    |    |    |
|------------------------------------------------|----|----|----|----|----|----|----|
| 31                                             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A0_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |
| 23                                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A0_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |
| 15                                             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A0_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |
| 7                                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A0_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |

**Table 2-635. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Register Field Descriptions**

| Bit  | Field                                                  | Type | Reset | Description                                                                                                                     |
|------|--------------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5A0_AXI_RD_B<br>US_SAFETY_ERR_STAT<br>_READ_STAT | R    | 0h    | Read this bitfield for comapartor status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus. |

### 2.2.2.212 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_RD\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_RD\_BUS\_SAFETY\_CTRL Register (Offset = 18240h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS0 CORE1 AXI RD Initiator Port.

Return to [Summary Table](#)

**Table 2-636. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8240h       |

**Figure 2-212. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_RD\_BUS\_SAFETY\_CTRL Name Register**

|                                       |    |    |    |    |                                         |    |                                            |
|---------------------------------------|----|----|----|----|-----------------------------------------|----|--------------------------------------------|
| 31                                    | 30 | 29 | 28 | 27 | 26                                      | 25 | 24                                         |
| RESERVED                              |    |    |    |    |                                         |    |                                            |
| NONE                                  |    |    |    |    |                                         |    |                                            |
| 0h                                    |    |    |    |    |                                         |    |                                            |
| 23                                    | 22 | 21 | 20 | 19 | 18                                      | 17 | 16                                         |
| MSS_CR5B0_AXI_RD_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                         |    |                                            |
| R                                     |    |    |    |    |                                         |    |                                            |
| 0h                                    |    |    |    |    |                                         |    |                                            |
| 15                                    | 14 | 13 | 12 | 11 | 10                                      | 9  | 8                                          |
| RESERVED                              |    |    |    |    |                                         |    | MSS_CR5B0_AXI_RD_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                                  |    |    |    |    |                                         |    | R/W                                        |
| 0h                                    |    |    |    |    |                                         |    | 0h                                         |
| 7                                     | 6  | 5  | 4  | 3  | 2                                       | 1  | 0                                          |
| RESERVED                              |    |    |    |    | MSS_CR5B0_AXI_RD_BUS_SAFETY_CTRL_ENABLE |    |                                            |
| NONE                                  |    |    |    |    | R/W                                     |    |                                            |
| 0h                                    |    |    |    |    | 7h                                      |    |                                            |

**Table 2-638. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_RD\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|--------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                                   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | MSS_CR5B0_AXI_RD_BUS_SAFETY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                                   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | MSS_CR5B0_AXI_RD_BUS_SAFETY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

**Table 2-638. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_RD\_BUS\_SAFETY\_CTRL Register Field Descriptions  
(continued)**

| Bit | Field                                           | Type | Reset | Description                                                                                                                                           |
|-----|-------------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:3 | RESERVED                                        | NONE | 0h    | Reserved                                                                                                                                              |
| 2:0 | MSS_CR5B0_AXI_RD_B<br>US_SAFETY_CTRL_ENA<br>BLE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.213 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_RD\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_RD\_BUS\_SAFETY\_FI Register (Offset = 18244h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of R5SS0 CORE1 AXI RD Initiator Port.

Return to [Summary Table](#)

**Table 2-639. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8244h       |

**Figure 2-213. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_RD\_BUS\_SAFETY\_FI Name Register**

| 31                                  | 30                                  | 29                                | 28                                | 27                                | 26                                | 25                                | 24                                |
|-------------------------------------|-------------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|
| MSS_CR5B0_AXI_RD_BUS_SAFETY_FI_SAFE |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| R/W                                 |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 0h                                  |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 23                                  | 22                                  | 21                                | 20                                | 19                                | 18                                | 17                                | 16                                |
| MSS_CR5B0_AXI_RD_BUS_SAFETY_FI_MAIN |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| R/W                                 |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 0h                                  |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 15                                  | 14                                  | 13                                | 12                                | 11                                | 10                                | 9                                 | 8                                 |
| MSS_CR5B0_AXI_RD_BUS_SAFETY_FI_DATA |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| R/W                                 |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 0h                                  |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 7                                   | 6                                   | 5                                 | 4                                 | 3                                 | 2                                 | 1                                 | 0                                 |
| RESERVED                            | MSS_CR5B0_AXI_RD_BUS_SAFETY_FI_DATA | MSS_CR5B0_AXI_RD_BUS_SAFETY_FI_SE | MSS_CR5B0_AXI_RD_BUS_SAFETY_FI_GL | MSS_CR5B0_AXI_RD_BUS_SAFETY_FI_GL | MSS_CR5B0_AXI_RD_BUS_SAFETY_FI_GL | MSS_CR5B0_AXI_RD_BUS_SAFETY_FI_GL | MSS_CR5B0_AXI_RD_BUS_SAFETY_FI_GL |
| NONE                                | R/W                                 | R/W                               | R/W                               | R/W                               | R/W                               | R/W                               | R/W                               |
| 0h                                  | 0h                                  | 0h                                | 0h                                | 0h                                | 0h                                | 0h                                | 0h                                |

**Table 2-641. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_RD\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5B0_AXI_RD_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_CR5B0_AXI_RD_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_CR5B0_AXI_RD_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |

**Table 2-641. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_RD\_BUS\_SAFETY\_FI Register Field Descriptions  
(continued)**

| Bit | Field                                                  | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|--------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | MSS_CR5B0_AXI_RD_B<br>US_SAFETY_FI_DED                 | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                             |
| 4   | MSS_CR5B0_AXI_RD_B<br>US_SAFETY_FI_SEC                 | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_CR5B0_AXI_RD_B<br>US_SAFETY_FI_GLOBAL<br>_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_CR5B0_AXI_RD_B<br>US_SAFETY_FI_GLOBAL<br>_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_CR5B0_AXI_RD_B<br>US_SAFETY_FI_GLOBAL<br>_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_CR5B0_AXI_RD_B<br>US_SAFETY_FI_GLOBAL<br>_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

### 2.2.2.214 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR Register (Offset = 18248h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of R5SS0 CORE1 AXI RD Initiator port.

Return to [Summary Table](#)

**Table 2-642. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8248h       |

**Figure 2-214. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR Name Register**

|                                            |    |    |    |    |    |    |    |
|--------------------------------------------|----|----|----|----|----|----|----|
| 31                                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B0_AXI_RD_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 23                                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B0_AXI_RD_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 15                                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B0_AXI_RD_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 7                                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B0_AXI_RD_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |

**Table 2-644. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                                              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5B0_AXI_RD_B<br>US_SAFETY_ERR_DED            | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_CR5B0_AXI_RD_B<br>US_SAFETY_ERR_SEC            | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_CR5B0_AXI_RD_B<br>US_SAFETY_ERR_COM<br>P_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-644. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR Register Field Descriptions (continued)**

| Bit | Field                                            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|--------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_CR5B0_AXI_RD_B<br>US_SAFETY_ERR_COM<br>P_ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |



### 2.2.2.215 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 1824Ch) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS0 CORE1 AXI RD Initiator Port.

Return to [Summary Table](#)

**Table 2-645. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 824Ch       |

**Figure 2-215. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                               |    |    |    |    |    |    |    |
|-----------------------------------------------|----|----|----|----|----|----|----|
| 31                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                                      |    |    |    |    |    |    |    |
| NONE                                          |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 23                                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                                      |    |    |    |    |    |    |    |
| NONE                                          |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 15                                            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 7                                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B0_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |

**Table 2-647. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                                 | Type | Reset | Description                                                                                                                                                |
|-------|-------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                                              | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_CR5B0_AXI_RD_B<br>US_SAFETY_ERR_STAT<br>_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_CR5B0_AXI_RD_B<br>US_SAFETY_ERR_STAT<br>_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.216 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 18250h) [reset = 0h]

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS0 CORE1 AXI RD Initiator Port.

Return to [Summary Table](#)

**Table 2-648. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8250h       |

**Figure 2-216. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                               |    |    |    |    |    |    |    |
|-----------------------------------------------|----|----|----|----|----|----|----|
| 31                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 23                                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 15                                            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 7                                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B0_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |

**Table 2-650. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                                 | Type | Reset | Description                                                                                                                       |
|------|-------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5B0_AXI_RD_B<br>US_SAFETY_ERR_STAT<br>_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.217 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Register (Offset = 18254h) [reset = 0h]

This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of R5SS0 CORE1 AXI RD Initiator Port.

Return to [Summary Table](#)

**Table 2-651. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8254h       |

**Figure 2-217. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Name Register**

|                                                |    |    |    |    |    |    |    |
|------------------------------------------------|----|----|----|----|----|----|----|
| 31                                             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B0_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |
| 23                                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B0_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |
| 15                                             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B0_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |
| 7                                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B0_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |

**Table 2-653. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Register Field Descriptions**

| Bit  | Field                                                  | Type | Reset | Description                                                                                                                     |
|------|--------------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5B0_AXI_RD_B<br>US_SAFETY_ERR_STAT<br>_READ_STAT | R    | 0h    | Read this bitfield for comapartor status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus. |

### 2.2.2.218 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_RD\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_RD\_BUS\_SAFETY\_CTRL Register (Offset = 18260h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS1 CORE0 AXI RD Initiator Port.

Return to [Summary Table](#)

**Table 2-654. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8260h       |

**Figure 2-218. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_RD\_BUS\_SAFETY\_CTRL Name Register**

|                                       |    |    |    |    |                                         |    |                                            |
|---------------------------------------|----|----|----|----|-----------------------------------------|----|--------------------------------------------|
| 31                                    | 30 | 29 | 28 | 27 | 26                                      | 25 | 24                                         |
| RESERVED                              |    |    |    |    |                                         |    |                                            |
| NONE                                  |    |    |    |    |                                         |    |                                            |
| 0h                                    |    |    |    |    |                                         |    |                                            |
| 23                                    | 22 | 21 | 20 | 19 | 18                                      | 17 | 16                                         |
| MSS_CR5A1_AXI_RD_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                         |    |                                            |
| R                                     |    |    |    |    |                                         |    |                                            |
| 0h                                    |    |    |    |    |                                         |    |                                            |
| 15                                    | 14 | 13 | 12 | 11 | 10                                      | 9  | 8                                          |
| RESERVED                              |    |    |    |    |                                         |    | MSS_CR5A1_AXI_RD_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                                  |    |    |    |    |                                         |    | R/W                                        |
| 0h                                    |    |    |    |    |                                         |    | 0h                                         |
| 7                                     | 6  | 5  | 4  | 3  | 2                                       | 1  | 0                                          |
| RESERVED                              |    |    |    |    | MSS_CR5A1_AXI_RD_BUS_SAFETY_CTRL_ENABLE |    |                                            |
| NONE                                  |    |    |    |    | R/W                                     |    |                                            |
| 0h                                    |    |    |    |    | 7h                                      |    |                                            |

**Table 2-656. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_RD\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                 | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|---------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                              | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | MSS_CR5A1_AXI_RD_BUS_SAFETY_CTRL_TYPE | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                              | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

**Table 2-656. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_RD\_BUS\_SAFETY\_CTRL Register Field Descriptions (continued)**

| Bit | Field                                              | Type | Reset | Description                                                                                                                                           |
|-----|----------------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8   | MSS_CR5A1_AXI_RD_B<br>US_SAFETY_CTRL_ERR<br>_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                          |
| 7:3 | RESERVED                                           | NONE | 0h    | Reserved                                                                                                                                              |
| 2:0 | MSS_CR5A1_AXI_RD_B<br>US_SAFETY_CTRL_ENA<br>BLE    | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.219 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_RD\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_RD\_BUS\_SAFETY\_FI Register (Offset = 18264h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of R5SS1 CORE0 AXI RD Initiator Port.

Return to [Summary Table](#)

**Table 2-657. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8264h       |

**Figure 2-219. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_RD\_BUS\_SAFETY\_FI Name Register**

| 31                                  | 30                                  | 29                                | 28                                | 27                                | 26                                | 25                                | 24                                |
|-------------------------------------|-------------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|
| MSS_CR5A1_AXI_RD_BUS_SAFETY_FI_SAFE |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| R/W                                 |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 0h                                  |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 23                                  | 22                                  | 21                                | 20                                | 19                                | 18                                | 17                                | 16                                |
| MSS_CR5A1_AXI_RD_BUS_SAFETY_FI_MAIN |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| R/W                                 |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 0h                                  |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 15                                  | 14                                  | 13                                | 12                                | 11                                | 10                                | 9                                 | 8                                 |
| MSS_CR5A1_AXI_RD_BUS_SAFETY_FI_DATA |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| R/W                                 |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 0h                                  |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 7                                   | 6                                   | 5                                 | 4                                 | 3                                 | 2                                 | 1                                 | 0                                 |
| RESERVED                            | MSS_CR5A1_AXI_RD_BUS_SAFETY_FI_DATA | MSS_CR5A1_AXI_RD_BUS_SAFETY_FI_SE | MSS_CR5A1_AXI_RD_BUS_SAFETY_FI_GL | MSS_CR5A1_AXI_RD_BUS_SAFETY_FI_GL | MSS_CR5A1_AXI_RD_BUS_SAFETY_FI_GL | MSS_CR5A1_AXI_RD_BUS_SAFETY_FI_GL | MSS_CR5A1_AXI_RD_BUS_SAFETY_FI_GL |
| NONE                                | R/W                                 | R/W                               | R/W                               | R/W                               | R/W                               | R/W                               | R/W                               |
| 0h                                  | 0h                                  | 0h                                | 0h                                | 0h                                | 0h                                | 0h                                | 0h                                |

**Table 2-659. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_RD\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5A1_AXI_RD_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_CR5A1_AXI_RD_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_CR5A1_AXI_RD_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |

**Table 2-659. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_RD\_BUS\_SAFETY\_FI Register Field Descriptions  
(continued)**

| Bit | Field                                                  | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|--------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | MSS_CR5A1_AXI_RD_B<br>US_SAFETY_FI_DED                 | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                             |
| 4   | MSS_CR5A1_AXI_RD_B<br>US_SAFETY_FI_SEC                 | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_CR5A1_AXI_RD_B<br>US_SAFETY_FI_GLOBAL<br>_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_CR5A1_AXI_RD_B<br>US_SAFETY_FI_GLOBAL<br>_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_CR5A1_AXI_RD_B<br>US_SAFETY_FI_GLOBAL<br>_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_CR5A1_AXI_RD_B<br>US_SAFETY_FI_GLOBAL<br>_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

### 2.2.2.220 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR Register (Offset = 18268h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of R5SS1 CORE0 AXI RD Initiator port.

Return to [Summary Table](#)

**Table 2-660. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8268h       |

**Figure 2-220. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR Name Register**

|                                            |    |    |    |    |    |    |    |
|--------------------------------------------|----|----|----|----|----|----|----|
| 31                                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A1_AXI_RD_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 23                                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A1_AXI_RD_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 15                                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A1_AXI_RD_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 7                                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A1_AXI_RD_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |

**Table 2-662. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                                              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5A1_AXI_RD_B<br>US_SAFETY_ERR_DED            | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_CR5A1_AXI_RD_B<br>US_SAFETY_ERR_SEC            | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_CR5A1_AXI_RD_B<br>US_SAFETY_ERR_COM<br>P_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |



**Table 2-662. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR Register Field Descriptions  
(continued)**

| Bit | Field                                            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|--------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_CR5A1_AXI_RD_B<br>US_SAFETY_ERR_COM<br>P_ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.221 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 1826Ch) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS1 CORE0 AXI RD Initiator Port.

Return to [Summary Table](#)

**Table 2-663. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 826Ch       |

**Figure 2-221. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                               |    |    |    |    |    |    |    |
|-----------------------------------------------|----|----|----|----|----|----|----|
| 31                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                                      |    |    |    |    |    |    |    |
| NONE                                          |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 23                                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                                      |    |    |    |    |    |    |    |
| NONE                                          |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 15                                            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A1_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 7                                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A1_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |

**Table 2-665. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                                 | Type | Reset | Description                                                                                                                                                |
|-------|-------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                                              | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_CR5A1_AXI_RD_B<br>US_SAFETY_ERR_STAT<br>_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_CR5A1_AXI_RD_B<br>US_SAFETY_ERR_STAT<br>_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.222 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 18270h) [reset = 0h]

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS1 CORE0 AXI RD Initiator Port.

Return to [Summary Table](#)

**Table 2-666. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8270h       |

**Figure 2-222. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                               |    |    |    |    |    |    |    |
|-----------------------------------------------|----|----|----|----|----|----|----|
| 31                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A1_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 23                                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A1_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 15                                            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A1_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 7                                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A1_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |

**Table 2-668. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                                 | Type | Reset | Description                                                                                                                       |
|------|-------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5A1_AXI_RD_B<br>US_SAFETY_ERR_STAT<br>_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.223 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Register (Offset = 18274h) [reset = 0h]

This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of R5SS1 CORE0 AXI RD Initiator Port.

Return to [Summary Table](#)

**Table 2-669. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8274h       |

**Figure 2-223. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Name Register**

|                                                |    |    |    |    |    |    |    |
|------------------------------------------------|----|----|----|----|----|----|----|
| 31                                             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A1_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |
| 23                                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A1_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |
| 15                                             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A1_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |
| 7                                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A1_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |

**Table 2-671. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Register Field Descriptions**

| Bit  | Field                                                  | Type | Reset | Description                                                                                                                     |
|------|--------------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5A1_AXI_RD_B<br>US_SAFETY_ERR_STAT<br>_READ_STAT | R    | 0h    | Read this bitfield for comapartor status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus. |

### 2.2.2.224 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_RD\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_RD\_BUS\_SAFETY\_CTRL Register (Offset = 18280h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS1 CORE1 AXI RD Initiator Port.

Return to [Summary Table](#)

**Table 2-672. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8280h       |

**Figure 2-224. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_RD\_BUS\_SAFETY\_CTRL Name Register**

|                                       |    |    |    |    |                                         |    |                                            |
|---------------------------------------|----|----|----|----|-----------------------------------------|----|--------------------------------------------|
| 31                                    | 30 | 29 | 28 | 27 | 26                                      | 25 | 24                                         |
| RESERVED                              |    |    |    |    |                                         |    |                                            |
| NONE                                  |    |    |    |    |                                         |    |                                            |
| 0h                                    |    |    |    |    |                                         |    |                                            |
| 23                                    | 22 | 21 | 20 | 19 | 18                                      | 17 | 16                                         |
| MSS_CR5B1_AXI_RD_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                         |    |                                            |
| R                                     |    |    |    |    |                                         |    |                                            |
| 0h                                    |    |    |    |    |                                         |    |                                            |
| 15                                    | 14 | 13 | 12 | 11 | 10                                      | 9  | 8                                          |
| RESERVED                              |    |    |    |    |                                         |    | MSS_CR5B1_AXI_RD_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                                  |    |    |    |    |                                         |    | R/W                                        |
| 0h                                    |    |    |    |    |                                         |    | 0h                                         |
| 7                                     | 6  | 5  | 4  | 3  | 2                                       | 1  | 0                                          |
| RESERVED                              |    |    |    |    | MSS_CR5B1_AXI_RD_BUS_SAFETY_CTRL_ENABLE |    |                                            |
| NONE                                  |    |    |    |    | R/W                                     |    |                                            |
| 0h                                    |    |    |    |    | 7h                                      |    |                                            |

**Table 2-674. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_RD\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                 | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|---------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                              | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | MSS_CR5B1_AXI_RD_BUS_SAFETY_CTRL_TYPE | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                              | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

**Table 2-674. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_RD\_BUS\_SAFETY\_CTRL Register Field Descriptions (continued)**

| Bit | Field                                              | Type | Reset | Description                                                                                                                                           |
|-----|----------------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8   | MSS_CR5B1_AXI_RD_B<br>US_SAFETY_CTRL_ERR<br>_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                          |
| 7:3 | RESERVED                                           | NONE | 0h    | Reserved                                                                                                                                              |
| 2:0 | MSS_CR5B1_AXI_RD_B<br>US_SAFETY_CTRL_ENA<br>BLE    | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.225 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_RD\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_RD\_BUS\_SAFETY\_FI Register (Offset = 18284h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of R5SS1 CORE1 AXI RD Initiator Port.

Return to [Summary Table](#)

**Table 2-675. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8284h       |

**Figure 2-225. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_RD\_BUS\_SAFETY\_FI Name Register**

| 31                                  | 30                                  | 29                                | 28                                | 27                                | 26                                | 25                                | 24                                |
|-------------------------------------|-------------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|
| MSS_CR5B1_AXI_RD_BUS_SAFETY_FI_SAFE |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| R/W                                 |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 0h                                  |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 23                                  | 22                                  | 21                                | 20                                | 19                                | 18                                | 17                                | 16                                |
| MSS_CR5B1_AXI_RD_BUS_SAFETY_FI_MAIN |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| R/W                                 |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 0h                                  |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 15                                  | 14                                  | 13                                | 12                                | 11                                | 10                                | 9                                 | 8                                 |
| MSS_CR5B1_AXI_RD_BUS_SAFETY_FI_DATA |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| R/W                                 |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 0h                                  |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 7                                   | 6                                   | 5                                 | 4                                 | 3                                 | 2                                 | 1                                 | 0                                 |
| RESERVED                            | MSS_CR5B1_AXI_RD_BUS_SAFETY_FI_DATA | MSS_CR5B1_AXI_RD_BUS_SAFETY_FI_SE | MSS_CR5B1_AXI_RD_BUS_SAFETY_FI_GL | MSS_CR5B1_AXI_RD_BUS_SAFETY_FI_GL | MSS_CR5B1_AXI_RD_BUS_SAFETY_FI_GL | MSS_CR5B1_AXI_RD_BUS_SAFETY_FI_GL | MSS_CR5B1_AXI_RD_BUS_SAFETY_FI_GL |
| NONE                                | R/W                                 | R/W                               | R/W                               | R/W                               | R/W                               | R/W                               | R/W                               |
| 0h                                  | 0h                                  | 0h                                | 0h                                | 0h                                | 0h                                | 0h                                | 0h                                |

**Table 2-677. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_RD\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5B1_AXI_RD_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_CR5B1_AXI_RD_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_CR5B1_AXI_RD_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |

**Table 2-677. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_RD\_BUS\_SAFETY\_FI Register Field Descriptions  
(continued)**

| Bit | Field                                                  | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|--------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | MSS_CR5B1_AXI_RD_B<br>US_SAFETY_FI_DED                 | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                             |
| 4   | MSS_CR5B1_AXI_RD_B<br>US_SAFETY_FI_SEC                 | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_CR5B1_AXI_RD_B<br>US_SAFETY_FI_GLOBAL<br>_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_CR5B1_AXI_RD_B<br>US_SAFETY_FI_GLOBAL<br>_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_CR5B1_AXI_RD_B<br>US_SAFETY_FI_GLOBAL<br>_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_CR5B1_AXI_RD_B<br>US_SAFETY_FI_GLOBAL<br>_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |



### 2.2.2.226 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR Register (Offset = 18288h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of R5SS1 CORE1 AXI RD Initiator port.

Return to [Summary Table](#)

**Table 2-678. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8288h       |

**Figure 2-226. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR Name Register**

|                                            |    |    |    |    |    |    |    |
|--------------------------------------------|----|----|----|----|----|----|----|
| 31                                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B1_AXI_RD_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 23                                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B1_AXI_RD_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 15                                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B1_AXI_RD_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 7                                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B1_AXI_RD_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |

**Table 2-680. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                                              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5B1_AXI_RD_B<br>US_SAFETY_ERR_DED            | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_CR5B1_AXI_RD_B<br>US_SAFETY_ERR_SEC            | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_CR5B1_AXI_RD_B<br>US_SAFETY_ERR_COM<br>P_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-680. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR Register Field Descriptions  
(continued)**

| Bit | Field                                            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|--------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_CR5B1_AXI_RD_B<br>US_SAFETY_ERR_COM<br>P_ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.227 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

**1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 1828Ch) [reset = 0h]**

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS1 CORE1 AXI RD Initiator Port.

Return to [Summary Table](#)

**Table 2-681. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 828Ch       |

**Figure 2-227. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                               |    |    |    |    |    |    |    |
|-----------------------------------------------|----|----|----|----|----|----|----|
| 31                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                                      |    |    |    |    |    |    |    |
| NONE                                          |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 23                                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                                      |    |    |    |    |    |    |    |
| NONE                                          |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 15                                            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B1_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 7                                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B1_AXI_RD_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |

**Table 2-683. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                                 | Type | Reset | Description                                                                                                                                                |
|-------|-------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                                              | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_CR5B1_AXI_RD_B<br>US_SAFETY_ERR_STAT<br>_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_CR5B1_AXI_RD_B<br>US_SAFETY_ERR_STAT<br>_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.228 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 18290h) [reset = 0h]

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS1 CORE1 AXI RD Initiator Port.

Return to [Summary Table](#)

**Table 2-684. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8290h       |

**Figure 2-228. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                               |    |    |    |    |    |    |    |
|-----------------------------------------------|----|----|----|----|----|----|----|
| 31                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B1_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 23                                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B1_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 15                                            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B1_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 7                                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B1_AXI_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |

**Table 2-686. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                                 | Type | Reset | Description                                                                                                                       |
|------|-------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5B1_AXI_RD_B<br>US_SAFETY_ERR_STAT<br>_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.229 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Register

**1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Register (Offset = 18294h) [reset = 0h]**

This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of R5SS1 CORE1 AXI RD Initiator Port.

Return to [Summary Table](#)

**Table 2-687. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8294h       |

**Figure 2-229. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Name Register**

|                                                |    |    |    |    |    |    |    |
|------------------------------------------------|----|----|----|----|----|----|----|
| 31                                             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B1_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |
| 23                                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B1_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |
| 15                                             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B1_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |
| 7                                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B1_AXI_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |

**Table 2-689. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Register Field Descriptions**

| Bit  | Field                                                  | Type | Reset | Description                                                                                                                     |
|------|--------------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5B1_AXI_RD_B<br>US_SAFETY_ERR_STAT<br>_READ_STAT | R    | 0h    | Read this bitfield for comapartor status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus. |

### 2.2.2.230 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_CTRL Register (Offset = 182A0h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS0 CORE0 AXI WR Initiator Port.

Return to [Summary Table](#)

**Table 2-690. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 82A0h       |

**Figure 2-230. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_CTRL Name Register**

|                                       |    |    |    |    |                                         |    |                                            |
|---------------------------------------|----|----|----|----|-----------------------------------------|----|--------------------------------------------|
| 31                                    | 30 | 29 | 28 | 27 | 26                                      | 25 | 24                                         |
| RESERVED                              |    |    |    |    |                                         |    |                                            |
| NONE                                  |    |    |    |    |                                         |    |                                            |
| 0h                                    |    |    |    |    |                                         |    |                                            |
| 23                                    | 22 | 21 | 20 | 19 | 18                                      | 17 | 16                                         |
| MSS_CR5A0_AXI_WR_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                         |    |                                            |
| R                                     |    |    |    |    |                                         |    |                                            |
| 0h                                    |    |    |    |    |                                         |    |                                            |
| 15                                    | 14 | 13 | 12 | 11 | 10                                      | 9  | 8                                          |
| RESERVED                              |    |    |    |    |                                         |    | MSS_CR5A0_AXI_WR_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                                  |    |    |    |    |                                         |    | R/W                                        |
| 0h                                    |    |    |    |    |                                         |    | 0h                                         |
| 7                                     | 6  | 5  | 4  | 3  | 2                                       | 1  | 0                                          |
| RESERVED                              |    |    |    |    | MSS_CR5A0_AXI_WR_BUS_SAFETY_CTRL_ENABLE |    |                                            |
| NONE                                  |    |    |    |    | R/W                                     |    |                                            |
| 0h                                    |    |    |    |    | 7h                                      |    |                                            |

**Table 2-692. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                 | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|---------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                              | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | MSS_CR5A0_AXI_WR_BUS_SAFETY_CTRL_TYPE | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                              | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

**Table 2-692. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_CTRL Register Field Descriptions (continued)**

| Bit | Field                                              | Type | Reset | Description                                                                                                                                           |
|-----|----------------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8   | MSS_CR5A0_AXI_WR_B<br>US_SAFETY_CTRL_ERR<br>_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                          |
| 7:3 | RESERVED                                           | NONE | 0h    | Reserved                                                                                                                                              |
| 2:0 | MSS_CR5A0_AXI_WR_B<br>US_SAFETY_CTRL_ENA<br>BLE    | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.231 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_FI Register (Offset = 182A4h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of R5SS0 CORE0 AXI WR Initiator Port.

Return to [Summary Table](#)

**Table 2-693. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 82A4h       |

**Figure 2-231. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_FI Name Register**

| 31                                  | 30                                  | 29                                | 28                                | 27                                | 26                                | 25                                | 24                                |
|-------------------------------------|-------------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|
| MSS_CR5A0_AXI_WR_BUS_SAFETY_FI_SAFE |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| R/W                                 |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 0h                                  |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 23                                  | 22                                  | 21                                | 20                                | 19                                | 18                                | 17                                | 16                                |
| MSS_CR5A0_AXI_WR_BUS_SAFETY_FI_MAIN |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| R/W                                 |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 0h                                  |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 15                                  | 14                                  | 13                                | 12                                | 11                                | 10                                | 9                                 | 8                                 |
| MSS_CR5A0_AXI_WR_BUS_SAFETY_FI_DATA |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| R/W                                 |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 0h                                  |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 7                                   | 6                                   | 5                                 | 4                                 | 3                                 | 2                                 | 1                                 | 0                                 |
| RESERVED                            | MSS_CR5A0_AXI_WR_BUS_SAFETY_FI_DATA | MSS_CR5A0_AXI_WR_BUS_SAFETY_FI_SE | MSS_CR5A0_AXI_WR_BUS_SAFETY_FI_GL | MSS_CR5A0_AXI_WR_BUS_SAFETY_FI_GL | MSS_CR5A0_AXI_WR_BUS_SAFETY_FI_GL | MSS_CR5A0_AXI_WR_BUS_SAFETY_FI_GL | MSS_CR5A0_AXI_WR_BUS_SAFETY_FI_GL |
| NONE                                | R/W                                 | R/W                               | R/W                               | R/W                               | R/W                               | R/W                               | R/W                               |
| 0h                                  | 0h                                  | 0h                                | 0h                                | 0h                                | 0h                                | 0h                                | 0h                                |

**Table 2-695. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5A0_AXI_WR_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_CR5A0_AXI_WR_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_CR5A0_AXI_WR_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |



**Table 2-695. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_FI Register Field Descriptions  
(continued)**

| Bit | Field                                                  | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|--------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | MSS_CR5A0_AXI_WR_B<br>US_SAFETY_FI_DED                 | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                             |
| 4   | MSS_CR5A0_AXI_WR_B<br>US_SAFETY_FI_SEC                 | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_CR5A0_AXI_WR_B<br>US_SAFETY_FI_GLOBAL<br>_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_CR5A0_AXI_WR_B<br>US_SAFETY_FI_GLOBAL<br>_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_CR5A0_AXI_WR_B<br>US_SAFETY_FI_GLOBAL<br>_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_CR5A0_AXI_WR_B<br>US_SAFETY_FI_GLOBAL<br>_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

### 2.2.2.232 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR Register (Offset = 182A8h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of R5SS0 CORE0 AXI WR Initiator port.

Return to [Summary Table](#)

**Table 2-696. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 82A8h       |

**Figure 2-232. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR Name Register**

|                                            |    |    |    |    |    |    |    |
|--------------------------------------------|----|----|----|----|----|----|----|
| 31                                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 23                                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 15                                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 7                                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |

**Table 2-698. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                                              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5A0_AXI_WR_B<br>US_SAFETY_ERR_DED            | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_CR5A0_AXI_WR_B<br>US_SAFETY_ERR_SEC            | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_CR5A0_AXI_WR_B<br>US_SAFETY_ERR_COM<br>P_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-698. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR Register Field Descriptions  
(continued)**

| Bit | Field                                            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|--------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_CR5A0_AXI_WR_B<br>US_SAFETY_ERR_COM<br>P_ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.233 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 182ACh) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS0 CORE0 AXI WR Initiator Port.

Return to [Summary Table](#)

**Table 2-699. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 82ACh       |

**Figure 2-233. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                               |    |    |    |    |    |    |    |
|-----------------------------------------------|----|----|----|----|----|----|----|
| 31                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                                      |    |    |    |    |    |    |    |
| NONE                                          |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 23                                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                                      |    |    |    |    |    |    |    |
| NONE                                          |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 15                                            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 7                                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |

**Table 2-701. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                                 | Type | Reset | Description                                                                                                                                                |
|-------|-------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                                              | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_CR5A0_AXI_WR_B<br>US_SAFETY_ERR_STAT<br>_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_CR5A0_AXI_WR_B<br>US_SAFETY_ERR_STAT<br>_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.234 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 182B0h) [reset = 0h]

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS0 CORE0 AXI WR Initiator Port.

Return to [Summary Table](#)

**Table 2-702. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 82B0h       |

**Figure 2-234. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                               |    |    |    |    |    |    |    |
|-----------------------------------------------|----|----|----|----|----|----|----|
| 31                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 23                                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 15                                            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 7                                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |

**Table 2-704. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                                 | Type | Reset | Description                                                                                                                       |
|------|-------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5A0_AXI_WR_B<br>US_SAFETY_ERR_STAT<br>_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.235 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register (Offset = 182B4h) [reset = 0h]

This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of R5SS0 CORE0 AXI WR Initiator Port.

Return to [Summary Table](#)

**Table 2-705. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 82B4h       |

**Figure 2-235. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Name Register**

|                                                 |    |    |    |    |    |    |    |
|-------------------------------------------------|----|----|----|----|----|----|----|
| 31                                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                               |    |    |    |    |    |    |    |
| 0h                                              |    |    |    |    |    |    |    |
| 23                                              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                               |    |    |    |    |    |    |    |
| 0h                                              |    |    |    |    |    |    |    |
| 15                                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                               |    |    |    |    |    |    |    |
| 0h                                              |    |    |    |    |    |    |    |
| 7                                               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                               |    |    |    |    |    |    |    |
| 0h                                              |    |    |    |    |    |    |    |

**Table 2-707. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register Field Descriptions**

| Bit  | Field                                                   | Type | Reset | Description                                                                                                           |
|------|---------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5A0_AXI_WR_B<br>US_SAFETY_ERR_STAT<br>_WRITE_STAT | R    | 0h    | Read this bitfield for comparator status for Write bus for this port.<br>1'b1 at any bit indicates error on Write Bus |

### 2.2.2.236 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register (Offset = 182B8h) [reset = 0h]

This register Indicates the Error Syndrome of Write Response errors in Bus Safety Comparator of R5SS0 CORE0 AXI WR Initiator Port.

Return to [Summary Table](#)

**Table 2-708. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 82B8h       |

**Figure 2-236. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Name Register**

| 31                                                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------------------------------|----|----|----|----|----|----|----|
| MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                   |    |    |    |    |    |    |    |
| 0h                                                  |    |    |    |    |    |    |    |
| 23                                                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                   |    |    |    |    |    |    |    |
| 0h                                                  |    |    |    |    |    |    |    |
| 15                                                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                   |    |    |    |    |    |    |    |
| 0h                                                  |    |    |    |    |    |    |    |
| 7                                                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                   |    |    |    |    |    |    |    |
| 0h                                                  |    |    |    |    |    |    |    |

**Table 2-710. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register Field Descriptions**

| Bit  | Field                                                       | Type | Reset | Description                                                                                                                           |
|------|-------------------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5A0_AXI_WR_B<br>US_SAFETY_ERR_STAT<br>_WRITERESP_STAT | R    | 0h    | Read this bitfield for comparator status for Write response bus for this port. 1'b1 at any bit indicates error on Write Response Bus. |

### 2.2.2.237 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_CTRL Register (Offset = 182C0h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS0 CORE1 AXI WR Initiator Port.

Return to [Summary Table](#)

**Table 2-711. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 82C0h       |

**Figure 2-237. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_CTRL Name Register**

|                                       |    |    |    |    |                                         |    |                                            |
|---------------------------------------|----|----|----|----|-----------------------------------------|----|--------------------------------------------|
| 31                                    | 30 | 29 | 28 | 27 | 26                                      | 25 | 24                                         |
| RESERVED                              |    |    |    |    |                                         |    |                                            |
| NONE                                  |    |    |    |    |                                         |    |                                            |
| 0h                                    |    |    |    |    |                                         |    |                                            |
| 23                                    | 22 | 21 | 20 | 19 | 18                                      | 17 | 16                                         |
| MSS_CR5B0_AXI_WR_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                         |    |                                            |
| R                                     |    |    |    |    |                                         |    |                                            |
| 0h                                    |    |    |    |    |                                         |    |                                            |
| 15                                    | 14 | 13 | 12 | 11 | 10                                      | 9  | 8                                          |
| RESERVED                              |    |    |    |    |                                         |    | MSS_CR5B0_AXI_WR_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                                  |    |    |    |    |                                         |    | R/W                                        |
| 0h                                    |    |    |    |    |                                         |    | 0h                                         |
| 7                                     | 6  | 5  | 4  | 3  | 2                                       | 1  | 0                                          |
| RESERVED                              |    |    |    |    | MSS_CR5B0_AXI_WR_BUS_SAFETY_CTRL_ENABLE |    |                                            |
| NONE                                  |    |    |    |    | R/W                                     |    |                                            |
| 0h                                    |    |    |    |    | 7h                                      |    |                                            |

**Table 2-713. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                 | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|---------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                              | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | MSS_CR5B0_AXI_WR_BUS_SAFETY_CTRL_TYPE | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                              | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |



**Table 2-713. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_CTRL Register Field Descriptions (continued)**

| Bit | Field                                              | Type | Reset | Description                                                                                                                                           |
|-----|----------------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8   | MSS_CR5B0_AXI_WR_B<br>US_SAFETY_CTRL_ERR<br>_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                          |
| 7:3 | RESERVED                                           | NONE | 0h    | Reserved                                                                                                                                              |
| 2:0 | MSS_CR5B0_AXI_WR_B<br>US_SAFETY_CTRL_ENA<br>BLE    | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.238 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_FI Register (Offset = 182C4h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of R5SS0 CORE1 AXI WR Initiator Port.

Return to [Summary Table](#)

**Table 2-714. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 82C4h       |

**Figure 2-238. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_FI Name Register**

| 31                                  | 30                                  | 29                                | 28                                | 27                                | 26                                | 25                                | 24                                |
|-------------------------------------|-------------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|
| MSS_CR5B0_AXI_WR_BUS_SAFETY_FI_SAFE |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| R/W                                 |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 0h                                  |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 23                                  | 22                                  | 21                                | 20                                | 19                                | 18                                | 17                                | 16                                |
| MSS_CR5B0_AXI_WR_BUS_SAFETY_FI_MAIN |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| R/W                                 |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 0h                                  |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 15                                  | 14                                  | 13                                | 12                                | 11                                | 10                                | 9                                 | 8                                 |
| MSS_CR5B0_AXI_WR_BUS_SAFETY_FI_DATA |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| R/W                                 |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 0h                                  |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 7                                   | 6                                   | 5                                 | 4                                 | 3                                 | 2                                 | 1                                 | 0                                 |
| RESERVED                            | MSS_CR5B0_AXI_WR_BUS_SAFETY_FI_DATA | MSS_CR5B0_AXI_WR_BUS_SAFETY_FI_SE | MSS_CR5B0_AXI_WR_BUS_SAFETY_FI_GL | MSS_CR5B0_AXI_WR_BUS_SAFETY_FI_GL | MSS_CR5B0_AXI_WR_BUS_SAFETY_FI_GL | MSS_CR5B0_AXI_WR_BUS_SAFETY_FI_GL | MSS_CR5B0_AXI_WR_BUS_SAFETY_FI_GL |
| NONE                                | R/W                                 | R/W                               | R/W                               | R/W                               | R/W                               | R/W                               | R/W                               |
| 0h                                  | 0h                                  | 0h                                | 0h                                | 0h                                | 0h                                | 0h                                | 0h                                |

**Table 2-716. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5B0_AXI_WR_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_CR5B0_AXI_WR_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_CR5B0_AXI_WR_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |

**Table 2-716. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_FI Register Field Descriptions  
(continued)**

| Bit | Field                                                  | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|--------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | MSS_CR5B0_AXI_WR_B<br>US_SAFETY_FI_DED                 | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                             |
| 4   | MSS_CR5B0_AXI_WR_B<br>US_SAFETY_FI_SEC                 | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_CR5B0_AXI_WR_B<br>US_SAFETY_FI_GLOBAL<br>_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_CR5B0_AXI_WR_B<br>US_SAFETY_FI_GLOBAL<br>_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_CR5B0_AXI_WR_B<br>US_SAFETY_FI_GLOBAL<br>_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_CR5B0_AXI_WR_B<br>US_SAFETY_FI_GLOBAL<br>_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

### 2.2.2.239 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR Register (Offset = 182C8h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of R5SS0 CORE1 AXI WR Initiator port.

Return to [Summary Table](#)

**Table 2-717. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 82C8h       |

**Figure 2-239. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR Name Register**

|                                            |    |    |    |    |    |    |    |
|--------------------------------------------|----|----|----|----|----|----|----|
| 31                                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 23                                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 15                                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 7                                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |

**Table 2-719. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                                              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5B0_AXI_WR_B<br>US_SAFETY_ERR_DED            | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_CR5B0_AXI_WR_B<br>US_SAFETY_ERR_SEC            | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_CR5B0_AXI_WR_B<br>US_SAFETY_ERR_COM<br>P_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-719. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR Register Field Descriptions  
(continued)**

| Bit | Field                                            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|--------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_CR5B0_AXI_WR_B<br>US_SAFETY_ERR_COM<br>P_ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.240 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 182CCh) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS0 CORE1 AXI WR Initiator Port.

Return to [Summary Table](#)

**Table 2-720. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 82CCh       |

**Figure 2-240. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                               |    |    |    |    |    |    |    |
|-----------------------------------------------|----|----|----|----|----|----|----|
| 31                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                                      |    |    |    |    |    |    |    |
| NONE                                          |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 23                                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                                      |    |    |    |    |    |    |    |
| NONE                                          |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 15                                            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 7                                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |

**Table 2-722. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                                 | Type | Reset | Description                                                                                                                                                |
|-------|-------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                                              | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_CR5B0_AXI_WR_B<br>US_SAFETY_ERR_STAT<br>_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_CR5B0_AXI_WR_B<br>US_SAFETY_ERR_STAT<br>_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.241 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 182D0h) [reset = 0h]

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS0 CORE1 AXI WR Initiator Port.

Return to [Summary Table](#)

**Table 2-723. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 82D0h       |

**Figure 2-241. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                               |    |    |    |    |    |    |    |
|-----------------------------------------------|----|----|----|----|----|----|----|
| 31                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 23                                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 15                                            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 7                                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |

**Table 2-725. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                                 | Type | Reset | Description                                                                                                                       |
|------|-------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5B0_AXI_WR_B<br>US_SAFETY_ERR_STAT<br>_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.242 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register (Offset = 182D4h) [reset = 0h]

This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of R5SS0 CORE1 AXI WR Initiator Port.

Return to [Summary Table](#)

**Table 2-726. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 82D4h       |

**Figure 2-242. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Name Register**

|                                                 |    |    |    |    |    |    |    |
|-------------------------------------------------|----|----|----|----|----|----|----|
| 31                                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                               |    |    |    |    |    |    |    |
| 0h                                              |    |    |    |    |    |    |    |
| 23                                              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                               |    |    |    |    |    |    |    |
| 0h                                              |    |    |    |    |    |    |    |
| 15                                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                               |    |    |    |    |    |    |    |
| 0h                                              |    |    |    |    |    |    |    |
| 7                                               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                               |    |    |    |    |    |    |    |
| 0h                                              |    |    |    |    |    |    |    |

**Table 2-728. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register Field Descriptions**

| Bit  | Field                                                   | Type | Reset | Description                                                                                                           |
|------|---------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5B0_AXI_WR_B<br>US_SAFETY_ERR_STAT<br>_WRITE_STAT | R    | 0h    | Read this bitfield for comparator status for Write bus for this port.<br>1'b1 at any bit indicates error on Write Bus |



### 2.2.2.243 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register (Offset = 182D8h) [reset = 0h]

This register Indicates the Error Syndrome of Write Response errors in Bus Safety Comparator of R5SS0 CORE1 AXI WR Initiator Port.

Return to [Summary Table](#)

**Table 2-729. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 82D8h       |

**Figure 2-243. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Name Register**

| 31                                                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------------------------------|----|----|----|----|----|----|----|
| MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                   |    |    |    |    |    |    |    |
| 0h                                                  |    |    |    |    |    |    |    |
| 23                                                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                   |    |    |    |    |    |    |    |
| 0h                                                  |    |    |    |    |    |    |    |
| 15                                                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                   |    |    |    |    |    |    |    |
| 0h                                                  |    |    |    |    |    |    |    |
| 7                                                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B0_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                   |    |    |    |    |    |    |    |
| 0h                                                  |    |    |    |    |    |    |    |

**Table 2-731. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register Field Descriptions**

| Bit  | Field                                                       | Type | Reset | Description                                                                                                                           |
|------|-------------------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5B0_AXI_WR_B<br>US_SAFETY_ERR_STAT<br>_WRITERESP_STAT | R    | 0h    | Read this bitfield for comparator status for Write response bus for this port. 1'b1 at any bit indicates error on Write Response Bus. |

### 2.2.2.244 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_CTRL Register (Offset = 182E0h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS1 CORE0 AXI WR Initiator Port.

Return to [Summary Table](#)

**Table 2-732. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 82E0h       |

**Figure 2-244. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_CTRL Name Register**

|                                       |    |    |    |    |                                         |    |                                            |
|---------------------------------------|----|----|----|----|-----------------------------------------|----|--------------------------------------------|
| 31                                    | 30 | 29 | 28 | 27 | 26                                      | 25 | 24                                         |
| RESERVED                              |    |    |    |    |                                         |    |                                            |
| NONE                                  |    |    |    |    |                                         |    |                                            |
| 0h                                    |    |    |    |    |                                         |    |                                            |
| 23                                    | 22 | 21 | 20 | 19 | 18                                      | 17 | 16                                         |
| MSS_CR5A1_AXI_WR_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                         |    |                                            |
| R                                     |    |    |    |    |                                         |    |                                            |
| 0h                                    |    |    |    |    |                                         |    |                                            |
| 15                                    | 14 | 13 | 12 | 11 | 10                                      | 9  | 8                                          |
| RESERVED                              |    |    |    |    |                                         |    | MSS_CR5A1_AXI_WR_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                                  |    |    |    |    |                                         |    | R/W                                        |
| 0h                                    |    |    |    |    |                                         |    | 0h                                         |
| 7                                     | 6  | 5  | 4  | 3  | 2                                       | 1  | 0                                          |
| RESERVED                              |    |    |    |    | MSS_CR5A1_AXI_WR_BUS_SAFETY_CTRL_ENABLE |    |                                            |
| NONE                                  |    |    |    |    | R/W                                     |    |                                            |
| 0h                                    |    |    |    |    | 7h                                      |    |                                            |

**Table 2-734. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                 | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|---------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                              | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | MSS_CR5A1_AXI_WR_BUS_SAFETY_CTRL_TYPE | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                              | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

**Table 2-734. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_CTRL Register Field Descriptions (continued)**

| Bit | Field                                              | Type | Reset | Description                                                                                                                                           |
|-----|----------------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8   | MSS_CR5A1_AXI_WR_B<br>US_SAFETY_CTRL_ERR<br>_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                          |
| 7:3 | RESERVED                                           | NONE | 0h    | Reserved                                                                                                                                              |
| 2:0 | MSS_CR5A1_AXI_WR_B<br>US_SAFETY_CTRL_ENA<br>BLE    | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.245 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_FI Register (Offset = 182E4h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of R5SS1 CORE0 AXI WR Initiator Port.

Return to [Summary Table](#)

**Table 2-735. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 82E4h       |

**Figure 2-245. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_FI Name Register**

| 31                                  | 30                                  | 29                                | 28                                | 27                                | 26                                | 25                                | 24                                |
|-------------------------------------|-------------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|
| MSS_CR5A1_AXI_WR_BUS_SAFETY_FI_SAFE |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| R/W                                 |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 0h                                  |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 23                                  | 22                                  | 21                                | 20                                | 19                                | 18                                | 17                                | 16                                |
| MSS_CR5A1_AXI_WR_BUS_SAFETY_FI_MAIN |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| R/W                                 |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 0h                                  |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 15                                  | 14                                  | 13                                | 12                                | 11                                | 10                                | 9                                 | 8                                 |
| MSS_CR5A1_AXI_WR_BUS_SAFETY_FI_DATA |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| R/W                                 |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 0h                                  |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 7                                   | 6                                   | 5                                 | 4                                 | 3                                 | 2                                 | 1                                 | 0                                 |
| RESERVED                            | MSS_CR5A1_AXI_WR_BUS_SAFETY_FI_DATA | MSS_CR5A1_AXI_WR_BUS_SAFETY_FI_SE | MSS_CR5A1_AXI_WR_BUS_SAFETY_FI_GL | MSS_CR5A1_AXI_WR_BUS_SAFETY_FI_GL | MSS_CR5A1_AXI_WR_BUS_SAFETY_FI_GL | MSS_CR5A1_AXI_WR_BUS_SAFETY_FI_GL | MSS_CR5A1_AXI_WR_BUS_SAFETY_FI_GL |
| NONE                                | R/W                                 | R/W                               | R/W                               | R/W                               | R/W                               | R/W                               | R/W                               |
| 0h                                  | 0h                                  | 0h                                | 0h                                | 0h                                | 0h                                | 0h                                | 0h                                |

**Table 2-737. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5A1_AXI_WR_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_CR5A1_AXI_WR_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_CR5A1_AXI_WR_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |

**Table 2-737. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_FI Register Field Descriptions  
(continued)**

| Bit | Field                                                  | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|--------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | MSS_CR5A1_AXI_WR_B<br>US_SAFETY_FI_DED                 | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                             |
| 4   | MSS_CR5A1_AXI_WR_B<br>US_SAFETY_FI_SEC                 | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_CR5A1_AXI_WR_B<br>US_SAFETY_FI_GLOBAL<br>_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_CR5A1_AXI_WR_B<br>US_SAFETY_FI_GLOBAL<br>_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_CR5A1_AXI_WR_B<br>US_SAFETY_FI_GLOBAL<br>_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_CR5A1_AXI_WR_B<br>US_SAFETY_FI_GLOBAL<br>_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

### 2.2.2.246 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR Register

**1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR Register (Offset = 182E8h) [reset = 0h]**

This Register provides the Error Status of Bus Safety Comparator of R5SS1 CORE0 AXI WR Initiator port.

Return to [Summary Table](#)

**Table 2-738. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 82E8h       |

**Figure 2-246. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR Name Register**

|                                            |    |    |    |    |    |    |    |
|--------------------------------------------|----|----|----|----|----|----|----|
| 31                                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 23                                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 15                                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 7                                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |

**Table 2-740. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                                              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5A1_AXI_WR_B<br>US_SAFETY_ERR_DED            | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_CR5A1_AXI_WR_B<br>US_SAFETY_ERR_SEC            | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_CR5A1_AXI_WR_B<br>US_SAFETY_ERR_COM<br>P_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-740. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR Register Field Descriptions (continued)**

| Bit | Field                                            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|--------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_CR5A1_AXI_WR_B<br>US_SAFETY_ERR_COM<br>P_ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.247 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 182ECh) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS1 CORE0 AXI WR Initiator Port.

Return to [Summary Table](#)

**Table 2-741. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 82ECh       |

**Figure 2-247. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                               |    |    |    |    |    |    |    |
|-----------------------------------------------|----|----|----|----|----|----|----|
| 31                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                                      |    |    |    |    |    |    |    |
| NONE                                          |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 23                                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                                      |    |    |    |    |    |    |    |
| NONE                                          |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 15                                            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 7                                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |

**Table 2-743. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                                 | Type | Reset | Description                                                                                                                                                |
|-------|-------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                                              | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_CR5A1_AXI_WR_B<br>US_SAFETY_ERR_STAT<br>_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_CR5A1_AXI_WR_B<br>US_SAFETY_ERR_STAT<br>_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |



### 2.2.2.248 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

**1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 182F0h) [reset = 0h]**

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS1 CORE0 AXI WR Initiator Port.

Return to [Summary Table](#)

**Table 2-744. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 82F0h       |

**Figure 2-248. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

| 31                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------------------------|----|----|----|----|----|----|----|
| MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 23                                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 15                                            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 7                                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |

**Table 2-746. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                                 | Type | Reset | Description                                                                                                                       |
|------|-------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5A1_AXI_WR_B<br>US_SAFETY_ERR_STAT<br>_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.249 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register (Offset = 182F4h) [reset = 0h]

This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of R5SS1 CORE0 AXI WR Initiator Port.

Return to [Summary Table](#)

**Table 2-747. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 82F4h       |

**Figure 2-249. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Name Register**

|                                                 |    |    |    |    |    |    |    |
|-------------------------------------------------|----|----|----|----|----|----|----|
| 31                                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                               |    |    |    |    |    |    |    |
| 0h                                              |    |    |    |    |    |    |    |
| 23                                              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                               |    |    |    |    |    |    |    |
| 0h                                              |    |    |    |    |    |    |    |
| 15                                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                               |    |    |    |    |    |    |    |
| 0h                                              |    |    |    |    |    |    |    |
| 7                                               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                               |    |    |    |    |    |    |    |
| 0h                                              |    |    |    |    |    |    |    |

**Table 2-749. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register Field Descriptions**

| Bit  | Field                                                   | Type | Reset | Description                                                                                                           |
|------|---------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5A1_AXI_WR_B<br>US_SAFETY_ERR_STAT<br>_WRITE_STAT | R    | 0h    | Read this bitfield for comparator status for Write bus for this port.<br>1'b1 at any bit indicates error on Write Bus |

### 2.2.2.250 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register

**1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register (Offset = 182F8h) [reset = 0h]**

This register Indicates the Error Syndrome of Write Response errors in Bus Safety Comparator of R5SS1 CORE0 AXI WR Initiator Port.

Return to [Summary Table](#)

**Table 2-750. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 82F8h       |

**Figure 2-250. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Name Register**

| 31                                                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------------------------------|----|----|----|----|----|----|----|
| MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                   |    |    |    |    |    |    |    |
| 0h                                                  |    |    |    |    |    |    |    |
| 23                                                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                   |    |    |    |    |    |    |    |
| 0h                                                  |    |    |    |    |    |    |    |
| 15                                                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                   |    |    |    |    |    |    |    |
| 0h                                                  |    |    |    |    |    |    |    |
| 7                                                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                   |    |    |    |    |    |    |    |
| 0h                                                  |    |    |    |    |    |    |    |

**Table 2-752. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register Field Descriptions**

| Bit  | Field                                                       | Type | Reset | Description                                                                                                                           |
|------|-------------------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5A1_AXI_WR_B<br>US_SAFETY_ERR_STAT<br>_WRITERESP_STAT | R    | 0h    | Read this bitfield for comparator status for Write response bus for this port. 1'b1 at any bit indicates error on Write Response Bus. |

### 2.2.2.251 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_CTRL Register (Offset = 18300h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS1 CORE1 AXI WR Initiator Port.

Return to [Summary Table](#)

**Table 2-753. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8300h       |

**Figure 2-251. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_CTRL Name Register**

|                                       |    |    |    |    |                                         |    |                                            |
|---------------------------------------|----|----|----|----|-----------------------------------------|----|--------------------------------------------|
| 31                                    | 30 | 29 | 28 | 27 | 26                                      | 25 | 24                                         |
| RESERVED                              |    |    |    |    |                                         |    |                                            |
| NONE                                  |    |    |    |    |                                         |    |                                            |
| 0h                                    |    |    |    |    |                                         |    |                                            |
| 23                                    | 22 | 21 | 20 | 19 | 18                                      | 17 | 16                                         |
| MSS_CR5B1_AXI_WR_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                         |    |                                            |
| R                                     |    |    |    |    |                                         |    |                                            |
| 0h                                    |    |    |    |    |                                         |    |                                            |
| 15                                    | 14 | 13 | 12 | 11 | 10                                      | 9  | 8                                          |
| RESERVED                              |    |    |    |    |                                         |    | MSS_CR5B1_AXI_WR_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                                  |    |    |    |    |                                         |    | R/W                                        |
| 0h                                    |    |    |    |    |                                         |    | 0h                                         |
| 7                                     | 6  | 5  | 4  | 3  | 2                                       | 1  | 0                                          |
| RESERVED                              |    |    |    |    | MSS_CR5B1_AXI_WR_BUS_SAFETY_CTRL_ENABLE |    |                                            |
| NONE                                  |    |    |    |    | R/W                                     |    |                                            |
| 0h                                    |    |    |    |    | 7h                                      |    |                                            |

**Table 2-755. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                 | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|---------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                              | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | MSS_CR5B1_AXI_WR_BUS_SAFETY_CTRL_TYPE | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                              | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

**Table 2-755. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_CTRL Register Field Descriptions (continued)**

| Bit | Field                                              | Type | Reset | Description                                                                                                                                           |
|-----|----------------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8   | MSS_CR5B1_AXI_WR_B<br>US_SAFETY_CTRL_ERR<br>_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                          |
| 7:3 | RESERVED                                           | NONE | 0h    | Reserved                                                                                                                                              |
| 2:0 | MSS_CR5B1_AXI_WR_B<br>US_SAFETY_CTRL_ENA<br>BLE    | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.252 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_FI Register (Offset = 18304h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of R5SS1 CORE1 AXI WR Initiator Port.

Return to [Summary Table](#)

**Table 2-756. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8304h       |

**Figure 2-252. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_FI Name Register**

| 31                                  | 30                                  | 29                                | 28                                | 27                                | 26                                | 25                                | 24                                |
|-------------------------------------|-------------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|
| MSS_CR5B1_AXI_WR_BUS_SAFETY_FI_SAFE |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| R/W                                 |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 0h                                  |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 23                                  | 22                                  | 21                                | 20                                | 19                                | 18                                | 17                                | 16                                |
| MSS_CR5B1_AXI_WR_BUS_SAFETY_FI_MAIN |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| R/W                                 |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 0h                                  |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 15                                  | 14                                  | 13                                | 12                                | 11                                | 10                                | 9                                 | 8                                 |
| MSS_CR5B1_AXI_WR_BUS_SAFETY_FI_DATA |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| R/W                                 |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 0h                                  |                                     |                                   |                                   |                                   |                                   |                                   |                                   |
| 7                                   | 6                                   | 5                                 | 4                                 | 3                                 | 2                                 | 1                                 | 0                                 |
| RESERVED                            | MSS_CR5B1_AXI_WR_BUS_SAFETY_FI_DATA | MSS_CR5B1_AXI_WR_BUS_SAFETY_FI_SE | MSS_CR5B1_AXI_WR_BUS_SAFETY_FI_GL | MSS_CR5B1_AXI_WR_BUS_SAFETY_FI_GL | MSS_CR5B1_AXI_WR_BUS_SAFETY_FI_GL | MSS_CR5B1_AXI_WR_BUS_SAFETY_FI_GL | MSS_CR5B1_AXI_WR_BUS_SAFETY_FI_GL |
| NONE                                | R/W                                 | R/W                               | R/W                               | R/W                               | R/W                               | R/W                               | R/W                               |
| 0h                                  | 0h                                  | 0h                                | 0h                                | 0h                                | 0h                                | 0h                                | 0h                                |

**Table 2-758. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5B1_AXI_WR_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_CR5B1_AXI_WR_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_CR5B1_AXI_WR_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |

**Table 2-758. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_FI Register Field Descriptions  
(continued)**

| Bit | Field                                                  | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|--------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | MSS_CR5B1_AXI_WR_B<br>US_SAFETY_FI_DED                 | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                             |
| 4   | MSS_CR5B1_AXI_WR_B<br>US_SAFETY_FI_SEC                 | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_CR5B1_AXI_WR_B<br>US_SAFETY_FI_GLOBAL<br>_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_CR5B1_AXI_WR_B<br>US_SAFETY_FI_GLOBAL<br>_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_CR5B1_AXI_WR_B<br>US_SAFETY_FI_GLOBAL<br>_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_CR5B1_AXI_WR_B<br>US_SAFETY_FI_GLOBAL<br>_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

### 2.2.2.253 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR Register (Offset = 18308h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of R5SS1 CORE1 AXI WR Initiator port.

Return to [Summary Table](#)

**Table 2-759. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8308h       |

**Figure 2-253. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR Name Register**

|                                            |    |    |    |    |    |    |    |
|--------------------------------------------|----|----|----|----|----|----|----|
| 31                                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 23                                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 15                                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 7                                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |

**Table 2-761. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                                              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|----------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5B1_AXI_WR_B<br>US_SAFETY_ERR_DED            | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_CR5B1_AXI_WR_B<br>US_SAFETY_ERR_SEC            | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_CR5B1_AXI_WR_B<br>US_SAFETY_ERR_COM<br>P_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |



**Table 2-761. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR Register Field Descriptions (continued)**

| Bit | Field                                            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|--------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_CR5B1_AXI_WR_B<br>US_SAFETY_ERR_COM<br>P_ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.254 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 1830Ch) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS1 CORE1 AXI WR Initiator Port.

Return to [Summary Table](#)

**Table 2-762. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 830Ch       |

**Figure 2-254. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                               |    |    |    |    |    |    |    |
|-----------------------------------------------|----|----|----|----|----|----|----|
| 31                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                                      |    |    |    |    |    |    |    |
| NONE                                          |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 23                                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                                      |    |    |    |    |    |    |    |
| NONE                                          |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 15                                            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 7                                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |

**Table 2-764. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                                 | Type | Reset | Description                                                                                                                                                |
|-------|-------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                                              | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_CR5B1_AXI_WR_B<br>US_SAFETY_ERR_STAT<br>_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_CR5B1_AXI_WR_B<br>US_SAFETY_ERR_STAT<br>_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.255 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

**1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 18310h) [reset = 0h]**

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS1 CORE1 AXI WR Initiator Port.

Return to [Summary Table](#)

**Table 2-765. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8310h       |

**Figure 2-255. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

| 31                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|-----------------------------------------------|----|----|----|----|----|----|----|
| MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 23                                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 15                                            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 7                                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |

**Table 2-767. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                                 | Type | Reset | Description                                                                                                                       |
|------|-------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5B1_AXI_WR_B<br>US_SAFETY_ERR_STAT<br>_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.256 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register (Offset = 18314h) [reset = 0h]

This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of R5SS1 CORE1 AXI WR Initiator Port.

Return to [Summary Table](#)

**Table 2-768. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8314h       |

**Figure 2-256. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Name Register**

|                                                 |    |    |    |    |    |    |    |
|-------------------------------------------------|----|----|----|----|----|----|----|
| 31                                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                               |    |    |    |    |    |    |    |
| 0h                                              |    |    |    |    |    |    |    |
| 23                                              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                               |    |    |    |    |    |    |    |
| 0h                                              |    |    |    |    |    |    |    |
| 15                                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                               |    |    |    |    |    |    |    |
| 0h                                              |    |    |    |    |    |    |    |
| 7                                               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                               |    |    |    |    |    |    |    |
| 0h                                              |    |    |    |    |    |    |    |

**Table 2-770. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register Field Descriptions**

| Bit  | Field                                                   | Type | Reset | Description                                                                                                           |
|------|---------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5B1_AXI_WR_B<br>US_SAFETY_ERR_STAT<br>_WRITE_STAT | R    | 0h    | Read this bitfield for comparator status for Write bus for this port.<br>1'b1 at any bit indicates error on Write Bus |

### 2.2.2.257 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register

**1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register (Offset = 18318h) [reset = 0h]**

This register Indicates the Error Syndrome of Write Response errors in Bus Safety Comparator of R5SS1 CORE1 AXI WR Initiator Port.

Return to [Summary Table](#)

**Table 2-771. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8318h       |

**Figure 2-257. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Name Register**

|                                                     |    |    |    |    |    |    |    |
|-----------------------------------------------------|----|----|----|----|----|----|----|
| 31                                                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                   |    |    |    |    |    |    |    |
| 0h                                                  |    |    |    |    |    |    |    |
| 23                                                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                   |    |    |    |    |    |    |    |
| 0h                                                  |    |    |    |    |    |    |    |
| 15                                                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                   |    |    |    |    |    |    |    |
| 0h                                                  |    |    |    |    |    |    |    |
| 7                                                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B1_AXI_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                   |    |    |    |    |    |    |    |
| 0h                                                  |    |    |    |    |    |    |    |

**Table 2-773. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register Field Descriptions**

| Bit  | Field                                                       | Type | Reset | Description                                                                                                                           |
|------|-------------------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5B1_AXI_WR_B<br>US_SAFETY_ERR_STAT<br>_WRITERESP_STAT | R    | 0h    | Read this bitfield for comparator status for Write response bus for this port. 1'b1 at any bit indicates error on Write Response Bus. |

### 2.2.2.258 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_CTRL Register (Offset = 18320h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS0 CORE0 AXI Target Port.

Return to [Summary Table](#)

**Table 2-774. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8320h       |

**Figure 2-258. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_CTRL Name Register**

|                                      |    |    |    |    |                                        |    |                                           |
|--------------------------------------|----|----|----|----|----------------------------------------|----|-------------------------------------------|
| 31                                   | 30 | 29 | 28 | 27 | 26                                     | 25 | 24                                        |
| RESERVED                             |    |    |    |    |                                        |    |                                           |
| NONE                                 |    |    |    |    |                                        |    |                                           |
| 0h                                   |    |    |    |    |                                        |    |                                           |
| 23                                   | 22 | 21 | 20 | 19 | 18                                     | 17 | 16                                        |
| MSS_CR5A0_AXI_S_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                        |    |                                           |
| R                                    |    |    |    |    |                                        |    |                                           |
| 0h                                   |    |    |    |    |                                        |    |                                           |
| 15                                   | 14 | 13 | 12 | 11 | 10                                     | 9  | 8                                         |
| RESERVED                             |    |    |    |    |                                        |    | MSS_CR5A0_AXI_S_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                                 |    |    |    |    |                                        |    | R/W                                       |
| 0h                                   |    |    |    |    |                                        |    | 0h                                        |
| 7                                    | 6  | 5  | 4  | 3  | 2                                      | 1  | 0                                         |
| RESERVED                             |    |    |    |    | MSS_CR5A0_AXI_S_BUS_SAFETY_CTRL_ENABLE |    |                                           |
| NONE                                 |    |    |    |    | R/W                                    |    |                                           |
| 0h                                   |    |    |    |    | 7h                                     |    |                                           |

**Table 2-776. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|-------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                                  | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | MSS_CR5A0_AXI_S_BUS_SAFETY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                                  | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | MSS_CR5A0_AXI_S_BUS_SAFETY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

**Table 2-776. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_CTRL Register Field Descriptions  
(continued)**

| Bit | Field                                          | Type | Reset | Description                                                                                                                                           |
|-----|------------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:3 | RESERVED                                       | NONE | 0h    | Reserved                                                                                                                                              |
| 2:0 | MSS_CR5A0_AXI_S_BU<br>S_SAFETY_CTRL_ENAB<br>LE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.259 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_FI Register (Offset = 18324h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of R5SS0 CORE0 AXI Target Port.

Return to [Summary Table](#)

**Table 2-777. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8324h       |

**Figure 2-259. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_FI Name Register**

| 31                                 | 30                                | 29                                | 28                                            | 27                                            | 26                                        | 25                                        | 24  |
|------------------------------------|-----------------------------------|-----------------------------------|-----------------------------------------------|-----------------------------------------------|-------------------------------------------|-------------------------------------------|-----|
| MSS_CR5A0_AXI_S_BUS_SAFETY_FI_SAFE |                                   |                                   |                                               |                                               |                                           |                                           |     |
| R/W                                |                                   |                                   |                                               |                                               |                                           |                                           |     |
| 0h                                 |                                   |                                   |                                               |                                               |                                           |                                           |     |
| 23                                 | 22                                | 21                                | 20                                            | 19                                            | 18                                        | 17                                        | 16  |
| MSS_CR5A0_AXI_S_BUS_SAFETY_FI_MAIN |                                   |                                   |                                               |                                               |                                           |                                           |     |
| R/W                                |                                   |                                   |                                               |                                               |                                           |                                           |     |
| 0h                                 |                                   |                                   |                                               |                                               |                                           |                                           |     |
| 15                                 | 14                                | 13                                | 12                                            | 11                                            | 10                                        | 9                                         | 8   |
| MSS_CR5A0_AXI_S_BUS_SAFETY_FI_DATA |                                   |                                   |                                               |                                               |                                           |                                           |     |
| R/W                                |                                   |                                   |                                               |                                               |                                           |                                           |     |
| 0h                                 |                                   |                                   |                                               |                                               |                                           |                                           |     |
| 7                                  | 6                                 | 5                                 | 4                                             | 3                                             | 2                                         | 1                                         | 0   |
| RESERVED                           | MSS_CR5A0_AXI_S_BUS_SAFETY_FI_DED | MSS_CR5A0_AXI_S_BUS_SAFETY_FI_SEC | MSS_CR5A0_AXI_S_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | MSS_CR5A0_AXI_S_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | MSS_CR5A0_AXI_S_BUS_SAFETY_FI_GLOBAL_SAFE | MSS_CR5A0_AXI_S_BUS_SAFETY_FI_GLOBAL_MAIN |     |
| NONE                               | R/W                               | R/W                               | R/W                                           | R/W                                           | R/W                                       | R/W                                       | R/W |
| 0h                                 | 0h                                | 0h                                | 0h                                            | 0h                                            | 0h                                        | 0h                                        | 0h  |

**Table 2-779. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5A0_AXI_S_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_CR5A0_AXI_S_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_CR5A0_AXI_S_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5     | MSS_CR5A0_AXI_S_BUS_SAFETY_FI_DED  | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                                                                                                                                                                                                        |



**Table 2-779. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_FI Register Field Descriptions  
(continued)**

| Bit | Field                                                 | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|-------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | MSS_CR5A0_AXI_S_BU<br>S_SAFETY_FI_SEC                 | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_CR5A0_AXI_S_BU<br>S_SAFETY_FI_GLOBAL_<br>SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_CR5A0_AXI_S_BU<br>S_SAFETY_FI_GLOBAL_<br>MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_CR5A0_AXI_S_BU<br>S_SAFETY_FI_GLOBAL_<br>SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_CR5A0_AXI_S_BU<br>S_SAFETY_FI_GLOBAL_<br>MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

### 2.2.2.260 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR Register (Offset = 18328h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of R5SS0 CORE0 AXI Target Port.

Return to [Summary Table](#)

**Table 2-780. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8328h       |

**Figure 2-260. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR Name Register**

|                                           |    |    |    |    |    |    |    |
|-------------------------------------------|----|----|----|----|----|----|----|
| 31                                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                         |    |    |    |    |    |    |    |
| 0h                                        |    |    |    |    |    |    |    |
| 23                                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                         |    |    |    |    |    |    |    |
| 0h                                        |    |    |    |    |    |    |    |
| 15                                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                         |    |    |    |    |    |    |    |
| 0h                                        |    |    |    |    |    |    |    |
| 7                                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                         |    |    |    |    |    |    |    |
| 0h                                        |    |    |    |    |    |    |    |

**Table 2-782. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                                             | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|---------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5A0_AXI_S_BU<br>S_SAFETY_ERR_DED            | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_CR5A0_AXI_S_BU<br>S_SAFETY_ERR_SEC            | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_CR5A0_AXI_S_BU<br>S_SAFETY_ERR_COMP_<br>CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-782. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR Register Field Descriptions  
(continued)**

| Bit | Field                                           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|-------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_CR5A0_AXI_S_BU<br>S_SAFETY_ERR_COMP_<br>ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.261 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 1832Ch) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS0 CORE0 AXI Target Port.

Return to [Summary Table](#)

**Table 2-783. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 832Ch       |

**Figure 2-261. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                              |    |    |    |    |    |    |    |
|----------------------------------------------|----|----|----|----|----|----|----|
| 31                                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                                     |    |    |    |    |    |    |    |
| NONE                                         |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 23                                           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                                     |    |    |    |    |    |    |    |
| NONE                                         |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 15                                           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 7                                            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |

**Table 2-785. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                                | Type | Reset | Description                                                                                                                                                |
|-------|------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                                             | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_CR5A0_AXI_S_BU<br>S_SAFETY_ERR_STAT_<br>DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_CR5A0_AXI_S_BU<br>S_SAFETY_ERR_STAT_<br>DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.262 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 18330h) [reset = 0h]

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS0 CORE0 AXI Target Port.

Return to [Summary Table](#)

**Table 2-786. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8330h       |

**Figure 2-262. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                              |    |    |    |    |    |    |    |
|----------------------------------------------|----|----|----|----|----|----|----|
| 31                                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 23                                           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 15                                           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 7                                            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |

**Table 2-788. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                                | Type | Reset | Description                                                                                                                       |
|------|------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5A0_AXI_S_BU<br>S_SAFETY_ERR_STAT_<br>CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.263 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register (Offset = 18334h) [reset = 0h]

This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of R5SS0 CORE0 AXI Target Port.

Return to [Summary Table](#)

**Table 2-789. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8334h       |

**Figure 2-263. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITE Name Register**

|                                                |    |    |    |    |    |    |    |
|------------------------------------------------|----|----|----|----|----|----|----|
| 31                                             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |
| 23                                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |
| 15                                             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |
| 7                                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |

**Table 2-791. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register Field Descriptions**

| Bit  | Field                                                  | Type | Reset | Description                                                                                                           |
|------|--------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5A0_AXI_S_BU<br>S_SAFETY_ERR_STAT_<br>WRITE_STAT | R    | 0h    | Read this bitfield for comparator status for Write bus for this port.<br>1'b1 at any bit indicates error on Write Bus |

### 2.2.2.264 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_READ Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_READ Register (Offset = 18338h) [reset = 0h]

This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of R5SS0 CORE0 AXI Target Port.

Return to [Summary Table](#)

**Table 2-792. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8338h       |

**Figure 2-264. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_READ Name Register**

|                                               |    |    |    |    |    |    |    |
|-----------------------------------------------|----|----|----|----|----|----|----|
| 31                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 23                                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 15                                            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 7                                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |

**Table 2-794. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_READ Register Field Descriptions**

| Bit  | Field                                                 | Type | Reset | Description                                                                                                                     |
|------|-------------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5A0_AXI_S_BU<br>S_SAFETY_ERR_STAT_<br>READ_STAT | R    | 0h    | Read this bitfield for comapartor status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus. |

### 2.2.2.265 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register (Offset = 1833Ch) [reset = 0h]

This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of R5SS0 CORE0 AXI Target Port.

Return to [Summary Table](#)

**Table 2-795. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 833Ch       |

**Figure 2-265. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Name Register**

| 31                                                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------------------------------------------------|----|----|----|----|----|----|----|
| MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                  |    |    |    |    |    |    |    |
| 0h                                                 |    |    |    |    |    |    |    |
| 23                                                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                  |    |    |    |    |    |    |    |
| 0h                                                 |    |    |    |    |    |    |    |
| 15                                                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                  |    |    |    |    |    |    |    |
| 0h                                                 |    |    |    |    |    |    |    |
| 7                                                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                  |    |    |    |    |    |    |    |
| 0h                                                 |    |    |    |    |    |    |    |

**Table 2-797. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register Field Descriptions**

| Bit  | Field                                                      | Type | Reset | Description                                                                                                                           |
|------|------------------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5A0_AXI_S_BU<br>S_SAFETY_ERR_STAT_<br>WRITERESP_STAT | R    | 0h    | Read this bitfield for comparator status for Write response bus for this port. 1'b1 at any bit indicates error on Write Response Bus. |



### 2.2.2.266 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_CTRL Register (Offset = 18340h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS0 CORE1 AXI Target Port.

Return to [Summary Table](#)

**Table 2-798. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8340h       |

**Figure 2-266. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_CTRL Name Register**

|                                      |    |    |    |    |                                        |    |                                           |
|--------------------------------------|----|----|----|----|----------------------------------------|----|-------------------------------------------|
| 31                                   | 30 | 29 | 28 | 27 | 26                                     | 25 | 24                                        |
| RESERVED                             |    |    |    |    |                                        |    |                                           |
| NONE                                 |    |    |    |    |                                        |    |                                           |
| 0h                                   |    |    |    |    |                                        |    |                                           |
| 23                                   | 22 | 21 | 20 | 19 | 18                                     | 17 | 16                                        |
| MSS_CR5B0_AXI_S_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                        |    |                                           |
| R                                    |    |    |    |    |                                        |    |                                           |
| 0h                                   |    |    |    |    |                                        |    |                                           |
| 15                                   | 14 | 13 | 12 | 11 | 10                                     | 9  | 8                                         |
| RESERVED                             |    |    |    |    |                                        |    | MSS_CR5B0_AXI_S_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                                 |    |    |    |    |                                        |    | R/W                                       |
| 0h                                   |    |    |    |    |                                        |    | 0h                                        |
| 7                                    | 6  | 5  | 4  | 3  | 2                                      | 1  | 0                                         |
| RESERVED                             |    |    |    |    | MSS_CR5B0_AXI_S_BUS_SAFETY_CTRL_ENABLE |    |                                           |
| NONE                                 |    |    |    |    | R/W                                    |    |                                           |
| 0h                                   |    |    |    |    | 7h                                     |    |                                           |

**Table 2-800. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|-------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                                  | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | MSS_CR5B0_AXI_S_BUS_SAFETY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                                  | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | MSS_CR5B0_AXI_S_BUS_SAFETY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

**Table 2-800. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_CTRL Register Field Descriptions  
(continued)**

| Bit | Field                                          | Type | Reset | Description                                                                                                                                           |
|-----|------------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:3 | RESERVED                                       | NONE | 0h    | Reserved                                                                                                                                              |
| 2:0 | MSS_CR5B0_AXI_S_BU<br>S_SAFETY_CTRL_ENAB<br>LE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.267 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_FI Register (Offset = 18344h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of R5SS0 CORE1 AXI Target Port.

Return to [Summary Table](#)

**Table 2-801. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8344h       |

**Figure 2-267. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_FI Name Register**

| 31                                 | 30                                | 29                                | 28                                            | 27                                            | 26                                        | 25                                        | 24                                        |
|------------------------------------|-----------------------------------|-----------------------------------|-----------------------------------------------|-----------------------------------------------|-------------------------------------------|-------------------------------------------|-------------------------------------------|
| MSS_CR5B0_AXI_S_BUS_SAFETY_FI_SAFE |                                   |                                   |                                               |                                               |                                           |                                           |                                           |
| R/W                                |                                   |                                   |                                               |                                               |                                           |                                           |                                           |
| 0h                                 |                                   |                                   |                                               |                                               |                                           |                                           |                                           |
| 23                                 | 22                                | 21                                | 20                                            | 19                                            | 18                                        | 17                                        | 16                                        |
| MSS_CR5B0_AXI_S_BUS_SAFETY_FI_MAIN |                                   |                                   |                                               |                                               |                                           |                                           |                                           |
| R/W                                |                                   |                                   |                                               |                                               |                                           |                                           |                                           |
| 0h                                 |                                   |                                   |                                               |                                               |                                           |                                           |                                           |
| 15                                 | 14                                | 13                                | 12                                            | 11                                            | 10                                        | 9                                         | 8                                         |
| MSS_CR5B0_AXI_S_BUS_SAFETY_FI_DATA |                                   |                                   |                                               |                                               |                                           |                                           |                                           |
| R/W                                |                                   |                                   |                                               |                                               |                                           |                                           |                                           |
| 0h                                 |                                   |                                   |                                               |                                               |                                           |                                           |                                           |
| 7                                  | 6                                 | 5                                 | 4                                             | 3                                             | 2                                         | 1                                         | 0                                         |
| RESERVED                           | MSS_CR5B0_AXI_S_BUS_SAFETY_FI_DED | MSS_CR5B0_AXI_S_BUS_SAFETY_FI_SEC | MSS_CR5B0_AXI_S_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | MSS_CR5B0_AXI_S_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | MSS_CR5B0_AXI_S_BUS_SAFETY_FI_GLOBAL_SAFE | MSS_CR5B0_AXI_S_BUS_SAFETY_FI_GLOBAL_MAIN | MSS_CR5B0_AXI_S_BUS_SAFETY_FI_GLOBAL_MAIN |
| NONE                               | R/W                               | R/W                               | R/W                                           | R/W                                           | R/W                                       | R/W                                       | R/W                                       |
| 0h                                 | 0h                                | 0h                                | 0h                                            | 0h                                            | 0h                                        | 0h                                        | 0h                                        |

**Table 2-803. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5B0_AXI_S_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_CR5B0_AXI_S_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_CR5B0_AXI_S_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5     | MSS_CR5B0_AXI_S_BUS_SAFETY_FI_DED  | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                                                                                                                                                                                                        |

**Table 2-803. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_FI Register Field Descriptions  
(continued)**

| Bit | Field                                                 | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|-------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | MSS_CR5B0_AXI_S_BU<br>S_SAFETY_FI_SEC                 | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_CR5B0_AXI_S_BU<br>S_SAFETY_FI_GLOBAL_<br>SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_CR5B0_AXI_S_BU<br>S_SAFETY_FI_GLOBAL_<br>MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_CR5B0_AXI_S_BU<br>S_SAFETY_FI_GLOBAL_<br>SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_CR5B0_AXI_S_BU<br>S_SAFETY_FI_GLOBAL_<br>MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

### 2.2.2.268 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR Register (Offset = 18348h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of R5SS0 CORE1 AXI Target Port.

Return to [Summary Table](#)

**Table 2-804. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8348h       |

**Figure 2-268. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR Name Register**

|                                           |    |    |    |    |    |    |    |
|-------------------------------------------|----|----|----|----|----|----|----|
| 31                                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                         |    |    |    |    |    |    |    |
| 0h                                        |    |    |    |    |    |    |    |
| 23                                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                         |    |    |    |    |    |    |    |
| 0h                                        |    |    |    |    |    |    |    |
| 15                                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                         |    |    |    |    |    |    |    |
| 0h                                        |    |    |    |    |    |    |    |
| 7                                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                         |    |    |    |    |    |    |    |
| 0h                                        |    |    |    |    |    |    |    |

**Table 2-806. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                                     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|-------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_DED        | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_SEC        | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_COMP_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-806. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR Register Field Descriptions  
(continued)**

| Bit | Field                                           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|-------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_CR5B0_AXI_S_BU<br>S_SAFETY_ERR_COMP_<br>ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.269 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 1834Ch) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS0 CORE1 AXI Target Port.

Return to [Summary Table](#)

**Table 2-807. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 834Ch       |

**Figure 2-269. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                              |    |    |    |    |    |    |    |
|----------------------------------------------|----|----|----|----|----|----|----|
| 31                                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                                     |    |    |    |    |    |    |    |
| NONE                                         |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 23                                           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                                     |    |    |    |    |    |    |    |
| NONE                                         |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 15                                           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 7                                            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |

**Table 2-809. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                                | Type | Reset | Description                                                                                                                                                |
|-------|------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                                             | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_CR5B0_AXI_S_BU<br>S_SAFETY_ERR_STAT_<br>DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_CR5B0_AXI_S_BU<br>S_SAFETY_ERR_STAT_<br>DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.270 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 18350h) [reset = 0h]

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS0 CORE1 AXI Target Port.

Return to [Summary Table](#)

**Table 2-810. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8350h       |

**Figure 2-270. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                              |    |    |    |    |    |    |    |
|----------------------------------------------|----|----|----|----|----|----|----|
| 31                                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 23                                           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 15                                           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 7                                            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |

**Table 2-812. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                                | Type | Reset | Description                                                                                                                       |
|------|------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5B0_AXI_S_BU<br>S_SAFETY_ERR_STAT_<br>CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |



### 2.2.2.271 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register (Offset = 18354h) [reset = 0h]

This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of R5SS0 CORE1 AXI Target Port.

Return to [Summary Table](#)

**Table 2-813. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8354h       |

**Figure 2-271. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITE Name Register**

|                                                |    |    |    |    |    |    |    |
|------------------------------------------------|----|----|----|----|----|----|----|
| 31                                             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |
| 23                                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |
| 15                                             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |
| 7                                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |

**Table 2-815. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register Field Descriptions**

| Bit  | Field                                                  | Type | Reset | Description                                                                                                           |
|------|--------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5B0_AXI_S_BU<br>S_SAFETY_ERR_STAT_<br>WRITE_STAT | R    | 0h    | Read this bitfield for comparator status for Write bus for this port.<br>1'b1 at any bit indicates error on Write Bus |

### 2.2.2.272 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_READ Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_READ Register (Offset = 18358h) [reset = 0h]

This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of R5SS0 CORE1 AXI Target Port.

Return to [Summary Table](#)

**Table 2-816. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8358h       |

**Figure 2-272. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_READ Name Register**

|                                               |    |    |    |    |    |    |    |
|-----------------------------------------------|----|----|----|----|----|----|----|
| 31                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 23                                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 15                                            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 7                                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |

**Table 2-818. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_READ Register Field Descriptions**

| Bit  | Field                                                 | Type | Reset | Description                                                                                                                     |
|------|-------------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5B0_AXI_S_BU<br>S_SAFETY_ERR_STAT_<br>READ_STAT | R    | 0h    | Read this bitfield for comapartor status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus. |

### 2.2.2.273 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register (Offset = 1835Ch) [reset = 0h]

This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of R5SS0 CORE1 AXI Target Port.

Return to [Summary Table](#)

**Table 2-819. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 835Ch       |

**Figure 2-273. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Name Register**

| 31                                                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------------------------------------------------|----|----|----|----|----|----|----|
| MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                  |    |    |    |    |    |    |    |
| 0h                                                 |    |    |    |    |    |    |    |
| 23                                                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                  |    |    |    |    |    |    |    |
| 0h                                                 |    |    |    |    |    |    |    |
| 15                                                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                  |    |    |    |    |    |    |    |
| 0h                                                 |    |    |    |    |    |    |    |
| 7                                                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B0_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                  |    |    |    |    |    |    |    |
| 0h                                                 |    |    |    |    |    |    |    |

**Table 2-821. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register Field Descriptions**

| Bit  | Field                                                      | Type | Reset | Description                                                                                                                           |
|------|------------------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5B0_AXI_S_BU<br>S_SAFETY_ERR_STAT_<br>WRITERESP_STAT | R    | 0h    | Read this bitfield for comparator status for Write response bus for this port. 1'b1 at any bit indicates error on Write Response Bus. |

### 2.2.2.274 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_CTRL Register (Offset = 18360h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS1 CORE0 AXI Target Port.

Return to [Summary Table](#)

**Table 2-822. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8360h       |

**Figure 2-274. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_CTRL Name Register**

|                                      |    |    |    |    |                                        |    |                                           |
|--------------------------------------|----|----|----|----|----------------------------------------|----|-------------------------------------------|
| 31                                   | 30 | 29 | 28 | 27 | 26                                     | 25 | 24                                        |
| RESERVED                             |    |    |    |    |                                        |    |                                           |
| NONE                                 |    |    |    |    |                                        |    |                                           |
| 0h                                   |    |    |    |    |                                        |    |                                           |
| 23                                   | 22 | 21 | 20 | 19 | 18                                     | 17 | 16                                        |
| MSS_CR5A1_AXI_S_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                        |    |                                           |
| R                                    |    |    |    |    |                                        |    |                                           |
| 0h                                   |    |    |    |    |                                        |    |                                           |
| 15                                   | 14 | 13 | 12 | 11 | 10                                     | 9  | 8                                         |
| RESERVED                             |    |    |    |    |                                        |    | MSS_CR5A1_AXI_S_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                                 |    |    |    |    |                                        |    | R/W                                       |
| 0h                                   |    |    |    |    |                                        |    | 0h                                        |
| 7                                    | 6  | 5  | 4  | 3  | 2                                      | 1  | 0                                         |
| RESERVED                             |    |    |    |    | MSS_CR5A1_AXI_S_BUS_SAFETY_CTRL_ENABLE |    |                                           |
| NONE                                 |    |    |    |    | R/W                                    |    |                                           |
| 0h                                   |    |    |    |    | 7h                                     |    |                                           |

**Table 2-824. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|-------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                                  | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | MSS_CR5A1_AXI_S_BUS_SAFETY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                                  | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | MSS_CR5A1_AXI_S_BUS_SAFETY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

**Table 2-824. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_CTRL Register Field Descriptions  
(continued)**

| Bit | Field                                          | Type | Reset | Description                                                                                                                                           |
|-----|------------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:3 | RESERVED                                       | NONE | 0h    | Reserved                                                                                                                                              |
| 2:0 | MSS_CR5A1_AXI_S_BU<br>S_SAFETY_CTRL_ENAB<br>LE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.275 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_FI Register (Offset = 18364h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of R5SS1 CORE0 AXI Target Port.

Return to [Summary Table](#)

**Table 2-825. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8364h       |

**Figure 2-275. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_FI Name Register**

| 31                                 | 30                                | 29                                | 28                                            | 27                                            | 26                                        | 25                                        | 24                                        |
|------------------------------------|-----------------------------------|-----------------------------------|-----------------------------------------------|-----------------------------------------------|-------------------------------------------|-------------------------------------------|-------------------------------------------|
| MSS_CR5A1_AXI_S_BUS_SAFETY_FI_SAFE |                                   |                                   |                                               |                                               |                                           |                                           |                                           |
| R/W                                |                                   |                                   |                                               |                                               |                                           |                                           |                                           |
| 0h                                 |                                   |                                   |                                               |                                               |                                           |                                           |                                           |
| 23                                 | 22                                | 21                                | 20                                            | 19                                            | 18                                        | 17                                        | 16                                        |
| MSS_CR5A1_AXI_S_BUS_SAFETY_FI_MAIN |                                   |                                   |                                               |                                               |                                           |                                           |                                           |
| R/W                                |                                   |                                   |                                               |                                               |                                           |                                           |                                           |
| 0h                                 |                                   |                                   |                                               |                                               |                                           |                                           |                                           |
| 15                                 | 14                                | 13                                | 12                                            | 11                                            | 10                                        | 9                                         | 8                                         |
| MSS_CR5A1_AXI_S_BUS_SAFETY_FI_DATA |                                   |                                   |                                               |                                               |                                           |                                           |                                           |
| R/W                                |                                   |                                   |                                               |                                               |                                           |                                           |                                           |
| 0h                                 |                                   |                                   |                                               |                                               |                                           |                                           |                                           |
| 7                                  | 6                                 | 5                                 | 4                                             | 3                                             | 2                                         | 1                                         | 0                                         |
| RESERVED                           | MSS_CR5A1_AXI_S_BUS_SAFETY_FI_DED | MSS_CR5A1_AXI_S_BUS_SAFETY_FI_SEC | MSS_CR5A1_AXI_S_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | MSS_CR5A1_AXI_S_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | MSS_CR5A1_AXI_S_BUS_SAFETY_FI_GLOBAL_SAFE | MSS_CR5A1_AXI_S_BUS_SAFETY_FI_GLOBAL_MAIN | MSS_CR5A1_AXI_S_BUS_SAFETY_FI_GLOBAL_MAIN |
| NONE                               | R/W                               | R/W                               | R/W                                           | R/W                                           | R/W                                       | R/W                                       | R/W                                       |
| 0h                                 | 0h                                | 0h                                | 0h                                            | 0h                                            | 0h                                        | 0h                                        | 0h                                        |

**Table 2-827. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5A1_AXI_S_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_CR5A1_AXI_S_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_CR5A1_AXI_S_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5     | MSS_CR5A1_AXI_S_BUS_SAFETY_FI_DED  | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                                                                                                                                                                                                        |

**Table 2-827. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_FI Register Field Descriptions  
(continued)**

| Bit | Field                                                 | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|-------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | MSS_CR5A1_AXI_S_BU<br>S_SAFETY_FI_SEC                 | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_CR5A1_AXI_S_BU<br>S_SAFETY_FI_GLOBAL_<br>SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_CR5A1_AXI_S_BU<br>S_SAFETY_FI_GLOBAL_<br>MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_CR5A1_AXI_S_BU<br>S_SAFETY_FI_GLOBAL_<br>SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_CR5A1_AXI_S_BU<br>S_SAFETY_FI_GLOBAL_<br>MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

### 2.2.2.276 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR Register (Offset = 18368h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of R5SS1 CORE0 AXI Target Port.

Return to [Summary Table](#)

**Table 2-828. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8368h       |

**Figure 2-276. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR Name Register**

|                                           |    |    |    |    |    |    |    |
|-------------------------------------------|----|----|----|----|----|----|----|
| 31                                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                         |    |    |    |    |    |    |    |
| 0h                                        |    |    |    |    |    |    |    |
| 23                                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                         |    |    |    |    |    |    |    |
| 0h                                        |    |    |    |    |    |    |    |
| 15                                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                         |    |    |    |    |    |    |    |
| 0h                                        |    |    |    |    |    |    |    |
| 7                                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                         |    |    |    |    |    |    |    |
| 0h                                        |    |    |    |    |    |    |    |

**Table 2-830. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                                     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|-------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_DED        | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_SEC        | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_COMP_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |



**Table 2-830. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR Register Field Descriptions  
(continued)**

| Bit | Field                                           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|-------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_CR5A1_AXI_S_BU<br>S_SAFETY_ERR_COMP_<br>ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.277 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 1836Ch) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS1 CORE0 AXI Target Port.

Return to [Summary Table](#)

**Table 2-831. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 836Ch       |

**Figure 2-277. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                              |    |    |    |    |    |    |    |
|----------------------------------------------|----|----|----|----|----|----|----|
| 31                                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                                     |    |    |    |    |    |    |    |
| NONE                                         |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 23                                           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                                     |    |    |    |    |    |    |    |
| NONE                                         |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 15                                           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 7                                            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |

**Table 2-833. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                        | Type | Reset | Description                                                                                                                                                |
|-------|----------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                                     | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.278 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 18370h) [reset = 0h]

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS1 CORE0 AXI Target Port.

Return to [Summary Table](#)

**Table 2-834. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8370h       |

**Figure 2-278. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                              |    |    |    |    |    |    |    |
|----------------------------------------------|----|----|----|----|----|----|----|
| 31                                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 23                                           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 15                                           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 7                                            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |

**Table 2-836. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                                | Type | Reset | Description                                                                                                                       |
|------|------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5A1_AXI_S_BU<br>S_SAFETY_ERR_STAT_<br>CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.279 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register

**1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register (Offset = 18374h) [reset = 0h]**

This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of R5SS1 CORE0 AXI Target Port.

Return to [Summary Table](#)

**Table 2-837. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8374h       |

**Figure 2-279. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITE Name Register**

| 31                                             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|------------------------------------------------|----|----|----|----|----|----|----|
| MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |
| 23                                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |
| 15                                             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |
| 7                                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |

**Table 2-839. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register Field Descriptions**

| Bit  | Field                                                  | Type | Reset | Description                                                                                                           |
|------|--------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5A1_AXI_S_BU<br>S_SAFETY_ERR_STAT_<br>WRITE_STAT | R    | 0h    | Read this bitfield for comparator status for Write bus for this port.<br>1'b1 at any bit indicates error on Write Bus |

### 2.2.2.280 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_READ Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_READ Register (Offset = 18378h) [reset = 0h]

This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of R5SS1 CORE0 AXI Target Port.

Return to [Summary Table](#)

**Table 2-840. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8378h       |

**Figure 2-280. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_READ Name Register**

|                                               |    |    |    |    |    |    |    |
|-----------------------------------------------|----|----|----|----|----|----|----|
| 31                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 23                                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 15                                            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 7                                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |

**Table 2-842. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_READ Register Field Descriptions**

| Bit  | Field                                                 | Type | Reset | Description                                                                                                                     |
|------|-------------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5A1_AXI_S_BU<br>S_SAFETY_ERR_STAT_<br>READ_STAT | R    | 0h    | Read this bitfield for comapartor status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus. |

### 2.2.2.281 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register (Offset = 1837Ch) [reset = 0h]

This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of R5SS1 CORE0 AXI Target Port.

Return to [Summary Table](#)

**Table 2-843. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 837Ch       |

**Figure 2-281. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Name Register**

| 31                                                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------------------------------------------------|----|----|----|----|----|----|----|
| MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                  |    |    |    |    |    |    |    |
| 0h                                                 |    |    |    |    |    |    |    |
| 23                                                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                  |    |    |    |    |    |    |    |
| 0h                                                 |    |    |    |    |    |    |    |
| 15                                                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                  |    |    |    |    |    |    |    |
| 0h                                                 |    |    |    |    |    |    |    |
| 7                                                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                  |    |    |    |    |    |    |    |
| 0h                                                 |    |    |    |    |    |    |    |

**Table 2-845. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register Field Descriptions**

| Bit  | Field                                                      | Type | Reset | Description                                                                                                                           |
|------|------------------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5A1_AXI_S_BU<br>S_SAFETY_ERR_STAT_<br>WRITERESP_STAT | R    | 0h    | Read this bitfield for comparator status for Write response bus for this port. 1'b1 at any bit indicates error on Write Response Bus. |

### 2.2.2.282 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_CTRL Register (Offset = 18380h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS1 CORE1 AXI Target Port.

Return to [Summary Table](#)

**Table 2-846. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8380h       |

**Figure 2-282. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_CTRL Name Register**

|                                      |    |    |    |    |                                        |    |                                           |
|--------------------------------------|----|----|----|----|----------------------------------------|----|-------------------------------------------|
| 31                                   | 30 | 29 | 28 | 27 | 26                                     | 25 | 24                                        |
| RESERVED                             |    |    |    |    |                                        |    |                                           |
| NONE                                 |    |    |    |    |                                        |    |                                           |
| 0h                                   |    |    |    |    |                                        |    |                                           |
| 23                                   | 22 | 21 | 20 | 19 | 18                                     | 17 | 16                                        |
| MSS_CR5B1_AXI_S_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                        |    |                                           |
| R                                    |    |    |    |    |                                        |    |                                           |
| 0h                                   |    |    |    |    |                                        |    |                                           |
| 15                                   | 14 | 13 | 12 | 11 | 10                                     | 9  | 8                                         |
| RESERVED                             |    |    |    |    |                                        |    | MSS_CR5B1_AXI_S_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                                 |    |    |    |    |                                        |    | R/W                                       |
| 0h                                   |    |    |    |    |                                        |    | 0h                                        |
| 7                                    | 6  | 5  | 4  | 3  | 2                                      | 1  | 0                                         |
| RESERVED                             |    |    |    |    | MSS_CR5B1_AXI_S_BUS_SAFETY_CTRL_ENABLE |    |                                           |
| NONE                                 |    |    |    |    | R/W                                    |    |                                           |
| 0h                                   |    |    |    |    | 7h                                     |    |                                           |

**Table 2-848. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|-------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                                  | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | MSS_CR5B1_AXI_S_BUS_SAFETY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                                  | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | MSS_CR5B1_AXI_S_BUS_SAFETY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

**Table 2-848. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_CTRL Register Field Descriptions  
(continued)**

| Bit | Field                                          | Type | Reset | Description                                                                                                                                           |
|-----|------------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:3 | RESERVED                                       | NONE | 0h    | Reserved                                                                                                                                              |
| 2:0 | MSS_CR5B1_AXI_S_BU<br>S_SAFETY_CTRL_ENAB<br>LE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |



### 2.2.2.283 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_FI Register (Offset = 18384h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of R5SS1 CORE1 AXI Target Port.

Return to [Summary Table](#)

**Table 2-849. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8384h       |

**Figure 2-283. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_FI Name Register**

| 31                                 | 30                                | 29                                | 28                                            | 27                                            | 26                                        | 25                                        | 24  |
|------------------------------------|-----------------------------------|-----------------------------------|-----------------------------------------------|-----------------------------------------------|-------------------------------------------|-------------------------------------------|-----|
| MSS_CR5B1_AXI_S_BUS_SAFETY_FI_SAFE |                                   |                                   |                                               |                                               |                                           |                                           |     |
| R/W                                |                                   |                                   |                                               |                                               |                                           |                                           |     |
| 0h                                 |                                   |                                   |                                               |                                               |                                           |                                           |     |
| 23                                 | 22                                | 21                                | 20                                            | 19                                            | 18                                        | 17                                        | 16  |
| MSS_CR5B1_AXI_S_BUS_SAFETY_FI_MAIN |                                   |                                   |                                               |                                               |                                           |                                           |     |
| R/W                                |                                   |                                   |                                               |                                               |                                           |                                           |     |
| 0h                                 |                                   |                                   |                                               |                                               |                                           |                                           |     |
| 15                                 | 14                                | 13                                | 12                                            | 11                                            | 10                                        | 9                                         | 8   |
| MSS_CR5B1_AXI_S_BUS_SAFETY_FI_DATA |                                   |                                   |                                               |                                               |                                           |                                           |     |
| R/W                                |                                   |                                   |                                               |                                               |                                           |                                           |     |
| 0h                                 |                                   |                                   |                                               |                                               |                                           |                                           |     |
| 7                                  | 6                                 | 5                                 | 4                                             | 3                                             | 2                                         | 1                                         | 0   |
| RESERVED                           | MSS_CR5B1_AXI_S_BUS_SAFETY_FI_DED | MSS_CR5B1_AXI_S_BUS_SAFETY_FI_SEC | MSS_CR5B1_AXI_S_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | MSS_CR5B1_AXI_S_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | MSS_CR5B1_AXI_S_BUS_SAFETY_FI_GLOBAL_SAFE | MSS_CR5B1_AXI_S_BUS_SAFETY_FI_GLOBAL_MAIN |     |
| NONE                               | R/W                               | R/W                               | R/W                                           | R/W                                           | R/W                                       | R/W                                       | R/W |
| 0h                                 | 0h                                | 0h                                | 0h                                            | 0h                                            | 0h                                        | 0h                                        | 0h  |

**Table 2-851. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5B1_AXI_S_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_CR5B1_AXI_S_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_CR5B1_AXI_S_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5     | MSS_CR5B1_AXI_S_BUS_SAFETY_FI_DED  | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                                                                                                                                                                                                        |

**Table 2-851. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_FI Register Field Descriptions  
(continued)**

| Bit | Field                                                 | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|-------------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | MSS_CR5B1_AXI_S_BU<br>S_SAFETY_FI_SEC                 | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_CR5B1_AXI_S_BU<br>S_SAFETY_FI_GLOBAL_<br>SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_CR5B1_AXI_S_BU<br>S_SAFETY_FI_GLOBAL_<br>MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_CR5B1_AXI_S_BU<br>S_SAFETY_FI_GLOBAL_<br>SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_CR5B1_AXI_S_BU<br>S_SAFETY_FI_GLOBAL_<br>MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

### 2.2.2.284 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR Register (Offset = 18388h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of R5SS1 CORE1 AXI Target Port.

Return to [Summary Table](#)

**Table 2-852. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8388h       |

**Figure 2-284. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR Name Register**

|                                           |    |    |    |    |    |    |    |
|-------------------------------------------|----|----|----|----|----|----|----|
| 31                                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                         |    |    |    |    |    |    |    |
| 0h                                        |    |    |    |    |    |    |    |
| 23                                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                         |    |    |    |    |    |    |    |
| 0h                                        |    |    |    |    |    |    |    |
| 15                                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                         |    |    |    |    |    |    |    |
| 0h                                        |    |    |    |    |    |    |    |
| 7                                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                         |    |    |    |    |    |    |    |
| 0h                                        |    |    |    |    |    |    |    |

**Table 2-854. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                                             | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|---------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5B1_AXI_S_BU<br>S_SAFETY_ERR_DED            | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_CR5B1_AXI_S_BU<br>S_SAFETY_ERR_SEC            | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_CR5B1_AXI_S_BU<br>S_SAFETY_ERR_COMP_<br>CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-854. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR Register Field Descriptions  
(continued)**

| Bit | Field                                           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|-------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_CR5B1_AXI_S_BU<br>S_SAFETY_ERR_COMP_<br>ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.285 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 1838Ch) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of R5SS1 CORE1 AXI Target Port.

Return to [Summary Table](#)

**Table 2-855. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 838Ch       |

**Figure 2-285. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                              |    |    |    |    |    |    |    |
|----------------------------------------------|----|----|----|----|----|----|----|
| 31                                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                                     |    |    |    |    |    |    |    |
| NONE                                         |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 23                                           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                                     |    |    |    |    |    |    |    |
| NONE                                         |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 15                                           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 7                                            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |

**Table 2-857. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                                | Type | Reset | Description                                                                                                                                                |
|-------|------------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                                             | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_CR5B1_AXI_S_BU<br>S_SAFETY_ERR_STAT_<br>DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_CR5B1_AXI_S_BU<br>S_SAFETY_ERR_STAT_<br>DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.286 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 18390h) [reset = 0h]

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of R5SS1 CORE1 AXI Target Port.

Return to [Summary Table](#)

**Table 2-858. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8390h       |

**Figure 2-286. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                              |    |    |    |    |    |    |    |
|----------------------------------------------|----|----|----|----|----|----|----|
| 31                                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 23                                           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 15                                           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 7                                            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |

**Table 2-860. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                                | Type | Reset | Description                                                                                                                       |
|------|------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5B1_AXI_S_BU<br>S_SAFETY_ERR_STAT_<br>CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.287 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register

**1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register (Offset = 18394h) [reset = 0h]**

This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of R5SS1 CORE1 AXI Target Port.

Return to [Summary Table](#)

**Table 2-861. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8394h       |

**Figure 2-287. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITE Name Register**

|                                                |    |    |    |    |    |    |    |
|------------------------------------------------|----|----|----|----|----|----|----|
| 31                                             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |
| 23                                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |
| 15                                             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |
| 7                                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                              |    |    |    |    |    |    |    |
| 0h                                             |    |    |    |    |    |    |    |

**Table 2-863. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register Field Descriptions**

| Bit  | Field                                                  | Type | Reset | Description                                                                                                           |
|------|--------------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5B1_AXI_S_BU<br>S_SAFETY_ERR_STAT_<br>WRITE_STAT | R    | 0h    | Read this bitfield for comparator status for Write bus for this port.<br>1'b1 at any bit indicates error on Write Bus |

### 2.2.2.288 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_READ Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_READ Register (Offset = 18398h) [reset = 0h]

This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of R5SS1 CORE1 AXI Target Port.

Return to [Summary Table](#)

**Table 2-864. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8398h       |

**Figure 2-288. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_READ Name Register**

|                                               |    |    |    |    |    |    |    |
|-----------------------------------------------|----|----|----|----|----|----|----|
| 31                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 23                                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 15                                            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 7                                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |

**Table 2-866. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_READ Register Field Descriptions**

| Bit  | Field                                                 | Type | Reset | Description                                                                                                                     |
|------|-------------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5B1_AXI_S_BU<br>S_SAFETY_ERR_STAT_<br>READ_STAT | R    | 0h    | Read this bitfield for comapartor status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus. |



### 2.2.2.289 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register (Offset = 1839Ch) [reset = 0h]

This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of R5SS1 CORE1 AXI Target Port.

Return to [Summary Table](#)

**Table 2-867. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 839Ch       |

**Figure 2-289. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Name Register**

| 31                                                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|----------------------------------------------------|----|----|----|----|----|----|----|
| MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                  |    |    |    |    |    |    |    |
| 0h                                                 |    |    |    |    |    |    |    |
| 23                                                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                  |    |    |    |    |    |    |    |
| 0h                                                 |    |    |    |    |    |    |    |
| 15                                                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                  |    |    |    |    |    |    |    |
| 0h                                                 |    |    |    |    |    |    |    |
| 7                                                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B1_AXI_S_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                  |    |    |    |    |    |    |    |
| 0h                                                 |    |    |    |    |    |    |    |

**Table 2-869. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AXI\_S\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register Field Descriptions**

| Bit  | Field                                                      | Type | Reset | Description                                                                                                                           |
|------|------------------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5B1_AXI_S_BU<br>S_SAFETY_ERR_STAT_<br>WRITERESP_STAT | R    | 0h    | Read this bitfield for comparator status for Write response bus for this port. 1'b1 at any bit indicates error on Write Response Bus. |

### 2.2.2.290 MSS\_CTRL\_MSS\_TPTC\_A0\_RD\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_TPTC\_A0\_RD\_BUS\_SAFETY\_CTRL Register (Offset = 183A0h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of TPTC00\_RD Initiator Port.

Return to [Summary Table](#)

**Table 2-870. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 83A0h       |

**Figure 2-290. MSS\_CTRL\_MSS\_TPTC\_A0\_RD\_BUS\_SAFETY\_CTRL Name Register**

|                                     |    |    |    |    |                                       |    |                                          |
|-------------------------------------|----|----|----|----|---------------------------------------|----|------------------------------------------|
| 31                                  | 30 | 29 | 28 | 27 | 26                                    | 25 | 24                                       |
| RESERVED                            |    |    |    |    |                                       |    |                                          |
| NONE                                |    |    |    |    |                                       |    |                                          |
| 0h                                  |    |    |    |    |                                       |    |                                          |
| 23                                  | 22 | 21 | 20 | 19 | 18                                    | 17 | 16                                       |
| MSS_TPTC_A0_RD_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                       |    |                                          |
| R                                   |    |    |    |    |                                       |    |                                          |
| 0h                                  |    |    |    |    |                                       |    |                                          |
| 15                                  | 14 | 13 | 12 | 11 | 10                                    | 9  | 8                                        |
| RESERVED                            |    |    |    |    |                                       |    | MSS_TPTC_A0_RD_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                                |    |    |    |    |                                       |    | R/W                                      |
| 0h                                  |    |    |    |    |                                       |    | 0h                                       |
| 7                                   | 6  | 5  | 4  | 3  | 2                                     | 1  | 0                                        |
| RESERVED                            |    |    |    |    | MSS_TPTC_A0_RD_BUS_SAFETY_CTRL_ENABLE |    |                                          |
| NONE                                |    |    |    |    | R/W                                   |    |                                          |
| 0h                                  |    |    |    |    | 7h                                    |    |                                          |

**Table 2-872. MSS\_CTRL\_MSS\_TPTC\_A0\_RD\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                                 | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | MSS_TPTC_A0_RD_BUS_SAFETY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                                 | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | MSS_TPTC_A0_RD_BUS_SAFETY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 7:3   | RESERVED                                 | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

**Table 2-872. MSS\_CTRL\_MSS\_TPTC\_A0\_RD\_BUS\_SAFETY\_CTRL Register Field Descriptions  
(continued)**

| Bit | Field                                     | Type | Reset | Description                                                                                                                                           |
|-----|-------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0 | MSS_TPTC_A0_RD_BUS_SAFETY_CTRL_ENAB<br>LE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.291 MSS\_CTRL\_MSS\_TPTC\_A0\_RD\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_TPTC\_A0\_RD\_BUS\_SAFETY\_FI Register (Offset = 183A4h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of TPTC00\_RD Initiator Port.

Return to [Summary Table](#)

**Table 2-873. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 83A4h       |

**Figure 2-291. MSS\_CTRL\_MSS\_TPTC\_A0\_RD\_BUS\_SAFETY\_FI Name Register**

| 31                                | 30                               | 29                               | 28                                           | 27                                           | 26                                       | 25                                       | 24  |
|-----------------------------------|----------------------------------|----------------------------------|----------------------------------------------|----------------------------------------------|------------------------------------------|------------------------------------------|-----|
| MSS_TPTC_A0_RD_BUS_SAFETY_FI_SAFE |                                  |                                  |                                              |                                              |                                          |                                          |     |
| R/W                               |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 0h                                |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 23                                | 22                               | 21                               | 20                                           | 19                                           | 18                                       | 17                                       | 16  |
| MSS_TPTC_A0_RD_BUS_SAFETY_FI_MAIN |                                  |                                  |                                              |                                              |                                          |                                          |     |
| R/W                               |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 0h                                |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 15                                | 14                               | 13                               | 12                                           | 11                                           | 10                                       | 9                                        | 8   |
| MSS_TPTC_A0_RD_BUS_SAFETY_FI_DATA |                                  |                                  |                                              |                                              |                                          |                                          |     |
| R/W                               |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 0h                                |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 7                                 | 6                                | 5                                | 4                                            | 3                                            | 2                                        | 1                                        | 0   |
| RESERVED                          | MSS_TPTC_A0_RD_BUS_SAFETY_FI_DED | MSS_TPTC_A0_RD_BUS_SAFETY_FI_SEC | MSS_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | MSS_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | MSS_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_SAFE | MSS_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_MAIN |     |
| NONE                              | R/W                              | R/W                              | R/W                                          | R/W                                          | R/W                                      | R/W                                      | R/W |
| 0h                                | 0h                               | 0h                               | 0h                                           | 0h                                           | 0h                                       | 0h                                       | 0h  |

**Table 2-875. MSS\_CTRL\_MSS\_TPTC\_A0\_RD\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                             | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-----------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_TPTC_A0_RD_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_TPTC_A0_RD_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_TPTC_A0_RD_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                          | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5     | MSS_TPTC_A0_RD_BUS_SAFETY_FI_DED  | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                                                                                                                                                                                                        |

**Table 2-875. MSS\_CTRL\_MSS\_TPTC\_A0\_RD\_BUS\_SAFETY\_FI Register Field Descriptions (continued)**

| Bit | Field                                        | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|----------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | MSS_TPTC_A0_RD_BUS_SAFETY_FI_SEC             | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

### 2.2.2.292 MSS\_CTRL\_MSS\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_MSS\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR Register (Offset = 183A8h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of TPTC00\_RD Initiator Port.

Return to [Summary Table](#)

**Table 2-876. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 83A8h       |

**Figure 2-292. MSS\_CTRL\_MSS\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR Name Register**

|                                          |    |    |    |    |    |    |    |
|------------------------------------------|----|----|----|----|----|----|----|
| 31                                       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_TPTC_A0_RD_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |
| 23                                       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_TPTC_A0_RD_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |
| 15                                       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_TPTC_A0_RD_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |
| 7                                        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_TPTC_A0_RD_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |

**Table 2-878. MSS\_CTRL\_MSS\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                                    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_TPTC_A0_RD_BUS_SAFETY_ERR_DED        | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_TPTC_A0_RD_BUS_SAFETY_ERR_SEC        | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_TPTC_A0_RD_BUS_SAFETY_ERR_COMP_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-878. MSS\_CTRL\_MSS\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR Register Field Descriptions (continued)**

| Bit | Field                                  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|----------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_TPTC_A0_RD_BUS_SAFETY_ERR_COMP_ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.293 MSS\_CTRL\_MSS\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_MSS\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 183ACh) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of TPTC00\_RD Initiator Port.

Return to [Summary Table](#)

**Table 2-879. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 83ACh       |

**Figure 2-293. MSS\_CTRL\_MSS\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                                    |    |    |    |    |    |    |    |
| NONE                                        |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                                    |    |    |    |    |    |    |    |
| NONE                                        |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-881. MSS\_CTRL\_MSS\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                       | Type | Reset | Description                                                                                                                                                |
|-------|---------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                                    | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |



### 2.2.2.294 MSS\_CTRL\_MSS\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

#### 1 MSS\_CTRL\_MSS\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 183B0h) [reset = 0h]

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of TPTC00\_RD Initiator Port.

Return to [Summary Table](#)

**Table 2-882. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 83B0h       |

**Figure 2-294. MSS\_CTRL\_MSS\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-884. MSS\_CTRL\_MSS\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                       | Type | Reset | Description                                                                                                                       |
|------|---------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.295 MSS\_CTRL\_MSS\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Register

#### 1 MSS\_CTRL\_MSS\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Register (Offset = 183B4h) [reset = 0h]

This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of TPTC00\_RD Initiator Port.

Return to [Summary Table](#)

**Table 2-885. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 83B4h       |

**Figure 2-295. MSS\_CTRL\_MSS\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Name Register**

|                                              |    |    |    |    |    |    |    |
|----------------------------------------------|----|----|----|----|----|----|----|
| 31                                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 23                                           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 15                                           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 7                                            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |

**Table 2-887. MSS\_CTRL\_MSS\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Register Field Descriptions**

| Bit  | Field                                        | Type | Reset | Description                                                                                                                     |
|------|----------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_READ_STAT | R    | 0h    | Read this bitfield for comparator status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus. |

### 2.2.2.296 MSS\_CTRL\_MSS\_TPTC\_A1\_RD\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_TPTC\_A1\_RD\_BUS\_SAFETY\_CTRL Register (Offset = 183C0h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of TPTC01\_RD Initiator Port.

Return to [Summary Table](#)

**Table 2-888. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 83C0h       |

**Figure 2-296. MSS\_CTRL\_MSS\_TPTC\_A1\_RD\_BUS\_SAFETY\_CTRL Name Register**

|                                     |    |    |    |    |                                       |    |                                          |
|-------------------------------------|----|----|----|----|---------------------------------------|----|------------------------------------------|
| 31                                  | 30 | 29 | 28 | 27 | 26                                    | 25 | 24                                       |
| RESERVED                            |    |    |    |    |                                       |    |                                          |
| NONE                                |    |    |    |    |                                       |    |                                          |
| 0h                                  |    |    |    |    |                                       |    |                                          |
| 23                                  | 22 | 21 | 20 | 19 | 18                                    | 17 | 16                                       |
| MSS_TPTC_A1_RD_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                       |    |                                          |
| R                                   |    |    |    |    |                                       |    |                                          |
| 0h                                  |    |    |    |    |                                       |    |                                          |
| 15                                  | 14 | 13 | 12 | 11 | 10                                    | 9  | 8                                        |
| RESERVED                            |    |    |    |    |                                       |    | MSS_TPTC_A1_RD_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                                |    |    |    |    |                                       |    | R/W                                      |
| 0h                                  |    |    |    |    |                                       |    | 0h                                       |
| 7                                   | 6  | 5  | 4  | 3  | 2                                     | 1  | 0                                        |
| RESERVED                            |    |    |    |    | MSS_TPTC_A1_RD_BUS_SAFETY_CTRL_ENABLE |    |                                          |
| NONE                                |    |    |    |    | R/W                                   |    |                                          |
| 0h                                  |    |    |    |    | 7h                                    |    |                                          |

**Table 2-890. MSS\_CTRL\_MSS\_TPTC\_A1\_RD\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                                 | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | MSS_TPTC_A1_RD_BUS_SAFETY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                                 | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | MSS_TPTC_A1_RD_BUS_SAFETY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 7:3   | RESERVED                                 | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

**Table 2-890. MSS\_CTRL\_MSS\_TPTC\_A1\_RD\_BUS\_SAFETY\_CTRL Register Field Descriptions  
(continued)**

| Bit | Field                                     | Type | Reset | Description                                                                                                                                           |
|-----|-------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0 | MSS_TPTC_A1_RD_BUS_SAFETY_CTRL_ENAB<br>LE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.297 MSS\_CTRL\_MSS\_TPTC\_A1\_RD\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_TPTC\_A1\_RD\_BUS\_SAFETY\_FI Register (Offset = 183C4h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of TPTC01\_RD Initiator Port.

Return to [Summary Table](#)

**Table 2-891. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 83C4h       |

**Figure 2-297. MSS\_CTRL\_MSS\_TPTC\_A1\_RD\_BUS\_SAFETY\_FI Name Register**

| 31                                | 30                               | 29                               | 28                                           | 27                                           | 26                                       | 25                                       | 24  |
|-----------------------------------|----------------------------------|----------------------------------|----------------------------------------------|----------------------------------------------|------------------------------------------|------------------------------------------|-----|
| MSS_TPTC_A1_RD_BUS_SAFETY_FI_SAFE |                                  |                                  |                                              |                                              |                                          |                                          |     |
| R/W                               |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 0h                                |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 23                                | 22                               | 21                               | 20                                           | 19                                           | 18                                       | 17                                       | 16  |
| MSS_TPTC_A1_RD_BUS_SAFETY_FI_MAIN |                                  |                                  |                                              |                                              |                                          |                                          |     |
| R/W                               |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 0h                                |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 15                                | 14                               | 13                               | 12                                           | 11                                           | 10                                       | 9                                        | 8   |
| MSS_TPTC_A1_RD_BUS_SAFETY_FI_DATA |                                  |                                  |                                              |                                              |                                          |                                          |     |
| R/W                               |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 0h                                |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 7                                 | 6                                | 5                                | 4                                            | 3                                            | 2                                        | 1                                        | 0   |
| RESERVED                          | MSS_TPTC_A1_RD_BUS_SAFETY_FI_DED | MSS_TPTC_A1_RD_BUS_SAFETY_FI_SEC | MSS_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | MSS_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | MSS_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_SAFE | MSS_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_MAIN |     |
| NONE                              | R/W                              | R/W                              | R/W                                          | R/W                                          | R/W                                      | R/W                                      | R/W |
| 0h                                | 0h                               | 0h                               | 0h                                           | 0h                                           | 0h                                       | 0h                                       | 0h  |

**Table 2-893. MSS\_CTRL\_MSS\_TPTC\_A1\_RD\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                             | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-----------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_TPTC_A1_RD_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_TPTC_A1_RD_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_TPTC_A1_RD_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                          | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5     | MSS_TPTC_A1_RD_BUS_SAFETY_FI_DED  | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                                                                                                                                                                                                        |

**Table 2-893. MSS\_CTRL\_MSS\_TPTC\_A1\_RD\_BUS\_SAFETY\_FI Register Field Descriptions (continued)**

| Bit | Field                                        | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|----------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | MSS_TPTC_A1_RD_BUS_SAFETY_FI_SEC             | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

## 2.2.2.298 MSS\_CTRL\_MSS\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR Register

### 1 MSS\_CTRL\_MSS\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR Register (Offset = 183C8h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of TPTC01\_RD Initiator Port.

Return to [Summary Table](#)

**Table 2-894. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 83C8h       |

**Figure 2-298. MSS\_CTRL\_MSS\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR Name Register**

|                                          |    |    |    |    |    |    |    |
|------------------------------------------|----|----|----|----|----|----|----|
| 31                                       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_TPTC_A1_RD_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |
| 23                                       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_TPTC_A1_RD_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |
| 15                                       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_TPTC_A1_RD_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |
| 7                                        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_TPTC_A1_RD_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |

**Table 2-896. MSS\_CTRL\_MSS\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                                    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_TPTC_A1_RD_BUS_SAFETY_ERR_DED        | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_TPTC_A1_RD_BUS_SAFETY_ERR_SEC        | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_TPTC_A1_RD_BUS_SAFETY_ERR_COMP_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-896. MSS\_CTRL\_MSS\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR Register Field Descriptions (continued)**

| Bit | Field                                  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|----------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_TPTC_A1_RD_BUS_SAFETY_ERR_COMP_ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |



### 2.2.2.299 MSS\_CTRL\_MSS\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_MSS\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 183CCh) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of TPTC01\_RD Initiator Port.

Return to [Summary Table](#)

**Table 2-897. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 83CCh       |

**Figure 2-299. MSS\_CTRL\_MSS\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                                    |    |    |    |    |    |    |    |
| NONE                                        |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                                    |    |    |    |    |    |    |    |
| NONE                                        |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-899. MSS\_CTRL\_MSS\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                       | Type | Reset | Description                                                                                                                                                |
|-------|---------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                                    | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.300 MSS\_CTRL\_MSS\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

#### 1 MSS\_CTRL\_MSS\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 183D0h) [reset = 0h]

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of TPTC01\_RD Initiator Port.

Return to [Summary Table](#)

**Table 2-900. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 83D0h       |

**Figure 2-300. MSS\_CTRL\_MSS\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-902. MSS\_CTRL\_MSS\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                       | Type | Reset | Description                                                                                                                       |
|------|---------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.301 MSS\_CTRL\_MSS\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Register

#### 1 MSS\_CTRL\_MSS\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Register (Offset = 183D4h) [reset = 0h]

This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of TPTC01\_RD Initiator Port.

Return to [Summary Table](#)

**Table 2-903. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 83D4h       |

**Figure 2-301. MSS\_CTRL\_MSS\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Name Register**

|                                              |    |    |    |    |    |    |    |
|----------------------------------------------|----|----|----|----|----|----|----|
| 31                                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 23                                           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 15                                           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 7                                            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |

**Table 2-905. MSS\_CTRL\_MSS\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Register Field Descriptions**

| Bit  | Field                                        | Type | Reset | Description                                                                                                                     |
|------|----------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_READ_STAT | R    | 0h    | Read this bitfield for comparator status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus. |

### 2.2.2.302 MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_CTRL Register (Offset = 183E0h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of TPTC00\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-906. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 83E0h       |

**Figure 2-302. MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_CTRL Name Register**

|                                     |    |    |    |    |                                       |    |                                          |
|-------------------------------------|----|----|----|----|---------------------------------------|----|------------------------------------------|
| 31                                  | 30 | 29 | 28 | 27 | 26                                    | 25 | 24                                       |
| RESERVED                            |    |    |    |    |                                       |    |                                          |
| NONE                                |    |    |    |    |                                       |    |                                          |
| 0h                                  |    |    |    |    |                                       |    |                                          |
| 23                                  | 22 | 21 | 20 | 19 | 18                                    | 17 | 16                                       |
| MSS_TPTC_A0_WR_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                       |    |                                          |
| R                                   |    |    |    |    |                                       |    |                                          |
| 0h                                  |    |    |    |    |                                       |    |                                          |
| 15                                  | 14 | 13 | 12 | 11 | 10                                    | 9  | 8                                        |
| RESERVED                            |    |    |    |    |                                       |    | MSS_TPTC_A0_WR_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                                |    |    |    |    |                                       |    | R/W                                      |
| 0h                                  |    |    |    |    |                                       |    | 0h                                       |
| 7                                   | 6  | 5  | 4  | 3  | 2                                     | 1  | 0                                        |
| RESERVED                            |    |    |    |    | MSS_TPTC_A0_WR_BUS_SAFETY_CTRL_ENABLE |    |                                          |
| NONE                                |    |    |    |    | R/W                                   |    |                                          |
| 0h                                  |    |    |    |    | 7h                                    |    |                                          |

**Table 2-908. MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                                 | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | MSS_TPTC_A0_WR_BUS_SAFETY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                                 | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | MSS_TPTC_A0_WR_BUS_SAFETY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 7:3   | RESERVED                                 | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

**Table 2-908. MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_CTRL Register Field Descriptions  
(continued)**

| Bit | Field                                         | Type | Reset | Description                                                                                                                                           |
|-----|-----------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0 | MSS_TPTC_A0_WR_BU<br>S_SAFETY_CTRL_ENAB<br>LE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.303 MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_FI Register (Offset = 183E4h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of TPTC00\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-909. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 83E4h       |

**Figure 2-303. MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_FI Name Register**

| 31                                | 30                               | 29                               | 28                                           | 27                                           | 26                                       | 25                                       | 24  |
|-----------------------------------|----------------------------------|----------------------------------|----------------------------------------------|----------------------------------------------|------------------------------------------|------------------------------------------|-----|
| MSS_TPTC_A0_WR_BUS_SAFETY_FI_SAFE |                                  |                                  |                                              |                                              |                                          |                                          |     |
| R/W                               |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 0h                                |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 23                                | 22                               | 21                               | 20                                           | 19                                           | 18                                       | 17                                       | 16  |
| MSS_TPTC_A0_WR_BUS_SAFETY_FI_MAIN |                                  |                                  |                                              |                                              |                                          |                                          |     |
| R/W                               |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 0h                                |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 15                                | 14                               | 13                               | 12                                           | 11                                           | 10                                       | 9                                        | 8   |
| MSS_TPTC_A0_WR_BUS_SAFETY_FI_DATA |                                  |                                  |                                              |                                              |                                          |                                          |     |
| R/W                               |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 0h                                |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 7                                 | 6                                | 5                                | 4                                            | 3                                            | 2                                        | 1                                        | 0   |
| RESERVED                          | MSS_TPTC_A0_WR_BUS_SAFETY_FI_DED | MSS_TPTC_A0_WR_BUS_SAFETY_FI_SEC | MSS_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | MSS_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | MSS_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_SAFE | MSS_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_MAIN |     |
| NONE                              | R/W                              | R/W                              | R/W                                          | R/W                                          | R/W                                      | R/W                                      | R/W |
| 0h                                | 0h                               | 0h                               | 0h                                           | 0h                                           | 0h                                       | 0h                                       | 0h  |

**Table 2-911. MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                             | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-----------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_TPTC_A0_WR_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_TPTC_A0_WR_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_TPTC_A0_WR_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                          | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5     | MSS_TPTC_A0_WR_BUS_SAFETY_FI_DED  | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                                                                                                                                                                                                        |

**Table 2-911. MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_FI Register Field Descriptions (continued)**

| Bit | Field                                        | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|----------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | MSS_TPTC_A0_WR_BUS_SAFETY_FI_SEC             | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

### 2.2.2.304 MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR Register (Offset = 183E8h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of TPTC00\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-912. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 83E8h       |

**Figure 2-304. MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR Name Register**

|                                          |    |    |    |    |    |    |    |
|------------------------------------------|----|----|----|----|----|----|----|
| 31                                       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_TPTC_A0_WR_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |
| 23                                       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_TPTC_A0_WR_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |
| 15                                       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_TPTC_A0_WR_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |
| 7                                        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_TPTC_A0_WR_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |

**Table 2-914. MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                                            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_TPTC_A0_WR_BU<br>S_SAFETY_ERR_DED            | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_TPTC_A0_WR_BU<br>S_SAFETY_ERR_SEC            | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_TPTC_A0_WR_BU<br>S_SAFETY_ERR_COMP_<br>CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |



**Table 2-914. MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR Register Field Descriptions  
(continued)**

| Bit | Field                                          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_TPTC_A0_WR_BU<br>S_SAFETY_ERR_COMP_<br>ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.305 MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 183ECh) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of TPTC00\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-915. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 83ECh       |

**Figure 2-305. MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                                    |    |    |    |    |    |    |    |
| NONE                                        |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                                    |    |    |    |    |    |    |    |
| NONE                                        |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-917. MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                       | Type | Reset | Description                                                                                                                                                |
|-------|---------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                                    | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.306 MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

#### 1 MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 183F0h) [reset = 0h]

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of TPTC00\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-918. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 83F0h       |

**Figure 2-306. MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-920. MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                               | Type | Reset | Description                                                                                                                       |
|------|-----------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_TPTC_A0_WR_BU<br>S_SAFETY_ERR_STAT_<br>CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.307 MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register

#### 1 MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register (Offset = 183F4h) [reset = 0h]

This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of TPTC00\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-921. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 83F4h       |

**Figure 2-307. MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Name Register**

|                                               |    |    |    |    |    |    |    |
|-----------------------------------------------|----|----|----|----|----|----|----|
| 31                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 23                                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 15                                            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 7                                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |

**Table 2-923. MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register Field Descriptions**

| Bit  | Field                                         | Type | Reset | Description                                                                                                        |
|------|-----------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT | R    | 0h    | Read this bitfield for comparator status for Write bus for this port. 1'b1 at any bit indicates error on Write Bus |

### 2.2.2.308 MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register

#### 1 MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register (Offset = 183F8h) [reset = 0h]

This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of TPTC00\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-924. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 83F8h       |

**Figure 2-308. MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Name Register**

|                                                   |    |    |    |    |    |    |    |
|---------------------------------------------------|----|----|----|----|----|----|----|
| 31                                                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                 |    |    |    |    |    |    |    |
| 0h                                                |    |    |    |    |    |    |    |
| 23                                                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                 |    |    |    |    |    |    |    |
| 0h                                                |    |    |    |    |    |    |    |
| 15                                                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                 |    |    |    |    |    |    |    |
| 0h                                                |    |    |    |    |    |    |    |
| 7                                                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                 |    |    |    |    |    |    |    |
| 0h                                                |    |    |    |    |    |    |    |

**Table 2-926. MSS\_CTRL\_MSS\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register Field Descriptions**

| Bit  | Field                                                     | Type | Reset | Description                                                                                                                           |
|------|-----------------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_TPTC_A0_WR_BU<br>S_SAFETY_ERR_STAT_<br>WRITERESP_STAT | R    | 0h    | Read this bitfield for comparator status for Write response bus for this port. 1'b1 at any bit indicates error on Write Response Bus. |

### 2.2.2.309 MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_CTRL Register (Offset = 18400h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of TPTC01\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-927. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8400h       |

**Figure 2-309. MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_CTRL Name Register**

|                                     |    |    |    |    |                                       |    |                                          |
|-------------------------------------|----|----|----|----|---------------------------------------|----|------------------------------------------|
| 31                                  | 30 | 29 | 28 | 27 | 26                                    | 25 | 24                                       |
| RESERVED                            |    |    |    |    |                                       |    |                                          |
| NONE                                |    |    |    |    |                                       |    |                                          |
| 0h                                  |    |    |    |    |                                       |    |                                          |
| 23                                  | 22 | 21 | 20 | 19 | 18                                    | 17 | 16                                       |
| MSS_TPTC_A1_WR_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                       |    |                                          |
| R                                   |    |    |    |    |                                       |    |                                          |
| 0h                                  |    |    |    |    |                                       |    |                                          |
| 15                                  | 14 | 13 | 12 | 11 | 10                                    | 9  | 8                                        |
| RESERVED                            |    |    |    |    |                                       |    | MSS_TPTC_A1_WR_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                                |    |    |    |    |                                       |    | R/W                                      |
| 0h                                  |    |    |    |    |                                       |    | 0h                                       |
| 7                                   | 6  | 5  | 4  | 3  | 2                                     | 1  | 0                                        |
| RESERVED                            |    |    |    |    | MSS_TPTC_A1_WR_BUS_SAFETY_CTRL_ENABLE |    |                                          |
| NONE                                |    |    |    |    | R/W                                   |    |                                          |
| 0h                                  |    |    |    |    | 7h                                    |    |                                          |

**Table 2-929. MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                                 | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | MSS_TPTC_A1_WR_BUS_SAFETY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                                 | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | MSS_TPTC_A1_WR_BUS_SAFETY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 7:3   | RESERVED                                 | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

**Table 2-929. MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_CTRL Register Field Descriptions  
(continued)**

| Bit | Field                                         | Type | Reset | Description                                                                                                                                           |
|-----|-----------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0 | MSS_TPTC_A1_WR_BU<br>S_SAFETY_CTRL_ENAB<br>LE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.310 MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_FI Register (Offset = 18404h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of TPTC01\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-930. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8404h       |

**Figure 2-310. MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_FI Name Register**

| 31                                | 30                               | 29                               | 28                                           | 27                                           | 26                                       | 25                                       | 24  |
|-----------------------------------|----------------------------------|----------------------------------|----------------------------------------------|----------------------------------------------|------------------------------------------|------------------------------------------|-----|
| MSS_TPTC_A1_WR_BUS_SAFETY_FI_SAFE |                                  |                                  |                                              |                                              |                                          |                                          |     |
| R/W                               |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 0h                                |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 23                                | 22                               | 21                               | 20                                           | 19                                           | 18                                       | 17                                       | 16  |
| MSS_TPTC_A1_WR_BUS_SAFETY_FI_MAIN |                                  |                                  |                                              |                                              |                                          |                                          |     |
| R/W                               |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 0h                                |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 15                                | 14                               | 13                               | 12                                           | 11                                           | 10                                       | 9                                        | 8   |
| MSS_TPTC_A1_WR_BUS_SAFETY_FI_DATA |                                  |                                  |                                              |                                              |                                          |                                          |     |
| R/W                               |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 0h                                |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 7                                 | 6                                | 5                                | 4                                            | 3                                            | 2                                        | 1                                        | 0   |
| RESERVED                          | MSS_TPTC_A1_WR_BUS_SAFETY_FI_DED | MSS_TPTC_A1_WR_BUS_SAFETY_FI_SEC | MSS_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | MSS_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | MSS_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_SAFE | MSS_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_MAIN |     |
| NONE                              | R/W                              | R/W                              | R/W                                          | R/W                                          | R/W                                      | R/W                                      | R/W |
| 0h                                | 0h                               | 0h                               | 0h                                           | 0h                                           | 0h                                       | 0h                                       | 0h  |

**Table 2-932. MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                             | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-----------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_TPTC_A1_WR_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_TPTC_A1_WR_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_TPTC_A1_WR_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                          | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5     | MSS_TPTC_A1_WR_BUS_SAFETY_FI_DED  | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                                                                                                                                                                                                        |



**Table 2-932. MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_FI Register Field Descriptions (continued)**

| Bit | Field                                        | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|----------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | MSS_TPTC_A1_WR_BUS_SAFETY_FI_SEC             | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

### 2.2.2.311 MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR Register (Offset = 18408h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of TPTC01\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-933. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8408h       |

**Figure 2-311. MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR Name Register**

|                                          |    |    |    |    |    |    |    |
|------------------------------------------|----|----|----|----|----|----|----|
| 31                                       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_TPTC_A1_WR_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |
| 23                                       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_TPTC_A1_WR_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |
| 15                                       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_TPTC_A1_WR_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |
| 7                                        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_TPTC_A1_WR_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |

**Table 2-935. MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                                            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_TPTC_A1_WR_BU<br>S_SAFETY_ERR_DED            | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_TPTC_A1_WR_BU<br>S_SAFETY_ERR_SEC            | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_TPTC_A1_WR_BU<br>S_SAFETY_ERR_COMP_<br>CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-935. MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR Register Field Descriptions  
(continued)**

| Bit | Field                                          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_TPTC_A1_WR_BU<br>S_SAFETY_ERR_COMP_<br>ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.312 MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 1840Ch) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of TPTC01\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-936. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 840Ch       |

**Figure 2-312. MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                                    |    |    |    |    |    |    |    |
| NONE                                        |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                                    |    |    |    |    |    |    |    |
| NONE                                        |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-938. MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                       | Type | Reset | Description                                                                                                                                                |
|-------|---------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                                    | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.313 MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

#### 1 MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 18410h) [reset = 0h]

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of TPTC01\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-939. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8410h       |

**Figure 2-313. MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-941. MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                       | Type | Reset | Description                                                                                                                       |
|------|---------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.314 MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register

#### 1 MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register (Offset = 18414h) [reset = 0h]

This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of TPTC01\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-942. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8414h       |

**Figure 2-314. MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Name Register**

|                                               |    |    |    |    |    |    |    |
|-----------------------------------------------|----|----|----|----|----|----|----|
| 31                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 23                                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 15                                            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 7                                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |

**Table 2-944. MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register Field Descriptions**

| Bit  | Field                                         | Type | Reset | Description                                                                                                        |
|------|-----------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT | R    | 0h    | Read this bitfield for comparator status for Write bus for this port. 1'b1 at any bit indicates error on Write Bus |

### 2.2.2.315 MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register

#### 1 MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register (Offset = 18418h) [reset = 0h]

This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of TPTC01\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-945. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8418h       |

**Figure 2-315. MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Name Register**

|                                                   |    |    |    |    |    |    |    |
|---------------------------------------------------|----|----|----|----|----|----|----|
| 31                                                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                 |    |    |    |    |    |    |    |
| 0h                                                |    |    |    |    |    |    |    |
| 23                                                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                 |    |    |    |    |    |    |    |
| 0h                                                |    |    |    |    |    |    |    |
| 15                                                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                 |    |    |    |    |    |    |    |
| 0h                                                |    |    |    |    |    |    |    |
| 7                                                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                 |    |    |    |    |    |    |    |
| 0h                                                |    |    |    |    |    |    |    |

**Table 2-947. MSS\_CTRL\_MSS\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register Field Descriptions**

| Bit  | Field                                                     | Type | Reset | Description                                                                                                                           |
|------|-----------------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_TPTC_A1_WR_BU<br>S_SAFETY_ERR_STAT_<br>WRITERESP_STAT | R    | 0h    | Read this bitfield for comparator status for Write response bus for this port. 1'b1 at any bit indicates error on Write Response Bus. |

### 2.2.2.316 MSS\_CTRL\_HSM\_TPTC\_A0\_RD\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_HSM\_TPTC\_A0\_RD\_BUS\_SAFETY\_CTRL Register (Offset = 18420h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of HSM\_TPTC0\_RD Initiator Port.

Return to [Summary Table](#)

**Table 2-948. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8420h       |

**Figure 2-316. MSS\_CTRL\_HSM\_TPTC\_A0\_RD\_BUS\_SAFETY\_CTRL Name Register**

|                                     |    |    |    |    |                                       |    |                                          |
|-------------------------------------|----|----|----|----|---------------------------------------|----|------------------------------------------|
| 31                                  | 30 | 29 | 28 | 27 | 26                                    | 25 | 24                                       |
| RESERVED                            |    |    |    |    |                                       |    |                                          |
| NONE                                |    |    |    |    |                                       |    |                                          |
| 0h                                  |    |    |    |    |                                       |    |                                          |
| 23                                  | 22 | 21 | 20 | 19 | 18                                    | 17 | 16                                       |
| HSM_TPTC_A0_RD_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                       |    |                                          |
| R                                   |    |    |    |    |                                       |    |                                          |
| 0h                                  |    |    |    |    |                                       |    |                                          |
| 15                                  | 14 | 13 | 12 | 11 | 10                                    | 9  | 8                                        |
| RESERVED                            |    |    |    |    |                                       |    | HSM_TPTC_A0_RD_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                                |    |    |    |    |                                       |    | R/W                                      |
| 0h                                  |    |    |    |    |                                       |    | 0h                                       |
| 7                                   | 6  | 5  | 4  | 3  | 2                                     | 1  | 0                                        |
| RESERVED                            |    |    |    |    | HSM_TPTC_A0_RD_BUS_SAFETY_CTRL_ENABLE |    |                                          |
| NONE                                |    |    |    |    | R/W                                   |    |                                          |
| 0h                                  |    |    |    |    | 7h                                    |    |                                          |

**Table 2-950. MSS\_CTRL\_HSM\_TPTC\_A0\_RD\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                                 | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | HSM_TPTC_A0_RD_BUS_SAFETY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                                 | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | HSM_TPTC_A0_RD_BUS_SAFETY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |



**Table 2-950. MSS\_CTRL\_HSM\_TPTC\_A0\_RD\_BUS\_SAFETY\_CTRL Register Field Descriptions  
(continued)**

| Bit | Field                                 | Type | Reset | Description                                                                                                                                           |
|-----|---------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:3 | RESERVED                              | NONE | 0h    | Reserved                                                                                                                                              |
| 2:0 | HSM_TPTC_A0_RD_BUS_SAFETY_CTRL_ENABLE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.317 MSS\_CTRL\_HSM\_TPTC\_A0\_RD\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_HSM\_TPTC\_A0\_RD\_BUS\_SAFETY\_FI Register (Offset = 18424h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of HSM\_TPTC0\_RD Initiator Port.

Return to [Summary Table](#)

**Table 2-951. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8424h       |

**Figure 2-317. MSS\_CTRL\_HSM\_TPTC\_A0\_RD\_BUS\_SAFETY\_FI Name Register**

| 31                                | 30                               | 29                               | 28                                           | 27                                           | 26                                       | 25                                       | 24  |
|-----------------------------------|----------------------------------|----------------------------------|----------------------------------------------|----------------------------------------------|------------------------------------------|------------------------------------------|-----|
| HSM_TPTC_A0_RD_BUS_SAFETY_FI_SAFE |                                  |                                  |                                              |                                              |                                          |                                          |     |
| R/W                               |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 0h                                |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 23                                | 22                               | 21                               | 20                                           | 19                                           | 18                                       | 17                                       | 16  |
| HSM_TPTC_A0_RD_BUS_SAFETY_FI_MAIN |                                  |                                  |                                              |                                              |                                          |                                          |     |
| R/W                               |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 0h                                |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 15                                | 14                               | 13                               | 12                                           | 11                                           | 10                                       | 9                                        | 8   |
| HSM_TPTC_A0_RD_BUS_SAFETY_FI_DATA |                                  |                                  |                                              |                                              |                                          |                                          |     |
| R/W                               |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 0h                                |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 7                                 | 6                                | 5                                | 4                                            | 3                                            | 2                                        | 1                                        | 0   |
| RESERVED                          | HSM_TPTC_A0_RD_BUS_SAFETY_FI_DED | HSM_TPTC_A0_RD_BUS_SAFETY_FI_SEC | HSM_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | HSM_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | HSM_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_SAFE | HSM_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_MAIN |     |
| NONE                              | R/W                              | R/W                              | R/W                                          | R/W                                          | R/W                                      | R/W                                      | R/W |
| 0h                                | 0h                               | 0h                               | 0h                                           | 0h                                           | 0h                                       | 0h                                       | 0h  |

**Table 2-953. MSS\_CTRL\_HSM\_TPTC\_A0\_RD\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                             | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-----------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | HSM_TPTC_A0_RD_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | HSM_TPTC_A0_RD_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | HSM_TPTC_A0_RD_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                          | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5     | HSM_TPTC_A0_RD_BUS_SAFETY_FI_DED  | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                                                                                                                                                                                                        |

**Table 2-953. MSS\_CTRL\_HSM\_TPTC\_A0\_RD\_BUS\_SAFETY\_FI Register Field Descriptions (continued)**

| Bit | Field                                        | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|----------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | HSM_TPTC_A0_RD_BUS_SAFETY_FI_SEC             | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | HSM_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | HSM_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | HSM_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | HSM_TPTC_A0_RD_BUS_SAFETY_FI_GLOBAL_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

### 2.2.2.318 MSS\_CTRL\_HSM\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_HSM\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR Register (Offset = 18428h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of HSM\_TPTC0\_RD Initiator Port.

Return to [Summary Table](#)

**Table 2-954. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8428h       |

**Figure 2-318. MSS\_CTRL\_HSM\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR Name Register**

|                                          |    |    |    |    |    |    |    |
|------------------------------------------|----|----|----|----|----|----|----|
| 31                                       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HSM_TPTC_A0_RD_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |
| 23                                       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HSM_TPTC_A0_RD_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |
| 15                                       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HSM_TPTC_A0_RD_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |
| 7                                        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HSM_TPTC_A0_RD_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |

**Table 2-956. MSS\_CTRL\_HSM\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                                    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | HSM_TPTC_A0_RD_BUS_SAFETY_ERR_DED        | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | HSM_TPTC_A0_RD_BUS_SAFETY_ERR_SEC        | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | HSM_TPTC_A0_RD_BUS_SAFETY_ERR_COMP_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-956. MSS\_CTRL\_HSM\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR Register Field Descriptions  
(continued)**

| Bit | Field                                  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|----------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | HSM_TPTC_A0_RD_BUS_SAFETY_ERR_COMP_ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.319 MSS\_CTRL\_HSM\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_HSM\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 1842Ch) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of HSM\_TPTC0\_RD Initiator Port.

Return to [Summary Table](#)

**Table 2-957. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 842Ch       |

**Figure 2-319. MSS\_CTRL\_HSM\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                                    |    |    |    |    |    |    |    |
| NONE                                        |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                                    |    |    |    |    |    |    |    |
| NONE                                        |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-959. MSS\_CTRL\_HSM\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                       | Type | Reset | Description                                                                                                                                                |
|-------|---------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                                    | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.320 MSS\_CTRL\_HSM\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

**1 MSS\_CTRL\_HSM\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 18430h) [reset = 0h]**

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of HSM\_TPTC0\_RD Initiator Port.

Return to [Summary Table](#)

**Table 2-960. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8430h       |

**Figure 2-320. MSS\_CTRL\_HSM\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-962. MSS\_CTRL\_HSM\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                       | Type | Reset | Description                                                                                                                       |
|------|---------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.321 MSS\_CTRL\_HSM\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Register

**1 MSS\_CTRL\_HSM\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Register (Offset = 18434h) [reset = 0h]**

This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of HSM\_TPTC0\_RD Initiator Port.

Return to [Summary Table](#)

**Table 2-963. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8434h       |

**Figure 2-321. MSS\_CTRL\_HSM\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Name Register**

|                                              |    |    |    |    |    |    |    |
|----------------------------------------------|----|----|----|----|----|----|----|
| 31                                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 23                                           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 15                                           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 7                                            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |

**Table 2-965. MSS\_CTRL\_HSM\_TPTC\_A0\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Register Field Descriptions**

| Bit  | Field                                        | Type | Reset | Description                                                                                                                     |
|------|----------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | HSM_TPTC_A0_RD_BUS_SAFETY_ERR_STAT_READ_STAT | R    | 0h    | Read this bitfield for comparator status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus. |



### 2.2.2.322 MSS\_CTRL\_HSM\_TPTC\_A1\_RD\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_HSM\_TPTC\_A1\_RD\_BUS\_SAFETY\_CTRL Register (Offset = 18440h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of HSM\_TPTC1\_RD Initiator Port.

Return to [Summary Table](#)

**Table 2-966. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8440h       |

**Figure 2-322. MSS\_CTRL\_HSM\_TPTC\_A1\_RD\_BUS\_SAFETY\_CTRL Name Register**

|                                     |    |    |    |    |                                       |    |                                          |
|-------------------------------------|----|----|----|----|---------------------------------------|----|------------------------------------------|
| 31                                  | 30 | 29 | 28 | 27 | 26                                    | 25 | 24                                       |
| RESERVED                            |    |    |    |    |                                       |    |                                          |
| NONE                                |    |    |    |    |                                       |    |                                          |
| 0h                                  |    |    |    |    |                                       |    |                                          |
| 23                                  | 22 | 21 | 20 | 19 | 18                                    | 17 | 16                                       |
| HSM_TPTC_A1_RD_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                       |    |                                          |
| R                                   |    |    |    |    |                                       |    |                                          |
| 0h                                  |    |    |    |    |                                       |    |                                          |
| 15                                  | 14 | 13 | 12 | 11 | 10                                    | 9  | 8                                        |
| RESERVED                            |    |    |    |    |                                       |    | HSM_TPTC_A1_RD_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                                |    |    |    |    |                                       |    | R/W                                      |
| 0h                                  |    |    |    |    |                                       |    | 0h                                       |
| 7                                   | 6  | 5  | 4  | 3  | 2                                     | 1  | 0                                        |
| RESERVED                            |    |    |    |    | HSM_TPTC_A1_RD_BUS_SAFETY_CTRL_ENABLE |    |                                          |
| NONE                                |    |    |    |    | R/W                                   |    |                                          |
| 0h                                  |    |    |    |    | 7h                                    |    |                                          |

**Table 2-968. MSS\_CTRL\_HSM\_TPTC\_A1\_RD\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                                 | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | HSM_TPTC_A1_RD_BUS_SAFETY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                                 | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | HSM_TPTC_A1_RD_BUS_SAFETY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

**Table 2-968. MSS\_CTRL\_HSM\_TPTC\_A1\_RD\_BUS\_SAFETY\_CTRL Register Field Descriptions  
(continued)**

| Bit | Field                                 | Type | Reset | Description                                                                                                                                           |
|-----|---------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:3 | RESERVED                              | NONE | 0h    | Reserved                                                                                                                                              |
| 2:0 | HSM_TPTC_A1_RD_BUS_SAFETY_CTRL_ENABLE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.323 MSS\_CTRL\_HSM\_TPTC\_A1\_RD\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_HSM\_TPTC\_A1\_RD\_BUS\_SAFETY\_FI Register (Offset = 18444h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of HSM\_TPTC1\_RD Initiator Port.

Return to [Summary Table](#)

**Table 2-969. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8444h       |

**Figure 2-323. MSS\_CTRL\_HSM\_TPTC\_A1\_RD\_BUS\_SAFETY\_FI Name Register**

| 31                                | 30                               | 29                               | 28                                           | 27                                           | 26                                       | 25                                       | 24  |
|-----------------------------------|----------------------------------|----------------------------------|----------------------------------------------|----------------------------------------------|------------------------------------------|------------------------------------------|-----|
| HSM_TPTC_A1_RD_BUS_SAFETY_FI_SAFE |                                  |                                  |                                              |                                              |                                          |                                          |     |
| R/W                               |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 0h                                |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 23                                | 22                               | 21                               | 20                                           | 19                                           | 18                                       | 17                                       | 16  |
| HSM_TPTC_A1_RD_BUS_SAFETY_FI_MAIN |                                  |                                  |                                              |                                              |                                          |                                          |     |
| R/W                               |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 0h                                |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 15                                | 14                               | 13                               | 12                                           | 11                                           | 10                                       | 9                                        | 8   |
| HSM_TPTC_A1_RD_BUS_SAFETY_FI_DATA |                                  |                                  |                                              |                                              |                                          |                                          |     |
| R/W                               |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 0h                                |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 7                                 | 6                                | 5                                | 4                                            | 3                                            | 2                                        | 1                                        | 0   |
| RESERVED                          | HSM_TPTC_A1_RD_BUS_SAFETY_FI_DED | HSM_TPTC_A1_RD_BUS_SAFETY_FI_SEC | HSM_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | HSM_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | HSM_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_SAFE | HSM_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_MAIN |     |
| NONE                              | R/W                              | R/W                              | R/W                                          | R/W                                          | R/W                                      | R/W                                      | R/W |
| 0h                                | 0h                               | 0h                               | 0h                                           | 0h                                           | 0h                                       | 0h                                       | 0h  |

**Table 2-971. MSS\_CTRL\_HSM\_TPTC\_A1\_RD\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                             | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-----------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | HSM_TPTC_A1_RD_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | HSM_TPTC_A1_RD_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | HSM_TPTC_A1_RD_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                          | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5     | HSM_TPTC_A1_RD_BUS_SAFETY_FI_DED  | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                                                                                                                                                                                                        |

**Table 2-971. MSS\_CTRL\_HSM\_TPTC\_A1\_RD\_BUS\_SAFETY\_FI Register Field Descriptions (continued)**

| Bit | Field                                        | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|----------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | HSM_TPTC_A1_RD_BUS_SAFETY_FI_SEC             | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | HSM_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | HSM_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | HSM_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | HSM_TPTC_A1_RD_BUS_SAFETY_FI_GLOBAL_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

### 2.2.2.324 MSS\_CTRL\_HSM\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_HSM\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR Register (Offset = 18448h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of HSM\_TPTC1\_RD Initiator Port.

Return to [Summary Table](#)

**Table 2-972. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8448h       |

**Figure 2-324. MSS\_CTRL\_HSM\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR Name Register**

|                                          |    |    |    |    |    |    |    |
|------------------------------------------|----|----|----|----|----|----|----|
| 31                                       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HSM_TPTC_A1_RD_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |
| 23                                       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HSM_TPTC_A1_RD_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |
| 15                                       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HSM_TPTC_A1_RD_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |
| 7                                        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HSM_TPTC_A1_RD_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |

**Table 2-974. MSS\_CTRL\_HSM\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                                    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | HSM_TPTC_A1_RD_BUS_SAFETY_ERR_DED        | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | HSM_TPTC_A1_RD_BUS_SAFETY_ERR_SEC        | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | HSM_TPTC_A1_RD_BUS_SAFETY_ERR_COMP_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-974. MSS\_CTRL\_HSM\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR Register Field Descriptions  
(continued)**

| Bit | Field                                  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|----------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | HSM_TPTC_A1_RD_BUS_SAFETY_ERR_COMP_ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.325 MSS\_CTRL\_HSM\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_HSM\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 1844Ch) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of HSM\_TPTC1\_RD Initiator Port.

Return to [Summary Table](#)

**Table 2-975. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 844Ch       |

**Figure 2-325. MSS\_CTRL\_HSM\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                                    |    |    |    |    |    |    |    |
| NONE                                        |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                                    |    |    |    |    |    |    |    |
| NONE                                        |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-977. MSS\_CTRL\_HSM\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                       | Type | Reset | Description                                                                                                                                                |
|-------|---------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                                    | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.326 MSS\_CTRL\_HSM\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

**1 MSS\_CTRL\_HSM\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 18450h) [reset = 0h]**

This register is used to Control and Configure the Interconnect Safety Behaviour of QSPI Target Port.

Return to [Summary Table](#)

**Table 2-978. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8450h       |

**Figure 2-326. MSS\_CTRL\_HSM\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-980. MSS\_CTRL\_HSM\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                       | Type | Reset | Description                                                                                                                       |
|------|---------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |



### 2.2.2.327 MSS\_CTRL\_HSM\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Register

**1 MSS\_CTRL\_HSM\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Register (Offset = 18454h) [reset = 0h]**

This register is used to Inject fault on the Interconnect Safety comparator of QSPI Target Port.

Return to [Summary Table](#)

**Table 2-981. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8454h       |

**Figure 2-327. MSS\_CTRL\_HSM\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Name Register**

|                                              |    |    |    |    |    |    |    |
|----------------------------------------------|----|----|----|----|----|----|----|
| 31                                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 23                                           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 15                                           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 7                                            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |

**Table 2-983. MSS\_CTRL\_HSM\_TPTC\_A1\_RD\_BUS\_SAFETY\_ERR\_STAT\_READ Register Field Descriptions**

| Bit  | Field                                        | Type | Reset | Description                                                                                                                     |
|------|----------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | HSM_TPTC_A1_RD_BUS_SAFETY_ERR_STAT_READ_STAT | R    | 0h    | Read this bitfield for comparator status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus. |

### 2.2.2.328 MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_CTRL Register (Offset = 18460h) [reset = 7h]

This Register provides the Error Status of Bus Safety Comparator of QSPI Target Port.

Return to [Summary Table](#)

**Table 2-984. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8460h       |

**Figure 2-328. MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_CTRL Name Register**

|                                     |    |    |    |    |                                       |    |                                          |
|-------------------------------------|----|----|----|----|---------------------------------------|----|------------------------------------------|
| 31                                  | 30 | 29 | 28 | 27 | 26                                    | 25 | 24                                       |
| RESERVED                            |    |    |    |    |                                       |    |                                          |
| NONE                                |    |    |    |    |                                       |    |                                          |
| 0h                                  |    |    |    |    |                                       |    |                                          |
| 23                                  | 22 | 21 | 20 | 19 | 18                                    | 17 | 16                                       |
| HSM_TPTC_A0_WR_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                       |    |                                          |
| R                                   |    |    |    |    |                                       |    |                                          |
| 0h                                  |    |    |    |    |                                       |    |                                          |
| 15                                  | 14 | 13 | 12 | 11 | 10                                    | 9  | 8                                        |
| RESERVED                            |    |    |    |    |                                       |    | HSM_TPTC_A0_WR_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                                |    |    |    |    |                                       |    | R/W                                      |
| 0h                                  |    |    |    |    |                                       |    | 0h                                       |
| 7                                   | 6  | 5  | 4  | 3  | 2                                     | 1  | 0                                        |
| RESERVED                            |    |    |    |    | HSM_TPTC_A0_WR_BUS_SAFETY_CTRL_ENABLE |    |                                          |
| NONE                                |    |    |    |    | R/W                                   |    |                                          |
| 0h                                  |    |    |    |    | 7h                                    |    |                                          |

**Table 2-986. MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                                 | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | HSM_TPTC_A0_WR_BUS_SAFETY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                                 | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | HSM_TPTC_A0_WR_BUS_SAFETY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 7:3   | RESERVED                                 | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

**Table 2-986. MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_CTRL Register Field Descriptions  
(continued)**

| Bit | Field                                         | Type | Reset | Description                                                                                                                                           |
|-----|-----------------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0 | HSM_TPTC_A0_WR_BU<br>S_SAFETY_CTRL_ENAB<br>LE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.329 MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_FI Register (Offset = 18464h) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of QSPI Target Port.

Return to [Summary Table](#)

**Table 2-987. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8464h       |

**Figure 2-329. MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_FI Name Register**

| 31                                | 30                               | 29                               | 28                                           | 27                                           | 26                                       | 25                                       | 24  |
|-----------------------------------|----------------------------------|----------------------------------|----------------------------------------------|----------------------------------------------|------------------------------------------|------------------------------------------|-----|
| HSM_TPTC_A0_WR_BUS_SAFETY_FI_SAFE |                                  |                                  |                                              |                                              |                                          |                                          |     |
| R/W                               |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 0h                                |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 23                                | 22                               | 21                               | 20                                           | 19                                           | 18                                       | 17                                       | 16  |
| HSM_TPTC_A0_WR_BUS_SAFETY_FI_MAIN |                                  |                                  |                                              |                                              |                                          |                                          |     |
| R/W                               |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 0h                                |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 15                                | 14                               | 13                               | 12                                           | 11                                           | 10                                       | 9                                        | 8   |
| HSM_TPTC_A0_WR_BUS_SAFETY_FI_DATA |                                  |                                  |                                              |                                              |                                          |                                          |     |
| R/W                               |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 0h                                |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 7                                 | 6                                | 5                                | 4                                            | 3                                            | 2                                        | 1                                        | 0   |
| RESERVED                          | HSM_TPTC_A0_WR_BUS_SAFETY_FI_DED | HSM_TPTC_A0_WR_BUS_SAFETY_FI_SEC | HSM_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | HSM_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | HSM_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_SAFE | HSM_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_MAIN |     |
| NONE                              | R/W                              | R/W                              | R/W                                          | R/W                                          | R/W                                      | R/W                                      | R/W |
| 0h                                | 0h                               | 0h                               | 0h                                           | 0h                                           | 0h                                       | 0h                                       | 0h  |

**Table 2-989. MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                             | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-----------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | HSM_TPTC_A0_WR_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | HSM_TPTC_A0_WR_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | HSM_TPTC_A0_WR_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                          | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5     | HSM_TPTC_A0_WR_BUS_SAFETY_FI_DED  | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                                                                                                                                                                                                        |

**Table 2-989. MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_FI Register Field Descriptions (continued)**

| Bit | Field                                        | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|----------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | HSM_TPTC_A0_WR_BUS_SAFETY_FI_SEC             | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | HSM_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | HSM_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | HSM_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | HSM_TPTC_A0_WR_BUS_SAFETY_FI_GLOBAL_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

### 2.2.2.330 MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR Register (Offset = 18468h) [reset = 0h]

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of QSPI Target Port.

Return to [Summary Table](#)

**Table 2-990. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8468h       |

**Figure 2-330. MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR Name Register**

|                                          |    |    |    |    |    |    |    |
|------------------------------------------|----|----|----|----|----|----|----|
| 31                                       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HSM_TPTC_A0_WR_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |
| 23                                       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HSM_TPTC_A0_WR_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |
| 15                                       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HSM_TPTC_A0_WR_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |
| 7                                        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HSM_TPTC_A0_WR_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |

**Table 2-992. MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                                    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | HSM_TPTC_A0_WR_BUS_SAFETY_ERR_DED        | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | HSM_TPTC_A0_WR_BUS_SAFETY_ERR_SEC        | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | HSM_TPTC_A0_WR_BUS_SAFETY_ERR_COMP_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-992. MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR Register Field Descriptions  
(continued)**

| Bit | Field                                          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | HSM_TPTC_A0_WR_BU<br>S_SAFETY_ERR_COMP_<br>ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.331 MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 1846Ch) [reset = 0h]

This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of QSPI Target Port.

Return to [Summary Table](#)

**Table 2-993. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 846Ch       |

**Figure 2-331. MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                                    |    |    |    |    |    |    |    |
| NONE                                        |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                                    |    |    |    |    |    |    |    |
| NONE                                        |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-995. MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                       | Type | Reset | Description                                                                                                                                                |
|-------|---------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                                    | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |



### 2.2.2.332 MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

**1 MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 18470h) [reset = 0h]**

This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of QSPI Target Port.

Return to [Summary Table](#)

**Table 2-996. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8470h       |

**Figure 2-332. MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-998. MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                       | Type | Reset | Description                                                                                                                       |
|------|---------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.333 MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register

#### 1 MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register (Offset = 18474h) [reset = 0h]

This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of QSPI Target Port.

Return to [Summary Table](#)

**Table 2-999. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8474h       |

**Figure 2-333. MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Name Register**

|                                               |    |    |    |    |    |    |    |
|-----------------------------------------------|----|----|----|----|----|----|----|
| 31                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 23                                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 15                                            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 7                                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |

**Table 2-1001. MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register Field Descriptions**

| Bit  | Field                                         | Type | Reset | Description                                                                                                        |
|------|-----------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------|
| 31:0 | HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT | R    | 0h    | Read this bitfield for comparator status for Write bus for this port. 1'b1 at any bit indicates error on Write Bus |

### 2.2.2.334 MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register

#### 1 MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register (Offset = 18478h) [reset = 0h]

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of HSM\_TPTC1\_RD Initiator Port.

Return to [Summary Table](#)

**Table 2-1002. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8478h       |

**Figure 2-334. MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Name Register**

|                                                   |    |    |    |    |    |    |    |
|---------------------------------------------------|----|----|----|----|----|----|----|
| 31                                                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                 |    |    |    |    |    |    |    |
| 0h                                                |    |    |    |    |    |    |    |
| 23                                                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                 |    |    |    |    |    |    |    |
| 0h                                                |    |    |    |    |    |    |    |
| 15                                                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                 |    |    |    |    |    |    |    |
| 0h                                                |    |    |    |    |    |    |    |
| 7                                                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HSM_TPTC_A0_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                 |    |    |    |    |    |    |    |
| 0h                                                |    |    |    |    |    |    |    |

**Table 2-1004. MSS\_CTRL\_HSM\_TPTC\_A0\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register Field Descriptions**

| Bit  | Field                                                     | Type | Reset | Description                                                                                                                           |
|------|-----------------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | HSM_TPTC_A0_WR_BU<br>S_SAFETY_ERR_STAT_<br>WRITERESP_STAT | R    | 0h    | Read this bitfield for comparator status for Write response bus for this port. 1'b1 at any bit indicates error on Write Response Bus. |

### 2.2.2.335 MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_CTRL Register (Offset = 18480h) [reset = 7h]

This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of HSM\_TPTC1\_RD Initiator Port.

Return to [Summary Table](#)

**Table 2-1005. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8480h       |

**Figure 2-335. MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_CTRL Name Register**

|                                     |    |    |    |    |                                       |    |                                          |
|-------------------------------------|----|----|----|----|---------------------------------------|----|------------------------------------------|
| 31                                  | 30 | 29 | 28 | 27 | 26                                    | 25 | 24                                       |
| RESERVED                            |    |    |    |    |                                       |    |                                          |
| NONE                                |    |    |    |    |                                       |    |                                          |
| 0h                                  |    |    |    |    |                                       |    |                                          |
| 23                                  | 22 | 21 | 20 | 19 | 18                                    | 17 | 16                                       |
| HSM_TPTC_A1_WR_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                       |    |                                          |
| R                                   |    |    |    |    |                                       |    |                                          |
| 0h                                  |    |    |    |    |                                       |    |                                          |
| 15                                  | 14 | 13 | 12 | 11 | 10                                    | 9  | 8                                        |
| RESERVED                            |    |    |    |    |                                       |    | HSM_TPTC_A1_WR_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                                |    |    |    |    |                                       |    | R/W                                      |
| 0h                                  |    |    |    |    |                                       |    | 0h                                       |
| 7                                   | 6  | 5  | 4  | 3  | 2                                     | 1  | 0                                        |
| RESERVED                            |    |    |    |    | HSM_TPTC_A1_WR_BUS_SAFETY_CTRL_ENABLE |    |                                          |
| NONE                                |    |    |    |    | R/W                                   |    |                                          |
| 0h                                  |    |    |    |    | 7h                                    |    |                                          |

**Table 2-1007. MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                                 | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | HSM_TPTC_A1_WR_BUS_SAFETY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                                 | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | HSM_TPTC_A1_WR_BUS_SAFETY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

**Table 2-1007. MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_CTRL Register Field Descriptions  
(continued)**

| Bit | Field                                 | Type | Reset | Description                                                                                                                                           |
|-----|---------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:3 | RESERVED                              | NONE | 0h    | Reserved                                                                                                                                              |
| 2:0 | HSM_TPTC_A1_WR_BUS_SAFETY_CTRL_ENABLE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.336 MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_FI Register (Offset = 18484h) [reset = 0h]

This register is used to Control and Configure the Interconnect Safety Behaviour of HSM\_TPTC0\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-1008. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8484h       |

**Figure 2-336. MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_FI Name Register**

| 31                                | 30                               | 29                               | 28                                           | 27                                           | 26                                       | 25                                       | 24  |
|-----------------------------------|----------------------------------|----------------------------------|----------------------------------------------|----------------------------------------------|------------------------------------------|------------------------------------------|-----|
| HSM_TPTC_A1_WR_BUS_SAFETY_FI_SAFE |                                  |                                  |                                              |                                              |                                          |                                          |     |
| R/W                               |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 0h                                |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 23                                | 22                               | 21                               | 20                                           | 19                                           | 18                                       | 17                                       | 16  |
| HSM_TPTC_A1_WR_BUS_SAFETY_FI_MAIN |                                  |                                  |                                              |                                              |                                          |                                          |     |
| R/W                               |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 0h                                |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 15                                | 14                               | 13                               | 12                                           | 11                                           | 10                                       | 9                                        | 8   |
| HSM_TPTC_A1_WR_BUS_SAFETY_FI_DATA |                                  |                                  |                                              |                                              |                                          |                                          |     |
| R/W                               |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 0h                                |                                  |                                  |                                              |                                              |                                          |                                          |     |
| 7                                 | 6                                | 5                                | 4                                            | 3                                            | 2                                        | 1                                        | 0   |
| RESERVED                          | HSM_TPTC_A1_WR_BUS_SAFETY_FI_DED | HSM_TPTC_A1_WR_BUS_SAFETY_FI_SEC | HSM_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | HSM_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | HSM_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_SAFE | HSM_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_MAIN |     |
| NONE                              | R/W                              | R/W                              | R/W                                          | R/W                                          | R/W                                      | R/W                                      | R/W |
| 0h                                | 0h                               | 0h                               | 0h                                           | 0h                                           | 0h                                       | 0h                                       | 0h  |

**Table 2-1010. MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                             | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-----------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | HSM_TPTC_A1_WR_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | HSM_TPTC_A1_WR_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | HSM_TPTC_A1_WR_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                          | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |

**Table 2-1010. MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_FI Register Field Descriptions (continued)**

| Bit | Field                                        | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|----------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | HSM_TPTC_A1_WR_BUS_SAFETY_FI_DED             | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                             |
| 4   | HSM_TPTC_A1_WR_BUS_SAFETY_FI_SEC             | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | HSM_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | HSM_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | HSM_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | HSM_TPTC_A1_WR_BUS_SAFETY_FI_GLOBAL_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

### 2.2.2.337 MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR Register (Offset = 18488h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of HSM\_TPTC0\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-1011. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8488h       |

**Figure 2-337. MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR Name Register**

|                                          |    |    |    |    |    |    |    |
|------------------------------------------|----|----|----|----|----|----|----|
| 31                                       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HSM_TPTC_A1_WR_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |
| 23                                       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HSM_TPTC_A1_WR_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |
| 15                                       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HSM_TPTC_A1_WR_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |
| 7                                        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HSM_TPTC_A1_WR_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                        |    |    |    |    |    |    |    |
| 0h                                       |    |    |    |    |    |    |    |

**Table 2-1013. MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                                    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | HSM_TPTC_A1_WR_BUS_SAFETY_ERR_DED        | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | HSM_TPTC_A1_WR_BUS_SAFETY_ERR_SEC        | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | HSM_TPTC_A1_WR_BUS_SAFETY_ERR_COMP_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |



**Table 2-1013. MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR Register Field Descriptions  
(continued)**

| Bit | Field                                          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | HSM_TPTC_A1_WR_BU<br>S_SAFETY_ERR_COMP_<br>ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.338 MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 1848Ch) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of HSM\_TPTC0\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-1014. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 848Ch       |

**Figure 2-338. MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                                    |    |    |    |    |    |    |    |
| NONE                                        |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                                    |    |    |    |    |    |    |    |
| NONE                                        |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-1016. MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                       | Type | Reset | Description                                                                                                                                                |
|-------|---------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                                    | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.339 MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

#### 1 MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 18490h) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of HSM\_TPTC0\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-1017. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8490h       |

**Figure 2-339. MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-1019. MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                       | Type | Reset | Description                                                                                                                       |
|------|---------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.340 MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register

**1 MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register (Offset = 18494h) [reset = 0h]**

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of HSM\_TPTC0\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-1020. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8494h       |

**Figure 2-340. MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Name Register**

|                                               |    |    |    |    |    |    |    |
|-----------------------------------------------|----|----|----|----|----|----|----|
| 31                                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 23                                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 15                                            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |
| 7                                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                             |    |    |    |    |    |    |    |
| 0h                                            |    |    |    |    |    |    |    |

**Table 2-1022. MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register Field Descriptions**

| Bit  | Field                                         | Type | Reset | Description                                                                                                        |
|------|-----------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------|
| 31:0 | HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITE_STAT | R    | 0h    | Read this bitfield for comparator status for Write bus for this port. 1'b1 at any bit indicates error on Write Bus |

### 2.2.2.341 MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register

#### 1 MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register (Offset = 18498h) [reset = 0h]

This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of HSM\_TPTC0\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-1023. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8498h       |

**Figure 2-341. MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Name Register**

| 31                                                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
|---------------------------------------------------|----|----|----|----|----|----|----|
| HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                 |    |    |    |    |    |    |    |
| 0h                                                |    |    |    |    |    |    |    |
| 23                                                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                 |    |    |    |    |    |    |    |
| 0h                                                |    |    |    |    |    |    |    |
| 15                                                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                 |    |    |    |    |    |    |    |
| 0h                                                |    |    |    |    |    |    |    |
| 7                                                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HSM_TPTC_A1_WR_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                 |    |    |    |    |    |    |    |
| 0h                                                |    |    |    |    |    |    |    |

**Table 2-1025. MSS\_CTRL\_HSM\_TPTC\_A1\_WR\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register Field Descriptions**

| Bit  | Field                                                     | Type | Reset | Description                                                                                                                           |
|------|-----------------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | HSM_TPTC_A1_WR_BU<br>S_SAFETY_ERR_STAT_<br>WRITERESP_STAT | R    | 0h    | Read this bitfield for comparator status for Write response bus for this port. 1'b1 at any bit indicates error on Write Response Bus. |

### 2.2.2.342 MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_CTRL Register (Offset = 184A0h) [reset = 7h]

This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of HSM\_TPTC0\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-1026. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 84A0h       |

**Figure 2-342. MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_CTRL Name Register**

|                               |    |    |    |    |                                 |    |                                               |
|-------------------------------|----|----|----|----|---------------------------------|----|-----------------------------------------------|
| 31                            | 30 | 29 | 28 | 27 | 26                              | 25 | 24                                            |
| RESERVED                      |    |    |    |    |                                 |    |                                               |
| NONE                          |    |    |    |    |                                 |    |                                               |
| 0h                            |    |    |    |    |                                 |    |                                               |
| 23                            | 22 | 21 | 20 | 19 | 18                              | 17 | 16                                            |
| MSS_QSPI_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                 |    |                                               |
| R                             |    |    |    |    |                                 |    |                                               |
| 0h                            |    |    |    |    |                                 |    |                                               |
| 15                            | 14 | 13 | 12 | 11 | 10                              | 9  | 8                                             |
| RESERVED                      |    |    |    |    |                                 |    | MSS_QSPI_B<br>S_SAFETY_CT<br>RL_ERR_CLEA<br>R |
| NONE                          |    |    |    |    |                                 |    | R/W                                           |
| 0h                            |    |    |    |    |                                 |    | 0h                                            |
| 7                             | 6  | 5  | 4  | 3  | 2                               | 1  | 0                                             |
| RESERVED                      |    |    |    |    | MSS_QSPI_BUS_SAFETY_CTRL_ENABLE |    |                                               |
| NONE                          |    |    |    |    | R/W                             |    |                                               |
| 0h                            |    |    |    |    | 7h                              |    |                                               |

**Table 2-1028. MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | MSS_QSPI_BUS_SAFETY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | MSS_QSPI_BUS_SAFETY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 7:3   | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

**Table 2-1028. MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_CTRL Register Field Descriptions (continued)**

| Bit | Field                           | Type | Reset | Description                                                                                                                                           |
|-----|---------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0 | MSS_QSPI_BUS_SAFETY_CTRL_ENABLE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.343 MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_FI Register (Offset = 184A4h) [reset = 0h]

This register is used to Control and Configure the Interconnect Safety Behaviour of HSM\_TPTC1\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-1029. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 84A4h       |

**Figure 2-343. MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_FI Name Register**

| 31                          | 30 | 29                                 | 28                                 | 27                                                 | 26                                                 | 25                                         | 24                                         |
|-----------------------------|----|------------------------------------|------------------------------------|----------------------------------------------------|----------------------------------------------------|--------------------------------------------|--------------------------------------------|
| MSS_QSPI_BUS_SAFETY_FI_SAFE |    |                                    |                                    |                                                    |                                                    |                                            |                                            |
| R/W                         |    |                                    |                                    |                                                    |                                                    |                                            |                                            |
| 0h                          |    |                                    |                                    |                                                    |                                                    |                                            |                                            |
| 23                          | 22 | 21                                 | 20                                 | 19                                                 | 18                                                 | 17                                         | 16                                         |
| MSS_QSPI_BUS_SAFETY_FI_MAIN |    |                                    |                                    |                                                    |                                                    |                                            |                                            |
| R/W                         |    |                                    |                                    |                                                    |                                                    |                                            |                                            |
| 0h                          |    |                                    |                                    |                                                    |                                                    |                                            |                                            |
| 15                          | 14 | 13                                 | 12                                 | 11                                                 | 10                                                 | 9                                          | 8                                          |
| MSS_QSPI_BUS_SAFETY_FI_DATA |    |                                    |                                    |                                                    |                                                    |                                            |                                            |
| R/W                         |    |                                    |                                    |                                                    |                                                    |                                            |                                            |
| 0h                          |    |                                    |                                    |                                                    |                                                    |                                            |                                            |
| 7                           | 6  | 5                                  | 4                                  | 3                                                  | 2                                                  | 1                                          | 0                                          |
| RESERVED                    |    | MSS_QSPI_BU<br>S_SAFETY_FI_<br>DED | MSS_QSPI_BU<br>S_SAFETY_FI_<br>SEC | MSS_QSPI_BU<br>S_SAFETY_FI_<br>GLOBAL_SAFE<br>_REQ | MSS_QSPI_BU<br>S_SAFETY_FI_<br>GLOBAL_MAIN<br>_REQ | MSS_QSPI_BU<br>S_SAFETY_FI_<br>GLOBAL_SAFE | MSS_QSPI_BU<br>S_SAFETY_FI_<br>GLOBAL_MAIN |
| NONE                        |    | R/W                                | R/W                                | R/W                                                | R/W                                                | R/W                                        | R/W                                        |
| 0h                          |    | 0h                                 | 0h                                 | 0h                                                 | 0h                                                 | 0h                                         | 0h                                         |

**Table 2-1031. MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-----------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_QSPI_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_QSPI_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_QSPI_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                    | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5     | MSS_QSPI_BUS_SAFETY_FI_DED  | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                                                                                                                                                                                                        |



**Table 2-1031. MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_FI Register Field Descriptions (continued)**

| Bit | Field                                  | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|----------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | MSS_QSPI_BUS_SAFETY_FI_SEC             | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_QSPI_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit corresponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_QSPI_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit corresponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_QSPI_BUS_SAFETY_FI_GLOBAL_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_QSPI_BUS_SAFETY_FI_GLOBAL_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

### 2.2.2.344 MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_ERR Register (Offset = 184A8h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of HSM\_TPTC1\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-1032. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 84A8h       |

**Figure 2-344. MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_ERR Name Register**

|                                    |    |    |    |    |    |    |    |
|------------------------------------|----|----|----|----|----|----|----|
| 31                                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_QSPI_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |
| 23                                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_QSPI_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |
| 15                                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_QSPI_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |
| 7                                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_QSPI_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |

**Table 2-1034. MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_QSPI_BUS_SAFETY_ERR_DED        | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_QSPI_BUS_SAFETY_ERR_SEC        | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_QSPI_BUS_SAFETY_ERR_COMP_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-1034. MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_ERR Register Field Descriptions (continued)**

| Bit | Field                            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|----------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_QSPI_BUS_SAFETY_ERR_COMP_ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.345 MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 184ACh) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of HSM\_TPTC1\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-1035. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 84ACh       |

**Figure 2-345. MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                       |    |    |    |    |    |    |    |
|---------------------------------------|----|----|----|----|----|----|----|
| 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 23                                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 15                                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_QSPI_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 7                                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_QSPI_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |

**Table 2-1037. MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                 | Type | Reset | Description                                                                                                                                                |
|-------|---------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                              | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_QSPI_BUS_SAFETY_ERR_STAT_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_QSPI_BUS_SAFETY_ERR_STAT_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.346 MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

#### 1 MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 184B0h) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of HSM\_TPTC1\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-1038. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 84B0h       |

**Figure 2-346. MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                       |    |    |    |    |    |    |    |
|---------------------------------------|----|----|----|----|----|----|----|
| 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_QSPI_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 23                                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_QSPI_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 15                                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_QSPI_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 7                                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_QSPI_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |

**Table 2-1040. MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                 | Type | Reset | Description                                                                                                                       |
|------|---------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_QSPI_BUS_SAFETY_ERR_STAT_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.347 MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register

#### 1 MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register (Offset = 184B4h) [reset = 0h]

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of HSM\_TPTC1\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-1041. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 84B4h       |

**Figure 2-347. MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_ERR\_STAT\_WRITE Name Register**

|                                         |    |    |    |    |    |    |    |
|-----------------------------------------|----|----|----|----|----|----|----|
| 31                                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_QSPI_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 23                                      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_QSPI_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 15                                      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_QSPI_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 7                                       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_QSPI_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |

**Table 2-1043. MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register Field Descriptions**

| Bit  | Field                                   | Type | Reset | Description                                                                                                        |
|------|-----------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_QSPI_BUS_SAFETY_ERR_STAT_WRITE_STAT | R    | 0h    | Read this bitfield for comparator status for Write bus for this port. 1'b1 at any bit indicates error on Write Bus |

### 2.2.2.348 MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_ERR\_STAT\_READ Register

#### 1 MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_ERR\_STAT\_READ Register (Offset = 184B8h) [reset = 0h]

This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of HSM\_TPTC1\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-1044. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 84B8h       |

**Figure 2-348. MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_ERR\_STAT\_READ Name Register**

|                                        |    |    |    |    |    |    |    |
|----------------------------------------|----|----|----|----|----|----|----|
| 31                                     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_QSPI_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 23                                     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_QSPI_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 15                                     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_QSPI_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 7                                      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_QSPI_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |

**Table 2-1046. MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_ERR\_STAT\_READ Register Field Descriptions**

| Bit  | Field                                  | Type | Reset | Description                                                                                                                     |
|------|----------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_QSPI_BUS_SAFETY_ERR_STAT_READ_STAT | R    | 0h    | Read this bitfield for comparator status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus. |

### 2.2.2.349 MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register

#### 1 MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register (Offset = 184BCh) [reset = 0h]

This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of HSM\_TPTC1\_WR Initiator Port.

Return to [Summary Table](#)

**Table 2-1047. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 84BCh       |

**Figure 2-349. MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_QSPI_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_QSPI_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_QSPI_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_QSPI_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-1049. MSS\_CTRL\_MSS\_QSPI\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register Field Descriptions**

| Bit  | Field                                       | Type | Reset | Description                                                                                                                           |
|------|---------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_QSPI_BUS_SAFETY_ERR_STAT_WRITERESP_STAT | R    | 0h    | Read this bitfield for comparator status for Write response bus for this port. 1'b1 at any bit indicates error on Write Response Bus. |



### 2.2.2.350 MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_CTRL Register (Offset = 18540h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of MCRC Target Port.

Return to [Summary Table](#)

**Table 2-1050. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8540h       |

**Figure 2-350. MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_CTRL Name Register**

|                               |    |    |    |    |                                 |    |                                                |
|-------------------------------|----|----|----|----|---------------------------------|----|------------------------------------------------|
| 31                            | 30 | 29 | 28 | 27 | 26                              | 25 | 24                                             |
| RESERVED                      |    |    |    |    |                                 |    |                                                |
| NONE                          |    |    |    |    |                                 |    |                                                |
| 0h                            |    |    |    |    |                                 |    |                                                |
| 23                            | 22 | 21 | 20 | 19 | 18                              | 17 | 16                                             |
| MSS_MCRC_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                 |    |                                                |
| R                             |    |    |    |    |                                 |    |                                                |
| 0h                            |    |    |    |    |                                 |    |                                                |
| 15                            | 14 | 13 | 12 | 11 | 10                              | 9  | 8                                              |
| RESERVED                      |    |    |    |    |                                 |    | MSS_MCRC_B<br>US_SAFETY_C<br>TRL_ERR_CLE<br>AR |
| NONE                          |    |    |    |    |                                 |    | R/W                                            |
| 0h                            |    |    |    |    |                                 |    | 0h                                             |
| 7                             | 6  | 5  | 4  | 3  | 2                               | 1  | 0                                              |
| RESERVED                      |    |    |    |    | MSS_MCRC_BUS_SAFETY_CTRL_ENABLE |    |                                                |
| NONE                          |    |    |    |    | R/W                             |    |                                                |
| 0h                            |    |    |    |    | 7h                              |    |                                                |

**Table 2-1052. MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|----------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                               | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 23:16 | MSS_MCRC_BUS_SAFE<br>TY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/ initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/ initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/ initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                               | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 8     | MSS_MCRC_BUS_SAFE<br>TY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 7:3   | RESERVED                               | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

**Table 2-1052. MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_CTRL Register Field Descriptions (continued)**

| Bit | Field                           | Type | Reset | Description                                                                                                                                           |
|-----|---------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0 | MSS_MCRC_BUS_SAFETY_CTRL_ENABLE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.351 MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_FI Register (Offset = 18544h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of MCRC Target Port.

Return to [Summary Table](#)

**Table 2-1053. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8544h       |

**Figure 2-351. MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_FI Name Register**

| 31                          | 30                                 | 29                                 | 28                                                 | 27                                                 | 26                                             | 25                                             | 24                                             |
|-----------------------------|------------------------------------|------------------------------------|----------------------------------------------------|----------------------------------------------------|------------------------------------------------|------------------------------------------------|------------------------------------------------|
| MSS_MCRC_BUS_SAFETY_FI_SAFE |                                    |                                    |                                                    |                                                    |                                                |                                                |                                                |
| R/W                         |                                    |                                    |                                                    |                                                    |                                                |                                                |                                                |
| 0h                          |                                    |                                    |                                                    |                                                    |                                                |                                                |                                                |
| 23                          | 22                                 | 21                                 | 20                                                 | 19                                                 | 18                                             | 17                                             | 16                                             |
| MSS_MCRC_BUS_SAFETY_FI_MAIN |                                    |                                    |                                                    |                                                    |                                                |                                                |                                                |
| R/W                         |                                    |                                    |                                                    |                                                    |                                                |                                                |                                                |
| 0h                          |                                    |                                    |                                                    |                                                    |                                                |                                                |                                                |
| 15                          | 14                                 | 13                                 | 12                                                 | 11                                                 | 10                                             | 9                                              | 8                                              |
| MSS_MCRC_BUS_SAFETY_FI_DATA |                                    |                                    |                                                    |                                                    |                                                |                                                |                                                |
| R/W                         |                                    |                                    |                                                    |                                                    |                                                |                                                |                                                |
| 0h                          |                                    |                                    |                                                    |                                                    |                                                |                                                |                                                |
| 7                           | 6                                  | 5                                  | 4                                                  | 3                                                  | 2                                              | 1                                              | 0                                              |
| RESERVED                    | MSS_MCRC_B<br>US_SAFETY_F<br>I_DED | MSS_MCRC_B<br>US_SAFETY_F<br>I_SEC | MSS_MCRC_B<br>US_SAFETY_F<br>I_GLOBAL_SA<br>FE_REQ | MSS_MCRC_B<br>US_SAFETY_F<br>I_GLOBAL_MAI<br>N_REQ | MSS_MCRC_B<br>US_SAFETY_F<br>I_GLOBAL_SA<br>FE | MSS_MCRC_B<br>US_SAFETY_F<br>I_GLOBAL_MAI<br>N | MSS_MCRC_B<br>US_SAFETY_F<br>I_GLOBAL_MAI<br>N |
| NONE                        | R/W                                | R/W                                | R/W                                                | R/W                                                | R/W                                            | R/W                                            | R/W                                            |
| 0h                          | 0h                                 | 0h                                 | 0h                                                 | 0h                                                 | 0h                                             | 0h                                             | 0h                                             |

**Table 2-1055. MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|---------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_MCRC_BUS_SAFE<br>TY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7- Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_MCRC_BUS_SAFE<br>TY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7- Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_MCRC_BUS_SAFE<br>TY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                        |
| 7:6   | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 5     | MSS_MCRC_BUS_SAFE<br>TY_FI_DED  | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                                                                                                                                                                                                       |

**Table 2-1055. MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_FI Register Field Descriptions (continued)**

| Bit | Field                                          | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|------------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | MSS_MCRC_BUS_SAFE<br>TY_FI_SEC                 | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_MCRC_BUS_SAFE<br>TY_FI_GLOBAL_SAFE_R<br>EQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_MCRC_BUS_SAFE<br>TY_FI_GLOBAL_MAIN_R<br>EQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_MCRC_BUS_SAFE<br>TY_FI_GLOBAL_SAFE         | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_MCRC_BUS_SAFE<br>TY_FI_GLOBAL_MAIN         | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

### 2.2.2.352 MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_ERR Register (Offset = 18548h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of MCRC Target Port.

Return to [Summary Table](#)

**Table 2-1056. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8548h       |

**Figure 2-352. MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_ERR Name Register**

|                                    |    |    |    |    |    |    |    |
|------------------------------------|----|----|----|----|----|----|----|
| 31                                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_MCRC_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |
| 23                                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_MCRC_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |
| 15                                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_MCRC_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |
| 7                                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_MCRC_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |

**Table 2-1058. MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_MCRC_BUS_SAFETY_ERR_DED        | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_MCRC_BUS_SAFETY_ERR_SEC        | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_MCRC_BUS_SAFETY_ERR_COMP_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-1058. MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_ERR Register Field Descriptions (continued)**

| Bit | Field                            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|----------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_MCRC_BUS_SAFETY_ERR_COMP_ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.353 MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 1854Ch) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of MCRC Target Port.

Return to [Summary Table](#)

**Table 2-1059. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 854Ch       |

**Figure 2-353. MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                       |    |    |    |    |    |    |    |
|---------------------------------------|----|----|----|----|----|----|----|
| 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 23                                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 15                                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_MCRC_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 7                                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_MCRC_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |

**Table 2-1061. MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                 | Type | Reset | Description                                                                                                                                                |
|-------|---------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                              | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_MCRC_BUS_SAFETY_ERR_STAT_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_MCRC_BUS_SAFETY_ERR_STAT_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.354 MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

#### 1 MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 18550h) [reset = 0h]

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of MCRC Target Port.

Return to [Summary Table](#)

**Table 2-1062. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8550h       |

**Figure 2-354. MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                       |    |    |    |    |    |    |    |
|---------------------------------------|----|----|----|----|----|----|----|
| 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_MCRC_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 23                                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_MCRC_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 15                                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_MCRC_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 7                                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_MCRC_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |

**Table 2-1064. MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                 | Type | Reset | Description                                                                                                                       |
|------|---------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_MCRC_BUS_SAFETY_ERR_STAT_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |



### 2.2.2.355 MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register

#### 1 MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register (Offset = 18554h) [reset = 0h]

This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of MCRC Target Port.

Return to [Summary Table](#)

**Table 2-1065. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8554h       |

**Figure 2-355. MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_ERR\_STAT\_WRITE Name Register**

|                                         |    |    |    |    |    |    |    |
|-----------------------------------------|----|----|----|----|----|----|----|
| 31                                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_MCRC_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 23                                      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_MCRC_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 15                                      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_MCRC_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 7                                       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_MCRC_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |

**Table 2-1067. MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register Field Descriptions**

| Bit  | Field                                   | Type | Reset | Description                                                                                                        |
|------|-----------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_MCRC_BUS_SAFETY_ERR_STAT_WRITE_STAT | R    | 0h    | Read this bitfield for comparator status for Write bus for this port. 1'b1 at any bit indicates error on Write Bus |

### 2.2.2.356 MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_ERR\_STAT\_READ Register

#### 1 MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_ERR\_STAT\_READ Register (Offset = 18558h) [reset = 0h]

This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of MCRC Target Port.

Return to [Summary Table](#)

**Table 2-1068. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8558h       |

**Figure 2-356. MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_ERR\_STAT\_READ Name Register**

|                                        |    |    |    |    |    |    |    |
|----------------------------------------|----|----|----|----|----|----|----|
| 31                                     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_MCRC_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 23                                     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_MCRC_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 15                                     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_MCRC_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 7                                      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_MCRC_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |

**Table 2-1070. MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_ERR\_STAT\_READ Register Field Descriptions**

| Bit  | Field                                  | Type | Reset | Description                                                                                                                     |
|------|----------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_MCRC_BUS_SAFETY_ERR_STAT_READ_STAT | R    | 0h    | Read this bitfield for comparator status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus. |

### 2.2.2.357 MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register

#### 1 MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register (Offset = 1855Ch) [reset = 0h]

This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of MCRC Target Port.

Return to [Summary Table](#)

**Table 2-1071. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 855Ch       |

**Figure 2-357. MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_MCRC_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_MCRC_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_MCRC_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_MCRC_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-1073. MSS\_CTRL\_MSS\_MCRC\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register Field Descriptions**

| Bit  | Field                                       | Type | Reset | Description                                                                                                                           |
|------|---------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_MCRC_BUS_SAFETY_ERR_STAT_WRITERESP_STAT | R    | 0h    | Read this bitfield for comparator status for Write response bus for this port. 1'b1 at any bit indicates error on Write Response Bus. |

### 2.2.2.358 MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_CTRL Register (Offset = 185E0h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of ICSSM Target Port.

Return to [Summary Table](#)

**Table 2-1074. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 85E0h       |

**Figure 2-358. MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_CTRL Name Register**

|                                    |    |    |    |    |                                      |    |                                         |
|------------------------------------|----|----|----|----|--------------------------------------|----|-----------------------------------------|
| 31                                 | 30 | 29 | 28 | 27 | 26                                   | 25 | 24                                      |
| RESERVED                           |    |    |    |    |                                      |    |                                         |
| NONE                               |    |    |    |    |                                      |    |                                         |
| 0h                                 |    |    |    |    |                                      |    |                                         |
| 23                                 | 22 | 21 | 20 | 19 | 18                                   | 17 | 16                                      |
| PRU_ICSSSLAVE_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                      |    |                                         |
| R                                  |    |    |    |    |                                      |    |                                         |
| 0h                                 |    |    |    |    |                                      |    |                                         |
| 15                                 | 14 | 13 | 12 | 11 | 10                                   | 9  | 8                                       |
| RESERVED                           |    |    |    |    |                                      |    | PRU_ICSSSLAVE_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                               |    |    |    |    |                                      |    | R/W                                     |
| 0h                                 |    |    |    |    |                                      |    | 0h                                      |
| 7                                  | 6  | 5  | 4  | 3  | 2                                    | 1  | 0                                       |
| RESERVED                           |    |    |    |    | PRU_ICSSSLAVE_BUS_SAFETY_CTRL_ENABLE |    |                                         |
| NONE                               |    |    |    |    | R/W                                  |    |                                         |
| 0h                                 |    |    |    |    | 7h                                   |    |                                         |

**Table 2-1076. MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|-----------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                                | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | PRU_ICSSSLAVE_BUS_SAFETY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                                | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | PRU_ICSSSLAVE_BUS_SAFETY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 7:3   | RESERVED                                | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

**Table 2-1076. MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_CTRL Register Field Descriptions  
(continued)**

| Bit | Field                                | Type | Reset | Description                                                                                                                                           |
|-----|--------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0 | PRU_ICSSSLAVE_BUS_SAFETY_CTRL_ENABLE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.359 MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_FI Register (Offset = 185E4h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of ICSSM Target Port.

Return to [Summary Table](#)

**Table 2-1077. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 85E4h       |

**Figure 2-359. MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_FI Name Register**

| 31                               | 30                              | 29                              | 28                                          | 27                                          | 26                                      | 25                                      | 24                                      |
|----------------------------------|---------------------------------|---------------------------------|---------------------------------------------|---------------------------------------------|-----------------------------------------|-----------------------------------------|-----------------------------------------|
| PRU_ICSSSLAVE_BUS_SAFETY_FI_SAFE |                                 |                                 |                                             |                                             |                                         |                                         |                                         |
| R/W                              |                                 |                                 |                                             |                                             |                                         |                                         |                                         |
| 0h                               |                                 |                                 |                                             |                                             |                                         |                                         |                                         |
| 23                               | 22                              | 21                              | 20                                          | 19                                          | 18                                      | 17                                      | 16                                      |
| PRU_ICSSSLAVE_BUS_SAFETY_FI_MAIN |                                 |                                 |                                             |                                             |                                         |                                         |                                         |
| R/W                              |                                 |                                 |                                             |                                             |                                         |                                         |                                         |
| 0h                               |                                 |                                 |                                             |                                             |                                         |                                         |                                         |
| 15                               | 14                              | 13                              | 12                                          | 11                                          | 10                                      | 9                                       | 8                                       |
| PRU_ICSSSLAVE_BUS_SAFETY_FI_DATA |                                 |                                 |                                             |                                             |                                         |                                         |                                         |
| R/W                              |                                 |                                 |                                             |                                             |                                         |                                         |                                         |
| 0h                               |                                 |                                 |                                             |                                             |                                         |                                         |                                         |
| 7                                | 6                               | 5                               | 4                                           | 3                                           | 2                                       | 1                                       | 0                                       |
| RESERVED                         | PRU_ICSSSLAVE_BUS_SAFETY_FI_DED | PRU_ICSSSLAVE_BUS_SAFETY_FI_SEC | PRU_ICSSSLAVE_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | PRU_ICSSSLAVE_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | PRU_ICSSSLAVE_BUS_SAFETY_FI_GLOBAL_SAFE | PRU_ICSSSLAVE_BUS_SAFETY_FI_GLOBAL_MAIN | PRU_ICSSSLAVE_BUS_SAFETY_FI_GLOBAL_MAIN |
| NONE                             | R/W                             | R/W                             | R/W                                         | R/W                                         | R/W                                     | R/W                                     | R/W                                     |
| 0h                               | 0h                              | 0h                              | 0h                                          | 0h                                          | 0h                                      | 0h                                      | 0h                                      |

**Table 2-1079. MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|----------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | PRU_ICSSSLAVE_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | PRU_ICSSSLAVE_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | PRU_ICSSSLAVE_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5     | PRU_ICSSSLAVE_BUS_SAFETY_FI_DED  | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                                                                                                                                                                                                        |

**Table 2-1079. MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_FI Register Field Descriptions (continued)**

| Bit | Field                                       | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|---------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | PRU_ICSSSLAVE_BUS_SAFETY_FI_SEC             | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | PRU_ICSSSLAVE_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | PRU_ICSSSLAVE_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | PRU_ICSSSLAVE_BUS_SAFETY_FI_GLOBAL_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | PRU_ICSSSLAVE_BUS_SAFETY_FI_GLOBAL_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

### 2.2.2.360 MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_ERR Register (Offset = 185E8h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of ICSSM Target Port.

Return to [Summary Table](#)

**Table 2-1080. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 85E8h       |

**Figure 2-360. MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_ERR Name Register**

|                                         |    |    |    |    |    |    |    |
|-----------------------------------------|----|----|----|----|----|----|----|
| 31                                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PRU_ICSSSLAVE_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 23                                      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PRU_ICSSSLAVE_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 15                                      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PRU_ICSSSLAVE_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 7                                       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PRU_ICSSSLAVE_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |

**Table 2-1082. MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                                   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|-----------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | PRU_ICSSSLAVE_BUS_SAFETY_ERR_DED        | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | PRU_ICSSSLAVE_BUS_SAFETY_ERR_SEC        | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | PRU_ICSSSLAVE_BUS_SAFETY_ERR_COMP_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |



**Table 2-1082. MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_ERR Register Field Descriptions (continued)**

| Bit | Field                                 | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|---------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | PRU_ICSSSLAVE_BUS_SAFETY_ERR_COMP_ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.361 MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

**1 MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 185ECh) [reset = 0h]**

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of ICSSM Target Port.

Return to [Summary Table](#)

**Table 2-1083. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 85ECh       |

**Figure 2-361. MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                            |    |    |    |    |    |    |    |
|--------------------------------------------|----|----|----|----|----|----|----|
| 31                                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                                   |    |    |    |    |    |    |    |
| NONE                                       |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 23                                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                                   |    |    |    |    |    |    |    |
| NONE                                       |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 15                                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PRU_ICSSSLAVE_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 7                                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PRU_ICSSSLAVE_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |

**Table 2-1085. MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                      | Type | Reset | Description                                                                                                                                                |
|-------|--------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                                   | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | PRU_ICSSSLAVE_BUS_SAFETY_ERR_STAT_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | PRU_ICSSSLAVE_BUS_SAFETY_ERR_STAT_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.362 MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

#### 1 MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 185F0h) [reset = 0h]

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of ICSSM Target Port.

Return to [Summary Table](#)

**Table 2-1086. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 85F0h       |

**Figure 2-362. MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                            |    |    |    |    |    |    |    |
|--------------------------------------------|----|----|----|----|----|----|----|
| 31                                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PRU_ICSSSLAVE_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 23                                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PRU_ICSSSLAVE_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 15                                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PRU_ICSSSLAVE_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 7                                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PRU_ICSSSLAVE_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |

**Table 2-1088. MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                      | Type | Reset | Description                                                                                                                       |
|------|--------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PRU_ICSSSLAVE_BUS_SAFETY_ERR_STAT_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.363 MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register

**1 MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register (Offset = 185F4h) [reset = 0h]**

This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of ICSSM Target Port.

Return to [Summary Table](#)

**Table 2-1089. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 85F4h       |

**Figure 2-363. MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_ERR\_STAT\_WRITE Name Register**

|                                              |    |    |    |    |    |    |    |
|----------------------------------------------|----|----|----|----|----|----|----|
| 31                                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PRU_ICSSSLAVE_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 23                                           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PRU_ICSSSLAVE_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 15                                           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PRU_ICSSSLAVE_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 7                                            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PRU_ICSSSLAVE_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |

**Table 2-1091. MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register Field Descriptions**

| Bit  | Field                                        | Type | Reset | Description                                                                                                        |
|------|----------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------|
| 31:0 | PRU_ICSSSLAVE_BUS_SAFETY_ERR_STAT_WRITE_STAT | R    | 0h    | Read this bitfield for comparator status for Write bus for this port. 1'b1 at any bit indicates error on Write Bus |

### 2.2.2.364 MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_ERR\_STAT\_READ Register

#### 1 MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_ERR\_STAT\_READ Register (Offset = 185F8h) [reset = 0h]

This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of ICSSM Target Port.

Return to [Summary Table](#)

**Table 2-1092. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 85F8h       |

**Figure 2-364. MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_ERR\_STAT\_READ Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PRU_ICSSSLAVE_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PRU_ICSSSLAVE_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PRU_ICSSSLAVE_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PRU_ICSSSLAVE_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-1094. MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_ERR\_STAT\_READ Register Field Descriptions**

| Bit  | Field                                       | Type | Reset | Description                                                                                                                     |
|------|---------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PRU_ICSSSLAVE_BUS_SAFETY_ERR_STAT_READ_STAT | R    | 0h    | Read this bitfield for comparator status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus. |

### 2.2.2.365 MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register

#### 1 MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register (Offset = 185FCh) [reset = 0h]

This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of ICSSM Target Port.

Return to [Summary Table](#)

**Table 2-1095. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 85FCh       |

**Figure 2-365. MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Name Register**

|                                                  |    |    |    |    |    |    |    |
|--------------------------------------------------|----|----|----|----|----|----|----|
| 31                                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PRU_ICSSSLAVE_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                |    |    |    |    |    |    |    |
| 0h                                               |    |    |    |    |    |    |    |
| 23                                               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PRU_ICSSSLAVE_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                |    |    |    |    |    |    |    |
| 0h                                               |    |    |    |    |    |    |    |
| 15                                               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PRU_ICSSSLAVE_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                |    |    |    |    |    |    |    |
| 0h                                               |    |    |    |    |    |    |    |
| 7                                                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PRU_ICSSSLAVE_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                |    |    |    |    |    |    |    |
| 0h                                               |    |    |    |    |    |    |    |

**Table 2-1097. MSS\_CTRL\_PRU\_ICSSSLAVE\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register Field Descriptions**

| Bit  | Field                                            | Type | Reset | Description                                                                                                                              |
|------|--------------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PRU_ICSSSLAVE_BUS_SAFETY_ERR_STAT_WRITERESP_STAT | R    | 0h    | Read this bitfield for comparator status for Write response bus for this port. 1'b1 at at any bit indicates error on Write Response Bus. |

### 2.2.2.366 MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_CTRL Register (Offset = 18620h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of L2 BANK0 Target Port.

Return to [Summary Table](#)

**Table 2-1098. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8620h       |

**Figure 2-366. MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_CTRL Name Register**

|                               |    |    |    |    |                                 |    |                                    |
|-------------------------------|----|----|----|----|---------------------------------|----|------------------------------------|
| 31                            | 30 | 29 | 28 | 27 | 26                              | 25 | 24                                 |
| RESERVED                      |    |    |    |    |                                 |    |                                    |
| NONE                          |    |    |    |    |                                 |    |                                    |
| 0h                            |    |    |    |    |                                 |    |                                    |
| 23                            | 22 | 21 | 20 | 19 | 18                              | 17 | 16                                 |
| MSS_L2_A_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                 |    |                                    |
| R                             |    |    |    |    |                                 |    |                                    |
| 0h                            |    |    |    |    |                                 |    |                                    |
| 15                            | 14 | 13 | 12 | 11 | 10                              | 9  | 8                                  |
| RESERVED                      |    |    |    |    |                                 |    | MSS_L2_A_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                          |    |    |    |    |                                 |    | R/W                                |
| 0h                            |    |    |    |    |                                 |    | 0h                                 |
| 7                             | 6  | 5  | 4  | 3  | 2                               | 1  | 0                                  |
| RESERVED                      |    |    |    |    | MSS_L2_A_BUS_SAFETY_CTRL_ENABLE |    |                                    |
| NONE                          |    |    |    |    | R/W                             |    |                                    |
| 0h                            |    |    |    |    | 7h                              |    |                                    |

**Table 2-1100. MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | MSS_L2_A_BUS_SAFETY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | MSS_L2_A_BUS_SAFETY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 7:3   | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

**Table 2-1100. MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_CTRL Register Field Descriptions (continued)**

| Bit | Field                           | Type | Reset | Description                                                                                                                                           |
|-----|---------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0 | MSS_L2_A_BUS_SAFETY_CTRL_ENABLE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |



### 2.2.2.367 MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_FI Register (Offset = 18624h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of L2 BANK0 Target Port.

Return to [Summary Table](#)

**Table 2-1101. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8624h       |

**Figure 2-367. MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_FI Name Register**

| 31                          | 30                                 | 29                                 | 28                                                 | 27                                                 | 26                                         | 25                                         | 24  |
|-----------------------------|------------------------------------|------------------------------------|----------------------------------------------------|----------------------------------------------------|--------------------------------------------|--------------------------------------------|-----|
| MSS_L2_A_BUS_SAFETY_FI_SAFE |                                    |                                    |                                                    |                                                    |                                            |                                            |     |
| R/W                         |                                    |                                    |                                                    |                                                    |                                            |                                            |     |
| 0h                          |                                    |                                    |                                                    |                                                    |                                            |                                            |     |
| 23                          | 22                                 | 21                                 | 20                                                 | 19                                                 | 18                                         | 17                                         | 16  |
| MSS_L2_A_BUS_SAFETY_FI_MAIN |                                    |                                    |                                                    |                                                    |                                            |                                            |     |
| R/W                         |                                    |                                    |                                                    |                                                    |                                            |                                            |     |
| 0h                          |                                    |                                    |                                                    |                                                    |                                            |                                            |     |
| 15                          | 14                                 | 13                                 | 12                                                 | 11                                                 | 10                                         | 9                                          | 8   |
| MSS_L2_A_BUS_SAFETY_FI_DATA |                                    |                                    |                                                    |                                                    |                                            |                                            |     |
| R/W                         |                                    |                                    |                                                    |                                                    |                                            |                                            |     |
| 0h                          |                                    |                                    |                                                    |                                                    |                                            |                                            |     |
| 7                           | 6                                  | 5                                  | 4                                                  | 3                                                  | 2                                          | 1                                          | 0   |
| RESERVED                    | MSS_L2_A_BU<br>S_SAFETY_FI_<br>DED | MSS_L2_A_BU<br>S_SAFETY_FI_<br>SEC | MSS_L2_A_BU<br>S_SAFETY_FI_<br>GLOBAL_SAFE<br>_REQ | MSS_L2_A_BU<br>S_SAFETY_FI_<br>GLOBAL_MAIN<br>_REQ | MSS_L2_A_BU<br>S_SAFETY_FI_<br>GLOBAL_SAFE | MSS_L2_A_BU<br>S_SAFETY_FI_<br>GLOBAL_MAIN |     |
| NONE                        | R/W                                | R/W                                | R/W                                                | R/W                                                | R/W                                        | R/W                                        | R/W |
| 0h                          | 0h                                 | 0h                                 | 0h                                                 | 0h                                                 | 0h                                         | 0h                                         | 0h  |

**Table 2-1103. MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-----------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_L2_A_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_L2_A_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_L2_A_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                    | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5     | MSS_L2_A_BUS_SAFETY_FI_DED  | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                                                                                                                                                                                                        |

**Table 2-1103. MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_FI Register Field Descriptions (continued)**

| Bit | Field                                  | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|----------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | MSS_L2_A_BUS_SAFETY_FI_SEC             | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_L2_A_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit corresponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_L2_A_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit corresponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_L2_A_BUS_SAFETY_FI_GLOBAL_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_L2_A_BUS_SAFETY_FI_GLOBAL_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

### 2.2.2.368 MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_ERR Register (Offset = 18628h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of L2 BANK0 Target Port.

Return to [Summary Table](#)

**Table 2-1104. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8628h       |

**Figure 2-368. MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_ERR Name Register**

|                                    |    |    |    |    |    |    |    |
|------------------------------------|----|----|----|----|----|----|----|
| 31                                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_L2_A_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |
| 23                                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_L2_A_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |
| 15                                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_L2_A_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |
| 7                                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_L2_A_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |

**Table 2-1106. MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_L2_A_BUS_SAFETY_ERR_DED        | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_L2_A_BUS_SAFETY_ERR_SEC        | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_L2_A_BUS_SAFETY_ERR_COMP_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-1106. MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_ERR Register Field Descriptions (continued)**

| Bit | Field                            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|----------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_L2_A_BUS_SAFETY_ERR_COMP_ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.369 MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 1862Ch) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of L2 BANK0 Target Port.

Return to [Summary Table](#)

**Table 2-1107. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 862Ch       |

**Figure 2-369. MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                       |    |    |    |    |    |    |    |
|---------------------------------------|----|----|----|----|----|----|----|
| 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 23                                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 15                                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_L2_A_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 7                                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_L2_A_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |

**Table 2-1109. MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                 | Type | Reset | Description                                                                                                                                                |
|-------|---------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                              | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_L2_A_BUS_SAFETY_ERR_STAT_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_L2_A_BUS_SAFETY_ERR_STAT_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.370 MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

#### 1 MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 18630h) [reset = 0h]

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of L2 BANK0 Target Port.

Return to [Summary Table](#)

**Table 2-1110. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8630h       |

**Figure 2-370. MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                       |    |    |    |    |    |    |    |
|---------------------------------------|----|----|----|----|----|----|----|
| 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_L2_A_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 23                                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_L2_A_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 15                                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_L2_A_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 7                                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_L2_A_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |

**Table 2-1112. MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                 | Type | Reset | Description                                                                                                                       |
|------|---------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_L2_A_BUS_SAFETY_ERR_STAT_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.371 MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register

#### 1 MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register (Offset = 18634h) [reset = 0h]

This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of L2 BANK0 Target Port.

Return to [Summary Table](#)

**Table 2-1113. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8634h       |

**Figure 2-371. MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_ERR\_STAT\_WRITE Name Register**

|                                         |    |    |    |    |    |    |    |
|-----------------------------------------|----|----|----|----|----|----|----|
| 31                                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_L2_A_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 23                                      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_L2_A_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 15                                      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_L2_A_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 7                                       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_L2_A_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |

**Table 2-1115. MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register Field Descriptions**

| Bit  | Field                                   | Type | Reset | Description                                                                                                        |
|------|-----------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_L2_A_BUS_SAFETY_ERR_STAT_WRITE_STAT | R    | 0h    | Read this bitfield for comparator status for Write bus for this port. 1'b1 at any bit indicates error on Write Bus |

### 2.2.2.372 MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_ERR\_STAT\_READ Register

#### 1 MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_ERR\_STAT\_READ Register (Offset = 18638h) [reset = 0h]

This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of L2 BANK0 Target Port.

Return to [Summary Table](#)

**Table 2-1116. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8638h       |

**Figure 2-372. MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_ERR\_STAT\_READ Name Register**

|                                        |    |    |    |    |    |    |    |
|----------------------------------------|----|----|----|----|----|----|----|
| 31                                     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_L2_A_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 23                                     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_L2_A_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 15                                     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_L2_A_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 7                                      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_L2_A_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |

**Table 2-1118. MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_ERR\_STAT\_READ Register Field Descriptions**

| Bit  | Field                                  | Type | Reset | Description                                                                                                                     |
|------|----------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_L2_A_BUS_SAFETY_ERR_STAT_READ_STAT | R    | 0h    | Read this bitfield for comparator status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus. |



### 2.2.2.373 MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register

#### 1 MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register (Offset = 1863Ch) [reset = 0h]

This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of L2 BANK0 Target Port.

Return to [Summary Table](#)

**Table 2-1119. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 863Ch       |

**Figure 2-373. MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_L2_A_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_L2_A_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_L2_A_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_L2_A_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-1121. MSS\_CTRL\_MSS\_L2\_A\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register Field Descriptions**

| Bit  | Field                                       | Type | Reset | Description                                                                                                                           |
|------|---------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_L2_A_BUS_SAFETY_ERR_STAT_WRITERESP_STAT | R    | 0h    | Read this bitfield for comparator status for Write response bus for this port. 1'b1 at any bit indicates error on Write Response Bus. |

### 2.2.2.374 MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_CTRL Register (Offset = 18640h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of L2 BANK1 Target Port.

Return to [Summary Table](#)

**Table 2-1122. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8640h       |

**Figure 2-374. MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_CTRL Name Register**

|                               |    |    |    |    |                                 |    |                                    |
|-------------------------------|----|----|----|----|---------------------------------|----|------------------------------------|
| 31                            | 30 | 29 | 28 | 27 | 26                              | 25 | 24                                 |
| RESERVED                      |    |    |    |    |                                 |    |                                    |
| NONE                          |    |    |    |    |                                 |    |                                    |
| 0h                            |    |    |    |    |                                 |    |                                    |
| 23                            | 22 | 21 | 20 | 19 | 18                              | 17 | 16                                 |
| MSS_L2_B_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                 |    |                                    |
| R                             |    |    |    |    |                                 |    |                                    |
| 0h                            |    |    |    |    |                                 |    |                                    |
| 15                            | 14 | 13 | 12 | 11 | 10                              | 9  | 8                                  |
| RESERVED                      |    |    |    |    |                                 |    | MSS_L2_B_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                          |    |    |    |    |                                 |    | R/W                                |
| 0h                            |    |    |    |    |                                 |    | 0h                                 |
| 7                             | 6  | 5  | 4  | 3  | 2                               | 1  | 0                                  |
| RESERVED                      |    |    |    |    | MSS_L2_B_BUS_SAFETY_CTRL_ENABLE |    |                                    |
| NONE                          |    |    |    |    | R/W                             |    |                                    |
| 0h                            |    |    |    |    | 7h                              |    |                                    |

**Table 2-1124. MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | MSS_L2_B_BUS_SAFETY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | MSS_L2_B_BUS_SAFETY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 7:3   | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

**Table 2-1124. MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_CTRL Register Field Descriptions (continued)**

| Bit | Field                           | Type | Reset | Description                                                                                                                                           |
|-----|---------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0 | MSS_L2_B_BUS_SAFETY_CTRL_ENABLE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.375 MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_FI Register (Offset = 18644h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of L2 BANK1 Target Port.

Return to [Summary Table](#)

**Table 2-1125. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8644h       |

**Figure 2-375. MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_FI Name Register**

| 31                          | 30                                 | 29                                 | 28                                                 | 27                                                 | 26                                         | 25                                         | 24  |
|-----------------------------|------------------------------------|------------------------------------|----------------------------------------------------|----------------------------------------------------|--------------------------------------------|--------------------------------------------|-----|
| MSS_L2_B_BUS_SAFETY_FI_SAFE |                                    |                                    |                                                    |                                                    |                                            |                                            |     |
| R/W                         |                                    |                                    |                                                    |                                                    |                                            |                                            |     |
| 0h                          |                                    |                                    |                                                    |                                                    |                                            |                                            |     |
| 23                          | 22                                 | 21                                 | 20                                                 | 19                                                 | 18                                         | 17                                         | 16  |
| MSS_L2_B_BUS_SAFETY_FI_MAIN |                                    |                                    |                                                    |                                                    |                                            |                                            |     |
| R/W                         |                                    |                                    |                                                    |                                                    |                                            |                                            |     |
| 0h                          |                                    |                                    |                                                    |                                                    |                                            |                                            |     |
| 15                          | 14                                 | 13                                 | 12                                                 | 11                                                 | 10                                         | 9                                          | 8   |
| MSS_L2_B_BUS_SAFETY_FI_DATA |                                    |                                    |                                                    |                                                    |                                            |                                            |     |
| R/W                         |                                    |                                    |                                                    |                                                    |                                            |                                            |     |
| 0h                          |                                    |                                    |                                                    |                                                    |                                            |                                            |     |
| 7                           | 6                                  | 5                                  | 4                                                  | 3                                                  | 2                                          | 1                                          | 0   |
| RESERVED                    | MSS_L2_B_BU<br>S_SAFETY_FI_<br>DED | MSS_L2_B_BU<br>S_SAFETY_FI_<br>SEC | MSS_L2_B_BU<br>S_SAFETY_FI_<br>GLOBAL_SAFE<br>_REQ | MSS_L2_B_BU<br>S_SAFETY_FI_<br>GLOBAL_MAIN<br>_REQ | MSS_L2_B_BU<br>S_SAFETY_FI_<br>GLOBAL_SAFE | MSS_L2_B_BU<br>S_SAFETY_FI_<br>GLOBAL_MAIN |     |
| NONE                        | R/W                                | R/W                                | R/W                                                | R/W                                                | R/W                                        | R/W                                        | R/W |
| 0h                          | 0h                                 | 0h                                 | 0h                                                 | 0h                                                 | 0h                                         | 0h                                         | 0h  |

**Table 2-1127. MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-----------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_L2_B_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_L2_B_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_L2_B_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                    | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5     | MSS_L2_B_BUS_SAFETY_FI_DED  | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                                                                                                                                                                                                        |

**Table 2-1127. MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_FI Register Field Descriptions (continued)**

| Bit | Field                                  | Type | Reset | Description                                                                                                                                                                                                                                           |
|-----|----------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | MSS_L2_B_BUS_SAFETY_FI_SEC             | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                         |
| 3   | MSS_L2_B_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coresponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_L2_B_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coresponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_L2_B_BUS_SAFETY_FI_GLOBAL_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                          |
| 0   | MSS_L2_B_BUS_SAFETY_FI_GLOBAL_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                 |

### 2.2.2.376 MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_ERR Register (Offset = 18648h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of L2 BANK1 Target Port.

Return to [Summary Table](#)

**Table 2-1128. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8648h       |

**Figure 2-376. MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_ERR Name Register**

|                                    |    |    |    |    |    |    |    |
|------------------------------------|----|----|----|----|----|----|----|
| 31                                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_L2_B_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |
| 23                                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_L2_B_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |
| 15                                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_L2_B_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |
| 7                                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_L2_B_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |

**Table 2-1130. MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_L2_B_BUS_SAFETY_ERR_DED        | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_L2_B_BUS_SAFETY_ERR_SEC        | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_L2_B_BUS_SAFETY_ERR_COMP_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-1130. MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_ERR Register Field Descriptions (continued)**

| Bit | Field                            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|----------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_L2_B_BUS_SAFETY_ERR_COMP_ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.377 MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 1864Ch) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of L2 BANK1 Target Port.

Return to [Summary Table](#)

**Table 2-1131. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 864Ch       |

**Figure 2-377. MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                       |    |    |    |    |    |    |    |
|---------------------------------------|----|----|----|----|----|----|----|
| 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 23                                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 15                                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_L2_B_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 7                                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_L2_B_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |

**Table 2-1133. MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                 | Type | Reset | Description                                                                                                                                                |
|-------|---------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                              | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_L2_B_BUS_SAFETY_ERR_STAT_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_L2_B_BUS_SAFETY_ERR_STAT_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |



### 2.2.2.378 MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

#### 1 MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 18650h) [reset = 0h]

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of L2 BANK1 Target Port.

Return to [Summary Table](#)

**Table 2-1134. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8650h       |

**Figure 2-378. MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                       |    |    |    |    |    |    |    |
|---------------------------------------|----|----|----|----|----|----|----|
| 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_L2_B_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 23                                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_L2_B_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 15                                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_L2_B_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 7                                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_L2_B_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |

**Table 2-1136. MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                 | Type | Reset | Description                                                                                                                       |
|------|---------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_L2_B_BUS_SAFETY_ERR_STAT_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.379 MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register

#### 1 MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register (Offset = 18654h) [reset = 0h]

This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of L2 BANK1 Target Port.

Return to [Summary Table](#)

**Table 2-1137. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8654h       |

**Figure 2-379. MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_ERR\_STAT\_WRITE Name Register**

|                                         |    |    |    |    |    |    |    |
|-----------------------------------------|----|----|----|----|----|----|----|
| 31                                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_L2_B_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 23                                      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_L2_B_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 15                                      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_L2_B_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 7                                       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_L2_B_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |

**Table 2-1139. MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register Field Descriptions**

| Bit  | Field                                   | Type | Reset | Description                                                                                                        |
|------|-----------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_L2_B_BUS_SAFETY_ERR_STAT_WRITE_STAT | R    | 0h    | Read this bitfield for comparator status for Write bus for this port. 1'b1 at any bit indicates error on Write Bus |

### 2.2.2.380 MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_ERR\_STAT\_READ Register

#### 1 MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_ERR\_STAT\_READ Register (Offset = 18658h) [reset = 0h]

This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of L2 BANK1 Target Port.

Return to [Summary Table](#)

**Table 2-1140. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8658h       |

**Figure 2-380. MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_ERR\_STAT\_READ Name Register**

|                                        |    |    |    |    |    |    |    |
|----------------------------------------|----|----|----|----|----|----|----|
| 31                                     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_L2_B_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 23                                     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_L2_B_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 15                                     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_L2_B_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 7                                      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_L2_B_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |

**Table 2-1142. MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_ERR\_STAT\_READ Register Field Descriptions**

| Bit  | Field                                  | Type | Reset | Description                                                                                                                     |
|------|----------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_L2_B_BUS_SAFETY_ERR_STAT_READ_STAT | R    | 0h    | Read this bitfield for comparator status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus. |

### 2.2.2.381 MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register

#### 1 MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register (Offset = 1865Ch) [reset = 0h]

This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of L2 BANK1 Target Port.

Return to [Summary Table](#)

**Table 2-1143. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 865Ch       |

**Figure 2-381. MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_L2_B_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_L2_B_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_L2_B_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_L2_B_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-1145. MSS\_CTRL\_MSS\_L2\_B\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register Field Descriptions**

| Bit  | Field                                       | Type | Reset | Description                                                                                                                           |
|------|---------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_L2_B_BUS_SAFETY_ERR_STAT_WRITERESP_STAT | R    | 0h    | Read this bitfield for comparator status for Write response bus for this port. 1'b1 at any bit indicates error on Write Response Bus. |

### 2.2.2.382 MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_CTRL Register (Offset = 18660h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of L2 BANK2 Target Port.

Return to [Summary Table](#)

**Table 2-1146. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8660h       |

**Figure 2-382. MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_CTRL Name Register**

|                               |    |    |    |    |                                 |    |                                    |
|-------------------------------|----|----|----|----|---------------------------------|----|------------------------------------|
| 31                            | 30 | 29 | 28 | 27 | 26                              | 25 | 24                                 |
| RESERVED                      |    |    |    |    |                                 |    |                                    |
| NONE                          |    |    |    |    |                                 |    |                                    |
| 0h                            |    |    |    |    |                                 |    |                                    |
| 23                            | 22 | 21 | 20 | 19 | 18                              | 17 | 16                                 |
| MSS_L2_C_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                 |    |                                    |
| R                             |    |    |    |    |                                 |    |                                    |
| 0h                            |    |    |    |    |                                 |    |                                    |
| 15                            | 14 | 13 | 12 | 11 | 10                              | 9  | 8                                  |
| RESERVED                      |    |    |    |    |                                 |    | MSS_L2_C_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                          |    |    |    |    |                                 |    | R/W                                |
| 0h                            |    |    |    |    |                                 |    | 0h                                 |
| 7                             | 6  | 5  | 4  | 3  | 2                               | 1  | 0                                  |
| RESERVED                      |    |    |    |    | MSS_L2_C_BUS_SAFETY_CTRL_ENABLE |    |                                    |
| NONE                          |    |    |    |    | R/W                             |    |                                    |
| 0h                            |    |    |    |    | 7h                              |    |                                    |

**Table 2-1148. MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | MSS_L2_C_BUS_SAFETY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | MSS_L2_C_BUS_SAFETY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 7:3   | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

**Table 2-1148. MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_CTRL Register Field Descriptions (continued)**

| Bit | Field                           | Type | Reset | Description                                                                                                                                           |
|-----|---------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0 | MSS_L2_C_BUS_SAFETY_CTRL_ENABLE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.383 MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_FI Register (Offset = 18664h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of L2 BANK2 Target Port.

Return to [Summary Table](#)

**Table 2-1149. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8664h       |

**Figure 2-383. MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_FI Name Register**

| 31                          | 30                                 | 29                                 | 28                                                 | 27                                                 | 26                                         | 25                                         | 24  |
|-----------------------------|------------------------------------|------------------------------------|----------------------------------------------------|----------------------------------------------------|--------------------------------------------|--------------------------------------------|-----|
| MSS_L2_C_BUS_SAFETY_FI_SAFE |                                    |                                    |                                                    |                                                    |                                            |                                            |     |
| R/W                         |                                    |                                    |                                                    |                                                    |                                            |                                            |     |
| 0h                          |                                    |                                    |                                                    |                                                    |                                            |                                            |     |
| 23                          | 22                                 | 21                                 | 20                                                 | 19                                                 | 18                                         | 17                                         | 16  |
| MSS_L2_C_BUS_SAFETY_FI_MAIN |                                    |                                    |                                                    |                                                    |                                            |                                            |     |
| R/W                         |                                    |                                    |                                                    |                                                    |                                            |                                            |     |
| 0h                          |                                    |                                    |                                                    |                                                    |                                            |                                            |     |
| 15                          | 14                                 | 13                                 | 12                                                 | 11                                                 | 10                                         | 9                                          | 8   |
| MSS_L2_C_BUS_SAFETY_FI_DATA |                                    |                                    |                                                    |                                                    |                                            |                                            |     |
| R/W                         |                                    |                                    |                                                    |                                                    |                                            |                                            |     |
| 0h                          |                                    |                                    |                                                    |                                                    |                                            |                                            |     |
| 7                           | 6                                  | 5                                  | 4                                                  | 3                                                  | 2                                          | 1                                          | 0   |
| RESERVED                    | MSS_L2_C_BU<br>S_SAFETY_FI_<br>DED | MSS_L2_C_BU<br>S_SAFETY_FI_<br>SEC | MSS_L2_C_BU<br>S_SAFETY_FI_<br>GLOBAL_SAFE<br>_REQ | MSS_L2_C_BU<br>S_SAFETY_FI_<br>GLOBAL_MAIN<br>_REQ | MSS_L2_C_BU<br>S_SAFETY_FI_<br>GLOBAL_SAFE | MSS_L2_C_BU<br>S_SAFETY_FI_<br>GLOBAL_MAIN |     |
| NONE                        | R/W                                | R/W                                | R/W                                                | R/W                                                | R/W                                        | R/W                                        | R/W |
| 0h                          | 0h                                 | 0h                                 | 0h                                                 | 0h                                                 | 0h                                         | 0h                                         | 0h  |

**Table 2-1151. MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-----------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_L2_C_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_L2_C_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_L2_C_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                    | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5     | MSS_L2_C_BUS_SAFETY_FI_DED  | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                                                                                                                                                                                                        |

**Table 2-1151. MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_FI Register Field Descriptions (continued)**

| Bit | Field                                  | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|----------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | MSS_L2_C_BUS_SAFETY_FI_SEC             | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_L2_C_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit corresponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_L2_C_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit corresponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_L2_C_BUS_SAFETY_FI_GLOBAL_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_L2_C_BUS_SAFETY_FI_GLOBAL_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |



### 2.2.2.384 MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_ERR Register (Offset = 18668h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of L2 BANK2 Target Port.

Return to [Summary Table](#)

**Table 2-1152. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8668h       |

**Figure 2-384. MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_ERR Name Register**

|                                    |    |    |    |    |    |    |    |
|------------------------------------|----|----|----|----|----|----|----|
| 31                                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_L2_C_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |
| 23                                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_L2_C_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |
| 15                                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_L2_C_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |
| 7                                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_L2_C_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |

**Table 2-1154. MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_L2_C_BUS_SAFETY_ERR_DED        | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_L2_C_BUS_SAFETY_ERR_SEC        | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_L2_C_BUS_SAFETY_ERR_COMP_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-1154. MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_ERR Register Field Descriptions (continued)**

| Bit | Field                            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|----------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_L2_C_BUS_SAFETY_ERR_COMP_ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.385 MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 1866Ch) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of L2 BANK2 Target Port.

Return to [Summary Table](#)

**Table 2-1155. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 866Ch       |

**Figure 2-385. MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                       |    |    |    |    |    |    |    |
|---------------------------------------|----|----|----|----|----|----|----|
| 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 23                                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 15                                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_L2_C_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 7                                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_L2_C_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |

**Table 2-1157. MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                 | Type | Reset | Description                                                                                                                                                |
|-------|---------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                              | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_L2_C_BUS_SAFETY_ERR_STAT_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_L2_C_BUS_SAFETY_ERR_STAT_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.386 MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

#### 1 MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 18670h) [reset = 0h]

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of L2 BANK2 Target Port.

Return to [Summary Table](#)

**Table 2-1158. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8670h       |

**Figure 2-386. MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                       |    |    |    |    |    |    |    |
|---------------------------------------|----|----|----|----|----|----|----|
| 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_L2_C_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 23                                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_L2_C_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 15                                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_L2_C_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 7                                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_L2_C_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |

**Table 2-1160. MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                 | Type | Reset | Description                                                                                                                       |
|------|---------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_L2_C_BUS_SAFETY_ERR_STAT_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.387 MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register

#### 1 MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register (Offset = 18674h) [reset = 0h]

This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of L2 BANK2 Target Port.

Return to [Summary Table](#)

**Table 2-1161. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8674h       |

**Figure 2-387. MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_ERR\_STAT\_WRITE Name Register**

|                                         |    |    |    |    |    |    |    |
|-----------------------------------------|----|----|----|----|----|----|----|
| 31                                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_L2_C_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 23                                      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_L2_C_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 15                                      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_L2_C_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 7                                       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_L2_C_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |

**Table 2-1163. MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register Field Descriptions**

| Bit  | Field                                   | Type | Reset | Description                                                                                                        |
|------|-----------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_L2_C_BUS_SAFETY_ERR_STAT_WRITE_STAT | R    | 0h    | Read this bitfield for comparator status for Write bus for this port. 1'b1 at any bit indicates error on Write Bus |

### 2.2.2.388 MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_ERR\_STAT\_READ Register

#### 1 MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_ERR\_STAT\_READ Register (Offset = 18678h) [reset = 0h]

This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of L2 BANK2 Target Port.

Return to [Summary Table](#)

**Table 2-1164. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8678h       |

**Figure 2-388. MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_ERR\_STAT\_READ Name Register**

|                                        |    |    |    |    |    |    |    |
|----------------------------------------|----|----|----|----|----|----|----|
| 31                                     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_L2_C_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 23                                     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_L2_C_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 15                                     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_L2_C_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 7                                      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_L2_C_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |

**Table 2-1166. MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_ERR\_STAT\_READ Register Field Descriptions**

| Bit  | Field                                  | Type | Reset | Description                                                                                                                     |
|------|----------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_L2_C_BUS_SAFETY_ERR_STAT_READ_STAT | R    | 0h    | Read this bitfield for comparator status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus. |

### 2.2.2.389 MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register

#### 1 MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register (Offset = 1867Ch) [reset = 0h]

This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of L2 BANK2 Target Port.

Return to [Summary Table](#)

**Table 2-1167. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 867Ch       |

**Figure 2-389. MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_L2_C_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_L2_C_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_L2_C_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_L2_C_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-1169. MSS\_CTRL\_MSS\_L2\_C\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register Field Descriptions**

| Bit  | Field                                       | Type | Reset | Description                                                                                                                           |
|------|---------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_L2_C_BUS_SAFETY_ERR_STAT_WRITERESP_STAT | R    | 0h    | Read this bitfield for comparator status for Write response bus for this port. 1'b1 at any bit indicates error on Write Response Bus. |

### 2.2.2.390 MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_CTRL Register (Offset = 18680h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of L2 BANK3 Target Port.

Return to [Summary Table](#)

**Table 2-1170. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8680h       |

**Figure 2-390. MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_CTRL Name Register**

|                               |    |    |    |    |                                 |    |                                    |
|-------------------------------|----|----|----|----|---------------------------------|----|------------------------------------|
| 31                            | 30 | 29 | 28 | 27 | 26                              | 25 | 24                                 |
| RESERVED                      |    |    |    |    |                                 |    |                                    |
| NONE                          |    |    |    |    |                                 |    |                                    |
| 0h                            |    |    |    |    |                                 |    |                                    |
| 23                            | 22 | 21 | 20 | 19 | 18                              | 17 | 16                                 |
| MSS_L2_D_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                 |    |                                    |
| R                             |    |    |    |    |                                 |    |                                    |
| 0h                            |    |    |    |    |                                 |    |                                    |
| 15                            | 14 | 13 | 12 | 11 | 10                              | 9  | 8                                  |
| RESERVED                      |    |    |    |    |                                 |    | MSS_L2_D_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                          |    |    |    |    |                                 |    | R/W                                |
| 0h                            |    |    |    |    |                                 |    | 0h                                 |
| 7                             | 6  | 5  | 4  | 3  | 2                               | 1  | 0                                  |
| RESERVED                      |    |    |    |    | MSS_L2_D_BUS_SAFETY_CTRL_ENABLE |    |                                    |
| NONE                          |    |    |    |    | R/W                             |    |                                    |
| 0h                            |    |    |    |    | 7h                              |    |                                    |

**Table 2-1172. MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | MSS_L2_D_BUS_SAFETY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | MSS_L2_D_BUS_SAFETY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 7:3   | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |



**Table 2-1172. MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_CTRL Register Field Descriptions (continued)**

| Bit | Field                           | Type | Reset | Description                                                                                                                                           |
|-----|---------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0 | MSS_L2_D_BUS_SAFETY_CTRL_ENABLE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.391 MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_FI Register (Offset = 18684h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of L2 BANK3 Target Port.

Return to [Summary Table](#)

**Table 2-1173. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8684h       |

**Figure 2-391. MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_FI Name Register**

| 31                          | 30                         | 29                         | 28                                     | 27                                     | 26                                 | 25                                 | 24  |
|-----------------------------|----------------------------|----------------------------|----------------------------------------|----------------------------------------|------------------------------------|------------------------------------|-----|
| MSS_L2_D_BUS_SAFETY_FI_SAFE |                            |                            |                                        |                                        |                                    |                                    |     |
| R/W                         |                            |                            |                                        |                                        |                                    |                                    |     |
| 0h                          |                            |                            |                                        |                                        |                                    |                                    |     |
| 23                          | 22                         | 21                         | 20                                     | 19                                     | 18                                 | 17                                 | 16  |
| MSS_L2_D_BUS_SAFETY_FI_MAIN |                            |                            |                                        |                                        |                                    |                                    |     |
| R/W                         |                            |                            |                                        |                                        |                                    |                                    |     |
| 0h                          |                            |                            |                                        |                                        |                                    |                                    |     |
| 15                          | 14                         | 13                         | 12                                     | 11                                     | 10                                 | 9                                  | 8   |
| MSS_L2_D_BUS_SAFETY_FI_DATA |                            |                            |                                        |                                        |                                    |                                    |     |
| R/W                         |                            |                            |                                        |                                        |                                    |                                    |     |
| 0h                          |                            |                            |                                        |                                        |                                    |                                    |     |
| 7                           | 6                          | 5                          | 4                                      | 3                                      | 2                                  | 1                                  | 0   |
| RESERVED                    | MSS_L2_D_BUS_SAFETY_FI_DED | MSS_L2_D_BUS_SAFETY_FI_SEC | MSS_L2_D_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | MSS_L2_D_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | MSS_L2_D_BUS_SAFETY_FI_GLOBAL_SAFE | MSS_L2_D_BUS_SAFETY_FI_GLOBAL_MAIN |     |
| NONE                        | R/W                        | R/W                        | R/W                                    | R/W                                    | R/W                                | R/W                                | R/W |
| 0h                          | 0h                         | 0h                         | 0h                                     | 0h                                     | 0h                                 | 0h                                 | 0h  |

**Table 2-1175. MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-----------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_L2_D_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_L2_D_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_L2_D_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                    | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5     | MSS_L2_D_BUS_SAFETY_FI_DED  | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                                                                                                                                                                                                        |

**Table 2-1175. MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_FI Register Field Descriptions (continued)**

| Bit | Field                                  | Type | Reset | Description                                                                                                                                                                                                                                           |
|-----|----------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | MSS_L2_D_BUS_SAFETY_FI_SEC             | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                         |
| 3   | MSS_L2_D_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coresponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_L2_D_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coresponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_L2_D_BUS_SAFETY_FI_GLOBAL_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                          |
| 0   | MSS_L2_D_BUS_SAFETY_FI_GLOBAL_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                 |

### 2.2.2.392 MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_ERR Register (Offset = 18688h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of L2 BANK3 Target Port.

Return to [Summary Table](#)

**Table 2-1176. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8688h       |

**Figure 2-392. MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_ERR Name Register**

|                                    |    |    |    |    |    |    |    |
|------------------------------------|----|----|----|----|----|----|----|
| 31                                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_L2_D_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |
| 23                                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_L2_D_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |
| 15                                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_L2_D_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |
| 7                                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_L2_D_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |

**Table 2-1178. MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_L2_D_BUS_SAFETY_ERR_DED        | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_L2_D_BUS_SAFETY_ERR_SEC        | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_L2_D_BUS_SAFETY_ERR_COMP_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-1178. MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_ERR Register Field Descriptions (continued)**

| Bit | Field                            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|----------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_L2_D_BUS_SAFETY_ERR_COMP_ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.393 MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 1868Ch) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of L2 BANK3 Target Port.

Return to [Summary Table](#)

**Table 2-1179. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 868Ch       |

**Figure 2-393. MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                       |    |    |    |    |    |    |    |
|---------------------------------------|----|----|----|----|----|----|----|
| 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 23                                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 15                                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_L2_D_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 7                                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_L2_D_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |

**Table 2-1181. MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                 | Type | Reset | Description                                                                                                                                                |
|-------|---------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                              | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_L2_D_BUS_SAFETY_ERR_STAT_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_L2_D_BUS_SAFETY_ERR_STAT_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.394 MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

#### 1 MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 18690h) [reset = 0h]

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of L2 BANK3 Target Port.

Return to [Summary Table](#)

**Table 2-1182. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8690h       |

**Figure 2-394. MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                       |    |    |    |    |    |    |    |
|---------------------------------------|----|----|----|----|----|----|----|
| 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_L2_D_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 23                                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_L2_D_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 15                                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_L2_D_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 7                                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_L2_D_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |

**Table 2-1184. MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                 | Type | Reset | Description                                                                                                                       |
|------|---------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_L2_D_BUS_SAFETY_ERR_STAT_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.395 MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register

#### 1 MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register (Offset = 18694h) [reset = 0h]

This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of L2 BANK3 Target Port.

Return to [Summary Table](#)

**Table 2-1185. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8694h       |

**Figure 2-395. MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_ERR\_STAT\_WRITE Name Register**

|                                         |    |    |    |    |    |    |    |
|-----------------------------------------|----|----|----|----|----|----|----|
| 31                                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_L2_D_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 23                                      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_L2_D_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 15                                      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_L2_D_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 7                                       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_L2_D_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |

**Table 2-1187. MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register Field Descriptions**

| Bit  | Field                                   | Type | Reset | Description                                                                                                        |
|------|-----------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_L2_D_BUS_SAFETY_ERR_STAT_WRITE_STAT | R    | 0h    | Read this bitfield for comparator status for Write bus for this port. 1'b1 at any bit indicates error on Write Bus |



### 2.2.2.396 MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_ERR\_STAT\_READ Register

#### 1 MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_ERR\_STAT\_READ Register (Offset = 18698h) [reset = 0h]

This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of L2 BANK3 Target Port.

Return to [Summary Table](#)

**Table 2-1188. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8698h       |

**Figure 2-396. MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_ERR\_STAT\_READ Name Register**

|                                        |    |    |    |    |    |    |    |
|----------------------------------------|----|----|----|----|----|----|----|
| 31                                     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_L2_D_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 23                                     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_L2_D_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 15                                     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_L2_D_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 7                                      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_L2_D_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |

**Table 2-1190. MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_ERR\_STAT\_READ Register Field Descriptions**

| Bit  | Field                                  | Type | Reset | Description                                                                                                                     |
|------|----------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_L2_D_BUS_SAFETY_ERR_STAT_READ_STAT | R    | 0h    | Read this bitfield for comparator status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus. |

### 2.2.2.397 MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register

#### 1 MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register (Offset = 1869Ch) [reset = 0h]

This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of L2 BANK3 Target Port.

Return to [Summary Table](#)

**Table 2-1191. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 869Ch       |

**Figure 2-397. MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_L2_D_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_L2_D_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_L2_D_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_L2_D_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-1193. MSS\_CTRL\_MSS\_L2\_D\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register Field Descriptions**

| Bit  | Field                                       | Type | Reset | Description                                                                                                                           |
|------|---------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_L2_D_BUS_SAFETY_ERR_STAT_WRITERESP_STAT | R    | 0h    | Read this bitfield for comparator status for Write response bus for this port. 1'b1 at any bit indicates error on Write Response Bus. |

### 2.2.2.398 MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_CTRL Register (Offset = 186A0h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of MBOX SRAM Target Port.

Return to [Summary Table](#)

**Table 2-1194. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 86A0h       |

**Figure 2-398. MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_CTRL Name Register**

|                               |    |    |    |    |                                 |    |                                                |
|-------------------------------|----|----|----|----|---------------------------------|----|------------------------------------------------|
| 31                            | 30 | 29 | 28 | 27 | 26                              | 25 | 24                                             |
| RESERVED                      |    |    |    |    |                                 |    |                                                |
| NONE                          |    |    |    |    |                                 |    |                                                |
| 0h                            |    |    |    |    |                                 |    |                                                |
| 23                            | 22 | 21 | 20 | 19 | 18                              | 17 | 16                                             |
| MSS_MBOX_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                 |    |                                                |
| R                             |    |    |    |    |                                 |    |                                                |
| 0h                            |    |    |    |    |                                 |    |                                                |
| 15                            | 14 | 13 | 12 | 11 | 10                              | 9  | 8                                              |
| RESERVED                      |    |    |    |    |                                 |    | MSS_MBOX_B<br>US_SAFETY_C<br>TRL_ERR_CLE<br>AR |
| NONE                          |    |    |    |    |                                 |    | R/W                                            |
| 0h                            |    |    |    |    |                                 |    | 0h                                             |
| 7                             | 6  | 5  | 4  | 3  | 2                               | 1  | 0                                              |
| RESERVED                      |    |    |    |    | MSS_MBOX_BUS_SAFETY_CTRL_ENABLE |    |                                                |
| NONE                          |    |    |    |    | R/W                             |    |                                                |
| 0h                            |    |    |    |    | 7h                              |    |                                                |

**Table 2-1196. MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|----------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                               | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 23:16 | MSS_MBOX_BUS_SAFE<br>TY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/ initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/ initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/ initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                               | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 8     | MSS_MBOX_BUS_SAFE<br>TY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 7:3   | RESERVED                               | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

**Table 2-1196. MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_CTRL Register Field Descriptions (continued)**

| Bit | Field                           | Type | Reset | Description                                                                                                                                           |
|-----|---------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0 | MSS_MBOX_BUS_SAFETY_CTRL_ENABLE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.399 MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_FI Register (Offset = 186A4h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of MBOX SRAM Target Port.

Return to [Summary Table](#)

**Table 2-1197. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 86A4h       |

**Figure 2-399. MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_FI Name Register**

| 31                          | 30                                 | 29                                 | 28                                                 | 27                                                 | 26                                             | 25                                             | 24                                             |
|-----------------------------|------------------------------------|------------------------------------|----------------------------------------------------|----------------------------------------------------|------------------------------------------------|------------------------------------------------|------------------------------------------------|
| MSS_MBOX_BUS_SAFETY_FI_SAFE |                                    |                                    |                                                    |                                                    |                                                |                                                |                                                |
| R/W                         |                                    |                                    |                                                    |                                                    |                                                |                                                |                                                |
| 0h                          |                                    |                                    |                                                    |                                                    |                                                |                                                |                                                |
| 23                          | 22                                 | 21                                 | 20                                                 | 19                                                 | 18                                             | 17                                             | 16                                             |
| MSS_MBOX_BUS_SAFETY_FI_MAIN |                                    |                                    |                                                    |                                                    |                                                |                                                |                                                |
| R/W                         |                                    |                                    |                                                    |                                                    |                                                |                                                |                                                |
| 0h                          |                                    |                                    |                                                    |                                                    |                                                |                                                |                                                |
| 15                          | 14                                 | 13                                 | 12                                                 | 11                                                 | 10                                             | 9                                              | 8                                              |
| MSS_MBOX_BUS_SAFETY_FI_DATA |                                    |                                    |                                                    |                                                    |                                                |                                                |                                                |
| R/W                         |                                    |                                    |                                                    |                                                    |                                                |                                                |                                                |
| 0h                          |                                    |                                    |                                                    |                                                    |                                                |                                                |                                                |
| 7                           | 6                                  | 5                                  | 4                                                  | 3                                                  | 2                                              | 1                                              | 0                                              |
| RESERVED                    | MSS_MBOX_B<br>US_SAFETY_F<br>I_DED | MSS_MBOX_B<br>US_SAFETY_F<br>I_SEC | MSS_MBOX_B<br>US_SAFETY_F<br>I_GLOBAL_SA<br>FE_REQ | MSS_MBOX_B<br>US_SAFETY_F<br>I_GLOBAL_MAI<br>N_REQ | MSS_MBOX_B<br>US_SAFETY_F<br>I_GLOBAL_SA<br>FE | MSS_MBOX_B<br>US_SAFETY_F<br>I_GLOBAL_MAI<br>N | MSS_MBOX_B<br>US_SAFETY_F<br>I_GLOBAL_MAI<br>N |
| NONE                        | R/W                                | R/W                                | R/W                                                | R/W                                                | R/W                                            | R/W                                            | R/W                                            |
| 0h                          | 0h                                 | 0h                                 | 0h                                                 | 0h                                                 | 0h                                             | 0h                                             | 0h                                             |

**Table 2-1199. MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|---------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_MBOX_BUS_SAFE<br>TY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_MBOX_BUS_SAFE<br>TY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_MBOX_BUS_SAFE<br>TY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5     | MSS_MBOX_BUS_SAFE<br>TY_FI_DED  | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                                                                                                                                                                                                        |

**Table 2-1199. MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_FI Register Field Descriptions (continued)**

| Bit | Field                                  | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|----------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | MSS_MBOX_BUS_SAFETY_FI_SEC             | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_MBOX_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_MBOX_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_MBOX_BUS_SAFETY_FI_GLOBAL_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_MBOX_BUS_SAFETY_FI_GLOBAL_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

## 2.2.2.400 MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_ERR Register

### 1 MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_ERR Register (Offset = 186A8h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of MBOX SRAM Target Port.

Return to [Summary Table](#)

**Table 2-1200. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 86A8h       |

**Figure 2-400. MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_ERR Name Register**

|                                    |    |    |    |    |    |    |    |
|------------------------------------|----|----|----|----|----|----|----|
| 31                                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_MBOX_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |
| 23                                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_MBOX_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |
| 15                                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_MBOX_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |
| 7                                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_MBOX_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |

**Table 2-1202. MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_MBOX_BUS_SAFETY_ERR_DED        | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_MBOX_BUS_SAFETY_ERR_SEC        | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_MBOX_BUS_SAFETY_ERR_COMP_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-1202. MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_ERR Register Field Descriptions (continued)**

| Bit | Field                            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|----------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_MBOX_BUS_SAFETY_ERR_COMP_ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |



### 2.2.2.401 MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 186ACh) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of MBOX SRAM Target Port.

Return to [Summary Table](#)

**Table 2-1203. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 86ACh       |

**Figure 2-401. MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                       |    |    |    |    |    |    |    |
|---------------------------------------|----|----|----|----|----|----|----|
| 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 23                                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 15                                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_MBOX_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 7                                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_MBOX_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |

**Table 2-1205. MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                 | Type | Reset | Description                                                                                                                                                |
|-------|---------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                              | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_MBOX_BUS_SAFETY_ERR_STAT_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_MBOX_BUS_SAFETY_ERR_STAT_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.402 MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

#### 1 MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 186B0h) [reset = 0h]

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of MBOX SRAM Target Port.

Return to [Summary Table](#)

**Table 2-1206. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 86B0h       |

**Figure 2-402. MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                       |    |    |    |    |    |    |    |
|---------------------------------------|----|----|----|----|----|----|----|
| 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_MBOX_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 23                                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_MBOX_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 15                                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_MBOX_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 7                                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_MBOX_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |

**Table 2-1208. MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                 | Type | Reset | Description                                                                                                                       |
|------|---------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_MBOX_BUS_SAFETY_ERR_STAT_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.403 MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register

#### 1 MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register (Offset = 186B4h) [reset = 0h]

This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of MBOX SRAM Target Port.

Return to [Summary Table](#)

**Table 2-1209. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 86B4h       |

**Figure 2-403. MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_ERR\_STAT\_WRITE Name Register**

|                                         |    |    |    |    |    |    |    |
|-----------------------------------------|----|----|----|----|----|----|----|
| 31                                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_MBOX_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 23                                      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_MBOX_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 15                                      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_MBOX_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 7                                       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_MBOX_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |

**Table 2-1211. MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register Field Descriptions**

| Bit  | Field                                   | Type | Reset | Description                                                                                                        |
|------|-----------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_MBOX_BUS_SAFETY_ERR_STAT_WRITE_STAT | R    | 0h    | Read this bitfield for comparator status for Write bus for this port. 1'b1 at any bit indicates error on Write Bus |

### 2.2.2.404 MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_ERR\_STAT\_READ Register

#### 1 MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_ERR\_STAT\_READ Register (Offset = 186B8h) [reset = 0h]

This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of MBOX SRAM Target Port.

Return to [Summary Table](#)

**Table 2-1212. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 86B8h       |

**Figure 2-404. MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_ERR\_STAT\_READ Name Register**

|                                        |    |    |    |    |    |    |    |
|----------------------------------------|----|----|----|----|----|----|----|
| 31                                     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_MBOX_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 23                                     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_MBOX_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 15                                     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_MBOX_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 7                                      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_MBOX_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |

**Table 2-1214. MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_ERR\_STAT\_READ Register Field Descriptions**

| Bit  | Field                                  | Type | Reset | Description                                                                                                                     |
|------|----------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_MBOX_BUS_SAFETY_ERR_STAT_READ_STAT | R    | 0h    | Read this bitfield for comparator status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus. |

### 2.2.2.405 MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register

#### 1 MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register (Offset = 186BCh) [reset = 0h]

This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of MBOX SRAM Target Port.

Return to [Summary Table](#)

**Table 2-1215. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 86BCh       |

**Figure 2-405. MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_MBOX_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_MBOX_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_MBOX_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_MBOX_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-1217. MSS\_CTRL\_MSS\_MBOX\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register Field Descriptions**

| Bit  | Field                                       | Type | Reset | Description                                                                                                                           |
|------|---------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_MBOX_BUS_SAFETY_ERR_STAT_WRITERESP_STAT | R    | 0h    | Read this bitfield for comparator status for Write response bus for this port. 1'b1 at any bit indicates error on Write Response Bus. |

### 2.2.2.406 MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_CTRL Register (Offset = 186C0h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of STM Target Port.

Return to [Summary Table](#)

**Table 2-1218. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 86C0h       |

**Figure 2-406. MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_CTRL Name Register**

|                                   |    |    |    |    |                                     |    |                                        |
|-----------------------------------|----|----|----|----|-------------------------------------|----|----------------------------------------|
| 31                                | 30 | 29 | 28 | 27 | 26                                  | 25 | 24                                     |
| RESERVED                          |    |    |    |    |                                     |    |                                        |
| NONE                              |    |    |    |    |                                     |    |                                        |
| 0h                                |    |    |    |    |                                     |    |                                        |
| 23                                | 22 | 21 | 20 | 19 | 18                                  | 17 | 16                                     |
| MSS_STM_STIM_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                     |    |                                        |
| R                                 |    |    |    |    |                                     |    |                                        |
| 0h                                |    |    |    |    |                                     |    |                                        |
| 15                                | 14 | 13 | 12 | 11 | 10                                  | 9  | 8                                      |
| RESERVED                          |    |    |    |    |                                     |    | MSS_STM_STIM_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                              |    |    |    |    |                                     |    | R/W                                    |
| 0h                                |    |    |    |    |                                     |    | 0h                                     |
| 7                                 | 6  | 5  | 4  | 3  | 2                                   | 1  | 0                                      |
| RESERVED                          |    |    |    |    | MSS_STM_STIM_BUS_SAFETY_CTRL_ENABLE |    |                                        |
| NONE                              |    |    |    |    | R/W                                 |    |                                        |
| 0h                                |    |    |    |    | 7h                                  |    |                                        |

**Table 2-1220. MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|----------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                               | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | MSS_STM_STIM_BUS_SAFETY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                               | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | MSS_STM_STIM_BUS_SAFETY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 7:3   | RESERVED                               | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

**Table 2-1220. MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_CTRL Register Field Descriptions (continued)**

| Bit | Field                               | Type | Reset | Description                                                                                                                                           |
|-----|-------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0 | MSS_STM_STIM_BUS_SAFETY_CTRL_ENABLE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.407 MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_FI Register (Offset = 186C4h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of STM Target Port.

Return to [Summary Table](#)

**Table 2-1221. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 86C4h       |

**Figure 2-407. MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_FI Name Register**

| 31                              | 30                             | 29                             | 28                                         | 27                                         | 26                                     | 25                                     | 24  |
|---------------------------------|--------------------------------|--------------------------------|--------------------------------------------|--------------------------------------------|----------------------------------------|----------------------------------------|-----|
| MSS_STM_STIM_BUS_SAFETY_FI_SAFE |                                |                                |                                            |                                            |                                        |                                        |     |
| R/W                             |                                |                                |                                            |                                            |                                        |                                        |     |
| 0h                              |                                |                                |                                            |                                            |                                        |                                        |     |
| 23                              | 22                             | 21                             | 20                                         | 19                                         | 18                                     | 17                                     | 16  |
| MSS_STM_STIM_BUS_SAFETY_FI_MAIN |                                |                                |                                            |                                            |                                        |                                        |     |
| R/W                             |                                |                                |                                            |                                            |                                        |                                        |     |
| 0h                              |                                |                                |                                            |                                            |                                        |                                        |     |
| 15                              | 14                             | 13                             | 12                                         | 11                                         | 10                                     | 9                                      | 8   |
| MSS_STM_STIM_BUS_SAFETY_FI_DATA |                                |                                |                                            |                                            |                                        |                                        |     |
| R/W                             |                                |                                |                                            |                                            |                                        |                                        |     |
| 0h                              |                                |                                |                                            |                                            |                                        |                                        |     |
| 7                               | 6                              | 5                              | 4                                          | 3                                          | 2                                      | 1                                      | 0   |
| RESERVED                        | MSS_STM_STIM_BUS_SAFETY_FI_DED | MSS_STM_STIM_BUS_SAFETY_FI_SEC | MSS_STM_STIM_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | MSS_STM_STIM_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | MSS_STM_STIM_BUS_SAFETY_FI_GLOBAL_SAFE | MSS_STM_STIM_BUS_SAFETY_FI_GLOBAL_MAIN |     |
| NONE                            | R/W                            | R/W                            | R/W                                        | R/W                                        | R/W                                    | R/W                                    | R/W |
| 0h                              | 0h                             | 0h                             | 0h                                         | 0h                                         | 0h                                     | 0h                                     | 0h  |

**Table 2-1223. MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|---------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_STM_STIM_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_STM_STIM_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_STM_STIM_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5     | MSS_STM_STIM_BUS_SAFETY_FI_DED  | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                                                                                                                                                                                                        |



**Table 2-1223. MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_FI Register Field Descriptions (continued)**

| Bit | Field                                      | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|--------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | MSS_STM_STIM_BUS_SAFETY_FI_SEC             | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_STM_STIM_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_STM_STIM_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_STM_STIM_BUS_SAFETY_FI_GLOBAL_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_STM_STIM_BUS_SAFETY_FI_GLOBAL_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

## 2.2.2.408 MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_ERR Register

### 1 MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_ERR Register (Offset = 186C8h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of STM Target Port.

Return to [Summary Table](#)

**Table 2-1224. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 86C8h       |

**Figure 2-408. MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_ERR Name Register**

|                                        |    |    |    |    |    |    |    |
|----------------------------------------|----|----|----|----|----|----|----|
| 31                                     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_STM_STIM_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 23                                     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_STM_STIM_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 15                                     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_STM_STIM_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 7                                      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_STM_STIM_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |

**Table 2-1226. MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                                  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|----------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_STM_STIM_BUS_SAFETY_ERR_DED        | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_STM_STIM_BUS_SAFETY_ERR_SEC        | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_STM_STIM_BUS_SAFETY_ERR_COMP_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-1226. MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_ERR Register Field Descriptions (continued)**

| Bit | Field                                | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|--------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_STM_STIM_BUS_SAFETY_ERR_COMP_ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.409 MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 186CCh) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of STM Target Port.

Return to [Summary Table](#)

**Table 2-1227. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 86CCh       |

**Figure 2-409. MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                           |    |    |    |    |    |    |    |
|-------------------------------------------|----|----|----|----|----|----|----|
| 31                                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                                  |    |    |    |    |    |    |    |
| NONE                                      |    |    |    |    |    |    |    |
| 0h                                        |    |    |    |    |    |    |    |
| 23                                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                                  |    |    |    |    |    |    |    |
| NONE                                      |    |    |    |    |    |    |    |
| 0h                                        |    |    |    |    |    |    |    |
| 15                                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_STM_STIM_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                         |    |    |    |    |    |    |    |
| 0h                                        |    |    |    |    |    |    |    |
| 7                                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_STM_STIM_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                         |    |    |    |    |    |    |    |
| 0h                                        |    |    |    |    |    |    |    |

**Table 2-1229. MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                     | Type | Reset | Description                                                                                                                                                |
|-------|-------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                                  | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_STM_STIM_BUS_SAFETY_ERR_STAT_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_STM_STIM_BUS_SAFETY_ERR_STAT_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.410 MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

#### 1 MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 186D0h) [reset = 0h]

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of STM Target Port.

Return to [Summary Table](#)

**Table 2-1230. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 86D0h       |

**Figure 2-410. MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                           |    |    |    |    |    |    |    |
|-------------------------------------------|----|----|----|----|----|----|----|
| 31                                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_STM_STIM_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                         |    |    |    |    |    |    |    |
| 0h                                        |    |    |    |    |    |    |    |
| 23                                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_STM_STIM_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                         |    |    |    |    |    |    |    |
| 0h                                        |    |    |    |    |    |    |    |
| 15                                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_STM_STIM_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                         |    |    |    |    |    |    |    |
| 0h                                        |    |    |    |    |    |    |    |
| 7                                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_STM_STIM_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                         |    |    |    |    |    |    |    |
| 0h                                        |    |    |    |    |    |    |    |

**Table 2-1232. MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                     | Type | Reset | Description                                                                                                                       |
|------|-------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_STM_STIM_BUS_SAFETY_ERR_STAT_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.411 MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register

#### 1 MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register (Offset = 186D4h) [reset = 0h]

This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of STM Target Port.

Return to [Summary Table](#)

**Table 2-1233. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 86D4h       |

**Figure 2-411. MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_ERR\_STAT\_WRITE Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_STM_STIM_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_STM_STIM_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_STM_STIM_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_STM_STIM_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-1235. MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register Field Descriptions**

| Bit  | Field                                       | Type | Reset | Description                                                                                                        |
|------|---------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_STM_STIM_BUS_SAFETY_ERR_STAT_WRITE_STAT | R    | 0h    | Read this bitfield for comparator status for Write bus for this port. 1'b1 at any bit indicates error on Write Bus |

### 2.2.2.412 MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_ERR\_STAT\_READ Register

#### 1 MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_ERR\_STAT\_READ Register (Offset = 186D8h) [reset = 0h]

This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of STM Target Port.

Return to [Summary Table](#)

**Table 2-1236. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 86D8h       |

**Figure 2-412. MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_ERR\_STAT\_READ Name Register**

|                                            |    |    |    |    |    |    |    |
|--------------------------------------------|----|----|----|----|----|----|----|
| 31                                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_STM_STIM_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 23                                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_STM_STIM_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 15                                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_STM_STIM_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 7                                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_STM_STIM_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |

**Table 2-1238. MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_ERR\_STAT\_READ Register Field Descriptions**

| Bit  | Field                                      | Type | Reset | Description                                                                                                                     |
|------|--------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_STM_STIM_BUS_SAFETY_ERR_STAT_READ_STAT | R    | 0h    | Read this bitfield for comparator status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus. |

### 2.2.2.413 MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register

#### 1 MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register (Offset = 186DCh) [reset = 0h]

This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of STM Target Port.

Return to [Summary Table](#)

**Table 2-1239. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 86DCh       |

**Figure 2-413. MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Name Register**

|                                                 |    |    |    |    |    |    |    |
|-------------------------------------------------|----|----|----|----|----|----|----|
| 31                                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_STM_STIM_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                               |    |    |    |    |    |    |    |
| 0h                                              |    |    |    |    |    |    |    |
| 23                                              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_STM_STIM_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                               |    |    |    |    |    |    |    |
| 0h                                              |    |    |    |    |    |    |    |
| 15                                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_STM_STIM_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                               |    |    |    |    |    |    |    |
| 0h                                              |    |    |    |    |    |    |    |
| 7                                               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_STM_STIM_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                               |    |    |    |    |    |    |    |
| 0h                                              |    |    |    |    |    |    |    |

**Table 2-1241. MSS\_CTRL\_MSS\_STM\_STIM\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register Field Descriptions**

| Bit  | Field                                           | Type | Reset | Description                                                                                                                           |
|------|-------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_STM_STIM_BUS_SAFETY_ERR_STAT_WRITERESP_STAT | R    | 0h    | Read this bitfield for comparator status for Write response bus for this port. 1'b1 at any bit indicates error on Write Response Bus. |



### 2.2.2.414 MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_CTRL Register (Offset = 186E0h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of MMC0 Target Port.

Return to [Summary Table](#)

**Table 2-1242. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 86E0h       |

**Figure 2-414. MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_CTRL Name Register**

|                              |    |    |    |    |                                |    |                                   |
|------------------------------|----|----|----|----|--------------------------------|----|-----------------------------------|
| 31                           | 30 | 29 | 28 | 27 | 26                             | 25 | 24                                |
| RESERVED                     |    |    |    |    |                                |    |                                   |
| NONE                         |    |    |    |    |                                |    |                                   |
| 0h                           |    |    |    |    |                                |    |                                   |
| 23                           | 22 | 21 | 20 | 19 | 18                             | 17 | 16                                |
| MSS_MMC_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                |    |                                   |
| R                            |    |    |    |    |                                |    |                                   |
| 0h                           |    |    |    |    |                                |    |                                   |
| 15                           | 14 | 13 | 12 | 11 | 10                             | 9  | 8                                 |
| RESERVED                     |    |    |    |    |                                |    | MSS_MMC_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                         |    |    |    |    |                                |    | R/W                               |
| 0h                           |    |    |    |    |                                |    | 0h                                |
| 7                            | 6  | 5  | 4  | 3  | 2                              | 1  | 0                                 |
| RESERVED                     |    |    |    |    | MSS_MMC_BUS_SAFETY_CTRL_ENABLE |    |                                   |
| NONE                         |    |    |    |    | R/W                            |    |                                   |
| 0h                           |    |    |    |    | 7h                             |    |                                   |

**Table 2-1244. MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                             | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|-----------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                          | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | MSS_MMC_BUS_SAFETY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                          | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | MSS_MMC_BUS_SAFETY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 7:3   | RESERVED                          | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

**Table 2-1244. MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_CTRL Register Field Descriptions (continued)**

| Bit | Field                          | Type | Reset | Description                                                                                                                                           |
|-----|--------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0 | MSS_MMC_BUS_SAFETY_CTRL_ENABLE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.415 MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_FI Register (Offset = 186E4h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of MMC0 Target Port.

Return to [Summary Table](#)

**Table 2-1245. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 86E4h       |

**Figure 2-415. MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_FI Name Register**

| 31                         | 30                                | 29                                | 28                                                | 27                                                | 26                                        | 25                                        | 24  |
|----------------------------|-----------------------------------|-----------------------------------|---------------------------------------------------|---------------------------------------------------|-------------------------------------------|-------------------------------------------|-----|
| MSS_MMC_BUS_SAFETY_FI_SAFE |                                   |                                   |                                                   |                                                   |                                           |                                           |     |
| R/W                        |                                   |                                   |                                                   |                                                   |                                           |                                           |     |
| 0h                         |                                   |                                   |                                                   |                                                   |                                           |                                           |     |
| 23                         | 22                                | 21                                | 20                                                | 19                                                | 18                                        | 17                                        | 16  |
| MSS_MMC_BUS_SAFETY_FI_MAIN |                                   |                                   |                                                   |                                                   |                                           |                                           |     |
| R/W                        |                                   |                                   |                                                   |                                                   |                                           |                                           |     |
| 0h                         |                                   |                                   |                                                   |                                                   |                                           |                                           |     |
| 15                         | 14                                | 13                                | 12                                                | 11                                                | 10                                        | 9                                         | 8   |
| MSS_MMC_BUS_SAFETY_FI_DATA |                                   |                                   |                                                   |                                                   |                                           |                                           |     |
| R/W                        |                                   |                                   |                                                   |                                                   |                                           |                                           |     |
| 0h                         |                                   |                                   |                                                   |                                                   |                                           |                                           |     |
| 7                          | 6                                 | 5                                 | 4                                                 | 3                                                 | 2                                         | 1                                         | 0   |
| RESERVED                   | MSS_MMC_BU<br>S_SAFETY_FI_<br>DED | MSS_MMC_BU<br>S_SAFETY_FI_<br>SEC | MSS_MMC_BU<br>S_SAFETY_FI_<br>GLOBAL_SAFE<br>_REQ | MSS_MMC_BU<br>S_SAFETY_FI_<br>GLOBAL_MAIN<br>_REQ | MSS_MMC_BU<br>S_SAFETY_FI_<br>GLOBAL_SAFE | MSS_MMC_BU<br>S_SAFETY_FI_<br>GLOBAL_MAIN |     |
| NONE                       | R/W                               | R/W                               | R/W                                               | R/W                                               | R/W                                       | R/W                                       | R/W |
| 0h                         | 0h                                | 0h                                | 0h                                                | 0h                                                | 0h                                        | 0h                                        | 0h  |

**Table 2-1247. MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|----------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_MMC_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_MMC_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_MMC_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5     | MSS_MMC_BUS_SAFETY_FI_DED  | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                                                                                                                                                                                                        |

**Table 2-1247. MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_FI Register Field Descriptions (continued)**

| Bit | Field                                 | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|---------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | MSS_MMC_BUS_SAFETY_FI_SEC             | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_MMC_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit corresponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_MMC_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit corresponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_MMC_BUS_SAFETY_FI_GLOBAL_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_MMC_BUS_SAFETY_FI_GLOBAL_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

### 2.2.2.416 MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_ERR Register (Offset = 186E8h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of MMC0 Target Port.

Return to [Summary Table](#)

**Table 2-1248. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 86E8h       |

**Figure 2-416. MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_ERR Name Register**

|                                   |    |    |    |    |    |    |    |
|-----------------------------------|----|----|----|----|----|----|----|
| 31                                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_MMC_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                 |    |    |    |    |    |    |    |
| 0h                                |    |    |    |    |    |    |    |
| 23                                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_MMC_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                 |    |    |    |    |    |    |    |
| 0h                                |    |    |    |    |    |    |    |
| 15                                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_MMC_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                 |    |    |    |    |    |    |    |
| 0h                                |    |    |    |    |    |    |    |
| 7                                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_MMC_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                 |    |    |    |    |    |    |    |
| 0h                                |    |    |    |    |    |    |    |

**Table 2-1250. MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                             | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|-----------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_MMC_BUS_SAFETY_ERR_DED        | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_MMC_BUS_SAFETY_ERR_SEC        | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_MMC_BUS_SAFETY_ERR_COMP_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-1250. MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_ERR Register Field Descriptions (continued)**

| Bit | Field                           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|---------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_MMC_BUS_SAFETY_ERR_COMP_ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.417 MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 186ECh) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of MMC0 Target Port.

Return to [Summary Table](#)

**Table 2-1251. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 86ECh       |

**Figure 2-417. MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                      |    |    |    |    |    |    |    |
|--------------------------------------|----|----|----|----|----|----|----|
| 31                                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                             |    |    |    |    |    |    |    |
| NONE                                 |    |    |    |    |    |    |    |
| 0h                                   |    |    |    |    |    |    |    |
| 23                                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                             |    |    |    |    |    |    |    |
| NONE                                 |    |    |    |    |    |    |    |
| 0h                                   |    |    |    |    |    |    |    |
| 15                                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_MMC_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                    |    |    |    |    |    |    |    |
| 0h                                   |    |    |    |    |    |    |    |
| 7                                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_MMC_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                    |    |    |    |    |    |    |    |
| 0h                                   |    |    |    |    |    |    |    |

**Table 2-1253. MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                | Type | Reset | Description                                                                                                                                                |
|-------|--------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_MMC_BUS_SAFETY_ERR_STAT_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_MMC_BUS_SAFETY_ERR_STAT_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.418 MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

#### 1 MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 186F0h) [reset = 0h]

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of MMC0 Target Port.

Return to [Summary Table](#)

**Table 2-1254. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 86F0h       |

**Figure 2-418. MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                      |    |    |    |    |    |    |    |
|--------------------------------------|----|----|----|----|----|----|----|
| 31                                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_MMC_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                    |    |    |    |    |    |    |    |
| 0h                                   |    |    |    |    |    |    |    |
| 23                                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_MMC_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                    |    |    |    |    |    |    |    |
| 0h                                   |    |    |    |    |    |    |    |
| 15                                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_MMC_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                    |    |    |    |    |    |    |    |
| 0h                                   |    |    |    |    |    |    |    |
| 7                                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_MMC_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                    |    |    |    |    |    |    |    |
| 0h                                   |    |    |    |    |    |    |    |

**Table 2-1256. MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                | Type | Reset | Description                                                                                                                       |
|------|--------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_MMC_BUS_SAFETY_ERR_STAT_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |



### 2.2.2.419 MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register

#### 1 MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register (Offset = 186F4h) [reset = 0h]

This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of MMC0 Target Port.

Return to [Summary Table](#)

**Table 2-1257. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 86F4h       |

**Figure 2-419. MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_ERR\_STAT\_WRITE Name Register**

|                                        |    |    |    |    |    |    |    |
|----------------------------------------|----|----|----|----|----|----|----|
| 31                                     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_MMC_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 23                                     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_MMC_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 15                                     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_MMC_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 7                                      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_MMC_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |

**Table 2-1259. MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register Field Descriptions**

| Bit  | Field                                  | Type | Reset | Description                                                                                                        |
|------|----------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_MMC_BUS_SAFETY_ERR_STAT_WRITE_STAT | R    | 0h    | Read this bitfield for comparator status for Write bus for this port. 1'b1 at any bit indicates error on Write Bus |

### 2.2.2.420 MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_ERR\_STAT\_READ Register

#### 1 MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_ERR\_STAT\_READ Register (Offset = 186F8h) [reset = 0h]

This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of MMC0 Target Port.

Return to [Summary Table](#)

**Table 2-1260. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 86F8h       |

**Figure 2-420. MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_ERR\_STAT\_READ Name Register**

|                                       |    |    |    |    |    |    |    |
|---------------------------------------|----|----|----|----|----|----|----|
| 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_MMC_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 23                                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_MMC_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 15                                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_MMC_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 7                                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_MMC_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |

**Table 2-1262. MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_ERR\_STAT\_READ Register Field Descriptions**

| Bit  | Field                                 | Type | Reset | Description                                                                                                                     |
|------|---------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_MMC_BUS_SAFETY_ERR_STAT_READ_STAT | R    | 0h    | Read this bitfield for comparator status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus. |

### 2.2.2.421 MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register

#### 1 MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register (Offset = 186FCh) [reset = 0h]

This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of MMC0 Target Port.

Return to [Summary Table](#)

**Table 2-1263. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 86FCh       |

**Figure 2-421. MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Name Register**

|                                            |    |    |    |    |    |    |    |
|--------------------------------------------|----|----|----|----|----|----|----|
| 31                                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_MMC_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 23                                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_MMC_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 15                                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_MMC_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 7                                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_MMC_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |

**Table 2-1265. MSS\_CTRL\_MSS\_MMC\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register Field Descriptions**

| Bit  | Field                                      | Type | Reset | Description                                                                                                                           |
|------|--------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_MMC_BUS_SAFETY_ERR_STAT_WRITERESP_STAT | R    | 0h    | Read this bitfield for comparator status for Write response bus for this port. 1'b1 at any bit indicates error on Write Response Bus. |

### 2.2.2.422 MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_CTRL Register (Offset = 18700h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of GPMC0 Target Port.

Return to [Summary Table](#)

**Table 2-1266. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8700h       |

**Figure 2-422. MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_CTRL Name Register**

|                               |    |    |    |    |                                 |    |                                                |
|-------------------------------|----|----|----|----|---------------------------------|----|------------------------------------------------|
| 31                            | 30 | 29 | 28 | 27 | 26                              | 25 | 24                                             |
| RESERVED                      |    |    |    |    |                                 |    |                                                |
| NONE                          |    |    |    |    |                                 |    |                                                |
| 0h                            |    |    |    |    |                                 |    |                                                |
| 23                            | 22 | 21 | 20 | 19 | 18                              | 17 | 16                                             |
| MSS_GPMC_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                 |    |                                                |
| R                             |    |    |    |    |                                 |    |                                                |
| 0h                            |    |    |    |    |                                 |    |                                                |
| 15                            | 14 | 13 | 12 | 11 | 10                              | 9  | 8                                              |
| RESERVED                      |    |    |    |    |                                 |    | MSS_GPMC_B<br>US_SAFETY_C<br>TRL_ERR_CLE<br>AR |
| NONE                          |    |    |    |    |                                 |    | R/W                                            |
| 0h                            |    |    |    |    |                                 |    | 0h                                             |
| 7                             | 6  | 5  | 4  | 3  | 2                               | 1  | 0                                              |
| RESERVED                      |    |    |    |    | MSS_GPMC_BUS_SAFETY_CTRL_ENABLE |    |                                                |
| NONE                          |    |    |    |    | R/W                             |    |                                                |
| 0h                            |    |    |    |    | 7h                              |    |                                                |

**Table 2-1268. MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|----------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                               | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 23:16 | MSS_GPMC_BUS_SAFE<br>TY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/ initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/ initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/ initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                               | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 8     | MSS_GPMC_BUS_SAFE<br>TY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 7:3   | RESERVED                               | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

**Table 2-1268. MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_CTRL Register Field Descriptions (continued)**

| Bit | Field                           | Type | Reset | Description                                                                                                                                           |
|-----|---------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0 | MSS_GPMC_BUS_SAFETY_CTRL_ENABLE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.423 MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_FI Register (Offset = 18704h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of GPMC0 Target Port.

Return to [Summary Table](#)

**Table 2-1269. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8704h       |

**Figure 2-423. MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_FI Name Register**

| 31                          | 30                                 | 29                                 | 28                                                 | 27                                                 | 26                                             | 25                                             | 24                                             |
|-----------------------------|------------------------------------|------------------------------------|----------------------------------------------------|----------------------------------------------------|------------------------------------------------|------------------------------------------------|------------------------------------------------|
| MSS_GPMC_BUS_SAFETY_FI_SAFE |                                    |                                    |                                                    |                                                    |                                                |                                                |                                                |
| R/W                         |                                    |                                    |                                                    |                                                    |                                                |                                                |                                                |
| 0h                          |                                    |                                    |                                                    |                                                    |                                                |                                                |                                                |
| 23                          | 22                                 | 21                                 | 20                                                 | 19                                                 | 18                                             | 17                                             | 16                                             |
| MSS_GPMC_BUS_SAFETY_FI_MAIN |                                    |                                    |                                                    |                                                    |                                                |                                                |                                                |
| R/W                         |                                    |                                    |                                                    |                                                    |                                                |                                                |                                                |
| 0h                          |                                    |                                    |                                                    |                                                    |                                                |                                                |                                                |
| 15                          | 14                                 | 13                                 | 12                                                 | 11                                                 | 10                                             | 9                                              | 8                                              |
| MSS_GPMC_BUS_SAFETY_FI_DATA |                                    |                                    |                                                    |                                                    |                                                |                                                |                                                |
| R/W                         |                                    |                                    |                                                    |                                                    |                                                |                                                |                                                |
| 0h                          |                                    |                                    |                                                    |                                                    |                                                |                                                |                                                |
| 7                           | 6                                  | 5                                  | 4                                                  | 3                                                  | 2                                              | 1                                              | 0                                              |
| RESERVED                    | MSS_GPMC_B<br>US_SAFETY_F<br>I_DED | MSS_GPMC_B<br>US_SAFETY_F<br>I_SEC | MSS_GPMC_B<br>US_SAFETY_F<br>I_GLOBAL_SA<br>FE_REQ | MSS_GPMC_B<br>US_SAFETY_F<br>I_GLOBAL_MAI<br>N_REQ | MSS_GPMC_B<br>US_SAFETY_F<br>I_GLOBAL_SA<br>FE | MSS_GPMC_B<br>US_SAFETY_F<br>I_GLOBAL_MAI<br>N | MSS_GPMC_B<br>US_SAFETY_F<br>I_GLOBAL_MAI<br>N |
| NONE                        | R/W                                | R/W                                | R/W                                                | R/W                                                | R/W                                            | R/W                                            | R/W                                            |
| 0h                          | 0h                                 | 0h                                 | 0h                                                 | 0h                                                 | 0h                                             | 0h                                             | 0h                                             |

**Table 2-1271. MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|---------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_GPMC_BUS_SAFE<br>TY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_GPMC_BUS_SAFE<br>TY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_GPMC_BUS_SAFE<br>TY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5     | MSS_GPMC_BUS_SAFE<br>TY_FI_DED  | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                                                                                                                                                                                                        |

**Table 2-1271. MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_FI Register Field Descriptions (continued)**

| Bit | Field                                  | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|----------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | MSS_GPMC_BUS_SAFETY_FI_SEC             | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_GPMC_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_GPMC_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_GPMC_BUS_SAFETY_FI_GLOBAL_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_GPMC_BUS_SAFETY_FI_GLOBAL_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

### 2.2.2.424 MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_ERR Register (Offset = 18708h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of GPMC0 Target Port.

Return to [Summary Table](#)

**Table 2-1272. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8708h       |

**Figure 2-424. MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_ERR Name Register**

|                                    |    |    |    |    |    |    |    |
|------------------------------------|----|----|----|----|----|----|----|
| 31                                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_GPMC_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |
| 23                                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_GPMC_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |
| 15                                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_GPMC_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |
| 7                                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_GPMC_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                  |    |    |    |    |    |    |    |
| 0h                                 |    |    |    |    |    |    |    |

**Table 2-1274. MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_GPMC_BUS_SAFETY_ERR_DED        | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_GPMC_BUS_SAFETY_ERR_SEC        | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_GPMC_BUS_SAFETY_ERR_COMP_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |



**Table 2-1274. MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_ERR Register Field Descriptions (continued)**

| Bit | Field                            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|----------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_GPMC_BUS_SAFETY_ERR_COMP_ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.425 MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

#### 1 MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 1870Ch) [reset = 0h]

This register Indicates the Error Syndrome of Data errors in Bus Safety Comparator of GPMC0 Target Port.

Return to [Summary Table](#)

**Table 2-1275. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 870Ch       |

**Figure 2-425. MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                       |    |    |    |    |    |    |    |
|---------------------------------------|----|----|----|----|----|----|----|
| 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 23                                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 15                                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_GPMC_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 7                                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_GPMC_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |

**Table 2-1277. MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                 | Type | Reset | Description                                                                                                                                                |
|-------|---------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                              | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_GPMC_BUS_SAFETY_ERR_STAT_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_GPMC_BUS_SAFETY_ERR_STAT_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.426 MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

#### 1 MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 18710h) [reset = 0h]

This register Indicates the Error Syndrome of Command errors in Bus Safety Comparator of GPMC0 Target Port.

Return to [Summary Table](#)

**Table 2-1278. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8710h       |

**Figure 2-426. MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                       |    |    |    |    |    |    |    |
|---------------------------------------|----|----|----|----|----|----|----|
| 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_GPMC_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 23                                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_GPMC_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 15                                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_GPMC_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 7                                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_GPMC_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |

**Table 2-1280. MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                 | Type | Reset | Description                                                                                                                       |
|------|---------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_GPMC_BUS_SAFETY_ERR_STAT_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.427 MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register

#### 1 MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register (Offset = 18714h) [reset = 0h]

This register Indicates the Error Syndrome of Write errors in Bus Safety Comparator of GPMC0 Target Port.

Return to [Summary Table](#)

**Table 2-1281. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8714h       |

**Figure 2-427. MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_ERR\_STAT\_WRITE Name Register**

|                                         |    |    |    |    |    |    |    |
|-----------------------------------------|----|----|----|----|----|----|----|
| 31                                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_GPMC_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 23                                      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_GPMC_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 15                                      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_GPMC_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 7                                       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_GPMC_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |

**Table 2-1283. MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register Field Descriptions**

| Bit  | Field                                   | Type | Reset | Description                                                                                                        |
|------|-----------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_GPMC_BUS_SAFETY_ERR_STAT_WRITE_STAT | R    | 0h    | Read this bitfield for comparator status for Write bus for this port. 1'b1 at any bit indicates error on Write Bus |

### 2.2.2.428 MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_ERR\_STAT\_READ Register

#### 1 MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_ERR\_STAT\_READ Register (Offset = 18718h) [reset = 0h]

This register Indicates the Error Syndrome of Read errors in Bus Safety Comparator of GPMC0 Target Port.

Return to [Summary Table](#)

**Table 2-1284. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8718h       |

**Figure 2-428. MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_ERR\_STAT\_READ Name Register**

|                                        |    |    |    |    |    |    |    |
|----------------------------------------|----|----|----|----|----|----|----|
| 31                                     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_GPMC_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 23                                     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_GPMC_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 15                                     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_GPMC_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |
| 7                                      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_GPMC_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                      |    |    |    |    |    |    |    |
| 0h                                     |    |    |    |    |    |    |    |

**Table 2-1286. MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_ERR\_STAT\_READ Register Field Descriptions**

| Bit  | Field                                  | Type | Reset | Description                                                                                                                     |
|------|----------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_GPMC_BUS_SAFETY_ERR_STAT_READ_STAT | R    | 0h    | Read this bitfield for comparator status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus. |

### 2.2.2.429 MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register

#### 1 MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register (Offset = 1871Ch) [reset = 0h]

This register Indicates the Error Syndrome of WriteResponse errors in Bus Safety Comparator of GPMC0 Target Port.

Return to [Summary Table](#)

**Table 2-1287. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 871Ch       |

**Figure 2-429. MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_GPMC_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_GPMC_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_GPMC_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_GPMC_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-1289. MSS\_CTRL\_MSS\_GPMC\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register Field Descriptions**

| Bit  | Field                                       | Type | Reset | Description                                                                                                                           |
|------|---------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_GPMC_BUS_SAFETY_ERR_STAT_WRITERESP_STAT | R    | 0h    | Read this bitfield for comparator status for Write response bus for this port. 1'b1 at any bit indicates error on Write Response Bus. |

### 2.2.2.430 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_CTRL Register (Offset = 18740h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS0 CORE0 Peripheral Port.

Return to [Summary Table](#)

**Table 2-1290. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8740h       |

**Figure 2-430. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_CTRL Name Register**

|                                    |    |    |    |    |                                      |    |                                         |
|------------------------------------|----|----|----|----|--------------------------------------|----|-----------------------------------------|
| 31                                 | 30 | 29 | 28 | 27 | 26                                   | 25 | 24                                      |
| RESERVED                           |    |    |    |    |                                      |    |                                         |
| NONE                               |    |    |    |    |                                      |    |                                         |
| 0h                                 |    |    |    |    |                                      |    |                                         |
| 23                                 | 22 | 21 | 20 | 19 | 18                                   | 17 | 16                                      |
| MSS_CR5A0_AHB_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                      |    |                                         |
| R                                  |    |    |    |    |                                      |    |                                         |
| 0h                                 |    |    |    |    |                                      |    |                                         |
| 15                                 | 14 | 13 | 12 | 11 | 10                                   | 9  | 8                                       |
| RESERVED                           |    |    |    |    |                                      |    | MSS_CR5A0_AHB_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                               |    |    |    |    |                                      |    | R/W                                     |
| 0h                                 |    |    |    |    |                                      |    | 0h                                      |
| 7                                  | 6  | 5  | 4  | 3  | 2                                    | 1  | 0                                       |
| RESERVED                           |    |    |    |    | MSS_CR5A0_AHB_BUS_SAFETY_CTRL_ENABLE |    |                                         |
| NONE                               |    |    |    |    | R/W                                  |    |                                         |
| 0h                                 |    |    |    |    | 7h                                   |    |                                         |

**Table 2-1292. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|-----------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                                | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | MSS_CR5A0_AHB_BUS_SAFETY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                                | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | MSS_CR5A0_AHB_BUS_SAFETY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

**Table 2-1292. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_CTRL Register Field Descriptions  
(continued)**

| Bit | Field                                | Type | Reset | Description                                                                                                                                           |
|-----|--------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:3 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                                              |
| 2:0 | MSS_CR5A0_AHB_BUS_SAFETY_CTRL_ENABLE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |



### 2.2.2.431 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_FI Register (Offset = 18744h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of R5SS0 CORE0 Peripheral Port.

Return to [Summary Table](#)

**Table 2-1293. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8744h       |

**Figure 2-431. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_FI Name Register**

| 31                               | 30                                      | 29                                      | 28                                                      | 27                                                      | 26                                                  | 25                                                  | 24  |
|----------------------------------|-----------------------------------------|-----------------------------------------|---------------------------------------------------------|---------------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|-----|
| MSS_CR5A0_AHB_BUS_SAFETY_FI_SAFE |                                         |                                         |                                                         |                                                         |                                                     |                                                     |     |
| R/W                              |                                         |                                         |                                                         |                                                         |                                                     |                                                     |     |
| 0h                               |                                         |                                         |                                                         |                                                         |                                                     |                                                     |     |
| 23                               | 22                                      | 21                                      | 20                                                      | 19                                                      | 18                                                  | 17                                                  | 16  |
| MSS_CR5A0_AHB_BUS_SAFETY_FI_MAIN |                                         |                                         |                                                         |                                                         |                                                     |                                                     |     |
| R/W                              |                                         |                                         |                                                         |                                                         |                                                     |                                                     |     |
| 0h                               |                                         |                                         |                                                         |                                                         |                                                     |                                                     |     |
| 15                               | 14                                      | 13                                      | 12                                                      | 11                                                      | 10                                                  | 9                                                   | 8   |
| MSS_CR5A0_AHB_BUS_SAFETY_FI_DATA |                                         |                                         |                                                         |                                                         |                                                     |                                                     |     |
| R/W                              |                                         |                                         |                                                         |                                                         |                                                     |                                                     |     |
| 0h                               |                                         |                                         |                                                         |                                                         |                                                     |                                                     |     |
| 7                                | 6                                       | 5                                       | 4                                                       | 3                                                       | 2                                                   | 1                                                   | 0   |
| RESERVED                         | MSS_CR5A0_A<br>HB_BUS_SAFE<br>TY_FI_DED | MSS_CR5A0_A<br>HB_BUS_SAFE<br>TY_FI_SEC | MSS_CR5A0_A<br>HB_BUS_SAFE<br>TY_FI_GLOBA<br>L_SAFE_REQ | MSS_CR5A0_A<br>HB_BUS_SAFE<br>TY_FI_GLOBA<br>L_MAIN_REQ | MSS_CR5A0_A<br>HB_BUS_SAFE<br>TY_FI_GLOBA<br>L_SAFE | MSS_CR5A0_A<br>HB_BUS_SAFE<br>TY_FI_GLOBA<br>L_MAIN |     |
| NONE                             | R/W                                     | R/W                                     | R/W                                                     | R/W                                                     | R/W                                                 | R/W                                                 | R/W |
| 0h                               | 0h                                      | 0h                                      | 0h                                                      | 0h                                                      | 0h                                                  | 0h                                                  | 0h  |

**Table 2-1295. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|----------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5A0_AHB_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_CR5A0_AHB_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_CR5A0_AHB_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5     | MSS_CR5A0_AHB_BUS_SAFETY_FI_DED  | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                                                                                                                                                                                                        |

**Table 2-1295. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_FI Register Field Descriptions  
(continued)**

| Bit | Field                                       | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|---------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | MSS_CR5A0_AHB_BUS_SAFETY_FI_SEC             | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_CR5A0_AHB_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_CR5A0_AHB_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_CR5A0_AHB_BUS_SAFETY_FI_GLOBAL_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_CR5A0_AHB_BUS_SAFETY_FI_GLOBAL_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

## 2.2.2.432 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_ERR Register

### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_ERR Register (Offset = 18748h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of R5SS0 CORE0 Peripheral Port.

Return to [Summary Table](#)

**Table 2-1296. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8748h       |

**Figure 2-432. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_ERR Name Register**

|                                         |    |    |    |    |    |    |    |
|-----------------------------------------|----|----|----|----|----|----|----|
| 31                                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A0_AHB_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 23                                      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A0_AHB_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 15                                      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A0_AHB_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 7                                       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A0_AHB_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |

**Table 2-1298. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                                   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|-----------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5A0_AHB_BUS_SAFETY_ERR_DED        | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_CR5A0_AHB_BUS_SAFETY_ERR_SEC        | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_CR5A0_AHB_BUS_SAFETY_ERR_COMP_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-1298. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_ERR Register Field Descriptions  
(continued)**

| Bit | Field                                 | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|---------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_CR5A0_AHB_BUS_SAFETY_ERR_COMP_ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.433 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

**1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 1874Ch)**  
[reset = 0h]

MSS\_CR5A\_AHB\_BUS\_SAFETY\_ERR\_STAT\_DATA0.

Return to [Summary Table](#)

**Table 2-1299. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 874Ch       |

**Figure 2-433. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                            |    |    |    |    |    |    |    |
|--------------------------------------------|----|----|----|----|----|----|----|
| 31                                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                                   |    |    |    |    |    |    |    |
| NONE                                       |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 23                                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                                   |    |    |    |    |    |    |    |
| NONE                                       |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 15                                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A0_AHB_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 7                                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A0_AHB_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |

**Table 2-1301. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                      | Type | Reset | Description                                                                                                                                                |
|-------|--------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                                   | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_CR5A0_AHB_BUS_SAFETY_ERR_STAT_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_CR5A0_AHB_BUS_SAFETY_ERR_STAT_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.434 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

**1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 18750h)**  
[reset = 0h]

MSS\_CR5A\_AHB\_BUS\_SAFETY\_ERR\_STAT\_CMD.

Return to [Summary Table](#)

**Table 2-1302. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8750h       |

**Figure 2-434. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                            |    |    |    |    |    |    |    |
|--------------------------------------------|----|----|----|----|----|----|----|
| 31                                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A0_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 23                                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A0_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 15                                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A0_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 7                                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A0_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |

**Table 2-1304. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                      | Type | Reset | Description                                                                                                                       |
|------|--------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5A0_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.435 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register

**1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register (Offset = 18754h)**  
[reset = 0h]

MSS\_CR5A0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITE.

Return to [Summary Table](#)

**Table 2-1305. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8754h       |

**Figure 2-435. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITE Name Register**

|                                              |    |    |    |    |    |    |    |
|----------------------------------------------|----|----|----|----|----|----|----|
| 31                                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A0_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 23                                           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A0_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 15                                           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A0_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 7                                            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A0_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |

**Table 2-1307. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register Field Descriptions**

| Bit  | Field                                        | Type | Reset | Description                                                                                                        |
|------|----------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5A0_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT | R    | 0h    | Read this bitfield for comparator status for Write bus for this port. 1'b1 at any bit indicates error on Write Bus |

### 2.2.2.436 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_READ Register

**1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_READ Register (Offset = 18758h)**  
[reset = 0h]

MSS\_CR5A0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_READ.

Return to [Summary Table](#)

**Table 2-1308. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8758h       |

**Figure 2-436. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_READ Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A0_AHB_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A0_AHB_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A0_AHB_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A0_AHB_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-1310. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_READ Register Field Descriptions**

| Bit  | Field                                       | Type | Reset | Description                                                                                                                     |
|------|---------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5A0_AHB_BUS_SAFETY_ERR_STAT_READ_STAT | R    | 0h    | Read this bitfield for comapartor status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus. |



### 2.2.2.437 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register

**1 MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register (Offset = 1875Ch) [reset = 0h]**

MSS\_CR5A\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP.

Return to [Summary Table](#)

**Table 2-1311. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 875Ch       |

**Figure 2-437. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Name Register**

|                                                  |    |    |    |    |    |    |    |
|--------------------------------------------------|----|----|----|----|----|----|----|
| 31                                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A0_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                |    |    |    |    |    |    |    |
| 0h                                               |    |    |    |    |    |    |    |
| 23                                               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A0_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                |    |    |    |    |    |    |    |
| 0h                                               |    |    |    |    |    |    |    |
| 15                                               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A0_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                |    |    |    |    |    |    |    |
| 0h                                               |    |    |    |    |    |    |    |
| 7                                                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A0_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                |    |    |    |    |    |    |    |
| 0h                                               |    |    |    |    |    |    |    |

**Table 2-1313. MSS\_CTRL\_MSS\_R5SS0\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register Field Descriptions**

| Bit  | Field                                            | Type | Reset | Description                                                                                                                           |
|------|--------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5A0_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT | R    | 0h    | Read this bitfield for comparator status for Write response bus for this port. 1'b1 at any bit indicates error on Write Response Bus. |

### 2.2.2.438 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_CTRL Register (Offset = 18760h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS0 CORE1 Peripheral Port.

Return to [Summary Table](#)

**Table 2-1314. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8760h       |

**Figure 2-438. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_CTRL Name Register**

|                                    |    |    |    |    |                                      |    |                                         |
|------------------------------------|----|----|----|----|--------------------------------------|----|-----------------------------------------|
| 31                                 | 30 | 29 | 28 | 27 | 26                                   | 25 | 24                                      |
| RESERVED                           |    |    |    |    |                                      |    |                                         |
| NONE                               |    |    |    |    |                                      |    |                                         |
| 0h                                 |    |    |    |    |                                      |    |                                         |
| 23                                 | 22 | 21 | 20 | 19 | 18                                   | 17 | 16                                      |
| MSS_CR5B0_AHB_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                      |    |                                         |
| R                                  |    |    |    |    |                                      |    |                                         |
| 0h                                 |    |    |    |    |                                      |    |                                         |
| 15                                 | 14 | 13 | 12 | 11 | 10                                   | 9  | 8                                       |
| RESERVED                           |    |    |    |    |                                      |    | MSS_CR5B0_AHB_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                               |    |    |    |    |                                      |    | R/W                                     |
| 0h                                 |    |    |    |    |                                      |    | 0h                                      |
| 7                                  | 6  | 5  | 4  | 3  | 2                                    | 1  | 0                                       |
| RESERVED                           |    |    |    |    | MSS_CR5B0_AHB_BUS_SAFETY_CTRL_ENABLE |    |                                         |
| NONE                               |    |    |    |    | R/W                                  |    |                                         |
| 0h                                 |    |    |    |    | 7h                                   |    |                                         |

**Table 2-1316. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|-----------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                                | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | MSS_CR5B0_AHB_BUS_SAFETY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                                | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | MSS_CR5B0_AHB_BUS_SAFETY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

**Table 2-1316. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_CTRL Register Field Descriptions  
(continued)**

| Bit | Field                                | Type | Reset | Description                                                                                                                                           |
|-----|--------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:3 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                                              |
| 2:0 | MSS_CR5B0_AHB_BUS_SAFETY_CTRL_ENABLE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.439 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_FI Register (Offset = 18764h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of R5SS0 CORE1 Peripheral Port.

Return to [Summary Table](#)

**Table 2-1317. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8764h       |

**Figure 2-439. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_FI Name Register**

| 31                               | 30                                      | 29                                      | 28                                                      | 27                                                      | 26                                                  | 25                                                  | 24                                                  |
|----------------------------------|-----------------------------------------|-----------------------------------------|---------------------------------------------------------|---------------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|
| MSS_CR5B0_AHB_BUS_SAFETY_FI_SAFE |                                         |                                         |                                                         |                                                         |                                                     |                                                     |                                                     |
| R/W                              |                                         |                                         |                                                         |                                                         |                                                     |                                                     |                                                     |
| 0h                               |                                         |                                         |                                                         |                                                         |                                                     |                                                     |                                                     |
| 23                               | 22                                      | 21                                      | 20                                                      | 19                                                      | 18                                                  | 17                                                  | 16                                                  |
| MSS_CR5B0_AHB_BUS_SAFETY_FI_MAIN |                                         |                                         |                                                         |                                                         |                                                     |                                                     |                                                     |
| R/W                              |                                         |                                         |                                                         |                                                         |                                                     |                                                     |                                                     |
| 0h                               |                                         |                                         |                                                         |                                                         |                                                     |                                                     |                                                     |
| 15                               | 14                                      | 13                                      | 12                                                      | 11                                                      | 10                                                  | 9                                                   | 8                                                   |
| MSS_CR5B0_AHB_BUS_SAFETY_FI_DATA |                                         |                                         |                                                         |                                                         |                                                     |                                                     |                                                     |
| R/W                              |                                         |                                         |                                                         |                                                         |                                                     |                                                     |                                                     |
| 0h                               |                                         |                                         |                                                         |                                                         |                                                     |                                                     |                                                     |
| 7                                | 6                                       | 5                                       | 4                                                       | 3                                                       | 2                                                   | 1                                                   | 0                                                   |
| RESERVED                         | MSS_CR5B0_A<br>HB_BUS_SAFE<br>TY_FI_DED | MSS_CR5B0_A<br>HB_BUS_SAFE<br>TY_FI_SEC | MSS_CR5B0_A<br>HB_BUS_SAFE<br>TY_FI_GLOBA<br>L_SAFE_REQ | MSS_CR5B0_A<br>HB_BUS_SAFE<br>TY_FI_GLOBA<br>L_MAIN_REQ | MSS_CR5B0_A<br>HB_BUS_SAFE<br>TY_FI_GLOBA<br>L_SAFE | MSS_CR5B0_A<br>HB_BUS_SAFE<br>TY_FI_GLOBA<br>L_MAIN | MSS_CR5B0_A<br>HB_BUS_SAFE<br>TY_FI_GLOBA<br>L_MAIN |
| NONE                             | R/W                                     | R/W                                     | R/W                                                     | R/W                                                     | R/W                                                 | R/W                                                 | R/W                                                 |
| 0h                               | 0h                                      | 0h                                      | 0h                                                      | 0h                                                      | 0h                                                  | 0h                                                  | 0h                                                  |

**Table 2-1319. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|----------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5B0_AHB_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_CR5B0_AHB_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_CR5B0_AHB_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5     | MSS_CR5B0_AHB_BUS_SAFETY_FI_DED  | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                                                                                                                                                                                                        |

**Table 2-1319. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_FI Register Field Descriptions  
(continued)**

| Bit | Field                                       | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|---------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | MSS_CR5B0_AHB_BUS_SAFETY_FI_SEC             | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_CR5B0_AHB_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_CR5B0_AHB_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_CR5B0_AHB_BUS_SAFETY_FI_GLOBAL_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_CR5B0_AHB_BUS_SAFETY_FI_GLOBAL_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

### 2.2.2.440 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_ERR Register (Offset = 18768h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of R5SS0 CORE1 Peripheral Port.

Return to [Summary Table](#)

**Table 2-1320. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8768h       |

**Figure 2-440. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_ERR Name Register**

|                                         |    |    |    |    |    |    |    |
|-----------------------------------------|----|----|----|----|----|----|----|
| 31                                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B0_AHB_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 23                                      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B0_AHB_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 15                                      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B0_AHB_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 7                                       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B0_AHB_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |

**Table 2-1322. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                                   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|-----------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5B0_AHB_BUS_SAFETY_ERR_DED        | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_CR5B0_AHB_BUS_SAFETY_ERR_SEC        | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_CR5B0_AHB_BUS_SAFETY_ERR_COMP_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-1322. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_ERR Register Field Descriptions  
(continued)**

| Bit | Field                                 | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|---------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_CR5B0_AHB_BUS_SAFETY_ERR_COMP_ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.441 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

**1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 1876Ch)**  
[reset = 0h]

MSS\_CR5B\_AHB\_BUS\_SAFETY\_ERR\_STAT\_DATA0.

Return to [Summary Table](#)

**Table 2-1323. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 876Ch       |

**Figure 2-441. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                            |    |    |    |    |    |    |    |
|--------------------------------------------|----|----|----|----|----|----|----|
| 31                                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                                   |    |    |    |    |    |    |    |
| NONE                                       |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 23                                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                                   |    |    |    |    |    |    |    |
| NONE                                       |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 15                                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B0_AHB_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 7                                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B0_AHB_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |

**Table 2-1325. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                      | Type | Reset | Description                                                                                                                                                |
|-------|--------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                                   | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_CR5B0_AHB_BUS_SAFETY_ERR_STAT_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_CR5B0_AHB_BUS_SAFETY_ERR_STAT_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |



### 2.2.2.442 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

**1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 18770h)**  
[reset = 0h]

MSS\_CR5B\_AHB\_BUS\_SAFETY\_ERR\_STAT\_CMD.

Return to [Summary Table](#)

**Table 2-1326. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8770h       |

**Figure 2-442. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                            |    |    |    |    |    |    |    |
|--------------------------------------------|----|----|----|----|----|----|----|
| 31                                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B0_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 23                                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B0_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 15                                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B0_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 7                                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B0_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |

**Table 2-1328. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                      | Type | Reset | Description                                                                                                                       |
|------|--------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5B0_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.443 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register

**1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register (Offset = 18774h)**  
[reset = 0h]

MSS\_CR5B\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITE.

Return to [Summary Table](#)

**Table 2-1329. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8774h       |

**Figure 2-443. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITE Name Register**

|                                              |    |    |    |    |    |    |    |
|----------------------------------------------|----|----|----|----|----|----|----|
| 31                                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B0_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 23                                           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B0_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 15                                           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B0_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 7                                            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B0_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |

**Table 2-1331. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register Field Descriptions**

| Bit  | Field                                        | Type | Reset | Description                                                                                                        |
|------|----------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5B0_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT | R    | 0h    | Read this bitfield for comparator status for Write bus for this port. 1'b1 at any bit indicates error on Write Bus |

### 2.2.2.444 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_READ Register

**1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_READ Register (Offset = 18778h)**  
[reset = 0h]

MSS\_CR5B\_AHB\_BUS\_SAFETY\_ERR\_STAT\_READ.

Return to [Summary Table](#)

**Table 2-1332. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8778h       |

**Figure 2-444. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_READ Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B0_AHB_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B0_AHB_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B0_AHB_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B0_AHB_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-1334. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_READ Register Field Descriptions**

| Bit  | Field                                       | Type | Reset | Description                                                                                                                     |
|------|---------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5B0_AHB_BUS_SAFETY_ERR_STAT_READ_STAT | R    | 0h    | Read this bitfield for comapartor status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus. |

### 2.2.2.445 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register

**1 MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register (Offset = 1877Ch) [reset = 0h]**

MSS\_CR5B\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP.

Return to [Summary Table](#)

**Table 2-1335. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 877Ch       |

**Figure 2-445. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Name Register**

|                                                  |    |    |    |    |    |    |    |
|--------------------------------------------------|----|----|----|----|----|----|----|
| 31                                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B0_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                |    |    |    |    |    |    |    |
| 0h                                               |    |    |    |    |    |    |    |
| 23                                               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B0_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                |    |    |    |    |    |    |    |
| 0h                                               |    |    |    |    |    |    |    |
| 15                                               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B0_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                |    |    |    |    |    |    |    |
| 0h                                               |    |    |    |    |    |    |    |
| 7                                                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B0_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                |    |    |    |    |    |    |    |
| 0h                                               |    |    |    |    |    |    |    |

**Table 2-1337. MSS\_CTRL\_MSS\_R5SS0\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register Field Descriptions**

| Bit  | Field                                            | Type | Reset | Description                                                                                                                           |
|------|--------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5B0_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT | R    | 0h    | Read this bitfield for comparator status for Write response bus for this port. 1'b1 at any bit indicates error on Write Response Bus. |

## 2.2.2.446 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_CTRL Register

### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_CTRL Register (Offset = 18780h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS1 CORE0 Peripheral Port.

Return to [Summary Table](#)

**Table 2-1338. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8780h       |

**Figure 2-446. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_CTRL Name Register**

|                                    |    |    |    |    |                                      |    |                                         |
|------------------------------------|----|----|----|----|--------------------------------------|----|-----------------------------------------|
| 31                                 | 30 | 29 | 28 | 27 | 26                                   | 25 | 24                                      |
| RESERVED                           |    |    |    |    |                                      |    |                                         |
| NONE                               |    |    |    |    |                                      |    |                                         |
| 0h                                 |    |    |    |    |                                      |    |                                         |
| 23                                 | 22 | 21 | 20 | 19 | 18                                   | 17 | 16                                      |
| MSS_CR5A1_AHB_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                      |    |                                         |
| R                                  |    |    |    |    |                                      |    |                                         |
| 0h                                 |    |    |    |    |                                      |    |                                         |
| 15                                 | 14 | 13 | 12 | 11 | 10                                   | 9  | 8                                       |
| RESERVED                           |    |    |    |    |                                      |    | MSS_CR5A1_AHB_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                               |    |    |    |    |                                      |    | R/W                                     |
| 0h                                 |    |    |    |    |                                      |    | 0h                                      |
| 7                                  | 6  | 5  | 4  | 3  | 2                                    | 1  | 0                                       |
| RESERVED                           |    |    |    |    | MSS_CR5A1_AHB_BUS_SAFETY_CTRL_ENABLE |    |                                         |
| NONE                               |    |    |    |    | R/W                                  |    |                                         |
| 0h                                 |    |    |    |    | 7h                                   |    |                                         |

**Table 2-1340. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|-----------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                                | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | MSS_CR5A1_AHB_BUS_SAFETY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                                | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | MSS_CR5A1_AHB_BUS_SAFETY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

**Table 2-1340. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_CTRL Register Field Descriptions  
(continued)**

| Bit | Field                                | Type | Reset | Description                                                                                                                                           |
|-----|--------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:3 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                                              |
| 2:0 | MSS_CR5A1_AHB_BUS_SAFETY_CTRL_ENABLE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.447 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_FI Register (Offset = 18784h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of R5SS1 CORE0 Peripheral Port.

Return to [Summary Table](#)

**Table 2-1341. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8784h       |

**Figure 2-447. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_FI Name Register**

| 31                               | 30                                      | 29                                      | 28                                                      | 27                                                      | 26                                                  | 25                                                  | 24                                                  |
|----------------------------------|-----------------------------------------|-----------------------------------------|---------------------------------------------------------|---------------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|
| MSS_CR5A1_AHB_BUS_SAFETY_FI_SAFE |                                         |                                         |                                                         |                                                         |                                                     |                                                     |                                                     |
| R/W                              |                                         |                                         |                                                         |                                                         |                                                     |                                                     |                                                     |
| 0h                               |                                         |                                         |                                                         |                                                         |                                                     |                                                     |                                                     |
| 23                               | 22                                      | 21                                      | 20                                                      | 19                                                      | 18                                                  | 17                                                  | 16                                                  |
| MSS_CR5A1_AHB_BUS_SAFETY_FI_MAIN |                                         |                                         |                                                         |                                                         |                                                     |                                                     |                                                     |
| R/W                              |                                         |                                         |                                                         |                                                         |                                                     |                                                     |                                                     |
| 0h                               |                                         |                                         |                                                         |                                                         |                                                     |                                                     |                                                     |
| 15                               | 14                                      | 13                                      | 12                                                      | 11                                                      | 10                                                  | 9                                                   | 8                                                   |
| MSS_CR5A1_AHB_BUS_SAFETY_FI_DATA |                                         |                                         |                                                         |                                                         |                                                     |                                                     |                                                     |
| R/W                              |                                         |                                         |                                                         |                                                         |                                                     |                                                     |                                                     |
| 0h                               |                                         |                                         |                                                         |                                                         |                                                     |                                                     |                                                     |
| 7                                | 6                                       | 5                                       | 4                                                       | 3                                                       | 2                                                   | 1                                                   | 0                                                   |
| RESERVED                         | MSS_CR5A1_A<br>HB_BUS_SAFE<br>TY_FI_DED | MSS_CR5A1_A<br>HB_BUS_SAFE<br>TY_FI_SEC | MSS_CR5A1_A<br>HB_BUS_SAFE<br>TY_FI_GLOBA<br>L_SAFE_REQ | MSS_CR5A1_A<br>HB_BUS_SAFE<br>TY_FI_GLOBA<br>L_MAIN_REQ | MSS_CR5A1_A<br>HB_BUS_SAFE<br>TY_FI_GLOBA<br>L_SAFE | MSS_CR5A1_A<br>HB_BUS_SAFE<br>TY_FI_GLOBA<br>L_MAIN | MSS_CR5A1_A<br>HB_BUS_SAFE<br>TY_FI_GLOBA<br>L_MAIN |
| NONE                             | R/W                                     | R/W                                     | R/W                                                     | R/W                                                     | R/W                                                 | R/W                                                 | R/W                                                 |
| 0h                               | 0h                                      | 0h                                      | 0h                                                      | 0h                                                      | 0h                                                  | 0h                                                  | 0h                                                  |

**Table 2-1343. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|----------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5A1_AHB_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_CR5A1_AHB_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_CR5A1_AHB_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5     | MSS_CR5A1_AHB_BUS_SAFETY_FI_DED  | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                                                                                                                                                                                                        |

**Table 2-1343. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_FI Register Field Descriptions  
(continued)**

| Bit | Field                                       | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|---------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | MSS_CR5A1_AHB_BUS_SAFETY_FI_SEC             | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_CR5A1_AHB_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_CR5A1_AHB_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_CR5A1_AHB_BUS_SAFETY_FI_GLOBAL_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_CR5A1_AHB_BUS_SAFETY_FI_GLOBAL_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |



### 2.2.2.448 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_ERR Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_ERR Register (Offset = 18788h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of R5SS1 CORE0 Peripheral Port.

Return to [Summary Table](#)

**Table 2-1344. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8788h       |

**Figure 2-448. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_ERR Name Register**

|                                         |    |    |    |    |    |    |    |
|-----------------------------------------|----|----|----|----|----|----|----|
| 31                                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A1_AHB_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 23                                      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A1_AHB_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 15                                      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A1_AHB_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 7                                       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A1_AHB_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |

**Table 2-1346. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                                   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|-----------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5A1_AHB_BUS_SAFETY_ERR_DED        | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_CR5A1_AHB_BUS_SAFETY_ERR_SEC        | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_CR5A1_AHB_BUS_SAFETY_ERR_COMP_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-1346. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_ERR Register Field Descriptions  
(continued)**

| Bit | Field                                 | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|---------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_CR5A1_AHB_BUS_SAFETY_ERR_COMP_ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.449 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

**1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 1878Ch)**  
[reset = 0h]

MSS\_CR5A\_AHB\_BUS\_SAFETY\_ERR\_STAT\_DATA0.

Return to [Summary Table](#)

**Table 2-1347. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 878Ch       |

**Figure 2-449. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                            |    |    |    |    |    |    |    |
|--------------------------------------------|----|----|----|----|----|----|----|
| 31                                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                                   |    |    |    |    |    |    |    |
| NONE                                       |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 23                                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                                   |    |    |    |    |    |    |    |
| NONE                                       |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 15                                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A1_AHB_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 7                                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A1_AHB_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |

**Table 2-1349. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                      | Type | Reset | Description                                                                                                                                                |
|-------|--------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                                   | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_CR5A1_AHB_BUS_SAFETY_ERR_STAT_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_CR5A1_AHB_BUS_SAFETY_ERR_STAT_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.450 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

**1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 18790h)**  
[reset = 0h]

MSS\_CR5A\_AHB\_BUS\_SAFETY\_ERR\_STAT\_CMD.

Return to [Summary Table](#)

**Table 2-1350. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8790h       |

**Figure 2-450. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                            |    |    |    |    |    |    |    |
|--------------------------------------------|----|----|----|----|----|----|----|
| 31                                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A1_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 23                                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A1_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 15                                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A1_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 7                                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A1_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |

**Table 2-1352. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                      | Type | Reset | Description                                                                                                                       |
|------|--------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5A1_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.451 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register

**1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register (Offset = 18794h)**  
[reset = 0h]

MSS\_CR5A\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITE.

Return to [Summary Table](#)

**Table 2-1353. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8794h       |

**Figure 2-451. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITE Name Register**

|                                              |    |    |    |    |    |    |    |
|----------------------------------------------|----|----|----|----|----|----|----|
| 31                                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A1_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 23                                           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A1_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 15                                           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A1_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 7                                            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A1_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |

**Table 2-1355. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register Field Descriptions**

| Bit  | Field                                        | Type | Reset | Description                                                                                                        |
|------|----------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5A1_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT | R    | 0h    | Read this bitfield for comparator status for Write bus for this port. 1'b1 at any bit indicates error on Write Bus |

### 2.2.2.452 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_READ Register

**1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_READ Register (Offset = 18798h)**  
[reset = 0h]

MSS\_CR5A\_AHB\_BUS\_SAFETY\_ERR\_STAT\_READ.

Return to [Summary Table](#)

**Table 2-1356. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 8798h       |

**Figure 2-452. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_READ Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A1_AHB_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A1_AHB_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A1_AHB_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A1_AHB_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-1358. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_READ Register Field Descriptions**

| Bit  | Field                                       | Type | Reset | Description                                                                                                                     |
|------|---------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5A1_AHB_BUS_SAFETY_ERR_STAT_READ_STAT | R    | 0h    | Read this bitfield for comapartor status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus. |

### 2.2.2.453 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register

**1 MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register (Offset = 1879Ch) [reset = 0h]**

MSS\_CR5A\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP.

Return to [Summary Table](#)

**Table 2-1359. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 879Ch       |

**Figure 2-453. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Name Register**

|                                                  |    |    |    |    |    |    |    |
|--------------------------------------------------|----|----|----|----|----|----|----|
| 31                                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5A1_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                |    |    |    |    |    |    |    |
| 0h                                               |    |    |    |    |    |    |    |
| 23                                               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5A1_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                |    |    |    |    |    |    |    |
| 0h                                               |    |    |    |    |    |    |    |
| 15                                               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5A1_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                |    |    |    |    |    |    |    |
| 0h                                               |    |    |    |    |    |    |    |
| 7                                                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5A1_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                |    |    |    |    |    |    |    |
| 0h                                               |    |    |    |    |    |    |    |

**Table 2-1361. MSS\_CTRL\_MSS\_R5FSS1\_CORE0\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register Field Descriptions**

| Bit  | Field                                            | Type | Reset | Description                                                                                                                           |
|------|--------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5A1_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT | R    | 0h    | Read this bitfield for comparator status for Write response bus for this port. 1'b1 at any bit indicates error on Write Response Bus. |

### 2.2.2.454 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_CTRL Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_CTRL Register (Offset = 187A0h) [reset = 7h]

This register is used to Control and Configure the Interconnect Safety Behaviour of R5SS1 CORE1 Peripheral Port.

Return to [Summary Table](#)

**Table 2-1362. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 87A0h       |

**Figure 2-454. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_CTRL Name Register**

|                                    |    |    |    |    |                                      |    |                                         |
|------------------------------------|----|----|----|----|--------------------------------------|----|-----------------------------------------|
| 31                                 | 30 | 29 | 28 | 27 | 26                                   | 25 | 24                                      |
| RESERVED                           |    |    |    |    |                                      |    |                                         |
| NONE                               |    |    |    |    |                                      |    |                                         |
| 0h                                 |    |    |    |    |                                      |    |                                         |
| 23                                 | 22 | 21 | 20 | 19 | 18                                   | 17 | 16                                      |
| MSS_CR5B1_AHB_BUS_SAFETY_CTRL_TYPE |    |    |    |    |                                      |    |                                         |
| R                                  |    |    |    |    |                                      |    |                                         |
| 0h                                 |    |    |    |    |                                      |    |                                         |
| 15                                 | 14 | 13 | 12 | 11 | 10                                   | 9  | 8                                       |
| RESERVED                           |    |    |    |    |                                      |    | MSS_CR5B1_AHB_BUS_SAFETY_CTRL_ERR_CLEAR |
| NONE                               |    |    |    |    |                                      |    | R/W                                     |
| 0h                                 |    |    |    |    |                                      |    | 0h                                      |
| 7                                  | 6  | 5  | 4  | 3  | 2                                    | 1  | 0                                       |
| RESERVED                           |    |    |    |    | MSS_CR5B1_AHB_BUS_SAFETY_CTRL_ENABLE |    |                                         |
| NONE                               |    |    |    |    | R/W                                  |    |                                         |
| 0h                                 |    |    |    |    | 7h                                   |    |                                         |

**Table 2-1364. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_CTRL Register Field Descriptions**

| Bit   | Field                                   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|-----------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                                | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 23:16 | MSS_CR5B1_AHB_BUS_SAFETY_CTRL_TYPE      | R    | 0h    | This bitfield gives a top level idea of the available bus [cmd,wr,ws,rd] for the particular Target/Initiator and whether it follows the VBUS protocol or not.<br>Bit 0 - 1'b1 indicates the Command bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 1 - 1'b1 indicates the write bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 2 - 1'b1 indicates the write status bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 3 - 1'b1 indicates the read bus is implemented to this target/initiator else it is set to 1'b0.<br>Bit 4 - 1'b0 indicates the port follows the VBUS protocol else it is set to 1'b1.<br>Bits 5-7 are set to 3'b000. |
| 15:9  | RESERVED                                | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8     | MSS_CR5B1_AHB_BUS_SAFETY_CTRL_ERR_CLEAR | R/W  | 0h    | Set this bit to 1'b1 to clear the error status for this port                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |



**Table 2-1364. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_CTRL Register Field Descriptions  
(continued)**

| Bit | Field                                | Type | Reset | Description                                                                                                                                           |
|-----|--------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:3 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                                              |
| 2:0 | MSS_CR5B1_AHB_BUS_SAFETY_CTRL_ENABLE | R/W  | 7h    | Set this bit to 3'b111 to enable the safety configuration for this port.<br>Set this bit to 3'b000 to disable the safety configuration for this port. |

### 2.2.2.455 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_FI Register

#### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_FI Register (Offset = 187A4h) [reset = 0h]

This register is used to Inject fault on the Interconnect Safety comparator of R5SS1 CORE1 Peripheral Port.

Return to [Summary Table](#)

**Table 2-1365. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 87A4h       |

**Figure 2-455. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_FI Name Register**

| 31                               | 30                                      | 29                                      | 28                                                      | 27                                                      | 26                                                  | 25                                                  | 24  |
|----------------------------------|-----------------------------------------|-----------------------------------------|---------------------------------------------------------|---------------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|-----|
| MSS_CR5B1_AHB_BUS_SAFETY_FI_SAFE |                                         |                                         |                                                         |                                                         |                                                     |                                                     |     |
| R/W                              |                                         |                                         |                                                         |                                                         |                                                     |                                                     |     |
| 0h                               |                                         |                                         |                                                         |                                                         |                                                     |                                                     |     |
| 23                               | 22                                      | 21                                      | 20                                                      | 19                                                      | 18                                                  | 17                                                  | 16  |
| MSS_CR5B1_AHB_BUS_SAFETY_FI_MAIN |                                         |                                         |                                                         |                                                         |                                                     |                                                     |     |
| R/W                              |                                         |                                         |                                                         |                                                         |                                                     |                                                     |     |
| 0h                               |                                         |                                         |                                                         |                                                         |                                                     |                                                     |     |
| 15                               | 14                                      | 13                                      | 12                                                      | 11                                                      | 10                                                  | 9                                                   | 8   |
| MSS_CR5B1_AHB_BUS_SAFETY_FI_DATA |                                         |                                         |                                                         |                                                         |                                                     |                                                     |     |
| R/W                              |                                         |                                         |                                                         |                                                         |                                                     |                                                     |     |
| 0h                               |                                         |                                         |                                                         |                                                         |                                                     |                                                     |     |
| 7                                | 6                                       | 5                                       | 4                                                       | 3                                                       | 2                                                   | 1                                                   | 0   |
| RESERVED                         | MSS_CR5B1_A<br>HB_BUS_SAFE<br>TY_FI_DED | MSS_CR5B1_A<br>HB_BUS_SAFE<br>TY_FI_SEC | MSS_CR5B1_A<br>HB_BUS_SAFE<br>TY_FI_GLOBA<br>L_SAFE_REQ | MSS_CR5B1_A<br>HB_BUS_SAFE<br>TY_FI_GLOBA<br>L_MAIN_REQ | MSS_CR5B1_A<br>HB_BUS_SAFE<br>TY_FI_GLOBA<br>L_SAFE | MSS_CR5B1_A<br>HB_BUS_SAFE<br>TY_FI_GLOBA<br>L_MAIN |     |
| NONE                             | R/W                                     | R/W                                     | R/W                                                     | R/W                                                     | R/W                                                 | R/W                                                 | R/W |
| 0h                               | 0h                                      | 0h                                      | 0h                                                      | 0h                                                      | 0h                                                  | 0h                                                  | 0h  |

**Table 2-1367. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_FI Register Field Descriptions**

| Bit   | Field                            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|----------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5B1_AHB_BUS_SAFETY_FI_SAFE | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the safe Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 23:16 | MSS_CR5B1_AHB_BUS_SAFETY_FI_MAIN | R/W  | 0h    | This bitfield is used to inject fault on Read, write, command and request bus on the main Interconnect.<br>Bit 0 - Set this bit to inject fault on the Command bus.<br>Bit 1 - Set this bit to inject fault on the Write bus.<br>Bit 2 - Set this bit to inject fault on the Write Status bus.<br>Bit 3 - Set this bit to inject fault on the Read bus.<br>Bit 7 - Set this bit to inject fault on the corresponding request bus. |
| 15:8  | MSS_CR5B1_AHB_BUS_SAFETY_FI_DATA | R/W  | 0h    | Set bit 0 to 1'b1 to inject sec and ded faults on [31:0] bits of data bus.<br>Set bit 1 to 1'b1 to inject sec and ded faults on [64:32] bits of data bus.                                                                                                                                                                                                                                                                         |
| 7:6   | RESERVED                         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 5     | MSS_CR5B1_AHB_BUS_SAFETY_FI_DED  | R/W  | 0h    | Set this bit to 1'b1 inject ded error on data at this port                                                                                                                                                                                                                                                                                                                                                                        |

**Table 2-1367. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_FI Register Field Descriptions  
(continued)**

| Bit | Field                                       | Type | Reset | Description                                                                                                                                                                                                                                            |
|-----|---------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | MSS_CR5B1_AHB_BUS_SAFETY_FI_SEC             | R/W  | 0h    | Set this bit to 1'b1 to inject sec error on data at this port                                                                                                                                                                                          |
| 3   | MSS_CR5B1_AHB_BUS_SAFETY_FI_GLOBAL_SAFE_REQ | R/W  | 0h    | Set this bit 1'b1 to inject fault for request signals on Safe Interconnect. This is enabled only when the 7th bit of safe bitfield of this register and particular bit coressponding to this port on the safe bitfield of this register is set HIGH    |
| 2   | MSS_CR5B1_AHB_BUS_SAFETY_FI_GLOBAL_MAIN_REQ | R/W  | 0h    | Set this bit to 1'b1 to inject fault for request signals on main Interconnect. This is enabled only when the 7th bit of main bitfield of this register and particular bit coressponding to this port on the main bitfield of this register is set HIGH |
| 1   | MSS_CR5B1_AHB_BUS_SAFETY_FI_GLOBAL_SAFE     | R/W  | 0h    | This is a global safe Fault injection signal. Set this bit to inject fault on all the safety buses of the safe interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                           |
| 0   | MSS_CR5B1_AHB_BUS_SAFETY_FI_GLOBAL_MAIN     | R/W  | 0h    | This is a global main Fault injection signal. Set this bit to inject fault on all the buses of the main interconnect except req signal. Writing a 1'b1 injects fault on interconnect.                                                                  |

## 2.2.2.456 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_ERR Register

### 1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_ERR Register (Offset = 187A8h) [reset = 0h]

This Register provides the Error Status of Bus Safety Comparator of R5SS1 CORE1 Peripheral Port.

Return to [Summary Table](#)

**Table 2-1368. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 87A8h       |

**Figure 2-456. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_ERR Name Register**

|                                         |    |    |    |    |    |    |    |
|-----------------------------------------|----|----|----|----|----|----|----|
| 31                                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B1_AHB_BUS_SAFETY_ERR_DED        |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 23                                      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B1_AHB_BUS_SAFETY_ERR_SEC        |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 15                                      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B1_AHB_BUS_SAFETY_ERR_COMP_CHECK |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |
| 7                                       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B1_AHB_BUS_SAFETY_ERR_COMP_ERR   |    |    |    |    |    |    |    |
| R                                       |    |    |    |    |    |    |    |
| 0h                                      |    |    |    |    |    |    |    |

**Table 2-1370. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_ERR Register Field Descriptions**

| Bit   | Field                                   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|-----------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | MSS_CR5B1_AHB_BUS_SAFETY_ERR_DED        | R    | 0h    | This flag signals detection of dual error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates ded on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates ded on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                   |
| 23:16 | MSS_CR5B1_AHB_BUS_SAFETY_ERR_SEC        | R    | 0h    | This flag signals detection of single error in Data at this port. Flag is generated for 32 bit segment of Data Bus<br>Bit 0 - 1'b1 indicates sec on [31:0] bit of Data bus<br>Bit 1 - 1'b1 indicates sec on [63:32] bit of Data bus<br>Bit [7:2] - Unused. Set to 1'b0                                                                                                                                                                                                                                                 |
| 15:8  | MSS_CR5B1_AHB_BUS_SAFETY_ERR_COMP_CHECK | R    | 0h    | This is used to verify the proper functioning of fault Injection on all the buses. 1'b1 indicates error in the corresponding Bus has been injected successfully.<br>Bit 0 - This is a Bitwise AND of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise AND of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise AND of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise AND of error compares of all read bus signals.<br>Bits [7:4] are unused. |

**Table 2-1370. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_ERR Register Field Descriptions  
(continued)**

| Bit | Field                                 | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|---------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | MSS_CR5B1_AHB_BUS_SAFETY_ERR_COMP_ERR | R    | 0h    | 1'b1 indicates error in the corresponding Bus whenever a fault is detected at any bus signal<br>Bit 0 - This is a Bitwise OR of error compares of all command bus signals.<br>Bit 1 - This is a Bitwise OR of error compares of all write bus signals.<br>Bit 2 - This is a Bitwise OR of error compares of all write status bus signals.<br>Bit 3 - This is a Bitwise OR of error compares of all read bus signals.<br>Bits [7:4] are unused. |

### 2.2.2.457 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register

**1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register (Offset = 187ACh)**  
[reset = 0h]

MSS\_CR5B\_AHB\_BUS\_SAFETY\_ERR\_STAT\_DATA0.

Return to [Summary Table](#)

**Table 2-1371. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 87ACh       |

**Figure 2-457. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Name Register**

|                                            |    |    |    |    |    |    |    |
|--------------------------------------------|----|----|----|----|----|----|----|
| 31                                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                                   |    |    |    |    |    |    |    |
| NONE                                       |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 23                                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                                   |    |    |    |    |    |    |    |
| NONE                                       |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 15                                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B1_AHB_BUS_SAFETY_ERR_STAT_DATA0_D1 |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 7                                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B1_AHB_BUS_SAFETY_ERR_STAT_DATA0_D0 |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |

**Table 2-1373. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_DATA0 Register Field Descriptions**

| Bit   | Field                                      | Type | Reset | Description                                                                                                                                                |
|-------|--------------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                                   | NONE | 0h    | Reserved                                                                                                                                                   |
| 15:8  | MSS_CR5B1_AHB_BUS_SAFETY_ERR_STAT_DATA0_D1 | R    | 0h    | Read this bitfield for Comparator status for Higher 32 bits [63:32] of data bus at this port. It represent the position of the flipped bit in case of SEC. |
| 7:0   | MSS_CR5B1_AHB_BUS_SAFETY_ERR_STAT_DATA0_D0 | R    | 0h    | Read this bitfield for Comparator status for lower 32 bits [31:0] of data bus at this port. It represent the position of the flipped bit in case of SEC.   |

### 2.2.2.458 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_CMD Register

**1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_CMD Register (Offset = 187B0h)**  
[reset = 0h]

MSS\_CR5B1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_CMD.

Return to [Summary Table](#)

**Table 2-1374. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 87B0h       |

**Figure 2-458. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_CMD Name Register**

|                                            |    |    |    |    |    |    |    |
|--------------------------------------------|----|----|----|----|----|----|----|
| 31                                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B1_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 23                                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B1_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 15                                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B1_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |
| 7                                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B1_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT |    |    |    |    |    |    |    |
| R                                          |    |    |    |    |    |    |    |
| 0h                                         |    |    |    |    |    |    |    |

**Table 2-1376. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_CMD Register Field Descriptions**

| Bit  | Field                                      | Type | Reset | Description                                                                                                                       |
|------|--------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5B1_AHB_BUS_SAFETY_ERR_STAT_CMD_STAT | R    | 0h    | Read this bitfield for comparator status for command bus for this port. 1'b1 on any of the bits indicates an error on Command Bus |

### 2.2.2.459 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register

**1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register (Offset = 187B4h)**  
[reset = 0h]

MSS\_CR5B\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITE.

Return to [Summary Table](#)

**Table 2-1377. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 87B4h       |

**Figure 2-459. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITE Name Register**

|                                              |    |    |    |    |    |    |    |
|----------------------------------------------|----|----|----|----|----|----|----|
| 31                                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B1_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 23                                           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B1_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 15                                           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B1_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |
| 7                                            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B1_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT |    |    |    |    |    |    |    |
| R                                            |    |    |    |    |    |    |    |
| 0h                                           |    |    |    |    |    |    |    |

**Table 2-1379. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITE Register Field Descriptions**

| Bit  | Field                                        | Type | Reset | Description                                                                                                        |
|------|----------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5B1_AHB_BUS_SAFETY_ERR_STAT_WRITE_STAT | R    | 0h    | Read this bitfield for comparator status for Write bus for this port. 1'b1 at any bit indicates error on Write Bus |



### 2.2.2.460 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_READ Register

**1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_READ Register (Offset = 187B8h)**  
[reset = 0h]

MSS\_CR5B\_AHB\_BUS\_SAFETY\_ERR\_STAT\_READ.

Return to [Summary Table](#)

**Table 2-1380. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 87B8h       |

**Figure 2-460. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_READ Name Register**

|                                             |    |    |    |    |    |    |    |
|---------------------------------------------|----|----|----|----|----|----|----|
| 31                                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B1_AHB_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 23                                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B1_AHB_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 15                                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B1_AHB_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |
| 7                                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B1_AHB_BUS_SAFETY_ERR_STAT_READ_STAT |    |    |    |    |    |    |    |
| R                                           |    |    |    |    |    |    |    |
| 0h                                          |    |    |    |    |    |    |    |

**Table 2-1382. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_READ Register Field Descriptions**

| Bit  | Field                                       | Type | Reset | Description                                                                                                                     |
|------|---------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5B1_AHB_BUS_SAFETY_ERR_STAT_READ_STAT | R    | 0h    | Read this bitfield for comapartor status for read signals at this port. 1'b1 on any of the bits indicates an error on Read bus. |

### 2.2.2.461 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register

**1 MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register (Offset = 187BCh) [reset = 0h]**

MSS\_CR5B\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP.

Return to [Summary Table](#)

**Table 2-1383. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_CTRL      | 50D1 87BCh       |

**Figure 2-461. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Name Register**

|                                                  |    |    |    |    |    |    |    |
|--------------------------------------------------|----|----|----|----|----|----|----|
| 31                                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSS_CR5B1_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                |    |    |    |    |    |    |    |
| 0h                                               |    |    |    |    |    |    |    |
| 23                                               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_CR5B1_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                |    |    |    |    |    |    |    |
| 0h                                               |    |    |    |    |    |    |    |
| 15                                               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CR5B1_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                |    |    |    |    |    |    |    |
| 0h                                               |    |    |    |    |    |    |    |
| 7                                                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CR5B1_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT |    |    |    |    |    |    |    |
| R                                                |    |    |    |    |    |    |    |
| 0h                                               |    |    |    |    |    |    |    |

**Table 2-1385. MSS\_CTRL\_MSS\_R5FSS1\_CORE1\_AHB\_BUS\_SAFETY\_ERR\_STAT\_WRITERESP Register Field Descriptions**

| Bit  | Field                                            | Type | Reset | Description                                                                                                                           |
|------|--------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSS_CR5B1_AHB_BUS_SAFETY_ERR_STAT_WRITERESP_STAT | R    | 0h    | Read this bitfield for comparator status for Write response bus for this port. 1'b1 at any bit indicates error on Write Response Bus. |

## 2.3 TOP\_CTRL

### TOP\_CTRL

#### 2.3.1 TOP\_CTRL Summaries

#### TOP\_CTRL Summaries

**Table 2-1386. TOP\_CTRL Registers, Base Address=50D8 0000h, Length=4096**

| Offset | Length | Register Name                                   | TOP_CTRL Physical Address |
|--------|--------|-------------------------------------------------|---------------------------|
| 10h    | 32     | <a href="#">TOP_CTRL_EFUSE_DIEID0</a>           | 50D8 0010h                |
| 14h    | 32     | <a href="#">TOP_CTRL_EFUSE_DIEID1</a>           | 50D8 0014h                |
| 18h    | 32     | <a href="#">TOP_CTRL_EFUSE_DIEID2</a>           | 50D8 0018h                |
| 1Ch    | 32     | <a href="#">TOP_CTRL_EFUSE_DIEID3</a>           | 50D8 001Ch                |
| 20h    | 32     | <a href="#">TOP_CTRL_EFUSE_UID0</a>             | 50D8 0020h                |
| 24h    | 32     | <a href="#">TOP_CTRL_EFUSE_UID1</a>             | 50D8 0024h                |
| 28h    | 32     | <a href="#">TOP_CTRL_EFUSE_UID2</a>             | 50D8 0028h                |
| 2Ch    | 32     | <a href="#">TOP_CTRL_EFUSE_UID3</a>             | 50D8 002Ch                |
| 30h    | 32     | <a href="#">TOP_CTRL_EFUSE_DEVICE_TYPE</a>      | 50D8 0030h                |
| 34h    | 32     | <a href="#">TOP_CTRL_EFUSE_FROM0_CHECKSUM</a>   | 50D8 0034h                |
| 38h    | 32     | <a href="#">TOP_CTRL_EFUSE_JTAG_USERCODE_ID</a> | 50D8 0038h                |
| 428h   | 32     | <a href="#">TOP_CTRL_EFUSE1_ROW_12</a>          | 50D8 0428h                |
| 434h   | 32     | <a href="#">TOP_CTRL_EFUSE1_ROW_15</a>          | 50D8 0434h                |
| 500h   | 32     | <a href="#">TOP_CTRL_MAC_ID0</a>                | 50D8 0500h                |
| 504h   | 32     | <a href="#">TOP_CTRL_MAC_ID1</a>                | 50D8 0504h                |
| C00h   | 32     | <a href="#">TOP_CTRL_ADC_REFBUF0_CTRL</a>       | 50D8 0C00h                |
| C04h   | 32     | <a href="#">TOP_CTRL_ADC_REFBUF1_CTRL</a>       | 50D8 0C04h                |
| C08h   | 32     | <a href="#">TOP_CTRL_ADC_REF_COMP_CTRL</a>      | 50D8 0C08h                |
| C0Ch   | 32     | <a href="#">TOP_CTRL_ADC_REF_GOOD_STATUS</a>    | 50D8 0C0Ch                |
| C10h   | 32     | <a href="#">TOP_CTRL_VMON_CTRL</a>              | 50D8 0C10h                |
| C14h   | 32     | <a href="#">TOP_CTRL_VMON_STAT</a>              | 50D8 0C14h                |
| C18h   | 32     | <a href="#">TOP_CTRL_PMU_COARSE_STAT</a>        | 50D8 0C18h                |
| C20h   | 32     | <a href="#">TOP_CTRL_MASK_VMON_ERROR_ESM_H</a>  | 50D8 0C20h                |
| C24h   | 32     | <a href="#">TOP_CTRL_MASK_VMON_ERROR_ESM_L</a>  | 50D8 0C24h                |
| C34h   | 32     | <a href="#">TOP_CTRL_VMON_FILTER_CTRL</a>       | 50D8 0C34h                |
| D00h   | 32     | <a href="#">TOP_CTRL_TSENSE_CFG</a>             | 50D8 0D00h                |
| D04h   | 32     | <a href="#">TOP_CTRL_TSENSE_STATUS</a>          | 50D8 0D04h                |
| D08h   | 32     | <a href="#">TOP_CTRL_TSENSE_STATUS_RAW</a>      | 50D8 0D08h                |
| D14h   | 32     | <a href="#">TOP_CTRL_TSENSE0_ALERT</a>          | 50D8 0D14h                |
| D18h   | 32     | <a href="#">TOP_CTRL_TSENSE0_CNTL</a>           | 50D8 0D18h                |
| D1Ch   | 32     | <a href="#">TOP_CTRL_TSENSE0_RESULT</a>         | 50D8 0D1Ch                |
| D20h   | 32     | <a href="#">TOP_CTRL_TSENSE0_DATA0</a>          | 50D8 0D20h                |
| D24h   | 32     | <a href="#">TOP_CTRL_TSENSE0_DATA1</a>          | 50D8 0D24h                |
| D28h   | 32     | <a href="#">TOP_CTRL_TSENSE0_DATA2</a>          | 50D8 0D28h                |
| D2Ch   | 32     | <a href="#">TOP_CTRL_TSENSE0_DATA3</a>          | 50D8 0D2Ch                |
| D30h   | 32     | <a href="#">TOP_CTRL_TSENSE0_ACCU</a>           | 50D8 0D30h                |
| D40h   | 32     | <a href="#">TOP_CTRL_TSENSE1_TSHUT</a>          | 50D8 0D40h                |
| D44h   | 32     | <a href="#">TOP_CTRL_TSENSE1_ALERT</a>          | 50D8 0D44h                |

**Table 2-1386. TOP\_CTRL Registers, Base Address=50D8 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                                      | TOP_CTRL Physical Address |
|--------|--------|----------------------------------------------------|---------------------------|
| D48h   | 32     | <a href="#">TOP_CTRL_TSENSE1_CNTL</a>              | 50D8 0D48h                |
| D4Ch   | 32     | <a href="#">TOP_CTRL_TSENSE1_RESULT</a>            | 50D8 0D4Ch                |
| D50h   | 32     | <a href="#">TOP_CTRL_TSENSE1_DATA0</a>             | 50D8 0D50h                |
| D54h   | 32     | <a href="#">TOP_CTRL_TSENSE1_DATA1</a>             | 50D8 0D54h                |
| D58h   | 32     | <a href="#">TOP_CTRL_TSENSE1_DATA2</a>             | 50D8 0D58h                |
| D5Ch   | 32     | <a href="#">TOP_CTRL_TSENSE1_DATA3</a>             | 50D8 0D5Ch                |
| D60h   | 32     | <a href="#">TOP_CTRL_TSENSE1_ACCU</a>              | 50D8 0D60h                |
| D7Ch   | 32     | <a href="#">TOP_CTRL_TSENSE2_RESULT</a>            | 50D8 0D7Ch                |
| DACH   | 32     | <a href="#">TOP_CTRL_TSENSE3_RESULT</a>            | 50D8 0DACH                |
| FD0h   | 32     | <a href="#">TOP_CTRL_HW_SPARE_RW0</a>              | 50D8 0FD0h                |
| FD4h   | 32     | <a href="#">TOP_CTRL_HW_SPARE_RW1</a>              | 50D8 0FD4h                |
| FD8h   | 32     | <a href="#">TOP_CTRL_HW_SPARE_RW2</a>              | 50D8 0FD8h                |
| FDCh   | 32     | <a href="#">TOP_CTRL_HW_SPARE_RW3</a>              | 50D8 0FDCh                |
| FE0h   | 32     | <a href="#">TOP_CTRL_HW_SPARE_RO0</a>              | 50D8 0FE0h                |
| FE4h   | 32     | <a href="#">TOP_CTRL_HW_SPARE_RO1</a>              | 50D8 0FE4h                |
| FE8h   | 32     | <a href="#">TOP_CTRL_HW_SPARE_RO2</a>              | 50D8 0FE8h                |
| FECh   | 32     | <a href="#">TOP_CTRL_HW_SPARE_RO3</a>              | 50D8 0FECh                |
| FF0h   | 32     | <a href="#">TOP_CTRL_HW_SPARE_WPH</a>              | 50D8 0FF0h                |
| FF4h   | 32     | <a href="#">TOP_CTRL_HW_SPARE_REC</a>              | 50D8 0FF4h                |
| 1008h  | 32     | <a href="#">TOP_CTRL_LOCK0_KICK0</a>               | 50D8 1008h                |
| 100Ch  | 32     | <a href="#">TOP_CTRL_LOCK0_KICK1</a>               | 50D8 100Ch                |
| 1010h  | 32     | <a href="#">TOP_CTRL_INTR_RAW_STATUS</a>           | 50D8 1010h                |
| 1014h  | 32     | <a href="#">TOP_CTRL_INTR_ENABLED_STATUS_CLEAR</a> | 50D8 1014h                |
| 1018h  | 32     | <a href="#">TOP_CTRL_INTR_ENABLE</a>               | 50D8 1018h                |
| 101Ch  | 32     | <a href="#">TOP_CTRL_INTR_ENABLE_CLEAR</a>         | 50D8 101Ch                |
| 1020h  | 32     | <a href="#">TOP_CTRL_EOI</a>                       | 50D8 1020h                |
| 1024h  | 32     | <a href="#">TOP_CTRL_FAULT_ADDRESS</a>             | 50D8 1024h                |
| 1028h  | 32     | <a href="#">TOP_CTRL_FAULT_TYPE_STATUS</a>         | 50D8 1028h                |
| 102Ch  | 32     | <a href="#">TOP_CTRL_FAULT_ATTR_STATUS</a>         | 50D8 102Ch                |
| 1030h  | 32     | <a href="#">TOP_CTRL_FAULT_CLEAR</a>               | 50D8 1030h                |

### 2.3.2 TOP\_CTRL Registers

#### TOP\_CTRL Registers

### 2.3.2.1 TOP\_CTRL\_EFUSE\_DIEID0 Register

#### 1 TOP\_CTRL\_EFUSE\_DIEID0 Register (Offset = 10h) [reset = 0h]

Register to read DIEID0.

Return to [Summary Table](#)

**Table 2-1387. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0010h       |

**Figure 2-462. TOP\_CTRL\_EFUSE\_DIEID0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| EFUSE_DIEID0_VAL |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| EFUSE_DIEID0_VAL |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| EFUSE_DIEID0_VAL |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| EFUSE_DIEID0_VAL |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 2-1389. TOP\_CTRL\_EFUSE\_DIEID0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description       |
|------|------------------|------|-------|-------------------|
| 31:0 | EFUSE_DIEID0_VAL | R    | 0h    | EFUSE DieID[31:0] |

### 2.3.2.2 TOP\_CTRL\_EFUSE\_DIEID1 Register

#### 1 TOP\_CTRL\_EFUSE\_DIEID1 Register (Offset = 14h) [reset = 0h]

Register to read DIEID1.

Return to [Summary Table](#)

**Table 2-1390. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0014h       |

**Figure 2-463. TOP\_CTRL\_EFUSE\_DIEID1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| EFUSE_DIEID1_VAL |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| EFUSE_DIEID1_VAL |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| EFUSE_DIEID1_VAL |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| EFUSE_DIEID1_VAL |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 2-1392. TOP\_CTRL\_EFUSE\_DIEID1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description        |
|------|------------------|------|-------|--------------------|
| 31:0 | EFUSE_DIEID1_VAL | R    | 0h    | EFUSE DieID[63:32] |

### 2.3.2.3 TOP\_CTRL\_EFUSE\_DIEID2 Register

#### 1 TOP\_CTRL\_EFUSE\_DIEID2 Register (Offset = 18h) [reset = 0h]

Register to read DIEID2.

Return to [Summary Table](#)

**Table 2-1393. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0018h       |

**Figure 2-464. TOP\_CTRL\_EFUSE\_DIEID2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| EFUSE_DIEID2_VAL |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| EFUSE_DIEID2_VAL |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| EFUSE_DIEID2_VAL |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| EFUSE_DIEID2_VAL |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 2-1395. TOP\_CTRL\_EFUSE\_DIEID2 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description        |
|------|------------------|------|-------|--------------------|
| 31:0 | EFUSE_DIEID2_VAL | R    | 0h    | EFUSE DieID[95:64] |

### 2.3.2.4 TOP\_CTRL\_EFUSE\_DIEID3 Register

#### 1 TOP\_CTRL\_EFUSE\_DIEID3 Register (Offset = 1Ch) [reset = 0h]

Register to read DIEID3.

Return to [Summary Table](#)

**Table 2-1396. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 001Ch       |

**Figure 2-465. TOP\_CTRL\_EFUSE\_DIEID3 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| EFUSE_DIEID3_VAL |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| EFUSE_DIEID3_VAL |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| EFUSE_DIEID3_VAL |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| EFUSE_DIEID3_VAL |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 2-1398. TOP\_CTRL\_EFUSE\_DIEID3 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description         |
|------|------------------|------|-------|---------------------|
| 31:0 | EFUSE_DIEID3_VAL | R    | 0h    | EFUSE DieID[127:96] |



### 2.3.2.5 TOP\_CTRL\_EFUSE\_UID0 Register

#### 1 TOP\_CTRL\_EFUSE\_UID0 Register (Offset = 20h) [reset = 0h]

Register to read UID0.

Return to [Summary Table](#)

**Table 2-1399. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0020h       |

**Figure 2-466. TOP\_CTRL\_EFUSE\_UID0 Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| EFUSE_UID0_VAL |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| EFUSE_UID0_VAL |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| EFUSE_UID0_VAL |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| EFUSE_UID0_VAL |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 2-1401. TOP\_CTRL\_EFUSE\_UID0 Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description     |
|------|----------------|------|-------|-----------------|
| 31:0 | EFUSE_UID0_VAL | R    | 0h    | EFUSE UID[31:0] |

### 2.3.2.6 TOP\_CTRL\_EFUSE\_UID1 Register

#### 1 TOP\_CTRL\_EFUSE\_UID1 Register (Offset = 24h) [reset = 0h]

Register to read UID1.

Return to [Summary Table](#)

**Table 2-1402. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0024h       |

**Figure 2-467. TOP\_CTRL\_EFUSE\_UID1 Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| EFUSE_UID1_VAL |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| EFUSE_UID1_VAL |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| EFUSE_UID1_VAL |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| EFUSE_UID1_VAL |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 2-1404. TOP\_CTRL\_EFUSE\_UID1 Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description      |
|------|----------------|------|-------|------------------|
| 31:0 | EFUSE_UID1_VAL | R    | 0h    | EFUSE UID[63:32] |

### 2.3.2.7 TOP\_CTRL\_EFUSE\_UID2 Register

#### 1 TOP\_CTRL\_EFUSE\_UID2 Register (Offset = 28h) [reset = 0h]

Register to read UID2.

Return to [Summary Table](#)

**Table 2-1405. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0028h       |

**Figure 2-468. TOP\_CTRL\_EFUSE\_UID2 Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| EFUSE_UID2_VAL |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| EFUSE_UID2_VAL |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| EFUSE_UID2_VAL |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| EFUSE_UID2_VAL |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 2-1407. TOP\_CTRL\_EFUSE\_UID2 Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description      |
|------|----------------|------|-------|------------------|
| 31:0 | EFUSE_UID2_VAL | R    | 0h    | EFUSE UID[95:64] |

### 2.3.2.8 TOP\_CTRL\_EFUSE\_UID3 Register

#### 1 TOP\_CTRL\_EFUSE\_UID3 Register (Offset = 2Ch) [reset = 0h]

Register to read UID3.

Return to [Summary Table](#)

**Table 2-1408. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 002Ch       |

**Figure 2-469. TOP\_CTRL\_EFUSE\_UID3 Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| EFUSE_UID3_VAL |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| EFUSE_UID3_VAL |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| EFUSE_UID3_VAL |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 2-1410. TOP\_CTRL\_EFUSE\_UID3 Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description       |
|-------|----------------|------|-------|-------------------|
| 31:24 | RESERVED       | NONE | 0h    | Reserved          |
| 23:0  | EFUSE_UID3_VAL | R    | 0h    | EFUSE UID[120:96] |

### 2.3.2.9 TOP\_CTRL\_EFUSE\_DEVICE\_TYPE Register

#### 1 TOP\_CTRL\_EFUSE\_DEVICE\_TYPE Register (Offset = 30h) [reset = 0h]

This register indicates Device Type-  
High Secure : 0b 1100 1100 (0xA).

Return to [Summary Table](#)

**Table 2-1411. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0030h       |

**Figure 2-470. TOP\_CTRL\_EFUSE\_DEVICE\_TYPE Name Register**

|                       |    |    |    |    |    |    |    |
|-----------------------|----|----|----|----|----|----|----|
| 31                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED              |    |    |    |    |    |    |    |
| NONE                  |    |    |    |    |    |    |    |
| 0h                    |    |    |    |    |    |    |    |
| 23                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED              |    |    |    |    |    |    |    |
| NONE                  |    |    |    |    |    |    |    |
| 0h                    |    |    |    |    |    |    |    |
| 15                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| EFUSE_DEVICE_TYPE_VAL |    |    |    |    |    |    |    |
| R                     |    |    |    |    |    |    |    |
| 0h                    |    |    |    |    |    |    |    |
| 7                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| EFUSE_DEVICE_TYPE_VAL |    |    |    |    |    |    |    |
| R                     |    |    |    |    |    |    |    |
| 0h                    |    |    |    |    |    |    |    |

**Table 2-1413. TOP\_CTRL\_EFUSE\_DEVICE\_TYPE Register Field Descriptions**

| Bit   | Field                 | Type | Reset | Description       |
|-------|-----------------------|------|-------|-------------------|
| 31:16 | RESERVED              | NONE | 0h    | Reserved          |
| 15:0  | EFUSE_DEVICE_TYPE_VAL | R    | 0h    | EFUSE Device Type |

### 2.3.2.10 TOP\_CTRL\_EFUSE\_FROM0\_CHECKSUM Register

#### 1 TOP\_CTRL\_EFUSE\_FROM0\_CHECKSUM Register (Offset = 34h) [reset = 0h]

The register provides checksum for efuse FROM0.

Return to [Summary Table](#)

**Table 2-1414. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0034h       |

**Figure 2-471. TOP\_CTRL\_EFUSE\_FROM0\_CHECKSUM Name Register**

|                          |    |    |    |    |    |    |    |
|--------------------------|----|----|----|----|----|----|----|
| 31                       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| EFUSE_FROM0_CHECKSUM_VAL |    |    |    |    |    |    |    |
| R                        |    |    |    |    |    |    |    |
| 0h                       |    |    |    |    |    |    |    |
| 23                       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| EFUSE_FROM0_CHECKSUM_VAL |    |    |    |    |    |    |    |
| R                        |    |    |    |    |    |    |    |
| 0h                       |    |    |    |    |    |    |    |
| 15                       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| EFUSE_FROM0_CHECKSUM_VAL |    |    |    |    |    |    |    |
| R                        |    |    |    |    |    |    |    |
| 0h                       |    |    |    |    |    |    |    |
| 7                        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| EFUSE_FROM0_CHECKSUM_VAL |    |    |    |    |    |    |    |
| R                        |    |    |    |    |    |    |    |
| 0h                       |    |    |    |    |    |    |    |

**Table 2-1416. TOP\_CTRL\_EFUSE\_FROM0\_CHECKSUM Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description           |
|------|--------------------------|------|-------|-----------------------|
| 31:0 | EFUSE_FROM0_CHECKSUM_VAL | R    | 0h    | 32 bit FROM0 Checksum |

### 2.3.2.11 TOP\_CTRL\_EFUSE\_JTAG\_USERCODE\_ID Register

#### 1 TOP\_CTRL\_EFUSE\_JTAG\_USERCODE\_ID Register (Offset = 38h) [reset = 0h]

Register to read JTAG user IDCODE.

Return to [Summary Table](#)

**Table 2-1417. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0038h       |

**Figure 2-472. TOP\_CTRL\_EFUSE\_JTAG\_USERCODE\_ID Name Register**

|                            |    |    |    |    |    |    |    |
|----------------------------|----|----|----|----|----|----|----|
| 31                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| EFUSE_JTAG_USERCODE_ID_VAL |    |    |    |    |    |    |    |
| R                          |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |
| 23                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| EFUSE_JTAG_USERCODE_ID_VAL |    |    |    |    |    |    |    |
| R                          |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |
| 15                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| EFUSE_JTAG_USERCODE_ID_VAL |    |    |    |    |    |    |    |
| R                          |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |
| 7                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| EFUSE_JTAG_USERCODE_ID_VAL |    |    |    |    |    |    |    |
| R                          |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |

**Table 2-1419. TOP\_CTRL\_EFUSE\_JTAG\_USERCODE\_ID Register Field Descriptions**

| Bit  | Field                      | Type | Reset | Description                                          |
|------|----------------------------|------|-------|------------------------------------------------------|
| 31:0 | EFUSE_JTAG_USERCODE_ID_VAL | R    | 0h    | EFUSE JTAG_USER_CODE_ID[31:0];. Denotes part variant |

### 2.3.2.12 TOP\_CTRL\_EFUSE1\_ROW\_12 Register

#### 1 TOP\_CTRL\_EFUSE1\_ROW\_12 Register (Offset = 428h) [reset = 0h]

This register provides details on EFUSE values written into Row 12.

Return to [Summary Table](#)

**Table 2-1420. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0428h       |

**Figure 2-473. TOP\_CTRL\_EFUSE1\_ROW\_12 Name Register**

| 31                                        | 30                                      | 29                                        | 28                                      | 27                             | 26                                        | 25                                    | 24                                     |
|-------------------------------------------|-----------------------------------------|-------------------------------------------|-----------------------------------------|--------------------------------|-------------------------------------------|---------------------------------------|----------------------------------------|
| RESERVED                                  |                                         |                                           |                                         |                                |                                           | EFUSE1_ROW_12_CUSTOME<br>R_IP_DISABLE | EFUSE1_ROW_12_EPWM_FE<br>ATURE_DISABLE |
| NONE                                      |                                         |                                           |                                         |                                |                                           | R                                     | R                                      |
| 0h                                        |                                         |                                           |                                         |                                |                                           | 0h                                    | 0h                                     |
| 23                                        | 22                                      | 21                                        | 20                                      | 19                             | 18                                        | 17                                    | 16                                     |
| EFUSE1_ROW_12_CANFD_DIS                   |                                         |                                           |                                         | EFUSE1_ROW_12_PRU_ICSS_HW_DIS  |                                           |                                       |                                        |
| R                                         |                                         |                                           |                                         | R                              |                                           |                                       |                                        |
| 0h                                        |                                         |                                           |                                         | 0h                             |                                           |                                       |                                        |
| 15                                        | 14                                      | 13                                        | 12                                      | 11                             | 10                                        | 9                                     | 8                                      |
| EFUSE1_ROW_12_PRU_ICSS_HW_DIS             |                                         |                                           |                                         | EFUSE1_ROW_12_PRU_ICSS<br>_DIS | EFUSE1_ROW_12_TWOW_CT<br>RL_PERIP_DISABLE | EFUSE1_ROW_12_R5SS_FR<br>EQ           | EFUSE1_ROW_12_R5SS1_DI<br>SABLE        |
| R                                         |                                         |                                           |                                         | R                              | R                                         | R                                     | R                                      |
| 0h                                        |                                         |                                           |                                         | 0h                             | 0h                                        | 0h                                    | 0h                                     |
| 7                                         | 6                                       | 5                                         | 4                                       | 3                              | 2                                         | 1                                     | 0                                      |
| EFUSE1_ROW_12_R5SS1_D<br>UAL_CORE_DISABLE | EFUSE1_ROW_12_R5SS1_F<br>ORCE_DUAL_CORE | EFUSE1_ROW_12_R5SS0_D<br>UAL_CORE_DISABLE | EFUSE1_ROW_12_R5SS0_F<br>ORCE_DUAL_CORE | EFUSE1_ROW_12_L2_MEM_SIZE      |                                           |                                       |                                        |
| R                                         | R                                       | R                                         | R                                       | R                              |                                           |                                       |                                        |
| 0h                                        | 0h                                      | 0h                                        | 0h                                      | 0h                             |                                           |                                       |                                        |

**Table 2-1422. TOP\_CTRL\_EFUSE1\_ROW\_12 Register Field Descriptions**

| Bit   | Field                                  | Type | Reset | Description                                                                                                               |
|-------|----------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------|
| 31:26 | RESERVED                               | NONE | 0h    | Reserved                                                                                                                  |
| 25    | EFUSE1_ROW_12_CUST<br>OMER_IP_DISABLE  | R    | 0h    | Customer IP set control<br>0 - All IPs enabled<br>1 - Customer IP set disabled [PWM24-31,CMPSSA6-9,CMPSSB6-9<br>disabled] |
| 24    | EFUSE1_ROW_12_EPW<br>M_FEATURE_DISABLE | R    | 0h    | Customer protected features inside PWM IP<br>0 - All features enabled<br>1 - Customer defined features are protected      |
| 23:20 | EFUSE1_ROW_12_CANF<br>D_DIS            | R    | 0h    | CANFD disables. Bit positions correspond to CAN instance.<br>0 - CAN is enabled<br>1 - CAN is disabled                    |
| 19:12 | EFUSE1_ROW_12_PRU_<br>ICSS_HW_DIS      | R    | 0h    | ICSSM IP feature configuration<br>0 - ICSSM feature enabled<br>1 - ICSSM feature disabled                                 |



**Table 2-1422. TOP\_CTRL\_EFUSE1\_ROW\_12 Register Field Descriptions (continued)**

| Bit | Field                                 | Type | Reset | Description                                                                                                          |
|-----|---------------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------|
| 11  | EFUSE1_ROW_12_PRU_ICSS_DIS            | R    | 0h    | ICSSM IP disable<br>0 - ICSSM enabled<br>1 - ICSSM disabled                                                          |
| 10  | EFUSE1_ROW_12_TWOX_CTRL_PERIP_DISABLE | R    | 0h    | 2x control IPs enabled<br>0 - 1x control IPs                                                                         |
| 9   | EFUSE1_ROW_12_R5SS_FREQ               | R    | 0h    | R5SS Freq<br>0 - 400 MHz<br>1 - 200 MHz                                                                              |
| 8   | EFUSE1_ROW_12_R5SS1_DISABLE           | R    | 0h    | Supports single R5SS0 cluster, disables R5SS1 cluster                                                                |
| 7   | EFUSE1_ROW_12_R5SS1_DUAL_CORE_DISABLE | R    | 0h    | Disabling switching to Dual Core mode by the application. Forced lockstep is forced dual core not enabled            |
| 6   | EFUSE1_ROW_12_R5SS1_FORCE_DUAL_CORE   | R    | 0h    | Enable MSS R5FSS1 dual core boot mode. Force Dual core                                                               |
| 5   | EFUSE1_ROW_12_R5SS0_DUAL_CORE_DISABLE | R    | 0h    | Disabling switching to Dual Core mode by the application. Forced lockstep is forced dual core not enabled            |
| 4   | EFUSE1_ROW_12_R5SS0_FORCE_DUAL_CORE   | R    | 0h    | Enable MSS R5FSS0 dual core boot mode. Force Dual core                                                               |
| 3:0 | EFUSE1_ROW_12_L2_MEM_SIZE             | R    | 0h    | Decides memory size<br>0000- L2- 2 MB<br>0001- L2- 1.5 MB<br>0010- L2- 1 MB<br>0011- L2- 0.5 MB<br>Others - Reserved |

### 2.3.2.13 TOP\_CTRL\_EFUSE1\_ROW\_15 Register

1 TOP\_CTRL\_EFUSE1\_ROW\_15 Register (Offset = 434h) [reset = 0h]

Return to [Summary Table](#)

**Table 2-1423. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0434h       |

**Figure 2-474. TOP\_CTRL\_EFUSE1\_ROW\_15 Name Register**

|                             |    |    |    |        |    |    |    |
|-----------------------------|----|----|----|--------|----|----|----|
| 31                          | 30 | 29 | 28 | 27     | 26 | 25 | 24 |
| EFUSE1_ROW_15_EFUSE1_ROW_15 |    |    |    |        |    |    |    |
| R                           |    |    |    |        |    |    |    |
| 0h                          |    |    |    |        |    |    |    |
| 23                          | 22 | 21 | 20 | 19     | 18 | 17 | 16 |
| EFUSE1_ROW_15_EFUSE1_ROW_15 |    |    |    |        |    |    |    |
| R                           |    |    |    |        |    |    |    |
| 0h                          |    |    |    |        |    |    |    |
| 15                          | 14 | 13 | 12 | 11     | 10 | 9  | 8  |
| EFUSE1_ROW_15_EFUSE1_ROW_15 |    |    |    |        |    |    |    |
| R                           |    |    |    |        |    |    |    |
| 0h                          |    |    |    |        |    |    |    |
| 7                           | 6  | 5  | 4  | 3      | 2  | 1  | 0  |
| EFUSE1_ROW_15_EFUSE1_ROW_15 |    |    |    | PG_VER |    |    |    |
| R                           |    |    |    | R      |    |    |    |
| 0h                          |    |    |    | 0h     |    |    |    |

**Table 2-1425. TOP\_CTRL\_EFUSE1\_ROW\_15 Register Field Descriptions**

| Bit  | Field                       | Type | Reset | Description                                                                                                                                                                                                                                           |
|------|-----------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | EFUSE1_ROW_15_EFUSE1_ROW_15 | R    | 0h    | Reserved                                                                                                                                                                                                                                              |
| 3:0  | PG_VER                      | R    | 0h    | The PG_version can be identified by reading these bits.<br>4'b0001 : Silicon Version 1.0(A).<br>4'b0010 : Silicon Version 1.0A (B).<br>4'b0011 : Silicon Version 1.1 (C).<br>4'b0100 : Silicon Version 1.2 (D).<br>4'b0101 : Silicon Version 1.3 (E). |

### 2.3.2.14 TOP\_CTRL\_MAC\_ID0 Register

#### 1 TOP\_CTRL\_MAC\_ID0 Register (Offset = 500h) [reset = 0h]

Ethernet MAC address lower 32-bits.

Return to [Summary Table](#)

**Table 2-1426. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0500h       |

**Figure 2-475. TOP\_CTRL\_MAC\_ID0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MAC_ID0_MACID_LO |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MAC_ID0_MACID_LO |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MAC_ID0_MACID_LO |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MAC_ID0_MACID_LO |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 2-1428. TOP\_CTRL\_MAC\_ID0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------|
| 31:0 | MAC_ID0_MACID_LO | R    | 0h    | 48-bit Ethernet MAC_ID field. Can be used by SW through MMR read - MAC ID low [32bits] |

### 2.3.2.15 TOP\_CTRL\_MAC\_ID1 Register

#### 1 TOP\_CTRL\_MAC\_ID1 Register (Offset = 504h) [reset = 0h]

Ethernet MAC address upper 16-bits.

Return to [Summary Table](#)

**Table 2-1429. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0504h       |

**Figure 2-476. TOP\_CTRL\_MAC\_ID1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MAC_ID1_MACID_HI |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MAC_ID1_MACID_HI |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 2-1431. TOP\_CTRL\_MAC\_ID1 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                             |
|-------|------------------|------|-------|-----------------------------------------------------------------------------------------|
| 31:16 | RESERVED         | NONE | 0h    | Reserved                                                                                |
| 15:0  | MAC_ID1_MACID_HI | R    | 0h    | 48-bit Ethernet MAC_ID field. Can be used by SW through MMR read - MAC ID high [16bits] |

### 2.3.2.16 TOP\_CTRL\_ADC\_REFBUF0\_CTRL Register

#### 1 TOP\_CTRL\_ADC\_REFBUF0\_CTRL Register (Offset = C00h) [reset = 0h]

This register is used to enable or disable ADC Reference buffer 0

Return to [Summary Table](#)

**Table 2-1432. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0C00h       |

**Figure 2-477. TOP\_CTRL\_ADC\_REFBUF0\_CTRL Name Register**

|          |    |    |    |    |                         |    |    |
|----------|----|----|----|----|-------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                      | 25 | 24 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                      | 17 | 16 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                      | 9  | 8  |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                       | 1  | 0  |
| RESERVED |    |    |    |    | ADC_REFBUF0_CTRL_ENABLE |    |    |
| NONE     |    |    |    |    | R/W                     |    |    |
| 0h       |    |    |    |    | 0h                      |    |    |

**Table 2-1434. TOP\_CTRL\_ADC\_REFBUF0\_CTRL Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                                                    |
|------|-------------------------|------|-------|--------------------------------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                                                       |
| 2:0  | ADC_REFBUF0_CTRL_ENABLE | R/W  | 0h    | Enables adc reference 0, mask hhv before enable<br>000:Disable<br>111 : Enable |

### 2.3.2.17 TOP\_CTRL\_ADC\_REFBUF1\_CTRL Register

#### 1 TOP\_CTRL\_ADC\_REFBUF1\_CTRL Register (Offset = C04h) [reset = 0h]

This register is used to enable or disable ADC Reference buffer 1

Return to [Summary Table](#)

**Table 2-1435. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0C04h       |

**Figure 2-478. TOP\_CTRL\_ADC\_REFBUF1\_CTRL Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | ADC_REFBUF1_CTRL_ENABLE |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-1437. TOP\_CTRL\_ADC\_REFBUF1\_CTRL Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                                                    |
|------|-------------------------|------|-------|--------------------------------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                                                       |
| 2:0  | ADC_REFBUF1_CTRL_ENABLE | R/W  | 0h    | Enables adc reference 1, mask hhv before enable<br>000:Disable<br>111 : Enable |

### 2.3.2.18 TOP\_CTRL\_ADC\_REF\_COMP\_CTRL Register

#### 1 TOP\_CTRL\_ADC\_REF\_COMP\_CTRL Register (Offset = C08h) [reset = 0h]

This register is used to enable or disable the voltage monitors which measure if the ADC reference voltage is good or not.

Return to [Summary Table](#)

**Table 2-1438. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0C08h       |

**Figure 2-479. TOP\_CTRL\_ADC\_REF\_COMP\_CTRL Name Register**

|          |                                  |    |    |          |                                  |    |    |
|----------|----------------------------------|----|----|----------|----------------------------------|----|----|
| 31       | 30                               | 29 | 28 | 27       | 26                               | 25 | 24 |
| RESERVED |                                  |    |    |          |                                  |    |    |
| NONE     |                                  |    |    |          |                                  |    |    |
| 0h       |                                  |    |    |          |                                  |    |    |
| 23       | 22                               | 21 | 20 | 19       | 18                               | 17 | 16 |
| RESERVED |                                  |    |    |          |                                  |    |    |
| NONE     |                                  |    |    |          |                                  |    |    |
| 0h       |                                  |    |    |          |                                  |    |    |
| 15       | 14                               | 13 | 12 | 11       | 10                               | 9  | 8  |
| RESERVED |                                  |    |    |          | ADC_REF_COMP_CTRL_ADC34_REFOK_EN |    |    |
| NONE     |                                  |    |    |          | R/W                              |    |    |
| 0h       |                                  |    |    |          | 0h                               |    |    |
| 7        | 6                                | 5  | 4  | 3        | 2                                | 1  | 0  |
| RESERVED | ADC_REF_COMP_CTRL_ADC12_REFOK_EN |    |    | RESERVED | ADC_REF_COMP_CTRL_ADC0_REFOK_EN  |    |    |
| NONE     | R/W                              |    |    | NONE     | R/W                              |    |    |
| 0h       | 0h                               |    |    | 0h       | 0h                               |    |    |

**Table 2-1440. TOP\_CTRL\_ADC\_REF\_COMP\_CTRL Register Field Descriptions**

| Bit   | Field                            | Type | Reset | Description                                                               |
|-------|----------------------------------|------|-------|---------------------------------------------------------------------------|
| 31:11 | RESERVED                         | NONE | 0h    | Reserved                                                                  |
| 10:8  | ADC_REF_COMP_CTRL_ADC34_REFOK_EN | R/W  | 0h    | Enables reference comparators [ROK1]. This monitors adc3 & adc4 refernc   |
| 7     | RESERVED                         | NONE | 0h    | Reserved                                                                  |
| 6:4   | ADC_REF_COMP_CTRL_ADC12_REFOK_EN | R/W  | 0h    | Enables reference comparators [ROK0B]. This monitors adc1 & adc2 refernce |
| 3     | RESERVED                         | NONE | 0h    | Reserved                                                                  |
| 2:0   | ADC_REF_COMP_CTRL_ADC0_REFOK_EN  | R/W  | 0h    | Enables reference comparators [ROK0]. This monitors adc0 refernce         |

### 2.3.2.19 TOP\_CTRL\_ADC\_REF\_GOOD\_STATUS Register

#### 1 TOP\_CTRL\_ADC\_REF\_GOOD\_STATUS Register (Offset = C0Ch) [reset = 3Fh]

This register shows the status of ADC reference voltages as measured by the ADC Reference OK voltage monitors.

Return to [Summary Table](#)

**Table 2-1441. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0C0Ch       |

**Figure 2-480. TOP\_CTRL\_ADC\_REF\_GOOD\_STATUS Name Register**

|          |                                       |                                       |                                      |                                      |                                       |                                       |                                       |
|----------|---------------------------------------|---------------------------------------|--------------------------------------|--------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|
| 31       | 30                                    | 29                                    | 28                                   | 27                                   | 26                                    | 25                                    | 24                                    |
| RESERVED |                                       |                                       |                                      |                                      |                                       |                                       |                                       |
| NONE     |                                       |                                       |                                      |                                      |                                       |                                       |                                       |
| 0h       |                                       |                                       |                                      |                                      |                                       |                                       |                                       |
| 23       | 22                                    | 21                                    | 20                                   | 19                                   | 18                                    | 17                                    | 16                                    |
| RESERVED |                                       |                                       |                                      |                                      |                                       |                                       |                                       |
| NONE     |                                       |                                       |                                      |                                      |                                       |                                       |                                       |
| 0h       |                                       |                                       |                                      |                                      |                                       |                                       |                                       |
| 15       | 14                                    | 13                                    | 12                                   | 11                                   | 10                                    | 9                                     | 8                                     |
| RESERVED |                                       |                                       |                                      |                                      |                                       |                                       |                                       |
| NONE     |                                       |                                       |                                      |                                      |                                       |                                       |                                       |
| 0h       |                                       |                                       |                                      |                                      |                                       |                                       |                                       |
| 7        | 6                                     | 5                                     | 4                                    | 3                                    | 2                                     | 1                                     | 0                                     |
| RESERVED | ADC_REF_GOOD_STATUS_ADC12_REF_UV_GOOD | ADC_REF_GOOD_STATUS_ADC12_REF_OV_GOOD | ADC_REF_GOOD_STATUS_ADC0_REF_UV_GOOD | ADC_REF_GOOD_STATUS_ADC0_REF_OV_GOOD | ADC_REF_GOOD_STATUS_ADC34_REF_UV_GOOD | ADC_REF_GOOD_STATUS_ADC34_REF_OV_GOOD | ADC_REF_GOOD_STATUS_ADC34_REF_OV_GOOD |
| NONE     | R                                     | R                                     | R                                    | R                                    | R                                     | R                                     | R                                     |
| 0h       | 1h                                    | 1h                                    | 1h                                   | 1h                                   | 1h                                    | 1h                                    | 1h                                    |

**Table 2-1443. TOP\_CTRL\_ADC\_REF\_GOOD\_STATUS Register Field Descriptions**

| Bit  | Field                                 | Type | Reset | Description            |
|------|---------------------------------------|------|-------|------------------------|
| 31:6 | RESERVED                              | NONE | 0h    | Reserved               |
| 5    | ADC_REF_GOOD_STATUS_ADC12_REF_UV_GOOD | R    | 1h    | Under Voltage check OK |
| 4    | ADC_REF_GOOD_STATUS_ADC12_REF_OV_GOOD | R    | 1h    | Over voltage check OK  |
| 3    | ADC_REF_GOOD_STATUS_ADC0_REF_UV_GOOD  | R    | 1h    | Under Voltage check OK |
| 2    | ADC_REF_GOOD_STATUS_ADC0_REF_OV_GOOD  | R    | 1h    | Over voltage check OK  |
| 1    | ADC_REF_GOOD_STATUS_ADC34_REF_UV_GOOD | R    | 1h    | Under Voltage check OK |



**Table 2-1443. TOP\_CTRL\_ADC\_REF\_GOOD\_STATUS Register Field Descriptions (continued)**

| Bit | Field                                         | Type | Reset | Description           |
|-----|-----------------------------------------------|------|-------|-----------------------|
| 0   | ADC_REF_GOOD_STAT<br>US_ADC34_REF_OV_GO<br>OD | R    | 1h    | Over voltage check OK |

### 2.3.2.20 TOP\_CTRL\_VMON\_CTRL Register

#### 1 TOP\_CTRL\_VMON\_CTRL Register (Offset = C10h) [reset = 7777777h]

This register is used to enable or disable the power supply voltage monitors present on the device.

Return to [Summary Table](#)

**Table 2-1444. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0C10h       |

**Figure 2-481. TOP\_CTRL\_VMON\_CTRL Name Register**

| 31       | 30                | 29 | 28 | 27       | 26                | 25                | 24 |
|----------|-------------------|----|----|----------|-------------------|-------------------|----|
| RESERVED |                   |    |    |          |                   | VMON_CTRL_CMP8_EN |    |
| NONE     |                   |    |    |          |                   | R/W               |    |
| 0h       |                   |    |    |          |                   | 7h                |    |
| 23       | 22                | 21 | 20 | 19       | 18                | 17                | 16 |
| RESERVED | VMON_CTRL_CMP7_EN |    |    | RESERVED | VMON_CTRL_CMP5_EN |                   |    |
| NONE     | R/W               |    |    | NONE     | R/W               |                   |    |
| 0h       | 7h                |    |    | 0h       | 7h                |                   |    |
| 15       | 14                | 13 | 12 | 11       | 10                | 9                 | 8  |
| RESERVED | VMON_CTRL_CMP3_EN |    |    | RESERVED | VMON_CTRL_CMP2_EN |                   |    |
| NONE     | R/W               |    |    | NONE     | R/W               |                   |    |
| 0h       | 7h                |    |    | 0h       | 7h                |                   |    |
| 7        | 6                 | 5  | 4  | 3        | 2                 | 1                 | 0  |
| RESERVED | VMON_CTRL_CMP1_EN |    |    | RESERVED | VMON_CTRL_CMP0_EN |                   |    |
| NONE     | R/W               |    |    | NONE     | R/W               |                   |    |
| 0h       | 7h                |    |    | 0h       | 7h                |                   |    |

**Table 2-1446. TOP\_CTRL\_VMON\_CTRL Register Field Descriptions**

| Bit   | Field             | Type | Reset | Description |
|-------|-------------------|------|-------|-------------|
| 31:27 | RESERVED          | NONE | 0h    | Reserved    |
| 26:24 | VMON_CTRL_CMP8_EN | R/W  | 7h    | VMON EN     |
| 23    | RESERVED          | NONE | 0h    | Reserved    |
| 22:20 | VMON_CTRL_CMP7_EN | R/W  | 7h    | VMON EN     |
| 19    | RESERVED          | NONE | 0h    | Reserved    |
| 18:16 | VMON_CTRL_CMP5_EN | R/W  | 7h    | VMON EN     |
| 15    | RESERVED          | NONE | 0h    | Reserved    |
| 14:12 | VMON_CTRL_CMP3_EN | R/W  | 7h    | VMON EN     |
| 11    | RESERVED          | NONE | 0h    | Reserved    |
| 10:8  | VMON_CTRL_CMP2_EN | R/W  | 7h    | VMON EN     |
| 7     | RESERVED          | NONE | 0h    | Reserved    |
| 6:4   | VMON_CTRL_CMP1_EN | R/W  | 7h    | VMON EN     |
| 3     | RESERVED          | NONE | 0h    | Reserved    |
| 2:0   | VMON_CTRL_CMP0_EN | R/W  | 7h    | VMON EN     |

### 2.3.2.21 TOP\_CTRL\_VMON\_STAT Register

#### 1 TOP\_CTRL\_VMON\_STAT Register (Offset = C14h) [reset = 7FFh]

This register shows the status output from the voltage monitors present on the device.

Return to [Summary Table](#)

**Table 2-1447. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0C14h       |

**Figure 2-482. TOP\_CTRL\_VMON\_STAT Name Register**

|                          |                          |                          |                          |                          |                          |                          |                          |
|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|
| 31                       | 30                       | 29                       | 28                       | 27                       | 26                       | 25                       | 24                       |
| RESERVED                 |                          |                          |                          |                          |                          |                          |                          |
| NONE                     |                          |                          |                          |                          |                          |                          |                          |
| 0h                       |                          |                          |                          |                          |                          |                          |                          |
| 23                       | 22                       | 21                       | 20                       | 19                       | 18                       | 17                       | 16                       |
| RESERVED                 |                          |                          |                          |                          |                          |                          |                          |
| NONE                     |                          |                          |                          |                          |                          |                          |                          |
| 0h                       |                          |                          |                          |                          |                          |                          |                          |
| 15                       | 14                       | 13                       | 12                       | 11                       | 10                       | 9                        | 8                        |
| RESERVED                 |                          |                          |                          |                          | VMON_STAT_C<br>MP8_UV_OK | VMON_STAT_C<br>MP7_UV_OK | VMON_STAT_C<br>MP5_UV_OK |
| NONE                     |                          |                          |                          |                          | R                        | R                        | R                        |
| 0h                       |                          |                          |                          |                          | 1h                       | 1h                       | 1h                       |
| 7                        | 6                        | 5                        | 4                        | 3                        | 2                        | 1                        | 0                        |
| VMON_STAT_C<br>MP5_OV_OK | VMON_STAT_C<br>MP3_UV_OK | VMON_STAT_C<br>MP3_OV_OK | VMON_STAT_C<br>MP2_UV_OK | VMON_STAT_C<br>MP2_OV_OK | VMON_STAT_C<br>MP1_UV_OK | VMON_STAT_C<br>MP1_OV_OK | VMON_STAT_C<br>MP0_UV_OK |
| R                        | R                        | R                        | R                        | R                        | R                        | R                        | R                        |
| 1h                       | 1h                       | 1h                       | 1h                       | 1h                       | 1h                       | 1h                       | 1h                       |

**Table 2-1449. TOP\_CTRL\_VMON\_STAT Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description |
|-------|----------------------|------|-------|-------------|
| 31:11 | RESERVED             | NONE | 0h    | Reserved    |
| 10    | VMON_STAT_CMP8_UV_OK | R    | 1h    | VMON OK     |
| 9     | VMON_STAT_CMP7_UV_OK | R    | 1h    | VMON OK     |
| 8     | VMON_STAT_CMP5_UV_OK | R    | 1h    | VMON OK     |
| 7     | VMON_STAT_CMP5_OV_OK | R    | 1h    | VMON OK     |
| 6     | VMON_STAT_CMP3_UV_OK | R    | 1h    | VMON OK     |
| 5     | VMON_STAT_CMP3_OV_OK | R    | 1h    | VMON OK     |
| 4     | VMON_STAT_CMP2_UV_OK | R    | 1h    | VMON OK     |
| 3     | VMON_STAT_CMP2_OV_OK | R    | 1h    | VMON OK     |
| 2     | VMON_STAT_CMP1_UV_OK | R    | 1h    | VMON OK     |

**Table 2-1449. TOP\_CTRL\_VMON\_STAT Register Field Descriptions (continued)**

| Bit | Field                | Type | Reset | Description |
|-----|----------------------|------|-------|-------------|
| 1   | VMON_STAT_CMP1_OV_OK | R    | 1h    | VMON OK     |
| 0   | VMON_STAT_CMP0_UV_OK | R    | 1h    | VMON OK     |

### 2.3.2.22 TOP\_CTRL\_PMU\_COARSE\_STAT Register

#### 1 TOP\_CTRL\_PMU\_COARSE\_STAT Register (Offset = C18h) [reset = Fh]

This register shows the status of coarse voltage monitors present in the device.

Return to [Summary Table](#)

**Table 2-1450. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0C18h       |

**Figure 2-483. TOP\_CTRL\_PMU\_COARSE\_STAT Name Register**

|          |    |    |    |                        |                         |                           |                            |
|----------|----|----|----|------------------------|-------------------------|---------------------------|----------------------------|
| 31       | 30 | 29 | 28 | 27                     | 26                      | 25                        | 24                         |
| RESERVED |    |    |    |                        |                         |                           |                            |
| NONE     |    |    |    |                        |                         |                           |                            |
| 0h       |    |    |    |                        |                         |                           |                            |
| 23       | 22 | 21 | 20 | 19                     | 18                      | 17                        | 16                         |
| RESERVED |    |    |    |                        |                         |                           |                            |
| NONE     |    |    |    |                        |                         |                           |                            |
| 0h       |    |    |    |                        |                         |                           |                            |
| 15       | 14 | 13 | 12 | 11                     | 10                      | 9                         | 8                          |
| RESERVED |    |    |    |                        |                         |                           |                            |
| NONE     |    |    |    |                        |                         |                           |                            |
| 0h       |    |    |    |                        |                         |                           |                            |
| 7        | 6  | 5  | 4  | 3                      | 2                       | 1                         | 0                          |
| RESERVED |    |    |    | PMU_COARSE_STAT_BG_RDY | PMU_COARSE_STAT_LDO_RDY | PMU_COARSE_STAT_VCORE_RDY | PMU_COARSE_STAT_VSUP18_RDY |
| NONE     |    |    |    | R                      | R                       | R                         | R                          |
| 0h       |    |    |    | 1h                     | 1h                      | 1h                        | 1h                         |

**Table 2-1452. TOP\_CTRL\_PMU\_COARSE\_STAT Register Field Descriptions**

| Bit  | Field                      | Type | Reset | Description                              |
|------|----------------------------|------|-------|------------------------------------------|
| 31:4 | RESERVED                   | NONE | 0h    | Reserved                                 |
| 3    | PMU_COARSE_STAT_BG_RDY     | R    | 1h    | Bandgap coarse detection status signals. |
| 2    | PMU_COARSE_STAT_LDO_RDY    | R    | 1h    | LDO coarse detection status signals.     |
| 1    | PMU_COARSE_STAT_VCORE_RDY  | R    | 1h    | vcore coarse detection status signals.   |
| 0    | PMU_COARSE_STAT_VSUP18_RDY | R    | 1h    | vdda18 coarse detection status signals.  |

### 2.3.2.23 TOP\_CTRL\_MASK\_VMON\_ERROR\_ESM\_H Register

#### 1 TOP\_CTRL\_MASK\_VMON\_ERROR\_ESM\_H Register (Offset = C20h) [reset = 1FFFFh]

This register is used to select the voltage monitors whose Error status should trigger the ESM High Interrupt.

Return to [Summary Table](#)

**Table 2-1453. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0C20h       |

**Figure 2-484. TOP\_CTRL\_MASK\_VMON\_ERROR\_ESM\_H Name Register**

|                                         |                                        |                                        |                                         |                                         |                                        |                                        |                                         |
|-----------------------------------------|----------------------------------------|----------------------------------------|-----------------------------------------|-----------------------------------------|----------------------------------------|----------------------------------------|-----------------------------------------|
| 31                                      | 30                                     | 29                                     | 28                                      | 27                                      | 26                                     | 25                                     | 24                                      |
| RESERVED                                |                                        |                                        |                                         |                                         |                                        |                                        |                                         |
| NONE                                    |                                        |                                        |                                         |                                         |                                        |                                        |                                         |
| 0h                                      |                                        |                                        |                                         |                                         |                                        |                                        |                                         |
| 23                                      | 22                                     | 21                                     | 20                                      | 19                                      | 18                                     | 17                                     | 16                                      |
| RESERVED                                |                                        |                                        |                                         |                                         |                                        |                                        | MASK_VMON_ERROR_ESM_H_ADC12_REF_UV_MASK |
| NONE                                    |                                        |                                        |                                         |                                         |                                        |                                        | R/W                                     |
| 0h                                      |                                        |                                        |                                         |                                         |                                        |                                        | 1h                                      |
| 15                                      | 14                                     | 13                                     | 12                                      | 11                                      | 10                                     | 9                                      | 8                                       |
| MASK_VMON_ERROR_ESM_H_ADC12_REF_OV_MASK | MASK_VMON_ERROR_ESM_H_ADC0_REF_UV_MASK | MASK_VMON_ERROR_ESM_H_ADC0_REF_OV_MASK | MASK_VMON_ERROR_ESM_H_ADC34_REF_UV_MASK | MASK_VMON_ERROR_ESM_H_ADC34_REF_OV_MASK | MASK_VMON_ERROR_ESM_H_CMP8_UV_ERR_MASK | MASK_VMON_ERROR_ESM_H_CMP7_UV_ERR_MASK | MASK_VMON_ERROR_ESM_H_CMP5_UV_ERR_MASK  |
| R/W                                     | R/W                                    | R/W                                    | R/W                                     | R/W                                     | R/W                                    | R/W                                    | R/W                                     |
| 1h                                      | 1h                                     | 1h                                     | 1h                                      | 1h                                      | 1h                                     | 1h                                     | 1h                                      |
| 7                                       | 6                                      | 5                                      | 4                                       | 3                                       | 2                                      | 1                                      | 0                                       |
| MASK_VMON_ERROR_ESM_H_CMP5_OV_ERR_MASK  | MASK_VMON_ERROR_ESM_H_CMP3_UV_ERR_MASK | MASK_VMON_ERROR_ESM_H_CMP3_OV_ERR_MASK | MASK_VMON_ERROR_ESM_H_CMP2_UV_ERR_MASK  | MASK_VMON_ERROR_ESM_H_CMP2_OV_ERR_MASK  | MASK_VMON_ERROR_ESM_H_CMP1_UV_ERR_MASK | MASK_VMON_ERROR_ESM_H_CMP1_OV_ERR_MASK | MASK_VMON_ERROR_ESM_H_CMP0_UV_ERR_MASK  |
| R/W                                     | R/W                                    | R/W                                    | R/W                                     | R/W                                     | R/W                                    | R/W                                    | R/W                                     |
| 1h                                      | 1h                                     | 1h                                     | 1h                                      | 1h                                      | 1h                                     | 1h                                     | 1h                                      |

**Table 2-1455. TOP\_CTRL\_MASK\_VMON\_ERROR\_ESM\_H Register Field Descriptions**

| Bit   | Field                                   | Type | Reset | Description            |
|-------|-----------------------------------------|------|-------|------------------------|
| 31:17 | RESERVED                                | NONE | 0h    | Reserved               |
| 16    | MASK_VMON_ERROR_ESM_H_ADC12_REF_UV_MASK | R/W  | 1h    | VMON Error Mask to ESM |
| 15    | MASK_VMON_ERROR_ESM_H_ADC12_REF_OV_MASK | R/W  | 1h    | VMON Error Mask to ESM |
| 14    | MASK_VMON_ERROR_ESM_H_ADC0_REF_UV_MASK  | R/W  | 1h    | VMON Error Mask to ESM |
| 13    | MASK_VMON_ERROR_ESM_H_ADC0_REF_OV_MASK  | R/W  | 1h    | VMON Error Mask to ESM |

**Table 2-1455. TOP\_CTRL\_MASK\_VMON\_ERROR\_ESM\_H Register Field Descriptions (continued)**

| Bit | Field                                   | Type | Reset | Description            |
|-----|-----------------------------------------|------|-------|------------------------|
| 12  | MASK_VMON_ERROR_ESM_H_ADC34_REF_UV_MASK | R/W  | 1h    | VMON Error Mask to ESM |
| 11  | MASK_VMON_ERROR_ESM_H_ADC34_REF_OV_MASK | R/W  | 1h    | VMON Error Mask to ESM |
| 10  | MASK_VMON_ERROR_ESM_H_CMP8_UV_ERR_MASK  | R/W  | 1h    | VMON Error Mask to ESM |
| 9   | MASK_VMON_ERROR_ESM_H_CMP7_UV_ERR_MASK  | R/W  | 1h    | VMON Error Mask to ESM |
| 8   | MASK_VMON_ERROR_ESM_H_CMP5_UV_ERR_MASK  | R/W  | 1h    | VMON Error Mask to ESM |
| 7   | MASK_VMON_ERROR_ESM_H_CMP5_OV_ERR_MASK  | R/W  | 1h    | VMON Error Mask to ESM |
| 6   | MASK_VMON_ERROR_ESM_H_CMP3_UV_ERR_MASK  | R/W  | 1h    | VMON Error Mask to ESM |
| 5   | MASK_VMON_ERROR_ESM_H_CMP3_OV_ERR_MASK  | R/W  | 1h    | VMON Error Mask to ESM |
| 4   | MASK_VMON_ERROR_ESM_H_CMP2_UV_ERR_MASK  | R/W  | 1h    | VMON Error Mask to ESM |
| 3   | MASK_VMON_ERROR_ESM_H_CMP2_OV_ERR_MASK  | R/W  | 1h    | VMON Error Mask to ESM |
| 2   | MASK_VMON_ERROR_ESM_H_CMP1_UV_ERR_MASK  | R/W  | 1h    | VMON Error Mask to ESM |
| 1   | MASK_VMON_ERROR_ESM_H_CMP1_OV_ERR_MASK  | R/W  | 1h    | VMON Error Mask to ESM |
| 0   | MASK_VMON_ERROR_ESM_H_CMP0_UV_ERR_MASK  | R/W  | 1h    | VMON Error Mask to ESM |

### 2.3.2.24 TOP\_CTRL\_MASK\_VMON\_ERROR\_ESM\_L Register

#### 1 TOP\_CTRL\_MASK\_VMON\_ERROR\_ESM\_L Register (Offset = C24h) [reset = 1FFFFh]

This register is used to select the voltage monitors whose Error status should trigger the ESM Low Interrupt.

Return to [Summary Table](#)

**Table 2-1456. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0C24h       |

**Figure 2-485. TOP\_CTRL\_MASK\_VMON\_ERROR\_ESM\_L Name Register**

| 31                                      | 30                                      | 29                                      | 28                                      | 27                                      | 26                                      | 25                                      | 24                                      |
|-----------------------------------------|-----------------------------------------|-----------------------------------------|-----------------------------------------|-----------------------------------------|-----------------------------------------|-----------------------------------------|-----------------------------------------|
| RESERVED                                |                                         |                                         |                                         |                                         |                                         |                                         |                                         |
| NONE                                    |                                         |                                         |                                         |                                         |                                         |                                         |                                         |
| 0h                                      |                                         |                                         |                                         |                                         |                                         |                                         |                                         |
| 23                                      | 22                                      | 21                                      | 20                                      | 19                                      | 18                                      | 17                                      | 16                                      |
| RESERVED                                |                                         |                                         |                                         |                                         |                                         |                                         | MASK_VMON_ERROR_ESM_L_ADC12_REF_UV_MASK |
| NONE                                    |                                         |                                         |                                         |                                         |                                         |                                         | R/W                                     |
| 0h                                      |                                         |                                         |                                         |                                         |                                         |                                         | 1h                                      |
| 15                                      | 14                                      | 13                                      | 12                                      | 11                                      | 10                                      | 9                                       | 8                                       |
| MASK_VMON_ERROR_ESM_L_ADC12_REF_OV_MASK | MASK_VMON_ERROR_ESM_L_ADC0_REF_UV_MASK  | MASK_VMON_ERROR_ESM_L_ADC0_REF_OV_MASK  | MASK_VMON_ERROR_ESM_L_ADC34_REF_UV_MASK | MASK_VMON_ERROR_ESM_L_ADC34_REF_OV_MASK | MASK_VMON_ERROR_ESM_L_CMP8_UV_E RR_MASK | MASK_VMON_ERROR_ESM_L_CMP7_UV_E RR_MASK | MASK_VMON_ERROR_ESM_L_CMP5_UV_E RR_MASK |
| R/W                                     | R/W                                     | R/W                                     | R/W                                     | R/W                                     | R/W                                     | R/W                                     | R/W                                     |
| 1h                                      | 1h                                      | 1h                                      | 1h                                      | 1h                                      | 1h                                      | 1h                                      | 1h                                      |
| 7                                       | 6                                       | 5                                       | 4                                       | 3                                       | 2                                       | 1                                       | 0                                       |
| MASK_VMON_ERROR_ESM_L_CMP5_OV_E RR_MASK | MASK_VMON_ERROR_ESM_L_CMP3_UV_E RR_MASK | MASK_VMON_ERROR_ESM_L_CMP3_OV_E RR_MASK | MASK_VMON_ERROR_ESM_L_CMP2_UV_E RR_MASK | MASK_VMON_ERROR_ESM_L_CMP2_OV_E RR_MASK | MASK_VMON_ERROR_ESM_L_CMP1_UV_E RR_MASK | MASK_VMON_ERROR_ESM_L_CMP1_OV_E RR_MASK | MASK_VMON_ERROR_ESM_L_CMP0_UV_E RR_MASK |
| R/W                                     | R/W                                     | R/W                                     | R/W                                     | R/W                                     | R/W                                     | R/W                                     | R/W                                     |
| 1h                                      | 1h                                      | 1h                                      | 1h                                      | 1h                                      | 1h                                      | 1h                                      | 1h                                      |

**Table 2-1458. TOP\_CTRL\_MASK\_VMON\_ERROR\_ESM\_L Register Field Descriptions**

| Bit   | Field                                   | Type | Reset | Description             |
|-------|-----------------------------------------|------|-------|-------------------------|
| 31:17 | RESERVED                                | NONE | 0h    | Reserved                |
| 16    | MASK_VMON_ERROR_ESM_L_ADC12_REF_UV_MASK | R/W  | 1h    | VMON Error Mask to INTR |
| 15    | MASK_VMON_ERROR_ESM_L_ADC12_REF_OV_MASK | R/W  | 1h    | VMON Error Mask to INTR |
| 14    | MASK_VMON_ERROR_ESM_L_ADC0_REF_UV_MASK  | R/W  | 1h    | VMON Error Mask to INTR |
| 13    | MASK_VMON_ERROR_ESM_L_ADC0_REF_OV_MASK  | R/W  | 1h    | VMON Error Mask to INTR |



**Table 2-1458. TOP\_CTRL\_MASK\_VMON\_ERROR\_ESM\_L Register Field Descriptions (continued)**

| Bit | Field                                   | Type | Reset | Description             |
|-----|-----------------------------------------|------|-------|-------------------------|
| 12  | MASK_VMON_ERROR_ESM_L_ADC34_REF_UV_MASK | R/W  | 1h    | VMON Error Mask to INTR |
| 11  | MASK_VMON_ERROR_ESM_L_ADC34_REF_OV_MASK | R/W  | 1h    | VMON Error Mask to INTR |
| 10  | MASK_VMON_ERROR_ESM_L_CMP8_UV_ERR_MASK  | R/W  | 1h    | VMON Error Mask to INTR |
| 9   | MASK_VMON_ERROR_ESM_L_CMP7_UV_ERR_MASK  | R/W  | 1h    | VMON Error Mask to INTR |
| 8   | MASK_VMON_ERROR_ESM_L_CMP5_UV_ERR_MASK  | R/W  | 1h    | VMON Error Mask to INTR |
| 7   | MASK_VMON_ERROR_ESM_L_CMP5_OV_ERR_MASK  | R/W  | 1h    | VMON Error Mask to INTR |
| 6   | MASK_VMON_ERROR_ESM_L_CMP3_UV_ERR_MASK  | R/W  | 1h    | VMON Error Mask to INTR |
| 5   | MASK_VMON_ERROR_ESM_L_CMP3_OV_ERR_MASK  | R/W  | 1h    | VMON Error Mask to INTR |
| 4   | MASK_VMON_ERROR_ESM_L_CMP2_UV_ERR_MASK  | R/W  | 1h    | VMON Error Mask to INTR |
| 3   | MASK_VMON_ERROR_ESM_L_CMP2_OV_ERR_MASK  | R/W  | 1h    | VMON Error Mask to INTR |
| 2   | MASK_VMON_ERROR_ESM_L_CMP1_UV_ERR_MASK  | R/W  | 1h    | VMON Error Mask to INTR |
| 1   | MASK_VMON_ERROR_ESM_L_CMP1_OV_ERR_MASK  | R/W  | 1h    | VMON Error Mask to INTR |
| 0   | MASK_VMON_ERROR_ESM_L_CMP0_UV_ERR_MASK  | R/W  | 1h    | VMON Error Mask to INTR |

### 2.3.2.25 TOP\_CTRL\_VMON\_FILTER\_CTRL Register

#### 1 TOP\_CTRL\_VMON\_FILTER\_CTRL Register (Offset = C34h) [reset = 0h]

This register is used to configure the filter present on the Voltage monitor outputs.

Return to [Summary Table](#)

**Table 2-1459. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0C34h       |

**Figure 2-486. TOP\_CTRL\_VMON\_FILTER\_CTRL Name Register**

|          |    |    |    |    |    |                               |    |
|----------|----|----|----|----|----|-------------------------------|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25                            | 24 |
| RESERVED |    |    |    |    |    |                               |    |
| NONE     |    |    |    |    |    |                               |    |
| 0h       |    |    |    |    |    |                               |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17                            | 16 |
| RESERVED |    |    |    |    |    |                               |    |
| NONE     |    |    |    |    |    |                               |    |
| 0h       |    |    |    |    |    |                               |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9                             | 8  |
| RESERVED |    |    |    |    |    |                               |    |
| NONE     |    |    |    |    |    |                               |    |
| 0h       |    |    |    |    |    |                               |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1                             | 0  |
| RESERVED |    |    |    |    |    | VMON_FILTER_CTRL_SELECT_VALUE |    |
| NONE     |    |    |    |    |    | R/W                           |    |
| 0h       |    |    |    |    |    | 0h                            |    |

**Table 2-1461. TOP\_CTRL\_VMON\_FILTER\_CTRL Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                                                                                                                                                                    |
|------|-------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED                      | NONE | 0h    | Reserved                                                                                                                                                                                       |
| 1:0  | VMON_FILTER_CTRL_SELECT_VALUE | R/W  | 0h    | VMON FILTER control select<br>00 : no filtering [default]<br>01 : filtering for 4.8us<br>10 : filtering for 9.6us<br>11 : filtering for 14.4us<br>**Note: This bit will only be reset by PORz. |

### 2.3.2.26 TOP\_CTRL\_TSENSE\_CFG Register

#### 1 TOP\_CTRL\_TSENSE\_CFG Register (Offset = D00h) [reset = 11110000h]

This register is used to enable and configure the Temperature sensors present in the device.

Return to [Summary Table](#)

**Table 2-1462. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0D00h       |

**Figure 2-487. TOP\_CTRL\_TSENSE\_CFG Name Register**

| 31                    | 30 | 29               | 28                 | 27       | 26 | 25 | 24                     |
|-----------------------|----|------------------|--------------------|----------|----|----|------------------------|
| RESERVED              |    |                  | TSENSE_CFG_TMPSOFF | RESERVED |    |    | TSENSE_CFG_BGROFF      |
| NONE                  |    |                  | R/W                | NONE     |    |    | R/W                    |
| 0h                    |    |                  | 1h                 | 0h       |    |    | 1h                     |
| 23                    | 22 | 21               | 20                 | 19       | 18 | 17 | 16                     |
| RESERVED              |    |                  | TSENSE_CFG_AIPOFF  | RESERVED |    |    | TSENSE_CFG_SNSR_MX_HIZ |
| NONE                  |    |                  | R/W                | NONE     |    |    | R/W                    |
| 0h                    |    |                  | 1h                 | 0h       |    |    | 1h                     |
| 15                    | 14 | 13               | 12                 | 11       | 10 | 9  | 8                      |
| RESERVED              |    | TSENSE_CFG_DELAY |                    |          |    |    |                        |
| NONE                  |    | R/W              |                    |          |    |    |                        |
| 0h                    |    | 0h               |                    |          |    |    |                        |
| 7                     | 6  | 5                | 4                  | 3        | 2  | 1  | 0                      |
| TSENSE_CFG_SENSOR_SEL |    |                  |                    | RESERVED |    |    | TSENSE_CFG_ENABLE      |
| R/W                   |    |                  |                    | NONE     |    |    | R/W                    |
| 0h                    |    |                  |                    | 0h       |    |    | 0h                     |

**Table 2-1464. TOP\_CTRL\_TSENSE\_CFG Register Field Descriptions**

| Bit   | Field                  | Type | Reset | Description                                                                                                                                                                       |
|-------|------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED               | NONE | 0h    | Reserved                                                                                                                                                                          |
| 28    | TSENSE_CFG_TMPSOFF     | R/W  | 1h    | Temperature sensor off<br>0 : on<br>1 : off<br>**Note: This bit will only be reset by PORz.                                                                                       |
| 27:25 | RESERVED               | NONE | 0h    | Reserved                                                                                                                                                                          |
| 24    | TSENSE_CFG_BGROFF      | R/W  | 1h    | BandGap on/off control<br>1 : off<br>0 : on<br>**Note: This bit will only be reset by PORz.                                                                                       |
| 23:21 | RESERVED               | NONE | 0h    | Reserved                                                                                                                                                                          |
| 20    | TSENSE_CFG_AIPOFF      | R/W  | 1h    | 1 : iddq mode select<br>0 : normal mode<br>**Note: This bit will only be reset by PORz.                                                                                           |
| 19:17 | RESERVED               | NONE | 0h    | Reserved                                                                                                                                                                          |
| 16    | TSENSE_CFG_SNSR_MX_HIZ | R/W  | 1h    | Sensor mux hiz control<br>0 : normal operation. Mux will select either one of the analog sensor<br>1 : mux will be high impedance<br>**Note: This bit will only be reset by PORz. |

**Table 2-1464. TOP\_CTRL\_TSENSE\_CFG Register Field Descriptions (continued)**

| Bit   | Field                 | Type | Reset | Description                                                                                                                                                                                                                                           |
|-------|-----------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | RESERVED              | NONE | 0h    | Reserved                                                                                                                                                                                                                                              |
| 13:8  | TSENSE_CFG_DELAY      | R/W  | 0h    | Number of wait clock cycles between each TMPS Readout. Configure a Non zero value as delay value since configuring 0 is not allowed<br>**Note: This bit will only be reset by PORz.                                                                   |
| 7:4   | TSENSE_CFG_SENSOR_SEL | R/W  | 0h    | Sensor Selection<br>sensor enable bits for each sensor<br>0 : sensor disable<br>1 : sensor enable<br>bit<br>3:temp_sensor3<br>bit<br>2:temp_sensor2<br>bit<br>1:temp_sensor1<br>bit<br>0:temp_sensor0<br>**Note: This bit will only be reset by PORz. |
| 3:1   | RESERVED              | NONE | 0h    | Reserved                                                                                                                                                                                                                                              |
| 0     | TSENSE_CFG_ENABLE     | R/W  | 0h    | Temperature controller enable<br>**Note: This bit will only be reset by PORz.                                                                                                                                                                         |

### 2.3.2.27 TOP\_CTRL\_TSENSE\_STATUS Register

#### 1 TOP\_CTRL\_TSENSE\_STATUS Register (Offset = D04h) [reset = 0h]

This register shows the status of Temperature comparator events which are unmasked.

Return to [Summary Table](#)

**Table 2-1465. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0D04h       |

**Figure 2-488. TOP\_CTRL\_TSENSE\_STATUS Name Register**

|          |                           |                          |                                     |          |                           |                          |                                     |
|----------|---------------------------|--------------------------|-------------------------------------|----------|---------------------------|--------------------------|-------------------------------------|
| 31       | 30                        | 29                       | 28                                  | 27       | 26                        | 25                       | 24                                  |
| RESERVED |                           |                          |                                     |          |                           |                          |                                     |
| NONE     |                           |                          |                                     |          |                           |                          |                                     |
| 0h       |                           |                          |                                     |          |                           |                          |                                     |
| 23       | 22                        | 21                       | 20                                  | 19       | 18                        | 17                       | 16                                  |
| RESERVED |                           |                          |                                     |          |                           |                          |                                     |
| NONE     |                           |                          |                                     |          |                           |                          |                                     |
| 0h       |                           |                          |                                     |          |                           |                          |                                     |
| 15       | 14                        | 13                       | 12                                  | 11       | 10                        | 9                        | 8                                   |
| RESERVED |                           |                          |                                     |          |                           |                          |                                     |
| NONE     |                           |                          |                                     |          |                           |                          |                                     |
| 0h       |                           |                          |                                     |          |                           |                          |                                     |
| 7        | 6                         | 5                        | 4                                   | 3        | 2                         | 1                        | 0                                   |
| RESERVED | TSENSE_STAT<br>US_S1_COLD | TSENSE_STAT<br>US_S1_HOT | TSENSE_STAT<br>US_S1_LOW_T<br>HRHLD | RESERVED | TSENSE_STAT<br>US_S0_COLD | TSENSE_STAT<br>US_S0_HOT | TSENSE_STAT<br>US_S0_LOW_T<br>HRHLD |
| NONE     | R                         | R                        | R                                   | NONE     | R                         | R                        | R                                   |
| 0h       | 0h                        | 0h                       | 0h                                  | 0h       | 0h                        | 0h                       | 0h                                  |

**Table 2-1467. TOP\_CTRL\_TSENSE\_STATUS Register Field Descriptions**

| Bit  | Field                           | Type | Reset | Description                                                                                                                                     |
|------|---------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                        |
| 6    | TSENSE_STATUS_S1_C<br>OLD       | R    | 0h    | temperature Sensor 1 hot event detect<br>0 : event not occurred<br>1 : event occurred<br>**Note: This bit will only be reset by PORz.           |
| 5    | TSENSE_STATUS_S1_H<br>OT        | R    | 0h    | temperature Sensor 1 cold event detect<br>0 : event not occurred<br>1 : event occurred<br>**Note: This bit will only be reset by PORz.          |
| 4    | TSENSE_STATUS_S1_L<br>OW_THRHLD | R    | 0h    | temperature Sensor 1 low threshold event detect<br>0 : event not occurred<br>1 : event occurred<br>**Note: This bit will only be reset by PORz. |
| 3    | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                        |
| 2    | TSENSE_STATUS_S0_C<br>OLD       | R    | 0h    | temperature Sensor 0 hot event detect<br>0 : event not occurred<br>1 : event occurred<br>**Note: This bit will only be reset by PORz.           |

**Table 2-1467. TOP\_CTRL\_TSENSE\_STATUS Register Field Descriptions (continued)**

| Bit | Field                       | Type | Reset | Description                                                                                                                                     |
|-----|-----------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | TSENSE_STATUS_S0_HOT        | R    | 0h    | temperature Sensor 0 cold event detect<br>0 : event not occurred<br>1 : event occurred<br>**Note: This bit will only be reset by PORz.          |
| 0   | TSENSE_STATUS_S0_LOW_THRHLD | R    | 0h    | temperature Sensor 0 low threshold event detect<br>0 : event not occurred<br>1 : event occurred<br>**Note: This bit will only be reset by PORz. |

### 2.3.2.28 TOP\_CTRL\_TSENSE\_STATUS\_RAW Register

#### 1 TOP\_CTRL\_TSENSE\_STATUS\_RAW Register (Offset = D08h) [reset = 0h]

This register shows the status of all Temperature comparators events including masked events.

Return to [Summary Table](#)

**Table 2-1468. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0D08h       |

**Figure 2-489. TOP\_CTRL\_TSENSE\_STATUS\_RAW Name Register**

|          |                                   |                                  |                                        |          |                                   |                                  |                                        |
|----------|-----------------------------------|----------------------------------|----------------------------------------|----------|-----------------------------------|----------------------------------|----------------------------------------|
| 31       | 30                                | 29                               | 28                                     | 27       | 26                                | 25                               | 24                                     |
| RESERVED |                                   |                                  |                                        |          |                                   |                                  |                                        |
| NONE     |                                   |                                  |                                        |          |                                   |                                  |                                        |
| 0h       |                                   |                                  |                                        |          |                                   |                                  |                                        |
| 23       | 22                                | 21                               | 20                                     | 19       | 18                                | 17                               | 16                                     |
| RESERVED |                                   |                                  |                                        |          |                                   |                                  |                                        |
| NONE     |                                   |                                  |                                        |          |                                   |                                  |                                        |
| 0h       |                                   |                                  |                                        |          |                                   |                                  |                                        |
| 15       | 14                                | 13                               | 12                                     | 11       | 10                                | 9                                | 8                                      |
| RESERVED |                                   |                                  |                                        |          |                                   |                                  |                                        |
| NONE     |                                   |                                  |                                        |          |                                   |                                  |                                        |
| 0h       |                                   |                                  |                                        |          |                                   |                                  |                                        |
| 7        | 6                                 | 5                                | 4                                      | 3        | 2                                 | 1                                | 0                                      |
| RESERVED | TSENSE_STAT<br>US_RAW_S1_<br>COLD | TSENSE_STAT<br>US_RAW_S1_<br>HOT | TSENSE_STAT<br>US_RAW_S1_<br>LOW_THRHL | RESERVED | TSENSE_STAT<br>US_RAW_S0_<br>COLD | TSENSE_STAT<br>US_RAW_S0_<br>HOT | TSENSE_STAT<br>US_RAW_S0_<br>LOW_THRHL |
| NONE     | R                                 | R                                | R                                      | NONE     | R                                 | R                                | R                                      |
| 0h       | 0h                                | 0h                               | 0h                                     | 0h       | 0h                                | 0h                               | 0h                                     |

**Table 2-1470. TOP\_CTRL\_TSENSE\_STATUS\_RAW Register Field Descriptions**

| Bit  | Field                              | Type | Reset | Description                                                                                                                                     |
|------|------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                        |
| 6    | TSENSE_STATUS_RAW_<br>S1_COLD      | R    | 0h    | temperature Sensor 1 hot event detect<br>0 : event not occurred<br>1 : event occurred<br>**Note: This bit will only be reset by PORz.           |
| 5    | TSENSE_STATUS_RAW_<br>S1_HOT       | R    | 0h    | temperature Sensor 1 cold event detect<br>0 : event not occurred<br>1 : event occurred<br>**Note: This bit will only be reset by PORz.          |
| 4    | TSENSE_STATUS_RAW_<br>S1_LOW_THRHL | R    | 0h    | temperature Sensor 1 low threshold event detect<br>0 : event not occurred<br>1 : event occurred<br>**Note: This bit will only be reset by PORz. |
| 3    | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                        |
| 2    | TSENSE_STATUS_RAW_<br>S0_COLD      | R    | 0h    | temperature Sensor 0 hot event detect<br>0 : event not occurred<br>1 : event occurred<br>**Note: This bit will only be reset by PORz.           |

**Table 2-1470. TOP\_CTRL\_TSENSE\_STATUS\_RAW Register Field Descriptions (continued)**

| Bit | Field                           | Type | Reset | Description                                                                                                                                     |
|-----|---------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | TSENSE_STATUS_RAW_S0_HOT        | R    | 0h    | temperature Sensor 0 cold event detect<br>0 : event not occurred<br>1 : event occurred<br>**Note: This bit will only be reset by PORz.          |
| 0   | TSENSE_STATUS_RAW_S0_LOW_THRHLD | R    | 0h    | temperature Sensor 0 low threshold event detect<br>0 : event not occurred<br>1 : event occurred<br>**Note: This bit will only be reset by PORz. |



### 2.3.2.29 TOP\_CTRL\_TSENSE0\_ALERT Register

#### 1 TOP\_CTRL\_TSENSE0\_ALERT Register (Offset = D14h) [reset = 0h]

This register is used to configure the temperature thresholds for Temp Sensor 0 for generating Alert Interrupts.

Return to [Summary Table](#)

**Table 2-1471. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0D14h       |

**Figure 2-490. TOP\_CTRL\_TSENSE0\_ALERT Name Register**

|                                 |    |    |    |    |    |    |    |
|---------------------------------|----|----|----|----|----|----|----|
| 31                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 23                              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TSENSE0_ALERT_ALERT_THRHLD_HOT  |    |    |    |    |    |    |    |
| R/W                             |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 15                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 7                               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TSENSE0_ALERT_ALERT_THRHLD_COLD |    |    |    |    |    |    |    |
| R/W                             |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |

**Table 2-1473. TOP\_CTRL\_TSENSE0\_ALERT Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                                       |
|-------|-------------------------------------|------|-------|-----------------------------------------------------------------------------------|
| 31:24 | RESERVED                            | NONE | 0h    | Reserved                                                                          |
| 23:16 | TSENSE0_ALERT_ALER<br>T_THRHLD_HOT  | R/W  | 0h    | cold threshold/low temp threshold<br>**Note: This bit will only be reset by PORz. |
| 15:8  | RESERVED                            | NONE | 0h    | Reserved                                                                          |
| 7:0   | TSENSE0_ALERT_ALER<br>T_THRHLD_COLD | R/W  | 0h    | Hot threshold/high temp threshold<br>**Note: This bit will only be reset by PORz. |

### 2.3.2.30 TOP\_CTRL\_TSENSE0\_CNTL Register

#### 1 TOP\_CTRL\_TSENSE0\_CNTL Register (Offset = D18h) [reset = 100000h]

This register is used to control and configure Temperature sensor 0

Return to [Summary Table](#)

**Table 2-1474. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0D18h       |

**Figure 2-491. TOP\_CTRL\_TSENSE0\_CNTL Name Register**

|          |    |    |                          |          |    |    |                              |
|----------|----|----|--------------------------|----------|----|----|------------------------------|
| 31       | 30 | 29 | 28                       | 27       | 26 | 25 | 24                           |
| RESERVED |    |    |                          |          |    |    | TSENSE0_CNTL_MASK_LOW_THRHLD |
| NONE     |    |    |                          |          |    |    | R/W                          |
| 0h       |    |    |                          |          |    |    | 0h                           |
| 23       | 22 | 21 | 20                       | 19       | 18 | 17 | 16                           |
| RESERVED |    |    | TSENSE0_CNTL_MASK_COLD   | RESERVED |    |    | TSENSE0_CNTL_MASK_HOT        |
| NONE     |    |    | R/W                      | NONE     |    |    | R/W                          |
| 0h       |    |    | 1h                       | 0h       |    |    | 0h                           |
| 15       | 14 | 13 | 12                       | 11       | 10 | 9  | 8                            |
| RESERVED |    |    |                          |          |    |    | TSENSE0_CNTL_ACCU_CLEAR      |
| NONE     |    |    |                          |          |    |    | R/W                          |
| 0h       |    |    |                          |          |    |    | 0h                           |
| 7        | 6  | 5  | 4                        | 3        | 2  | 1  | 0                            |
| RESERVED |    |    | TSENSE0_CNTL_FIFO_FREEZE | RESERVED |    |    | TSENSE0_CNTL_FIFO_CLEAR      |
| NONE     |    |    | R/W                      | NONE     |    |    | R/W                          |
| 0h       |    |    | 0h                       | 0h       |    |    | 0h                           |

**Table 2-1476. TOP\_CTRL\_TSENSE0\_CNTL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                                          |
|-------|------------------------------|------|-------|--------------------------------------------------------------------------------------|
| 31:25 | RESERVED                     | NONE | 0h    | Reserved                                                                             |
| 24    | TSENSE0_CNTL_MASK_LOW_THRHLD | R/W  | 0h    | mask low threshold comparator output<br>**Note: This bit will only be reset by PORz. |
| 23:21 | RESERVED                     | NONE | 0h    | Reserved                                                                             |
| 20    | TSENSE0_CNTL_MASK_COLD       | R/W  | 1h    | Mask hot comparator output<br>**Note: This bit will only be reset by PORz.           |
| 19:17 | RESERVED                     | NONE | 0h    | Reserved                                                                             |
| 16    | TSENSE0_CNTL_MASK_HOT        | R/W  | 0h    | mask cold comparator output<br>**Note: This bit will only be reset by PORz.          |
| 15:9  | RESERVED                     | NONE | 0h    | Reserved                                                                             |
| 8     | TSENSE0_CNTL_ACCU_CLEAR      | R/W  | 0h    | Accumulator clear<br>**Note: This bit will only be reset by PORz.                    |
| 7:5   | RESERVED                     | NONE | 0h    | Reserved                                                                             |

**Table 2-1476. TOP\_CTRL\_TSENSE0\_CNTL Register Field Descriptions (continued)**

| Bit | Field                        | Type | Reset | Description                                                 |
|-----|------------------------------|------|-------|-------------------------------------------------------------|
| 4   | TSENSE0_CNTL_FIFO_F<br>REEZE | R/W  | 0h    | fifo freeze<br>**Note: This bit will only be reset by PORz. |
| 3:1 | RESERVED                     | NONE | 0h    | Reserved                                                    |
| 0   | TSENSE0_CNTL_FIFO_C<br>LEAR  | R/W  | 0h    | fifo clear<br>**Note: This bit will only be reset by PORz.  |

### 2.3.2.31 TOP\_CTRL\_TSENSE0\_RESULT Register

#### 1 TOP\_CTRL\_TSENSE0\_RESULT Register (Offset = D1Ch) [reset = 0h]

This register shows the most recent temperature readout and status of any ongoing Temperature measurement from Temperature Sensor 0

Return to [Summary Table](#)

**Table 2-1477. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0D1Ch       |

**Figure 2-492. TOP\_CTRL\_TSENSE0\_RESULT Name Register**

|                      |    |    |    |    |    |    |                     |
|----------------------|----|----|----|----|----|----|---------------------|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24                  |
| RESERVED             |    |    |    |    |    |    |                     |
| NONE                 |    |    |    |    |    |    |                     |
| 0h                   |    |    |    |    |    |    |                     |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16                  |
| RESERVED             |    |    |    |    |    |    | TSENSE0_RESULT_ECOZ |
| NONE                 |    |    |    |    |    |    | R                   |
| 0h                   |    |    |    |    |    |    | 0h                  |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8                   |
| RESERVED             |    |    |    |    |    |    |                     |
| NONE                 |    |    |    |    |    |    |                     |
| 0h                   |    |    |    |    |    |    |                     |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0                   |
| TSENSE0_RESULT_DTEMP |    |    |    |    |    |    |                     |
| R                    |    |    |    |    |    |    |                     |
| 0h                   |    |    |    |    |    |    |                     |

**Table 2-1479. TOP\_CTRL\_TSENSE0\_RESULT Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description                                                                                                                    |
|-------|----------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | RESERVED             | NONE | 0h    | Reserved                                                                                                                       |
| 16    | TSENSE0_RESULT_ECOZ  | R    | 0h    | Conversion in Progress.<br>1 : Conversion on going<br>0 : conversion completed<br>**Note: This bit will only be reset by PORz. |
| 15:8  | RESERVED             | NONE | 0h    | Reserved                                                                                                                       |
| 7:0   | TSENSE0_RESULT_DTEMP | R    | 0h    | Temp Code readout<br>**Note: This bit will only be reset by PORz.                                                              |

### 2.3.2.32 TOP\_CTRL\_TSENSE0\_DATA0 Register

#### 1 TOP\_CTRL\_TSENSE0\_DATA0 Register (Offset = D20h) [reset = 0h]

This register shows Temp Sensor 0 result data in FIFO Register 0

Return to [Summary Table](#)

**Table 2-1480. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0D20h       |

**Figure 2-493. TOP\_CTRL\_TSENSE0\_DATA0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TSENSE0_DATA0_TAG  |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TSENSE0_DATA0_TAG  |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TSENSE0_DATA0_TAG  |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TSENSE0_DATA0_DATA |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 2-1482. TOP\_CTRL\_TSENSE0\_DATA0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                        |
|------|--------------------|------|-------|----------------------------------------------------------------------------------------------------|
| 31:8 | TSENSE0_DATA0_TAG  | R    | 0h    | Timestamp for temperature sesnor 0 Data 0 measured<br>**Note: This bit will only be reset by PORz. |
| 7:0  | TSENSE0_DATA0_DATA | R    | 0h    | Temperature Sensor0 FIFO data 0<br>**Note: This bit will only be reset by PORz.                    |

### 2.3.2.33 TOP\_CTRL\_TSENSE0\_DATA1 Register

#### 1 TOP\_CTRL\_TSENSE0\_DATA1 Register (Offset = D24h) [reset = 0h]

This register shows Temp Sensor 0 result data in FIFO Register 1

Return to [Summary Table](#)

**Table 2-1483. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0D24h       |

**Figure 2-494. TOP\_CTRL\_TSENSE0\_DATA1 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TSENSE0_DATA1_TAG  |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TSENSE0_DATA1_TAG  |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TSENSE0_DATA1_TAG  |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TSENSE0_DATA1_DATA |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 2-1485. TOP\_CTRL\_TSENSE0\_DATA1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                        |
|------|--------------------|------|-------|----------------------------------------------------------------------------------------------------|
| 31:8 | TSENSE0_DATA1_TAG  | R    | 0h    | Timestamp for temperature sesnor 0 Data 1 measured<br>**Note: This bit will only be reset by PORz. |
| 7:0  | TSENSE0_DATA1_DATA | R    | 0h    | Temperature Sensor0 FIFO data 1<br>**Note: This bit will only be reset by PORz.                    |

### 2.3.2.34 TOP\_CTRL\_TSENSE0\_DATA2 Register

#### 1 TOP\_CTRL\_TSENSE0\_DATA2 Register (Offset = D28h) [reset = 0h]

This register shows Temp Sensor 0 result data in FIFO Register 2

Return to [Summary Table](#)

**Table 2-1486. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0D28h       |

**Figure 2-495. TOP\_CTRL\_TSENSE0\_DATA2 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TSENSE0_DATA2_TAG  |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TSENSE0_DATA2_TAG  |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TSENSE0_DATA2_TAG  |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TSENSE0_DATA2_DATA |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 2-1488. TOP\_CTRL\_TSENSE0\_DATA2 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                        |
|------|--------------------|------|-------|----------------------------------------------------------------------------------------------------|
| 31:8 | TSENSE0_DATA2_TAG  | R    | 0h    | Timestamp for temperature sesnor 0 Data 2 measured<br>**Note: This bit will only be reset by PORz. |
| 7:0  | TSENSE0_DATA2_DATA | R    | 0h    | Temperature Sensor0 FIFO data 2<br>**Note: This bit will only be reset by PORz.                    |

### 2.3.2.35 TOP\_CTRL\_TSENSE0\_DATA3 Register

#### 1 TOP\_CTRL\_TSENSE0\_DATA3 Register (Offset = D2Ch) [reset = 0h]

This register shows Temp Sensor 0 result data in FIFO Register 3

Return to [Summary Table](#)

**Table 2-1489. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0D2Ch       |

**Figure 2-496. TOP\_CTRL\_TSENSE0\_DATA3 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TSENSE0_DATA3_TAG  |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TSENSE0_DATA3_TAG  |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TSENSE0_DATA3_TAG  |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TSENSE0_DATA3_DATA |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 2-1491. TOP\_CTRL\_TSENSE0\_DATA3 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                        |
|------|--------------------|------|-------|----------------------------------------------------------------------------------------------------|
| 31:8 | TSENSE0_DATA3_TAG  | R    | 0h    | Timestamp for temperature sesnor 0 Data 3 measured<br>**Note: This bit will only be reset by PORz. |
| 7:0  | TSENSE0_DATA3_DATA | R    | 0h    | Temperature Sensor0 FIFO data 3<br>**Note: This bit will only be reset by PORz.                    |



### 2.3.2.36 TOP\_CTRL\_TSENSE0\_ACCU Register

#### 1 TOP\_CTRL\_TSENSE0\_ACCU Register (Offset = D30h) [reset = 0h]

Temp Sensor 0 Result Accumulator Register.

Return to [Summary Table](#)

**Table 2-1492. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0D30h       |

**Figure 2-497. TOP\_CTRL\_TSENSE0\_ACCU Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TSENSE0_ACCU_CUMUL |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TSENSE0_ACCU_CUMUL |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TSENSE0_ACCU_CUMUL |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TSENSE0_ACCU_CUMUL |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 2-1494. TOP\_CTRL\_TSENSE0\_ACCU Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                   |
|------|--------------------|------|-------|-------------------------------------------------------------------------------|
| 31:0 | TSENSE0_ACCU_CUMUL | R    | 0h    | cumulative sum of past DTEMPs<br>**Note: This bit will only be reset by PORz. |

### 2.3.2.37 TOP\_CTRL\_TSENSE1\_TSHUT Register

#### 1 TOP\_CTRL\_TSENSE1\_TSHUT Register (Offset = D40h) [reset = 0h]

This register is used to override the factory specified Tshut temperature with an application specific Tshut temperature for Temperature sensor 1

Return to [Summary Table](#)

**Table 2-1495. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0D40h       |

**Figure 2-498. TOP\_CTRL\_TSENSE1\_TSHUT Name Register**

|                                  |    |    |    |          |    |    |    |
|----------------------------------|----|----|----|----------|----|----|----|
| 31                               | 30 | 29 | 28 | 27       | 26 | 25 | 24 |
| TSENSE1_TSHUT_EFUSE_OVERRIDE     |    |    |    | RESERVED |    |    |    |
| R/W                              |    |    |    | NONE     |    |    |    |
| 0h                               |    |    |    | 0h       |    |    |    |
| 23                               | 22 | 21 | 20 | 19       | 18 | 17 | 16 |
| TSENSE1_TSHUT_TSHUT_THRHLTD_HOT  |    |    |    |          |    |    |    |
| R/W                              |    |    |    |          |    |    |    |
| 0h                               |    |    |    |          |    |    |    |
| 15                               | 14 | 13 | 12 | 11       | 10 | 9  | 8  |
| RESERVED                         |    |    |    |          |    |    |    |
| NONE                             |    |    |    |          |    |    |    |
| 0h                               |    |    |    |          |    |    |    |
| 7                                | 6  | 5  | 4  | 3        | 2  | 1  | 0  |
| TSENSE1_TSHUT_TSHUT_THRSHLD_COLD |    |    |    |          |    |    |    |
| R/W                              |    |    |    |          |    |    |    |
| 0h                               |    |    |    |          |    |    |    |

**Table 2-1497. TOP\_CTRL\_TSENSE1\_TSHUT Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                                                                                                   |
|-------|------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | TSENSE1_TSHUT_EFUSE_OVERRIDE       | R/W  | 0h    | Efuse override<br>000 -- Value from EFUSE is used as tshut hot and tshut cold thresholds<br>111 - Override value takes effect<br>**Note: This bit will only be reset by PORz. |
| 28:24 | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                      |
| 23:16 | TSENSE1_TSHUT_TSHUT_T_THRHLTD_HOT  | R/W  | 0h    | tshut hot threshold. Reads efuse value until overwritten with override = 111<br>**Note: This bit will only be reset by PORz.                                                  |
| 15:8  | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                      |
| 7:0   | TSENSE1_TSHUT_TSHUT_T_THRSHLD_COLD | R/W  | 0h    | tshut cold threshold. Reads efuse value until overwritten with override = 111<br>**Note: This bit will only be reset by PORz.                                                 |

### 2.3.2.38 TOP\_CTRL\_TSENSE1\_ALERT Register

#### 1 TOP\_CTRL\_TSENSE1\_ALERT Register (Offset = D44h) [reset = 0h]

This register is used to configure the temperature thresholds for Temp Sensor 1 for generating Alert Interrupts.

Return to [Summary Table](#)

**Table 2-1498. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0D44h       |

**Figure 2-499. TOP\_CTRL\_TSENSE1\_ALERT Name Register**

|                                 |    |    |    |    |    |    |    |
|---------------------------------|----|----|----|----|----|----|----|
| 31                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 23                              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TSENSE1_ALERT_ALERT_THRHLD_HOT  |    |    |    |    |    |    |    |
| R/W                             |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 15                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 7                               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TSENSE1_ALERT_ALERT_THRHLD_COLD |    |    |    |    |    |    |    |
| R/W                             |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |

**Table 2-1500. TOP\_CTRL\_TSENSE1\_ALERT Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                       |
|-------|---------------------------------|------|-------|-----------------------------------------------------------------------------------|
| 31:24 | RESERVED                        | NONE | 0h    | Reserved                                                                          |
| 23:16 | TSENSE1_ALERT_ALERT_THRHLD_HOT  | R/W  | 0h    | cold threshold/low temp threshold<br>**Note: This bit will only be reset by PORz. |
| 15:8  | RESERVED                        | NONE | 0h    | Reserved                                                                          |
| 7:0   | TSENSE1_ALERT_ALERT_THRHLD_COLD | R/W  | 0h    | Hot threshold/high temp threshold<br>**Note: This bit will only be reset by PORz. |

### 2.3.2.39 TOP\_CTRL\_TSENSE1\_CNTL Register

#### 1 TOP\_CTRL\_TSENSE1\_CNTL Register (Offset = D48h) [reset = 100000h]

This register is used to control and configure Temperature sensor 1

Return to [Summary Table](#)

**Table 2-1501. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0D48h       |

**Figure 2-500. TOP\_CTRL\_TSENSE1\_CNTL Name Register**

|          |    |    |                          |          |    |    |                              |
|----------|----|----|--------------------------|----------|----|----|------------------------------|
| 31       | 30 | 29 | 28                       | 27       | 26 | 25 | 24                           |
| RESERVED |    |    |                          |          |    |    | TSENSE1_CNTL_MASK_LOW_THRHLD |
| NONE     |    |    |                          |          |    |    | R/W                          |
| 0h       |    |    |                          |          |    |    | 0h                           |
| 23       | 22 | 21 | 20                       | 19       | 18 | 17 | 16                           |
| RESERVED |    |    | TSENSE1_CNTL_MASK_COLD   | RESERVED |    |    | TSENSE1_CNTL_MASK_HOT        |
| NONE     |    |    | R/W                      | NONE     |    |    | R/W                          |
| 0h       |    |    | 1h                       | 0h       |    |    | 0h                           |
| 15       | 14 | 13 | 12                       | 11       | 10 | 9  | 8                            |
| RESERVED |    |    |                          |          |    |    | TSENSE1_CNTL_ACCU_CLEAR      |
| NONE     |    |    |                          |          |    |    | R/W                          |
| 0h       |    |    |                          |          |    |    | 0h                           |
| 7        | 6  | 5  | 4                        | 3        | 2  | 1  | 0                            |
| RESERVED |    |    | TSENSE1_CNTL_FIFO_FREEZE | RESERVED |    |    | TSENSE1_CNTL_FIFO_CLEAR      |
| NONE     |    |    | R/W                      | NONE     |    |    | R/W                          |
| 0h       |    |    | 0h                       | 0h       |    |    | 0h                           |

**Table 2-1503. TOP\_CTRL\_TSENSE1\_CNTL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                                          |
|-------|------------------------------|------|-------|--------------------------------------------------------------------------------------|
| 31:25 | RESERVED                     | NONE | 0h    | Reserved                                                                             |
| 24    | TSENSE1_CNTL_MASK_LOW_THRHLD | R/W  | 0h    | mask low threshold comparator output<br>**Note: This bit will only be reset by PORz. |
| 23:21 | RESERVED                     | NONE | 0h    | Reserved                                                                             |
| 20    | TSENSE1_CNTL_MASK_COLD       | R/W  | 1h    | Mask hot comparator output<br>**Note: This bit will only be reset by PORz.           |
| 19:17 | RESERVED                     | NONE | 0h    | Reserved                                                                             |
| 16    | TSENSE1_CNTL_MASK_HOT        | R/W  | 0h    | mask cold comparator output<br>**Note: This bit will only be reset by PORz.          |
| 15:9  | RESERVED                     | NONE | 0h    | Reserved                                                                             |
| 8     | TSENSE1_CNTL_ACCU_CLEAR      | R/W  | 0h    | Accumulator clear<br>**Note: This bit will only be reset by PORz.                    |
| 7:5   | RESERVED                     | NONE | 0h    | Reserved                                                                             |

**Table 2-1503. TOP\_CTRL\_TSENSE1\_CNTL Register Field Descriptions (continued)**

| Bit | Field                    | Type | Reset | Description                                                 |
|-----|--------------------------|------|-------|-------------------------------------------------------------|
| 4   | TSENSE1_CNTL_FIFO_FREEZE | R/W  | 0h    | fifo freeze<br>**Note: This bit will only be reset by PORz. |
| 3:1 | RESERVED                 | NONE | 0h    | Reserved                                                    |
| 0   | TSENSE1_CNTL_FIFO_CLEAR  | R/W  | 0h    | fifo clear<br>**Note: This bit will only be reset by PORz.  |

### 2.3.2.40 TOP\_CTRL\_TSENSE1\_RESULT Register

#### 1 TOP\_CTRL\_TSENSE1\_RESULT Register (Offset = D4Ch) [reset = 0h]

This register shows the most recent temperature readout and status of any ongoing Temperature measurement from Temperature Sensor 1

Return to [Summary Table](#)

**Table 2-1504. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0D4Ch       |

**Figure 2-501. TOP\_CTRL\_TSENSE1\_RESULT Name Register**

|                      |    |    |    |    |    |    |                     |
|----------------------|----|----|----|----|----|----|---------------------|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24                  |
| RESERVED             |    |    |    |    |    |    |                     |
| NONE                 |    |    |    |    |    |    |                     |
| 0h                   |    |    |    |    |    |    |                     |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16                  |
| RESERVED             |    |    |    |    |    |    | TSENSE1_RESULT_ECOZ |
| NONE                 |    |    |    |    |    |    | R                   |
| 0h                   |    |    |    |    |    |    | 0h                  |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8                   |
| RESERVED             |    |    |    |    |    |    |                     |
| NONE                 |    |    |    |    |    |    |                     |
| 0h                   |    |    |    |    |    |    |                     |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0                   |
| TSENSE1_RESULT_DTEMP |    |    |    |    |    |    |                     |
| R                    |    |    |    |    |    |    |                     |
| 0h                   |    |    |    |    |    |    |                     |

**Table 2-1506. TOP\_CTRL\_TSENSE1\_RESULT Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description                                                                                                                    |
|-------|----------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | RESERVED             | NONE | 0h    | Reserved                                                                                                                       |
| 16    | TSENSE1_RESULT_ECOZ  | R    | 0h    | Conversion in Progress.<br>1 : Conversion on going<br>0 : conversion completed<br>**Note: This bit will only be reset by PORz. |
| 15:8  | RESERVED             | NONE | 0h    | Reserved                                                                                                                       |
| 7:0   | TSENSE1_RESULT_DTEMP | R    | 0h    | Temp Code readout<br>**Note: This bit will only be reset by PORz.                                                              |

### 2.3.2.41 TOP\_CTRL\_TSENSE1\_DATA0 Register

#### 1 TOP\_CTRL\_TSENSE1\_DATA0 Register (Offset = D50h) [reset = 0h]

This register shows Temp Sensor 1 result data in FIFO Register 0

Return to [Summary Table](#)

**Table 2-1507. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0D50h       |

**Figure 2-502. TOP\_CTRL\_TSENSE1\_DATA0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TSENSE1_DATA0_TAG  |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TSENSE1_DATA0_TAG  |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TSENSE1_DATA0_TAG  |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TSENSE1_DATA0_DATA |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 2-1509. TOP\_CTRL\_TSENSE1\_DATA0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                        |
|------|--------------------|------|-------|----------------------------------------------------------------------------------------------------|
| 31:8 | TSENSE1_DATA0_TAG  | R    | 0h    | Timestamp for temperature sesnor 1 Data 0 measured<br>**Note: This bit will only be reset by PORz. |
| 7:0  | TSENSE1_DATA0_DATA | R    | 0h    | Temperature sensor 1 FIFO Data 0<br>**Note: This bit will only be reset by PORz.                   |

### 2.3.2.42 TOP\_CTRL\_TSENSE1\_DATA1 Register

#### 1 TOP\_CTRL\_TSENSE1\_DATA1 Register (Offset = D54h) [reset = 0h]

This register shows Temp Sensor 1 result data in FIFO Register 1

Return to [Summary Table](#)

**Table 2-1510. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0D54h       |

**Figure 2-503. TOP\_CTRL\_TSENSE1\_DATA1 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TSENSE1_DATA1_TAG  |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TSENSE1_DATA1_TAG  |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TSENSE1_DATA1_TAG  |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TSENSE1_DATA1_DATA |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 2-1512. TOP\_CTRL\_TSENSE1\_DATA1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                        |
|------|--------------------|------|-------|----------------------------------------------------------------------------------------------------|
| 31:8 | TSENSE1_DATA1_TAG  | R    | 0h    | Timestamp for temperature sesnor 1 Data 1 measured<br>**Note: This bit will only be reset by PORz. |
| 7:0  | TSENSE1_DATA1_DATA | R    | 0h    | Temperature sensor 1 FIFO Data 1<br>**Note: This bit will only be reset by PORz.                   |



### 2.3.2.43 TOP\_CTRL\_TSENSE1\_DATA2 Register

#### 1 TOP\_CTRL\_TSENSE1\_DATA2 Register (Offset = D58h) [reset = 0h]

This register shows Temp Sensor 1 result data in FIFO Register 2

Return to [Summary Table](#)

**Table 2-1513. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0D58h       |

**Figure 2-504. TOP\_CTRL\_TSENSE1\_DATA2 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TSENSE1_DATA2_TAG  |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TSENSE1_DATA2_TAG  |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TSENSE1_DATA2_TAG  |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TSENSE1_DATA2_DATA |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 2-1515. TOP\_CTRL\_TSENSE1\_DATA2 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                        |
|------|--------------------|------|-------|----------------------------------------------------------------------------------------------------|
| 31:8 | TSENSE1_DATA2_TAG  | R    | 0h    | Timestamp for temperature sesnor 1 Data 2 measured<br>**Note: This bit will only be reset by PORz. |
| 7:0  | TSENSE1_DATA2_DATA | R    | 0h    | Temperature sensor 1 FIFO Data 2<br>**Note: This bit will only be reset by PORz.                   |

### 2.3.2.44 TOP\_CTRL\_TSENSE1\_DATA3 Register

#### 1 TOP\_CTRL\_TSENSE1\_DATA3 Register (Offset = D5Ch) [reset = 0h]

This register shows Temp Sensor 1 result data in FIFO Register 3

Return to [Summary Table](#)

**Table 2-1516. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0D5Ch       |

**Figure 2-505. TOP\_CTRL\_TSENSE1\_DATA3 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TSENSE1_DATA3_TAG  |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TSENSE1_DATA3_TAG  |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TSENSE1_DATA3_TAG  |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TSENSE1_DATA3_DATA |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 2-1518. TOP\_CTRL\_TSENSE1\_DATA3 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                        |
|------|--------------------|------|-------|----------------------------------------------------------------------------------------------------|
| 31:8 | TSENSE1_DATA3_TAG  | R    | 0h    | Timestamp for temperature sesnor 1 Data 3 measured<br>**Note: This bit will only be reset by PORz. |
| 7:0  | TSENSE1_DATA3_DATA | R    | 0h    | Temperature sensor 1 FIFO Data 3<br>**Note: This bit will only be reset by PORz.                   |

### 2.3.2.45 TOP\_CTRL\_TSENSE1\_ACCU Register

#### 1 TOP\_CTRL\_TSENSE1\_ACCU Register (Offset = D60h) [reset = 0h]

Temp Sensor 1 Result Accumulator Register.

Return to [Summary Table](#)

**Table 2-1519. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0D60h       |

**Figure 2-506. TOP\_CTRL\_TSENSE1\_ACCU Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TSENSE1_ACCU_CUMUL |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TSENSE1_ACCU_CUMUL |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TSENSE1_ACCU_CUMUL |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TSENSE1_ACCU_CUMUL |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 2-1521. TOP\_CTRL\_TSENSE1\_ACCU Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                   |
|------|--------------------|------|-------|-------------------------------------------------------------------------------|
| 31:0 | TSENSE1_ACCU_CUMUL | R    | 0h    | cumulative sum of past DTEMPs<br>**Note: This bit will only be reset by PORz. |

### 2.3.2.46 TOP\_CTRL\_TSENSE2\_RESULT Register

#### 1 TOP\_CTRL\_TSENSE2\_RESULT Register (Offset = D7Ch) [reset = 0h]

This register shows the most recent temperature readout and status of any ongoing Temperature measurement from Temperature Sensor 2

Return to [Summary Table](#)

**Table 2-1522. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0D7Ch       |

**Figure 2-507. TOP\_CTRL\_TSENSE2\_RESULT Name Register**

|                      |    |    |    |    |    |    |                     |
|----------------------|----|----|----|----|----|----|---------------------|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24                  |
| RESERVED             |    |    |    |    |    |    |                     |
| NONE                 |    |    |    |    |    |    |                     |
| 0h                   |    |    |    |    |    |    |                     |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16                  |
| RESERVED             |    |    |    |    |    |    | TSENSE2_RESULT_ECOZ |
| NONE                 |    |    |    |    |    |    | R                   |
| 0h                   |    |    |    |    |    |    | 0h                  |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8                   |
| RESERVED             |    |    |    |    |    |    |                     |
| NONE                 |    |    |    |    |    |    |                     |
| 0h                   |    |    |    |    |    |    |                     |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0                   |
| TSENSE2_RESULT_DTEMP |    |    |    |    |    |    |                     |
| R                    |    |    |    |    |    |    |                     |
| 0h                   |    |    |    |    |    |    |                     |

**Table 2-1524. TOP\_CTRL\_TSENSE2\_RESULT Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description                                                                                                                    |
|-------|----------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | RESERVED             | NONE | 0h    | Reserved                                                                                                                       |
| 16    | TSENSE2_RESULT_ECOZ  | R    | 0h    | Conversion in Progress.<br>1 : Conversion on going<br>0 : conversion completed<br>**Note: This bit will only be reset by PORz. |
| 15:8  | RESERVED             | NONE | 0h    | Reserved                                                                                                                       |
| 7:0   | TSENSE2_RESULT_DTEMP | R    | 0h    | Temp Code readout<br>**Note: This bit will only be reset by PORz.                                                              |

### 2.3.2.47 TOP\_CTRL\_TSENSE3\_RESULT Register

#### 1 TOP\_CTRL\_TSENSE3\_RESULT Register (Offset = DACH) [reset = 0h]

This register shows the most recent temperature readout and status of any ongoing Temperature measurement from Temperature Sensor 3

Return to [Summary Table](#)

**Table 2-1525. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0DACH       |

**Figure 2-508. TOP\_CTRL\_TSENSE3\_RESULT Name Register**

|                      |    |    |    |    |    |    |                     |
|----------------------|----|----|----|----|----|----|---------------------|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24                  |
| RESERVED             |    |    |    |    |    |    |                     |
| NONE                 |    |    |    |    |    |    |                     |
| 0h                   |    |    |    |    |    |    |                     |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16                  |
| RESERVED             |    |    |    |    |    |    | TSENSE3_RESULT_ECOZ |
| NONE                 |    |    |    |    |    |    | R                   |
| 0h                   |    |    |    |    |    |    | 0h                  |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8                   |
| RESERVED             |    |    |    |    |    |    |                     |
| NONE                 |    |    |    |    |    |    |                     |
| 0h                   |    |    |    |    |    |    |                     |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0                   |
| TSENSE3_RESULT_DTEMP |    |    |    |    |    |    |                     |
| R                    |    |    |    |    |    |    |                     |
| 0h                   |    |    |    |    |    |    |                     |

**Table 2-1527. TOP\_CTRL\_TSENSE3\_RESULT Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description                                                                                                                    |
|-------|----------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | RESERVED             | NONE | 0h    | Reserved                                                                                                                       |
| 16    | TSENSE3_RESULT_ECOZ  | R    | 0h    | Conversion in Progress.<br>1 : Conversion on going<br>0 : conversion completed<br>**Note: This bit will only be reset by PORz. |
| 15:8  | RESERVED             | NONE | 0h    | Reserved                                                                                                                       |
| 7:0   | TSENSE3_RESULT_DTEMP | R    | 0h    | Temp Code readout<br>**Note: This bit will only be reset by PORz.                                                              |

### 2.3.2.48 TOP\_CTRL\_HW\_SPARE\_RW0 Register

#### 1 TOP\_CTRL\_HW\_SPARE\_RW0 Register (Offset = FD0h) [reset = 0h]

Return to [Summary Table](#)

**Table 2-1528. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0FD0h       |

**Figure 2-509. TOP\_CTRL\_HW\_SPARE\_RW0 Name Register**

|                           |    |    |    |    |    |    |    |
|---------------------------|----|----|----|----|----|----|----|
| 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HW_SPARE_RW0_HW_SPARE_RW0 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 23                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HW_SPARE_RW0_HW_SPARE_RW0 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 15                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HW_SPARE_RW0_HW_SPARE_RW0 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 7                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HW_SPARE_RW0_HW_SPARE_RW0 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |

**Table 2-1530. TOP\_CTRL\_HW\_SPARE\_RW0 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description         |
|------|---------------------------|------|-------|---------------------|
| 31:0 | HW_SPARE_RW0_HW_SPARE_RW0 | R/W  | 0h    | Reserved for HW R&D |

### 2.3.2.49 TOP\_CTRL\_HW\_SPARE\_RW1 Register

1 TOP\_CTRL\_HW\_SPARE\_RW1 Register (Offset = FD4h) [reset = 0h]

Return to [Summary Table](#)

**Table 2-1531. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0FD4h       |

**Figure 2-510. TOP\_CTRL\_HW\_SPARE\_RW1 Name Register**

|                           |    |    |    |    |    |    |    |
|---------------------------|----|----|----|----|----|----|----|
| 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HW_SPARE_RW1_HW_SPARE_RW1 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 23                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HW_SPARE_RW1_HW_SPARE_RW1 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 15                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HW_SPARE_RW1_HW_SPARE_RW1 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 7                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HW_SPARE_RW1_HW_SPARE_RW1 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |

**Table 2-1533. TOP\_CTRL\_HW\_SPARE\_RW1 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description         |
|------|---------------------------|------|-------|---------------------|
| 31:0 | HW_SPARE_RW1_HW_SPARE_RW1 | R/W  | 0h    | Reserved for HW R&D |

### 2.3.2.50 TOP\_CTRL\_HW\_SPARE\_RW2 Register

1 TOP\_CTRL\_HW\_SPARE\_RW2 Register (Offset = FD8h) [reset = 0h]

Return to [Summary Table](#)

**Table 2-1534. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0FD8h       |

**Figure 2-511. TOP\_CTRL\_HW\_SPARE\_RW2 Name Register**

|                           |    |    |    |    |    |    |    |
|---------------------------|----|----|----|----|----|----|----|
| 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HW_SPARE_RW2_HW_SPARE_RW2 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 23                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HW_SPARE_RW2_HW_SPARE_RW2 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 15                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HW_SPARE_RW2_HW_SPARE_RW2 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 7                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HW_SPARE_RW2_HW_SPARE_RW2 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |

**Table 2-1536. TOP\_CTRL\_HW\_SPARE\_RW2 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description         |
|------|---------------------------|------|-------|---------------------|
| 31:0 | HW_SPARE_RW2_HW_SPARE_RW2 | R/W  | 0h    | Reserved for HW R&D |



### 2.3.2.51 TOP\_CTRL\_HW\_SPARE\_RW3 Register

#### 1 TOP\_CTRL\_HW\_SPARE\_RW3 Register (Offset = FDCh) [reset = 0h]

Return to [Summary Table](#)

**Table 2-1537. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0FDCh       |

**Figure 2-512. TOP\_CTRL\_HW\_SPARE\_RW3 Name Register**

|                           |    |    |    |    |    |    |    |
|---------------------------|----|----|----|----|----|----|----|
| 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HW_SPARE_RW3_HW_SPARE_RW3 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 23                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HW_SPARE_RW3_HW_SPARE_RW3 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 15                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HW_SPARE_RW3_HW_SPARE_RW3 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 7                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HW_SPARE_RW3_HW_SPARE_RW3 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |

**Table 2-1539. TOP\_CTRL\_HW\_SPARE\_RW3 Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description         |
|------|-------------------------------|------|-------|---------------------|
| 31:0 | HW_SPARE_RW3_HW_S<br>PARE_RW3 | R/W  | 0h    | Reserved for HW R&D |

### 2.3.2.52 TOP\_CTRL\_HW\_SPARE\_RO0 Register

1 TOP\_CTRL\_HW\_SPARE\_RO0 Register (Offset = FE0h) [reset = 0h]

Return to [Summary Table](#)

**Table 2-1540. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0FE0h       |

**Figure 2-513. TOP\_CTRL\_HW\_SPARE\_RO0 Name Register**

|                           |    |    |    |    |    |    |    |
|---------------------------|----|----|----|----|----|----|----|
| 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HW_SPARE_RO0_HW_SPARE_RO0 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 23                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HW_SPARE_RO0_HW_SPARE_RO0 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 15                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HW_SPARE_RO0_HW_SPARE_RO0 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 7                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HW_SPARE_RO0_HW_SPARE_RO0 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |

**Table 2-1542. TOP\_CTRL\_HW\_SPARE\_RO0 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description         |
|------|---------------------------|------|-------|---------------------|
| 31:0 | HW_SPARE_RO0_HW_SPARE_RO0 | R    | 0h    | Reserved for HW R&D |

### 2.3.2.53 TOP\_CTRL\_HW\_SPARE\_RO1 Register

1 TOP\_CTRL\_HW\_SPARE\_RO1 Register (Offset = FE4h) [reset = 0h]

Return to [Summary Table](#)

**Table 2-1543. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0FE4h       |

**Figure 2-514. TOP\_CTRL\_HW\_SPARE\_RO1 Name Register**

|                           |    |    |    |    |    |    |    |
|---------------------------|----|----|----|----|----|----|----|
| 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HW_SPARE_RO1_HW_SPARE_RO1 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 23                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HW_SPARE_RO1_HW_SPARE_RO1 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 15                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HW_SPARE_RO1_HW_SPARE_RO1 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 7                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HW_SPARE_RO1_HW_SPARE_RO1 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |

**Table 2-1545. TOP\_CTRL\_HW\_SPARE\_RO1 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description         |
|------|---------------------------|------|-------|---------------------|
| 31:0 | HW_SPARE_RO1_HW_SPARE_RO1 | R    | 0h    | Reserved for HW R&D |

### 2.3.2.54 TOP\_CTRL\_HW\_SPARE\_RO2 Register

1 TOP\_CTRL\_HW\_SPARE\_RO2 Register (Offset = FE8h) [reset = 0h]

Return to [Summary Table](#)

**Table 2-1546. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0FE8h       |

**Figure 2-515. TOP\_CTRL\_HW\_SPARE\_RO2 Name Register**

|                           |    |    |    |    |    |    |    |
|---------------------------|----|----|----|----|----|----|----|
| 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HW_SPARE_RO2_HW_SPARE_RO2 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 23                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HW_SPARE_RO2_HW_SPARE_RO2 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 15                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HW_SPARE_RO2_HW_SPARE_RO2 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 7                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HW_SPARE_RO2_HW_SPARE_RO2 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |

**Table 2-1548. TOP\_CTRL\_HW\_SPARE\_RO2 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description         |
|------|---------------------------|------|-------|---------------------|
| 31:0 | HW_SPARE_RO2_HW_SPARE_RO2 | R    | 0h    | Reserved for HW R&D |

### 2.3.2.55 TOP\_CTRL\_HW\_SPARE\_RO3 Register

1 TOP\_CTRL\_HW\_SPARE\_RO3 Register (Offset = FECh) [reset = 0h]

Return to [Summary Table](#)

**Table 2-1549. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0FECh       |

**Figure 2-516. TOP\_CTRL\_HW\_SPARE\_RO3 Name Register**

|                           |    |    |    |    |    |    |    |
|---------------------------|----|----|----|----|----|----|----|
| 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HW_SPARE_RO3_HW_SPARE_RO3 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 23                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HW_SPARE_RO3_HW_SPARE_RO3 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 15                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HW_SPARE_RO3_HW_SPARE_RO3 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 7                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HW_SPARE_RO3_HW_SPARE_RO3 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |

**Table 2-1551. TOP\_CTRL\_HW\_SPARE\_RO3 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description         |
|------|---------------------------|------|-------|---------------------|
| 31:0 | HW_SPARE_RO3_HW_SPARE_RO3 | R    | 0h    | Reserved for HW R&D |

### 2.3.2.56 TOP\_CTRL\_HW\_SPARE\_WPH Register

#### 1 TOP\_CTRL\_HW\_SPARE\_WPH Register (Offset = FF0h) [reset = 0h]

Return to [Summary Table](#)

**Table 2-1552. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0FF0h       |

**Figure 2-517. TOP\_CTRL\_HW\_SPARE\_WPH Name Register**

|                           |    |    |    |    |    |    |    |
|---------------------------|----|----|----|----|----|----|----|
| 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HW_SPARE_WPH_HW_SPARE_WPH |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 23                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HW_SPARE_WPH_HW_SPARE_WPH |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 15                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HW_SPARE_WPH_HW_SPARE_WPH |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 7                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HW_SPARE_WPH_HW_SPARE_WPH |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |

**Table 2-1554. TOP\_CTRL\_HW\_SPARE\_WPH Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description         |
|------|---------------------------|------|-------|---------------------|
| 31:0 | HW_SPARE_WPH_HW_SPARE_WPH | R/W  | 0h    | Reserved for HW R&D |

### 2.3.2.57 TOP\_CTRL\_HW\_SPARE\_REC Register

#### 1 TOP\_CTRL\_HW\_SPARE\_REC Register (Offset = FF4h) [reset = 0h]

Return to [Summary Table](#)

**Table 2-1555. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 0FF4h       |

**Figure 2-518. TOP\_CTRL\_HW\_SPARE\_REC Name Register**

| 31                                  | 30                                  | 29                                  | 28                                  | 27                                  | 26                                  | 25                                  | 24                                  |
|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|
| HW_SPARE_R<br>EC_HW_SPAR<br>E_REC31 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC30 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC29 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC28 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC27 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC26 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC25 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC24 |
| R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 |
| 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  |
| 23                                  | 22                                  | 21                                  | 20                                  | 19                                  | 18                                  | 17                                  | 16                                  |
| HW_SPARE_R<br>EC_HW_SPAR<br>E_REC23 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC22 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC21 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC20 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC19 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC18 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC17 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC16 |
| R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 |
| 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  |
| 15                                  | 14                                  | 13                                  | 12                                  | 11                                  | 10                                  | 9                                   | 8                                   |
| HW_SPARE_R<br>EC_HW_SPAR<br>E_REC15 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC14 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC13 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC12 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC11 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC10 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC9  | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC8  |
| R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 |
| 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  |
| 7                                   | 6                                   | 5                                   | 4                                   | 3                                   | 2                                   | 1                                   | 0                                   |
| HW_SPARE_R<br>EC_HW_SPAR<br>E_REC7  | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC6  | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC5  | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC4  | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC3  | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC2  | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC1  | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC0  |
| R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 |
| 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  |

**Table 2-1557. TOP\_CTRL\_HW\_SPARE\_REC Register Field Descriptions**

| Bit | Field                           | Type | Reset | Description         |
|-----|---------------------------------|------|-------|---------------------|
| 31  | HW_SPARE_REC_HW_S<br>PARE_REC31 | R/W  | 0h    | Reserved for HW R&D |
| 30  | HW_SPARE_REC_HW_S<br>PARE_REC30 | R/W  | 0h    | Reserved for HW R&D |
| 29  | HW_SPARE_REC_HW_S<br>PARE_REC29 | R/W  | 0h    | Reserved for HW R&D |
| 28  | HW_SPARE_REC_HW_S<br>PARE_REC28 | R/W  | 0h    | Reserved for HW R&D |
| 27  | HW_SPARE_REC_HW_S<br>PARE_REC27 | R/W  | 0h    | Reserved for HW R&D |
| 26  | HW_SPARE_REC_HW_S<br>PARE_REC26 | R/W  | 0h    | Reserved for HW R&D |
| 25  | HW_SPARE_REC_HW_S<br>PARE_REC25 | R/W  | 0h    | Reserved for HW R&D |
| 24  | HW_SPARE_REC_HW_S<br>PARE_REC24 | R/W  | 0h    | Reserved for HW R&D |

**Table 2-1557. TOP\_CTRL\_HW\_SPARE\_REC Register Field Descriptions (continued)**

| Bit | Field                           | Type | Reset | Description         |
|-----|---------------------------------|------|-------|---------------------|
| 23  | HW_SPARE_REC_HW_S<br>PARE_REC23 | R/W  | 0h    | Reserved for HW R&D |
| 22  | HW_SPARE_REC_HW_S<br>PARE_REC22 | R/W  | 0h    | Reserved for HW R&D |
| 21  | HW_SPARE_REC_HW_S<br>PARE_REC21 | R/W  | 0h    | Reserved for HW R&D |
| 20  | HW_SPARE_REC_HW_S<br>PARE_REC20 | R/W  | 0h    | Reserved for HW R&D |
| 19  | HW_SPARE_REC_HW_S<br>PARE_REC19 | R/W  | 0h    | Reserved for HW R&D |
| 18  | HW_SPARE_REC_HW_S<br>PARE_REC18 | R/W  | 0h    | Reserved for HW R&D |
| 17  | HW_SPARE_REC_HW_S<br>PARE_REC17 | R/W  | 0h    | Reserved for HW R&D |
| 16  | HW_SPARE_REC_HW_S<br>PARE_REC16 | R/W  | 0h    | Reserved for HW R&D |
| 15  | HW_SPARE_REC_HW_S<br>PARE_REC15 | R/W  | 0h    | Reserved for HW R&D |
| 14  | HW_SPARE_REC_HW_S<br>PARE_REC14 | R/W  | 0h    | Reserved for HW R&D |
| 13  | HW_SPARE_REC_HW_S<br>PARE_REC13 | R/W  | 0h    | Reserved for HW R&D |
| 12  | HW_SPARE_REC_HW_S<br>PARE_REC12 | R/W  | 0h    | Reserved for HW R&D |
| 11  | HW_SPARE_REC_HW_S<br>PARE_REC11 | R/W  | 0h    | Reserved for HW R&D |
| 10  | HW_SPARE_REC_HW_S<br>PARE_REC10 | R/W  | 0h    | Reserved for HW R&D |
| 9   | HW_SPARE_REC_HW_S<br>PARE_REC9  | R/W  | 0h    | Reserved for HW R&D |
| 8   | HW_SPARE_REC_HW_S<br>PARE_REC8  | R/W  | 0h    | Reserved for HW R&D |
| 7   | HW_SPARE_REC_HW_S<br>PARE_REC7  | R/W  | 0h    | Reserved for HW R&D |
| 6   | HW_SPARE_REC_HW_S<br>PARE_REC6  | R/W  | 0h    | Reserved for HW R&D |
| 5   | HW_SPARE_REC_HW_S<br>PARE_REC5  | R/W  | 0h    | Reserved for HW R&D |
| 4   | HW_SPARE_REC_HW_S<br>PARE_REC4  | R/W  | 0h    | Reserved for HW R&D |
| 3   | HW_SPARE_REC_HW_S<br>PARE_REC3  | R/W  | 0h    | Reserved for HW R&D |
| 2   | HW_SPARE_REC_HW_S<br>PARE_REC2  | R/W  | 0h    | Reserved for HW R&D |
| 1   | HW_SPARE_REC_HW_S<br>PARE_REC1  | R/W  | 0h    | Reserved for HW R&D |
| 0   | HW_SPARE_REC_HW_S<br>PARE_REC0  | R/W  | 0h    | Reserved for HW R&D |



### 2.3.2.58 TOP\_CTRL\_LOCK0\_KICK0 Register

#### 1 TOP\_CTRL\_LOCK0\_KICK0 Register (Offset = 1008h) [reset = 0h]

- KICK0 component.

Return to [Summary Table](#)

**Table 2-1558. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 1008h       |

**Figure 2-519. TOP\_CTRL\_LOCK0\_KICK0 Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| LOCK0_KICK0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LOCK0_KICK0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| LOCK0_KICK0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LOCK0_KICK0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 2-1560. TOP\_CTRL\_LOCK0\_KICK0 Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description       |
|------|-------------|------|-------|-------------------|
| 31:0 | LOCK0_KICK0 | R/W  | 0h    | - KICK0 component |

### 2.3.2.59 TOP\_CTRL\_LOCK0\_KICK1 Register

#### 1 TOP\_CTRL\_LOCK0\_KICK1 Register (Offset = 100Ch) [reset = 0h]

- KICK1 component.

Return to [Summary Table](#)

**Table 2-1561. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 100Ch       |

**Figure 2-520. TOP\_CTRL\_LOCK0\_KICK1 Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| LOCK0_KICK1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LOCK0_KICK1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| LOCK0_KICK1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LOCK0_KICK1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 2-1563. TOP\_CTRL\_LOCK0\_KICK1 Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description       |
|------|-------------|------|-------|-------------------|
| 31:0 | LOCK0_KICK1 | R/W  | 0h    | - KICK1 component |

### 2.3.2.60 TOP\_CTRL\_INTR\_RAW\_STATUS Register

#### 1 TOP\_CTRL\_INTR\_RAW\_STATUS Register (Offset = 1010h) [reset = 0h]

Interrupt Raw Status/Set Register.

Return to [Summary Table](#)

**Table 2-1564. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 1010h       |

**Figure 2-521. TOP\_CTRL\_INTR\_RAW\_STATUS Name Register**

|          |    |    |    |           |          |          |          |
|----------|----|----|----|-----------|----------|----------|----------|
| 31       | 30 | 29 | 28 | 27        | 26       | 25       | 24       |
| RESERVED |    |    |    |           |          |          |          |
| NONE     |    |    |    |           |          |          |          |
| 0h       |    |    |    |           |          |          |          |
| 23       | 22 | 21 | 20 | 19        | 18       | 17       | 16       |
| RESERVED |    |    |    |           |          |          |          |
| NONE     |    |    |    |           |          |          |          |
| 0h       |    |    |    |           |          |          |          |
| 15       | 14 | 13 | 12 | 11        | 10       | 9        | 8        |
| RESERVED |    |    |    |           |          |          |          |
| NONE     |    |    |    |           |          |          |          |
| 0h       |    |    |    |           |          |          |          |
| 7        | 6  | 5  | 4  | 3         | 2        | 1        | 0        |
| RESERVED |    |    |    | PROXY_ERR | KICK_ERR | ADDR_ERR | PROT_ERR |
| NONE     |    |    |    | R/W1TS    | R/W1TS   | R/W1TS   | R/W1TS   |
| 0h       |    |    |    | 0h        | 0h       | 0h       | 0h       |

**Table 2-1566. TOP\_CTRL\_INTR\_RAW\_STATUS Register Field Descriptions**

| Bit  | Field     | Type   | Reset | Description                                                                                                |
|------|-----------|--------|-------|------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED  | NONE   | 0h    | Reserved                                                                                                   |
| 3    | PROXY_ERR | R/W1TS | 0h    | Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. |
| 2    | KICK_ERR  | R/W1TS | 0h    | Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.   |
| 1    | ADDR_ERR  | R/W1TS | 0h    | Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.    |
| 0    | PROT_ERR  | R/W1TS | 0h    | Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.    |

### 2.3.2.61 TOP\_CTRL\_INTR\_ENABLED\_STATUS\_CLEAR Register

#### 1 TOP\_CTRL\_INTR\_ENABLED\_STATUS\_CLEAR Register (Offset = 1014h) [reset = 0h]

Interrupt Enabled Status/Clear register.

Return to [Summary Table](#)

**Table 2-1567. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 1014h       |

**Figure 2-522. TOP\_CTRL\_INTR\_ENABLED\_STATUS\_CLEAR Name Register**

|          |    |    |    |                   |                  |                  |                  |
|----------|----|----|----|-------------------|------------------|------------------|------------------|
| 31       | 30 | 29 | 28 | 27                | 26               | 25               | 24               |
| RESERVED |    |    |    |                   |                  |                  |                  |
| NONE     |    |    |    |                   |                  |                  |                  |
| 0h       |    |    |    |                   |                  |                  |                  |
| 23       | 22 | 21 | 20 | 19                | 18               | 17               | 16               |
| RESERVED |    |    |    |                   |                  |                  |                  |
| NONE     |    |    |    |                   |                  |                  |                  |
| 0h       |    |    |    |                   |                  |                  |                  |
| 15       | 14 | 13 | 12 | 11                | 10               | 9                | 8                |
| RESERVED |    |    |    |                   |                  |                  |                  |
| NONE     |    |    |    |                   |                  |                  |                  |
| 0h       |    |    |    |                   |                  |                  |                  |
| 7        | 6  | 5  | 4  | 3                 | 2                | 1                | 0                |
| RESERVED |    |    |    | ENABLED_PROXY_ERR | ENABLED_KICK_ERR | ENABLED_ADDR_ERR | ENABLED_PROT_ERR |
| NONE     |    |    |    | R/W1TC            | R/W1TC           | R/W1TC           | R/W1TC           |
| 0h       |    |    |    | 0h                | 0h               | 0h               | 0h               |

**Table 2-1569. TOP\_CTRL\_INTR\_ENABLED\_STATUS\_CLEAR Register Field Descriptions**

| Bit  | Field             | Type   | Reset | Description                                                                                                      |
|------|-------------------|--------|-------|------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED          | NONE   | 0h    | Reserved                                                                                                         |
| 3    | ENABLED_PROXY_ERR | R/W1TC | 0h    | Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. |
| 2    | ENABLED_KICK_ERR  | R/W1TC | 0h    | Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.   |
| 1    | ENABLED_ADDR_ERR  | R/W1TC | 0h    | Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.    |
| 0    | ENABLED_PROT_ERR  | R/W1TC | 0h    | Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.    |

### 2.3.2.62 TOP\_CTRL\_INTR\_ENABLE Register

#### 1 TOP\_CTRL\_INTR\_ENABLE Register (Offset = 1018h) [reset = 0h]

Interrupt Enable register.

Return to [Summary Table](#)

**Table 2-1570. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 1018h       |

**Figure 2-523. TOP\_CTRL\_INTR\_ENABLE Name Register**

|          |    |    |    |              |             |             |             |
|----------|----|----|----|--------------|-------------|-------------|-------------|
| 31       | 30 | 29 | 28 | 27           | 26          | 25          | 24          |
| RESERVED |    |    |    |              |             |             |             |
| NONE     |    |    |    |              |             |             |             |
| 0h       |    |    |    |              |             |             |             |
| 23       | 22 | 21 | 20 | 19           | 18          | 17          | 16          |
| RESERVED |    |    |    |              |             |             |             |
| NONE     |    |    |    |              |             |             |             |
| 0h       |    |    |    |              |             |             |             |
| 15       | 14 | 13 | 12 | 11           | 10          | 9           | 8           |
| RESERVED |    |    |    |              |             |             |             |
| NONE     |    |    |    |              |             |             |             |
| 0h       |    |    |    |              |             |             |             |
| 7        | 6  | 5  | 4  | 3            | 2           | 1           | 0           |
| RESERVED |    |    |    | PROXY_ERR_EN | KICK_ERR_EN | ADDR_ERR_EN | PROT_ERR_EN |
| NONE     |    |    |    | R/W1TS       | R/W1TS      | R/W1TS      | R/W1TS      |
| 0h       |    |    |    | 0h           | 0h          | 0h          | 0h          |

**Table 2-1572. TOP\_CTRL\_INTR\_ENABLE Register Field Descriptions**

| Bit  | Field        | Type   | Reset | Description                                                                                   |
|------|--------------|--------|-------|-----------------------------------------------------------------------------------------------|
| 31:4 | RESERVED     | NONE   | 0h    | Reserved                                                                                      |
| 3    | PROXY_ERR_EN | R/W1TS | 0h    | Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. |
| 2    | KICK_ERR_EN  | R/W1TS | 0h    | Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.   |
| 1    | ADDR_ERR_EN  | R/W1TS | 0h    | Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.    |
| 0    | PROT_ERR_EN  | R/W1TS | 0h    | Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.    |

### 2.3.2.63 TOP\_CTRL\_INTR\_ENABLE\_CLEAR Register

#### 1 TOP\_CTRL\_INTR\_ENABLE\_CLEAR Register (Offset = 101Ch) [reset = 0h]

Interrupt Enable Clear register.

Return to [Summary Table](#)

**Table 2-1573. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 101Ch       |

**Figure 2-524. TOP\_CTRL\_INTR\_ENABLE\_CLEAR Name Register**

|          |    |    |    |                  |                 |                 |                 |
|----------|----|----|----|------------------|-----------------|-----------------|-----------------|
| 31       | 30 | 29 | 28 | 27               | 26              | 25              | 24              |
| RESERVED |    |    |    |                  |                 |                 |                 |
| NONE     |    |    |    |                  |                 |                 |                 |
| 0h       |    |    |    |                  |                 |                 |                 |
| 23       | 22 | 21 | 20 | 19               | 18              | 17              | 16              |
| RESERVED |    |    |    |                  |                 |                 |                 |
| NONE     |    |    |    |                  |                 |                 |                 |
| 0h       |    |    |    |                  |                 |                 |                 |
| 15       | 14 | 13 | 12 | 11               | 10              | 9               | 8               |
| RESERVED |    |    |    |                  |                 |                 |                 |
| NONE     |    |    |    |                  |                 |                 |                 |
| 0h       |    |    |    |                  |                 |                 |                 |
| 7        | 6  | 5  | 4  | 3                | 2               | 1               | 0               |
| RESERVED |    |    |    | PROXY_ERR_EN_CLR | KICK_ERR_EN_CLR | ADDR_ERR_EN_CLR | PROT_ERR_EN_CLR |
| NONE     |    |    |    | R/W1TC           | R/W1TC          | R/W1TC          | R/W1TC          |
| 0h       |    |    |    | 0h               | 0h              | 0h              | 0h              |

**Table 2-1575. TOP\_CTRL\_INTR\_ENABLE\_CLEAR Register Field Descriptions**

| Bit  | Field            | Type   | Reset | Description                                                                                           |
|------|------------------|--------|-------|-------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED         | NONE   | 0h    | Reserved                                                                                              |
| 3    | PROXY_ERR_EN_CLR | R/W1TC | 0h    | Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. |
| 2    | KICK_ERR_EN_CLR  | R/W1TC | 0h    | Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.   |
| 1    | ADDR_ERR_EN_CLR  | R/W1TC | 0h    | Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.    |
| 0    | PROT_ERR_EN_CLR  | R/W1TC | 0h    | Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.    |

### 2.3.2.64 TOP\_CTRL\_EOI Register

#### 1 TOP\_CTRL\_EOI Register (Offset = 1020h) [reset = 0h]

EOI register.

Return to [Summary Table](#)

**Table 2-1576. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 1020h       |

**Figure 2-525. TOP\_CTRL\_EOI Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| EOI_VECTOR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 2-1578. TOP\_CTRL\_EOI Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                 |
|------|------------|------|-------|-----------------------------------------------------------------------------|
| 31:8 | RESERVED   | NONE | 0h    | Reserved                                                                    |
| 7:0  | EOI_VECTOR | R/W  | 0h    | EOI vector value. Write this with interrupt distribution value in the chip. |

### 2.3.2.65 TOP\_CTRL\_FAULT\_ADDRESS Register

#### 1 TOP\_CTRL\_FAULT\_ADDRESS Register (Offset = 1024h) [reset = 0h]

Fault Address register.

Return to [Summary Table](#)

**Table 2-1579. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 1024h       |

**Figure 2-526. TOP\_CTRL\_FAULT\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 2-1581. TOP\_CTRL\_FAULT\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description    |
|------|------------|------|-------|----------------|
| 31:0 | FAULT_ADDR | R    | 0h    | Fault Address. |



### 2.3.2.66 TOP\_CTRL\_FAULT\_TYPE\_STATUS Register

#### 1 TOP\_CTRL\_FAULT\_TYPE\_STATUS Register (Offset = 1028h) [reset = 0h]

Fault Type Status register.

Return to [Summary Table](#)

**Table 2-1582. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 1028h       |

**Figure 2-527. TOP\_CTRL\_FAULT\_TYPE\_STATUS Name Register**

|          |          |            |    |    |    |    |    |
|----------|----------|------------|----|----|----|----|----|
| 31       | 30       | 29         | 28 | 27 | 26 | 25 | 24 |
| RESERVED |          |            |    |    |    |    |    |
| NONE     |          |            |    |    |    |    |    |
| 0h       |          |            |    |    |    |    |    |
| 23       | 22       | 21         | 20 | 19 | 18 | 17 | 16 |
| RESERVED |          |            |    |    |    |    |    |
| NONE     |          |            |    |    |    |    |    |
| 0h       |          |            |    |    |    |    |    |
| 15       | 14       | 13         | 12 | 11 | 10 | 9  | 8  |
| RESERVED |          |            |    |    |    |    |    |
| NONE     |          |            |    |    |    |    |    |
| 0h       |          |            |    |    |    |    |    |
| 7        | 6        | 5          | 4  | 3  | 2  | 1  | 0  |
| RESERVED | FAULT_NS | FAULT_TYPE |    |    |    |    |    |
| NONE     | R        | R          |    |    |    |    |    |
| 0h       | 0h       | 0h         |    |    |    |    |    |

**Table 2-1584. TOP\_CTRL\_FAULT\_TYPE\_STATUS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                         |
|------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                            |
| 6    | FAULT_NS   | R    | 0h    | Non-secure access.                                                                                                                                                                                                                                                                                                                                                                                  |
| 5:0  | FAULT_TYPE | R    | 0h    | Fault Type<br>10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1<br>01_0000 = Supervisor write fault - priv = 1 dir = 0<br>00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1<br>00_0100 = User read fault - priv = 0 dir = 1 dtype = 1<br>00_0010 = User write fault - priv = 0 dir = 0<br>00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1<br>00_0000 = No fault |

### 2.3.2.67 TOP\_CTRL\_FAULT\_ATTR\_STATUS Register

#### 1 TOP\_CTRL\_FAULT\_ATTR\_STATUS Register (Offset = 102Ch) [reset = 0h]

Fault Attribute Status register.

Return to [Summary Table](#)

**Table 2-1585. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 102Ch       |

**Figure 2-528. TOP\_CTRL\_FAULT\_ATTR\_STATUS Name Register**

|               |    |    |    |               |    |    |    |
|---------------|----|----|----|---------------|----|----|----|
| 31            | 30 | 29 | 28 | 27            | 26 | 25 | 24 |
| FAULT_XID     |    |    |    |               |    |    |    |
| R             |    |    |    |               |    |    |    |
| 0h            |    |    |    |               |    |    |    |
| 23            | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
| FAULT_XID     |    |    |    | FAULT_ROUTEID |    |    |    |
| R             |    |    |    | R             |    |    |    |
| 0h            |    |    |    | 0h            |    |    |    |
| 15            | 14 | 13 | 12 | 11            | 10 | 9  | 8  |
| FAULT_ROUTEID |    |    |    |               |    |    |    |
| R             |    |    |    |               |    |    |    |
| 0h            |    |    |    |               |    |    |    |
| 7             | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| FAULT_PRIVID  |    |    |    |               |    |    |    |
| R             |    |    |    |               |    |    |    |
| 0h            |    |    |    |               |    |    |    |

**Table 2-1587. TOP\_CTRL\_FAULT\_ATTR\_STATUS Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description   |
|-------|---------------|------|-------|---------------|
| 31:20 | FAULT_XID     | R    | 0h    | XID.          |
| 19:8  | FAULT_ROUTEID | R    | 0h    | Route ID.     |
| 7:0   | FAULT_PRIVID  | R    | 0h    | Privilege ID. |

### 2.3.2.68 TOP\_CTRL\_FAULT\_CLEAR Register

#### 1 TOP\_CTRL\_FAULT\_CLEAR Register (Offset = 1030h) [reset = 0h]

Fault Clear register.

Return to [Summary Table](#)

**Table 2-1588. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| TOP_CTRL      | 50D8 1030h       |

**Figure 2-529. TOP\_CTRL\_FAULT\_CLEAR Name Register**

|          |    |    |    |    |    |    |           |
|----------|----|----|----|----|----|----|-----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24        |
| RESERVED |    |    |    |    |    |    |           |
| NONE     |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16        |
| RESERVED |    |    |    |    |    |    |           |
| NONE     |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8         |
| RESERVED |    |    |    |    |    |    |           |
| NONE     |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0         |
| RESERVED |    |    |    |    |    |    | FAULT_CLR |
| NONE     |    |    |    |    |    |    | W         |
| 0h       |    |    |    |    |    |    | 0h        |

**Table 2-1590. TOP\_CTRL\_FAULT\_CLEAR Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                   |
|------|-----------|------|-------|-------------------------------------------------------------------------------|
| 31:1 | RESERVED  | NONE | 0h    | Reserved                                                                      |
| 0    | FAULT_CLR | W    | 0h    | Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. |

## 2.4 MSS\_IOMUX

### MSS\_IOMUX

#### 2.4.1 MSS\_IOMUX Summaries

#### MSS\_IOMUX Summaries

**Table 2-1591. IOMUX Registers, Base Address=5310 0000h, Length=4096**

| Offset | Length | Register Name                               | io_mux Physical Address |
|--------|--------|---------------------------------------------|-------------------------|
| 0h     | 32     | <a href="#">IOMUX_QSPI0_CSN0_CFG_REG</a>    | 5310 0000h              |
| 4h     | 32     | <a href="#">IOMUX_QSPI0_CSN1_CFG_REG</a>    | 5310 0004h              |
| 8h     | 32     | <a href="#">IOMUX_QSPI0_CLK_CFG_REG</a>     | 5310 0008h              |
| Ch     | 32     | <a href="#">IOMUX_QSPI0_D0_CFG_REG</a>      | 5310 000Ch              |
| 10h    | 32     | <a href="#">IOMUX_QSPI0_D1_CFG_REG</a>      | 5310 0010h              |
| 14h    | 32     | <a href="#">IOMUX_QSPI0_D2_CFG_REG</a>      | 5310 0014h              |
| 18h    | 32     | <a href="#">IOMUX_QSPI0_D3_CFG_REG</a>      | 5310 0018h              |
| 1Ch    | 32     | <a href="#">IOMUX_MCAN0_RX_CFG_REG</a>      | 5310 001Ch              |
| 20h    | 32     | <a href="#">IOMUX_MCAN0_TX_CFG_REG</a>      | 5310 0020h              |
| 24h    | 32     | <a href="#">IOMUX_MCAN1_RX_CFG_REG</a>      | 5310 0024h              |
| 28h    | 32     | <a href="#">IOMUX_MCAN1_TX_CFG_REG</a>      | 5310 0028h              |
| 2Ch    | 32     | <a href="#">IOMUX_SPI0_CS0_CFG_REG</a>      | 5310 002Ch              |
| 30h    | 32     | <a href="#">IOMUX_SPI0_CLK_CFG_REG</a>      | 5310 0030h              |
| 34h    | 32     | <a href="#">IOMUX_SPI0_D0_CFG_REG</a>       | 5310 0034h              |
| 38h    | 32     | <a href="#">IOMUX_SPI0_D1_CFG_REG</a>       | 5310 0038h              |
| 3Ch    | 32     | <a href="#">IOMUX_SPI1_CS0_CFG_REG</a>      | 5310 003Ch              |
| 40h    | 32     | <a href="#">IOMUX_SPI1_CLK_CFG_REG</a>      | 5310 0040h              |
| 44h    | 32     | <a href="#">IOMUX_SPI1_D0_CFG_REG</a>       | 5310 0044h              |
| 48h    | 32     | <a href="#">IOMUX_SPI1_D1_CFG_REG</a>       | 5310 0048h              |
| 4Ch    | 32     | <a href="#">IOMUX_LIN1_RXD_CFG_REG</a>      | 5310 004Ch              |
| 50h    | 32     | <a href="#">IOMUX_LIN1_TXD_CFG_REG</a>      | 5310 0050h              |
| 54h    | 32     | <a href="#">IOMUX_LIN2_RXD_CFG_REG</a>      | 5310 0054h              |
| 58h    | 32     | <a href="#">IOMUX_LIN2_TXD_CFG_REG</a>      | 5310 0058h              |
| 5Ch    | 32     | <a href="#">IOMUX_I2C1_SCL_CFG_REG</a>      | 5310 005Ch              |
| 60h    | 32     | <a href="#">IOMUX_I2C1_SDA_CFG_REG</a>      | 5310 0060h              |
| 64h    | 32     | <a href="#">IOMUX_UART0_RTSN_CFG_REG</a>    | 5310 0064h              |
| 68h    | 32     | <a href="#">IOMUX_UART0_CTSN_CFG_REG</a>    | 5310 0068h              |
| 6Ch    | 32     | <a href="#">IOMUX_UART0_RXD_CFG_REG</a>     | 5310 006Ch              |
| 70h    | 32     | <a href="#">IOMUX_UART0_TXD_CFG_REG</a>     | 5310 0070h              |
| 74h    | 32     | <a href="#">IOMUX_RGMII1_RXC_CFG_REG</a>    | 5310 0074h              |
| 78h    | 32     | <a href="#">IOMUX_RGMII1_RX_CTL_CFG_REG</a> | 5310 0078h              |
| 7Ch    | 32     | <a href="#">IOMUX_RGMII1_RD0_CFG_REG</a>    | 5310 007Ch              |
| 80h    | 32     | <a href="#">IOMUX_RGMII1_RD1_CFG_REG</a>    | 5310 0080h              |
| 84h    | 32     | <a href="#">IOMUX_RGMII1_RD2_CFG_REG</a>    | 5310 0084h              |
| 88h    | 32     | <a href="#">IOMUX_RGMII1_RD3_CFG_REG</a>    | 5310 0088h              |
| 8Ch    | 32     | <a href="#">IOMUX_RGMII1_TXC_CFG_REG</a>    | 5310 008Ch              |
| 90h    | 32     | <a href="#">IOMUX_RGMII1_TX_CTL_CFG_REG</a> | 5310 0090h              |
| 94h    | 32     | <a href="#">IOMUX_RGMII1_TD0_CFG_REG</a>    | 5310 0094h              |

**Table 2-1591. IOMUX Registers, Base Address=5310 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                            | io_mux Physical Address |
|--------|--------|------------------------------------------|-------------------------|
| 98h    | 32     | <a href="#">IOMUX_RGMII1_TD1_CFG_REG</a> | 5310 0098h              |
| 9Ch    | 32     | <a href="#">IOMUX_RGMII1_TD2_CFG_REG</a> | 5310 009Ch              |
| A0h    | 32     | <a href="#">IOMUX_RGMII1_TD3_CFG_REG</a> | 5310 00A0h              |
| A4h    | 32     | <a href="#">IOMUX_MDIO0_MDIO_CFG_REG</a> | 5310 00A4h              |
| A8h    | 32     | <a href="#">IOMUX_MDIO0_MDC_CFG_REG</a>  | 5310 00A8h              |
| ACH    | 32     | <a href="#">IOMUX_EPWM0_A_CFG_REG</a>    | 5310 00ACH              |
| B0h    | 32     | <a href="#">IOMUX_EPWM0_B_CFG_REG</a>    | 5310 00B0h              |
| B4h    | 32     | <a href="#">IOMUX_EPWM1_A_CFG_REG</a>    | 5310 00B4h              |
| B8h    | 32     | <a href="#">IOMUX_EPWM1_B_CFG_REG</a>    | 5310 00B8h              |
| BCh    | 32     | <a href="#">IOMUX_EPWM2_A_CFG_REG</a>    | 5310 00BCh              |
| C0h    | 32     | <a href="#">IOMUX_EPWM2_B_CFG_REG</a>    | 5310 00C0h              |
| C4h    | 32     | <a href="#">IOMUX_EPWM3_A_CFG_REG</a>    | 5310 00C4h              |
| C8h    | 32     | <a href="#">IOMUX_EPWM3_B_CFG_REG</a>    | 5310 00C8h              |
| CCh    | 32     | <a href="#">IOMUX_EPWM4_A_CFG_REG</a>    | 5310 00CCh              |
| D0h    | 32     | <a href="#">IOMUX_EPWM4_B_CFG_REG</a>    | 5310 00D0h              |
| D4h    | 32     | <a href="#">IOMUX_EPWM5_A_CFG_REG</a>    | 5310 00D4h              |
| D8h    | 32     | <a href="#">IOMUX_EPWM5_B_CFG_REG</a>    | 5310 00D8h              |
| DCh    | 32     | <a href="#">IOMUX_EPWM6_A_CFG_REG</a>    | 5310 00DCh              |
| E0h    | 32     | <a href="#">IOMUX_EPWM6_B_CFG_REG</a>    | 5310 00E0h              |
| E4h    | 32     | <a href="#">IOMUX_EPWM7_A_CFG_REG</a>    | 5310 00E4h              |
| E8h    | 32     | <a href="#">IOMUX_EPWM7_B_CFG_REG</a>    | 5310 00E8h              |
| ECh    | 32     | <a href="#">IOMUX_EPWM8_A_CFG_REG</a>    | 5310 00ECh              |
| F0h    | 32     | <a href="#">IOMUX_EPWM8_B_CFG_REG</a>    | 5310 00F0h              |
| F4h    | 32     | <a href="#">IOMUX_EPWM9_A_CFG_REG</a>    | 5310 00F4h              |
| F8h    | 32     | <a href="#">IOMUX_EPWM9_B_CFG_REG</a>    | 5310 00F8h              |
| FCh    | 32     | <a href="#">IOMUX_EPWM10_A_CFG_REG</a>   | 5310 00FCh              |
| 100h   | 32     | <a href="#">IOMUX_EPWM10_B_CFG_REG</a>   | 5310 0100h              |
| 104h   | 32     | <a href="#">IOMUX_EPWM11_A_CFG_REG</a>   | 5310 0104h              |
| 108h   | 32     | <a href="#">IOMUX_EPWM11_B_CFG_REG</a>   | 5310 0108h              |
| 10Ch   | 32     | <a href="#">IOMUX_EPWM12_A_CFG_REG</a>   | 5310 010Ch              |
| 110h   | 32     | <a href="#">IOMUX_EPWM12_B_CFG_REG</a>   | 5310 0110h              |
| 114h   | 32     | <a href="#">IOMUX_EPWM13_A_CFG_REG</a>   | 5310 0114h              |
| 118h   | 32     | <a href="#">IOMUX_EPWM13_B_CFG_REG</a>   | 5310 0118h              |
| 11Ch   | 32     | <a href="#">IOMUX_EPWM14_A_CFG_REG</a>   | 5310 011Ch              |
| 120h   | 32     | <a href="#">IOMUX_EPWM14_B_CFG_REG</a>   | 5310 0120h              |
| 124h   | 32     | <a href="#">IOMUX_EPWM15_A_CFG_REG</a>   | 5310 0124h              |
| 128h   | 32     | <a href="#">IOMUX_EPWM15_B_CFG_REG</a>   | 5310 0128h              |
| 12Ch   | 32     | <a href="#">IOMUX_UART1_RXD_CFG_REG</a>  | 5310 012Ch              |
| 130h   | 32     | <a href="#">IOMUX_UART1_TXD_CFG_REG</a>  | 5310 0130h              |
| 134h   | 32     | <a href="#">IOMUX_MMC0_CLK_CFG_REG</a>   | 5310 0134h              |
| 138h   | 32     | <a href="#">IOMUX_MMC0_CMD_CFG_REG</a>   | 5310 0138h              |
| 13Ch   | 32     | <a href="#">IOMUX_MMC0_D0_CFG_REG</a>    | 5310 013Ch              |
| 140h   | 32     | <a href="#">IOMUX_MMC0_D1_CFG_REG</a>    | 5310 0140h              |
| 144h   | 32     | <a href="#">IOMUX_MMC0_D2_CFG_REG</a>    | 5310 0144h              |
| 148h   | 32     | <a href="#">IOMUX_MMC0_D3_CFG_REG</a>    | 5310 0148h              |

**Table 2-1591. IOMUX Registers, Base Address=5310 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                                | io_mux Physical Address |
|--------|--------|----------------------------------------------|-------------------------|
| 14Ch   | 32     | <a href="#">IOMUX_MMC0_WP_CFG_REG</a>        | 5310 014Ch              |
| 150h   | 32     | <a href="#">IOMUX_MMC0_CD_CFG_REG</a>        | 5310 0150h              |
| 154h   | 32     | <a href="#">IOMUX_PR0_MDIO0_MDIO_CFG_REG</a> | 5310 0154h              |
| 158h   | 32     | <a href="#">IOMUX_PR0_MDIO0_MDC_CFG_REG</a>  | 5310 0158h              |
| 15Ch   | 32     | <a href="#">IOMUX_PR0_PRU0_GPO5_CFG_REG</a>  | 5310 015Ch              |
| 160h   | 32     | <a href="#">IOMUX_PR0_PRU0_GPO9_CFG_REG</a>  | 5310 0160h              |
| 164h   | 32     | <a href="#">IOMUX_PR0_PRU0_GPO10_CFG_REG</a> | 5310 0164h              |
| 168h   | 32     | <a href="#">IOMUX_PR0_PRU0_GPO8_CFG_REG</a>  | 5310 0168h              |
| 16Ch   | 32     | <a href="#">IOMUX_PR0_PRU0_GPO6_CFG_REG</a>  | 5310 016Ch              |
| 170h   | 32     | <a href="#">IOMUX_PR0_PRU0_GPO4_CFG_REG</a>  | 5310 0170h              |
| 174h   | 32     | <a href="#">IOMUX_PR0_PRU0_GPO0_CFG_REG</a>  | 5310 0174h              |
| 178h   | 32     | <a href="#">IOMUX_PR0_PRU0_GPO1_CFG_REG</a>  | 5310 0178h              |
| 17Ch   | 32     | <a href="#">IOMUX_PR0_PRU0_GPO2_CFG_REG</a>  | 5310 017Ch              |
| 180h   | 32     | <a href="#">IOMUX_PR0_PRU0_GPO3_CFG_REG</a>  | 5310 0180h              |
| 184h   | 32     | <a href="#">IOMUX_PR0_PRU0_GPO16_CFG_REG</a> | 5310 0184h              |
| 188h   | 32     | <a href="#">IOMUX_PR0_PRU0_GPO15_CFG_REG</a> | 5310 0188h              |
| 18Ch   | 32     | <a href="#">IOMUX_PR0_PRU0_GPO11_CFG_REG</a> | 5310 018Ch              |
| 190h   | 32     | <a href="#">IOMUX_PR0_PRU0_GPO12_CFG_REG</a> | 5310 0190h              |
| 194h   | 32     | <a href="#">IOMUX_PR0_PRU0_GPO13_CFG_REG</a> | 5310 0194h              |
| 198h   | 32     | <a href="#">IOMUX_PR0_PRU0_GPO14_CFG_REG</a> | 5310 0198h              |
| 19Ch   | 32     | <a href="#">IOMUX_PR0_PRU1_GPO5_CFG_REG</a>  | 5310 019Ch              |
| 1A0h   | 32     | <a href="#">IOMUX_PR0_PRU1_GPO9_CFG_REG</a>  | 5310 01A0h              |
| 1A4h   | 32     | <a href="#">IOMUX_PR0_PRU1_GPO10_CFG_REG</a> | 5310 01A4h              |
| 1A8h   | 32     | <a href="#">IOMUX_PR0_PRU1_GPO8_CFG_REG</a>  | 5310 01A8h              |
| 1ACh   | 32     | <a href="#">IOMUX_PR0_PRU1_GPO6_CFG_REG</a>  | 5310 01ACh              |
| 1B0h   | 32     | <a href="#">IOMUX_PR0_PRU1_GPO4_CFG_REG</a>  | 5310 01B0h              |
| 1B4h   | 32     | <a href="#">IOMUX_PR0_PRU1_GPO0_CFG_REG</a>  | 5310 01B4h              |
| 1B8h   | 32     | <a href="#">IOMUX_PR0_PRU1_GPO1_CFG_REG</a>  | 5310 01B8h              |
| 1BCh   | 32     | <a href="#">IOMUX_PR0_PRU1_GPO2_CFG_REG</a>  | 5310 01BCh              |
| 1C0h   | 32     | <a href="#">IOMUX_PR0_PRU1_GPO3_CFG_REG</a>  | 5310 01C0h              |
| 1C4h   | 32     | <a href="#">IOMUX_PR0_PRU1_GPO16_CFG_REG</a> | 5310 01C4h              |
| 1C8h   | 32     | <a href="#">IOMUX_PR0_PRU1_GPO15_CFG_REG</a> | 5310 01C8h              |
| 1CCh   | 32     | <a href="#">IOMUX_PR0_PRU1_GPO11_CFG_REG</a> | 5310 01CCh              |
| 1D0h   | 32     | <a href="#">IOMUX_PR0_PRU1_GPO12_CFG_REG</a> | 5310 01D0h              |
| 1D4h   | 32     | <a href="#">IOMUX_PR0_PRU1_GPO13_CFG_REG</a> | 5310 01D4h              |
| 1D8h   | 32     | <a href="#">IOMUX_PR0_PRU1_GPO14_CFG_REG</a> | 5310 01D8h              |
| 1DCh   | 32     | <a href="#">IOMUX_PR0_PRU1_GPO19_CFG_REG</a> | 5310 01DCh              |
| 1E0h   | 32     | <a href="#">IOMUX_PR0_PRU1_GPO18_CFG_REG</a> | 5310 01E0h              |
| 1E4h   | 32     | <a href="#">IOMUX_EXT_REFCLK0_CFG_REG</a>    | 5310 01E4h              |
| 1E8h   | 32     | <a href="#">IOMUX_SDFM0_CLK0_CFG_REG</a>     | 5310 01E8h              |
| 1ECh   | 32     | <a href="#">IOMUX_SDFM0_D0_CFG_REG</a>       | 5310 01ECh              |
| 1F0h   | 32     | <a href="#">IOMUX_SDFM0_CLK1_CFG_REG</a>     | 5310 01F0h              |
| 1F4h   | 32     | <a href="#">IOMUX_SDFM0_D1_CFG_REG</a>       | 5310 01F4h              |
| 1F8h   | 32     | <a href="#">IOMUX_SDFM0_CLK2_CFG_REG</a>     | 5310 01F8h              |
| 1FCh   | 32     | <a href="#">IOMUX_SDFM0_D2_CFG_REG</a>       | 5310 01FCh              |

**Table 2-1591. IOMUX Registers, Base Address=5310 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                               | io_mux Physical Address |
|--------|--------|---------------------------------------------|-------------------------|
| 200h   | 32     | <a href="#">IOMUX_SDFM0_CLK3_CFG_REG</a>    | 5310 0200h              |
| 204h   | 32     | <a href="#">IOMUX_SDFM0_D3_CFG_REG</a>      | 5310 0204h              |
| 208h   | 32     | <a href="#">IOMUX_EQEP0_A_CFG_REG</a>       | 5310 0208h              |
| 20Ch   | 32     | <a href="#">IOMUX_EQEP0_B_CFG_REG</a>       | 5310 020Ch              |
| 210h   | 32     | <a href="#">IOMUX_EQEP0_STROBE_CFG_REG</a>  | 5310 0210h              |
| 214h   | 32     | <a href="#">IOMUX_EQEP0_INDEX_CFG_REG</a>   | 5310 0214h              |
| 218h   | 32     | <a href="#">IOMUX_I2C0_SDA_CFG_REG</a>      | 5310 0218h              |
| 21Ch   | 32     | <a href="#">IOMUX_I2C0_SCL_CFG_REG</a>      | 5310 021Ch              |
| 220h   | 32     | <a href="#">IOMUX_MCAN2_TX_CFG_REG</a>      | 5310 0220h              |
| 224h   | 32     | <a href="#">IOMUX_MCAN2_RX_CFG_REG</a>      | 5310 0224h              |
| 228h   | 32     | <a href="#">IOMUX_CLKOUT0_CFG_REG</a>       | 5310 0228h              |
| 22Ch   | 32     | <a href="#">IOMUX_WARMRSTN_CFG_REG</a>      | 5310 022Ch              |
| 230h   | 32     | <a href="#">IOMUX_SAFETY_ERRORN_CFG_REG</a> | 5310 0230h              |
| 234h   | 32     | <a href="#">IOMUX_TDI_CFG_REG</a>           | 5310 0234h              |
| 238h   | 32     | <a href="#">IOMUX_TDO_CFG_REG</a>           | 5310 0238h              |
| 23Ch   | 32     | <a href="#">IOMUX_TMS_CFG_REG</a>           | 5310 023Ch              |
| 240h   | 32     | <a href="#">IOMUX_TCK_CFG_REG</a>           | 5310 0240h              |
| 244h   | 32     | <a href="#">IOMUX_OSPI0_CLKLB_CFG_REG</a>   | 5310 0244h              |
| 248h   | 32     | <a href="#">IOMUX_QUAL_GRP_0_CFG_REG</a>    | 5310 0248h              |
| 24Ch   | 32     | <a href="#">IOMUX_QUAL_GRP_1_CFG_REG</a>    | 5310 024Ch              |
| 250h   | 32     | <a href="#">IOMUX_QUAL_GRP_2_CFG_REG</a>    | 5310 0250h              |
| 254h   | 32     | <a href="#">IOMUX_QUAL_GRP_3_CFG_REG</a>    | 5310 0254h              |
| 258h   | 32     | <a href="#">IOMUX_QUAL_GRP_4_CFG_REG</a>    | 5310 0258h              |
| 25Ch   | 32     | <a href="#">IOMUX_QUAL_GRP_5_CFG_REG</a>    | 5310 025Ch              |
| 260h   | 32     | <a href="#">IOMUX_QUAL_GRP_6_CFG_REG</a>    | 5310 0260h              |
| 264h   | 32     | <a href="#">IOMUX_QUAL_GRP_7_CFG_REG</a>    | 5310 0264h              |
| 268h   | 32     | <a href="#">IOMUX_QUAL_GRP_8_CFG_REG</a>    | 5310 0268h              |
| 26Ch   | 32     | <a href="#">IOMUX_QUAL_GRP_9_CFG_REG</a>    | 5310 026Ch              |
| 270h   | 32     | <a href="#">IOMUX_QUAL_GRP_10_CFG_REG</a>   | 5310 0270h              |
| 274h   | 32     | <a href="#">IOMUX_QUAL_GRP_11_CFG_REG</a>   | 5310 0274h              |
| 278h   | 32     | <a href="#">IOMUX_QUAL_GRP_12_CFG_REG</a>   | 5310 0278h              |
| 27Ch   | 32     | <a href="#">IOMUX_QUAL_GRP_13_CFG_REG</a>   | 5310 027Ch              |
| 280h   | 32     | <a href="#">IOMUX_QUAL_GRP_14_CFG_REG</a>   | 5310 0280h              |
| 284h   | 32     | <a href="#">IOMUX_QUAL_GRP_15_CFG_REG</a>   | 5310 0284h              |
| 288h   | 32     | <a href="#">IOMUX_QUAL_GRP_16_CFG_REG</a>   | 5310 0288h              |
| 28Ch   | 32     | <a href="#">IOMUX_QUAL_GRP_17_CFG_REG</a>   | 5310 028Ch              |
| 290h   | 32     | <a href="#">IOMUX_USER_MODE_EN</a>          | 5310 0290h              |
| 294h   | 32     | <a href="#">IOMUX_PADGLBL_CFG_REG</a>       | 5310 0294h              |
| 298h   | 32     | <a href="#">IOMUX_IO_CFG_KICK0</a>          | 5310 0298h              |
| 29Ch   | 32     | <a href="#">IOMUX_IO_CFG_KICK1</a>          | 5310 029Ch              |

## 2.4.2 MSS\_IOMUX Registers

### MSS\_IOMUX Registers

### 2.4.2.1 IOMUX\_QSPI0\_CSN0\_CFG\_REG Register

#### 1 IOMUX\_QSPI0\_CSN0\_CFG\_REG Register (Offset = 0h) [reset = 5F7h]

QSPI0\_CSn0 IO config register.

Return to [Summary Table](#)

**Table 2-1592. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0000h       |

**Figure 2-530. IOMUX\_QSPI0\_CSN0\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1594. IOMUX\_QSPI0\_CSN0\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1594. IOMUX\_QSPI0\_CSN0\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.2 IOMUX\_QSPI0\_CSN1\_CFG\_REG Register

#### 1 IOMUX\_QSPI0\_CSN1\_CFG\_REG Register (Offset = 4h) [reset = 5F7h]

QSPI0\_CSn1 IO config register.

Return to [Summary Table](#)

**Table 2-1595. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0004h       |

**Figure 2-531. IOMUX\_QSPI0\_CSN1\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1597. IOMUX\_QSPI0\_CSN1\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1597. IOMUX\_QSPI0\_CSN1\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.3 IOMUX\_QSPI0\_CLK\_CFG\_REG Register

#### 1 IOMUX\_QSPI0\_CLK\_CFG\_REG Register (Offset = 8h) [reset = 5F7h]

QSPI0\_CLK IO config register.

Return to [Summary Table](#)

**Table 2-1598. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0008h       |

**Figure 2-532. IOMUX\_QSPI0\_CLK\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1600. IOMUX\_QSPI0\_CLK\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1600. IOMUX\_QSPI0\_CLK\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

#### 2.4.2.4 IOMUX\_QSPI0\_D0\_CFG\_REG Register

##### 1 IOMUX\_QSPI0\_D0\_CFG\_REG Register (Offset = Ch) [reset = 5D7h]

QSPI0\_D0 IO config register.

Return to [Summary Table](#)

**Table 2-1601. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 000Ch       |

**Figure 2-533. IOMUX\_QSPI0\_D0\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 0h             | 1h               | 7h       |     |          |     |

**Table 2-1603. IOMUX\_QSPI0\_D0\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1603. IOMUX\_QSPI0\_D0\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 0h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.5 IOMUX\_QSPI0\_D1\_CFG\_REG Register

#### 1 IOMUX\_QSPI0\_D1\_CFG\_REG Register (Offset = 10h) [reset = 5D7h]

QSPI0\_D1 IO config register.

Return to [Summary Table](#)

**Table 2-1604. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0010h       |

**Figure 2-534. IOMUX\_QSPI0\_D1\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 0h             | 1h               | 7h       |     |          |     |

**Table 2-1606. IOMUX\_QSPI0\_D1\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1606. IOMUX\_QSPI0\_D1\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 0h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.6 IOMUX\_QSPI0\_D2\_CFG\_REG Register

#### 1 IOMUX\_QSPI0\_D2\_CFG\_REG Register (Offset = 14h) [reset = 5F7h]

QSPI0\_D2 IO config register.

Return to [Summary Table](#)

**Table 2-1607. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0014h       |

**Figure 2-535. IOMUX\_QSPI0\_D2\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1609. IOMUX\_QSPI0\_D2\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1609. IOMUX\_QSPI0\_D2\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.7 IOMUX\_QSPI0\_D3\_CFG\_REG Register

#### 1 IOMUX\_QSPI0\_D3\_CFG\_REG Register (Offset = 18h) [reset = 5F7h]

QSPI0\_D3 IO config register.

Return to [Summary Table](#)

**Table 2-1610. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0018h       |

**Figure 2-536. IOMUX\_QSPI0\_D3\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1612. IOMUX\_QSPI0\_D3\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1612. IOMUX\_QSPI0\_D3\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.8 IOMUX\_MCAN0\_RX\_CFG\_REG Register

#### 1 IOMUX\_MCAN0\_RX\_CFG\_REG Register (Offset = 1Ch) [reset = 5F7h]

MCAN0\_RX IO config register.

Return to [Summary Table](#)

**Table 2-1613. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 001Ch       |

**Figure 2-537. IOMUX\_MCAN0\_RX\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1615. IOMUX\_MCAN0\_RX\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1615. IOMUX\_MCAN0\_RX\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.9 IOMUX\_MCAN0\_TX\_CFG\_REG Register

#### 1 IOMUX\_MCAN0\_TX\_CFG\_REG Register (Offset = 20h) [reset = 5F7h]

MCAN0\_TX IO config register.

Return to [Summary Table](#)

**Table 2-1616. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0020h       |

**Figure 2-538. IOMUX\_MCAN0\_TX\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1618. IOMUX\_MCAN0\_TX\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1618. IOMUX\_MCAN0\_TX\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.10 IOMUX\_MCAN1\_RX\_CFG\_REG Register

#### 1 IOMUX\_MCAN1\_RX\_CFG\_REG Register (Offset = 24h) [reset = 5F7h]

MCAN1\_RX IO config register.

Return to [Summary Table](#)

**Table 2-1619. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0024h       |

**Figure 2-539. IOMUX\_MCAN1\_RX\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1621. IOMUX\_MCAN1\_RX\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1621. IOMUX\_MCAN1\_RX\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.11 IOMUX\_MCAN1\_TX\_CFG\_REG Register

#### 1 IOMUX\_MCAN1\_TX\_CFG\_REG Register (Offset = 28h) [reset = 5F7h]

MCAN1\_TX IO config register.

Return to [Summary Table](#)

**Table 2-1622. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0028h       |

**Figure 2-540. IOMUX\_MCAN1\_TX\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1624. IOMUX\_MCAN1\_TX\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1624. IOMUX\_MCAN1\_TX\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.12 IOMUX\_SPI0\_CS0\_CFG\_REG Register

#### 1 IOMUX\_SPI0\_CS0\_CFG\_REG Register (Offset = 2Ch) [reset = 5F7h]

SPI0\_CS0 IO config register.

Return to [Summary Table](#)

**Table 2-1625. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 002Ch       |

**Figure 2-541. IOMUX\_SPI0\_CS0\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1627. IOMUX\_SPI0\_CS0\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1627. IOMUX\_SPI0\_CS0\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.13 IOMUX\_SPI0\_CLK\_CFG\_REG Register

#### 1 IOMUX\_SPI0\_CLK\_CFG\_REG Register (Offset = 30h) [reset = 5D7h]

SPI0\_CLK IO config register.

Return to [Summary Table](#)

**Table 2-1628. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0030h       |

**Figure 2-542. IOMUX\_SPI0\_CLK\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 0h             | 1h               | 7h       |     |          |     |

**Table 2-1630. IOMUX\_SPI0\_CLK\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1630. IOMUX\_SPI0\_CLK\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 0h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

#### 2.4.2.14 IOMUX\_SPI0\_D0\_CFG\_REG Register

##### 1 IOMUX\_SPI0\_D0\_CFG\_REG Register (Offset = 34h) [reset = 5D7h]

SPI0\_D0 IO config register.

Return to [Summary Table](#)

**Table 2-1631. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0034h       |

**Figure 2-543. IOMUX\_SPI0\_D0\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 0h             | 1h               | 7h       |     |          |     |

**Table 2-1633. IOMUX\_SPI0\_D0\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1633. IOMUX\_SPI0\_D0\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 0h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.15 IOMUX\_SPI0\_D1\_CFG\_REG Register

#### 1 IOMUX\_SPI0\_D1\_CFG\_REG Register (Offset = 38h) [reset = 5F7h]

SPI0\_D1 IO config register.

Return to [Summary Table](#)

**Table 2-1634. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0038h       |

**Figure 2-544. IOMUX\_SPI0\_D1\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1636. IOMUX\_SPI0\_D1\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1636. IOMUX\_SPI0\_D1\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.16 IOMUX\_SPI1\_CS0\_CFG\_REG Register

#### 1 IOMUX\_SPI1\_CS0\_CFG\_REG Register (Offset = 3Ch) [reset = 5F7h]

SPI1\_CS0 IO config register.

Return to [Summary Table](#)

**Table 2-1637. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 003Ch       |

**Figure 2-545. IOMUX\_SPI1\_CS0\_CFG\_REG Name Register**

| 31          | 30                      | 29                 | 28                   | 27       | 26  | 25       | 24  |
|-------------|-------------------------|--------------------|----------------------|----------|-----|----------|-----|
| RSVD        | RSVD                    | RESERVED           |                      |          |     |          |     |
|             |                         | NONE               |                      |          |     |          |     |
| 0h          | 0h                      | 0h                 |                      |          |     |          |     |
| 23          | 22                      | 21                 | 20                   | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVE<br>RRIDE_SEL | ICSSM_GPIO_<br>SEL | INP_INV_SEL          | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                     | R/W                | R/W                  | R/W      |     | R/W      |     |
| 0h          | 0h                      | 0h                 | 0h                   | 0h       |     | 0h       |     |
| 15          | 14                      | 13                 | 12                   | 11       | 10  | 9        | 8   |
| RESERVED    |                         |                    |                      |          | SC1 | PUPDSEL  | PE  |
| NONE        |                         |                    |                      |          | R/W | R/W      | R/W |
| 0h          |                         |                    |                      |          | 1h  | 0h       | 1h  |
| 7           | 6                       | 5                  | 4                    | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_<br>CTRL    | IE_OVERRIDE        | IE_OVERRIDE_<br>CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                     | R/W                | R/W                  | R/W      |     |          |     |
| 1h          | 1h                      | 1h                 | 1h                   | 7h       |     |          |     |

**Table 2-1639. IOMUX\_SPI1\_CS0\_CFG\_REG Register Field Descriptions**

| Bit   | Field                   | Type | Reset | Description                                                                                                                                                               |
|-------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |
| 22    | SAFETY_OVERRIDE_SE<br>L | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety<br>override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL          | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal<br>GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL             | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                     |
| 19:18 | QUAL_SEL                | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                           |
| 17:16 | GPIO_SEL                | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                              |
| 15:11 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |

**Table 2-1639. IOMUX\_SPI1\_CS0\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.17 IOMUX\_SPI1\_CLK\_CFG\_REG Register

#### 1 IOMUX\_SPI1\_CLK\_CFG\_REG Register (Offset = 40h) [reset = 5F7h]

SPI1\_CLK IO config register.

Return to [Summary Table](#)

**Table 2-1640. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0040h       |

**Figure 2-546. IOMUX\_SPI1\_CLK\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1642. IOMUX\_SPI1\_CLK\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1642. IOMUX\_SPI1\_CLK\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.18 IOMUX\_SPI1\_D0\_CFG\_REG Register

#### 1 IOMUX\_SPI1\_D0\_CFG\_REG Register (Offset = 44h) [reset = 5F7h]

SPI1\_D0 IO config register.

Return to [Summary Table](#)

**Table 2-1643. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0044h       |

**Figure 2-547. IOMUX\_SPI1\_D0\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1645. IOMUX\_SPI1\_D0\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1645. IOMUX\_SPI1\_D0\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.19 IOMUX\_SPI1\_D1\_CFG\_REG Register

#### 1 IOMUX\_SPI1\_D1\_CFG\_REG Register (Offset = 48h) [reset = 5F7h]

SPI1\_D1 IO config register.

Return to [Summary Table](#)

**Table 2-1646. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0048h       |

**Figure 2-548. IOMUX\_SPI1\_D1\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1648. IOMUX\_SPI1\_D1\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1648. IOMUX\_SPI1\_D1\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.20 IOMUX\_LIN1\_RXD\_CFG\_REG Register

### 1 IOMUX\_LIN1\_RXD\_CFG\_REG Register (Offset = 4Ch) [reset = 5F7h]

LIN1\_RXD IO config register.

Return to [Summary Table](#)

**Table 2-1649. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 004Ch       |

**Figure 2-549. IOMUX\_LIN1\_RXD\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1651. IOMUX\_LIN1\_RXD\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1651. IOMUX\_LIN1\_RXD\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.21 IOMUX\_LIN1\_TXD\_CFG\_REG Register

#### 1 IOMUX\_LIN1\_TXD\_CFG\_REG Register (Offset = 50h) [reset = 5F7h]

LIN1\_TXD IO config register.

Return to [Summary Table](#)

**Table 2-1652. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0050h       |

**Figure 2-550. IOMUX\_LIN1\_TXD\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1654. IOMUX\_LIN1\_TXD\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1654. IOMUX\_LIN1\_TXD\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.22 IOMUX\_LIN2\_RXD\_CFG\_REG Register

#### 1 IOMUX\_LIN2\_RXD\_CFG\_REG Register (Offset = 54h) [reset = 5F7h]

LIN2\_RXD IO config register.

Return to [Summary Table](#)

**Table 2-1655. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0054h       |

**Figure 2-551. IOMUX\_LIN2\_RXD\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1657. IOMUX\_LIN2\_RXD\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1657. IOMUX\_LIN2\_RXD\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.23 IOMUX\_LIN2\_TXD\_CFG\_REG Register

#### 1 IOMUX\_LIN2\_TXD\_CFG\_REG Register (Offset = 58h) [reset = 5F7h]

LIN2\_TXD IO config register.

Return to [Summary Table](#)

**Table 2-1658. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0058h       |

**Figure 2-552. IOMUX\_LIN2\_TXD\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1660. IOMUX\_LIN2\_TXD\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1660. IOMUX\_LIN2\_TXD\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.24 IOMUX\_I2C1\_SCL\_CFG\_REG Register

### 1 IOMUX\_I2C1\_SCL\_CFG\_REG Register (Offset = 5Ch) [reset = 5F7h]

I2C1\_SCL IO config register.

Return to [Summary Table](#)

**Table 2-1661. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 005Ch       |

**Figure 2-553. IOMUX\_I2C1\_SCL\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1663. IOMUX\_I2C1\_SCL\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1663. IOMUX\_I2C1\_SCL\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.25 IOMUX\_I2C1\_SDA\_CFG\_REG Register

#### 1 IOMUX\_I2C1\_SDA\_CFG\_REG Register (Offset = 60h) [reset = 5F7h]

I2C1\_SDA IO config register.

Return to [Summary Table](#)

**Table 2-1664. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0060h       |

**Figure 2-554. IOMUX\_I2C1\_SDA\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1666. IOMUX\_I2C1\_SDA\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1666. IOMUX\_I2C1\_SDA\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.26 IOMUX\_UART0\_RTSN\_CFG\_REG Register

### 1 IOMUX\_UART0\_RTSN\_CFG\_REG Register (Offset = 64h) [reset = 5F7h]

UART0\_RTSn IO config register.

Return to [Summary Table](#)

**Table 2-1667. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0064h       |

**Figure 2-555. IOMUX\_UART0\_RTSN\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1669. IOMUX\_UART0\_RTSN\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1669. IOMUX\_UART0\_RTSM\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.27 IOMUX\_UART0\_CTSN\_CFG\_REG Register

#### 1 IOMUX\_UART0\_CTSN\_CFG\_REG Register (Offset = 68h) [reset = 5F7h]

UART0\_CTSn IO config register.

Return to [Summary Table](#)

**Table 2-1670. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0068h       |

**Figure 2-556. IOMUX\_UART0\_CTSN\_CFG\_REG Name Register**

| 31          |                         | 30                 |  | 29                   |  | 28       |  | 27 |  | 26       |  | 25      |  | 24  |  |
|-------------|-------------------------|--------------------|--|----------------------|--|----------|--|----|--|----------|--|---------|--|-----|--|
| RSVD        |                         | RSVD               |  | RESERVED             |  |          |  |    |  |          |  |         |  |     |  |
|             |                         |                    |  | NONE                 |  |          |  |    |  |          |  |         |  |     |  |
| 0h          |                         | 0h                 |  | 0h                   |  |          |  |    |  |          |  |         |  |     |  |
| 23          |                         | 22                 |  | 21                   |  | 20       |  | 19 |  | 18       |  | 17      |  | 16  |  |
| RESERVED    | SAFETY_OVE<br>RRIDE_SEL | ICSSM_GPIO_<br>SEL |  | INP_INV_SEL          |  | QUAL_SEL |  |    |  | GPIO_SEL |  |         |  |     |  |
| NONE        | R/W                     | R/W                |  | R/W                  |  | R/W      |  |    |  | R/W      |  |         |  |     |  |
| 0h          | 0h                      | 0h                 |  | 0h                   |  | 0h       |  |    |  | 0h       |  |         |  |     |  |
| 15          |                         | 14                 |  | 13                   |  | 12       |  | 11 |  | 10       |  | 9       |  | 8   |  |
| RESERVED    |                         |                    |  |                      |  |          |  |    |  | SC1      |  | PUPDSEL |  | PE  |  |
| NONE        |                         |                    |  |                      |  |          |  |    |  | R/W      |  | R/W     |  | R/W |  |
| 0h          |                         |                    |  |                      |  |          |  |    |  | 1h       |  | 0h      |  | 1h  |  |
| 7           |                         | 6                  |  | 5                    |  | 4        |  | 3  |  | 2        |  | 1       |  | 0   |  |
| OE_OVERRIDE | OE_OVERRIDE_<br>CTRL    | IE_OVERRIDE        |  | IE_OVERRIDE_<br>CTRL |  | FUNC_SEL |  |    |  |          |  |         |  |     |  |
| R/W         | R/W                     | R/W                |  | R/W                  |  | R/W      |  |    |  |          |  |         |  |     |  |
| 1h          | 1h                      | 1h                 |  | 1h                   |  | 7h       |  |    |  |          |  |         |  |     |  |

**Table 2-1672. IOMUX\_UART0\_CTSN\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1672. IOMUX\_UART0\_CTSN\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.28 IOMUX\_UART0\_RXD\_CFG\_REG Register

### 1 IOMUX\_UART0\_RXD\_CFG\_REG Register (Offset = 6Ch) [reset = 5F7h]

UART0\_RXD IO config register.

Return to [Summary Table](#)

**Table 2-1673. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 006Ch       |

**Figure 2-557. IOMUX\_UART0\_RXD\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1675. IOMUX\_UART0\_RXD\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1675. IOMUX\_UART0\_RXD\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.29 IOMUX\_UART0\_TXD\_CFG\_REG Register

### 1 IOMUX\_UART0\_TXD\_CFG\_REG Register (Offset = 70h) [reset = 5F7h]

UART0\_TXD IO config register.

Return to [Summary Table](#)

**Table 2-1676. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0070h       |

**Figure 2-558. IOMUX\_UART0\_TXD\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1678. IOMUX\_UART0\_TXD\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1678. IOMUX\_UART0\_TXD\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.30 IOMUX\_RGMII1\_RXC\_CFG\_REG Register

#### 1 IOMUX\_RGMII1\_RXC\_CFG\_REG Register (Offset = 74h) [reset = 5F7h]

RGMII1\_RXC IO config register.

Return to [Summary Table](#)

**Table 2-1679. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0074h       |

**Figure 2-559. IOMUX\_RGMII1\_RXC\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1681. IOMUX\_RGMII1\_RXC\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1681. IOMUX\_RGMII1\_RXC\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.31 IOMUX\_RGMII1\_RX\_CTL\_CFG\_REG Register

#### 1 IOMUX\_RGMII1\_RX\_CTL\_CFG\_REG Register (Offset = 78h) [reset = 5F7h]

RGMII1\_RX\_CTL IO config register.

Return to [Summary Table](#)

**Table 2-1682. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0078h       |

**Figure 2-560. IOMUX\_RGMII1\_RX\_CTL\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1684. IOMUX\_RGMII1\_RX\_CTL\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1684. IOMUX\_RGMII1\_RX\_CTL\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.32 IOMUX\_RGMII1\_RD0\_CFG\_REG Register

#### 1 IOMUX\_RGMII1\_RD0\_CFG\_REG Register (Offset = 7Ch) [reset = 5F7h]

RGMII1\_RD0 IO config register.

Return to [Summary Table](#)

**Table 2-1685. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 007Ch       |

**Figure 2-561. IOMUX\_RGMII1\_RD0\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1687. IOMUX\_RGMII1\_RD0\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1687. IOMUX\_RGMII1\_RD0\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.33 IOMUX\_RGMII1\_RD1\_CFG\_REG Register

#### 1 IOMUX\_RGMII1\_RD1\_CFG\_REG Register (Offset = 80h) [reset = 5F7h]

RGMII1\_RD1 IO config register.

Return to [Summary Table](#)

**Table 2-1688. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0080h       |

**Figure 2-562. IOMUX\_RGMII1\_RD1\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1690. IOMUX\_RGMII1\_RD1\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1690. IOMUX\_RGMII1\_RD1\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.34 IOMUX\_RGMII1\_RD2\_CFG\_REG Register

#### 1 IOMUX\_RGMII1\_RD2\_CFG\_REG Register (Offset = 84h) [reset = 5F7h]

RGMII1\_RD2 IO config register.

Return to [Summary Table](#)

**Table 2-1691. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0084h       |

**Figure 2-563. IOMUX\_RGMII1\_RD2\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1693. IOMUX\_RGMII1\_RD2\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1693. IOMUX\_RGMII1\_RD2\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.35 IOMUX\_RGMII1\_RD3\_CFG\_REG Register

#### 1 IOMUX\_RGMII1\_RD3\_CFG\_REG Register (Offset = 88h) [reset = 5F7h]

RGMII1\_RD3 IO config register.

Return to [Summary Table](#)

**Table 2-1694. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0088h       |

**Figure 2-564. IOMUX\_RGMII1\_RD3\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1696. IOMUX\_RGMII1\_RD3\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1696. IOMUX\_RGMII1\_RD3\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.36 IOMUX\_RGMII1\_TXC\_CFG\_REG Register

#### 1 IOMUX\_RGMII1\_TXC\_CFG\_REG Register (Offset = 8Ch) [reset = 5F7h]

RGMII1\_TXC IO config register.

Return to [Summary Table](#)

**Table 2-1697. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 008Ch       |

**Figure 2-565. IOMUX\_RGMII1\_TXC\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1699. IOMUX\_RGMII1\_TXC\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1699. IOMUX\_RGMII1\_TXC\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.37 IOMUX\_RGMII1\_TX\_CTL\_CFG\_REG Register

#### 1 IOMUX\_RGMII1\_TX\_CTL\_CFG\_REG Register (Offset = 90h) [reset = 5F7h]

RGMII1\_TX\_CTL IO config register.

Return to [Summary Table](#)

**Table 2-1700. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0090h       |

**Figure 2-566. IOMUX\_RGMII1\_TX\_CTL\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1702. IOMUX\_RGMII1\_TX\_CTL\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1702. IOMUX\_RGMII1\_TX\_CTL\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.38 IOMUX\_RGMII1\_TD0\_CFG\_REG Register

#### 1 IOMUX\_RGMII1\_TD0\_CFG\_REG Register (Offset = 94h) [reset = 5F7h]

RGMII1\_TD0 IO config register.

Return to [Summary Table](#)

**Table 2-1703. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0094h       |

**Figure 2-567. IOMUX\_RGMII1\_TD0\_CFG\_REG Name Register**

|             |                     |                |                  |          |     |          |     |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1705. IOMUX\_RGMII1\_TD0\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1705. IOMUX\_RGMII1\_TD0\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.39 IOMUX\_RGMII1\_TD1\_CFG\_REG Register

#### 1 IOMUX\_RGMII1\_TD1\_CFG\_REG Register (Offset = 98h) [reset = 5F7h]

RGMII1\_TD1 IO config register.

Return to [Summary Table](#)

**Table 2-1706. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0098h       |

**Figure 2-568. IOMUX\_RGMII1\_TD1\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1708. IOMUX\_RGMII1\_TD1\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1708. IOMUX\_RGMII1\_TD1\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

#### 2.4.2.40 IOMUX\_RGMII1\_TD2\_CFG\_REG Register

##### 1 IOMUX\_RGMII1\_TD2\_CFG\_REG Register (Offset = 9Ch) [reset = 5F7h]

RGMII1\_TD2 IO config register.

Return to [Summary Table](#)

**Table 2-1709. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 009Ch       |

**Figure 2-569. IOMUX\_RGMII1\_TD2\_CFG\_REG Name Register**

| 31          | 30                      | 29                 | 28                   | 27       | 26  | 25       | 24  |
|-------------|-------------------------|--------------------|----------------------|----------|-----|----------|-----|
| RSVD        | RSVD                    | RESERVED           |                      |          |     |          |     |
|             |                         | NONE               |                      |          |     |          |     |
| 0h          | 0h                      | 0h                 |                      |          |     |          |     |
| 23          | 22                      | 21                 | 20                   | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVE<br>RRIDE_SEL | ICSSM_GPIO_<br>SEL | INP_INV_SEL          | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                     | R/W                | R/W                  | R/W      |     | R/W      |     |
| 0h          | 0h                      | 0h                 | 0h                   | 0h       |     | 0h       |     |
| 15          | 14                      | 13                 | 12                   | 11       | 10  | 9        | 8   |
| RESERVED    |                         |                    |                      |          | SC1 | PUPDSEL  | PE  |
| NONE        |                         |                    |                      |          | R/W | R/W      | R/W |
| 0h          |                         |                    |                      |          | 1h  | 0h       | 1h  |
| 7           | 6                       | 5                  | 4                    | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_<br>CTRL    | IE_OVERRIDE        | IE_OVERRIDE_<br>CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                     | R/W                | R/W                  | R/W      |     |          |     |
| 1h          | 1h                      | 1h                 | 1h                   | 7h       |     |          |     |

**Table 2-1711. IOMUX\_RGMII1\_TD2\_CFG\_REG Register Field Descriptions**

| Bit   | Field                   | Type | Reset | Description                                                                                                                                                               |
|-------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |
| 22    | SAFETY_OVERRIDE_SE<br>L | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety<br>override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL          | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal<br>GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL             | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                     |
| 19:18 | QUAL_SEL                | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                           |
| 17:16 | GPIO_SEL                | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                              |
| 15:11 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |

**Table 2-1711. IOMUX\_RGMII1\_TD2\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

#### 2.4.2.41 IOMUX\_RGMII1\_TD3\_CFG\_REG Register

##### 1 IOMUX\_RGMII1\_TD3\_CFG\_REG Register (Offset = A0h) [reset = 5F7h]

RGMII1\_TD3 IO config register.

Return to [Summary Table](#)

**Table 2-1712. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 00A0h       |

**Figure 2-570. IOMUX\_RGMII1\_TD3\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1714. IOMUX\_RGMII1\_TD3\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1714. IOMUX\_RGMII1\_TD3\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.42 IOMUX\_MDIO0\_MDIO\_CFG\_REG Register

### 1 IOMUX\_MDIO0\_MDIO\_CFG\_REG Register (Offset = A4h) [reset = 5F7h]

MDIO0\_MDIO IO config register.

Return to [Summary Table](#)

**Table 2-1715. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 00A4h       |

**Figure 2-571. IOMUX\_MDIO0\_MDIO\_CFG\_REG Name Register**

|             |                     |                |                  |          |     |          |     |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1717. IOMUX\_MDIO0\_MDIO\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1717. IOMUX\_MDIO0\_MDIO\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.43 IOMUX\_MDIO0\_MDC\_CFG\_REG Register

#### 1 IOMUX\_MDIO0\_MDC\_CFG\_REG Register (Offset = A8h) [reset = 5F7h]

MDIO0\_MDC IO config register.

Return to [Summary Table](#)

**Table 2-1718. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 00A8h       |

**Figure 2-572. IOMUX\_MDIO0\_MDC\_CFG\_REG Name Register**

|             |                     |                |                  |          |     |          |     |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1720. IOMUX\_MDIO0\_MDC\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1720. IOMUX\_MDIO0\_MDC\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

#### 2.4.2.44 IOMUX\_EPWM0\_A\_CFG\_REG Register

##### 1 IOMUX\_EPWM0\_A\_CFG\_REG Register (Offset = ACh) [reset = 5F7h]

EPWM0\_A IO config register.

Return to [Summary Table](#)

**Table 2-1721. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 00ACh       |

**Figure 2-573. IOMUX\_EPWM0\_A\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1723. IOMUX\_EPWM0\_A\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1723. IOMUX\_EPWM0\_A\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.45 IOMUX\_EPWM0\_B\_CFG\_REG Register

#### 1 IOMUX\_EPWM0\_B\_CFG\_REG Register (Offset = B0h) [reset = 5F7h]

EPWM0\_B IO config register.

Return to [Summary Table](#)

**Table 2-1724. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 00B0h       |

**Figure 2-574. IOMUX\_EPWM0\_B\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1726. IOMUX\_EPWM0\_B\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1726. IOMUX\_EPWM0\_B\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.46 IOMUX\_EPWM1\_A\_CFG\_REG Register

#### 1 IOMUX\_EPWM1\_A\_CFG\_REG Register (Offset = B4h) [reset = 5F7h]

EPWM1\_A IO config register.

Return to [Summary Table](#)

**Table 2-1727. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 00B4h       |

**Figure 2-575. IOMUX\_EPWM1\_A\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1729. IOMUX\_EPWM1\_A\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1729. IOMUX\_EPWM1\_A\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.47 IOMUX\_EPWM1\_B\_CFG\_REG Register

#### 1 IOMUX\_EPWM1\_B\_CFG\_REG Register (Offset = B8h) [reset = 5F7h]

EPWM1\_B IO config register.

Return to [Summary Table](#)

**Table 2-1730. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 00B8h       |

**Figure 2-576. IOMUX\_EPWM1\_B\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1732. IOMUX\_EPWM1\_B\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1732. IOMUX\_EPWM1\_B\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

#### 2.4.2.48 IOMUX\_EPWM2\_A\_CFG\_REG Register

##### 1 IOMUX\_EPWM2\_A\_CFG\_REG Register (Offset = BCh) [reset = 5F7h]

EPWM2\_A IO config register.

Return to [Summary Table](#)

**Table 2-1733. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 00BCh       |

**Figure 2-577. IOMUX\_EPWM2\_A\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1735. IOMUX\_EPWM2\_A\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1735. IOMUX\_EPWM2\_A\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.49 IOMUX\_EPWM2\_B\_CFG\_REG Register

#### 1 IOMUX\_EPWM2\_B\_CFG\_REG Register (Offset = C0h) [reset = 5F7h]

EPWM2\_B IO config register.

Return to [Summary Table](#)

**Table 2-1736. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 00C0h       |

**Figure 2-578. IOMUX\_EPWM2\_B\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1738. IOMUX\_EPWM2\_B\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1738. IOMUX\_EPWM2\_B\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.50 IOMUX\_EPWM3\_A\_CFG\_REG Register

#### 1 IOMUX\_EPWM3\_A\_CFG\_REG Register (Offset = C4h) [reset = 5F7h]

EPWM3\_A IO config register.

Return to [Summary Table](#)

**Table 2-1739. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 00C4h       |

**Figure 2-579. IOMUX\_EPWM3\_A\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1741. IOMUX\_EPWM3\_A\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1741. IOMUX\_EPWM3\_A\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.51 IOMUX\_EPWM3\_B\_CFG\_REG Register

#### 1 IOMUX\_EPWM3\_B\_CFG\_REG Register (Offset = C8h) [reset = 5F7h]

EPWM3\_B IO config register.

Return to [Summary Table](#)

**Table 2-1742. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 00C8h       |

**Figure 2-580. IOMUX\_EPWM3\_B\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1744. IOMUX\_EPWM3\_B\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1744. IOMUX\_EPWM3\_B\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.52 IOMUX\_EPWM4\_A\_CFG\_REG Register

### 1 IOMUX\_EPWM4\_A\_CFG\_REG Register (Offset = CCh) [reset = 5F7h]

EPWM4\_A IO config register.

Return to [Summary Table](#)

**Table 2-1745. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 00CCh       |

**Figure 2-581. IOMUX\_EPWM4\_A\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1747. IOMUX\_EPWM4\_A\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1747. IOMUX\_EPWM4\_A\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.53 IOMUX\_EPWM4\_B\_CFG\_REG Register

#### 1 IOMUX\_EPWM4\_B\_CFG\_REG Register (Offset = D0h) [reset = 5F7h]

EPWM4\_B IO config register.

Return to [Summary Table](#)

**Table 2-1748. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 00D0h       |

**Figure 2-582. IOMUX\_EPWM4\_B\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1750. IOMUX\_EPWM4\_B\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1750. IOMUX\_EPWM4\_B\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

#### 2.4.2.54 IOMUX\_EPWM5\_A\_CFG\_REG Register

##### 1 IOMUX\_EPWM5\_A\_CFG\_REG Register (Offset = D4h) [reset = 5F7h]

EPWM5\_A IO config register.

Return to [Summary Table](#)

**Table 2-1751. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 00D4h       |

**Figure 2-583. IOMUX\_EPWM5\_A\_CFG\_REG Name Register**

| 31          | 30                      | 29                 | 28                   | 27       | 26  | 25       | 24  |
|-------------|-------------------------|--------------------|----------------------|----------|-----|----------|-----|
| RSVD        | RSVD                    | RESERVED           |                      |          |     |          |     |
|             |                         | NONE               |                      |          |     |          |     |
| 0h          | 0h                      | 0h                 |                      |          |     |          |     |
| 23          | 22                      | 21                 | 20                   | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVE<br>RRIDE_SEL | ICSSM_GPIO_<br>SEL | INP_INV_SEL          | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                     | R/W                | R/W                  | R/W      |     | R/W      |     |
| 0h          | 0h                      | 0h                 | 0h                   | 0h       |     | 0h       |     |
| 15          | 14                      | 13                 | 12                   | 11       | 10  | 9        | 8   |
| RESERVED    |                         |                    |                      |          | SC1 | PUPDSEL  | PE  |
| NONE        |                         |                    |                      |          | R/W | R/W      | R/W |
| 0h          |                         |                    |                      |          | 1h  | 0h       | 1h  |
| 7           | 6                       | 5                  | 4                    | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_<br>CTRL    | IE_OVERRIDE        | IE_OVERRIDE_<br>CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                     | R/W                | R/W                  | R/W      |     |          |     |
| 1h          | 1h                      | 1h                 | 1h                   | 7h       |     |          |     |

**Table 2-1753. IOMUX\_EPWM5\_A\_CFG\_REG Register Field Descriptions**

| Bit   | Field                   | Type | Reset | Description                                                                                                                                                               |
|-------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |
| 22    | SAFETY_OVERRIDE_SE<br>L | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety<br>override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL          | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal<br>GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL             | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                     |
| 19:18 | QUAL_SEL                | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                           |
| 17:16 | GPIO_SEL                | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                              |
| 15:11 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |

**Table 2-1753. IOMUX\_EPWM5\_A\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.55 IOMUX\_EPWM5\_B\_CFG\_REG Register

#### 1 IOMUX\_EPWM5\_B\_CFG\_REG Register (Offset = D8h) [reset = 5F7h]

EPWM5\_B IO config register.

Return to [Summary Table](#)

**Table 2-1754. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 00D8h       |

**Figure 2-584. IOMUX\_EPWM5\_B\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1756. IOMUX\_EPWM5\_B\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1756. IOMUX\_EPWM5\_B\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.56 IOMUX\_EPWM6\_A\_CFG\_REG Register

#### 1 IOMUX\_EPWM6\_A\_CFG\_REG Register (Offset = DCh) [reset = 5F7h]

EPWM6\_A IO config register.

Return to [Summary Table](#)

**Table 2-1757. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 00DCh       |

**Figure 2-585. IOMUX\_EPWM6\_A\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1759. IOMUX\_EPWM6\_A\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1759. IOMUX\_EPWM6\_A\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.57 IOMUX\_EPWM6\_B\_CFG\_REG Register

#### 1 IOMUX\_EPWM6\_B\_CFG\_REG Register (Offset = E0h) [reset = 5F7h]

EPWM6\_B IO config register.

Return to [Summary Table](#)

**Table 2-1760. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 00E0h       |

**Figure 2-586. IOMUX\_EPWM6\_B\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1762. IOMUX\_EPWM6\_B\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1762. IOMUX\_EPWM6\_B\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.58 IOMUX\_EPWM7\_A\_CFG\_REG Register

### 1 IOMUX\_EPWM7\_A\_CFG\_REG Register (Offset = E4h) [reset = 5F7h]

EPWM7\_A IO config register.

Return to [Summary Table](#)

**Table 2-1763. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 00E4h       |

**Figure 2-587. IOMUX\_EPWM7\_A\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1765. IOMUX\_EPWM7\_A\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1765. IOMUX\_EPWM7\_A\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.59 IOMUX\_EPWM7\_B\_CFG\_REG Register

#### 1 IOMUX\_EPWM7\_B\_CFG\_REG Register (Offset = E8h) [reset = 5F7h]

EPWM7\_B IO config register.

Return to [Summary Table](#)

**Table 2-1766. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 00E8h       |

**Figure 2-588. IOMUX\_EPWM7\_B\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1768. IOMUX\_EPWM7\_B\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1768. IOMUX\_EPWM7\_B\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.60 IOMUX\_EPWM8\_A\_CFG\_REG Register

### 1 IOMUX\_EPWM8\_A\_CFG\_REG Register (Offset = ECh) [reset = 5F7h]

EPWM8\_A IO config register.

Return to [Summary Table](#)

**Table 2-1769. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 00ECh       |

**Figure 2-589. IOMUX\_EPWM8\_A\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1771. IOMUX\_EPWM8\_A\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1771. IOMUX\_EPWM8\_A\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.61 IOMUX\_EPWM8\_B\_CFG\_REG Register

#### 1 IOMUX\_EPWM8\_B\_CFG\_REG Register (Offset = F0h) [reset = 5F7h]

EPWM8\_B IO config register.

Return to [Summary Table](#)

**Table 2-1772. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 00F0h       |

**Figure 2-590. IOMUX\_EPWM8\_B\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1774. IOMUX\_EPWM8\_B\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1774. IOMUX\_EPWM8\_B\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.62 IOMUX\_EPWM9\_A\_CFG\_REG Register

### 1 IOMUX\_EPWM9\_A\_CFG\_REG Register (Offset = F4h) [reset = 5F7h]

EPWM9\_A IO config register.

Return to [Summary Table](#)

**Table 2-1775. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 00F4h       |

**Figure 2-591. IOMUX\_EPWM9\_A\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1777. IOMUX\_EPWM9\_A\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1777. IOMUX\_EPWM9\_A\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.63 IOMUX\_EPWM9\_B\_CFG\_REG Register

#### 1 IOMUX\_EPWM9\_B\_CFG\_REG Register (Offset = F8h) [reset = 5F7h]

EPWM9\_B IO config register.

Return to [Summary Table](#)

**Table 2-1778. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 00F8h       |

**Figure 2-592. IOMUX\_EPWM9\_B\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1780. IOMUX\_EPWM9\_B\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1780. IOMUX\_EPWM9\_B\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.64 IOMUX\_EPWM10\_A\_CFG\_REG Register

### 1 IOMUX\_EPWM10\_A\_CFG\_REG Register (Offset = FCh) [reset = 5F7h]

EPWM10\_A IO config register.

Return to [Summary Table](#)

**Table 2-1781. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 00FCh       |

**Figure 2-593. IOMUX\_EPWM10\_A\_CFG\_REG Name Register**

| 31          | 30                      | 29                 | 28                   | 27       | 26  | 25       | 24  |
|-------------|-------------------------|--------------------|----------------------|----------|-----|----------|-----|
| RSVD        | RSVD                    | RESERVED           |                      |          |     |          |     |
|             |                         | NONE               |                      |          |     |          |     |
| 0h          | 0h                      | 0h                 |                      |          |     |          |     |
| 23          | 22                      | 21                 | 20                   | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVE<br>RRIDE_SEL | ICSSM_GPIO_<br>SEL | INP_INV_SEL          | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                     | R/W                | R/W                  | R/W      |     | R/W      |     |
| 0h          | 0h                      | 0h                 | 0h                   | 0h       |     | 0h       |     |
| 15          | 14                      | 13                 | 12                   | 11       | 10  | 9        | 8   |
| RESERVED    |                         |                    |                      |          | SC1 | PUPDSEL  | PE  |
| NONE        |                         |                    |                      |          | R/W | R/W      | R/W |
| 0h          |                         |                    |                      |          | 1h  | 0h       | 1h  |
| 7           | 6                       | 5                  | 4                    | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_<br>CTRL    | IE_OVERRIDE        | IE_OVERRIDE_<br>CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                     | R/W                | R/W                  | R/W      |     |          |     |
| 1h          | 1h                      | 1h                 | 1h                   | 7h       |     |          |     |

**Table 2-1783. IOMUX\_EPWM10\_A\_CFG\_REG Register Field Descriptions**

| Bit   | Field                   | Type | Reset | Description                                                                                                                                                               |
|-------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |
| 22    | SAFETY_OVERRIDE_SE<br>L | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety<br>override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL          | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal<br>GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL             | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                     |
| 19:18 | QUAL_SEL                | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                           |
| 17:16 | GPIO_SEL                | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                              |
| 15:11 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |

**Table 2-1783. IOMUX\_EPWM10\_A\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.65 IOMUX\_EPWM10\_B\_CFG\_REG Register

#### 1 IOMUX\_EPWM10\_B\_CFG\_REG Register (Offset = 100h) [reset = 5F7h]

EPWM10\_B IO config register.

Return to [Summary Table](#)

**Table 2-1784. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0100h       |

**Figure 2-594. IOMUX\_EPWM10\_B\_CFG\_REG Name Register**

|             |                         |                    |                      |          |     |          |     |
|-------------|-------------------------|--------------------|----------------------|----------|-----|----------|-----|
| 31          | 30                      | 29                 | 28                   | 27       | 26  | 25       | 24  |
| RSVD        | RSVD                    | RESERVED           |                      |          |     |          |     |
|             |                         | NONE               |                      |          |     |          |     |
| 0h          | 0h                      | 0h                 |                      |          |     |          |     |
| 23          | 22                      | 21                 | 20                   | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVE<br>RRIDE_SEL | ICSSM_GPIO_<br>SEL | INP_INV_SEL          | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                     | R/W                | R/W                  | R/W      |     | R/W      |     |
| 0h          | 0h                      | 0h                 | 0h                   | 0h       |     | 0h       |     |
| 15          | 14                      | 13                 | 12                   | 11       | 10  | 9        | 8   |
| RESERVED    |                         |                    |                      |          | SC1 | PUPDSEL  | PE  |
| NONE        |                         |                    |                      |          | R/W | R/W      | R/W |
| 0h          |                         |                    |                      |          | 1h  | 0h       | 1h  |
| 7           | 6                       | 5                  | 4                    | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_<br>CTRL    | IE_OVERRIDE        | IE_OVERRIDE_<br>CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                     | R/W                | R/W                  | R/W      |     |          |     |
| 1h          | 1h                      | 1h                 | 1h                   | 7h       |     |          |     |

**Table 2-1786. IOMUX\_EPWM10\_B\_CFG\_REG Register Field Descriptions**

| Bit   | Field                   | Type | Reset | Description                                                                                                                                                               |
|-------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |
| 22    | SAFETY_OVERRIDE_SE<br>L | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety<br>override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL          | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal<br>GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL             | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                     |
| 19:18 | QUAL_SEL                | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                           |
| 17:16 | GPIO_SEL                | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                              |
| 15:11 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |



**Table 2-1786. IOMUX\_EPWM10\_B\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.66 IOMUX\_EPWM11\_A\_CFG\_REG Register

#### 1 IOMUX\_EPWM11\_A\_CFG\_REG Register (Offset = 104h) [reset = 5F7h]

EPWM11\_A IO config register.

Return to [Summary Table](#)

**Table 2-1787. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0104h       |

**Figure 2-595. IOMUX\_EPWM11\_A\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1789. IOMUX\_EPWM11\_A\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1789. IOMUX\_EPWM11\_A\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.67 IOMUX\_EPWM11\_B\_CFG\_REG Register

#### 1 IOMUX\_EPWM11\_B\_CFG\_REG Register (Offset = 108h) [reset = 5F7h]

EPWM11\_B IO config register.

Return to [Summary Table](#)

**Table 2-1790. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0108h       |

**Figure 2-596. IOMUX\_EPWM11\_B\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1792. IOMUX\_EPWM11\_B\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1792. IOMUX\_EPWM11\_B\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.68 IOMUX\_EPWM12\_A\_CFG\_REG Register

#### 1 IOMUX\_EPWM12\_A\_CFG\_REG Register (Offset = 10Ch) [reset = 5F7h]

EPWM12\_A IO config register.

Return to [Summary Table](#)

**Table 2-1793. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 010Ch       |

**Figure 2-597. IOMUX\_EPWM12\_A\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1795. IOMUX\_EPWM12\_A\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1795. IOMUX\_EPWM12\_A\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.69 IOMUX\_EPWM12\_B\_CFG\_REG Register

### 1 IOMUX\_EPWM12\_B\_CFG\_REG Register (Offset = 110h) [reset = 5F7h]

EPWM12\_B IO config register.

Return to [Summary Table](#)

**Table 2-1796. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0110h       |

**Figure 2-598. IOMUX\_EPWM12\_B\_CFG\_REG Name Register**

| 31          | 30                      | 29                 | 28                   | 27       | 26  | 25       | 24  |
|-------------|-------------------------|--------------------|----------------------|----------|-----|----------|-----|
| RSVD        | RSVD                    | RESERVED           |                      |          |     |          |     |
|             |                         | NONE               |                      |          |     |          |     |
| 0h          | 0h                      | 0h                 |                      |          |     |          |     |
| 23          | 22                      | 21                 | 20                   | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVE<br>RRIDE_SEL | ICSSM_GPIO_<br>SEL | INP_INV_SEL          | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                     | R/W                | R/W                  | R/W      |     | R/W      |     |
| 0h          | 0h                      | 0h                 | 0h                   | 0h       |     | 0h       |     |
| 15          | 14                      | 13                 | 12                   | 11       | 10  | 9        | 8   |
| RESERVED    |                         |                    |                      |          | SC1 | PUPDSEL  | PE  |
| NONE        |                         |                    |                      |          | R/W | R/W      | R/W |
| 0h          |                         |                    |                      |          | 1h  | 0h       | 1h  |
| 7           | 6                       | 5                  | 4                    | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_<br>CTRL    | IE_OVERRIDE        | IE_OVERRIDE_<br>CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                     | R/W                | R/W                  | R/W      |     |          |     |
| 1h          | 1h                      | 1h                 | 1h                   | 7h       |     |          |     |

**Table 2-1798. IOMUX\_EPWM12\_B\_CFG\_REG Register Field Descriptions**

| Bit   | Field                   | Type | Reset | Description                                                                                                                                                               |
|-------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |
| 22    | SAFETY_OVERRIDE_SE<br>L | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety<br>override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL          | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal<br>GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL             | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                     |
| 19:18 | QUAL_SEL                | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                           |
| 17:16 | GPIO_SEL                | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                              |
| 15:11 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |



**Table 2-1798. IOMUX\_EPWM12\_B\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.70 IOMUX\_EPWM13\_A\_CFG\_REG Register

### 1 IOMUX\_EPWM13\_A\_CFG\_REG Register (Offset = 114h) [reset = 5F7h]

EPWM13\_A IO config register.

Return to [Summary Table](#)

**Table 2-1799. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0114h       |

**Figure 2-599. IOMUX\_EPWM13\_A\_CFG\_REG Name Register**

| 31          | 30                      | 29                 | 28                   | 27       | 26  | 25       | 24  |
|-------------|-------------------------|--------------------|----------------------|----------|-----|----------|-----|
| RSVD        | RSVD                    | RESERVED           |                      |          |     |          |     |
|             |                         | NONE               |                      |          |     |          |     |
| 0h          | 0h                      | 0h                 |                      |          |     |          |     |
| 23          | 22                      | 21                 | 20                   | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVE<br>RRIDE_SEL | ICSSM_GPIO_<br>SEL | INP_INV_SEL          | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                     | R/W                | R/W                  | R/W      |     | R/W      |     |
| 0h          | 0h                      | 0h                 | 0h                   | 0h       |     | 0h       |     |
| 15          | 14                      | 13                 | 12                   | 11       | 10  | 9        | 8   |
| RESERVED    |                         |                    |                      |          | SC1 | PUPDSEL  | PE  |
| NONE        |                         |                    |                      |          | R/W | R/W      | R/W |
| 0h          |                         |                    |                      |          | 1h  | 0h       | 1h  |
| 7           | 6                       | 5                  | 4                    | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_<br>CTRL    | IE_OVERRIDE        | IE_OVERRIDE_<br>CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                     | R/W                | R/W                  | R/W      |     |          |     |
| 1h          | 1h                      | 1h                 | 1h                   | 7h       |     |          |     |

**Table 2-1801. IOMUX\_EPWM13\_A\_CFG\_REG Register Field Descriptions**

| Bit   | Field                   | Type | Reset | Description                                                                                                                                                               |
|-------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |
| 22    | SAFETY_OVERRIDE_SE<br>L | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety<br>override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL          | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal<br>GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL             | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                     |
| 19:18 | QUAL_SEL                | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                           |
| 17:16 | GPIO_SEL                | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                              |
| 15:11 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |

**Table 2-1801. IOMUX\_EPWM13\_A\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.71 IOMUX\_EPWM13\_B\_CFG\_REG Register

#### 1 IOMUX\_EPWM13\_B\_CFG\_REG Register (Offset = 118h) [reset = 5F7h]

EPWM13\_B IO config register.

Return to [Summary Table](#)

**Table 2-1802. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0118h       |

**Figure 2-600. IOMUX\_EPWM13\_B\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1804. IOMUX\_EPWM13\_B\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1804. IOMUX\_EPWM13\_B\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.72 IOMUX\_EPWM14\_A\_CFG\_REG Register

### 1 IOMUX\_EPWM14\_A\_CFG\_REG Register (Offset = 11Ch) [reset = 5F7h]

EPWM14\_A IO config register.

Return to [Summary Table](#)

**Table 2-1805. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 011Ch       |

**Figure 2-601. IOMUX\_EPWM14\_A\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1807. IOMUX\_EPWM14\_A\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1807. IOMUX\_EPWM14\_A\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.73 IOMUX\_EPWM14\_B\_CFG\_REG Register

#### 1 IOMUX\_EPWM14\_B\_CFG\_REG Register (Offset = 120h) [reset = 5F7h]

EPWM14\_B IO config register.

Return to [Summary Table](#)

**Table 2-1808. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0120h       |

**Figure 2-602. IOMUX\_EPWM14\_B\_CFG\_REG Name Register**

| 31          | 30                      | 29                 | 28                   | 27       | 26  | 25       | 24  |
|-------------|-------------------------|--------------------|----------------------|----------|-----|----------|-----|
| RSVD        | RSVD                    | RESERVED           |                      |          |     |          |     |
|             |                         | NONE               |                      |          |     |          |     |
| 0h          | 0h                      | 0h                 |                      |          |     |          |     |
| 23          | 22                      | 21                 | 20                   | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVE<br>RRIDE_SEL | ICSSM_GPIO_<br>SEL | INP_INV_SEL          | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                     | R/W                | R/W                  | R/W      |     | R/W      |     |
| 0h          | 0h                      | 0h                 | 0h                   | 0h       |     | 0h       |     |
| 15          | 14                      | 13                 | 12                   | 11       | 10  | 9        | 8   |
| RESERVED    |                         |                    |                      |          | SC1 | PUPDSEL  | PE  |
| NONE        |                         |                    |                      |          | R/W | R/W      | R/W |
| 0h          |                         |                    |                      |          | 1h  | 0h       | 1h  |
| 7           | 6                       | 5                  | 4                    | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_<br>CTRL    | IE_OVERRIDE        | IE_OVERRIDE_<br>CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                     | R/W                | R/W                  | R/W      |     |          |     |
| 1h          | 1h                      | 1h                 | 1h                   | 7h       |     |          |     |

**Table 2-1810. IOMUX\_EPWM14\_B\_CFG\_REG Register Field Descriptions**

| Bit   | Field                   | Type | Reset | Description                                                                                                                                                               |
|-------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |
| 22    | SAFETY_OVERRIDE_SE<br>L | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety<br>override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL          | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal<br>GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL             | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                     |
| 19:18 | QUAL_SEL                | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                           |
| 17:16 | GPIO_SEL                | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                              |
| 15:11 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |



**Table 2-1810. IOMUX\_EPWM14\_B\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.74 IOMUX\_EPWM15\_A\_CFG\_REG Register

### 1 IOMUX\_EPWM15\_A\_CFG\_REG Register (Offset = 124h) [reset = 5F7h]

EPWM15\_A IO config register.

Return to [Summary Table](#)

**Table 2-1811. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0124h       |

**Figure 2-603. IOMUX\_EPWM15\_A\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1813. IOMUX\_EPWM15\_A\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1813. IOMUX\_EPWM15\_A\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.75 IOMUX\_EPWM15\_B\_CFG\_REG Register

#### 1 IOMUX\_EPWM15\_B\_CFG\_REG Register (Offset = 128h) [reset = 5F7h]

EPWM15\_B IO config register.

Return to [Summary Table](#)

**Table 2-1814. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0128h       |

**Figure 2-604. IOMUX\_EPWM15\_B\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1816. IOMUX\_EPWM15\_B\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1816. IOMUX\_EPWM15\_B\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.76 IOMUX\_UART1\_RXD\_CFG\_REG Register

### 1 IOMUX\_UART1\_RXD\_CFG\_REG Register (Offset = 12Ch) [reset = 5F7h]

UART1\_RXD IO config register.

Return to [Summary Table](#)

**Table 2-1817. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 012Ch       |

**Figure 2-605. IOMUX\_UART1\_RXD\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1819. IOMUX\_UART1\_RXD\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1819. IOMUX\_UART1\_RXD\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.77 IOMUX\_UART1\_TXD\_CFG\_REG Register

#### 1 IOMUX\_UART1\_TXD\_CFG\_REG Register (Offset = 130h) [reset = 5F7h]

UART1\_TXD IO config register.

Return to [Summary Table](#)

**Table 2-1820. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0130h       |

**Figure 2-606. IOMUX\_UART1\_TXD\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1822. IOMUX\_UART1\_TXD\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1822. IOMUX\_UART1\_TXD\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.78 IOMUX\_MMC0\_CLK\_CFG\_REG Register

#### 1 IOMUX\_MMC0\_CLK\_CFG\_REG Register (Offset = 134h) [reset = 5F7h]

MMC0\_CLK IO config register.

Return to [Summary Table](#)

**Table 2-1823. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0134h       |

**Figure 2-607. IOMUX\_MMC0\_CLK\_CFG\_REG Name Register**

| 31          | 30                      | 29                 | 28                   | 27       | 26  | 25       | 24  |
|-------------|-------------------------|--------------------|----------------------|----------|-----|----------|-----|
| RSVD        | RSVD                    | RESERVED           |                      |          |     |          |     |
|             |                         | NONE               |                      |          |     |          |     |
| 0h          | 0h                      | 0h                 |                      |          |     |          |     |
| 23          | 22                      | 21                 | 20                   | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVE<br>RRIDE_SEL | ICSSM_GPIO_<br>SEL | INP_INV_SEL          | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                     | R/W                | R/W                  | R/W      |     | R/W      |     |
| 0h          | 0h                      | 0h                 | 0h                   | 0h       |     | 0h       |     |
| 15          | 14                      | 13                 | 12                   | 11       | 10  | 9        | 8   |
| RESERVED    |                         |                    |                      |          | SC1 | PUPDSEL  | PE  |
| NONE        |                         |                    |                      |          | R/W | R/W      | R/W |
| 0h          |                         |                    |                      |          | 1h  | 0h       | 1h  |
| 7           | 6                       | 5                  | 4                    | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_<br>CTRL    | IE_OVERRIDE        | IE_OVERRIDE_<br>CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                     | R/W                | R/W                  | R/W      |     |          |     |
| 1h          | 1h                      | 1h                 | 1h                   | 7h       |     |          |     |

**Table 2-1825. IOMUX\_MMC0\_CLK\_CFG\_REG Register Field Descriptions**

| Bit   | Field                   | Type | Reset | Description                                                                                                                                                               |
|-------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |
| 22    | SAFETY_OVERRIDE_SE<br>L | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety<br>override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL          | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal<br>GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL             | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                     |
| 19:18 | QUAL_SEL                | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                           |
| 17:16 | GPIO_SEL                | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                              |
| 15:11 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |

**Table 2-1825. IOMUX\_MMC0\_CLK\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.79 IOMUX\_MMC0\_CMD\_CFG\_REG Register

### 1 IOMUX\_MMC0\_CMD\_CFG\_REG Register (Offset = 138h) [reset = 5F7h]

MMC0\_CMD IO config register.

Return to [Summary Table](#)

**Table 2-1826. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0138h       |

**Figure 2-608. IOMUX\_MMC0\_CMD\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1828. IOMUX\_MMC0\_CMD\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1828. IOMUX\_MMC0\_CMD\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.80 IOMUX\_MMC0\_D0\_CFG\_REG Register

### 1 IOMUX\_MMC0\_D0\_CFG\_REG Register (Offset = 13Ch) [reset = 5F7h]

MMC0\_D0 IO config register.

Return to [Summary Table](#)

**Table 2-1829. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 013Ch       |

**Figure 2-609. IOMUX\_MMC0\_D0\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1831. IOMUX\_MMC0\_D0\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1831. IOMUX\_MMC0\_D0\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.81 IOMUX\_MMC0\_D1\_CFG\_REG Register

#### 1 IOMUX\_MMC0\_D1\_CFG\_REG Register (Offset = 140h) [reset = 5F7h]

MMC0\_D1 IO config register.

Return to [Summary Table](#)

**Table 2-1832. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0140h       |

**Figure 2-610. IOMUX\_MMC0\_D1\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1834. IOMUX\_MMC0\_D1\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1834. IOMUX\_MMC0\_D1\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.82 IOMUX\_MMC0\_D2\_CFG\_REG Register

### 1 IOMUX\_MMC0\_D2\_CFG\_REG Register (Offset = 144h) [reset = 5F7h]

MMC0\_D2 IO config register.

Return to [Summary Table](#)

**Table 2-1835. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0144h       |

**Figure 2-611. IOMUX\_MMC0\_D2\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1837. IOMUX\_MMC0\_D2\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1837. IOMUX\_MMC0\_D2\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.83 IOMUX\_MMC0\_D3\_CFG\_REG Register

#### 1 IOMUX\_MMC0\_D3\_CFG\_REG Register (Offset = 148h) [reset = 5F7h]

MMC0\_D3 IO config register.

Return to [Summary Table](#)

**Table 2-1838. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0148h       |

**Figure 2-612. IOMUX\_MMC0\_D3\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1840. IOMUX\_MMC0\_D3\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1840. IOMUX\_MMC0\_D3\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.84 IOMUX\_MMC0\_WP\_CFG\_REG Register

### 1 IOMUX\_MMC0\_WP\_CFG\_REG Register (Offset = 14Ch) [reset = 5F7h]

MMC0\_WP IO config register.

Return to [Summary Table](#)

**Table 2-1841. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 014Ch       |

**Figure 2-613. IOMUX\_MMC0\_WP\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1843. IOMUX\_MMC0\_WP\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1843. IOMUX\_MMC0\_WP\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.85 IOMUX\_MMC0\_CD\_CFG\_REG Register

#### 1 IOMUX\_MMC0\_CD\_CFG\_REG Register (Offset = 150h) [reset = 5F7h]

MMC0\_CD IO config register.

Return to [Summary Table](#)

**Table 2-1844. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0150h       |

**Figure 2-614. IOMUX\_MMC0\_CD\_CFG\_REG Name Register**

| 31          | 30                      | 29                 | 28                   | 27       | 26  | 25       | 24  |
|-------------|-------------------------|--------------------|----------------------|----------|-----|----------|-----|
| RSVD        | RSVD                    | RESERVED           |                      |          |     |          |     |
|             |                         | NONE               |                      |          |     |          |     |
| 0h          | 0h                      | 0h                 |                      |          |     |          |     |
| 23          | 22                      | 21                 | 20                   | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVE<br>RRIDE_SEL | ICSSM_GPIO_<br>SEL | INP_INV_SEL          | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                     | R/W                | R/W                  | R/W      |     | R/W      |     |
| 0h          | 0h                      | 0h                 | 0h                   | 0h       |     | 0h       |     |
| 15          | 14                      | 13                 | 12                   | 11       | 10  | 9        | 8   |
| RESERVED    |                         |                    |                      |          | SC1 | PUPDSEL  | PE  |
| NONE        |                         |                    |                      |          | R/W | R/W      | R/W |
| 0h          |                         |                    |                      |          | 1h  | 0h       | 1h  |
| 7           | 6                       | 5                  | 4                    | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_<br>CTRL    | IE_OVERRIDE        | IE_OVERRIDE_<br>CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                     | R/W                | R/W                  | R/W      |     |          |     |
| 1h          | 1h                      | 1h                 | 1h                   | 7h       |     |          |     |

**Table 2-1846. IOMUX\_MMC0\_CD\_CFG\_REG Register Field Descriptions**

| Bit   | Field                   | Type | Reset | Description                                                                                                                                                               |
|-------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |
| 22    | SAFETY_OVERRIDE_SE<br>L | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety<br>override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL          | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal<br>GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL             | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                     |
| 19:18 | QUAL_SEL                | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                           |
| 17:16 | GPIO_SEL                | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                              |
| 15:11 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |



**Table 2-1846. IOMUX\_MMC0\_CD\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.86 IOMUX\_PR0\_MDIO0\_MDIO\_CFG\_REG Register

### 1 IOMUX\_PR0\_MDIO0\_MDIO\_CFG\_REG Register (Offset = 154h) [reset = 5F7h]

PR0\_MDIO0\_MDIO IO config register.

Return to [Summary Table](#)

**Table 2-1847. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0154h       |

**Figure 2-615. IOMUX\_PR0\_MDIO0\_MDIO\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1849. IOMUX\_PR0\_MDIO0\_MDIO\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1849. IOMUX\_PR0\_MDIO0\_MDIO\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.87 IOMUX\_PR0\_MDIO0\_MDC\_CFG\_REG Register

#### 1 IOMUX\_PR0\_MDIO0\_MDC\_CFG\_REG Register (Offset = 158h) [reset = 5F7h]

PR0\_MDIO0\_MDC IO config register.

Return to [Summary Table](#)

**Table 2-1850. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0158h       |

**Figure 2-616. IOMUX\_PR0\_MDIO0\_MDC\_CFG\_REG Name Register**

|             |                     |                |                  |          |     |          |     |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1852. IOMUX\_PR0\_MDIO0\_MDC\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1852. IOMUX\_PRO0\_MDIO0\_MDC\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.88 IOMUX\_PR0\_PRU0\_GPO5\_CFG\_REG Register

#### 1 IOMUX\_PR0\_PRU0\_GPO5\_CFG\_REG Register (Offset = 15Ch) [reset = 5F7h]

PR0\_PRU0\_GPO5 IO config register.

Return to [Summary Table](#)

**Table 2-1853. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 015Ch       |

**Figure 2-617. IOMUX\_PR0\_PRU0\_GPO5\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1855. IOMUX\_PR0\_PRU0\_GPO5\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1855. IOMUX\_PR0\_PRU0\_GPO5\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.89 IOMUX\_PR0\_PRU0\_GPO9\_CFG\_REG Register

#### 1 IOMUX\_PR0\_PRU0\_GPO9\_CFG\_REG Register (Offset = 160h) [reset = 5F7h]

PR0\_PRU0\_GPO9 IO config register.

Return to [Summary Table](#)

**Table 2-1856. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0160h       |

**Figure 2-618. IOMUX\_PR0\_PRU0\_GPO9\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1858. IOMUX\_PR0\_PRU0\_GPO9\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1858. IOMUX\_PR0\_PRU0\_GPO9\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.90 IOMUX\_PR0\_PRU0\_GPO10\_CFG\_REG Register

#### 1 IOMUX\_PR0\_PRU0\_GPO10\_CFG\_REG Register (Offset = 164h) [reset = 5F7h]

PR0\_PRU0\_GPO10 IO config register.

Return to [Summary Table](#)

**Table 2-1859. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0164h       |

**Figure 2-619. IOMUX\_PR0\_PRU0\_GPO10\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1861. IOMUX\_PR0\_PRU0\_GPO10\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1861. IOMUX\_PR0\_PRU0\_GPO10\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.91 IOMUX\_PR0\_PRU0\_GPO8\_CFG\_REG Register

#### 1 IOMUX\_PR0\_PRU0\_GPO8\_CFG\_REG Register (Offset = 168h) [reset = 5F7h]

PR0\_PRU0\_GPO8 IO config register.

Return to [Summary Table](#)

**Table 2-1862. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0168h       |

**Figure 2-620. IOMUX\_PR0\_PRU0\_GPO8\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1864. IOMUX\_PR0\_PRU0\_GPO8\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1864. IOMUX\_PR0\_PRU0\_GPO8\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.92 IOMUX\_PR0\_PRU0\_GPO6\_CFG\_REG Register

### 1 IOMUX\_PR0\_PRU0\_GPO6\_CFG\_REG Register (Offset = 16Ch) [reset = 5F7h]

PR0\_PRU0\_GPO6 IO config register.

Return to [Summary Table](#)

**Table 2-1865. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 016Ch       |

**Figure 2-621. IOMUX\_PR0\_PRU0\_GPO6\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1867. IOMUX\_PR0\_PRU0\_GPO6\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1867. IOMUX\_PR0\_PRU0\_GPO6\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.93 IOMUX\_PR0\_PRU0\_GPO4\_CFG\_REG Register

#### 1 IOMUX\_PR0\_PRU0\_GPO4\_CFG\_REG Register (Offset = 170h) [reset = 5F7h]

PR0\_PRU0\_GPO4 IO config register.

Return to [Summary Table](#)

**Table 2-1868. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0170h       |

**Figure 2-622. IOMUX\_PR0\_PRU0\_GPO4\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1870. IOMUX\_PR0\_PRU0\_GPO4\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1870. IOMUX\_PR0\_PRU0\_GPO4\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.94 IOMUX\_PR0\_PRU0\_GPO0\_CFG\_REG Register

### 1 IOMUX\_PR0\_PRU0\_GPO0\_CFG\_REG Register (Offset = 174h) [reset = 5F7h]

PR0\_PRU0\_GPO0 IO config register.

Return to [Summary Table](#)

**Table 2-1871. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0174h       |

**Figure 2-623. IOMUX\_PR0\_PRU0\_GPO0\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1873. IOMUX\_PR0\_PRU0\_GPO0\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1873. IOMUX\_PR0\_PRU0\_GPO0\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.95 IOMUX\_PR0\_PRU0\_GPO1\_CFG\_REG Register

#### 1 IOMUX\_PR0\_PRU0\_GPO1\_CFG\_REG Register (Offset = 178h) [reset = 5F7h]

PR0\_PRU0\_GPO1 IO config register.

Return to [Summary Table](#)

**Table 2-1874. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0178h       |

**Figure 2-624. IOMUX\_PR0\_PRU0\_GPO1\_CFG\_REG Name Register**

| 31          | 30                      | 29                 | 28                   | 27       | 26  | 25       | 24  |
|-------------|-------------------------|--------------------|----------------------|----------|-----|----------|-----|
| RSVD        | RSVD                    | RESERVED           |                      |          |     |          |     |
|             |                         | NONE               |                      |          |     |          |     |
| 0h          | 0h                      | 0h                 |                      |          |     |          |     |
| 23          | 22                      | 21                 | 20                   | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVE<br>RRIDE_SEL | ICSSM_GPIO_<br>SEL | INP_INV_SEL          | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                     | R/W                | R/W                  | R/W      |     | R/W      |     |
| 0h          | 0h                      | 0h                 | 0h                   | 0h       |     | 0h       |     |
| 15          | 14                      | 13                 | 12                   | 11       | 10  | 9        | 8   |
| RESERVED    |                         |                    |                      |          | SC1 | PUPDSEL  | PE  |
| NONE        |                         |                    |                      |          | R/W | R/W      | R/W |
| 0h          |                         |                    |                      |          | 1h  | 0h       | 1h  |
| 7           | 6                       | 5                  | 4                    | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_<br>CTRL    | IE_OVERRIDE        | IE_OVERRIDE_<br>CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                     | R/W                | R/W                  | R/W      |     |          |     |
| 1h          | 1h                      | 1h                 | 1h                   | 7h       |     |          |     |

**Table 2-1876. IOMUX\_PR0\_PRU0\_GPO1\_CFG\_REG Register Field Descriptions**

| Bit   | Field                   | Type | Reset | Description                                                                                                                                                               |
|-------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |
| 22    | SAFETY_OVERRIDE_SE<br>L | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety<br>override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL          | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal<br>GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL             | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                     |
| 19:18 | QUAL_SEL                | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                           |
| 17:16 | GPIO_SEL                | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                              |
| 15:11 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |

**Table 2-1876. IOMUX\_PR0\_PRU0\_GPO1\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.96 IOMUX\_PR0\_PRU0\_GPO2\_CFG\_REG Register

#### 1 IOMUX\_PR0\_PRU0\_GPO2\_CFG\_REG Register (Offset = 17Ch) [reset = 5F7h]

PR0\_PRU0\_GPO2 IO config register.

Return to [Summary Table](#)

**Table 2-1877. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 017Ch       |

**Figure 2-625. IOMUX\_PR0\_PRU0\_GPO2\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1879. IOMUX\_PR0\_PRU0\_GPO2\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1879. IOMUX\_PR0\_PRU0\_GPO2\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.97 IOMUX\_PR0\_PRU0\_GPO3\_CFG\_REG Register

#### 1 IOMUX\_PR0\_PRU0\_GPO3\_CFG\_REG Register (Offset = 180h) [reset = 5F7h]

PR0\_PRU0\_GPO3 IO config register.

Return to [Summary Table](#)

**Table 2-1880. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0180h       |

**Figure 2-626. IOMUX\_PR0\_PRU0\_GPO3\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1882. IOMUX\_PR0\_PRU0\_GPO3\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1882. IOMUX\_PR0\_PRU0\_GPO3\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.98 IOMUX\_PR0\_PRU0\_GPO16\_CFG\_REG Register

### 1 IOMUX\_PR0\_PRU0\_GPO16\_CFG\_REG Register (Offset = 184h) [reset = 5F7h]

PR0\_PRU0\_GPO16 IO config register.

Return to [Summary Table](#)

**Table 2-1883. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0184h       |

**Figure 2-627. IOMUX\_PR0\_PRU0\_GPO16\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1885. IOMUX\_PR0\_PRU0\_GPO16\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1885. IOMUX\_PR0\_PRU0\_GPO16\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.99 IOMUX\_PR0\_PRU0\_GPO15\_CFG\_REG Register

#### 1 IOMUX\_PR0\_PRU0\_GPO15\_CFG\_REG Register (Offset = 188h) [reset = 5F7h]

PR0\_PRU0\_GPO15 IO config register.

Return to [Summary Table](#)

**Table 2-1886. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0188h       |

**Figure 2-628. IOMUX\_PR0\_PRU0\_GPO15\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1888. IOMUX\_PR0\_PRU0\_GPO15\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1888. IOMUX\_PR0\_PRU0\_GPO15\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.100 IOMUX\_PR0\_PRU0\_GPO11\_CFG\_REG Register

#### 1 IOMUX\_PR0\_PRU0\_GPO11\_CFG\_REG Register (Offset = 18Ch) [reset = 5F7h]

PR0\_PRU0\_GPO11 IO config register.

Return to [Summary Table](#)

**Table 2-1889. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 018Ch       |

**Figure 2-629. IOMUX\_PR0\_PRU0\_GPO11\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1891. IOMUX\_PR0\_PRU0\_GPO11\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1891. IOMUX\_PR0\_PRU0\_GPO11\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.101 IOMUX\_PR0\_PRU0\_GPO12\_CFG\_REG Register

#### 1 IOMUX\_PR0\_PRU0\_GPO12\_CFG\_REG Register (Offset = 190h) [reset = 5F7h]

PR0\_PRU0\_GPO12 IO config register.

Return to [Summary Table](#)

**Table 2-1892. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0190h       |

**Figure 2-630. IOMUX\_PR0\_PRU0\_GPO12\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1894. IOMUX\_PR0\_PRU0\_GPO12\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1894. IOMUX\_PR0\_PRU0\_GPO12\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.102 IOMUX\_PR0\_PRU0\_GPO13\_CFG\_REG Register

#### 1 IOMUX\_PR0\_PRU0\_GPO13\_CFG\_REG Register (Offset = 194h) [reset = 5F7h]

PR0\_PRU0\_GPO13 IO config register.

Return to [Summary Table](#)

**Table 2-1895. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0194h       |

**Figure 2-631. IOMUX\_PR0\_PRU0\_GPO13\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1897. IOMUX\_PR0\_PRU0\_GPO13\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1897. IOMUX\_PR0\_PRU0\_GPO13\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.103 IOMUX\_PR0\_PRU0\_GPO14\_CFG\_REG Register

#### 1 IOMUX\_PR0\_PRU0\_GPO14\_CFG\_REG Register (Offset = 198h) [reset = 5F7h]

PR0\_PRU0\_GPO14 IO config register.

Return to [Summary Table](#)

**Table 2-1898. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0198h       |

**Figure 2-632. IOMUX\_PR0\_PRU0\_GPO14\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1900. IOMUX\_PR0\_PRU0\_GPO14\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1900. IOMUX\_PR0\_PRU0\_GPO14\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.104 IOMUX\_PR0\_PRU1\_GPO5\_CFG\_REG Register

#### 1 IOMUX\_PR0\_PRU1\_GPO5\_CFG\_REG Register (Offset = 19Ch) [reset = 5F7h]

PR0\_PRU1\_GPO5 IO config register.

Return to [Summary Table](#)

**Table 2-1901. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 019Ch       |

**Figure 2-633. IOMUX\_PR0\_PRU1\_GPO5\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1903. IOMUX\_PR0\_PRU1\_GPO5\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1903. IOMUX\_PR0\_PRU1\_GPO5\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.105 IOMUX\_PR0\_PRU1\_GPO9\_CFG\_REG Register

#### 1 IOMUX\_PR0\_PRU1\_GPO9\_CFG\_REG Register (Offset = 1A0h) [reset = 5F7h]

PR0\_PRU1\_GPO9 IO config register.

Return to [Summary Table](#)

**Table 2-1904. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 01A0h       |

**Figure 2-634. IOMUX\_PR0\_PRU1\_GPO9\_CFG\_REG Name Register**

| 31          | 30                      | 29                 | 28                   | 27       | 26  | 25       | 24  |
|-------------|-------------------------|--------------------|----------------------|----------|-----|----------|-----|
| RSVD        | RSVD                    | RESERVED           |                      |          |     |          |     |
|             |                         | NONE               |                      |          |     |          |     |
| 0h          | 0h                      | 0h                 |                      |          |     |          |     |
| 23          | 22                      | 21                 | 20                   | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVE<br>RRIDE_SEL | ICSSM_GPIO_<br>SEL | INP_INV_SEL          | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                     | R/W                | R/W                  | R/W      |     | R/W      |     |
| 0h          | 0h                      | 0h                 | 0h                   | 0h       |     | 0h       |     |
| 15          | 14                      | 13                 | 12                   | 11       | 10  | 9        | 8   |
| RESERVED    |                         |                    |                      |          | SC1 | PUPDSEL  | PE  |
| NONE        |                         |                    |                      |          | R/W | R/W      | R/W |
| 0h          |                         |                    |                      |          | 1h  | 0h       | 1h  |
| 7           | 6                       | 5                  | 4                    | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_<br>CTRL    | IE_OVERRIDE        | IE_OVERRIDE_<br>CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                     | R/W                | R/W                  | R/W      |     |          |     |
| 1h          | 1h                      | 1h                 | 1h                   | 7h       |     |          |     |

**Table 2-1906. IOMUX\_PR0\_PRU1\_GPO9\_CFG\_REG Register Field Descriptions**

| Bit   | Field                   | Type | Reset | Description                                                                                                                                                               |
|-------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |
| 22    | SAFETY_OVERRIDE_SE<br>L | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety<br>override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL          | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal<br>GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL             | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                     |
| 19:18 | QUAL_SEL                | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                           |
| 17:16 | GPIO_SEL                | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                              |
| 15:11 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |



**Table 2-1906. IOMUX\_PR0\_PRU1\_GPO9\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.106 IOMUX\_PR0\_PRU1\_GPO10\_CFG\_REG Register

#### 1 IOMUX\_PR0\_PRU1\_GPO10\_CFG\_REG Register (Offset = 1A4h) [reset = 5F7h]

PR0\_PRU1\_GPO10 IO config register.

Return to [Summary Table](#)

**Table 2-1907. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 01A4h       |

**Figure 2-635. IOMUX\_PR0\_PRU1\_GPO10\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1909. IOMUX\_PR0\_PRU1\_GPO10\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1909. IOMUX\_PR0\_PRU1\_GPO10\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.107 IOMUX\_PR0\_PRU1\_GPO8\_CFG\_REG Register

#### 1 IOMUX\_PR0\_PRU1\_GPO8\_CFG\_REG Register (Offset = 1A8h) [reset = 5F7h]

PR0\_PRU1\_GPO8 IO config register.

Return to [Summary Table](#)

**Table 2-1910. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 01A8h       |

**Figure 2-636. IOMUX\_PR0\_PRU1\_GPO8\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1912. IOMUX\_PR0\_PRU1\_GPO8\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1912. IOMUX\_PR0\_PRU1\_GPO8\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.108 IOMUX\_PR0\_PRU1\_GPO6\_CFG\_REG Register

#### 1 IOMUX\_PR0\_PRU1\_GPO6\_CFG\_REG Register (Offset = 1ACh) [reset = 5F7h]

PR0\_PRU1\_GPO6 IO config register.

Return to [Summary Table](#)

**Table 2-1913. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 01ACh       |

**Figure 2-637. IOMUX\_PR0\_PRU1\_GPO6\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1915. IOMUX\_PR0\_PRU1\_GPO6\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1915. IOMUX\_PR0\_PRU1\_GPO6\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.109 IOMUX\_PR0\_PRU1\_GPO4\_CFG\_REG Register

#### 1 IOMUX\_PR0\_PRU1\_GPO4\_CFG\_REG Register (Offset = 1B0h) [reset = 5F7h]

PR0\_PRU1\_GPO4 IO config register.

Return to [Summary Table](#)

**Table 2-1916. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 01B0h       |

**Figure 2-638. IOMUX\_PR0\_PRU1\_GPO4\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1918. IOMUX\_PR0\_PRU1\_GPO4\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1918. IOMUX\_PR0\_PRU1\_GPO4\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.110 IOMUX\_PR0\_PRU1\_GPO0\_CFG\_REG Register

#### 1 IOMUX\_PR0\_PRU1\_GPO0\_CFG\_REG Register (Offset = 1B4h) [reset = 5F7h]

PR0\_PRU1\_GPO0 IO config register.

Return to [Summary Table](#)

**Table 2-1919. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 01B4h       |

**Figure 2-639. IOMUX\_PR0\_PRU1\_GPO0\_CFG\_REG Name Register**

|             |                     |                |                  |          |     |          |     |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1921. IOMUX\_PR0\_PRU1\_GPO0\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1921. IOMUX\_PR0\_PRU1\_GPO0\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.111 IOMUX\_PR0\_PRU1\_GPO1\_CFG\_REG Register

### 1 IOMUX\_PR0\_PRU1\_GPO1\_CFG\_REG Register (Offset = 1B8h) [reset = 5F7h]

PR0\_PRU1\_GPO1 IO config register.

Return to [Summary Table](#)

**Table 2-1922. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 01B8h       |

**Figure 2-640. IOMUX\_PR0\_PRU1\_GPO1\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1924. IOMUX\_PR0\_PRU1\_GPO1\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1924. IOMUX\_PR0\_PRU1\_GPO1\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.112 IOMUX\_PR0\_PRU1\_GPO2\_CFG\_REG Register

### 1 IOMUX\_PR0\_PRU1\_GPO2\_CFG\_REG Register (Offset = 1BCh) [reset = 5F7h]

PR0\_PRU1\_GPO2 IO config register.

Return to [Summary Table](#)

**Table 2-1925. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 01BCh       |

**Figure 2-641. IOMUX\_PR0\_PRU1\_GPO2\_CFG\_REG Name Register**

|             |                         |                    |                      |          |     |          |     |
|-------------|-------------------------|--------------------|----------------------|----------|-----|----------|-----|
| 31          | 30                      | 29                 | 28                   | 27       | 26  | 25       | 24  |
| RSVD        | RSVD                    | RESERVED           |                      |          |     |          |     |
|             |                         | NONE               |                      |          |     |          |     |
| 0h          | 0h                      | 0h                 |                      |          |     |          |     |
| 23          | 22                      | 21                 | 20                   | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVE<br>RRIDE_SEL | ICSSM_GPIO_<br>SEL | INP_INV_SEL          | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                     | R/W                | R/W                  | R/W      |     | R/W      |     |
| 0h          | 0h                      | 0h                 | 0h                   | 0h       |     | 0h       |     |
| 15          | 14                      | 13                 | 12                   | 11       | 10  | 9        | 8   |
| RESERVED    |                         |                    |                      |          | SC1 | PUPDSEL  | PE  |
| NONE        |                         |                    |                      |          | R/W | R/W      | R/W |
| 0h          |                         |                    |                      |          | 1h  | 0h       | 1h  |
| 7           | 6                       | 5                  | 4                    | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_<br>CTRL    | IE_OVERRIDE        | IE_OVERRIDE_<br>CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                     | R/W                | R/W                  | R/W      |     |          |     |
| 1h          | 1h                      | 1h                 | 1h                   | 7h       |     |          |     |

**Table 2-1927. IOMUX\_PR0\_PRU1\_GPO2\_CFG\_REG Register Field Descriptions**

| Bit   | Field                   | Type | Reset | Description                                                                                                                                                               |
|-------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |
| 22    | SAFETY_OVERRIDE_SE<br>L | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety<br>override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL          | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal<br>GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL             | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                     |
| 19:18 | QUAL_SEL                | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                           |
| 17:16 | GPIO_SEL                | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                              |
| 15:11 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |

**Table 2-1927. IOMUX\_PR0\_PRU1\_GPO2\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.113 IOMUX\_PR0\_PRU1\_GPO3\_CFG\_REG Register

#### 1 IOMUX\_PR0\_PRU1\_GPO3\_CFG\_REG Register (Offset = 1C0h) [reset = 5F7h]

PR0\_PRU1\_GPO3 IO config register.

Return to [Summary Table](#)

**Table 2-1928. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 01C0h       |

**Figure 2-642. IOMUX\_PR0\_PRU1\_GPO3\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1930. IOMUX\_PR0\_PRU1\_GPO3\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1930. IOMUX\_PR0\_PRU1\_GPO3\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.114 IOMUX\_PR0\_PRU1\_GPO16\_CFG\_REG Register

### 1 IOMUX\_PR0\_PRU1\_GPO16\_CFG\_REG Register (Offset = 1C4h) [reset = 5F7h]

PR0\_PRU1\_GPO16 IO config register.

Return to [Summary Table](#)

**Table 2-1931. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 01C4h       |

**Figure 2-643. IOMUX\_PR0\_PRU1\_GPO16\_CFG\_REG Name Register**

|             |                     |                |                  |          |     |          |     |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1933. IOMUX\_PR0\_PRU1\_GPO16\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1933. IOMUX\_PR0\_PRU1\_GPO16\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.115 IOMUX\_PR0\_PRU1\_GPO15\_CFG\_REG Register

### 1 IOMUX\_PR0\_PRU1\_GPO15\_CFG\_REG Register (Offset = 1C8h) [reset = 5F7h]

PR0\_PRU1\_GPO15 IO config register.

Return to [Summary Table](#)

**Table 2-1934. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 01C8h       |

**Figure 2-644. IOMUX\_PR0\_PRU1\_GPO15\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1936. IOMUX\_PR0\_PRU1\_GPO15\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1936. IOMUX\_PR0\_PRU1\_GPO15\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.116 IOMUX\_PR0\_PRU1\_GPO11\_CFG\_REG Register

### 1 IOMUX\_PR0\_PRU1\_GPO11\_CFG\_REG Register (Offset = 1CCh) [reset = 5F7h]

PR0\_PRU1\_GPO11 IO config register.

Return to [Summary Table](#)

**Table 2-1937. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 01CCh       |

**Figure 2-645. IOMUX\_PR0\_PRU1\_GPO11\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1939. IOMUX\_PR0\_PRU1\_GPO11\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1939. IOMUX\_PR0\_PRU1\_GPO11\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.117 IOMUX\_PR0\_PRU1\_GPO12\_CFG\_REG Register

### 1 IOMUX\_PR0\_PRU1\_GPO12\_CFG\_REG Register (Offset = 1D0h) [reset = 5F7h]

PR0\_PRU1\_GPO12 IO config register.

Return to [Summary Table](#)

**Table 2-1940. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 01D0h       |

**Figure 2-646. IOMUX\_PR0\_PRU1\_GPO12\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1942. IOMUX\_PR0\_PRU1\_GPO12\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1942. IOMUX\_PR0\_PRU1\_GPO12\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.118 IOMUX\_PR0\_PRU1\_GPO13\_CFG\_REG Register

### 1 IOMUX\_PR0\_PRU1\_GPO13\_CFG\_REG Register (Offset = 1D4h) [reset = 5F7h]

PR0\_PRU1\_GPO13 IO config register.

Return to [Summary Table](#)

**Table 2-1943. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 01D4h       |

**Figure 2-647. IOMUX\_PR0\_PRU1\_GPO13\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1945. IOMUX\_PR0\_PRU1\_GPO13\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1945. IOMUX\_PR0\_PRU1\_GPO13\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.119 IOMUX\_PR0\_PRU1\_GPO14\_CFG\_REG Register

### 1 IOMUX\_PR0\_PRU1\_GPO14\_CFG\_REG Register (Offset = 1D8h) [reset = 5F7h]

PR0\_PRU1\_GPO14 IO config register.

Return to [Summary Table](#)

**Table 2-1946. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 01D8h       |

**Figure 2-648. IOMUX\_PR0\_PRU1\_GPO14\_CFG\_REG Name Register**

|             |                     |                |                  |          |     |          |     |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1948. IOMUX\_PR0\_PRU1\_GPO14\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1948. IOMUX\_PR0\_PRU1\_GPO14\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.120 IOMUX\_PR0\_PRU1\_GPO19\_CFG\_REG Register

### 1 IOMUX\_PR0\_PRU1\_GPO19\_CFG\_REG Register (Offset = 1DCh) [reset = 5F7h]

PR0\_PRU1\_GPO19 IO config register.

Return to [Summary Table](#)

**Table 2-1949. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 01DCh       |

**Figure 2-649. IOMUX\_PR0\_PRU1\_GPO19\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1951. IOMUX\_PR0\_PRU1\_GPO19\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1951. IOMUX\_PR0\_PRU1\_GPO19\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.121 IOMUX\_PR0\_PRU1\_GPO18\_CFG\_REG Register

#### 1 IOMUX\_PR0\_PRU1\_GPO18\_CFG\_REG Register (Offset = 1E0h) [reset = 5F7h]

PR0\_PRU1\_GPO18 IO config register.

Return to [Summary Table](#)

**Table 2-1952. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 01E0h       |

**Figure 2-650. IOMUX\_PR0\_PRU1\_GPO18\_CFG\_REG Name Register**

|             |                     |                |                  |          |     |          |     |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1954. IOMUX\_PR0\_PRU1\_GPO18\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1954. IOMUX\_PR0\_PRU1\_GPO18\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.122 IOMUX\_EXT\_REFCLK0\_CFG\_REG Register

### 1 IOMUX\_EXT\_REFCLK0\_CFG\_REG Register (Offset = 1E4h) [reset = 5F7h]

EXT\_REFCLK0 IO config register.

Return to [Summary Table](#)

**Table 2-1955. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 01E4h       |

**Figure 2-651. IOMUX\_EXT\_REFCLK0\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1957. IOMUX\_EXT\_REFCLK0\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1957. IOMUX\_EXT\_REFCLK0\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.123 IOMUX\_SDFM0\_CLK0\_CFG\_REG Register

#### 1 IOMUX\_SDFM0\_CLK0\_CFG\_REG Register (Offset = 1E8h) [reset = 5F7h]

SDFM0\_CLK0 IO config register.

Return to [Summary Table](#)

**Table 2-1958. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 01E8h       |

**Figure 2-652. IOMUX\_SDFM0\_CLK0\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1960. IOMUX\_SDFM0\_CLK0\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1960. IOMUX\_SDFM0\_CLK0\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.124 IOMUX\_SDFM0\_D0\_CFG\_REG Register

#### 1 IOMUX\_SDFM0\_D0\_CFG\_REG Register (Offset = 1ECh) [reset = 5F7h]

SDFM0\_D0 IO config register.

Return to [Summary Table](#)

**Table 2-1961. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 01ECh       |

**Figure 2-653. IOMUX\_SDFM0\_D0\_CFG\_REG Name Register**

| 31          | 30                      | 29                 | 28                   | 27       | 26  | 25       | 24  |
|-------------|-------------------------|--------------------|----------------------|----------|-----|----------|-----|
| RSVD        | RSVD                    | RESERVED           |                      |          |     |          |     |
|             |                         | NONE               |                      |          |     |          |     |
| 0h          | 0h                      | 0h                 |                      |          |     |          |     |
| 23          | 22                      | 21                 | 20                   | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVE<br>RRIDE_SEL | ICSSM_GPIO_<br>SEL | INP_INV_SEL          | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                     | R/W                | R/W                  | R/W      |     | R/W      |     |
| 0h          | 0h                      | 0h                 | 0h                   | 0h       |     | 0h       |     |
| 15          | 14                      | 13                 | 12                   | 11       | 10  | 9        | 8   |
| RESERVED    |                         |                    |                      |          | SC1 | PUPDSEL  | PE  |
| NONE        |                         |                    |                      |          | R/W | R/W      | R/W |
| 0h          |                         |                    |                      |          | 1h  | 0h       | 1h  |
| 7           | 6                       | 5                  | 4                    | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_<br>CTRL    | IE_OVERRIDE        | IE_OVERRIDE_<br>CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                     | R/W                | R/W                  | R/W      |     |          |     |
| 1h          | 1h                      | 1h                 | 1h                   | 7h       |     |          |     |

**Table 2-1963. IOMUX\_SDFM0\_D0\_CFG\_REG Register Field Descriptions**

| Bit   | Field                   | Type | Reset | Description                                                                                                                                                               |
|-------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |
| 22    | SAFETY_OVERRIDE_SE<br>L | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety<br>override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL          | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal<br>GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL             | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                     |
| 19:18 | QUAL_SEL                | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                           |
| 17:16 | GPIO_SEL                | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                              |
| 15:11 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |

**Table 2-1963. IOMUX\_SDFM0\_D0\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.125 IOMUX\_SDFM0\_CLK1\_CFG\_REG Register

#### 1 IOMUX\_SDFM0\_CLK1\_CFG\_REG Register (Offset = 1F0h) [reset = 5F7h]

SDFM0\_CLK1 IO config register.

Return to [Summary Table](#)

**Table 2-1964. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 01F0h       |

**Figure 2-654. IOMUX\_SDFM0\_CLK1\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1966. IOMUX\_SDFM0\_CLK1\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1966. IOMUX\_SDFM0\_CLK1\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.126 IOMUX\_SDFM0\_D1\_CFG\_REG Register

#### 1 IOMUX\_SDFM0\_D1\_CFG\_REG Register (Offset = 1F4h) [reset = 5F7h]

SDFM0\_D1 IO config register.

Return to [Summary Table](#)

**Table 2-1967. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 01F4h       |

**Figure 2-655. IOMUX\_SDFM0\_D1\_CFG\_REG Name Register**

| 31          | 30                      | 29                 | 28                   | 27       | 26  | 25       | 24  |
|-------------|-------------------------|--------------------|----------------------|----------|-----|----------|-----|
| RSVD        | RSVD                    | RESERVED           |                      |          |     |          |     |
|             |                         | NONE               |                      |          |     |          |     |
| 0h          | 0h                      | 0h                 |                      |          |     |          |     |
| 23          | 22                      | 21                 | 20                   | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVE<br>RRIDE_SEL | ICSSM_GPIO_<br>SEL | INP_INV_SEL          | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                     | R/W                | R/W                  | R/W      |     | R/W      |     |
| 0h          | 0h                      | 0h                 | 0h                   | 0h       |     | 0h       |     |
| 15          | 14                      | 13                 | 12                   | 11       | 10  | 9        | 8   |
| RESERVED    |                         |                    |                      |          | SC1 | PUPDSEL  | PE  |
| NONE        |                         |                    |                      |          | R/W | R/W      | R/W |
| 0h          |                         |                    |                      |          | 1h  | 0h       | 1h  |
| 7           | 6                       | 5                  | 4                    | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_<br>CTRL    | IE_OVERRIDE        | IE_OVERRIDE_<br>CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                     | R/W                | R/W                  | R/W      |     |          |     |
| 1h          | 1h                      | 1h                 | 1h                   | 7h       |     |          |     |

**Table 2-1969. IOMUX\_SDFM0\_D1\_CFG\_REG Register Field Descriptions**

| Bit   | Field                   | Type | Reset | Description                                                                                                                                                               |
|-------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |
| 22    | SAFETY_OVERRIDE_SE<br>L | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety<br>override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL          | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal<br>GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL             | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                     |
| 19:18 | QUAL_SEL                | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                           |
| 17:16 | GPIO_SEL                | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                              |
| 15:11 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |

**Table 2-1969. IOMUX\_SDFM0\_D1\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.127 IOMUX\_SDFM0\_CLK2\_CFG\_REG Register

#### 1 IOMUX\_SDFM0\_CLK2\_CFG\_REG Register (Offset = 1F8h) [reset = 5F7h]

SDFM0\_CLK2 IO config register.

Return to [Summary Table](#)

**Table 2-1970. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 01F8h       |

**Figure 2-656. IOMUX\_SDFM0\_CLK2\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1972. IOMUX\_SDFM0\_CLK2\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1972. IOMUX\_SDFM0\_CLK2\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.128 IOMUX\_SDFM0\_D2\_CFG\_REG Register

#### 1 IOMUX\_SDFM0\_D2\_CFG\_REG Register (Offset = 1FCh) [reset = 5F7h]

SDFM0\_D2 IO config register.

Return to [Summary Table](#)

**Table 2-1973. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 01FCh       |

**Figure 2-657. IOMUX\_SDFM0\_D2\_CFG\_REG Name Register**

| 31          | 30                      | 29                 | 28                   | 27       | 26  | 25       | 24  |
|-------------|-------------------------|--------------------|----------------------|----------|-----|----------|-----|
| RSVD        | RSVD                    | RESERVED           |                      |          |     |          |     |
|             |                         | NONE               |                      |          |     |          |     |
| 0h          | 0h                      | 0h                 |                      |          |     |          |     |
| 23          | 22                      | 21                 | 20                   | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVE<br>RRIDE_SEL | ICSSM_GPIO_<br>SEL | INP_INV_SEL          | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                     | R/W                | R/W                  | R/W      |     | R/W      |     |
| 0h          | 0h                      | 0h                 | 0h                   | 0h       |     | 0h       |     |
| 15          | 14                      | 13                 | 12                   | 11       | 10  | 9        | 8   |
| RESERVED    |                         |                    |                      |          | SC1 | PUPDSEL  | PE  |
| NONE        |                         |                    |                      |          | R/W | R/W      | R/W |
| 0h          |                         |                    |                      |          | 1h  | 0h       | 1h  |
| 7           | 6                       | 5                  | 4                    | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_<br>CTRL    | IE_OVERRIDE        | IE_OVERRIDE_<br>CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                     | R/W                | R/W                  | R/W      |     |          |     |
| 1h          | 1h                      | 1h                 | 1h                   | 7h       |     |          |     |

**Table 2-1975. IOMUX\_SDFM0\_D2\_CFG\_REG Register Field Descriptions**

| Bit   | Field                   | Type | Reset | Description                                                                                                                                                               |
|-------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |
| 22    | SAFETY_OVERRIDE_SE<br>L | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety<br>override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL          | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal<br>GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL             | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                     |
| 19:18 | QUAL_SEL                | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                           |
| 17:16 | GPIO_SEL                | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                              |
| 15:11 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |

**Table 2-1975. IOMUX\_SDFM0\_D2\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.129 IOMUX\_SDFM0\_CLK3\_CFG\_REG Register

#### 1 IOMUX\_SDFM0\_CLK3\_CFG\_REG Register (Offset = 200h) [reset = 5F7h]

SDFM0\_CLK3 IO config register.

Return to [Summary Table](#)

**Table 2-1976. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0200h       |

**Figure 2-658. IOMUX\_SDFM0\_CLK3\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1978. IOMUX\_SDFM0\_CLK3\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1978. IOMUX\_SDFM0\_CLK3\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.130 IOMUX\_SDFM0\_D3\_CFG\_REG Register

#### 1 IOMUX\_SDFM0\_D3\_CFG\_REG Register (Offset = 204h) [reset = 5F7h]

SDFM0\_D3 IO config register.

Return to [Summary Table](#)

**Table 2-1979. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0204h       |

**Figure 2-659. IOMUX\_SDFM0\_D3\_CFG\_REG Name Register**

| 31          | 30                      | 29                 | 28                   | 27       | 26  | 25       | 24  |
|-------------|-------------------------|--------------------|----------------------|----------|-----|----------|-----|
| RSVD        | RSVD                    | RESERVED           |                      |          |     |          |     |
|             |                         | NONE               |                      |          |     |          |     |
| 0h          | 0h                      | 0h                 |                      |          |     |          |     |
| 23          | 22                      | 21                 | 20                   | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVE<br>RRIDE_SEL | ICSSM_GPIO_<br>SEL | INP_INV_SEL          | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                     | R/W                | R/W                  | R/W      |     | R/W      |     |
| 0h          | 0h                      | 0h                 | 0h                   | 0h       |     | 0h       |     |
| 15          | 14                      | 13                 | 12                   | 11       | 10  | 9        | 8   |
| RESERVED    |                         |                    |                      |          | SC1 | PUPDSEL  | PE  |
| NONE        |                         |                    |                      |          | R/W | R/W      | R/W |
| 0h          |                         |                    |                      |          | 1h  | 0h       | 1h  |
| 7           | 6                       | 5                  | 4                    | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_<br>CTRL    | IE_OVERRIDE        | IE_OVERRIDE_<br>CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                     | R/W                | R/W                  | R/W      |     |          |     |
| 1h          | 1h                      | 1h                 | 1h                   | 7h       |     |          |     |

**Table 2-1981. IOMUX\_SDFM0\_D3\_CFG\_REG Register Field Descriptions**

| Bit   | Field                   | Type | Reset | Description                                                                                                                                                               |
|-------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |
| 22    | SAFETY_OVERRIDE_SE<br>L | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety<br>override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL          | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal<br>GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL             | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                     |
| 19:18 | QUAL_SEL                | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                           |
| 17:16 | GPIO_SEL                | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                              |
| 15:11 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                  |

**Table 2-1981. IOMUX\_SDFM0\_D3\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.131 IOMUX\_EQEP0\_A\_CFG\_REG Register

#### 1 IOMUX\_EQEP0\_A\_CFG\_REG Register (Offset = 208h) [reset = 5F7h]

EQEP0\_A IO config register.

Return to [Summary Table](#)

**Table 2-1982. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0208h       |

**Figure 2-660. IOMUX\_EQEP0\_A\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1984. IOMUX\_EQEP0\_A\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1984. IOMUX\_EQEP0\_A\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.132 IOMUX\_EQEP0\_B\_CFG\_REG Register

#### 1 IOMUX\_EQEP0\_B\_CFG\_REG Register (Offset = 20Ch) [reset = 5F7h]

EQEP0\_B IO config register.

Return to [Summary Table](#)

**Table 2-1985. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 020Ch       |

**Figure 2-661. IOMUX\_EQEP0\_B\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1987. IOMUX\_EQEP0\_B\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1987. IOMUX\_EQEP0\_B\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.133 IOMUX\_EQEP0\_STROBE\_CFG\_REG Register

#### 1 IOMUX\_EQEP0\_STROBE\_CFG\_REG Register (Offset = 210h) [reset = 5F7h]

EQEP0\_STROBE IO config register.

Return to [Summary Table](#)

**Table 2-1988. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0210h       |

**Figure 2-662. IOMUX\_EQEP0\_STROBE\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1990. IOMUX\_EQEP0\_STROBE\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-1990. IOMUX\_EQEP0\_STROBE\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.134 IOMUX\_EQEP0\_INDEX\_CFG\_REG Register

#### 1 IOMUX\_EQEP0\_INDEX\_CFG\_REG Register (Offset = 214h) [reset = 5F7h]

EQEP0\_INDEX IO config register.

Return to [Summary Table](#)

**Table 2-1991. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0214h       |

**Figure 2-663. IOMUX\_EQEP0\_INDEX\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1993. IOMUX\_EQEP0\_INDEX\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1993. IOMUX\_EQEP0\_INDEX\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.135 IOMUX\_I2C0\_SDA\_CFG\_REG Register

#### 1 IOMUX\_I2C0\_SDA\_CFG\_REG Register (Offset = 218h) [reset = 5F7h]

I2C0\_SDA IO config register.

Return to [Summary Table](#)

**Table 2-1994. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0218h       |

**Figure 2-664. IOMUX\_I2C0\_SDA\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1996. IOMUX\_I2C0\_SDA\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1996. IOMUX\_I2C0\_SDA\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.136 IOMUX\_I2C0\_SCL\_CFG\_REG Register

#### 1 IOMUX\_I2C0\_SCL\_CFG\_REG Register (Offset = 21Ch) [reset = 5F7h]

I2C0\_SCL IO config register.

Return to [Summary Table](#)

**Table 2-1997. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 021Ch       |

**Figure 2-665. IOMUX\_I2C0\_SCL\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-1999. IOMUX\_I2C0\_SCL\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-1999. IOMUX\_I2C0\_SCL\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.137 IOMUX\_MCAN2\_TX\_CFG\_REG Register

#### 1 IOMUX\_MCAN2\_TX\_CFG\_REG Register (Offset = 220h) [reset = 5F7h]

MCAN2\_TX IO config register.

Return to [Summary Table](#)

**Table 2-2000. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0220h       |

**Figure 2-666. IOMUX\_MCAN2\_TX\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-2002. IOMUX\_MCAN2\_TX\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |



**Table 2-2002. IOMUX\_MCAN2\_TX\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.138 IOMUX\_MCAN2\_RX\_CFG\_REG Register

#### 1 IOMUX\_MCAN2\_RX\_CFG\_REG Register (Offset = 224h) [reset = 5F7h]

MCAN2\_RX IO config register.

Return to [Summary Table](#)

**Table 2-2003. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0224h       |

**Figure 2-667. IOMUX\_MCAN2\_RX\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 1h          | 1h                  | 1h             | 1h               | 7h       |     |          |     |

**Table 2-2005. IOMUX\_MCAN2\_RX\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-2005. IOMUX\_MCAN2\_RX\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 7h    | Function select                                                                                                                                                                                                                                                                                                                    |

### 2.4.2.139 IOMUX\_CLKOUT0\_CFG\_REG Register

#### 1 IOMUX\_CLKOUT0\_CFG\_REG Register (Offset = 228h) [reset = 570h]

CLKOUT0 IO config register.

Return to [Summary Table](#)

**Table 2-2006. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0228h       |

**Figure 2-668. IOMUX\_CLKOUT0\_CFG\_REG Name Register**

| 31          | 30                  | 29             | 28               | 27       | 26  | 25       | 24  |
|-------------|---------------------|----------------|------------------|----------|-----|----------|-----|
| RSVD        | RSVD                | RESERVED       |                  |          |     |          |     |
|             |                     | NONE           |                  |          |     |          |     |
| 0h          | 0h                  | 0h             |                  |          |     |          |     |
| 23          | 22                  | 21             | 20               | 19       | 18  | 17       | 16  |
| RESERVED    | SAFETY_OVERRIDE_SEL | ICSSM_GPIO_SEL | INP_INV_SEL      | QUAL_SEL |     | GPIO_SEL |     |
| NONE        | R/W                 | R/W            | R/W              | R/W      |     | R/W      |     |
| 0h          | 0h                  | 0h             | 0h               | 0h       |     | 0h       |     |
| 15          | 14                  | 13             | 12               | 11       | 10  | 9        | 8   |
| RESERVED    |                     |                |                  |          | SC1 | PUPDSEL  | PE  |
| NONE        |                     |                |                  |          | R/W | R/W      | R/W |
| 0h          |                     |                |                  |          | 1h  | 0h       | 1h  |
| 7           | 6                   | 5              | 4                | 3        | 2   | 1        | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL    | IE_OVERRIDE    | IE_OVERRIDE_CTRL | FUNC_SEL |     |          |     |
| R/W         | R/W                 | R/W            | R/W              | R/W      |     |          |     |
| 0h          | 1h                  | 1h             | 1h               | 0h       |     |          |     |

**Table 2-2008. IOMUX\_CLKOUT0\_CFG\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                            |
|-------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:23 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |
| 22    | SAFETY_OVERRIDE_SEL | R/W  | 0h    | mux Select Value to choose between Actual IO pad input and Safety override mux output<br>1 Safety override mux output is selected<br>0 Actual IO pad input is selected |
| 21    | ICSSM_GPIO_SEL      | R/W  | 0h    | mux Select Value to choose between ICSSM_GPIO and normal GPIO<br>1 ICSSM_GPIO is selected<br>0 Normal GPIO is selected                                                 |
| 20    | INP_INV_SEL         | R/W  | 0h    | Select Value for choosing inverted version of PAD input for chip:<br>0 : Non Inverted<br>1 : Inverted                                                                  |
| 19:18 | QUAL_SEL            | R/W  | 0h    | Select Value for choosing input qualifer type for PAD.<br>00 : Sync,<br>01 : 3 Sample qual<br>10 : 6 Samples qual<br>11 : Async                                        |
| 17:16 | GPIO_SEL            | R/W  | 0h    | R5F CPU ownership select for GPIO.<br>0 : GPO0, 1 :GPO1,<br>2 : GPO2, 3:GPO3                                                                                           |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                               |

**Table 2-2008. IOMUX\_CLKOUT0\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                                                                                                              |
| 9   | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                                                                                                         |
| 8   | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                                                                                                             |
| 7   | OE_OVERRIDE      | R/W  | 0h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral.                                                                                        |
| 6   | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                                                                                                                |
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | FUNC_SEL         | R/W  | 0h    | Function select                                                                                                                                                                                                                                                                                                                    |

## 2.4.2.140 IOMUX\_WARMRSTN\_CFG\_REG Register

### 1 IOMUX\_WARMRSTN\_CFG\_REG Register (Offset = 22Ch) [reset = 510h]

WARMRSTn IO config register.

Return to [Summary Table](#)

**Table 2-2009. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 022Ch       |

**Figure 2-669. IOMUX\_WARMRSTN\_CFG\_REG Name Register**

|             |                  |             |                  |          |     |         |     |
|-------------|------------------|-------------|------------------|----------|-----|---------|-----|
| 31          | 30               | 29          | 28               | 27       | 26  | 25      | 24  |
| RESERVED    | RESERVED         |             |                  |          |     |         |     |
| R           | NONE             |             |                  |          |     |         |     |
| 0h          | 0h               |             |                  |          |     |         |     |
| 23          | 22               | 21          | 20               | 19       | 18  | 17      | 16  |
| RESERVED    |                  |             |                  |          |     |         |     |
| NONE        |                  |             |                  |          |     |         |     |
| 0h          |                  |             |                  |          |     |         |     |
| 15          | 14               | 13          | 12               | 11       | 10  | 9       | 8   |
| RESERVED    |                  |             |                  |          | SC1 | PUPDSEL | PE  |
| NONE        |                  |             |                  |          | R/W | R/W     | R/W |
| 0h          |                  |             |                  |          | 1h  | 0h      | 1h  |
| 7           | 6                | 5           | 4                | 3        | 2   | 1       | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL | IE_OVERRIDE | IE_OVERRIDE_CTRL | RESERVED |     |         |     |
| R/W         | R/W              | R/W         | R/W              | NONE     |     |         |     |
| 0h          | 0h               | 0h          | 1h               | 0h       |     |         |     |

**Table 2-2011. IOMUX\_WARMRSTN\_CFG\_REG Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                 |
|-------|------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | RESERVED         | R    | 0h    | Reserved                                                                                                                                                                                                                                    |
| 30:11 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                    |
| 10    | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                       |
| 9     | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                  |
| 8     | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                      |
| 7     | OE_OVERRIDE      | R/W  | 0h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral. |
| 6     | OE_OVERRIDE_CTRL | R/W  | 0h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                         |

**Table 2-2011. IOMUX\_WARMRSTN\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | IE_OVERRIDE      | R/W  | 0h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                           |

### 2.4.2.141 IOMUX\_SAFETY\_ERRORN\_CFG\_REG Register

#### 1 IOMUX\_SAFETY\_ERRORN\_CFG\_REG Register (Offset = 230h) [reset = 410h]

SAFETY\_ERRORn IO config register.

Return to [Summary Table](#)

**Table 2-2012. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0230h       |

**Figure 2-670. IOMUX\_SAFETY\_ERRORN\_CFG\_REG Name Register**

|             |                  |             |                  |          |     |         |     |
|-------------|------------------|-------------|------------------|----------|-----|---------|-----|
| 31          | 30               | 29          | 28               | 27       | 26  | 25      | 24  |
| RESERVED    | RESERVED         |             |                  |          |     |         |     |
| R           | NONE             |             |                  |          |     |         |     |
| 0h          | 0h               |             |                  |          |     |         |     |
| 23          | 22               | 21          | 20               | 19       | 18  | 17      | 16  |
| RESERVED    |                  |             |                  |          |     |         |     |
| NONE        |                  |             |                  |          |     |         |     |
| 0h          |                  |             |                  |          |     |         |     |
| 15          | 14               | 13          | 12               | 11       | 10  | 9       | 8   |
| RESERVED    |                  |             |                  |          | SC1 | PUPDSEL | PE  |
| NONE        |                  |             |                  |          | R/W | R/W     | R/W |
| 0h          |                  |             |                  |          | 1h  | 0h      | 0h  |
| 7           | 6                | 5           | 4                | 3        | 2   | 1       | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL | IE_OVERRIDE | IE_OVERRIDE_CTRL | RESERVED |     |         |     |
| R/W         | R/W              | R/W         | R/W              | NONE     |     |         |     |
| 0h          | 0h               | 0h          | 1h               | 0h       |     |         |     |

**Table 2-2014. IOMUX\_SAFETY\_ERRORN\_CFG\_REG Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                 |
|-------|------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | RESERVED         | R    | 0h    | Reserved                                                                                                                                                                                                                                    |
| 30:11 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                    |
| 10    | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                       |
| 9     | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                  |
| 8     | PE               | R/W  | 0h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                      |
| 7     | OE_OVERRIDE      | R/W  | 0h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral. |
| 6     | OE_OVERRIDE_CTRL | R/W  | 0h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                         |



**Table 2-2014. IOMUX\_SAFETY\_ERRORN\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | IE_OVERRIDE      | R/W  | 0h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                           |

## 2.4.2.142 IOMUX\_TDI\_CFG\_REG Register

### 1 IOMUX\_TDI\_CFG\_REG Register (Offset = 234h) [reset = 6D0h]

TDI IO config register.

Return to [Summary Table](#)

**Table 2-2015. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0234h       |

**Figure 2-671. IOMUX\_TDI\_CFG\_REG Name Register**

|             |                  |             |                  |          |     |         |     |
|-------------|------------------|-------------|------------------|----------|-----|---------|-----|
| 31          | 30               | 29          | 28               | 27       | 26  | 25      | 24  |
| RESERVED    | RESERVED         |             |                  |          |     |         |     |
| R           | NONE             |             |                  |          |     |         |     |
| 0h          | 0h               |             |                  |          |     |         |     |
| 23          | 22               | 21          | 20               | 19       | 18  | 17      | 16  |
| RESERVED    |                  |             |                  |          |     |         |     |
| NONE        |                  |             |                  |          |     |         |     |
| 0h          |                  |             |                  |          |     |         |     |
| 15          | 14               | 13          | 12               | 11       | 10  | 9       | 8   |
| RESERVED    |                  |             |                  |          | SC1 | PUPDSEL | PE  |
| NONE        |                  |             |                  |          | R/W | R/W     | R/W |
| 0h          |                  |             |                  |          | 1h  | 1h      | 0h  |
| 7           | 6                | 5           | 4                | 3        | 2   | 1       | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL | IE_OVERRIDE | IE_OVERRIDE_CTRL | RESERVED |     |         |     |
| R/W         | R/W              | R/W         | R/W              | NONE     |     |         |     |
| 1h          | 1h               | 0h          | 1h               | 0h       |     |         |     |

**Table 2-2017. IOMUX\_TDI\_CFG\_REG Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                 |
|-------|------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | RESERVED         | R    | 0h    | Reserved                                                                                                                                                                                                                                    |
| 30:11 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                    |
| 10    | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                       |
| 9     | PUPDSEL          | R/W  | 1h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                  |
| 8     | PE               | R/W  | 0h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                      |
| 7     | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral. |
| 6     | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                         |

**Table 2-2017. IOMUX\_TDI\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | IE_OVERRIDE      | R/W  | 0h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                           |

### 2.4.2.143 IOMUX\_TDO\_CFG\_REG Register

#### 1 IOMUX\_TDO\_CFG\_REG Register (Offset = 238h) [reset = 630h]

TDO IO config register.

Return to [Summary Table](#)

**Table 2-2018. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0238h       |

**Figure 2-672. IOMUX\_TDO\_CFG\_REG Name Register**

|             |                  |             |                  |          |     |         |     |
|-------------|------------------|-------------|------------------|----------|-----|---------|-----|
| 31          | 30               | 29          | 28               | 27       | 26  | 25      | 24  |
| RESERVED    | RESERVED         |             |                  |          |     |         |     |
| R           | NONE             |             |                  |          |     |         |     |
| 0h          | 0h               |             |                  |          |     |         |     |
| 23          | 22               | 21          | 20               | 19       | 18  | 17      | 16  |
| RESERVED    |                  |             |                  |          |     |         |     |
| NONE        |                  |             |                  |          |     |         |     |
| 0h          |                  |             |                  |          |     |         |     |
| 15          | 14               | 13          | 12               | 11       | 10  | 9       | 8   |
| RESERVED    |                  |             |                  |          | SC1 | PUPDSEL | PE  |
| NONE        |                  |             |                  |          | R/W | R/W     | R/W |
| 0h          |                  |             |                  |          | 1h  | 1h      | 0h  |
| 7           | 6                | 5           | 4                | 3        | 2   | 1       | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL | IE_OVERRIDE | IE_OVERRIDE_CTRL | RESERVED |     |         |     |
| R/W         | R/W              | R/W         | R/W              | NONE     |     |         |     |
| 0h          | 0h               | 1h          | 1h               | 0h       |     |         |     |

**Table 2-2020. IOMUX\_TDO\_CFG\_REG Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                 |
|-------|------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | RESERVED         | R    | 0h    | Reserved                                                                                                                                                                                                                                    |
| 30:11 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                    |
| 10    | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                       |
| 9     | PUPDSEL          | R/W  | 1h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                  |
| 8     | PE               | R/W  | 0h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                      |
| 7     | OE_OVERRIDE      | R/W  | 0h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral. |
| 6     | OE_OVERRIDE_CTRL | R/W  | 0h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                         |

**Table 2-2020. IOMUX\_TDO\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                           |

### 2.4.2.144 IOMUX\_TMS\_CFG\_REG Register

#### 1 IOMUX\_TMS\_CFG\_REG Register (Offset = 23Ch) [reset = 610h]

TMS IO config register.

Return to [Summary Table](#)

**Table 2-2021. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 023Ch       |

**Figure 2-673. IOMUX\_TMS\_CFG\_REG Name Register**

|             |                  |             |                  |          |     |         |     |
|-------------|------------------|-------------|------------------|----------|-----|---------|-----|
| 31          | 30               | 29          | 28               | 27       | 26  | 25      | 24  |
| RESERVED    | RESERVED         |             |                  |          |     |         |     |
| R           | NONE             |             |                  |          |     |         |     |
| 0h          | 0h               |             |                  |          |     |         |     |
| 23          | 22               | 21          | 20               | 19       | 18  | 17      | 16  |
| RESERVED    |                  |             |                  |          |     |         |     |
| NONE        |                  |             |                  |          |     |         |     |
| 0h          |                  |             |                  |          |     |         |     |
| 15          | 14               | 13          | 12               | 11       | 10  | 9       | 8   |
| RESERVED    |                  |             |                  |          | SC1 | PUPDSEL | PE  |
| NONE        |                  |             |                  |          | R/W | R/W     | R/W |
| 0h          |                  |             |                  |          | 1h  | 1h      | 0h  |
| 7           | 6                | 5           | 4                | 3        | 2   | 1       | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL | IE_OVERRIDE | IE_OVERRIDE_CTRL | RESERVED |     |         |     |
| R/W         | R/W              | R/W         | R/W              | NONE     |     |         |     |
| 0h          | 0h               | 0h          | 1h               | 0h       |     |         |     |

**Table 2-2023. IOMUX\_TMS\_CFG\_REG Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                 |
|-------|------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | RESERVED         | R    | 0h    | Reserved                                                                                                                                                                                                                                    |
| 30:11 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                    |
| 10    | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                       |
| 9     | PUPDSEL          | R/W  | 1h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                  |
| 8     | PE               | R/W  | 0h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                      |
| 7     | OE_OVERRIDE      | R/W  | 0h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral. |
| 6     | OE_OVERRIDE_CTRL | R/W  | 0h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                         |

**Table 2-2023. IOMUX\_TMS\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | IE_OVERRIDE      | R/W  | 0h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                           |

## 2.4.2.145 IOMUX\_TCK\_CFG\_REG Register

### 1 IOMUX\_TCK\_CFG\_REG Register (Offset = 240h) [reset = 210h]

TCK IO config register.

Return to [Summary Table](#)

**Table 2-2024. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0240h       |

**Figure 2-674. IOMUX\_TCK\_CFG\_REG Name Register**

|             |                  |             |                  |          |     |         |     |
|-------------|------------------|-------------|------------------|----------|-----|---------|-----|
| 31          | 30               | 29          | 28               | 27       | 26  | 25      | 24  |
| RESERVED    | RESERVED         |             |                  |          |     |         |     |
| R           | NONE             |             |                  |          |     |         |     |
| 0h          | 0h               |             |                  |          |     |         |     |
| 23          | 22               | 21          | 20               | 19       | 18  | 17      | 16  |
| RESERVED    |                  |             |                  |          |     |         |     |
| NONE        |                  |             |                  |          |     |         |     |
| 0h          |                  |             |                  |          |     |         |     |
| 15          | 14               | 13          | 12               | 11       | 10  | 9       | 8   |
| RESERVED    |                  |             |                  |          | SC1 | PUPDSEL | PE  |
| NONE        |                  |             |                  |          | R/W | R/W     | R/W |
| 0h          |                  |             |                  |          | 0h  | 1h      | 0h  |
| 7           | 6                | 5           | 4                | 3        | 2   | 1       | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL | IE_OVERRIDE | IE_OVERRIDE_CTRL | RESERVED |     |         |     |
| R/W         | R/W              | R/W         | R/W              | NONE     |     |         |     |
| 0h          | 0h               | 0h          | 1h               | 0h       |     |         |     |

**Table 2-2026. IOMUX\_TCK\_CFG\_REG Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                 |
|-------|------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | RESERVED         | R    | 0h    | Reserved                                                                                                                                                                                                                                    |
| 30:11 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                    |
| 10    | SC1              | R/W  | 0h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                       |
| 9     | PUPDSEL          | R/W  | 1h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                  |
| 8     | PE               | R/W  | 0h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                      |
| 7     | OE_OVERRIDE      | R/W  | 0h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral. |
| 6     | OE_OVERRIDE_CTRL | R/W  | 0h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                         |



**Table 2-2026. IOMUX\_TCK\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | IE_OVERRIDE      | R/W  | 0h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                           |

## 2.4.2.146 IOMUX\_OSPI0\_CLKLB\_CFG\_REG Register

### 1 IOMUX\_OSPI0\_CLKLB\_CFG\_REG Register (Offset = 244h) [reset = 5F0h]

OSPI0\_CLKLB IO config register.

Return to [Summary Table](#)

**Table 2-2027. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0244h       |

**Figure 2-675. IOMUX\_OSPI0\_CLKLB\_CFG\_REG Name Register**

|             |                  |             |                  |          |     |         |     |
|-------------|------------------|-------------|------------------|----------|-----|---------|-----|
| 31          | 30               | 29          | 28               | 27       | 26  | 25      | 24  |
| RESERVED    | RESERVED         |             |                  |          |     |         |     |
| R           | NONE             |             |                  |          |     |         |     |
| 0h          | 0h               |             |                  |          |     |         |     |
| 23          | 22               | 21          | 20               | 19       | 18  | 17      | 16  |
| RESERVED    |                  |             |                  |          |     |         |     |
| NONE        |                  |             |                  |          |     |         |     |
| 0h          |                  |             |                  |          |     |         |     |
| 15          | 14               | 13          | 12               | 11       | 10  | 9       | 8   |
| RESERVED    |                  |             |                  |          | SC1 | PUPDSEL | PE  |
| NONE        |                  |             |                  |          | R/W | R/W     | R/W |
| 0h          |                  |             |                  |          | 1h  | 0h      | 1h  |
| 7           | 6                | 5           | 4                | 3        | 2   | 1       | 0   |
| OE_OVERRIDE | OE_OVERRIDE_CTRL | IE_OVERRIDE | IE_OVERRIDE_CTRL | RESERVED |     |         |     |
| R/W         | R/W              | R/W         | R/W              | NONE     |     |         |     |
| 1h          | 1h               | 1h          | 1h               | 0h       |     |         |     |

**Table 2-2029. IOMUX\_OSPI0\_CLKLB\_CFG\_REG Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                 |
|-------|------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | RESERVED         | R    | 0h    | Reserved                                                                                                                                                                                                                                    |
| 30:11 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                    |
| 10    | SC1              | R/W  | 1h    | IO Slew Rate Control :<br>0 : higher slew rate.<br>1:Lower slew rate.                                                                                                                                                                       |
| 9     | PUPDSEL          | R/W  | 0h    | Internal Pull Resistor Direction Control bit<br>0:Pull-down Resistor<br>1:Pull-up Resistor                                                                                                                                                  |
| 8     | PE               | R/W  | 1h    | PE = Pull Enable [Active Low]<br>0 = Pull Enabled<br>1 = Pull Disabled                                                                                                                                                                      |
| 7     | OE_OVERRIDE      | R/W  | 1h    | Output Enable Override.<br>Effective only when OE_OVERRIDE_CTRL is set (1).<br>0 - The HW peripheral drives the output buffer; pad is actively driven.<br>1 - The output buffer is tristated (HiZ); pad is not driven by the HW peripheral. |
| 6     | OE_OVERRIDE_CTRL | R/W  | 1h    | Output Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the output buffer(GZ).<br>1 - The value programmed in (PAD)_CFG_REG.OE_OVERRIDE is the gatekeeper for the output buffer.                                         |

**Table 2-2029. IOMUX\_OSPI0\_CLKLB\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | IE_OVERRIDE      | R/W  | 1h    | Input Enable Override.<br>Effective only when IE_OVERRIDE_CTRL is set as 1.<br>0 - Input buffer is enabled; the input path is active.<br>1 - Input buffer is tristated (HiZ); the input path is disabled.<br>When IE_OVERRIDE_CTRL is cleared (0), this field has no effect and the peripheral controls the input buffer directly. |
| 4   | IE_OVERRIDE_CTRL | R/W  | 1h    | Input Enable Override Control.<br>0 - HW peripheral is the gatekeeper for the input buffer.(IE)<br>1 - The value programmed in (PAD)_CFG_REG.IE_OVERRIDE is the gatekeeper for the input buffer.                                                                                                                                   |
| 3:0 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                           |

### 2.4.2.147 IOMUX\_QUAL\_GRP\_0\_CFG\_REG Register

#### 1 IOMUX\_QUAL\_GRP\_0\_CFG\_REG Register (Offset = 248h) [reset = 0h]

QUAL\_GRP\_0 config register.

Return to [Summary Table](#)

**Table 2-2030. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0248h       |

**Figure 2-676. IOMUX\_QUAL\_GRP\_0\_CFG\_REG Name Register**

|                        |          |    |    |    |    |    |    |
|------------------------|----------|----|----|----|----|----|----|
| 31                     | 30       | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED               | RESERVED |    |    |    |    |    |    |
| R                      | NONE     |    |    |    |    |    |    |
| 0h                     | 0h       |    |    |    |    |    |    |
| 23                     | 22       | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 15                     | 14       | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 7                      | 6        | 5  | 4  | 3  | 2  | 1  | 0  |
| QUAL_PERIOD_PER_SAMPLE |          |    |    |    |    |    |    |
| R/W                    |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |

**Table 2-2032. IOMUX\_QUAL\_GRP\_0\_CFG\_REG Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                   |
|------|------------------------|------|-------|---------------------------------------------------------------|
| 31   | RESERVED               | R    | 0h    | Reserved                                                      |
| 30:8 | RESERVED               | NONE | 0h    | Reserved                                                      |
| 7:0  | QUAL_PERIOD_PER_SAMPLE | R/W  | 0h    | MMR bits for programming the qualifier clock count per sample |

### 2.4.2.148 IOMUX\_QUAL\_GRP\_1\_CFG\_REG Register

#### 1 IOMUX\_QUAL\_GRP\_1\_CFG\_REG Register (Offset = 24Ch) [reset = 0h]

QUAL\_GRP\_1 config register.

Return to [Summary Table](#)

**Table 2-2033. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 024Ch       |

**Figure 2-677. IOMUX\_QUAL\_GRP\_1\_CFG\_REG Name Register**

|                        |          |    |    |    |    |    |    |
|------------------------|----------|----|----|----|----|----|----|
| 31                     | 30       | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED               | RESERVED |    |    |    |    |    |    |
| R                      | NONE     |    |    |    |    |    |    |
| 0h                     | 0h       |    |    |    |    |    |    |
| 23                     | 22       | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 15                     | 14       | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 7                      | 6        | 5  | 4  | 3  | 2  | 1  | 0  |
| QUAL_PERIOD_PER_SAMPLE |          |    |    |    |    |    |    |
| R/W                    |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |

**Table 2-2035. IOMUX\_QUAL\_GRP\_1\_CFG\_REG Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                   |
|------|------------------------|------|-------|---------------------------------------------------------------|
| 31   | RESERVED               | R    | 0h    | Reserved                                                      |
| 30:8 | RESERVED               | NONE | 0h    | Reserved                                                      |
| 7:0  | QUAL_PERIOD_PER_SAMPLE | R/W  | 0h    | MMR bits for programming the qualifier clock count per sample |

### 2.4.2.149 IOMUX\_QUAL\_GRP\_2\_CFG\_REG Register

#### 1 IOMUX\_QUAL\_GRP\_2\_CFG\_REG Register (Offset = 250h) [reset = 0h]

QUAL\_GRP\_2 config register.

Return to [Summary Table](#)

**Table 2-2036. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0250h       |

**Figure 2-678. IOMUX\_QUAL\_GRP\_2\_CFG\_REG Name Register**

|                        |          |    |    |    |    |    |    |
|------------------------|----------|----|----|----|----|----|----|
| 31                     | 30       | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED               | RESERVED |    |    |    |    |    |    |
| R                      | NONE     |    |    |    |    |    |    |
| 0h                     | 0h       |    |    |    |    |    |    |
| 23                     | 22       | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 15                     | 14       | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 7                      | 6        | 5  | 4  | 3  | 2  | 1  | 0  |
| QUAL_PERIOD_PER_SAMPLE |          |    |    |    |    |    |    |
| R/W                    |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |

**Table 2-2038. IOMUX\_QUAL\_GRP\_2\_CFG\_REG Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                   |
|------|------------------------|------|-------|---------------------------------------------------------------|
| 31   | RESERVED               | R    | 0h    | Reserved                                                      |
| 30:8 | RESERVED               | NONE | 0h    | Reserved                                                      |
| 7:0  | QUAL_PERIOD_PER_SAMPLE | R/W  | 0h    | MMR bits for programming the qualifier clock count per sample |

### 2.4.2.150 IOMUX\_QUAL\_GRP\_3\_CFG\_REG Register

#### 1 IOMUX\_QUAL\_GRP\_3\_CFG\_REG Register (Offset = 254h) [reset = 0h]

QUAL\_GRP\_3 config register.

Return to [Summary Table](#)

**Table 2-2039. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0254h       |

**Figure 2-679. IOMUX\_QUAL\_GRP\_3\_CFG\_REG Name Register**

|                        |          |    |    |    |    |    |    |
|------------------------|----------|----|----|----|----|----|----|
| 31                     | 30       | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED               | RESERVED |    |    |    |    |    |    |
| R                      | NONE     |    |    |    |    |    |    |
| 0h                     | 0h       |    |    |    |    |    |    |
| 23                     | 22       | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 15                     | 14       | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 7                      | 6        | 5  | 4  | 3  | 2  | 1  | 0  |
| QUAL_PERIOD_PER_SAMPLE |          |    |    |    |    |    |    |
| R/W                    |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |

**Table 2-2041. IOMUX\_QUAL\_GRP\_3\_CFG\_REG Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                   |
|------|------------------------|------|-------|---------------------------------------------------------------|
| 31   | RESERVED               | R    | 0h    | Reserved                                                      |
| 30:8 | RESERVED               | NONE | 0h    | Reserved                                                      |
| 7:0  | QUAL_PERIOD_PER_SAMPLE | R/W  | 0h    | MMR bits for programming the qualifier clock count per sample |

### 2.4.2.151 IOMUX\_QUAL\_GRP\_4\_CFG\_REG Register

#### 1 IOMUX\_QUAL\_GRP\_4\_CFG\_REG Register (Offset = 258h) [reset = 0h]

QUAL\_GRP\_4 config register.

Return to [Summary Table](#)

**Table 2-2042. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0258h       |

**Figure 2-680. IOMUX\_QUAL\_GRP\_4\_CFG\_REG Name Register**

|                        |          |    |    |    |    |    |    |
|------------------------|----------|----|----|----|----|----|----|
| 31                     | 30       | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED               | RESERVED |    |    |    |    |    |    |
| R                      | NONE     |    |    |    |    |    |    |
| 0h                     | 0h       |    |    |    |    |    |    |
| 23                     | 22       | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 15                     | 14       | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 7                      | 6        | 5  | 4  | 3  | 2  | 1  | 0  |
| QUAL_PERIOD_PER_SAMPLE |          |    |    |    |    |    |    |
| R/W                    |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |

**Table 2-2044. IOMUX\_QUAL\_GRP\_4\_CFG\_REG Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                   |
|------|------------------------|------|-------|---------------------------------------------------------------|
| 31   | RESERVED               | R    | 0h    | Reserved                                                      |
| 30:8 | RESERVED               | NONE | 0h    | Reserved                                                      |
| 7:0  | QUAL_PERIOD_PER_SAMPLE | R/W  | 0h    | MMR bits for programming the qualifier clock count per sample |



### 2.4.2.152 IOMUX\_QUAL\_GRP\_5\_CFG\_REG Register

#### 1 IOMUX\_QUAL\_GRP\_5\_CFG\_REG Register (Offset = 25Ch) [reset = 0h]

QUAL\_GRP\_5 config register.

Return to [Summary Table](#)

**Table 2-2045. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 025Ch       |

**Figure 2-681. IOMUX\_QUAL\_GRP\_5\_CFG\_REG Name Register**

|                        |          |    |    |    |    |    |    |
|------------------------|----------|----|----|----|----|----|----|
| 31                     | 30       | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED               | RESERVED |    |    |    |    |    |    |
| R                      | NONE     |    |    |    |    |    |    |
| 0h                     | 0h       |    |    |    |    |    |    |
| 23                     | 22       | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 15                     | 14       | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 7                      | 6        | 5  | 4  | 3  | 2  | 1  | 0  |
| QUAL_PERIOD_PER_SAMPLE |          |    |    |    |    |    |    |
| R/W                    |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |

**Table 2-2047. IOMUX\_QUAL\_GRP\_5\_CFG\_REG Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                   |
|------|------------------------|------|-------|---------------------------------------------------------------|
| 31   | RESERVED               | R    | 0h    | Reserved                                                      |
| 30:8 | RESERVED               | NONE | 0h    | Reserved                                                      |
| 7:0  | QUAL_PERIOD_PER_SAMPLE | R/W  | 0h    | MMR bits for programming the qualifier clock count per sample |

### 2.4.2.153 IOMUX\_QUAL\_GRP\_6\_CFG\_REG Register

#### 1 IOMUX\_QUAL\_GRP\_6\_CFG\_REG Register (Offset = 260h) [reset = 0h]

QUAL\_GRP\_6 config register.

Return to [Summary Table](#)

**Table 2-2048. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0260h       |

**Figure 2-682. IOMUX\_QUAL\_GRP\_6\_CFG\_REG Name Register**

|                        |          |    |    |    |    |    |    |
|------------------------|----------|----|----|----|----|----|----|
| 31                     | 30       | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED               | RESERVED |    |    |    |    |    |    |
| R                      | NONE     |    |    |    |    |    |    |
| 0h                     | 0h       |    |    |    |    |    |    |
| 23                     | 22       | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 15                     | 14       | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 7                      | 6        | 5  | 4  | 3  | 2  | 1  | 0  |
| QUAL_PERIOD_PER_SAMPLE |          |    |    |    |    |    |    |
| R/W                    |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |

**Table 2-2050. IOMUX\_QUAL\_GRP\_6\_CFG\_REG Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                   |
|------|------------------------|------|-------|---------------------------------------------------------------|
| 31   | RESERVED               | R    | 0h    | Reserved                                                      |
| 30:8 | RESERVED               | NONE | 0h    | Reserved                                                      |
| 7:0  | QUAL_PERIOD_PER_SAMPLE | R/W  | 0h    | MMR bits for programming the qualifier clock count per sample |

### 2.4.2.154 IOMUX\_QUAL\_GRP\_7\_CFG\_REG Register

#### 1 IOMUX\_QUAL\_GRP\_7\_CFG\_REG Register (Offset = 264h) [reset = 0h]

QUAL\_GRP\_7 config register.

Return to [Summary Table](#)

**Table 2-2051. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0264h       |

**Figure 2-683. IOMUX\_QUAL\_GRP\_7\_CFG\_REG Name Register**

|                        |          |    |    |    |    |    |    |
|------------------------|----------|----|----|----|----|----|----|
| 31                     | 30       | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED               | RESERVED |    |    |    |    |    |    |
| R                      | NONE     |    |    |    |    |    |    |
| 0h                     | 0h       |    |    |    |    |    |    |
| 23                     | 22       | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 15                     | 14       | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 7                      | 6        | 5  | 4  | 3  | 2  | 1  | 0  |
| QUAL_PERIOD_PER_SAMPLE |          |    |    |    |    |    |    |
| R/W                    |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |

**Table 2-2053. IOMUX\_QUAL\_GRP\_7\_CFG\_REG Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                   |
|------|------------------------|------|-------|---------------------------------------------------------------|
| 31   | RESERVED               | R    | 0h    | Reserved                                                      |
| 30:8 | RESERVED               | NONE | 0h    | Reserved                                                      |
| 7:0  | QUAL_PERIOD_PER_SAMPLE | R/W  | 0h    | MMR bits for programming the qualifier clock count per sample |

### 2.4.2.155 IOMUX\_QUAL\_GRP\_8\_CFG\_REG Register

#### 1 IOMUX\_QUAL\_GRP\_8\_CFG\_REG Register (Offset = 268h) [reset = 0h]

QUAL\_GRP\_8 config register.

Return to [Summary Table](#)

**Table 2-2054. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0268h       |

**Figure 2-684. IOMUX\_QUAL\_GRP\_8\_CFG\_REG Name Register**

|                        |          |    |    |    |    |    |    |
|------------------------|----------|----|----|----|----|----|----|
| 31                     | 30       | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED               | RESERVED |    |    |    |    |    |    |
| R                      | NONE     |    |    |    |    |    |    |
| 0h                     | 0h       |    |    |    |    |    |    |
| 23                     | 22       | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 15                     | 14       | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 7                      | 6        | 5  | 4  | 3  | 2  | 1  | 0  |
| QUAL_PERIOD_PER_SAMPLE |          |    |    |    |    |    |    |
| R/W                    |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |

**Table 2-2056. IOMUX\_QUAL\_GRP\_8\_CFG\_REG Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                   |
|------|------------------------|------|-------|---------------------------------------------------------------|
| 31   | RESERVED               | R    | 0h    | Reserved                                                      |
| 30:8 | RESERVED               | NONE | 0h    | Reserved                                                      |
| 7:0  | QUAL_PERIOD_PER_SAMPLE | R/W  | 0h    | MMR bits for programming the qualifier clock count per sample |

### 2.4.2.156 IOMUX\_QUAL\_GRP\_9\_CFG\_REG Register

#### 1 IOMUX\_QUAL\_GRP\_9\_CFG\_REG Register (Offset = 26Ch) [reset = 0h]

QUAL\_GRP\_9 config register.

Return to [Summary Table](#)

**Table 2-2057. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 026Ch       |

**Figure 2-685. IOMUX\_QUAL\_GRP\_9\_CFG\_REG Name Register**

|                        |          |    |    |    |    |    |    |
|------------------------|----------|----|----|----|----|----|----|
| 31                     | 30       | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED               | RESERVED |    |    |    |    |    |    |
| R                      | NONE     |    |    |    |    |    |    |
| 0h                     | 0h       |    |    |    |    |    |    |
| 23                     | 22       | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 15                     | 14       | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 7                      | 6        | 5  | 4  | 3  | 2  | 1  | 0  |
| QUAL_PERIOD_PER_SAMPLE |          |    |    |    |    |    |    |
| R/W                    |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |

**Table 2-2059. IOMUX\_QUAL\_GRP\_9\_CFG\_REG Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                   |
|------|------------------------|------|-------|---------------------------------------------------------------|
| 31   | RESERVED               | R    | 0h    | Reserved                                                      |
| 30:8 | RESERVED               | NONE | 0h    | Reserved                                                      |
| 7:0  | QUAL_PERIOD_PER_SAMPLE | R/W  | 0h    | MMR bits for programming the qualifier clock count per sample |

### 2.4.2.157 IOMUX\_QUAL\_GRP\_10\_CFG\_REG Register

#### 1 IOMUX\_QUAL\_GRP\_10\_CFG\_REG Register (Offset = 270h) [reset = 0h]

QUAL\_GRP\_10 config register.

Return to [Summary Table](#)

**Table 2-2060. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0270h       |

**Figure 2-686. IOMUX\_QUAL\_GRP\_10\_CFG\_REG Name Register**

|                        |          |    |    |    |    |    |    |
|------------------------|----------|----|----|----|----|----|----|
| 31                     | 30       | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED               | RESERVED |    |    |    |    |    |    |
| R                      | NONE     |    |    |    |    |    |    |
| 0h                     | 0h       |    |    |    |    |    |    |
| 23                     | 22       | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 15                     | 14       | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 7                      | 6        | 5  | 4  | 3  | 2  | 1  | 0  |
| QUAL_PERIOD_PER_SAMPLE |          |    |    |    |    |    |    |
| R/W                    |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |

**Table 2-2062. IOMUX\_QUAL\_GRP\_10\_CFG\_REG Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                   |
|------|------------------------|------|-------|---------------------------------------------------------------|
| 31   | RESERVED               | R    | 0h    | Reserved                                                      |
| 30:8 | RESERVED               | NONE | 0h    | Reserved                                                      |
| 7:0  | QUAL_PERIOD_PER_SAMPLE | R/W  | 0h    | MMR bits for programming the qualifier clock count per sample |

### 2.4.2.158 IOMUX\_QUAL\_GRP\_11\_CFG\_REG Register

#### 1 IOMUX\_QUAL\_GRP\_11\_CFG\_REG Register (Offset = 274h) [reset = 0h]

QUAL\_GRP\_11 config register.

Return to [Summary Table](#)

**Table 2-2063. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0274h       |

**Figure 2-687. IOMUX\_QUAL\_GRP\_11\_CFG\_REG Name Register**

|                        |          |    |    |    |    |    |    |
|------------------------|----------|----|----|----|----|----|----|
| 31                     | 30       | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED               | RESERVED |    |    |    |    |    |    |
| R                      | NONE     |    |    |    |    |    |    |
| 0h                     | 0h       |    |    |    |    |    |    |
| 23                     | 22       | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 15                     | 14       | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 7                      | 6        | 5  | 4  | 3  | 2  | 1  | 0  |
| QUAL_PERIOD_PER_SAMPLE |          |    |    |    |    |    |    |
| R/W                    |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |

**Table 2-2065. IOMUX\_QUAL\_GRP\_11\_CFG\_REG Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                   |
|------|------------------------|------|-------|---------------------------------------------------------------|
| 31   | RESERVED               | R    | 0h    | Reserved                                                      |
| 30:8 | RESERVED               | NONE | 0h    | Reserved                                                      |
| 7:0  | QUAL_PERIOD_PER_SAMPLE | R/W  | 0h    | MMR bits for programming the qualifier clock count per sample |

### 2.4.2.159 IOMUX\_QUAL\_GRP\_12\_CFG\_REG Register

#### 1 IOMUX\_QUAL\_GRP\_12\_CFG\_REG Register (Offset = 278h) [reset = 0h]

QUAL\_GRP\_12 config register.

Return to [Summary Table](#)

**Table 2-2066. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0278h       |

**Figure 2-688. IOMUX\_QUAL\_GRP\_12\_CFG\_REG Name Register**

|                        |          |    |    |    |    |    |    |
|------------------------|----------|----|----|----|----|----|----|
| 31                     | 30       | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED               | RESERVED |    |    |    |    |    |    |
| R                      | NONE     |    |    |    |    |    |    |
| 0h                     | 0h       |    |    |    |    |    |    |
| 23                     | 22       | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 15                     | 14       | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 7                      | 6        | 5  | 4  | 3  | 2  | 1  | 0  |
| QUAL_PERIOD_PER_SAMPLE |          |    |    |    |    |    |    |
| R/W                    |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |

**Table 2-2068. IOMUX\_QUAL\_GRP\_12\_CFG\_REG Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                   |
|------|------------------------|------|-------|---------------------------------------------------------------|
| 31   | RESERVED               | R    | 0h    | Reserved                                                      |
| 30:8 | RESERVED               | NONE | 0h    | Reserved                                                      |
| 7:0  | QUAL_PERIOD_PER_SAMPLE | R/W  | 0h    | MMR bits for programming the qualifier clock count per sample |



### 2.4.2.160 IOMUX\_QUAL\_GRP\_13\_CFG\_REG Register

#### 1 IOMUX\_QUAL\_GRP\_13\_CFG\_REG Register (Offset = 27Ch) [reset = 0h]

QUAL\_GRP\_13 config register.

Return to [Summary Table](#)

**Table 2-2069. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 027Ch       |

**Figure 2-689. IOMUX\_QUAL\_GRP\_13\_CFG\_REG Name Register**

|                        |          |    |    |    |    |    |    |
|------------------------|----------|----|----|----|----|----|----|
| 31                     | 30       | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED               | RESERVED |    |    |    |    |    |    |
| R                      | NONE     |    |    |    |    |    |    |
| 0h                     | 0h       |    |    |    |    |    |    |
| 23                     | 22       | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 15                     | 14       | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 7                      | 6        | 5  | 4  | 3  | 2  | 1  | 0  |
| QUAL_PERIOD_PER_SAMPLE |          |    |    |    |    |    |    |
| R/W                    |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |

**Table 2-2071. IOMUX\_QUAL\_GRP\_13\_CFG\_REG Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                   |
|------|------------------------|------|-------|---------------------------------------------------------------|
| 31   | RESERVED               | R    | 0h    | Reserved                                                      |
| 30:8 | RESERVED               | NONE | 0h    | Reserved                                                      |
| 7:0  | QUAL_PERIOD_PER_SAMPLE | R/W  | 0h    | MMR bits for programming the qualifier clock count per sample |

### 2.4.2.161 IOMUX\_QUAL\_GRP\_14\_CFG\_REG Register

#### 1 IOMUX\_QUAL\_GRP\_14\_CFG\_REG Register (Offset = 280h) [reset = 0h]

QUAL\_GRP\_14 config register.

Return to [Summary Table](#)

**Table 2-2072. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0280h       |

**Figure 2-690. IOMUX\_QUAL\_GRP\_14\_CFG\_REG Name Register**

|                        |          |    |    |    |    |    |    |
|------------------------|----------|----|----|----|----|----|----|
| 31                     | 30       | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED               | RESERVED |    |    |    |    |    |    |
| R                      | NONE     |    |    |    |    |    |    |
| 0h                     | 0h       |    |    |    |    |    |    |
| 23                     | 22       | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 15                     | 14       | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 7                      | 6        | 5  | 4  | 3  | 2  | 1  | 0  |
| QUAL_PERIOD_PER_SAMPLE |          |    |    |    |    |    |    |
| R/W                    |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |

**Table 2-2074. IOMUX\_QUAL\_GRP\_14\_CFG\_REG Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                   |
|------|------------------------|------|-------|---------------------------------------------------------------|
| 31   | RESERVED               | R    | 0h    | Reserved                                                      |
| 30:8 | RESERVED               | NONE | 0h    | Reserved                                                      |
| 7:0  | QUAL_PERIOD_PER_SAMPLE | R/W  | 0h    | MMR bits for programming the qualifier clock count per sample |

### 2.4.2.162 IOMUX\_QUAL\_GRP\_15\_CFG\_REG Register

#### 1 IOMUX\_QUAL\_GRP\_15\_CFG\_REG Register (Offset = 284h) [reset = 0h]

QUAL\_GRP\_15 config register.

Return to [Summary Table](#)

**Table 2-2075. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0284h       |

**Figure 2-691. IOMUX\_QUAL\_GRP\_15\_CFG\_REG Name Register**

|                        |          |    |    |    |    |    |    |
|------------------------|----------|----|----|----|----|----|----|
| 31                     | 30       | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED               | RESERVED |    |    |    |    |    |    |
| R                      | NONE     |    |    |    |    |    |    |
| 0h                     | 0h       |    |    |    |    |    |    |
| 23                     | 22       | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 15                     | 14       | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 7                      | 6        | 5  | 4  | 3  | 2  | 1  | 0  |
| QUAL_PERIOD_PER_SAMPLE |          |    |    |    |    |    |    |
| R/W                    |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |

**Table 2-2077. IOMUX\_QUAL\_GRP\_15\_CFG\_REG Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                   |
|------|------------------------|------|-------|---------------------------------------------------------------|
| 31   | RESERVED               | R    | 0h    | Reserved                                                      |
| 30:8 | RESERVED               | NONE | 0h    | Reserved                                                      |
| 7:0  | QUAL_PERIOD_PER_SAMPLE | R/W  | 0h    | MMR bits for programming the qualifier clock count per sample |

### 2.4.2.163 IOMUX\_QUAL\_GRP\_16\_CFG\_REG Register

#### 1 IOMUX\_QUAL\_GRP\_16\_CFG\_REG Register (Offset = 288h) [reset = 0h]

QUAL\_GRP\_16 config register.

Return to [Summary Table](#)

**Table 2-2078. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0288h       |

**Figure 2-692. IOMUX\_QUAL\_GRP\_16\_CFG\_REG Name Register**

|                        |          |    |    |    |    |    |    |
|------------------------|----------|----|----|----|----|----|----|
| 31                     | 30       | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED               | RESERVED |    |    |    |    |    |    |
| R                      | NONE     |    |    |    |    |    |    |
| 0h                     | 0h       |    |    |    |    |    |    |
| 23                     | 22       | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 15                     | 14       | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 7                      | 6        | 5  | 4  | 3  | 2  | 1  | 0  |
| QUAL_PERIOD_PER_SAMPLE |          |    |    |    |    |    |    |
| R/W                    |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |

**Table 2-2080. IOMUX\_QUAL\_GRP\_16\_CFG\_REG Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                   |
|------|------------------------|------|-------|---------------------------------------------------------------|
| 31   | RESERVED               | R    | 0h    | Reserved                                                      |
| 30:8 | RESERVED               | NONE | 0h    | Reserved                                                      |
| 7:0  | QUAL_PERIOD_PER_SAMPLE | R/W  | 0h    | MMR bits for programming the qualifier clock count per sample |

### 2.4.2.164 IOMUX\_QUAL\_GRP\_17\_CFG\_REG Register

#### 1 IOMUX\_QUAL\_GRP\_17\_CFG\_REG Register (Offset = 28Ch) [reset = 0h]

QUAL\_GRP\_17 config register.

Return to [Summary Table](#)

**Table 2-2081. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 028Ch       |

**Figure 2-693. IOMUX\_QUAL\_GRP\_17\_CFG\_REG Name Register**

|                        |          |    |    |    |    |    |    |
|------------------------|----------|----|----|----|----|----|----|
| 31                     | 30       | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED               | RESERVED |    |    |    |    |    |    |
| R                      | NONE     |    |    |    |    |    |    |
| 0h                     | 0h       |    |    |    |    |    |    |
| 23                     | 22       | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 15                     | 14       | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED               |          |    |    |    |    |    |    |
| NONE                   |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |
| 7                      | 6        | 5  | 4  | 3  | 2  | 1  | 0  |
| QUAL_PERIOD_PER_SAMPLE |          |    |    |    |    |    |    |
| R/W                    |          |    |    |    |    |    |    |
| 0h                     |          |    |    |    |    |    |    |

**Table 2-2083. IOMUX\_QUAL\_GRP\_17\_CFG\_REG Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                   |
|------|------------------------|------|-------|---------------------------------------------------------------|
| 31   | RESERVED               | R    | 0h    | Reserved                                                      |
| 30:8 | RESERVED               | NONE | 0h    | Reserved                                                      |
| 7:0  | QUAL_PERIOD_PER_SAMPLE | R/W  | 0h    | MMR bits for programming the qualifier clock count per sample |

## 2.4.2.165 IOMUX\_USER\_MODE\_EN Register

### 1 IOMUX\_USER\_MODE\_EN Register (Offset = 290h) [reset = 0h]

USER\_MODE\_EN config register.

Return to [Summary Table](#)

**Table 2-2084. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0290h       |

**Figure 2-694. IOMUX\_USER\_MODE\_EN Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| USER_MODE_EN |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| USER_MODE_EN |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| USER_MODE_EN |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| USER_MODE_EN |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 2-2086. IOMUX\_USER\_MODE\_EN Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                       |
|------|--------------|------|-------|-------------------------------------------------------------------|
| 31:0 | USER_MODE_EN | R/W  | 0h    | Write 0XADADADAD to enable user mode write access to IO CFG space |

### 2.4.2.166 IOMUX\_PADGLBL\_CFG\_REG Register

#### 1 IOMUX\_PADGLBL\_CFG\_REG Register (Offset = 294h) [reset = 0h]

Global config register for IO.

Return to [Summary Table](#)

**Table 2-2087. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0294h       |

**Figure 2-695. IOMUX\_PADGLBL\_CFG\_REG Name Register**

|          |    |    |               |                 |                 |    |    |
|----------|----|----|---------------|-----------------|-----------------|----|----|
| 31       | 30 | 29 | 28            | 27              | 26              | 25 | 24 |
| RESERVED |    |    |               |                 |                 |    |    |
| NONE     |    |    |               |                 |                 |    |    |
| 0h       |    |    |               |                 |                 |    |    |
| 23       | 22 | 21 | 20            | 19              | 18              | 17 | 16 |
| RESERVED |    |    | GLOBAL_PU_VAL | GLOBAL_PI_VAL   | GLOBAL_PI_CTL   |    |    |
| NONE     |    |    | R/W           | R/W             | R/W             |    |    |
| 0h       |    |    | 0h            | 0h              | 0h              |    |    |
| 15       | 14 | 13 | 12            | 11              | 10              | 9  | 8  |
| RESERVED |    |    |               | GLOBAL_OE_N_VAL | GLOBAL_OE_N_CTL |    |    |
| NONE     |    |    |               | R/W             | R/W             |    |    |
| 0h       |    |    |               | 0h              | 0h              |    |    |
| 7        | 6  | 5  | 4             | 3               | 2               | 1  | 0  |
| RESERVED |    |    |               | GLOBAL_IE_N_VAL | GLOBAL_IE_N_CTL |    |    |
| NONE     |    |    |               | R/W             | R/W             |    |    |
| 0h       |    |    |               | 0h              | 0h              |    |    |

**Table 2-2089. IOMUX\_PADGLBL\_CFG\_REG Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                          |
|-------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:21 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                             |
| 20    | GLOBAL_PU_VAL   | R/W  | 0h    | Specifies the pull resistor direction applied to all IOs when global_pi_ctl is 3'b111. Only meaningful when global_pi_val is 0 (pull enabled).<br>0 - Pull-down resistor selected.<br>1 - Pull-up resistor selected.                 |
| 19    | GLOBAL_PI_VAL   | R/W  | 0h    | Specifies the pull resistor enable state applied to all IOs when global_pi_ctl is 3'b111.<br>0 - Pull resistor enabled.<br>1 - Pull resistor disabled.                                                                               |
| 18:16 | GLOBAL_PI_CTL   | R/W  | 0h    | Controls the pull resistor override for all IOs. Write 3'b111 to apply global_pi_val and global_pu_val globally to every IO. Any other value defers control to each IO's individual PADCFG.PI register.                              |
| 15:12 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                             |
| 11    | GLOBAL_OE_N_VAL | R/W  | 0h    | Controls the output enable (OE, active-low) override for all IOs. Write 3'b111 to apply global_oe_n_val globally to the GZ pin of every IO. Any other value defers control to each IO's individual PADCFG.OE_OVERRIDE_CTRL register. |

**Table 2-2089. IOMUX\_PADGLBL\_CFG\_REG Register Field Descriptions (continued)**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                  |
|------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10:8 | GLOBAL_OE_N_CTL | R/W  | 0h    | Controls the output enable (OE, active-low) override for all IOs. Write 3'b111 to apply global_oe_n_val globally to the GZ pin of every IO. Any other value defers control to each IO's individual PADCFG.OE_OVERRIDE_CTRL register.                                                                                                                                                         |
| 7:4  | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                     |
| 3    | GLOBAL_IE_N_VAL | R/W  | 0h    | Specifies the input enable state applied to all IOs when GLOBAL_IE_N_CTL is 3'b111. Has no effect when global_ie_n_ctl is not 3'b111; in that case, the HW peripheral or per-pad PADCFG register controls the input buffer directly.<br>0 - Input buffer enabled; the HW peripheral actively drives the pad.<br>1 - Input buffer tristated (Hi-Z); the HW peripheral does not drive the pad. |
| 2:0  | GLOBAL_IE_N_CTL | R/W  | 0h    | Controls the input enable (IE) override for all IOs. Write 3'b111 to apply global_ie_n_val globally to the IE pin of every IO. Any other value defers control to each IO's individual PADCFG.IE_OVERRIDE_CTRL register.                                                                                                                                                                      |



## 2.4.2.167 IOMUX\_IO\_CFG\_KICK0 Register

### 1 IOMUX\_IO\_CFG\_KICK0 Register (Offset = 298h) [reset = 0h]

KICK0 config register.

Return to [Summary Table](#)

**Table 2-2090. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 0298h       |

**Figure 2-696. IOMUX\_IO\_CFG\_KICK0 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| IO_CFG_KICK0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| IO_CFG_KICK0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| IO_CFG_KICK0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| IO_CFG_KICK0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 2-2092. IOMUX\_IO\_CFG\_KICK0 Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                                                                                                  |
|------|--------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | IO_CFG_KICK0 | R/W  | 0h    | Kicker 0 Register. The value 83E7 0B13h must be written to KICK0 as part of the process to unlock the CPU.write access to the above PIN MUX registers [including IOCFGKICK1] |

### 2.4.2.168 IOMUX\_IO\_CFG\_KICK1 Register

#### 1 IOMUX\_IO\_CFG\_KICK1 Register (Offset = 29Ch) [reset = C1h]

KICK1 config register.

Return to [Summary Table](#)

**Table 2-2093. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| IO_MUX        | 5310 029Ch       |

**Figure 2-697. IOMUX\_IO\_CFG\_KICK1 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| IO_CFG_KICK1 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| C1h          |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| IO_CFG_KICK1 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| C1h          |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| IO_CFG_KICK1 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| C1h          |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| IO_CFG_KICK1 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| C1h          |    |    |    |    |    |    |    |

**Table 2-2095. IOMUX\_IO\_CFG\_KICK1 Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                                                                                                                                                                              |
|------|--------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | IO_CFG_KICK1 | R/W  | C1h   | Kicker 1 Register. The value 95A4 F1E0h must be written to the KICK1 as part of the process to unlock the CPU write access to above PINMUX registers [excluding IOCFGKICK0]. IOCFGKICK0 has to be written with 83E70B13h to enable access to IOCFGKICK1. |

## 2.5 MSS\_TOPRCM

### MSS\_TOPRCM

#### 2.5.1 MSS\_TOPRCM Summaries

#### MSS\_TOPRCM Summaries

**Table 2-2096. MSS\_TOPRCM Registers, Base Address=5320 0000h, Length=4096**

| Offset | Length | Register Name                                         | MSS_TOPRCM Physical Address |
|--------|--------|-------------------------------------------------------|-----------------------------|
| 4h     | 32     | <a href="#">MSS_TOPRCM_WARM_RESET_CONFIG</a>          | 5320 0004h                  |
| 8h     | 32     | <a href="#">MSS_TOPRCM_WARM_RESET_REQ</a>             | 5320 0008h                  |
| Ch     | 32     | <a href="#">MSS_TOPRCM_SYS_RST_CAUSE</a>              | 5320 000Ch                  |
| 10h    | 32     | <a href="#">MSS_TOPRCM_SYS_RST_CAUSE_CLR</a>          | 5320 0010h                  |
| 14h    | 32     | <a href="#">MSS_TOPRCM_RCOSC32K_CTRL</a>              | 5320 0014h                  |
| 18h    | 32     | <a href="#">MSS_TOPRCM_LIMP_MODE_EN</a>               | 5320 0018h                  |
| 1Ch    | 32     | <a href="#">MSS_TOPRCM_PLL_REF_CLK_SRC_SEL</a>        | 5320 001Ch                  |
| 24h    | 32     | <a href="#">MSS_TOPRCM_SOP_MODE_VALUE</a>             | 5320 0024h                  |
| 28h    | 32     | <a href="#">MSS_TOPRCM_CLK_LOSS_STATUS</a>            | 5320 0028h                  |
| 30h    | 32     | <a href="#">MSS_TOPRCM_WARM_RSTTIME1</a>              | 5320 0030h                  |
| 34h    | 32     | <a href="#">MSS_TOPRCM_WARM_RSTTIME2</a>              | 5320 0034h                  |
| 38h    | 32     | <a href="#">MSS_TOPRCM_WARM_RSTTIME3</a>              | 5320 0038h                  |
| 400h   | 32     | <a href="#">MSS_TOPRCM_PLL_CORE_PWRCTRL</a>           | 5320 0400h                  |
| 404h   | 32     | <a href="#">MSS_TOPRCM_PLL_CORE_CLKCTRL</a>           | 5320 0404h                  |
| 408h   | 32     | <a href="#">MSS_TOPRCM_PLL_CORE_TENABLE</a>           | 5320 0408h                  |
| 40Ch   | 32     | <a href="#">MSS_TOPRCM_PLL_CORE_TENABLEDIV</a>        | 5320 040Ch                  |
| 410h   | 32     | <a href="#">MSS_TOPRCM_PLL_CORE_M2NDIV</a>            | 5320 0410h                  |
| 414h   | 32     | <a href="#">MSS_TOPRCM_PLL_CORE_MN2DIV</a>            | 5320 0414h                  |
| 418h   | 32     | <a href="#">MSS_TOPRCM_PLL_CORE_FRACDIV</a>           | 5320 0418h                  |
| 41Ch   | 32     | <a href="#">MSS_TOPRCM_PLL_CORE_BWCTRL</a>            | 5320 041Ch                  |
| 420h   | 32     | <a href="#">MSS_TOPRCM_PLL_CORE_FRACCTRL</a>          | 5320 0420h                  |
| 424h   | 32     | <a href="#">MSS_TOPRCM_PLL_CORE_STATUS</a>            | 5320 0424h                  |
| 428h   | 32     | <a href="#">MSS_TOPRCM_PLL_CORE_HSDIVIDER</a>         | 5320 0428h                  |
| 42Ch   | 32     | <a href="#">MSS_TOPRCM_PLL_CORE_HSDIVIDER_CLKOUT0</a> | 5320 042Ch                  |
| 430h   | 32     | <a href="#">MSS_TOPRCM_PLL_CORE_HSDIVIDER_CLKOUT1</a> | 5320 0430h                  |
| 434h   | 32     | <a href="#">MSS_TOPRCM_PLL_CORE_HSDIVIDER_CLKOUT2</a> | 5320 0434h                  |
| 43Ch   | 32     | <a href="#">MSS_TOPRCM_PLL_CORE_RSTCTRL</a>           | 5320 043Ch                  |
| 440h   | 32     | <a href="#">MSS_TOPRCM_PLL_CORE_HSDIVIDER_RSTCTRL</a> | 5320 0440h                  |
| 500h   | 32     | <a href="#">MSS_TOPRCM_MSS_R5SS_CLK_SRC_SEL</a>       | 5320 0500h                  |
| 504h   | 32     | <a href="#">MSS_TOPRCM_MSS_ROOT_R5SS_CLK_STATUS</a>   | 5320 0504h                  |
| 510h   | 32     | <a href="#">MSS_TOPRCM_MSS_CR50_CLK_DIV_SEL</a>       | 5320 0510h                  |
| 514h   | 32     | <a href="#">MSS_TOPRCM_MSS_CR51_CLK_DIV_SEL</a>       | 5320 0514h                  |
| 518h   | 32     | <a href="#">MSS_TOPRCM_MSS_CR50_CLK_GATE</a>          | 5320 0518h                  |
| 51Ch   | 32     | <a href="#">MSS_TOPRCM_MSS_CR51_CLK_GATE</a>          | 5320 051Ch                  |
| 520h   | 32     | <a href="#">MSS_TOPRCM_SYS_CLK_DIV_VAL</a>            | 5320 0520h                  |
| 524h   | 32     | <a href="#">MSS_TOPRCM_SYS_CLK_GATE</a>               | 5320 0524h                  |
| 528h   | 32     | <a href="#">MSS_TOPRCM_SYS_CLK_STATUS</a>             | 5320 0528h                  |
| 800h   | 32     | <a href="#">MSS_TOPRCM_PLL_PER_PWRCTRL</a>            | 5320 0800h                  |

**Table 2-2096. MSS\_TOPRCM Registers, Base Address=5320 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                                        | MSS_TOPRCM Physical Address |
|--------|--------|------------------------------------------------------|-----------------------------|
| 804h   | 32     | <a href="#">MSS_TOPRCM_PLL_PER_CLKCTRL</a>           | 5320 0804h                  |
| 808h   | 32     | <a href="#">MSS_TOPRCM_PLL_PER_TENABLE</a>           | 5320 0808h                  |
| 80Ch   | 32     | <a href="#">MSS_TOPRCM_PLL_PER_TENABLEDIV</a>        | 5320 080Ch                  |
| 810h   | 32     | <a href="#">MSS_TOPRCM_PLL_PER_M2NDIV</a>            | 5320 0810h                  |
| 814h   | 32     | <a href="#">MSS_TOPRCM_PLL_PER_MN2DIV</a>            | 5320 0814h                  |
| 818h   | 32     | <a href="#">MSS_TOPRCM_PLL_PER_FRACDIV</a>           | 5320 0818h                  |
| 81Ch   | 32     | <a href="#">MSS_TOPRCM_PLL_PER_BWCTRL</a>            | 5320 081Ch                  |
| 820h   | 32     | <a href="#">MSS_TOPRCM_PLL_PER_FRACCTRL</a>          | 5320 0820h                  |
| 824h   | 32     | <a href="#">MSS_TOPRCM_PLL_PER_STATUS</a>            | 5320 0824h                  |
| 828h   | 32     | <a href="#">MSS_TOPRCM_PLL_PER_HSDIVIDER</a>         | 5320 0828h                  |
| 82Ch   | 32     | <a href="#">MSS_TOPRCM_PLL_PER_HSDIVIDER_CLKOUT0</a> | 5320 082Ch                  |
| 830h   | 32     | <a href="#">MSS_TOPRCM_PLL_PER_HSDIVIDER_CLKOUT1</a> | 5320 0830h                  |
| 83Ch   | 32     | <a href="#">MSS_TOPRCM_PLL_PER_RSTCTRL</a>           | 5320 083Ch                  |
| 840h   | 32     | <a href="#">MSS_TOPRCM_PLL_PER_HSDIVIDER_RSTCTRL</a> | 5320 0840h                  |
| C00h   | 32     | <a href="#">MSS_TOPRCM_CLKOUT0_CLK_SRC_SEL</a>       | 5320 0C00h                  |
| C04h   | 32     | <a href="#">MSS_TOPRCM_CLKOUT1_CLK_SRC_SEL</a>       | 5320 0C04h                  |
| C08h   | 32     | <a href="#">MSS_TOPRCM_CLKOUT0_DIV_VAL</a>           | 5320 0C08h                  |
| C0Ch   | 32     | <a href="#">MSS_TOPRCM_CLKOUT1_DIV_VAL</a>           | 5320 0C0Ch                  |
| C10h   | 32     | <a href="#">MSS_TOPRCM_CLKOUT0_CLK_GATE</a>          | 5320 0C10h                  |
| C14h   | 32     | <a href="#">MSS_TOPRCM_CLKOUT1_CLK_GATE</a>          | 5320 0C14h                  |
| C18h   | 32     | <a href="#">MSS_TOPRCM_CLKOUT0_CLK_STATUS</a>        | 5320 0C18h                  |
| C1Ch   | 32     | <a href="#">MSS_TOPRCM_CLKOUT1_CLK_STATUS</a>        | 5320 0C1Ch                  |
| C20h   | 32     | <a href="#">MSS_TOPRCM_TRCCLKOUT_CLK_SRC_SEL</a>     | 5320 0C20h                  |
| C24h   | 32     | <a href="#">MSS_TOPRCM_TRCCLKOUT_DIV_VAL</a>         | 5320 0C24h                  |
| C28h   | 32     | <a href="#">MSS_TOPRCM_TRCCLKOUT_CLK_GATE</a>        | 5320 0C28h                  |
| C2Ch   | 32     | <a href="#">MSS_TOPRCM_TRCCLKOUT_CLK_STATUS</a>      | 5320 0C2Ch                  |
| E00h   | 32     | <a href="#">MSS_TOPRCM_HW_REG0</a>                   | 5320 0E00h                  |
| E04h   | 32     | <a href="#">MSS_TOPRCM_HW_REG1</a>                   | 5320 0E04h                  |
| E08h   | 32     | <a href="#">MSS_TOPRCM_HW_REG2</a>                   | 5320 0E08h                  |
| E0Ch   | 32     | <a href="#">MSS_TOPRCM_HW_REG3</a>                   | 5320 0E0Ch                  |
| FD0h   | 32     | <a href="#">MSS_TOPRCM_HW_SPARE_RW0</a>              | 5320 0FD0h                  |
| FD4h   | 32     | <a href="#">MSS_TOPRCM_HW_SPARE_RW1</a>              | 5320 0FD4h                  |
| FD8h   | 32     | <a href="#">MSS_TOPRCM_HW_SPARE_RW2</a>              | 5320 0FD8h                  |
| FDCh   | 32     | <a href="#">MSS_TOPRCM_HW_SPARE_RW3</a>              | 5320 0FDCh                  |
| FE0h   | 32     | <a href="#">MSS_TOPRCM_HW_SPARE_RO0</a>              | 5320 0FE0h                  |
| FE4h   | 32     | <a href="#">MSS_TOPRCM_HW_SPARE_RO1</a>              | 5320 0FE4h                  |
| FE8h   | 32     | <a href="#">MSS_TOPRCM_HW_SPARE_RO2</a>              | 5320 0FE8h                  |
| FECh   | 32     | <a href="#">MSS_TOPRCM_HW_SPARE_RO3</a>              | 5320 0FECh                  |
| FF0h   | 32     | <a href="#">MSS_TOPRCM_HW_SPARE_WPH</a>              | 5320 0FF0h                  |
| FF4h   | 32     | <a href="#">MSS_TOPRCM_HW_SPARE_REC</a>              | 5320 0FF4h                  |
| 1008h  | 32     | <a href="#">MSS_TOPRCM_LOCK0_KICK0</a>               | 5320 1008h                  |
| 100Ch  | 32     | <a href="#">MSS_TOPRCM_LOCK0_KICK1</a>               | 5320 100Ch                  |
| 1010h  | 32     | <a href="#">MSS_TOPRCM_INTR_RAW_STATUS</a>           | 5320 1010h                  |
| 1014h  | 32     | <a href="#">MSS_TOPRCM_INTR_ENABLED_STATUS_CLEAR</a> | 5320 1014h                  |
| 1018h  | 32     | <a href="#">MSS_TOPRCM_INTR_ENABLE</a>               | 5320 1018h                  |

**Table 2-2096. MSS\_TOPRCM Registers, Base Address=5320 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                                | MSS_TOPRCM Physical Address |
|--------|--------|----------------------------------------------|-----------------------------|
| 101Ch  | 32     | <a href="#">MSS_TOPRCM_INTR_ENABLE_CLEAR</a> | 5320 101Ch                  |
| 1020h  | 32     | <a href="#">MSS_TOPRCM_EOI</a>               | 5320 1020h                  |
| 1024h  | 32     | <a href="#">MSS_TOPRCM_FAULT_ADDRESS</a>     | 5320 1024h                  |
| 1028h  | 32     | <a href="#">MSS_TOPRCM_FAULT_TYPE_STATUS</a> | 5320 1028h                  |
| 102Ch  | 32     | <a href="#">MSS_TOPRCM_FAULT_ATTR_STATUS</a> | 5320 102Ch                  |
| 1030h  | 32     | <a href="#">MSS_TOPRCM_FAULT_CLEAR</a>       | 5320 1030h                  |

### 2.5.2 MSS\_TOPRCM Registers

#### MSS\_TOPRCM Registers

### 2.5.2.1 MSS\_TOPRCM\_WARM\_RESET\_CONFIG Register

#### 1 MSS\_TOPRCM\_WARM\_RESET\_CONFIG Register (Offset = 4h) [reset = 7777777h]

Warm Reset Config options.

Return to [Summary Table](#)

**Table 2-2097. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0004h       |

**Figure 2-698. MSS\_TOPRCM\_WARM\_RESET\_CONFIG Name Register**

| 31       | 30                               | 29 | 28 | 27       | 26                               | 25 | 24 |
|----------|----------------------------------|----|----|----------|----------------------------------|----|----|
| RESERVED | WARM_RESET_CONFIG_WDOG3_RST_EN   |    |    | RESERVED | WARM_RESET_CONFIG_WDOG2_RST_EN   |    |    |
| NONE     | R/W                              |    |    | NONE     | R/W                              |    |    |
| 0h       | 7h                               |    |    | 0h       | 7h                               |    |    |
| 23       | 22                               | 21 | 20 | 19       | 18                               | 17 | 16 |
| RESERVED | WARM_RESET_CONFIG_WDOG1_RST_EN   |    |    | RESERVED | WARM_RESET_CONFIG_WDOG0_RST_EN   |    |    |
| NONE     | R/W                              |    |    | NONE     | R/W                              |    |    |
| 0h       | 7h                               |    |    | 0h       | 7h                               |    |    |
| 15       | 14                               | 13 | 12 | 11       | 10                               | 9  | 8  |
| RESERVED | WARM_RESET_CONFIG_TSENSE1_RST_EN |    |    | RESERVED | WARM_RESET_CONFIG_TSENSE0_RST_EN |    |    |
| NONE     | R/W                              |    |    | NONE     | R/W                              |    |    |
| 0h       | 7h                               |    |    | 0h       | 7h                               |    |    |
| 7        | 6                                | 5  | 4  | 3        | 2                                | 1  | 0  |
| RESERVED | WARM_RESET_CONFIG_DEBUGSS_RST_EN |    |    | RESERVED | WARM_RESET_CONFIG_PAD_BYPASS     |    |    |
| NONE     | R/W                              |    |    | NONE     | R/W                              |    |    |
| 0h       | 7h                               |    |    | 0h       | 7h                               |    |    |

**Table 2-2099. MSS\_TOPRCM\_WARM\_RESET\_CONFIG Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                                                                                                                                                                    |
|-------|--------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                                       |
| 30:28 | WARM_RESET_CONFIG_WDOG3_RST_EN | R/W  | 7h    | Enable/Disable WATCHDOG3 triggering Warm Reset<br>Data should be loaded as multibit.<br>Write 3'b000 to disable corresponding Watchdog control on warmreset<br>Write 3'b111 enable corresponding Watchdog control on warmreset |
| 27    | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                                       |
| 26:24 | WARM_RESET_CONFIG_WDOG2_RST_EN | R/W  | 7h    | Enable/Disable WATCHDOG2 triggering Warm Reset<br>Data should be loaded as multibit.<br>Write 3'b000 to disable corresponding Watchdog control on warmreset<br>Write 3'b111 enable corresponding Watchdog control on warmreset |
| 23    | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                                       |
| 22:20 | WARM_RESET_CONFIG_WDOG1_RST_EN | R/W  | 7h    | Enable/Disable WATCHDOG1 triggering Warm Reset<br>Data should be loaded as multibit.<br>Write 3'b000 to disable corresponding Watchdog control on warmreset<br>Write 3'b111 enable corresponding Watchdog control on warmreset |
| 19    | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                                       |

**Table 2-2099. MSS\_TOPRCM\_WARM\_RESET\_CONFIG Register Field Descriptions (continued)**

| Bit   | Field                            | Type | Reset | Description                                                                                                                                                                                                                                                    |
|-------|----------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 18:16 | WARM_RESET_CONFIG_WDOG0_RST_EN   | R/W  | 7h    | Enable/Disable WATCHDOG0 triggering Warm Reset<br>Data should be loaded as multibit.<br>Write 3'b000 to disable corresponding Watchdog control on warmreset<br>Write 3'b111 enable corresponding Watchdog control on warmreset                                 |
| 15    | RESERVED                         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                       |
| 14:12 | WARM_RESET_CONFIG_TSENSE1_RST_EN | R/W  | 7h    | Data should be loaded as multibit.<br>Write 3'b000 to disable temperature sensor 1 on Warm reset<br>Write 3'b111 to enable temperature sensor 1l on Warm reset                                                                                                 |
| 11    | RESERVED                         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                       |
| 10:8  | WARM_RESET_CONFIG_TSENSE0_RST_EN | R/W  | 7h    | Data should be loaded as multibit.<br>Write 3'b000 to disable temperature sensor 0 control on Warm reset<br>Write 3'b111 to enable temperature sensor 0 control on Warm reset                                                                                  |
| 7     | RESERVED                         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                       |
| 6:4   | WARM_RESET_CONFIG_DEBUGSS_RST_EN | R/W  | 7h    | Enable/Disable DEBUGSS triggering Warm Reset<br>Data should be loaded as multibit.<br>Write 3'b000 to disable debugger control on Warm Reset<br>Write 3'b111 enable debugger control on Warm Reset                                                             |
| 3     | RESERVED                         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                       |
| 2:0   | WARM_RESET_CONFIG_PAD_BYPASS     | R/W  | 7h    | Bypass the Warm reset from Pad Input<br>Data should be loaded as multibit.<br>Write 3'b000 : Pad Warm Reset pin has control over warm reset<br>Write 3'b111 : Pad warm reset pin has no control on warm reset<br>***Note: This bit will only be reset by PORz. |

### 2.5.2.2 MSS\_TOPRCM\_WARM\_RESET\_REQ Register

#### 1 MSS\_TOPRCM\_WARM\_RESET\_REQ Register (Offset = 8h) [reset = 7h]

Warm Reset Config options.

Return to [Summary Table](#)

**Table 2-2100. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0008h       |

**Figure 2-699. MSS\_TOPRCM\_WARM\_RESET\_REQ Name Register**

|          |    |    |    |                       |    |    |    |
|----------|----|----|----|-----------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                    | 26 | 25 | 24 |
| RESERVED |    |    |    |                       |    |    |    |
| NONE     |    |    |    |                       |    |    |    |
| 0h       |    |    |    |                       |    |    |    |
| 23       | 22 | 21 | 20 | 19                    | 18 | 17 | 16 |
| RESERVED |    |    |    |                       |    |    |    |
| NONE     |    |    |    |                       |    |    |    |
| 0h       |    |    |    |                       |    |    |    |
| 15       | 14 | 13 | 12 | 11                    | 10 | 9  | 8  |
| RESERVED |    |    |    |                       |    |    |    |
| NONE     |    |    |    |                       |    |    |    |
| 0h       |    |    |    |                       |    |    |    |
| 7        | 6  | 5  | 4  | 3                     | 2  | 1  | 0  |
| RESERVED |    |    |    | WARM_RESET_REQ_SW_RST |    |    |    |
| NONE     |    |    |    | R/W                   |    |    |    |
| 0h       |    |    |    | 7h                    |    |    |    |

**Table 2-2102. MSS\_TOPRCM\_WARM\_RESET\_REQ Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                                                                                                                             |
|------|-----------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED              | NONE | 0h    | Reserved                                                                                                                                                                |
| 2:0  | WARM_RESET_REQ_SW_RST | R/W  | 7h    | Data should be loaded as multibit.<br>Write 3'b000 to assert warm reset from SW<br>Write 3'b111 to deassert warm reset from SW if this is the only source of warm reset |



### 2.5.2.3 MSS\_TOPRCM\_SYS\_RST\_CAUSE Register

#### 1 MSS\_TOPRCM\_SYS\_RST\_CAUSE Register (Offset = Ch) [reset = 41h]

System Reset Cause Register.

Return to [Summary Table](#)

**Table 2-2103. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 000Ch       |

**Figure 2-700. MSS\_TOPRCM\_SYS\_RST\_CAUSE Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| RESERVED            |    |    |    | SYS_RST_CAUSE_CAUSE |    |    |    |
| NONE                |    |    |    | R                   |    |    |    |
| 0h                  |    |    |    | 41h                 |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| SYS_RST_CAUSE_CAUSE |    |    |    |                     |    |    |    |
| R                   |    |    |    |                     |    |    |    |
| 41h                 |    |    |    |                     |    |    |    |

**Table 2-2105. MSS\_TOPRCM\_SYS\_RST\_CAUSE Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|---------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 11:0  | SYS_RST_CAUSE_CAUSE | R    | 41h   | System Reset Cause register<br>12'b0000_0100_0001 - POR reset<br>12'b0000_0100_0010 - Warm reset due to MSS_WDT0<br>12'b0000_0100_0100 - Warm reset due to MSS_WDT1<br>12'b0000_0100_1000 - Warm reset due to MSS_WDT2<br>12'b0000_0101_0000 - Warm reset due to MSS_WDT3<br>12'b0000_0110_0000 - Warm reset due to TOP_RMC:WARM_RESET_REQ<br>12'b0000_0100_0000 - External Pad reset<br>12'b0000_1100_0000 - Warm reset due to HSM_WDT<br>12'b0001_0100_0000 - Warm Reset due to Deugger reset<br>12'b0010_0100_0000 - Warm Reset due to Temp Sense0 Reset<br>12'b0100_0100_0000 - Warm Reset due to Temp Sense1 Reset |

### 2.5.2.4 MSS\_TOPRCM\_SYS\_RST\_CAUSE\_CLR Register

#### 1 MSS\_TOPRCM\_SYS\_RST\_CAUSE\_CLR Register (Offset = 10h) [reset = 0h]

System Reset Cause Register Clear.

Return to [Summary Table](#)

**Table 2-2106. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0010h       |

**Figure 2-701. MSS\_TOPRCM\_SYS\_RST\_CAUSE\_CLR Name Register**

|          |    |    |    |    |                         |    |    |
|----------|----|----|----|----|-------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                      | 25 | 24 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                      | 17 | 16 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                      | 9  | 8  |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                       | 1  | 0  |
| RESERVED |    |    |    |    | SYS_RST_CAUSE_CLR_CLEAR |    |    |
| NONE     |    |    |    |    | R/W                     |    |    |
| 0h       |    |    |    |    | 0h                      |    |    |

**Table 2-2108. MSS\_TOPRCM\_SYS\_RST\_CAUSE\_CLR Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                                                                                                                    |
|------|-------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                       |
| 2:0  | SYS_RST_CAUSE_CLR_CLEAR | R/W  | 0h    | Write pulse bit field: Data should be loaded as multibit. System Reset Cause register Clear. Write 3'b111 to clear System Reset Cause register |

### 2.5.2.5 MSS\_TOPRCM\_RCOSC32K\_CTRL Register

#### 1 MSS\_TOPRCM\_RCOSC32K\_CTRL Register (Offset = 14h) [reset = 0h]

RC OSC 32KHz clock control.

Return to [Summary Table](#)

**Table 2-2109. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0014h       |

**Figure 2-702. MSS\_TOPRCM\_RCOSC32K\_CTRL Name Register**

|          |    |    |    |    |                       |    |    |
|----------|----|----|----|----|-----------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                    | 25 | 24 |
| RESERVED |    |    |    |    |                       |    |    |
| NONE     |    |    |    |    |                       |    |    |
| 0h       |    |    |    |    |                       |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                    | 17 | 16 |
| RESERVED |    |    |    |    |                       |    |    |
| NONE     |    |    |    |    |                       |    |    |
| 0h       |    |    |    |    |                       |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                    | 9  | 8  |
| RESERVED |    |    |    |    |                       |    |    |
| NONE     |    |    |    |    |                       |    |    |
| 0h       |    |    |    |    |                       |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                     | 1  | 0  |
| RESERVED |    |    |    |    | RCOSC32K_CTRL_STOPOSC |    |    |
| NONE     |    |    |    |    | R/W                   |    |    |
| 0h       |    |    |    |    | 0h                    |    |    |

**Table 2-2111. MSS\_TOPRCM\_RCOSC32K\_CTRL Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                     |
|------|------------------------|------|-------|-------------------------------------------------|
| 31:3 | RESERVED               | NONE | 0h    | Reserved                                        |
| 2:0  | RCOSC32K_CTRL_STOP OSC | R/W  | 0h    | Stop 32KHz RCOSC.<br>Write 3'b111 to stop clock |

### 2.5.2.6 MSS\_TOPRCM\_LIMP\_MODE\_EN Register

#### 1 MSS\_TOPRCM\_LIMP\_MODE\_EN Register (Offset = 18h) [reset = 0h]

Control to enabled limp mode.

Return to [Summary Table](#)

**Table 2-2112. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0018h       |

**Figure 2-703. MSS\_TOPRCM\_LIMP\_MODE\_EN Name Register**

|          |                              |    |    |          |                              |    |    |
|----------|------------------------------|----|----|----------|------------------------------|----|----|
| 31       | 30                           | 29 | 28 | 27       | 26                           | 25 | 24 |
| RESERVED |                              |    |    |          |                              |    |    |
| NONE     |                              |    |    |          |                              |    |    |
| 0h       |                              |    |    |          |                              |    |    |
| 23       | 22                           | 21 | 20 | 19       | 18                           | 17 | 16 |
| RESERVED |                              |    |    |          |                              |    |    |
| NONE     |                              |    |    |          |                              |    |    |
| 0h       |                              |    |    |          |                              |    |    |
| 15       | 14                           | 13 | 12 | 11       | 10                           | 9  | 8  |
| RESERVED |                              |    |    |          | LIMP_MODE_EN_COREPLL_LOSS_EN |    |    |
| NONE     |                              |    |    |          | R/W                          |    |    |
| 0h       |                              |    |    |          | 0h                           |    |    |
| 7        | 6                            | 5  | 4  | 3        | 2                            | 1  | 0  |
| RESERVED | LIMP_MODE_EN_XTALCLK_LOSS_EN |    |    | RESERVED | LIMP_MODE_EN_DCC0_ERROR_EN   |    |    |
| NONE     | R/W                          |    |    | NONE     | R/W                          |    |    |
| 0h       | 0h                           |    |    | 0h       | 0h                           |    |    |

**Table 2-2114. MSS\_TOPRCM\_LIMP\_MODE\_EN Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                                                                                                                            |
|-------|------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:11 | RESERVED                     | NONE | 0h    | Reserved                                                                                                                                                               |
| 10:8  | LIMP_MODE_EN_COREPLL_LOSS_EN | R/W  | 0h    | Enable for core pll phase lock loss to generate Limp mode<br>3'b000: will not generate Limp mode [multibit 000]<br>3'b111 : will generate Limp mode [multibit 111]     |
| 7     | RESERVED                     | NONE | 0h    | Reserved                                                                                                                                                               |
| 6:4   | LIMP_MODE_EN_XTALCLK_LOSS_EN | R/W  | 0h    | Enable for crystal_clock_loss to generate Limp mode<br>3'b000: will not generate Limp mode [multibit 000]<br>3'b111 : will generate Limp mode [multibit 111]           |
| 3     | RESERVED                     | NONE | 0h    | Reserved                                                                                                                                                               |
| 2:0   | LIMP_MODE_EN_DCC0_ERROR_EN   | R/W  | 0h    | Enable DCC0 Error to generate Limp mode<br>3'b000: DCC0 Error will not generate Limp mode [multibit 000]<br>3'b111 : DCC0 Error will generate Limp mode [multibit 111] |

### 2.5.2.7 MSS\_TOPRCM\_PLL\_REF\_CLK\_SRC\_SEL Register

#### 1 MSS\_TOPRCM\_PLL\_REF\_CLK\_SRC\_SEL Register (Offset = 1Ch) [reset = 0h]

CORE PLL and PERI PLL reference clock select.

Return to [Summary Table](#)

**Table 2-2115. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 001Ch       |

**Figure 2-704. MSS\_TOPRCM\_PLL\_REF\_CLK\_SRC\_SEL Name Register**

|          |                                              |    |    |          |                                              |    |    |
|----------|----------------------------------------------|----|----|----------|----------------------------------------------|----|----|
| 31       | 30                                           | 29 | 28 | 27       | 26                                           | 25 | 24 |
| RESERVED |                                              |    |    |          |                                              |    |    |
| NONE     |                                              |    |    |          |                                              |    |    |
| 0h       |                                              |    |    |          |                                              |    |    |
| 23       | 22                                           | 21 | 20 | 19       | 18                                           | 17 | 16 |
| RESERVED |                                              |    |    |          |                                              |    |    |
| NONE     |                                              |    |    |          |                                              |    |    |
| 0h       |                                              |    |    |          |                                              |    |    |
| 15       | 14                                           | 13 | 12 | 11       | 10                                           | 9  | 8  |
| RESERVED |                                              |    |    |          |                                              |    |    |
| NONE     |                                              |    |    |          |                                              |    |    |
| 0h       |                                              |    |    |          |                                              |    |    |
| 7        | 6                                            | 5  | 4  | 3        | 2                                            | 1  | 0  |
| RESERVED | PLL_REF_CLK_SRC_SEL_PLL_PERI_REF_CLK_SRC_SEL |    |    | RESERVED | PLL_REF_CLK_SRC_SEL_PLL_CORE_REF_CLK_SRC_SEL |    |    |
| NONE     | R/W                                          |    |    | NONE     | R/W                                          |    |    |
| 0h       | 0h                                           |    |    | 0h       | 0h                                           |    |    |

**Table 2-2117. MSS\_TOPRCM\_PLL\_REF\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit  | Field                                                | Type | Reset | Description                                                                                                                                                                |
|------|------------------------------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED                                             | NONE | 0h    | Reserved                                                                                                                                                                   |
| 6:4  | PLL_REF_CLK_SRC_SE<br>L_PLL_PERI_REF_CLK_<br>SRC_SEL | R/W  | 0h    | Mux selct for PERI PLL REF clock<br>Write 3'b111 : to select external reference clock as PLL reference clock<br>Write 3'b000 : to select XTAL clock as PLL reference clock |
| 3    | RESERVED                                             | NONE | 0h    | Reserved                                                                                                                                                                   |
| 2:0  | PLL_REF_CLK_SRC_SE<br>L_PLL_CORE_REF_CLK_<br>SRC_SEL | R/W  | 0h    | Mux selct for CORE PLL REF clock<br>Write 3'b111 : to select external reference clock as PLL reference clock<br>Write 3'b000 : to select XTAL clock as PLL reference clock |

### 2.5.2.8 MSS\_TOPRCM\_SOP\_MODE\_VALUE Register

#### 1 MSS\_TOPRCM\_SOP\_MODE\_VALUE Register (Offset = 24h) [reset = 0h]

Sense on Power mode value.

Return to [Summary Table](#)

**Table 2-2118. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0024h       |

**Figure 2-705. MSS\_TOPRCM\_SOP\_MODE\_VALUE Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SOP_MODE_VALUE_VAL |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SOP_MODE_VALUE_VAL |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SOP_MODE_VALUE_VAL |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SOP_MODE_VALUE_VAL |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 2-2120. MSS\_TOPRCM\_SOP\_MODE\_VALUE Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | SOP_MODE_VALUE_VAL | R    | 0h    | <p>Bootmode (SOP_MODE) values and their corresponding mapping</p> <p>SOP3 SOP2 SOP1 SOP0 Bootmode</p> <p>0 0 0 0 QSPI Functional Mode[4S]</p> <p>0 0 0 1 UART Functional Mode</p> <p>0 0 1 0 QSPI Functional Mode[1S]</p> <p>0 1 0 0 QSPI Functional Mode[4S]</p> <p>0 1 0 0 QSPI [4S] - Quad Read UART Fallback Mode</p> <p>0 1 0 1 QSPI [1S] - Quad Read UART Fallback Mode</p> <p>Any undefined values are reserved for future use.</p> <p>Note: Reset value of MMR is 0, but true SOP pin values will latch immediately after PORz reset is released. CPU reads to the MMR will only reflect the SOP mode values latched at reset.</p> |

### 2.5.2.9 MSS\_TOPRCM\_CLK\_LOSS\_STATUS Register

#### 1 MSS\_TOPRCM\_CLK\_LOSS\_STATUS Register (Offset = 28h) [reset = 100h]

Coarse detection clock loss status for RC and Crystal.

Return to [Summary Table](#)

**Table 2-2121. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0028h       |

**Figure 2-706. MSS\_TOPRCM\_CLK\_LOSS\_STATUS Name Register**

|          |    |    |                                                    |          |    |    |                                                             |
|----------|----|----|----------------------------------------------------|----------|----|----|-------------------------------------------------------------|
| 31       | 30 | 29 | 28                                                 | 27       | 26 | 25 | 24                                                          |
| RESERVED |    |    |                                                    |          |    |    |                                                             |
| NONE     |    |    |                                                    |          |    |    |                                                             |
| 0h       |    |    |                                                    |          |    |    |                                                             |
| 23       | 22 | 21 | 20                                                 | 19       | 18 | 17 | 16                                                          |
| RESERVED |    |    |                                                    |          |    |    |                                                             |
| NONE     |    |    |                                                    |          |    |    |                                                             |
| 0h       |    |    |                                                    |          |    |    |                                                             |
| 15       | 14 | 13 | 12                                                 | 11       | 10 | 9  | 8                                                           |
| RESERVED |    |    |                                                    |          |    |    | CLK_LOSS_ST<br>ATU <sub>S</sub> _RC_GO<br>OD_BOOT           |
| NONE     |    |    |                                                    |          |    |    | R                                                           |
| 0h       |    |    |                                                    |          |    |    | 1h                                                          |
| 7        | 6  | 5  | 4                                                  | 3        | 2  | 1  | 0                                                           |
| RESERVED |    |    | CLK_LOSS_ST<br>ATU <sub>S</sub> _RC_CLO<br>CK_LOSS | RESERVED |    |    | CLK_LOSS_ST<br>ATU <sub>S</sub> _CRYSTA<br>L_CLOCK_LOS<br>S |
| NONE     |    |    | R                                                  | NONE     |    |    | R                                                           |
| 0h       |    |    | 0h                                                 | 0h       |    |    | 0h                                                          |

**Table 2-2123. MSS\_TOPRCM\_CLK\_LOSS\_STATUS Register Field Descriptions**

| Bit  | Field                              | Type | Reset | Description                                                                                                                                    |
|------|------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:9 | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                       |
| 8    | CLK_LOSS_STATUS_RC_GOOD_BOOT       | R    | 1h    | Clock status of RC clock at boot. Reset value will reflect the actual status<br>1 --> clock present at boot<br>0 --> clock not present at boot |
| 7:5  | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                       |
| 4    | CLK_LOSS_STATUS_RC_CLOCK_LOSS      | R    | 0h    | Coarse detection clock loss status for RC clock. Reset value will reflect the actual status<br>1 --> clock lost<br>0 --> clock good            |
| 3:1  | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                       |
| 0    | CLK_LOSS_STATUS_CRYSTAL_CLOCK_LOSS | R    | 0h    | Coarse detection clock loss status for Crystal clock. Reset value will reflect the actual status<br>1 --> clock lost<br>0 --> clock good       |

### 2.5.2.10 MSS\_TOPRCM\_WARM\_RSTTIME1 Register

#### 1 MSS\_TOPRCM\_WARM\_RSTTIME1 Register (Offset = 30h) [reset = 888h]

programming Output delay: time between internal warm reset source assert to warm reset pad deassert.

Return to [Summary Table](#)

**Table 2-2124. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0030h       |

**Figure 2-707. MSS\_TOPRCM\_WARM\_RSTTIME1 Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| RESERVED            |    |    |    | WARM_RSTTIME1_DELAY |    |    |    |
| NONE                |    |    |    | R/W                 |    |    |    |
| 0h                  |    |    |    | 888h                |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| WARM_RSTTIME1_DELAY |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 888h                |    |    |    |                     |    |    |    |

**Table 2-2126. MSS\_TOPRCM\_WARM\_RSTTIME1 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                          |
|-------|---------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                             |
| 11:0  | WARM_RSTTIME1_DELAY | R/W  | 888h  | Program sufficient delay using this bitfield to keep the WARMRSTn pad active for any external devices relying on the reset signal. Refer to Reset Details Section in TRM for more details.<br>Data should be loaded as multibit.<br>For example: if value of 0x5 should be selected then 0x555 should be configured to the register.<br>**Note: This bit will only be reset by PORz. |



### 2.5.2.11 MSS\_TOPRCM\_WARM\_RSTTIME2 Register

#### 1 MSS\_TOPRCM\_WARM\_RSTTIME2 Register (Offset = 34h) [reset = 888h]

programming input Rise delay : time between warm reset pad deassert to chip warm reset deassert.

Return to [Summary Table](#)

**Table 2-2127. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0034h       |

**Figure 2-708. MSS\_TOPRCM\_WARM\_RSTTIME2 Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| RESERVED            |    |    |    | WARM_RSTTIME2_DELAY |    |    |    |
| NONE                |    |    |    | R/W                 |    |    |    |
| 0h                  |    |    |    | 888h                |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| WARM_RSTTIME2_DELAY |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 888h                |    |    |    |                     |    |    |    |

**Table 2-2129. MSS\_TOPRCM\_WARM\_RSTTIME2 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                   |
|-------|---------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                      |
| 11:0  | WARM_RSTTIME2_DELAY | R/W  | 888h  | Program the deassertion delay with this bitfield to control internal system reset deassertion which is relative to the deassertion of WARMRSTn pad.<br>Data should be loaded as multibit.<br>For example: if value of 0x5 should be selected then 0x555 should be configured to the register.<br>**Note: This bit will only be reset by PORz. |

### 2.5.2.12 MSS\_TOPRCM\_WARM\_RSTTIME3 Register

#### 1 MSS\_TOPRCM\_WARM\_RSTTIME3 Register (Offset = 38h) [reset = 111h]

programming Input Fall delay : time between warm reset pad assert to chip warm reset assert.

Return to [Summary Table](#)

**Table 2-2130. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0038h       |

**Figure 2-709. MSS\_TOPRCM\_WARM\_RSTTIME3 Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| RESERVED            |    |    |    | WARM_RSTTIME3_DELAY |    |    |    |
| NONE                |    |    |    | R/W                 |    |    |    |
| 0h                  |    |    |    | 111h                |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| WARM_RSTTIME3_DELAY |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 111h                |    |    |    |                     |    |    |    |

**Table 2-2132. MSS\_TOPRCM\_WARM\_RSTTIME3 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|---------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 11:0  | WARM_RSTTIME3_DELAY | R/W  | 111h  | The glitch filter logic will filter any input pad signal which is LOW for any time less than the delay programmed with this bit. This parameter also programmes the delay from external Warmresetn assertion to Internal system warm resetn assertion.<br>Data should be loaded as multibit.<br>For example: if value of 0x5 should be selected then 0x555 should be configured to the register.<br>**Note: This bit will only be reset by PORz. |

### 2.5.2.13 MSS\_TOPRCM\_PLL\_CORE\_PWRCTRL Register

#### 1 MSS\_TOPRCM\_PLL\_CORE\_PWRCTRL Register (Offset = 400h) [reset = 30h]

Power control for Core PLL.

Return to [Summary Table](#)

**Table 2-2133. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0400h       |

**Figure 2-710. MSS\_TOPRCM\_PLL\_CORE\_PWRCTRL Name Register**

|          |                                |                                  |                          |                                 |                                  |                                  |     |
|----------|--------------------------------|----------------------------------|--------------------------|---------------------------------|----------------------------------|----------------------------------|-----|
| 31       | 30                             | 29                               | 28                       | 27                              | 26                               | 25                               | 24  |
| RESERVED |                                |                                  |                          |                                 |                                  |                                  |     |
| NONE     |                                |                                  |                          |                                 |                                  |                                  |     |
| 0h       |                                |                                  |                          |                                 |                                  |                                  |     |
| 23       | 22                             | 21                               | 20                       | 19                              | 18                               | 17                               | 16  |
| RESERVED |                                |                                  |                          |                                 |                                  |                                  |     |
| NONE     |                                |                                  |                          |                                 |                                  |                                  |     |
| 0h       |                                |                                  |                          |                                 |                                  |                                  |     |
| 15       | 14                             | 13                               | 12                       | 11                              | 10                               | 9                                | 8   |
| RESERVED |                                |                                  |                          |                                 |                                  |                                  |     |
| NONE     |                                |                                  |                          |                                 |                                  |                                  |     |
| 0h       |                                |                                  |                          |                                 |                                  |                                  |     |
| 7        | 6                              | 5                                | 4                        | 3                               | 2                                | 1                                | 0   |
| RESERVED | PLL_CORE_P<br>WRCTRL_PON<br>IN | PLL_CORE_P<br>WRCTRL_PGO<br>ODIN | PLL_CORE_P<br>WRCTRL_RET | PLL_CORE_P<br>WRCTRL_ISO<br>RET | PLL_CORE_P<br>WRCTRL_ISOS<br>CAN | PLL_CORE_P<br>WRCTRL_OFF<br>MODE |     |
| NONE     | R/W                            | R/W                              | R/W                      | R/W                             | R/W                              | R/W                              | R/W |
| 0h       | 1h                             | 1h                               | 0h                       | 0h                              | 0h                               | 0h                               | 0h  |

**Table 2-2135. MSS\_TOPRCM\_PLL\_CORE\_PWRCTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                   |
|------|--------------------------|------|-------|-----------------------------------------------------------------------------------------------|
| 31:6 | RESERVED                 | NONE | 0h    | Reserved                                                                                      |
| 5    | PLL_CORE_PWRCTRL_PONIN   | R/W  | 1h    | ON/OFF control of the weak power switch digital. For functional mode it should be 1'b1        |
| 4    | PLL_CORE_PWRCTRL_PGOODIN | R/W  | 1h    | ON/OFF control of the strong power switch digital. For functional mode it should be 1'b1      |
| 3    | PLL_CORE_PWRCTRL_RET     | R/W  | 0h    | Save/Restore control for Retention mode. For functional mode it should be 1'b0                |
| 2    | PLL_CORE_PWRCTRL_ISORET  | R/W  | 0h    | Save/Restore control for Isolation of output pins For functional mode it should be 1'b0       |
| 1    | PLL_CORE_PWRCTRL_ISOSCAN | R/W  | 0h    | Save/Restore control for Isolation of the Scanout pins. For functional mode it should be 1'b0 |
| 0    | PLL_CORE_PWRCTRL_OFFMODE | R/W  | 0h    | Used to switch OFF the logic on VDDA. For functional mode it should be 1'b0                   |

### 2.5.2.14 MSS\_TOPRCM\_PLL\_CORE\_CLKCTRL Register

#### 1 MSS\_TOPRCM\_PLL\_CORE\_CLKCTRL Register (Offset = 404h) [reset = 895000h]

Clock control for Core PLL.

Return to [Summary Table](#)

**Table 2-2136. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0404h       |

**Figure 2-711. MSS\_TOPRCM\_PLL\_CORE\_CLKCTRL Name Register**

| 31                           | 30                          | 29                           | 28                          | 27                           | 26                         | 25                              | 24                            |
|------------------------------|-----------------------------|------------------------------|-----------------------------|------------------------------|----------------------------|---------------------------------|-------------------------------|
| PLL_CORE_CLKCTRL_CYCLESLIPEN | PLL_CORE_CLKCTRL_ENSSC      | PLL_CORE_CLKCTRL_CLKDCOLDOEN | RESERVED                    |                              |                            |                                 |                               |
| R/W                          | R/W                         | R/W                          | NONE                        |                              |                            |                                 |                               |
| 0h                           | 0h                          | 0h                           | 0h                          |                              |                            |                                 |                               |
| 23                           | 22                          | 21                           | 20                          | 19                           | 18                         | 17                              | 16                            |
| PLL_CORE_CLKCTRL_IDLE        | PLL_CORE_CLKCTRL_BYPASSACKZ | PLL_CORE_CLKCTRL_STBYRET     | PLL_CORE_CLKCTRL_CLKOUTEN   | PLL_CORE_CLKCTRL_CLKOUTLDOEN | PLL_CORE_CLKCTRL_ULOWCLKEN | PLL_CORE_CLKCTRL_CLKDCOLDOPWDNZ | PLL_CORE_CLKCTRL_M2PWDNZ      |
| R/W                          | R/W                         | R/W                          | R/W                         | R/W                          | R/W                        | R/W                             | R/W                           |
| 1h                           | 0h                          | 0h                           | 0h                          | 1h                           | 0h                         | 0h                              | 1h                            |
| 15                           | 14                          | 13                           | 12                          | 11                           | 10                         | 9                               | 8                             |
| RESERVED                     | PLL_CORE_CLKCTRL_STOPMODE   | RESERVED                     | PLL_CORE_CLKCTRL_SELFREQDCO |                              |                            | RESERVED                        | PLL_CORE_CLKCTRL_RELAXED_LOCK |
| NONE                         | R/W                         | NONE                         | R/W                         |                              |                            | NONE                            | R/W                           |
| 0h                           | 1h                          | 0h                           | 4h                          |                              |                            | 0h                              | 0h                            |
| 7                            | 6                           | 5                            | 4                           | 3                            | 2                          | 1                               | 0                             |
| RESERVED                     |                             |                              |                             |                              |                            | PLL_CORE_CLKCTRL_SSCTYPE        | PLL_CORE_CLKCTRL_TINTZ        |
| NONE                         |                             |                              |                             |                              |                            | R/W                             | R/W                           |
| 0h                           |                             |                              |                             |                              |                            | 0h                              | 0h                            |

**Table 2-2138. MSS\_TOPRCM\_PLL\_CORE\_CLKCTRL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                                                                                                                                                       |
|-------|------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | PLL_CORE_CLKCTRL_CYCLESLIPEN | R/W  | 0h    | FailSafe enable to trigger re-calibration in case CycleSlip occurs between REFCLK and FBCLK. Cycleslip could be caused if loop is not able to track input clock. Default = 1'b0 recommended       |
| 30    | PLL_CORE_CLKCTRL_ENSSC       | R/W  | 0h    | Controls Clock SpReading. SSC is not supported. Should be set to 0x0 to disable clock spReading.                                                                                                  |
| 29    | PLL_CORE_CLKCTRL_CLKDCOLDOEN | R/W  | 0h    | Synchronously enables/disables CLKDCOLDO<br>0x0 : synchronously disables CLKDCOLDO<br>0x1 : synchronously enables CLKDCOLDO                                                                       |
| 28:24 | RESERVED                     | NONE | 0h    | Reserved                                                                                                                                                                                          |
| 23    | PLL_CORE_CLKCTRL_IDLE        | R/W  | 1h    | Sets PLL to Idle mode<br>0x0 : When SYSRESET = 0 and TINITZ = 1 IDLE = 0 PLL will go to Active and Locked<br>0x1 : When SYSRESET = 0 and TINITZ = 1 IDLE = 1 PLL will go to Idle Bypass low power |

**Table 2-2138. MSS\_TOPRCM\_PLL\_CORE\_CLKCTRL Register Field Descriptions (continued)**

| Bit   | Field                           | Type | Reset | Description                                                                                                                                                                                                                                                                          |
|-------|---------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 22    | PLL_CORE_CLKCTRL_BYPASSACKZ     | R/W  | 0h    | BYPASSACKZ is a special purpose input to the module. In general this input is expected to be tied to static low. For the output clocks of the module that do not have an internal bypass mux viz. CLKDCOLDO and CLKOUTLDO, a bypass mux could be implemented external to the module. |
| 21    | PLL_CORE_CLKCTRL_STBYRET        | R/W  | 0h    | Standby retention control<br>0x0 : prepares ADPLLJ for relock when out of retention by removing the gating on all internal clocks.<br>0x1 : prepares ADPLLJ for retention by gating all the internal clocks.                                                                         |
| 20    | PLL_CORE_CLKCTRL_CLKOUTEN       | R/W  | 0h    | CLKOUT enable or disable<br>0x0 : synchronously disables CLKOUT<br>0x1 : synchronously enables CLKOUT                                                                                                                                                                                |
| 19    | PLL_CORE_CLKCTRL_CLKOUTLDOEN    | R/W  | 1h    | Synchronously enables/disables CLKOUTLDO<br>0x0 : synchronously disables CLKOUTLDO<br>0x1 : synchronously enables CLKOUTLDO                                                                                                                                                          |
| 18    | PLL_CORE_CLKCTRL_LOWCLKEN       | R/W  | 0h    | Select CLKOUT source in bypass<br>0x0: When ADPLLJ in bypass mode, CLKOUT = CLKINP/[N2+1]<br>0x1: When ADPLLJ in bypass mode, CLKOUT = CLKINPULOW.                                                                                                                                   |
| 17    | PLL_CORE_CLKCTRL_CLKDCOLDOPWDNZ | R/W  | 0h    | 0 Asynchronous power down for CLKDCOLDO o/p.                                                                                                                                                                                                                                         |
| 16    | PLL_CORE_CLKCTRL_M2PWDNZ        | R/W  | 1h    | M2 divider power down mode<br>0x0: Asynchronous power down for M2 divider<br>0x1 : M2 divider is functional                                                                                                                                                                          |
| 15    | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                             |
| 14    | PLL_CORE_CLKCTRL_STOPMODE       | R/W  | 1h    | When in Lossclk/Stbyret 0x0 : Limp mode 0x1 : Stopmode                                                                                                                                                                                                                               |
| 13    | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                             |
| 12:10 | PLL_CORE_CLKCTRL_SELFREQDCO     | R/W  | 4h    | DCO Clock [DCOCLK = CLKINP * [M/[N+1]]] frequency range selector.<br>0x0: Reserved<br>0x2: HS2 : DCOCLK range is from 500 MHz to 1000MHz<br>0x3: Reserved<br>0x4: HS1: DCOCLK range is from 1000MHz to 2000MHz<br>0x5: Reserved                                                      |
| 9     | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                             |
| 8     | PLL_CORE_CLKCTRL_RELAXED_LOCK   | R/W  | 0h    | Decides when FREQLOCK asserted<br>0x0: FREQLOCK asserted when DC frequency error less than 1%<br>0x1: FREQLOCK asserted when DC frequency error less than 2%                                                                                                                         |
| 7:2   | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                             |
| 1     | PLL_CORE_CLKCTRL_SCTYPE         | R/W  | 0h    | SSC Type - This should be configured as 1'b0. The module does not supports spread spectrum clocking [SSC] on its output clocks.                                                                                                                                                      |
| 0     | PLL_CORE_CLKCTRL_TINITZ         | R/W  | 0h    | PLL core soft reset. TINITZ activation [Low] gives softreset to ADPLLJ. TINITZ does not reset the entire digital control logic; it forces the FSM into RESET State so that ADPLLJ could restart.                                                                                     |

### 2.5.2.15 MSS\_TOPRCM\_PLL\_CORE\_TENABLE Register

#### 1 MSS\_TOPRCM\_PLL\_CORE\_TENABLE Register (Offset = 408h) [reset = 0h]

Trigger enable for core PLL.

Return to [Summary Table](#)

**Table 2-2139. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0408h       |

**Figure 2-712. MSS\_TOPRCM\_PLL\_CORE\_TENABLE Name Register**

|          |    |    |    |    |    |    |                  |
|----------|----|----|----|----|----|----|------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24               |
| RESERVED |    |    |    |    |    |    |                  |
| NONE     |    |    |    |    |    |    |                  |
| 0h       |    |    |    |    |    |    |                  |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16               |
| RESERVED |    |    |    |    |    |    |                  |
| NONE     |    |    |    |    |    |    |                  |
| 0h       |    |    |    |    |    |    |                  |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                |
| RESERVED |    |    |    |    |    |    |                  |
| NONE     |    |    |    |    |    |    |                  |
| 0h       |    |    |    |    |    |    |                  |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                |
| RESERVED |    |    |    |    |    |    | PLL_CORE_TENABLE |
| NONE     |    |    |    |    |    |    | R/W              |
| 0h       |    |    |    |    |    |    | 0h               |

**Table 2-2141. MSS\_TOPRCM\_PLL\_CORE\_TENABLE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                  |
|------|--------------------------|------|-------|--------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED                 | NONE | 0h    | Reserved                                                                                                     |
| 0    | PLL_CORE_TENABLE_TENABLE | R/W  | 0h    | Signal TENABLE loads REGM, REGN, REGSD and SELFREQDCO data. M, N, SD and SELFREQDCO latch [active rise edge] |

### 2.5.2.16 MSS\_TOPRCM\_PLL\_CORE\_TENABLEDIV Register

#### 1 MSS\_TOPRCM\_PLL\_CORE\_TENABLEDIV Register (Offset = 40Ch) [reset = 0h]

Load Trigger for divider control value for Core PLL.

Return to [Summary Table](#)

**Table 2-2142. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 040Ch       |

**Figure 2-713. MSS\_TOPRCM\_PLL\_CORE\_TENABLEDIV Name Register**

|          |    |    |    |    |    |    |                                |
|----------|----|----|----|----|----|----|--------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                             |
| RESERVED |    |    |    |    |    |    |                                |
| NONE     |    |    |    |    |    |    |                                |
| 0h       |    |    |    |    |    |    |                                |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                             |
| RESERVED |    |    |    |    |    |    |                                |
| NONE     |    |    |    |    |    |    |                                |
| 0h       |    |    |    |    |    |    |                                |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                              |
| RESERVED |    |    |    |    |    |    |                                |
| NONE     |    |    |    |    |    |    |                                |
| 0h       |    |    |    |    |    |    |                                |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                              |
| RESERVED |    |    |    |    |    |    | PLL_CORE_TENABLEDIV_TENABLEDIV |
| NONE     |    |    |    |    |    |    | R/W                            |
| 0h       |    |    |    |    |    |    | 0h                             |

**Table 2-2144. MSS\_TOPRCM\_PLL\_CORE\_TENABLEDIV Register Field Descriptions**

| Bit  | Field                          | Type | Reset | Description                                                                                                                                                                                               |
|------|--------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                  |
| 0    | PLL_CORE_TENABLEDIV_TENABLEDIV | R/W  | 0h    | TENABLEDIV rising edge loads the values of M2REG and N2REG into ADPLLJ register. TENABLEDIV could be activated anytime when the DPLL digital is in power-up condition. M2 and N2 latch [active rise edge] |

### 2.5.2.17 MSS\_TOPRCM\_PLL\_CORE\_M2NDIV Register

#### 1 MSS\_TOPRCM\_PLL\_CORE\_M2NDIV Register (Offset = 410h) [reset = 13h]

M2N config register for core PLL.

Return to [Summary Table](#)

**Table 2-2145. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0410h       |

**Figure 2-714. MSS\_TOPRCM\_PLL\_CORE\_M2NDIV Name Register**

|                   |                    |    |    |    |    |    |    |
|-------------------|--------------------|----|----|----|----|----|----|
| 31                | 30                 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED          |                    |    |    |    |    |    |    |
| NONE              |                    |    |    |    |    |    |    |
| 0h                |                    |    |    |    |    |    |    |
| 23                | 22                 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED          | PLL_CORE_M2NDIV_M2 |    |    |    |    |    |    |
| NONE              | R/W                |    |    |    |    |    |    |
| 0h                | 0h                 |    |    |    |    |    |    |
| 15                | 14                 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED          |                    |    |    |    |    |    |    |
| NONE              |                    |    |    |    |    |    |    |
| 0h                |                    |    |    |    |    |    |    |
| 7                 | 6                  | 5  | 4  | 3  | 2  | 1  | 0  |
| PLL_CORE_M2NDIV_N |                    |    |    |    |    |    |    |
| R/W               |                    |    |    |    |    |    |    |
| 13h               |                    |    |    |    |    |    |    |

**Table 2-2147. MSS\_TOPRCM\_PLL\_CORE\_M2NDIV Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description           |
|-------|--------------------|------|-------|-----------------------|
| 31:23 | RESERVED           | NONE | 0h    | Reserved              |
| 22:16 | PLL_CORE_M2NDIV_M2 | R/W  | 0h    | Post-divider is REGM2 |
| 15:8  | RESERVED           | NONE | 0h    | Reserved              |
| 7:0   | PLL_CORE_M2NDIV_N  | R/W  | 13h   | Pre-divider is REGN+1 |



### 2.5.2.18 MSS\_TOPRCM\_PLL\_CORE\_MN2DIV Register

#### 1 MSS\_TOPRCM\_PLL\_CORE\_MN2DIV Register (Offset = 414h) [reset = 640h]

MN2 config register for core PLL.

Return to [Summary Table](#)

**Table 2-2148. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0414h       |

**Figure 2-715. MSS\_TOPRCM\_PLL\_CORE\_MN2DIV Name Register**

|                   |    |    |    |                    |    |    |    |
|-------------------|----|----|----|--------------------|----|----|----|
| 31                | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED          |    |    |    |                    |    |    |    |
| NONE              |    |    |    |                    |    |    |    |
| 0h                |    |    |    |                    |    |    |    |
| 23                | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED          |    |    |    | PLL_CORE_MN2DIV_N2 |    |    |    |
| NONE              |    |    |    | R/W                |    |    |    |
| 0h                |    |    |    | 0h                 |    |    |    |
| 15                | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED          |    |    |    | PLL_CORE_MN2DIV_M  |    |    |    |
| NONE              |    |    |    | R/W                |    |    |    |
| 0h                |    |    |    | 640h               |    |    |    |
| 7                 | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| PLL_CORE_MN2DIV_M |    |    |    |                    |    |    |    |
| R/W               |    |    |    |                    |    |    |    |
| 640h              |    |    |    |                    |    |    |    |

**Table 2-2150. MSS\_TOPRCM\_PLL\_CORE\_MN2DIV Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                 |
|-------|--------------------|------|-------|-----------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                    |
| 19:16 | PLL_CORE_MN2DIV_N2 | R/W  | 0h    | Bypass divider is REGN2+1   |
| 15:12 | RESERVED           | NONE | 0h    | Reserved                    |
| 11:0  | PLL_CORE_MN2DIV_M  | R/W  | 640h  | Feedback Multiplier is REGM |

### 2.5.2.19 MSS\_TOPRCM\_PLL\_CORE\_FRACDIV Register

#### 1 MSS\_TOPRCM\_PLL\_CORE\_FRACDIV Register (Offset = 418h) [reset = 8000000h]

Fractional divider and Sigma Delta config register for Core PLL.

Return to [Summary Table](#)

**Table 2-2151. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0418h       |

**Figure 2-716. MSS\_TOPRCM\_PLL\_CORE\_FRACDIV Name Register**

|                              |    |    |    |    |    |                              |    |
|------------------------------|----|----|----|----|----|------------------------------|----|
| 31                           | 30 | 29 | 28 | 27 | 26 | 25                           | 24 |
| PLL_CORE_FRACDIV_REGSD       |    |    |    |    |    |                              |    |
| R/W                          |    |    |    |    |    |                              |    |
| 8h                           |    |    |    |    |    |                              |    |
| 23                           | 22 | 21 | 20 | 19 | 18 | 17                           | 16 |
| RESERVED                     |    |    |    |    |    | PLL_CORE_FRACDIV_FRACTIONALM |    |
| NONE                         |    |    |    |    |    | R/W                          |    |
| 0h                           |    |    |    |    |    | 0h                           |    |
| 15                           | 14 | 13 | 12 | 11 | 10 | 9                            | 8  |
| PLL_CORE_FRACDIV_FRACTIONALM |    |    |    |    |    |                              |    |
| R/W                          |    |    |    |    |    |                              |    |
| 0h                           |    |    |    |    |    |                              |    |
| 7                            | 6  | 5  | 4  | 3  | 2  | 1                            | 0  |
| PLL_CORE_FRACDIV_FRACTIONALM |    |    |    |    |    |                              |    |
| R/W                          |    |    |    |    |    |                              |    |
| 0h                           |    |    |    |    |    |                              |    |

**Table 2-2153. MSS\_TOPRCM\_PLL\_CORE\_FRACDIV Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | PLL_CORE_FRACDIV_REGSD       | R/W  | 8h    | Sigma-Delta Divider<br>Should be set by s/w to provide optimum jitter performance.<br>$DPLL\_SD\_DIV = \text{CEILING} \left[ \frac{DPLL\_MULT}{DPLL\_DIV+1} \right] * CLKINP / 250$ , where CLKINP is the input clock of the DPLL in MHz |
| 23:18 | RESERVED                     | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 17:0  | PLL_CORE_FRACDIV_FRACTIONALM | R/W  | 0h    | Fractional part of the M divider. The 18bit FractionalM value is loaded into DPLL on the rising edge of TENABLE signal. To enable Integer only division FractionalM should be set to 18'b0.                                              |

### 2.5.2.20 MSS\_TOPRCM\_PLL\_CORE\_BWCTRL Register

#### 1 MSS\_TOPRCM\_PLL\_CORE\_BWCTRL Register (Offset = 41Ch) [reset = 0h]

Loop bandwidth control for Core PLL.

Return to [Summary Table](#)

**Table 2-2154. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 041Ch       |

**Figure 2-717. MSS\_TOPRCM\_PLL\_CORE\_BWCTRL Name Register**

|          |    |    |    |    |                               |                                   |    |
|----------|----|----|----|----|-------------------------------|-----------------------------------|----|
| 31       | 30 | 29 | 28 | 27 | 26                            | 25                                | 24 |
| RESERVED |    |    |    |    |                               |                                   |    |
| NONE     |    |    |    |    |                               |                                   |    |
| 0h       |    |    |    |    |                               |                                   |    |
| 23       | 22 | 21 | 20 | 19 | 18                            | 17                                | 16 |
| RESERVED |    |    |    |    |                               |                                   |    |
| NONE     |    |    |    |    |                               |                                   |    |
| 0h       |    |    |    |    |                               |                                   |    |
| 15       | 14 | 13 | 12 | 11 | 10                            | 9                                 | 8  |
| RESERVED |    |    |    |    |                               |                                   |    |
| NONE     |    |    |    |    |                               |                                   |    |
| 0h       |    |    |    |    |                               |                                   |    |
| 7        | 6  | 5  | 4  | 3  | 2                             | 1                                 | 0  |
| RESERVED |    |    |    |    | PLL_CORE_BWCTRL_BWCONT<br>ROL | PLL_CORE_BWCTRL_BW_I<br>NCR_DECRZ |    |
| NONE     |    |    |    |    | R/W                           | R/W                               |    |
| 0h       |    |    |    |    | 0h                            | 0h                                |    |

**Table 2-2156. MSS\_TOPRCM\_PLL\_CORE\_BWCTRL Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                                           |
|------|-------------------------------|------|-------|-----------------------------------------------------------------------|
| 31:3 | RESERVED                      | NONE | 0h    | Reserved                                                              |
| 2:1  | PLL_CORE_BWCTRL_BWCONTROL     | R/W  | 0h    | Change Loop Bandwidth                                                 |
| 0    | PLL_CORE_BWCTRL_BW_INCR_DECRZ | R/W  | 0h    | Direction of Loop Bandwidth<br>0x0 : decrease BW<br>0x1 : increase BW |

### 2.5.2.21 MSS\_TOPRCM\_PLL\_CORE\_FRACCTRL Register

#### 1 MSS\_TOPRCM\_PLL\_CORE\_FRACCTRL Register (Offset = 420h) [reset = 0h]

Spread Spectrum control for Core PLL - Not Supported.

Return to [Summary Table](#)

**Table 2-2157. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0420h       |

**Figure 2-718. MSS\_TOPRCM\_PLL\_CORE\_FRACCTRL Name Register**

| 31                                       | 30                                       | 29 | 28                                  | 27                                       | 26 | 25                                   | 24 |
|------------------------------------------|------------------------------------------|----|-------------------------------------|------------------------------------------|----|--------------------------------------|----|
| PLL_CORE_FRACCTRL_DOWNSPREAD             | PLL_CORE_FRACCTRL_MODFREQDIVIDEREXPONENT |    |                                     | PLL_CORE_FRACCTRL_MODFREQDIVIDERMANТИSSA |    |                                      |    |
| R/W                                      | R/W                                      |    |                                     | R/W                                      |    |                                      |    |
| 0h                                       | 0h                                       |    |                                     | 0h                                       |    |                                      |    |
| 23                                       | 22                                       | 21 | 20                                  | 19                                       | 18 | 17                                   | 16 |
| PLL_CORE_FRACCTRL_MODFREQDIVIDERMANТИSSA |                                          |    | PLL_CORE_FRACCTRL_DELTAMSTEPINTEGER |                                          |    | PLL_CORE_FRACCTRL_DELTAMSTEPFRACTION |    |
| R/W                                      |                                          |    | R/W                                 |                                          |    | R/W                                  |    |
| 0h                                       |                                          |    | 0h                                  |                                          |    | 0h                                   |    |
| 15                                       | 14                                       | 13 | 12                                  | 11                                       | 10 | 9                                    | 8  |
| PLL_CORE_FRACCTRL_DELTAMSTEPFRACTION     |                                          |    |                                     |                                          |    |                                      |    |
| R/W                                      |                                          |    |                                     |                                          |    |                                      |    |
| 0h                                       |                                          |    |                                     |                                          |    |                                      |    |
| 7                                        | 6                                        | 5  | 4                                   | 3                                        | 2  | 1                                    | 0  |
| PLL_CORE_FRACCTRL_DELTAMSTEPFRACTION     |                                          |    |                                     |                                          |    |                                      |    |
| R/W                                      |                                          |    |                                     |                                          |    |                                      |    |
| 0h                                       |                                          |    |                                     |                                          |    |                                      |    |

**Table 2-2159. MSS\_TOPRCM\_PLL\_CORE\_FRACCTRL Register Field Descriptions**

| Bit   | Field                                    | Type | Reset | Description                                                                                                                                      |
|-------|------------------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | PLL_CORE_FRACCTRL_DOWNSPREAD             | R/W  | 0h    | Controls frequency spread<br>0x0 : enables both side frequency spread about the programmed frequency.<br>0x1 : enables low frequency spread only |
| 30:28 | PLL_CORE_FRACCTRL_MODFREQDIVIDEREXPONENT | R/W  | 0h    | Exponent of the REFCLK divider to define the modulation frequency.                                                                               |
| 27:21 | PLL_CORE_FRACCTRL_MODFREQDIVIDERMANТИSSA | R/W  | 0h    | Mantissa of the REFCLK divider to define the modulation frequency                                                                                |
| 20:18 | PLL_CORE_FRACCTRL_DELTAMSTEPINTEGER      | R/W  | 0h    | Integer part of Frequency Spread control                                                                                                         |
| 17:0  | PLL_CORE_FRACCTRL_DELTAMSTEPFRACTION     | R/W  | 0h    | The fraction part of Frequency Spread control                                                                                                    |

### 2.5.2.22 MSS\_TOPRCM\_PLL\_CORE\_STATUS Register

#### 1 MSS\_TOPRCM\_PLL\_CORE\_STATUS Register (Offset = 424h) [reset = E0001141h]

Core PLL status register.

Return to [Summary Table](#)

**Table 2-2160. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0424h       |

**Figure 2-719. MSS\_TOPRCM\_PLL\_CORE\_STATUS Name Register**

| 31                                 | 30                               | 29                                  | 28                                     | 27                                   | 26                                | 25                                 | 24                                |
|------------------------------------|----------------------------------|-------------------------------------|----------------------------------------|--------------------------------------|-----------------------------------|------------------------------------|-----------------------------------|
| PLL_CORE_ST<br>ATUS_PONOU<br>T     | PLL_CORE_ST<br>ATUS_PGOOD<br>OUT | PLL_CORE_ST<br>ATUS_LDOPW<br>DN     | PLL_CORE_ST<br>ATUS_RECAL_<br>BSTATUS3 | PLL_CORE_ST<br>ATUS_RECAL_<br>OPPIN  | RESERVED                          |                                    |                                   |
| R                                  | R                                | R                                   | R                                      | R                                    | NONE                              |                                    |                                   |
| 1h                                 | 1h                               | 1h                                  | 0h                                     | 0h                                   | 0h                                |                                    |                                   |
| 23                                 | 22                               | 21                                  | 20                                     | 19                                   | 18                                | 17                                 | 16                                |
| RESERVED                           |                                  |                                     |                                        |                                      |                                   |                                    |                                   |
| NONE                               |                                  |                                     |                                        |                                      |                                   |                                    |                                   |
| 0h                                 |                                  |                                     |                                        |                                      |                                   |                                    |                                   |
| 15                                 | 14                               | 13                                  | 12                                     | 11                                   | 10                                | 9                                  | 8                                 |
| RESERVED                           |                                  |                                     | PLL_CORE_ST<br>ATUS_CLKOUT<br>LDOENACK | PLL_CORE_ST<br>ATUS_CLKDC<br>OLDOACK | PLL_CORE_ST<br>ATUS_PHASEL<br>OCK | PLL_CORE_ST<br>ATUS_FREQ<br>LDOCK  | PLL_CORE_ST<br>ATUS_BYPASS<br>ACK |
| NONE                               |                                  |                                     | R                                      | R                                    | R                                 | R                                  | R                                 |
| 0h                                 |                                  |                                     | 1h                                     | 0h                                   | 0h                                | 0h                                 | 1h                                |
| 7                                  | 6                                | 5                                   | 4                                      | 3                                    | 2                                 | 1                                  | 0                                 |
| PLL_CORE_ST<br>ATUS_STBYRE<br>TACK | PLL_CORE_ST<br>ATUS_LOSSRE<br>F  | PLL_CORE_ST<br>ATUS_CLKOUT<br>ENACK | PLL_CORE_ST<br>ATUS_LOCK2              | PLL_CORE_ST<br>ATUS_M2CHA<br>NGEACK  | PLL_CORE_ST<br>ATUS_SSCAC<br>K    | PLL_CORE_ST<br>ATUS_HIGHJIT<br>TER | PLL_CORE_ST<br>ATUS_BYPASS        |
| R                                  | R                                | R                                   | R                                      | R                                    | R                                 | R                                  | R                                 |
| 0h                                 | 1h                               | 0h                                  | 0h                                     | 0h                                   | 0h                                | 0h                                 | 1h                                |

**Table 2-2162. MSS\_TOPRCM\_PLL\_CORE\_STATUS Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                                                                                                                           |
|-------|------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | PLL_CORE_STATUS_PO<br>NOUT         | R    | 1h    | Status of the weak power-switch<br>0x0 : indicates the/OFF status of the weak power-switch in digital to<br>SOC.<br>0x1 : ndicates the ON status of the weak power-switch in digital to<br>SOC.       |
| 30    | PLL_CORE_STATUS_PG<br>OODOUT       | R    | 1h    | Status of the strong power-switch<br>0x0 : indicates the/OFF status of the strong power-switch in digital to<br>SOC.<br>0x1 : ndicates the ON status of the strong power-switch in digital to<br>SOC. |
| 29    | PLL_CORE_STATUS_LD<br>OPWDN        | R    | 1h    | 1'b1 indicates ADPLLLJ internal LDO is power down. VDDLDOOUT<br>will<br>be un-defined in this condition                                                                                               |
| 28    | PLL_CORE_STATUS_RE<br>CAL_BSTATUS3 | R    | 0h    | Recalibration status flag. 1'b1 ADPLLLJ requires recalibration                                                                                                                                        |
| 27    | PLL_CORE_STATUS_RE<br>CAL_OPPIN    | R    | 0h    | Recalibration status flag. 1'b1 ADPLLLJ requires recalibration                                                                                                                                        |
| 26:13 | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                                              |

**Table 2-2162. MSS\_TOPRCM\_PLL\_CORE\_STATUS Register Field Descriptions (continued)**

| Bit | Field                          | Type | Reset | Description                                                                                                                                                                                                                                       |
|-----|--------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12  | PLL_CORE_STATUS_CLKOUTLDOENACK | R    | 1h    | Indicates the enable/disable condition of CLKOUTLDOEN<br>0x0 = CLKOUTLDO gating completed<br>0x1 = CLKOUTLDO enabling completed                                                                                                                   |
| 11  | PLL_CORE_STATUS_CLKDCOLDOACK   | R    | 0h    | Indicates the enable/disable condition of CLKDCOLDOEN<br>0x0 = CLKDCOLDO gating completed<br>0x1 = CLKDCOLOD enabling completed                                                                                                                   |
| 10  | PLL_CORE_STATUS_PHASELOCK      | R    | 0h    | Status on PHASELOCK output pin                                                                                                                                                                                                                    |
| 9   | PLL_CORE_STATUS_FREQLOCK       | R    | 0h    | Status on FREQLOCK output pin                                                                                                                                                                                                                     |
| 8   | PLL_CORE_STATUS_BYPASSACK      | R    | 1h    | Status of BYPASSACK output pin                                                                                                                                                                                                                    |
| 7   | PLL_CORE_STATUS_STBYRETACK     | R    | 0h    | Standby and retention status<br>0x0: indicates to SOC that all internal clocks in ADPLLLJ are active and it is starting the relock process.<br>0x1: indicates to SOC that all internal clocks in ADPLLLJ are gated and it is ready for retention. |
| 6   | PLL_CORE_STATUS_LOSSREF        | R    | 1h    | Reference input loss is indicated by 1'b0.                                                                                                                                                                                                        |
| 5   | PLL_CORE_STATUS_CLKOUTENACK    | R    | 0h    | Indicates the enable/disable condition of CLKOUTEN<br>0x0 = CLKOUT gating completed<br>0x1 = CLKOUT enabling completed                                                                                                                            |
| 4   | PLL_CORE_STATUS_LOOPLOCK2      | R    | 0h    | ADPLL internal loop lock status                                                                                                                                                                                                                   |
| 3   | PLL_CORE_STATUS_M2CHANGEACK    | R    | 0h    | Acknowledge for change to M2 divider. Toggles from 1-0 or 0-1 [depending on current value] once CLKOUT frequency change has completed.                                                                                                            |
| 2   | PLL_CORE_STATUS_SSCLKACK       | R    | 0h    | Spread Spectrum status<br>0x0 : Spread-spectrum Clocking is disabled on output clocks<br>0x1 : Spread-spectrum Clocking is enabled on output clocks                                                                                               |
| 1   | PLL_CORE_STATUS_HIGHJITTER     | R    | 0h    | 1'b1 indicates jitter. After PHASELOCK is asserted high, the HIGHJITTER flag is asserted high if phase error between REFCLK and FBCLK greater than 24%.                                                                                           |
| 0   | PLL_CORE_STATUS_BYPASS         | R    | 1h    | Bypass status signal. 1 CLKOUT in bypass                                                                                                                                                                                                          |

### 2.5.2.23 MSS\_TOPRCM\_PLL\_CORE\_HSDIVIDER Register

#### 1 MSS\_TOPRCM\_PLL\_CORE\_HSDIVIDER Register (Offset = 428h) [reset = 0h]

Core PLL high speed divider config.

Return to [Summary Table](#)

**Table 2-2163. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0428h       |

**Figure 2-720. MSS\_TOPRCM\_PLL\_CORE\_HSDIVIDER Name Register**

|          |    |    |    |    |                                       |                                       |                                       |
|----------|----|----|----|----|---------------------------------------|---------------------------------------|---------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26                                    | 25                                    | 24                                    |
| RESERVED |    |    |    |    |                                       |                                       |                                       |
| NONE     |    |    |    |    |                                       |                                       |                                       |
| 0h       |    |    |    |    |                                       |                                       |                                       |
| 23       | 22 | 21 | 20 | 19 | 18                                    | 17                                    | 16                                    |
| RESERVED |    |    |    |    |                                       | PLL_CORE_HS<br>DIVIDER_LDO<br>PWDNACK | PLL_CORE_HS<br>DIVIDER_BYPA<br>SSACKZ |
| NONE     |    |    |    |    |                                       | R                                     | R                                     |
| 0h       |    |    |    |    |                                       | 0h                                    | 0h                                    |
| 15       | 14 | 13 | 12 | 11 | 10                                    | 9                                     | 8                                     |
| RESERVED |    |    |    |    |                                       |                                       |                                       |
| NONE     |    |    |    |    |                                       |                                       |                                       |
| 0h       |    |    |    |    |                                       |                                       |                                       |
| 7        | 6  | 5  | 4  | 3  | 2                                     | 1                                     | 0                                     |
| RESERVED |    |    |    |    | PLL_CORE_HS<br>DIVIDER_TEN<br>ABLEDIV | PLL_CORE_HS<br>DIVIDER_LDO<br>PWDN    | PLL_CORE_HS<br>DIVIDER_BYPA<br>SS     |
| NONE     |    |    |    |    | R/W                                   | R/W                                   | R/W                                   |
| 0h       |    |    |    |    | 0h                                    | 0h                                    | 0h                                    |

**Table 2-2165. MSS\_TOPRCM\_PLL\_CORE\_HSDIVIDER Register Field Descriptions**

| Bit   | Field                         | Type | Reset | Description                                                                                                                                                                                               |
|-------|-------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                      | NONE | 0h    | Reserved                                                                                                                                                                                                  |
| 17    | PLL_CORE_HSDIVIDER_LDOPWDNACK | R    | 0h    | LDO Power Down Ack                                                                                                                                                                                        |
| 16    | PLL_CORE_HSDIVIDER_BYPASSACKZ | R    | 0h    | HSDIVIDER Bypass Ack                                                                                                                                                                                      |
| 15:3  | RESERVED                      | NONE | 0h    | Reserved                                                                                                                                                                                                  |
| 2     | PLL_CORE_HSDIVIDER_TENABLEDIV | R/W  | 0h    | TENABLEDIV rising edge loads the values of M2REG and N2REG into ADPLLJ register. TENABLEDIV could be activated anytime when the DPLL digital is in power-up condition. M2 and N2 latch [active rise edge] |
| 1     | PLL_CORE_HSDIVIDER_LDOPWDN    | R/W  | 0h    | 1'b1 indicates ADPLLJ internal LDO is power down. VDDLDOOUT will be un-defined in this condition                                                                                                          |
| 0     | PLL_CORE_HSDIVIDER_BYPASS     | R/W  | 0h    | HSDIVIDER Bypass. Set it to 1'b1 to bypass the HSDIVIDER.                                                                                                                                                 |

### 2.5.2.24 MSS\_TOPRCM\_PLL\_CORE\_HSDIVIDER\_CLKOUT0 Register

#### 1 MSS\_TOPRCM\_PLL\_CORE\_HSDIVIDER\_CLKOUT0 Register (Offset = 42Ch) [reset = 4h]

Core PLL high speed divider clock 0 control.

Return to [Summary Table](#)

**Table 2-2166. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 042Ch       |

**Figure 2-721. MSS\_TOPRCM\_PLL\_CORE\_HSDIVIDER\_CLKOUT0 Name Register**

|          |    |                                                 |                                         |          |    |                                           |                                                  |
|----------|----|-------------------------------------------------|-----------------------------------------|----------|----|-------------------------------------------|--------------------------------------------------|
| 31       | 30 | 29                                              | 28                                      | 27       | 26 | 25                                        | 24                                               |
| RESERVED |    |                                                 |                                         |          |    |                                           |                                                  |
| NONE     |    |                                                 |                                         |          |    |                                           |                                                  |
| 0h       |    |                                                 |                                         |          |    |                                           |                                                  |
| 23       | 22 | 21                                              | 20                                      | 19       | 18 | 17                                        | 16                                               |
| RESERVED |    |                                                 |                                         |          |    |                                           |                                                  |
| NONE     |    |                                                 |                                         |          |    |                                           |                                                  |
| 0h       |    |                                                 |                                         |          |    |                                           |                                                  |
| 15       | 14 | 13                                              | 12                                      | 11       | 10 | 9                                         | 8                                                |
| RESERVED |    |                                                 | PLL_CORE_HS<br>DIVIDER_CLK<br>OUT0_PWDN | RESERVED |    | PLL_CORE_HS<br>DIVIDER_CLK<br>OUT0_STATUS | PLL_CORE_HS<br>DIVIDER_CLK<br>OUT0_GATE_C<br>TRL |
| NONE     |    |                                                 | R/W                                     | NONE     |    | R                                         | R/W                                              |
| 0h       |    |                                                 | 0h                                      | 0h       |    | 0h                                        | 0h                                               |
| 7        | 6  | 5                                               | 4                                       | 3        | 2  | 1                                         | 0                                                |
| RESERVED |    | PLL_CORE_HS<br>DIVIDER_CLK<br>OUT0_DIVCHA<br>CK | PLL_CORE_HSDIVIDER_CLKOUT0_DIV          |          |    |                                           |                                                  |
| NONE     |    | R                                               | R/W                                     |          |    |                                           |                                                  |
| 0h       |    | 0h                                              | 4h                                      |          |    |                                           |                                                  |

**Table 2-2168. MSS\_TOPRCM\_PLL\_CORE\_HSDIVIDER\_CLKOUT0 Register Field Descriptions**

| Bit   | Field                                | Type | Reset | Description                                                                                                                                                                                 |
|-------|--------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:13 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                                                                                    |
| 12    | PLL_CORE_HSDIVIDER_CLKOUT0_PWDN      | R/W  | 0h    | Power down for HSDIVIDER CLKOUT0 divider and hence CLKOUT0 output<br>0h[R/W] = CLKOUT0 divider active<br>1h[R/W] = CLKOUT0 divider is powered down                                          |
| 11:10 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                                                                                    |
| 9     | PLL_CORE_HSDIVIDER_CLKOUT0_STATUS    | R    | 0h    | HSDIVIDER CLKOUT0 status<br>0h[R] = The clock output is gated<br>1h[R] = The clock output is enabled                                                                                        |
| 8     | PLL_CORE_HSDIVIDER_CLKOUT0_GATE_CTRL | R/W  | 0h    | Control gating of HSDIVIDER CLKOUT0<br>0h[R/W] = Automatically gate this clock when there is no dependency for it<br>1h[R/W] = Force this clock to stay enabled even if there is no request |
| 7:6   | RESERVED                             | NONE | 0h    | Reserved                                                                                                                                                                                    |
| 5     | PLL_CORE_HSDIVIDER_CLKOUT0_DIVCHACK  | R    | 0h    | Toggle on this status bit after changing HSDIVIDER_CLKOUT0_DIV indicates that the change in divider value has taken effect                                                                  |



**Table 2-2168. MSS\_TOPRCM\_PLL\_CORE\_HSDIVIDER\_CLKOUT0 Register Field Descriptions (continued)**

| Bit | Field                          | Type | Reset | Description                                                                                                                      |
|-----|--------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | PLL_CORE_HSDIVIDER_CLKOUT0_DIV | R/W  | 4h    | DPLL post-divider factor, HSDIVIDER CLKOUT0, for internal clock generation.<br>Divide values from 1 to 31.<br>0h[R/W] = Reserved |

### 2.5.2.25 MSS\_TOPRCM\_PLL\_CORE\_HSDIVIDER\_CLKOUT1 Register

#### 1 MSS\_TOPRCM\_PLL\_CORE\_HSDIVIDER\_CLKOUT1 Register (Offset = 430h) [reset = 3h]

Core PLL high speed divider clock 1 control.

Return to [Summary Table](#)

**Table 2-2169. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0430h       |

**Figure 2-722. MSS\_TOPRCM\_PLL\_CORE\_HSDIVIDER\_CLKOUT1 Name Register**

|          |    |                                                 |                                         |          |    |                                           |                                                  |
|----------|----|-------------------------------------------------|-----------------------------------------|----------|----|-------------------------------------------|--------------------------------------------------|
| 31       | 30 | 29                                              | 28                                      | 27       | 26 | 25                                        | 24                                               |
| RESERVED |    |                                                 |                                         |          |    |                                           |                                                  |
| NONE     |    |                                                 |                                         |          |    |                                           |                                                  |
| 0h       |    |                                                 |                                         |          |    |                                           |                                                  |
| 23       | 22 | 21                                              | 20                                      | 19       | 18 | 17                                        | 16                                               |
| RESERVED |    |                                                 |                                         |          |    |                                           |                                                  |
| NONE     |    |                                                 |                                         |          |    |                                           |                                                  |
| 0h       |    |                                                 |                                         |          |    |                                           |                                                  |
| 15       | 14 | 13                                              | 12                                      | 11       | 10 | 9                                         | 8                                                |
| RESERVED |    |                                                 | PLL_CORE_HS<br>DIVIDER_CLK<br>OUT1_PWDN | RESERVED |    | PLL_CORE_HS<br>DIVIDER_CLK<br>OUT1_STATUS | PLL_CORE_HS<br>DIVIDER_CLK<br>OUT1_GATE_C<br>TRL |
| NONE     |    |                                                 | R/W                                     | NONE     |    | R                                         | R/W                                              |
| 0h       |    |                                                 | 0h                                      | 0h       |    | 0h                                        | 0h                                               |
| 7        | 6  | 5                                               | 4                                       | 3        | 2  | 1                                         | 0                                                |
| RESERVED |    | PLL_CORE_HS<br>DIVIDER_CLK<br>OUT1_DIVCHA<br>CK | PLL_CORE_HSDIVIDER_CLKOUT1_DIV          |          |    |                                           |                                                  |
| NONE     |    | R                                               | R/W                                     |          |    |                                           |                                                  |
| 0h       |    | 0h                                              | 3h                                      |          |    |                                           |                                                  |

**Table 2-2171. MSS\_TOPRCM\_PLL\_CORE\_HSDIVIDER\_CLKOUT1 Register Field Descriptions**

| Bit   | Field                                | Type | Reset | Description                                                                                                                                                                                 |
|-------|--------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:13 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                                                                                    |
| 12    | PLL_CORE_HSDIVIDER_CLKOUT1_PWDN      | R/W  | 0h    | Power down for HSDIVIDER CLKOUT1 divider and hence CLKOUT1 output<br>0h[R/W] = CLKOUT1 divider active<br>1h[R/W] = CLKOUT1 divider is powered down                                          |
| 11:10 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                                                                                    |
| 9     | PLL_CORE_HSDIVIDER_CLKOUT1_STATUS    | R    | 0h    | HSDIVIDER CLKOUT1 status<br>0h[R] = The clock output is gated<br>1h[R] = The clock output is enabled                                                                                        |
| 8     | PLL_CORE_HSDIVIDER_CLKOUT1_GATE_CTRL | R/W  | 0h    | Control gating of HSDIVIDER CLKOUT1<br>0h[R/W] = Automatically gate this clock when there is no dependency for it<br>1h[R/W] = Force this clock to stay enabled even if there is no request |
| 7:6   | RESERVED                             | NONE | 0h    | Reserved                                                                                                                                                                                    |
| 5     | PLL_CORE_HSDIVIDER_CLKOUT1_DIVCHACK  | R    | 0h    | Toggle on this status bit after changing HSDIVIDER_CLKOUT1_DIV indicates that the change in divider value has taken effect                                                                  |

**Table 2-2171. MSS\_TOPRCM\_PLL\_CORE\_HSDIVIDER\_CLKOUT1 Register Field Descriptions (continued)**

| Bit | Field                          | Type | Reset | Description                                                                                                                      |
|-----|--------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | PLL_CORE_HSDIVIDER_CLKOUT1_DIV | R/W  | 3h    | DPLL post-divider factor, HSDIVIDER CLKOUT1, for internal clock generation.<br>Divide values from 1 to 31.<br>0h[R/W] = Reserved |

### 2.5.2.26 MSS\_TOPRCM\_PLL\_CORE\_HSDIVIDER\_CLKOUT2 Register

#### 1 MSS\_TOPRCM\_PLL\_CORE\_HSDIVIDER\_CLKOUT2 Register (Offset = 434h) [reset = 4h]

Core PLL high speed divider clock 2 control.

Return to [Summary Table](#)

**Table 2-2172. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0434h       |

**Figure 2-723. MSS\_TOPRCM\_PLL\_CORE\_HSDIVIDER\_CLKOUT2 Name Register**

|          |    |                                                 |                                         |          |    |                                           |                                                  |
|----------|----|-------------------------------------------------|-----------------------------------------|----------|----|-------------------------------------------|--------------------------------------------------|
| 31       | 30 | 29                                              | 28                                      | 27       | 26 | 25                                        | 24                                               |
| RESERVED |    |                                                 |                                         |          |    |                                           |                                                  |
| NONE     |    |                                                 |                                         |          |    |                                           |                                                  |
| 0h       |    |                                                 |                                         |          |    |                                           |                                                  |
| 23       | 22 | 21                                              | 20                                      | 19       | 18 | 17                                        | 16                                               |
| RESERVED |    |                                                 |                                         |          |    |                                           |                                                  |
| NONE     |    |                                                 |                                         |          |    |                                           |                                                  |
| 0h       |    |                                                 |                                         |          |    |                                           |                                                  |
| 15       | 14 | 13                                              | 12                                      | 11       | 10 | 9                                         | 8                                                |
| RESERVED |    |                                                 | PLL_CORE_HS<br>DIVIDER_CLK<br>OUT2_PWDN | RESERVED |    | PLL_CORE_HS<br>DIVIDER_CLK<br>OUT2_STATUS | PLL_CORE_HS<br>DIVIDER_CLK<br>OUT2_GATE_C<br>TRL |
| NONE     |    |                                                 | R/W                                     | NONE     |    | R                                         | R/W                                              |
| 0h       |    |                                                 | 0h                                      | 0h       |    | 0h                                        | 0h                                               |
| 7        | 6  | 5                                               | 4                                       | 3        | 2  | 1                                         | 0                                                |
| RESERVED |    | PLL_CORE_HS<br>DIVIDER_CLK<br>OUT2_DIVCHA<br>CK | PLL_CORE_HSDIVIDER_CLKOUT2_DIV          |          |    |                                           |                                                  |
| NONE     |    | R                                               | R/W                                     |          |    |                                           |                                                  |
| 0h       |    | 0h                                              | 4h                                      |          |    |                                           |                                                  |

**Table 2-2174. MSS\_TOPRCM\_PLL\_CORE\_HSDIVIDER\_CLKOUT2 Register Field Descriptions**

| Bit   | Field                                | Type | Reset | Description                                                                                                                                                                                 |
|-------|--------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:13 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                                                                                    |
| 12    | PLL_CORE_HSDIVIDER_CLKOUT2_PWDN      | R/W  | 0h    | Power down for HSDIVIDER CLKOUT2 divider and hence CLKOUT2 output<br>0h[R/W] = CLKOUT2 divider active<br>1h[R/W] = CLKOUT2 divider is powered down                                          |
| 11:10 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                                                                                    |
| 9     | PLL_CORE_HSDIVIDER_CLKOUT2_STATUS    | R    | 0h    | HSDIVIDER CLKOUT2 status<br>0h[R] = The clock output is gated<br>1h[R] = The clock output is enabled                                                                                        |
| 8     | PLL_CORE_HSDIVIDER_CLKOUT2_GATE_CTRL | R/W  | 0h    | Control gating of HSDIVIDER CLKOUT2<br>0h[R/W] = Automatically gate this clock when there is no dependency for it<br>1h[R/W] = Force this clock to stay enabled even if there is no request |
| 7:6   | RESERVED                             | NONE | 0h    | Reserved                                                                                                                                                                                    |
| 5     | PLL_CORE_HSDIVIDER_CLKOUT2_DIVCHACK  | R    | 0h    | Toggle on this status bit after changing HSDIVIDER_CLKOUT2_DIV indicates that the change in divider value has taken effect                                                                  |

**Table 2-2174. MSS\_TOPRCM\_PLL\_CORE\_HSDIVIDER\_CLKOUT2 Register Field Descriptions (continued)**

| Bit | Field                          | Type | Reset | Description                                                                                                                      |
|-----|--------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | PLL_CORE_HSDIVIDER_CLKOUT2_DIV | R/W  | 4h    | DPLL post-divider factor, HSDIVIDER CLKOUT2, for internal clock generation.<br>Divide values from 1 to 31.<br>0h[R/W] = Reserved |

### 2.5.2.27 MSS\_TOPRCM\_PLL\_CORE\_RSTCTRL Register

#### 1 MSS\_TOPRCM\_PLL\_CORE\_RSTCTRL Register (Offset = 43Ch) [reset = 0h]

Core PLL reset control .

Return to [Summary Table](#)

**Table 2-2175. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 043Ch       |

**Figure 2-724. MSS\_TOPRCM\_PLL\_CORE\_RSTCTRL Name Register**

|          |    |    |    |    |                         |    |    |
|----------|----|----|----|----|-------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                      | 25 | 24 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                      | 17 | 16 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                      | 9  | 8  |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                       | 1  | 0  |
| RESERVED |    |    |    |    | PLL_CORE_RSTCTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                     |    |    |
| 0h       |    |    |    |    | 0h                      |    |    |

**Table 2-2177. MSS\_TOPRCM\_PLL\_CORE\_RSTCTRL Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                                                               |
|------|-------------------------|------|-------|-------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                                                                  |
| 2:0  | PLL_CORE_RSTCTRL_ASSERT | R/W  | 0h    | SW Reset override for the PLL<br>Write 3'b111 : Override is enabled and Reset is asserted |

### 2.5.2.28 MSS\_TOPRCM\_PLL\_CORE\_HSDIVIDER\_RSTCTRL Register

#### 1 MSS\_TOPRCM\_PLL\_CORE\_HSDIVIDER\_RSTCTRL Register (Offset = 440h) [reset = 0h]

Core PLL high speed divider reset control.

Return to [Summary Table](#)

**Table 2-2178. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0440h       |

**Figure 2-725. MSS\_TOPRCM\_PLL\_CORE\_HSDIVIDER\_RSTCTRL Name Register**

|          |    |    |    |    |                                   |    |    |
|----------|----|----|----|----|-----------------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                                | 25 | 24 |
| RESERVED |    |    |    |    |                                   |    |    |
| NONE     |    |    |    |    |                                   |    |    |
| 0h       |    |    |    |    |                                   |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                                | 17 | 16 |
| RESERVED |    |    |    |    |                                   |    |    |
| NONE     |    |    |    |    |                                   |    |    |
| 0h       |    |    |    |    |                                   |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                                | 9  | 8  |
| RESERVED |    |    |    |    |                                   |    |    |
| NONE     |    |    |    |    |                                   |    |    |
| 0h       |    |    |    |    |                                   |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                                 | 1  | 0  |
| RESERVED |    |    |    |    | PLL_CORE_HSDIVIDER_RSTCTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                               |    |    |
| 0h       |    |    |    |    | 0h                                |    |    |

**Table 2-2180. MSS\_TOPRCM\_PLL\_CORE\_HSDIVIDER\_RSTCTRL Register Field Descriptions**

| Bit  | Field                             | Type | Reset | Description                                                                                     |
|------|-----------------------------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                          | NONE | 0h    | Reserved                                                                                        |
| 2:0  | PLL_CORE_HSDIVIDER_RSTCTRL_ASSERT | R/W  | 0h    | SW Reset override for the HSDIVIDER<br>Write 3'b111 : Override is enabled and Reset is asserted |

### 2.5.2.29 MSS\_TOPRCM\_MSS\_R5SS\_CLK\_SRC\_SEL Register

#### 1 MSS\_TOPRCM\_MSS\_R5SS\_CLK\_SRC\_SEL Register (Offset = 500h) [reset = 0h]

Clock Source select register for MSS CortexR5 clock.

Return to [Summary Table](#)

**Table 2-2181. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0500h       |

**Figure 2-726. MSS\_TOPRCM\_MSS\_R5SS\_CLK\_SRC\_SEL Name Register**

|                               |    |    |    |                               |    |    |    |
|-------------------------------|----|----|----|-------------------------------|----|----|----|
| 31                            | 30 | 29 | 28 | 27                            | 26 | 25 | 24 |
| RESERVED                      |    |    |    |                               |    |    |    |
| NONE                          |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |
| 23                            | 22 | 21 | 20 | 19                            | 18 | 17 | 16 |
| RESERVED                      |    |    |    |                               |    |    |    |
| NONE                          |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |
| 15                            | 14 | 13 | 12 | 11                            | 10 | 9  | 8  |
| RESERVED                      |    |    |    | MSS_CR5_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                          |    |    |    | R/W                           |    |    |    |
| 0h                            |    |    |    | 0h                            |    |    |    |
| 7                             | 6  | 5  | 4  | 3                             | 2  | 1  | 0  |
| MSS_CR5_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                               |    |    |    |
| R/W                           |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |

**Table 2-2183. MSS\_TOPRCM\_MSS\_R5SS\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                         | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|-------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                      | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 11:0  | MSS_CR5_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for MSS Coretex R5 and System bus Clock.<br>Data should be loaded as multibit.<br>For example: if Clock source 0x5 should be selected then 0x555 should be configured to the register.<br>Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - EXT_REFCLK<br>0x222 - DPLL_CORE_HSDIV0_CLKOUT0<br>0x333 - RCCLK10M<br>0x444 - RCCLK10M<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - RCCLK10M |



### 2.5.2.30 MSS\_TOPRCM\_MSS\_ROOT\_R5SS\_CLK\_STATUS Register

#### 1 MSS\_TOPRCM\_MSS\_ROOT\_R5SS\_CLK\_STATUS Register (Offset = 504h) [reset = 1h]

Clock Status register for MSS Root clock for CortexR5 and SYS clock.

Return to [Summary Table](#)

**Table 2-2184. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0504h       |

**Figure 2-727. MSS\_TOPRCM\_MSS\_ROOT\_R5SS\_CLK\_STATUS Name Register**

|                                  |    |    |    |    |    |    |    |
|----------------------------------|----|----|----|----|----|----|----|
| 31                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                         |    |    |    |    |    |    |    |
| NONE                             |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 23                               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                         |    |    |    |    |    |    |    |
| NONE                             |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 15                               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED                         |    |    |    |    |    |    |    |
| NONE                             |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 7                                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_ROOT_CR5_CLK_STATUS_CLKINUSE |    |    |    |    |    |    |    |
| R                                |    |    |    |    |    |    |    |
| 1h                               |    |    |    |    |    |    |    |

**Table 2-2186. MSS\_TOPRCM\_MSS\_ROOT\_R5SS\_CLK\_STATUS Register Field Descriptions**

| Bit  | Field                            | Type | Reset | Description                                                                                          |
|------|----------------------------------|------|-------|------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED                         | NONE | 0h    | Reserved                                                                                             |
| 7:0  | MSS_ROOT_CR5_CLK_STATUS_CLKINUSE | R    | 1h    | Status shows the source clock selected for Root clock for CortexR5 and Sysclk using one hot encoding |

### 2.5.2.31 MSS\_TOPRCM\_MSS\_CR50\_CLK\_DIV\_SEL Register

#### 1 MSS\_TOPRCM\_MSS\_CR50\_CLK\_DIV\_SEL Register (Offset = 510h) [reset = 0h]

Clock Divider register for Respective R5SS clock .

Return to [Summary Table](#)

**Table 2-2187. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0510h       |

**Figure 2-728. MSS\_TOPRCM\_MSS\_CR50\_CLK\_DIV\_SEL Name Register**

|          |    |    |    |    |                                |    |    |
|----------|----|----|----|----|--------------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                             | 25 | 24 |
| RESERVED |    |    |    |    |                                |    |    |
| NONE     |    |    |    |    |                                |    |    |
| 0h       |    |    |    |    |                                |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                             | 17 | 16 |
| RESERVED |    |    |    |    |                                |    |    |
| NONE     |    |    |    |    |                                |    |    |
| 0h       |    |    |    |    |                                |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                             | 9  | 8  |
| RESERVED |    |    |    |    |                                |    |    |
| NONE     |    |    |    |    |                                |    |    |
| 0h       |    |    |    |    |                                |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                              | 1  | 0  |
| RESERVED |    |    |    |    | MSS_CR50_CLK_DIV_SEL_CLKSRCSEL |    |    |
| NONE     |    |    |    |    | R/W                            |    |    |
| 0h       |    |    |    |    | 0h                             |    |    |

**Table 2-2189. MSS\_TOPRCM\_MSS\_CR50\_CLK\_DIV\_SEL Register Field Descriptions**

| Bit  | Field                              | Type | Reset | Description                                                                             |
|------|------------------------------------|------|-------|-----------------------------------------------------------------------------------------|
| 31:3 | RESERVED                           | NONE | 0h    | Reserved                                                                                |
| 2:0  | MSS_CR50_CLK_DIV_SE<br>L_CLKSRCSEL | R/W  | 0h    | Writing 3'b000 Sets R5 clock = R5SS Root clock<br>Writing 3'b111 Sets R5 Clock = SYSCLK |

### 2.5.2.32 MSS\_TOPRCM\_MSS\_CR51\_CLK\_DIV\_SEL Register

#### 1 MSS\_TOPRCM\_MSS\_CR51\_CLK\_DIV\_SEL Register (Offset = 514h) [reset = 0h]

Clock Divider register for Respective R5SS clock .

Return to [Summary Table](#)

**Table 2-2190. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0514h       |

**Figure 2-729. MSS\_TOPRCM\_MSS\_CR51\_CLK\_DIV\_SEL Name Register**

|          |    |    |    |    |                                |    |    |
|----------|----|----|----|----|--------------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                             | 25 | 24 |
| RESERVED |    |    |    |    |                                |    |    |
| NONE     |    |    |    |    |                                |    |    |
| 0h       |    |    |    |    |                                |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                             | 17 | 16 |
| RESERVED |    |    |    |    |                                |    |    |
| NONE     |    |    |    |    |                                |    |    |
| 0h       |    |    |    |    |                                |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                             | 9  | 8  |
| RESERVED |    |    |    |    |                                |    |    |
| NONE     |    |    |    |    |                                |    |    |
| 0h       |    |    |    |    |                                |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                              | 1  | 0  |
| RESERVED |    |    |    |    | MSS_CR51_CLK_DIV_SEL_CLKSRCSEL |    |    |
| NONE     |    |    |    |    | R/W                            |    |    |
| 0h       |    |    |    |    | 0h                             |    |    |

**Table 2-2192. MSS\_TOPRCM\_MSS\_CR51\_CLK\_DIV\_SEL Register Field Descriptions**

| Bit  | Field                              | Type | Reset | Description                                                                             |
|------|------------------------------------|------|-------|-----------------------------------------------------------------------------------------|
| 31:3 | RESERVED                           | NONE | 0h    | Reserved                                                                                |
| 2:0  | MSS_CR51_CLK_DIV_SE<br>L_CLKSRCSEL | R/W  | 0h    | Writing 3'b000 Sets R5 clock = R5SS Root clock<br>Writing 3'b111 Sets R5 Clock = SYSCLK |

### 2.5.2.33 MSS\_TOPRCM\_MSS\_CR50\_CLK\_GATE Register

#### 1 MSS\_TOPRCM\_MSS\_CR50\_CLK\_GATE Register (Offset = 518h) [reset = 0h]

Clock Gating register for Respective R5SS clock.

Return to [Summary Table](#)

**Table 2-2193. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0518h       |

**Figure 2-730. MSS\_TOPRCM\_MSS\_CR50\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_CR50_CLK_GATE_GATED |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-2195. MSS\_TOPRCM\_MSS\_CR50\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                                                                                                                                                                                                     |
|------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                                                                        |
| 2:0  | MSS_CR50_CLK_GATE_GATED | R/W  | 0h    | Only for debug- Functionality not guaranteed<br>Clock gating config for MSS Coretex R5.<br>Data should be loaded as multibit.<br>Write 3'b000 : Clock is ungated [multibit 000]<br>Write 3'b111 : Clock is gated [multibit 111] |

### 2.5.2.34 MSS\_TOPRCM\_MSS\_CR51\_CLK\_GATE Register

#### 1 MSS\_TOPRCM\_MSS\_CR51\_CLK\_GATE Register (Offset = 51Ch) [reset = 0h]

Clock Gating register for Respective R5SS clock.

Return to [Summary Table](#)

**Table 2-2196. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 051Ch       |

**Figure 2-731. MSS\_TOPRCM\_MSS\_CR51\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_CR51_CLK_GATE_GATED |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-2198. MSS\_TOPRCM\_MSS\_CR51\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                                                                                                                                                                                                     |
|------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                                                                                        |
| 2:0  | MSS_CR51_CLK_GATE_GATED | R/W  | 0h    | Only for debug- Functionality not guaranteed<br>Clock gating config for MSS Coretex R5.<br>Data should be loaded as multibit.<br>Write 3'b000 : Clock is ungated [multibit 000]<br>Write 3'b111 : Clock is gated [multibit 111] |

### 2.5.2.35 MSS\_TOPRCM\_SYS\_CLK\_DIV\_VAL Register

#### 1 MSS\_TOPRCM\_SYS\_CLK\_DIV\_VAL Register (Offset = 520h) [reset = 0h]

Clock Divider register for System Clock.

Return to [Summary Table](#)

**Table 2-2199. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0520h       |

**Figure 2-732. MSS\_TOPRCM\_SYS\_CLK\_DIV\_VAL Name Register**

|                        |    |    |    |                        |    |    |    |
|------------------------|----|----|----|------------------------|----|----|----|
| 31                     | 30 | 29 | 28 | 27                     | 26 | 25 | 24 |
| RESERVED               |    |    |    |                        |    |    |    |
| NONE                   |    |    |    |                        |    |    |    |
| 0h                     |    |    |    |                        |    |    |    |
| 23                     | 22 | 21 | 20 | 19                     | 18 | 17 | 16 |
| RESERVED               |    |    |    |                        |    |    |    |
| NONE                   |    |    |    |                        |    |    |    |
| 0h                     |    |    |    |                        |    |    |    |
| 15                     | 14 | 13 | 12 | 11                     | 10 | 9  | 8  |
| RESERVED               |    |    |    | SYS_CLK_DIV_VAL_CLKDIV |    |    |    |
| NONE                   |    |    |    | R/W                    |    |    |    |
| 0h                     |    |    |    | 0h                     |    |    |    |
| 7                      | 6  | 5  | 4  | 3                      | 2  | 1  | 0  |
| SYS_CLK_DIV_VAL_CLKDIV |    |    |    |                        |    |    |    |
| R/W                    |    |    |    |                        |    |    |    |
| 0h                     |    |    |    |                        |    |    |    |

**Table 2-2201. MSS\_TOPRCM\_SYS\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                  | Type | Reset | Description                                                                                                                                                                                                                                                    |
|-------|------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED               | NONE | 0h    | Reserved                                                                                                                                                                                                                                                       |
| 11:0  | SYS_CLK_DIV_VAL_CLKDIV | R/W  | 0h    | Divider value for System Clock selected clock..To set the divider value of [n+1] configure the register to '0xnnn'.Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

### 2.5.2.36 MSS\_TOPRCM\_SYS\_CLK\_GATE Register

#### 1 MSS\_TOPRCM\_SYS\_CLK\_GATE Register (Offset = 524h) [reset = 0h]

Clock Gating register for System Clock.

Return to [Summary Table](#)

**Table 2-2202. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0524h       |

**Figure 2-733. MSS\_TOPRCM\_SYS\_CLK\_GATE Name Register**

|          |    |    |    |    |                    |    |    |
|----------|----|----|----|----|--------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                 | 25 | 24 |
| RESERVED |    |    |    |    |                    |    |    |
| NONE     |    |    |    |    |                    |    |    |
| 0h       |    |    |    |    |                    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                 | 17 | 16 |
| RESERVED |    |    |    |    |                    |    |    |
| NONE     |    |    |    |    |                    |    |    |
| 0h       |    |    |    |    |                    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                 | 9  | 8  |
| RESERVED |    |    |    |    |                    |    |    |
| NONE     |    |    |    |    |                    |    |    |
| 0h       |    |    |    |    |                    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                  | 1  | 0  |
| RESERVED |    |    |    |    | SYS_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                |    |    |
| 0h       |    |    |    |    | 0h                 |    |    |

**Table 2-2204. MSS\_TOPRCM\_SYS\_CLK\_GATE Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                                                                                                                  |
|------|--------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                     |
| 2:0  | SYS_CLK_GATE_GATED | R/W  | 0h    | Only for debug- Functionality not guaranteed<br>Clock gating config for System Clock<br>Data should be loaded as multibit.<br>Write 3'b000 : Clock is ungated [multibit 000]<br>Write 3'b111 : Clock is gated [multibit 111] |

### 2.5.2.37 MSS\_TOPRCM\_SYS\_CLK\_STATUS Register

#### 1 MSS\_TOPRCM\_SYS\_CLK\_STATUS Register (Offset = 528h) [reset = 0h]

Clock Status register for System Clock.

Return to [Summary Table](#)

**Table 2-2205. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0528h       |

**Figure 2-734. MSS\_TOPRCM\_SYS\_CLK\_STATUS Name Register**

|                            |    |    |    |    |    |    |    |
|----------------------------|----|----|----|----|----|----|----|
| 31                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                   |    |    |    |    |    |    |    |
| NONE                       |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |
| 23                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                   |    |    |    |    |    |    |    |
| NONE                       |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |
| 15                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SYS_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                          |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |
| 7                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED                   |    |    |    |    |    |    |    |
| NONE                       |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |

**Table 2-2207. MSS\_TOPRCM\_SYS\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                      | Type | Reset | Description                                                 |
|-------|----------------------------|------|-------|-------------------------------------------------------------|
| 31:16 | RESERVED                   | NONE | 0h    | Reserved                                                    |
| 15:8  | SYS_CLK_STATUS_CURRDIVIDER | R    | 0h    | Status shows the current divider value chosen for Sys Clock |
| 7:0   | RESERVED                   | NONE | 0h    | Reserved                                                    |



### 2.5.2.38 MSS\_TOPRCM\_PLL\_PER\_PWRCTRL Register

#### 1 MSS\_TOPRCM\_PLL\_PER\_PWRCTRL Register (Offset = 800h) [reset = 30h]

Power control for peripheral PLL.

Return to [Summary Table](#)

**Table 2-2208. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0800h       |

**Figure 2-735. MSS\_TOPRCM\_PLL\_PER\_PWRCTRL Name Register**

|          |                       |                         |                     |                        |                         |                         |     |
|----------|-----------------------|-------------------------|---------------------|------------------------|-------------------------|-------------------------|-----|
| 31       | 30                    | 29                      | 28                  | 27                     | 26                      | 25                      | 24  |
| RESERVED |                       |                         |                     |                        |                         |                         |     |
| NONE     |                       |                         |                     |                        |                         |                         |     |
| 0h       |                       |                         |                     |                        |                         |                         |     |
| 23       | 22                    | 21                      | 20                  | 19                     | 18                      | 17                      | 16  |
| RESERVED |                       |                         |                     |                        |                         |                         |     |
| NONE     |                       |                         |                     |                        |                         |                         |     |
| 0h       |                       |                         |                     |                        |                         |                         |     |
| 15       | 14                    | 13                      | 12                  | 11                     | 10                      | 9                       | 8   |
| RESERVED |                       |                         |                     |                        |                         |                         |     |
| NONE     |                       |                         |                     |                        |                         |                         |     |
| 0h       |                       |                         |                     |                        |                         |                         |     |
| 7        | 6                     | 5                       | 4                   | 3                      | 2                       | 1                       | 0   |
| RESERVED | PLL_PER_PWRCTRL_PONIN | PLL_PER_PWRCTRL_PGOODIN | PLL_PER_PWRCTRL_RET | PLL_PER_PWRCTRL_ISORET | PLL_PER_PWRCTRL_ISOSCAN | PLL_PER_PWRCTRL_OFFMODE |     |
| NONE     | R/W                   | R/W                     | R/W                 | R/W                    | R/W                     | R/W                     | R/W |
| 0h       | 1h                    | 1h                      | 0h                  | 0h                     | 0h                      | 0h                      | 0h  |

**Table 2-2210. MSS\_TOPRCM\_PLL\_PER\_PWRCTRL Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                                                                   |
|------|-------------------------|------|-------|-----------------------------------------------------------------------------------------------|
| 31:6 | RESERVED                | NONE | 0h    | Reserved                                                                                      |
| 5    | PLL_PER_PWRCTRL_PONIN   | R/W  | 1h    | ON/OFF control of the weak power switch digital. For functional mode it should be 1           |
| 4    | PLL_PER_PWRCTRL_PGOODIN | R/W  | 1h    | ON/OFF control of the strong power switch digital. For functional mode it should be 1         |
| 3    | PLL_PER_PWRCTRL_RET     | R/W  | 0h    | Save/Restore control for Retention mode. For functional mode it should be 0                   |
| 2    | PLL_PER_PWRCTRL_ISORET  | R/W  | 0h    | Save/Restore control for Isolation of output pins For functional mode it should be 1'b0       |
| 1    | PLL_PER_PWRCTRL_ISOSCAN | R/W  | 0h    | Save/Restore control for Isolation of the Scanout pins. For functional mode it should be 1'b0 |
| 0    | PLL_PER_PWRCTRL_OFFMODE | R/W  | 0h    | Used to switch OFF the logic on VDDA. For functional mode it should be 0                      |

### 2.5.2.39 MSS\_TOPRCM\_PLL\_PER\_CLKCTRL Register

#### 1 MSS\_TOPRCM\_PLL\_PER\_CLKCTRL Register (Offset = 804h) [reset = 895000h]

Clock control for Peripheral PLL.

Return to [Summary Table](#)

**Table 2-2211. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0804h       |

**Figure 2-736. MSS\_TOPRCM\_PLL\_PER\_CLKCTRL Name Register**

| 31                                  | 30                                 | 29                                  | 28                               | 27                                  | 26                                | 25                                     | 24                                   |
|-------------------------------------|------------------------------------|-------------------------------------|----------------------------------|-------------------------------------|-----------------------------------|----------------------------------------|--------------------------------------|
| PLL_PER_CLK<br>CTRL_CYCLES<br>LIPEN | PLL_PER_CLK<br>CTRL_ENSSC          | PLL_PER_CLK<br>CTRL_CLKDC<br>OLDOEN | RESERVED                         |                                     |                                   |                                        |                                      |
| R/W                                 | R/W                                | R/W                                 | NONE                             |                                     |                                   |                                        |                                      |
| 0h                                  | 0h                                 | 0h                                  | 0h                               |                                     |                                   |                                        |                                      |
| 23                                  | 22                                 | 21                                  | 20                               | 19                                  | 18                                | 17                                     | 16                                   |
| PLL_PER_CLK<br>CTRL_IDLE            | PLL_PER_CLK<br>CTRL_BYPASS<br>ACKZ | PLL_PER_CLK<br>CTRL_STBYRE<br>T     | PLL_PER_CLK<br>CTRL_CLKOUT<br>EN | PLL_PER_CLK<br>CTRL_CLKOUT<br>LDOEN | PLL_PER_CLK<br>CTRL_ULOWC<br>LKEN | PLL_PER_CLK<br>CTRL_CLKDC<br>OLDOPWDNZ | PLL_PER_CLK<br>CTRL_M2PWD<br>NZ      |
| R/W                                 | R/W                                | R/W                                 | R/W                              | R/W                                 | R/W                               | R/W                                    | R/W                                  |
| 1h                                  | 0h                                 | 0h                                  | 0h                               | 1h                                  | 0h                                | 0h                                     | 1h                                   |
| 15                                  | 14                                 | 13                                  | 12                               | 11                                  | 10                                | 9                                      | 8                                    |
| RESERVED                            | PLL_PER_CLK<br>CTRL_STOPM<br>ODE   | RESERVED                            | PLL_PER_CLKCTRL_SELFREQDCO       |                                     |                                   | RESERVED                               | PLL_PER_CLK<br>CTRL_RELAXE<br>D_LOCK |
| NONE                                | R/W                                | NONE                                | R/W                              |                                     |                                   | NONE                                   | R/W                                  |
| 0h                                  | 1h                                 | 0h                                  | 4h                               |                                     |                                   | 0h                                     | 0h                                   |
| 7                                   | 6                                  | 5                                   | 4                                | 3                                   | 2                                 | 1                                      | 0                                    |
| RESERVED                            |                                    |                                     |                                  |                                     |                                   | PLL_PER_CLK<br>CTRL_SSCTYP<br>E        | PLL_PER_CLK<br>CTRL_TINTZ            |
| NONE                                |                                    |                                     |                                  |                                     |                                   | R/W                                    | R/W                                  |
| 0h                                  |                                    |                                     |                                  |                                     |                                   | 0h                                     | 0h                                   |

**Table 2-2213. MSS\_TOPRCM\_PLL\_PER\_CLKCTRL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                                                                                                                                                       |
|-------|------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | PLL_PER_CLKCTRL_CYCLES_LIPEN | R/W  | 0h    | FailSafe enable to trigger re-calibration in case CycleSlip occurs between REFCLK and FBCLK. Cycleslip could be caused if loop is not able to track input clock. Default = 1'b0 recommended       |
| 30    | PLL_PER_CLKCTRL_ENSSC        | R/W  | 0h    | Controls Clock SpReading. SSC is not supported. Should be set to 0x0 to disable clock spReading.                                                                                                  |
| 29    | PLL_PER_CLKCTRL_CLKDCOLD_OEN | R/W  | 0h    | Synchronously enables/disables CLKDCOLD_OEN<br>0x0 : synchronously disables CLKDCOLD_OEN<br>0x1 : synchronously enables CLKDCOLD_OEN                                                              |
| 28:24 | RESERVED                     | NONE | 0h    | Reserved                                                                                                                                                                                          |
| 23    | PLL_PER_CLKCTRL_IDLE         | R/W  | 1h    | Sets PLL to Idle mode<br>0x0 : When SYSRESET = 0 and TINITZ = 1 IDLE = 0 PLL will go to Active and Locked<br>0x1 : When SYSRESET = 0 and TINITZ = 1 IDLE = 1 PLL will go to Idle Bypass low power |

**Table 2-2213. MSS\_TOPRCM\_PLL\_PER\_CLKCTRL Register Field Descriptions (continued)**

| Bit   | Field                          | Type | Reset | Description                                                                                                                                                                                                                                                                          |
|-------|--------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 22    | PLL_PER_CLKCTRL_BYPASSACKZ     | R/W  | 0h    | BYPASSACKZ is a special purpose input to the module. In general this input is expected to be tied to static low. For the output clocks of the module that do not have an internal bypass mux viz. CLKDCOLDO and CLKOUTLDO, a bypass mux could be implemented external to the module. |
| 21    | PLL_PER_CLKCTRL_STBYRET        | R/W  | 0h    | Standby retention control<br>0x0 : prepares ADPLLLJ for relock when out of retention by removing the gating on all internal clocks.<br>0x1 : prepares ADPLLLJ for retention by gating all the internal clocks.                                                                       |
| 20    | PLL_PER_CLKCTRL_CLKOUTEN       | R/W  | 0h    | CLKOUT enable or disable<br>0x0 : synchronously disables CLKOUT<br>0x1 : synchronously enables CLKOUT                                                                                                                                                                                |
| 19    | PLL_PER_CLKCTRL_CLKOUTLDOEN    | R/W  | 1h    | Synchronously enables/disables CLKOUTLDO<br>0x0 : synchronously disables CLKOUTLDO<br>0x1 : synchronously enables CLKOUTLDO                                                                                                                                                          |
| 18    | PLL_PER_CLKCTRL_ULOWCLKEN      | R/W  | 0h    | Select CLKOUT source in bypass<br>0x0: When ADPLLLJ in bypass mode, CLKOUT = CLKINP/[N2+1]<br>0x1: When ADPLLLJ in bypass mode, CLKOUT = CLKINPULOW.                                                                                                                                 |
| 17    | PLL_PER_CLKCTRL_CLKDCOLDOPWDNZ | R/W  | 0h    | 0 Asynchronous power down for CLKDCOLDO o/p.                                                                                                                                                                                                                                         |
| 16    | PLL_PER_CLKCTRL_M2PWDNZ        | R/W  | 1h    | M2 divider power down mode<br>0x0: Asynchronous power down for M2 divider<br>0x1 : M2 divider is functional                                                                                                                                                                          |
| 15    | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                             |
| 14    | PLL_PER_CLKCTRL_STOPMODE       | R/W  | 1h    | When in Lossclk/Stbyret 0x0 : Limp mode 0x1 : Stopmode                                                                                                                                                                                                                               |
| 13    | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                             |
| 12:10 | PLL_PER_CLKCTRL_SELFREQDCO     | R/W  | 4h    | DCO Clock [DCOCLK = CLKINP * [M/[N+1]]] frequency range selector.<br>0x0: Reserved<br>0x2: HS2 : DCOCLK range is from 500 MHz to 1000MHz<br>0x3: Reserved<br>0x4: HS1: DCOCLK range is from 1000MHz to 2000MHz<br>0x5: Reserved                                                      |
| 9     | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                             |
| 8     | PLL_PER_CLKCTRL_RELAXED_LOCK   | R/W  | 0h    | Decides when FREQLOCK asserted<br>0x0: FREQLOCK asserted when DC frequency error less than 1%<br>0x1: FREQLOCK asserted when DC frequency error less than 2%                                                                                                                         |
| 7:2   | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                             |
| 1     | PLL_PER_CLKCTRL_SSCCTYPE       | R/W  | 0h    | SSC Type - This should be configured as 1'b0. The module does not support spread spectrum clocking [SSC] on its output clocks.                                                                                                                                                       |
| 0     | PLL_PER_CLKCTRL_TINTZ          | R/W  | 0h    | PLL core soft reset. TINITZ activation [Low] gives softreset to ADPLLLJ. TINITZ does not reset the entire digital control logic; it forces the FSM into RESET State so that ADPLLLJ could restart.                                                                                   |

### 2.5.2.40 MSS\_TOPRCM\_PLL\_PER\_TENABLE Register

#### 1 MSS\_TOPRCM\_PLL\_PER\_TENABLE Register (Offset = 808h) [reset = 0h]

Trigger enable for Peripheral PLL.

Return to [Summary Table](#)

**Table 2-2214. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0808h       |

**Figure 2-737. MSS\_TOPRCM\_PLL\_PER\_TENABLE Name Register**

|          |    |    |    |    |    |    |                         |
|----------|----|----|----|----|----|----|-------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                      |
| RESERVED |    |    |    |    |    |    |                         |
| NONE     |    |    |    |    |    |    |                         |
| 0h       |    |    |    |    |    |    |                         |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                      |
| RESERVED |    |    |    |    |    |    |                         |
| NONE     |    |    |    |    |    |    |                         |
| 0h       |    |    |    |    |    |    |                         |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                       |
| RESERVED |    |    |    |    |    |    |                         |
| NONE     |    |    |    |    |    |    |                         |
| 0h       |    |    |    |    |    |    |                         |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                       |
| RESERVED |    |    |    |    |    |    | PLL_PER_TENABLE_TENABLE |
| NONE     |    |    |    |    |    |    | R/W                     |
| 0h       |    |    |    |    |    |    | 0h                      |

**Table 2-2216. MSS\_TOPRCM\_PLL\_PER\_TENABLE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                                                                                  |
|------|-------------------------|------|-------|--------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED                | NONE | 0h    | Reserved                                                                                                     |
| 0    | PLL_PER_TENABLE_TENABLE | R/W  | 0h    | Signal TENABLE loads REGM, REGN, REGSD and SELFREQDCO data. M, N, SD and SELFREQDCO latch [active rise edge] |

### 2.5.2.41 MSS\_TOPRCM\_PLL\_PER\_TENABLEDIV Register

#### 1 MSS\_TOPRCM\_PLL\_PER\_TENABLEDIV Register (Offset = 80Ch) [reset = 0h]

Load Trigger for divider control value for peripheral PLL.

Return to [Summary Table](#)

**Table 2-2217. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 080Ch       |

**Figure 2-738. MSS\_TOPRCM\_PLL\_PER\_TENABLEDIV Name Register**

|          |    |    |    |    |    |    |                                       |
|----------|----|----|----|----|----|----|---------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                                    |
| RESERVED |    |    |    |    |    |    |                                       |
| NONE     |    |    |    |    |    |    |                                       |
| 0h       |    |    |    |    |    |    |                                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                                    |
| RESERVED |    |    |    |    |    |    |                                       |
| NONE     |    |    |    |    |    |    |                                       |
| 0h       |    |    |    |    |    |    |                                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                                     |
| RESERVED |    |    |    |    |    |    |                                       |
| NONE     |    |    |    |    |    |    |                                       |
| 0h       |    |    |    |    |    |    |                                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                                     |
| RESERVED |    |    |    |    |    |    | PLL_PER_TEN<br>ABLEDIV_TEN<br>ABLEDIV |
| NONE     |    |    |    |    |    |    | R/W                                   |
| 0h       |    |    |    |    |    |    | 0h                                    |

**Table 2-2219. MSS\_TOPRCM\_PLL\_PER\_TENABLEDIV Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                                                                                                                                                                                |
|------|-------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED                      | NONE | 0h    | Reserved                                                                                                                                                                                                   |
| 0    | PLL_PER_TENABLEDIV_TENABLEDIV | R/W  | 0h    | TENABLEDIV rising edge loads the values of M2REG and N2REG into ADPLLLJ register. TENABLEDIV could be activated anytime when the DPLL digital is in power-up condition. M2 and N2 latch [active rise edge] |

### 2.5.2.42 MSS\_TOPRCM\_PLL\_PER\_M2NDIV Register

#### 1 MSS\_TOPRCM\_PLL\_PER\_M2NDIV Register (Offset = 810h) [reset = 13h]

M2N config register for peripheral PLL.

Return to [Summary Table](#)

**Table 2-2220. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0810h       |

**Figure 2-739. MSS\_TOPRCM\_PLL\_PER\_M2NDIV Name Register**

|                  |                   |    |    |    |    |    |    |
|------------------|-------------------|----|----|----|----|----|----|
| 31               | 30                | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |                   |    |    |    |    |    |    |
| NONE             |                   |    |    |    |    |    |    |
| 0h               |                   |    |    |    |    |    |    |
| 23               | 22                | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED         | PLL_PER_M2NDIV_M2 |    |    |    |    |    |    |
| NONE             | R/W               |    |    |    |    |    |    |
| 0h               | 0h                |    |    |    |    |    |    |
| 15               | 14                | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED         |                   |    |    |    |    |    |    |
| NONE             |                   |    |    |    |    |    |    |
| 0h               |                   |    |    |    |    |    |    |
| 7                | 6                 | 5  | 4  | 3  | 2  | 1  | 0  |
| PLL_PER_M2NDIV_N |                   |    |    |    |    |    |    |
| R/W              |                   |    |    |    |    |    |    |
| 13h              |                   |    |    |    |    |    |    |

**Table 2-2222. MSS\_TOPRCM\_PLL\_PER\_M2NDIV Register Field Descriptions**

| Bit   | Field             | Type | Reset | Description           |
|-------|-------------------|------|-------|-----------------------|
| 31:23 | RESERVED          | NONE | 0h    | Reserved              |
| 22:16 | PLL_PER_M2NDIV_M2 | R/W  | 0h    | Post-divider is REGM2 |
| 15:8  | RESERVED          | NONE | 0h    | Reserved              |
| 7:0   | PLL_PER_M2NDIV_N  | R/W  | 13h   | Pre-divider is REGN+1 |

### 2.5.2.43 MSS\_TOPRCM\_PLL\_PER\_MN2DIV Register

#### 1 MSS\_TOPRCM\_PLL\_PER\_MN2DIV Register (Offset = 814h) [reset = 600h]

MN2 config register for peripheral PLL.

Return to [Summary Table](#)

**Table 2-2223. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0814h       |

**Figure 2-740. MSS\_TOPRCM\_PLL\_PER\_MN2DIV Name Register**

|                  |    |    |    |                   |    |    |    |
|------------------|----|----|----|-------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27                | 26 | 25 | 24 |
| RESERVED         |    |    |    |                   |    |    |    |
| NONE             |    |    |    |                   |    |    |    |
| 0h               |    |    |    |                   |    |    |    |
| 23               | 22 | 21 | 20 | 19                | 18 | 17 | 16 |
| RESERVED         |    |    |    | PLL_PER_MN2DIV_N2 |    |    |    |
| NONE             |    |    |    | R/W               |    |    |    |
| 0h               |    |    |    | 0h                |    |    |    |
| 15               | 14 | 13 | 12 | 11                | 10 | 9  | 8  |
| RESERVED         |    |    |    | PLL_PER_MN2DIV_M  |    |    |    |
| NONE             |    |    |    | R/W               |    |    |    |
| 0h               |    |    |    | 600h              |    |    |    |
| 7                | 6  | 5  | 4  | 3                 | 2  | 1  | 0  |
| PLL_PER_MN2DIV_M |    |    |    |                   |    |    |    |
| R/W              |    |    |    |                   |    |    |    |
| 600h             |    |    |    |                   |    |    |    |

**Table 2-2225. MSS\_TOPRCM\_PLL\_PER\_MN2DIV Register Field Descriptions**

| Bit   | Field             | Type | Reset | Description                 |
|-------|-------------------|------|-------|-----------------------------|
| 31:20 | RESERVED          | NONE | 0h    | Reserved                    |
| 19:16 | PLL_PER_MN2DIV_N2 | R/W  | 0h    | Bypass divider is REGN2+1   |
| 15:12 | RESERVED          | NONE | 0h    | Reserved                    |
| 11:0  | PLL_PER_MN2DIV_M  | R/W  | 600h  | Feedback Multiplier is REGM |

### 2.5.2.44 MSS\_TOPRCM\_PLL\_PER\_FRACDIV Register

#### 1 MSS\_TOPRCM\_PLL\_PER\_FRACDIV Register (Offset = 818h) [reset = 8000000h]

Fractional divider and Sigma Delta config register for peripheral PLL.

Return to [Summary Table](#)

**Table 2-2226. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0818h       |

**Figure 2-741. MSS\_TOPRCM\_PLL\_PER\_FRACDIV Name Register**

|                             |    |    |    |    |    |                             |    |
|-----------------------------|----|----|----|----|----|-----------------------------|----|
| 31                          | 30 | 29 | 28 | 27 | 26 | 25                          | 24 |
| PLL_PER_FRACDIV_REGSD       |    |    |    |    |    |                             |    |
| R/W                         |    |    |    |    |    |                             |    |
| 8h                          |    |    |    |    |    |                             |    |
| 23                          | 22 | 21 | 20 | 19 | 18 | 17                          | 16 |
| RESERVED                    |    |    |    |    |    | PLL_PER_FRACDIV_FRACTIONALM |    |
| NONE                        |    |    |    |    |    | R/W                         |    |
| 0h                          |    |    |    |    |    | 0h                          |    |
| 15                          | 14 | 13 | 12 | 11 | 10 | 9                           | 8  |
| PLL_PER_FRACDIV_FRACTIONALM |    |    |    |    |    |                             |    |
| R/W                         |    |    |    |    |    |                             |    |
| 0h                          |    |    |    |    |    |                             |    |
| 7                           | 6  | 5  | 4  | 3  | 2  | 1                           | 0  |
| PLL_PER_FRACDIV_FRACTIONALM |    |    |    |    |    |                             |    |
| R/W                         |    |    |    |    |    |                             |    |
| 0h                          |    |    |    |    |    |                             |    |

**Table 2-2228. MSS\_TOPRCM\_PLL\_PER\_FRACDIV Register Field Descriptions**

| Bit   | Field                       | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|-----------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | PLL_PER_FRACDIV_REGSD       | R/W  | 8h    | Sigma-Delta Divider<br>Should be set by s/w to provide optimum jitter performance.<br>$DPLL\_SD\_DIV = \text{CEILING} \left[ \frac{DPLL\_MULT}{DPLL\_DIV+1} \right] * CLKINP / 250$ , where CLKINP is the input clock of the DPLL in MHz |
| 23:18 | RESERVED                    | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 17:0  | PLL_PER_FRACDIV_FRACTIONALM | R/W  | 0h    | Fractional part of the M divider. The 18bit FractionalM value is loaded into DPLL on the rising edge of TENABLE signal. To enable Integer only division FractionalM should be set to 18'b0.                                              |



### 2.5.2.45 MSS\_TOPRCM\_PLL\_PER\_BWCTRL Register

#### 1 MSS\_TOPRCM\_PLL\_PER\_BWCTRL Register (Offset = 81Ch) [reset = 0h]

Loop bandwidth control for peripheral PLL.

Return to [Summary Table](#)

**Table 2-2229. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 081Ch       |

**Figure 2-742. MSS\_TOPRCM\_PLL\_PER\_BWCTRL Name Register**

|          |    |    |    |    |                              |                                      |    |
|----------|----|----|----|----|------------------------------|--------------------------------------|----|
| 31       | 30 | 29 | 28 | 27 | 26                           | 25                                   | 24 |
| RESERVED |    |    |    |    |                              |                                      |    |
| NONE     |    |    |    |    |                              |                                      |    |
| 0h       |    |    |    |    |                              |                                      |    |
| 23       | 22 | 21 | 20 | 19 | 18                           | 17                                   | 16 |
| RESERVED |    |    |    |    |                              |                                      |    |
| NONE     |    |    |    |    |                              |                                      |    |
| 0h       |    |    |    |    |                              |                                      |    |
| 15       | 14 | 13 | 12 | 11 | 10                           | 9                                    | 8  |
| RESERVED |    |    |    |    |                              |                                      |    |
| NONE     |    |    |    |    |                              |                                      |    |
| 0h       |    |    |    |    |                              |                                      |    |
| 7        | 6  | 5  | 4  | 3  | 2                            | 1                                    | 0  |
| RESERVED |    |    |    |    | PLL_PER_BWCTRL_BWCONTR<br>OL | PLL_PER_BW<br>CTRL_BW_INC<br>R_DECRZ |    |
| NONE     |    |    |    |    | R/W                          | R/W                                  |    |
| 0h       |    |    |    |    | 0h                           | 0h                                   |    |

**Table 2-2231. MSS\_TOPRCM\_PLL\_PER\_BWCTRL Register Field Descriptions**

| Bit  | Field                            | Type | Reset | Description                                                           |
|------|----------------------------------|------|-------|-----------------------------------------------------------------------|
| 31:3 | RESERVED                         | NONE | 0h    | Reserved                                                              |
| 2:1  | PLL_PER_BWCTRL_BW<br>CONTROL     | R/W  | 0h    | Change Loop Bandwidth                                                 |
| 0    | PLL_PER_BWCTRL_BW_<br>INCR_DECRZ | R/W  | 0h    | Direction of Loop Bandwidth<br>0x0 : decrease BW<br>0x1 : increase BW |

## 2.5.2.46 MSS\_TOPRCM\_PLL\_PER\_FRACCTRL Register

### 1 MSS\_TOPRCM\_PLL\_PER\_FRACCTRL Register (Offset = 820h) [reset = 0h]

Spread Spectrum control for peripheral PLL - Not Supported.

Return to [Summary Table](#)

**Table 2-2232. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0820h       |

**Figure 2-743. MSS\_TOPRCM\_PLL\_PER\_FRACCTRL Name Register**

| 31                                          | 30                                          | 29 | 28                                      | 27                                          | 26 | 25                                      | 24 |
|---------------------------------------------|---------------------------------------------|----|-----------------------------------------|---------------------------------------------|----|-----------------------------------------|----|
| PLL_PER_FRA<br>CTRL_DOWN<br>SPREAD          | PLL_PER_FRACCTRL_MODFREQDIVIDEREXPO<br>NENT |    |                                         | PLL_PER_FRACCTRL_MODFREQDIVIDERMAN<br>TISSA |    |                                         |    |
| R/W                                         | R/W                                         |    |                                         | R/W                                         |    |                                         |    |
| 0h                                          | 0h                                          |    |                                         | 0h                                          |    |                                         |    |
| 23                                          | 22                                          | 21 | 20                                      | 19                                          | 18 | 17                                      | 16 |
| PLL_PER_FRACCTRL_MODFREQDIVIDERMAN<br>TISSA |                                             |    | PLL_PER_FRACCTRL_DELTAMSTEPINTE<br>GGER |                                             |    | PLL_PER_FRACCTRL_DELTAM<br>STEPFRACTION |    |
| R/W                                         |                                             |    | R/W                                     |                                             |    | R/W                                     |    |
| 0h                                          |                                             |    | 0h                                      |                                             |    | 0h                                      |    |
| 15                                          | 14                                          | 13 | 12                                      | 11                                          | 10 | 9                                       | 8  |
| PLL_PER_FRACCTRL_DELTAMSTEPFRACTION         |                                             |    |                                         |                                             |    |                                         |    |
| R/W                                         |                                             |    |                                         |                                             |    |                                         |    |
| 0h                                          |                                             |    |                                         |                                             |    |                                         |    |
| 7                                           | 6                                           | 5  | 4                                       | 3                                           | 2  | 1                                       | 0  |
| PLL_PER_FRACCTRL_DELTAMSTEPFRACTION         |                                             |    |                                         |                                             |    |                                         |    |
| R/W                                         |                                             |    |                                         |                                             |    |                                         |    |
| 0h                                          |                                             |    |                                         |                                             |    |                                         |    |

**Table 2-2234. MSS\_TOPRCM\_PLL\_PER\_FRACCTRL Register Field Descriptions**

| Bit   | Field                                           | Type | Reset | Description                                                                                                                                         |
|-------|-------------------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | PLL_PER_FRACCTRL_D<br>OWNSPREAD                 | R/W  | 0h    | Controls frequency spread<br>0x0 : enables both side frequency spread about the programmed<br>frequency.<br>0x1 : enables low frequency spread only |
| 30:28 | PLL_PER_FRACCTRL_M<br>ODFREQDIVIDEREXPON<br>ENT | R/W  | 0h    | Exponent of the REFCLK divider to define the modulation frequency.                                                                                  |
| 27:21 | PLL_PER_FRACCTRL_M<br>ODFREQDIVIDERMAN<br>TISSA | R/W  | 0h    | Mantissa of the REFCLK divider to define the modulation frequency                                                                                   |
| 20:18 | PLL_PER_FRACCTRL_D<br>ELTAMSTEPINTE<br>GGER     | R/W  | 0h    | Integer part of Frequency Spread control                                                                                                            |
| 17:0  | PLL_PER_FRACCTRL_D<br>ELTAMSTEPFRACTION         | R/W  | 0h    | The fraction part of Frequency Spread control                                                                                                       |

### 2.5.2.47 MSS\_TOPRCM\_PLL\_PER\_STATUS Register

#### 1 MSS\_TOPRCM\_PLL\_PER\_STATUS Register (Offset = 824h) [reset = E0001141h]

Peripheral PLL status regiser.

Return to [Summary Table](#)

**Table 2-2235. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0824h       |

**Figure 2-744. MSS\_TOPRCM\_PLL\_PER\_STATUS Name Register**

| 31                                | 30                              | 29                                 | 28                                    | 27                                  | 26                               | 25                                | 24                               |
|-----------------------------------|---------------------------------|------------------------------------|---------------------------------------|-------------------------------------|----------------------------------|-----------------------------------|----------------------------------|
| PLL_PER_STA<br>TUS_PONOUT         | PLL_PER_STA<br>TUS_PGOODO<br>UT | PLL_PER_STA<br>TUS_LDOPWD<br>N     | PLL_PER_STA<br>TUS_RECAL_B<br>STATUS3 | PLL_PER_STA<br>TUS_RECAL_O<br>PPIN  | RESERVED                         |                                   |                                  |
| R                                 | R                               | R                                  | R                                     | R                                   | NONE                             |                                   |                                  |
| 1h                                | 1h                              | 1h                                 | 0h                                    | 0h                                  | 0h                               |                                   |                                  |
| 23                                | 22                              | 21                                 | 20                                    | 19                                  | 18                               | 17                                | 16                               |
| RESERVED                          |                                 |                                    |                                       |                                     |                                  |                                   |                                  |
| NONE                              |                                 |                                    |                                       |                                     |                                  |                                   |                                  |
| 0h                                |                                 |                                    |                                       |                                     |                                  |                                   |                                  |
| 15                                | 14                              | 13                                 | 12                                    | 11                                  | 10                               | 9                                 | 8                                |
| RESERVED                          |                                 |                                    | PLL_PER_STA<br>TUS_CLKOUTL<br>DOENACK | PLL_PER_STA<br>TUS_CLKDCO<br>LDOACK | PLL_PER_STA<br>TUS_PHASEL<br>OCK | PLL_PER_STA<br>TUS_FREQLO<br>CK   | PLL_PER_STA<br>TUS_BYPASSA<br>CK |
| NONE                              |                                 |                                    | R                                     | R                                   | R                                | R                                 | R                                |
| 0h                                |                                 |                                    | 1h                                    | 0h                                  | 0h                               | 0h                                | 1h                               |
| 7                                 | 6                               | 5                                  | 4                                     | 3                                   | 2                                | 1                                 | 0                                |
| PLL_PER_STA<br>TUS_STBYRET<br>ACK | PLL_PER_STA<br>TUS_LOSSREF      | PLL_PER_STA<br>TUS_CLKOUT<br>ENACK | PLL_PER_STA<br>TUS_LOCK2              | PLL_PER_STA<br>TUS_M2CHAN<br>GEACK  | PLL_PER_STA<br>TUS_SSCACK        | PLL_PER_STA<br>TUS_HIGHJITT<br>ER | PLL_PER_STA<br>TUS_BYPASS        |
| R                                 | R                               | R                                  | R                                     | R                                   | R                                | R                                 | R                                |
| 0h                                | 1h                              | 0h                                 | 0h                                    | 0h                                  | 0h                               | 0h                                | 1h                               |

**Table 2-2237. MSS\_TOPRCM\_PLL\_PER\_STATUS Register Field Descriptions**

| Bit   | Field                             | Type | Reset | Description                                                                                                                                                                                           |
|-------|-----------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | PLL_PER_STATUS_PON<br>OUT         | R    | 1h    | Status of the weak power-switch<br>0x0 : indicates the/OFF status of the weak power-switch in digital to<br>SOC.<br>0x1 : ndicates the ON status of the weak power-switch in digital to<br>SOC.       |
| 30    | PLL_PER_STATUS_PGO<br>ODOUT       | R    | 1h    | Status of the strong power-switch<br>0x0 : indicates the/OFF status of the strong power-switch in digital to<br>SOC.<br>0x1 : ndicates the ON status of the strong power-switch in digital to<br>SOC. |
| 29    | PLL_PER_STATUS_LDO<br>PWDN        | R    | 1h    | 1'b1 indicates ADPLLJ internal LDO is power down. VDDLDOOUT<br>will<br>be un-defined in this condition                                                                                                |
| 28    | PLL_PER_STATUS_REC<br>AL_BSTATUS3 | R    | 0h    | Recalibration status flag. 1 ADPLLJ requires recalibration                                                                                                                                            |
| 27    | PLL_PER_STATUS_REC<br>AL_OPPIN    | R    | 0h    | Recalibration status flag. 1 ADPLLJ requires recalibration                                                                                                                                            |
| 26:13 | RESERVED                          | NONE | 0h    | Reserved                                                                                                                                                                                              |

**Table 2-2237. MSS\_TOPRCM\_PLL\_PER\_STATUS Register Field Descriptions (continued)**

| Bit | Field                             | Type | Reset | Description                                                                                                                                                                                                                                       |
|-----|-----------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12  | PLL_PER_STATUS_CLK<br>OUTLDOENACK | R    | 1h    | Indicates the enable/disable condition of CLKOUTLDOEN<br>0x0 = CLKOUTLDO gating completed<br>0x1 = CLKOUTLDO enabling completed                                                                                                                   |
| 11  | PLL_PER_STATUS_CLK<br>DCOLDOACK   | R    | 0h    | Indicates the enable/disable condition of CLKDCOLDOEN<br>0x0 = CLKDCOLDO gating completed<br>0x1 = CLKDCOLDO enabling completed                                                                                                                   |
| 10  | PLL_PER_STATUS_PHA<br>SELOCK      | R    | 0h    | Status on PHASELOCK output pin                                                                                                                                                                                                                    |
| 9   | PLL_PER_STATUS_FRE<br>QLOCK       | R    | 0h    | Status on FREQLOCK output pin                                                                                                                                                                                                                     |
| 8   | PLL_PER_STATUS_BYPA<br>SSACK      | R    | 1h    | Status of BYPASSACK output pin                                                                                                                                                                                                                    |
| 7   | PLL_PER_STATUS_STBY<br>RETACK     | R    | 0h    | Standby and retention status<br>0x0: indicates to SOC that all internal clocks in ADPLLLJ are active and it is starting the relock process.<br>0x1: indicates to SOC that all internal clocks in ADPLLLJ are gated and it is ready for retention. |
| 6   | PLL_PER_STATUS_LOS<br>SREF        | R    | 1h    | Reference input loss is indicated by 1'b0.                                                                                                                                                                                                        |
| 5   | PLL_PER_STATUS_CLK<br>OUTENACK    | R    | 0h    | Indicates the enable/disable condition of CLKOUTEN<br>0x0 = CLKOUT gating completed<br>0x1 = CLKOUT enabling completed                                                                                                                            |
| 4   | PLL_PER_STATUS_LOC<br>K2          | R    | 0h    | ADPLL internal loop lock status                                                                                                                                                                                                                   |
| 3   | PLL_PER_STATUS_M2C<br>HANGEACK    | R    | 0h    | Acknowledge for change to M2 divider. Toggles from 1-0 or 0-1 [depending on current value] once CLKOUT frequency change has completed.                                                                                                            |
| 2   | PLL_PER_STATUS_SSC<br>ACK         | R    | 0h    | Spread Spectrum status<br>0x0 : Spread-spectrum Clocking is disabled on output clocks<br>0x1 : Spread-spectrum Clocking is enabled on output clocks                                                                                               |
| 1   | PLL_PER_STATUS_HIGH<br>JITTER     | R    | 0h    | 1'b1 indicates jitter. After PHASELOCK is asserted high, the HIGHJITTER flag is asserted high if phase error between REFCLK and FBCLK greater than 24%.                                                                                           |
| 0   | PLL_PER_STATUS_BYPA<br>SS         | R    | 1h    | Bypass status signal. 1'b1 CLKOUT in bypass                                                                                                                                                                                                       |

### 2.5.2.48 MSS\_TOPRCM\_PLL\_PER\_HSDIVIDER Register

#### 1 MSS\_TOPRCM\_PLL\_PER\_HSDIVIDER Register (Offset = 828h) [reset = 0h]

Peripheral PLL high speed divider config.

Return to [Summary Table](#)

**Table 2-2238. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0828h       |

**Figure 2-745. MSS\_TOPRCM\_PLL\_PER\_HSDIVIDER Name Register**

|          |    |    |    |    |                                      |                                      |                                      |
|----------|----|----|----|----|--------------------------------------|--------------------------------------|--------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26                                   | 25                                   | 24                                   |
| RESERVED |    |    |    |    |                                      |                                      |                                      |
| NONE     |    |    |    |    |                                      |                                      |                                      |
| 0h       |    |    |    |    |                                      |                                      |                                      |
| 23       | 22 | 21 | 20 | 19 | 18                                   | 17                                   | 16                                   |
| RESERVED |    |    |    |    |                                      | PLL_PER_HSD<br>IDIVER_LDOP<br>WDNACK | PLL_PER_HSD<br>IDIVER_BYPAS<br>SACKZ |
| NONE     |    |    |    |    |                                      | R                                    | R                                    |
| 0h       |    |    |    |    |                                      | 0h                                   | 0h                                   |
| 15       | 14 | 13 | 12 | 11 | 10                                   | 9                                    | 8                                    |
| RESERVED |    |    |    |    |                                      |                                      |                                      |
| NONE     |    |    |    |    |                                      |                                      |                                      |
| 0h       |    |    |    |    |                                      |                                      |                                      |
| 7        | 6  | 5  | 4  | 3  | 2                                    | 1                                    | 0                                    |
| RESERVED |    |    |    |    | PLL_PER_HSD<br>IDIVER_TENAB<br>LEDIV | PLL_PER_HSD<br>IDIVER_LDOP<br>WDN    | PLL_PER_HSD<br>IDIVER_BYPAS<br>S     |
| NONE     |    |    |    |    | R/W                                  | R/W                                  | R/W                                  |
| 0h       |    |    |    |    | 0h                                   | 0h                                   | 0h                                   |

**Table 2-2240. MSS\_TOPRCM\_PLL\_PER\_HSDIVIDER Register Field Descriptions**

| Bit   | Field                            | Type | Reset | Description                                                                                                                                                                                               |
|-------|----------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED                         | NONE | 0h    | Reserved                                                                                                                                                                                                  |
| 17    | PLL_PER_HSDIVIDER_L<br>DOPWDNACK | R    | 0h    | LDO Power Down Ack                                                                                                                                                                                        |
| 16    | PLL_PER_HSDIVIDER_B<br>YPASSACKZ | R    | 0h    | HSDIVIDER Bypass Ack                                                                                                                                                                                      |
| 15:3  | RESERVED                         | NONE | 0h    | Reserved                                                                                                                                                                                                  |
| 2     | PLL_PER_HSDIVIDER_T<br>ENABLEDIV | R/W  | 0h    | TENABLEDIV rising edge loads the values of M2REG and N2REG into ADPLLJ register. TENABLEDIV could be activated anytime when the DPPL digital is in power-up condition. M2 and N2 latch [active rise edge] |
| 1     | PLL_PER_HSDIVIDER_L<br>DOPWDN    | R/W  | 0h    | 1'b1 indicates ADPLLJ internal LDO is power down. VDDLDOOUT will be un-defined in this condition                                                                                                          |
| 0     | PLL_PER_HSDIVIDER_B<br>YPASS     | R/W  | 0h    | HSDIVIDER Bypass                                                                                                                                                                                          |

### 2.5.2.49 MSS\_TOPRCM\_PLL\_PER\_HSDIVIDER\_CLKOUT0 Register

#### 1 MSS\_TOPRCM\_PLL\_PER\_HSDIVIDER\_CLKOUT0 Register (Offset = 82Ch) [reset = Bh]

Peripheral PLL high speed divider clock 0 control.

Return to [Summary Table](#)

**Table 2-2241. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 082Ch       |

**Figure 2-746. MSS\_TOPRCM\_PLL\_PER\_HSDIVIDER\_CLKOUT0 Name Register**

|          |    |                                    |                                |          |    |                                  |                                     |
|----------|----|------------------------------------|--------------------------------|----------|----|----------------------------------|-------------------------------------|
| 31       | 30 | 29                                 | 28                             | 27       | 26 | 25                               | 24                                  |
| RESERVED |    |                                    |                                |          |    |                                  |                                     |
| NONE     |    |                                    |                                |          |    |                                  |                                     |
| 0h       |    |                                    |                                |          |    |                                  |                                     |
| 23       | 22 | 21                                 | 20                             | 19       | 18 | 17                               | 16                                  |
| RESERVED |    |                                    |                                |          |    |                                  |                                     |
| NONE     |    |                                    |                                |          |    |                                  |                                     |
| 0h       |    |                                    |                                |          |    |                                  |                                     |
| 15       | 14 | 13                                 | 12                             | 11       | 10 | 9                                | 8                                   |
| RESERVED |    |                                    | PLL_PER_HSDIVIDER_CLKOUT0_PWDN | RESERVED |    | PLL_PER_HSDIVIDER_CLKOUT0_STATUS | PLL_PER_HSDIVIDER_CLKOUT0_GATE_CTRL |
| NONE     |    |                                    | R/W                            | NONE     |    | R                                | R/W                                 |
| 0h       |    |                                    | 0h                             | 0h       |    | 0h                               | 0h                                  |
| 7        | 6  | 5                                  | 4                              | 3        | 2  | 1                                | 0                                   |
| RESERVED |    | PLL_PER_HSDIVIDER_CLKOUT0_DIVCHACK | PLL_PER_HSDIVIDER_CLKOUT0_DIV  |          |    |                                  |                                     |
| NONE     |    | R                                  | R/W                            |          |    |                                  |                                     |
| 0h       |    | 0h                                 | Bh                             |          |    |                                  |                                     |

**Table 2-2243. MSS\_TOPRCM\_PLL\_PER\_HSDIVIDER\_CLKOUT0 Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                                                                                                                                                 |
|-------|-------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:13 | RESERVED                            | NONE | 0h    | Reserved                                                                                                                                                                                    |
| 12    | PLL_PER_HSDIVIDER_CLKOUT0_PWDN      | R/W  | 0h    | Power down for HSDIVIDER CLKOUT0 divider and hence CLKOUT0 output<br>0h[R/W] = CLKOUT0 divider active<br>1h[R/W] = CLKOUT0 divider is powered down                                          |
| 11:10 | RESERVED                            | NONE | 0h    | Reserved                                                                                                                                                                                    |
| 9     | PLL_PER_HSDIVIDER_CLKOUT0_STATUS    | R    | 0h    | HSDIVIDER CLKOUT0 status<br>0h[R] = The clock output is gated<br>1h[R] = The clock output is enabled                                                                                        |
| 8     | PLL_PER_HSDIVIDER_CLKOUT0_GATE_CTRL | R/W  | 0h    | Control gating of HSDIVIDER CLKOUT0<br>0h[R/W] = Automatically gate this clock when there is no dependency for it<br>1h[R/W] = Force this clock to stay enabled even if there is no request |
| 7:6   | RESERVED                            | NONE | 0h    | Reserved                                                                                                                                                                                    |
| 5     | PLL_PER_HSDIVIDER_CLKOUT0_DIVCHACK  | R    | 0h    | Toggle on this status bit after changing HSDIVIDER_CLKOUT0_DIV indicates that the change in divider value has taken effect                                                                  |

**Table 2-2243. MSS\_TOPRCM\_PLL\_PER\_HSDIVIDER\_CLKOUT0 Register Field Descriptions (continued)**

| Bit | Field                         | Type | Reset | Description                                                                                                                      |
|-----|-------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | PLL_PER_HSDIVIDER_CLKOUT0_DIV | R/W  | Bh    | DPLL post-divider factor, HSDIVIDER CLKOUT0, for internal clock generation.<br>Divide values from 1 to 31.<br>0h[R/W] = Reserved |

### 2.5.2.50 MSS\_TOPRCM\_PLL\_PER\_HSDIVIDER\_CLKOUT1 Register

#### 1 MSS\_TOPRCM\_PLL\_PER\_HSDIVIDER\_CLKOUT1 Register (Offset = 830h) [reset = 9h]

Peripheral PLL high speed divider clock 1 control.

Return to [Summary Table](#)

**Table 2-2244. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0830h       |

**Figure 2-747. MSS\_TOPRCM\_PLL\_PER\_HSDIVIDER\_CLKOUT1 Name Register**

|          |    |                                    |                                |          |    |                                  |                                     |
|----------|----|------------------------------------|--------------------------------|----------|----|----------------------------------|-------------------------------------|
| 31       | 30 | 29                                 | 28                             | 27       | 26 | 25                               | 24                                  |
| RESERVED |    |                                    |                                |          |    |                                  |                                     |
| NONE     |    |                                    |                                |          |    |                                  |                                     |
| 0h       |    |                                    |                                |          |    |                                  |                                     |
| 23       | 22 | 21                                 | 20                             | 19       | 18 | 17                               | 16                                  |
| RESERVED |    |                                    |                                |          |    |                                  |                                     |
| NONE     |    |                                    |                                |          |    |                                  |                                     |
| 0h       |    |                                    |                                |          |    |                                  |                                     |
| 15       | 14 | 13                                 | 12                             | 11       | 10 | 9                                | 8                                   |
| RESERVED |    |                                    | PLL_PER_HSDIVIDER_CLKOUT1_PWDN | RESERVED |    | PLL_PER_HSDIVIDER_CLKOUT1_STATUS | PLL_PER_HSDIVIDER_CLKOUT1_GATE_CTRL |
| NONE     |    |                                    | R/W                            | NONE     |    | R                                | R/W                                 |
| 0h       |    |                                    | 0h                             | 0h       |    | 0h                               | 0h                                  |
| 7        | 6  | 5                                  | 4                              | 3        | 2  | 1                                | 0                                   |
| RESERVED |    | PLL_PER_HSDIVIDER_CLKOUT1_DIVCHACK | PLL_PER_HSDIVIDER_CLKOUT1_DIV  |          |    |                                  |                                     |
| NONE     |    | R                                  | R/W                            |          |    |                                  |                                     |
| 0h       |    | 0h                                 | 9h                             |          |    |                                  |                                     |

**Table 2-2246. MSS\_TOPRCM\_PLL\_PER\_HSDIVIDER\_CLKOUT1 Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                                                                                                                                                 |
|-------|-------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:13 | RESERVED                            | NONE | 0h    | Reserved                                                                                                                                                                                    |
| 12    | PLL_PER_HSDIVIDER_CLKOUT1_PWDN      | R/W  | 0h    | Power down for HSDIVIDER CLKOUT1 divider and hence CLKOUT1 output<br>0h[R/W] = CLKOUT1 divider active<br>1h[R/W] = CLKOUT1 divider is powered down                                          |
| 11:10 | RESERVED                            | NONE | 0h    | Reserved                                                                                                                                                                                    |
| 9     | PLL_PER_HSDIVIDER_CLKOUT1_STATUS    | R    | 0h    | HSDIVIDER CLKOUT1 status<br>0h[R] = The clock output is gated<br>1h[R] = The clock output is enabled                                                                                        |
| 8     | PLL_PER_HSDIVIDER_CLKOUT1_GATE_CTRL | R/W  | 0h    | Control gating of HSDIVIDER CLKOUT1<br>0h[R/W] = Automatically gate this clock when there is no dependency for it<br>1h[R/W] = Force this clock to stay enabled even if there is no request |
| 7:6   | RESERVED                            | NONE | 0h    | Reserved                                                                                                                                                                                    |
| 5     | PLL_PER_HSDIVIDER_CLKOUT1_DIVCHACK  | R    | 0h    | Toggle on this status bit after changing HSDIVIDER_CLKOUT1_DIV indicates that the change in divider value has taken effect                                                                  |



**Table 2-2246. MSS\_TOPRCM\_PLL\_PER\_HSDIVIDER\_CLKOUT1 Register Field Descriptions (continued)**

| Bit | Field                         | Type | Reset | Description                                                                                                                      |
|-----|-------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | PLL_PER_HSDIVIDER_CLKOUT1_DIV | R/W  | 9h    | DPLL post-divider factor, HSDIVIDER CLKOUT1, for internal clock generation.<br>Divide values from 1 to 31.<br>0h[R/W] = Reserved |

### 2.5.2.51 MSS\_TOPRCM\_PLL\_PER\_RSTCTRL Register

#### 1 MSS\_TOPRCM\_PLL\_PER\_RSTCTRL Register (Offset = 83Ch) [reset = 0h]

Peripheral PLL reset control.

Return to [Summary Table](#)

**Table 2-2247. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 083Ch       |

**Figure 2-748. MSS\_TOPRCM\_PLL\_PER\_RSTCTRL Name Register**

|          |    |    |    |    |                        |    |    |
|----------|----|----|----|----|------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                     | 25 | 24 |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                     | 17 | 16 |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                     | 9  | 8  |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                      | 1  | 0  |
| RESERVED |    |    |    |    | PLL_PER_RSTCTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                    |    |    |
| 0h       |    |    |    |    | 0h                     |    |    |

**Table 2-2249. MSS\_TOPRCM\_PLL\_PER\_RSTCTRL Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                                               |
|------|------------------------|------|-------|-------------------------------------------------------------------------------------------|
| 31:3 | RESERVED               | NONE | 0h    | Reserved                                                                                  |
| 2:0  | PLL_PER_RSTCTRL_ASSERT | R/W  | 0h    | SW Reset override for the PLL<br>Write 3'b111 : Override is enabled and Reset is asserted |

### 2.5.2.52 MSS\_TOPRCM\_PLL\_PER\_HSDIVIDER\_RSTCTRL Register

#### 1 MSS\_TOPRCM\_PLL\_PER\_HSDIVIDER\_RSTCTRL Register (Offset = 840h) [reset = 0h]

Peripheral PLL high speed divider reset control.

Return to [Summary Table](#)

**Table 2-2250. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0840h       |

**Figure 2-749. MSS\_TOPRCM\_PLL\_PER\_HSDIVIDER\_RSTCTRL Name Register**

|          |    |    |    |    |                                  |    |    |
|----------|----|----|----|----|----------------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                               | 25 | 24 |
| RESERVED |    |    |    |    |                                  |    |    |
| NONE     |    |    |    |    |                                  |    |    |
| 0h       |    |    |    |    |                                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                               | 17 | 16 |
| RESERVED |    |    |    |    |                                  |    |    |
| NONE     |    |    |    |    |                                  |    |    |
| 0h       |    |    |    |    |                                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                               | 9  | 8  |
| RESERVED |    |    |    |    |                                  |    |    |
| NONE     |    |    |    |    |                                  |    |    |
| 0h       |    |    |    |    |                                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                                | 1  | 0  |
| RESERVED |    |    |    |    | PLL_PER_HSDIVIDER_RSTCTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                              |    |    |
| 0h       |    |    |    |    | 0h                               |    |    |

**Table 2-2252. MSS\_TOPRCM\_PLL\_PER\_HSDIVIDER\_RSTCTRL Register Field Descriptions**

| Bit  | Field                            | Type | Reset | Description                                                                                     |
|------|----------------------------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                         | NONE | 0h    | Reserved                                                                                        |
| 2:0  | PLL_PER_HSDIVIDER_RSTCTRL_ASSERT | R/W  | 0h    | SW Reset override for the HSDIVIDER<br>Write 3'b111 : Override is enabled and Reset is asserted |

### 2.5.2.53 MSS\_TOPRCM\_CLKOUT0\_CLK\_SRC\_SEL Register

#### 1 MSS\_TOPRCM\_CLKOUT0\_CLK\_SRC\_SEL Register (Offset = C00h) [reset = 0h]

Clock Source select register for CLKOUT clock.

Return to [Summary Table](#)

**Table 2-2253. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0C00h       |

**Figure 2-750. MSS\_TOPRCM\_CLKOUT0\_CLK\_SRC\_SEL Name Register**

|                               |    |    |    |                               |    |    |    |
|-------------------------------|----|----|----|-------------------------------|----|----|----|
| 31                            | 30 | 29 | 28 | 27                            | 26 | 25 | 24 |
| RESERVED                      |    |    |    |                               |    |    |    |
| NONE                          |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |
| 23                            | 22 | 21 | 20 | 19                            | 18 | 17 | 16 |
| RESERVED                      |    |    |    |                               |    |    |    |
| NONE                          |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |
| 15                            | 14 | 13 | 12 | 11                            | 10 | 9  | 8  |
| RESERVED                      |    |    |    | CLKOUT0_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                          |    |    |    | R/W                           |    |    |    |
| 0h                            |    |    |    | 0h                            |    |    |    |
| 7                             | 6  | 5  | 4  | 3                             | 2  | 1  | 0  |
| CLKOUT0_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                               |    |    |    |
| R/W                           |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |

**Table 2-2255. MSS\_TOPRCM\_CLKOUT0\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                         | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|-------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                      | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 11:0  | CLKOUT0_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for MSS CLKOUT .<br>Data should be loaded as multibit.<br>For example: if Clock source 0x5 should be selected then 0x555 should be configured to the register.<br>Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - DPLL_CORE_HSDIV0_CLKOUT0<br>0x222 - DPLL_CORE_HSDIV0_CLKOUT1<br>0x333 - DPLL_PER_HSDIV0_CLKOUT0<br>0x444 - DPLL_PER_HSDIV0_CLKOUT1<br>0x555 - RCCLK10M<br>0x666 - RCCLK32K<br>0x777 - CTPS_GENF0 |

### 2.5.2.54 MSS\_TOPRCM\_CLKOUT1\_CLK\_SRC\_SEL Register

#### 1 MSS\_TOPRCM\_CLKOUT1\_CLK\_SRC\_SEL Register (Offset = C04h) [reset = 0h]

Clock Source select register for CLKOUT clock.

Return to [Summary Table](#)

**Table 2-2256. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0C04h       |

**Figure 2-751. MSS\_TOPRCM\_CLKOUT1\_CLK\_SRC\_SEL Name Register**

|                               |    |    |    |                               |    |    |    |
|-------------------------------|----|----|----|-------------------------------|----|----|----|
| 31                            | 30 | 29 | 28 | 27                            | 26 | 25 | 24 |
| RESERVED                      |    |    |    |                               |    |    |    |
| NONE                          |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |
| 23                            | 22 | 21 | 20 | 19                            | 18 | 17 | 16 |
| RESERVED                      |    |    |    |                               |    |    |    |
| NONE                          |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |
| 15                            | 14 | 13 | 12 | 11                            | 10 | 9  | 8  |
| RESERVED                      |    |    |    | CLKOUT1_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                          |    |    |    | R/W                           |    |    |    |
| 0h                            |    |    |    | 0h                            |    |    |    |
| 7                             | 6  | 5  | 4  | 3                             | 2  | 1  | 0  |
| CLKOUT1_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                               |    |    |    |
| R/W                           |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |

**Table 2-2258. MSS\_TOPRCM\_CLKOUT1\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                         | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|-------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                      | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 11:0  | CLKOUT1_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for MSS CLKOUT .<br>Data should be loaded as multibit.<br>For example: if Clock source 0x5 should be selected then 0x555 should be configured to the register.<br>Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - DPLL_CORE_HSDIV0_CLKOUT0<br>0x222 - DPLL_CORE_HSDIV0_CLKOUT1<br>0x333 - DPLL_PER_HSDIV0_CLKOUT0<br>0x444 - DPLL_PER_HSDIV0_CLKOUT1<br>0x555 - RCCLK10M<br>0x666 - RCCLK32K<br>0x777 - CTPS_GENF0 |

### 2.5.2.55 MSS\_TOPRCM\_CLKOUT0\_DIV\_VAL Register

#### 1 MSS\_TOPRCM\_CLKOUT0\_DIV\_VAL Register (Offset = C08h) [reset = 0h]

Clock Divider register for CLKOUT clock.

Return to [Summary Table](#)

**Table 2-2259. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0C08h       |

**Figure 2-752. MSS\_TOPRCM\_CLKOUT0\_DIV\_VAL Name Register**

|                        |    |    |    |                        |    |    |    |
|------------------------|----|----|----|------------------------|----|----|----|
| 31                     | 30 | 29 | 28 | 27                     | 26 | 25 | 24 |
| RESERVED               |    |    |    |                        |    |    |    |
| NONE                   |    |    |    |                        |    |    |    |
| 0h                     |    |    |    |                        |    |    |    |
| 23                     | 22 | 21 | 20 | 19                     | 18 | 17 | 16 |
| RESERVED               |    |    |    |                        |    |    |    |
| NONE                   |    |    |    |                        |    |    |    |
| 0h                     |    |    |    |                        |    |    |    |
| 15                     | 14 | 13 | 12 | 11                     | 10 | 9  | 8  |
| RESERVED               |    |    |    | CLKOUT0_DIV_VAL_CLKDIV |    |    |    |
| NONE                   |    |    |    | R/W                    |    |    |    |
| 0h                     |    |    |    | 0h                     |    |    |    |
| 7                      | 6  | 5  | 4  | 3                      | 2  | 1  | 0  |
| CLKOUT0_DIV_VAL_CLKDIV |    |    |    |                        |    |    |    |
| R/W                    |    |    |    |                        |    |    |    |
| 0h                     |    |    |    |                        |    |    |    |

**Table 2-2261. MSS\_TOPRCM\_CLKOUT0\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                  | Type | Reset | Description                                                                                                                                                                                                                                              |
|-------|------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED               | NONE | 0h    | Reserved                                                                                                                                                                                                                                                 |
| 11:0  | CLKOUT0_DIV_VAL_CLKDIV | R/W  | 0h    | Divider value for CLKOUT selected clock..To set the divider value of [n+1] configure the register to '0xnnn'.Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

### 2.5.2.56 MSS\_TOPRCM\_CLKOUT1\_DIV\_VAL Register

#### 1 MSS\_TOPRCM\_CLKOUT1\_DIV\_VAL Register (Offset = C0Ch) [reset = 0h]

Clock Divider register for CLKOUT clock.

Return to [Summary Table](#)

**Table 2-2262. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0C0Ch       |

**Figure 2-753. MSS\_TOPRCM\_CLKOUT1\_DIV\_VAL Name Register**

|                        |    |    |    |                        |    |    |    |
|------------------------|----|----|----|------------------------|----|----|----|
| 31                     | 30 | 29 | 28 | 27                     | 26 | 25 | 24 |
| RESERVED               |    |    |    |                        |    |    |    |
| NONE                   |    |    |    |                        |    |    |    |
| 0h                     |    |    |    |                        |    |    |    |
| 23                     | 22 | 21 | 20 | 19                     | 18 | 17 | 16 |
| RESERVED               |    |    |    |                        |    |    |    |
| NONE                   |    |    |    |                        |    |    |    |
| 0h                     |    |    |    |                        |    |    |    |
| 15                     | 14 | 13 | 12 | 11                     | 10 | 9  | 8  |
| RESERVED               |    |    |    | CLKOUT1_DIV_VAL_CLKDIV |    |    |    |
| NONE                   |    |    |    | R/W                    |    |    |    |
| 0h                     |    |    |    | 0h                     |    |    |    |
| 7                      | 6  | 5  | 4  | 3                      | 2  | 1  | 0  |
| CLKOUT1_DIV_VAL_CLKDIV |    |    |    |                        |    |    |    |
| R/W                    |    |    |    |                        |    |    |    |
| 0h                     |    |    |    |                        |    |    |    |

**Table 2-2264. MSS\_TOPRCM\_CLKOUT1\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                  | Type | Reset | Description                                                                                                                                                                                                                                              |
|-------|------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED               | NONE | 0h    | Reserved                                                                                                                                                                                                                                                 |
| 11:0  | CLKOUT1_DIV_VAL_CLKDIV | R/W  | 0h    | Divider value for CLKOUT selected clock..To set the divider value of [n+1] configure the register to '0xnnn'.Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

### 2.5.2.57 MSS\_TOPRCM\_CLKOUT0\_CLK\_GATE Register

#### 1 MSS\_TOPRCM\_CLKOUT0\_CLK\_GATE Register (Offset = C10h) [reset = 0h]

Clock Gating register for CLKOUT clock.

Return to [Summary Table](#)

**Table 2-2265. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0C10h       |

**Figure 2-754. MSS\_TOPRCM\_CLKOUT0\_CLK\_GATE Name Register**

|          |    |    |    |                        |    |    |    |
|----------|----|----|----|------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                     | 26 | 25 | 24 |
| RESERVED |    |    |    |                        |    |    |    |
| NONE     |    |    |    |                        |    |    |    |
| 0h       |    |    |    |                        |    |    |    |
| 23       | 22 | 21 | 20 | 19                     | 18 | 17 | 16 |
| RESERVED |    |    |    |                        |    |    |    |
| NONE     |    |    |    |                        |    |    |    |
| 0h       |    |    |    |                        |    |    |    |
| 15       | 14 | 13 | 12 | 11                     | 10 | 9  | 8  |
| RESERVED |    |    |    |                        |    |    |    |
| NONE     |    |    |    |                        |    |    |    |
| 0h       |    |    |    |                        |    |    |    |
| 7        | 6  | 5  | 4  | 3                      | 2  | 1  | 0  |
| RESERVED |    |    |    | CLKOUT0_CLK_GATE_GATED |    |    |    |
| NONE     |    |    |    | R/W                    |    |    |    |
| 0h       |    |    |    | 0h                     |    |    |    |

**Table 2-2267. MSS\_TOPRCM\_CLKOUT0\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                                                                                                                                                                                |
|------|------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED               | NONE | 0h    | Reserved                                                                                                                                                                                                                   |
| 2:0  | CLKOUT0_CLK_GATE_GATED | R/W  | 0h    | Only for debug- Functionality not guaranteed<br>Clock gating config for MSS CLKOUT<br>Data should be loaded as multibit.<br>Write 3'b000 : Clock is ungated [multibit 000]<br>Write 3'b111 : Clock is gated [multibit 111] |



### 2.5.2.58 MSS\_TOPRCM\_CLKOUT1\_CLK\_GATE Register

#### 1 MSS\_TOPRCM\_CLKOUT1\_CLK\_GATE Register (Offset = C14h) [reset = 0h]

Clock Gating register for CLKOUT clock.

Return to [Summary Table](#)

**Table 2-2268. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0C14h       |

**Figure 2-755. MSS\_TOPRCM\_CLKOUT1\_CLK\_GATE Name Register**

|          |    |    |    |    |                        |    |    |
|----------|----|----|----|----|------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                     | 25 | 24 |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                     | 17 | 16 |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                     | 9  | 8  |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                      | 1  | 0  |
| RESERVED |    |    |    |    | CLKOUT1_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                    |    |    |
| 0h       |    |    |    |    | 0h                     |    |    |

**Table 2-2270. MSS\_TOPRCM\_CLKOUT1\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                                                                                                                                                                                |
|------|------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED               | NONE | 0h    | Reserved                                                                                                                                                                                                                   |
| 2:0  | CLKOUT1_CLK_GATE_GATED | R/W  | 0h    | Only for debug- Functionality not guaranteed<br>Clock gating config for MSS CLKOUT<br>Data should be loaded as multibit.<br>Write 3'b000 : Clock is ungated [multibit 000]<br>Write 3'b111 : Clock is gated [multibit 111] |

### 2.5.2.59 MSS\_TOPRCM\_CLKOUT0\_CLK\_STATUS Register

#### 1 MSS\_TOPRCM\_CLKOUT0\_CLK\_STATUS Register (Offset = C18h) [reset = 1h]

Clock Status register for CLKOUT clock.

Return to [Summary Table](#)

**Table 2-2271. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0C18h       |

**Figure 2-756. MSS\_TOPRCM\_CLKOUT0\_CLK\_STATUS Name Register**

|                                |    |    |    |    |    |    |    |
|--------------------------------|----|----|----|----|----|----|----|
| 31                             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                       |    |    |    |    |    |    |    |
| NONE                           |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |
| 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                       |    |    |    |    |    |    |    |
| NONE                           |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |
| 15                             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CLKOUT0_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                              |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |
| 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CLKOUT0_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                              |    |    |    |    |    |    |    |
| 1h                             |    |    |    |    |    |    |    |

**Table 2-2273. MSS\_TOPRCM\_CLKOUT0\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                     |
|-------|--------------------------------|------|-------|-----------------------------------------------------------------|
| 31:16 | RESERVED                       | NONE | 0h    | Reserved                                                        |
| 15:8  | CLKOUT0_CLK_STATUS_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for CLKOUT Clock |
| 7:0   | CLKOUT0_CLK_STATUS_CLKINUSE    | R    | 1h    | Status shows the source clock slected for CLKOUT Clock          |

### 2.5.2.60 MSS\_TOPRCM\_CLKOUT1\_CLK\_STATUS Register

#### 1 MSS\_TOPRCM\_CLKOUT1\_CLK\_STATUS Register (Offset = C1Ch) [reset = 1h]

Clock Status register for CLKOUT clock.

Return to [Summary Table](#)

**Table 2-2274. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0C1Ch       |

**Figure 2-757. MSS\_TOPRCM\_CLKOUT1\_CLK\_STATUS Name Register**

|                                |    |    |    |    |    |    |    |
|--------------------------------|----|----|----|----|----|----|----|
| 31                             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                       |    |    |    |    |    |    |    |
| NONE                           |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |
| 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                       |    |    |    |    |    |    |    |
| NONE                           |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |
| 15                             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CLKOUT1_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                              |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |
| 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CLKOUT1_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                              |    |    |    |    |    |    |    |
| 1h                             |    |    |    |    |    |    |    |

**Table 2-2276. MSS\_TOPRCM\_CLKOUT1\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                     |
|-------|--------------------------------|------|-------|-----------------------------------------------------------------|
| 31:16 | RESERVED                       | NONE | 0h    | Reserved                                                        |
| 15:8  | CLKOUT1_CLK_STATUS_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for CLKOUT Clock |
| 7:0   | CLKOUT1_CLK_STATUS_CLKINUSE    | R    | 1h    | Status shows the source clock slected for CLKOUT Clock          |

### 2.5.2.61 MSS\_TOPRCM\_TRCCLKOUT\_CLK\_SRC\_SEL Register

#### 1 MSS\_TOPRCM\_TRCCLKOUT\_CLK\_SRC\_SEL Register (Offset = C20h) [reset = 0h]

Clock Source select register for TRC clkout.

Return to [Summary Table](#)

**Table 2-2277. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0C20h       |

**Figure 2-758. MSS\_TOPRCM\_TRCCLKOUT\_CLK\_SRC\_SEL Name Register**

|                                 |    |    |    |                                 |    |    |    |
|---------------------------------|----|----|----|---------------------------------|----|----|----|
| 31                              | 30 | 29 | 28 | 27                              | 26 | 25 | 24 |
| RESERVED                        |    |    |    |                                 |    |    |    |
| NONE                            |    |    |    |                                 |    |    |    |
| 0h                              |    |    |    |                                 |    |    |    |
| 23                              | 22 | 21 | 20 | 19                              | 18 | 17 | 16 |
| RESERVED                        |    |    |    |                                 |    |    |    |
| NONE                            |    |    |    |                                 |    |    |    |
| 0h                              |    |    |    |                                 |    |    |    |
| 15                              | 14 | 13 | 12 | 11                              | 10 | 9  | 8  |
| RESERVED                        |    |    |    | TRCCLKOUT_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                            |    |    |    | R/W                             |    |    |    |
| 0h                              |    |    |    | 0h                              |    |    |    |
| 7                               | 6  | 5  | 4  | 3                               | 2  | 1  | 0  |
| TRCCLKOUT_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                 |    |    |    |
| R/W                             |    |    |    |                                 |    |    |    |
| 0h                              |    |    |    |                                 |    |    |    |

**Table 2-2279. MSS\_TOPRCM\_TRCCLKOUT\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|---------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 11:0  | TRCCLKOUT_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for TRC Clkout<br>Data should be loaded as multibit.<br>For example: if Clock source 0x5 should be selected then 0x555 should be configured to the register.<br>Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - DPLL_CORE_HSDIV0_CLKOUT0<br>0x222 - DPLL_CORE_HSDIV0_CLKOUT1<br>0x333 - DPLL_PER_HSDIV0_CLKOUT0<br>0x444 - DPLL_PER_HSDIV0_CLKOUT1<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - RCCLK10M |

### 2.5.2.62 MSS\_TOPRCM\_TRCCLKOUT\_DIV\_VAL Register

#### 1 MSS\_TOPRCM\_TRCCLKOUT\_DIV\_VAL Register (Offset = C24h) [reset = 0h]

Clock Divider register for TRC clkout.

Return to [Summary Table](#)

**Table 2-2280. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0C24h       |

**Figure 2-759. MSS\_TOPRCM\_TRCCLKOUT\_DIV\_VAL Name Register**

|                          |    |    |    |                          |    |    |    |
|--------------------------|----|----|----|--------------------------|----|----|----|
| 31                       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED                 |    |    |    |                          |    |    |    |
| NONE                     |    |    |    |                          |    |    |    |
| 0h                       |    |    |    |                          |    |    |    |
| 23                       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED                 |    |    |    |                          |    |    |    |
| NONE                     |    |    |    |                          |    |    |    |
| 0h                       |    |    |    |                          |    |    |    |
| 15                       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED                 |    |    |    | TRCCLKOUT_DIV_VAL_CLKDIV |    |    |    |
| NONE                     |    |    |    | R/W                      |    |    |    |
| 0h                       |    |    |    | 0h                       |    |    |    |
| 7                        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| TRCCLKOUT_DIV_VAL_CLKDIV |    |    |    |                          |    |    |    |
| R/W                      |    |    |    |                          |    |    |    |
| 0h                       |    |    |    |                          |    |    |    |

**Table 2-2282. MSS\_TOPRCM\_TRCCLKOUT\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                    | Type | Reset | Description                                                                                                                                                                                                                                        |
|-------|--------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                                                                                                                           |
| 11:0  | TRCCLKOUT_DIV_VAL_CLKDIV | R/W  | 0h    | Divider value for TRC selected clock..To set the divider value of [n+1] configure the register to '0xnnn'.Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

### 2.5.2.63 MSS\_TOPRCM\_TRCCLKOUT\_CLK\_GATE Register

#### 1 MSS\_TOPRCM\_TRCCLKOUT\_CLK\_GATE Register (Offset = C28h) [reset = 0h]

Clock Gating register for TRC clkout.

Return to [Summary Table](#)

**Table 2-2283. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0C28h       |

**Figure 2-760. MSS\_TOPRCM\_TRCCLKOUT\_CLK\_GATE Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | TRCCLKOUT_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-2285. MSS\_TOPRCM\_TRCCLKOUT\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                                                |
|------|--------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                                                   |
| 2:0  | TRCCLKOUT_CLK_GATE_GATED | R/W  | 0h    | Clock gating config for TRC Clkout<br>Data should be loaded as multibit.<br>Write 3'b000 : Clock is ungated [multibit 000]<br>Write 3'b111 : Clock is gated [multibit 111] |

### 2.5.2.64 MSS\_TOPRCM\_TRCCLKOUT\_CLK\_STATUS Register

#### 1 MSS\_TOPRCM\_TRCCLKOUT\_CLK\_STATUS Register (Offset = C2Ch) [reset = 1h]

Clock Status register for TRC clkout.

Return to [Summary Table](#)

**Table 2-2286. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0C2Ch       |

**Figure 2-761. MSS\_TOPRCM\_TRCCLKOUT\_CLK\_STATUS Name Register**

|                                  |    |    |    |    |    |    |    |
|----------------------------------|----|----|----|----|----|----|----|
| 31                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                         |    |    |    |    |    |    |    |
| NONE                             |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 23                               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                         |    |    |    |    |    |    |    |
| NONE                             |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 15                               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TRCCLKOUT_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                                |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 7                                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TRCCLKOUT_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                                |    |    |    |    |    |    |    |
| 1h                               |    |    |    |    |    |    |    |

**Table 2-2288. MSS\_TOPRCM\_TRCCLKOUT\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                            | Type | Reset | Description                                                           |
|-------|----------------------------------|------|-------|-----------------------------------------------------------------------|
| 31:16 | RESERVED                         | NONE | 0h    | Reserved                                                              |
| 15:8  | TRCCLKOUT_CLK_STATUS_CURRDIVIDER | R    | 0h    | Status shows the current divider value chosen for TRCCLK Clkout Clock |
| 7:0   | TRCCLKOUT_CLK_STATUS_CLKINUSE    | R    | 1h    | Status shows the source clock selected for TRCCLK Clkout Clock        |

### 2.5.2.65 MSS\_TOPRCM\_HW\_REG0 Register

#### 1 MSS\_TOPRCM\_HW\_REG0 Register (Offset = E00h) [reset = 0h]

Reserved for Hardware RnD.

Return to [Summary Table](#)

**Table 2-2289. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0E00h       |

**Figure 2-762. MSS\_TOPRCM\_HW\_REG0 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HW_REG0_HWREG |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HW_REG0_HWREG |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HW_REG0_HWREG |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HW_REG0_HWREG |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 2-2291. MSS\_TOPRCM\_HW\_REG0 Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                              |
|------|---------------|------|-------|------------------------------------------|
| 31:0 | HW_REG0_HWREG | R/W  | 0h    | HW Reserved regiser. Reserved for HW RnD |



### 2.5.2.66 MSS\_TOPRCM\_HW\_REG1 Register

#### 1 MSS\_TOPRCM\_HW\_REG1 Register (Offset = E04h) [reset = 0h]

Reserved for Hardware RnD.

Return to [Summary Table](#)

**Table 2-2292. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0E04h       |

**Figure 2-763. MSS\_TOPRCM\_HW\_REG1 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HW_REG1_HWREG |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HW_REG1_HWREG |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HW_REG1_HWREG |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HW_REG1_HWREG |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 2-2294. MSS\_TOPRCM\_HW\_REG1 Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                              |
|------|---------------|------|-------|------------------------------------------|
| 31:0 | HW_REG1_HWREG | R/W  | 0h    | HW Reserved regiser. Reserved for HW RnD |

### 2.5.2.67 MSS\_TOPRCM\_HW\_REG2 Register

#### 1 MSS\_TOPRCM\_HW\_REG2 Register (Offset = E08h) [reset = 0h]

Reserved for Hardware RnD.

Return to [Summary Table](#)

**Table 2-2295. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0E08h       |

**Figure 2-764. MSS\_TOPRCM\_HW\_REG2 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HW_REG2_HWREG |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HW_REG2_HWREG |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HW_REG2_HWREG |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HW_REG2_HWREG |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 2-2297. MSS\_TOPRCM\_HW\_REG2 Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                              |
|------|---------------|------|-------|------------------------------------------|
| 31:0 | HW_REG2_HWREG | R/W  | 0h    | HW Reserved regiser. Reserved for HW RnD |

### 2.5.2.68 MSS\_TOPRCM\_HW\_REG3 Register

#### 1 MSS\_TOPRCM\_HW\_REG3 Register (Offset = E0Ch) [reset = 0h]

Reserved for Hardware RnD.

Return to [Summary Table](#)

**Table 2-2298. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0E0Ch       |

**Figure 2-765. MSS\_TOPRCM\_HW\_REG3 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HW_REG3_HWREG |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HW_REG3_HWREG |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HW_REG3_HWREG |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HW_REG3_HWREG |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 2-2300. MSS\_TOPRCM\_HW\_REG3 Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                              |
|------|---------------|------|-------|------------------------------------------|
| 31:0 | HW_REG3_HWREG | R/W  | 0h    | HW Reserved regiser. Reserved for HW RnD |

### 2.5.2.69 MSS\_TOPRCM\_HW\_SPARE\_RW0 Register

#### 1 MSS\_TOPRCM\_HW\_SPARE\_RW0 Register (Offset = FD0h) [reset = 0h]

HW\_SPARE\_RW0.

Return to [Summary Table](#)

**Table 2-2301. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0FD0h       |

**Figure 2-766. MSS\_TOPRCM\_HW\_SPARE\_RW0 Name Register**

|                           |    |    |    |    |    |    |    |
|---------------------------|----|----|----|----|----|----|----|
| 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HW_SPARE_RW0_HW_SPARE_RW0 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 23                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HW_SPARE_RW0_HW_SPARE_RW0 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 15                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HW_SPARE_RW0_HW_SPARE_RW0 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 7                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HW_SPARE_RW0_HW_SPARE_RW0 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |

**Table 2-2303. MSS\_TOPRCM\_HW\_SPARE\_RW0 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description         |
|------|---------------------------|------|-------|---------------------|
| 31:0 | HW_SPARE_RW0_HW_SPARE_RW0 | R/W  | 0h    | Reserved for HW R&D |

### 2.5.2.70 MSS\_TOPRCM\_HW\_SPARE\_RW1 Register

#### 1 MSS\_TOPRCM\_HW\_SPARE\_RW1 Register (Offset = FD4h) [reset = 0h]

HW\_SPARE\_RW1.

Return to [Summary Table](#)

**Table 2-2304. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0FD4h       |

**Figure 2-767. MSS\_TOPRCM\_HW\_SPARE\_RW1 Name Register**

|                           |    |    |    |    |    |    |    |
|---------------------------|----|----|----|----|----|----|----|
| 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HW_SPARE_RW1_HW_SPARE_RW1 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 23                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HW_SPARE_RW1_HW_SPARE_RW1 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 15                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HW_SPARE_RW1_HW_SPARE_RW1 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 7                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HW_SPARE_RW1_HW_SPARE_RW1 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |

**Table 2-2306. MSS\_TOPRCM\_HW\_SPARE\_RW1 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description         |
|------|---------------------------|------|-------|---------------------|
| 31:0 | HW_SPARE_RW1_HW_SPARE_RW1 | R/W  | 0h    | Reserved for HW R&D |

### 2.5.2.71 MSS\_TOPRCM\_HW\_SPARE\_RW2 Register

#### 1 MSS\_TOPRCM\_HW\_SPARE\_RW2 Register (Offset = FD8h) [reset = 0h]

HW\_SPARE\_RW2.

Return to [Summary Table](#)

**Table 2-2307. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0FD8h       |

**Figure 2-768. MSS\_TOPRCM\_HW\_SPARE\_RW2 Name Register**

|                           |    |    |    |    |    |    |    |
|---------------------------|----|----|----|----|----|----|----|
| 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HW_SPARE_RW2_HW_SPARE_RW2 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 23                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HW_SPARE_RW2_HW_SPARE_RW2 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 15                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HW_SPARE_RW2_HW_SPARE_RW2 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 7                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HW_SPARE_RW2_HW_SPARE_RW2 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |

**Table 2-2309. MSS\_TOPRCM\_HW\_SPARE\_RW2 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description         |
|------|---------------------------|------|-------|---------------------|
| 31:0 | HW_SPARE_RW2_HW_SPARE_RW2 | R/W  | 0h    | Reserved for HW R&D |

### 2.5.2.72 MSS\_TOPRCM\_HW\_SPARE\_RW3 Register

#### 1 MSS\_TOPRCM\_HW\_SPARE\_RW3 Register (Offset = FDCh) [reset = 0h]

HW\_SPARE\_RW3.

Return to [Summary Table](#)

**Table 2-2310. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0FDCh       |

**Figure 2-769. MSS\_TOPRCM\_HW\_SPARE\_RW3 Name Register**

|                           |    |    |    |    |    |    |    |
|---------------------------|----|----|----|----|----|----|----|
| 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HW_SPARE_RW3_HW_SPARE_RW3 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 23                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HW_SPARE_RW3_HW_SPARE_RW3 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 15                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HW_SPARE_RW3_HW_SPARE_RW3 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 7                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HW_SPARE_RW3_HW_SPARE_RW3 |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |

**Table 2-2312. MSS\_TOPRCM\_HW\_SPARE\_RW3 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description         |
|------|---------------------------|------|-------|---------------------|
| 31:0 | HW_SPARE_RW3_HW_SPARE_RW3 | R/W  | 0h    | Reserved for HW R&D |

### 2.5.2.73 MSS\_TOPRCM\_HW\_SPARE\_RO0 Register

#### 1 MSS\_TOPRCM\_HW\_SPARE\_RO0 Register (Offset = FE0h) [reset = 0h]

HW\_SPARE\_RO0.

Return to [Summary Table](#)

**Table 2-2313. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0FE0h       |

**Figure 2-770. MSS\_TOPRCM\_HW\_SPARE\_RO0 Name Register**

|                           |    |    |    |    |    |    |    |
|---------------------------|----|----|----|----|----|----|----|
| 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HW_SPARE_RO0_HW_SPARE_RO0 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 23                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HW_SPARE_RO0_HW_SPARE_RO0 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 15                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HW_SPARE_RO0_HW_SPARE_RO0 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 7                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HW_SPARE_RO0_HW_SPARE_RO0 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |

**Table 2-2315. MSS\_TOPRCM\_HW\_SPARE\_RO0 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description         |
|------|---------------------------|------|-------|---------------------|
| 31:0 | HW_SPARE_RO0_HW_SPARE_RO0 | R    | 0h    | Reserved for HW R&D |



## 2.5.2.74 MSS\_TOPRCM\_HW\_SPARE\_RO1 Register

### 1 MSS\_TOPRCM\_HW\_SPARE\_RO1 Register (Offset = FE4h) [reset = 0h]

HW\_SPARE\_RO1.

Return to [Summary Table](#)

**Table 2-2316. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0FE4h       |

**Figure 2-771. MSS\_TOPRCM\_HW\_SPARE\_RO1 Name Register**

|                           |    |    |    |    |    |    |    |
|---------------------------|----|----|----|----|----|----|----|
| 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HW_SPARE_RO1_HW_SPARE_RO1 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 23                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HW_SPARE_RO1_HW_SPARE_RO1 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 15                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HW_SPARE_RO1_HW_SPARE_RO1 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 7                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HW_SPARE_RO1_HW_SPARE_RO1 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |

**Table 2-2318. MSS\_TOPRCM\_HW\_SPARE\_RO1 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description         |
|------|---------------------------|------|-------|---------------------|
| 31:0 | HW_SPARE_RO1_HW_SPARE_RO1 | R    | 0h    | Reserved for HW R&D |

### 2.5.2.75 MSS\_TOPRCM\_HW\_SPARE\_RO2 Register

#### 1 MSS\_TOPRCM\_HW\_SPARE\_RO2 Register (Offset = FE8h) [reset = 0h]

HW\_SPARE\_RO2.

Return to [Summary Table](#)

**Table 2-2319. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0FE8h       |

**Figure 2-772. MSS\_TOPRCM\_HW\_SPARE\_RO2 Name Register**

|                           |    |    |    |    |    |    |    |
|---------------------------|----|----|----|----|----|----|----|
| 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HW_SPARE_RO2_HW_SPARE_RO2 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 23                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HW_SPARE_RO2_HW_SPARE_RO2 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 15                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HW_SPARE_RO2_HW_SPARE_RO2 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 7                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HW_SPARE_RO2_HW_SPARE_RO2 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |

**Table 2-2321. MSS\_TOPRCM\_HW\_SPARE\_RO2 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description         |
|------|---------------------------|------|-------|---------------------|
| 31:0 | HW_SPARE_RO2_HW_SPARE_RO2 | R    | 0h    | Reserved for HW R&D |

### 2.5.2.76 MSS\_TOPRCM\_HW\_SPARE\_RO3 Register

#### 1 MSS\_TOPRCM\_HW\_SPARE\_RO3 Register (Offset = FECh) [reset = 0h]

HW\_SPARE\_RO3.

Return to [Summary Table](#)

**Table 2-2322. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0FECh       |

**Figure 2-773. MSS\_TOPRCM\_HW\_SPARE\_RO3 Name Register**

|                           |    |    |    |    |    |    |    |
|---------------------------|----|----|----|----|----|----|----|
| 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HW_SPARE_RO3_HW_SPARE_RO3 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 23                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HW_SPARE_RO3_HW_SPARE_RO3 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 15                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HW_SPARE_RO3_HW_SPARE_RO3 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 7                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HW_SPARE_RO3_HW_SPARE_RO3 |    |    |    |    |    |    |    |
| R                         |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |

**Table 2-2324. MSS\_TOPRCM\_HW\_SPARE\_RO3 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description         |
|------|---------------------------|------|-------|---------------------|
| 31:0 | HW_SPARE_RO3_HW_SPARE_RO3 | R    | 0h    | Reserved for HW R&D |

### 2.5.2.77 MSS\_TOPRCM\_HW\_SPARE\_WPH Register

#### 1 MSS\_TOPRCM\_HW\_SPARE\_WPH Register (Offset = FF0h) [reset = 0h]

HW\_SPARE\_WPH.

Return to [Summary Table](#)

**Table 2-2325. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0FF0h       |

**Figure 2-774. MSS\_TOPRCM\_HW\_SPARE\_WPH Name Register**

|                           |    |    |    |    |    |    |    |
|---------------------------|----|----|----|----|----|----|----|
| 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| HW_SPARE_WPH_HW_SPARE_WPH |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 23                        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| HW_SPARE_WPH_HW_SPARE_WPH |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 15                        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HW_SPARE_WPH_HW_SPARE_WPH |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |
| 7                         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HW_SPARE_WPH_HW_SPARE_WPH |    |    |    |    |    |    |    |
| R/W                       |    |    |    |    |    |    |    |
| 0h                        |    |    |    |    |    |    |    |

**Table 2-2327. MSS\_TOPRCM\_HW\_SPARE\_WPH Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description         |
|------|---------------------------|------|-------|---------------------|
| 31:0 | HW_SPARE_WPH_HW_SPARE_WPH | R/W  | 0h    | Reserved for HW R&D |

## 2.5.2.78 MSS\_TOPRCM\_HW\_SPARE\_REC Register

### 1 MSS\_TOPRCM\_HW\_SPARE\_REC Register (Offset = FF4h) [reset = 0h]

HW\_SPARE\_REC.

Return to [Summary Table](#)

**Table 2-2328. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 0FF4h       |

**Figure 2-775. MSS\_TOPRCM\_HW\_SPARE\_REC Name Register**

| 31                                  | 30                                  | 29                                  | 28                                  | 27                                  | 26                                  | 25                                  | 24                                  |
|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|
| HW_SPARE_R<br>EC_HW_SPAR<br>E_REC31 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC30 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC29 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC28 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC27 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC26 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC25 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC24 |
| R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 |
| 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  |
| 23                                  | 22                                  | 21                                  | 20                                  | 19                                  | 18                                  | 17                                  | 16                                  |
| HW_SPARE_R<br>EC_HW_SPAR<br>E_REC23 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC22 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC21 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC20 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC19 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC18 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC17 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC16 |
| R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 |
| 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  |
| 15                                  | 14                                  | 13                                  | 12                                  | 11                                  | 10                                  | 9                                   | 8                                   |
| HW_SPARE_R<br>EC_HW_SPAR<br>E_REC15 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC14 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC13 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC12 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC11 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC10 | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC9  | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC8  |
| R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 |
| 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  |
| 7                                   | 6                                   | 5                                   | 4                                   | 3                                   | 2                                   | 1                                   | 0                                   |
| HW_SPARE_R<br>EC_HW_SPAR<br>E_REC7  | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC6  | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC5  | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC4  | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC3  | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC2  | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC1  | HW_SPARE_R<br>EC_HW_SPAR<br>E_REC0  |
| R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 | R/W                                 |
| 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  | 0h                                  |

**Table 2-2330. MSS\_TOPRCM\_HW\_SPARE\_REC Register Field Descriptions**

| Bit | Field                           | Type | Reset | Description         |
|-----|---------------------------------|------|-------|---------------------|
| 31  | HW_SPARE_REC_HW_S<br>PARE_REC31 | R/W  | 0h    | Reserved for HW R&D |
| 30  | HW_SPARE_REC_HW_S<br>PARE_REC30 | R/W  | 0h    | Reserved for HW R&D |
| 29  | HW_SPARE_REC_HW_S<br>PARE_REC29 | R/W  | 0h    | Reserved for HW R&D |
| 28  | HW_SPARE_REC_HW_S<br>PARE_REC28 | R/W  | 0h    | Reserved for HW R&D |
| 27  | HW_SPARE_REC_HW_S<br>PARE_REC27 | R/W  | 0h    | Reserved for HW R&D |
| 26  | HW_SPARE_REC_HW_S<br>PARE_REC26 | R/W  | 0h    | Reserved for HW R&D |
| 25  | HW_SPARE_REC_HW_S<br>PARE_REC25 | R/W  | 0h    | Reserved for HW R&D |

**Table 2-2330. MSS\_TOPRCM\_HW\_SPARE\_REC Register Field Descriptions (continued)**

| Bit | Field                           | Type | Reset | Description         |
|-----|---------------------------------|------|-------|---------------------|
| 24  | HW_SPARE_REC_HW_S<br>PARE_REC24 | R/W  | 0h    | Reserved for HW R&D |
| 23  | HW_SPARE_REC_HW_S<br>PARE_REC23 | R/W  | 0h    | Reserved for HW R&D |
| 22  | HW_SPARE_REC_HW_S<br>PARE_REC22 | R/W  | 0h    | Reserved for HW R&D |
| 21  | HW_SPARE_REC_HW_S<br>PARE_REC21 | R/W  | 0h    | Reserved for HW R&D |
| 20  | HW_SPARE_REC_HW_S<br>PARE_REC20 | R/W  | 0h    | Reserved for HW R&D |
| 19  | HW_SPARE_REC_HW_S<br>PARE_REC19 | R/W  | 0h    | Reserved for HW R&D |
| 18  | HW_SPARE_REC_HW_S<br>PARE_REC18 | R/W  | 0h    | Reserved for HW R&D |
| 17  | HW_SPARE_REC_HW_S<br>PARE_REC17 | R/W  | 0h    | Reserved for HW R&D |
| 16  | HW_SPARE_REC_HW_S<br>PARE_REC16 | R/W  | 0h    | Reserved for HW R&D |
| 15  | HW_SPARE_REC_HW_S<br>PARE_REC15 | R/W  | 0h    | Reserved for HW R&D |
| 14  | HW_SPARE_REC_HW_S<br>PARE_REC14 | R/W  | 0h    | Reserved for HW R&D |
| 13  | HW_SPARE_REC_HW_S<br>PARE_REC13 | R/W  | 0h    | Reserved for HW R&D |
| 12  | HW_SPARE_REC_HW_S<br>PARE_REC12 | R/W  | 0h    | Reserved for HW R&D |
| 11  | HW_SPARE_REC_HW_S<br>PARE_REC11 | R/W  | 0h    | Reserved for HW R&D |
| 10  | HW_SPARE_REC_HW_S<br>PARE_REC10 | R/W  | 0h    | Reserved for HW R&D |
| 9   | HW_SPARE_REC_HW_S<br>PARE_REC9  | R/W  | 0h    | Reserved for HW R&D |
| 8   | HW_SPARE_REC_HW_S<br>PARE_REC8  | R/W  | 0h    | Reserved for HW R&D |
| 7   | HW_SPARE_REC_HW_S<br>PARE_REC7  | R/W  | 0h    | Reserved for HW R&D |
| 6   | HW_SPARE_REC_HW_S<br>PARE_REC6  | R/W  | 0h    | Reserved for HW R&D |
| 5   | HW_SPARE_REC_HW_S<br>PARE_REC5  | R/W  | 0h    | Reserved for HW R&D |
| 4   | HW_SPARE_REC_HW_S<br>PARE_REC4  | R/W  | 0h    | Reserved for HW R&D |
| 3   | HW_SPARE_REC_HW_S<br>PARE_REC3  | R/W  | 0h    | Reserved for HW R&D |
| 2   | HW_SPARE_REC_HW_S<br>PARE_REC2  | R/W  | 0h    | Reserved for HW R&D |
| 1   | HW_SPARE_REC_HW_S<br>PARE_REC1  | R/W  | 0h    | Reserved for HW R&D |
| 0   | HW_SPARE_REC_HW_S<br>PARE_REC0  | R/W  | 0h    | Reserved for HW R&D |

### 2.5.2.79 MSS\_TOPRCM\_LOCK0\_KICK0 Register

#### 1 MSS\_TOPRCM\_LOCK0\_KICK0 Register (Offset = 1008h) [reset = 0h]

- KICK0 component.

Return to [Summary Table](#)

**Table 2-2331. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 1008h       |

**Figure 2-776. MSS\_TOPRCM\_LOCK0\_KICK0 Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| LOCK0_KICK0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LOCK0_KICK0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| LOCK0_KICK0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LOCK0_KICK0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 2-2333. MSS\_TOPRCM\_LOCK0\_KICK0 Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description       |
|------|-------------|------|-------|-------------------|
| 31:0 | LOCK0_KICK0 | R/W  | 0h    | - KICK0 component |

### 2.5.2.80 MSS\_TOPRCM\_LOCK0\_KICK1 Register

#### 1 MSS\_TOPRCM\_LOCK0\_KICK1 Register (Offset = 100Ch) [reset = 0h]

- KICK1 component.

Return to [Summary Table](#)

**Table 2-2334. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 100Ch       |

**Figure 2-777. MSS\_TOPRCM\_LOCK0\_KICK1 Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| LOCK0_KICK1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LOCK0_KICK1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| LOCK0_KICK1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LOCK0_KICK1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 2-2336. MSS\_TOPRCM\_LOCK0\_KICK1 Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description       |
|------|-------------|------|-------|-------------------|
| 31:0 | LOCK0_KICK1 | R/W  | 0h    | - KICK1 component |



### 2.5.2.81 MSS\_TOPRCM\_INTR\_RAW\_STATUS Register

#### 1 MSS\_TOPRCM\_INTR\_RAW\_STATUS Register (Offset = 1010h) [reset = 0h]

Interrupt Raw Status/Set Register.

Return to [Summary Table](#)

**Table 2-2337. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 1010h       |

**Figure 2-778. MSS\_TOPRCM\_INTR\_RAW\_STATUS Name Register**

|          |    |    |    |           |          |          |          |
|----------|----|----|----|-----------|----------|----------|----------|
| 31       | 30 | 29 | 28 | 27        | 26       | 25       | 24       |
| RESERVED |    |    |    |           |          |          |          |
| NONE     |    |    |    |           |          |          |          |
| 0h       |    |    |    |           |          |          |          |
| 23       | 22 | 21 | 20 | 19        | 18       | 17       | 16       |
| RESERVED |    |    |    |           |          |          |          |
| NONE     |    |    |    |           |          |          |          |
| 0h       |    |    |    |           |          |          |          |
| 15       | 14 | 13 | 12 | 11        | 10       | 9        | 8        |
| RESERVED |    |    |    |           |          |          |          |
| NONE     |    |    |    |           |          |          |          |
| 0h       |    |    |    |           |          |          |          |
| 7        | 6  | 5  | 4  | 3         | 2        | 1        | 0        |
| RESERVED |    |    |    | PROXY_ERR | KICK_ERR | ADDR_ERR | PROT_ERR |
| NONE     |    |    |    | R/W1TS    | R/W1TS   | R/W1TS   | R/W1TS   |
| 0h       |    |    |    | 0h        | 0h       | 0h       | 0h       |

**Table 2-2339. MSS\_TOPRCM\_INTR\_RAW\_STATUS Register Field Descriptions**

| Bit  | Field     | Type   | Reset | Description                                                                                                |
|------|-----------|--------|-------|------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED  | NONE   | 0h    | Reserved                                                                                                   |
| 3    | PROXY_ERR | R/W1TS | 0h    | Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. |
| 2    | KICK_ERR  | R/W1TS | 0h    | Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.   |
| 1    | ADDR_ERR  | R/W1TS | 0h    | Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.    |
| 0    | PROT_ERR  | R/W1TS | 0h    | Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.    |

## 2.5.2.82 MSS\_TOPRCM\_INTR\_ENABLED\_STATUS\_CLEAR Register

### 1 MSS\_TOPRCM\_INTR\_ENABLED\_STATUS\_CLEAR Register (Offset = 1014h) [reset = 0h]

Interrupt Enabled Status/Clear register.

Return to [Summary Table](#)

**Table 2-2340. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 1014h       |

**Figure 2-779. MSS\_TOPRCM\_INTR\_ENABLED\_STATUS\_CLEAR Name Register**

|          |    |    |    |                   |                  |                  |                  |
|----------|----|----|----|-------------------|------------------|------------------|------------------|
| 31       | 30 | 29 | 28 | 27                | 26               | 25               | 24               |
| RESERVED |    |    |    |                   |                  |                  |                  |
| NONE     |    |    |    |                   |                  |                  |                  |
| 0h       |    |    |    |                   |                  |                  |                  |
| 23       | 22 | 21 | 20 | 19                | 18               | 17               | 16               |
| RESERVED |    |    |    |                   |                  |                  |                  |
| NONE     |    |    |    |                   |                  |                  |                  |
| 0h       |    |    |    |                   |                  |                  |                  |
| 15       | 14 | 13 | 12 | 11                | 10               | 9                | 8                |
| RESERVED |    |    |    |                   |                  |                  |                  |
| NONE     |    |    |    |                   |                  |                  |                  |
| 0h       |    |    |    |                   |                  |                  |                  |
| 7        | 6  | 5  | 4  | 3                 | 2                | 1                | 0                |
| RESERVED |    |    |    | ENABLED_PROXY_ERR | ENABLED_KICK_ERR | ENABLED_ADDR_ERR | ENABLED_PROT_ERR |
| NONE     |    |    |    | R/W1TC            | R/W1TC           | R/W1TC           | R/W1TC           |
| 0h       |    |    |    | 0h                | 0h               | 0h               | 0h               |

**Table 2-2342. MSS\_TOPRCM\_INTR\_ENABLED\_STATUS\_CLEAR Register Field Descriptions**

| Bit  | Field             | Type   | Reset | Description                                                                                                      |
|------|-------------------|--------|-------|------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED          | NONE   | 0h    | Reserved                                                                                                         |
| 3    | ENABLED_PROXY_ERR | R/W1TC | 0h    | Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. |
| 2    | ENABLED_KICK_ERR  | R/W1TC | 0h    | Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.   |
| 1    | ENABLED_ADDR_ERR  | R/W1TC | 0h    | Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.    |
| 0    | ENABLED_PROT_ERR  | R/W1TC | 0h    | Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.    |

### 2.5.2.83 MSS\_TOPRCM\_INTR\_ENABLE Register

#### 1 MSS\_TOPRCM\_INTR\_ENABLE Register (Offset = 1018h) [reset = 0h]

Interrupt Enable register.

Return to [Summary Table](#)

**Table 2-2343. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 1018h       |

**Figure 2-780. MSS\_TOPRCM\_INTR\_ENABLE Name Register**

|          |    |    |    |              |             |             |             |
|----------|----|----|----|--------------|-------------|-------------|-------------|
| 31       | 30 | 29 | 28 | 27           | 26          | 25          | 24          |
| RESERVED |    |    |    |              |             |             |             |
| NONE     |    |    |    |              |             |             |             |
| 0h       |    |    |    |              |             |             |             |
| 23       | 22 | 21 | 20 | 19           | 18          | 17          | 16          |
| RESERVED |    |    |    |              |             |             |             |
| NONE     |    |    |    |              |             |             |             |
| 0h       |    |    |    |              |             |             |             |
| 15       | 14 | 13 | 12 | 11           | 10          | 9           | 8           |
| RESERVED |    |    |    |              |             |             |             |
| NONE     |    |    |    |              |             |             |             |
| 0h       |    |    |    |              |             |             |             |
| 7        | 6  | 5  | 4  | 3            | 2           | 1           | 0           |
| RESERVED |    |    |    | PROXY_ERR_EN | KICK_ERR_EN | ADDR_ERR_EN | PROT_ERR_EN |
| NONE     |    |    |    | R/W1TS       | R/W1TS      | R/W1TS      | R/W1TS      |
| 0h       |    |    |    | 0h           | 0h          | 0h          | 0h          |

**Table 2-2345. MSS\_TOPRCM\_INTR\_ENABLE Register Field Descriptions**

| Bit  | Field        | Type   | Reset | Description                                                                                   |
|------|--------------|--------|-------|-----------------------------------------------------------------------------------------------|
| 31:4 | RESERVED     | NONE   | 0h    | Reserved                                                                                      |
| 3    | PROXY_ERR_EN | R/W1TS | 0h    | Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. |
| 2    | KICK_ERR_EN  | R/W1TS | 0h    | Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.   |
| 1    | ADDR_ERR_EN  | R/W1TS | 0h    | Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.    |
| 0    | PROT_ERR_EN  | R/W1TS | 0h    | Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.    |

## 2.5.2.84 MSS\_TOPRCM\_INTR\_ENABLE\_CLEAR Register

### 1 MSS\_TOPRCM\_INTR\_ENABLE\_CLEAR Register (Offset = 101Ch) [reset = 0h]

Interrupt Enable Clear register.

Return to [Summary Table](#)

**Table 2-2346. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 101Ch       |

**Figure 2-781. MSS\_TOPRCM\_INTR\_ENABLE\_CLEAR Name Register**

|          |    |    |    |                  |                 |                 |                 |
|----------|----|----|----|------------------|-----------------|-----------------|-----------------|
| 31       | 30 | 29 | 28 | 27               | 26              | 25              | 24              |
| RESERVED |    |    |    |                  |                 |                 |                 |
| NONE     |    |    |    |                  |                 |                 |                 |
| 0h       |    |    |    |                  |                 |                 |                 |
| 23       | 22 | 21 | 20 | 19               | 18              | 17              | 16              |
| RESERVED |    |    |    |                  |                 |                 |                 |
| NONE     |    |    |    |                  |                 |                 |                 |
| 0h       |    |    |    |                  |                 |                 |                 |
| 15       | 14 | 13 | 12 | 11               | 10              | 9               | 8               |
| RESERVED |    |    |    |                  |                 |                 |                 |
| NONE     |    |    |    |                  |                 |                 |                 |
| 0h       |    |    |    |                  |                 |                 |                 |
| 7        | 6  | 5  | 4  | 3                | 2               | 1               | 0               |
| RESERVED |    |    |    | PROXY_ERR_EN_CLR | KICK_ERR_EN_CLR | ADDR_ERR_EN_CLR | PROT_ERR_EN_CLR |
| NONE     |    |    |    | R/W1TC           | R/W1TC          | R/W1TC          | R/W1TC          |
| 0h       |    |    |    | 0h               | 0h              | 0h              | 0h              |

**Table 2-2348. MSS\_TOPRCM\_INTR\_ENABLE\_CLEAR Register Field Descriptions**

| Bit  | Field            | Type   | Reset | Description                                                                                           |
|------|------------------|--------|-------|-------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED         | NONE   | 0h    | Reserved                                                                                              |
| 3    | PROXY_ERR_EN_CLR | R/W1TC | 0h    | Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. |
| 2    | KICK_ERR_EN_CLR  | R/W1TC | 0h    | Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.   |
| 1    | ADDR_ERR_EN_CLR  | R/W1TC | 0h    | Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.    |
| 0    | PROT_ERR_EN_CLR  | R/W1TC | 0h    | Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.    |

### 2.5.2.85 MSS\_TOPRCM\_EOI Register

#### 1 MSS\_TOPRCM\_EOI Register (Offset = 1020h) [reset = 0h]

EOI register.

Return to [Summary Table](#)

**Table 2-2349. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 1020h       |

**Figure 2-782. MSS\_TOPRCM\_EOI Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| EOI_VECTOR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 2-2351. MSS\_TOPRCM\_EOI Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                 |
|------|------------|------|-------|-----------------------------------------------------------------------------|
| 31:8 | RESERVED   | NONE | 0h    | Reserved                                                                    |
| 7:0  | EOI_VECTOR | R/W  | 0h    | EOI vector value. Write this with interrupt distribution value in the chip. |

## 2.5.2.86 MSS\_TOPRCM\_FAULT\_ADDRESS Register

### 1 MSS\_TOPRCM\_FAULT\_ADDRESS Register (Offset = 1024h) [reset = 0h]

Fault Address register.

Return to [Summary Table](#)

**Table 2-2352. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 1024h       |

**Figure 2-783. MSS\_TOPRCM\_FAULT\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 2-2354. MSS\_TOPRCM\_FAULT\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description    |
|------|------------|------|-------|----------------|
| 31:0 | FAULT_ADDR | R    | 0h    | Fault Address. |

### 2.5.2.87 MSS\_TOPRCM\_FAULT\_TYPE\_STATUS Register

#### 1 MSS\_TOPRCM\_FAULT\_TYPE\_STATUS Register (Offset = 1028h) [reset = 0h]

Fault Type Status register.

Return to [Summary Table](#)

**Table 2-2355. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 1028h       |

**Figure 2-784. MSS\_TOPRCM\_FAULT\_TYPE\_STATUS Name Register**

|          |          |            |    |    |    |    |    |
|----------|----------|------------|----|----|----|----|----|
| 31       | 30       | 29         | 28 | 27 | 26 | 25 | 24 |
| RESERVED |          |            |    |    |    |    |    |
| NONE     |          |            |    |    |    |    |    |
| 0h       |          |            |    |    |    |    |    |
| 23       | 22       | 21         | 20 | 19 | 18 | 17 | 16 |
| RESERVED |          |            |    |    |    |    |    |
| NONE     |          |            |    |    |    |    |    |
| 0h       |          |            |    |    |    |    |    |
| 15       | 14       | 13         | 12 | 11 | 10 | 9  | 8  |
| RESERVED |          |            |    |    |    |    |    |
| NONE     |          |            |    |    |    |    |    |
| 0h       |          |            |    |    |    |    |    |
| 7        | 6        | 5          | 4  | 3  | 2  | 1  | 0  |
| RESERVED | FAULT_NS | FAULT_TYPE |    |    |    |    |    |
| NONE     | R        | R          |    |    |    |    |    |
| 0h       | 0h       | 0h         |    |    |    |    |    |

**Table 2-2357. MSS\_TOPRCM\_FAULT\_TYPE\_STATUS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                         |
|------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                            |
| 6    | FAULT_NS   | R    | 0h    | Non-secure access.                                                                                                                                                                                                                                                                                                                                                                                  |
| 5:0  | FAULT_TYPE | R    | 0h    | Fault Type<br>10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1<br>01_0000 = Supervisor write fault - priv = 1 dir = 0<br>00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1<br>00_0100 = User read fault - priv = 0 dir = 1 dtype = 1<br>00_0010 = User write fault - priv = 0 dir = 0<br>00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1<br>00_0000 = No fault |

### 2.5.2.88 MSS\_TOPRCM\_FAULT\_ATTR\_STATUS Register

#### 1 MSS\_TOPRCM\_FAULT\_ATTR\_STATUS Register (Offset = 102Ch) [reset = 0h]

Fault Attribute Status register.

Return to [Summary Table](#)

**Table 2-2358. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 102Ch       |

**Figure 2-785. MSS\_TOPRCM\_FAULT\_ATTR\_STATUS Name Register**

|               |    |    |    |               |    |    |    |
|---------------|----|----|----|---------------|----|----|----|
| 31            | 30 | 29 | 28 | 27            | 26 | 25 | 24 |
| FAULT_XID     |    |    |    |               |    |    |    |
| R             |    |    |    |               |    |    |    |
| 0h            |    |    |    |               |    |    |    |
| 23            | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
| FAULT_XID     |    |    |    | FAULT_ROUTEID |    |    |    |
| R             |    |    |    | R             |    |    |    |
| 0h            |    |    |    | 0h            |    |    |    |
| 15            | 14 | 13 | 12 | 11            | 10 | 9  | 8  |
| FAULT_ROUTEID |    |    |    |               |    |    |    |
| R             |    |    |    |               |    |    |    |
| 0h            |    |    |    |               |    |    |    |
| 7             | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| FAULT_PRIVID  |    |    |    |               |    |    |    |
| R             |    |    |    |               |    |    |    |
| 0h            |    |    |    |               |    |    |    |

**Table 2-2360. MSS\_TOPRCM\_FAULT\_ATTR\_STATUS Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description   |
|-------|---------------|------|-------|---------------|
| 31:20 | FAULT_XID     | R    | 0h    | XID.          |
| 19:8  | FAULT_ROUTEID | R    | 0h    | Route ID.     |
| 7:0   | FAULT_PRIVID  | R    | 0h    | Privilege ID. |



### 2.5.2.89 MSS\_TOPRCM\_FAULT\_CLEAR Register

#### 1 MSS\_TOPRCM\_FAULT\_CLEAR Register (Offset = 1030h) [reset = 0h]

Fault Clear register.

Return to [Summary Table](#)

**Table 2-2361. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_TOPRCM    | 5320 1030h       |

**Figure 2-786. MSS\_TOPRCM\_FAULT\_CLEAR Name Register**

|          |    |    |    |    |    |    |           |
|----------|----|----|----|----|----|----|-----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24        |
| RESERVED |    |    |    |    |    |    |           |
| NONE     |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16        |
| RESERVED |    |    |    |    |    |    |           |
| NONE     |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8         |
| RESERVED |    |    |    |    |    |    |           |
| NONE     |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0         |
| RESERVED |    |    |    |    |    |    | FAULT_CLR |
| NONE     |    |    |    |    |    |    | W         |
| 0h       |    |    |    |    |    |    | 0h        |

**Table 2-2363. MSS\_TOPRCM\_FAULT\_CLEAR Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                   |
|------|-----------|------|-------|-------------------------------------------------------------------------------|
| 31:1 | RESERVED  | NONE | 0h    | Reserved                                                                      |
| 0    | FAULT_CLR | W    | 0h    | Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. |

## 2.6 MSS\_RCM

### MSS\_RCM

#### 2.6.1 MSS\_RCM Summaries

#### MSS\_RCM Summaries

**Table 2-2364. MSS\_RCM Registers, Base Address=5320 8000h, Length=4096**

| Offset | Length | Register Name                                      | MSS_RCM Physical Address |
|--------|--------|----------------------------------------------------|--------------------------|
| 10h    | 32     | <a href="#">MSS_RCM_R5SS0_RST_STATUS</a>           | 5320 8010h               |
| 14h    | 32     | <a href="#">MSS_RCM_R5SS0_RST_CAUSE_CLR</a>        | 5320 8014h               |
| 18h    | 32     | <a href="#">MSS_RCM_SYSRST_BY_DBG_RST0</a>         | 5320 8018h               |
| 1Ch    | 32     | <a href="#">MSS_RCM_RST_ASSERTDLY0</a>             | 5320 801Ch               |
| 20h    | 32     | <a href="#">MSS_RCM_RST2ASSERTDLY0</a>             | 5320 8020h               |
| 24h    | 32     | <a href="#">MSS_RCM_RST_WFICHECK0</a>              | 5320 8024h               |
| 30h    | 32     | <a href="#">MSS_RCM_R5SS1_RST_STATUS</a>           | 5320 8030h               |
| 34h    | 32     | <a href="#">MSS_RCM_R5SS1_RST_CAUSE_CLR</a>        | 5320 8034h               |
| 38h    | 32     | <a href="#">MSS_RCM_SYSRST_BY_DBG_RST1</a>         | 5320 8038h               |
| 3Ch    | 32     | <a href="#">MSS_RCM_RST_ASSERTDLY1</a>             | 5320 803Ch               |
| 40h    | 32     | <a href="#">MSS_RCM_RST2ASSERTDLY1</a>             | 5320 8040h               |
| 44h    | 32     | <a href="#">MSS_RCM_RST_WFICHECK1</a>              | 5320 8044h               |
| 100h   | 32     | <a href="#">MSS_RCM_MSS_MCAN0_CLK_SRC_SEL</a>      | 5320 8100h               |
| 104h   | 32     | <a href="#">MSS_RCM_MSS_MCAN1_CLK_SRC_SEL</a>      | 5320 8104h               |
| 108h   | 32     | <a href="#">MSS_RCM_MSS_MCAN2_CLK_SRC_SEL</a>      | 5320 8108h               |
| 10Ch   | 32     | <a href="#">MSS_RCM_MSS_MCAN3_CLK_SRC_SEL</a>      | 5320 810Ch               |
| 110h   | 32     | <a href="#">MSS_RCM_MSS_QSPI_CLK_SRC_SEL</a>       | 5320 8110h               |
| 114h   | 32     | <a href="#">MSS_RCM_MSS_RTIO_CLK_SRC_SEL</a>       | 5320 8114h               |
| 118h   | 32     | <a href="#">MSS_RCM_MSS_RTII_CLK_SRC_SEL</a>       | 5320 8118h               |
| 11Ch   | 32     | <a href="#">MSS_RCM_MSS_RTII2_CLK_SRC_SEL</a>      | 5320 811Ch               |
| 120h   | 32     | <a href="#">MSS_RCM_MSS_RTII3_CLK_SRC_SEL</a>      | 5320 8120h               |
| 128h   | 32     | <a href="#">MSS_RCM_MSS_WDT0_CLK_SRC_SEL</a>       | 5320 8128h               |
| 12Ch   | 32     | <a href="#">MSS_RCM_MSS_WDT1_CLK_SRC_SEL</a>       | 5320 812Ch               |
| 130h   | 32     | <a href="#">MSS_RCM_MSS_WDT2_CLK_SRC_SEL</a>       | 5320 8130h               |
| 134h   | 32     | <a href="#">MSS_RCM_MSS_WDT3_CLK_SRC_SEL</a>       | 5320 8134h               |
| 13Ch   | 32     | <a href="#">MSS_RCM_MSS_SPI0_CLK_SRC_SEL</a>       | 5320 813Ch               |
| 140h   | 32     | <a href="#">MSS_RCM_MSS_SPI1_CLK_SRC_SEL</a>       | 5320 8140h               |
| 144h   | 32     | <a href="#">MSS_RCM_MSS_SPI2_CLK_SRC_SEL</a>       | 5320 8144h               |
| 148h   | 32     | <a href="#">MSS_RCM_MSS_SPI3_CLK_SRC_SEL</a>       | 5320 8148h               |
| 14Ch   | 32     | <a href="#">MSS_RCM_MSS_SPI4_CLK_SRC_SEL</a>       | 5320 814Ch               |
| 150h   | 32     | <a href="#">MSS_RCM_MSS_MMCSD_CLK_SRC_SEL</a>      | 5320 8150h               |
| 154h   | 32     | <a href="#">MSS_RCM_PRU_ICSS_UCLK_CLK_SRC_SEL</a>  | 5320 8154h               |
| 158h   | 32     | <a href="#">MSS_RCM_MSS_CPTS_CLK_SRC_SEL</a>       | 5320 8158h               |
| 15Ch   | 32     | <a href="#">MSS_RCM_GPMC_CLK_SRC_SEL</a>           | 5320 815Ch               |
| 160h   | 32     | <a href="#">MSS_RCM_CONTROLSS_PLL_CLK_SRC_SEL</a>  | 5320 8160h               |
| 164h   | 32     | <a href="#">MSS_RCM_MSS_I2C_CLK_SRC_SEL</a>        | 5320 8164h               |
| 174h   | 32     | <a href="#">MSS_RCM_MSS_LIN0_UART0_CLK_SRC_SEL</a> | 5320 8174h               |
| 178h   | 32     | <a href="#">MSS_RCM_MSS_LIN1_UART1_CLK_SRC_SEL</a> | 5320 8178h               |

**Table 2-2364. MSS\_RCM Registers, Base Address=5320 8000h, Length=4096 (continued)**

| Offset | Length | Register Name                                          | MSS_RCM Physical Address |
|--------|--------|--------------------------------------------------------|--------------------------|
| 17Ch   | 32     | <a href="#">MSS_RCM_MSS_LIN2_UART2_CLK_SRC_SEL</a>     | 5320 817Ch               |
| 180h   | 32     | <a href="#">MSS_RCM_MSS_LIN3_UART3_CLK_SRC_SEL</a>     | 5320 8180h               |
| 184h   | 32     | <a href="#">MSS_RCM_MSS_LIN4_UART4_CLK_SRC_SEL</a>     | 5320 8184h               |
| 188h   | 32     | <a href="#">MSS_RCM_MSS_LIN5_UART5_CLK_SRC_SEL</a>     | 5320 8188h               |
| 200h   | 32     | <a href="#">MSS_RCM_MSS_MCAN0_CLK_DIV_VAL</a>          | 5320 8200h               |
| 204h   | 32     | <a href="#">MSS_RCM_MSS_MCAN1_CLK_DIV_VAL</a>          | 5320 8204h               |
| 208h   | 32     | <a href="#">MSS_RCM_MSS_MCAN2_CLK_DIV_VAL</a>          | 5320 8208h               |
| 20Ch   | 32     | <a href="#">MSS_RCM_MSS_MCAN3_CLK_DIV_VAL</a>          | 5320 820Ch               |
| 210h   | 32     | <a href="#">MSS_RCM_MSS_QSPI_CLK_DIV_VAL</a>           | 5320 8210h               |
| 214h   | 32     | <a href="#">MSS_RCM_MSS_RTIO_CLK_DIV_VAL</a>           | 5320 8214h               |
| 218h   | 32     | <a href="#">MSS_RCM_MSS_RTII_CLK_DIV_VAL</a>           | 5320 8218h               |
| 21Ch   | 32     | <a href="#">MSS_RCM_MSS_RTII2_CLK_DIV_VAL</a>          | 5320 821Ch               |
| 220h   | 32     | <a href="#">MSS_RCM_MSS_RTII3_CLK_DIV_VAL</a>          | 5320 8220h               |
| 228h   | 32     | <a href="#">MSS_RCM_MSS_WDT0_CLK_DIV_VAL</a>           | 5320 8228h               |
| 22Ch   | 32     | <a href="#">MSS_RCM_MSS_WDT1_CLK_DIV_VAL</a>           | 5320 822Ch               |
| 230h   | 32     | <a href="#">MSS_RCM_MSS_WDT2_CLK_DIV_VAL</a>           | 5320 8230h               |
| 234h   | 32     | <a href="#">MSS_RCM_MSS_WDT3_CLK_DIV_VAL</a>           | 5320 8234h               |
| 23Ch   | 32     | <a href="#">MSS_RCM_MSS_SPI0_CLK_DIV_VAL</a>           | 5320 823Ch               |
| 240h   | 32     | <a href="#">MSS_RCM_MSS_SPI1_CLK_DIV_VAL</a>           | 5320 8240h               |
| 244h   | 32     | <a href="#">MSS_RCM_MSS_SPI2_CLK_DIV_VAL</a>           | 5320 8244h               |
| 248h   | 32     | <a href="#">MSS_RCM_MSS_SPI3_CLK_DIV_VAL</a>           | 5320 8248h               |
| 24Ch   | 32     | <a href="#">MSS_RCM_MSS_SPI4_CLK_DIV_VAL</a>           | 5320 824Ch               |
| 250h   | 32     | <a href="#">MSS_RCM_MSS_MMCSO_CLK_DIV_VAL</a>          | 5320 8250h               |
| 254h   | 32     | <a href="#">MSS_RCM_PRU_ICSS_UCLK_CLK_DIV_VAL</a>      | 5320 8254h               |
| 258h   | 32     | <a href="#">MSS_RCM_MSS_CPTS_CLK_DIV_VAL</a>           | 5320 8258h               |
| 25Ch   | 32     | <a href="#">MSS_RCM_GPMC_CLK_DIV_VAL</a>               | 5320 825Ch               |
| 260h   | 32     | <a href="#">MSS_RCM_CONTROLSS_PLL_CLK_DIV_VAL</a>      | 5320 8260h               |
| 264h   | 32     | <a href="#">MSS_RCM_MSS_I2C_CLK_DIV_VAL</a>            | 5320 8264h               |
| 274h   | 32     | <a href="#">MSS_RCM_MSS_LIN0_UART0_CLK_DIV_VAL</a>     | 5320 8274h               |
| 278h   | 32     | <a href="#">MSS_RCM_MSS_LIN1_UART1_CLK_DIV_VAL</a>     | 5320 8278h               |
| 27Ch   | 32     | <a href="#">MSS_RCM_MSS_LIN2_UART2_CLK_DIV_VAL</a>     | 5320 827Ch               |
| 280h   | 32     | <a href="#">MSS_RCM_MSS_LIN3_UART3_CLK_DIV_VAL</a>     | 5320 8280h               |
| 284h   | 32     | <a href="#">MSS_RCM_MSS_LIN4_UART4_CLK_DIV_VAL</a>     | 5320 8284h               |
| 288h   | 32     | <a href="#">MSS_RCM_MSS_LIN5_UART5_CLK_DIV_VAL</a>     | 5320 8288h               |
| 28Ch   | 32     | <a href="#">MSS_RCM_MSS_RGMII_CLK_DIV_VAL</a>          | 5320 828Ch               |
| 290h   | 32     | <a href="#">MSS_RCM_MSS_MII100_CLK_DIV_VAL</a>         | 5320 8290h               |
| 294h   | 32     | <a href="#">MSS_RCM_MSS_MII10_CLK_DIV_VAL</a>          | 5320 8294h               |
| 298h   | 32     | <a href="#">MSS_RCM_MSS_XTAL_32K_CLK_DIV_VAL</a>       | 5320 8298h               |
| 29Ch   | 32     | <a href="#">MSS_RCM_XTAL_TEMPSENSE_32K_CLK_DIV_VAL</a> | 5320 829Ch               |
| 2A0h   | 32     | <a href="#">MSS_RCM_MSS_ELM_CLK_DIV_VAL</a>            | 5320 82A0h               |
| 300h   | 32     | <a href="#">MSS_RCM_MSS_MCAN0_CLK_GATE</a>             | 5320 8300h               |
| 304h   | 32     | <a href="#">MSS_RCM_MSS_MCAN1_CLK_GATE</a>             | 5320 8304h               |
| 308h   | 32     | <a href="#">MSS_RCM_MSS_MCAN2_CLK_GATE</a>             | 5320 8308h               |
| 30Ch   | 32     | <a href="#">MSS_RCM_MSS_MCAN3_CLK_GATE</a>             | 5320 830Ch               |
| 310h   | 32     | <a href="#">MSS_RCM_MSS_QSPI_CLK_GATE</a>              | 5320 8310h               |

**Table 2-2364. MSS\_RCM Registers, Base Address=5320 8000h, Length=4096 (continued)**

| Offset | Length | Register Name                                      | MSS_RCM Physical Address |
|--------|--------|----------------------------------------------------|--------------------------|
| 314h   | 32     | <a href="#">MSS_RCM_MSS_RTIO_CLK_GATE</a>          | 5320 8314h               |
| 318h   | 32     | <a href="#">MSS_RCM_MSS_RT11_CLK_GATE</a>          | 5320 8318h               |
| 31Ch   | 32     | <a href="#">MSS_RCM_MSS_RT12_CLK_GATE</a>          | 5320 831Ch               |
| 320h   | 32     | <a href="#">MSS_RCM_MSS_RT13_CLK_GATE</a>          | 5320 8320h               |
| 328h   | 32     | <a href="#">MSS_RCM_MSS_WDT0_CLK_GATE</a>          | 5320 8328h               |
| 32Ch   | 32     | <a href="#">MSS_RCM_MSS_WDT1_CLK_GATE</a>          | 5320 832Ch               |
| 330h   | 32     | <a href="#">MSS_RCM_MSS_WDT2_CLK_GATE</a>          | 5320 8330h               |
| 334h   | 32     | <a href="#">MSS_RCM_MSS_WDT3_CLK_GATE</a>          | 5320 8334h               |
| 33Ch   | 32     | <a href="#">MSS_RCM_MSS_SPI0_CLK_GATE</a>          | 5320 833Ch               |
| 340h   | 32     | <a href="#">MSS_RCM_MSS_SPI1_CLK_GATE</a>          | 5320 8340h               |
| 344h   | 32     | <a href="#">MSS_RCM_MSS_SPI2_CLK_GATE</a>          | 5320 8344h               |
| 348h   | 32     | <a href="#">MSS_RCM_MSS_SPI3_CLK_GATE</a>          | 5320 8348h               |
| 34Ch   | 32     | <a href="#">MSS_RCM_MSS_SPI4_CLK_GATE</a>          | 5320 834Ch               |
| 350h   | 32     | <a href="#">MSS_RCM_MSS_MMCSO_CLK_GATE</a>         | 5320 8350h               |
| 354h   | 32     | <a href="#">MSS_RCM_PRU_ICSS_UCLK_CLK_GATE</a>     | 5320 8354h               |
| 358h   | 32     | <a href="#">MSS_RCM_MSS_CPTS_CLK_GATE</a>          | 5320 8358h               |
| 35Ch   | 32     | <a href="#">MSS_RCM_GPMC_CLK_GATE</a>              | 5320 835Ch               |
| 360h   | 32     | <a href="#">MSS_RCM_CONTROLSS_PLL_CLK_GATE</a>     | 5320 8360h               |
| 364h   | 32     | <a href="#">MSS_RCM_MSS_I2C0_CLK_GATE</a>          | 5320 8364h               |
| 368h   | 32     | <a href="#">MSS_RCM_MSS_I2C1_CLK_GATE</a>          | 5320 8368h               |
| 36Ch   | 32     | <a href="#">MSS_RCM_MSS_I2C2_CLK_GATE</a>          | 5320 836Ch               |
| 370h   | 32     | <a href="#">MSS_RCM_MSS_I2C3_CLK_GATE</a>          | 5320 8370h               |
| 374h   | 32     | <a href="#">MSS_RCM_MSS_LIN0_CLK_GATE</a>          | 5320 8374h               |
| 378h   | 32     | <a href="#">MSS_RCM_MSS_LIN1_CLK_GATE</a>          | 5320 8378h               |
| 37Ch   | 32     | <a href="#">MSS_RCM_MSS_LIN2_CLK_GATE</a>          | 5320 837Ch               |
| 380h   | 32     | <a href="#">MSS_RCM_MSS_LIN3_CLK_GATE</a>          | 5320 8380h               |
| 384h   | 32     | <a href="#">MSS_RCM_MSS_LIN4_CLK_GATE</a>          | 5320 8384h               |
| 38Ch   | 32     | <a href="#">MSS_RCM_MSS_UART0_CLK_GATE</a>         | 5320 838Ch               |
| 390h   | 32     | <a href="#">MSS_RCM_MSS_UART1_CLK_GATE</a>         | 5320 8390h               |
| 394h   | 32     | <a href="#">MSS_RCM_MSS_UART2_CLK_GATE</a>         | 5320 8394h               |
| 398h   | 32     | <a href="#">MSS_RCM_MSS_UART3_CLK_GATE</a>         | 5320 8398h               |
| 39Ch   | 32     | <a href="#">MSS_RCM_MSS_UART4_CLK_GATE</a>         | 5320 839Ch               |
| 3A0h   | 32     | <a href="#">MSS_RCM_MSS_UART5_CLK_GATE</a>         | 5320 83A0h               |
| 3A4h   | 32     | <a href="#">MSS_RCM_MSS_RGMII_CLK_GATE</a>         | 5320 83A4h               |
| 3A8h   | 32     | <a href="#">MSS_RCM_MSS_MII100_CLK_GATE</a>        | 5320 83A8h               |
| 3ACh   | 32     | <a href="#">MSS_RCM_MSS_MII10_CLK_GATE</a>         | 5320 83ACh               |
| 3B0h   | 32     | <a href="#">MSS_RCM_MSS_MMCSO_32K_CLK_GATE</a>     | 5320 83B0h               |
| 3B4h   | 32     | <a href="#">MSS_RCM_MSS_TEMPSENSE_32K_CLK_GATE</a> | 5320 83B4h               |
| 3B8h   | 32     | <a href="#">MSS_RCM_MSS_CPSW_CLK_GATE</a>          | 5320 83B8h               |
| 3BCh   | 32     | <a href="#">MSS_RCM_MSS_PRU_ICSS_IEP_CLK_GATE</a>  | 5320 83BCh               |
| 3C0h   | 32     | <a href="#">MSS_RCM_MSS_PRU_ICSS_CORE_CLK_GATE</a> | 5320 83C0h               |
| 3C4h   | 32     | <a href="#">MSS_RCM_MSS_PRU_ICSS_SYS_CLK_GATE</a>  | 5320 83C4h               |
| 3C8h   | 32     | <a href="#">MSS_RCM_MSS_ELM_CLK_GATE</a>           | 5320 83C8h               |
| 3CCh   | 32     | <a href="#">MSS_RCM_R5_CORE0_GATE0</a>             | 5320 83CCh               |
| 3D0h   | 32     | <a href="#">MSS_RCM_R5_CORE0_GATE1</a>             | 5320 83D0h               |

**Table 2-2364. MSS\_RCM Registers, Base Address=5320 8000h, Length=4096 (continued)**

| Offset | Length | Register Name                                     | MSS_RCM Physical Address |
|--------|--------|---------------------------------------------------|--------------------------|
| 3D4h   | 32     | <a href="#">MSS_RCM_R5_CORE1_GATE0</a>            | 5320 83D4h               |
| 3D8h   | 32     | <a href="#">MSS_RCM_R5_CORE1_GATE1</a>            | 5320 83D8h               |
| 400h   | 32     | <a href="#">MSS_RCM_MSS_MCAN0_CLK_STATUS</a>      | 5320 8400h               |
| 404h   | 32     | <a href="#">MSS_RCM_MSS_MCAN1_CLK_STATUS</a>      | 5320 8404h               |
| 408h   | 32     | <a href="#">MSS_RCM_MSS_MCAN2_CLK_STATUS</a>      | 5320 8408h               |
| 40Ch   | 32     | <a href="#">MSS_RCM_MSS_MCAN3_CLK_STATUS</a>      | 5320 840Ch               |
| 410h   | 32     | <a href="#">MSS_RCM_MSS_QSPI_CLK_STATUS</a>       | 5320 8410h               |
| 414h   | 32     | <a href="#">MSS_RCM_MSS_RTIO_CLK_STATUS</a>       | 5320 8414h               |
| 418h   | 32     | <a href="#">MSS_RCM_MSS_RTII_CLK_STATUS</a>       | 5320 8418h               |
| 41Ch   | 32     | <a href="#">MSS_RCM_MSS_RTII2_CLK_STATUS</a>      | 5320 841Ch               |
| 420h   | 32     | <a href="#">MSS_RCM_MSS_RTII3_CLK_STATUS</a>      | 5320 8420h               |
| 428h   | 32     | <a href="#">MSS_RCM_MSS_WDT0_CLK_STATUS</a>       | 5320 8428h               |
| 42Ch   | 32     | <a href="#">MSS_RCM_MSS_WDT1_CLK_STATUS</a>       | 5320 842Ch               |
| 430h   | 32     | <a href="#">MSS_RCM_MSS_WDT2_CLK_STATUS</a>       | 5320 8430h               |
| 434h   | 32     | <a href="#">MSS_RCM_MSS_WDT3_CLK_STATUS</a>       | 5320 8434h               |
| 43Ch   | 32     | <a href="#">MSS_RCM_MSS_SPI0_CLK_STATUS</a>       | 5320 843Ch               |
| 440h   | 32     | <a href="#">MSS_RCM_MSS_SPI1_CLK_STATUS</a>       | 5320 8440h               |
| 444h   | 32     | <a href="#">MSS_RCM_MSS_SPI2_CLK_STATUS</a>       | 5320 8444h               |
| 448h   | 32     | <a href="#">MSS_RCM_MSS_SPI3_CLK_STATUS</a>       | 5320 8448h               |
| 44Ch   | 32     | <a href="#">MSS_RCM_MSS_SPI4_CLK_STATUS</a>       | 5320 844Ch               |
| 450h   | 32     | <a href="#">MSS_RCM_MSS_MMCS0_CLK_STATUS</a>      | 5320 8450h               |
| 454h   | 32     | <a href="#">MSS_RCM_PRU_ICSS_UCLK_CLK_STATUS</a>  | 5320 8454h               |
| 458h   | 32     | <a href="#">MSS_RCM_MSS_CPTS_CLK_STATUS</a>       | 5320 8458h               |
| 45Ch   | 32     | <a href="#">MSS_RCM_GPMC_CLK_STATUS</a>           | 5320 845Ch               |
| 460h   | 32     | <a href="#">MSS_RCM_CONTROLSS_PLL_CLK_STATUS</a>  | 5320 8460h               |
| 464h   | 32     | <a href="#">MSS_RCM_MSS_I2C_CLK_STATUS</a>        | 5320 8464h               |
| 474h   | 32     | <a href="#">MSS_RCM_MSS_LIN0_UART0_CLK_STATUS</a> | 5320 8474h               |
| 478h   | 32     | <a href="#">MSS_RCM_MSS_LIN1_UART1_CLK_STATUS</a> | 5320 8478h               |
| 47Ch   | 32     | <a href="#">MSS_RCM_MSS_LIN2_UART2_CLK_STATUS</a> | 5320 847Ch               |
| 480h   | 32     | <a href="#">MSS_RCM_MSS_LIN3_UART3_CLK_STATUS</a> | 5320 8480h               |
| 484h   | 32     | <a href="#">MSS_RCM_MSS_LIN4_UART4_CLK_STATUS</a> | 5320 8484h               |
| 488h   | 32     | <a href="#">MSS_RCM_MSS_LIN5_UART5_CLK_STATUS</a> | 5320 8488h               |
| 48Ch   | 32     | <a href="#">MSS_RCM_MSS_RGMII_CLK_STATUS</a>      | 5320 848Ch               |
| 490h   | 32     | <a href="#">MSS_RCM_MSS_MII100_CLK_STATUS</a>     | 5320 8490h               |
| 494h   | 32     | <a href="#">MSS_RCM_MSS_MII10_CLK_STATUS</a>      | 5320 8494h               |
| 49Ch   | 32     | <a href="#">MSS_RCM_MMC0_32K_CLK_STATUS</a>       | 5320 849Ch               |
| 4A0h   | 32     | <a href="#">MSS_RCM_TEMPSENSE_32K_CLK_STATUS</a>  | 5320 84A0h               |
| 4A4h   | 32     | <a href="#">MSS_RCM_MSS_ELM_CLK_STATUS</a>        | 5320 84A4h               |
| 500h   | 32     | <a href="#">MSS_RCM_MSS_R5SS0_POR_RST_CTRL0</a>   | 5320 8500h               |
| 504h   | 32     | <a href="#">MSS_RCM_MSS_R5SS0_POR_RST_CTRL1</a>   | 5320 8504h               |
| 508h   | 32     | <a href="#">MSS_RCM_MSS_CR5SSA_RST_CTRL0</a>      | 5320 8508h               |
| 50Ch   | 32     | <a href="#">MSS_RCM_MSS_CR5SSA_RST_CTRL1</a>      | 5320 850Ch               |
| 510h   | 32     | <a href="#">MSS_RCM_MSS_CR5SSB_RST_CTRL0</a>      | 5320 8510h               |
| 514h   | 32     | <a href="#">MSS_RCM_MSS_CR5SSB_RST_CTRL1</a>      | 5320 8514h               |
| 518h   | 32     | <a href="#">MSS_RCM_MSS_R5SS0_CORE0_RST_CTRL0</a> | 5320 8518h               |

**Table 2-2364. MSS\_RCM Registers, Base Address=5320 8000h, Length=4096 (continued)**

| Offset | Length | Register Name                                     | MSS_RCM Physical Address |
|--------|--------|---------------------------------------------------|--------------------------|
| 51Ch   | 32     | <a href="#">MSS_RCM_MSS_R5SS0_CORE0_RST_CTRL1</a> | 5320 851Ch               |
| 520h   | 32     | <a href="#">MSS_RCM_MSS_R5SS0_CORE1_RST_CTRL0</a> | 5320 8520h               |
| 524h   | 32     | <a href="#">MSS_RCM_MSS_R5SS0_CORE1_RST_CTRL1</a> | 5320 8524h               |
| 528h   | 32     | <a href="#">MSS_RCM_MSS_VIMA_RST_CTRL0</a>        | 5320 8528h               |
| 52Ch   | 32     | <a href="#">MSS_RCM_MSS_VIMA_RST_CTRL1</a>        | 5320 852Ch               |
| 530h   | 32     | <a href="#">MSS_RCM_MSS_VIMB_RST_CTRL0</a>        | 5320 8530h               |
| 534h   | 32     | <a href="#">MSS_RCM_MSS_VIMB_RST_CTRL1</a>        | 5320 8534h               |
| 538h   | 32     | <a href="#">MSS_RCM_MSS_CRC_RST_CTRL</a>          | 5320 8538h               |
| 53Ch   | 32     | <a href="#">MSS_RCM_MSS_RTIO_RST_CTRL</a>         | 5320 853Ch               |
| 540h   | 32     | <a href="#">MSS_RCM_MSS_RTII_RST_CTRL</a>         | 5320 8540h               |
| 544h   | 32     | <a href="#">MSS_RCM_MSS_RTII_RST_CTRL</a>         | 5320 8544h               |
| 548h   | 32     | <a href="#">MSS_RCM_MSS_RTII_RST_CTRL</a>         | 5320 8548h               |
| 54Ch   | 32     | <a href="#">MSS_RCM_MSS_WDT0_RST_CTRL</a>         | 5320 854Ch               |
| 550h   | 32     | <a href="#">MSS_RCM_MSS_WDT1_RST_CTRL</a>         | 5320 8550h               |
| 554h   | 32     | <a href="#">MSS_RCM_MSS_WDT2_RST_CTRL</a>         | 5320 8554h               |
| 558h   | 32     | <a href="#">MSS_RCM_MSS_WDT3_RST_CTRL</a>         | 5320 8558h               |
| 55Ch   | 32     | <a href="#">MSS_RCM_MSS_ESM_RST_CTRL</a>          | 5320 855Ch               |
| 560h   | 32     | <a href="#">MSS_RCM_MSS_DCC0_RST_CTRL</a>         | 5320 8560h               |
| 564h   | 32     | <a href="#">MSS_RCM_MSS_DCC1_RST_CTRL</a>         | 5320 8564h               |
| 568h   | 32     | <a href="#">MSS_RCM_MSS_DCC2_RST_CTRL</a>         | 5320 8568h               |
| 56Ch   | 32     | <a href="#">MSS_RCM_MSS_DCC3_RST_CTRL</a>         | 5320 856Ch               |
| 570h   | 32     | <a href="#">MSS_RCM_MSS_SPI0_RST_CTRL</a>         | 5320 8570h               |
| 574h   | 32     | <a href="#">MSS_RCM_MSS_SPI1_RST_CTRL</a>         | 5320 8574h               |
| 578h   | 32     | <a href="#">MSS_RCM_MSS_SPI2_RST_CTRL</a>         | 5320 8578h               |
| 57Ch   | 32     | <a href="#">MSS_RCM_MSS_SPI3_RST_CTRL</a>         | 5320 857Ch               |
| 580h   | 32     | <a href="#">MSS_RCM_MSS_SPI4_RST_CTRL</a>         | 5320 8580h               |
| 584h   | 32     | <a href="#">MSS_RCM_MSS_QSPI_RST_CTRL</a>         | 5320 8584h               |
| 588h   | 32     | <a href="#">MSS_RCM_MSS_MCAN0_RST_CTRL</a>        | 5320 8588h               |
| 58Ch   | 32     | <a href="#">MSS_RCM_MSS_MCAN1_RST_CTRL</a>        | 5320 858Ch               |
| 590h   | 32     | <a href="#">MSS_RCM_MSS_MCAN2_RST_CTRL</a>        | 5320 8590h               |
| 594h   | 32     | <a href="#">MSS_RCM_MSS_MCAN3_RST_CTRL</a>        | 5320 8594h               |
| 598h   | 32     | <a href="#">MSS_RCM_MSS_I2C0_RST_CTRL</a>         | 5320 8598h               |
| 59Ch   | 32     | <a href="#">MSS_RCM_MSS_I2C1_RST_CTRL</a>         | 5320 859Ch               |
| 5A0h   | 32     | <a href="#">MSS_RCM_MSS_I2C2_RST_CTRL</a>         | 5320 85A0h               |
| 5A4h   | 32     | <a href="#">MSS_RCM_MSS_I2C3_RST_CTRL</a>         | 5320 85A4h               |
| 5A8h   | 32     | <a href="#">MSS_RCM_MSS_UART0_RST_CTRL</a>        | 5320 85A8h               |
| 5ACh   | 32     | <a href="#">MSS_RCM_MSS_UART1_RST_CTRL</a>        | 5320 85ACh               |
| 5B0h   | 32     | <a href="#">MSS_RCM_MSS_UART2_RST_CTRL</a>        | 5320 85B0h               |
| 5B4h   | 32     | <a href="#">MSS_RCM_MSS_UART3_RST_CTRL</a>        | 5320 85B4h               |
| 5B8h   | 32     | <a href="#">MSS_RCM_MSS_UART4_RST_CTRL</a>        | 5320 85B8h               |
| 5BCh   | 32     | <a href="#">MSS_RCM_MSS_UART5_RST_CTRL</a>        | 5320 85BCh               |
| 5C0h   | 32     | <a href="#">MSS_RCM_MSS_LIN0_RST_CTRL</a>         | 5320 85C0h               |
| 5C4h   | 32     | <a href="#">MSS_RCM_MSS_LIN1_RST_CTRL</a>         | 5320 85C4h               |
| 5C8h   | 32     | <a href="#">MSS_RCM_MSS_LIN2_RST_CTRL</a>         | 5320 85C8h               |
| 5CCh   | 32     | <a href="#">MSS_RCM_MSS_LIN3_RST_CTRL</a>         | 5320 85CCh               |

**Table 2-2364. MSS\_RCM Registers, Base Address=5320 8000h, Length=4096 (continued)**

| Offset | Length | Register Name                                       | MSS_RCM Physical Address |
|--------|--------|-----------------------------------------------------|--------------------------|
| 5D0h   | 32     | <a href="#">MSS_RCM_MSS_LIN4_RST_CTRL</a>           | 5320 85D0h               |
| 5D8h   | 32     | <a href="#">MSS_RCM_MSS_EDMA_RST_CTRL</a>           | 5320 85D8h               |
| 5DCh   | 32     | <a href="#">MSS_RCM_MSS_INFRA_RST_CTRL</a>          | 5320 85DCh               |
| 5E0h   | 32     | <a href="#">MSS_RCM_MSS_CPSW_RST_CTRL</a>           | 5320 85E0h               |
| 5E4h   | 32     | <a href="#">MSS_RCM_MSS_PRU_ICSS_RST_CTRL</a>       | 5320 85E4h               |
| 5E8h   | 32     | <a href="#">MSS_RCM_MSS_MMCSDB_RST_CTRL</a>         | 5320 85E8h               |
| 5ECh   | 32     | <a href="#">MSS_RCM_MSS_GPIO0_RST_CTRL</a>          | 5320 85ECh               |
| 5F0h   | 32     | <a href="#">MSS_RCM_MSS_GPIO1_RST_CTRL</a>          | 5320 85F0h               |
| 5F4h   | 32     | <a href="#">MSS_RCM_MSS_GPIO2_RST_CTRL</a>          | 5320 85F4h               |
| 5F8h   | 32     | <a href="#">MSS_RCM_MSS_GPIO3_RST_CTRL</a>          | 5320 85F8h               |
| 5FCh   | 32     | <a href="#">MSS_RCM_MSS_SPINLOCK_RST_CTRL</a>       | 5320 85FCh               |
| 600h   | 32     | <a href="#">MSS_RCM_GPMC_RST_CTRL</a>               | 5320 8600h               |
| 604h   | 32     | <a href="#">MSS_RCM_TEMPSENSE_32K_RST_CTRL</a>      | 5320 8604h               |
| 608h   | 32     | <a href="#">MSS_RCM_MSS_ELM_RST_CTRL</a>            | 5320 8608h               |
| 700h   | 32     | <a href="#">MSS_RCM_MSS_L2OCRAM_BANK0_PD_CTRL</a>   | 5320 8700h               |
| 704h   | 32     | <a href="#">MSS_RCM_MSS_L2OCRAM_BANK1_PD_CTRL</a>   | 5320 8704h               |
| 708h   | 32     | <a href="#">MSS_RCM_MSS_L2OCRAM_BANK2_PD_CTRL</a>   | 5320 8708h               |
| 70Ch   | 32     | <a href="#">MSS_RCM_MSS_L2_BANKD_PD_CTRL</a>        | 5320 870Ch               |
| 710h   | 32     | <a href="#">MSS_RCM_MSS_L2OCRAM_BANK0_PD_STATUS</a> | 5320 8710h               |
| 714h   | 32     | <a href="#">MSS_RCM_MSS_L2OCRAM_BANK1_PD_STATUS</a> | 5320 8714h               |
| 718h   | 32     | <a href="#">MSS_RCM_MSS_L2OCRAM_BANK2_PD_STATUS</a> | 5320 8718h               |
| 71Ch   | 32     | <a href="#">MSS_RCM_MSS_L2_BANKD_PD_STATUS</a>      | 5320 871Ch               |
| 800h   | 32     | <a href="#">MSS_RCM_HSM_RTIA_CLK_SRC_SEL</a>        | 5320 8800h               |
| 804h   | 32     | <a href="#">MSS_RCM_HSM_WDT_CLK_SRC_SEL</a>         | 5320 8804h               |
| 808h   | 32     | <a href="#">MSS_RCM_HSM_RTC_CLK_SRC_SEL</a>         | 5320 8808h               |
| 80Ch   | 32     | <a href="#">MSS_RCM_HSM_DMTA_CLK_SRC_SEL</a>        | 5320 880Ch               |
| 810h   | 32     | <a href="#">MSS_RCM_HSM_DMTB_CLK_SRC_SEL</a>        | 5320 8810h               |
| 814h   | 32     | <a href="#">MSS_RCM_HSM_RTI_CLK_DIV_VAL</a>         | 5320 8814h               |
| 818h   | 32     | <a href="#">MSS_RCM_HSM_WDT_CLK_DIV_VAL</a>         | 5320 8818h               |
| 81Ch   | 32     | <a href="#">MSS_RCM_HSM_RTC_CLK_DIV_VAL</a>         | 5320 881Ch               |
| 820h   | 32     | <a href="#">MSS_RCM_HSM_DMTA_CLK_DIV_VAL</a>        | 5320 8820h               |
| 824h   | 32     | <a href="#">MSS_RCM_HSM_DMTB_CLK_DIV_VAL</a>        | 5320 8824h               |
| 828h   | 32     | <a href="#">MSS_RCM_HSM_RTI_CLK_GATE</a>            | 5320 8828h               |
| 82Ch   | 32     | <a href="#">MSS_RCM_HSM_WDT_CLK_GATE</a>            | 5320 882Ch               |
| 830h   | 32     | <a href="#">MSS_RCM_HSM_RTC_CLK_GATE</a>            | 5320 8830h               |
| 834h   | 32     | <a href="#">MSS_RCM_HSM_DMTA_CLK_GATE</a>           | 5320 8834h               |
| 838h   | 32     | <a href="#">MSS_RCM_HSM_DMTB_CLK_GATE</a>           | 5320 8838h               |
| 83Ch   | 32     | <a href="#">MSS_RCM_HSM_RTI_CLK_STATUS</a>          | 5320 883Ch               |
| 840h   | 32     | <a href="#">MSS_RCM_HSM_WDT_CLK_STATUS</a>          | 5320 8840h               |
| 844h   | 32     | <a href="#">MSS_RCM_HSM_RTC_CLK_STATUS</a>          | 5320 8844h               |
| 848h   | 32     | <a href="#">MSS_RCM_HSM_DMTA_CLK_STATUS</a>         | 5320 8848h               |
| 84Ch   | 32     | <a href="#">MSS_RCM_HSM_DMTB_CLK_STATUS</a>         | 5320 884Ch               |
| 1008h  | 32     | <a href="#">MSS_RCM_LOCK0_KICK0</a>                 | 5320 9008h               |
| 100Ch  | 32     | <a href="#">MSS_RCM_LOCK0_KICK1</a>                 | 5320 900Ch               |
| 1010h  | 32     | <a href="#">MSS_RCM_INTR_RAW_STATUS</a>             | 5320 9010h               |

**Table 2-2364. MSS\_RCM Registers, Base Address=5320 8000h, Length=4096 (continued)**

| Offset | Length | Register Name                                     | MSS_RCM Physical Address |
|--------|--------|---------------------------------------------------|--------------------------|
| 1014h  | 32     | <a href="#">MSS_RCM_INTR_ENABLED_STATUS_CLEAR</a> | 5320 9014h               |
| 1018h  | 32     | <a href="#">MSS_RCM_INTR_ENABLE</a>               | 5320 9018h               |
| 101Ch  | 32     | <a href="#">MSS_RCM_INTR_ENABLE_CLEAR</a>         | 5320 901Ch               |
| 1020h  | 32     | <a href="#">MSS_RCM_EOI</a>                       | 5320 9020h               |
| 1024h  | 32     | <a href="#">MSS_RCM_FAULT_ADDRESS</a>             | 5320 9024h               |
| 1028h  | 32     | <a href="#">MSS_RCM_FAULT_TYPE_STATUS</a>         | 5320 9028h               |
| 102Ch  | 32     | <a href="#">MSS_RCM_FAULT_ATTR_STATUS</a>         | 5320 902Ch               |
| 1030h  | 32     | <a href="#">MSS_RCM_FAULT_CLEAR</a>               | 5320 9030h               |

## 2.6.2 MSS\_RCM Registers

### MSS\_RCM Registers



### 2.6.2.1 MSS\_RCM\_R5SS0\_RST\_STATUS Register

#### 1 MSS\_RCM\_R5SS0\_RST\_STATUS Register (Offset = 10h) [reset = 3h]

R5SS Reset Cause Status register of corresponding R5SS.

Return to [Summary Table](#)

**Table 2-2365. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8010h       |

**Figure 2-787. MSS\_RCM\_R5SS0\_RST\_STATUS Name Register**

|                        |    |    |    |    |                        |    |    |
|------------------------|----|----|----|----|------------------------|----|----|
| 31                     | 30 | 29 | 28 | 27 | 26                     | 25 | 24 |
| RESERVED               |    |    |    |    |                        |    |    |
| NONE                   |    |    |    |    |                        |    |    |
| 0h                     |    |    |    |    |                        |    |    |
| 23                     | 22 | 21 | 20 | 19 | 18                     | 17 | 16 |
| RESERVED               |    |    |    |    |                        |    |    |
| NONE                   |    |    |    |    |                        |    |    |
| 0h                     |    |    |    |    |                        |    |    |
| 15                     | 14 | 13 | 12 | 11 | 10                     | 9  | 8  |
| RESERVED               |    |    |    |    | R5SS0_RST_STATUS_CAUSE |    |    |
| NONE                   |    |    |    |    | R                      |    |    |
| 0h                     |    |    |    |    | 3h                     |    |    |
| 7                      | 6  | 5  | 4  | 3  | 2                      | 1  | 0  |
| R5SS0_RST_STATUS_CAUSE |    |    |    |    |                        |    |    |
| R                      |    |    |    |    |                        |    |    |
| 3h                     |    |    |    |    |                        |    |    |

**Table 2-2367. MSS\_RCM\_R5SS0\_RST\_STATUS Register Field Descriptions**

| Bit   | Field                  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:11 | RESERVED               | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 10:0  | R5SS0_RST_STATUS_CAUSE | R    | 3h    | Has the status because of which reset has happened.<br>Bit0: POR Reset<br>Bit1: Warm Reset [Also set during POR Reset]<br>Bit2: CR5SS0 STC Reset<br>Bit3: Reset for CORE0 and MSS_CORE00_VIM using MSS_RCM::MSS_CR5SSA0_RST_CTRL<br>Bit4: Reset for CORE1 and MSS_CORE10_VIM using MSS_RCM::MSS_CR5SSB0_RST_CTRL<br>Bit5: Reset for CORE0 only using MSS_RCM::MSS_CORE00_RST_CTRL<br>Bit6: Reset for CORE1 only using MSS_RCM::MSS_CORE10_RST_CTRL<br>Bit7: Reset for CORE0 and MSS_CORE00_VIM caused because of reset request by debugger in CORE00<br>Bit8: Reset for CORE10 and MSS_CORE10_VIM caused because of reset request by debugger in CORE10<br>Bit9: Reset for CR5SS0 by the RESET FSM using MSS_CTRL::R5SS0_CONTROL_RESET_FSM_TRIGGER<br>Bit 10: Reset for CR5SS0 using MSS_RCM.MSS_CR5SS_POR_RST_CTRL0 |

### 2.6.2.2 MSS\_RCM\_R5SS0\_RST\_CAUSE\_CLR Register

#### 1 MSS\_RCM\_R5SS0\_RST\_CAUSE\_CLR Register (Offset = 14h) [reset = 0h]

R5SS Reset Cause Clear register of corresponding R5SS.

Return to [Summary Table](#)

**Table 2-2368. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8014h       |

**Figure 2-788. MSS\_RCM\_R5SS0\_RST\_CAUSE\_CLR Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | R5SS0_RST_CAUSE_CLR_CLR |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-2370. MSS\_RCM\_R5SS0\_RST\_CAUSE\_CLR Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                                                                                   |
|------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                                                                                      |
| 2:0  | R5SS0_RST_CAUSE_CLR_CLR | R/W  | 0h    | Write pulse bit field:<br>Clear bit for rst cause register [Writing 3'b111 will clear the rst cause register] |

### 2.6.2.3 MSS\_RCM\_SYSRST\_BY\_DBG\_RST0 Register

#### 1 MSS\_RCM\_SYSRST\_BY\_DBG\_RST0 Register (Offset = 18h) [reset = 0h]

This register enables Core debug reset request to propagate to RCM.

Return to [Summary Table](#)

**Table 2-2371. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8018h       |

**Figure 2-789. MSS\_RCM\_SYSRST\_BY\_DBG\_RST0 Name Register**

|          |    |    |    |                        |    |    |    |
|----------|----|----|----|------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                     | 26 | 25 | 24 |
| RESERVED |    |    |    |                        |    |    |    |
| NONE     |    |    |    |                        |    |    |    |
| 0h       |    |    |    |                        |    |    |    |
| 23       | 22 | 21 | 20 | 19                     | 18 | 17 | 16 |
| RESERVED |    |    |    | SYSRST_BY_DBG_RST0_R5B |    |    |    |
| NONE     |    |    |    | R/W                    |    |    |    |
| 0h       |    |    |    | 0h                     |    |    |    |
| 15       | 14 | 13 | 12 | 11                     | 10 | 9  | 8  |
| RESERVED |    |    |    |                        |    |    |    |
| NONE     |    |    |    |                        |    |    |    |
| 0h       |    |    |    |                        |    |    |    |
| 7        | 6  | 5  | 4  | 3                      | 2  | 1  | 0  |
| RESERVED |    |    |    | SYSRST_BY_DBG_RST0_R5A |    |    |    |
| NONE     |    |    |    | R/W                    |    |    |    |
| 0h       |    |    |    | 0h                     |    |    |    |

**Table 2-2373. MSS\_RCM\_SYSRST\_BY\_DBG\_RST0 Register Field Descriptions**

| Bit   | Field                  | Type | Reset | Description                                                                                          |
|-------|------------------------|------|-------|------------------------------------------------------------------------------------------------------|
| 31:19 | RESERVED               | NONE | 0h    | Reserved                                                                                             |
| 18:16 | SYSRST_BY_DBG_RST0_R5B | R/W  | 0h    | Writing 3'b111 will block debug reset request from CORE1 toggling reset for CORE1 of respective R5SS |
| 15:3  | RESERVED               | NONE | 0h    | Reserved                                                                                             |
| 2:0   | SYSRST_BY_DBG_RST0_R5A | R/W  | 0h    | Writing 3'b111 will block debug reset request from CORE0 toggling reset for CORE0 of respective R5SS |

### 2.6.2.4 MSS\_RCM\_RST\_ASSERDLY0 Register

#### 1 MSS\_RCM\_RST\_ASSERDLY0 Register (Offset = 1Ch) [reset = Fh]

This register controls the reset duration of the corresponding R5SS.

Return to [Summary Table](#)

**Table 2-2374. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 801Ch       |

**Figure 2-790. MSS\_RCM\_RST\_ASSERDLY0 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RST_ASSERDLY0_COMMON |    |    |    |    |    |    |    |
| R/W                  |    |    |    |    |    |    |    |
| Fh                   |    |    |    |    |    |    |    |

**Table 2-2376. MSS\_RCM\_RST\_ASSERDLY0 Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                   |
|------|----------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED             | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                      |
| 7:0  | RST_ASSERDLY0_COMMON | R/W  | Fh    | Value decides number of cycles reset should be kept asserted for CR5SS related resets. Programming a value of 0xFF will keep the reset asserted until a new value other than 0xFF is written to this register<br>The actual duration is count + 2 cycles. S/W Recommended value for this is 0x0F<br>The COUNT is applicable to both CPU cores |

### 2.6.2.5 MSS\_RCM\_RST2ASSERTDLY0 Register

#### 1 MSS\_RCM\_RST2ASSERTDLY0 Register (Offset = 20h) [reset = 0h]

This register controls the delay of Reset assertion to the corresponding R5SS.

Return to [Summary Table](#)

**Table 2-2377. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8020h       |

**Figure 2-791. MSS\_RCM\_RST2ASSERTDLY0 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RST2ASSERTDLY0_R5B   |    |    |    |    |    |    |    |
| R/W                  |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RST2ASSERTDLY0_R5A   |    |    |    |    |    |    |    |
| R/W                  |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RST2ASSERTDLY0_R5SSB |    |    |    |    |    |    |    |
| R/W                  |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RST2ASSERTDLY0_R5SSA |    |    |    |    |    |    |    |
| R/W                  |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 2-2379. MSS\_RCM\_RST2ASSERTDLY0 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description                                                                               |
|-------|----------------------|------|-------|-------------------------------------------------------------------------------------------|
| 31:24 | RST2ASSERTDLY0_R5B   | R/W  | 0h    | Value decides number of cycles to wait before asserting reset for local reset for CORE1   |
| 23:16 | RST2ASSERTDLY0_R5A   | R/W  | 0h    | Value decides number of cycles to wait before asserting reset for local reset for CORE0.  |
| 15:8  | RST2ASSERTDLY0_R5SSB | R/W  | 0h    | Value decides number of cycles to wait before asserting reset for global reset for CORE1  |
| 7:0   | RST2ASSERTDLY0_R5SSA | R/W  | 0h    | Value decides number of cycles to wait before asserting reset for global reset for CORE0. |

### 2.6.2.6 MSS\_RCM\_RST\_WFICHECK0 Register

#### 1 MSS\_RCM\_RST\_WFICHECK0 Register (Offset = 24h) [reset = 7070707h]

Enable WFI check before R5 Reset is asserted.

Return to [Summary Table](#)

**Table 2-2380. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8024h       |

**Figure 2-792. MSS\_RCM\_RST\_WFICHECK0 Name Register**

|          |    |    |    |    |                     |    |    |
|----------|----|----|----|----|---------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                  | 25 | 24 |
| RESERVED |    |    |    |    | RST_WFICHECK0_R5B   |    |    |
| NONE     |    |    |    |    | R/W                 |    |    |
| 0h       |    |    |    |    | 7h                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                  | 17 | 16 |
| RESERVED |    |    |    |    | RST_WFICHECK0_R5A   |    |    |
| NONE     |    |    |    |    | R/W                 |    |    |
| 0h       |    |    |    |    | 7h                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                  | 9  | 8  |
| RESERVED |    |    |    |    | RST_WFICHECK0_R5SSB |    |    |
| NONE     |    |    |    |    | R/W                 |    |    |
| 0h       |    |    |    |    | 7h                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                   | 1  | 0  |
| RESERVED |    |    |    |    | RST_WFICHECK0_R5SSA |    |    |
| NONE     |    |    |    |    | R/W                 |    |    |
| 0h       |    |    |    |    | 7h                  |    |    |

**Table 2-2382. MSS\_RCM\_RST\_WFICHECK0 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                               |
|-------|---------------------|------|-------|-------------------------------------------------------------------------------------------|
| 31:27 | RESERVED            | NONE | 0h    | Reserved                                                                                  |
| 26:24 | RST_WFICHECK0_R5B   | R/W  | 7h    | Writing 3'b000 will disable check for WFI before local reset assertion of Cluster0 CORE1  |
| 23:19 | RESERVED            | NONE | 0h    | Reserved                                                                                  |
| 18:16 | RST_WFICHECK0_R5A   | R/W  | 7h    | Writing 3'b000 will disable check for WFI before local reset assertion of Cluster0 CORE0  |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                  |
| 10:8  | RST_WFICHECK0_R5SSB | R/W  | 7h    | Writing 3'b000 will disable check for WFI before global reset assertion of Cluster0 CORE1 |
| 7:3   | RESERVED            | NONE | 0h    | Reserved                                                                                  |
| 2:0   | RST_WFICHECK0_R5SSA | R/W  | 7h    | Writing 3'b000 will disable check for WFI before global reset assertion of Cluster0 CORE0 |

### 2.6.2.7 MSS\_RCM\_R5SS1\_RST\_STATUS Register

#### 1 MSS\_RCM\_R5SS1\_RST\_STATUS Register (Offset = 30h) [reset = 3h]

R5SS Reset Cause Status register of corresponding R5SS.

Return to [Summary Table](#)

**Table 2-2383. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8030h       |

**Figure 2-793. MSS\_RCM\_R5SS1\_RST\_STATUS Name Register**

|                        |    |    |    |    |                        |    |    |
|------------------------|----|----|----|----|------------------------|----|----|
| 31                     | 30 | 29 | 28 | 27 | 26                     | 25 | 24 |
| RESERVED               |    |    |    |    |                        |    |    |
| NONE                   |    |    |    |    |                        |    |    |
| 0h                     |    |    |    |    |                        |    |    |
| 23                     | 22 | 21 | 20 | 19 | 18                     | 17 | 16 |
| RESERVED               |    |    |    |    |                        |    |    |
| NONE                   |    |    |    |    |                        |    |    |
| 0h                     |    |    |    |    |                        |    |    |
| 15                     | 14 | 13 | 12 | 11 | 10                     | 9  | 8  |
| RESERVED               |    |    |    |    | R5SS1_RST_STATUS_CAUSE |    |    |
| NONE                   |    |    |    |    | R                      |    |    |
| 0h                     |    |    |    |    | 3h                     |    |    |
| 7                      | 6  | 5  | 4  | 3  | 2                      | 1  | 0  |
| R5SS1_RST_STATUS_CAUSE |    |    |    |    |                        |    |    |
| R                      |    |    |    |    |                        |    |    |
| 3h                     |    |    |    |    |                        |    |    |

**Table 2-2385. MSS\_RCM\_R5SS1\_RST\_STATUS Register Field Descriptions**

| Bit   | Field                  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:11 | RESERVED               | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 10:0  | R5SS1_RST_STATUS_CAUSE | R    | 3h    | Has the status because of which reset has happened.<br>Bit0: POR Reset<br>Bit1: Warm Reset [Also set during POR Reset]<br>Bit2: CR5SS1 STC Reset<br>Bit3: Reset for CORE0 and MSS_CORE00_VIM using MSS_RCM::MSS_CR5SSA0_RST_CTRL<br>Bit4: Reset for CORE1 and MSS_CORE10_VIM using MSS_RCM::MSS_CR5SSB0_RST_CTRL<br>Bit5: Reset for CORE0 only using MSS_RCM::MSS_CORE00_RST_CTRL<br>Bit6: Reset for CORE1 only using MSS_RCM::MSS_CORE10_RST_CTRL<br>Bit7: Reset for CORE0 and MSS_CORE00_VIM caused because of reset request by debugger in CORE00<br>Bit8: Reset for CORE10 and MSS_CORE10_VIM caused because of reset request by debugger in CORE10<br>Bit9: Reset for CR5SS0 by the RESET FSM using MSS_CTRL::R5SS0_CONTROL_RESET_FSM_TRIGGER Bit<br>10 : Reset for CR5SS1 using MSS_RCM.MSS_CR5SS_POR_RST_CTRL0 |

### 2.6.2.8 MSS\_RCM\_R5SS1\_RST\_CAUSE\_CLR Register

#### 1 MSS\_RCM\_R5SS1\_RST\_CAUSE\_CLR Register (Offset = 34h) [reset = 0h]

R5SS Reset Cause Clear register of corresponding R5SS.

Return to [Summary Table](#)

**Table 2-2386. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8034h       |

**Figure 2-794. MSS\_RCM\_R5SS1\_RST\_CAUSE\_CLR Name Register**

|          |    |    |    |    |                         |    |    |
|----------|----|----|----|----|-------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                      | 25 | 24 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                      | 17 | 16 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                      | 9  | 8  |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                       | 1  | 0  |
| RESERVED |    |    |    |    | R5SS1_RST_CAUSE_CLR_CLR |    |    |
| NONE     |    |    |    |    | R/W                     |    |    |
| 0h       |    |    |    |    | 0h                      |    |    |

**Table 2-2388. MSS\_RCM\_R5SS1\_RST\_CAUSE\_CLR Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                                                                                   |
|------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                                                                                      |
| 2:0  | R5SS1_RST_CAUSE_CLR_CLR | R/W  | 0h    | Write pulse bit field:<br>Clear bit for rst cause register [Writing 3'b111 will clear the rst cause register] |



### 2.6.2.9 MSS\_RCM\_SYSRST\_BY\_DBG\_RST1 Register

#### 1 MSS\_RCM\_SYSRST\_BY\_DBG\_RST1 Register (Offset = 38h) [reset = 0h]

This register enables Core debug reset request to propagate to RCM.

Return to [Summary Table](#)

**Table 2-2389. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8038h       |

**Figure 2-795. MSS\_RCM\_SYSRST\_BY\_DBG\_RST1 Name Register**

|          |    |    |    |                        |    |    |    |
|----------|----|----|----|------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                     | 26 | 25 | 24 |
| RESERVED |    |    |    |                        |    |    |    |
| NONE     |    |    |    |                        |    |    |    |
| 0h       |    |    |    |                        |    |    |    |
| 23       | 22 | 21 | 20 | 19                     | 18 | 17 | 16 |
| RESERVED |    |    |    | SYSRST_BY_DBG_RST1_R5B |    |    |    |
| NONE     |    |    |    | R/W                    |    |    |    |
| 0h       |    |    |    | 0h                     |    |    |    |
| 15       | 14 | 13 | 12 | 11                     | 10 | 9  | 8  |
| RESERVED |    |    |    |                        |    |    |    |
| NONE     |    |    |    |                        |    |    |    |
| 0h       |    |    |    |                        |    |    |    |
| 7        | 6  | 5  | 4  | 3                      | 2  | 1  | 0  |
| RESERVED |    |    |    | SYSRST_BY_DBG_RST1_R5A |    |    |    |
| NONE     |    |    |    | R/W                    |    |    |    |
| 0h       |    |    |    | 0h                     |    |    |    |

**Table 2-2391. MSS\_RCM\_SYSRST\_BY\_DBG\_RST1 Register Field Descriptions**

| Bit   | Field                  | Type | Reset | Description                                                                                          |
|-------|------------------------|------|-------|------------------------------------------------------------------------------------------------------|
| 31:19 | RESERVED               | NONE | 0h    | Reserved                                                                                             |
| 18:16 | SYSRST_BY_DBG_RST1_R5B | R/W  | 0h    | Writing 3'b111 will block debug reset request from CORE1 toggling reset for CORE1 of respective R5SS |
| 15:3  | RESERVED               | NONE | 0h    | Reserved                                                                                             |
| 2:0   | SYSRST_BY_DBG_RST1_R5A | R/W  | 0h    | Writing 3'b111 will block debug reset request from CORE0 toggling reset for CORE0 of respective R5SS |

### 2.6.2.10 MSS\_RCM\_RST\_ASSERTDLY1 Register

#### 1 MSS\_RCM\_RST\_ASSERTDLY1 Register (Offset = 3Ch) [reset = Fh]

This register controls the reset duration of the corresponding R5SS.

Return to [Summary Table](#)

**Table 2-2392. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 803Ch       |

**Figure 2-796. MSS\_RCM\_RST\_ASSERTDLY1 Name Register**

|                       |    |    |    |    |    |    |    |
|-----------------------|----|----|----|----|----|----|----|
| 31                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED              |    |    |    |    |    |    |    |
| NONE                  |    |    |    |    |    |    |    |
| 0h                    |    |    |    |    |    |    |    |
| 23                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED              |    |    |    |    |    |    |    |
| NONE                  |    |    |    |    |    |    |    |
| 0h                    |    |    |    |    |    |    |    |
| 15                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED              |    |    |    |    |    |    |    |
| NONE                  |    |    |    |    |    |    |    |
| 0h                    |    |    |    |    |    |    |    |
| 7                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RST_ASSERTDLY1_COMMON |    |    |    |    |    |    |    |
| R/W                   |    |    |    |    |    |    |    |
| Fh                    |    |    |    |    |    |    |    |

**Table 2-2394. MSS\_RCM\_RST\_ASSERTDLY1 Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                   |
|------|-----------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED              | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                      |
| 7:0  | RST_ASSERTDLY1_COMMON | R/W  | Fh    | Value decides number of cycles reset should be kept asserted for CR5SS related resets. Programming a value of 0xFF will keep the reset asserted until a new value other than 0xFF is written to this register<br>The actual duration is count + 2 cycles. S/W Recommended value for this is 0x0F<br>The COUNT is applicable to both CPU cores |

### 2.6.2.11 MSS\_RCM\_RST2ASSERTDLY1 Register

#### 1 MSS\_RCM\_RST2ASSERTDLY1 Register (Offset = 40h) [reset = 0h]

This register controls the delay of Reset assertion to the corresponding R5SS.

Return to [Summary Table](#)

**Table 2-2395. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8040h       |

**Figure 2-797. MSS\_RCM\_RST2ASSERTDLY1 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RST2ASSERTDLY1_R5B   |    |    |    |    |    |    |    |
| R/W                  |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RST2ASSERTDLY1_R5A   |    |    |    |    |    |    |    |
| R/W                  |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RST2ASSERTDLY1_R5SSB |    |    |    |    |    |    |    |
| R/W                  |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RST2ASSERTDLY1_R5SSA |    |    |    |    |    |    |    |
| R/W                  |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 2-2397. MSS\_RCM\_RST2ASSERTDLY1 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description                                                                               |
|-------|----------------------|------|-------|-------------------------------------------------------------------------------------------|
| 31:24 | RST2ASSERTDLY1_R5B   | R/W  | 0h    | Value decides number of cycles to wait before asserting reset for local reset for CORE1   |
| 23:16 | RST2ASSERTDLY1_R5A   | R/W  | 0h    | Value decides number of cycles to wait before asserting reset for local reset for CORE0.  |
| 15:8  | RST2ASSERTDLY1_R5SSB | R/W  | 0h    | Value decides number of cycles to wait before asserting reset for global reset for CORE1  |
| 7:0   | RST2ASSERTDLY1_R5SSA | R/W  | 0h    | Value decides number of cycles to wait before asserting reset for global reset for CORE0. |

## 2.6.2.12 MSS\_RCM\_RST\_WFICHECK1 Register

### 1 MSS\_RCM\_RST\_WFICHECK1 Register (Offset = 44h) [reset = 7070707h]

Enable WFI check before R5 Reset is asserted.

Return to [Summary Table](#)

**Table 2-2398. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8044h       |

**Figure 2-798. MSS\_RCM\_RST\_WFICHECK1 Name Register**

| 31       | 30 | 29 | 28 | 27 | 26 | 25                  | 24 |
|----------|----|----|----|----|----|---------------------|----|
| RESERVED |    |    |    |    |    | RST_WFICHECK1_R5B   |    |
| NONE     |    |    |    |    |    | R/W                 |    |
| 0h       |    |    |    |    |    | 7h                  |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17                  | 16 |
| RESERVED |    |    |    |    |    | RST_WFICHECK1_R5A   |    |
| NONE     |    |    |    |    |    | R/W                 |    |
| 0h       |    |    |    |    |    | 7h                  |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9                   | 8  |
| RESERVED |    |    |    |    |    | RST_WFICHECK1_R5SSB |    |
| NONE     |    |    |    |    |    | R/W                 |    |
| 0h       |    |    |    |    |    | 7h                  |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1                   | 0  |
| RESERVED |    |    |    |    |    | RST_WFICHECK1_R5SSA |    |
| NONE     |    |    |    |    |    | R/W                 |    |
| 0h       |    |    |    |    |    | 7h                  |    |

**Table 2-2400. MSS\_RCM\_RST\_WFICHECK1 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                               |
|-------|---------------------|------|-------|-------------------------------------------------------------------------------------------|
| 31:27 | RESERVED            | NONE | 0h    | Reserved                                                                                  |
| 26:24 | RST_WFICHECK1_R5B   | R/W  | 7h    | Writing 3'b000 will disable check for WFI before local reset assertion of Cluster1 CORE1  |
| 23:19 | RESERVED            | NONE | 0h    | Reserved                                                                                  |
| 18:16 | RST_WFICHECK1_R5A   | R/W  | 7h    | Writing 3'b000 will disable check for WFI before local reset assertion of Cluster1 CORE0  |
| 15:11 | RESERVED            | NONE | 0h    | Reserved                                                                                  |
| 10:8  | RST_WFICHECK1_R5SSB | R/W  | 7h    | Writing 3'b000 will disable check for WFI before global reset assertion of Cluster1 CORE1 |
| 7:3   | RESERVED            | NONE | 0h    | Reserved                                                                                  |
| 2:0   | RST_WFICHECK1_R5SSA | R/W  | 7h    | Writing 3'b000 will disable check for WFI before global reset assertion of Cluster1 CORE0 |

### 2.6.2.13 MSS\_RCM\_MSS\_MCAN0\_CLK\_SRC\_SEL Register

#### 1 MSS\_RCM\_MSS\_MCAN0\_CLK\_SRC\_SEL Register (Offset = 100h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-2401. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8100h       |

**Figure 2-799. MSS\_RCM\_MSS\_MCAN0\_CLK\_SRC\_SEL Name Register**

|                                 |    |    |    |                                 |    |    |    |
|---------------------------------|----|----|----|---------------------------------|----|----|----|
| 31                              | 30 | 29 | 28 | 27                              | 26 | 25 | 24 |
| RESERVED                        |    |    |    |                                 |    |    |    |
| NONE                            |    |    |    |                                 |    |    |    |
| 0h                              |    |    |    |                                 |    |    |    |
| 23                              | 22 | 21 | 20 | 19                              | 18 | 17 | 16 |
| RESERVED                        |    |    |    |                                 |    |    |    |
| NONE                            |    |    |    |                                 |    |    |    |
| 0h                              |    |    |    |                                 |    |    |    |
| 15                              | 14 | 13 | 12 | 11                              | 10 | 9  | 8  |
| RESERVED                        |    |    |    | MSS_MCAN0_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                            |    |    |    | R/W                             |    |    |    |
| 0h                              |    |    |    | 0h                              |    |    |    |
| 7                               | 6  | 5  | 4  | 3                               | 2  | 1  | 0  |
| MSS_MCAN0_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                 |    |    |    |
| R/W                             |    |    |    |                                 |    |    |    |
| 0h                              |    |    |    |                                 |    |    |    |

**Table 2-2403. MSS\_RCM\_MSS\_MCAN0\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|---------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 11:0  | MSS_MCAN0_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for corresponding MCAN. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register.<br>Use the following values for selecting clock source-<br>0x000 - WUCPUCLK<br>0x111 - EXT_REFCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT0<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - RCCLK10M |

### 2.6.2.14 MSS\_RCM\_MSS\_MCAN1\_CLK\_SRC\_SEL Register

#### 1 MSS\_RCM\_MSS\_MCAN1\_CLK\_SRC\_SEL Register (Offset = 104h) [reset = 0h]

Clock Source selection Register for corresponding Root clock.

Return to [Summary Table](#)

**Table 2-2404. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8104h       |

**Figure 2-800. MSS\_RCM\_MSS\_MCAN1\_CLK\_SRC\_SEL Name Register**

|                                 |    |    |    |                                 |    |    |    |
|---------------------------------|----|----|----|---------------------------------|----|----|----|
| 31                              | 30 | 29 | 28 | 27                              | 26 | 25 | 24 |
| RESERVED                        |    |    |    |                                 |    |    |    |
| NONE                            |    |    |    |                                 |    |    |    |
| 0h                              |    |    |    |                                 |    |    |    |
| 23                              | 22 | 21 | 20 | 19                              | 18 | 17 | 16 |
| RESERVED                        |    |    |    |                                 |    |    |    |
| NONE                            |    |    |    |                                 |    |    |    |
| 0h                              |    |    |    |                                 |    |    |    |
| 15                              | 14 | 13 | 12 | 11                              | 10 | 9  | 8  |
| RESERVED                        |    |    |    | MSS_MCAN1_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                            |    |    |    | R/W                             |    |    |    |
| 0h                              |    |    |    | 0h                              |    |    |    |
| 7                               | 6  | 5  | 4  | 3                               | 2  | 1  | 0  |
| MSS_MCAN1_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                 |    |    |    |
| R/W                             |    |    |    |                                 |    |    |    |
| 0h                              |    |    |    |                                 |    |    |    |

**Table 2-2406. MSS\_RCM\_MSS\_MCAN1\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|---------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 11:0  | MSS_MCAN1_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for corresponding MCAN. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register.<br>Use the following values for selecting clock source-<br>0x000 - WUCPUCLK<br>0x111 - EXT_REFCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT0<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - RCCLK10M |

### 2.6.2.15 MSS\_RCM\_MSS\_MCAN2\_CLK\_SRC\_SEL Register

#### 1 MSS\_RCM\_MSS\_MCAN2\_CLK\_SRC\_SEL Register (Offset = 108h) [reset = 0h]

Clock Source selection Register for corresponding Root clock.

Return to [Summary Table](#)

**Table 2-2407. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8108h       |

**Figure 2-801. MSS\_RCM\_MSS\_MCAN2\_CLK\_SRC\_SEL Name Register**

|                                 |    |    |    |                                 |    |    |    |
|---------------------------------|----|----|----|---------------------------------|----|----|----|
| 31                              | 30 | 29 | 28 | 27                              | 26 | 25 | 24 |
| RESERVED                        |    |    |    |                                 |    |    |    |
| NONE                            |    |    |    |                                 |    |    |    |
| 0h                              |    |    |    |                                 |    |    |    |
| 23                              | 22 | 21 | 20 | 19                              | 18 | 17 | 16 |
| RESERVED                        |    |    |    |                                 |    |    |    |
| NONE                            |    |    |    |                                 |    |    |    |
| 0h                              |    |    |    |                                 |    |    |    |
| 15                              | 14 | 13 | 12 | 11                              | 10 | 9  | 8  |
| RESERVED                        |    |    |    | MSS_MCAN2_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                            |    |    |    | R/W                             |    |    |    |
| 0h                              |    |    |    | 0h                              |    |    |    |
| 7                               | 6  | 5  | 4  | 3                               | 2  | 1  | 0  |
| MSS_MCAN2_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                 |    |    |    |
| R/W                             |    |    |    |                                 |    |    |    |
| 0h                              |    |    |    |                                 |    |    |    |

**Table 2-2409. MSS\_RCM\_MSS\_MCAN2\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|---------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 11:0  | MSS_MCAN2_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for corresponding MCAN. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register.<br>Use the following values for selecting clock source-<br>0x000 - WUCPUCLK<br>0x111 - EXT_REFCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT0<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - RCCLK10M |

### 2.6.2.16 MSS\_RCM\_MSS\_MCAN3\_CLK\_SRC\_SEL Register

#### 1 MSS\_RCM\_MSS\_MCAN3\_CLK\_SRC\_SEL Register (Offset = 10Ch) [reset = 0h]

Clock Source selection Register for corresponding Root clock.

Return to [Summary Table](#)

**Table 2-2410. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 810Ch       |

**Figure 2-802. MSS\_RCM\_MSS\_MCAN3\_CLK\_SRC\_SEL Name Register**

|                                 |    |    |    |                                 |    |    |    |
|---------------------------------|----|----|----|---------------------------------|----|----|----|
| 31                              | 30 | 29 | 28 | 27                              | 26 | 25 | 24 |
| RESERVED                        |    |    |    |                                 |    |    |    |
| NONE                            |    |    |    |                                 |    |    |    |
| 0h                              |    |    |    |                                 |    |    |    |
| 23                              | 22 | 21 | 20 | 19                              | 18 | 17 | 16 |
| RESERVED                        |    |    |    |                                 |    |    |    |
| NONE                            |    |    |    |                                 |    |    |    |
| 0h                              |    |    |    |                                 |    |    |    |
| 15                              | 14 | 13 | 12 | 11                              | 10 | 9  | 8  |
| RESERVED                        |    |    |    | MSS_MCAN3_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                            |    |    |    | R/W                             |    |    |    |
| 0h                              |    |    |    | 0h                              |    |    |    |
| 7                               | 6  | 5  | 4  | 3                               | 2  | 1  | 0  |
| MSS_MCAN3_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                 |    |    |    |
| R/W                             |    |    |    |                                 |    |    |    |
| 0h                              |    |    |    |                                 |    |    |    |

**Table 2-2412. MSS\_RCM\_MSS\_MCAN3\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|---------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 11:0  | MSS_MCAN3_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for corresponding MCAN. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register.<br>Use the following values for selecting clock source-<br>0x000 - WUCPUCLK<br>0x111 - EXT_REFCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT0<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - RCCLK10M |



### 2.6.2.17 MSS\_RCM\_MSS\_QSPI\_CLK\_SRC\_SEL Register

#### 1 MSS\_RCM\_MSS\_QSPI\_CLK\_SRC\_SEL Register (Offset = 110h) [reset = 0h]

Clock Source selection Register for corresponding Root clock.

Return to [Summary Table](#)

**Table 2-2413. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8110h       |

**Figure 2-803. MSS\_RCM\_MSS\_QSPI\_CLK\_SRC\_SEL Name Register**

|                                |    |    |    |                                |    |    |    |
|--------------------------------|----|----|----|--------------------------------|----|----|----|
| 31                             | 30 | 29 | 28 | 27                             | 26 | 25 | 24 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 23                             | 22 | 21 | 20 | 19                             | 18 | 17 | 16 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 15                             | 14 | 13 | 12 | 11                             | 10 | 9  | 8  |
| RESERVED                       |    |    |    | MSS_QSPI_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                           |    |    |    | R/W                            |    |    |    |
| 0h                             |    |    |    | 0h                             |    |    |    |
| 7                              | 6  | 5  | 4  | 3                              | 2  | 1  | 0  |
| MSS_QSPI_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                |    |    |    |
| R/W                            |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |

**Table 2-2415. MSS\_RCM\_MSS\_QSPI\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 11:0  | MSS_QSPI_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for QSPI. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values for selecting clock source-<br>0x000 - WUCPUCLK<br>0x111 - EXT_REFCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT0<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - RCCLK10M |

### 2.6.2.18 MSS\_RCM\_MSS\_RTIO\_CLK\_SRC\_SEL Register

#### 1 MSS\_RCM\_MSS\_RTIO\_CLK\_SRC\_SEL Register (Offset = 114h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-2416. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8114h       |

**Figure 2-804. MSS\_RCM\_MSS\_RTIO\_CLK\_SRC\_SEL Name Register**

|                                |    |    |    |                                |    |    |    |
|--------------------------------|----|----|----|--------------------------------|----|----|----|
| 31                             | 30 | 29 | 28 | 27                             | 26 | 25 | 24 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 23                             | 22 | 21 | 20 | 19                             | 18 | 17 | 16 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 15                             | 14 | 13 | 12 | 11                             | 10 | 9  | 8  |
| RESERVED                       |    |    |    | MSS_RTIO_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                           |    |    |    | R/W                            |    |    |    |
| 0h                             |    |    |    | 0h                             |    |    |    |
| 7                              | 6  | 5  | 4  | 3                              | 2  | 1  | 0  |
| MSS_RTIO_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                |    |    |    |
| R/W                            |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |

**Table 2-2418. MSS\_RCM\_MSS\_RTIO\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|--------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 11:0  | MSS_RTIO_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for Corresponding RTI. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - EXT_REFCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT1<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - CTPS_GENF0 |

### 2.6.2.19 MSS\_RCM\_MSS\_RT11\_CLK\_SRC\_SEL Register

#### 1 MSS\_RCM\_MSS\_RT11\_CLK\_SRC\_SEL Register (Offset = 118h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-2419. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8118h       |

**Figure 2-805. MSS\_RCM\_MSS\_RT11\_CLK\_SRC\_SEL Name Register**

|                                |    |    |    |                                |    |    |    |
|--------------------------------|----|----|----|--------------------------------|----|----|----|
| 31                             | 30 | 29 | 28 | 27                             | 26 | 25 | 24 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 23                             | 22 | 21 | 20 | 19                             | 18 | 17 | 16 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 15                             | 14 | 13 | 12 | 11                             | 10 | 9  | 8  |
| RESERVED                       |    |    |    | MSS_RT11_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                           |    |    |    | R/W                            |    |    |    |
| 0h                             |    |    |    | 0h                             |    |    |    |
| 7                              | 6  | 5  | 4  | 3                              | 2  | 1  | 0  |
| MSS_RT11_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                |    |    |    |
| R/W                            |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |

**Table 2-2421. MSS\_RCM\_MSS\_RT11\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|--------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 11:0  | MSS_RT11_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for Corresponding RTI. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - EXT_REFCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT1<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - CTPS_GENF0 |

## 2.6.2.20 MSS\_RCM\_MSS\_RT12\_CLK\_SRC\_SEL Register

### 1 MSS\_RCM\_MSS\_RT12\_CLK\_SRC\_SEL Register (Offset = 11Ch) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-2422. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 811Ch       |

**Figure 2-806. MSS\_RCM\_MSS\_RT12\_CLK\_SRC\_SEL Name Register**

|                                |    |    |    |                                |    |    |    |
|--------------------------------|----|----|----|--------------------------------|----|----|----|
| 31                             | 30 | 29 | 28 | 27                             | 26 | 25 | 24 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 23                             | 22 | 21 | 20 | 19                             | 18 | 17 | 16 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 15                             | 14 | 13 | 12 | 11                             | 10 | 9  | 8  |
| RESERVED                       |    |    |    | MSS_RT12_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                           |    |    |    | R/W                            |    |    |    |
| 0h                             |    |    |    | 0h                             |    |    |    |
| 7                              | 6  | 5  | 4  | 3                              | 2  | 1  | 0  |
| MSS_RT12_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                |    |    |    |
| R/W                            |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |

**Table 2-2424. MSS\_RCM\_MSS\_RT12\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|--------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 11:0  | MSS_RT12_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for Corresponding RTI. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - EXT_REFCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT1<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - CTPS_GENF0 |

### 2.6.2.21 MSS\_RCM\_MSS\_RT13\_CLK\_SRC\_SEL Register

#### 1 MSS\_RCM\_MSS\_RT13\_CLK\_SRC\_SEL Register (Offset = 120h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-2425. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8120h       |

**Figure 2-807. MSS\_RCM\_MSS\_RT13\_CLK\_SRC\_SEL Name Register**

|                                |    |    |    |                                |    |    |    |
|--------------------------------|----|----|----|--------------------------------|----|----|----|
| 31                             | 30 | 29 | 28 | 27                             | 26 | 25 | 24 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 23                             | 22 | 21 | 20 | 19                             | 18 | 17 | 16 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 15                             | 14 | 13 | 12 | 11                             | 10 | 9  | 8  |
| RESERVED                       |    |    |    | MSS_RT13_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                           |    |    |    | R/W                            |    |    |    |
| 0h                             |    |    |    | 0h                             |    |    |    |
| 7                              | 6  | 5  | 4  | 3                              | 2  | 1  | 0  |
| MSS_RT13_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                |    |    |    |
| R/W                            |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |

**Table 2-2427. MSS\_RCM\_MSS\_RT13\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|--------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 11:0  | MSS_RT13_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for Corresponding RTI. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - EXT_REFCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT1<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - CTPS_GENF0 |

### 2.6.2.22 MSS\_RCM\_MSS\_WDT0\_CLK\_SRC\_SEL Register

#### 1 MSS\_RCM\_MSS\_WDT0\_CLK\_SRC\_SEL Register (Offset = 128h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-2428. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8128h       |

**Figure 2-808. MSS\_RCM\_MSS\_WDT0\_CLK\_SRC\_SEL Name Register**

|                                |    |    |    |                                |    |    |    |
|--------------------------------|----|----|----|--------------------------------|----|----|----|
| 31                             | 30 | 29 | 28 | 27                             | 26 | 25 | 24 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 23                             | 22 | 21 | 20 | 19                             | 18 | 17 | 16 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 15                             | 14 | 13 | 12 | 11                             | 10 | 9  | 8  |
| RESERVED                       |    |    |    | MSS_WDT0_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                           |    |    |    | R/W                            |    |    |    |
| 0h                             |    |    |    | 0h                             |    |    |    |
| 7                              | 6  | 5  | 4  | 3                              | 2  | 1  | 0  |
| MSS_WDT0_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                |    |    |    |
| R/W                            |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |

**Table 2-2430. MSS\_RCM\_MSS\_WDT0\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|--------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 11:0  | MSS_WDT0_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for WDT.Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register.Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - RCCLK10M<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT1<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - RCCLK32K |

### 2.6.2.23 MSS\_RCM\_MSS\_WDT1\_CLK\_SRC\_SEL Register

#### 1 MSS\_RCM\_MSS\_WDT1\_CLK\_SRC\_SEL Register (Offset = 12Ch) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-2431. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 812Ch       |

**Figure 2-809. MSS\_RCM\_MSS\_WDT1\_CLK\_SRC\_SEL Name Register**

|                                |    |    |    |                                |    |    |    |
|--------------------------------|----|----|----|--------------------------------|----|----|----|
| 31                             | 30 | 29 | 28 | 27                             | 26 | 25 | 24 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 23                             | 22 | 21 | 20 | 19                             | 18 | 17 | 16 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 15                             | 14 | 13 | 12 | 11                             | 10 | 9  | 8  |
| RESERVED                       |    |    |    | MSS_WDT1_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                           |    |    |    | R/W                            |    |    |    |
| 0h                             |    |    |    | 0h                             |    |    |    |
| 7                              | 6  | 5  | 4  | 3                              | 2  | 1  | 0  |
| MSS_WDT1_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                |    |    |    |
| R/W                            |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |

**Table 2-2433. MSS\_RCM\_MSS\_WDT1\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|--------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 11:0  | MSS_WDT1_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for WDT.Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register.Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - RCCLK10M<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT1<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - RCCLK32K |

### 2.6.2.24 MSS\_RCM\_MSS\_WDT2\_CLK\_SRC\_SEL Register

#### 1 MSS\_RCM\_MSS\_WDT2\_CLK\_SRC\_SEL Register (Offset = 130h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-2434. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8130h       |

**Figure 2-810. MSS\_RCM\_MSS\_WDT2\_CLK\_SRC\_SEL Name Register**

|                                |    |    |    |                                |    |    |    |
|--------------------------------|----|----|----|--------------------------------|----|----|----|
| 31                             | 30 | 29 | 28 | 27                             | 26 | 25 | 24 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 23                             | 22 | 21 | 20 | 19                             | 18 | 17 | 16 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 15                             | 14 | 13 | 12 | 11                             | 10 | 9  | 8  |
| RESERVED                       |    |    |    | MSS_WDT2_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                           |    |    |    | R/W                            |    |    |    |
| 0h                             |    |    |    | 0h                             |    |    |    |
| 7                              | 6  | 5  | 4  | 3                              | 2  | 1  | 0  |
| MSS_WDT2_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                |    |    |    |
| R/W                            |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |

**Table 2-2436. MSS\_RCM\_MSS\_WDT2\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|--------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 11:0  | MSS_WDT2_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for WDT.Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register.Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - RCCLK10M<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT1<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - RCCLK32K |



### 2.6.2.25 MSS\_RCM\_MSS\_WDT3\_CLK\_SRC\_SEL Register

#### 1 MSS\_RCM\_MSS\_WDT3\_CLK\_SRC\_SEL Register (Offset = 134h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-2437. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8134h       |

**Figure 2-811. MSS\_RCM\_MSS\_WDT3\_CLK\_SRC\_SEL Name Register**

|                                |    |    |    |                                |    |    |    |
|--------------------------------|----|----|----|--------------------------------|----|----|----|
| 31                             | 30 | 29 | 28 | 27                             | 26 | 25 | 24 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 23                             | 22 | 21 | 20 | 19                             | 18 | 17 | 16 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 15                             | 14 | 13 | 12 | 11                             | 10 | 9  | 8  |
| RESERVED                       |    |    |    | MSS_WDT3_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                           |    |    |    | R/W                            |    |    |    |
| 0h                             |    |    |    | 0h                             |    |    |    |
| 7                              | 6  | 5  | 4  | 3                              | 2  | 1  | 0  |
| MSS_WDT3_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                |    |    |    |
| R/W                            |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |

**Table 2-2439. MSS\_RCM\_MSS\_WDT3\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|--------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 11:0  | MSS_WDT3_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for WDT.Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register.Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - RCCLK10M<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT1<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - RCCLK32K |

### 2.6.2.26 MSS\_RCM\_MSS\_SPI0\_CLK\_SRC\_SEL Register

#### 1 MSS\_RCM\_MSS\_SPI0\_CLK\_SRC\_SEL Register (Offset = 13Ch) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-2440. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 813Ch       |

**Figure 2-812. MSS\_RCM\_MSS\_SPI0\_CLK\_SRC\_SEL Name Register**

|                                |    |    |    |                                |    |    |    |
|--------------------------------|----|----|----|--------------------------------|----|----|----|
| 31                             | 30 | 29 | 28 | 27                             | 26 | 25 | 24 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 23                             | 22 | 21 | 20 | 19                             | 18 | 17 | 16 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 15                             | 14 | 13 | 12 | 11                             | 10 | 9  | 8  |
| RESERVED                       |    |    |    | MSS_SPI0_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                           |    |    |    | R/W                            |    |    |    |
| 0h                             |    |    |    | 0h                             |    |    |    |
| 7                              | 6  | 5  | 4  | 3                              | 2  | 1  | 0  |
| MSS_SPI0_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                |    |    |    |
| R/W                            |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |

**Table 2-2442. MSS\_RCM\_MSS\_SPI0\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 11:0  | MSS_SPI0_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for Corresponding SPI. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - EXT_REFCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT0<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - RCCLK10M |

### 2.6.2.27 MSS\_RCM\_MSS\_SPI1\_CLK\_SRC\_SEL Register

#### 1 MSS\_RCM\_MSS\_SPI1\_CLK\_SRC\_SEL Register (Offset = 140h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-2443. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8140h       |

**Figure 2-813. MSS\_RCM\_MSS\_SPI1\_CLK\_SRC\_SEL Name Register**

|                                |    |    |    |                                |    |    |    |
|--------------------------------|----|----|----|--------------------------------|----|----|----|
| 31                             | 30 | 29 | 28 | 27                             | 26 | 25 | 24 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 23                             | 22 | 21 | 20 | 19                             | 18 | 17 | 16 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 15                             | 14 | 13 | 12 | 11                             | 10 | 9  | 8  |
| RESERVED                       |    |    |    | MSS_SPI1_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                           |    |    |    | R/W                            |    |    |    |
| 0h                             |    |    |    | 0h                             |    |    |    |
| 7                              | 6  | 5  | 4  | 3                              | 2  | 1  | 0  |
| MSS_SPI1_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                |    |    |    |
| R/W                            |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |

**Table 2-2445. MSS\_RCM\_MSS\_SPI1\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 11:0  | MSS_SPI1_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for Corresponding SPI. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - EXT_REFCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT0<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - RCCLK10M |

### 2.6.2.28 MSS\_RCM\_MSS\_SPI2\_CLK\_SRC\_SEL Register

#### 1 MSS\_RCM\_MSS\_SPI2\_CLK\_SRC\_SEL Register (Offset = 144h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-2446. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8144h       |

**Figure 2-814. MSS\_RCM\_MSS\_SPI2\_CLK\_SRC\_SEL Name Register**

|                                |    |    |    |                                |    |    |    |
|--------------------------------|----|----|----|--------------------------------|----|----|----|
| 31                             | 30 | 29 | 28 | 27                             | 26 | 25 | 24 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 23                             | 22 | 21 | 20 | 19                             | 18 | 17 | 16 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 15                             | 14 | 13 | 12 | 11                             | 10 | 9  | 8  |
| RESERVED                       |    |    |    | MSS_SPI2_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                           |    |    |    | R/W                            |    |    |    |
| 0h                             |    |    |    | 0h                             |    |    |    |
| 7                              | 6  | 5  | 4  | 3                              | 2  | 1  | 0  |
| MSS_SPI2_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                |    |    |    |
| R/W                            |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |

**Table 2-2448. MSS\_RCM\_MSS\_SPI2\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 11:0  | MSS_SPI2_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for Corresponding SPI. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - EXT_REFCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT0<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - RCCLK10M |

### 2.6.2.29 MSS\_RCM\_MSS\_SPI3\_CLK\_SRC\_SEL Register

#### 1 MSS\_RCM\_MSS\_SPI3\_CLK\_SRC\_SEL Register (Offset = 148h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-2449. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8148h       |

**Figure 2-815. MSS\_RCM\_MSS\_SPI3\_CLK\_SRC\_SEL Name Register**

|                                |    |    |    |                                |    |    |    |
|--------------------------------|----|----|----|--------------------------------|----|----|----|
| 31                             | 30 | 29 | 28 | 27                             | 26 | 25 | 24 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 23                             | 22 | 21 | 20 | 19                             | 18 | 17 | 16 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 15                             | 14 | 13 | 12 | 11                             | 10 | 9  | 8  |
| RESERVED                       |    |    |    | MSS_SPI3_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                           |    |    |    | R/W                            |    |    |    |
| 0h                             |    |    |    | 0h                             |    |    |    |
| 7                              | 6  | 5  | 4  | 3                              | 2  | 1  | 0  |
| MSS_SPI3_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                |    |    |    |
| R/W                            |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |

**Table 2-2451. MSS\_RCM\_MSS\_SPI3\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 11:0  | MSS_SPI3_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for Corresponding SPI. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - EXT_REFCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT0<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - RCCLK10M |

### 2.6.2.30 MSS\_RCM\_MSS\_SPI4\_CLK\_SRC\_SEL Register

#### 1 MSS\_RCM\_MSS\_SPI4\_CLK\_SRC\_SEL Register (Offset = 14Ch) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-2452. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 814Ch       |

**Figure 2-816. MSS\_RCM\_MSS\_SPI4\_CLK\_SRC\_SEL Name Register**

|                                |    |    |    |                                |    |    |    |
|--------------------------------|----|----|----|--------------------------------|----|----|----|
| 31                             | 30 | 29 | 28 | 27                             | 26 | 25 | 24 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 23                             | 22 | 21 | 20 | 19                             | 18 | 17 | 16 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 15                             | 14 | 13 | 12 | 11                             | 10 | 9  | 8  |
| RESERVED                       |    |    |    | MSS_SPI4_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                           |    |    |    | R/W                            |    |    |    |
| 0h                             |    |    |    | 0h                             |    |    |    |
| 7                              | 6  | 5  | 4  | 3                              | 2  | 1  | 0  |
| MSS_SPI4_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                |    |    |    |
| R/W                            |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |

**Table 2-2454. MSS\_RCM\_MSS\_SPI4\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 11:0  | MSS_SPI4_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for Corresponding SPI. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register. Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - EXT_REFCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT0<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - RCCLK10M |

### 2.6.2.31 MSS\_RCM\_MSS\_MMCSO\_CLK\_SRC\_SEL Register

#### 1 MSS\_RCM\_MSS\_MMCSO\_CLK\_SRC\_SEL Register (Offset = 150h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-2455. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8150h       |

**Figure 2-817. MSS\_RCM\_MSS\_MMCSO\_CLK\_SRC\_SEL Name Register**

|                                 |    |    |    |                                 |    |    |    |
|---------------------------------|----|----|----|---------------------------------|----|----|----|
| 31                              | 30 | 29 | 28 | 27                              | 26 | 25 | 24 |
| RESERVED                        |    |    |    |                                 |    |    |    |
| NONE                            |    |    |    |                                 |    |    |    |
| 0h                              |    |    |    |                                 |    |    |    |
| 23                              | 22 | 21 | 20 | 19                              | 18 | 17 | 16 |
| RESERVED                        |    |    |    |                                 |    |    |    |
| NONE                            |    |    |    |                                 |    |    |    |
| 0h                              |    |    |    |                                 |    |    |    |
| 15                              | 14 | 13 | 12 | 11                              | 10 | 9  | 8  |
| RESERVED                        |    |    |    | MSS_MMCSO_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                            |    |    |    | R/W                             |    |    |    |
| 0h                              |    |    |    | 0h                              |    |    |    |
| 7                               | 6  | 5  | 4  | 3                               | 2  | 1  | 0  |
| MSS_MMCSO_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                 |    |    |    |
| R/W                             |    |    |    |                                 |    |    |    |
| 0h                              |    |    |    |                                 |    |    |    |

**Table 2-2457. MSS\_RCM\_MSS\_MMCSO\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|---------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 11:0  | MSS_MMCSO_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for MMCSO. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register.<br>Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - EXT_REFCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT0<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - RCCLK10M |

### 2.6.2.32 MSS\_RCM\_PRU\_ICSS\_UCLK\_CLK\_SRC\_SEL Register

#### 1 MSS\_RCM\_PRU\_ICSS\_UCLK\_CLK\_SRC\_SEL Register (Offset = 154h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-2458. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8154h       |

**Figure 2-818. MSS\_RCM\_PRU\_ICSS\_UCLK\_CLK\_SRC\_SEL Name Register**

|                                     |    |    |    |                                     |    |    |    |
|-------------------------------------|----|----|----|-------------------------------------|----|----|----|
| 31                                  | 30 | 29 | 28 | 27                                  | 26 | 25 | 24 |
| RESERVED                            |    |    |    |                                     |    |    |    |
| NONE                                |    |    |    |                                     |    |    |    |
| 0h                                  |    |    |    |                                     |    |    |    |
| 23                                  | 22 | 21 | 20 | 19                                  | 18 | 17 | 16 |
| RESERVED                            |    |    |    |                                     |    |    |    |
| NONE                                |    |    |    |                                     |    |    |    |
| 0h                                  |    |    |    |                                     |    |    |    |
| 15                                  | 14 | 13 | 12 | 11                                  | 10 | 9  | 8  |
| RESERVED                            |    |    |    | PRU_ICSS_UCLK_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                                |    |    |    | R/W                                 |    |    |    |
| 0h                                  |    |    |    | 0h                                  |    |    |    |
| 7                                   | 6  | 5  | 4  | 3                                   | 2  | 1  | 0  |
| PRU_ICSS_UCLK_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                     |    |    |    |
| R/W                                 |    |    |    |                                     |    |    |    |
| 0h                                  |    |    |    |                                     |    |    |    |

**Table 2-2460. MSS\_RCM\_PRU\_ICSS\_UCLK\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|-------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 11:0  | PRU_ICSS_UCLK_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for ICSSM_UCLK. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register.<br>Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - EXT_REFCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT0<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - DPLL_PER_HSDIV0_CLKOUT0 |



### 2.6.2.33 MSS\_RCM\_MSS\_CPTS\_CLK\_SRC\_SEL Register

#### 1 MSS\_RCM\_MSS\_CPTS\_CLK\_SRC\_SEL Register (Offset = 158h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-2461. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8158h       |

**Figure 2-819. MSS\_RCM\_MSS\_CPTS\_CLK\_SRC\_SEL Name Register**

|                                |    |    |    |                                |    |    |    |
|--------------------------------|----|----|----|--------------------------------|----|----|----|
| 31                             | 30 | 29 | 28 | 27                             | 26 | 25 | 24 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 23                             | 22 | 21 | 20 | 19                             | 18 | 17 | 16 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 15                             | 14 | 13 | 12 | 11                             | 10 | 9  | 8  |
| RESERVED                       |    |    |    | MSS_CPTS_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                           |    |    |    | R/W                            |    |    |    |
| 0h                             |    |    |    | 0h                             |    |    |    |
| 7                              | 6  | 5  | 4  | 3                              | 2  | 1  | 0  |
| MSS_CPTS_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                |    |    |    |
| R/W                            |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |

**Table 2-2463. MSS\_RCM\_MSS\_CPTS\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|--------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 11:0  | MSS_CPTS_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for CPTS. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register.<br>Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - EXT_REFCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_CORE_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT0<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - RCCLK10M |

### 2.6.2.34 MSS\_RCM\_GPMC\_CLK\_SRC\_SEL Register

#### 1 MSS\_RCM\_GPMC\_CLK\_SRC\_SEL Register (Offset = 15Ch) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-2464. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 815Ch       |

**Figure 2-820. MSS\_RCM\_GPMC\_CLK\_SRC\_SEL Name Register**

|                            |    |    |    |                            |    |    |    |
|----------------------------|----|----|----|----------------------------|----|----|----|
| 31                         | 30 | 29 | 28 | 27                         | 26 | 25 | 24 |
| RESERVED                   |    |    |    |                            |    |    |    |
| NONE                       |    |    |    |                            |    |    |    |
| 0h                         |    |    |    |                            |    |    |    |
| 23                         | 22 | 21 | 20 | 19                         | 18 | 17 | 16 |
| RESERVED                   |    |    |    |                            |    |    |    |
| NONE                       |    |    |    |                            |    |    |    |
| 0h                         |    |    |    |                            |    |    |    |
| 15                         | 14 | 13 | 12 | 11                         | 10 | 9  | 8  |
| RESERVED                   |    |    |    | GPMC_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                       |    |    |    | R/W                        |    |    |    |
| 0h                         |    |    |    | 0h                         |    |    |    |
| 7                          | 6  | 5  | 4  | 3                          | 2  | 1  | 0  |
| GPMC_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                            |    |    |    |
| R/W                        |    |    |    |                            |    |    |    |
| 0h                         |    |    |    |                            |    |    |    |

**Table 2-2466. MSS\_RCM\_GPMC\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|----------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 11:0  | GPMC_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for GPMC. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register.<br>Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - EXT_REFCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT0<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - RCCLK10M |

### 2.6.2.35 MSS\_RCM\_CONTROLSS\_PLL\_CLK\_SRC\_SEL Register

#### 1 MSS\_RCM\_CONTROLSS\_PLL\_CLK\_SRC\_SEL Register (Offset = 160h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-2467. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8160h       |

**Figure 2-821. MSS\_RCM\_CONTROLSS\_PLL\_CLK\_SRC\_SEL Name Register**

|                                     |    |    |    |                                     |    |    |    |
|-------------------------------------|----|----|----|-------------------------------------|----|----|----|
| 31                                  | 30 | 29 | 28 | 27                                  | 26 | 25 | 24 |
| RESERVED                            |    |    |    |                                     |    |    |    |
| NONE                                |    |    |    |                                     |    |    |    |
| 0h                                  |    |    |    |                                     |    |    |    |
| 23                                  | 22 | 21 | 20 | 19                                  | 18 | 17 | 16 |
| RESERVED                            |    |    |    |                                     |    |    |    |
| NONE                                |    |    |    |                                     |    |    |    |
| 0h                                  |    |    |    |                                     |    |    |    |
| 15                                  | 14 | 13 | 12 | 11                                  | 10 | 9  | 8  |
| RESERVED                            |    |    |    | CONTROLSS_PLL_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                                |    |    |    | R/W                                 |    |    |    |
| 0h                                  |    |    |    | 0h                                  |    |    |    |
| 7                                   | 6  | 5  | 4  | 3                                   | 2  | 1  | 0  |
| CONTROLSS_PLL_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                     |    |    |    |
| R/W                                 |    |    |    |                                     |    |    |    |
| 0h                                  |    |    |    |                                     |    |    |    |

**Table 2-2469. MSS\_RCM\_CONTROLSS\_PLL\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|-------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 11:0  | CONTROLSS_PLL_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for CONTROLSS_PLL. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register.<br>Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - EXT_REFCLK<br>0x222 - DPLL_CORE_HSDIV0_CLKOUT2<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT0<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - RCCLK10M |

### 2.6.2.36 MSS\_RCM\_MSS\_I2C\_CLK\_SRC\_SEL Register

#### 1 MSS\_RCM\_MSS\_I2C\_CLK\_SRC\_SEL Register (Offset = 164h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-2470. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8164h       |

**Figure 2-822. MSS\_RCM\_MSS\_I2C\_CLK\_SRC\_SEL Name Register**

|                               |    |    |    |                               |    |    |    |
|-------------------------------|----|----|----|-------------------------------|----|----|----|
| 31                            | 30 | 29 | 28 | 27                            | 26 | 25 | 24 |
| RESERVED                      |    |    |    |                               |    |    |    |
| NONE                          |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |
| 23                            | 22 | 21 | 20 | 19                            | 18 | 17 | 16 |
| RESERVED                      |    |    |    |                               |    |    |    |
| NONE                          |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |
| 15                            | 14 | 13 | 12 | 11                            | 10 | 9  | 8  |
| RESERVED                      |    |    |    | MSS_I2C_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                          |    |    |    | R/W                           |    |    |    |
| 0h                            |    |    |    | 0h                            |    |    |    |
| 7                             | 6  | 5  | 4  | 3                             | 2  | 1  | 0  |
| MSS_I2C_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                               |    |    |    |
| R/W                           |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |

**Table 2-2472. MSS\_RCM\_MSS\_I2C\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                         | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|-------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                      | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 11:0  | MSS_I2C_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for I2C. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register.<br>Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - EXT_REFCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT0<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - RCCLK10M |

### 2.6.2.37 MSS\_RCM\_MSS\_LIN0\_UART0\_CLK\_SRC\_SEL Register

#### 1 MSS\_RCM\_MSS\_LIN0\_UART0\_CLK\_SRC\_SEL Register (Offset = 174h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-2473. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8174h       |

**Figure 2-823. MSS\_RCM\_MSS\_LIN0\_UART0\_CLK\_SRC\_SEL Name Register**

|                                      |    |    |    |                                      |    |    |    |
|--------------------------------------|----|----|----|--------------------------------------|----|----|----|
| 31                                   | 30 | 29 | 28 | 27                                   | 26 | 25 | 24 |
| RESERVED                             |    |    |    |                                      |    |    |    |
| NONE                                 |    |    |    |                                      |    |    |    |
| 0h                                   |    |    |    |                                      |    |    |    |
| 23                                   | 22 | 21 | 20 | 19                                   | 18 | 17 | 16 |
| RESERVED                             |    |    |    |                                      |    |    |    |
| NONE                                 |    |    |    |                                      |    |    |    |
| 0h                                   |    |    |    |                                      |    |    |    |
| 15                                   | 14 | 13 | 12 | 11                                   | 10 | 9  | 8  |
| RESERVED                             |    |    |    | MSS_LIN0_UART0_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                                 |    |    |    | R/W                                  |    |    |    |
| 0h                                   |    |    |    | 0h                                   |    |    |    |
| 7                                    | 6  | 5  | 4  | 3                                    | 2  | 1  | 0  |
| MSS_LIN0_UART0_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                      |    |    |    |
| R/W                                  |    |    |    |                                      |    |    |    |
| 0h                                   |    |    |    |                                      |    |    |    |

**Table 2-2475. MSS\_RCM\_MSS\_LIN0\_UART0\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                                | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|--------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 11:0  | MSS_LIN0_UART0_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for corresponding UART and LIN. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register.<br>Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - EXT_REFCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT0<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - DPLL_PER_HSDIV0_CLKOUT0 |

### 2.6.2.38 MSS\_RCM\_MSS\_LIN1\_UART1\_CLK\_SRC\_SEL Register

#### 1 MSS\_RCM\_MSS\_LIN1\_UART1\_CLK\_SRC\_SEL Register (Offset = 178h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-2476. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8178h       |

**Figure 2-824. MSS\_RCM\_MSS\_LIN1\_UART1\_CLK\_SRC\_SEL Name Register**

|                                      |    |    |    |                                      |    |    |    |
|--------------------------------------|----|----|----|--------------------------------------|----|----|----|
| 31                                   | 30 | 29 | 28 | 27                                   | 26 | 25 | 24 |
| RESERVED                             |    |    |    |                                      |    |    |    |
| NONE                                 |    |    |    |                                      |    |    |    |
| 0h                                   |    |    |    |                                      |    |    |    |
| 23                                   | 22 | 21 | 20 | 19                                   | 18 | 17 | 16 |
| RESERVED                             |    |    |    |                                      |    |    |    |
| NONE                                 |    |    |    |                                      |    |    |    |
| 0h                                   |    |    |    |                                      |    |    |    |
| 15                                   | 14 | 13 | 12 | 11                                   | 10 | 9  | 8  |
| RESERVED                             |    |    |    | MSS_LIN1_UART1_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                                 |    |    |    | R/W                                  |    |    |    |
| 0h                                   |    |    |    | 0h                                   |    |    |    |
| 7                                    | 6  | 5  | 4  | 3                                    | 2  | 1  | 0  |
| MSS_LIN1_UART1_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                      |    |    |    |
| R/W                                  |    |    |    |                                      |    |    |    |
| 0h                                   |    |    |    |                                      |    |    |    |

**Table 2-2478. MSS\_RCM\_MSS\_LIN1\_UART1\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                                | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|--------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 11:0  | MSS_LIN1_UART1_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for corresponding UART and LIN. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register.<br>Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - EXT_REFCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT0<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - DPLL_PER_HSDIV0_CLKOUT0 |

### 2.6.2.39 MSS\_RCM\_MSS\_LIN2\_UART2\_CLK\_SRC\_SEL Register

#### 1 MSS\_RCM\_MSS\_LIN2\_UART2\_CLK\_SRC\_SEL Register (Offset = 17Ch) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-2479. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 817Ch       |

**Figure 2-825. MSS\_RCM\_MSS\_LIN2\_UART2\_CLK\_SRC\_SEL Name Register**

|                                      |    |    |    |                                      |    |    |    |
|--------------------------------------|----|----|----|--------------------------------------|----|----|----|
| 31                                   | 30 | 29 | 28 | 27                                   | 26 | 25 | 24 |
| RESERVED                             |    |    |    |                                      |    |    |    |
| NONE                                 |    |    |    |                                      |    |    |    |
| 0h                                   |    |    |    |                                      |    |    |    |
| 23                                   | 22 | 21 | 20 | 19                                   | 18 | 17 | 16 |
| RESERVED                             |    |    |    |                                      |    |    |    |
| NONE                                 |    |    |    |                                      |    |    |    |
| 0h                                   |    |    |    |                                      |    |    |    |
| 15                                   | 14 | 13 | 12 | 11                                   | 10 | 9  | 8  |
| RESERVED                             |    |    |    | MSS_LIN2_UART2_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                                 |    |    |    | R/W                                  |    |    |    |
| 0h                                   |    |    |    | 0h                                   |    |    |    |
| 7                                    | 6  | 5  | 4  | 3                                    | 2  | 1  | 0  |
| MSS_LIN2_UART2_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                      |    |    |    |
| R/W                                  |    |    |    |                                      |    |    |    |
| 0h                                   |    |    |    |                                      |    |    |    |

**Table 2-2481. MSS\_RCM\_MSS\_LIN2\_UART2\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                                | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|--------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 11:0  | MSS_LIN2_UART2_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for corresponding UART and LIN. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register.<br>Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - EXT_REFCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT0<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - DPLL_PER_HSDIV0_CLKOUT0 |

## 2.6.2.40 MSS\_RCM\_MSS\_LIN3\_UART3\_CLK\_SRC\_SEL Register

### 1 MSS\_RCM\_MSS\_LIN3\_UART3\_CLK\_SRC\_SEL Register (Offset = 180h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-2482. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8180h       |

**Figure 2-826. MSS\_RCM\_MSS\_LIN3\_UART3\_CLK\_SRC\_SEL Name Register**

|                                      |    |    |    |                                      |    |    |    |
|--------------------------------------|----|----|----|--------------------------------------|----|----|----|
| 31                                   | 30 | 29 | 28 | 27                                   | 26 | 25 | 24 |
| RESERVED                             |    |    |    |                                      |    |    |    |
| NONE                                 |    |    |    |                                      |    |    |    |
| 0h                                   |    |    |    |                                      |    |    |    |
| 23                                   | 22 | 21 | 20 | 19                                   | 18 | 17 | 16 |
| RESERVED                             |    |    |    |                                      |    |    |    |
| NONE                                 |    |    |    |                                      |    |    |    |
| 0h                                   |    |    |    |                                      |    |    |    |
| 15                                   | 14 | 13 | 12 | 11                                   | 10 | 9  | 8  |
| RESERVED                             |    |    |    | MSS_LIN3_UART3_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                                 |    |    |    | R/W                                  |    |    |    |
| 0h                                   |    |    |    | 0h                                   |    |    |    |
| 7                                    | 6  | 5  | 4  | 3                                    | 2  | 1  | 0  |
| MSS_LIN3_UART3_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                      |    |    |    |
| R/W                                  |    |    |    |                                      |    |    |    |
| 0h                                   |    |    |    |                                      |    |    |    |

**Table 2-2484. MSS\_RCM\_MSS\_LIN3\_UART3\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                                | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|--------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 11:0  | MSS_LIN3_UART3_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for corresponding UART and LIN. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register.<br>Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - EXT_REFCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT0<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - DPLL_PER_HSDIV0_CLKOUT0 |



### 2.6.2.41 MSS\_RCM\_MSS\_LIN4\_UART4\_CLK\_SRC\_SEL Register

#### 1 MSS\_RCM\_MSS\_LIN4\_UART4\_CLK\_SRC\_SEL Register (Offset = 184h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-2485. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8184h       |

**Figure 2-827. MSS\_RCM\_MSS\_LIN4\_UART4\_CLK\_SRC\_SEL Name Register**

|                                      |    |    |    |                                      |    |    |    |
|--------------------------------------|----|----|----|--------------------------------------|----|----|----|
| 31                                   | 30 | 29 | 28 | 27                                   | 26 | 25 | 24 |
| RESERVED                             |    |    |    |                                      |    |    |    |
| NONE                                 |    |    |    |                                      |    |    |    |
| 0h                                   |    |    |    |                                      |    |    |    |
| 23                                   | 22 | 21 | 20 | 19                                   | 18 | 17 | 16 |
| RESERVED                             |    |    |    |                                      |    |    |    |
| NONE                                 |    |    |    |                                      |    |    |    |
| 0h                                   |    |    |    |                                      |    |    |    |
| 15                                   | 14 | 13 | 12 | 11                                   | 10 | 9  | 8  |
| RESERVED                             |    |    |    | MSS_LIN4_UART4_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                                 |    |    |    | R/W                                  |    |    |    |
| 0h                                   |    |    |    | 0h                                   |    |    |    |
| 7                                    | 6  | 5  | 4  | 3                                    | 2  | 1  | 0  |
| MSS_LIN4_UART4_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                      |    |    |    |
| R/W                                  |    |    |    |                                      |    |    |    |
| 0h                                   |    |    |    |                                      |    |    |    |

**Table 2-2487. MSS\_RCM\_MSS\_LIN4\_UART4\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                                | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|--------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 11:0  | MSS_LIN4_UART4_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for corresponding UART and LIN. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register.<br>Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - EXT_REFCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT0<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - DPLL_PER_HSDIV0_CLKOUT0 |

## 2.6.2.42 MSS\_RCM\_MSS\_LIN5\_UART5\_CLK\_SRC\_SEL Register

### 1 MSS\_RCM\_MSS\_LIN5\_UART5\_CLK\_SRC\_SEL Register (Offset = 188h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-2488. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8188h       |

**Figure 2-828. MSS\_RCM\_MSS\_LIN5\_UART5\_CLK\_SRC\_SEL Name Register**

|                                      |    |    |    |                                      |    |    |    |
|--------------------------------------|----|----|----|--------------------------------------|----|----|----|
| 31                                   | 30 | 29 | 28 | 27                                   | 26 | 25 | 24 |
| RESERVED                             |    |    |    |                                      |    |    |    |
| NONE                                 |    |    |    |                                      |    |    |    |
| 0h                                   |    |    |    |                                      |    |    |    |
| 23                                   | 22 | 21 | 20 | 19                                   | 18 | 17 | 16 |
| RESERVED                             |    |    |    |                                      |    |    |    |
| NONE                                 |    |    |    |                                      |    |    |    |
| 0h                                   |    |    |    |                                      |    |    |    |
| 15                                   | 14 | 13 | 12 | 11                                   | 10 | 9  | 8  |
| RESERVED                             |    |    |    | MSS_LIN5_UART5_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                                 |    |    |    | R/W                                  |    |    |    |
| 0h                                   |    |    |    | 0h                                   |    |    |    |
| 7                                    | 6  | 5  | 4  | 3                                    | 2  | 1  | 0  |
| MSS_LIN5_UART5_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                      |    |    |    |
| R/W                                  |    |    |    |                                      |    |    |    |
| 0h                                   |    |    |    |                                      |    |    |    |

**Table 2-2490. MSS\_RCM\_MSS\_LIN5\_UART5\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                                | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|--------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                             | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 11:0  | MSS_LIN5_UART5_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for corresponding UART and LIN. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register.<br>Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - EXT_REFCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - DPLL_CORE_HSDIV0_CLKOUT0<br>0x555 - RCCLK10M<br>0x666 - XTALCLK<br>0x777 - DPLL_PER_HSDIV0_CLKOUT0 |

### 2.6.2.43 MSS\_RCM\_MSS\_MCAN0\_CLK\_DIV\_VAL Register

#### 1 MSS\_RCM\_MSS\_MCAN0\_CLK\_DIV\_VAL Register (Offset = 200h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-2491. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8200h       |

**Figure 2-829. MSS\_RCM\_MSS\_MCAN0\_CLK\_DIV\_VAL Name Register**

|                               |    |    |    |                               |    |    |    |
|-------------------------------|----|----|----|-------------------------------|----|----|----|
| 31                            | 30 | 29 | 28 | 27                            | 26 | 25 | 24 |
| RESERVED                      |    |    |    |                               |    |    |    |
| NONE                          |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |
| 23                            | 22 | 21 | 20 | 19                            | 18 | 17 | 16 |
| RESERVED                      |    |    |    |                               |    |    |    |
| NONE                          |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |
| 15                            | 14 | 13 | 12 | 11                            | 10 | 9  | 8  |
| RESERVED                      |    |    |    | MSS_MCAN0_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                          |    |    |    | R/W                           |    |    |    |
| 0h                            |    |    |    | 0h                            |    |    |    |
| 7                             | 6  | 5  | 4  | 3                             | 2  | 1  | 0  |
| MSS_MCAN0_CLK_DIV_VAL_CLKDIVR |    |    |    |                               |    |    |    |
| R/W                           |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |

**Table 2-2493. MSS\_RCM\_MSS\_MCAN0\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                         | Type | Reset | Description                                                                                                                                                                                                                                                                |
|-------|-------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                      | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                   |
| 11:0  | MSS_MCAN0_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value corresponding MCAN selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

### 2.6.2.44 MSS\_RCM\_MSS\_MCAN1\_CLK\_DIV\_VAL Register

#### 1 MSS\_RCM\_MSS\_MCAN1\_CLK\_DIV\_VAL Register (Offset = 204h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2494. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8204h       |

**Figure 2-830. MSS\_RCM\_MSS\_MCAN1\_CLK\_DIV\_VAL Name Register**

|                               |    |    |    |                               |    |    |    |
|-------------------------------|----|----|----|-------------------------------|----|----|----|
| 31                            | 30 | 29 | 28 | 27                            | 26 | 25 | 24 |
| RESERVED                      |    |    |    |                               |    |    |    |
| NONE                          |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |
| 23                            | 22 | 21 | 20 | 19                            | 18 | 17 | 16 |
| RESERVED                      |    |    |    |                               |    |    |    |
| NONE                          |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |
| 15                            | 14 | 13 | 12 | 11                            | 10 | 9  | 8  |
| RESERVED                      |    |    |    | MSS_MCAN1_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                          |    |    |    | R/W                           |    |    |    |
| 0h                            |    |    |    | 0h                            |    |    |    |
| 7                             | 6  | 5  | 4  | 3                             | 2  | 1  | 0  |
| MSS_MCAN1_CLK_DIV_VAL_CLKDIVR |    |    |    |                               |    |    |    |
| R/W                           |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |

**Table 2-2496. MSS\_RCM\_MSS\_MCAN1\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                         | Type | Reset | Description                                                                                                                                                                                                                                                                |
|-------|-------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                      | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                   |
| 11:0  | MSS_MCAN1_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value corresponding MCAN selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

### 2.6.2.45 MSS\_RCM\_MSS\_MCAN2\_CLK\_DIV\_VAL Register

#### 1 MSS\_RCM\_MSS\_MCAN2\_CLK\_DIV\_VAL Register (Offset = 208h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2497. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8208h       |

**Figure 2-831. MSS\_RCM\_MSS\_MCAN2\_CLK\_DIV\_VAL Name Register**

|                               |    |    |    |                               |    |    |    |
|-------------------------------|----|----|----|-------------------------------|----|----|----|
| 31                            | 30 | 29 | 28 | 27                            | 26 | 25 | 24 |
| RESERVED                      |    |    |    |                               |    |    |    |
| NONE                          |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |
| 23                            | 22 | 21 | 20 | 19                            | 18 | 17 | 16 |
| RESERVED                      |    |    |    |                               |    |    |    |
| NONE                          |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |
| 15                            | 14 | 13 | 12 | 11                            | 10 | 9  | 8  |
| RESERVED                      |    |    |    | MSS_MCAN2_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                          |    |    |    | R/W                           |    |    |    |
| 0h                            |    |    |    | 0h                            |    |    |    |
| 7                             | 6  | 5  | 4  | 3                             | 2  | 1  | 0  |
| MSS_MCAN2_CLK_DIV_VAL_CLKDIVR |    |    |    |                               |    |    |    |
| R/W                           |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |

**Table 2-2499. MSS\_RCM\_MSS\_MCAN2\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                         | Type | Reset | Description                                                                                                                                                                                                                                                                |
|-------|-------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                      | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                   |
| 11:0  | MSS_MCAN2_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value corresponding MCAN selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

## 2.6.2.46 MSS\_RCM\_MSS\_MCAN3\_CLK\_DIV\_VAL Register

### 1 MSS\_RCM\_MSS\_MCAN3\_CLK\_DIV\_VAL Register (Offset = 20Ch) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2500. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 820Ch       |

**Figure 2-832. MSS\_RCM\_MSS\_MCAN3\_CLK\_DIV\_VAL Name Register**

|                               |    |    |    |                               |    |    |    |
|-------------------------------|----|----|----|-------------------------------|----|----|----|
| 31                            | 30 | 29 | 28 | 27                            | 26 | 25 | 24 |
| RESERVED                      |    |    |    |                               |    |    |    |
| NONE                          |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |
| 23                            | 22 | 21 | 20 | 19                            | 18 | 17 | 16 |
| RESERVED                      |    |    |    |                               |    |    |    |
| NONE                          |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |
| 15                            | 14 | 13 | 12 | 11                            | 10 | 9  | 8  |
| RESERVED                      |    |    |    | MSS_MCAN3_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                          |    |    |    | R/W                           |    |    |    |
| 0h                            |    |    |    | 0h                            |    |    |    |
| 7                             | 6  | 5  | 4  | 3                             | 2  | 1  | 0  |
| MSS_MCAN3_CLK_DIV_VAL_CLKDIVR |    |    |    |                               |    |    |    |
| R/W                           |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |

**Table 2-2502. MSS\_RCM\_MSS\_MCAN3\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                         | Type | Reset | Description                                                                                                                                                                                                                                                                |
|-------|-------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                      | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                   |
| 11:0  | MSS_MCAN3_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value corresponding MCAN selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

### 2.6.2.47 MSS\_RCM\_MSS\_QSPI\_CLK\_DIV\_VAL Register

#### 1 MSS\_RCM\_MSS\_QSPI\_CLK\_DIV\_VAL Register (Offset = 210h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2503. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8210h       |

**Figure 2-833. MSS\_RCM\_MSS\_QSPI\_CLK\_DIV\_VAL Name Register**

|                              |    |    |    |                              |    |    |    |
|------------------------------|----|----|----|------------------------------|----|----|----|
| 31                           | 30 | 29 | 28 | 27                           | 26 | 25 | 24 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 23                           | 22 | 21 | 20 | 19                           | 18 | 17 | 16 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 15                           | 14 | 13 | 12 | 11                           | 10 | 9  | 8  |
| RESERVED                     |    |    |    | MSS_QSPI_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                         |    |    |    | R/W                          |    |    |    |
| 0h                           |    |    |    | 0h                           |    |    |    |
| 7                            | 6  | 5  | 4  | 3                            | 2  | 1  | 0  |
| MSS_QSPI_CLK_DIV_VAL_CLKDIVR |    |    |    |                              |    |    |    |
| R/W                          |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |

**Table 2-2505. MSS\_RCM\_MSS\_QSPI\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                                                                                                                                                                                                                                |
|-------|------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                     | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                   |
| 11:0  | MSS_QSPI_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value corresponding QSPI selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

## 2.6.2.48 MSS\_RCM\_MSS\_RTIO\_CLK\_DIV\_VAL Register

### 1 MSS\_RCM\_MSS\_RTIO\_CLK\_DIV\_VAL Register (Offset = 214h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2506. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8214h       |

**Figure 2-834. MSS\_RCM\_MSS\_RTIO\_CLK\_DIV\_VAL Name Register**

|                              |    |    |    |                              |    |    |    |
|------------------------------|----|----|----|------------------------------|----|----|----|
| 31                           | 30 | 29 | 28 | 27                           | 26 | 25 | 24 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 23                           | 22 | 21 | 20 | 19                           | 18 | 17 | 16 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 15                           | 14 | 13 | 12 | 11                           | 10 | 9  | 8  |
| RESERVED                     |    |    |    | MSS_RTIO_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                         |    |    |    | R/W                          |    |    |    |
| 0h                           |    |    |    | 0h                           |    |    |    |
| 7                            | 6  | 5  | 4  | 3                            | 2  | 1  | 0  |
| MSS_RTIO_CLK_DIV_VAL_CLKDIVR |    |    |    |                              |    |    |    |
| R/W                          |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |

**Table 2-2508. MSS\_RCM\_MSS\_RTIO\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                                                                                                                                                                                                                               |
|-------|------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                     | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                  |
| 11:0  | MSS_RTIO_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value Corresponding RTI selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |



## 2.6.2.49 MSS\_RCM\_MSS\_RT11\_CLK\_DIV\_VAL Register

### 1 MSS\_RCM\_MSS\_RT11\_CLK\_DIV\_VAL Register (Offset = 218h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2509. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8218h       |

**Figure 2-835. MSS\_RCM\_MSS\_RT11\_CLK\_DIV\_VAL Name Register**

|                              |    |    |    |                              |    |    |    |
|------------------------------|----|----|----|------------------------------|----|----|----|
| 31                           | 30 | 29 | 28 | 27                           | 26 | 25 | 24 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 23                           | 22 | 21 | 20 | 19                           | 18 | 17 | 16 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 15                           | 14 | 13 | 12 | 11                           | 10 | 9  | 8  |
| RESERVED                     |    |    |    | MSS_RT11_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                         |    |    |    | R/W                          |    |    |    |
| 0h                           |    |    |    | 0h                           |    |    |    |
| 7                            | 6  | 5  | 4  | 3                            | 2  | 1  | 0  |
| MSS_RT11_CLK_DIV_VAL_CLKDIVR |    |    |    |                              |    |    |    |
| R/W                          |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |

**Table 2-2511. MSS\_RCM\_MSS\_RT11\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                                                                                                                                                                                                                               |
|-------|------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                     | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                  |
| 11:0  | MSS_RT11_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value Corresponding RTI selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

### 2.6.2.50 MSS\_RCM\_MSS\_RT12\_CLK\_DIV\_VAL Register

#### 1 MSS\_RCM\_MSS\_RT12\_CLK\_DIV\_VAL Register (Offset = 21Ch) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2512. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 821Ch       |

**Figure 2-836. MSS\_RCM\_MSS\_RT12\_CLK\_DIV\_VAL Name Register**

|                              |    |    |    |                              |    |    |    |
|------------------------------|----|----|----|------------------------------|----|----|----|
| 31                           | 30 | 29 | 28 | 27                           | 26 | 25 | 24 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 23                           | 22 | 21 | 20 | 19                           | 18 | 17 | 16 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 15                           | 14 | 13 | 12 | 11                           | 10 | 9  | 8  |
| RESERVED                     |    |    |    | MSS_RT12_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                         |    |    |    | R/W                          |    |    |    |
| 0h                           |    |    |    | 0h                           |    |    |    |
| 7                            | 6  | 5  | 4  | 3                            | 2  | 1  | 0  |
| MSS_RT12_CLK_DIV_VAL_CLKDIVR |    |    |    |                              |    |    |    |
| R/W                          |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |

**Table 2-2514. MSS\_RCM\_MSS\_RT12\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                                                                                                                                                                                                                               |
|-------|------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                     | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                  |
| 11:0  | MSS_RT12_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value Corresponding RTI selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

### 2.6.2.51 MSS\_RCM\_MSS\_RT13\_CLK\_DIV\_VAL Register

#### 1 MSS\_RCM\_MSS\_RT13\_CLK\_DIV\_VAL Register (Offset = 220h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2515. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8220h       |

**Figure 2-837. MSS\_RCM\_MSS\_RT13\_CLK\_DIV\_VAL Name Register**

|                              |    |    |    |                              |    |    |    |
|------------------------------|----|----|----|------------------------------|----|----|----|
| 31                           | 30 | 29 | 28 | 27                           | 26 | 25 | 24 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 23                           | 22 | 21 | 20 | 19                           | 18 | 17 | 16 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 15                           | 14 | 13 | 12 | 11                           | 10 | 9  | 8  |
| RESERVED                     |    |    |    | MSS_RT13_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                         |    |    |    | R/W                          |    |    |    |
| 0h                           |    |    |    | 0h                           |    |    |    |
| 7                            | 6  | 5  | 4  | 3                            | 2  | 1  | 0  |
| MSS_RT13_CLK_DIV_VAL_CLKDIVR |    |    |    |                              |    |    |    |
| R/W                          |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |

**Table 2-2517. MSS\_RCM\_MSS\_RT13\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                                                                                                                                                                                                                               |
|-------|------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                     | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                  |
| 11:0  | MSS_RT13_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value Corresponding RTI selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

### 2.6.2.52 MSS\_RCM\_MSS\_WDT0\_CLK\_DIV\_VAL Register

#### 1 MSS\_RCM\_MSS\_WDT0\_CLK\_DIV\_VAL Register (Offset = 228h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2518. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8228h       |

**Figure 2-838. MSS\_RCM\_MSS\_WDT0\_CLK\_DIV\_VAL Name Register**

|                              |    |    |    |                              |    |    |    |
|------------------------------|----|----|----|------------------------------|----|----|----|
| 31                           | 30 | 29 | 28 | 27                           | 26 | 25 | 24 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 23                           | 22 | 21 | 20 | 19                           | 18 | 17 | 16 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 15                           | 14 | 13 | 12 | 11                           | 10 | 9  | 8  |
| RESERVED                     |    |    |    | MSS_WDT0_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                         |    |    |    | R/W                          |    |    |    |
| 0h                           |    |    |    | 0h                           |    |    |    |
| 7                            | 6  | 5  | 4  | 3                            | 2  | 1  | 0  |
| MSS_WDT0_CLK_DIV_VAL_CLKDIVR |    |    |    |                              |    |    |    |
| R/W                          |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |

**Table 2-2520. MSS\_RCM\_MSS\_WDT0\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                                                                                                                                                                                                                 |
|-------|------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                     | NONE | 0h    | Reserved                                                                                                                                                                                                                                                    |
| 11:0  | MSS_WDT0_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value WDT selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

### 2.6.2.53 MSS\_RCM\_MSS\_WDT1\_CLK\_DIV\_VAL Register

#### 1 MSS\_RCM\_MSS\_WDT1\_CLK\_DIV\_VAL Register (Offset = 22Ch) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2521. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 822Ch       |

**Figure 2-839. MSS\_RCM\_MSS\_WDT1\_CLK\_DIV\_VAL Name Register**

|                              |    |    |    |                              |    |    |    |
|------------------------------|----|----|----|------------------------------|----|----|----|
| 31                           | 30 | 29 | 28 | 27                           | 26 | 25 | 24 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 23                           | 22 | 21 | 20 | 19                           | 18 | 17 | 16 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 15                           | 14 | 13 | 12 | 11                           | 10 | 9  | 8  |
| RESERVED                     |    |    |    | MSS_WDT1_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                         |    |    |    | R/W                          |    |    |    |
| 0h                           |    |    |    | 0h                           |    |    |    |
| 7                            | 6  | 5  | 4  | 3                            | 2  | 1  | 0  |
| MSS_WDT1_CLK_DIV_VAL_CLKDIVR |    |    |    |                              |    |    |    |
| R/W                          |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |

**Table 2-2523. MSS\_RCM\_MSS\_WDT1\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                                                                                                                                                                                                                 |
|-------|------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                     | NONE | 0h    | Reserved                                                                                                                                                                                                                                                    |
| 11:0  | MSS_WDT1_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value WDT selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

### 2.6.2.54 MSS\_RCM\_MSS\_WDT2\_CLK\_DIV\_VAL Register

#### 1 MSS\_RCM\_MSS\_WDT2\_CLK\_DIV\_VAL Register (Offset = 230h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2524. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8230h       |

**Figure 2-840. MSS\_RCM\_MSS\_WDT2\_CLK\_DIV\_VAL Name Register**

|                              |    |    |    |                              |    |    |    |
|------------------------------|----|----|----|------------------------------|----|----|----|
| 31                           | 30 | 29 | 28 | 27                           | 26 | 25 | 24 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 23                           | 22 | 21 | 20 | 19                           | 18 | 17 | 16 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 15                           | 14 | 13 | 12 | 11                           | 10 | 9  | 8  |
| RESERVED                     |    |    |    | MSS_WDT2_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                         |    |    |    | R/W                          |    |    |    |
| 0h                           |    |    |    | 0h                           |    |    |    |
| 7                            | 6  | 5  | 4  | 3                            | 2  | 1  | 0  |
| MSS_WDT2_CLK_DIV_VAL_CLKDIVR |    |    |    |                              |    |    |    |
| R/W                          |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |

**Table 2-2526. MSS\_RCM\_MSS\_WDT2\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                                                                                                                                                                                                                 |
|-------|------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                     | NONE | 0h    | Reserved                                                                                                                                                                                                                                                    |
| 11:0  | MSS_WDT2_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value WDT selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

### 2.6.2.55 MSS\_RCM\_MSS\_WDT3\_CLK\_DIV\_VAL Register

#### 1 MSS\_RCM\_MSS\_WDT3\_CLK\_DIV\_VAL Register (Offset = 234h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2527. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8234h       |

**Figure 2-841. MSS\_RCM\_MSS\_WDT3\_CLK\_DIV\_VAL Name Register**

|                              |    |    |    |                              |    |    |    |
|------------------------------|----|----|----|------------------------------|----|----|----|
| 31                           | 30 | 29 | 28 | 27                           | 26 | 25 | 24 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 23                           | 22 | 21 | 20 | 19                           | 18 | 17 | 16 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 15                           | 14 | 13 | 12 | 11                           | 10 | 9  | 8  |
| RESERVED                     |    |    |    | MSS_WDT3_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                         |    |    |    | R/W                          |    |    |    |
| 0h                           |    |    |    | 0h                           |    |    |    |
| 7                            | 6  | 5  | 4  | 3                            | 2  | 1  | 0  |
| MSS_WDT3_CLK_DIV_VAL_CLKDIVR |    |    |    |                              |    |    |    |
| R/W                          |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |

**Table 2-2529. MSS\_RCM\_MSS\_WDT3\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                                                                                                                                                                                                                 |
|-------|------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                     | NONE | 0h    | Reserved                                                                                                                                                                                                                                                    |
| 11:0  | MSS_WDT3_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value WDT selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

## 2.6.2.56 MSS\_RCM\_MSS\_SPI0\_CLK\_DIV\_VAL Register

### 1 MSS\_RCM\_MSS\_SPI0\_CLK\_DIV\_VAL Register (Offset = 23Ch) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2530. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 823Ch       |

**Figure 2-842. MSS\_RCM\_MSS\_SPI0\_CLK\_DIV\_VAL Name Register**

|                              |    |    |    |                              |    |    |    |
|------------------------------|----|----|----|------------------------------|----|----|----|
| 31                           | 30 | 29 | 28 | 27                           | 26 | 25 | 24 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 23                           | 22 | 21 | 20 | 19                           | 18 | 17 | 16 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 15                           | 14 | 13 | 12 | 11                           | 10 | 9  | 8  |
| RESERVED                     |    |    |    | MSS_SPI0_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                         |    |    |    | R/W                          |    |    |    |
| 0h                           |    |    |    | 0h                           |    |    |    |
| 7                            | 6  | 5  | 4  | 3                            | 2  | 1  | 0  |
| MSS_SPI0_CLK_DIV_VAL_CLKDIVR |    |    |    |                              |    |    |    |
| R/W                          |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |

**Table 2-2532. MSS\_RCM\_MSS\_SPI0\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                                                                                                                                                                                                                               |
|-------|------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                     | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                  |
| 11:0  | MSS_SPI0_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value Corresponding SPI selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |



## 2.6.2.57 MSS\_RCM\_MSS\_SPI1\_CLK\_DIV\_VAL Register

### 1 MSS\_RCM\_MSS\_SPI1\_CLK\_DIV\_VAL Register (Offset = 240h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2533. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8240h       |

**Figure 2-843. MSS\_RCM\_MSS\_SPI1\_CLK\_DIV\_VAL Name Register**

|                              |    |    |    |                              |    |    |    |
|------------------------------|----|----|----|------------------------------|----|----|----|
| 31                           | 30 | 29 | 28 | 27                           | 26 | 25 | 24 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 23                           | 22 | 21 | 20 | 19                           | 18 | 17 | 16 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 15                           | 14 | 13 | 12 | 11                           | 10 | 9  | 8  |
| RESERVED                     |    |    |    | MSS_SPI1_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                         |    |    |    | R/W                          |    |    |    |
| 0h                           |    |    |    | 0h                           |    |    |    |
| 7                            | 6  | 5  | 4  | 3                            | 2  | 1  | 0  |
| MSS_SPI1_CLK_DIV_VAL_CLKDIVR |    |    |    |                              |    |    |    |
| R/W                          |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |

**Table 2-2535. MSS\_RCM\_MSS\_SPI1\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                                                                                                                                                                                                                               |
|-------|------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                     | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                  |
| 11:0  | MSS_SPI1_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value Corresponding SPI selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

## 2.6.2.58 MSS\_RCM\_MSS\_SPI2\_CLK\_DIV\_VAL Register

### 1 MSS\_RCM\_MSS\_SPI2\_CLK\_DIV\_VAL Register (Offset = 244h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2536. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8244h       |

**Figure 2-844. MSS\_RCM\_MSS\_SPI2\_CLK\_DIV\_VAL Name Register**

|                              |    |    |    |                              |    |    |    |
|------------------------------|----|----|----|------------------------------|----|----|----|
| 31                           | 30 | 29 | 28 | 27                           | 26 | 25 | 24 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 23                           | 22 | 21 | 20 | 19                           | 18 | 17 | 16 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 15                           | 14 | 13 | 12 | 11                           | 10 | 9  | 8  |
| RESERVED                     |    |    |    | MSS_SPI2_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                         |    |    |    | R/W                          |    |    |    |
| 0h                           |    |    |    | 0h                           |    |    |    |
| 7                            | 6  | 5  | 4  | 3                            | 2  | 1  | 0  |
| MSS_SPI2_CLK_DIV_VAL_CLKDIVR |    |    |    |                              |    |    |    |
| R/W                          |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |

**Table 2-2538. MSS\_RCM\_MSS\_SPI2\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                                                                                                                                                                                                                               |
|-------|------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                     | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                  |
| 11:0  | MSS_SPI2_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value Corresponding SPI selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

## 2.6.2.59 MSS\_RCM\_MSS\_SPI3\_CLK\_DIV\_VAL Register

### 1 MSS\_RCM\_MSS\_SPI3\_CLK\_DIV\_VAL Register (Offset = 248h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2539. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8248h       |

**Figure 2-845. MSS\_RCM\_MSS\_SPI3\_CLK\_DIV\_VAL Name Register**

|                              |    |    |    |                              |    |    |    |
|------------------------------|----|----|----|------------------------------|----|----|----|
| 31                           | 30 | 29 | 28 | 27                           | 26 | 25 | 24 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 23                           | 22 | 21 | 20 | 19                           | 18 | 17 | 16 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 15                           | 14 | 13 | 12 | 11                           | 10 | 9  | 8  |
| RESERVED                     |    |    |    | MSS_SPI3_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                         |    |    |    | R/W                          |    |    |    |
| 0h                           |    |    |    | 0h                           |    |    |    |
| 7                            | 6  | 5  | 4  | 3                            | 2  | 1  | 0  |
| MSS_SPI3_CLK_DIV_VAL_CLKDIVR |    |    |    |                              |    |    |    |
| R/W                          |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |

**Table 2-2541. MSS\_RCM\_MSS\_SPI3\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                                                                                                                                                                                                                               |
|-------|------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                     | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                  |
| 11:0  | MSS_SPI3_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value Corresponding SPI selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

### 2.6.2.60 MSS\_RCM\_MSS\_SPI4\_CLK\_DIV\_VAL Register

#### 1 MSS\_RCM\_MSS\_SPI4\_CLK\_DIV\_VAL Register (Offset = 24Ch) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2542. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 824Ch       |

**Figure 2-846. MSS\_RCM\_MSS\_SPI4\_CLK\_DIV\_VAL Name Register**

|                              |    |    |    |                              |    |    |    |
|------------------------------|----|----|----|------------------------------|----|----|----|
| 31                           | 30 | 29 | 28 | 27                           | 26 | 25 | 24 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 23                           | 22 | 21 | 20 | 19                           | 18 | 17 | 16 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 15                           | 14 | 13 | 12 | 11                           | 10 | 9  | 8  |
| RESERVED                     |    |    |    | MSS_SPI4_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                         |    |    |    | R/W                          |    |    |    |
| 0h                           |    |    |    | 0h                           |    |    |    |
| 7                            | 6  | 5  | 4  | 3                            | 2  | 1  | 0  |
| MSS_SPI4_CLK_DIV_VAL_CLKDIVR |    |    |    |                              |    |    |    |
| R/W                          |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |

**Table 2-2544. MSS\_RCM\_MSS\_SPI4\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                                                                                                                                                                                                                               |
|-------|------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                     | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                  |
| 11:0  | MSS_SPI4_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value Corresponding SPI selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

### 2.6.2.61 MSS\_RCM\_MSS\_MMCSO\_CLK\_DIV\_VAL Register

#### 1 MSS\_RCM\_MSS\_MMCSO\_CLK\_DIV\_VAL Register (Offset = 250h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2545. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8250h       |

**Figure 2-847. MSS\_RCM\_MSS\_MMCSO\_CLK\_DIV\_VAL Name Register**

|                               |    |    |    |                               |    |    |    |
|-------------------------------|----|----|----|-------------------------------|----|----|----|
| 31                            | 30 | 29 | 28 | 27                            | 26 | 25 | 24 |
| RESERVED                      |    |    |    |                               |    |    |    |
| NONE                          |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |
| 23                            | 22 | 21 | 20 | 19                            | 18 | 17 | 16 |
| RESERVED                      |    |    |    |                               |    |    |    |
| NONE                          |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |
| 15                            | 14 | 13 | 12 | 11                            | 10 | 9  | 8  |
| RESERVED                      |    |    |    | MSS_MMCSO_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                          |    |    |    | R/W                           |    |    |    |
| 0h                            |    |    |    | 0h                            |    |    |    |
| 7                             | 6  | 5  | 4  | 3                             | 2  | 1  | 0  |
| MSS_MMCSO_CLK_DIV_VAL_CLKDIVR |    |    |    |                               |    |    |    |
| R/W                           |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |

**Table 2-2547. MSS\_RCM\_MSS\_MMCSO\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                         | Type | Reset | Description                                                                                                                                                                                                                                                   |
|-------|-------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                      | NONE | 0h    | Reserved                                                                                                                                                                                                                                                      |
| 11:0  | MSS_MMCSO_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value MMCSO selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

### 2.6.2.62 MSS\_RCM\_PRU\_ICSS\_UCLK\_CLK\_DIV\_VAL Register

#### 1 MSS\_RCM\_PRU\_ICSS\_UCLK\_CLK\_DIV\_VAL Register (Offset = 254h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2548. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8254h       |

**Figure 2-848. MSS\_RCM\_PRU\_ICSS\_UCLK\_CLK\_DIV\_VAL Name Register**

|                                   |    |    |    |                                   |    |    |    |
|-----------------------------------|----|----|----|-----------------------------------|----|----|----|
| 31                                | 30 | 29 | 28 | 27                                | 26 | 25 | 24 |
| RESERVED                          |    |    |    |                                   |    |    |    |
| NONE                              |    |    |    |                                   |    |    |    |
| 0h                                |    |    |    |                                   |    |    |    |
| 23                                | 22 | 21 | 20 | 19                                | 18 | 17 | 16 |
| RESERVED                          |    |    |    |                                   |    |    |    |
| NONE                              |    |    |    |                                   |    |    |    |
| 0h                                |    |    |    |                                   |    |    |    |
| 15                                | 14 | 13 | 12 | 11                                | 10 | 9  | 8  |
| RESERVED                          |    |    |    | PRU_ICSS_UCLK_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                              |    |    |    | R/W                               |    |    |    |
| 0h                                |    |    |    | 0h                                |    |    |    |
| 7                                 | 6  | 5  | 4  | 3                                 | 2  | 1  | 0  |
| PRU_ICSS_UCLK_CLK_DIV_VAL_CLKDIVR |    |    |    |                                   |    |    |    |
| R/W                               |    |    |    |                                   |    |    |    |
| 0h                                |    |    |    |                                   |    |    |    |

**Table 2-2550. MSS\_RCM\_PRU\_ICSS\_UCLK\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                             | Type | Reset | Description                                                                                                                                                                                                                                                        |
|-------|-----------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                          | NONE | 0h    | Reserved                                                                                                                                                                                                                                                           |
| 11:0  | PRU_ICSS_UCLK_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value ICSSM_UCLK selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

### 2.6.2.63 MSS\_RCM\_MSS\_CPTS\_CLK\_DIV\_VAL Register

#### 1 MSS\_RCM\_MSS\_CPTS\_CLK\_DIV\_VAL Register (Offset = 258h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2551. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8258h       |

**Figure 2-849. MSS\_RCM\_MSS\_CPTS\_CLK\_DIV\_VAL Name Register**

|                              |    |    |    |                              |    |    |    |
|------------------------------|----|----|----|------------------------------|----|----|----|
| 31                           | 30 | 29 | 28 | 27                           | 26 | 25 | 24 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 23                           | 22 | 21 | 20 | 19                           | 18 | 17 | 16 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 15                           | 14 | 13 | 12 | 11                           | 10 | 9  | 8  |
| RESERVED                     |    |    |    | MSS_CPTS_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                         |    |    |    | R/W                          |    |    |    |
| 0h                           |    |    |    | 0h                           |    |    |    |
| 7                            | 6  | 5  | 4  | 3                            | 2  | 1  | 0  |
| MSS_CPTS_CLK_DIV_VAL_CLKDIVR |    |    |    |                              |    |    |    |
| R/W                          |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |

**Table 2-2553. MSS\_RCM\_MSS\_CPTS\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                                                                                                                                                                                                                  |
|-------|------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                     | NONE | 0h    | Reserved                                                                                                                                                                                                                                                     |
| 11:0  | MSS_CPTS_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value CPTS selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

### 2.6.2.64 MSS\_RCM\_GPMC\_CLK\_DIV\_VAL Register

#### 1 MSS\_RCM\_GPMC\_CLK\_DIV\_VAL Register (Offset = 25Ch) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2554. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 825Ch       |

**Figure 2-850. MSS\_RCM\_GPMC\_CLK\_DIV\_VAL Name Register**

|                          |    |    |    |                          |    |    |    |
|--------------------------|----|----|----|--------------------------|----|----|----|
| 31                       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED                 |    |    |    |                          |    |    |    |
| NONE                     |    |    |    |                          |    |    |    |
| 0h                       |    |    |    |                          |    |    |    |
| 23                       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED                 |    |    |    |                          |    |    |    |
| NONE                     |    |    |    |                          |    |    |    |
| 0h                       |    |    |    |                          |    |    |    |
| 15                       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED                 |    |    |    | GPMC_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                     |    |    |    | R/W                      |    |    |    |
| 0h                       |    |    |    | 0h                       |    |    |    |
| 7                        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| GPMC_CLK_DIV_VAL_CLKDIVR |    |    |    |                          |    |    |    |
| R/W                      |    |    |    |                          |    |    |    |
| 0h                       |    |    |    |                          |    |    |    |

**Table 2-2556. MSS\_RCM\_GPMC\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                                                                                                                                                                                                                  |
|-------|------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                     | NONE | 0h    | Reserved                                                                                                                                                                                                                                                     |
| 11:0  | GPMC_CLK_DIV_VAL_C<br>LKDIVR | R/W  | 0h    | Divider value GPMC selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |



### 2.6.2.65 MSS\_RCM\_CONTROLSS\_PLL\_CLK\_DIV\_VAL Register

#### 1 MSS\_RCM\_CONTROLSS\_PLL\_CLK\_DIV\_VAL Register (Offset = 260h) [reset = 0h]

CONTROLSS\_PLL\_CLK Divider Value for Control subsystem.

Return to [Summary Table](#)

**Table 2-2557. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8260h       |

**Figure 2-851. MSS\_RCM\_CONTROLSS\_PLL\_CLK\_DIV\_VAL Name Register**

|                                   |    |    |    |                                   |    |    |    |
|-----------------------------------|----|----|----|-----------------------------------|----|----|----|
| 31                                | 30 | 29 | 28 | 27                                | 26 | 25 | 24 |
| RESERVED                          |    |    |    |                                   |    |    |    |
| NONE                              |    |    |    |                                   |    |    |    |
| 0h                                |    |    |    |                                   |    |    |    |
| 23                                | 22 | 21 | 20 | 19                                | 18 | 17 | 16 |
| RESERVED                          |    |    |    |                                   |    |    |    |
| NONE                              |    |    |    |                                   |    |    |    |
| 0h                                |    |    |    |                                   |    |    |    |
| 15                                | 14 | 13 | 12 | 11                                | 10 | 9  | 8  |
| RESERVED                          |    |    |    | CONTROLSS_PLL_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                              |    |    |    | R/W                               |    |    |    |
| 0h                                |    |    |    | 0h                                |    |    |    |
| 7                                 | 6  | 5  | 4  | 3                                 | 2  | 1  | 0  |
| CONTROLSS_PLL_CLK_DIV_VAL_CLKDIVR |    |    |    |                                   |    |    |    |
| R/W                               |    |    |    |                                   |    |    |    |
| 0h                                |    |    |    |                                   |    |    |    |

**Table 2-2559. MSS\_RCM\_CONTROLSS\_PLL\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                             | Type | Reset | Description                                                                                                                                                                                                                                                           |
|-------|-----------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                          | NONE | 0h    | Reserved                                                                                                                                                                                                                                                              |
| 11:0  | CONTROLSS_PLL_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value CONTROLSS_PLL selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

## 2.6.2.66 MSS\_RCM\_MSS\_I2C\_CLK\_DIV\_VAL Register

### 1 MSS\_RCM\_MSS\_I2C\_CLK\_DIV\_VAL Register (Offset = 264h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2560. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8264h       |

**Figure 2-852. MSS\_RCM\_MSS\_I2C\_CLK\_DIV\_VAL Name Register**

|                             |    |    |    |                             |    |    |    |
|-----------------------------|----|----|----|-----------------------------|----|----|----|
| 31                          | 30 | 29 | 28 | 27                          | 26 | 25 | 24 |
| RESERVED                    |    |    |    |                             |    |    |    |
| NONE                        |    |    |    |                             |    |    |    |
| 0h                          |    |    |    |                             |    |    |    |
| 23                          | 22 | 21 | 20 | 19                          | 18 | 17 | 16 |
| RESERVED                    |    |    |    |                             |    |    |    |
| NONE                        |    |    |    |                             |    |    |    |
| 0h                          |    |    |    |                             |    |    |    |
| 15                          | 14 | 13 | 12 | 11                          | 10 | 9  | 8  |
| RESERVED                    |    |    |    | MSS_I2C_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                        |    |    |    | R/W                         |    |    |    |
| 0h                          |    |    |    | 0h                          |    |    |    |
| 7                           | 6  | 5  | 4  | 3                           | 2  | 1  | 0  |
| MSS_I2C_CLK_DIV_VAL_CLKDIVR |    |    |    |                             |    |    |    |
| R/W                         |    |    |    |                             |    |    |    |
| 0h                          |    |    |    |                             |    |    |    |

**Table 2-2562. MSS\_RCM\_MSS\_I2C\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                       | Type | Reset | Description                                                                                                                                                                                                                                                 |
|-------|-----------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                    | NONE | 0h    | Reserved                                                                                                                                                                                                                                                    |
| 11:0  | MSS_I2C_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value I2C selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

### 2.6.2.67 MSS\_RCM\_MSS\_LIN0\_UART0\_CLK\_DIV\_VAL Register

#### 1 MSS\_RCM\_MSS\_LIN0\_UART0\_CLK\_DIV\_VAL Register (Offset = 274h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2563. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8274h       |

**Figure 2-853. MSS\_RCM\_MSS\_LIN0\_UART0\_CLK\_DIV\_VAL Name Register**

|                                    |    |    |    |                                    |    |    |    |
|------------------------------------|----|----|----|------------------------------------|----|----|----|
| 31                                 | 30 | 29 | 28 | 27                                 | 26 | 25 | 24 |
| RESERVED                           |    |    |    |                                    |    |    |    |
| NONE                               |    |    |    |                                    |    |    |    |
| 0h                                 |    |    |    |                                    |    |    |    |
| 23                                 | 22 | 21 | 20 | 19                                 | 18 | 17 | 16 |
| RESERVED                           |    |    |    |                                    |    |    |    |
| NONE                               |    |    |    |                                    |    |    |    |
| 0h                                 |    |    |    |                                    |    |    |    |
| 15                                 | 14 | 13 | 12 | 11                                 | 10 | 9  | 8  |
| RESERVED                           |    |    |    | MSS_LIN0_UART0_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                               |    |    |    | R/W                                |    |    |    |
| 0h                                 |    |    |    | 0h                                 |    |    |    |
| 7                                  | 6  | 5  | 4  | 3                                  | 2  | 1  | 0  |
| MSS_LIN0_UART0_CLK_DIV_VAL_CLKDIVR |    |    |    |                                    |    |    |    |
| R/W                                |    |    |    |                                    |    |    |    |
| 0h                                 |    |    |    |                                    |    |    |    |

**Table 2-2565. MSS\_RCM\_MSS\_LIN0\_UART0\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                                                                                                                                                                                                         |
|-------|------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                            |
| 11:0  | MSS_LIN0_UART0_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value for corresponding UART and LIN selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

## 2.6.2.68 MSS\_RCM\_MSS\_LIN1\_UART1\_CLK\_DIV\_VAL Register

### 1 MSS\_RCM\_MSS\_LIN1\_UART1\_CLK\_DIV\_VAL Register (Offset = 278h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2566. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8278h       |

**Figure 2-854. MSS\_RCM\_MSS\_LIN1\_UART1\_CLK\_DIV\_VAL Name Register**

|                                    |    |    |    |                                    |    |    |    |
|------------------------------------|----|----|----|------------------------------------|----|----|----|
| 31                                 | 30 | 29 | 28 | 27                                 | 26 | 25 | 24 |
| RESERVED                           |    |    |    |                                    |    |    |    |
| NONE                               |    |    |    |                                    |    |    |    |
| 0h                                 |    |    |    |                                    |    |    |    |
| 23                                 | 22 | 21 | 20 | 19                                 | 18 | 17 | 16 |
| RESERVED                           |    |    |    |                                    |    |    |    |
| NONE                               |    |    |    |                                    |    |    |    |
| 0h                                 |    |    |    |                                    |    |    |    |
| 15                                 | 14 | 13 | 12 | 11                                 | 10 | 9  | 8  |
| RESERVED                           |    |    |    | MSS_LIN1_UART1_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                               |    |    |    | R/W                                |    |    |    |
| 0h                                 |    |    |    | 0h                                 |    |    |    |
| 7                                  | 6  | 5  | 4  | 3                                  | 2  | 1  | 0  |
| MSS_LIN1_UART1_CLK_DIV_VAL_CLKDIVR |    |    |    |                                    |    |    |    |
| R/W                                |    |    |    |                                    |    |    |    |
| 0h                                 |    |    |    |                                    |    |    |    |

**Table 2-2568. MSS\_RCM\_MSS\_LIN1\_UART1\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                                                                                                                                                                                                         |
|-------|------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                            |
| 11:0  | MSS_LIN1_UART1_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value for corresponding UART and LIN selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

## 2.6.2.69 MSS\_RCM\_MSS\_LIN2\_UART2\_CLK\_DIV\_VAL Register

### 1 MSS\_RCM\_MSS\_LIN2\_UART2\_CLK\_DIV\_VAL Register (Offset = 27Ch) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2569. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 827Ch       |

**Figure 2-855. MSS\_RCM\_MSS\_LIN2\_UART2\_CLK\_DIV\_VAL Name Register**

|                                    |    |    |    |                                    |    |    |    |
|------------------------------------|----|----|----|------------------------------------|----|----|----|
| 31                                 | 30 | 29 | 28 | 27                                 | 26 | 25 | 24 |
| RESERVED                           |    |    |    |                                    |    |    |    |
| NONE                               |    |    |    |                                    |    |    |    |
| 0h                                 |    |    |    |                                    |    |    |    |
| 23                                 | 22 | 21 | 20 | 19                                 | 18 | 17 | 16 |
| RESERVED                           |    |    |    |                                    |    |    |    |
| NONE                               |    |    |    |                                    |    |    |    |
| 0h                                 |    |    |    |                                    |    |    |    |
| 15                                 | 14 | 13 | 12 | 11                                 | 10 | 9  | 8  |
| RESERVED                           |    |    |    | MSS_LIN2_UART2_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                               |    |    |    | R/W                                |    |    |    |
| 0h                                 |    |    |    | 0h                                 |    |    |    |
| 7                                  | 6  | 5  | 4  | 3                                  | 2  | 1  | 0  |
| MSS_LIN2_UART2_CLK_DIV_VAL_CLKDIVR |    |    |    |                                    |    |    |    |
| R/W                                |    |    |    |                                    |    |    |    |
| 0h                                 |    |    |    |                                    |    |    |    |

**Table 2-2571. MSS\_RCM\_MSS\_LIN2\_UART2\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                                                                                                                                                                                                         |
|-------|------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                            |
| 11:0  | MSS_LIN2_UART2_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value for corresponding UART and LIN selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

## 2.6.2.70 MSS\_RCM\_MSS\_LIN3\_UART3\_CLK\_DIV\_VAL Register

### 1 MSS\_RCM\_MSS\_LIN3\_UART3\_CLK\_DIV\_VAL Register (Offset = 280h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2572. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8280h       |

**Figure 2-856. MSS\_RCM\_MSS\_LIN3\_UART3\_CLK\_DIV\_VAL Name Register**

|                                    |    |    |    |                                    |    |    |    |
|------------------------------------|----|----|----|------------------------------------|----|----|----|
| 31                                 | 30 | 29 | 28 | 27                                 | 26 | 25 | 24 |
| RESERVED                           |    |    |    |                                    |    |    |    |
| NONE                               |    |    |    |                                    |    |    |    |
| 0h                                 |    |    |    |                                    |    |    |    |
| 23                                 | 22 | 21 | 20 | 19                                 | 18 | 17 | 16 |
| RESERVED                           |    |    |    |                                    |    |    |    |
| NONE                               |    |    |    |                                    |    |    |    |
| 0h                                 |    |    |    |                                    |    |    |    |
| 15                                 | 14 | 13 | 12 | 11                                 | 10 | 9  | 8  |
| RESERVED                           |    |    |    | MSS_LIN3_UART3_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                               |    |    |    | R/W                                |    |    |    |
| 0h                                 |    |    |    | 0h                                 |    |    |    |
| 7                                  | 6  | 5  | 4  | 3                                  | 2  | 1  | 0  |
| MSS_LIN3_UART3_CLK_DIV_VAL_CLKDIVR |    |    |    |                                    |    |    |    |
| R/W                                |    |    |    |                                    |    |    |    |
| 0h                                 |    |    |    |                                    |    |    |    |

**Table 2-2574. MSS\_RCM\_MSS\_LIN3\_UART3\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                                                                                                                                                                                                         |
|-------|------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                            |
| 11:0  | MSS_LIN3_UART3_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value for corresponding UART and LIN selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

### 2.6.2.71 MSS\_RCM\_MSS\_LIN4\_UART4\_CLK\_DIV\_VAL Register

#### 1 MSS\_RCM\_MSS\_LIN4\_UART4\_CLK\_DIV\_VAL Register (Offset = 284h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2575. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8284h       |

**Figure 2-857. MSS\_RCM\_MSS\_LIN4\_UART4\_CLK\_DIV\_VAL Name Register**

|                                    |    |    |    |                                    |    |    |    |
|------------------------------------|----|----|----|------------------------------------|----|----|----|
| 31                                 | 30 | 29 | 28 | 27                                 | 26 | 25 | 24 |
| RESERVED                           |    |    |    |                                    |    |    |    |
| NONE                               |    |    |    |                                    |    |    |    |
| 0h                                 |    |    |    |                                    |    |    |    |
| 23                                 | 22 | 21 | 20 | 19                                 | 18 | 17 | 16 |
| RESERVED                           |    |    |    |                                    |    |    |    |
| NONE                               |    |    |    |                                    |    |    |    |
| 0h                                 |    |    |    |                                    |    |    |    |
| 15                                 | 14 | 13 | 12 | 11                                 | 10 | 9  | 8  |
| RESERVED                           |    |    |    | MSS_LIN4_UART4_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                               |    |    |    | R/W                                |    |    |    |
| 0h                                 |    |    |    | 0h                                 |    |    |    |
| 7                                  | 6  | 5  | 4  | 3                                  | 2  | 1  | 0  |
| MSS_LIN4_UART4_CLK_DIV_VAL_CLKDIVR |    |    |    |                                    |    |    |    |
| R/W                                |    |    |    |                                    |    |    |    |
| 0h                                 |    |    |    |                                    |    |    |    |

**Table 2-2577. MSS\_RCM\_MSS\_LIN4\_UART4\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                                                                                                                                                                                                         |
|-------|------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                            |
| 11:0  | MSS_LIN4_UART4_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value for corresponding UART and LIN selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

## 2.6.2.72 MSS\_RCM\_MSS\_LIN5\_UART5\_CLK\_DIV\_VAL Register

### 1 MSS\_RCM\_MSS\_LIN5\_UART5\_CLK\_DIV\_VAL Register (Offset = 288h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-2578. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8288h       |

**Figure 2-858. MSS\_RCM\_MSS\_LIN5\_UART5\_CLK\_DIV\_VAL Name Register**

|                                    |    |    |    |                                    |    |    |    |
|------------------------------------|----|----|----|------------------------------------|----|----|----|
| 31                                 | 30 | 29 | 28 | 27                                 | 26 | 25 | 24 |
| RESERVED                           |    |    |    |                                    |    |    |    |
| NONE                               |    |    |    |                                    |    |    |    |
| 0h                                 |    |    |    |                                    |    |    |    |
| 23                                 | 22 | 21 | 20 | 19                                 | 18 | 17 | 16 |
| RESERVED                           |    |    |    |                                    |    |    |    |
| NONE                               |    |    |    |                                    |    |    |    |
| 0h                                 |    |    |    |                                    |    |    |    |
| 15                                 | 14 | 13 | 12 | 11                                 | 10 | 9  | 8  |
| RESERVED                           |    |    |    | MSS_LIN5_UART5_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                               |    |    |    | R/W                                |    |    |    |
| 0h                                 |    |    |    | 0h                                 |    |    |    |
| 7                                  | 6  | 5  | 4  | 3                                  | 2  | 1  | 0  |
| MSS_LIN5_UART5_CLK_DIV_VAL_CLKDIVR |    |    |    |                                    |    |    |    |
| R/W                                |    |    |    |                                    |    |    |    |
| 0h                                 |    |    |    |                                    |    |    |    |

**Table 2-2580. MSS\_RCM\_MSS\_LIN5\_UART5\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                              | Type | Reset | Description                                                                                                                                                                                                                                                                         |
|-------|------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                            |
| 11:0  | MSS_LIN5_UART5_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value for corresponding UART and LIN selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |



### 2.6.2.73 MSS\_RCM\_MSS\_RGMII\_CLK\_DIV\_VAL Register

#### 1 MSS\_RCM\_MSS\_RGMII\_CLK\_DIV\_VAL Register (Offset = 28Ch) [reset = 111h]

RGMII 250 CLK Divider Value.

Return to [Summary Table](#)

**Table 2-2581. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 828Ch       |

**Figure 2-859. MSS\_RCM\_MSS\_RGMII\_CLK\_DIV\_VAL Name Register**

|                               |    |    |    |                               |    |    |    |
|-------------------------------|----|----|----|-------------------------------|----|----|----|
| 31                            | 30 | 29 | 28 | 27                            | 26 | 25 | 24 |
| RESERVED                      |    |    |    |                               |    |    |    |
| NONE                          |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |
| 23                            | 22 | 21 | 20 | 19                            | 18 | 17 | 16 |
| RESERVED                      |    |    |    |                               |    |    |    |
| NONE                          |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |
| 15                            | 14 | 13 | 12 | 11                            | 10 | 9  | 8  |
| RESERVED                      |    |    |    | MSS_RGMII_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                          |    |    |    | R/W                           |    |    |    |
| 0h                            |    |    |    | 111h                          |    |    |    |
| 7                             | 6  | 5  | 4  | 3                             | 2  | 1  | 0  |
| MSS_RGMII_CLK_DIV_VAL_CLKDIVR |    |    |    |                               |    |    |    |
| R/W                           |    |    |    |                               |    |    |    |
| 111h                          |    |    |    |                               |    |    |    |

**Table 2-2583. MSS\_RCM\_MSS\_RGMII\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                         | Type | Reset | Description                                                                                                                                                                                                                                                   |
|-------|-------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                      | NONE | 0h    | Reserved                                                                                                                                                                                                                                                      |
| 11:0  | MSS_RGMII_CLK_DIV_VAL_CLKDIVR | R/W  | 111h  | Divider value RGMII selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

## 2.6.2.74 MSS\_RCM\_MSS\_MII100\_CLK\_DIV\_VAL Register

### 1 MSS\_RCM\_MSS\_MII100\_CLK\_DIV\_VAL Register (Offset = 290h) [reset = 999h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2584. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8290h       |

**Figure 2-860. MSS\_RCM\_MSS\_MII100\_CLK\_DIV\_VAL Name Register**

|                                |    |    |    |                                |    |    |    |
|--------------------------------|----|----|----|--------------------------------|----|----|----|
| 31                             | 30 | 29 | 28 | 27                             | 26 | 25 | 24 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 23                             | 22 | 21 | 20 | 19                             | 18 | 17 | 16 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 15                             | 14 | 13 | 12 | 11                             | 10 | 9  | 8  |
| RESERVED                       |    |    |    | MSS_MII100_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                           |    |    |    | R/W                            |    |    |    |
| 0h                             |    |    |    | 999h                           |    |    |    |
| 7                              | 6  | 5  | 4  | 3                              | 2  | 1  | 0  |
| MSS_MII100_CLK_DIV_VAL_CLKDIVR |    |    |    |                                |    |    |    |
| R/W                            |    |    |    |                                |    |    |    |
| 999h                           |    |    |    |                                |    |    |    |

**Table 2-2586. MSS\_RCM\_MSS\_MII100\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                                                                                                                                                                                                    |
|-------|--------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                       |
| 11:0  | MSS_MII100_CLK_DIV_VAL_CLKDIVR | R/W  | 999h  | Divider value MII100 selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

### 2.6.2.75 MSS\_RCM\_MSS\_MII10\_CLK\_DIV\_VAL Register

#### 1 MSS\_RCM\_MSS\_MII10\_CLK\_DIV\_VAL Register (Offset = 294h) [reset = 636363h]

RGMII 50 CLK Divider Value.

Return to [Summary Table](#)

**Table 2-2587. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8294h       |

**Figure 2-861. MSS\_RCM\_MSS\_MII10\_CLK\_DIV\_VAL Name Register**

|                               |    |    |    |    |    |    |    |
|-------------------------------|----|----|----|----|----|----|----|
| 31                            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                      |    |    |    |    |    |    |    |
| NONE                          |    |    |    |    |    |    |    |
| 0h                            |    |    |    |    |    |    |    |
| 23                            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSS_MII10_CLK_DIV_VAL_CLKDIVR |    |    |    |    |    |    |    |
| R/W                           |    |    |    |    |    |    |    |
| 636363h                       |    |    |    |    |    |    |    |
| 15                            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_MII10_CLK_DIV_VAL_CLKDIVR |    |    |    |    |    |    |    |
| R/W                           |    |    |    |    |    |    |    |
| 636363h                       |    |    |    |    |    |    |    |
| 7                             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_MII10_CLK_DIV_VAL_CLKDIVR |    |    |    |    |    |    |    |
| R/W                           |    |    |    |    |    |    |    |
| 636363h                       |    |    |    |    |    |    |    |

**Table 2-2589. MSS\_RCM\_MSS\_MII10\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                         | Type | Reset   | Description                                                                                                                                                                                                                                                       |
|-------|-------------------------------|------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED                      | NONE | 0h      | Reserved                                                                                                                                                                                                                                                          |
| 23:0  | MSS_MII10_CLK_DIV_VAL_CLKDIVR | R/W  | 636363h | Divider value MII10 selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x15' is required then '0x151515' should be configured to the register. |

## 2.6.2.76 MSS\_RCM\_MSS\_XTAL\_32K\_CLK\_DIV\_VAL Register

### 1 MSS\_RCM\_MSS\_XTAL\_32K\_CLK\_DIV\_VAL Register (Offset = 298h) [reset = 30CC330Ch]

RGMII 5 CLK Divider Value.

Return to [Summary Table](#)

**Table 2-2590. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8298h       |

**Figure 2-862. MSS\_RCM\_MSS\_XTAL\_32K\_CLK\_DIV\_VAL Name Register**

|                                  |    |                                  |    |    |    |    |    |
|----------------------------------|----|----------------------------------|----|----|----|----|----|
| 31                               | 30 | 29                               | 28 | 27 | 26 | 25 | 24 |
| RESERVED                         |    | MSS_XTAL_32K_CLK_DIV_VAL_CLKDIVR |    |    |    |    |    |
| NONE                             |    | R/W                              |    |    |    |    |    |
| 0h                               |    | 30CC330Ch                        |    |    |    |    |    |
| 23                               | 22 | 21                               | 20 | 19 | 18 | 17 | 16 |
| MSS_XTAL_32K_CLK_DIV_VAL_CLKDIVR |    |                                  |    |    |    |    |    |
| R/W                              |    |                                  |    |    |    |    |    |
| 30CC330Ch                        |    |                                  |    |    |    |    |    |
| 15                               | 14 | 13                               | 12 | 11 | 10 | 9  | 8  |
| MSS_XTAL_32K_CLK_DIV_VAL_CLKDIVR |    |                                  |    |    |    |    |    |
| R/W                              |    |                                  |    |    |    |    |    |
| 30CC330Ch                        |    |                                  |    |    |    |    |    |
| 7                                | 6  | 5                                | 4  | 3  | 2  | 1  | 0  |
| MSS_XTAL_32K_CLK_DIV_VAL_CLKDIVR |    |                                  |    |    |    |    |    |
| R/W                              |    |                                  |    |    |    |    |    |
| 30CC330Ch                        |    |                                  |    |    |    |    |    |

**Table 2-2592. MSS\_RCM\_MSS\_XTAL\_32K\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                            | Type | Reset     | Description                                                                                                                                                                                                                                                                                                                                                              |
|-------|----------------------------------|------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | RESERVED                         | NONE | 0h        | Reserved                                                                                                                                                                                                                                                                                                                                                                 |
| 29:0  | MSS_XTAL_32K_CLK_DIV_VAL_CLKDIVR | R/W  | 30CC330Ch | Divider value for XTAL_32K clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit. For example: if divider value of '0x30C' is required then register should be configured as follows -<br>bits[9:0] = 0x30C<br>bits[19:10] = 0x30C<br>bits[29:20] = 0x30C<br>This configures the register to 0x30CC330C |

## 2.6.2.77 MSS\_RCM\_XTAL\_TEMPSENSE\_32K\_CLK\_DIV\_VAL Register

### 1 MSS\_RCM\_XTAL\_TEMPSENSE\_32K\_CLK\_DIV\_VAL Register (Offset = 29Ch) [reset = 30CC330Ch]

XTAL 32K CLK Divider Value for MMC.

Return to [Summary Table](#)

**Table 2-2593. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 829Ch       |

**Figure 2-863. MSS\_RCM\_XTAL\_TEMPSENSE\_32K\_CLK\_DIV\_VAL Name Register**

|                                        |    |                                        |    |    |    |    |    |
|----------------------------------------|----|----------------------------------------|----|----|----|----|----|
| 31                                     | 30 | 29                                     | 28 | 27 | 26 | 25 | 24 |
| RESERVED                               |    | XTAL_TEMPSENSE_32K_CLK_DIV_VAL_CLKDIVR |    |    |    |    |    |
| NONE                                   |    | R/W                                    |    |    |    |    |    |
| 0h                                     |    | 30CC330Ch                              |    |    |    |    |    |
| 23                                     | 22 | 21                                     | 20 | 19 | 18 | 17 | 16 |
| XTAL_TEMPSENSE_32K_CLK_DIV_VAL_CLKDIVR |    |                                        |    |    |    |    |    |
| R/W                                    |    |                                        |    |    |    |    |    |
| 30CC330Ch                              |    |                                        |    |    |    |    |    |
| 15                                     | 14 | 13                                     | 12 | 11 | 10 | 9  | 8  |
| XTAL_TEMPSENSE_32K_CLK_DIV_VAL_CLKDIVR |    |                                        |    |    |    |    |    |
| R/W                                    |    |                                        |    |    |    |    |    |
| 30CC330Ch                              |    |                                        |    |    |    |    |    |
| 7                                      | 6  | 5                                      | 4  | 3  | 2  | 1  | 0  |
| XTAL_TEMPSENSE_32K_CLK_DIV_VAL_CLKDIVR |    |                                        |    |    |    |    |    |
| R/W                                    |    |                                        |    |    |    |    |    |
| 30CC330Ch                              |    |                                        |    |    |    |    |    |

**Table 2-2595. MSS\_RCM\_XTAL\_TEMPSENSE\_32K\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                                  | Type | Reset     | Description                                                                                                                                                                                                                                                                                                                                                              |
|-------|----------------------------------------|------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | RESERVED                               | NONE | 0h        | Reserved                                                                                                                                                                                                                                                                                                                                                                 |
| 29:0  | XTAL_TEMPSENSE_32K_CLK_DIV_VAL_CLKDIVR | R/W  | 30CC330Ch | Divider value for XTAL_32K clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit. For example: if divider value of '0x30C' is required then register should be configured as follows -<br>bits[9:0] = 0x30C<br>bits[19:10] = 0x30C<br>bits[29:20] = 0x30C<br>This configures the register to 0x30CC330C |

## 2.6.2.78 MSS\_RCM\_MSS\_ELM\_CLK\_DIV\_VAL Register

### 1 MSS\_RCM\_MSS\_ELM\_CLK\_DIV\_VAL Register (Offset = 2A0h) [reset = 333h]

XTAL 32K CLK Divider Value for Temp Sensor.

Return to [Summary Table](#)

**Table 2-2596. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 82A0h       |

**Figure 2-864. MSS\_RCM\_MSS\_ELM\_CLK\_DIV\_VAL Name Register**

|                             |    |    |    |                             |    |    |    |
|-----------------------------|----|----|----|-----------------------------|----|----|----|
| 31                          | 30 | 29 | 28 | 27                          | 26 | 25 | 24 |
| RESERVED                    |    |    |    |                             |    |    |    |
| NONE                        |    |    |    |                             |    |    |    |
| 0h                          |    |    |    |                             |    |    |    |
| 23                          | 22 | 21 | 20 | 19                          | 18 | 17 | 16 |
| RESERVED                    |    |    |    |                             |    |    |    |
| NONE                        |    |    |    |                             |    |    |    |
| 0h                          |    |    |    |                             |    |    |    |
| 15                          | 14 | 13 | 12 | 11                          | 10 | 9  | 8  |
| RESERVED                    |    |    |    | MSS_ELM_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                        |    |    |    | R/W                         |    |    |    |
| 0h                          |    |    |    | 333h                        |    |    |    |
| 7                           | 6  | 5  | 4  | 3                           | 2  | 1  | 0  |
| MSS_ELM_CLK_DIV_VAL_CLKDIVR |    |    |    |                             |    |    |    |
| R/W                         |    |    |    |                             |    |    |    |
| 333h                        |    |    |    |                             |    |    |    |

**Table 2-2598. MSS\_RCM\_MSS\_ELM\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                       | Type | Reset | Description                                                                                                                                                                                                                                     |
|-------|-----------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                    | NONE | 0h    | Reserved                                                                                                                                                                                                                                        |
| 11:0  | MSS_ELM_CLK_DIV_VAL_CLKDIVR | R/W  | 333h  | Divider value ELM clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit. For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

## 2.6.2.79 MSS\_RCM\_MSS\_MCAN0\_CLK\_GATE Register

### 1 MSS\_RCM\_MSS\_MCAN0\_CLK\_GATE Register (Offset = 300h) [reset = 0h]

ELM CLK Divider Value.

Return to [Summary Table](#)

**Table 2-2599. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8300h       |

**Figure 2-865. MSS\_RCM\_MSS\_MCAN0\_CLK\_GATE Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | MSS_MCAN0_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-2601. MSS\_RCM\_MSS\_MCAN0\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | MSS_MCAN0_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding MCAN |

### 2.6.2.80 MSS\_RCM\_MSS\_MCAN1\_CLK\_GATE Register

#### 1 MSS\_RCM\_MSS\_MCAN1\_CLK\_GATE Register (Offset = 304h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2602. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8304h       |

**Figure 2-866. MSS\_RCM\_MSS\_MCAN1\_CLK\_GATE Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | MSS_MCAN1_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-2604. MSS\_RCM\_MSS\_MCAN1\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | MSS_MCAN1_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding MCAN |



## 2.6.2.81 MSS\_RCM\_MSS\_MCAN2\_CLK\_GATE Register

### 1 MSS\_RCM\_MSS\_MCAN2\_CLK\_GATE Register (Offset = 308h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2605. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8308h       |

**Figure 2-867. MSS\_RCM\_MSS\_MCAN2\_CLK\_GATE Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | MSS_MCAN2_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-2607. MSS\_RCM\_MSS\_MCAN2\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | MSS_MCAN2_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding MCAN |

## 2.6.2.82 MSS\_RCM\_MSS\_MCAN3\_CLK\_GATE Register

### 1 MSS\_RCM\_MSS\_MCAN3\_CLK\_GATE Register (Offset = 30Ch) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2608. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 830Ch       |

**Figure 2-868. MSS\_RCM\_MSS\_MCAN3\_CLK\_GATE Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | MSS_MCAN3_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-2610. MSS\_RCM\_MSS\_MCAN3\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | MSS_MCAN3_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding MCAN |

### 2.6.2.83 MSS\_RCM\_MSS\_QSPI\_CLK\_GATE Register

#### 1 MSS\_RCM\_MSS\_QSPI\_CLK\_GATE Register (Offset = 310h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2611. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8310h       |

**Figure 2-869. MSS\_RCM\_MSS\_QSPI\_CLK\_GATE Name Register**

|          |    |    |    |    |                         |    |    |
|----------|----|----|----|----|-------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                      | 25 | 24 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                      | 17 | 16 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                      | 9  | 8  |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                       | 1  | 0  |
| RESERVED |    |    |    |    | MSS_QSPI_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                     |    |    |
| 0h       |    |    |    |    | 0h                      |    |    |

**Table 2-2613. MSS\_RCM\_MSS\_QSPI\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                             |
|------|-------------------------|------|-------|-----------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                |
| 2:0  | MSS_QSPI_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for QSPI |

### 2.6.2.84 MSS\_RCM\_MSS\_RTIO\_CLK\_GATE Register

#### 1 MSS\_RCM\_MSS\_RTIO\_CLK\_GATE Register (Offset = 314h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2614. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8314h       |

**Figure 2-870. MSS\_RCM\_MSS\_RTIO\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_RTIO_CLK_GATE_GATED |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-2616. MSS\_RCM\_MSS\_RTIO\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                          |
|------|-------------------------|------|-------|------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                             |
| 2:0  | MSS_RTIO_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for Corresponding RTI |

### 2.6.2.85 MSS\_RCM\_MSS\_RT11\_CLK\_GATE Register

#### 1 MSS\_RCM\_MSS\_RT11\_CLK\_GATE Register (Offset = 318h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2617. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8318h       |

**Figure 2-871. MSS\_RCM\_MSS\_RT11\_CLK\_GATE Name Register**

|          |    |    |    |    |                         |    |    |
|----------|----|----|----|----|-------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                      | 25 | 24 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                      | 17 | 16 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                      | 9  | 8  |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                       | 1  | 0  |
| RESERVED |    |    |    |    | MSS_RT11_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                     |    |    |
| 0h       |    |    |    |    | 0h                      |    |    |

**Table 2-2619. MSS\_RCM\_MSS\_RT11\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                          |
|------|-------------------------|------|-------|------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                             |
| 2:0  | MSS_RT11_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for Corresponding RTI |

## 2.6.2.86 MSS\_RCM\_MSS\_RT12\_CLK\_GATE Register

### 1 MSS\_RCM\_MSS\_RT12\_CLK\_GATE Register (Offset = 31Ch) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2620. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 831Ch       |

**Figure 2-872. MSS\_RCM\_MSS\_RT12\_CLK\_GATE Name Register**

|          |    |    |    |    |                         |    |    |
|----------|----|----|----|----|-------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                      | 25 | 24 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                      | 17 | 16 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                      | 9  | 8  |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                       | 1  | 0  |
| RESERVED |    |    |    |    | MSS_RT12_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                     |    |    |
| 0h       |    |    |    |    | 0h                      |    |    |

**Table 2-2622. MSS\_RCM\_MSS\_RT12\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                          |
|------|-------------------------|------|-------|------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                             |
| 2:0  | MSS_RT12_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for Corresponding RTI |

## 2.6.2.87 MSS\_RCM\_MSS\_RT13\_CLK\_GATE Register

### 1 MSS\_RCM\_MSS\_RT13\_CLK\_GATE Register (Offset = 320h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2623. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8320h       |

**Figure 2-873. MSS\_RCM\_MSS\_RT13\_CLK\_GATE Name Register**

|          |    |    |    |    |                         |    |    |
|----------|----|----|----|----|-------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                      | 25 | 24 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                      | 17 | 16 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                      | 9  | 8  |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                       | 1  | 0  |
| RESERVED |    |    |    |    | MSS_RT13_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                     |    |    |
| 0h       |    |    |    |    | 0h                      |    |    |

**Table 2-2625. MSS\_RCM\_MSS\_RT13\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                          |
|------|-------------------------|------|-------|------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                             |
| 2:0  | MSS_RT13_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for Corresponding RTI |

### 2.6.2.88 MSS\_RCM\_MSS\_WDT0\_CLK\_GATE Register

#### 1 MSS\_RCM\_MSS\_WDT0\_CLK\_GATE Register (Offset = 328h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2626. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8328h       |

**Figure 2-874. MSS\_RCM\_MSS\_WDT0\_CLK\_GATE Name Register**

|          |    |    |    |    |                         |    |    |
|----------|----|----|----|----|-------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                      | 25 | 24 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                      | 17 | 16 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                      | 9  | 8  |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                       | 1  | 0  |
| RESERVED |    |    |    |    | MSS_WDT0_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                     |    |    |
| 0h       |    |    |    |    | 0h                      |    |    |

**Table 2-2628. MSS\_RCM\_MSS\_WDT0\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                          |
|------|-------------------------|------|-------|------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                             |
| 2:0  | MSS_WDT0_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding WDT |



## 2.6.2.89 MSS\_RCM\_MSS\_WDT1\_CLK\_GATE Register

### 1 MSS\_RCM\_MSS\_WDT1\_CLK\_GATE Register (Offset = 32Ch) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2629. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 832Ch       |

**Figure 2-875. MSS\_RCM\_MSS\_WDT1\_CLK\_GATE Name Register**

|          |    |    |    |    |                         |    |    |
|----------|----|----|----|----|-------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                      | 25 | 24 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                      | 17 | 16 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                      | 9  | 8  |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                       | 1  | 0  |
| RESERVED |    |    |    |    | MSS_WDT1_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                     |    |    |
| 0h       |    |    |    |    | 0h                      |    |    |

**Table 2-2631. MSS\_RCM\_MSS\_WDT1\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                          |
|------|-------------------------|------|-------|------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                             |
| 2:0  | MSS_WDT1_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding WDT |

## 2.6.2.90 MSS\_RCM\_MSS\_WDT2\_CLK\_GATE Register

### 1 MSS\_RCM\_MSS\_WDT2\_CLK\_GATE Register (Offset = 330h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2632. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8330h       |

**Figure 2-876. MSS\_RCM\_MSS\_WDT2\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_WDT2_CLK_GATE_GATED |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-2634. MSS\_RCM\_MSS\_WDT2\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                          |
|------|-------------------------|------|-------|------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                             |
| 2:0  | MSS_WDT2_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding WDT |

### 2.6.2.91 MSS\_RCM\_MSS\_WDT3\_CLK\_GATE Register

#### 1 MSS\_RCM\_MSS\_WDT3\_CLK\_GATE Register (Offset = 334h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2635. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8334h       |

**Figure 2-877. MSS\_RCM\_MSS\_WDT3\_CLK\_GATE Name Register**

|          |    |    |    |    |                         |    |    |
|----------|----|----|----|----|-------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                      | 25 | 24 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                      | 17 | 16 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                      | 9  | 8  |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                       | 1  | 0  |
| RESERVED |    |    |    |    | MSS_WDT3_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                     |    |    |
| 0h       |    |    |    |    | 0h                      |    |    |

**Table 2-2637. MSS\_RCM\_MSS\_WDT3\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                          |
|------|-------------------------|------|-------|------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                             |
| 2:0  | MSS_WDT3_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding WDT |

## 2.6.2.92 MSS\_RCM\_MSS\_SPI0\_CLK\_GATE Register

### 1 MSS\_RCM\_MSS\_SPI0\_CLK\_GATE Register (Offset = 33Ch) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2638. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 833Ch       |

**Figure 2-878. MSS\_RCM\_MSS\_SPI0\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_SPI0_CLK_GATE_GATED |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-2640. MSS\_RCM\_MSS\_SPI0\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                          |
|------|-------------------------|------|-------|------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                             |
| 2:0  | MSS_SPI0_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for Corresponding SPI |

### 2.6.2.93 MSS\_RCM\_MSS\_SPI1\_CLK\_GATE Register

#### 1 MSS\_RCM\_MSS\_SPI1\_CLK\_GATE Register (Offset = 340h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2641. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8340h       |

**Figure 2-879. MSS\_RCM\_MSS\_SPI1\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_SPI1_CLK_GATE_GATED |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-2643. MSS\_RCM\_MSS\_SPI1\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                          |
|------|-------------------------|------|-------|------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                             |
| 2:0  | MSS_SPI1_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for Corresponding SPI |

## 2.6.2.94 MSS\_RCM\_MSS\_SPI2\_CLK\_GATE Register

### 1 MSS\_RCM\_MSS\_SPI2\_CLK\_GATE Register (Offset = 344h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2644. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8344h       |

**Figure 2-880. MSS\_RCM\_MSS\_SPI2\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_SPI2_CLK_GATE_GATED |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-2646. MSS\_RCM\_MSS\_SPI2\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                          |
|------|-------------------------|------|-------|------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                             |
| 2:0  | MSS_SPI2_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for Corresponding SPI |

### 2.6.2.95 MSS\_RCM\_MSS\_SPI3\_CLK\_GATE Register

#### 1 MSS\_RCM\_MSS\_SPI3\_CLK\_GATE Register (Offset = 348h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2647. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8348h       |

**Figure 2-881. MSS\_RCM\_MSS\_SPI3\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_SPI3_CLK_GATE_GATED |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-2649. MSS\_RCM\_MSS\_SPI3\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                          |
|------|-------------------------|------|-------|------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                             |
| 2:0  | MSS_SPI3_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for Corresponding SPI |

### 2.6.2.96 MSS\_RCM\_MSS\_SPI4\_CLK\_GATE Register

#### 1 MSS\_RCM\_MSS\_SPI4\_CLK\_GATE Register (Offset = 34Ch) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2650. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 834Ch       |

**Figure 2-882. MSS\_RCM\_MSS\_SPI4\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_SPI4_CLK_GATE_GATED |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-2652. MSS\_RCM\_MSS\_SPI4\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                          |
|------|-------------------------|------|-------|------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                             |
| 2:0  | MSS_SPI4_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for Corresponding SPI |



## 2.6.2.97 MSS\_RCM\_MSS\_MMCSO\_CLK\_GATE Register

### 1 MSS\_RCM\_MSS\_MMCSO\_CLK\_GATE Register (Offset = 350h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2653. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8350h       |

**Figure 2-883. MSS\_RCM\_MSS\_MMCSO\_CLK\_GATE Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | MSS_MMCSO_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-2655. MSS\_RCM\_MSS\_MMCSO\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                              |
|------|--------------------------|------|-------|------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                 |
| 2:0  | MSS_MMCSO_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for MMCSO |

## 2.6.2.98 MSS\_RCM\_PRU\_ICSS\_UCLK\_CLK\_GATE Register

### 1 MSS\_RCM\_PRU\_ICSS\_UCLK\_CLK\_GATE Register (Offset = 354h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2656. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8354h       |

**Figure 2-884. MSS\_RCM\_PRU\_ICSS\_UCLK\_CLK\_GATE Name Register**

|          |    |    |    |    |                              |    |    |
|----------|----|----|----|----|------------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                           | 25 | 24 |
| RESERVED |    |    |    |    |                              |    |    |
| NONE     |    |    |    |    |                              |    |    |
| 0h       |    |    |    |    |                              |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                           | 17 | 16 |
| RESERVED |    |    |    |    |                              |    |    |
| NONE     |    |    |    |    |                              |    |    |
| 0h       |    |    |    |    |                              |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                           | 9  | 8  |
| RESERVED |    |    |    |    |                              |    |    |
| NONE     |    |    |    |    |                              |    |    |
| 0h       |    |    |    |    |                              |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                            | 1  | 0  |
| RESERVED |    |    |    |    | PRU_ICSS_UCLK_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                          |    |    |
| 0h       |    |    |    |    | 0h                           |    |    |

**Table 2-2658. MSS\_RCM\_PRU\_ICSS\_UCLK\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                        | Type | Reset | Description                                   |
|------|------------------------------|------|-------|-----------------------------------------------|
| 31:3 | RESERVED                     | NONE | 0h    | Reserved                                      |
| 2:0  | PRU_ICSS_UCLK_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for ICSSM_UCLK |

## 2.6.2.99 MSS\_RCM\_MSS\_CPTS\_CLK\_GATE Register

### 1 MSS\_RCM\_MSS\_CPTS\_CLK\_GATE Register (Offset = 358h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2659. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8358h       |

**Figure 2-885. MSS\_RCM\_MSS\_CPTS\_CLK\_GATE Name Register**

|          |    |    |    |    |                         |    |    |
|----------|----|----|----|----|-------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                      | 25 | 24 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                      | 17 | 16 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                      | 9  | 8  |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                       | 1  | 0  |
| RESERVED |    |    |    |    | MSS_CPTS_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                     |    |    |
| 0h       |    |    |    |    | 0h                      |    |    |

**Table 2-2661. MSS\_RCM\_MSS\_CPTS\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                             |
|------|-------------------------|------|-------|-----------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                |
| 2:0  | MSS_CPTS_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for CPTS |

## 2.6.2.100 MSS\_RCM\_GPMC\_CLK\_GATE Register

### 1 MSS\_RCM\_GPMC\_CLK\_GATE Register (Offset = 35Ch) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2662. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 835Ch       |

**Figure 2-886. MSS\_RCM\_GPMC\_CLK\_GATE Name Register**

|          |    |    |    |    |                     |    |    |
|----------|----|----|----|----|---------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                  | 25 | 24 |
| RESERVED |    |    |    |    |                     |    |    |
| NONE     |    |    |    |    |                     |    |    |
| 0h       |    |    |    |    |                     |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                  | 17 | 16 |
| RESERVED |    |    |    |    |                     |    |    |
| NONE     |    |    |    |    |                     |    |    |
| 0h       |    |    |    |    |                     |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                  | 9  | 8  |
| RESERVED |    |    |    |    |                     |    |    |
| NONE     |    |    |    |    |                     |    |    |
| 0h       |    |    |    |    |                     |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                   | 1  | 0  |
| RESERVED |    |    |    |    | GPMC_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                 |    |    |
| 0h       |    |    |    |    | 0h                  |    |    |

**Table 2-2664. MSS\_RCM\_GPMC\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                             |
|------|-------------------------|------|-------|-----------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                |
| 2:0  | GPMC_CLK_GATE_GATE<br>D | R/W  | 0h    | Writing 3'b111 will gate clock for GPMC |

### 2.6.2.101 MSS\_RCM\_CONTROLSS\_PLL\_CLK\_GATE Register

#### 1 MSS\_RCM\_CONTROLSS\_PLL\_CLK\_GATE Register (Offset = 360h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2665. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8360h       |

**Figure 2-887. MSS\_RCM\_CONTROLSS\_PLL\_CLK\_GATE Name Register**

|          |    |    |    |    |                              |    |    |
|----------|----|----|----|----|------------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                           | 25 | 24 |
| RESERVED |    |    |    |    |                              |    |    |
| NONE     |    |    |    |    |                              |    |    |
| 0h       |    |    |    |    |                              |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                           | 17 | 16 |
| RESERVED |    |    |    |    |                              |    |    |
| NONE     |    |    |    |    |                              |    |    |
| 0h       |    |    |    |    |                              |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                           | 9  | 8  |
| RESERVED |    |    |    |    |                              |    |    |
| NONE     |    |    |    |    |                              |    |    |
| 0h       |    |    |    |    |                              |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                            | 1  | 0  |
| RESERVED |    |    |    |    | CONTROLSS_PLL_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                          |    |    |
| 0h       |    |    |    |    | 0h                           |    |    |

**Table 2-2667. MSS\_RCM\_CONTROLSS\_PLL\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                        | Type | Reset | Description                                      |
|------|------------------------------|------|-------|--------------------------------------------------|
| 31:3 | RESERVED                     | NONE | 0h    | Reserved                                         |
| 2:0  | CONTROLSS_PLL_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for CONTROLSS_PLL |

## 2.6.2.102 MSS\_RCM\_MSS\_I2C0\_CLK\_GATE Register

### 1 MSS\_RCM\_MSS\_I2C0\_CLK\_GATE Register (Offset = 364h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2668. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8364h       |

**Figure 2-888. MSS\_RCM\_MSS\_I2C0\_CLK\_GATE Name Register**

|          |    |    |    |    |                         |    |    |
|----------|----|----|----|----|-------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                      | 25 | 24 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                      | 17 | 16 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                      | 9  | 8  |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                       | 1  | 0  |
| RESERVED |    |    |    |    | MSS_I2C0_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                     |    |    |
| 0h       |    |    |    |    | 0h                      |    |    |

**Table 2-2670. MSS\_RCM\_MSS\_I2C0\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                          |
|------|-------------------------|------|-------|------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                             |
| 2:0  | MSS_I2C0_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding I2C |

### 2.6.2.103 MSS\_RCM\_MSS\_I2C1\_CLK\_GATE Register

#### 1 MSS\_RCM\_MSS\_I2C1\_CLK\_GATE Register (Offset = 368h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2671. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8368h       |

**Figure 2-889. MSS\_RCM\_MSS\_I2C1\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_I2C1_CLK_GATE_GATED |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-2673. MSS\_RCM\_MSS\_I2C1\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                          |
|------|-------------------------|------|-------|------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                             |
| 2:0  | MSS_I2C1_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding I2C |

### 2.6.2.104 MSS\_RCM\_MSS\_I2C2\_CLK\_GATE Register

#### 1 MSS\_RCM\_MSS\_I2C2\_CLK\_GATE Register (Offset = 36Ch) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2674. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 836Ch       |

**Figure 2-890. MSS\_RCM\_MSS\_I2C2\_CLK\_GATE Name Register**

|          |    |    |    |    |                         |    |    |
|----------|----|----|----|----|-------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                      | 25 | 24 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                      | 17 | 16 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                      | 9  | 8  |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                       | 1  | 0  |
| RESERVED |    |    |    |    | MSS_I2C2_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                     |    |    |
| 0h       |    |    |    |    | 0h                      |    |    |

**Table 2-2676. MSS\_RCM\_MSS\_I2C2\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                          |
|------|-------------------------|------|-------|------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                             |
| 2:0  | MSS_I2C2_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding I2C |



### 2.6.2.105 MSS\_RCM\_MSS\_I2C3\_CLK\_GATE Register

#### 1 MSS\_RCM\_MSS\_I2C3\_CLK\_GATE Register (Offset = 370h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2677. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8370h       |

**Figure 2-891. MSS\_RCM\_MSS\_I2C3\_CLK\_GATE Name Register**

|          |    |    |    |    |                         |    |    |
|----------|----|----|----|----|-------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                      | 25 | 24 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                      | 17 | 16 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                      | 9  | 8  |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                       | 1  | 0  |
| RESERVED |    |    |    |    | MSS_I2C3_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                     |    |    |
| 0h       |    |    |    |    | 0h                      |    |    |

**Table 2-2679. MSS\_RCM\_MSS\_I2C3\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                          |
|------|-------------------------|------|-------|------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                             |
| 2:0  | MSS_I2C3_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding I2C |

### 2.6.2.106 MSS\_RCM\_MSS\_LIN0\_CLK\_GATE Register

#### 1 MSS\_RCM\_MSS\_LIN0\_CLK\_GATE Register (Offset = 374h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2680. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8374h       |

**Figure 2-892. MSS\_RCM\_MSS\_LIN0\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_LIN0_CLK_GATE_GATED |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-2682. MSS\_RCM\_MSS\_LIN0\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                          |
|------|-------------------------|------|-------|------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                             |
| 2:0  | MSS_LIN0_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding LIN |

## 2.6.2.107 MSS\_RCM\_MSS\_LIN1\_CLK\_GATE Register

### 1 MSS\_RCM\_MSS\_LIN1\_CLK\_GATE Register (Offset = 378h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2683. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8378h       |

**Figure 2-893. MSS\_RCM\_MSS\_LIN1\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_LIN1_CLK_GATE_GATED |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-2685. MSS\_RCM\_MSS\_LIN1\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                          |
|------|-------------------------|------|-------|------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                             |
| 2:0  | MSS_LIN1_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding LIN |

## 2.6.2.108 MSS\_RCM\_MSS\_LIN2\_CLK\_GATE Register

### 1 MSS\_RCM\_MSS\_LIN2\_CLK\_GATE Register (Offset = 37Ch) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2686. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 837Ch       |

**Figure 2-894. MSS\_RCM\_MSS\_LIN2\_CLK\_GATE Name Register**

|          |    |    |    |    |                         |    |    |
|----------|----|----|----|----|-------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                      | 25 | 24 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                      | 17 | 16 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                      | 9  | 8  |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                       | 1  | 0  |
| RESERVED |    |    |    |    | MSS_LIN2_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                     |    |    |
| 0h       |    |    |    |    | 0h                      |    |    |

**Table 2-2688. MSS\_RCM\_MSS\_LIN2\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                          |
|------|-------------------------|------|-------|------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                             |
| 2:0  | MSS_LIN2_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding LIN |

### 2.6.2.109 MSS\_RCM\_MSS\_LIN3\_CLK\_GATE Register

#### 1 MSS\_RCM\_MSS\_LIN3\_CLK\_GATE Register (Offset = 380h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2689. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8380h       |

**Figure 2-895. MSS\_RCM\_MSS\_LIN3\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_LIN3_CLK_GATE_GATED |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-2691. MSS\_RCM\_MSS\_LIN3\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                          |
|------|-------------------------|------|-------|------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                             |
| 2:0  | MSS_LIN3_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding LIN |

### 2.6.2.110 MSS\_RCM\_MSS\_LIN4\_CLK\_GATE Register

#### 1 MSS\_RCM\_MSS\_LIN4\_CLK\_GATE Register (Offset = 384h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2692. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8384h       |

**Figure 2-896. MSS\_RCM\_MSS\_LIN4\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_LIN4_CLK_GATE_GATED |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-2694. MSS\_RCM\_MSS\_LIN4\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                          |
|------|-------------------------|------|-------|------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                             |
| 2:0  | MSS_LIN4_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding LIN |

### 2.6.2.111 MSS\_RCM\_MSS\_UART0\_CLK\_GATE Register

#### 1 MSS\_RCM\_MSS\_UART0\_CLK\_GATE Register (Offset = 38Ch) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2695. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 838Ch       |

**Figure 2-897. MSS\_RCM\_MSS\_UART0\_CLK\_GATE Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | MSS_UART0_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-2697. MSS\_RCM\_MSS\_UART0\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | MSS_UART0_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding UART |

## 2.6.2.112 MSS\_RCM\_MSS\_UART1\_CLK\_GATE Register

### 1 MSS\_RCM\_MSS\_UART1\_CLK\_GATE Register (Offset = 390h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2698. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8390h       |

**Figure 2-898. MSS\_RCM\_MSS\_UART1\_CLK\_GATE Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | MSS_UART1_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-2700. MSS\_RCM\_MSS\_UART1\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | MSS_UART1_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding UART |



### 2.6.2.113 MSS\_RCM\_MSS\_UART2\_CLK\_GATE Register

#### 1 MSS\_RCM\_MSS\_UART2\_CLK\_GATE Register (Offset = 394h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2701. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8394h       |

**Figure 2-899. MSS\_RCM\_MSS\_UART2\_CLK\_GATE Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | MSS_UART2_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-2703. MSS\_RCM\_MSS\_UART2\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | MSS_UART2_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding UART |

## 2.6.2.114 MSS\_RCM\_MSS\_UART3\_CLK\_GATE Register

### 1 MSS\_RCM\_MSS\_UART3\_CLK\_GATE Register (Offset = 398h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2704. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8398h       |

**Figure 2-900. MSS\_RCM\_MSS\_UART3\_CLK\_GATE Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | MSS_UART3_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-2706. MSS\_RCM\_MSS\_UART3\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | MSS_UART3_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding UART |

### 2.6.2.115 MSS\_RCM\_MSS\_UART4\_CLK\_GATE Register

#### 1 MSS\_RCM\_MSS\_UART4\_CLK\_GATE Register (Offset = 39Ch) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2707. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 839Ch       |

**Figure 2-901. MSS\_RCM\_MSS\_UART4\_CLK\_GATE Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | MSS_UART4_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-2709. MSS\_RCM\_MSS\_UART4\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | MSS_UART4_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding UART |

### 2.6.2.116 MSS\_RCM\_MSS\_UART5\_CLK\_GATE Register

#### 1 MSS\_RCM\_MSS\_UART5\_CLK\_GATE Register (Offset = 3A0h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2710. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 83A0h       |

**Figure 2-902. MSS\_RCM\_MSS\_UART5\_CLK\_GATE Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | MSS_UART5_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-2712. MSS\_RCM\_MSS\_UART5\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | MSS_UART5_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding UART |

## 2.6.2.117 MSS\_RCM\_MSS\_RGMII\_CLK\_GATE Register

### 1 MSS\_RCM\_MSS\_RGMII\_CLK\_GATE Register (Offset = 3A4h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2713. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 83A4h       |

**Figure 2-903. MSS\_RCM\_MSS\_RGMII\_CLK\_GATE Name Register**

|          |    |    |    |                          |    |    |    |
|----------|----|----|----|--------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 23       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 15       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 7        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_RGMII_CLK_GATE_GATED |    |    |    |
| NONE     |    |    |    | R/W                      |    |    |    |
| 0h       |    |    |    | 0h                       |    |    |    |

**Table 2-2715. MSS\_RCM\_MSS\_RGMII\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                              |
|------|--------------------------|------|-------|------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                 |
| 2:0  | MSS_RGMII_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for RGMII |

## 2.6.2.118 MSS\_RCM\_MSS\_MII100\_CLK\_GATE Register

### 1 MSS\_RCM\_MSS\_MII100\_CLK\_GATE Register (Offset = 3A8h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2716. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 83A8h       |

**Figure 2-904. MSS\_RCM\_MSS\_MII100\_CLK\_GATE Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | MSS_MII100_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-2718. MSS\_RCM\_MSS\_MII100\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                               |
|------|---------------------------|------|-------|-------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                  |
| 2:0  | MSS_MII100_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for MII100 |

### 2.6.2.119 MSS\_RCM\_MSS\_MII10\_CLK\_GATE Register

#### 1 MSS\_RCM\_MSS\_MII10\_CLK\_GATE Register (Offset = 3ACh) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2719. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 83ACh       |

**Figure 2-905. MSS\_RCM\_MSS\_MII10\_CLK\_GATE Name Register**

|          |    |    |    |                          |    |    |    |
|----------|----|----|----|--------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 23       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 15       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 7        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_MII10_CLK_GATE_GATED |    |    |    |
| NONE     |    |    |    | R/W                      |    |    |    |
| 0h       |    |    |    | 0h                       |    |    |    |

**Table 2-2721. MSS\_RCM\_MSS\_MII10\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                              |
|------|--------------------------|------|-------|------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                 |
| 2:0  | MSS_MII10_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for MII10 |

### 2.6.2.120 MSS\_RCM\_MSS\_MMCS\_D\_32K\_CLK\_GATE Register

#### 1 MSS\_RCM\_MSS\_MMCS\_D\_32K\_CLK\_GATE Register (Offset = 3B0h) [reset = 0h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2722. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 83B0h       |

**Figure 2-906. MSS\_RCM\_MSS\_MMCS\_D\_32K\_CLK\_GATE Name Register**

|          |    |    |    |    |                               |    |    |
|----------|----|----|----|----|-------------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                            | 25 | 24 |
| RESERVED |    |    |    |    |                               |    |    |
| NONE     |    |    |    |    |                               |    |    |
| 0h       |    |    |    |    |                               |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                            | 17 | 16 |
| RESERVED |    |    |    |    |                               |    |    |
| NONE     |    |    |    |    |                               |    |    |
| 0h       |    |    |    |    |                               |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                            | 9  | 8  |
| RESERVED |    |    |    |    |                               |    |    |
| NONE     |    |    |    |    |                               |    |    |
| 0h       |    |    |    |    |                               |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                             | 1  | 0  |
| RESERVED |    |    |    |    | MSS_MMCS_D_32K_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                           |    |    |
| 0h       |    |    |    |    | 0h                            |    |    |

**Table 2-2724. MSS\_RCM\_MSS\_MMCS\_D\_32K\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                   |
|------|-------------------------------|------|-------|-----------------------------------------------|
| 31:3 | RESERVED                      | NONE | 0h    | Reserved                                      |
| 2:0  | MSS_MMCS_D_32K_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for MMCS_D_32K |



## 2.6.2.121 MSS\_RCM\_MSS\_TEMPSENSE\_32K\_CLK\_GATE Register

### 1 MSS\_RCM\_MSS\_TEMPSENSE\_32K\_CLK\_GATE Register (Offset = 3B4h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2725. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 83B4h       |

**Figure 2-907. MSS\_RCM\_MSS\_TEMPSENSE\_32K\_CLK\_GATE Name Register**

|          |    |    |    |    |                                  |    |    |
|----------|----|----|----|----|----------------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                               | 25 | 24 |
| RESERVED |    |    |    |    |                                  |    |    |
| NONE     |    |    |    |    |                                  |    |    |
| 0h       |    |    |    |    |                                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                               | 17 | 16 |
| RESERVED |    |    |    |    |                                  |    |    |
| NONE     |    |    |    |    |                                  |    |    |
| 0h       |    |    |    |    |                                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                               | 9  | 8  |
| RESERVED |    |    |    |    |                                  |    |    |
| NONE     |    |    |    |    |                                  |    |    |
| 0h       |    |    |    |    |                                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                                | 1  | 0  |
| RESERVED |    |    |    |    | MSS_TEMPSENSE_32K_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                              |    |    |
| 0h       |    |    |    |    | 0h                               |    |    |

**Table 2-2727. MSS\_RCM\_MSS\_TEMPSENSE\_32K\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                            | Type | Reset | Description                                      |
|------|----------------------------------|------|-------|--------------------------------------------------|
| 31:3 | RESERVED                         | NONE | 0h    | Reserved                                         |
| 2:0  | MSS_TEMPSENSE_32K_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for TEMPSENSE_32K |

### 2.6.2.122 MSS\_RCM\_MSS\_CPSW\_CLK\_GATE Register

#### 1 MSS\_RCM\_MSS\_CPSW\_CLK\_GATE Register (Offset = 3B8h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2728. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 83B8h       |

**Figure 2-908. MSS\_RCM\_MSS\_CPSW\_CLK\_GATE Name Register**

|          |    |    |    |    |                         |    |    |
|----------|----|----|----|----|-------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                      | 25 | 24 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                      | 17 | 16 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                      | 9  | 8  |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                       | 1  | 0  |
| RESERVED |    |    |    |    | MSS_CPSW_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                     |    |    |
| 0h       |    |    |    |    | 0h                      |    |    |

**Table 2-2730. MSS\_RCM\_MSS\_CPSW\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                  |
|------|-------------------------|------|-------|----------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                     |
| 2:0  | MSS_CPSW_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for CPSW CPPI |

### 2.6.2.123 MSS\_RCM\_MSS\_PRU\_ICSS\_IEP\_CLK\_GATE Register

#### 1 MSS\_RCM\_MSS\_PRU\_ICSS\_IEP\_CLK\_GATE Register (Offset = 3BCh) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2731. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 83BCh       |

**Figure 2-909. MSS\_RCM\_MSS\_PRU\_ICSS\_IEP\_CLK\_GATE Name Register**

|          |    |    |    |    |                                 |    |    |
|----------|----|----|----|----|---------------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                              | 25 | 24 |
| RESERVED |    |    |    |    |                                 |    |    |
| NONE     |    |    |    |    |                                 |    |    |
| 0h       |    |    |    |    |                                 |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                              | 17 | 16 |
| RESERVED |    |    |    |    |                                 |    |    |
| NONE     |    |    |    |    |                                 |    |    |
| 0h       |    |    |    |    |                                 |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                              | 9  | 8  |
| RESERVED |    |    |    |    |                                 |    |    |
| NONE     |    |    |    |    |                                 |    |    |
| 0h       |    |    |    |    |                                 |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                               | 1  | 0  |
| RESERVED |    |    |    |    | MSS_PRU_ICSS_IEP_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                             |    |    |
| 0h       |    |    |    |    | 0h                              |    |    |

**Table 2-2733. MSS\_RCM\_MSS\_PRU\_ICSS\_IEP\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                           | Type | Reset | Description                                  |
|------|---------------------------------|------|-------|----------------------------------------------|
| 31:3 | RESERVED                        | NONE | 0h    | Reserved                                     |
| 2:0  | MSS_PRU_ICSS_IEP_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for ICSSM_IEP |

### 2.6.2.124 MSS\_RCM\_MSS\_PRU\_ICSS\_CORE\_CLK\_GATE Register

#### 1 MSS\_RCM\_MSS\_PRU\_ICSS\_CORE\_CLK\_GATE Register (Offset = 3C0h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2734. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 83C0h       |

**Figure 2-910. MSS\_RCM\_MSS\_PRU\_ICSS\_CORE\_CLK\_GATE Name Register**

|          |    |    |    |    |                                  |    |    |
|----------|----|----|----|----|----------------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                               | 25 | 24 |
| RESERVED |    |    |    |    |                                  |    |    |
| NONE     |    |    |    |    |                                  |    |    |
| 0h       |    |    |    |    |                                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                               | 17 | 16 |
| RESERVED |    |    |    |    |                                  |    |    |
| NONE     |    |    |    |    |                                  |    |    |
| 0h       |    |    |    |    |                                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                               | 9  | 8  |
| RESERVED |    |    |    |    |                                  |    |    |
| NONE     |    |    |    |    |                                  |    |    |
| 0h       |    |    |    |    |                                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                                | 1  | 0  |
| RESERVED |    |    |    |    | MSS_PRU_ICSS_CORE_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                              |    |    |
| 0h       |    |    |    |    | 0h                               |    |    |

**Table 2-2736. MSS\_RCM\_MSS\_PRU\_ICSS\_CORE\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                            | Type | Reset | Description                                   |
|------|----------------------------------|------|-------|-----------------------------------------------|
| 31:3 | RESERVED                         | NONE | 0h    | Reserved                                      |
| 2:0  | MSS_PRU_ICSS_CORE_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for ICSSM_CORE |

## 2.6.2.125 MSS\_RCM\_MSS\_PRU\_ICSS\_SYS\_CLK\_GATE Register

### 1 MSS\_RCM\_MSS\_PRU\_ICSS\_SYS\_CLK\_GATE Register (Offset = 3C4h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2737. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 83C4h       |

**Figure 2-911. MSS\_RCM\_MSS\_PRU\_ICSS\_SYS\_CLK\_GATE Name Register**

|          |    |    |    |    |                                 |    |    |
|----------|----|----|----|----|---------------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                              | 25 | 24 |
| RESERVED |    |    |    |    |                                 |    |    |
| NONE     |    |    |    |    |                                 |    |    |
| 0h       |    |    |    |    |                                 |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                              | 17 | 16 |
| RESERVED |    |    |    |    |                                 |    |    |
| NONE     |    |    |    |    |                                 |    |    |
| 0h       |    |    |    |    |                                 |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                              | 9  | 8  |
| RESERVED |    |    |    |    |                                 |    |    |
| NONE     |    |    |    |    |                                 |    |    |
| 0h       |    |    |    |    |                                 |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                               | 1  | 0  |
| RESERVED |    |    |    |    | MSS_PRU_ICSS_SYS_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                             |    |    |
| 0h       |    |    |    |    | 0h                              |    |    |

**Table 2-2739. MSS\_RCM\_MSS\_PRU\_ICSS\_SYS\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                           | Type | Reset | Description                                  |
|------|---------------------------------|------|-------|----------------------------------------------|
| 31:3 | RESERVED                        | NONE | 0h    | Reserved                                     |
| 2:0  | MSS_PRU_ICSS_SYS_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for ICSSM_SYS |

## 2.6.2.126 MSS\_RCM\_MSS\_ELM\_CLK\_GATE Register

### 1 MSS\_RCM\_MSS\_ELM\_CLK\_GATE Register (Offset = 3C8h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2740. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 83C8h       |

**Figure 2-912. MSS\_RCM\_MSS\_ELM\_CLK\_GATE Name Register**

|          |    |    |    |    |                        |    |    |
|----------|----|----|----|----|------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                     | 25 | 24 |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                     | 17 | 16 |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                     | 9  | 8  |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                      | 1  | 0  |
| RESERVED |    |    |    |    | MSS_ELM_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                    |    |    |
| 0h       |    |    |    |    | 0h                     |    |    |

**Table 2-2742. MSS\_RCM\_MSS\_ELM\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                            |
|------|------------------------|------|-------|----------------------------------------|
| 31:3 | RESERVED               | NONE | 0h    | Reserved                               |
| 2:0  | MSS_ELM_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for ELM |

### 2.6.2.127 MSS\_RCM\_R5\_CORE0\_GATE0 Register

#### 1 MSS\_RCM\_R5\_CORE0\_GATE0 Register (Offset = 3CCh) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-2743. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 83CCh       |

**Figure 2-913. MSS\_RCM\_R5\_CORE0\_GATE0 Name Register**

|          |    |    |    |                        |    |    |    |
|----------|----|----|----|------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                     | 26 | 25 | 24 |
| RESERVED |    |    |    |                        |    |    |    |
| NONE     |    |    |    |                        |    |    |    |
| 0h       |    |    |    |                        |    |    |    |
| 23       | 22 | 21 | 20 | 19                     | 18 | 17 | 16 |
| RESERVED |    |    |    |                        |    |    |    |
| NONE     |    |    |    |                        |    |    |    |
| 0h       |    |    |    |                        |    |    |    |
| 15       | 14 | 13 | 12 | 11                     | 10 | 9  | 8  |
| RESERVED |    |    |    |                        |    |    |    |
| NONE     |    |    |    |                        |    |    |    |
| 0h       |    |    |    |                        |    |    |    |
| 7        | 6  | 5  | 4  | 3                      | 2  | 1  | 0  |
| RESERVED |    |    |    | R5_COREA_GATE0_CLKGATE |    |    |    |
| NONE     |    |    |    | R/W                    |    |    |    |
| 0h       |    |    |    | 0h                     |    |    |    |

**Table 2-2745. MSS\_RCM\_R5\_CORE0\_GATE0 Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                                                 |
|------|------------------------|------|-------|---------------------------------------------------------------------------------------------|
| 31:3 | RESERVED               | NONE | 0h    | Reserved                                                                                    |
| 2:0  | R5_COREA_GATE0_CLKGATE | R/W  | 0h    | Writing 3'b111 will gate clock to CORE0 related peripherals inside corresponding Cortexr5ss |

## 2.6.2.128 MSS\_RCM\_R5\_CORE0\_GATE1 Register

### 1 MSS\_RCM\_R5\_CORE0\_GATE1 Register (Offset = 3D0h) [reset = 0h]

Clock gating for individual CPU core.

Return to [Summary Table](#)

**Table 2-2746. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 83D0h       |

**Figure 2-914. MSS\_RCM\_R5\_CORE0\_GATE1 Name Register**

|          |    |    |    |    |                        |    |    |
|----------|----|----|----|----|------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                     | 25 | 24 |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                     | 17 | 16 |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                     | 9  | 8  |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                      | 1  | 0  |
| RESERVED |    |    |    |    | R5_COREA_GATE1_CLKGATE |    |    |
| NONE     |    |    |    |    | R/W                    |    |    |
| 0h       |    |    |    |    | 0h                     |    |    |

**Table 2-2748. MSS\_RCM\_R5\_CORE0\_GATE1 Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                                                 |
|------|------------------------|------|-------|---------------------------------------------------------------------------------------------|
| 31:3 | RESERVED               | NONE | 0h    | Reserved                                                                                    |
| 2:0  | R5_COREA_GATE1_CLKGATE | R/W  | 0h    | Writing 3'b111 will gate clock to CORE0 related peripherals inside corresponding Cortexr5ss |



## 2.6.2.129 MSS\_RCM\_R5\_CORE1\_GATE0 Register

### 1 MSS\_RCM\_R5\_CORE1\_GATE0 Register (Offset = 3D4h) [reset = 0h]

Clock gating for individual CPU core.

Return to [Summary Table](#)

**Table 2-2749. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 83D4h       |

**Figure 2-915. MSS\_RCM\_R5\_CORE1\_GATE0 Name Register**

|          |    |    |    |                        |    |    |    |
|----------|----|----|----|------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                     | 26 | 25 | 24 |
| RESERVED |    |    |    |                        |    |    |    |
| NONE     |    |    |    |                        |    |    |    |
| 0h       |    |    |    |                        |    |    |    |
| 23       | 22 | 21 | 20 | 19                     | 18 | 17 | 16 |
| RESERVED |    |    |    |                        |    |    |    |
| NONE     |    |    |    |                        |    |    |    |
| 0h       |    |    |    |                        |    |    |    |
| 15       | 14 | 13 | 12 | 11                     | 10 | 9  | 8  |
| RESERVED |    |    |    |                        |    |    |    |
| NONE     |    |    |    |                        |    |    |    |
| 0h       |    |    |    |                        |    |    |    |
| 7        | 6  | 5  | 4  | 3                      | 2  | 1  | 0  |
| RESERVED |    |    |    | R5_COREB_GATE0_CLKGATE |    |    |    |
| NONE     |    |    |    | R/W                    |    |    |    |
| 0h       |    |    |    | 0h                     |    |    |    |

**Table 2-2751. MSS\_RCM\_R5\_CORE1\_GATE0 Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                                                 |
|------|------------------------|------|-------|---------------------------------------------------------------------------------------------|
| 31:3 | RESERVED               | NONE | 0h    | Reserved                                                                                    |
| 2:0  | R5_COREB_GATE0_CLKGATE | R/W  | 0h    | Writing 3'b111 will gate clock to CORE1 related peripherals inside corresponding Cortexr5ss |

## 2.6.2.130 MSS\_RCM\_R5\_CORE1\_GATE1 Register

### 1 MSS\_RCM\_R5\_CORE1\_GATE1 Register (Offset = 3D8h) [reset = 0h]

Clock gating for individual CPU core.

Return to [Summary Table](#)

**Table 2-2752. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 83D8h       |

**Figure 2-916. MSS\_RCM\_R5\_CORE1\_GATE1 Name Register**

|          |    |    |    |    |                        |    |    |
|----------|----|----|----|----|------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                     | 25 | 24 |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                     | 17 | 16 |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                     | 9  | 8  |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                      | 1  | 0  |
| RESERVED |    |    |    |    | R5_COREB_GATE1_CLKGATE |    |    |
| NONE     |    |    |    |    | R/W                    |    |    |
| 0h       |    |    |    |    | 0h                     |    |    |

**Table 2-2754. MSS\_RCM\_R5\_CORE1\_GATE1 Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                                                 |
|------|------------------------|------|-------|---------------------------------------------------------------------------------------------|
| 31:3 | RESERVED               | NONE | 0h    | Reserved                                                                                    |
| 2:0  | R5_COREB_GATE1_CLKGATE | R/W  | 0h    | Writing 3'b111 will gate clock to CORE1 related peripherals inside corresponding Cortexr5ss |

### 2.6.2.131 MSS\_RCM\_MSS\_MCAN0\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_MCAN0\_CLK\_STATUS Register (Offset = 400h) [reset = 1h]

Clock gating for individual CPU core.

Return to [Summary Table](#)

**Table 2-2755. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8400h       |

**Figure 2-917. MSS\_RCM\_MSS\_MCAN0\_CLK\_STATUS Name Register**

|                                  |    |    |    |    |    |    |    |
|----------------------------------|----|----|----|----|----|----|----|
| 31                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                         |    |    |    |    |    |    |    |
| NONE                             |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 23                               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                         |    |    |    |    |    |    |    |
| NONE                             |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 15                               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_MCAN0_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                                |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 7                                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_MCAN0_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                                |    |    |    |    |    |    |    |
| 1h                               |    |    |    |    |    |    |    |

**Table 2-2757. MSS\_RCM\_MSS\_MCAN0\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                                | Type | Reset | Description                                                                                        |
|-------|--------------------------------------|------|-------|----------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                             | NONE | 0h    | Reserved                                                                                           |
| 15:8  | MSS_MCAN0_CLK_STAT<br>US_CURRDIVIDER | R    | 0h    | Status shows the current divider value chosen for corresponding MCAN                               |
| 7:0   | MSS_MCAN0_CLK_STAT<br>US_CLKINUSE    | R    | 1h    | Status shows the source clock selected for corresponding MCAN based on one hot encoding technique. |

### 2.6.2.132 MSS\_RCM\_MSS\_MCAN1\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_MCAN1\_CLK\_STATUS Register (Offset = 404h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2758. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8404h       |

**Figure 2-918. MSS\_RCM\_MSS\_MCAN1\_CLK\_STATUS Name Register**

|                                  |    |    |    |    |    |    |    |
|----------------------------------|----|----|----|----|----|----|----|
| 31                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                         |    |    |    |    |    |    |    |
| NONE                             |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 23                               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                         |    |    |    |    |    |    |    |
| NONE                             |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 15                               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_MCAN1_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                                |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 7                                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_MCAN1_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                                |    |    |    |    |    |    |    |
| 1h                               |    |    |    |    |    |    |    |

**Table 2-2760. MSS\_RCM\_MSS\_MCAN1\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                                | Type | Reset | Description                                                                                       |
|-------|--------------------------------------|------|-------|---------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                             | NONE | 0h    | Reserved                                                                                          |
| 15:8  | MSS_MCAN1_CLK_STAT<br>US_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for corresponding MCAN                             |
| 7:0   | MSS_MCAN1_CLK_STAT<br>US_CLKINUSE    | R    | 1h    | Status shows the source clock slected for corresponding MCAN based on one hot encoding technique. |

### 2.6.2.133 MSS\_RCM\_MSS\_MCAN2\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_MCAN2\_CLK\_STATUS Register (Offset = 408h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2761. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8408h       |

**Figure 2-919. MSS\_RCM\_MSS\_MCAN2\_CLK\_STATUS Name Register**

|                                  |    |    |    |    |    |    |    |
|----------------------------------|----|----|----|----|----|----|----|
| 31                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                         |    |    |    |    |    |    |    |
| NONE                             |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 23                               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                         |    |    |    |    |    |    |    |
| NONE                             |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 15                               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_MCAN2_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                                |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 7                                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_MCAN2_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                                |    |    |    |    |    |    |    |
| 1h                               |    |    |    |    |    |    |    |

**Table 2-2763. MSS\_RCM\_MSS\_MCAN2\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                                | Type | Reset | Description                                                                                       |
|-------|--------------------------------------|------|-------|---------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                             | NONE | 0h    | Reserved                                                                                          |
| 15:8  | MSS_MCAN2_CLK_STAT<br>US_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for corresponding MCAN                             |
| 7:0   | MSS_MCAN2_CLK_STAT<br>US_CLKINUSE    | R    | 1h    | Status shows the source clock slected for corresponding MCAN based on one hot encoding technique. |

### 2.6.2.134 MSS\_RCM\_MSS\_MCAN3\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_MCAN3\_CLK\_STATUS Register (Offset = 40Ch) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2764. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 840Ch       |

**Figure 2-920. MSS\_RCM\_MSS\_MCAN3\_CLK\_STATUS Name Register**

|                                  |    |    |    |    |    |    |    |
|----------------------------------|----|----|----|----|----|----|----|
| 31                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                         |    |    |    |    |    |    |    |
| NONE                             |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 23                               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                         |    |    |    |    |    |    |    |
| NONE                             |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 15                               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_MCAN3_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                                |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 7                                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_MCAN3_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                                |    |    |    |    |    |    |    |
| 1h                               |    |    |    |    |    |    |    |

**Table 2-2766. MSS\_RCM\_MSS\_MCAN3\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                                | Type | Reset | Description                                                                                       |
|-------|--------------------------------------|------|-------|---------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                             | NONE | 0h    | Reserved                                                                                          |
| 15:8  | MSS_MCAN3_CLK_STAT<br>US_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for corresponding MCAN                             |
| 7:0   | MSS_MCAN3_CLK_STAT<br>US_CLKINUSE    | R    | 1h    | Status shows the source clock slected for corresponding MCAN based on one hot encoding technique. |

### 2.6.2.135 MSS\_RCM\_MSS\_QSPI\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_QSPI\_CLK\_STATUS Register (Offset = 410h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2767. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8410h       |

**Figure 2-921. MSS\_RCM\_MSS\_QSPI\_CLK\_STATUS Name Register**

|                                 |    |    |    |    |    |    |    |
|---------------------------------|----|----|----|----|----|----|----|
| 31                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 23                              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 15                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_QSPI_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 7                               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_QSPI_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 1h                              |    |    |    |    |    |    |    |

**Table 2-2769. MSS\_RCM\_MSS\_QSPI\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                                         |
|-------|-------------------------------------|------|-------|-------------------------------------------------------------------------------------|
| 31:16 | RESERVED                            | NONE | 0h    | Reserved                                                                            |
| 15:8  | MSS_QSPI_CLK_STATU<br>S_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for QSPI                             |
| 7:0   | MSS_QSPI_CLK_STATU<br>S_CLKINUSE    | R    | 1h    | Status shows the source clock slected for QSPI based on one hot encoding technique. |

## 2.6.2.136 MSS\_RCM\_MSS\_RTIO\_CLK\_STATUS Register

### 1 MSS\_RCM\_MSS\_RTIO\_CLK\_STATUS Register (Offset = 414h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2770. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8414h       |

**Figure 2-922. MSS\_RCM\_MSS\_RTIO\_CLK\_STATUS Name Register**

|                                 |    |    |    |    |    |    |    |
|---------------------------------|----|----|----|----|----|----|----|
| 31                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 23                              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 15                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_RTIO_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 7                               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_RTIO_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 1h                              |    |    |    |    |    |    |    |

**Table 2-2772. MSS\_RCM\_MSS\_RTIO\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                      |
|-------|---------------------------------|------|-------|--------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                        | NONE | 0h    | Reserved                                                                                         |
| 15:8  | MSS_RTIO_CLK_STATUS_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for Corresponding RTI                             |
| 7:0   | MSS_RTIO_CLK_STATUS_CLKINUSE    | R    | 1h    | Status shows the source clock slected for Corresponding RTI based on one hot encoding technique. |



### 2.6.2.137 MSS\_RCM\_MSS\_RT11\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_RT11\_CLK\_STATUS Register (Offset = 418h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2773. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8418h       |

**Figure 2-923. MSS\_RCM\_MSS\_RT11\_CLK\_STATUS Name Register**

|                                 |    |    |    |    |    |    |    |
|---------------------------------|----|----|----|----|----|----|----|
| 31                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 23                              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 15                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_RT11_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 7                               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_RT11_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 1h                              |    |    |    |    |    |    |    |

**Table 2-2775. MSS\_RCM\_MSS\_RT11\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                      |
|-------|---------------------------------|------|-------|--------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                        | NONE | 0h    | Reserved                                                                                         |
| 15:8  | MSS_RT11_CLK_STATUS_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for Corresponding RTI                             |
| 7:0   | MSS_RT11_CLK_STATUS_CLKINUSE    | R    | 1h    | Status shows the source clock slected for Corresponding RTI based on one hot encoding technique. |

### 2.6.2.138 MSS\_RCM\_MSS\_RT12\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_RT12\_CLK\_STATUS Register (Offset = 41Ch) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2776. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 841Ch       |

**Figure 2-924. MSS\_RCM\_MSS\_RT12\_CLK\_STATUS Name Register**

|                                 |    |    |    |    |    |    |    |
|---------------------------------|----|----|----|----|----|----|----|
| 31                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 23                              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 15                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_RT12_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 7                               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_RT12_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 1h                              |    |    |    |    |    |    |    |

**Table 2-2778. MSS\_RCM\_MSS\_RT12\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                      |
|-------|---------------------------------|------|-------|--------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                        | NONE | 0h    | Reserved                                                                                         |
| 15:8  | MSS_RT12_CLK_STATUS_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for Corresponding RTI                             |
| 7:0   | MSS_RT12_CLK_STATUS_CLKINUSE    | R    | 1h    | Status shows the source clock slected for Corresponding RTI based on one hot encoding technique. |

### 2.6.2.139 MSS\_RCM\_MSS\_RT13\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_RT13\_CLK\_STATUS Register (Offset = 420h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2779. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8420h       |

**Figure 2-925. MSS\_RCM\_MSS\_RT13\_CLK\_STATUS Name Register**

|                                 |    |    |    |    |    |    |    |
|---------------------------------|----|----|----|----|----|----|----|
| 31                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 23                              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 15                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_RT13_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 7                               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_RT13_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 1h                              |    |    |    |    |    |    |    |

**Table 2-2781. MSS\_RCM\_MSS\_RT13\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                      |
|-------|---------------------------------|------|-------|--------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                        | NONE | 0h    | Reserved                                                                                         |
| 15:8  | MSS_RT13_CLK_STATUS_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for Corresponding RTI                             |
| 7:0   | MSS_RT13_CLK_STATUS_CLKINUSE    | R    | 1h    | Status shows the source clock slected for Corresponding RTI based on one hot encoding technique. |

### 2.6.2.140 MSS\_RCM\_MSS\_WDT0\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_WDT0\_CLK\_STATUS Register (Offset = 428h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2782. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8428h       |

**Figure 2-926. MSS\_RCM\_MSS\_WDT0\_CLK\_STATUS Name Register**

|                                 |    |    |    |    |    |    |    |
|---------------------------------|----|----|----|----|----|----|----|
| 31                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 23                              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 15                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_WDT0_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 7                               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_WDT0_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 1h                              |    |    |    |    |    |    |    |

**Table 2-2784. MSS\_RCM\_MSS\_WDT0\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                                                      |
|-------|-------------------------------------|------|-------|--------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                            | NONE | 0h    | Reserved                                                                                         |
| 15:8  | MSS_WDT0_CLK_STATU<br>S_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for corresponding WDT                             |
| 7:0   | MSS_WDT0_CLK_STATU<br>S_CLKINUSE    | R    | 1h    | Status shows the source clock slected for Corresponding WDT based on one hot encoding technique. |

### 2.6.2.141 MSS\_RCM\_MSS\_WDT1\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_WDT1\_CLK\_STATUS Register (Offset = 42Ch) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2785. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 842Ch       |

**Figure 2-927. MSS\_RCM\_MSS\_WDT1\_CLK\_STATUS Name Register**

|                                 |    |    |    |    |    |    |    |
|---------------------------------|----|----|----|----|----|----|----|
| 31                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 23                              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 15                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_WDT1_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 7                               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_WDT1_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 1h                              |    |    |    |    |    |    |    |

**Table 2-2787. MSS\_RCM\_MSS\_WDT1\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                                                      |
|-------|-------------------------------------|------|-------|--------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                            | NONE | 0h    | Reserved                                                                                         |
| 15:8  | MSS_WDT1_CLK_STATU<br>S_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for corresponding WDT                             |
| 7:0   | MSS_WDT1_CLK_STATU<br>S_CLKINUSE    | R    | 1h    | Status shows the source clock slected for Corresponding WDT based on one hot encoding technique. |

### 2.6.2.142 MSS\_RCM\_MSS\_WDT2\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_WDT2\_CLK\_STATUS Register (Offset = 430h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2788. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8430h       |

**Figure 2-928. MSS\_RCM\_MSS\_WDT2\_CLK\_STATUS Name Register**

|                                 |    |    |    |    |    |    |    |
|---------------------------------|----|----|----|----|----|----|----|
| 31                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 23                              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 15                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_WDT2_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 7                               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_WDT2_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 1h                              |    |    |    |    |    |    |    |

**Table 2-2790. MSS\_RCM\_MSS\_WDT2\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                                                      |
|-------|-------------------------------------|------|-------|--------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                            | NONE | 0h    | Reserved                                                                                         |
| 15:8  | MSS_WDT2_CLK_STATU<br>S_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for corresponding WDT                             |
| 7:0   | MSS_WDT2_CLK_STATU<br>S_CLKINUSE    | R    | 1h    | Status shows the source clock slected for Corresponding WDT based on one hot encoding technique. |

### 2.6.2.143 MSS\_RCM\_MSS\_WDT3\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_WDT3\_CLK\_STATUS Register (Offset = 434h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2791. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8434h       |

**Figure 2-929. MSS\_RCM\_MSS\_WDT3\_CLK\_STATUS Name Register**

|                                 |    |    |    |    |    |    |    |
|---------------------------------|----|----|----|----|----|----|----|
| 31                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 23                              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 15                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_WDT3_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 7                               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_WDT3_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 1h                              |    |    |    |    |    |    |    |

**Table 2-2793. MSS\_RCM\_MSS\_WDT3\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                                                      |
|-------|-------------------------------------|------|-------|--------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                            | NONE | 0h    | Reserved                                                                                         |
| 15:8  | MSS_WDT3_CLK_STATU<br>S_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for corresponding WDT                             |
| 7:0   | MSS_WDT3_CLK_STATU<br>S_CLKINUSE    | R    | 1h    | Status shows the source clock slected for Corresponding WDT based on one hot encoding technique. |

### 2.6.2.144 MSS\_RCM\_MSS\_SPI0\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_SPI0\_CLK\_STATUS Register (Offset = 43Ch) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2794. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 843Ch       |

**Figure 2-930. MSS\_RCM\_MSS\_SPI0\_CLK\_STATUS Name Register**

|                                 |    |    |    |    |    |    |    |
|---------------------------------|----|----|----|----|----|----|----|
| 31                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 23                              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 15                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_SPI0_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 7                               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_SPI0_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 1h                              |    |    |    |    |    |    |    |

**Table 2-2796. MSS\_RCM\_MSS\_SPI0\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                      |
|-------|---------------------------------|------|-------|--------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                        | NONE | 0h    | Reserved                                                                                         |
| 15:8  | MSS_SPI0_CLK_STATUS_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for Corresponding SPI                             |
| 7:0   | MSS_SPI0_CLK_STATUS_CLKINUSE    | R    | 1h    | Status shows the source clock slected for Corresponding SPI based on one hot encoding technique. |



### 2.6.2.145 MSS\_RCM\_MSS\_SPI1\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_SPI1\_CLK\_STATUS Register (Offset = 440h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2797. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8440h       |

**Figure 2-931. MSS\_RCM\_MSS\_SPI1\_CLK\_STATUS Name Register**

|                                 |    |    |    |    |    |    |    |
|---------------------------------|----|----|----|----|----|----|----|
| 31                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 23                              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 15                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_SPI1_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 7                               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_SPI1_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 1h                              |    |    |    |    |    |    |    |

**Table 2-2799. MSS\_RCM\_MSS\_SPI1\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                      |
|-------|---------------------------------|------|-------|--------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                        | NONE | 0h    | Reserved                                                                                         |
| 15:8  | MSS_SPI1_CLK_STATUS_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for Corresponding SPI                             |
| 7:0   | MSS_SPI1_CLK_STATUS_CLKINUSE    | R    | 1h    | Status shows the source clock slected for Corresponding SPI based on one hot encoding technique. |

### 2.6.2.146 MSS\_RCM\_MSS\_SPI2\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_SPI2\_CLK\_STATUS Register (Offset = 444h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2800. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8444h       |

**Figure 2-932. MSS\_RCM\_MSS\_SPI2\_CLK\_STATUS Name Register**

|                                 |    |    |    |    |    |    |    |
|---------------------------------|----|----|----|----|----|----|----|
| 31                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 23                              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 15                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_SPI2_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 7                               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_SPI2_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 1h                              |    |    |    |    |    |    |    |

**Table 2-2802. MSS\_RCM\_MSS\_SPI2\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                      |
|-------|---------------------------------|------|-------|--------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                        | NONE | 0h    | Reserved                                                                                         |
| 15:8  | MSS_SPI2_CLK_STATUS_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for Corresponding SPI                             |
| 7:0   | MSS_SPI2_CLK_STATUS_CLKINUSE    | R    | 1h    | Status shows the source clock slected for Corresponding SPI based on one hot encoding technique. |

### 2.6.2.147 MSS\_RCM\_MSS\_SPI3\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_SPI3\_CLK\_STATUS Register (Offset = 448h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2803. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8448h       |

**Figure 2-933. MSS\_RCM\_MSS\_SPI3\_CLK\_STATUS Name Register**

|                                 |    |    |    |    |    |    |    |
|---------------------------------|----|----|----|----|----|----|----|
| 31                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 23                              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 15                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_SPI3_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 7                               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_SPI3_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 1h                              |    |    |    |    |    |    |    |

**Table 2-2805. MSS\_RCM\_MSS\_SPI3\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                      |
|-------|---------------------------------|------|-------|--------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                        | NONE | 0h    | Reserved                                                                                         |
| 15:8  | MSS_SPI3_CLK_STATUS_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for Corresponding SPI                             |
| 7:0   | MSS_SPI3_CLK_STATUS_CLKINUSE    | R    | 1h    | Status shows the source clock slected for Corresponding SPI based on one hot encoding technique. |

### 2.6.2.148 MSS\_RCM\_MSS\_SPI4\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_SPI4\_CLK\_STATUS Register (Offset = 44Ch) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2806. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 844Ch       |

**Figure 2-934. MSS\_RCM\_MSS\_SPI4\_CLK\_STATUS Name Register**

|                                 |    |    |    |    |    |    |    |
|---------------------------------|----|----|----|----|----|----|----|
| 31                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 23                              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 15                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_SPI4_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 7                               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_SPI4_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 1h                              |    |    |    |    |    |    |    |

**Table 2-2808. MSS\_RCM\_MSS\_SPI4\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                      |
|-------|---------------------------------|------|-------|--------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                        | NONE | 0h    | Reserved                                                                                         |
| 15:8  | MSS_SPI4_CLK_STATUS_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for Corresponding SPI                             |
| 7:0   | MSS_SPI4_CLK_STATUS_CLKINUSE    | R    | 1h    | Status shows the source clock slected for Corresponding SPI based on one hot encoding technique. |

### 2.6.2.149 MSS\_RCM\_MSS\_MMCSO\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_MMCSO\_CLK\_STATUS Register (Offset = 450h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2809. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8450h       |

**Figure 2-935. MSS\_RCM\_MSS\_MMCSO\_CLK\_STATUS Name Register**

|                                  |    |    |    |    |    |    |    |
|----------------------------------|----|----|----|----|----|----|----|
| 31                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                         |    |    |    |    |    |    |    |
| NONE                             |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 23                               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                         |    |    |    |    |    |    |    |
| NONE                             |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 15                               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_MMCSO_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                                |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 7                                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_MMCSO_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                                |    |    |    |    |    |    |    |
| 1h                               |    |    |    |    |    |    |    |

**Table 2-2811. MSS\_RCM\_MSS\_MMCSO\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                            | Type | Reset | Description                                                                           |
|-------|----------------------------------|------|-------|---------------------------------------------------------------------------------------|
| 31:16 | RESERVED                         | NONE | 0h    | Reserved                                                                              |
| 15:8  | MSS_MMCSO_CLK_STATUS_CURRDIVIDER | R    | 0h    | Status shows the current divider value chosen for MMCSO                               |
| 7:0   | MSS_MMCSO_CLK_STATUS_CLKINUSE    | R    | 1h    | Status shows the source clock selected for MMCSO based on one hot encoding technique. |

## 2.6.2.150 MSS\_RCM\_PRU\_ICSS\_UCLK\_CLK\_STATUS Register

### 1 MSS\_RCM\_PRU\_ICSS\_UCLK\_CLK\_STATUS Register (Offset = 454h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2812. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8454h       |

**Figure 2-936. MSS\_RCM\_PRU\_ICSS\_UCLK\_CLK\_STATUS Name Register**

|                                      |    |    |    |    |    |    |    |
|--------------------------------------|----|----|----|----|----|----|----|
| 31                                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                             |    |    |    |    |    |    |    |
| NONE                                 |    |    |    |    |    |    |    |
| 0h                                   |    |    |    |    |    |    |    |
| 23                                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                             |    |    |    |    |    |    |    |
| NONE                                 |    |    |    |    |    |    |    |
| 0h                                   |    |    |    |    |    |    |    |
| 15                                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PRU_ICSS_UCLK_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                                    |    |    |    |    |    |    |    |
| 0h                                   |    |    |    |    |    |    |    |
| 7                                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PRU_ICSS_UCLK_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                                    |    |    |    |    |    |    |    |
| 1h                                   |    |    |    |    |    |    |    |

**Table 2-2814. MSS\_RCM\_PRU\_ICSS\_UCLK\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                                | Type | Reset | Description                                                                               |
|-------|--------------------------------------|------|-------|-------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                             | NONE | 0h    | Reserved                                                                                  |
| 15:8  | PRU_ICSS_UCLK_CLK_STATUS_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for ICSSM_UCLK                             |
| 7:0   | PRU_ICSS_UCLK_CLK_STATUS_CLKINUSE    | R    | 1h    | Status shows the source clock slected for ICSSM_UCLK based on one hot encoding technique. |

### 2.6.2.151 MSS\_RCM\_MSS\_CPTS\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_CPTS\_CLK\_STATUS Register (Offset = 458h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2815. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8458h       |

**Figure 2-937. MSS\_RCM\_MSS\_CPTS\_CLK\_STATUS Name Register**

|                                 |    |    |    |    |    |    |    |
|---------------------------------|----|----|----|----|----|----|----|
| 31                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 23                              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 15                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_CPTS_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 7                               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_CPTS_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 1h                              |    |    |    |    |    |    |    |

**Table 2-2817. MSS\_RCM\_MSS\_CPTS\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                                         |
|-------|-------------------------------------|------|-------|-------------------------------------------------------------------------------------|
| 31:16 | RESERVED                            | NONE | 0h    | Reserved                                                                            |
| 15:8  | MSS_CPTS_CLK_STATU<br>S_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for CPTS                             |
| 7:0   | MSS_CPTS_CLK_STATU<br>S_CLKINUSE    | R    | 1h    | Status shows the source clock slected for CPTS based on one hot encoding technique. |

## 2.6.2.152 MSS\_RCM\_GPMC\_CLK\_STATUS Register

### 1 MSS\_RCM\_GPMC\_CLK\_STATUS Register (Offset = 45Ch) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2818. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 845Ch       |

**Figure 2-938. MSS\_RCM\_GPMC\_CLK\_STATUS Name Register**

|                             |    |    |    |    |    |    |    |
|-----------------------------|----|----|----|----|----|----|----|
| 31                          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                    |    |    |    |    |    |    |    |
| NONE                        |    |    |    |    |    |    |    |
| 0h                          |    |    |    |    |    |    |    |
| 23                          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                    |    |    |    |    |    |    |    |
| NONE                        |    |    |    |    |    |    |    |
| 0h                          |    |    |    |    |    |    |    |
| 15                          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| GPMC_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                           |    |    |    |    |    |    |    |
| 0h                          |    |    |    |    |    |    |    |
| 7                           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| GPMC_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                           |    |    |    |    |    |    |    |
| 1h                          |    |    |    |    |    |    |    |

**Table 2-2820. MSS\_RCM\_GPMC\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                       | Type | Reset | Description                                                                          |
|-------|-----------------------------|------|-------|--------------------------------------------------------------------------------------|
| 31:16 | RESERVED                    | NONE | 0h    | Reserved                                                                             |
| 15:8  | GPMC_CLK_STATUS_CURRDIVIDER | R    | 0h    | Status shows the current divider value chosen for GPMC                               |
| 7:0   | GPMC_CLK_STATUS_CLKINUSE    | R    | 1h    | Status shows the source clock selected for GPMC based on one hot encoding technique. |



### 2.6.2.153 MSS\_RCM\_CONTROLSS\_PLL\_CLK\_STATUS Register

#### 1 MSS\_RCM\_CONTROLSS\_PLL\_CLK\_STATUS Register (Offset = 460h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2821. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8460h       |

**Figure 2-939. MSS\_RCM\_CONTROLSS\_PLL\_CLK\_STATUS Name Register**

|                                      |    |    |    |    |    |    |    |
|--------------------------------------|----|----|----|----|----|----|----|
| 31                                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                             |    |    |    |    |    |    |    |
| NONE                                 |    |    |    |    |    |    |    |
| 0h                                   |    |    |    |    |    |    |    |
| 23                                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                             |    |    |    |    |    |    |    |
| NONE                                 |    |    |    |    |    |    |    |
| 0h                                   |    |    |    |    |    |    |    |
| 15                                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CONTROLSS_PLL_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                                    |    |    |    |    |    |    |    |
| 0h                                   |    |    |    |    |    |    |    |
| 7                                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CONTROLSS_PLL_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                                    |    |    |    |    |    |    |    |
| 1h                                   |    |    |    |    |    |    |    |

**Table 2-2823. MSS\_RCM\_CONTROLSS\_PLL\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                                | Type | Reset | Description                                                                                   |
|-------|--------------------------------------|------|-------|-----------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                             | NONE | 0h    | Reserved                                                                                      |
| 15:8  | CONTROLSS_PLL_CLK_STATUS_CURRDIVIDER | R    | 0h    | Status shows the current divider value chosen for CONTROLSS_PLL                               |
| 7:0   | CONTROLSS_PLL_CLK_STATUS_CLKINUSE    | R    | 1h    | Status shows the source clock selected for CONTROLSS_PLL based on one hot encoding technique. |

### 2.6.2.154 MSS\_RCM\_MSS\_I2C\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_I2C\_CLK\_STATUS Register (Offset = 464h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2824. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8464h       |

**Figure 2-940. MSS\_RCM\_MSS\_I2C\_CLK\_STATUS Name Register**

|                                |    |    |    |    |    |    |    |
|--------------------------------|----|----|----|----|----|----|----|
| 31                             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                       |    |    |    |    |    |    |    |
| NONE                           |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |
| 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                       |    |    |    |    |    |    |    |
| NONE                           |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |
| 15                             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_I2C_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                              |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |
| 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_I2C_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                              |    |    |    |    |    |    |    |
| 1h                             |    |    |    |    |    |    |    |

**Table 2-2826. MSS\_RCM\_MSS\_I2C\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                        |
|-------|--------------------------------|------|-------|------------------------------------------------------------------------------------|
| 31:16 | RESERVED                       | NONE | 0h    | Reserved                                                                           |
| 15:8  | MSS_I2C_CLK_STATUS_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for I2C                             |
| 7:0   | MSS_I2C_CLK_STATUS_CLKINUSE    | R    | 1h    | Status shows the source clock slected for I2C based on one hot encoding technique. |

### 2.6.2.155 MSS\_RCM\_MSS\_LIN0\_UART0\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_LIN0\_UART0\_CLK\_STATUS Register (Offset = 474h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2827. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8474h       |

**Figure 2-941. MSS\_RCM\_MSS\_LIN0\_UART0\_CLK\_STATUS Name Register**

|                                       |    |    |    |    |    |    |    |
|---------------------------------------|----|----|----|----|----|----|----|
| 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 23                                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 15                                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_LIN0_UART0_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 7                                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_LIN0_UART0_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 1h                                    |    |    |    |    |    |    |    |

**Table 2-2829. MSS\_RCM\_MSS\_LIN0\_UART0\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                                 | Type | Reset | Description                                                                                                |
|-------|---------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                              | NONE | 0h    | Reserved                                                                                                   |
| 15:8  | MSS_LIN0_UART0_CLK_STATUS_CURRDIVIDER | R    | 0h    | Status shows the current divider value chosen for corresponding UART and LIN                               |
| 7:0   | MSS_LIN0_UART0_CLK_STATUS_CLKINUSE    | R    | 1h    | Status shows the source clock selected for corresponding UART and LIN based on one hot encoding technique. |

### 2.6.2.156 MSS\_RCM\_MSS\_LIN1\_UART1\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_LIN1\_UART1\_CLK\_STATUS Register (Offset = 478h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2830. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8478h       |

**Figure 2-942. MSS\_RCM\_MSS\_LIN1\_UART1\_CLK\_STATUS Name Register**

|                                       |    |    |    |    |    |    |    |
|---------------------------------------|----|----|----|----|----|----|----|
| 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 23                                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 15                                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_LIN1_UART1_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 7                                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_LIN1_UART1_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 1h                                    |    |    |    |    |    |    |    |

**Table 2-2832. MSS\_RCM\_MSS\_LIN1\_UART1\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                                 | Type | Reset | Description                                                                                               |
|-------|---------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                              | NONE | 0h    | Reserved                                                                                                  |
| 15:8  | MSS_LIN1_UART1_CLK_STATUS_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for corresponding UART and LIN                             |
| 7:0   | MSS_LIN1_UART1_CLK_STATUS_CLKINUSE    | R    | 1h    | Status shows the source clock slected for corresponding UART and LIN based on one hot encoding technique. |

### 2.6.2.157 MSS\_RCM\_MSS\_LIN2\_UART2\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_LIN2\_UART2\_CLK\_STATUS Register (Offset = 47Ch) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2833. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 847Ch       |

**Figure 2-943. MSS\_RCM\_MSS\_LIN2\_UART2\_CLK\_STATUS Name Register**

|                                       |    |    |    |    |    |    |    |
|---------------------------------------|----|----|----|----|----|----|----|
| 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 23                                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 15                                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_LIN2_UART2_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 7                                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_LIN2_UART2_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 1h                                    |    |    |    |    |    |    |    |

**Table 2-2835. MSS\_RCM\_MSS\_LIN2\_UART2\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                                 | Type | Reset | Description                                                                                                |
|-------|---------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                              | NONE | 0h    | Reserved                                                                                                   |
| 15:8  | MSS_LIN2_UART2_CLK_STATUS_CURRDIVIDER | R    | 0h    | Status shows the current divider value chosen for corresponding UART and LIN                               |
| 7:0   | MSS_LIN2_UART2_CLK_STATUS_CLKINUSE    | R    | 1h    | Status shows the source clock selected for corresponding UART and LIN based on one hot encoding technique. |

### 2.6.2.158 MSS\_RCM\_MSS\_LIN3\_UART3\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_LIN3\_UART3\_CLK\_STATUS Register (Offset = 480h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2836. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8480h       |

**Figure 2-944. MSS\_RCM\_MSS\_LIN3\_UART3\_CLK\_STATUS Name Register**

|                                       |    |    |    |    |    |    |    |
|---------------------------------------|----|----|----|----|----|----|----|
| 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 23                                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 15                                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_LIN3_UART3_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 7                                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_LIN3_UART3_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 1h                                    |    |    |    |    |    |    |    |

**Table 2-2838. MSS\_RCM\_MSS\_LIN3\_UART3\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                                 | Type | Reset | Description                                                                                               |
|-------|---------------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                              | NONE | 0h    | Reserved                                                                                                  |
| 15:8  | MSS_LIN3_UART3_CLK_STATUS_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for corresponding UART and LIN                             |
| 7:0   | MSS_LIN3_UART3_CLK_STATUS_CLKINUSE    | R    | 1h    | Status shows the source clock slected for corresponding UART and LIN based on one hot encoding technique. |

## 2.6.2.159 MSS\_RCM\_MSS\_LIN4\_UART4\_CLK\_STATUS Register

### 1 MSS\_RCM\_MSS\_LIN4\_UART4\_CLK\_STATUS Register (Offset = 484h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2839. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8484h       |

**Figure 2-945. MSS\_RCM\_MSS\_LIN4\_UART4\_CLK\_STATUS Name Register**

|                                       |    |    |    |    |    |    |    |
|---------------------------------------|----|----|----|----|----|----|----|
| 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 23                                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 15                                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_LIN4_UART4_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 7                                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_LIN4_UART4_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 1h                                    |    |    |    |    |    |    |    |

**Table 2-2841. MSS\_RCM\_MSS\_LIN4\_UART4\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                                 | Type | Reset | Description                                                                                                |
|-------|---------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                              | NONE | 0h    | Reserved                                                                                                   |
| 15:8  | MSS_LIN4_UART4_CLK_STATUS_CURRDIVIDER | R    | 0h    | Status shows the current divider value chosen for corresponding UART and LIN                               |
| 7:0   | MSS_LIN4_UART4_CLK_STATUS_CLKINUSE    | R    | 1h    | Status shows the source clock selected for corresponding UART and LIN based on one hot encoding technique. |

## 2.6.2.160 MSS\_RCM\_MSS\_LIN5\_UART5\_CLK\_STATUS Register

### 1 MSS\_RCM\_MSS\_LIN5\_UART5\_CLK\_STATUS Register (Offset = 488h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2842. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8488h       |

**Figure 2-946. MSS\_RCM\_MSS\_LIN5\_UART5\_CLK\_STATUS Name Register**

|                                       |    |    |    |    |    |    |    |
|---------------------------------------|----|----|----|----|----|----|----|
| 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 23                                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                              |    |    |    |    |    |    |    |
| NONE                                  |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 15                                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_LIN5_UART5_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 0h                                    |    |    |    |    |    |    |    |
| 7                                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSS_LIN5_UART5_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                                     |    |    |    |    |    |    |    |
| 1h                                    |    |    |    |    |    |    |    |

**Table 2-2844. MSS\_RCM\_MSS\_LIN5\_UART5\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                                 | Type | Reset | Description                                                                                                |
|-------|---------------------------------------|------|-------|------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                              | NONE | 0h    | Reserved                                                                                                   |
| 15:8  | MSS_LIN5_UART5_CLK_STATUS_CURRDIVIDER | R    | 0h    | Status shows the current divider value chosen for corresponding UART and LIN                               |
| 7:0   | MSS_LIN5_UART5_CLK_STATUS_CLKINUSE    | R    | 1h    | Status shows the source clock selected for corresponding UART and LIN based on one hot encoding technique. |



### 2.6.2.161 MSS\_RCM\_MSS\_RGMII\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_RGMII\_CLK\_STATUS Register (Offset = 48Ch) [reset = 100h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2845. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 848Ch       |

**Figure 2-947. MSS\_RCM\_MSS\_RGMII\_CLK\_STATUS Name Register**

|                                  |    |    |    |    |    |    |    |
|----------------------------------|----|----|----|----|----|----|----|
| 31                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                         |    |    |    |    |    |    |    |
| NONE                             |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 23                               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                         |    |    |    |    |    |    |    |
| NONE                             |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 15                               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_RGMII_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                                |    |    |    |    |    |    |    |
| 1h                               |    |    |    |    |    |    |    |
| 7                                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED                         |    |    |    |    |    |    |    |
| NONE                             |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |

**Table 2-2847. MSS\_RCM\_MSS\_RGMII\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                                | Type | Reset | Description                                              |
|-------|--------------------------------------|------|-------|----------------------------------------------------------|
| 31:16 | RESERVED                             | NONE | 0h    | Reserved                                                 |
| 15:8  | MSS_RGMII_CLK_STATU<br>S_CURRDIVIDER | R    | 1h    | Status shows the current divider value choosen for RGMII |
| 7:0   | RESERVED                             | NONE | 0h    | Reserved                                                 |

### 2.6.2.162 MSS\_RCM\_MSS\_MII100\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_MII100\_CLK\_STATUS Register (Offset = 490h) [reset = 900h]

RGMII\_50\_CLK\_STATUS.

Return to [Summary Table](#)

**Table 2-2848. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8490h       |

**Figure 2-948. MSS\_RCM\_MSS\_MII100\_CLK\_STATUS Name Register**

|                                   |    |    |    |    |    |    |    |
|-----------------------------------|----|----|----|----|----|----|----|
| 31                                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                          |    |    |    |    |    |    |    |
| NONE                              |    |    |    |    |    |    |    |
| 0h                                |    |    |    |    |    |    |    |
| 23                                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                          |    |    |    |    |    |    |    |
| NONE                              |    |    |    |    |    |    |    |
| 0h                                |    |    |    |    |    |    |    |
| 15                                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_MII100_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                                 |    |    |    |    |    |    |    |
| 9h                                |    |    |    |    |    |    |    |
| 7                                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED                          |    |    |    |    |    |    |    |
| NONE                              |    |    |    |    |    |    |    |
| 0h                                |    |    |    |    |    |    |    |

**Table 2-2850. MSS\_RCM\_MSS\_MII100\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                                 | Type | Reset | Description                                               |
|-------|---------------------------------------|------|-------|-----------------------------------------------------------|
| 31:16 | RESERVED                              | NONE | 0h    | Reserved                                                  |
| 15:8  | MSS_MII100_CLK_STAT<br>US_CURRDIVIDER | R    | 9h    | Status shows the current divider value choosen for MII100 |
| 7:0   | RESERVED                              | NONE | 0h    | Reserved                                                  |

### 2.6.2.163 MSS\_RCM\_MSS\_MII10\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_MII10\_CLK\_STATUS Register (Offset = 494h) [reset = 6300h]

RGMII\_5\_CLK\_STATUS.

Return to [Summary Table](#)
**Table 2-2851. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8494h       |

**Figure 2-949. MSS\_RCM\_MSS\_MII10\_CLK\_STATUS Name Register**

|                                  |    |    |    |    |    |    |    |
|----------------------------------|----|----|----|----|----|----|----|
| 31                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                         |    |    |    |    |    |    |    |
| NONE                             |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 23                               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                         |    |    |    |    |    |    |    |
| NONE                             |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 15                               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_MII10_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                                |    |    |    |    |    |    |    |
| 63h                              |    |    |    |    |    |    |    |
| 7                                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED                         |    |    |    |    |    |    |    |
| NONE                             |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |

**Table 2-2853. MSS\_RCM\_MSS\_MII10\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                                | Type | Reset | Description                                              |
|-------|--------------------------------------|------|-------|----------------------------------------------------------|
| 31:16 | RESERVED                             | NONE | 0h    | Reserved                                                 |
| 15:8  | MSS_MII10_CLK_STATU<br>S_CURRDIVIDER | R    | 63h   | Status shows the current divider value choosen for MII10 |
| 7:0   | RESERVED                             | NONE | 0h    | Reserved                                                 |

### 2.6.2.164 MSS\_RCM\_MMC0\_32K\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MMC0\_32K\_CLK\_STATUS Register (Offset = 49Ch) [reset = 30C00h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2854. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 849Ch       |

**Figure 2-950. MSS\_RCM\_MMC0\_32K\_CLK\_STATUS Name Register**

|                                      |    |    |    |    |    |                                      |    |
|--------------------------------------|----|----|----|----|----|--------------------------------------|----|
| 31                                   | 30 | 29 | 28 | 27 | 26 | 25                                   | 24 |
| RESERVED                             |    |    |    |    |    |                                      |    |
| NONE                                 |    |    |    |    |    |                                      |    |
| 0h                                   |    |    |    |    |    |                                      |    |
| 23                                   | 22 | 21 | 20 | 19 | 18 | 17                                   | 16 |
| RESERVED                             |    |    |    |    |    | MMC0_32K_CLK_STATUS_CURR<br>RDIVIDER |    |
| NONE                                 |    |    |    |    |    | R                                    |    |
| 0h                                   |    |    |    |    |    | 30Ch                                 |    |
| 15                                   | 14 | 13 | 12 | 11 | 10 | 9                                    | 8  |
| MMC0_32K_CLK_STATUS_CURR<br>RDIVIDER |    |    |    |    |    |                                      |    |
| R                                    |    |    |    |    |    |                                      |    |
| 30Ch                                 |    |    |    |    |    |                                      |    |
| 7                                    | 6  | 5  | 4  | 3  | 2  | 1                                    | 0  |
| RESERVED                             |    |    |    |    |    |                                      |    |
| NONE                                 |    |    |    |    |    |                                      |    |
| 0h                                   |    |    |    |    |    |                                      |    |

**Table 2-2856. MSS\_RCM\_MMC0\_32K\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                 |
|-------|-------------------------------------|------|-------|-------------------------------------------------------------|
| 31:18 | RESERVED                            | NONE | 0h    | Reserved                                                    |
| 17:8  | MMC0_32K_CLK_STATU<br>S_CURRDIVIDER | R    | 30Ch  | Status shows the current divider value choosen for XTAL_32K |
| 7:0   | RESERVED                            | NONE | 0h    | Reserved                                                    |

### 2.6.2.165 MSS\_RCM\_TEMPSENSE\_32K\_CLK\_STATUS Register

#### 1 MSS\_RCM\_TEMPSENSE\_32K\_CLK\_STATUS Register (Offset = 4A0h) [reset = 30C00h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-2857. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 84A0h       |

**Figure 2-951. MSS\_RCM\_TEMPSENSE\_32K\_CLK\_STATUS Name Register**

|                                      |    |    |    |    |    |                                          |    |
|--------------------------------------|----|----|----|----|----|------------------------------------------|----|
| 31                                   | 30 | 29 | 28 | 27 | 26 | 25                                       | 24 |
| RESERVED                             |    |    |    |    |    |                                          |    |
| NONE                                 |    |    |    |    |    |                                          |    |
| 0h                                   |    |    |    |    |    |                                          |    |
| 23                                   | 22 | 21 | 20 | 19 | 18 | 17                                       | 16 |
| RESERVED                             |    |    |    |    |    | TEMPSENSE_32K_CLK_STATU<br>S_CURRDIVIDER |    |
| NONE                                 |    |    |    |    |    | R                                        |    |
| 0h                                   |    |    |    |    |    | 30Ch                                     |    |
| 15                                   | 14 | 13 | 12 | 11 | 10 | 9                                        | 8  |
| TEMPSENSE_32K_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |                                          |    |
| R                                    |    |    |    |    |    |                                          |    |
| 30Ch                                 |    |    |    |    |    |                                          |    |
| 7                                    | 6  | 5  | 4  | 3  | 2  | 1                                        | 0  |
| RESERVED                             |    |    |    |    |    |                                          |    |
| NONE                                 |    |    |    |    |    |                                          |    |
| 0h                                   |    |    |    |    |    |                                          |    |

**Table 2-2859. MSS\_RCM\_TEMPSENSE\_32K\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                                | Type | Reset | Description                                                 |
|-------|--------------------------------------|------|-------|-------------------------------------------------------------|
| 31:18 | RESERVED                             | NONE | 0h    | Reserved                                                    |
| 17:8  | TEMPSENSE_32K_CLK_STATUS_CURRDIVIDER | R    | 30Ch  | Status shows the current divider value choosen for XTAL_32K |
| 7:0   | RESERVED                             | NONE | 0h    | Reserved                                                    |

### 2.6.2.166 MSS\_RCM\_MSS\_ELM\_CLK\_STATUS Register

#### 1 MSS\_RCM\_MSS\_ELM\_CLK\_STATUS Register (Offset = 4A4h) [reset = 300h]

MSS\_ELM\_CLK\_STATUS.

Return to [Summary Table](#)

**Table 2-2860. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 84A4h       |

**Figure 2-952. MSS\_RCM\_MSS\_ELM\_CLK\_STATUS Name Register**

|                                |    |    |    |    |    |    |    |
|--------------------------------|----|----|----|----|----|----|----|
| 31                             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                       |    |    |    |    |    |    |    |
| NONE                           |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |
| 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                       |    |    |    |    |    |    |    |
| NONE                           |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |
| 15                             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSS_ELM_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                              |    |    |    |    |    |    |    |
| 3h                             |    |    |    |    |    |    |    |
| 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED                       |    |    |    |    |    |    |    |
| NONE                           |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |

**Table 2-2862. MSS\_RCM\_MSS\_ELM\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                           |
|-------|--------------------------------|------|-------|-------------------------------------------------------|
| 31:16 | RESERVED                       | NONE | 0h    | Reserved                                              |
| 15:8  | MSS_ELM_CLK_STATUS_CURRDIVIDER | R    | 3h    | Status shows the current divider value chosen for ELM |
| 7:0   | RESERVED                       | NONE | 0h    | Reserved                                              |

### 2.6.2.167 MSS\_RCM\_MSS\_R5SS0\_POR\_RST\_CTRL0 Register

#### 1 MSS\_RCM\_MSS\_R5SS0\_POR\_RST\_CTRL0 Register (Offset = 500h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2863. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8500h       |

**Figure 2-953. MSS\_RCM\_MSS\_R5SS0\_POR\_RST\_CTRL0 Name Register**

|          |    |    |    |    |                                |    |    |
|----------|----|----|----|----|--------------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                             | 25 | 24 |
| RESERVED |    |    |    |    |                                |    |    |
| NONE     |    |    |    |    |                                |    |    |
| 0h       |    |    |    |    |                                |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                             | 17 | 16 |
| RESERVED |    |    |    |    |                                |    |    |
| NONE     |    |    |    |    |                                |    |    |
| 0h       |    |    |    |    |                                |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                             | 9  | 8  |
| RESERVED |    |    |    |    |                                |    |    |
| NONE     |    |    |    |    |                                |    |    |
| 0h       |    |    |    |    |                                |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                              | 1  | 0  |
| RESERVED |    |    |    |    | MSS_CR5SS_POR_RST_CTRL0_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                            |    |    |
| 0h       |    |    |    |    | 0h                             |    |    |

**Table 2-2865. MSS\_RCM\_MSS\_R5SS0\_POR\_RST\_CTRL0 Register Field Descriptions**

| Bit  | Field                          | Type | Reset | Description                                                                                                                                                                                                     |
|------|--------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                        |
| 2:0  | MSS_CR5SS_POR_RST_CTRL0_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.<br>write pulse bit field:<br>Writing 3'b111 will assert por reset to R5SS<br>Read is always 000 |

## 2.6.2.168 MSS\_RCM\_MSS\_R5SS0\_POR\_RST\_CTRL1 Register

### 1 MSS\_RCM\_MSS\_R5SS0\_POR\_RST\_CTRL1 Register (Offset = 504h) [reset = 0h]

R5SS POR Reset.

Return to [Summary Table](#)

**Table 2-2866. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8504h       |

**Figure 2-954. MSS\_RCM\_MSS\_R5SS0\_POR\_RST\_CTRL1 Name Register**

|          |    |    |    |    |                                |    |    |
|----------|----|----|----|----|--------------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                             | 25 | 24 |
| RESERVED |    |    |    |    |                                |    |    |
| NONE     |    |    |    |    |                                |    |    |
| 0h       |    |    |    |    |                                |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                             | 17 | 16 |
| RESERVED |    |    |    |    |                                |    |    |
| NONE     |    |    |    |    |                                |    |    |
| 0h       |    |    |    |    |                                |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                             | 9  | 8  |
| RESERVED |    |    |    |    |                                |    |    |
| NONE     |    |    |    |    |                                |    |    |
| 0h       |    |    |    |    |                                |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                              | 1  | 0  |
| RESERVED |    |    |    |    | MSS_CR5SS_POR_RST_CTRL1_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                            |    |    |
| 0h       |    |    |    |    | 0h                             |    |    |

**Table 2-2868. MSS\_RCM\_MSS\_R5SS0\_POR\_RST\_CTRL1 Register Field Descriptions**

| Bit  | Field                          | Type | Reset | Description                                                                                                                                                                                                     |
|------|--------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                        |
| 2:0  | MSS_CR5SS_POR_RST_CTRL1_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.<br>write pulse bit field:<br>Writing 3'b111 will assert por reset to R5SS<br>Read is always 000 |



### 2.6.2.169 MSS\_RCM\_MSS\_CR5SSA\_RST\_CTRL0 Register

#### 1 MSS\_RCM\_MSS\_CR5SSA\_RST\_CTRL0 Register (Offset = 508h) [reset = 0h]

R5SS POR Reset.

Return to [Summary Table](#)

**Table 2-2869. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8508h       |

**Figure 2-955. MSS\_RCM\_MSS\_CR5SSA\_RST\_CTRL0 Name Register**

|          |    |    |    |    |                             |    |    |
|----------|----|----|----|----|-----------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                          | 25 | 24 |
| RESERVED |    |    |    |    |                             |    |    |
| NONE     |    |    |    |    |                             |    |    |
| 0h       |    |    |    |    |                             |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                          | 17 | 16 |
| RESERVED |    |    |    |    |                             |    |    |
| NONE     |    |    |    |    |                             |    |    |
| 0h       |    |    |    |    |                             |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                          | 9  | 8  |
| RESERVED |    |    |    |    |                             |    |    |
| NONE     |    |    |    |    |                             |    |    |
| 0h       |    |    |    |    |                             |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                           | 1  | 0  |
| RESERVED |    |    |    |    | MSS_CR5SSA_RST_CTRL0_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                         |    |    |
| 0h       |    |    |    |    | 0h                          |    |    |

**Table 2-2871. MSS\_RCM\_MSS\_CR5SSA\_RST\_CTRL0 Register Field Descriptions**

| Bit  | Field                       | Type | Reset | Description                                                                                                                                                                                    |
|------|-----------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                    | NONE | 0h    | Reserved                                                                                                                                                                                       |
| 2:0  | MSS_CR5SSA_RST_CTRL0_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.<br>write pulse bit field:<br>Writing 3'b111 will reset CORE0 and MSS_CORE0_VIM |

## 2.6.2.170 MSS\_RCM\_MSS\_CR5SSA\_RST\_CTRL1 Register

### 1 MSS\_RCM\_MSS\_CR5SSA\_RST\_CTRL1 Register (Offset = 50Ch) [reset = 0h]

Core 0 Global Reset.

Return to [Summary Table](#)

**Table 2-2872. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 850Ch       |

**Figure 2-956. MSS\_RCM\_MSS\_CR5SSA\_RST\_CTRL1 Name Register**

|          |    |    |    |    |                             |    |    |
|----------|----|----|----|----|-----------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                          | 25 | 24 |
| RESERVED |    |    |    |    |                             |    |    |
| NONE     |    |    |    |    |                             |    |    |
| 0h       |    |    |    |    |                             |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                          | 17 | 16 |
| RESERVED |    |    |    |    |                             |    |    |
| NONE     |    |    |    |    |                             |    |    |
| 0h       |    |    |    |    |                             |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                          | 9  | 8  |
| RESERVED |    |    |    |    |                             |    |    |
| NONE     |    |    |    |    |                             |    |    |
| 0h       |    |    |    |    |                             |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                           | 1  | 0  |
| RESERVED |    |    |    |    | MSS_CR5SSA_RST_CTRL1_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                         |    |    |
| 0h       |    |    |    |    | 0h                          |    |    |

**Table 2-2874. MSS\_RCM\_MSS\_CR5SSA\_RST\_CTRL1 Register Field Descriptions**

| Bit  | Field                       | Type | Reset | Description                                                                                                                                                                                    |
|------|-----------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                    | NONE | 0h    | Reserved                                                                                                                                                                                       |
| 2:0  | MSS_CR5SSA_RST_CTRL1_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.<br>write pulse bit field:<br>Writing 3'b111 will reset CORE0 and MSS_CORE0_VIM |

## 2.6.2.171 MSS\_RCM\_MSS\_CR5SSB\_RST\_CTRL0 Register

### 1 MSS\_RCM\_MSS\_CR5SSB\_RST\_CTRL0 Register (Offset = 510h) [reset = 0h]

Core 0 Global Reset.

Return to [Summary Table](#)

**Table 2-2875. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8510h       |

**Figure 2-957. MSS\_RCM\_MSS\_CR5SSB\_RST\_CTRL0 Name Register**

|          |    |    |    |    |                             |    |    |
|----------|----|----|----|----|-----------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                          | 25 | 24 |
| RESERVED |    |    |    |    |                             |    |    |
| NONE     |    |    |    |    |                             |    |    |
| 0h       |    |    |    |    |                             |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                          | 17 | 16 |
| RESERVED |    |    |    |    |                             |    |    |
| NONE     |    |    |    |    |                             |    |    |
| 0h       |    |    |    |    |                             |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                          | 9  | 8  |
| RESERVED |    |    |    |    |                             |    |    |
| NONE     |    |    |    |    |                             |    |    |
| 0h       |    |    |    |    |                             |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                           | 1  | 0  |
| RESERVED |    |    |    |    | MSS_CR5SSB_RST_CTRL0_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                         |    |    |
| 0h       |    |    |    |    | 0h                          |    |    |

**Table 2-2877. MSS\_RCM\_MSS\_CR5SSB\_RST\_CTRL0 Register Field Descriptions**

| Bit  | Field                       | Type | Reset | Description                                                                                                                                                                                    |
|------|-----------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                    | NONE | 0h    | Reserved                                                                                                                                                                                       |
| 2:0  | MSS_CR5SSB_RST_CTRL0_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.<br>write pulse bit field:<br>Writing 3'b111 will reset CORE1 and MSS_CORE1_VIM |

## 2.6.2.172 MSS\_RCM\_MSS\_CR5SSB\_RST\_CTRL1 Register

### 1 MSS\_RCM\_MSS\_CR5SSB\_RST\_CTRL1 Register (Offset = 514h) [reset = 0h]

Core 1 Global Reset.

Return to [Summary Table](#)

**Table 2-2878. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8514h       |

**Figure 2-958. MSS\_RCM\_MSS\_CR5SSB\_RST\_CTRL1 Name Register**

|          |    |    |    |    |                             |    |    |
|----------|----|----|----|----|-----------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                          | 25 | 24 |
| RESERVED |    |    |    |    |                             |    |    |
| NONE     |    |    |    |    |                             |    |    |
| 0h       |    |    |    |    |                             |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                          | 17 | 16 |
| RESERVED |    |    |    |    |                             |    |    |
| NONE     |    |    |    |    |                             |    |    |
| 0h       |    |    |    |    |                             |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                          | 9  | 8  |
| RESERVED |    |    |    |    |                             |    |    |
| NONE     |    |    |    |    |                             |    |    |
| 0h       |    |    |    |    |                             |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                           | 1  | 0  |
| RESERVED |    |    |    |    | MSS_CR5SSB_RST_CTRL1_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                         |    |    |
| 0h       |    |    |    |    | 0h                          |    |    |

**Table 2-2880. MSS\_RCM\_MSS\_CR5SSB\_RST\_CTRL1 Register Field Descriptions**

| Bit  | Field                       | Type | Reset | Description                                                                                                                                                                                    |
|------|-----------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                    | NONE | 0h    | Reserved                                                                                                                                                                                       |
| 2:0  | MSS_CR5SSB_RST_CTRL1_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.<br>write pulse bit field:<br>Writing 3'b111 will reset CORE1 and MSS_CORE1_VIM |

### 2.6.2.173 MSS\_RCM\_MSS\_R5SS0\_CORE0\_RST\_CTRL0 Register

#### 1 MSS\_RCM\_MSS\_R5SS0\_CORE0\_RST\_CTRL0 Register (Offset = 518h) [reset = 0h]

Core 1 Global Reset.

Return to [Summary Table](#)

**Table 2-2881. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8518h       |

**Figure 2-959. MSS\_RCM\_MSS\_R5SS0\_CORE0\_RST\_CTRL0 Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | MSS_CR5A_RST_CTRL0_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-2883. MSS\_RCM\_MSS\_R5SS0\_CORE0\_RST\_CTRL0 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                                                                                       |
|------|---------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                                                                                                                                          |
| 2:0  | MSS_CR5A_RST_CTRL0_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.<br>write pulse bit field:<br>Writing 3'b111 will reset CORE0 only |

### 2.6.2.174 MSS\_RCM\_MSS\_R5SS0\_CORE0\_RST\_CTRL1 Register

#### 1 MSS\_RCM\_MSS\_R5SS0\_CORE0\_RST\_CTRL1 Register (Offset = 51Ch) [reset = 0h]

Core 0 Local Reset.

Return to [Summary Table](#)

**Table 2-2884. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 851Ch       |

**Figure 2-960. MSS\_RCM\_MSS\_R5SS0\_CORE0\_RST\_CTRL1 Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | MSS_CR5A_RST_CTRL1_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-2886. MSS\_RCM\_MSS\_R5SS0\_CORE0\_RST\_CTRL1 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                                                                                       |
|------|---------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                                                                                                                                          |
| 2:0  | MSS_CR5A_RST_CTRL1_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.<br>write pulse bit field:<br>Writing 3'b111 will reset CORE0 only |

### 2.6.2.175 MSS\_RCM\_MSS\_R5SS0\_CORE1\_RST\_CTRL0 Register

#### 1 MSS\_RCM\_MSS\_R5SS0\_CORE1\_RST\_CTRL0 Register (Offset = 520h) [reset = 0h]

Core 0 Local Reset.

Return to [Summary Table](#)

**Table 2-2887. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8520h       |

**Figure 2-961. MSS\_RCM\_MSS\_R5SS0\_CORE1\_RST\_CTRL0 Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | MSS_CR5B_RST_CTRL0_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-2889. MSS\_RCM\_MSS\_R5SS0\_CORE1\_RST\_CTRL0 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                                                                                       |
|------|---------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                                                                                                                                          |
| 2:0  | MSS_CR5B_RST_CTRL0_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.<br>write pulse bit field:<br>Writing 3'b111 will reset CORE1 only |

## 2.6.2.176 MSS\_RCM\_MSS\_R5SS0\_CORE1\_RST\_CTRL1 Register

### 1 MSS\_RCM\_MSS\_R5SS0\_CORE1\_RST\_CTRL1 Register (Offset = 524h) [reset = 0h]

Core 1 Local Reset.

Return to [Summary Table](#)

**Table 2-2890. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8524h       |

**Figure 2-962. MSS\_RCM\_MSS\_R5SS0\_CORE1\_RST\_CTRL1 Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | MSS_CR5B_RST_CTRL1_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-2892. MSS\_RCM\_MSS\_R5SS0\_CORE1\_RST\_CTRL1 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                                                                                       |
|------|---------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                                                                                                                                          |
| 2:0  | MSS_CR5B_RST_CTRL1_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring.<br>write pulse bit field:<br>Writing 3'b111 will reset CORE1 only |



### 2.6.2.177 MSS\_RCM\_MSS\_VIMA\_RST\_CTRL0 Register

#### 1 MSS\_RCM\_MSS\_VIMA\_RST\_CTRL0 Register (Offset = 528h) [reset = 0h]

Core 1 Local Reset.

Return to [Summary Table](#)

**Table 2-2893. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8528h       |

**Figure 2-963. MSS\_RCM\_MSS\_VIMA\_RST\_CTRL0 Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | MSS_VIMA_RST_CTRL0_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-2895. MSS\_RCM\_MSS\_VIMA\_RST\_CTRL0 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                                                                                                    |
|------|---------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                                                                                                                                                       |
| 2:0  | MSS_VIMA_RST_CTRL0_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS_CORE0_VIM Writing 3'b000 will deassert the reset |

### 2.6.2.178 MSS\_RCM\_MSS\_VIMA\_RST\_CTRL1 Register

#### 1 MSS\_RCM\_MSS\_VIMA\_RST\_CTRL1 Register (Offset = 52Ch) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2896. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 852Ch       |

**Figure 2-964. MSS\_RCM\_MSS\_VIMA\_RST\_CTRL1 Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | MSS_VIMA_RST_CTRL1_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-2898. MSS\_RCM\_MSS\_VIMA\_RST\_CTRL1 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                                                                                                    |
|------|---------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                                                                                                                                                       |
| 2:0  | MSS_VIMA_RST_CTRL1_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS_CORE0_VIM Writing 3'b000 will deassert the reset |

### 2.6.2.179 MSS\_RCM\_MSS\_VIMB\_RST\_CTRL0 Register

#### 1 MSS\_RCM\_MSS\_VIMB\_RST\_CTRL0 Register (Offset = 530h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2899. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8530h       |

**Figure 2-965. MSS\_RCM\_MSS\_VIMB\_RST\_CTRL0 Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | MSS_VIMB_RST_CTRL0_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-2901. MSS\_RCM\_MSS\_VIMB\_RST\_CTRL0 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                                                             |
|------|---------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                                                                                                                |
| 2:0  | MSS_VIMB_RST_CTRL0_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS_CORE1_VIM |

### 2.6.2.180 MSS\_RCM\_MSS\_VIMB\_RST\_CTRL1 Register

#### 1 MSS\_RCM\_MSS\_VIMB\_RST\_CTRL1 Register (Offset = 534h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2902. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8534h       |

**Figure 2-966. MSS\_RCM\_MSS\_VIMB\_RST\_CTRL1 Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | MSS_VIMB_RST_CTRL1_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-2904. MSS\_RCM\_MSS\_VIMB\_RST\_CTRL1 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                                                             |
|------|---------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                                                                                                                |
| 2:0  | MSS_VIMB_RST_CTRL1_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS_CORE1_VIM |

### 2.6.2.181 MSS\_RCM\_MSS\_CRC\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_CRC\_RST\_CTRL Register (Offset = 538h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2905. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8538h       |

**Figure 2-967. MSS\_RCM\_MSS\_CRC\_RST\_CTRL Name Register**

|          |    |    |    |    |                         |    |    |
|----------|----|----|----|----|-------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                      | 25 | 24 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                      | 17 | 16 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                      | 9  | 8  |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                       | 1  | 0  |
| RESERVED |    |    |    |    | MSS_CRC_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                     |    |    |
| 0h       |    |    |    |    | 0h                      |    |    |

**Table 2-2907. MSS\_RCM\_MSS\_CRC\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                                                                                                                    |
|------|-------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                       |
| 2:0  | MSS_CRC_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MCRC |

### 2.6.2.182 MSS\_RCM\_MSS\_RTIO\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_RTIO\_RST\_CTRL Register (Offset = 53Ch) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2908. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 853Ch       |

**Figure 2-968. MSS\_RCM\_MSS\_RTIO\_RST\_CTRL Name Register**

|          |    |    |    |                          |    |    |    |
|----------|----|----|----|--------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 23       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 15       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 7        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_RTIO_RST_CTRL_ASSERT |    |    |    |
| NONE     |    |    |    | R/W                      |    |    |    |
| 0h       |    |    |    | 0h                       |    |    |    |

**Table 2-2910. MSS\_RCM\_MSS\_RTIO\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                                 |
|------|--------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                                    |
| 2:0  | MSS_RTIO_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding RTI |

### 2.6.2.183 MSS\_RCM\_MSS\_RT11\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_RT11\_RST\_CTRL Register (Offset = 540h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2911. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8540h       |

**Figure 2-969. MSS\_RCM\_MSS\_RT11\_RST\_CTRL Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | MSS_RT11_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-2913. MSS\_RCM\_MSS\_RT11\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                                 |
|------|--------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                                    |
| 2:0  | MSS_RT11_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding RTI |

### 2.6.2.184 MSS\_RCM\_MSS\_RT2\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_RT2\_RST\_CTRL Register (Offset = 544h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2914. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8544h       |

**Figure 2-970. MSS\_RCM\_MSS\_RT2\_RST\_CTRL Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_RT2_RST_CTRL_ASSERT |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-2916. MSS\_RCM\_MSS\_RT2\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                                                                                                                                 |
|------|-------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                                    |
| 2:0  | MSS_RT2_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding RTI |



## 2.6.2.185 MSS\_RCM\_MSS\_RTl3\_RST\_CTRL Register

### 1 MSS\_RCM\_MSS\_RTl3\_RST\_CTRL Register (Offset = 548h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2917. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8548h       |

**Figure 2-971. MSS\_RCM\_MSS\_RTl3\_RST\_CTRL Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | MSS_RTl3_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-2919. MSS\_RCM\_MSS\_RTl3\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                                 |
|------|--------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                                    |
| 2:0  | MSS_RTl3_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding RTI |

## 2.6.2.186 MSS\_RCM\_MSS\_WDT0\_RST\_CTRL Register

### 1 MSS\_RCM\_MSS\_WDT0\_RST\_CTRL Register (Offset = 54Ch) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2920. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 854Ch       |

**Figure 2-972. MSS\_RCM\_MSS\_WDT0\_RST\_CTRL Name Register**

|          |    |    |    |                          |    |    |    |
|----------|----|----|----|--------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 23       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 15       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 7        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_WDT0_RST_CTRL_ASSERT |    |    |    |
| NONE     |    |    |    | R/W                      |    |    |    |
| 0h       |    |    |    | 0h                       |    |    |    |

**Table 2-2922. MSS\_RCM\_MSS\_WDT0\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                                 |
|------|--------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                                    |
| 2:0  | MSS_WDT0_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding WDT |

## 2.6.2.187 MSS\_RCM\_MSS\_WDT1\_RST\_CTRL Register

### 1 MSS\_RCM\_MSS\_WDT1\_RST\_CTRL Register (Offset = 550h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2923. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8550h       |

**Figure 2-973. MSS\_RCM\_MSS\_WDT1\_RST\_CTRL Name Register**

|          |    |    |    |                          |    |    |    |
|----------|----|----|----|--------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 23       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 15       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 7        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_WDT1_RST_CTRL_ASSERT |    |    |    |
| NONE     |    |    |    | R/W                      |    |    |    |
| 0h       |    |    |    | 0h                       |    |    |    |

**Table 2-2925. MSS\_RCM\_MSS\_WDT1\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                                 |
|------|--------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                                    |
| 2:0  | MSS_WDT1_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding WDT |

### 2.6.2.188 MSS\_RCM\_MSS\_WDT2\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_WDT2\_RST\_CTRL Register (Offset = 554h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2926. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8554h       |

**Figure 2-974. MSS\_RCM\_MSS\_WDT2\_RST\_CTRL Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | MSS_WDT2_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-2928. MSS\_RCM\_MSS\_WDT2\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                                 |
|------|--------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                                    |
| 2:0  | MSS_WDT2_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding WDT |

### 2.6.2.189 MSS\_RCM\_MSS\_WDT3\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_WDT3\_RST\_CTRL Register (Offset = 558h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2929. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8558h       |

**Figure 2-975. MSS\_RCM\_MSS\_WDT3\_RST\_CTRL Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | MSS_WDT3_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-2931. MSS\_RCM\_MSS\_WDT3\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                                 |
|------|--------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                                    |
| 2:0  | MSS_WDT3_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding WDT |

## 2.6.2.190 MSS\_RCM\_MSS\_ESM\_RST\_CTRL Register

### 1 MSS\_RCM\_MSS\_ESM\_RST\_CTRL Register (Offset = 55Ch) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2932. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 855Ch       |

**Figure 2-976. MSS\_RCM\_MSS\_ESM\_RST\_CTRL Name Register**

|          |    |    |    |    |                         |    |    |
|----------|----|----|----|----|-------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                      | 25 | 24 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                      | 17 | 16 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                      | 9  | 8  |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                       | 1  | 0  |
| RESERVED |    |    |    |    | MSS_ESM_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                     |    |    |
| 0h       |    |    |    |    | 0h                      |    |    |

**Table 2-2934. MSS\_RCM\_MSS\_ESM\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                                                                                                                   |
|------|-------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                      |
| 2:0  | MSS_ESM_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset ESM |

### 2.6.2.191 MSS\_RCM\_MSS\_DCC0\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_DCC0\_RST\_CTRL Register (Offset = 560h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2935. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8560h       |

**Figure 2-977. MSS\_RCM\_MSS\_DCC0\_RST\_CTRL Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | MSS_DCC0_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-2937. MSS\_RCM\_MSS\_DCC0\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                    |
|------|--------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                       |
| 2:0  | MSS_DCC0_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset DCC1 |

### 2.6.2.192 MSS\_RCM\_MSS\_DCC1\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_DCC1\_RST\_CTRL Register (Offset = 564h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2938. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8564h       |

**Figure 2-978. MSS\_RCM\_MSS\_DCC1\_RST\_CTRL Name Register**

|          |    |    |    |                          |    |    |    |
|----------|----|----|----|--------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 23       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 15       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 7        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_DCC1_RST_CTRL_ASSERT |    |    |    |
| NONE     |    |    |    | R/W                      |    |    |    |
| 0h       |    |    |    | 0h                       |    |    |    |

**Table 2-2940. MSS\_RCM\_MSS\_DCC1\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                    |
|------|--------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                       |
| 2:0  | MSS_DCC1_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset DCC2 |



### 2.6.2.193 MSS\_RCM\_MSS\_DCC2\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_DCC2\_RST\_CTRL Register (Offset = 568h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2941. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8568h       |

**Figure 2-979. MSS\_RCM\_MSS\_DCC2\_RST\_CTRL Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | MSS_DCC2_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-2943. MSS\_RCM\_MSS\_DCC2\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                    |
|------|--------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                       |
| 2:0  | MSS_DCC2_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset DCC3 |

### 2.6.2.194 MSS\_RCM\_MSS\_DCC3\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_DCC3\_RST\_CTRL Register (Offset = 56Ch) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2944. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 856Ch       |

**Figure 2-980. MSS\_RCM\_MSS\_DCC3\_RST\_CTRL Name Register**

|          |    |    |    |                          |    |    |    |
|----------|----|----|----|--------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 23       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 15       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 7        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_DCC3_RST_CTRL_ASSERT |    |    |    |
| NONE     |    |    |    | R/W                      |    |    |    |
| 0h       |    |    |    | 0h                       |    |    |    |

**Table 2-2946. MSS\_RCM\_MSS\_DCC3\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                    |
|------|--------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                       |
| 2:0  | MSS_DCC3_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset DCC4 |

## 2.6.2.195 MSS\_RCM\_MSS\_SPI0\_RST\_CTRL Register

### 1 MSS\_RCM\_MSS\_SPI0\_RST\_CTRL Register (Offset = 570h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2947. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8570h       |

**Figure 2-981. MSS\_RCM\_MSS\_SPI0\_RST\_CTRL Name Register**

|          |    |    |    |                          |    |    |    |
|----------|----|----|----|--------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 23       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 15       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 7        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_SPI0_RST_CTRL_ASSERT |    |    |    |
| NONE     |    |    |    | R/W                      |    |    |    |
| 0h       |    |    |    | 0h                       |    |    |    |

**Table 2-2949. MSS\_RCM\_MSS\_SPI0\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                                 |
|------|--------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                                    |
| 2:0  | MSS_SPI0_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset Corresponding SPI |

## 2.6.2.196 MSS\_RCM\_MSS\_SPI1\_RST\_CTRL Register

### 1 MSS\_RCM\_MSS\_SPI1\_RST\_CTRL Register (Offset = 574h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2950. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8574h       |

**Figure 2-982. MSS\_RCM\_MSS\_SPI1\_RST\_CTRL Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | MSS_SPI1_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-2952. MSS\_RCM\_MSS\_SPI1\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                                 |
|------|--------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                                    |
| 2:0  | MSS_SPI1_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset Corresponding SPI |

### 2.6.2.197 MSS\_RCM\_MSS\_SPI2\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_SPI2\_RST\_CTRL Register (Offset = 578h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2953. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8578h       |

**Figure 2-983. MSS\_RCM\_MSS\_SPI2\_RST\_CTRL Name Register**

|          |    |    |    |                          |    |    |    |
|----------|----|----|----|--------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 23       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 15       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 7        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_SPI2_RST_CTRL_ASSERT |    |    |    |
| NONE     |    |    |    | R/W                      |    |    |    |
| 0h       |    |    |    | 0h                       |    |    |    |

**Table 2-2955. MSS\_RCM\_MSS\_SPI2\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                                 |
|------|--------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                                    |
| 2:0  | MSS_SPI2_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset Corresponding SPI |

## 2.6.2.198 MSS\_RCM\_MSS\_SPI3\_RST\_CTRL Register

### 1 MSS\_RCM\_MSS\_SPI3\_RST\_CTRL Register (Offset = 57Ch) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2956. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 857Ch       |

**Figure 2-984. MSS\_RCM\_MSS\_SPI3\_RST\_CTRL Name Register**

|          |    |    |    |                          |    |    |    |
|----------|----|----|----|--------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 23       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 15       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 7        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_SPI3_RST_CTRL_ASSERT |    |    |    |
| NONE     |    |    |    | R/W                      |    |    |    |
| 0h       |    |    |    | 0h                       |    |    |    |

**Table 2-2958. MSS\_RCM\_MSS\_SPI3\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                                 |
|------|--------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                                    |
| 2:0  | MSS_SPI3_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset Corresponding SPI |

## 2.6.2.199 MSS\_RCM\_MSS\_SPI4\_RST\_CTRL Register

### 1 MSS\_RCM\_MSS\_SPI4\_RST\_CTRL Register (Offset = 580h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2959. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8580h       |

**Figure 2-985. MSS\_RCM\_MSS\_SPI4\_RST\_CTRL Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | MSS_SPI4_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-2961. MSS\_RCM\_MSS\_SPI4\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                                 |
|------|--------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                                    |
| 2:0  | MSS_SPI4_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset Corresponding SPI |

### 2.6.2.200 MSS\_RCM\_MSS\_QSPI\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_QSPI\_RST\_CTRL Register (Offset = 584h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2962. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8584h       |

**Figure 2-986. MSS\_RCM\_MSS\_QSPI\_RST\_CTRL Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | MSS_QSPI_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-2964. MSS\_RCM\_MSS\_QSPI\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                    |
|------|--------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                       |
| 2:0  | MSS_QSPI_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset QSPI |



### 2.6.2.201 MSS\_RCM\_MSS\_MCAN0\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_MCAN0\_RST\_CTRL Register (Offset = 588h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2965. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8588h       |

**Figure 2-987. MSS\_RCM\_MSS\_MCAN0\_RST\_CTRL Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | MSS_MCAN0_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-2967. MSS\_RCM\_MSS\_MCAN0\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                                                                  |
|------|---------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                                                                                                                     |
| 2:0  | MSS_MCAN0_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding MCAN |

### 2.6.2.202 MSS\_RCM\_MSS\_MCAN1\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_MCAN1\_RST\_CTRL Register (Offset = 58Ch) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2968. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 858Ch       |

**Figure 2-988. MSS\_RCM\_MSS\_MCAN1\_RST\_CTRL Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | MSS_MCAN1_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-2970. MSS\_RCM\_MSS\_MCAN1\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                                                                  |
|------|---------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                                                                                                                     |
| 2:0  | MSS_MCAN1_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding MCAN |

### 2.6.2.203 MSS\_RCM\_MSS\_MCAN2\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_MCAN2\_RST\_CTRL Register (Offset = 590h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2971. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8590h       |

**Figure 2-989. MSS\_RCM\_MSS\_MCAN2\_RST\_CTRL Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | MSS_MCAN2_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-2973. MSS\_RCM\_MSS\_MCAN2\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                                                                  |
|------|---------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                                                                                                                     |
| 2:0  | MSS_MCAN2_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding MCAN |

### 2.6.2.204 MSS\_RCM\_MSS\_MCAN3\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_MCAN3\_RST\_CTRL Register (Offset = 594h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2974. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8594h       |

**Figure 2-990. MSS\_RCM\_MSS\_MCAN3\_RST\_CTRL Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | MSS_MCAN3_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-2976. MSS\_RCM\_MSS\_MCAN3\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                                                                  |
|------|---------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                                                                                                                     |
| 2:0  | MSS_MCAN3_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding MCAN |

## 2.6.2.205 MSS\_RCM\_MSS\_I2C0\_RST\_CTRL Register

### 1 MSS\_RCM\_MSS\_I2C0\_RST\_CTRL Register (Offset = 598h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2977. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8598h       |

**Figure 2-991. MSS\_RCM\_MSS\_I2C0\_RST\_CTRL Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | MSS_I2C0_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-2979. MSS\_RCM\_MSS\_I2C0\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                                 |
|------|--------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                                    |
| 2:0  | MSS_I2C0_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding I2C |

## 2.6.2.206 MSS\_RCM\_MSS\_I2C1\_RST\_CTRL Register

### 1 MSS\_RCM\_MSS\_I2C1\_RST\_CTRL Register (Offset = 59Ch) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2980. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 859Ch       |

**Figure 2-992. MSS\_RCM\_MSS\_I2C1\_RST\_CTRL Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | MSS_I2C1_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-2982. MSS\_RCM\_MSS\_I2C1\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                                 |
|------|--------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                                    |
| 2:0  | MSS_I2C1_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding I2C |

### 2.6.2.207 MSS\_RCM\_MSS\_I2C2\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_I2C2\_RST\_CTRL Register (Offset = 5A0h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2983. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 85A0h       |

**Figure 2-993. MSS\_RCM\_MSS\_I2C2\_RST\_CTRL Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | MSS_I2C2_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-2985. MSS\_RCM\_MSS\_I2C2\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                                 |
|------|--------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                                    |
| 2:0  | MSS_I2C2_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding I2C |

## 2.6.2.208 MSS\_RCM\_MSS\_I2C3\_RST\_CTRL Register

### 1 MSS\_RCM\_MSS\_I2C3\_RST\_CTRL Register (Offset = 5A4h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2986. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 85A4h       |

**Figure 2-994. MSS\_RCM\_MSS\_I2C3\_RST\_CTRL Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | MSS_I2C3_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-2988. MSS\_RCM\_MSS\_I2C3\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                                 |
|------|--------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                                    |
| 2:0  | MSS_I2C3_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding I2C |



### 2.6.2.209 MSS\_RCM\_MSS\_UART0\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_UART0\_RST\_CTRL Register (Offset = 5A8h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2989. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 85A8h       |

**Figure 2-995. MSS\_RCM\_MSS\_UART0\_RST\_CTRL Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | MSS_UART0_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-2991. MSS\_RCM\_MSS\_UART0\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                                                                           |
|------|---------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                                                                                                                              |
| 2:0  | MSS_UART0_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding UART instance |

### 2.6.2.210 MSS\_RCM\_MSS\_UART1\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_UART1\_RST\_CTRL Register (Offset = 5ACh) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2992. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 85ACh       |

**Figure 2-996. MSS\_RCM\_MSS\_UART1\_RST\_CTRL Name Register**

|          |    |    |    |                           |    |    |    |
|----------|----|----|----|---------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                        | 26 | 25 | 24 |
| RESERVED |    |    |    |                           |    |    |    |
| NONE     |    |    |    |                           |    |    |    |
| 0h       |    |    |    |                           |    |    |    |
| 23       | 22 | 21 | 20 | 19                        | 18 | 17 | 16 |
| RESERVED |    |    |    |                           |    |    |    |
| NONE     |    |    |    |                           |    |    |    |
| 0h       |    |    |    |                           |    |    |    |
| 15       | 14 | 13 | 12 | 11                        | 10 | 9  | 8  |
| RESERVED |    |    |    |                           |    |    |    |
| NONE     |    |    |    |                           |    |    |    |
| 0h       |    |    |    |                           |    |    |    |
| 7        | 6  | 5  | 4  | 3                         | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_UART1_RST_CTRL_ASSERT |    |    |    |
| NONE     |    |    |    | R/W                       |    |    |    |
| 0h       |    |    |    | 0h                        |    |    |    |

**Table 2-2994. MSS\_RCM\_MSS\_UART1\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                                                                           |
|------|---------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                                                                                                                              |
| 2:0  | MSS_UART1_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding UART instance |

### 2.6.2.211 MSS\_RCM\_MSS\_UART2\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_UART2\_RST\_CTRL Register (Offset = 5B0h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2995. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 85B0h       |

**Figure 2-997. MSS\_RCM\_MSS\_UART2\_RST\_CTRL Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | MSS_UART2_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-2997. MSS\_RCM\_MSS\_UART2\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                                                                           |
|------|---------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                                                                                                                              |
| 2:0  | MSS_UART2_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding UART instance |

### 2.6.2.212 MSS\_RCM\_MSS\_UART3\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_UART3\_RST\_CTRL Register (Offset = 5B4h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-2998. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 85B4h       |

**Figure 2-998. MSS\_RCM\_MSS\_UART3\_RST\_CTRL Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | MSS_UART3_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3000. MSS\_RCM\_MSS\_UART3\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                                                                           |
|------|---------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                                                                                                                              |
| 2:0  | MSS_UART3_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding UART instance |

### 2.6.2.213 MSS\_RCM\_MSS\_UART4\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_UART4\_RST\_CTRL Register (Offset = 5B8h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-3001. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 85B8h       |

**Figure 2-999. MSS\_RCM\_MSS\_UART4\_RST\_CTRL Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | MSS_UART4_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3003. MSS\_RCM\_MSS\_UART4\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                                                                           |
|------|---------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                                                                                                                              |
| 2:0  | MSS_UART4_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding UART instance |

### 2.6.2.214 MSS\_RCM\_MSS\_UART5\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_UART5\_RST\_CTRL Register (Offset = 5BCh) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-3004. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 85BCh       |

**Figure 2-1000. MSS\_RCM\_MSS\_UART5\_RST\_CTRL Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | MSS_UART5_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3006. MSS\_RCM\_MSS\_UART5\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                                                                           |
|------|---------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                                                                                                                              |
| 2:0  | MSS_UART5_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding UART instance |

### 2.6.2.215 MSS\_RCM\_MSS\_LIN0\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_LIN0\_RST\_CTRL Register (Offset = 5C0h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-3007. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 85C0h       |

**Figure 2-1001. MSS\_RCM\_MSS\_LIN0\_RST\_CTRL Name Register**

|          |    |    |    |                          |    |    |    |
|----------|----|----|----|--------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 23       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 15       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 7        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_LIN0_RST_CTRL_ASSERT |    |    |    |
| NONE     |    |    |    | R/W                      |    |    |    |
| 0h       |    |    |    | 0h                       |    |    |    |

**Table 2-3009. MSS\_RCM\_MSS\_LIN0\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                                 |
|------|--------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                                    |
| 2:0  | MSS_LIN0_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding LIN |

### 2.6.2.216 MSS\_RCM\_MSS\_LIN1\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_LIN1\_RST\_CTRL Register (Offset = 5C4h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-3010. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 85C4h       |

**Figure 2-1002. MSS\_RCM\_MSS\_LIN1\_RST\_CTRL Name Register**

|          |    |    |    |                          |    |    |    |
|----------|----|----|----|--------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 23       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 15       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 7        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_LIN1_RST_CTRL_ASSERT |    |    |    |
| NONE     |    |    |    | R/W                      |    |    |    |
| 0h       |    |    |    | 0h                       |    |    |    |

**Table 2-3012. MSS\_RCM\_MSS\_LIN1\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                                 |
|------|--------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                                    |
| 2:0  | MSS_LIN1_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding LIN |



### 2.6.2.217 MSS\_RCM\_MSS\_LIN2\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_LIN2\_RST\_CTRL Register (Offset = 5C8h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-3013. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 85C8h       |

**Figure 2-1003. MSS\_RCM\_MSS\_LIN2\_RST\_CTRL Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | MSS_LIN2_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-3015. MSS\_RCM\_MSS\_LIN2\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                                 |
|------|--------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                                    |
| 2:0  | MSS_LIN2_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding LIN |

### 2.6.2.218 MSS\_RCM\_MSS\_LIN3\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_LIN3\_RST\_CTRL Register (Offset = 5CCh) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-3016. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 85CCh       |

**Figure 2-1004. MSS\_RCM\_MSS\_LIN3\_RST\_CTRL Name Register**

|          |    |    |    |                          |    |    |    |
|----------|----|----|----|--------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 23       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 15       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 7        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_LIN3_RST_CTRL_ASSERT |    |    |    |
| NONE     |    |    |    | R/W                      |    |    |    |
| 0h       |    |    |    | 0h                       |    |    |    |

**Table 2-3018. MSS\_RCM\_MSS\_LIN3\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                                 |
|------|--------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                                    |
| 2:0  | MSS_LIN3_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding LIN |

### 2.6.2.219 MSS\_RCM\_MSS\_LIN4\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_LIN4\_RST\_CTRL Register (Offset = 5D0h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-3019. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 85D0h       |

**Figure 2-1005. MSS\_RCM\_MSS\_LIN4\_RST\_CTRL Name Register**

|          |    |    |    |                          |    |    |    |
|----------|----|----|----|--------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 23       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 15       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 7        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_LIN4_RST_CTRL_ASSERT |    |    |    |
| NONE     |    |    |    | R/W                      |    |    |    |
| 0h       |    |    |    | 0h                       |    |    |    |

**Table 2-3021. MSS\_RCM\_MSS\_LIN4\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                                 |
|------|--------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                                    |
| 2:0  | MSS_LIN4_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding LIN |

## 2.6.2.220 MSS\_RCM\_MSS\_EDMA\_RST\_CTRL Register

### 1 MSS\_RCM\_MSS\_EDMA\_RST\_CTRL Register (Offset = 5D8h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-3022. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 85D8h       |

**Figure 2-1006. MSS\_RCM\_MSS\_EDMA\_RST\_CTRL Name Register**

|          |                                 |    |    |          |                                 |    |    |
|----------|---------------------------------|----|----|----------|---------------------------------|----|----|
| 31       | 30                              | 29 | 28 | 27       | 26                              | 25 | 24 |
| RESERVED |                                 |    |    |          |                                 |    |    |
| NONE     |                                 |    |    |          |                                 |    |    |
| 0h       |                                 |    |    |          |                                 |    |    |
| 23       | 22                              | 21 | 20 | 19       | 18                              | 17 | 16 |
| RESERVED |                                 |    |    |          |                                 |    |    |
| NONE     |                                 |    |    |          |                                 |    |    |
| 0h       |                                 |    |    |          |                                 |    |    |
| 15       | 14                              | 13 | 12 | 11       | 10                              | 9  | 8  |
| RESERVED | MSS_EDMA_RST_CTRL_TPTCA1_ASSERT |    |    | RESERVED | MSS_EDMA_RST_CTRL_TPTCA0_ASSERT |    |    |
| NONE     | R/W                             |    |    | NONE     | R/W                             |    |    |
| 0h       | 0h                              |    |    | 0h       | 0h                              |    |    |
| 7        | 6                               | 5  | 4  | 3        | 2                               | 1  | 0  |
| RESERVED | MSS_EDMA_RST_CTRL_TPCCA_ASSERT  |    |    | RESERVED | MSS_EDMA_RST_CTRL_ASSERT        |    |    |
| NONE     | R/W                             |    |    | NONE     | R/W                             |    |    |
| 0h       | 0h                              |    |    | 0h       | 0h                              |    |    |

**Table 2-3024. MSS\_RCM\_MSS\_EDMA\_RST\_CTRL Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                                                                          |
|-------|---------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:15 | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                             |
| 14:12 | MSS_EDMA_RST_CTRL_TPTCA1_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS_TPTCA1 |
| 11    | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                             |
| 10:8  | MSS_EDMA_RST_CTRL_TPTCA0_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS_TPTCA0 |
| 7     | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                             |
| 6:4   | MSS_EDMA_RST_CTRL_TPCCA_ASSERT  | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS_TPCCA  |
| 3     | RESERVED                        | NONE | 0h    | Reserved                                                                                                                                             |
| 2:0   | MSS_EDMA_RST_CTRL_ASSERT        | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset EDMA       |

## 2.6.2.221 MSS\_RCM\_MSS\_INFRA\_RST\_CTRL Register

### 1 MSS\_RCM\_MSS\_INFRA\_RST\_CTRL Register (Offset = 5DCh) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-3025. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 85DCh       |

**Figure 2-1007. MSS\_RCM\_MSS\_INFRA\_RST\_CTRL Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | MSS_INFRA_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3027. MSS\_RCM\_MSS\_INFRA\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                                                         |
|------|---------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                                                                                                            |
| 2:0  | MSS_INFRA_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS INFRA |

## 2.6.2.222 MSS\_RCM\_MSS\_CPSW\_RST\_CTRL Register

### 1 MSS\_RCM\_MSS\_CPSW\_RST\_CTRL Register (Offset = 5E0h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-3028. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 85E0h       |

**Figure 2-1008. MSS\_RCM\_MSS\_CPSW\_RST\_CTRL Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | MSS_CPSW_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-3030. MSS\_RCM\_MSS\_CPSW\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                        |
|------|--------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                           |
| 2:0  | MSS_CPSW_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS CPSW |

### 2.6.2.223 MSS\_RCM\_MSS\_PRU\_ICSS\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_PRU\_ICSS\_RST\_CTRL Register (Offset = 5E4h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-3031. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 85E4h       |

**Figure 2-1009. MSS\_RCM\_MSS\_PRU\_ICSS\_RST\_CTRL Name Register**

|          |    |    |    |    |                              |    |    |
|----------|----|----|----|----|------------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                           | 25 | 24 |
| RESERVED |    |    |    |    |                              |    |    |
| NONE     |    |    |    |    |                              |    |    |
| 0h       |    |    |    |    |                              |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                           | 17 | 16 |
| RESERVED |    |    |    |    |                              |    |    |
| NONE     |    |    |    |    |                              |    |    |
| 0h       |    |    |    |    |                              |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                           | 9  | 8  |
| RESERVED |    |    |    |    |                              |    |    |
| NONE     |    |    |    |    |                              |    |    |
| 0h       |    |    |    |    |                              |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                            | 1  | 0  |
| RESERVED |    |    |    |    | MSS_PRU_ICSS_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                          |    |    |
| 0h       |    |    |    |    | 0h                           |    |    |

**Table 2-3033. MSS\_RCM\_MSS\_PRU\_ICSS\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                        | Type | Reset | Description                                                                                                                                         |
|------|------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                     | NONE | 0h    | Reserved                                                                                                                                            |
| 2:0  | MSS_PRU_ICSS_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MSS ICSSM |

## 2.6.2.224 MSS\_RCM\_MSS\_MMCSO\_RST\_CTRL Register

### 1 MSS\_RCM\_MSS\_MMCSO\_RST\_CTRL Register (Offset = 5E8h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-3034. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 85E8h       |

**Figure 2-1010. MSS\_RCM\_MSS\_MMCSO\_RST\_CTRL Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | MSS_MMCSO_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3036. MSS\_RCM\_MSS\_MMCSO\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                                                     |
|------|---------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                                                                                                        |
| 2:0  | MSS_MMCSO_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset MMCSO |



## 2.6.2.225 MSS\_RCM\_MSS\_GPIO0\_RST\_CTRL Register

### 1 MSS\_RCM\_MSS\_GPIO0\_RST\_CTRL Register (Offset = 5ECh) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-3037. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 85ECh       |

**Figure 2-1011. MSS\_RCM\_MSS\_GPIO0\_RST\_CTRL Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | MSS_GPIO0_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3039. MSS\_RCM\_MSS\_GPIO0\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                                                                         |
|------|---------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                                                                                                                            |
| 2:0  | MSS_GPIO0_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding GPIO module |

## 2.6.2.226 MSS\_RCM\_MSS\_GPIO1\_RST\_CTRL Register

### 1 MSS\_RCM\_MSS\_GPIO1\_RST\_CTRL Register (Offset = 5F0h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-3040. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 85F0h       |

**Figure 2-1012. MSS\_RCM\_MSS\_GPIO1\_RST\_CTRL Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | MSS_GPIO1_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3042. MSS\_RCM\_MSS\_GPIO1\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                                                                         |
|------|---------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                                                                                                                            |
| 2:0  | MSS_GPIO1_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding GPIO module |

## 2.6.2.227 MSS\_RCM\_MSS\_GPIO2\_RST\_CTRL Register

### 1 MSS\_RCM\_MSS\_GPIO2\_RST\_CTRL Register (Offset = 5F4h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-3043. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 85F4h       |

**Figure 2-1013. MSS\_RCM\_MSS\_GPIO2\_RST\_CTRL Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | MSS_GPIO2_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3045. MSS\_RCM\_MSS\_GPIO2\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                                                                         |
|------|---------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                                                                                                                            |
| 2:0  | MSS_GPIO2_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding GPIO module |

## 2.6.2.228 MSS\_RCM\_MSS\_GPIO3\_RST\_CTRL Register

### 1 MSS\_RCM\_MSS\_GPIO3\_RST\_CTRL Register (Offset = 5F8h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-3046. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 85F8h       |

**Figure 2-1014. MSS\_RCM\_MSS\_GPIO3\_RST\_CTRL Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | MSS_GPIO3_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3048. MSS\_RCM\_MSS\_GPIO3\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                                                                         |
|------|---------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                                                                                                                            |
| 2:0  | MSS_GPIO3_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset corresponding GPIO module |

## 2.6.2.229 MSS\_RCM\_MSS\_SPINLOCK\_RST\_CTRL Register

### 1 MSS\_RCM\_MSS\_SPINLOCK\_RST\_CTRL Register (Offset = 5FCh) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-3049. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 85FCh       |

**Figure 2-1015. MSS\_RCM\_MSS\_SPINLOCK\_RST\_CTRL Name Register**

|          |    |    |    |    |                              |    |    |
|----------|----|----|----|----|------------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                           | 25 | 24 |
| RESERVED |    |    |    |    |                              |    |    |
| NONE     |    |    |    |    |                              |    |    |
| 0h       |    |    |    |    |                              |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                           | 17 | 16 |
| RESERVED |    |    |    |    |                              |    |    |
| NONE     |    |    |    |    |                              |    |    |
| 0h       |    |    |    |    |                              |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                           | 9  | 8  |
| RESERVED |    |    |    |    |                              |    |    |
| NONE     |    |    |    |    |                              |    |    |
| 0h       |    |    |    |    |                              |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                            | 1  | 0  |
| RESERVED |    |    |    |    | MSS_SPINLOCK_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                          |    |    |
| 0h       |    |    |    |    | 0h                           |    |    |

**Table 2-3051. MSS\_RCM\_MSS\_SPINLOCK\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                        | Type | Reset | Description                                                                                                                                        |
|------|------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                     | NONE | 0h    | Reserved                                                                                                                                           |
| 2:0  | MSS_SPINLOCK_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset SPINLOCK |

### 2.6.2.230 MSS\_RCM\_GPMC\_RST\_CTRL Register

#### 1 MSS\_RCM\_GPMC\_RST\_CTRL Register (Offset = 600h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-3052. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8600h       |

**Figure 2-1016. MSS\_RCM\_GPMC\_RST\_CTRL Name Register**

|          |    |    |    |                      |    |    |    |
|----------|----|----|----|----------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                   | 26 | 25 | 24 |
| RESERVED |    |    |    |                      |    |    |    |
| NONE     |    |    |    |                      |    |    |    |
| 0h       |    |    |    |                      |    |    |    |
| 23       | 22 | 21 | 20 | 19                   | 18 | 17 | 16 |
| RESERVED |    |    |    |                      |    |    |    |
| NONE     |    |    |    |                      |    |    |    |
| 0h       |    |    |    |                      |    |    |    |
| 15       | 14 | 13 | 12 | 11                   | 10 | 9  | 8  |
| RESERVED |    |    |    |                      |    |    |    |
| NONE     |    |    |    |                      |    |    |    |
| 0h       |    |    |    |                      |    |    |    |
| 7        | 6  | 5  | 4  | 3                    | 2  | 1  | 0  |
| RESERVED |    |    |    | GPMC_RST_CTRL_ASSERT |    |    |    |
| NONE     |    |    |    | R/W                  |    |    |    |
| 0h       |    |    |    | 0h                   |    |    |    |

**Table 2-3054. MSS\_RCM\_GPMC\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                                                                                                    |
|------|----------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED             | NONE | 0h    | Reserved                                                                                                                                       |
| 2:0  | GPMC_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset GPMC |

### 2.6.2.231 MSS\_RCM\_TEMPSENSE\_32K\_RST\_CTRL Register

#### 1 MSS\_RCM\_TEMPSENSE\_32K\_RST\_CTRL Register (Offset = 604h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-3055. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8604h       |

**Figure 2-1017. MSS\_RCM\_TEMPSENSE\_32K\_RST\_CTRL Name Register**

|          |    |    |    |    |                               |    |    |
|----------|----|----|----|----|-------------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                            | 25 | 24 |
| RESERVED |    |    |    |    |                               |    |    |
| NONE     |    |    |    |    |                               |    |    |
| 0h       |    |    |    |    |                               |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                            | 17 | 16 |
| RESERVED |    |    |    |    |                               |    |    |
| NONE     |    |    |    |    |                               |    |    |
| 0h       |    |    |    |    |                               |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                            | 9  | 8  |
| RESERVED |    |    |    |    |                               |    |    |
| NONE     |    |    |    |    |                               |    |    |
| 0h       |    |    |    |    |                               |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                             | 1  | 0  |
| RESERVED |    |    |    |    | TEMPSENSE_32K_RST_CTRL_ASSERT |    |    |
| NONE     |    |    |    |    | R/W                           |    |    |
| 0h       |    |    |    |    | 0h                            |    |    |

**Table 2-3057. MSS\_RCM\_TEMPSENSE\_32K\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                                                                                                                                                                          |
|------|-------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                      | NONE | 0h    | Reserved                                                                                                                                                                                             |
| 2:0  | TEMPSENSE_32K_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset TEMPSSENSE<br>**Note: This bit will only be reset by PORz. |

### 2.6.2.232 MSS\_RCM\_MSS\_ELM\_RST\_CTRL Register

#### 1 MSS\_RCM\_MSS\_ELM\_RST\_CTRL Register (Offset = 608h) [reset = 0h]

This register is used to Reset respective IP.

Return to [Summary Table](#)

**Table 2-3058. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8608h       |

**Figure 2-1018. MSS\_RCM\_MSS\_ELM\_RST\_CTRL Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | MSS_ELM_RST_CTRL_ASSERT |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-3060. MSS\_RCM\_MSS\_ELM\_RST\_CTRL Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                                                                                                                   |
|------|-------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                      |
| 2:0  | MSS_ELM_RST_CTRL_ASSERT | R/W  | 0h    | This feature is for debug purpose only. Software needs to ensure the state of the Device/IP before configuring. Writing 3'b111 will reset ELM |



### 2.6.2.233 MSS\_RCM\_MSS\_L2OCRAM\_BANK0\_PD\_CTRL Register

#### 1 MSS\_RCM\_MSS\_L2OCRAM\_BANK0\_PD\_CTRL Register (Offset = 700h) [reset = 770h]

S/W control to Powers down the L2 Bank 0 and disconnect from Interconnect. AON AGOOD 0 or ISO =1 causes bus disconnect.

Return to [Summary Table](#)

**Table 2-3061. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8700h       |

**Figure 2-1019. MSS\_RCM\_MSS\_L2OCRAM\_BANK0\_PD\_CTRL Name Register**

|          |                            |    |    |          |                              |    |    |
|----------|----------------------------|----|----|----------|------------------------------|----|----|
| 31       | 30                         | 29 | 28 | 27       | 26                           | 25 | 24 |
| RESERVED |                            |    |    |          |                              |    |    |
| NONE     |                            |    |    |          |                              |    |    |
| 0h       |                            |    |    |          |                              |    |    |
| 23       | 22                         | 21 | 20 | 19       | 18                           | 17 | 16 |
| RESERVED |                            |    |    |          |                              |    |    |
| NONE     |                            |    |    |          |                              |    |    |
| 0h       |                            |    |    |          |                              |    |    |
| 15       | 14                         | 13 | 12 | 11       | 10                           | 9  | 8  |
| RESERVED |                            |    |    |          | MSS_L2_BANKA_PD_CTRL_AGOODIN |    |    |
| NONE     |                            |    |    |          | R/W                          |    |    |
| 0h       |                            |    |    |          | 7h                           |    |    |
| 7        | 6                          | 5  | 4  | 3        | 2                            | 1  | 0  |
| RESERVED | MSS_L2_BANKA_PD_CTRL_AONIN |    |    | RESERVED | MSS_L2_BANKA_PD_CTRL_ISO     |    |    |
| NONE     | R/W                        |    |    | NONE     | R/W                          |    |    |
| 0h       | 7h                         |    |    | 0h       | 0h                           |    |    |

**Table 2-3063. MSS\_RCM\_MSS\_L2OCRAM\_BANK0\_PD\_CTRL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                            |
|-------|------------------------------|------|-------|--------------------------------------------------------|
| 31:11 | RESERVED                     | NONE | 0h    | Reserved                                               |
| 10:8  | MSS_L2_BANKA_PD_CTRL_AGOODIN | R/W  | 7h    | SW control for power signal 'AGOODIN' for MSS_L2_BANKA |
| 7     | RESERVED                     | NONE | 0h    | Reserved                                               |
| 6:4   | MSS_L2_BANKA_PD_CTRL_AONIN   | R/W  | 7h    | SW control for power signal 'AONIN' for MSS_L2_BANKA   |
| 3     | RESERVED                     | NONE | 0h    | Reserved                                               |
| 2:0   | MSS_L2_BANKA_PD_CTRL_ISO     | R/W  | 0h    | SW control for power signal 'ISO' for MSS_L2_BANKA.    |

## 2.6.2.234 MSS\_RCM\_MSS\_L2OCRAM\_BANK1\_PD\_CTRL Register

### 1 MSS\_RCM\_MSS\_L2OCRAM\_BANK1\_PD\_CTRL Register (Offset = 704h) [reset = 770h]

S/W control to Powers down the L2 Bank 1 and disconnect from Interconnect.

Return to [Summary Table](#)

**Table 2-3064. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8704h       |

**Figure 2-1020. MSS\_RCM\_MSS\_L2OCRAM\_BANK1\_PD\_CTRL Name Register**

|          |                            |    |    |          |                              |    |    |
|----------|----------------------------|----|----|----------|------------------------------|----|----|
| 31       | 30                         | 29 | 28 | 27       | 26                           | 25 | 24 |
| RESERVED |                            |    |    |          |                              |    |    |
| NONE     |                            |    |    |          |                              |    |    |
| 0h       |                            |    |    |          |                              |    |    |
| 23       | 22                         | 21 | 20 | 19       | 18                           | 17 | 16 |
| RESERVED |                            |    |    |          |                              |    |    |
| NONE     |                            |    |    |          |                              |    |    |
| 0h       |                            |    |    |          |                              |    |    |
| 15       | 14                         | 13 | 12 | 11       | 10                           | 9  | 8  |
| RESERVED |                            |    |    |          | MSS_L2_BANKB_PD_CTRL_AGOODIN |    |    |
| NONE     |                            |    |    |          | R/W                          |    |    |
| 0h       |                            |    |    |          | 7h                           |    |    |
| 7        | 6                          | 5  | 4  | 3        | 2                            | 1  | 0  |
| RESERVED | MSS_L2_BANKB_PD_CTRL_AONIN |    |    | RESERVED | MSS_L2_BANKB_PD_CTRL_ISO     |    |    |
| NONE     | R/W                        |    |    | NONE     | R/W                          |    |    |
| 0h       | 7h                         |    |    | 0h       | 0h                           |    |    |

**Table 2-3066. MSS\_RCM\_MSS\_L2OCRAM\_BANK1\_PD\_CTRL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                            |
|-------|------------------------------|------|-------|--------------------------------------------------------|
| 31:11 | RESERVED                     | NONE | 0h    | Reserved                                               |
| 10:8  | MSS_L2_BANKB_PD_CTRL_AGOODIN | R/W  | 7h    | SW control for power signal 'AGOODIN' for MSS_L2_BANKB |
| 7     | RESERVED                     | NONE | 0h    | Reserved                                               |
| 6:4   | MSS_L2_BANKB_PD_CTRL_AONIN   | R/W  | 7h    | SW control for power signal 'AONIN' for MSS_L2_BANKB   |
| 3     | RESERVED                     | NONE | 0h    | Reserved                                               |
| 2:0   | MSS_L2_BANKB_PD_CTRL_ISO     | R/W  | 0h    | SW control for power signal 'ISO' for MSS_L2_BANKB     |

## 2.6.2.235 MSS\_RCM\_MSS\_L2OCRAM\_BANK2\_PD\_CTRL Register

### 1 MSS\_RCM\_MSS\_L2OCRAM\_BANK2\_PD\_CTRL Register (Offset = 708h) [reset = 770h]

S/W control to Powers down the L2 Bank 2 and disconnect from Interconnect.

Return to [Summary Table](#)

**Table 2-3067. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8708h       |

**Figure 2-1021. MSS\_RCM\_MSS\_L2OCRAM\_BANK2\_PD\_CTRL Name Register**

|          |                            |    |    |          |                              |    |    |
|----------|----------------------------|----|----|----------|------------------------------|----|----|
| 31       | 30                         | 29 | 28 | 27       | 26                           | 25 | 24 |
| RESERVED |                            |    |    |          |                              |    |    |
| NONE     |                            |    |    |          |                              |    |    |
| 0h       |                            |    |    |          |                              |    |    |
| 23       | 22                         | 21 | 20 | 19       | 18                           | 17 | 16 |
| RESERVED |                            |    |    |          |                              |    |    |
| NONE     |                            |    |    |          |                              |    |    |
| 0h       |                            |    |    |          |                              |    |    |
| 15       | 14                         | 13 | 12 | 11       | 10                           | 9  | 8  |
| RESERVED |                            |    |    |          | MSS_L2_BANKC_PD_CTRL_AGOODIN |    |    |
| NONE     |                            |    |    |          | R/W                          |    |    |
| 0h       |                            |    |    |          | 7h                           |    |    |
| 7        | 6                          | 5  | 4  | 3        | 2                            | 1  | 0  |
| RESERVED | MSS_L2_BANKC_PD_CTRL_AONIN |    |    | RESERVED | MSS_L2_BANKC_PD_CTRL_ISO     |    |    |
| NONE     | R/W                        |    |    | NONE     | R/W                          |    |    |
| 0h       | 7h                         |    |    | 0h       | 0h                           |    |    |

**Table 2-3069. MSS\_RCM\_MSS\_L2OCRAM\_BANK2\_PD\_CTRL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                            |
|-------|------------------------------|------|-------|--------------------------------------------------------|
| 31:11 | RESERVED                     | NONE | 0h    | Reserved                                               |
| 10:8  | MSS_L2_BANKC_PD_CTRL_AGOODIN | R/W  | 7h    | SW control for power signal 'AGOODIN' for MSS_L2_BANKC |
| 7     | RESERVED                     | NONE | 0h    | Reserved                                               |
| 6:4   | MSS_L2_BANKC_PD_CTRL_AONIN   | R/W  | 7h    | SW control for power signal 'AONIN' for MSS_L2_BANKC   |
| 3     | RESERVED                     | NONE | 0h    | Reserved                                               |
| 2:0   | MSS_L2_BANKC_PD_CTRL_ISO     | R/W  | 0h    | SW control for power signal 'ISO' for MSS_L2_BANKC     |

## 2.6.2.236 MSS\_RCM\_MSS\_L2\_BANKD\_PD\_CTRL Register

### 1 MSS\_RCM\_MSS\_L2\_BANKD\_PD\_CTRL Register (Offset = 70Ch) [reset = 770h]

S/W control to Powers down the L2 Bank 3 and disconnect from Interconnect.

Return to [Summary Table](#)

**Table 2-3070. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 870Ch       |

**Figure 2-1022. MSS\_RCM\_MSS\_L2\_BANKD\_PD\_CTRL Name Register**

|          |                            |    |    |          |                              |    |    |
|----------|----------------------------|----|----|----------|------------------------------|----|----|
| 31       | 30                         | 29 | 28 | 27       | 26                           | 25 | 24 |
| RESERVED |                            |    |    |          |                              |    |    |
| NONE     |                            |    |    |          |                              |    |    |
| 0h       |                            |    |    |          |                              |    |    |
| 23       | 22                         | 21 | 20 | 19       | 18                           | 17 | 16 |
| RESERVED |                            |    |    |          |                              |    |    |
| NONE     |                            |    |    |          |                              |    |    |
| 0h       |                            |    |    |          |                              |    |    |
| 15       | 14                         | 13 | 12 | 11       | 10                           | 9  | 8  |
| RESERVED |                            |    |    |          | MSS_L2_BANKD_PD_CTRL_AGOODIN |    |    |
| NONE     |                            |    |    |          | R/W                          |    |    |
| 0h       |                            |    |    |          | 7h                           |    |    |
| 7        | 6                          | 5  | 4  | 3        | 2                            | 1  | 0  |
| RESERVED | MSS_L2_BANKD_PD_CTRL_AONIN |    |    | RESERVED | MSS_L2_BANKD_PD_CTRL_ISO     |    |    |
| NONE     | R/W                        |    |    | NONE     | R/W                          |    |    |
| 0h       | 7h                         |    |    | 0h       | 0h                           |    |    |

**Table 2-3072. MSS\_RCM\_MSS\_L2\_BANKD\_PD\_CTRL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                            |
|-------|------------------------------|------|-------|--------------------------------------------------------|
| 31:11 | RESERVED                     | NONE | 0h    | Reserved                                               |
| 10:8  | MSS_L2_BANKD_PD_CTRL_AGOODIN | R/W  | 7h    | SW control for power signal 'AGOODIN' for MSS_L2_BANKD |
| 7     | RESERVED                     | NONE | 0h    | Reserved                                               |
| 6:4   | MSS_L2_BANKD_PD_CTRL_AONIN   | R/W  | 7h    | SW control for power signal 'AONIN' for MSS_L2_BANKD   |
| 3     | RESERVED                     | NONE | 0h    | Reserved                                               |
| 2:0   | MSS_L2_BANKD_PD_CTRL_ISO     | R/W  | 0h    | SW control for power signal 'ISO' for MSS_L2_BANKD     |

## 2.6.2.237 MSS\_RCM\_MSS\_L2OCRAM\_BANK0\_PD\_STATUS Register

### 1 MSS\_RCM\_MSS\_L2OCRAM\_BANK0\_PD\_STATUS Register (Offset = 710h) [reset = 3h]

L2 Bank PD status. Pgood out observation.

Return to [Summary Table](#)

**Table 2-3073. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8710h       |

**Figure 2-1023. MSS\_RCM\_MSS\_L2OCRAM\_BANK0\_PD\_STATUS Name Register**

|          |    |    |    |    |    |                                         |                                       |
|----------|----|----|----|----|----|-----------------------------------------|---------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25                                      | 24                                    |
| RESERVED |    |    |    |    |    |                                         |                                       |
| NONE     |    |    |    |    |    |                                         |                                       |
| 0h       |    |    |    |    |    |                                         |                                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17                                      | 16                                    |
| RESERVED |    |    |    |    |    |                                         |                                       |
| NONE     |    |    |    |    |    |                                         |                                       |
| 0h       |    |    |    |    |    |                                         |                                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9                                       | 8                                     |
| RESERVED |    |    |    |    |    |                                         |                                       |
| NONE     |    |    |    |    |    |                                         |                                       |
| 0h       |    |    |    |    |    |                                         |                                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1                                       | 0                                     |
| RESERVED |    |    |    |    |    | MSS_L2_BANK<br>A_PD_STATUS<br>_AGOODOUT | MSS_L2_BANK<br>A_PD_STATUS<br>_AONOUT |
| NONE     |    |    |    |    |    | R                                       | R                                     |
| 0h       |    |    |    |    |    | 1h                                      | 1h                                    |

**Table 2-3075. MSS\_RCM\_MSS\_L2OCRAM\_BANK0\_PD\_STATUS Register Field Descriptions**

| Bit  | Field                               | Type | Reset | Description                                        |
|------|-------------------------------------|------|-------|----------------------------------------------------|
| 31:2 | RESERVED                            | NONE | 0h    | Reserved                                           |
| 1    | MSS_L2_BANKA_PD_ST<br>ATUS_AGOODOUT | R    | 1h    | SW status indicating the 'pgoodin' of MSS_L2_BANKA |
| 0    | MSS_L2_BANKA_PD_ST<br>ATUS_AONOUT   | R    | 1h    | SW status indicating the 'ponin' of MSS_L2_BANKA   |

## 2.6.2.238 MSS\_RCM\_MSS\_L2OCRAM\_BANK1\_PD\_STATUS Register

### 1 MSS\_RCM\_MSS\_L2OCRAM\_BANK1\_PD\_STATUS Register (Offset = 714h) [reset = 3h]

L2 Bank PD status. Pgood out observation.

Return to [Summary Table](#)

**Table 2-3076. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8714h       |

**Figure 2-1024. MSS\_RCM\_MSS\_L2OCRAM\_BANK1\_PD\_STATUS Name Register**

|          |    |    |    |    |    |                                         |                                       |
|----------|----|----|----|----|----|-----------------------------------------|---------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25                                      | 24                                    |
| RESERVED |    |    |    |    |    |                                         |                                       |
| NONE     |    |    |    |    |    |                                         |                                       |
| 0h       |    |    |    |    |    |                                         |                                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17                                      | 16                                    |
| RESERVED |    |    |    |    |    |                                         |                                       |
| NONE     |    |    |    |    |    |                                         |                                       |
| 0h       |    |    |    |    |    |                                         |                                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9                                       | 8                                     |
| RESERVED |    |    |    |    |    |                                         |                                       |
| NONE     |    |    |    |    |    |                                         |                                       |
| 0h       |    |    |    |    |    |                                         |                                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1                                       | 0                                     |
| RESERVED |    |    |    |    |    | MSS_L2_BANK<br>B_PD_STATUS<br>_AGOODOUT | MSS_L2_BANK<br>B_PD_STATUS<br>_AONOUT |
| NONE     |    |    |    |    |    | R                                       | R                                     |
| 0h       |    |    |    |    |    | 1h                                      | 1h                                    |

**Table 2-3078. MSS\_RCM\_MSS\_L2OCRAM\_BANK1\_PD\_STATUS Register Field Descriptions**

| Bit  | Field                               | Type | Reset | Description                                        |
|------|-------------------------------------|------|-------|----------------------------------------------------|
| 31:2 | RESERVED                            | NONE | 0h    | Reserved                                           |
| 1    | MSS_L2_BANKB_PD_ST<br>ATUS_AGOODOUT | R    | 1h    | SW status indicating the 'pgoodin' of MSS_L2_BANKB |
| 0    | MSS_L2_BANKB_PD_ST<br>ATUS_AONOUT   | R    | 1h    | SW status indicating the 'ponin' of MSS_L2_BANKB   |

## 2.6.2.239 MSS\_RCM\_MSS\_L2OCRAM\_BANK2\_PD\_STATUS Register

### 1 MSS\_RCM\_MSS\_L2OCRAM\_BANK2\_PD\_STATUS Register (Offset = 718h) [reset = 3h]

L2 Bank PD status. Pgood out observation.

Return to [Summary Table](#)

**Table 2-3079. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8718h       |

**Figure 2-1025. MSS\_RCM\_MSS\_L2OCRAM\_BANK2\_PD\_STATUS Name Register**

|          |    |    |    |    |    |                                         |                                       |
|----------|----|----|----|----|----|-----------------------------------------|---------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25                                      | 24                                    |
| RESERVED |    |    |    |    |    |                                         |                                       |
| NONE     |    |    |    |    |    |                                         |                                       |
| 0h       |    |    |    |    |    |                                         |                                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17                                      | 16                                    |
| RESERVED |    |    |    |    |    |                                         |                                       |
| NONE     |    |    |    |    |    |                                         |                                       |
| 0h       |    |    |    |    |    |                                         |                                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9                                       | 8                                     |
| RESERVED |    |    |    |    |    |                                         |                                       |
| NONE     |    |    |    |    |    |                                         |                                       |
| 0h       |    |    |    |    |    |                                         |                                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1                                       | 0                                     |
| RESERVED |    |    |    |    |    | MSS_L2_BANK<br>C_PD_STATUS<br>_AGOODOUT | MSS_L2_BANK<br>C_PD_STATUS<br>_AONOUT |
| NONE     |    |    |    |    |    | R                                       | R                                     |
| 0h       |    |    |    |    |    | 1h                                      | 1h                                    |

**Table 2-3081. MSS\_RCM\_MSS\_L2OCRAM\_BANK2\_PD\_STATUS Register Field Descriptions**

| Bit  | Field                               | Type | Reset | Description                                        |
|------|-------------------------------------|------|-------|----------------------------------------------------|
| 31:2 | RESERVED                            | NONE | 0h    | Reserved                                           |
| 1    | MSS_L2_BANKC_PD_ST<br>ATUS_AGOODOUT | R    | 1h    | SW status indicating the 'pgoodin' of MSS_L2_BANKC |
| 0    | MSS_L2_BANKC_PD_ST<br>ATUS_AONOUT   | R    | 1h    | SW status indicating the 'ponin' of MSS_L2_BANKC   |

## 2.6.2.240 MSS\_RCM\_MSS\_L2\_BANKD\_PD\_STATUS Register

### 1 MSS\_RCM\_MSS\_L2\_BANKD\_PD\_STATUS Register (Offset = 71Ch) [reset = 3h]

L2 Bank PD status. Pgood out observation.

Return to [Summary Table](#)

**Table 2-3082. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 871Ch       |

**Figure 2-1026. MSS\_RCM\_MSS\_L2\_BANKD\_PD\_STATUS Name Register**

|          |    |    |    |    |    |                                         |                                       |
|----------|----|----|----|----|----|-----------------------------------------|---------------------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25                                      | 24                                    |
| RESERVED |    |    |    |    |    |                                         |                                       |
| NONE     |    |    |    |    |    |                                         |                                       |
| 0h       |    |    |    |    |    |                                         |                                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17                                      | 16                                    |
| RESERVED |    |    |    |    |    |                                         |                                       |
| NONE     |    |    |    |    |    |                                         |                                       |
| 0h       |    |    |    |    |    |                                         |                                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9                                       | 8                                     |
| RESERVED |    |    |    |    |    |                                         |                                       |
| NONE     |    |    |    |    |    |                                         |                                       |
| 0h       |    |    |    |    |    |                                         |                                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1                                       | 0                                     |
| RESERVED |    |    |    |    |    | MSS_L2_BANK<br>D_PD_STATUS<br>_AGOODOUT | MSS_L2_BANK<br>D_PD_STATUS<br>_AONOUT |
| NONE     |    |    |    |    |    | R                                       | R                                     |
| 0h       |    |    |    |    |    | 1h                                      | 1h                                    |

**Table 2-3084. MSS\_RCM\_MSS\_L2\_BANKD\_PD\_STATUS Register Field Descriptions**

| Bit  | Field                               | Type | Reset | Description                                        |
|------|-------------------------------------|------|-------|----------------------------------------------------|
| 31:2 | RESERVED                            | NONE | 0h    | Reserved                                           |
| 1    | MSS_L2_BANKD_PD_ST<br>ATUS_AGOODOUT | R    | 1h    | SW status indicating the 'pgoodin' of MSS_L2_BANKD |
| 0    | MSS_L2_BANKD_PD_ST<br>ATUS_AONOUT   | R    | 1h    | SW status indicating the 'ponin' of MSS_L2_BANKD   |



## 2.6.2.241 MSS\_RCM\_HSM\_RTIA\_CLK\_SRC\_SEL Register

### 1 MSS\_RCM\_HSM\_RTIA\_CLK\_SRC\_SEL Register (Offset = 800h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-3085. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8800h       |

**Figure 2-1027. MSS\_RCM\_HSM\_RTIA\_CLK\_SRC\_SEL Name Register**

|                                |    |    |    |                                |    |    |    |
|--------------------------------|----|----|----|--------------------------------|----|----|----|
| 31                             | 30 | 29 | 28 | 27                             | 26 | 25 | 24 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 23                             | 22 | 21 | 20 | 19                             | 18 | 17 | 16 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 15                             | 14 | 13 | 12 | 11                             | 10 | 9  | 8  |
| RESERVED                       |    |    |    | HSM_RTIA_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                           |    |    |    | R/W                            |    |    |    |
| 0h                             |    |    |    | 0h                             |    |    |    |
| 7                              | 6  | 5  | 4  | 3                              | 2  | 1  | 0  |
| HSM_RTIA_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                |    |    |    |
| R/W                            |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |

**Table 2-3087. MSS\_RCM\_HSM\_RTIA\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|--------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 11:0  | HSM_RTIA_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for HSM_Corresponding RTI. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register.<br>Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - XTALCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - RCCLK10M<br>0x555 - RCCLK10M<br>0x666 - EXT_REFCLK<br>0x777 - RCCLK32K |

## 2.6.2.242 MSS\_RCM\_HSM\_WDT\_CLK\_SRC\_SEL Register

### 1 MSS\_RCM\_HSM\_WDT\_CLK\_SRC\_SEL Register (Offset = 804h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-3088. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8804h       |

**Figure 2-1028. MSS\_RCM\_HSM\_WDT\_CLK\_SRC\_SEL Name Register**

|                               |    |    |    |                               |    |    |    |
|-------------------------------|----|----|----|-------------------------------|----|----|----|
| 31                            | 30 | 29 | 28 | 27                            | 26 | 25 | 24 |
| RESERVED                      |    |    |    |                               |    |    |    |
| NONE                          |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |
| 23                            | 22 | 21 | 20 | 19                            | 18 | 17 | 16 |
| RESERVED                      |    |    |    |                               |    |    |    |
| NONE                          |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |
| 15                            | 14 | 13 | 12 | 11                            | 10 | 9  | 8  |
| RESERVED                      |    |    |    | HSM_WDT_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                          |    |    |    | R/W                           |    |    |    |
| 0h                            |    |    |    | 0h                            |    |    |    |
| 7                             | 6  | 5  | 4  | 3                             | 2  | 1  | 0  |
| HSM_WDT_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                               |    |    |    |
| R/W                           |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |

**Table 2-3090. MSS\_RCM\_HSM\_WDT\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                         | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|-------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                      | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                            |
| 11:0  | HSM_WDT_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for HSM_WDT. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register.<br>Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - XTALCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - RCCLK10M<br>0x555 - RCCLK10M<br>0x666 - EXT_REFCLK<br>0x777 - RCCLK32K |

## 2.6.2.243 MSS\_RCM\_HSM\_RTC\_CLK\_SRC\_SEL Register

### 1 MSS\_RCM\_HSM\_RTC\_CLK\_SRC\_SEL Register (Offset = 808h) [reset = 777h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-3091. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8808h       |

**Figure 2-1029. MSS\_RCM\_HSM\_RTC\_CLK\_SRC\_SEL Name Register**

|                               |    |    |    |                               |    |    |    |
|-------------------------------|----|----|----|-------------------------------|----|----|----|
| 31                            | 30 | 29 | 28 | 27                            | 26 | 25 | 24 |
| RESERVED                      |    |    |    |                               |    |    |    |
| NONE                          |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |
| 23                            | 22 | 21 | 20 | 19                            | 18 | 17 | 16 |
| RESERVED                      |    |    |    |                               |    |    |    |
| NONE                          |    |    |    |                               |    |    |    |
| 0h                            |    |    |    |                               |    |    |    |
| 15                            | 14 | 13 | 12 | 11                            | 10 | 9  | 8  |
| RESERVED                      |    |    |    | HSM_RTC_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                          |    |    |    | R/W                           |    |    |    |
| 0h                            |    |    |    | 777h                          |    |    |    |
| 7                             | 6  | 5  | 4  | 3                             | 2  | 1  | 0  |
| HSM_RTC_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                               |    |    |    |
| R/W                           |    |    |    |                               |    |    |    |
| 777h                          |    |    |    |                               |    |    |    |

**Table 2-3093. MSS\_RCM\_HSM\_RTC\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                             | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|-----------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                          | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                            |
| 11:0  | HSM_RTC_CLK_SRC_SE<br>L_CLKSRCSEL | R/W  | 777h  | Select line for selecting source clock for HSM_RTC. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register.<br>Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - XTALCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - RCCLK10M<br>0x555 - RCCLK10M<br>0x666 - EXT_REFCLK<br>0x777 - RCCLK32K |

## 2.6.2.244 MSS\_RCM\_HSM\_DMTA\_CLK\_SRC\_SEL Register

### 1 MSS\_RCM\_HSM\_DMTA\_CLK\_SRC\_SEL Register (Offset = 80Ch) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-3094. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 880Ch       |

**Figure 2-1030. MSS\_RCM\_HSM\_DMTA\_CLK\_SRC\_SEL Name Register**

|                                |    |    |    |                                |    |    |    |
|--------------------------------|----|----|----|--------------------------------|----|----|----|
| 31                             | 30 | 29 | 28 | 27                             | 26 | 25 | 24 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 23                             | 22 | 21 | 20 | 19                             | 18 | 17 | 16 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 15                             | 14 | 13 | 12 | 11                             | 10 | 9  | 8  |
| RESERVED                       |    |    |    | HSM_DMTA_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                           |    |    |    | R/W                            |    |    |    |
| 0h                             |    |    |    | 0h                             |    |    |    |
| 7                              | 6  | 5  | 4  | 3                              | 2  | 1  | 0  |
| HSM_DMTA_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                |    |    |    |
| R/W                            |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |

**Table 2-3096. MSS\_RCM\_HSM\_DMTA\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|--------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                             |
| 11:0  | HSM_DMTA_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for HSM_DMTA. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register.<br>Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - XTALCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - RCCLK10M<br>0x555 - RCCLK10M<br>0x666 - EXT_REFCLK<br>0x777 - RCCLK32K |

## 2.6.2.245 MSS\_RCM\_HSM\_DMTB\_CLK\_SRC\_SEL Register

### 1 MSS\_RCM\_HSM\_DMTB\_CLK\_SRC\_SEL Register (Offset = 810h) [reset = 0h]

This Register is used for selecting the clock source for Corresponding root clock.

Return to [Summary Table](#)

**Table 2-3097. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8810h       |

**Figure 2-1031. MSS\_RCM\_HSM\_DMTB\_CLK\_SRC\_SEL Name Register**

|                                |    |    |    |                                |    |    |    |
|--------------------------------|----|----|----|--------------------------------|----|----|----|
| 31                             | 30 | 29 | 28 | 27                             | 26 | 25 | 24 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 23                             | 22 | 21 | 20 | 19                             | 18 | 17 | 16 |
| RESERVED                       |    |    |    |                                |    |    |    |
| NONE                           |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |
| 15                             | 14 | 13 | 12 | 11                             | 10 | 9  | 8  |
| RESERVED                       |    |    |    | HSM_DMTB_CLK_SRC_SEL_CLKSRCSEL |    |    |    |
| NONE                           |    |    |    | R/W                            |    |    |    |
| 0h                             |    |    |    | 0h                             |    |    |    |
| 7                              | 6  | 5  | 4  | 3                              | 2  | 1  | 0  |
| HSM_DMTB_CLK_SRC_SEL_CLKSRCSEL |    |    |    |                                |    |    |    |
| R/W                            |    |    |    |                                |    |    |    |
| 0h                             |    |    |    |                                |    |    |    |

**Table 2-3099. MSS\_RCM\_HSM\_DMTB\_CLK\_SRC\_SEL Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|--------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                             |
| 11:0  | HSM_DMTB_CLK_SRC_SEL_CLKSRCSEL | R/W  | 0h    | Select line for selecting source clock for HSM_DMTB. Data should be loaded as multibit.<br>For example: if '0x5' should be selected then '0x555' should be configured to the register.<br>Use the following values to select clk src-<br>0x000 - WUCPUCLK<br>0x111 - XTALCLK<br>0x222 - SYS_CLK<br>0x333 - DPLL_PER_HSDIV0_CLKOUT1<br>0x444 - RCCLK10M<br>0x555 - RCCLK10M<br>0x666 - EXT_REFCLK<br>0x777 - RCCLK32K |

## 2.6.2.246 MSS\_RCM\_HSM\_RTI\_CLK\_DIV\_VAL Register

### 1 MSS\_RCM\_HSM\_RTI\_CLK\_DIV\_VAL Register (Offset = 814h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-3100. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8814h       |

**Figure 2-1032. MSS\_RCM\_HSM\_RTI\_CLK\_DIV\_VAL Name Register**

|                             |    |    |    |                             |    |    |    |
|-----------------------------|----|----|----|-----------------------------|----|----|----|
| 31                          | 30 | 29 | 28 | 27                          | 26 | 25 | 24 |
| RESERVED                    |    |    |    |                             |    |    |    |
| NONE                        |    |    |    |                             |    |    |    |
| 0h                          |    |    |    |                             |    |    |    |
| 23                          | 22 | 21 | 20 | 19                          | 18 | 17 | 16 |
| RESERVED                    |    |    |    |                             |    |    |    |
| NONE                        |    |    |    |                             |    |    |    |
| 0h                          |    |    |    |                             |    |    |    |
| 15                          | 14 | 13 | 12 | 11                          | 10 | 9  | 8  |
| RESERVED                    |    |    |    | HSM_RTI_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                        |    |    |    | R/W                         |    |    |    |
| 0h                          |    |    |    | 0h                          |    |    |    |
| 7                           | 6  | 5  | 4  | 3                           | 2  | 1  | 0  |
| HSM_RTI_CLK_DIV_VAL_CLKDIVR |    |    |    |                             |    |    |    |
| R/W                         |    |    |    |                             |    |    |    |
| 0h                          |    |    |    |                             |    |    |    |

**Table 2-3102. MSS\_RCM\_HSM\_RTI\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                       | Type | Reset | Description                                                                                                                                                                                                                                                     |
|-------|-----------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                    | NONE | 0h    | Reserved                                                                                                                                                                                                                                                        |
| 11:0  | HSM_RTI_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value HSM RTI selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

## 2.6.2.247 MSS\_RCM\_HSM\_WDT\_CLK\_DIV\_VAL Register

### 1 MSS\_RCM\_HSM\_WDT\_CLK\_DIV\_VAL Register (Offset = 818h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-3103. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8818h       |

**Figure 2-1033. MSS\_RCM\_HSM\_WDT\_CLK\_DIV\_VAL Name Register**

|                             |    |    |    |                             |    |    |    |
|-----------------------------|----|----|----|-----------------------------|----|----|----|
| 31                          | 30 | 29 | 28 | 27                          | 26 | 25 | 24 |
| RESERVED                    |    |    |    |                             |    |    |    |
| NONE                        |    |    |    |                             |    |    |    |
| 0h                          |    |    |    |                             |    |    |    |
| 23                          | 22 | 21 | 20 | 19                          | 18 | 17 | 16 |
| RESERVED                    |    |    |    |                             |    |    |    |
| NONE                        |    |    |    |                             |    |    |    |
| 0h                          |    |    |    |                             |    |    |    |
| 15                          | 14 | 13 | 12 | 11                          | 10 | 9  | 8  |
| RESERVED                    |    |    |    | HSM_WDT_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                        |    |    |    | R/W                         |    |    |    |
| 0h                          |    |    |    | 0h                          |    |    |    |
| 7                           | 6  | 5  | 4  | 3                           | 2  | 1  | 0  |
| HSM_WDT_CLK_DIV_VAL_CLKDIVR |    |    |    |                             |    |    |    |
| R/W                         |    |    |    |                             |    |    |    |
| 0h                          |    |    |    |                             |    |    |    |

**Table 2-3105. MSS\_RCM\_HSM\_WDT\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                       | Type | Reset | Description                                                                                                                                                                                                                                                     |
|-------|-----------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                    | NONE | 0h    | Reserved                                                                                                                                                                                                                                                        |
| 11:0  | HSM_WDT_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value HSM WDT selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

## 2.6.2.248 MSS\_RCM\_HSM\_RTC\_CLK\_DIV\_VAL Register

### 1 MSS\_RCM\_HSM\_RTC\_CLK\_DIV\_VAL Register (Offset = 81Ch) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-3106. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 881Ch       |

**Figure 2-1034. MSS\_RCM\_HSM\_RTC\_CLK\_DIV\_VAL Name Register**

|                             |    |    |    |                             |    |    |    |
|-----------------------------|----|----|----|-----------------------------|----|----|----|
| 31                          | 30 | 29 | 28 | 27                          | 26 | 25 | 24 |
| RESERVED                    |    |    |    |                             |    |    |    |
| NONE                        |    |    |    |                             |    |    |    |
| 0h                          |    |    |    |                             |    |    |    |
| 23                          | 22 | 21 | 20 | 19                          | 18 | 17 | 16 |
| RESERVED                    |    |    |    |                             |    |    |    |
| NONE                        |    |    |    |                             |    |    |    |
| 0h                          |    |    |    |                             |    |    |    |
| 15                          | 14 | 13 | 12 | 11                          | 10 | 9  | 8  |
| RESERVED                    |    |    |    | HSM_RTC_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                        |    |    |    | R/W                         |    |    |    |
| 0h                          |    |    |    | 0h                          |    |    |    |
| 7                           | 6  | 5  | 4  | 3                           | 2  | 1  | 0  |
| HSM_RTC_CLK_DIV_VAL_CLKDIVR |    |    |    |                             |    |    |    |
| R/W                         |    |    |    |                             |    |    |    |
| 0h                          |    |    |    |                             |    |    |    |

**Table 2-3108. MSS\_RCM\_HSM\_RTC\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                       | Type | Reset | Description                                                                                                                                                                                                                                                     |
|-------|-----------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                    | NONE | 0h    | Reserved                                                                                                                                                                                                                                                        |
| 11:0  | HSM_RTC_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value HSM RTC selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |



### 2.6.2.249 MSS\_RCM\_HSM\_DMTA\_CLK\_DIV\_VAL Register

#### 1 MSS\_RCM\_HSM\_DMTA\_CLK\_DIV\_VAL Register (Offset = 820h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-3109. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8820h       |

**Figure 2-1035. MSS\_RCM\_HSM\_DMTA\_CLK\_DIV\_VAL Name Register**

|                              |    |    |    |                              |    |    |    |
|------------------------------|----|----|----|------------------------------|----|----|----|
| 31                           | 30 | 29 | 28 | 27                           | 26 | 25 | 24 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 23                           | 22 | 21 | 20 | 19                           | 18 | 17 | 16 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 15                           | 14 | 13 | 12 | 11                           | 10 | 9  | 8  |
| RESERVED                     |    |    |    | HSM_DMTA_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                         |    |    |    | R/W                          |    |    |    |
| 0h                           |    |    |    | 0h                           |    |    |    |
| 7                            | 6  | 5  | 4  | 3                            | 2  | 1  | 0  |
| HSM_DMTA_CLK_DIV_VAL_CLKDIVR |    |    |    |                              |    |    |    |
| R/W                          |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |

**Table 2-3111. MSS\_RCM\_HSM\_DMTA\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                                                                                                                                                                                                                      |
|-------|------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                     | NONE | 0h    | Reserved                                                                                                                                                                                                                                                         |
| 11:0  | HSM_DMTA_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value HSM DMTA selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

### 2.6.2.250 MSS\_RCM\_HSM\_DMTB\_CLK\_DIV\_VAL Register

#### 1 MSS\_RCM\_HSM\_DMTB\_CLK\_DIV\_VAL Register (Offset = 824h) [reset = 0h]

This Register is used to select the Divider value for respective clk.

Return to [Summary Table](#)

**Table 2-3112. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8824h       |

**Figure 2-1036. MSS\_RCM\_HSM\_DMTB\_CLK\_DIV\_VAL Name Register**

|                              |    |    |    |                              |    |    |    |
|------------------------------|----|----|----|------------------------------|----|----|----|
| 31                           | 30 | 29 | 28 | 27                           | 26 | 25 | 24 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 23                           | 22 | 21 | 20 | 19                           | 18 | 17 | 16 |
| RESERVED                     |    |    |    |                              |    |    |    |
| NONE                         |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |
| 15                           | 14 | 13 | 12 | 11                           | 10 | 9  | 8  |
| RESERVED                     |    |    |    | HSM_DMTB_CLK_DIV_VAL_CLKDIVR |    |    |    |
| NONE                         |    |    |    | R/W                          |    |    |    |
| 0h                           |    |    |    | 0h                           |    |    |    |
| 7                            | 6  | 5  | 4  | 3                            | 2  | 1  | 0  |
| HSM_DMTB_CLK_DIV_VAL_CLKDIVR |    |    |    |                              |    |    |    |
| R/W                          |    |    |    |                              |    |    |    |
| 0h                           |    |    |    |                              |    |    |    |

**Table 2-3114. MSS\_RCM\_HSM\_DMTB\_CLK\_DIV\_VAL Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description                                                                                                                                                                                                                                                      |
|-------|------------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED                     | NONE | 0h    | Reserved                                                                                                                                                                                                                                                         |
| 11:0  | HSM_DMTB_CLK_DIV_VAL_CLKDIVR | R/W  | 0h    | Divider value HSM DMTB selected clock. To set the divider value of [n+1] configure the register to value of '0xnnn'. Data should be loaded as multibit.<br>For example: if divider value of '0x9' is required then '0x888' should be configured to the register. |

## 2.6.2.251 MSS\_RCM\_HSM\_RTI\_CLK\_GATE Register

### 1 MSS\_RCM\_HSM\_RTI\_CLK\_GATE Register (Offset = 828h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-3115. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8828h       |

**Figure 2-1037. MSS\_RCM\_HSM\_RTI\_CLK\_GATE Name Register**

|          |    |    |    |    |                        |    |    |
|----------|----|----|----|----|------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                     | 25 | 24 |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                     | 17 | 16 |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                     | 9  | 8  |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                      | 1  | 0  |
| RESERVED |    |    |    |    | HSM_RTI_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                    |    |    |
| 0h       |    |    |    |    | 0h                     |    |    |

**Table 2-3117. MSS\_RCM\_HSM\_RTI\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                |
|------|------------------------|------|-------|--------------------------------------------|
| 31:3 | RESERVED               | NONE | 0h    | Reserved                                   |
| 2:0  | HSM_RTI_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for HSM RTI |

## 2.6.2.252 MSS\_RCM\_HSM\_WDT\_CLK\_GATE Register

### 1 MSS\_RCM\_HSM\_WDT\_CLK\_GATE Register (Offset = 82Ch) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-3118. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 882Ch       |

**Figure 2-1038. MSS\_RCM\_HSM\_WDT\_CLK\_GATE Name Register**

|          |    |    |    |                        |    |    |    |
|----------|----|----|----|------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                     | 26 | 25 | 24 |
| RESERVED |    |    |    |                        |    |    |    |
| NONE     |    |    |    |                        |    |    |    |
| 0h       |    |    |    |                        |    |    |    |
| 23       | 22 | 21 | 20 | 19                     | 18 | 17 | 16 |
| RESERVED |    |    |    |                        |    |    |    |
| NONE     |    |    |    |                        |    |    |    |
| 0h       |    |    |    |                        |    |    |    |
| 15       | 14 | 13 | 12 | 11                     | 10 | 9  | 8  |
| RESERVED |    |    |    |                        |    |    |    |
| NONE     |    |    |    |                        |    |    |    |
| 0h       |    |    |    |                        |    |    |    |
| 7        | 6  | 5  | 4  | 3                      | 2  | 1  | 0  |
| RESERVED |    |    |    | HSM_WDT_CLK_GATE_GATED |    |    |    |
| NONE     |    |    |    | R/W                    |    |    |    |
| 0h       |    |    |    | 0h                     |    |    |    |

**Table 2-3120. MSS\_RCM\_HSM\_WDT\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                |
|------|------------------------|------|-------|--------------------------------------------|
| 31:3 | RESERVED               | NONE | 0h    | Reserved                                   |
| 2:0  | HSM_WDT_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for HSM WDT |

### 2.6.2.253 MSS\_RCM\_HSM\_RTC\_CLK\_GATE Register

#### 1 MSS\_RCM\_HSM\_RTC\_CLK\_GATE Register (Offset = 830h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-3121. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8830h       |

**Figure 2-1039. MSS\_RCM\_HSM\_RTC\_CLK\_GATE Name Register**

|          |    |    |    |    |                        |    |    |
|----------|----|----|----|----|------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                     | 25 | 24 |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                     | 17 | 16 |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                     | 9  | 8  |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                      | 1  | 0  |
| RESERVED |    |    |    |    | HSM_RTC_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                    |    |    |
| 0h       |    |    |    |    | 0h                     |    |    |

**Table 2-3123. MSS\_RCM\_HSM\_RTC\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                |
|------|------------------------|------|-------|--------------------------------------------|
| 31:3 | RESERVED               | NONE | 0h    | Reserved                                   |
| 2:0  | HSM_RTC_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for HSM RTC |

### 2.6.2.254 MSS\_RCM\_HSM\_DMTA\_CLK\_GATE Register

#### 1 MSS\_RCM\_HSM\_DMTA\_CLK\_GATE Register (Offset = 834h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-3124. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8834h       |

**Figure 2-1040. MSS\_RCM\_HSM\_DMTA\_CLK\_GATE Name Register**

|          |    |    |    |    |                         |    |    |
|----------|----|----|----|----|-------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                      | 25 | 24 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                      | 17 | 16 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                      | 9  | 8  |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                       | 1  | 0  |
| RESERVED |    |    |    |    | HSM_DMTA_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                     |    |    |
| 0h       |    |    |    |    | 0h                      |    |    |

**Table 2-3126. MSS\_RCM\_HSM\_DMTA\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                 |
|------|-------------------------|------|-------|---------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                    |
| 2:0  | HSM_DMTA_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for HSM DMTA |

## 2.6.2.255 MSS\_RCM\_HSM\_DMTB\_CLK\_GATE Register

### 1 MSS\_RCM\_HSM\_DMTB\_CLK\_GATE Register (Offset = 838h) [reset = 0h]

This Register is used to enable clk gating for the respective clk.

Return to [Summary Table](#)

**Table 2-3127. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8838h       |

**Figure 2-1041. MSS\_RCM\_HSM\_DMTB\_CLK\_GATE Name Register**

|          |    |    |    |    |                         |    |    |
|----------|----|----|----|----|-------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                      | 25 | 24 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                      | 17 | 16 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                      | 9  | 8  |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                       | 1  | 0  |
| RESERVED |    |    |    |    | HSM_DMTB_CLK_GATE_GATED |    |    |
| NONE     |    |    |    |    | R/W                     |    |    |
| 0h       |    |    |    |    | 0h                      |    |    |

**Table 2-3129. MSS\_RCM\_HSM\_DMTB\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                 |
|------|-------------------------|------|-------|---------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                    |
| 2:0  | HSM_DMTB_CLK_GATE_GATED | R/W  | 0h    | Writing 3'b111 will gate clock for HSM DMTB |

## 2.6.2.256 MSS\_RCM\_HSM\_RTI\_CLK\_STATUS Register

### 1 MSS\_RCM\_HSM\_RTI\_CLK\_STATUS Register (Offset = 83Ch) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-3130. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 883Ch       |

**Figure 2-1042. MSS\_RCM\_HSM\_RTI\_CLK\_STATUS Name Register**

|                                |    |    |    |    |    |    |    |
|--------------------------------|----|----|----|----|----|----|----|
| 31                             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                       |    |    |    |    |    |    |    |
| NONE                           |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |
| 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                       |    |    |    |    |    |    |    |
| NONE                           |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |
| 15                             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HSM_RTI_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                              |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |
| 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HSM_RTI_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                              |    |    |    |    |    |    |    |
| 1h                             |    |    |    |    |    |    |    |

**Table 2-3132. MSS\_RCM\_HSM\_RTI\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                            |
|-------|--------------------------------|------|-------|----------------------------------------------------------------------------------------|
| 31:16 | RESERVED                       | NONE | 0h    | Reserved                                                                               |
| 15:8  | HSM_RTI_CLK_STATUS_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for HSM_RTI                             |
| 7:0   | HSM_RTI_CLK_STATUS_CLKINUSE    | R    | 1h    | Status shows the source clock slected for HSM_RTI based on one hot encoding technique. |



### 2.6.2.257 MSS\_RCM\_HSM\_WDT\_CLK\_STATUS Register

#### 1 MSS\_RCM\_HSM\_WDT\_CLK\_STATUS Register (Offset = 840h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-3133. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8840h       |

**Figure 2-1043. MSS\_RCM\_HSM\_WDT\_CLK\_STATUS Name Register**

|                                |    |    |    |    |    |    |    |
|--------------------------------|----|----|----|----|----|----|----|
| 31                             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                       |    |    |    |    |    |    |    |
| NONE                           |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |
| 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                       |    |    |    |    |    |    |    |
| NONE                           |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |
| 15                             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HSM_WDT_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                              |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |
| 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HSM_WDT_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                              |    |    |    |    |    |    |    |
| 1h                             |    |    |    |    |    |    |    |

**Table 2-3135. MSS\_RCM\_HSM\_WDT\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                            |
|-------|--------------------------------|------|-------|----------------------------------------------------------------------------------------|
| 31:16 | RESERVED                       | NONE | 0h    | Reserved                                                                               |
| 15:8  | HSM_WDT_CLK_STATUS_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for HSM_WDT                             |
| 7:0   | HSM_WDT_CLK_STATUS_CLKINUSE    | R    | 1h    | Status shows the source clock slected for HSM_WDT based on one hot encoding technique. |

## 2.6.2.258 MSS\_RCM\_HSM\_RTC\_CLK\_STATUS Register

### 1 MSS\_RCM\_HSM\_RTC\_CLK\_STATUS Register (Offset = 844h) [reset = 80h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-3136. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8844h       |

**Figure 2-1044. MSS\_RCM\_HSM\_RTC\_CLK\_STATUS Name Register**

|                                |    |    |    |    |    |    |    |
|--------------------------------|----|----|----|----|----|----|----|
| 31                             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                       |    |    |    |    |    |    |    |
| NONE                           |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |
| 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                       |    |    |    |    |    |    |    |
| NONE                           |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |
| 15                             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HSM_RTC_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                              |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |
| 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HSM_RTC_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                              |    |    |    |    |    |    |    |
| 80h                            |    |    |    |    |    |    |    |

**Table 2-3138. MSS\_RCM\_HSM\_RTC\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description                                                                            |
|-------|--------------------------------|------|-------|----------------------------------------------------------------------------------------|
| 31:16 | RESERVED                       | NONE | 0h    | Reserved                                                                               |
| 15:8  | HSM_RTC_CLK_STATUS_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for HSM_RTC                             |
| 7:0   | HSM_RTC_CLK_STATUS_CLKINUSE    | R    | 80h   | Status shows the source clock slected for HSM_RTC based on one hot encoding technique. |

## 2.6.2.259 MSS\_RCM\_HSM\_DMTA\_CLK\_STATUS Register

### 1 MSS\_RCM\_HSM\_DMTA\_CLK\_STATUS Register (Offset = 848h) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-3139. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 8848h       |

**Figure 2-1045. MSS\_RCM\_HSM\_DMTA\_CLK\_STATUS Name Register**

|                                 |    |    |    |    |    |    |    |
|---------------------------------|----|----|----|----|----|----|----|
| 31                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 23                              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 15                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HSM_DMTA_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 7                               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HSM_DMTA_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 1h                              |    |    |    |    |    |    |    |

**Table 2-3141. MSS\_RCM\_HSM\_DMTA\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                                             |
|-------|-------------------------------------|------|-------|-----------------------------------------------------------------------------------------|
| 31:16 | RESERVED                            | NONE | 0h    | Reserved                                                                                |
| 15:8  | HSM_DMTA_CLK_STATU<br>S_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for HSM_DMTA                             |
| 7:0   | HSM_DMTA_CLK_STATU<br>S_CLKINUSE    | R    | 1h    | Status shows the source clock slected for HSM_DMTA based on one hot encoding technique. |

### 2.6.2.260 MSS\_RCM\_HSM\_DMTB\_CLK\_STATUS Register

#### 1 MSS\_RCM\_HSM\_DMTB\_CLK\_STATUS Register (Offset = 84Ch) [reset = 1h]

Clock source selection and Divider Value of respective clock.

Return to [Summary Table](#)

**Table 2-3142. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 884Ch       |

**Figure 2-1046. MSS\_RCM\_HSM\_DMTB\_CLK\_STATUS Name Register**

|                                 |    |    |    |    |    |    |    |
|---------------------------------|----|----|----|----|----|----|----|
| 31                              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 23                              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                        |    |    |    |    |    |    |    |
| NONE                            |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 15                              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| HSM_DMTB_CLK_STATUS_CURRDIVIDER |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 0h                              |    |    |    |    |    |    |    |
| 7                               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HSM_DMTB_CLK_STATUS_CLKINUSE    |    |    |    |    |    |    |    |
| R                               |    |    |    |    |    |    |    |
| 1h                              |    |    |    |    |    |    |    |

**Table 2-3144. MSS\_RCM\_HSM\_DMTB\_CLK\_STATUS Register Field Descriptions**

| Bit   | Field                               | Type | Reset | Description                                                                             |
|-------|-------------------------------------|------|-------|-----------------------------------------------------------------------------------------|
| 31:16 | RESERVED                            | NONE | 0h    | Reserved                                                                                |
| 15:8  | HSM_DMTB_CLK_STATU<br>S_CURRDIVIDER | R    | 0h    | Status shows the current divider value choosen for HSM_DMTB                             |
| 7:0   | HSM_DMTB_CLK_STATU<br>S_CLKINUSE    | R    | 1h    | Status shows the source clock slected for HSM_DMTB based on one hot encoding technique. |

## 2.6.2.261 MSS\_RCM\_LOCK0\_KICK0 Register

### 1 MSS\_RCM\_LOCK0\_KICK0 Register (Offset = 1008h) [reset = 0h]

- KICK0 component.

Return to [Summary Table](#)

**Table 2-3145. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 9008h       |

**Figure 2-1047. MSS\_RCM\_LOCK0\_KICK0 Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| LOCK0_KICK0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LOCK0_KICK0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| LOCK0_KICK0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LOCK0_KICK0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 2-3147. MSS\_RCM\_LOCK0\_KICK0 Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description       |
|------|-------------|------|-------|-------------------|
| 31:0 | LOCK0_KICK0 | R/W  | 0h    | - KICK0 component |

### 2.6.2.262 MSS\_RCM\_LOCK0\_KICK1 Register

#### 1 MSS\_RCM\_LOCK0\_KICK1 Register (Offset = 100Ch) [reset = 0h]

- KICK1 component.

Return to [Summary Table](#)

**Table 2-3148. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 900Ch       |

**Figure 2-1048. MSS\_RCM\_LOCK0\_KICK1 Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| LOCK0_KICK1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LOCK0_KICK1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| LOCK0_KICK1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LOCK0_KICK1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 2-3150. MSS\_RCM\_LOCK0\_KICK1 Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description       |
|------|-------------|------|-------|-------------------|
| 31:0 | LOCK0_KICK1 | R/W  | 0h    | - KICK1 component |

### 2.6.2.263 MSS\_RCM\_INTR\_RAW\_STATUS Register

#### 1 MSS\_RCM\_INTR\_RAW\_STATUS Register (Offset = 1010h) [reset = 0h]

Interrupt Raw Status/Set Register.

Return to [Summary Table](#)

**Table 2-3151. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 9010h       |

**Figure 2-1049. MSS\_RCM\_INTR\_RAW\_STATUS Name Register**

|          |    |    |    |           |          |          |          |
|----------|----|----|----|-----------|----------|----------|----------|
| 31       | 30 | 29 | 28 | 27        | 26       | 25       | 24       |
| RESERVED |    |    |    |           |          |          |          |
| NONE     |    |    |    |           |          |          |          |
| 0h       |    |    |    |           |          |          |          |
| 23       | 22 | 21 | 20 | 19        | 18       | 17       | 16       |
| RESERVED |    |    |    |           |          |          |          |
| NONE     |    |    |    |           |          |          |          |
| 0h       |    |    |    |           |          |          |          |
| 15       | 14 | 13 | 12 | 11        | 10       | 9        | 8        |
| RESERVED |    |    |    |           |          |          |          |
| NONE     |    |    |    |           |          |          |          |
| 0h       |    |    |    |           |          |          |          |
| 7        | 6  | 5  | 4  | 3         | 2        | 1        | 0        |
| RESERVED |    |    |    | PROXY_ERR | KICK_ERR | ADDR_ERR | PROT_ERR |
| NONE     |    |    |    | R/W1TS    | R/W1TS   | R/W1TS   | R/W1TS   |
| 0h       |    |    |    | 0h        | 0h       | 0h       | 0h       |

**Table 2-3153. MSS\_RCM\_INTR\_RAW\_STATUS Register Field Descriptions**

| Bit  | Field     | Type   | Reset | Description                                                                                                |
|------|-----------|--------|-------|------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED  | NONE   | 0h    | Reserved                                                                                                   |
| 3    | PROXY_ERR | R/W1TS | 0h    | Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. |
| 2    | KICK_ERR  | R/W1TS | 0h    | Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.   |
| 1    | ADDR_ERR  | R/W1TS | 0h    | Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.    |
| 0    | PROT_ERR  | R/W1TS | 0h    | Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.    |

## 2.6.2.264 MSS\_RCM\_INTR\_ENABLED\_STATUS\_CLEAR Register

### 1 MSS\_RCM\_INTR\_ENABLED\_STATUS\_CLEAR Register (Offset = 1014h) [reset = 0h]

Interrupt Enabled Status/Clear register.

Return to [Summary Table](#)

**Table 2-3154. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 9014h       |

**Figure 2-1050. MSS\_RCM\_INTR\_ENABLED\_STATUS\_CLEAR Name Register**

|          |    |    |    |                   |                  |                  |                  |
|----------|----|----|----|-------------------|------------------|------------------|------------------|
| 31       | 30 | 29 | 28 | 27                | 26               | 25               | 24               |
| RESERVED |    |    |    |                   |                  |                  |                  |
| NONE     |    |    |    |                   |                  |                  |                  |
| 0h       |    |    |    |                   |                  |                  |                  |
| 23       | 22 | 21 | 20 | 19                | 18               | 17               | 16               |
| RESERVED |    |    |    |                   |                  |                  |                  |
| NONE     |    |    |    |                   |                  |                  |                  |
| 0h       |    |    |    |                   |                  |                  |                  |
| 15       | 14 | 13 | 12 | 11                | 10               | 9                | 8                |
| RESERVED |    |    |    |                   |                  |                  |                  |
| NONE     |    |    |    |                   |                  |                  |                  |
| 0h       |    |    |    |                   |                  |                  |                  |
| 7        | 6  | 5  | 4  | 3                 | 2                | 1                | 0                |
| RESERVED |    |    |    | ENABLED_PROXY_ERR | ENABLED_KICK_ERR | ENABLED_ADDR_ERR | ENABLED_PROT_ERR |
| NONE     |    |    |    | R/W1TC            | R/W1TC           | R/W1TC           | R/W1TC           |
| 0h       |    |    |    | 0h                | 0h               | 0h               | 0h               |

**Table 2-3156. MSS\_RCM\_INTR\_ENABLED\_STATUS\_CLEAR Register Field Descriptions**

| Bit  | Field             | Type   | Reset | Description                                                                                                      |
|------|-------------------|--------|-------|------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED          | NONE   | 0h    | Reserved                                                                                                         |
| 3    | ENABLED_PROXY_ERR | R/W1TC | 0h    | Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. |
| 2    | ENABLED_KICK_ERR  | R/W1TC | 0h    | Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.   |
| 1    | ENABLED_ADDR_ERR  | R/W1TC | 0h    | Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.    |
| 0    | ENABLED_PROT_ERR  | R/W1TC | 0h    | Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.    |



## 2.6.2.265 MSS\_RCM\_INTR\_ENABLE Register

### 1 MSS\_RCM\_INTR\_ENABLE Register (Offset = 1018h) [reset = 0h]

Interrupt Enable register.

Return to [Summary Table](#)

**Table 2-3157. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 9018h       |

**Figure 2-1051. MSS\_RCM\_INTR\_ENABLE Name Register**

|          |    |    |    |              |             |             |             |
|----------|----|----|----|--------------|-------------|-------------|-------------|
| 31       | 30 | 29 | 28 | 27           | 26          | 25          | 24          |
| RESERVED |    |    |    |              |             |             |             |
| NONE     |    |    |    |              |             |             |             |
| 0h       |    |    |    |              |             |             |             |
| 23       | 22 | 21 | 20 | 19           | 18          | 17          | 16          |
| RESERVED |    |    |    |              |             |             |             |
| NONE     |    |    |    |              |             |             |             |
| 0h       |    |    |    |              |             |             |             |
| 15       | 14 | 13 | 12 | 11           | 10          | 9           | 8           |
| RESERVED |    |    |    |              |             |             |             |
| NONE     |    |    |    |              |             |             |             |
| 0h       |    |    |    |              |             |             |             |
| 7        | 6  | 5  | 4  | 3            | 2           | 1           | 0           |
| RESERVED |    |    |    | PROXY_ERR_EN | KICK_ERR_EN | ADDR_ERR_EN | PROT_ERR_EN |
| NONE     |    |    |    | R/W1TS       | R/W1TS      | R/W1TS      | R/W1TS      |
| 0h       |    |    |    | 0h           | 0h          | 0h          | 0h          |

**Table 2-3159. MSS\_RCM\_INTR\_ENABLE Register Field Descriptions**

| Bit  | Field        | Type   | Reset | Description                                                                                   |
|------|--------------|--------|-------|-----------------------------------------------------------------------------------------------|
| 31:4 | RESERVED     | NONE   | 0h    | Reserved                                                                                      |
| 3    | PROXY_ERR_EN | R/W1TS | 0h    | Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. |
| 2    | KICK_ERR_EN  | R/W1TS | 0h    | Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.   |
| 1    | ADDR_ERR_EN  | R/W1TS | 0h    | Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.    |
| 0    | PROT_ERR_EN  | R/W1TS | 0h    | Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.    |

## 2.6.2.266 MSS\_RCM\_INTR\_ENABLE\_CLEAR Register

### 1 MSS\_RCM\_INTR\_ENABLE\_CLEAR Register (Offset = 101Ch) [reset = 0h]

Interrupt Enable Clear register.

Return to [Summary Table](#)

**Table 2-3160. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 901Ch       |

**Figure 2-1052. MSS\_RCM\_INTR\_ENABLE\_CLEAR Name Register**

|          |    |    |    |                  |                 |                 |                 |
|----------|----|----|----|------------------|-----------------|-----------------|-----------------|
| 31       | 30 | 29 | 28 | 27               | 26              | 25              | 24              |
| RESERVED |    |    |    |                  |                 |                 |                 |
| NONE     |    |    |    |                  |                 |                 |                 |
| 0h       |    |    |    |                  |                 |                 |                 |
| 23       | 22 | 21 | 20 | 19               | 18              | 17              | 16              |
| RESERVED |    |    |    |                  |                 |                 |                 |
| NONE     |    |    |    |                  |                 |                 |                 |
| 0h       |    |    |    |                  |                 |                 |                 |
| 15       | 14 | 13 | 12 | 11               | 10              | 9               | 8               |
| RESERVED |    |    |    |                  |                 |                 |                 |
| NONE     |    |    |    |                  |                 |                 |                 |
| 0h       |    |    |    |                  |                 |                 |                 |
| 7        | 6  | 5  | 4  | 3                | 2               | 1               | 0               |
| RESERVED |    |    |    | PROXY_ERR_EN_CLR | KICK_ERR_EN_CLR | ADDR_ERR_EN_CLR | PROT_ERR_EN_CLR |
| NONE     |    |    |    | R/W1TC           | R/W1TC          | R/W1TC          | R/W1TC          |
| 0h       |    |    |    | 0h               | 0h              | 0h              | 0h              |

**Table 2-3162. MSS\_RCM\_INTR\_ENABLE\_CLEAR Register Field Descriptions**

| Bit  | Field            | Type   | Reset | Description                                                                                           |
|------|------------------|--------|-------|-------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED         | NONE   | 0h    | Reserved                                                                                              |
| 3    | PROXY_ERR_EN_CLR | R/W1TC | 0h    | Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. |
| 2    | KICK_ERR_EN_CLR  | R/W1TC | 0h    | Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.   |
| 1    | ADDR_ERR_EN_CLR  | R/W1TC | 0h    | Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.    |
| 0    | PROT_ERR_EN_CLR  | R/W1TC | 0h    | Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.    |

## 2.6.2.267 MSS\_RCM\_EOI Register

### 1 MSS\_RCM\_EOI Register (Offset = 1020h) [reset = 0h]

EOI register.

Return to [Summary Table](#)

**Table 2-3163. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 9020h       |

**Figure 2-1053. MSS\_RCM\_EOI Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| EOI_VECTOR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 2-3165. MSS\_RCM\_EOI Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                 |
|------|------------|------|-------|-----------------------------------------------------------------------------|
| 31:8 | RESERVED   | NONE | 0h    | Reserved                                                                    |
| 7:0  | EOI_VECTOR | R/W  | 0h    | EOI vector value. Write this with interrupt distribution value in the chip. |

## 2.6.2.268 MSS\_RCM\_FAULT\_ADDRESS Register

### 1 MSS\_RCM\_FAULT\_ADDRESS Register (Offset = 1024h) [reset = 0h]

Fault Address register.

Return to [Summary Table](#)

**Table 2-3166. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 9024h       |

**Figure 2-1054. MSS\_RCM\_FAULT\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 2-3168. MSS\_RCM\_FAULT\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description    |
|------|------------|------|-------|----------------|
| 31:0 | FAULT_ADDR | R    | 0h    | Fault Address. |

## 2.6.2.269 MSS\_RCM\_FAULT\_TYPE\_STATUS Register

### 1 MSS\_RCM\_FAULT\_TYPE\_STATUS Register (Offset = 1028h) [reset = 0h]

Fault Type Status register.

Return to [Summary Table](#)

**Table 2-3169. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 9028h       |

**Figure 2-1055. MSS\_RCM\_FAULT\_TYPE\_STATUS Name Register**

|          |          |            |    |    |    |    |    |
|----------|----------|------------|----|----|----|----|----|
| 31       | 30       | 29         | 28 | 27 | 26 | 25 | 24 |
| RESERVED |          |            |    |    |    |    |    |
| NONE     |          |            |    |    |    |    |    |
| 0h       |          |            |    |    |    |    |    |
| 23       | 22       | 21         | 20 | 19 | 18 | 17 | 16 |
| RESERVED |          |            |    |    |    |    |    |
| NONE     |          |            |    |    |    |    |    |
| 0h       |          |            |    |    |    |    |    |
| 15       | 14       | 13         | 12 | 11 | 10 | 9  | 8  |
| RESERVED |          |            |    |    |    |    |    |
| NONE     |          |            |    |    |    |    |    |
| 0h       |          |            |    |    |    |    |    |
| 7        | 6        | 5          | 4  | 3  | 2  | 1  | 0  |
| RESERVED | FAULT_NS | FAULT_TYPE |    |    |    |    |    |
| NONE     | R        | R          |    |    |    |    |    |
| 0h       | 0h       | 0h         |    |    |    |    |    |

**Table 2-3171. MSS\_RCM\_FAULT\_TYPE\_STATUS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                         |
|------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                            |
| 6    | FAULT_NS   | R    | 0h    | Non-secure access.                                                                                                                                                                                                                                                                                                                                                                                  |
| 5:0  | FAULT_TYPE | R    | 0h    | Fault Type<br>10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1<br>01_0000 = Supervisor write fault - priv = 1 dir = 0<br>00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1<br>00_0100 = User read fault - priv = 0 dir = 1 dtype = 1<br>00_0010 = User write fault - priv = 0 dir = 0<br>00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1<br>00_0000 = No fault |

## 2.6.2.270 MSS\_RCM\_FAULT\_ATTR\_STATUS Register

### 1 MSS\_RCM\_FAULT\_ATTR\_STATUS Register (Offset = 102Ch) [reset = 0h]

Fault Attribute Status register.

Return to [Summary Table](#)

**Table 2-3172. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 902Ch       |

**Figure 2-1056. MSS\_RCM\_FAULT\_ATTR\_STATUS Name Register**

|               |    |    |    |               |    |    |    |
|---------------|----|----|----|---------------|----|----|----|
| 31            | 30 | 29 | 28 | 27            | 26 | 25 | 24 |
| FAULT_XID     |    |    |    |               |    |    |    |
| R             |    |    |    |               |    |    |    |
| 0h            |    |    |    |               |    |    |    |
| 23            | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
| FAULT_XID     |    |    |    | FAULT_ROUTEID |    |    |    |
| R             |    |    |    | R             |    |    |    |
| 0h            |    |    |    | 0h            |    |    |    |
| 15            | 14 | 13 | 12 | 11            | 10 | 9  | 8  |
| FAULT_ROUTEID |    |    |    |               |    |    |    |
| R             |    |    |    |               |    |    |    |
| 0h            |    |    |    |               |    |    |    |
| 7             | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| FAULT_PRIVID  |    |    |    |               |    |    |    |
| R             |    |    |    |               |    |    |    |
| 0h            |    |    |    |               |    |    |    |

**Table 2-3174. MSS\_RCM\_FAULT\_ATTR\_STATUS Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description   |
|-------|---------------|------|-------|---------------|
| 31:20 | FAULT_XID     | R    | 0h    | XID.          |
| 19:8  | FAULT_ROUTEID | R    | 0h    | Route ID.     |
| 7:0   | FAULT_PRIVID  | R    | 0h    | Privilege ID. |

## 2.6.2.271 MSS\_RCM\_FAULT\_CLEAR Register

### 1 MSS\_RCM\_FAULT\_CLEAR Register (Offset = 1030h) [reset = 0h]

Fault Clear register.

Return to [Summary Table](#)

**Table 2-3175. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_RCM       | 5320 9030h       |

**Figure 2-1057. MSS\_RCM\_FAULT\_CLEAR Name Register**

|          |    |    |    |    |    |    |           |
|----------|----|----|----|----|----|----|-----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24        |
| RESERVED |    |    |    |    |    |    |           |
| NONE     |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16        |
| RESERVED |    |    |    |    |    |    |           |
| NONE     |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8         |
| RESERVED |    |    |    |    |    |    |           |
| NONE     |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0         |
| RESERVED |    |    |    |    |    |    | FAULT_CLR |
| NONE     |    |    |    |    |    |    | W         |
| 0h       |    |    |    |    |    |    | 0h        |

**Table 2-3177. MSS\_RCM\_FAULT\_CLEAR Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                   |
|------|-----------|------|-------|-------------------------------------------------------------------------------|
| 31:1 | RESERVED  | NONE | 0h    | Reserved                                                                      |
| 0    | FAULT_CLR | W    | 0h    | Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. |

## 2.7 CONTROLSS\_GLOBAL\_CTRL

### CONTROLSS\_GLOBAL\_CTRL

#### 2.7.1 CONTROLSS\_GLOBAL\_CTRL Summaries

#### CONTROLSS\_GLOBAL\_CTRL Summaries

**Table 2-3178. CONTROLSS\_CTRL Registers, Base Address=502F 0000h, Length=4096**

| Offset | Length | Register Name                                       | CONTROLSS_GLOBAL_CTRL Physical Address |
|--------|--------|-----------------------------------------------------|----------------------------------------|
| 4h     | 32     | <a href="#">CONTROLSS_CTRL_EPWM_STATICXBAR_SEL0</a> | 502F 0004h                             |
| 8h     | 32     | <a href="#">CONTROLSS_CTRL_EPWM_STATICXBAR_SEL1</a> | 502F 0008h                             |
| 10h    | 32     | <a href="#">CONTROLSS_CTRL_EPWM_CLKSYNC</a>         | 502F 0010h                             |
| 18h    | 32     | <a href="#">CONTROLSS_CTRL_SDFM1_CLK0_SEL</a>       | 502F 0018h                             |
| 20h    | 32     | <a href="#">CONTROLSS_CTRL_EMUSTOPN_MASK</a>        | 502F 0020h                             |
| 28h    | 32     | <a href="#">CONTROLSS_CTRL_CLB_AQ_EN0</a>           | 502F 0028h                             |
| 30h    | 32     | <a href="#">CONTROLSS_CTRL_CLB_AQ_EN1</a>           | 502F 0030h                             |
| 38h    | 32     | <a href="#">CONTROLSS_CTRL_CLB_DB_EN0</a>           | 502F 0038h                             |
| 40h    | 32     | <a href="#">CONTROLSS_CTRL_CLB_DB_EN1</a>           | 502F 0040h                             |
| 100h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM0_CLK_GATE</a>       | 502F 0100h                             |
| 104h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM1_CLK_GATE</a>       | 502F 0104h                             |
| 108h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM2_CLK_GATE</a>       | 502F 0108h                             |
| 10Ch   | 32     | <a href="#">CONTROLSS_CTRL_EPWM3_CLK_GATE</a>       | 502F 010Ch                             |
| 110h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM4_CLK_GATE</a>       | 502F 0110h                             |
| 114h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM5_CLK_GATE</a>       | 502F 0114h                             |
| 118h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM6_CLK_GATE</a>       | 502F 0118h                             |
| 11Ch   | 32     | <a href="#">CONTROLSS_CTRL_EPWM7_CLK_GATE</a>       | 502F 011Ch                             |
| 120h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM8_CLK_GATE</a>       | 502F 0120h                             |
| 124h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM9_CLK_GATE</a>       | 502F 0124h                             |
| 128h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM10_CLK_GATE</a>      | 502F 0128h                             |
| 12Ch   | 32     | <a href="#">CONTROLSS_CTRL_EPWM11_CLK_GATE</a>      | 502F 012Ch                             |
| 130h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM12_CLK_GATE</a>      | 502F 0130h                             |
| 134h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM13_CLK_GATE</a>      | 502F 0134h                             |
| 138h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM14_CLK_GATE</a>      | 502F 0138h                             |
| 13Ch   | 32     | <a href="#">CONTROLSS_CTRL_EPWM15_CLK_GATE</a>      | 502F 013Ch                             |
| 140h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM16_CLK_GATE</a>      | 502F 0140h                             |
| 144h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM17_CLK_GATE</a>      | 502F 0144h                             |
| 148h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM18_CLK_GATE</a>      | 502F 0148h                             |
| 14Ch   | 32     | <a href="#">CONTROLSS_CTRL_EPWM19_CLK_GATE</a>      | 502F 014Ch                             |
| 150h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM20_CLK_GATE</a>      | 502F 0150h                             |
| 154h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM21_CLK_GATE</a>      | 502F 0154h                             |
| 158h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM22_CLK_GATE</a>      | 502F 0158h                             |
| 15Ch   | 32     | <a href="#">CONTROLSS_CTRL_EPWM23_CLK_GATE</a>      | 502F 015Ch                             |
| 160h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM24_CLK_GATE</a>      | 502F 0160h                             |
| 164h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM25_CLK_GATE</a>      | 502F 0164h                             |
| 168h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM26_CLK_GATE</a>      | 502F 0168h                             |
| 16Ch   | 32     | <a href="#">CONTROLSS_CTRL_EPWM27_CLK_GATE</a>      | 502F 016Ch                             |



**Table 2-3178. CONTROLSS\_CTRL Registers, Base Address=502F 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                                   | CONTROLSS_GLOBAL_CTRL Physical Address |
|--------|--------|-------------------------------------------------|----------------------------------------|
| 170h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM28_CLK_GATE</a>  | 502F 0170h                             |
| 174h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM29_CLK_GATE</a>  | 502F 0174h                             |
| 178h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM30_CLK_GATE</a>  | 502F 0178h                             |
| 17Ch   | 32     | <a href="#">CONTROLSS_CTRL_EPWM31_CLK_GATE</a>  | 502F 017Ch                             |
| 180h   | 32     | <a href="#">CONTROLSS_CTRL_FSI_TX0_CLK_GATE</a> | 502F 0180h                             |
| 184h   | 32     | <a href="#">CONTROLSS_CTRL_FSI_TX1_CLK_GATE</a> | 502F 0184h                             |
| 188h   | 32     | <a href="#">CONTROLSS_CTRL_FSI_TX2_CLK_GATE</a> | 502F 0188h                             |
| 18Ch   | 32     | <a href="#">CONTROLSS_CTRL_FSI_TX3_CLK_GATE</a> | 502F 018Ch                             |
| 190h   | 32     | <a href="#">CONTROLSS_CTRL_FSI_RX0_CLK_GATE</a> | 502F 0190h                             |
| 194h   | 32     | <a href="#">CONTROLSS_CTRL_FSI_RX1_CLK_GATE</a> | 502F 0194h                             |
| 198h   | 32     | <a href="#">CONTROLSS_CTRL_FSI_RX2_CLK_GATE</a> | 502F 0198h                             |
| 19Ch   | 32     | <a href="#">CONTROLSS_CTRL_FSI_RX3_CLK_GATE</a> | 502F 019Ch                             |
| 1A0h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA0_CLK_GATE</a> | 502F 01A0h                             |
| 1A4h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA1_CLK_GATE</a> | 502F 01A4h                             |
| 1A8h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA2_CLK_GATE</a> | 502F 01A8h                             |
| 1ACh   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA3_CLK_GATE</a> | 502F 01ACh                             |
| 1B0h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA4_CLK_GATE</a> | 502F 01B0h                             |
| 1B4h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA5_CLK_GATE</a> | 502F 01B4h                             |
| 1B8h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA6_CLK_GATE</a> | 502F 01B8h                             |
| 1BCh   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA7_CLK_GATE</a> | 502F 01BCh                             |
| 1C0h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA8_CLK_GATE</a> | 502F 01C0h                             |
| 1C4h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA9_CLK_GATE</a> | 502F 01C4h                             |
| 1D0h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB0_CLK_GATE</a> | 502F 01D0h                             |
| 1D4h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB1_CLK_GATE</a> | 502F 01D4h                             |
| 1D8h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB2_CLK_GATE</a> | 502F 01D8h                             |
| 1DCh   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB3_CLK_GATE</a> | 502F 01DCh                             |
| 1E0h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB4_CLK_GATE</a> | 502F 01E0h                             |
| 1E4h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB5_CLK_GATE</a> | 502F 01E4h                             |
| 1E8h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB6_CLK_GATE</a> | 502F 01E8h                             |
| 1ECh   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB7_CLK_GATE</a> | 502F 01ECh                             |
| 1F0h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB8_CLK_GATE</a> | 502F 01F0h                             |
| 1F4h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB9_CLK_GATE</a> | 502F 01F4h                             |
| 200h   | 32     | <a href="#">CONTROLSS_CTRL_ECAP0_CLK_GATE</a>   | 502F 0200h                             |
| 204h   | 32     | <a href="#">CONTROLSS_CTRL_ECAP1_CLK_GATE</a>   | 502F 0204h                             |
| 208h   | 32     | <a href="#">CONTROLSS_CTRL_ECAP2_CLK_GATE</a>   | 502F 0208h                             |
| 20Ch   | 32     | <a href="#">CONTROLSS_CTRL_ECAP3_CLK_GATE</a>   | 502F 020Ch                             |
| 210h   | 32     | <a href="#">CONTROLSS_CTRL_ECAP4_CLK_GATE</a>   | 502F 0210h                             |
| 214h   | 32     | <a href="#">CONTROLSS_CTRL_ECAP5_CLK_GATE</a>   | 502F 0214h                             |
| 218h   | 32     | <a href="#">CONTROLSS_CTRL_ECAP6_CLK_GATE</a>   | 502F 0218h                             |
| 21Ch   | 32     | <a href="#">CONTROLSS_CTRL_ECAP7_CLK_GATE</a>   | 502F 021Ch                             |
| 220h   | 32     | <a href="#">CONTROLSS_CTRL_ECAP8_CLK_GATE</a>   | 502F 0220h                             |
| 224h   | 32     | <a href="#">CONTROLSS_CTRL_ECAP9_CLK_GATE</a>   | 502F 0224h                             |
| 240h   | 32     | <a href="#">CONTROLSS_CTRL_EQEP0_CLK_GATE</a>   | 502F 0240h                             |
| 244h   | 32     | <a href="#">CONTROLSS_CTRL_EQEP1_CLK_GATE</a>   | 502F 0244h                             |

**Table 2-3178. CONTROLSS\_CTRL Registers, Base Address=502F 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                                       | CONTROLSS_GLOBAL_CTRL Physical Address |
|--------|--------|-----------------------------------------------------|----------------------------------------|
| 248h   | 32     | <a href="#">CONTROLSS_CTRL_EQEP2_CLK_GATE</a>       | 502F 0248h                             |
| 250h   | 32     | <a href="#">CONTROLSS_CTRL_SDFM0_CLK_GATE</a>       | 502F 0250h                             |
| 254h   | 32     | <a href="#">CONTROLSS_CTRL_SDFM1_CLK_GATE</a>       | 502F 0254h                             |
| 258h   | 32     | <a href="#">CONTROLSS_CTRL_DAC_CLK_GATE</a>         | 502F 0258h                             |
| 25Ch   | 32     | <a href="#">CONTROLSS_CTRL_ADC0_CLK_GATE</a>        | 502F 025Ch                             |
| 260h   | 32     | <a href="#">CONTROLSS_CTRL_ADC1_CLK_GATE</a>        | 502F 0260h                             |
| 264h   | 32     | <a href="#">CONTROLSS_CTRL_ADC2_CLK_GATE</a>        | 502F 0264h                             |
| 268h   | 32     | <a href="#">CONTROLSS_CTRL_ADC3_CLK_GATE</a>        | 502F 0268h                             |
| 26Ch   | 32     | <a href="#">CONTROLSS_CTRL_ADC4_CLK_GATE</a>        | 502F 026Ch                             |
| 270h   | 32     | <a href="#">CONTROLSS_CTRL_OTTO0_CLK_GATE</a>       | 502F 0270h                             |
| 274h   | 32     | <a href="#">CONTROLSS_CTRL_OTTO1_CLK_GATE</a>       | 502F 0274h                             |
| 278h   | 32     | <a href="#">CONTROLSS_CTRL_OTTO2_CLK_GATE</a>       | 502F 0278h                             |
| 27Ch   | 32     | <a href="#">CONTROLSS_CTRL_OTTO3_CLK_GATE</a>       | 502F 027Ch                             |
| 280h   | 32     | <a href="#">CONTROLSS_CTRL_SDFM0_PLL_CLK_GATE</a>   | 502F 0280h                             |
| 284h   | 32     | <a href="#">CONTROLSS_CTRL_SDFM1_PLL_CLK_GATE</a>   | 502F 0284h                             |
| 288h   | 32     | <a href="#">CONTROLSS_CTRL_FSI_TX0_PLL_CLK_GATE</a> | 502F 0288h                             |
| 28Ch   | 32     | <a href="#">CONTROLSS_CTRL_FSI_TX1_PLL_CLK_GATE</a> | 502F 028Ch                             |
| 290h   | 32     | <a href="#">CONTROLSS_CTRL_FSI_TX2_PLL_CLK_GATE</a> | 502F 0290h                             |
| 294h   | 32     | <a href="#">CONTROLSS_CTRL_FSI_TX3_PLL_CLK_GATE</a> | 502F 0294h                             |
| 300h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM0_RST</a>            | 502F 0300h                             |
| 304h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM1_RST</a>            | 502F 0304h                             |
| 308h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM2_RST</a>            | 502F 0308h                             |
| 30Ch   | 32     | <a href="#">CONTROLSS_CTRL_EPWM3_RST</a>            | 502F 030Ch                             |
| 310h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM4_RST</a>            | 502F 0310h                             |
| 314h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM5_RST</a>            | 502F 0314h                             |
| 318h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM6_RST</a>            | 502F 0318h                             |
| 31Ch   | 32     | <a href="#">CONTROLSS_CTRL_EPWM7_RST</a>            | 502F 031Ch                             |
| 320h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM8_RST</a>            | 502F 0320h                             |
| 324h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM9_RST</a>            | 502F 0324h                             |
| 328h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM10_RST</a>           | 502F 0328h                             |
| 32Ch   | 32     | <a href="#">CONTROLSS_CTRL_EPWM11_RST</a>           | 502F 032Ch                             |
| 330h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM12_RST</a>           | 502F 0330h                             |
| 334h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM13_RST</a>           | 502F 0334h                             |
| 338h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM14_RST</a>           | 502F 0338h                             |
| 33Ch   | 32     | <a href="#">CONTROLSS_CTRL_EPWM15_RST</a>           | 502F 033Ch                             |
| 340h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM16_RST</a>           | 502F 0340h                             |
| 344h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM17_RST</a>           | 502F 0344h                             |
| 348h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM18_RST</a>           | 502F 0348h                             |
| 34Ch   | 32     | <a href="#">CONTROLSS_CTRL_EPWM19_RST</a>           | 502F 034Ch                             |
| 350h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM20_RST</a>           | 502F 0350h                             |
| 354h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM21_RST</a>           | 502F 0354h                             |
| 358h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM22_RST</a>           | 502F 0358h                             |
| 35Ch   | 32     | <a href="#">CONTROLSS_CTRL_EPWM23_RST</a>           | 502F 035Ch                             |
| 360h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM24_RST</a>           | 502F 0360h                             |

**Table 2-3178. CONTROLSS\_CTRL Registers, Base Address=502F 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                              | CONTROLSS_GLOBAL_CTRL Physical Address |
|--------|--------|--------------------------------------------|----------------------------------------|
| 364h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM25_RST</a>  | 502F 0364h                             |
| 368h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM26_RST</a>  | 502F 0368h                             |
| 36Ch   | 32     | <a href="#">CONTROLSS_CTRL_EPWM27_RST</a>  | 502F 036Ch                             |
| 370h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM28_RST</a>  | 502F 0370h                             |
| 374h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM29_RST</a>  | 502F 0374h                             |
| 378h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM30_RST</a>  | 502F 0378h                             |
| 37Ch   | 32     | <a href="#">CONTROLSS_CTRL_EPWM31_RST</a>  | 502F 037Ch                             |
| 380h   | 32     | <a href="#">CONTROLSS_CTRL_FSI_TX0_RST</a> | 502F 0380h                             |
| 384h   | 32     | <a href="#">CONTROLSS_CTRL_FSI_TX1_RST</a> | 502F 0384h                             |
| 388h   | 32     | <a href="#">CONTROLSS_CTRL_FSI_TX2_RST</a> | 502F 0388h                             |
| 38Ch   | 32     | <a href="#">CONTROLSS_CTRL_FSI_TX3_RST</a> | 502F 038Ch                             |
| 390h   | 32     | <a href="#">CONTROLSS_CTRL_FSI_RX0_RST</a> | 502F 0390h                             |
| 394h   | 32     | <a href="#">CONTROLSS_CTRL_FSI_RX1_RST</a> | 502F 0394h                             |
| 398h   | 32     | <a href="#">CONTROLSS_CTRL_FSI_RX2_RST</a> | 502F 0398h                             |
| 39Ch   | 32     | <a href="#">CONTROLSS_CTRL_FSI_RX3_RST</a> | 502F 039Ch                             |
| 3A0h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA0_RST</a> | 502F 03A0h                             |
| 3A4h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA1_RST</a> | 502F 03A4h                             |
| 3A8h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA2_RST</a> | 502F 03A8h                             |
| 3ACh   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA3_RST</a> | 502F 03ACh                             |
| 3B0h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA4_RST</a> | 502F 03B0h                             |
| 3B4h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA5_RST</a> | 502F 03B4h                             |
| 3B8h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA6_RST</a> | 502F 03B8h                             |
| 3BCh   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA7_RST</a> | 502F 03BCh                             |
| 3C0h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA8_RST</a> | 502F 03C0h                             |
| 3C4h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA9_RST</a> | 502F 03C4h                             |
| 3D0h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB0_RST</a> | 502F 03D0h                             |
| 3D4h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB1_RST</a> | 502F 03D4h                             |
| 3D8h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB2_RST</a> | 502F 03D8h                             |
| 3DCh   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB3_RST</a> | 502F 03DCh                             |
| 3E0h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB4_RST</a> | 502F 03E0h                             |
| 3E4h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB5_RST</a> | 502F 03E4h                             |
| 3E8h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB6_RST</a> | 502F 03E8h                             |
| 3ECh   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB7_RST</a> | 502F 03ECh                             |
| 3F0h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB8_RST</a> | 502F 03F0h                             |
| 3F4h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB9_RST</a> | 502F 03F4h                             |
| 400h   | 32     | <a href="#">CONTROLSS_CTRL_ECAP0_RST</a>   | 502F 0400h                             |
| 404h   | 32     | <a href="#">CONTROLSS_CTRL_ECAP1_RST</a>   | 502F 0404h                             |
| 408h   | 32     | <a href="#">CONTROLSS_CTRL_ECAP2_RST</a>   | 502F 0408h                             |
| 40Ch   | 32     | <a href="#">CONTROLSS_CTRL_ECAP3_RST</a>   | 502F 040Ch                             |
| 410h   | 32     | <a href="#">CONTROLSS_CTRL_ECAP4_RST</a>   | 502F 0410h                             |
| 414h   | 32     | <a href="#">CONTROLSS_CTRL_ECAP5_RST</a>   | 502F 0414h                             |
| 418h   | 32     | <a href="#">CONTROLSS_CTRL_ECAP6_RST</a>   | 502F 0418h                             |
| 41Ch   | 32     | <a href="#">CONTROLSS_CTRL_ECAP7_RST</a>   | 502F 041Ch                             |
| 420h   | 32     | <a href="#">CONTROLSS_CTRL_ECAP8_RST</a>   | 502F 0420h                             |

**Table 2-3178. CONTROLSS\_CTRL Registers, Base Address=502F 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                                | CONTROLSS_GLOBAL_CTRL Physical Address |
|--------|--------|----------------------------------------------|----------------------------------------|
| 424h   | 32     | <a href="#">CONTROLSS_CTRL_ECAP9_RST</a>     | 502F 0424h                             |
| 440h   | 32     | <a href="#">CONTROLSS_CTRL_EQEP0_RST</a>     | 502F 0440h                             |
| 444h   | 32     | <a href="#">CONTROLSS_CTRL_EQEP1_RST</a>     | 502F 0444h                             |
| 448h   | 32     | <a href="#">CONTROLSS_CTRL_EQEP2_RST</a>     | 502F 0448h                             |
| 450h   | 32     | <a href="#">CONTROLSS_CTRL_SDFM0_RST</a>     | 502F 0450h                             |
| 454h   | 32     | <a href="#">CONTROLSS_CTRL_SDFM1_RST</a>     | 502F 0454h                             |
| 458h   | 32     | <a href="#">CONTROLSS_CTRL_DAC_RST</a>       | 502F 0458h                             |
| 45Ch   | 32     | <a href="#">CONTROLSS_CTRL_ADC0_RST</a>      | 502F 045Ch                             |
| 460h   | 32     | <a href="#">CONTROLSS_CTRL_ADC1_RST</a>      | 502F 0460h                             |
| 464h   | 32     | <a href="#">CONTROLSS_CTRL_ADC2_RST</a>      | 502F 0464h                             |
| 468h   | 32     | <a href="#">CONTROLSS_CTRL_ADC3_RST</a>      | 502F 0468h                             |
| 46Ch   | 32     | <a href="#">CONTROLSS_CTRL_ADC4_RST</a>      | 502F 046Ch                             |
| 470h   | 32     | <a href="#">CONTROLSS_CTRL_OTTO0_RST</a>     | 502F 0470h                             |
| 474h   | 32     | <a href="#">CONTROLSS_CTRL_OTTO1_RST</a>     | 502F 0474h                             |
| 478h   | 32     | <a href="#">CONTROLSS_CTRL_OTTO2_RST</a>     | 502F 0478h                             |
| 47Ch   | 32     | <a href="#">CONTROLSS_CTRL_OTTO3_RST</a>     | 502F 047Ch                             |
| 500h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM0_HALTEN</a>  | 502F 0500h                             |
| 504h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM1_HALTEN</a>  | 502F 0504h                             |
| 508h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM2_HALTEN</a>  | 502F 0508h                             |
| 50Ch   | 32     | <a href="#">CONTROLSS_CTRL_EPWM3_HALTEN</a>  | 502F 050Ch                             |
| 510h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM4_HALTEN</a>  | 502F 0510h                             |
| 514h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM5_HALTEN</a>  | 502F 0514h                             |
| 518h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM6_HALTEN</a>  | 502F 0518h                             |
| 51Ch   | 32     | <a href="#">CONTROLSS_CTRL_EPWM7_HALTEN</a>  | 502F 051Ch                             |
| 520h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM8_HALTEN</a>  | 502F 0520h                             |
| 524h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM9_HALTEN</a>  | 502F 0524h                             |
| 528h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM10_HALTEN</a> | 502F 0528h                             |
| 52Ch   | 32     | <a href="#">CONTROLSS_CTRL_EPWM11_HALTEN</a> | 502F 052Ch                             |
| 530h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM12_HALTEN</a> | 502F 0530h                             |
| 534h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM13_HALTEN</a> | 502F 0534h                             |
| 538h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM14_HALTEN</a> | 502F 0538h                             |
| 53Ch   | 32     | <a href="#">CONTROLSS_CTRL_EPWM15_HALTEN</a> | 502F 053Ch                             |
| 540h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM16_HALTEN</a> | 502F 0540h                             |
| 544h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM17_HALTEN</a> | 502F 0544h                             |
| 548h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM18_HALTEN</a> | 502F 0548h                             |
| 54Ch   | 32     | <a href="#">CONTROLSS_CTRL_EPWM19_HALTEN</a> | 502F 054Ch                             |
| 550h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM20_HALTEN</a> | 502F 0550h                             |
| 554h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM21_HALTEN</a> | 502F 0554h                             |
| 558h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM22_HALTEN</a> | 502F 0558h                             |
| 55Ch   | 32     | <a href="#">CONTROLSS_CTRL_EPWM23_HALTEN</a> | 502F 055Ch                             |
| 560h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM24_HALTEN</a> | 502F 0560h                             |
| 564h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM25_HALTEN</a> | 502F 0564h                             |
| 568h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM26_HALTEN</a> | 502F 0568h                             |
| 56Ch   | 32     | <a href="#">CONTROLSS_CTRL_EPWM27_HALTEN</a> | 502F 056Ch                             |

**Table 2-3178. CONTROLSS\_CTRL Registers, Base Address=502F 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                                            | CONTROLSS_GLOBAL_CTRL Physical Address |
|--------|--------|----------------------------------------------------------|----------------------------------------|
| 570h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM28_HALTEN</a>             | 502F 0570h                             |
| 574h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM29_HALTEN</a>             | 502F 0574h                             |
| 578h   | 32     | <a href="#">CONTROLSS_CTRL_EPWM30_HALTEN</a>             | 502F 0578h                             |
| 57Ch   | 32     | <a href="#">CONTROLSS_CTRL_EPWM31_HALTEN</a>             | 502F 057Ch                             |
| 580h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA0_HALTEN</a>            | 502F 0580h                             |
| 584h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA1_HALTEN</a>            | 502F 0584h                             |
| 588h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA2_HALTEN</a>            | 502F 0588h                             |
| 58Ch   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA3_HALTEN</a>            | 502F 058Ch                             |
| 590h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA4_HALTEN</a>            | 502F 0590h                             |
| 594h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA5_HALTEN</a>            | 502F 0594h                             |
| 598h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA6_HALTEN</a>            | 502F 0598h                             |
| 59Ch   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA7_HALTEN</a>            | 502F 059Ch                             |
| 5A0h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA8_HALTEN</a>            | 502F 05A0h                             |
| 5A4h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSA9_HALTEN</a>            | 502F 05A4h                             |
| 5A8h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB0_HALTEN</a>            | 502F 05A8h                             |
| 5ACh   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB1_HALTEN</a>            | 502F 05ACh                             |
| 5B0h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB2_HALTEN</a>            | 502F 05B0h                             |
| 5B4h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB3_HALTEN</a>            | 502F 05B4h                             |
| 5B8h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB4_HALTEN</a>            | 502F 05B8h                             |
| 5BCh   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB5_HALTEN</a>            | 502F 05BCh                             |
| 5C0h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB6_HALTEN</a>            | 502F 05C0h                             |
| 5C4h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB7_HALTEN</a>            | 502F 05C4h                             |
| 5C8h   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB8_HALTEN</a>            | 502F 05C8h                             |
| 5CCh   | 32     | <a href="#">CONTROLSS_CTRL_CMPSSB9_HALTEN</a>            | 502F 05CCh                             |
| 5D0h   | 32     | <a href="#">CONTROLSS_CTRL_ECAP0_HALTEN</a>              | 502F 05D0h                             |
| 5D4h   | 32     | <a href="#">CONTROLSS_CTRL_ECAP1_HALTEN</a>              | 502F 05D4h                             |
| 5D8h   | 32     | <a href="#">CONTROLSS_CTRL_ECAP2_HALTEN</a>              | 502F 05D8h                             |
| 5DCh   | 32     | <a href="#">CONTROLSS_CTRL_ECAP3_HALTEN</a>              | 502F 05DCh                             |
| 5E0h   | 32     | <a href="#">CONTROLSS_CTRL_ECAP4_HALTEN</a>              | 502F 05E0h                             |
| 5E4h   | 32     | <a href="#">CONTROLSS_CTRL_ECAP5_HALTEN</a>              | 502F 05E4h                             |
| 5E8h   | 32     | <a href="#">CONTROLSS_CTRL_ECAP6_HALTEN</a>              | 502F 05E8h                             |
| 5ECh   | 32     | <a href="#">CONTROLSS_CTRL_ECAP7_HALTEN</a>              | 502F 05ECh                             |
| 5F0h   | 32     | <a href="#">CONTROLSS_CTRL_ECAP8_HALTEN</a>              | 502F 05F0h                             |
| 5F4h   | 32     | <a href="#">CONTROLSS_CTRL_ECAP9_HALTEN</a>              | 502F 05F4h                             |
| 5F8h   | 32     | <a href="#">CONTROLSS_CTRL_EQEP0_HALTEN</a>              | 502F 05F8h                             |
| 5FCh   | 32     | <a href="#">CONTROLSS_CTRL_EQEP1_HALTEN</a>              | 502F 05FCh                             |
| 600h   | 32     | <a href="#">CONTROLSS_CTRL_EQEP2_HALTEN</a>              | 502F 0600h                             |
| 1008h  | 32     | <a href="#">CONTROLSS_CTRL_LOCK0_KICK0</a>               | 502F 1008h                             |
| 100Ch  | 32     | <a href="#">CONTROLSS_CTRL_LOCK0_KICK1</a>               | 502F 100Ch                             |
| 1010h  | 32     | <a href="#">CONTROLSS_CTRL_INTR_RAW_STATUS</a>           | 502F 1010h                             |
| 1014h  | 32     | <a href="#">CONTROLSS_CTRL_INTR_ENABLED_STATUS_CLEAR</a> | 502F 1014h                             |
| 1018h  | 32     | <a href="#">CONTROLSS_CTRL_INTR_ENABLE</a>               | 502F 1018h                             |
| 101Ch  | 32     | <a href="#">CONTROLSS_CTRL_INTR_ENABLE_CLEAR</a>         | 502F 101Ch                             |
| 1020h  | 32     | <a href="#">CONTROLSS_CTRL_EOI</a>                       | 502F 1020h                             |

**Table 2-3178. CONTROLSS\_CTRL Registers, Base Address=502F 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                                    | CONTROLSS_GLOBAL_CTRL Physical Address |
|--------|--------|--------------------------------------------------|----------------------------------------|
| 1024h  | 32     | <a href="#">CONTROLSS_CTRL_FAULT_ADDRESS</a>     | 502F 1024h                             |
| 1028h  | 32     | <a href="#">CONTROLSS_CTRL_FAULT_TYPE_STATUS</a> | 502F 1028h                             |
| 102Ch  | 32     | <a href="#">CONTROLSS_CTRL_FAULT_ATTR_STATUS</a> | 502F 102Ch                             |
| 1030h  | 32     | <a href="#">CONTROLSS_CTRL_FAULT_CLEAR</a>       | 502F 1030h                             |

## 2.7.2 CONTROLSS\_GLOBAL\_CTRL Registers

### CONTROLSS\_GLOBAL\_CTRL Registers

### 2.7.2.1 CONTROLSS\_CTRL\_EPWM\_STATICXBAR\_SEL0 Register

#### 1 CONTROLSS\_CTRL\_EPWM\_STATICXBAR\_SEL0 Register (Offset = 4h) [reset = 0h]

Static crossbar for epwm select.

Return to [Summary Table](#)

**Table 2-3179. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0004h       |

**Figure 2-1058. CONTROLSS\_CTRL\_EPWM\_STATICXBAR\_SEL0 Name Register**

| 31                              | 30                              | 29                              | 28                              | 27                              | 26                              | 25                              | 24                              |
|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|
| EPWM_STATICXBAR_SEL0_EP<br>WM15 | EPWM_STATICXBAR_SEL0_EP<br>WM14 | EPWM_STATICXBAR_SEL0_EP<br>WM13 | EPWM_STATICXBAR_SEL0_EP<br>WM12 | EPWM_STATICXBAR_SEL0_EP<br>WM11 | EPWM_STATICXBAR_SEL0_EP<br>WM10 | EPWM_STATICXBAR_SEL0_EP<br>WM9  | EPWM_STATICXBAR_SEL0_EP<br>WM8  |
| R/W                             | R/W                             | R/W                             | R/W                             | R/W                             | R/W                             | R/W                             | R/W                             |
| 0h                              | 0h                              | 0h                              | 0h                              | 0h                              | 0h                              | 0h                              | 0h                              |
| 23                              | 22                              | 21                              | 20                              | 19                              | 18                              | 17                              | 16                              |
| EPWM_STATICXBAR_SEL0_EP<br>WM7  | EPWM_STATICXBAR_SEL0_EP<br>WM6  | EPWM_STATICXBAR_SEL0_EP<br>WM5  | EPWM_STATICXBAR_SEL0_EP<br>WM4  | EPWM_STATICXBAR_SEL0_EP<br>WM3  | EPWM_STATICXBAR_SEL0_EP<br>WM2  | EPWM_STATICXBAR_SEL0_EP<br>WM1  | EPWM_STATICXBAR_SEL0_EP<br>WM0  |
| R/W                             | R/W                             | R/W                             | R/W                             | R/W                             | R/W                             | R/W                             | R/W                             |
| 0h                              | 0h                              | 0h                              | 0h                              | 0h                              | 0h                              | 0h                              | 0h                              |
| 15                              | 14                              | 13                              | 12                              | 11                              | 10                              | 9                               | 8                               |
| EPWM_STATICXBAR_SEL0_EP<br>WM3  | EPWM_STATICXBAR_SEL0_EP<br>WM2  | EPWM_STATICXBAR_SEL0_EP<br>WM1  | EPWM_STATICXBAR_SEL0_EP<br>WM0  | EPWM_STATICXBAR_SEL0_EP<br>WM15 | EPWM_STATICXBAR_SEL0_EP<br>WM14 | EPWM_STATICXBAR_SEL0_EP<br>WM13 | EPWM_STATICXBAR_SEL0_EP<br>WM12 |
| R/W                             | R/W                             | R/W                             | R/W                             | R/W                             | R/W                             | R/W                             | R/W                             |
| 0h                              | 0h                              | 0h                              | 0h                              | 0h                              | 0h                              | 0h                              | 0h                              |
| 7                               | 6                               | 5                               | 4                               | 3                               | 2                               | 1                               | 0                               |
| EPWM_STATICXBAR_SEL0_EP<br>WM3  | EPWM_STATICXBAR_SEL0_EP<br>WM2  | EPWM_STATICXBAR_SEL0_EP<br>WM1  | EPWM_STATICXBAR_SEL0_EP<br>WM0  | EPWM_STATICXBAR_SEL0_EP<br>WM15 | EPWM_STATICXBAR_SEL0_EP<br>WM14 | EPWM_STATICXBAR_SEL0_EP<br>WM13 | EPWM_STATICXBAR_SEL0_EP<br>WM12 |
| R/W                             | R/W                             | R/W                             | R/W                             | R/W                             | R/W                             | R/W                             | R/W                             |
| 0h                              | 0h                              | 0h                              | 0h                              | 0h                              | 0h                              | 0h                              | 0h                              |

**Table 2-3181. CONTROLSS\_CTRL\_EPWM\_STATICXBAR\_SEL0 Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                                                    |
|-------|---------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | EPWM_STATICXBAR_SE<br>L0_EPWM15 | R/W  | 0h    | EPWM15 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 = G1, 2'b10 = G2, 2'b11 = G3 |
| 29:28 | EPWM_STATICXBAR_SE<br>L0_EPWM14 | R/W  | 0h    | EPWM14 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 = G1, 2'b10 = G2, 2'b11 = G3 |
| 27:26 | EPWM_STATICXBAR_SE<br>L0_EPWM13 | R/W  | 0h    | EPWM13 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 = G1, 2'b10 = G2, 2'b11 = G3 |
| 25:24 | EPWM_STATICXBAR_SE<br>L0_EPWM12 | R/W  | 0h    | EPWM12 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 = G1, 2'b10 = G2, 2'b11 = G3 |
| 23:22 | EPWM_STATICXBAR_SE<br>L0_EPWM11 | R/W  | 0h    | EPWM11 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 = G1, 2'b10 = G2, 2'b11 = G3 |
| 21:20 | EPWM_STATICXBAR_SE<br>L0_EPWM10 | R/W  | 0h    | EPWM10 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 = G1, 2'b10 = G2, 2'b11 = G3 |
| 19:18 | EPWM_STATICXBAR_SE<br>L0_EPWM9  | R/W  | 0h    | EPWM9 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 = G1, 2'b10 = G2, 2'b11 = G3  |
| 17:16 | EPWM_STATICXBAR_SE<br>L0_EPWM8  | R/W  | 0h    | EPWM8 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 = G1, 2'b10 = G2, 2'b11 = G3  |
| 15:14 | EPWM_STATICXBAR_SE<br>L0_EPWM7  | R/W  | 0h    | EPWM7 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 = G1, 2'b10 = G2, 2'b11 = G3  |

**Table 2-3181. CONTROLSS\_CTRL\_EPWM\_STATICXBAR\_SEL0 Register Field Descriptions (continued)**

| Bit   | Field                      | Type | Reset | Description                                                                                                                |
|-------|----------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------|
| 13:12 | EPWM_STATICXBAR_SELO_EPWM6 | R/W  | 0h    | EPWM6 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 |
| 11:10 | EPWM_STATICXBAR_SELO_EPWM5 | R/W  | 0h    | EPWM5 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 |
| 9:8   | EPWM_STATICXBAR_SELO_EPWM4 | R/W  | 0h    | EPWM4 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 |
| 7:6   | EPWM_STATICXBAR_SELO_EPWM3 | R/W  | 0h    | EPWM3 access from PCR grouping. Write the following value to access groups - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3   |
| 5:4   | EPWM_STATICXBAR_SELO_EPWM2 | R/W  | 0h    | EPWM2 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 |
| 3:2   | EPWM_STATICXBAR_SELO_EPWM1 | R/W  | 0h    | EPWM1 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 |
| 1:0   | EPWM_STATICXBAR_SELO_EPWM0 | R/W  | 0h    | EPWM0 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 |



### 2.7.2.2 CONTROLSS\_CTRL\_EPWM\_STATICXBAR\_SEL1 Register

#### 1 CONTROLSS\_CTRL\_EPWM\_STATICXBAR\_SEL1 Register (Offset = 8h) [reset = 0h]

Static crossbar for epwm select.

Return to [Summary Table](#)

**Table 2-3182. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0008h       |

**Figure 2-1059. CONTROLSS\_CTRL\_EPWM\_STATICXBAR\_SEL1 Name Register**

| 31                              | 30                              | 29                              | 28                              | 27                              | 26                              | 25                              | 24                              |
|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|
| EPWM_STATICXBAR_SEL1_EP<br>WM31 | EPWM_STATICXBAR_SEL1_EP<br>WM30 | EPWM_STATICXBAR_SEL1_EP<br>WM29 | EPWM_STATICXBAR_SEL1_EP<br>WM28 | EPWM_STATICXBAR_SEL1_EP<br>WM27 | EPWM_STATICXBAR_SEL1_EP<br>WM26 | EPWM_STATICXBAR_SEL1_EP<br>WM25 | EPWM_STATICXBAR_SEL1_EP<br>WM24 |
| R/W                             | R/W                             | R/W                             | R/W                             | R/W                             | R/W                             | R/W                             | R/W                             |
| 0h                              | 0h                              | 0h                              | 0h                              | 0h                              | 0h                              | 0h                              | 0h                              |
| 23                              | 22                              | 21                              | 20                              | 19                              | 18                              | 17                              | 16                              |
| EPWM_STATICXBAR_SEL1_EP<br>WM23 | EPWM_STATICXBAR_SEL1_EP<br>WM22 | EPWM_STATICXBAR_SEL1_EP<br>WM21 | EPWM_STATICXBAR_SEL1_EP<br>WM20 | EPWM_STATICXBAR_SEL1_EP<br>WM19 | EPWM_STATICXBAR_SEL1_EP<br>WM18 | EPWM_STATICXBAR_SEL1_EP<br>WM17 | EPWM_STATICXBAR_SEL1_EP<br>WM16 |
| R/W                             | R/W                             | R/W                             | R/W                             | R/W                             | R/W                             | R/W                             | R/W                             |
| 0h                              | 0h                              | 0h                              | 0h                              | 0h                              | 0h                              | 0h                              | 0h                              |
| 15                              | 14                              | 13                              | 12                              | 11                              | 10                              | 9                               | 8                               |
| EPWM_STATICXBAR_SEL1_EP<br>WM15 | EPWM_STATICXBAR_SEL1_EP<br>WM14 | EPWM_STATICXBAR_SEL1_EP<br>WM13 | EPWM_STATICXBAR_SEL1_EP<br>WM12 | EPWM_STATICXBAR_SEL1_EP<br>WM11 | EPWM_STATICXBAR_SEL1_EP<br>WM10 | EPWM_STATICXBAR_SEL1_EP<br>WM9  | EPWM_STATICXBAR_SEL1_EP<br>WM8  |
| R/W                             | R/W                             | R/W                             | R/W                             | R/W                             | R/W                             | R/W                             | R/W                             |
| 0h                              | 0h                              | 0h                              | 0h                              | 0h                              | 0h                              | 0h                              | 0h                              |
| 7                               | 6                               | 5                               | 4                               | 3                               | 2                               | 1                               | 0                               |
| EPWM_STATICXBAR_SEL1_EP<br>WM7  | EPWM_STATICXBAR_SEL1_EP<br>WM6  | EPWM_STATICXBAR_SEL1_EP<br>WM5  | EPWM_STATICXBAR_SEL1_EP<br>WM4  | EPWM_STATICXBAR_SEL1_EP<br>WM3  | EPWM_STATICXBAR_SEL1_EP<br>WM2  | EPWM_STATICXBAR_SEL1_EP<br>WM1  | EPWM_STATICXBAR_SEL1_EP<br>WM0  |
| R/W                             | R/W                             | R/W                             | R/W                             | R/W                             | R/W                             | R/W                             | R/W                             |
| 0h                              | 0h                              | 0h                              | 0h                              | 0h                              | 0h                              | 0h                              | 0h                              |

**Table 2-3184. CONTROLSS\_CTRL\_EPWM\_STATICXBAR\_SEL1 Register Field Descriptions**

| Bit   | Field                           | Type | Reset | Description                                                                                                                 |
|-------|---------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:30 | EPWM_STATICXBAR_SE<br>L1_EPWM31 | R/W  | 0h    | EPWM31 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 |
| 29:28 | EPWM_STATICXBAR_SE<br>L1_EPWM30 | R/W  | 0h    | EPWM30 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 |
| 27:26 | EPWM_STATICXBAR_SE<br>L1_EPWM29 | R/W  | 0h    | EPWM29 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 |
| 25:24 | EPWM_STATICXBAR_SE<br>L1_EPWM28 | R/W  | 0h    | EPWM28 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 |
| 23:22 | EPWM_STATICXBAR_SE<br>L1_EPWM27 | R/W  | 0h    | EPWM27 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 |
| 21:20 | EPWM_STATICXBAR_SE<br>L1_EPWM26 | R/W  | 0h    | EPWM26 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 |
| 19:18 | EPWM_STATICXBAR_SE<br>L1_EPWM25 | R/W  | 0h    | EPWM25 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 |
| 17:16 | EPWM_STATICXBAR_SE<br>L1_EPWM24 | R/W  | 0h    | EPWM24 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 |
| 15:14 | EPWM_STATICXBAR_SE<br>L1_EPWM23 | R/W  | 0h    | EPWM23 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 |

**Table 2-3184. CONTROLSS\_CTRL\_EPWM\_STATICXBAR\_SEL1 Register Field Descriptions (continued)**

| Bit   | Field                           | Type | Reset | Description                                                                                                                 |
|-------|---------------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 13:12 | EPWM_STATICXBAR_SE<br>L1_EPWM22 | R/W  | 0h    | EPWM22 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 |
| 11:10 | EPWM_STATICXBAR_SE<br>L1_EPWM21 | R/W  | 0h    | EPWM21 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 |
| 9:8   | EPWM_STATICXBAR_SE<br>L1_EPWM20 | R/W  | 0h    | EPWM20 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 |
| 7:6   | EPWM_STATICXBAR_SE<br>L1_EPWM19 | R/W  | 0h    | EPWM19 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 |
| 5:4   | EPWM_STATICXBAR_SE<br>L1_EPWM18 | R/W  | 0h    | EPWM18 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 |
| 3:2   | EPWM_STATICXBAR_SE<br>L1_EPWM17 | R/W  | 0h    | EPWM17 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 |
| 1:0   | EPWM_STATICXBAR_SE<br>L1_EPWM16 | R/W  | 0h    | EPWM16 access from PCR grouping. Write the following value to access groups - - 2'b00 = G0, 2'b01 =G1, 2'b10 =G2, 2'b11 =G3 |

### 2.7.2.3 CONTROLSS\_CTRL\_EPWM\_CLKSYNC Register

#### 1 CONTROLSS\_CTRL\_EPWM\_CLKSYNC Register (Offset = 10h) [reset = 0h]

Epwm clock sync.

Return to [Summary Table](#)

**Table 2-3185. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0010h       |

**Figure 2-1060. CONTROLSS\_CTRL\_EPWM\_CLKSYNC Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| EPWM_CLKSYNC_BIT |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| EPWM_CLKSYNC_BIT |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| EPWM_CLKSYNC_BIT |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| EPWM_CLKSYNC_BIT |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 2-3187. CONTROLSS\_CTRL\_EPWM\_CLKSYNC Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                        |
|------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | EPWM_CLKSYNC_BIT | R/W  | 0h    | EPWM clock sync for each EPWM instance. Set the bit corresponding to the instance number to enable that EPWM instance. When set, all enabled EPWM module clocks are started with the first rising edge of TBCLK aligned. Refer to TRM for more details.<br>Writing 1'b1 will allow to enable corresponding EPWM instance<br>Writing 1'b0 will disable corresponding EPWM instance. |

### 2.7.2.4 CONTROLSS\_CTRL\_SDFM1\_CLK0\_SEL Register

#### 1 CONTROLSS\_CTRL\_SDFM1\_CLK0\_SEL Register (Offset = 18h) [reset = 0h]

Sdfm1 clock select.

Return to [Summary Table](#)

**Table 2-3188. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0018h       |

**Figure 2-1061. CONTROLSS\_CTRL\_SDFM1\_CLK0\_SEL Name Register**

|          |    |    |    |    |    |    |                    |
|----------|----|----|----|----|----|----|--------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                 |
| RESERVED |    |    |    |    |    |    |                    |
| NONE     |    |    |    |    |    |    |                    |
| 0h       |    |    |    |    |    |    |                    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
| RESERVED |    |    |    |    |    |    |                    |
| NONE     |    |    |    |    |    |    |                    |
| 0h       |    |    |    |    |    |    |                    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                  |
| RESERVED |    |    |    |    |    |    |                    |
| NONE     |    |    |    |    |    |    |                    |
| 0h       |    |    |    |    |    |    |                    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| RESERVED |    |    |    |    |    |    | SDFM1_CLK0_SEL_SEL |
| NONE     |    |    |    |    |    |    | R/W                |
| 0h       |    |    |    |    |    |    | 0h                 |

**Table 2-3190. CONTROLSS\_CTRL\_SDFM1\_CLK0\_SEL Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                          |
|------|--------------------|------|-------|----------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED           | NONE | 0h    | Reserved                                                                                                             |
| 0    | SDFM1_CLK0_SEL_SEL | R/W  | 0h    | SDFM1 clock CK0 select<br>Write 1'b0: source is SDFM1 CK0 from Pinmux<br>Write 1'b1: source is SDFM0 CK0 from Pinmux |

### 2.7.2.5 CONTROLSS\_CTRL\_EMUSTOPN\_MASK Register

#### 1 CONTROLSS\_CTRL\_EMUSTOPN\_MASK Register (Offset = 20h) [reset = 0h]

Bit-mask for debug suspend cpu cores to EPWM.

Return to [Summary Table](#)

**Table 2-3191. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0020h       |

**Figure 2-1062. CONTROLSS\_CTRL\_EMUSTOPN\_MASK Name Register**

|          |    |    |    |                         |                         |                         |                         |
|----------|----|----|----|-------------------------|-------------------------|-------------------------|-------------------------|
| 31       | 30 | 29 | 28 | 27                      | 26                      | 25                      | 24                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 23       | 22 | 21 | 20 | 19                      | 18                      | 17                      | 16                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 15       | 14 | 13 | 12 | 11                      | 10                      | 9                       | 8                       |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 7        | 6  | 5  | 4  | 3                       | 2                       | 1                       | 0                       |
| RESERVED |    |    |    | EMUSTOPN_M<br>ASK_CR5B1 | EMUSTOPN_M<br>ASK_CR5A1 | EMUSTOPN_M<br>ASK_CR5B0 | EMUSTOPN_M<br>ASK_CR5A0 |
| NONE     |    |    |    | R/W                     | R/W                     | R/W                     | R/W                     |
| 0h       |    |    |    | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 2-3193. CONTROLSS\_CTRL\_EMUSTOPN\_MASK Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                                                                                                                         |
|------|-------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                | NONE | 0h    | Reserved                                                                                                                                            |
| 3    | EMUSTOPN_MASK_CR5<br>B1 | R/W  | 0h    | Bit-mask for debug suspend cpu cores to EPWM<br>1'b0 : R5FSS1_CORE1 enabled to control EMUSTOPn<br>1'b1 : R5FSS1_CORE1 disabled to control EMUSTOPn |
| 2    | EMUSTOPN_MASK_CR5<br>A1 | R/W  | 0h    | Bit-mask for debug suspend cpu cores to EPWM<br>1'b0 : R5FSS1_CORE0 enabled to control EMUSTOPn<br>1'b1 : R5FSS1_CORE0 disabled to control EMUSTOPn |
| 1    | EMUSTOPN_MASK_CR5<br>B0 | R/W  | 0h    | Bit-mask for debug suspend cpu cores to EPWM<br>1'b0 : R5FSS0_CORE1 enabled to control EMUSTOPn<br>1'b1 : R5FSS0_CORE1 disabled to control EMUSTOPn |
| 0    | EMUSTOPN_MASK_CR5<br>A0 | R/W  | 0h    | Bit-mask for debug suspend cpu cores to EPWM<br>1'b0 : R5FSS0_CORE0 enabled to control EMUSTOPn<br>1'b1 : R5FSS0_CORE0 disabled to control EMUSTOPn |

### 2.7.2.6 CONTROLSS\_CTRL\_CLB\_AQ\_EN0 Register

#### 1 CONTROLSS\_CTRL\_CLB\_AQ\_EN0 Register (Offset = 28h) [reset = 0h]

clb\_aq\_en0.

Return to [Summary Table](#)

**Table 2-3194. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0028h       |

**Figure 2-1063. CONTROLSS\_CTRL\_CLB\_AQ\_EN0 Name Register**

|                   |    |    |    |    |    |    |    |
|-------------------|----|----|----|----|----|----|----|
| 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CLB_AQ_EN0_ENABLE |    |    |    |    |    |    |    |
| R/W               |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CLB_AQ_EN0_ENABLE |    |    |    |    |    |    |    |
| R/W               |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CLB_AQ_EN0_ENABLE |    |    |    |    |    |    |    |
| R/W               |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CLB_AQ_EN0_ENABLE |    |    |    |    |    |    |    |
| R/W               |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |

**Table 2-3196. CONTROLSS\_CTRL\_CLB\_AQ\_EN0 Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                                                                                                         |
|------|-------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:0 | CLB_AQ_EN0_ENABLE | R/W  | 0h    | Enable ICCS control to CLB_AQ signal of PWM[15:0]. Set Bitx to 1'b1 to enable it for PWMx. Here x varies from 0-15. |

### 2.7.2.7 CONTROLSS\_CTRL\_CLB\_AQ\_EN1 Register

#### 1 CONTROLSS\_CTRL\_CLB\_AQ\_EN1 Register (Offset = 30h) [reset = 0h]

clb\_aq\_en1.

Return to [Summary Table](#)

**Table 2-3197. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0030h       |

**Figure 2-1064. CONTROLSS\_CTRL\_CLB\_AQ\_EN1 Name Register**

|                   |    |    |    |    |    |    |    |
|-------------------|----|----|----|----|----|----|----|
| 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CLB_AQ_EN1_ENABLE |    |    |    |    |    |    |    |
| R/W               |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CLB_AQ_EN1_ENABLE |    |    |    |    |    |    |    |
| R/W               |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CLB_AQ_EN1_ENABLE |    |    |    |    |    |    |    |
| R/W               |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CLB_AQ_EN1_ENABLE |    |    |    |    |    |    |    |
| R/W               |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |

**Table 2-3199. CONTROLSS\_CTRL\_CLB\_AQ\_EN1 Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                                                                                                           |
|------|-------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------|
| 31:0 | CLB_AQ_EN1_ENABLE | R/W  | 0h    | Enable ICCS control to CLB_AQ signal of PWM[31:16]. Set Bitx to 1'b1 to enable it for PWMx. Here x varies from 16-31. |

### 2.7.2.8 CONTROLSS\_CTRL\_CLB\_DB\_EN0 Register

#### 1 CONTROLSS\_CTRL\_CLB\_DB\_EN0 Register (Offset = 38h) [reset = 0h]

clb\_db\_en0.

Return to [Summary Table](#)

**Table 2-3200. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0038h       |

**Figure 2-1065. CONTROLSS\_CTRL\_CLB\_DB\_EN0 Name Register**

|                   |    |    |    |    |    |    |    |
|-------------------|----|----|----|----|----|----|----|
| 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CLB_DB_EN0_ENABLE |    |    |    |    |    |    |    |
| R/W               |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CLB_DB_EN0_ENABLE |    |    |    |    |    |    |    |
| R/W               |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CLB_DB_EN0_ENABLE |    |    |    |    |    |    |    |
| R/W               |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CLB_DB_EN0_ENABLE |    |    |    |    |    |    |    |
| R/W               |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |

**Table 2-3202. CONTROLSS\_CTRL\_CLB\_DB\_EN0 Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                                                                                                         |
|------|-------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:0 | CLB_DB_EN0_ENABLE | R/W  | 0h    | Enable ICCS control to CLB_DB signal of PWM[15:0]. Set Bitx to 1'b1 to enable it for PWMx. Here x varies from 0-15. |



### 2.7.2.9 CONTROLSS\_CTRL\_CLB\_DB\_EN1 Register

#### 1 CONTROLSS\_CTRL\_CLB\_DB\_EN1 Register (Offset = 40h) [reset = 0h]

clb\_db\_en1.

Return to [Summary Table](#)

**Table 2-3203. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0040h       |

**Figure 2-1066. CONTROLSS\_CTRL\_CLB\_DB\_EN1 Name Register**

|                   |    |    |    |    |    |    |    |
|-------------------|----|----|----|----|----|----|----|
| 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CLB_DB_EN1_ENABLE |    |    |    |    |    |    |    |
| R/W               |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CLB_DB_EN1_ENABLE |    |    |    |    |    |    |    |
| R/W               |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CLB_DB_EN1_ENABLE |    |    |    |    |    |    |    |
| R/W               |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CLB_DB_EN1_ENABLE |    |    |    |    |    |    |    |
| R/W               |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |

**Table 2-3205. CONTROLSS\_CTRL\_CLB\_DB\_EN1 Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                                                                                                           |
|------|-------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------|
| 31:0 | CLB_DB_EN1_ENABLE | R/W  | 0h    | Enable ICCS control to CLB_DB signal of PWM[31:16]. Set Bitx to 1'b1 to enable it for PWMx. Here x varies from 16-31. |

### 2.7.2.10 CONTROLSS\_CTRL\_EPWM0\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM0\_CLK\_GATE Register (Offset = 100h) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3206. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0100h       |

**Figure 2-1067. CONTROLSS\_CTRL\_EPWM0\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM0_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-3208. CONTROLSS\_CTRL\_EPWM0\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM0_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

### 2.7.2.11 CONTROLSS\_CTRL\_EPWM1\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM1\_CLK\_GATE Register (Offset = 104h) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3209. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0104h       |

**Figure 2-1068. CONTROLSS\_CTRL\_EPWM1\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM1_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-3211. CONTROLSS\_CTRL\_EPWM1\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM1_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

### 2.7.2.12 CONTROLSS\_CTRL\_EPWM2\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM2\_CLK\_GATE Register (Offset = 108h) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3212. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0108h       |

**Figure 2-1069. CONTROLSS\_CTRL\_EPWM2\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM2_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-3214. CONTROLSS\_CTRL\_EPWM2\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM2_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

### 2.7.2.13 CONTROLSS\_CTRL\_EPWM3\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM3\_CLK\_GATE Register (Offset = 10Ch) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3215. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 010Ch       |

**Figure 2-1070. CONTROLSS\_CTRL\_EPWM3\_CLK\_GATE Name Register**

|          |    |    |    |    |                         |    |    |
|----------|----|----|----|----|-------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                      | 25 | 24 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                      | 17 | 16 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                      | 9  | 8  |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                       | 1  | 0  |
| RESERVED |    |    |    |    | EPWM3_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                     |    |    |
| 0h       |    |    |    |    | 0h                      |    |    |

**Table 2-3217. CONTROLSS\_CTRL\_EPWM3\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM3_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

### 2.7.2.14 CONTROLSS\_CTRL\_EPWM4\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM4\_CLK\_GATE Register (Offset = 110h) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3218. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0110h       |

**Figure 2-1071. CONTROLSS\_CTRL\_EPWM4\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM4_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-3220. CONTROLSS\_CTRL\_EPWM4\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM4_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

### 2.7.2.15 CONTROLSS\_CTRL\_EPWM5\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM5\_CLK\_GATE Register (Offset = 114h) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3221. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0114h       |

**Figure 2-1072. CONTROLSS\_CTRL\_EPWM5\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM5_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-3223. CONTROLSS\_CTRL\_EPWM5\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM5_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

### 2.7.2.16 CONTROLSS\_CTRL\_EPWM6\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM6\_CLK\_GATE Register (Offset = 118h) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3224. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0118h       |

**Figure 2-1073. CONTROLSS\_CTRL\_EPWM6\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM6_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-3226. CONTROLSS\_CTRL\_EPWM6\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM6_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |



### 2.7.2.17 CONTROLSS\_CTRL\_EPWM7\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM7\_CLK\_GATE Register (Offset = 11Ch) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3227. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 011Ch       |

**Figure 2-1074. CONTROLSS\_CTRL\_EPWM7\_CLK\_GATE Name Register**

|          |    |    |    |    |                         |    |    |
|----------|----|----|----|----|-------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                      | 25 | 24 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                      | 17 | 16 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                      | 9  | 8  |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                       | 1  | 0  |
| RESERVED |    |    |    |    | EPWM7_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                     |    |    |
| 0h       |    |    |    |    | 0h                      |    |    |

**Table 2-3229. CONTROLSS\_CTRL\_EPWM7\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM7_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

### 2.7.2.18 CONTROLSS\_CTRL\_EPWM8\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM8\_CLK\_GATE Register (Offset = 120h) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3230. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0120h       |

**Figure 2-1075. CONTROLSS\_CTRL\_EPWM8\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM8_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-3232. CONTROLSS\_CTRL\_EPWM8\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM8_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

### 2.7.2.19 CONTROLSS\_CTRL\_EPWM9\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM9\_CLK\_GATE Register (Offset = 124h) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3233. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0124h       |

**Figure 2-1076. CONTROLSS\_CTRL\_EPWM9\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM9_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-3235. CONTROLSS\_CTRL\_EPWM9\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM9_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

## 2.7.2.20 CONTROLSS\_CTRL\_EPWM10\_CLK\_GATE Register

### 1 CONTROLSS\_CTRL\_EPWM10\_CLK\_GATE Register (Offset = 128h) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3236. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0128h       |

**Figure 2-1077. CONTROLSS\_CTRL\_EPWM10\_CLK\_GATE Name Register**

|          |    |    |    |                          |    |    |    |
|----------|----|----|----|--------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 23       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 15       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 7        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM10_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                      |    |    |    |
| 0h       |    |    |    | 0h                       |    |    |    |

**Table 2-3238. CONTROLSS\_CTRL\_EPWM10\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM10_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

### 2.7.2.21 CONTROLSS\_CTRL\_EPWM11\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM11\_CLK\_GATE Register (Offset = 12Ch) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3239. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 012Ch       |

**Figure 2-1078. CONTROLSS\_CTRL\_EPWM11\_CLK\_GATE Name Register**

|          |    |    |    |                          |    |    |    |
|----------|----|----|----|--------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 23       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 15       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 7        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM11_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                      |    |    |    |
| 0h       |    |    |    | 0h                       |    |    |    |

**Table 2-3241. CONTROLSS\_CTRL\_EPWM11\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM11_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

### 2.7.2.22 CONTROLSS\_CTRL\_EPWM12\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM12\_CLK\_GATE Register (Offset = 130h) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3242. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0130h       |

**Figure 2-1079. CONTROLSS\_CTRL\_EPWM12\_CLK\_GATE Name Register**

|          |    |    |    |                          |    |    |    |
|----------|----|----|----|--------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 23       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 15       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 7        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM12_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                      |    |    |    |
| 0h       |    |    |    | 0h                       |    |    |    |

**Table 2-3244. CONTROLSS\_CTRL\_EPWM12\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM12_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

### 2.7.2.23 CONTROLSS\_CTRL\_EPWM13\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM13\_CLK\_GATE Register (Offset = 134h) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3245. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0134h       |

**Figure 2-1080. CONTROLSS\_CTRL\_EPWM13\_CLK\_GATE Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | EPWM13_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-3247. CONTROLSS\_CTRL\_EPWM13\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM13_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

### 2.7.2.24 CONTROLSS\_CTRL\_EPWM14\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM14\_CLK\_GATE Register (Offset = 138h) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3248. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0138h       |

**Figure 2-1081. CONTROLSS\_CTRL\_EPWM14\_CLK\_GATE Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | EPWM14_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-3250. CONTROLSS\_CTRL\_EPWM14\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM14_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |



### 2.7.2.25 CONTROLSS\_CTRL\_EPWM15\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM15\_CLK\_GATE Register (Offset = 13Ch) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3251. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 013Ch       |

**Figure 2-1082. CONTROLSS\_CTRL\_EPWM15\_CLK\_GATE Name Register**

|          |    |    |    |                          |    |    |    |
|----------|----|----|----|--------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 23       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 15       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 7        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM15_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                      |    |    |    |
| 0h       |    |    |    | 0h                       |    |    |    |

**Table 2-3253. CONTROLSS\_CTRL\_EPWM15\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM15_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

### 2.7.2.26 CONTROLSS\_CTRL\_EPWM16\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM16\_CLK\_GATE Register (Offset = 140h) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3254. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0140h       |

**Figure 2-1083. CONTROLSS\_CTRL\_EPWM16\_CLK\_GATE Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | EPWM16_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-3256. CONTROLSS\_CTRL\_EPWM16\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM16_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

### 2.7.2.27 CONTROLSS\_CTRL\_EPWM17\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM17\_CLK\_GATE Register (Offset = 144h) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3257. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0144h       |

**Figure 2-1084. CONTROLSS\_CTRL\_EPWM17\_CLK\_GATE Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | EPWM17_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-3259. CONTROLSS\_CTRL\_EPWM17\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM17_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

### 2.7.2.28 CONTROLSS\_CTRL\_EPWM18\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM18\_CLK\_GATE Register (Offset = 148h) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3260. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0148h       |

**Figure 2-1085. CONTROLSS\_CTRL\_EPWM18\_CLK\_GATE Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | EPWM18_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-3262. CONTROLSS\_CTRL\_EPWM18\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM18_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

### 2.7.2.29 CONTROLSS\_CTRL\_EPWM19\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM19\_CLK\_GATE Register (Offset = 14Ch) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3263. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 014Ch       |

**Figure 2-1086. CONTROLSS\_CTRL\_EPWM19\_CLK\_GATE Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | EPWM19_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-3265. CONTROLSS\_CTRL\_EPWM19\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM19_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

### 2.7.2.30 CONTROLSS\_CTRL\_EPWM20\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM20\_CLK\_GATE Register (Offset = 150h) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3266. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0150h       |

**Figure 2-1087. CONTROLSS\_CTRL\_EPWM20\_CLK\_GATE Name Register**

|          |    |    |    |                          |    |    |    |
|----------|----|----|----|--------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 23       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 15       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 7        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM20_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                      |    |    |    |
| 0h       |    |    |    | 0h                       |    |    |    |

**Table 2-3268. CONTROLSS\_CTRL\_EPWM20\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM20_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

### 2.7.2.31 CONTROLSS\_CTRL\_EPWM21\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM21\_CLK\_GATE Register (Offset = 154h) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3269. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0154h       |

**Figure 2-1088. CONTROLSS\_CTRL\_EPWM21\_CLK\_GATE Name Register**

|          |    |    |    |                          |    |    |    |
|----------|----|----|----|--------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 23       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 15       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 7        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM21_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                      |    |    |    |
| 0h       |    |    |    | 0h                       |    |    |    |

**Table 2-3271. CONTROLSS\_CTRL\_EPWM21\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM21_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

### 2.7.2.32 CONTROLSS\_CTRL\_EPWM22\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM22\_CLK\_GATE Register (Offset = 158h) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3272. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0158h       |

**Figure 2-1089. CONTROLSS\_CTRL\_EPWM22\_CLK\_GATE Name Register**

|          |    |    |    |                          |    |    |    |
|----------|----|----|----|--------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 23       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 15       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 7        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM22_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                      |    |    |    |
| 0h       |    |    |    | 0h                       |    |    |    |

**Table 2-3274. CONTROLSS\_CTRL\_EPWM22\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM22_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |



### 2.7.2.33 CONTROLSS\_CTRL\_EPWM23\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM23\_CLK\_GATE Register (Offset = 15Ch) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3275. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 015Ch       |

**Figure 2-1090. CONTROLSS\_CTRL\_EPWM23\_CLK\_GATE Name Register**

|          |    |    |    |                          |    |    |    |
|----------|----|----|----|--------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 23       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 15       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 7        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM23_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                      |    |    |    |
| 0h       |    |    |    | 0h                       |    |    |    |

**Table 2-3277. CONTROLSS\_CTRL\_EPWM23\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM23_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

### 2.7.2.34 CONTROLSS\_CTRL\_EPWM24\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM24\_CLK\_GATE Register (Offset = 160h) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3278. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0160h       |

**Figure 2-1091. CONTROLSS\_CTRL\_EPWM24\_CLK\_GATE Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | EPWM24_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-3280. CONTROLSS\_CTRL\_EPWM24\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM24_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

### 2.7.2.35 CONTROLSS\_CTRL\_EPWM25\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM25\_CLK\_GATE Register (Offset = 164h) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3281. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0164h       |

**Figure 2-1092. CONTROLSS\_CTRL\_EPWM25\_CLK\_GATE Name Register**

|          |    |    |    |                          |    |    |    |
|----------|----|----|----|--------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 23       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 15       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 7        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM25_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                      |    |    |    |
| 0h       |    |    |    | 0h                       |    |    |    |

**Table 2-3283. CONTROLSS\_CTRL\_EPWM25\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM25_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

### 2.7.2.36 CONTROLSS\_CTRL\_EPWM26\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM26\_CLK\_GATE Register (Offset = 168h) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3284. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0168h       |

**Figure 2-1093. CONTROLSS\_CTRL\_EPWM26\_CLK\_GATE Name Register**

|          |    |    |    |                          |    |    |    |
|----------|----|----|----|--------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 23       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 15       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 7        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM26_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                      |    |    |    |
| 0h       |    |    |    | 0h                       |    |    |    |

**Table 2-3286. CONTROLSS\_CTRL\_EPWM26\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM26_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

### 2.7.2.37 CONTROLSS\_CTRL\_EPWM27\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM27\_CLK\_GATE Register (Offset = 16Ch) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3287. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 016Ch       |

**Figure 2-1094. CONTROLSS\_CTRL\_EPWM27\_CLK\_GATE Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | EPWM27_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-3289. CONTROLSS\_CTRL\_EPWM27\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM27_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

### 2.7.2.38 CONTROLSS\_CTRL\_EPWM28\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM28\_CLK\_GATE Register (Offset = 170h) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3290. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0170h       |

**Figure 2-1095. CONTROLSS\_CTRL\_EPWM28\_CLK\_GATE Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | EPWM28_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-3292. CONTROLSS\_CTRL\_EPWM28\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM28_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

### 2.7.2.39 CONTROLSS\_CTRL\_EPWM29\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM29\_CLK\_GATE Register (Offset = 174h) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3293. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0174h       |

**Figure 2-1096. CONTROLSS\_CTRL\_EPWM29\_CLK\_GATE Name Register**

|          |    |    |    |                          |    |    |    |
|----------|----|----|----|--------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 23       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 15       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 7        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM29_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                      |    |    |    |
| 0h       |    |    |    | 0h                       |    |    |    |

**Table 2-3295. CONTROLSS\_CTRL\_EPWM29\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM29_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

### 2.7.2.40 CONTROLSS\_CTRL\_EPWM30\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM30\_CLK\_GATE Register (Offset = 178h) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3296. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0178h       |

**Figure 2-1097. CONTROLSS\_CTRL\_EPWM30\_CLK\_GATE Name Register**

|          |    |    |    |                          |    |    |    |
|----------|----|----|----|--------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                       | 26 | 25 | 24 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 23       | 22 | 21 | 20 | 19                       | 18 | 17 | 16 |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 15       | 14 | 13 | 12 | 11                       | 10 | 9  | 8  |
| RESERVED |    |    |    |                          |    |    |    |
| NONE     |    |    |    |                          |    |    |    |
| 0h       |    |    |    |                          |    |    |    |
| 7        | 6  | 5  | 4  | 3                        | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM30_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                      |    |    |    |
| 0h       |    |    |    | 0h                       |    |    |    |

**Table 2-3298. CONTROLSS\_CTRL\_EPWM30\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM30_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |



### 2.7.2.41 CONTROLSS\_CTRL\_EPWM31\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EPWM31\_CLK\_GATE Register (Offset = 17Ch) [reset = 0h]

To clock gate epwm[x].

Return to [Summary Table](#)

**Table 2-3299. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 017Ch       |

**Figure 2-1098. CONTROLSS\_CTRL\_EPWM31\_CLK\_GATE Name Register**

|          |    |    |    |    |                          |    |    |
|----------|----|----|----|----|--------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                       | 25 | 24 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                       | 17 | 16 |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                       | 9  | 8  |
| RESERVED |    |    |    |    |                          |    |    |
| NONE     |    |    |    |    |                          |    |    |
| 0h       |    |    |    |    |                          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                        | 1  | 0  |
| RESERVED |    |    |    |    | EPWM31_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                      |    |    |
| 0h       |    |    |    |    | 0h                       |    |    |

**Table 2-3301. CONTROLSS\_CTRL\_EPWM31\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                           |
|------|--------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                 | NONE | 0h    | Reserved                                              |
| 2:0  | EPWM31_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding epwm |

### 2.7.2.42 CONTROLSS\_CTRL\_FSI\_TX0\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_FSI\_TX0\_CLK\_GATE Register (Offset = 180h) [reset = 0h]

fsi\_tx[x] clock gate.

Return to [Summary Table](#)

**Table 2-3302. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0180h       |

**Figure 2-1099. CONTROLSS\_CTRL\_FSI\_TX0\_CLK\_GATE Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | FSI_TX0_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3304. CONTROLSS\_CTRL\_FSI\_TX0\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                             |
|------|---------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                |
| 2:0  | FSI_TX0_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding fsi_tx |

### 2.7.2.43 CONTROLSS\_CTRL\_FSI\_TX1\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_FSI\_TX1\_CLK\_GATE Register (Offset = 184h) [reset = 0h]

fsi\_tx[x] clock gate.

Return to [Summary Table](#)

**Table 2-3305. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0184h       |

**Figure 2-1100. CONTROLSS\_CTRL\_FSI\_TX1\_CLK\_GATE Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | FSI_TX1_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3307. CONTROLSS\_CTRL\_FSI\_TX1\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                             |
|------|---------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                |
| 2:0  | FSI_TX1_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding fsi_tx |

### 2.7.2.44 CONTROLSS\_CTRL\_FSI\_TX2\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_FSI\_TX2\_CLK\_GATE Register (Offset = 188h) [reset = 0h]

fsi\_tx[x] clock gate.

Return to [Summary Table](#)

**Table 2-3308. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0188h       |

**Figure 2-1101. CONTROLSS\_CTRL\_FSI\_TX2\_CLK\_GATE Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | FSI_TX2_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3310. CONTROLSS\_CTRL\_FSI\_TX2\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                             |
|------|---------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                |
| 2:0  | FSI_TX2_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding fsi_tx |

### 2.7.2.45 CONTROLSS\_CTRL\_FSI\_TX3\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_FSI\_TX3\_CLK\_GATE Register (Offset = 18Ch) [reset = 0h]

fsi\_tx[x] clock gate.

Return to [Summary Table](#)

**Table 2-3311. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 018Ch       |

**Figure 2-1102. CONTROLSS\_CTRL\_FSI\_TX3\_CLK\_GATE Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | FSI_TX3_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3313. CONTROLSS\_CTRL\_FSI\_TX3\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                             |
|------|---------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                |
| 2:0  | FSI_TX3_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding fsi_tx |

### 2.7.2.46 CONTROLSS\_CTRL\_FSI\_RX0\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_FSI\_RX0\_CLK\_GATE Register (Offset = 190h) [reset = 0h]

fsi\_rx[x] clock gate.

Return to [Summary Table](#)

**Table 2-3314. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0190h       |

**Figure 2-1103. CONTROLSS\_CTRL\_FSI\_RX0\_CLK\_GATE Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | FSI_RX0_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3316. CONTROLSS\_CTRL\_FSI\_RX0\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                             |
|------|---------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                |
| 2:0  | FSI_RX0_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding fsi_rx |

### 2.7.2.47 CONTROLSS\_CTRL\_FSI\_RX1\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_FSI\_RX1\_CLK\_GATE Register (Offset = 194h) [reset = 0h]

fsi\_rx[x] clock gate.

Return to [Summary Table](#)

**Table 2-3317. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0194h       |

**Figure 2-1104. CONTROLSS\_CTRL\_FSI\_RX1\_CLK\_GATE Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | FSI_RX1_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3319. CONTROLSS\_CTRL\_FSI\_RX1\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                             |
|------|---------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                |
| 2:0  | FSI_RX1_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding fsi_rx |

### 2.7.2.48 CONTROLSS\_CTRL\_FSI\_RX2\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_FSI\_RX2\_CLK\_GATE Register (Offset = 198h) [reset = 0h]

fsi\_rx[x] clock gate.

Return to [Summary Table](#)

**Table 2-3320. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0198h       |

**Figure 2-1105. CONTROLSS\_CTRL\_FSI\_RX2\_CLK\_GATE Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | FSI_RX2_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3322. CONTROLSS\_CTRL\_FSI\_RX2\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                             |
|------|---------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                |
| 2:0  | FSI_RX2_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding fsi_rx |



### 2.7.2.49 CONTROLSS\_CTRL\_FSI\_RX3\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_FSI\_RX3\_CLK\_GATE Register (Offset = 19Ch) [reset = 0h]

fsi\_rx[x] clock gate.

Return to [Summary Table](#)

**Table 2-3323. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 019Ch       |

**Figure 2-1106. CONTROLSS\_CTRL\_FSI\_RX3\_CLK\_GATE Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | FSI_RX3_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3325. CONTROLSS\_CTRL\_FSI\_RX3\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                             |
|------|---------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                  | NONE | 0h    | Reserved                                                |
| 2:0  | FSI_RX3_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding fsi_rx |

### 2.7.2.50 CONTROLSS\_CTRL\_CMPSSA0\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_CMPSSA0\_CLK\_GATE Register (Offset = 1A0h) [reset = 0h]

cmpssa[x] clock gate.

Return to [Summary Table](#)

**Table 2-3326. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 01A0h       |

**Figure 2-1107. CONTROLSS\_CTRL\_CMPSSA0\_CLK\_GATE Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | CMPSSA0_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3328. CONTROLSS\_CTRL\_CMPSSA0\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                             |
|------|-------------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                      | NONE | 0h    | Reserved                                                |
| 2:0  | CMPSSA0_CLK_GATE_C<br>LK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding cmpssa |

### 2.7.2.51 CONTROLSS\_CTRL\_CMPSSA1\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_CMPSSA1\_CLK\_GATE Register (Offset = 1A4h) [reset = 0h]

cmpssa[x] clock gate.

Return to [Summary Table](#)

**Table 2-3329. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 01A4h       |

**Figure 2-1108. CONTROLSS\_CTRL\_CMPSSA1\_CLK\_GATE Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | CMPSSA1_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3331. CONTROLSS\_CTRL\_CMPSSA1\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                             |
|------|-------------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                      | NONE | 0h    | Reserved                                                |
| 2:0  | CMPSSA1_CLK_GATE_C<br>LK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding cmpssa |

### 2.7.2.52 CONTROLSS\_CTRL\_CMPSSA2\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_CMPSSA2\_CLK\_GATE Register (Offset = 1A8h) [reset = 0h]

cmpssa[x] clock gate.

Return to [Summary Table](#)

**Table 2-3332. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 01A8h       |

**Figure 2-1109. CONTROLSS\_CTRL\_CMPSSA2\_CLK\_GATE Name Register**

|          |    |    |    |                           |    |    |    |
|----------|----|----|----|---------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                        | 26 | 25 | 24 |
| RESERVED |    |    |    |                           |    |    |    |
| NONE     |    |    |    |                           |    |    |    |
| 0h       |    |    |    |                           |    |    |    |
| 23       | 22 | 21 | 20 | 19                        | 18 | 17 | 16 |
| RESERVED |    |    |    |                           |    |    |    |
| NONE     |    |    |    |                           |    |    |    |
| 0h       |    |    |    |                           |    |    |    |
| 15       | 14 | 13 | 12 | 11                        | 10 | 9  | 8  |
| RESERVED |    |    |    |                           |    |    |    |
| NONE     |    |    |    |                           |    |    |    |
| 0h       |    |    |    |                           |    |    |    |
| 7        | 6  | 5  | 4  | 3                         | 2  | 1  | 0  |
| RESERVED |    |    |    | CMPSSA2_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                       |    |    |    |
| 0h       |    |    |    | 0h                        |    |    |    |

**Table 2-3334. CONTROLSS\_CTRL\_CMPSSA2\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                             |
|------|-------------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                      | NONE | 0h    | Reserved                                                |
| 2:0  | CMPSSA2_CLK_GATE_C<br>LK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding cmpssa |

### 2.7.2.53 CONTROLSS\_CTRL\_CMPSSA3\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_CMPSSA3\_CLK\_GATE Register (Offset = 1ACh) [reset = 0h]

cmpssa[x] clock gate.

Return to [Summary Table](#)

**Table 2-3335. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 01ACh       |

**Figure 2-1110. CONTROLSS\_CTRL\_CMPSSA3\_CLK\_GATE Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | CMPSSA3_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3337. CONTROLSS\_CTRL\_CMPSSA3\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                             |
|------|-------------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                      | NONE | 0h    | Reserved                                                |
| 2:0  | CMPSSA3_CLK_GATE_C<br>LK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding cmpssa |

### 2.7.2.54 CONTROLSS\_CTRL\_CMPSSA4\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_CMPSSA4\_CLK\_GATE Register (Offset = 1B0h) [reset = 0h]

cmpssa[x] clock gate.

Return to [Summary Table](#)

**Table 2-3338. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 01B0h       |

**Figure 2-1111. CONTROLSS\_CTRL\_CMPSSA4\_CLK\_GATE Name Register**

|          |    |    |    |                           |    |    |    |
|----------|----|----|----|---------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                        | 26 | 25 | 24 |
| RESERVED |    |    |    |                           |    |    |    |
| NONE     |    |    |    |                           |    |    |    |
| 0h       |    |    |    |                           |    |    |    |
| 23       | 22 | 21 | 20 | 19                        | 18 | 17 | 16 |
| RESERVED |    |    |    |                           |    |    |    |
| NONE     |    |    |    |                           |    |    |    |
| 0h       |    |    |    |                           |    |    |    |
| 15       | 14 | 13 | 12 | 11                        | 10 | 9  | 8  |
| RESERVED |    |    |    |                           |    |    |    |
| NONE     |    |    |    |                           |    |    |    |
| 0h       |    |    |    |                           |    |    |    |
| 7        | 6  | 5  | 4  | 3                         | 2  | 1  | 0  |
| RESERVED |    |    |    | CMPSSA4_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                       |    |    |    |
| 0h       |    |    |    | 0h                        |    |    |    |

**Table 2-3340. CONTROLSS\_CTRL\_CMPSSA4\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                             |
|------|-------------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                      | NONE | 0h    | Reserved                                                |
| 2:0  | CMPSSA4_CLK_GATE_C<br>LK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding cmpssa |

### 2.7.2.55 CONTROLSS\_CTRL\_CMPSSA5\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_CMPSSA5\_CLK\_GATE Register (Offset = 1B4h) [reset = 0h]

cmpssa[x] clock gate.

Return to [Summary Table](#)

**Table 2-3341. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 01B4h       |

**Figure 2-1112. CONTROLSS\_CTRL\_CMPSSA5\_CLK\_GATE Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | CMPSSA5_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3343. CONTROLSS\_CTRL\_CMPSSA5\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                             |
|------|-------------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                      | NONE | 0h    | Reserved                                                |
| 2:0  | CMPSSA5_CLK_GATE_C<br>LK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding cmpssa |

### 2.7.2.56 CONTROLSS\_CTRL\_CMPSSA6\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_CMPSSA6\_CLK\_GATE Register (Offset = 1B8h) [reset = 0h]

cmpssa[x] clock gate.

Return to [Summary Table](#)

**Table 2-3344. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 01B8h       |

**Figure 2-1113. CONTROLSS\_CTRL\_CMPSSA6\_CLK\_GATE Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | CMPSSA6_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3346. CONTROLSS\_CTRL\_CMPSSA6\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                             |
|------|-------------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                      | NONE | 0h    | Reserved                                                |
| 2:0  | CMPSSA6_CLK_GATE_C<br>LK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding cmpssa |



## 2.7.2.57 CONTROLSS\_CTRL\_CMPSSA7\_CLK\_GATE Register

### 1 CONTROLSS\_CTRL\_CMPSSA7\_CLK\_GATE Register (Offset = 1BCh) [reset = 0h]

cmpssa[x] clock gate.

Return to [Summary Table](#)

**Table 2-3347. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 01BCh       |

**Figure 2-1114. CONTROLSS\_CTRL\_CMPSSA7\_CLK\_GATE Name Register**

|          |    |    |    |                           |    |    |    |
|----------|----|----|----|---------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                        | 26 | 25 | 24 |
| RESERVED |    |    |    |                           |    |    |    |
| NONE     |    |    |    |                           |    |    |    |
| 0h       |    |    |    |                           |    |    |    |
| 23       | 22 | 21 | 20 | 19                        | 18 | 17 | 16 |
| RESERVED |    |    |    |                           |    |    |    |
| NONE     |    |    |    |                           |    |    |    |
| 0h       |    |    |    |                           |    |    |    |
| 15       | 14 | 13 | 12 | 11                        | 10 | 9  | 8  |
| RESERVED |    |    |    |                           |    |    |    |
| NONE     |    |    |    |                           |    |    |    |
| 0h       |    |    |    |                           |    |    |    |
| 7        | 6  | 5  | 4  | 3                         | 2  | 1  | 0  |
| RESERVED |    |    |    | CMPSSA7_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                       |    |    |    |
| 0h       |    |    |    | 0h                        |    |    |    |

**Table 2-3349. CONTROLSS\_CTRL\_CMPSSA7\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                             |
|------|-------------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                      | NONE | 0h    | Reserved                                                |
| 2:0  | CMPSSA7_CLK_GATE_C<br>LK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding cmpssa |

### 2.7.2.58 CONTROLSS\_CTRL\_CMPSSA8\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_CMPSSA8\_CLK\_GATE Register (Offset = 1C0h) [reset = 0h]

cmpssa[x] clock gate.

Return to [Summary Table](#)

**Table 2-3350. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 01C0h       |

**Figure 2-1115. CONTROLSS\_CTRL\_CMPSSA8\_CLK\_GATE Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | CMPSSA8_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3352. CONTROLSS\_CTRL\_CMPSSA8\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                             |
|------|-------------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                      | NONE | 0h    | Reserved                                                |
| 2:0  | CMPSSA8_CLK_GATE_C<br>LK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding cmpssa |

### 2.7.2.59 CONTROLSS\_CTRL\_CMPSSA9\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_CMPSSA9\_CLK\_GATE Register (Offset = 1C4h) [reset = 0h]

cmpssa[x] clock gate.

Return to [Summary Table](#)

**Table 2-3353. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 01C4h       |

**Figure 2-1116. CONTROLSS\_CTRL\_CMPSSA9\_CLK\_GATE Name Register**

|          |    |    |    |                           |    |    |    |
|----------|----|----|----|---------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                        | 26 | 25 | 24 |
| RESERVED |    |    |    |                           |    |    |    |
| NONE     |    |    |    |                           |    |    |    |
| 0h       |    |    |    |                           |    |    |    |
| 23       | 22 | 21 | 20 | 19                        | 18 | 17 | 16 |
| RESERVED |    |    |    |                           |    |    |    |
| NONE     |    |    |    |                           |    |    |    |
| 0h       |    |    |    |                           |    |    |    |
| 15       | 14 | 13 | 12 | 11                        | 10 | 9  | 8  |
| RESERVED |    |    |    |                           |    |    |    |
| NONE     |    |    |    |                           |    |    |    |
| 0h       |    |    |    |                           |    |    |    |
| 7        | 6  | 5  | 4  | 3                         | 2  | 1  | 0  |
| RESERVED |    |    |    | CMPSSA9_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                       |    |    |    |
| 0h       |    |    |    | 0h                        |    |    |    |

**Table 2-3355. CONTROLSS\_CTRL\_CMPSSA9\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                             |
|------|-------------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                      | NONE | 0h    | Reserved                                                |
| 2:0  | CMPSSA9_CLK_GATE_C<br>LK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding cmpssa |

## 2.7.2.60 CONTROLSS\_CTRL\_CMPSSB0\_CLK\_GATE Register

### 1 CONTROLSS\_CTRL\_CMPSSB0\_CLK\_GATE Register (Offset = 1D0h) [reset = 0h]

cmpssb[x] clock gate.

Return to [Summary Table](#)

**Table 2-3356. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 01D0h       |

**Figure 2-1117. CONTROLSS\_CTRL\_CMPSSB0\_CLK\_GATE Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | CMPSSB0_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3358. CONTROLSS\_CTRL\_CMPSSB0\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                             |
|------|-------------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                      | NONE | 0h    | Reserved                                                |
| 2:0  | CMPSSB0_CLK_GATE_C<br>LK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding cmpssb |

## 2.7.2.61 CONTROLSS\_CTRL\_CMPSSB1\_CLK\_GATE Register

### 1 CONTROLSS\_CTRL\_CMPSSB1\_CLK\_GATE Register (Offset = 1D4h) [reset = 0h]

cmpssb[x] clock gate.

Return to [Summary Table](#)

**Table 2-3359. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 01D4h       |

**Figure 2-1118. CONTROLSS\_CTRL\_CMPSSB1\_CLK\_GATE Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | CMPSSB1_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3361. CONTROLSS\_CTRL\_CMPSSB1\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                             |
|------|-------------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                      | NONE | 0h    | Reserved                                                |
| 2:0  | CMPSSB1_CLK_GATE_C<br>LK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding cmpssb |

### 2.7.2.62 CONTROLSS\_CTRL\_CMPSSB2\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_CMPSSB2\_CLK\_GATE Register (Offset = 1D8h) [reset = 0h]

cmpssb[x] clock gate.

Return to [Summary Table](#)

**Table 2-3362. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 01D8h       |

**Figure 2-1119. CONTROLSS\_CTRL\_CMPSSB2\_CLK\_GATE Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | CMPSSB2_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3364. CONTROLSS\_CTRL\_CMPSSB2\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                             |
|------|-------------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                      | NONE | 0h    | Reserved                                                |
| 2:0  | CMPSSB2_CLK_GATE_C<br>LK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding cmpssb |

### 2.7.2.63 CONTROLSS\_CTRL\_CMPSSB3\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_CMPSSB3\_CLK\_GATE Register (Offset = 1DCh) [reset = 0h]

cmpssb[x] clock gate.

Return to [Summary Table](#)

**Table 2-3365. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 01DCh       |

**Figure 2-1120. CONTROLSS\_CTRL\_CMPSSB3\_CLK\_GATE Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | CMPSSB3_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3367. CONTROLSS\_CTRL\_CMPSSB3\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                             |
|------|-------------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                      | NONE | 0h    | Reserved                                                |
| 2:0  | CMPSSB3_CLK_GATE_C<br>LK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding cmpssb |

### 2.7.2.64 CONTROLSS\_CTRL\_CMPSSB4\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_CMPSSB4\_CLK\_GATE Register (Offset = 1E0h) [reset = 0h]

cmpssb[x] clock gate.

Return to [Summary Table](#)

**Table 2-3368. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 01E0h       |

**Figure 2-1121. CONTROLSS\_CTRL\_CMPSSB4\_CLK\_GATE Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | CMPSSB4_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3370. CONTROLSS\_CTRL\_CMPSSB4\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                             |
|------|-------------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                      | NONE | 0h    | Reserved                                                |
| 2:0  | CMPSSB4_CLK_GATE_C<br>LK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding cmpssb |



### 2.7.2.65 CONTROLSS\_CTRL\_CMPSSB5\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_CMPSSB5\_CLK\_GATE Register (Offset = 1E4h) [reset = 0h]

cmpssb[x] clock gate.

Return to [Summary Table](#)

**Table 2-3371. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 01E4h       |

**Figure 2-1122. CONTROLSS\_CTRL\_CMPSSB5\_CLK\_GATE Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | CMPSSB5_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3373. CONTROLSS\_CTRL\_CMPSSB5\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                             |
|------|-------------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                      | NONE | 0h    | Reserved                                                |
| 2:0  | CMPSSB5_CLK_GATE_C<br>LK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding cmpssb |

### 2.7.2.66 CONTROLSS\_CTRL\_CMPSSB6\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_CMPSSB6\_CLK\_GATE Register (Offset = 1E8h) [reset = 0h]

cmpssb[x] clock gate.

Return to [Summary Table](#)

**Table 2-3374. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 01E8h       |

**Figure 2-1123. CONTROLSS\_CTRL\_CMPSSB6\_CLK\_GATE Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | CMPSSB6_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3376. CONTROLSS\_CTRL\_CMPSSB6\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                             |
|------|-------------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                      | NONE | 0h    | Reserved                                                |
| 2:0  | CMPSSB6_CLK_GATE_C<br>LK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding cmpssb |

### 2.7.2.67 CONTROLSS\_CTRL\_CMPSSB7\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_CMPSSB7\_CLK\_GATE Register (Offset = 1ECh) [reset = 0h]

cmpssb[x] clock gate.

Return to [Summary Table](#)

**Table 2-3377. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 01ECh       |

**Figure 2-1124. CONTROLSS\_CTRL\_CMPSSB7\_CLK\_GATE Name Register**

|          |    |    |    |                           |    |    |    |
|----------|----|----|----|---------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                        | 26 | 25 | 24 |
| RESERVED |    |    |    |                           |    |    |    |
| NONE     |    |    |    |                           |    |    |    |
| 0h       |    |    |    |                           |    |    |    |
| 23       | 22 | 21 | 20 | 19                        | 18 | 17 | 16 |
| RESERVED |    |    |    |                           |    |    |    |
| NONE     |    |    |    |                           |    |    |    |
| 0h       |    |    |    |                           |    |    |    |
| 15       | 14 | 13 | 12 | 11                        | 10 | 9  | 8  |
| RESERVED |    |    |    |                           |    |    |    |
| NONE     |    |    |    |                           |    |    |    |
| 0h       |    |    |    |                           |    |    |    |
| 7        | 6  | 5  | 4  | 3                         | 2  | 1  | 0  |
| RESERVED |    |    |    | CMPSSB7_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                       |    |    |    |
| 0h       |    |    |    | 0h                        |    |    |    |

**Table 2-3379. CONTROLSS\_CTRL\_CMPSSB7\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                             |
|------|-------------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                      | NONE | 0h    | Reserved                                                |
| 2:0  | CMPSSB7_CLK_GATE_C<br>LK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding cmpssb |

## 2.7.2.68 CONTROLSS\_CTRL\_CMPSSB8\_CLK\_GATE Register

### 1 CONTROLSS\_CTRL\_CMPSSB8\_CLK\_GATE Register (Offset = 1F0h) [reset = 0h]

cmpssb[x] clock gate.

Return to [Summary Table](#)

**Table 2-3380. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 01F0h       |

**Figure 2-1125. CONTROLSS\_CTRL\_CMPSSB8\_CLK\_GATE Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | CMPSSB8_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3382. CONTROLSS\_CTRL\_CMPSSB8\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                             |
|------|-------------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                      | NONE | 0h    | Reserved                                                |
| 2:0  | CMPSSB8_CLK_GATE_C<br>LK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding cmpssb |

### 2.7.2.69 CONTROLSS\_CTRL\_CMPSSB9\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_CMPSSB9\_CLK\_GATE Register (Offset = 1F4h) [reset = 0h]

cmpssb[x] clock gate.

Return to [Summary Table](#)

**Table 2-3383. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 01F4h       |

**Figure 2-1126. CONTROLSS\_CTRL\_CMPSSB9\_CLK\_GATE Name Register**

|          |    |    |    |    |                           |    |    |
|----------|----|----|----|----|---------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                        | 25 | 24 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                        | 17 | 16 |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                        | 9  | 8  |
| RESERVED |    |    |    |    |                           |    |    |
| NONE     |    |    |    |    |                           |    |    |
| 0h       |    |    |    |    |                           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                         | 1  | 0  |
| RESERVED |    |    |    |    | CMPSSB9_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                       |    |    |
| 0h       |    |    |    |    | 0h                        |    |    |

**Table 2-3385. CONTROLSS\_CTRL\_CMPSSB9\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                             |
|------|-------------------------------|------|-------|---------------------------------------------------------|
| 31:3 | RESERVED                      | NONE | 0h    | Reserved                                                |
| 2:0  | CMPSSB9_CLK_GATE_C<br>LK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding cmpssb |

### 2.7.2.70 CONTROLSS\_CTRL\_ECAP0\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_ECAP0\_CLK\_GATE Register (Offset = 200h) [reset = 0h]

Ecap[x] clock gate.

Return to [Summary Table](#)

**Table 2-3386. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0200h       |

**Figure 2-1127. CONTROLSS\_CTRL\_ECAP0\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | ECAP0_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-3388. CONTROLSS\_CTRL\_ECAP0\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | ECAP0_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding ecap |

### 2.7.2.71 CONTROLSS\_CTRL\_ECAP1\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_ECAP1\_CLK\_GATE Register (Offset = 204h) [reset = 0h]

Ecap[x] clock gate.

Return to [Summary Table](#)

**Table 2-3389. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0204h       |

**Figure 2-1128. CONTROLSS\_CTRL\_ECAP1\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | ECAP1_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-3391. CONTROLSS\_CTRL\_ECAP1\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | ECAP1_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding ecap |

### 2.7.2.72 CONTROLSS\_CTRL\_ECAP2\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_ECAP2\_CLK\_GATE Register (Offset = 208h) [reset = 0h]

Ecap[x] clock gate.

Return to [Summary Table](#)

**Table 2-3392. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0208h       |

**Figure 2-1129. CONTROLSS\_CTRL\_ECAP2\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | ECAP2_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-3394. CONTROLSS\_CTRL\_ECAP2\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | ECAP2_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding ecap |



### 2.7.2.73 CONTROLSS\_CTRL\_ECAP3\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_ECAP3\_CLK\_GATE Register (Offset = 20Ch) [reset = 0h]

Ecap[x] clock gate.

Return to [Summary Table](#)

**Table 2-3395. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 020Ch       |

**Figure 2-1130. CONTROLSS\_CTRL\_ECAP3\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | ECAP3_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-3397. CONTROLSS\_CTRL\_ECAP3\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | ECAP3_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding ecap |

### 2.7.2.74 CONTROLSS\_CTRL\_ECAP4\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_ECAP4\_CLK\_GATE Register (Offset = 210h) [reset = 0h]

Ecap[x] clock gate.

Return to [Summary Table](#)

**Table 2-3398. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0210h       |

**Figure 2-1131. CONTROLSS\_CTRL\_ECAP4\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | ECAP4_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-3400. CONTROLSS\_CTRL\_ECAP4\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | ECAP4_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding ecap |

### 2.7.2.75 CONTROLSS\_CTRL\_ECAP5\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_ECAP5\_CLK\_GATE Register (Offset = 214h) [reset = 0h]

Ecap[x] clock gate.

Return to [Summary Table](#)

**Table 2-3401. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0214h       |

**Figure 2-1132. CONTROLSS\_CTRL\_ECAP5\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | ECAP5_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-3403. CONTROLSS\_CTRL\_ECAP5\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | ECAP5_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding ecap |

## 2.7.2.76 CONTROLSS\_CTRL\_ECAP6\_CLK\_GATE Register

### 1 CONTROLSS\_CTRL\_ECAP6\_CLK\_GATE Register (Offset = 218h) [reset = 0h]

Ecap[x] clock gate.

Return to [Summary Table](#)

**Table 2-3404. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0218h       |

**Figure 2-1133. CONTROLSS\_CTRL\_ECAP6\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | ECAP6_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-3406. CONTROLSS\_CTRL\_ECAP6\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | ECAP6_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding ecap |

### 2.7.2.77 CONTROLSS\_CTRL\_ECAP7\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_ECAP7\_CLK\_GATE Register (Offset = 21Ch) [reset = 0h]

Ecap[x] clock gate.

Return to [Summary Table](#)

**Table 2-3407. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 021Ch       |

**Figure 2-1134. CONTROLSS\_CTRL\_ECAP7\_CLK\_GATE Name Register**

|          |    |    |    |    |                         |    |    |
|----------|----|----|----|----|-------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                      | 25 | 24 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                      | 17 | 16 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                      | 9  | 8  |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                       | 1  | 0  |
| RESERVED |    |    |    |    | ECAP7_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                     |    |    |
| 0h       |    |    |    |    | 0h                      |    |    |

**Table 2-3409. CONTROLSS\_CTRL\_ECAP7\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | ECAP7_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding ecap |

### 2.7.2.78 CONTROLSS\_CTRL\_ECAP8\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_ECAP8\_CLK\_GATE Register (Offset = 220h) [reset = 0h]

Ecap[x] clock gate.

Return to [Summary Table](#)

**Table 2-3410. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0220h       |

**Figure 2-1135. CONTROLSS\_CTRL\_ECAP8\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | ECAP8_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-3412. CONTROLSS\_CTRL\_ECAP8\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | ECAP8_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding ecap |

### 2.7.2.79 CONTROLSS\_CTRL\_ECAP9\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_ECAP9\_CLK\_GATE Register (Offset = 224h) [reset = 0h]

Ecap[x] clock gate.

Return to [Summary Table](#)

**Table 2-3413. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0224h       |

**Figure 2-1136. CONTROLSS\_CTRL\_ECAP9\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | ECAP9_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-3415. CONTROLSS\_CTRL\_ECAP9\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | ECAP9_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding ecap |

### 2.7.2.80 CONTROLSS\_CTRL\_EQEP0\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EQEP0\_CLK\_GATE Register (Offset = 240h) [reset = 0h]

Eqep[x] clock gate.

Return to [Summary Table](#)

**Table 2-3416. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0240h       |

**Figure 2-1137. CONTROLSS\_CTRL\_EQEP0\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | EQEP0_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-3418. CONTROLSS\_CTRL\_EQEP0\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | EQEP0_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding eqep |



### 2.7.2.81 CONTROLSS\_CTRL\_EQEP1\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EQEP1\_CLK\_GATE Register (Offset = 244h) [reset = 0h]

Eqep[x] clock gate.

Return to [Summary Table](#)

**Table 2-3419. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0244h       |

**Figure 2-1138. CONTROLSS\_CTRL\_EQEP1\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | EQEP1_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-3421. CONTROLSS\_CTRL\_EQEP1\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | EQEP1_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding eqep |

### 2.7.2.82 CONTROLSS\_CTRL\_EQEP2\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_EQEP2\_CLK\_GATE Register (Offset = 248h) [reset = 0h]

Eqep[x] clock gate.

Return to [Summary Table](#)

**Table 2-3422. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0248h       |

**Figure 2-1139. CONTROLSS\_CTRL\_EQEP2\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | EQEP2_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-3424. CONTROLSS\_CTRL\_EQEP2\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | EQEP2_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding eqep |

### 2.7.2.83 CONTROLSS\_CTRL\_SDFM0\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_SDFM0\_CLK\_GATE Register (Offset = 250h) [reset = 0h]

Sdfm[x] clock gate.

Return to [Summary Table](#)

**Table 2-3425. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0250h       |

**Figure 2-1140. CONTROLSS\_CTRL\_SDFM0\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | SDFM0_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-3427. CONTROLSS\_CTRL\_SDFM0\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | SDFM0_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding sdfm |

### 2.7.2.84 CONTROLSS\_CTRL\_SDFM1\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_SDFM1\_CLK\_GATE Register (Offset = 254h) [reset = 0h]

Sdfm[x] clock gate.

Return to [Summary Table](#)

**Table 2-3428. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0254h       |

**Figure 2-1141. CONTROLSS\_CTRL\_SDFM1\_CLK\_GATE Name Register**

|          |    |    |    |    |                         |    |    |
|----------|----|----|----|----|-------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                      | 25 | 24 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                      | 17 | 16 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                      | 9  | 8  |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                       | 1  | 0  |
| RESERVED |    |    |    |    | SDFM1_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                     |    |    |
| 0h       |    |    |    |    | 0h                      |    |    |

**Table 2-3430. CONTROLSS\_CTRL\_SDFM1\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | SDFM1_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding sdfm |

### 2.7.2.85 CONTROLSS\_CTRL\_DAC\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_DAC\_CLK\_GATE Register (Offset = 258h) [reset = 0h]

dac clock gate.

Return to [Summary Table](#)

**Table 2-3431. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0258h       |

**Figure 2-1142. CONTROLSS\_CTRL\_DAC\_CLK\_GATE Name Register**

|          |    |    |    |    |                       |    |    |
|----------|----|----|----|----|-----------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                    | 25 | 24 |
| RESERVED |    |    |    |    |                       |    |    |
| NONE     |    |    |    |    |                       |    |    |
| 0h       |    |    |    |    |                       |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                    | 17 | 16 |
| RESERVED |    |    |    |    |                       |    |    |
| NONE     |    |    |    |    |                       |    |    |
| 0h       |    |    |    |    |                       |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                    | 9  | 8  |
| RESERVED |    |    |    |    |                       |    |    |
| NONE     |    |    |    |    |                       |    |    |
| 0h       |    |    |    |    |                       |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                     | 1  | 0  |
| RESERVED |    |    |    |    | DAC_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                   |    |    |
| 0h       |    |    |    |    | 0h                    |    |    |

**Table 2-3433. CONTROLSS\_CTRL\_DAC\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                            |
|------|-----------------------|------|-------|----------------------------------------|
| 31:3 | RESERVED              | NONE | 0h    | Reserved                               |
| 2:0  | DAC_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for dac |

### 2.7.2.86 CONTROLSS\_CTRL\_ADC0\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_ADC0\_CLK\_GATE Register (Offset = 25Ch) [reset = 0h]

Adc[x] clock gate.

Return to [Summary Table](#)

**Table 2-3434. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 025Ch       |

**Figure 2-1143. CONTROLSS\_CTRL\_ADC0\_CLK\_GATE Name Register**

|          |    |    |    |                        |    |    |    |
|----------|----|----|----|------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                     | 26 | 25 | 24 |
| RESERVED |    |    |    |                        |    |    |    |
| NONE     |    |    |    |                        |    |    |    |
| 0h       |    |    |    |                        |    |    |    |
| 23       | 22 | 21 | 20 | 19                     | 18 | 17 | 16 |
| RESERVED |    |    |    |                        |    |    |    |
| NONE     |    |    |    |                        |    |    |    |
| 0h       |    |    |    |                        |    |    |    |
| 15       | 14 | 13 | 12 | 11                     | 10 | 9  | 8  |
| RESERVED |    |    |    |                        |    |    |    |
| NONE     |    |    |    |                        |    |    |    |
| 0h       |    |    |    |                        |    |    |    |
| 7        | 6  | 5  | 4  | 3                      | 2  | 1  | 0  |
| RESERVED |    |    |    | ADC0_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                    |    |    |    |
| 0h       |    |    |    | 0h                     |    |    |    |

**Table 2-3436. CONTROLSS\_CTRL\_ADC0\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                          |
|------|------------------------|------|-------|------------------------------------------------------|
| 31:3 | RESERVED               | NONE | 0h    | Reserved                                             |
| 2:0  | ADC0_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding adc |

### 2.7.2.87 CONTROLSS\_CTRL\_ADC1\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_ADC1\_CLK\_GATE Register (Offset = 260h) [reset = 0h]

Adc[x] clock gate.

Return to [Summary Table](#)

**Table 2-3437. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0260h       |

**Figure 2-1144. CONTROLSS\_CTRL\_ADC1\_CLK\_GATE Name Register**

|          |    |    |    |    |                        |    |    |
|----------|----|----|----|----|------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                     | 25 | 24 |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                     | 17 | 16 |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                     | 9  | 8  |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                      | 1  | 0  |
| RESERVED |    |    |    |    | ADC1_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                    |    |    |
| 0h       |    |    |    |    | 0h                     |    |    |

**Table 2-3439. CONTROLSS\_CTRL\_ADC1\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                          |
|------|------------------------|------|-------|------------------------------------------------------|
| 31:3 | RESERVED               | NONE | 0h    | Reserved                                             |
| 2:0  | ADC1_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding adc |

## 2.7.2.88 CONTROLSS\_CTRL\_ADC2\_CLK\_GATE Register

### 1 CONTROLSS\_CTRL\_ADC2\_CLK\_GATE Register (Offset = 264h) [reset = 0h]

Adc[x] clock gate.

Return to [Summary Table](#)

**Table 2-3440. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0264h       |

**Figure 2-1145. CONTROLSS\_CTRL\_ADC2\_CLK\_GATE Name Register**

|          |    |    |    |                        |    |    |    |
|----------|----|----|----|------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                     | 26 | 25 | 24 |
| RESERVED |    |    |    |                        |    |    |    |
| NONE     |    |    |    |                        |    |    |    |
| 0h       |    |    |    |                        |    |    |    |
| 23       | 22 | 21 | 20 | 19                     | 18 | 17 | 16 |
| RESERVED |    |    |    |                        |    |    |    |
| NONE     |    |    |    |                        |    |    |    |
| 0h       |    |    |    |                        |    |    |    |
| 15       | 14 | 13 | 12 | 11                     | 10 | 9  | 8  |
| RESERVED |    |    |    |                        |    |    |    |
| NONE     |    |    |    |                        |    |    |    |
| 0h       |    |    |    |                        |    |    |    |
| 7        | 6  | 5  | 4  | 3                      | 2  | 1  | 0  |
| RESERVED |    |    |    | ADC2_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                    |    |    |    |
| 0h       |    |    |    | 0h                     |    |    |    |

**Table 2-3442. CONTROLSS\_CTRL\_ADC2\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                          |
|------|------------------------|------|-------|------------------------------------------------------|
| 31:3 | RESERVED               | NONE | 0h    | Reserved                                             |
| 2:0  | ADC2_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding adc |



### 2.7.2.89 CONTROLSS\_CTRL\_ADC3\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_ADC3\_CLK\_GATE Register (Offset = 268h) [reset = 0h]

Adc[x] clock gate.

Return to [Summary Table](#)

**Table 2-3443. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0268h       |

**Figure 2-1146. CONTROLSS\_CTRL\_ADC3\_CLK\_GATE Name Register**

|          |    |    |    |    |                        |    |    |
|----------|----|----|----|----|------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                     | 25 | 24 |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                     | 17 | 16 |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                     | 9  | 8  |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                      | 1  | 0  |
| RESERVED |    |    |    |    | ADC3_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                    |    |    |
| 0h       |    |    |    |    | 0h                     |    |    |

**Table 2-3445. CONTROLSS\_CTRL\_ADC3\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                          |
|------|------------------------|------|-------|------------------------------------------------------|
| 31:3 | RESERVED               | NONE | 0h    | Reserved                                             |
| 2:0  | ADC3_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding adc |

## 2.7.2.90 CONTROLSS\_CTRL\_ADC4\_CLK\_GATE Register

### 1 CONTROLSS\_CTRL\_ADC4\_CLK\_GATE Register (Offset = 26Ch) [reset = 0h]

Adc[x] clock gate.

Return to [Summary Table](#)

**Table 2-3446. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 026Ch       |

**Figure 2-1147. CONTROLSS\_CTRL\_ADC4\_CLK\_GATE Name Register**

|          |    |    |    |    |                        |    |    |
|----------|----|----|----|----|------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                     | 25 | 24 |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                     | 17 | 16 |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                     | 9  | 8  |
| RESERVED |    |    |    |    |                        |    |    |
| NONE     |    |    |    |    |                        |    |    |
| 0h       |    |    |    |    |                        |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                      | 1  | 0  |
| RESERVED |    |    |    |    | ADC4_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                    |    |    |
| 0h       |    |    |    |    | 0h                     |    |    |

**Table 2-3448. CONTROLSS\_CTRL\_ADC4\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                          |
|------|------------------------|------|-------|------------------------------------------------------|
| 31:3 | RESERVED               | NONE | 0h    | Reserved                                             |
| 2:0  | ADC4_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding adc |

### 2.7.2.91 CONTROLSS\_CTRL\_OTTO0\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_OTTO0\_CLK\_GATE Register (Offset = 270h) [reset = 0h]

Otto[x] clock gate.

Return to [Summary Table](#)

**Table 2-3449. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0270h       |

**Figure 2-1148. CONTROLSS\_CTRL\_OTTO0\_CLK\_GATE Name Register**

|          |    |    |    |    |                         |    |    |
|----------|----|----|----|----|-------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                      | 25 | 24 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                      | 17 | 16 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                      | 9  | 8  |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                       | 1  | 0  |
| RESERVED |    |    |    |    | OTTO0_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                     |    |    |
| 0h       |    |    |    |    | 0h                      |    |    |

**Table 2-3451. CONTROLSS\_CTRL\_OTTO0\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | OTTO0_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding otto |

### 2.7.2.92 CONTROLSS\_CTRL\_OTTO1\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_OTTO1\_CLK\_GATE Register (Offset = 274h) [reset = 0h]

Otto[x] clock gate.

Return to [Summary Table](#)

**Table 2-3452. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0274h       |

**Figure 2-1149. CONTROLSS\_CTRL\_OTTO1\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | OTTO1_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-3454. CONTROLSS\_CTRL\_OTTO1\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | OTTO1_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding otto |

### 2.7.2.93 CONTROLSS\_CTRL\_OTTO2\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_OTTO2\_CLK\_GATE Register (Offset = 278h) [reset = 0h]

Otto[x] clock gate.

Return to [Summary Table](#)

**Table 2-3455. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0278h       |

**Figure 2-1150. CONTROLSS\_CTRL\_OTTO2\_CLK\_GATE Name Register**

|          |    |    |    |                         |    |    |    |
|----------|----|----|----|-------------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                      | 26 | 25 | 24 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 23       | 22 | 21 | 20 | 19                      | 18 | 17 | 16 |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 15       | 14 | 13 | 12 | 11                      | 10 | 9  | 8  |
| RESERVED |    |    |    |                         |    |    |    |
| NONE     |    |    |    |                         |    |    |    |
| 0h       |    |    |    |                         |    |    |    |
| 7        | 6  | 5  | 4  | 3                       | 2  | 1  | 0  |
| RESERVED |    |    |    | OTTO2_CLK_GATE_CLK_GATE |    |    |    |
| NONE     |    |    |    | R/W                     |    |    |    |
| 0h       |    |    |    | 0h                      |    |    |    |

**Table 2-3457. CONTROLSS\_CTRL\_OTTO2\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | OTTO2_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding otto |

### 2.7.2.94 CONTROLSS\_CTRL\_OTTO3\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_OTTO3\_CLK\_GATE Register (Offset = 27Ch) [reset = 0h]

Otto[x] clock gate.

Return to [Summary Table](#)

**Table 2-3458. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 027Ch       |

**Figure 2-1151. CONTROLSS\_CTRL\_OTTO3\_CLK\_GATE Name Register**

|          |    |    |    |    |                         |    |    |
|----------|----|----|----|----|-------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                      | 25 | 24 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                      | 17 | 16 |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                      | 9  | 8  |
| RESERVED |    |    |    |    |                         |    |    |
| NONE     |    |    |    |    |                         |    |    |
| 0h       |    |    |    |    |                         |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                       | 1  | 0  |
| RESERVED |    |    |    |    | OTTO3_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                     |    |    |
| 0h       |    |    |    |    | 0h                      |    |    |

**Table 2-3460. CONTROLSS\_CTRL\_OTTO3\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                           |
|------|-------------------------|------|-------|-------------------------------------------------------|
| 31:3 | RESERVED                | NONE | 0h    | Reserved                                              |
| 2:0  | OTTO3_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding otto |

## 2.7.2.95 CONTROLSS\_CTRL\_SDFM0\_PLL\_CLK\_GATE Register

### 1 CONTROLSS\_CTRL\_SDFM0\_PLL\_CLK\_GATE Register (Offset = 280h) [reset = 0h]

Sdfm[x]\_pll clock gate.

Return to [Summary Table](#)

**Table 2-3461. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0280h       |

**Figure 2-1152. CONTROLSS\_CTRL\_SDFM0\_PLL\_CLK\_GATE Name Register**

|          |    |    |    |    |                             |    |    |
|----------|----|----|----|----|-----------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                          | 25 | 24 |
| RESERVED |    |    |    |    |                             |    |    |
| NONE     |    |    |    |    |                             |    |    |
| 0h       |    |    |    |    |                             |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                          | 17 | 16 |
| RESERVED |    |    |    |    |                             |    |    |
| NONE     |    |    |    |    |                             |    |    |
| 0h       |    |    |    |    |                             |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                          | 9  | 8  |
| RESERVED |    |    |    |    |                             |    |    |
| NONE     |    |    |    |    |                             |    |    |
| 0h       |    |    |    |    |                             |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                           | 1  | 0  |
| RESERVED |    |    |    |    | SDFM0_PLL_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                         |    |    |
| 0h       |    |    |    |    | 0h                          |    |    |

**Table 2-3463. CONTROLSS\_CTRL\_SDFM0\_PLL\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                       | Type | Reset | Description                                                     |
|------|-----------------------------|------|-------|-----------------------------------------------------------------|
| 31:3 | RESERVED                    | NONE | 0h    | Reserved                                                        |
| 2:0  | SDFM0_PLL_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding sdfm pll clock |

## 2.7.2.96 CONTROLSS\_CTRL\_SDFM1\_PLL\_CLK\_GATE Register

### 1 CONTROLSS\_CTRL\_SDFM1\_PLL\_CLK\_GATE Register (Offset = 284h) [reset = 0h]

Sdfm[x]\_pll clock gate.

Return to [Summary Table](#)

**Table 2-3464. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0284h       |

**Figure 2-1153. CONTROLSS\_CTRL\_SDFM1\_PLL\_CLK\_GATE Name Register**

|          |    |    |    |    |                             |    |    |
|----------|----|----|----|----|-----------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                          | 25 | 24 |
| RESERVED |    |    |    |    |                             |    |    |
| NONE     |    |    |    |    |                             |    |    |
| 0h       |    |    |    |    |                             |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                          | 17 | 16 |
| RESERVED |    |    |    |    |                             |    |    |
| NONE     |    |    |    |    |                             |    |    |
| 0h       |    |    |    |    |                             |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                          | 9  | 8  |
| RESERVED |    |    |    |    |                             |    |    |
| NONE     |    |    |    |    |                             |    |    |
| 0h       |    |    |    |    |                             |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                           | 1  | 0  |
| RESERVED |    |    |    |    | SDFM1_PLL_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                         |    |    |
| 0h       |    |    |    |    | 0h                          |    |    |

**Table 2-3466. CONTROLSS\_CTRL\_SDFM1\_PLL\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                       | Type | Reset | Description                                                     |
|------|-----------------------------|------|-------|-----------------------------------------------------------------|
| 31:3 | RESERVED                    | NONE | 0h    | Reserved                                                        |
| 2:0  | SDFM1_PLL_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding sdfm pll clock |



### 2.7.2.97 CONTROLSS\_CTRL\_FSI\_TX0\_PLL\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_FSI\_TX0\_PLL\_CLK\_GATE Register (Offset = 288h) [reset = 0h]

fsi\_tx[x]\_pll clock gate.

Return to [Summary Table](#)

**Table 2-3467. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0288h       |

**Figure 2-1154. CONTROLSS\_CTRL\_FSI\_TX0\_PLL\_CLK\_GATE Name Register**

|          |    |    |    |    |                               |    |    |
|----------|----|----|----|----|-------------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                            | 25 | 24 |
| RESERVED |    |    |    |    |                               |    |    |
| NONE     |    |    |    |    |                               |    |    |
| 0h       |    |    |    |    |                               |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                            | 17 | 16 |
| RESERVED |    |    |    |    |                               |    |    |
| NONE     |    |    |    |    |                               |    |    |
| 0h       |    |    |    |    |                               |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                            | 9  | 8  |
| RESERVED |    |    |    |    |                               |    |    |
| NONE     |    |    |    |    |                               |    |    |
| 0h       |    |    |    |    |                               |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                             | 1  | 0  |
| RESERVED |    |    |    |    | FSI_TX0_PLL_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                           |    |    |
| 0h       |    |    |    |    | 0h                            |    |    |

**Table 2-3469. CONTROLSS\_CTRL\_FSI\_TX0\_PLL\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                                       |
|------|-------------------------------|------|-------|-------------------------------------------------------------------|
| 31:3 | RESERVED                      | NONE | 0h    | Reserved                                                          |
| 2:0  | FSI_TX0_PLL_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding fsi rx pll clock |

### 2.7.2.98 CONTROLSS\_CTRL\_FSI\_TX1\_PLL\_CLK\_GATE Register

#### 1 CONTROLSS\_CTRL\_FSI\_TX1\_PLL\_CLK\_GATE Register (Offset = 28Ch) [reset = 0h]

fsi\_tx[x]\_pll clock gate.

Return to [Summary Table](#)

**Table 2-3470. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 028Ch       |

**Figure 2-1155. CONTROLSS\_CTRL\_FSI\_TX1\_PLL\_CLK\_GATE Name Register**

|          |    |    |    |    |                               |    |    |
|----------|----|----|----|----|-------------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                            | 25 | 24 |
| RESERVED |    |    |    |    |                               |    |    |
| NONE     |    |    |    |    |                               |    |    |
| 0h       |    |    |    |    |                               |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                            | 17 | 16 |
| RESERVED |    |    |    |    |                               |    |    |
| NONE     |    |    |    |    |                               |    |    |
| 0h       |    |    |    |    |                               |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                            | 9  | 8  |
| RESERVED |    |    |    |    |                               |    |    |
| NONE     |    |    |    |    |                               |    |    |
| 0h       |    |    |    |    |                               |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                             | 1  | 0  |
| RESERVED |    |    |    |    | FSI_TX1_PLL_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                           |    |    |
| 0h       |    |    |    |    | 0h                            |    |    |

**Table 2-3472. CONTROLSS\_CTRL\_FSI\_TX1\_PLL\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                                       |
|------|-------------------------------|------|-------|-------------------------------------------------------------------|
| 31:3 | RESERVED                      | NONE | 0h    | Reserved                                                          |
| 2:0  | FSI_TX1_PLL_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding fsi rx pll clock |

## 2.7.2.99 CONTROLSS\_CTRL\_FSI\_TX2\_PLL\_CLK\_GATE Register

### 1 CONTROLSS\_CTRL\_FSI\_TX2\_PLL\_CLK\_GATE Register (Offset = 290h) [reset = 0h]

fsi\_tx[x]\_pll clock gate.

Return to [Summary Table](#)

**Table 2-3473. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0290h       |

**Figure 2-1156. CONTROLSS\_CTRL\_FSI\_TX2\_PLL\_CLK\_GATE Name Register**

|          |    |    |    |    |                               |    |    |
|----------|----|----|----|----|-------------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                            | 25 | 24 |
| RESERVED |    |    |    |    |                               |    |    |
| NONE     |    |    |    |    |                               |    |    |
| 0h       |    |    |    |    |                               |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                            | 17 | 16 |
| RESERVED |    |    |    |    |                               |    |    |
| NONE     |    |    |    |    |                               |    |    |
| 0h       |    |    |    |    |                               |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                            | 9  | 8  |
| RESERVED |    |    |    |    |                               |    |    |
| NONE     |    |    |    |    |                               |    |    |
| 0h       |    |    |    |    |                               |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                             | 1  | 0  |
| RESERVED |    |    |    |    | FSI_TX2_PLL_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                           |    |    |
| 0h       |    |    |    |    | 0h                            |    |    |

**Table 2-3475. CONTROLSS\_CTRL\_FSI\_TX2\_PLL\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                                       |
|------|-------------------------------|------|-------|-------------------------------------------------------------------|
| 31:3 | RESERVED                      | NONE | 0h    | Reserved                                                          |
| 2:0  | FSI_TX2_PLL_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding fsi rx pll clock |

## 2.7.2.100 CONTROLSS\_CTRL\_FSI\_TX3\_PLL\_CLK\_GATE Register

### 1 CONTROLSS\_CTRL\_FSI\_TX3\_PLL\_CLK\_GATE Register (Offset = 294h) [reset = 0h]

fsi\_tx[x]\_pll clock gate.

Return to [Summary Table](#)

**Table 2-3476. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0294h       |

**Figure 2-1157. CONTROLSS\_CTRL\_FSI\_TX3\_PLL\_CLK\_GATE Name Register**

|          |    |    |    |    |                               |    |    |
|----------|----|----|----|----|-------------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                            | 25 | 24 |
| RESERVED |    |    |    |    |                               |    |    |
| NONE     |    |    |    |    |                               |    |    |
| 0h       |    |    |    |    |                               |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                            | 17 | 16 |
| RESERVED |    |    |    |    |                               |    |    |
| NONE     |    |    |    |    |                               |    |    |
| 0h       |    |    |    |    |                               |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                            | 9  | 8  |
| RESERVED |    |    |    |    |                               |    |    |
| NONE     |    |    |    |    |                               |    |    |
| 0h       |    |    |    |    |                               |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                             | 1  | 0  |
| RESERVED |    |    |    |    | FSI_TX3_PLL_CLK_GATE_CLK_GATE |    |    |
| NONE     |    |    |    |    | R/W                           |    |    |
| 0h       |    |    |    |    | 0h                            |    |    |

**Table 2-3478. CONTROLSS\_CTRL\_FSI\_TX3\_PLL\_CLK\_GATE Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                                       |
|------|-------------------------------|------|-------|-------------------------------------------------------------------|
| 31:3 | RESERVED                      | NONE | 0h    | Reserved                                                          |
| 2:0  | FSI_TX3_PLL_CLK_GATE_CLK_GATE | R/W  | 0h    | Writing 3'b111 will gate clock for corresponding fsi rx pll clock |

### 2.7.2.101 CONTROLSS\_CTRL\_EPWM0\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM0\_RST Register (Offset = 300h) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3479. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0300h       |

**Figure 2-1158. CONTROLSS\_CTRL\_EPWM0\_RST Name Register**

|          |    |    |    |               |    |    |    |
|----------|----|----|----|---------------|----|----|----|
| 31       | 30 | 29 | 28 | 27            | 26 | 25 | 24 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 23       | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 15       | 14 | 13 | 12 | 11            | 10 | 9  | 8  |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 7        | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM0_RST_RST |    |    |    |
| NONE     |    |    |    | R/W           |    |    |    |
| 0h       |    |    |    | 0h            |    |    |    |

**Table 2-3481. CONTROLSS\_CTRL\_EPWM0\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM0_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

### 2.7.2.102 CONTROLSS\_CTRL\_EPWM1\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM1\_RST Register (Offset = 304h) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3482. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0304h       |

**Figure 2-1159. CONTROLSS\_CTRL\_EPWM1\_RST Name Register**

|          |    |    |    |               |    |    |    |
|----------|----|----|----|---------------|----|----|----|
| 31       | 30 | 29 | 28 | 27            | 26 | 25 | 24 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 23       | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 15       | 14 | 13 | 12 | 11            | 10 | 9  | 8  |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 7        | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM1_RST_RST |    |    |    |
| NONE     |    |    |    | R/W           |    |    |    |
| 0h       |    |    |    | 0h            |    |    |    |

**Table 2-3484. CONTROLSS\_CTRL\_EPWM1\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM1_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

### 2.7.2.103 CONTROLSS\_CTRL\_EPWM2\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM2\_RST Register (Offset = 308h) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3485. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0308h       |

**Figure 2-1160. CONTROLSS\_CTRL\_EPWM2\_RST Name Register**

|          |    |    |    |    |               |    |    |
|----------|----|----|----|----|---------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26            | 25 | 24 |
| RESERVED |    |    |    |    |               |    |    |
| NONE     |    |    |    |    |               |    |    |
| 0h       |    |    |    |    |               |    |    |
| 23       | 22 | 21 | 20 | 19 | 18            | 17 | 16 |
| RESERVED |    |    |    |    |               |    |    |
| NONE     |    |    |    |    |               |    |    |
| 0h       |    |    |    |    |               |    |    |
| 15       | 14 | 13 | 12 | 11 | 10            | 9  | 8  |
| RESERVED |    |    |    |    |               |    |    |
| NONE     |    |    |    |    |               |    |    |
| 0h       |    |    |    |    |               |    |    |
| 7        | 6  | 5  | 4  | 3  | 2             | 1  | 0  |
| RESERVED |    |    |    |    | EPWM2_RST_RST |    |    |
| NONE     |    |    |    |    | R/W           |    |    |
| 0h       |    |    |    |    | 0h            |    |    |

**Table 2-3487. CONTROLSS\_CTRL\_EPWM2\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM2_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

### 2.7.2.104 CONTROLSS\_CTRL\_EPWM3\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM3\_RST Register (Offset = 30Ch) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3488. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 030Ch       |

**Figure 2-1161. CONTROLSS\_CTRL\_EPWM3\_RST Name Register**

|          |    |    |    |               |    |    |    |
|----------|----|----|----|---------------|----|----|----|
| 31       | 30 | 29 | 28 | 27            | 26 | 25 | 24 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 23       | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 15       | 14 | 13 | 12 | 11            | 10 | 9  | 8  |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 7        | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM3_RST_RST |    |    |    |
| NONE     |    |    |    | R/W           |    |    |    |
| 0h       |    |    |    | 0h            |    |    |    |

**Table 2-3490. CONTROLSS\_CTRL\_EPWM3\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM3_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |



### 2.7.2.105 CONTROLSS\_CTRL\_EPWM4\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM4\_RST Register (Offset = 310h) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3491. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0310h       |

**Figure 2-1162. CONTROLSS\_CTRL\_EPWM4\_RST Name Register**

|          |    |    |    |               |    |    |    |
|----------|----|----|----|---------------|----|----|----|
| 31       | 30 | 29 | 28 | 27            | 26 | 25 | 24 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 23       | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 15       | 14 | 13 | 12 | 11            | 10 | 9  | 8  |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 7        | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM4_RST_RST |    |    |    |
| NONE     |    |    |    | R/W           |    |    |    |
| 0h       |    |    |    | 0h            |    |    |    |

**Table 2-3493. CONTROLSS\_CTRL\_EPWM4\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM4_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

### 2.7.2.106 CONTROLSS\_CTRL\_EPWM5\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM5\_RST Register (Offset = 314h) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3494. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0314h       |

**Figure 2-1163. CONTROLSS\_CTRL\_EPWM5\_RST Name Register**

|          |    |    |    |               |    |    |    |
|----------|----|----|----|---------------|----|----|----|
| 31       | 30 | 29 | 28 | 27            | 26 | 25 | 24 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 23       | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 15       | 14 | 13 | 12 | 11            | 10 | 9  | 8  |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 7        | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM5_RST_RST |    |    |    |
| NONE     |    |    |    | R/W           |    |    |    |
| 0h       |    |    |    | 0h            |    |    |    |

**Table 2-3496. CONTROLSS\_CTRL\_EPWM5\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM5_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

### 2.7.2.107 CONTROLSS\_CTRL\_EPWM6\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM6\_RST Register (Offset = 318h) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3497. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0318h       |

**Figure 2-1164. CONTROLSS\_CTRL\_EPWM6\_RST Name Register**

|          |    |    |    |               |    |    |    |
|----------|----|----|----|---------------|----|----|----|
| 31       | 30 | 29 | 28 | 27            | 26 | 25 | 24 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 23       | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 15       | 14 | 13 | 12 | 11            | 10 | 9  | 8  |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 7        | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM6_RST_RST |    |    |    |
| NONE     |    |    |    | R/W           |    |    |    |
| 0h       |    |    |    | 0h            |    |    |    |

**Table 2-3499. CONTROLSS\_CTRL\_EPWM6\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM6_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

### 2.7.2.108 CONTROLSS\_CTRL\_EPWM7\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM7\_RST Register (Offset = 31Ch) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3500. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 031Ch       |

**Figure 2-1165. CONTROLSS\_CTRL\_EPWM7\_RST Name Register**

|          |    |    |    |               |    |    |    |
|----------|----|----|----|---------------|----|----|----|
| 31       | 30 | 29 | 28 | 27            | 26 | 25 | 24 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 23       | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 15       | 14 | 13 | 12 | 11            | 10 | 9  | 8  |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 7        | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM7_RST_RST |    |    |    |
| NONE     |    |    |    | R/W           |    |    |    |
| 0h       |    |    |    | 0h            |    |    |    |

**Table 2-3502. CONTROLSS\_CTRL\_EPWM7\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM7_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

### 2.7.2.109 CONTROLSS\_CTRL\_EPWM8\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM8\_RST Register (Offset = 320h) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3503. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0320h       |

**Figure 2-1166. CONTROLSS\_CTRL\_EPWM8\_RST Name Register**

|          |    |    |    |               |    |    |    |
|----------|----|----|----|---------------|----|----|----|
| 31       | 30 | 29 | 28 | 27            | 26 | 25 | 24 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 23       | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 15       | 14 | 13 | 12 | 11            | 10 | 9  | 8  |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 7        | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM8_RST_RST |    |    |    |
| NONE     |    |    |    | R/W           |    |    |    |
| 0h       |    |    |    | 0h            |    |    |    |

**Table 2-3505. CONTROLSS\_CTRL\_EPWM8\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM8_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

### 2.7.2.110 CONTROLSS\_CTRL\_EPWM9\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM9\_RST Register (Offset = 324h) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3506. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0324h       |

**Figure 2-1167. CONTROLSS\_CTRL\_EPWM9\_RST Name Register**

|          |    |    |    |    |               |    |    |
|----------|----|----|----|----|---------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26            | 25 | 24 |
| RESERVED |    |    |    |    |               |    |    |
| NONE     |    |    |    |    |               |    |    |
| 0h       |    |    |    |    |               |    |    |
| 23       | 22 | 21 | 20 | 19 | 18            | 17 | 16 |
| RESERVED |    |    |    |    |               |    |    |
| NONE     |    |    |    |    |               |    |    |
| 0h       |    |    |    |    |               |    |    |
| 15       | 14 | 13 | 12 | 11 | 10            | 9  | 8  |
| RESERVED |    |    |    |    |               |    |    |
| NONE     |    |    |    |    |               |    |    |
| 0h       |    |    |    |    |               |    |    |
| 7        | 6  | 5  | 4  | 3  | 2             | 1  | 0  |
| RESERVED |    |    |    |    | EPWM9_RST_RST |    |    |
| NONE     |    |    |    |    | R/W           |    |    |
| 0h       |    |    |    |    | 0h            |    |    |

**Table 2-3508. CONTROLSS\_CTRL\_EPWM9\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM9_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

### 2.7.2.111 CONTROLSS\_CTRL\_EPWM10\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM10\_RST Register (Offset = 328h) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3509. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0328h       |

**Figure 2-1168. CONTROLSS\_CTRL\_EPWM10\_RST Name Register**

|          |    |    |    |                |    |    |    |
|----------|----|----|----|----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 23       | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 15       | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 7        | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM10_RST_RST |    |    |    |
| NONE     |    |    |    | R/W            |    |    |    |
| 0h       |    |    |    | 0h             |    |    |    |

**Table 2-3511. CONTROLSS\_CTRL\_EPWM10\_RST Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                               |
|------|----------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED       | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM10_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

### 2.7.2.112 CONTROLSS\_CTRL\_EPWM11\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM11\_RST Register (Offset = 32Ch) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3512. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 032Ch       |

**Figure 2-1169. CONTROLSS\_CTRL\_EPWM11\_RST Name Register**

|          |    |    |    |                |    |    |    |
|----------|----|----|----|----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 23       | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 15       | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 7        | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM11_RST_RST |    |    |    |
| NONE     |    |    |    | R/W            |    |    |    |
| 0h       |    |    |    | 0h             |    |    |    |

**Table 2-3514. CONTROLSS\_CTRL\_EPWM11\_RST Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                               |
|------|----------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED       | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM11_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |



### 2.7.2.113 CONTROLSS\_CTRL\_EPWM12\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM12\_RST Register (Offset = 330h) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3515. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0330h       |

**Figure 2-1170. CONTROLSS\_CTRL\_EPWM12\_RST Name Register**

|          |    |    |    |                |    |    |    |
|----------|----|----|----|----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 23       | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 15       | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 7        | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM12_RST_RST |    |    |    |
| NONE     |    |    |    | R/W            |    |    |    |
| 0h       |    |    |    | 0h             |    |    |    |

**Table 2-3517. CONTROLSS\_CTRL\_EPWM12\_RST Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                               |
|------|----------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED       | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM12_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

### 2.7.2.114 CONTROLSS\_CTRL\_EPWM13\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM13\_RST Register (Offset = 334h) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3518. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0334h       |

**Figure 2-1171. CONTROLSS\_CTRL\_EPWM13\_RST Name Register**

|          |    |    |    |                |    |    |    |
|----------|----|----|----|----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 23       | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 15       | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 7        | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM13_RST_RST |    |    |    |
| NONE     |    |    |    | R/W            |    |    |    |
| 0h       |    |    |    | 0h             |    |    |    |

**Table 2-3520. CONTROLSS\_CTRL\_EPWM13\_RST Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                               |
|------|----------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED       | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM13_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

### 2.7.2.115 CONTROLSS\_CTRL\_EPWM14\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM14\_RST Register (Offset = 338h) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3521. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0338h       |

**Figure 2-1172. CONTROLSS\_CTRL\_EPWM14\_RST Name Register**

|          |    |    |    |                |    |    |    |
|----------|----|----|----|----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 23       | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 15       | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 7        | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM14_RST_RST |    |    |    |
| NONE     |    |    |    | R/W            |    |    |    |
| 0h       |    |    |    | 0h             |    |    |    |

**Table 2-3523. CONTROLSS\_CTRL\_EPWM14\_RST Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                               |
|------|----------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED       | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM14_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

## 2.7.2.116 CONTROLSS\_CTRL\_EPWM15\_RST Register

### 1 CONTROLSS\_CTRL\_EPWM15\_RST Register (Offset = 33Ch) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3524. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 033Ch       |

**Figure 2-1173. CONTROLSS\_CTRL\_EPWM15\_RST Name Register**

|          |    |    |    |                |    |    |    |
|----------|----|----|----|----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 23       | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 15       | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 7        | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM15_RST_RST |    |    |    |
| NONE     |    |    |    | R/W            |    |    |    |
| 0h       |    |    |    | 0h             |    |    |    |

**Table 2-3526. CONTROLSS\_CTRL\_EPWM15\_RST Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                               |
|------|----------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED       | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM15_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

### 2.7.2.117 CONTROLSS\_CTRL\_EPWM16\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM16\_RST Register (Offset = 340h) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3527. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0340h       |

**Figure 2-1174. CONTROLSS\_CTRL\_EPWM16\_RST Name Register**

|          |    |    |    |                |    |    |    |
|----------|----|----|----|----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 23       | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 15       | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 7        | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM16_RST_RST |    |    |    |
| NONE     |    |    |    | R/W            |    |    |    |
| 0h       |    |    |    | 0h             |    |    |    |

**Table 2-3529. CONTROLSS\_CTRL\_EPWM16\_RST Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                               |
|------|----------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED       | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM16_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

### 2.7.2.118 CONTROLSS\_CTRL\_EPWM17\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM17\_RST Register (Offset = 344h) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3530. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0344h       |

**Figure 2-1175. CONTROLSS\_CTRL\_EPWM17\_RST Name Register**

|          |    |    |    |                |    |    |    |
|----------|----|----|----|----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 23       | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 15       | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 7        | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM17_RST_RST |    |    |    |
| NONE     |    |    |    | R/W            |    |    |    |
| 0h       |    |    |    | 0h             |    |    |    |

**Table 2-3532. CONTROLSS\_CTRL\_EPWM17\_RST Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                               |
|------|----------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED       | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM17_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

### 2.7.2.119 CONTROLSS\_CTRL\_EPWM18\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM18\_RST Register (Offset = 348h) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3533. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0348h       |

**Figure 2-1176. CONTROLSS\_CTRL\_EPWM18\_RST Name Register**

|          |    |    |    |                |    |    |    |
|----------|----|----|----|----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 23       | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 15       | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 7        | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM18_RST_RST |    |    |    |
| NONE     |    |    |    | R/W            |    |    |    |
| 0h       |    |    |    | 0h             |    |    |    |

**Table 2-3535. CONTROLSS\_CTRL\_EPWM18\_RST Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                               |
|------|----------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED       | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM18_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

### 2.7.2.120 CONTROLSS\_CTRL\_EPWM19\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM19\_RST Register (Offset = 34Ch) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3536. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 034Ch       |

**Figure 2-1177. CONTROLSS\_CTRL\_EPWM19\_RST Name Register**

|          |    |    |    |                |    |    |    |
|----------|----|----|----|----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 23       | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 15       | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 7        | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM19_RST_RST |    |    |    |
| NONE     |    |    |    | R/W            |    |    |    |
| 0h       |    |    |    | 0h             |    |    |    |

**Table 2-3538. CONTROLSS\_CTRL\_EPWM19\_RST Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                               |
|------|----------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED       | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM19_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |



### 2.7.2.121 CONTROLSS\_CTRL\_EPWM20\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM20\_RST Register (Offset = 350h) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3539. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0350h       |

**Figure 2-1178. CONTROLSS\_CTRL\_EPWM20\_RST Name Register**

|          |    |    |    |                |    |    |    |
|----------|----|----|----|----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 23       | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 15       | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 7        | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM20_RST_RST |    |    |    |
| NONE     |    |    |    | R/W            |    |    |    |
| 0h       |    |    |    | 0h             |    |    |    |

**Table 2-3541. CONTROLSS\_CTRL\_EPWM20\_RST Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                               |
|------|----------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED       | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM20_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

### 2.7.2.122 CONTROLSS\_CTRL\_EPWM21\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM21\_RST Register (Offset = 354h) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3542. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0354h       |

**Figure 2-1179. CONTROLSS\_CTRL\_EPWM21\_RST Name Register**

|          |    |    |    |                |    |    |    |
|----------|----|----|----|----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 23       | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 15       | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 7        | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM21_RST_RST |    |    |    |
| NONE     |    |    |    | R/W            |    |    |    |
| 0h       |    |    |    | 0h             |    |    |    |

**Table 2-3544. CONTROLSS\_CTRL\_EPWM21\_RST Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                               |
|------|----------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED       | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM21_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

### 2.7.2.123 CONTROLSS\_CTRL\_EPWM22\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM22\_RST Register (Offset = 358h) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3545. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0358h       |

**Figure 2-1180. CONTROLSS\_CTRL\_EPWM22\_RST Name Register**

|          |    |    |    |                |    |    |    |
|----------|----|----|----|----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 23       | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 15       | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 7        | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM22_RST_RST |    |    |    |
| NONE     |    |    |    | R/W            |    |    |    |
| 0h       |    |    |    | 0h             |    |    |    |

**Table 2-3547. CONTROLSS\_CTRL\_EPWM22\_RST Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                               |
|------|----------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED       | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM22_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

### 2.7.2.124 CONTROLSS\_CTRL\_EPWM23\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM23\_RST Register (Offset = 35Ch) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3548. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 035Ch       |

**Figure 2-1181. CONTROLSS\_CTRL\_EPWM23\_RST Name Register**

|          |    |    |    |                |    |    |    |
|----------|----|----|----|----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 23       | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 15       | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 7        | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM23_RST_RST |    |    |    |
| NONE     |    |    |    | R/W            |    |    |    |
| 0h       |    |    |    | 0h             |    |    |    |

**Table 2-3550. CONTROLSS\_CTRL\_EPWM23\_RST Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                               |
|------|----------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED       | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM23_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

### 2.7.2.125 CONTROLSS\_CTRL\_EPWM24\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM24\_RST Register (Offset = 360h) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3551. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0360h       |

**Figure 2-1182. CONTROLSS\_CTRL\_EPWM24\_RST Name Register**

|          |    |    |    |                |    |    |    |
|----------|----|----|----|----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 23       | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 15       | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 7        | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM24_RST_RST |    |    |    |
| NONE     |    |    |    | R/W            |    |    |    |
| 0h       |    |    |    | 0h             |    |    |    |

**Table 2-3553. CONTROLSS\_CTRL\_EPWM24\_RST Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                               |
|------|----------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED       | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM24_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

### 2.7.2.126 CONTROLSS\_CTRL\_EPWM25\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM25\_RST Register (Offset = 364h) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3554. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0364h       |

**Figure 2-1183. CONTROLSS\_CTRL\_EPWM25\_RST Name Register**

|          |    |    |    |                |    |    |    |
|----------|----|----|----|----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 23       | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 15       | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 7        | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM25_RST_RST |    |    |    |
| NONE     |    |    |    | R/W            |    |    |    |
| 0h       |    |    |    | 0h             |    |    |    |

**Table 2-3556. CONTROLSS\_CTRL\_EPWM25\_RST Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                               |
|------|----------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED       | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM25_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

### 2.7.2.127 CONTROLSS\_CTRL\_EPWM26\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM26\_RST Register (Offset = 368h) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3557. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0368h       |

**Figure 2-1184. CONTROLSS\_CTRL\_EPWM26\_RST Name Register**

|          |    |    |    |                |    |    |    |
|----------|----|----|----|----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 23       | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 15       | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 7        | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM26_RST_RST |    |    |    |
| NONE     |    |    |    | R/W            |    |    |    |
| 0h       |    |    |    | 0h             |    |    |    |

**Table 2-3559. CONTROLSS\_CTRL\_EPWM26\_RST Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                               |
|------|----------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED       | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM26_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

### 2.7.2.128 CONTROLSS\_CTRL\_EPWM27\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM27\_RST Register (Offset = 36Ch) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3560. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 036Ch       |

**Figure 2-1185. CONTROLSS\_CTRL\_EPWM27\_RST Name Register**

|          |    |    |    |                |    |    |    |
|----------|----|----|----|----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 23       | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 15       | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 7        | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM27_RST_RST |    |    |    |
| NONE     |    |    |    | R/W            |    |    |    |
| 0h       |    |    |    | 0h             |    |    |    |

**Table 2-3562. CONTROLSS\_CTRL\_EPWM27\_RST Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                               |
|------|----------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED       | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM27_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |



### 2.7.2.129 CONTROLSS\_CTRL\_EPWM28\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM28\_RST Register (Offset = 370h) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3563. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0370h       |

**Figure 2-1186. CONTROLSS\_CTRL\_EPWM28\_RST Name Register**

|          |    |    |    |                |    |    |    |
|----------|----|----|----|----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 23       | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 15       | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 7        | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM28_RST_RST |    |    |    |
| NONE     |    |    |    | R/W            |    |    |    |
| 0h       |    |    |    | 0h             |    |    |    |

**Table 2-3565. CONTROLSS\_CTRL\_EPWM28\_RST Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                               |
|------|----------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED       | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM28_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

### 2.7.2.130 CONTROLSS\_CTRL\_EPWM29\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM29\_RST Register (Offset = 374h) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3566. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0374h       |

**Figure 2-1187. CONTROLSS\_CTRL\_EPWM29\_RST Name Register**

|          |    |    |    |                |    |    |    |
|----------|----|----|----|----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 23       | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 15       | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 7        | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM29_RST_RST |    |    |    |
| NONE     |    |    |    | R/W            |    |    |    |
| 0h       |    |    |    | 0h             |    |    |    |

**Table 2-3568. CONTROLSS\_CTRL\_EPWM29\_RST Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                               |
|------|----------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED       | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM29_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

### 2.7.2.131 CONTROLSS\_CTRL\_EPWM30\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM30\_RST Register (Offset = 378h) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3569. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0378h       |

**Figure 2-1188. CONTROLSS\_CTRL\_EPWM30\_RST Name Register**

|          |    |    |    |                |    |    |    |
|----------|----|----|----|----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 23       | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 15       | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 7        | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| RESERVED |    |    |    | EPWM30_RST_RST |    |    |    |
| NONE     |    |    |    | R/W            |    |    |    |
| 0h       |    |    |    | 0h             |    |    |    |

**Table 2-3571. CONTROLSS\_CTRL\_EPWM30\_RST Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                               |
|------|----------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED       | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM30_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

### 2.7.2.132 CONTROLSS\_CTRL\_EPWM31\_RST Register

#### 1 CONTROLSS\_CTRL\_EPWM31\_RST Register (Offset = 37Ch) [reset = 0h]

Epwm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3572. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 037Ch       |

**Figure 2-1189. CONTROLSS\_CTRL\_EPWM31\_RST Name Register**

|          |    |    |    |    |                |    |    |
|----------|----|----|----|----|----------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26             | 25 | 24 |
| RESERVED |    |    |    |    |                |    |    |
| NONE     |    |    |    |    |                |    |    |
| 0h       |    |    |    |    |                |    |    |
| 23       | 22 | 21 | 20 | 19 | 18             | 17 | 16 |
| RESERVED |    |    |    |    |                |    |    |
| NONE     |    |    |    |    |                |    |    |
| 0h       |    |    |    |    |                |    |    |
| 15       | 14 | 13 | 12 | 11 | 10             | 9  | 8  |
| RESERVED |    |    |    |    |                |    |    |
| NONE     |    |    |    |    |                |    |    |
| 0h       |    |    |    |    |                |    |    |
| 7        | 6  | 5  | 4  | 3  | 2              | 1  | 0  |
| RESERVED |    |    |    |    | EPWM31_RST_RST |    |    |
| NONE     |    |    |    |    | R/W            |    |    |
| 0h       |    |    |    |    | 0h             |    |    |

**Table 2-3574. CONTROLSS\_CTRL\_EPWM31\_RST Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                               |
|------|----------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED       | NONE | 0h    | Reserved                                                  |
| 2:0  | EPWM31_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding epwm |

### 2.7.2.133 CONTROLSS\_CTRL\_FSI\_TX0\_RST Register

#### 1 CONTROLSS\_CTRL\_FSI\_TX0\_RST Register (Offset = 380h) [reset = 0h]

fsi\_tx[x]\_reset.

Return to [Summary Table](#)

**Table 2-3575. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0380h       |

**Figure 2-1190. CONTROLSS\_CTRL\_FSI\_TX0\_RST Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | FSI_TX0_RST_RST |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 2-3577. CONTROLSS\_CTRL\_FSI\_TX0\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | FSI_TX0_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding fsi_tx |

### 2.7.2.134 CONTROLSS\_CTRL\_FSI\_TX1\_RST Register

#### 1 CONTROLSS\_CTRL\_FSI\_TX1\_RST Register (Offset = 384h) [reset = 0h]

fsi\_tx[x]\_reset.

Return to [Summary Table](#)

**Table 2-3578. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0384h       |

**Figure 2-1191. CONTROLSS\_CTRL\_FSI\_TX1\_RST Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | FSI_TX1_RST_RST |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 2-3580. CONTROLSS\_CTRL\_FSI\_TX1\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | FSI_TX1_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding fsi_tx |

### 2.7.2.135 CONTROLSS\_CTRL\_FSI\_TX2\_RST Register

#### 1 CONTROLSS\_CTRL\_FSI\_TX2\_RST Register (Offset = 388h) [reset = 0h]

fsi\_tx[x]\_reset.

Return to [Summary Table](#)

**Table 2-3581. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0388h       |

**Figure 2-1192. CONTROLSS\_CTRL\_FSI\_TX2\_RST Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | FSI_TX2_RST_RST |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 2-3583. CONTROLSS\_CTRL\_FSI\_TX2\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | FSI_TX2_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding fsi_tx |

### 2.7.2.136 CONTROLSS\_CTRL\_FSI\_TX3\_RST Register

#### 1 CONTROLSS\_CTRL\_FSI\_TX3\_RST Register (Offset = 38Ch) [reset = 0h]

fsi\_tx[x]\_reset.

Return to [Summary Table](#)

**Table 2-3584. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 038Ch       |

**Figure 2-1193. CONTROLSS\_CTRL\_FSI\_TX3\_RST Name Register**

|          |    |    |    |    |                 |    |    |
|----------|----|----|----|----|-----------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26              | 25 | 24 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 23       | 22 | 21 | 20 | 19 | 18              | 17 | 16 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 15       | 14 | 13 | 12 | 11 | 10              | 9  | 8  |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 7        | 6  | 5  | 4  | 3  | 2               | 1  | 0  |
| RESERVED |    |    |    |    | FSI_TX3_RST_RST |    |    |
| NONE     |    |    |    |    | R/W             |    |    |
| 0h       |    |    |    |    | 0h              |    |    |

**Table 2-3586. CONTROLSS\_CTRL\_FSI\_TX3\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | FSI_TX3_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding fsi_tx |



### 2.7.2.137 CONTROLSS\_CTRL\_FSI\_RX0\_RST Register

#### 1 CONTROLSS\_CTRL\_FSI\_RX0\_RST Register (Offset = 390h) [reset = 0h]

fsi\_rx[x]\_reset.

Return to [Summary Table](#)

**Table 2-3587. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0390h       |

**Figure 2-1194. CONTROLSS\_CTRL\_FSI\_RX0\_RST Name Register**

|          |    |    |    |    |                 |    |    |
|----------|----|----|----|----|-----------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26              | 25 | 24 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 23       | 22 | 21 | 20 | 19 | 18              | 17 | 16 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 15       | 14 | 13 | 12 | 11 | 10              | 9  | 8  |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 7        | 6  | 5  | 4  | 3  | 2               | 1  | 0  |
| RESERVED |    |    |    |    | FSI_RX0_RST_RST |    |    |
| NONE     |    |    |    |    | R/W             |    |    |
| 0h       |    |    |    |    | 0h              |    |    |

**Table 2-3589. CONTROLSS\_CTRL\_FSI\_RX0\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | FSI_RX0_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding fsi_rx |

### 2.7.2.138 CONTROLSS\_CTRL\_FSI\_RX1\_RST Register

#### 1 CONTROLSS\_CTRL\_FSI\_RX1\_RST Register (Offset = 394h) [reset = 0h]

fsi\_rx[x]\_reset.

Return to [Summary Table](#)

**Table 2-3590. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0394h       |

**Figure 2-1195. CONTROLSS\_CTRL\_FSI\_RX1\_RST Name Register**

|          |    |    |    |    |                 |    |    |
|----------|----|----|----|----|-----------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26              | 25 | 24 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 23       | 22 | 21 | 20 | 19 | 18              | 17 | 16 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 15       | 14 | 13 | 12 | 11 | 10              | 9  | 8  |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 7        | 6  | 5  | 4  | 3  | 2               | 1  | 0  |
| RESERVED |    |    |    |    | FSI_RX1_RST_RST |    |    |
| NONE     |    |    |    |    | R/W             |    |    |
| 0h       |    |    |    |    | 0h              |    |    |

**Table 2-3592. CONTROLSS\_CTRL\_FSI\_RX1\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | FSI_RX1_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding fsi_rx |

### 2.7.2.139 CONTROLSS\_CTRL\_FSI\_RX2\_RST Register

#### 1 CONTROLSS\_CTRL\_FSI\_RX2\_RST Register (Offset = 398h) [reset = 0h]

fsi\_rx[x]\_reset.

Return to [Summary Table](#)

**Table 2-3593. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0398h       |

**Figure 2-1196. CONTROLSS\_CTRL\_FSI\_RX2\_RST Name Register**

|          |    |    |    |    |                 |    |    |
|----------|----|----|----|----|-----------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26              | 25 | 24 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 23       | 22 | 21 | 20 | 19 | 18              | 17 | 16 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 15       | 14 | 13 | 12 | 11 | 10              | 9  | 8  |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 7        | 6  | 5  | 4  | 3  | 2               | 1  | 0  |
| RESERVED |    |    |    |    | FSI_RX2_RST_RST |    |    |
| NONE     |    |    |    |    | R/W             |    |    |
| 0h       |    |    |    |    | 0h              |    |    |

**Table 2-3595. CONTROLSS\_CTRL\_FSI\_RX2\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | FSI_RX2_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding fsi_rx |

### 2.7.2.140 CONTROLSS\_CTRL\_FSI\_RX3\_RST Register

#### 1 CONTROLSS\_CTRL\_FSI\_RX3\_RST Register (Offset = 39Ch) [reset = 0h]

fsi\_rx[x]\_reset.

Return to [Summary Table](#)
**Table 2-3596. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 039Ch       |

**Figure 2-1197. CONTROLSS\_CTRL\_FSI\_RX3\_RST Name Register**

|          |    |    |    |    |                 |    |    |
|----------|----|----|----|----|-----------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26              | 25 | 24 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 23       | 22 | 21 | 20 | 19 | 18              | 17 | 16 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 15       | 14 | 13 | 12 | 11 | 10              | 9  | 8  |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 7        | 6  | 5  | 4  | 3  | 2               | 1  | 0  |
| RESERVED |    |    |    |    | FSI_RX3_RST_RST |    |    |
| NONE     |    |    |    |    | R/W             |    |    |
| 0h       |    |    |    |    | 0h              |    |    |

**Table 2-3598. CONTROLSS\_CTRL\_FSI\_RX3\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | FSI_RX3_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding fsi_rx |

### 2.7.2.141 CONTROLSS\_CTRL\_CMPSSA0\_RST Register

#### 1 CONTROLSS\_CTRL\_CMPSSA0\_RST Register (Offset = 3A0h) [reset = 0h]

cmpssa[x]\_reset.

Return to [Summary Table](#)

**Table 2-3599. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 03A0h       |

**Figure 2-1198. CONTROLSS\_CTRL\_CMPSSA0\_RST Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | CMPSSA0_RST_RST |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 2-3601. CONTROLSS\_CTRL\_CMPSSA0\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | CMPSSA0_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding cmpssa |

### 2.7.2.142 CONTROLSS\_CTRL\_CMPSSA1\_RST Register

#### 1 CONTROLSS\_CTRL\_CMPSSA1\_RST Register (Offset = 3A4h) [reset = 0h]

cmpssa[x]\_reset.

Return to [Summary Table](#)

**Table 2-3602. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 03A4h       |

**Figure 2-1199. CONTROLSS\_CTRL\_CMPSSA1\_RST Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | CMPSSA1_RST_RST |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 2-3604. CONTROLSS\_CTRL\_CMPSSA1\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | CMPSSA1_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding cmpssa |

### 2.7.2.143 CONTROLSS\_CTRL\_CMPSSA2\_RST Register

#### 1 CONTROLSS\_CTRL\_CMPSSA2\_RST Register (Offset = 3A8h) [reset = 0h]

cmpssa[x]\_reset.

Return to [Summary Table](#)

**Table 2-3605. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 03A8h       |

**Figure 2-1200. CONTROLSS\_CTRL\_CMPSSA2\_RST Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | CMPSSA2_RST_RST |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 2-3607. CONTROLSS\_CTRL\_CMPSSA2\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | CMPSSA2_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding cmpssa |

### 2.7.2.144 CONTROLSS\_CTRL\_CMPSSA3\_RST Register

#### 1 CONTROLSS\_CTRL\_CMPSSA3\_RST Register (Offset = 3ACh) [reset = 0h]

cmpssa[x]\_reset.

Return to [Summary Table](#)

**Table 2-3608. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 03ACh       |

**Figure 2-1201. CONTROLSS\_CTRL\_CMPSSA3\_RST Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | CMPSSA3_RST_RST |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 2-3610. CONTROLSS\_CTRL\_CMPSSA3\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | CMPSSA3_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding cmpssa |



### 2.7.2.145 CONTROLSS\_CTRL\_CMPSSA4\_RST Register

#### 1 CONTROLSS\_CTRL\_CMPSSA4\_RST Register (Offset = 3B0h) [reset = 0h]

cmpssa[x]\_reset.

Return to [Summary Table](#)

**Table 2-3611. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 03B0h       |

**Figure 2-1202. CONTROLSS\_CTRL\_CMPSSA4\_RST Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | CMPSSA4_RST_RST |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 2-3613. CONTROLSS\_CTRL\_CMPSSA4\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | CMPSSA4_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding cmpssa |

### 2.7.2.146 CONTROLSS\_CTRL\_CMPSSA5\_RST Register

#### 1 CONTROLSS\_CTRL\_CMPSSA5\_RST Register (Offset = 3B4h) [reset = 0h]

cmpssa[x]\_reset.

Return to [Summary Table](#)

**Table 2-3614. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 03B4h       |

**Figure 2-1203. CONTROLSS\_CTRL\_CMPSSA5\_RST Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | CMPSSA5_RST_RST |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 2-3616. CONTROLSS\_CTRL\_CMPSSA5\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | CMPSSA5_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding cmpssa |

### 2.7.2.147 CONTROLSS\_CTRL\_CMPSSA6\_RST Register

#### 1 CONTROLSS\_CTRL\_CMPSSA6\_RST Register (Offset = 3B8h) [reset = 0h]

cmpssa[x]\_reset.

Return to [Summary Table](#)

**Table 2-3617. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 03B8h       |

**Figure 2-1204. CONTROLSS\_CTRL\_CMPSSA6\_RST Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | CMPSSA6_RST_RST |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 2-3619. CONTROLSS\_CTRL\_CMPSSA6\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | CMPSSA6_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding cmpssa |

## 2.7.2.148 CONTROLSS\_CTRL\_CMPSSA7\_RST Register

### 1 CONTROLSS\_CTRL\_CMPSSA7\_RST Register (Offset = 3BCh) [reset = 0h]

cmpssa[x]\_reset.

Return to [Summary Table](#)

**Table 2-3620. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 03BCh       |

**Figure 2-1205. CONTROLSS\_CTRL\_CMPSSA7\_RST Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | CMPSSA7_RST_RST |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 2-3622. CONTROLSS\_CTRL\_CMPSSA7\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | CMPSSA7_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding cmpssa |

### 2.7.2.149 CONTROLSS\_CTRL\_CMPSSA8\_RST Register

#### 1 CONTROLSS\_CTRL\_CMPSSA8\_RST Register (Offset = 3C0h) [reset = 0h]

cmpssa[x]\_reset.

Return to [Summary Table](#)
**Table 2-3623. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 03C0h       |

**Figure 2-1206. CONTROLSS\_CTRL\_CMPSSA8\_RST Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | CMPSSA8_RST_RST |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 2-3625. CONTROLSS\_CTRL\_CMPSSA8\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | CMPSSA8_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding cmpssa |

## 2.7.2.150 CONTROLSS\_CTRL\_CMPSSA9\_RST Register

### 1 CONTROLSS\_CTRL\_CMPSSA9\_RST Register (Offset = 3C4h) [reset = 0h]

cmpssa[x]\_reset.

Return to [Summary Table](#)

**Table 2-3626. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 03C4h       |

**Figure 2-1207. CONTROLSS\_CTRL\_CMPSSA9\_RST Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | CMPSSA9_RST_RST |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 2-3628. CONTROLSS\_CTRL\_CMPSSA9\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | CMPSSA9_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding cmpssa |

### 2.7.2.151 CONTROLSS\_CTRL\_CMPSSB0\_RST Register

#### 1 CONTROLSS\_CTRL\_CMPSSB0\_RST Register (Offset = 3D0h) [reset = 0h]

cmpssb[x]\_reset.

Return to [Summary Table](#)
**Table 2-3629. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 03D0h       |

**Figure 2-1208. CONTROLSS\_CTRL\_CMPSSB0\_RST Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | CMPSSB0_RST_RST |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 2-3631. CONTROLSS\_CTRL\_CMPSSB0\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | CMPSSB0_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding cmpssb |

### 2.7.2.152 CONTROLSS\_CTRL\_CMPSSB1\_RST Register

#### 1 CONTROLSS\_CTRL\_CMPSSB1\_RST Register (Offset = 3D4h) [reset = 0h]

cmpssb[x]\_reset.

Return to [Summary Table](#)
**Table 2-3632. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 03D4h       |

**Figure 2-1209. CONTROLSS\_CTRL\_CMPSSB1\_RST Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | CMPSSB1_RST_RST |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 2-3634. CONTROLSS\_CTRL\_CMPSSB1\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | CMPSSB1_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding cmpssb |



### 2.7.2.153 CONTROLSS\_CTRL\_CMPSSB2\_RST Register

#### 1 CONTROLSS\_CTRL\_CMPSSB2\_RST Register (Offset = 3D8h) [reset = 0h]

cmpssb[x]\_reset.

Return to [Summary Table](#)
**Table 2-3635. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 03D8h       |

**Figure 2-1210. CONTROLSS\_CTRL\_CMPSSB2\_RST Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | CMPSSB2_RST_RST |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 2-3637. CONTROLSS\_CTRL\_CMPSSB2\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | CMPSSB2_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding cmpssb |

## 2.7.2.154 CONTROLSS\_CTRL\_CMPSSB3\_RST Register

### 1 CONTROLSS\_CTRL\_CMPSSB3\_RST Register (Offset = 3DCh) [reset = 0h]

cmpssb[x]\_reset.

Return to [Summary Table](#)
**Table 2-3638. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 03DCh       |

**Figure 2-1211. CONTROLSS\_CTRL\_CMPSSB3\_RST Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | CMPSSB3_RST_RST |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 2-3640. CONTROLSS\_CTRL\_CMPSSB3\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | CMPSSB3_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding cmpssb |

### 2.7.2.155 CONTROLSS\_CTRL\_CMPSSB4\_RST Register

#### 1 CONTROLSS\_CTRL\_CMPSSB4\_RST Register (Offset = 3E0h) [reset = 0h]

cmpssb[x]\_reset.

Return to [Summary Table](#)
**Table 2-3641. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 03E0h       |

**Figure 2-1212. CONTROLSS\_CTRL\_CMPSSB4\_RST Name Register**

|          |    |    |    |    |                 |    |    |
|----------|----|----|----|----|-----------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26              | 25 | 24 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 23       | 22 | 21 | 20 | 19 | 18              | 17 | 16 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 15       | 14 | 13 | 12 | 11 | 10              | 9  | 8  |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 7        | 6  | 5  | 4  | 3  | 2               | 1  | 0  |
| RESERVED |    |    |    |    | CMPSSB4_RST_RST |    |    |
| NONE     |    |    |    |    | R/W             |    |    |
| 0h       |    |    |    |    | 0h              |    |    |

**Table 2-3643. CONTROLSS\_CTRL\_CMPSSB4\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | CMPSSB4_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding cmpssb |

### 2.7.2.156 CONTROLSS\_CTRL\_CMPSSB5\_RST Register

#### 1 CONTROLSS\_CTRL\_CMPSSB5\_RST Register (Offset = 3E4h) [reset = 0h]

cmpssb[x]\_reset.

Return to [Summary Table](#)
**Table 2-3644. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 03E4h       |

**Figure 2-1213. CONTROLSS\_CTRL\_CMPSSB5\_RST Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | CMPSSB5_RST_RST |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 2-3646. CONTROLSS\_CTRL\_CMPSSB5\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | CMPSSB5_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding cmpssb |

### 2.7.2.157 CONTROLSS\_CTRL\_CMPSSB6\_RST Register

#### 1 CONTROLSS\_CTRL\_CMPSSB6\_RST Register (Offset = 3E8h) [reset = 0h]

cmpssb[x]\_reset.

Return to [Summary Table](#)
**Table 2-3647. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 03E8h       |

**Figure 2-1214. CONTROLSS\_CTRL\_CMPSSB6\_RST Name Register**

|          |    |    |    |    |                 |    |    |
|----------|----|----|----|----|-----------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26              | 25 | 24 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 23       | 22 | 21 | 20 | 19 | 18              | 17 | 16 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 15       | 14 | 13 | 12 | 11 | 10              | 9  | 8  |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 7        | 6  | 5  | 4  | 3  | 2               | 1  | 0  |
| RESERVED |    |    |    |    | CMPSSB6_RST_RST |    |    |
| NONE     |    |    |    |    | R/W             |    |    |
| 0h       |    |    |    |    | 0h              |    |    |

**Table 2-3649. CONTROLSS\_CTRL\_CMPSSB6\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | CMPSSB6_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding cmpssb |

### 2.7.2.158 CONTROLSS\_CTRL\_CMPSSB7\_RST Register

#### 1 CONTROLSS\_CTRL\_CMPSSB7\_RST Register (Offset = 3ECh) [reset = 0h]

cmpssb[x]\_reset.

Return to [Summary Table](#)
**Table 2-3650. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 03ECh       |

**Figure 2-1215. CONTROLSS\_CTRL\_CMPSSB7\_RST Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | CMPSSB7_RST_RST |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 2-3652. CONTROLSS\_CTRL\_CMPSSB7\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | CMPSSB7_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding cmpssb |

### 2.7.2.159 CONTROLSS\_CTRL\_CMPSSB8\_RST Register

#### 1 CONTROLSS\_CTRL\_CMPSSB8\_RST Register (Offset = 3F0h) [reset = 0h]

cmpssb[x]\_reset.

Return to [Summary Table](#)
**Table 2-3653. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 03F0h       |

**Figure 2-1216. CONTROLSS\_CTRL\_CMPSSB8\_RST Name Register**

|          |    |    |    |    |                 |    |    |
|----------|----|----|----|----|-----------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26              | 25 | 24 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 23       | 22 | 21 | 20 | 19 | 18              | 17 | 16 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 15       | 14 | 13 | 12 | 11 | 10              | 9  | 8  |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 7        | 6  | 5  | 4  | 3  | 2               | 1  | 0  |
| RESERVED |    |    |    |    | CMPSSB8_RST_RST |    |    |
| NONE     |    |    |    |    | R/W             |    |    |
| 0h       |    |    |    |    | 0h              |    |    |

**Table 2-3655. CONTROLSS\_CTRL\_CMPSSB8\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | CMPSSB8_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding cmpssb |

### 2.7.2.160 CONTROLSS\_CTRL\_CMPSSB9\_RST Register

#### 1 CONTROLSS\_CTRL\_CMPSSB9\_RST Register (Offset = 3F4h) [reset = 0h]

cmpssb[x]\_reset.

Return to [Summary Table](#)
**Table 2-3656. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 03F4h       |

**Figure 2-1217. CONTROLSS\_CTRL\_CMPSSB9\_RST Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | CMPSSB9_RST_RST |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 2-3658. CONTROLSS\_CTRL\_CMPSSB9\_RST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                    |
| 2:0  | CMPSSB9_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding cmpssb |



### 2.7.2.161 CONTROLSS\_CTRL\_ECAP0\_RST Register

#### 1 CONTROLSS\_CTRL\_ECAP0\_RST Register (Offset = 400h) [reset = 0h]

Ecap[x]\_reset.

Return to [Summary Table](#)

**Table 2-3659. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0400h       |

**Figure 2-1218. CONTROLSS\_CTRL\_ECAP0\_RST Name Register**

|          |    |    |    |               |    |    |    |
|----------|----|----|----|---------------|----|----|----|
| 31       | 30 | 29 | 28 | 27            | 26 | 25 | 24 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 23       | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 15       | 14 | 13 | 12 | 11            | 10 | 9  | 8  |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 7        | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| RESERVED |    |    |    | ECAP0_RST_RST |    |    |    |
| NONE     |    |    |    | R/W           |    |    |    |
| 0h       |    |    |    | 0h            |    |    |    |

**Table 2-3661. CONTROLSS\_CTRL\_ECAP0\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | ECAP0_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding ecap |

## 2.7.2.162 CONTROLSS\_CTRL\_ECAP1\_RST Register

### 1 CONTROLSS\_CTRL\_ECAP1\_RST Register (Offset = 404h) [reset = 0h]

Ecap[x]\_reset.

Return to [Summary Table](#)

**Table 2-3662. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0404h       |

**Figure 2-1219. CONTROLSS\_CTRL\_ECAP1\_RST Name Register**

|          |    |    |    |               |    |    |    |
|----------|----|----|----|---------------|----|----|----|
| 31       | 30 | 29 | 28 | 27            | 26 | 25 | 24 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 23       | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 15       | 14 | 13 | 12 | 11            | 10 | 9  | 8  |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 7        | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| RESERVED |    |    |    | ECAP1_RST_RST |    |    |    |
| NONE     |    |    |    | R/W           |    |    |    |
| 0h       |    |    |    | 0h            |    |    |    |

**Table 2-3664. CONTROLSS\_CTRL\_ECAP1\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | ECAP1_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding ecap |

### 2.7.2.163 CONTROLSS\_CTRL\_ECAP2\_RST Register

#### 1 CONTROLSS\_CTRL\_ECAP2\_RST Register (Offset = 408h) [reset = 0h]

Ecap[x]\_reset.

Return to [Summary Table](#)

**Table 2-3665. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0408h       |

**Figure 2-1220. CONTROLSS\_CTRL\_ECAP2\_RST Name Register**

|          |    |    |    |               |    |    |    |
|----------|----|----|----|---------------|----|----|----|
| 31       | 30 | 29 | 28 | 27            | 26 | 25 | 24 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 23       | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 15       | 14 | 13 | 12 | 11            | 10 | 9  | 8  |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 7        | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| RESERVED |    |    |    | ECAP2_RST_RST |    |    |    |
| NONE     |    |    |    | R/W           |    |    |    |
| 0h       |    |    |    | 0h            |    |    |    |

**Table 2-3667. CONTROLSS\_CTRL\_ECAP2\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | ECAP2_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding ecap |

### 2.7.2.164 CONTROLSS\_CTRL\_ECAP3\_RST Register

#### 1 CONTROLSS\_CTRL\_ECAP3\_RST Register (Offset = 40Ch) [reset = 0h]

Ecap[x]\_reset.

Return to [Summary Table](#)

**Table 2-3668. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 040Ch       |

**Figure 2-1221. CONTROLSS\_CTRL\_ECAP3\_RST Name Register**

|          |    |    |    |               |    |    |    |
|----------|----|----|----|---------------|----|----|----|
| 31       | 30 | 29 | 28 | 27            | 26 | 25 | 24 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 23       | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 15       | 14 | 13 | 12 | 11            | 10 | 9  | 8  |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 7        | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| RESERVED |    |    |    | ECAP3_RST_RST |    |    |    |
| NONE     |    |    |    | R/W           |    |    |    |
| 0h       |    |    |    | 0h            |    |    |    |

**Table 2-3670. CONTROLSS\_CTRL\_ECAP3\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | ECAP3_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding ecap |

## 2.7.2.165 CONTROLSS\_CTRL\_ECAP4\_RST Register

### 1 CONTROLSS\_CTRL\_ECAP4\_RST Register (Offset = 410h) [reset = 0h]

Ecap[x]\_reset.

Return to [Summary Table](#)

**Table 2-3671. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0410h       |

**Figure 2-1222. CONTROLSS\_CTRL\_ECAP4\_RST Name Register**

|          |    |    |    |               |    |    |    |
|----------|----|----|----|---------------|----|----|----|
| 31       | 30 | 29 | 28 | 27            | 26 | 25 | 24 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 23       | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 15       | 14 | 13 | 12 | 11            | 10 | 9  | 8  |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 7        | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| RESERVED |    |    |    | ECAP4_RST_RST |    |    |    |
| NONE     |    |    |    | R/W           |    |    |    |
| 0h       |    |    |    | 0h            |    |    |    |

**Table 2-3673. CONTROLSS\_CTRL\_ECAP4\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | ECAP4_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding ecap |

### 2.7.2.166 CONTROLSS\_CTRL\_ECAP5\_RST Register

#### 1 CONTROLSS\_CTRL\_ECAP5\_RST Register (Offset = 414h) [reset = 0h]

Ecap[x]\_reset.

Return to [Summary Table](#)

**Table 2-3674. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0414h       |

**Figure 2-1223. CONTROLSS\_CTRL\_ECAP5\_RST Name Register**

|          |    |    |    |               |    |    |    |
|----------|----|----|----|---------------|----|----|----|
| 31       | 30 | 29 | 28 | 27            | 26 | 25 | 24 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 23       | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 15       | 14 | 13 | 12 | 11            | 10 | 9  | 8  |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 7        | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| RESERVED |    |    |    | ECAP5_RST_RST |    |    |    |
| NONE     |    |    |    | R/W           |    |    |    |
| 0h       |    |    |    | 0h            |    |    |    |

**Table 2-3676. CONTROLSS\_CTRL\_ECAP5\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | ECAP5_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding ecap |

### 2.7.2.167 CONTROLSS\_CTRL\_ECAP6\_RST Register

#### 1 CONTROLSS\_CTRL\_ECAP6\_RST Register (Offset = 418h) [reset = 0h]

Ecap[x]\_reset.

Return to [Summary Table](#)

**Table 2-3677. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0418h       |

**Figure 2-1224. CONTROLSS\_CTRL\_ECAP6\_RST Name Register**

|          |    |    |    |               |    |    |    |
|----------|----|----|----|---------------|----|----|----|
| 31       | 30 | 29 | 28 | 27            | 26 | 25 | 24 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 23       | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 15       | 14 | 13 | 12 | 11            | 10 | 9  | 8  |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 7        | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| RESERVED |    |    |    | ECAP6_RST_RST |    |    |    |
| NONE     |    |    |    | R/W           |    |    |    |
| 0h       |    |    |    | 0h            |    |    |    |

**Table 2-3679. CONTROLSS\_CTRL\_ECAP6\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | ECAP6_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding ecap |

### 2.7.2.168 CONTROLSS\_CTRL\_ECAP7\_RST Register

#### 1 CONTROLSS\_CTRL\_ECAP7\_RST Register (Offset = 41Ch) [reset = 0h]

Ecap[x]\_reset.

Return to [Summary Table](#)

**Table 2-3680. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 041Ch       |

**Figure 2-1225. CONTROLSS\_CTRL\_ECAP7\_RST Name Register**

|          |    |    |    |               |    |    |    |
|----------|----|----|----|---------------|----|----|----|
| 31       | 30 | 29 | 28 | 27            | 26 | 25 | 24 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 23       | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 15       | 14 | 13 | 12 | 11            | 10 | 9  | 8  |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 7        | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| RESERVED |    |    |    | ECAP7_RST_RST |    |    |    |
| NONE     |    |    |    | R/W           |    |    |    |
| 0h       |    |    |    | 0h            |    |    |    |

**Table 2-3682. CONTROLSS\_CTRL\_ECAP7\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | ECAP7_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding ecap |



### 2.7.2.169 CONTROLSS\_CTRL\_ECAP8\_RST Register

#### 1 CONTROLSS\_CTRL\_ECAP8\_RST Register (Offset = 420h) [reset = 0h]

Ecap[x]\_reset.

Return to [Summary Table](#)

**Table 2-3683. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0420h       |

**Figure 2-1226. CONTROLSS\_CTRL\_ECAP8\_RST Name Register**

|          |    |    |    |               |    |    |    |
|----------|----|----|----|---------------|----|----|----|
| 31       | 30 | 29 | 28 | 27            | 26 | 25 | 24 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 23       | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 15       | 14 | 13 | 12 | 11            | 10 | 9  | 8  |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 7        | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| RESERVED |    |    |    | ECAP8_RST_RST |    |    |    |
| NONE     |    |    |    | R/W           |    |    |    |
| 0h       |    |    |    | 0h            |    |    |    |

**Table 2-3685. CONTROLSS\_CTRL\_ECAP8\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | ECAP8_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding ecap |

### 2.7.2.170 CONTROLSS\_CTRL\_ECAP9\_RST Register

#### 1 CONTROLSS\_CTRL\_ECAP9\_RST Register (Offset = 424h) [reset = 0h]

Ecap[x]\_reset.

Return to [Summary Table](#)

**Table 2-3686. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0424h       |

**Figure 2-1227. CONTROLSS\_CTRL\_ECAP9\_RST Name Register**

|          |    |    |    |               |    |    |    |
|----------|----|----|----|---------------|----|----|----|
| 31       | 30 | 29 | 28 | 27            | 26 | 25 | 24 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 23       | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 15       | 14 | 13 | 12 | 11            | 10 | 9  | 8  |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 7        | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| RESERVED |    |    |    | ECAP9_RST_RST |    |    |    |
| NONE     |    |    |    | R/W           |    |    |    |
| 0h       |    |    |    | 0h            |    |    |    |

**Table 2-3688. CONTROLSS\_CTRL\_ECAP9\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | ECAP9_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding ecap |

### 2.7.2.171 CONTROLSS\_CTRL\_EQEP0\_RST Register

#### 1 CONTROLSS\_CTRL\_EQEP0\_RST Register (Offset = 440h) [reset = 0h]

Eqep[x]\_reset.

Return to [Summary Table](#)

**Table 2-3689. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0440h       |

**Figure 2-1228. CONTROLSS\_CTRL\_EQEP0\_RST Name Register**

|          |    |    |    |    |               |    |    |
|----------|----|----|----|----|---------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26            | 25 | 24 |
| RESERVED |    |    |    |    |               |    |    |
| NONE     |    |    |    |    |               |    |    |
| 0h       |    |    |    |    |               |    |    |
| 23       | 22 | 21 | 20 | 19 | 18            | 17 | 16 |
| RESERVED |    |    |    |    |               |    |    |
| NONE     |    |    |    |    |               |    |    |
| 0h       |    |    |    |    |               |    |    |
| 15       | 14 | 13 | 12 | 11 | 10            | 9  | 8  |
| RESERVED |    |    |    |    |               |    |    |
| NONE     |    |    |    |    |               |    |    |
| 0h       |    |    |    |    |               |    |    |
| 7        | 6  | 5  | 4  | 3  | 2             | 1  | 0  |
| RESERVED |    |    |    |    | EQEP0_RST_RST |    |    |
| NONE     |    |    |    |    | R/W           |    |    |
| 0h       |    |    |    |    | 0h            |    |    |

**Table 2-3691. CONTROLSS\_CTRL\_EQEP0\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | EQEP0_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding eqep |

### 2.7.2.172 CONTROLSS\_CTRL\_EQEP1\_RST Register

#### 1 CONTROLSS\_CTRL\_EQEP1\_RST Register (Offset = 444h) [reset = 0h]

Eqep[x]\_reset.

Return to [Summary Table](#)

**Table 2-3692. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0444h       |

**Figure 2-1229. CONTROLSS\_CTRL\_EQEP1\_RST Name Register**

|          |    |    |    |    |               |    |    |
|----------|----|----|----|----|---------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26            | 25 | 24 |
| RESERVED |    |    |    |    |               |    |    |
| NONE     |    |    |    |    |               |    |    |
| 0h       |    |    |    |    |               |    |    |
| 23       | 22 | 21 | 20 | 19 | 18            | 17 | 16 |
| RESERVED |    |    |    |    |               |    |    |
| NONE     |    |    |    |    |               |    |    |
| 0h       |    |    |    |    |               |    |    |
| 15       | 14 | 13 | 12 | 11 | 10            | 9  | 8  |
| RESERVED |    |    |    |    |               |    |    |
| NONE     |    |    |    |    |               |    |    |
| 0h       |    |    |    |    |               |    |    |
| 7        | 6  | 5  | 4  | 3  | 2             | 1  | 0  |
| RESERVED |    |    |    |    | EQEP1_RST_RST |    |    |
| NONE     |    |    |    |    | R/W           |    |    |
| 0h       |    |    |    |    | 0h            |    |    |

**Table 2-3694. CONTROLSS\_CTRL\_EQEP1\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | EQEP1_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding eqep |

### 2.7.2.173 CONTROLSS\_CTRL\_EQEP2\_RST Register

#### 1 CONTROLSS\_CTRL\_EQEP2\_RST Register (Offset = 448h) [reset = 0h]

Eqep[x]\_reset.

Return to [Summary Table](#)

**Table 2-3695. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0448h       |

**Figure 2-1230. CONTROLSS\_CTRL\_EQEP2\_RST Name Register**

|          |    |    |    |    |               |    |    |
|----------|----|----|----|----|---------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26            | 25 | 24 |
| RESERVED |    |    |    |    |               |    |    |
| NONE     |    |    |    |    |               |    |    |
| 0h       |    |    |    |    |               |    |    |
| 23       | 22 | 21 | 20 | 19 | 18            | 17 | 16 |
| RESERVED |    |    |    |    |               |    |    |
| NONE     |    |    |    |    |               |    |    |
| 0h       |    |    |    |    |               |    |    |
| 15       | 14 | 13 | 12 | 11 | 10            | 9  | 8  |
| RESERVED |    |    |    |    |               |    |    |
| NONE     |    |    |    |    |               |    |    |
| 0h       |    |    |    |    |               |    |    |
| 7        | 6  | 5  | 4  | 3  | 2             | 1  | 0  |
| RESERVED |    |    |    |    | EQEP2_RST_RST |    |    |
| NONE     |    |    |    |    | R/W           |    |    |
| 0h       |    |    |    |    | 0h            |    |    |

**Table 2-3697. CONTROLSS\_CTRL\_EQEP2\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | EQEP2_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding eqep |

### 2.7.2.174 CONTROLSS\_CTRL\_SDFM0\_RST Register

#### 1 CONTROLSS\_CTRL\_SDFM0\_RST Register (Offset = 450h) [reset = 0h]

Sdfm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3698. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0450h       |

**Figure 2-1231. CONTROLSS\_CTRL\_SDFM0\_RST Name Register**

|          |    |    |    |               |    |    |    |
|----------|----|----|----|---------------|----|----|----|
| 31       | 30 | 29 | 28 | 27            | 26 | 25 | 24 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 23       | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 15       | 14 | 13 | 12 | 11            | 10 | 9  | 8  |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 7        | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| RESERVED |    |    |    | SDFM0_RST_RST |    |    |    |
| NONE     |    |    |    | R/W           |    |    |    |
| 0h       |    |    |    | 0h            |    |    |    |

**Table 2-3700. CONTROLSS\_CTRL\_SDFM0\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | SDFM0_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding sdfm |

### 2.7.2.175 CONTROLSS\_CTRL\_SDFM1\_RST Register

#### 1 CONTROLSS\_CTRL\_SDFM1\_RST Register (Offset = 454h) [reset = 0h]

Sdfm[x]\_reset.

Return to [Summary Table](#)

**Table 2-3701. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0454h       |

**Figure 2-1232. CONTROLSS\_CTRL\_SDFM1\_RST Name Register**

|          |    |    |    |               |    |    |    |
|----------|----|----|----|---------------|----|----|----|
| 31       | 30 | 29 | 28 | 27            | 26 | 25 | 24 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 23       | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 15       | 14 | 13 | 12 | 11            | 10 | 9  | 8  |
| RESERVED |    |    |    |               |    |    |    |
| NONE     |    |    |    |               |    |    |    |
| 0h       |    |    |    |               |    |    |    |
| 7        | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| RESERVED |    |    |    | SDFM1_RST_RST |    |    |    |
| NONE     |    |    |    | R/W           |    |    |    |
| 0h       |    |    |    | 0h            |    |    |    |

**Table 2-3703. CONTROLSS\_CTRL\_SDFM1\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | SDFM1_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding sdfm |

### 2.7.2.176 CONTROLSS\_CTRL\_DAC\_RST Register

#### 1 CONTROLSS\_CTRL\_DAC\_RST Register (Offset = 458h) [reset = 0h]

dac\_reset.

Return to [Summary Table](#)

**Table 2-3704. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0458h       |

**Figure 2-1233. CONTROLSS\_CTRL\_DAC\_RST Name Register**

|          |    |    |    |    |             |    |    |
|----------|----|----|----|----|-------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26          | 25 | 24 |
| RESERVED |    |    |    |    |             |    |    |
| NONE     |    |    |    |    |             |    |    |
| 0h       |    |    |    |    |             |    |    |
| 23       | 22 | 21 | 20 | 19 | 18          | 17 | 16 |
| RESERVED |    |    |    |    |             |    |    |
| NONE     |    |    |    |    |             |    |    |
| 0h       |    |    |    |    |             |    |    |
| 15       | 14 | 13 | 12 | 11 | 10          | 9  | 8  |
| RESERVED |    |    |    |    |             |    |    |
| NONE     |    |    |    |    |             |    |    |
| 0h       |    |    |    |    |             |    |    |
| 7        | 6  | 5  | 4  | 3  | 2           | 1  | 0  |
| RESERVED |    |    |    |    | DAC_RST_RST |    |    |
| NONE     |    |    |    |    | R/W         |    |    |
| 0h       |    |    |    |    | 0h          |    |    |

**Table 2-3706. CONTROLSS\_CTRL\_DAC\_RST Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                |
|------|-------------|------|-------|--------------------------------------------|
| 31:3 | RESERVED    | NONE | 0h    | Reserved                                   |
| 2:0  | DAC_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for dac |



### 2.7.2.177 CONTROLSS\_CTRL\_ADC0\_RST Register

#### 1 CONTROLSS\_CTRL\_ADC0\_RST Register (Offset = 45Ch) [reset = 0h]

Adc[x]\_reset.

Return to [Summary Table](#)

**Table 2-3707. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 045Ch       |

**Figure 2-1234. CONTROLSS\_CTRL\_ADC0\_RST Name Register**

|          |    |    |    |              |    |    |    |
|----------|----|----|----|--------------|----|----|----|
| 31       | 30 | 29 | 28 | 27           | 26 | 25 | 24 |
| RESERVED |    |    |    |              |    |    |    |
| NONE     |    |    |    |              |    |    |    |
| 0h       |    |    |    |              |    |    |    |
| 23       | 22 | 21 | 20 | 19           | 18 | 17 | 16 |
| RESERVED |    |    |    |              |    |    |    |
| NONE     |    |    |    |              |    |    |    |
| 0h       |    |    |    |              |    |    |    |
| 15       | 14 | 13 | 12 | 11           | 10 | 9  | 8  |
| RESERVED |    |    |    |              |    |    |    |
| NONE     |    |    |    |              |    |    |    |
| 0h       |    |    |    |              |    |    |    |
| 7        | 6  | 5  | 4  | 3            | 2  | 1  | 0  |
| RESERVED |    |    |    | ADC0_RST_RST |    |    |    |
| NONE     |    |    |    | R/W          |    |    |    |
| 0h       |    |    |    | 0h           |    |    |    |

**Table 2-3709. CONTROLSS\_CTRL\_ADC0\_RST Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                              |
|------|--------------|------|-------|----------------------------------------------------------|
| 31:3 | RESERVED     | NONE | 0h    | Reserved                                                 |
| 2:0  | ADC0_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding adc |

### 2.7.2.178 CONTROLSS\_CTRL\_ADC1\_RST Register

#### 1 CONTROLSS\_CTRL\_ADC1\_RST Register (Offset = 460h) [reset = 0h]

Adc[x]\_reset.

Return to [Summary Table](#)

**Table 2-3710. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0460h       |

**Figure 2-1235. CONTROLSS\_CTRL\_ADC1\_RST Name Register**

|          |    |    |    |    |              |    |    |
|----------|----|----|----|----|--------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26           | 25 | 24 |
| RESERVED |    |    |    |    |              |    |    |
| NONE     |    |    |    |    |              |    |    |
| 0h       |    |    |    |    |              |    |    |
| 23       | 22 | 21 | 20 | 19 | 18           | 17 | 16 |
| RESERVED |    |    |    |    |              |    |    |
| NONE     |    |    |    |    |              |    |    |
| 0h       |    |    |    |    |              |    |    |
| 15       | 14 | 13 | 12 | 11 | 10           | 9  | 8  |
| RESERVED |    |    |    |    |              |    |    |
| NONE     |    |    |    |    |              |    |    |
| 0h       |    |    |    |    |              |    |    |
| 7        | 6  | 5  | 4  | 3  | 2            | 1  | 0  |
| RESERVED |    |    |    |    | ADC1_RST_RST |    |    |
| NONE     |    |    |    |    | R/W          |    |    |
| 0h       |    |    |    |    | 0h           |    |    |

**Table 2-3712. CONTROLSS\_CTRL\_ADC1\_RST Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                              |
|------|--------------|------|-------|----------------------------------------------------------|
| 31:3 | RESERVED     | NONE | 0h    | Reserved                                                 |
| 2:0  | ADC1_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding adc |

### 2.7.2.179 CONTROLSS\_CTRL\_ADC2\_RST Register

#### 1 CONTROLSS\_CTRL\_ADC2\_RST Register (Offset = 464h) [reset = 0h]

Adc[x]\_reset.

Return to [Summary Table](#)

**Table 2-3713. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0464h       |

**Figure 2-1236. CONTROLSS\_CTRL\_ADC2\_RST Name Register**

|          |    |    |    |    |              |    |    |
|----------|----|----|----|----|--------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26           | 25 | 24 |
| RESERVED |    |    |    |    |              |    |    |
| NONE     |    |    |    |    |              |    |    |
| 0h       |    |    |    |    |              |    |    |
| 23       | 22 | 21 | 20 | 19 | 18           | 17 | 16 |
| RESERVED |    |    |    |    |              |    |    |
| NONE     |    |    |    |    |              |    |    |
| 0h       |    |    |    |    |              |    |    |
| 15       | 14 | 13 | 12 | 11 | 10           | 9  | 8  |
| RESERVED |    |    |    |    |              |    |    |
| NONE     |    |    |    |    |              |    |    |
| 0h       |    |    |    |    |              |    |    |
| 7        | 6  | 5  | 4  | 3  | 2            | 1  | 0  |
| RESERVED |    |    |    |    | ADC2_RST_RST |    |    |
| NONE     |    |    |    |    | R/W          |    |    |
| 0h       |    |    |    |    | 0h           |    |    |

**Table 2-3715. CONTROLSS\_CTRL\_ADC2\_RST Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                              |
|------|--------------|------|-------|----------------------------------------------------------|
| 31:3 | RESERVED     | NONE | 0h    | Reserved                                                 |
| 2:0  | ADC2_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding adc |

### 2.7.2.180 CONTROLSS\_CTRL\_ADC3\_RST Register

#### 1 CONTROLSS\_CTRL\_ADC3\_RST Register (Offset = 468h) [reset = 0h]

Adc[x]\_reset.

Return to [Summary Table](#)

**Table 2-3716. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0468h       |

**Figure 2-1237. CONTROLSS\_CTRL\_ADC3\_RST Name Register**

|          |    |    |    |              |    |    |    |
|----------|----|----|----|--------------|----|----|----|
| 31       | 30 | 29 | 28 | 27           | 26 | 25 | 24 |
| RESERVED |    |    |    |              |    |    |    |
| NONE     |    |    |    |              |    |    |    |
| 0h       |    |    |    |              |    |    |    |
| 23       | 22 | 21 | 20 | 19           | 18 | 17 | 16 |
| RESERVED |    |    |    |              |    |    |    |
| NONE     |    |    |    |              |    |    |    |
| 0h       |    |    |    |              |    |    |    |
| 15       | 14 | 13 | 12 | 11           | 10 | 9  | 8  |
| RESERVED |    |    |    |              |    |    |    |
| NONE     |    |    |    |              |    |    |    |
| 0h       |    |    |    |              |    |    |    |
| 7        | 6  | 5  | 4  | 3            | 2  | 1  | 0  |
| RESERVED |    |    |    | ADC3_RST_RST |    |    |    |
| NONE     |    |    |    | R/W          |    |    |    |
| 0h       |    |    |    | 0h           |    |    |    |

**Table 2-3718. CONTROLSS\_CTRL\_ADC3\_RST Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                              |
|------|--------------|------|-------|----------------------------------------------------------|
| 31:3 | RESERVED     | NONE | 0h    | Reserved                                                 |
| 2:0  | ADC3_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding adc |

### 2.7.2.181 CONTROLSS\_CTRL\_ADC4\_RST Register

#### 1 CONTROLSS\_CTRL\_ADC4\_RST Register (Offset = 46Ch) [reset = 0h]

Adc[x]\_reset.

Return to [Summary Table](#)

**Table 2-3719. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 046Ch       |

**Figure 2-1238. CONTROLSS\_CTRL\_ADC4\_RST Name Register**

|          |    |    |    |    |              |    |    |
|----------|----|----|----|----|--------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26           | 25 | 24 |
| RESERVED |    |    |    |    |              |    |    |
| NONE     |    |    |    |    |              |    |    |
| 0h       |    |    |    |    |              |    |    |
| 23       | 22 | 21 | 20 | 19 | 18           | 17 | 16 |
| RESERVED |    |    |    |    |              |    |    |
| NONE     |    |    |    |    |              |    |    |
| 0h       |    |    |    |    |              |    |    |
| 15       | 14 | 13 | 12 | 11 | 10           | 9  | 8  |
| RESERVED |    |    |    |    |              |    |    |
| NONE     |    |    |    |    |              |    |    |
| 0h       |    |    |    |    |              |    |    |
| 7        | 6  | 5  | 4  | 3  | 2            | 1  | 0  |
| RESERVED |    |    |    |    | ADC4_RST_RST |    |    |
| NONE     |    |    |    |    | R/W          |    |    |
| 0h       |    |    |    |    | 0h           |    |    |

**Table 2-3721. CONTROLSS\_CTRL\_ADC4\_RST Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                              |
|------|--------------|------|-------|----------------------------------------------------------|
| 31:3 | RESERVED     | NONE | 0h    | Reserved                                                 |
| 2:0  | ADC4_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding adc |

### 2.7.2.182 CONTROLSS\_CTRL\_OTTO0\_RST Register

#### 1 CONTROLSS\_CTRL\_OTTO0\_RST Register (Offset = 470h) [reset = 0h]

Otto[x]\_reset.

Return to [Summary Table](#)

**Table 2-3722. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0470h       |

**Figure 2-1239. CONTROLSS\_CTRL\_OTTO0\_RST Name Register**

|          |    |    |    |    |               |    |    |
|----------|----|----|----|----|---------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26            | 25 | 24 |
| RESERVED |    |    |    |    |               |    |    |
| NONE     |    |    |    |    |               |    |    |
| 0h       |    |    |    |    |               |    |    |
| 23       | 22 | 21 | 20 | 19 | 18            | 17 | 16 |
| RESERVED |    |    |    |    |               |    |    |
| NONE     |    |    |    |    |               |    |    |
| 0h       |    |    |    |    |               |    |    |
| 15       | 14 | 13 | 12 | 11 | 10            | 9  | 8  |
| RESERVED |    |    |    |    |               |    |    |
| NONE     |    |    |    |    |               |    |    |
| 0h       |    |    |    |    |               |    |    |
| 7        | 6  | 5  | 4  | 3  | 2             | 1  | 0  |
| RESERVED |    |    |    |    | OTTO0_RST_RST |    |    |
| NONE     |    |    |    |    | R/W           |    |    |
| 0h       |    |    |    |    | 0h            |    |    |

**Table 2-3724. CONTROLSS\_CTRL\_OTTO0\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | OTTO0_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding otto |

### 2.7.2.183 CONTROLSS\_CTRL\_OTTO1\_RST Register

#### 1 CONTROLSS\_CTRL\_OTTO1\_RST Register (Offset = 474h) [reset = 0h]

Otto[x]\_reset.

Return to [Summary Table](#)

**Table 2-3725. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0474h       |

**Figure 2-1240. CONTROLSS\_CTRL\_OTTO1\_RST Name Register**

|          |    |    |    |    |               |    |    |
|----------|----|----|----|----|---------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26            | 25 | 24 |
| RESERVED |    |    |    |    |               |    |    |
| NONE     |    |    |    |    |               |    |    |
| 0h       |    |    |    |    |               |    |    |
| 23       | 22 | 21 | 20 | 19 | 18            | 17 | 16 |
| RESERVED |    |    |    |    |               |    |    |
| NONE     |    |    |    |    |               |    |    |
| 0h       |    |    |    |    |               |    |    |
| 15       | 14 | 13 | 12 | 11 | 10            | 9  | 8  |
| RESERVED |    |    |    |    |               |    |    |
| NONE     |    |    |    |    |               |    |    |
| 0h       |    |    |    |    |               |    |    |
| 7        | 6  | 5  | 4  | 3  | 2             | 1  | 0  |
| RESERVED |    |    |    |    | OTTO1_RST_RST |    |    |
| NONE     |    |    |    |    | R/W           |    |    |
| 0h       |    |    |    |    | 0h            |    |    |

**Table 2-3727. CONTROLSS\_CTRL\_OTTO1\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | OTTO1_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding otto |

### 2.7.2.184 CONTROLSS\_CTRL\_OTTO2\_RST Register

#### 1 CONTROLSS\_CTRL\_OTTO2\_RST Register (Offset = 478h) [reset = 0h]

Otto[x]\_reset.

Return to [Summary Table](#)

**Table 2-3728. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0478h       |

**Figure 2-1241. CONTROLSS\_CTRL\_OTTO2\_RST Name Register**

|          |    |    |    |    |               |    |    |
|----------|----|----|----|----|---------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26            | 25 | 24 |
| RESERVED |    |    |    |    |               |    |    |
| NONE     |    |    |    |    |               |    |    |
| 0h       |    |    |    |    |               |    |    |
| 23       | 22 | 21 | 20 | 19 | 18            | 17 | 16 |
| RESERVED |    |    |    |    |               |    |    |
| NONE     |    |    |    |    |               |    |    |
| 0h       |    |    |    |    |               |    |    |
| 15       | 14 | 13 | 12 | 11 | 10            | 9  | 8  |
| RESERVED |    |    |    |    |               |    |    |
| NONE     |    |    |    |    |               |    |    |
| 0h       |    |    |    |    |               |    |    |
| 7        | 6  | 5  | 4  | 3  | 2             | 1  | 0  |
| RESERVED |    |    |    |    | OTTO2_RST_RST |    |    |
| NONE     |    |    |    |    | R/W           |    |    |
| 0h       |    |    |    |    | 0h            |    |    |

**Table 2-3730. CONTROLSS\_CTRL\_OTTO2\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | OTTO2_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding otto |



### 2.7.2.185 CONTROLSS\_CTRL\_OTTO3\_RST Register

#### 1 CONTROLSS\_CTRL\_OTTO3\_RST Register (Offset = 47Ch) [reset = 0h]

Otto[x]\_reset.

Return to [Summary Table](#)

**Table 2-3731. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 047Ch       |

**Figure 2-1242. CONTROLSS\_CTRL\_OTTO3\_RST Name Register**

|          |    |    |    |    |               |    |    |
|----------|----|----|----|----|---------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26            | 25 | 24 |
| RESERVED |    |    |    |    |               |    |    |
| NONE     |    |    |    |    |               |    |    |
| 0h       |    |    |    |    |               |    |    |
| 23       | 22 | 21 | 20 | 19 | 18            | 17 | 16 |
| RESERVED |    |    |    |    |               |    |    |
| NONE     |    |    |    |    |               |    |    |
| 0h       |    |    |    |    |               |    |    |
| 15       | 14 | 13 | 12 | 11 | 10            | 9  | 8  |
| RESERVED |    |    |    |    |               |    |    |
| NONE     |    |    |    |    |               |    |    |
| 0h       |    |    |    |    |               |    |    |
| 7        | 6  | 5  | 4  | 3  | 2             | 1  | 0  |
| RESERVED |    |    |    |    | OTTO3_RST_RST |    |    |
| NONE     |    |    |    |    | R/W           |    |    |
| 0h       |    |    |    |    | 0h            |    |    |

**Table 2-3733. CONTROLSS\_CTRL\_OTTO3\_RST Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                               |
|------|---------------|------|-------|-----------------------------------------------------------|
| 31:3 | RESERVED      | NONE | 0h    | Reserved                                                  |
| 2:0  | OTTO3_RST_RST | R/W  | 0h    | Writing 3'b111 will generate reset for corresponding otto |

### 2.7.2.186 CONTROLSS\_CTRL\_EPWM0\_HALTEN Register

#### 1 CONTROLSS\_CTRL\_EPWM0\_HALTEN Register (Offset = 500h) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3734. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0500h       |

**Figure 2-1243. CONTROLSS\_CTRL\_EPWM0\_HALTEN Name Register**

|          |    |    |    |                        |                        |                        |                        |
|----------|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 31       | 30 | 29 | 28 | 27                     | 26                     | 25                     | 24                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 23       | 22 | 21 | 20 | 19                     | 18                     | 17                     | 16                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 15       | 14 | 13 | 12 | 11                     | 10                     | 9                      | 8                      |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 7        | 6  | 5  | 4  | 3                      | 2                      | 1                      | 0                      |
| RESERVED |    |    |    | EPWM0_HALT<br>EN_CR5B1 | EPWM0_HALT<br>EN_CR5A1 | EPWM0_HALT<br>EN_CR5B0 | EPWM0_HALT<br>EN_CR5A0 |
| NONE     |    |    |    | R/W                    | R/W                    | R/W                    | R/W                    |
| 0h       |    |    |    | 0h                     | 0h                     | 0h                     | 0h                     |

**Table 2-3736. CONTROLSS\_CTRL\_EPWM0\_HALTEN Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                         |
|------|--------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED           | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM0_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM0_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM0_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM0_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

### 2.7.2.187 CONTROLSS\_CTRL\_EPWM1\_HALTEN Register

#### 1 CONTROLSS\_CTRL\_EPWM1\_HALTEN Register (Offset = 504h) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3737. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0504h       |

**Figure 2-1244. CONTROLSS\_CTRL\_EPWM1\_HALTEN Name Register**

|          |    |    |    |                        |                        |                        |                        |
|----------|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 31       | 30 | 29 | 28 | 27                     | 26                     | 25                     | 24                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 23       | 22 | 21 | 20 | 19                     | 18                     | 17                     | 16                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 15       | 14 | 13 | 12 | 11                     | 10                     | 9                      | 8                      |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 7        | 6  | 5  | 4  | 3                      | 2                      | 1                      | 0                      |
| RESERVED |    |    |    | EPWM1_HALT<br>EN_CR5B1 | EPWM1_HALT<br>EN_CR5A1 | EPWM1_HALT<br>EN_CR5B0 | EPWM1_HALT<br>EN_CR5A0 |
| NONE     |    |    |    | R/W                    | R/W                    | R/W                    | R/W                    |
| 0h       |    |    |    | 0h                     | 0h                     | 0h                     | 0h                     |

**Table 2-3739. CONTROLSS\_CTRL\_EPWM1\_HALTEN Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                         |
|------|--------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED           | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM1_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM1_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM1_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM1_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

### 2.7.2.188 CONTROLSS\_CTRL\_EPWM2\_HALTEN Register

#### 1 CONTROLSS\_CTRL\_EPWM2\_HALTEN Register (Offset = 508h) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3740. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0508h       |

**Figure 2-1245. CONTROLSS\_CTRL\_EPWM2\_HALTEN Name Register**

|          |    |    |    |                        |                        |                        |                        |
|----------|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 31       | 30 | 29 | 28 | 27                     | 26                     | 25                     | 24                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 23       | 22 | 21 | 20 | 19                     | 18                     | 17                     | 16                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 15       | 14 | 13 | 12 | 11                     | 10                     | 9                      | 8                      |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 7        | 6  | 5  | 4  | 3                      | 2                      | 1                      | 0                      |
| RESERVED |    |    |    | EPWM2_HALT<br>EN_CR5B1 | EPWM2_HALT<br>EN_CR5A1 | EPWM2_HALT<br>EN_CR5B0 | EPWM2_HALT<br>EN_CR5A0 |
| NONE     |    |    |    | R/W                    | R/W                    | R/W                    | R/W                    |
| 0h       |    |    |    | 0h                     | 0h                     | 0h                     | 0h                     |

**Table 2-3742. CONTROLSS\_CTRL\_EPWM2\_HALTEN Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                         |
|------|--------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED           | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM2_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM2_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM2_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM2_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

### 2.7.2.189 CONTROLSS\_CTRL\_EPWM3\_HALTEN Register

#### 1 CONTROLSS\_CTRL\_EPWM3\_HALTEN Register (Offset = 50Ch) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3743. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 050Ch       |

**Figure 2-1246. CONTROLSS\_CTRL\_EPWM3\_HALTEN Name Register**

|          |    |    |    |                        |                        |                        |                        |
|----------|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 31       | 30 | 29 | 28 | 27                     | 26                     | 25                     | 24                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 23       | 22 | 21 | 20 | 19                     | 18                     | 17                     | 16                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 15       | 14 | 13 | 12 | 11                     | 10                     | 9                      | 8                      |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 7        | 6  | 5  | 4  | 3                      | 2                      | 1                      | 0                      |
| RESERVED |    |    |    | EPWM3_HALT<br>EN_CR5B1 | EPWM3_HALT<br>EN_CR5A1 | EPWM3_HALT<br>EN_CR5B0 | EPWM3_HALT<br>EN_CR5A0 |
| NONE     |    |    |    | R/W                    | R/W                    | R/W                    | R/W                    |
| 0h       |    |    |    | 0h                     | 0h                     | 0h                     | 0h                     |

**Table 2-3745. CONTROLSS\_CTRL\_EPWM3\_HALTEN Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                         |
|------|--------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED           | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM3_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM3_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM3_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM3_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

### 2.7.2.190 CONTROLSS\_CTRL\_EPWM4\_HALTEN Register

#### 1 CONTROLSS\_CTRL\_EPWM4\_HALTEN Register (Offset = 510h) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3746. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0510h       |

**Figure 2-1247. CONTROLSS\_CTRL\_EPWM4\_HALTEN Name Register**

|          |    |    |    |                        |                        |                        |                        |
|----------|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 31       | 30 | 29 | 28 | 27                     | 26                     | 25                     | 24                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 23       | 22 | 21 | 20 | 19                     | 18                     | 17                     | 16                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 15       | 14 | 13 | 12 | 11                     | 10                     | 9                      | 8                      |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 7        | 6  | 5  | 4  | 3                      | 2                      | 1                      | 0                      |
| RESERVED |    |    |    | EPWM4_HALT<br>EN_CR5B1 | EPWM4_HALT<br>EN_CR5A1 | EPWM4_HALT<br>EN_CR5B0 | EPWM4_HALT<br>EN_CR5A0 |
| NONE     |    |    |    | R/W                    | R/W                    | R/W                    | R/W                    |
| 0h       |    |    |    | 0h                     | 0h                     | 0h                     | 0h                     |

**Table 2-3748. CONTROLSS\_CTRL\_EPWM4\_HALTEN Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                         |
|------|--------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED           | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM4_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM4_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM4_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM4_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.191 CONTROLSS\_CTRL\_EPWM5 HALTEN Register

### 1 CONTROLSS\_CTRL\_EPWM5 HALTEN Register (Offset = 514h) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3749. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0514h       |

**Figure 2-1248. CONTROLSS\_CTRL\_EPWM5 HALTEN Name Register**

|          |    |    |    |                        |                        |                        |                        |
|----------|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 31       | 30 | 29 | 28 | 27                     | 26                     | 25                     | 24                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 23       | 22 | 21 | 20 | 19                     | 18                     | 17                     | 16                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 15       | 14 | 13 | 12 | 11                     | 10                     | 9                      | 8                      |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 7        | 6  | 5  | 4  | 3                      | 2                      | 1                      | 0                      |
| RESERVED |    |    |    | EPWM5_HALT<br>EN_CR5B1 | EPWM5_HALT<br>EN_CR5A1 | EPWM5_HALT<br>EN_CR5B0 | EPWM5_HALT<br>EN_CR5A0 |
| NONE     |    |    |    | R/W                    | R/W                    | R/W                    | R/W                    |
| 0h       |    |    |    | 0h                     | 0h                     | 0h                     | 0h                     |

**Table 2-3751. CONTROLSS\_CTRL\_EPWM5 HALTEN Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                         |
|------|--------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED           | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM5_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM5_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM5_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM5_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

### 2.7.2.192 CONTROLSS\_CTRL\_EPWM6\_HALTEN Register

#### 1 CONTROLSS\_CTRL\_EPWM6\_HALTEN Register (Offset = 518h) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3752. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0518h       |

**Figure 2-1249. CONTROLSS\_CTRL\_EPWM6\_HALTEN Name Register**

|          |    |    |    |                        |                        |                        |                        |
|----------|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 31       | 30 | 29 | 28 | 27                     | 26                     | 25                     | 24                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 23       | 22 | 21 | 20 | 19                     | 18                     | 17                     | 16                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 15       | 14 | 13 | 12 | 11                     | 10                     | 9                      | 8                      |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 7        | 6  | 5  | 4  | 3                      | 2                      | 1                      | 0                      |
| RESERVED |    |    |    | EPWM6_HALT<br>EN_CR5B1 | EPWM6_HALT<br>EN_CR5A1 | EPWM6_HALT<br>EN_CR5B0 | EPWM6_HALT<br>EN_CR5A0 |
| NONE     |    |    |    | R/W                    | R/W                    | R/W                    | R/W                    |
| 0h       |    |    |    | 0h                     | 0h                     | 0h                     | 0h                     |

**Table 2-3754. CONTROLSS\_CTRL\_EPWM6\_HALTEN Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                         |
|------|--------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED           | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM6_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM6_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM6_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM6_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |



### 2.7.2.193 CONTROLSS\_CTRL\_EPWM7\_HALTEN Register

#### 1 CONTROLSS\_CTRL\_EPWM7\_HALTEN Register (Offset = 51Ch) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3755. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 051Ch       |

**Figure 2-1250. CONTROLSS\_CTRL\_EPWM7\_HALTEN Name Register**

|          |    |    |    |                        |                        |                        |                        |
|----------|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 31       | 30 | 29 | 28 | 27                     | 26                     | 25                     | 24                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 23       | 22 | 21 | 20 | 19                     | 18                     | 17                     | 16                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 15       | 14 | 13 | 12 | 11                     | 10                     | 9                      | 8                      |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 7        | 6  | 5  | 4  | 3                      | 2                      | 1                      | 0                      |
| RESERVED |    |    |    | EPWM7_HALT<br>EN_CR5B1 | EPWM7_HALT<br>EN_CR5A1 | EPWM7_HALT<br>EN_CR5B0 | EPWM7_HALT<br>EN_CR5A0 |
| NONE     |    |    |    | R/W                    | R/W                    | R/W                    | R/W                    |
| 0h       |    |    |    | 0h                     | 0h                     | 0h                     | 0h                     |

**Table 2-3757. CONTROLSS\_CTRL\_EPWM7\_HALTEN Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                         |
|------|--------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED           | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM7_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM7_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM7_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM7_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

### 2.7.2.194 CONTROLSS\_CTRL\_EPWM8\_HALTEN Register

#### 1 CONTROLSS\_CTRL\_EPWM8\_HALTEN Register (Offset = 520h) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3758. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0520h       |

**Figure 2-1251. CONTROLSS\_CTRL\_EPWM8\_HALTEN Name Register**

|          |    |    |    |                        |                        |                        |                        |
|----------|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 31       | 30 | 29 | 28 | 27                     | 26                     | 25                     | 24                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 23       | 22 | 21 | 20 | 19                     | 18                     | 17                     | 16                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 15       | 14 | 13 | 12 | 11                     | 10                     | 9                      | 8                      |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 7        | 6  | 5  | 4  | 3                      | 2                      | 1                      | 0                      |
| RESERVED |    |    |    | EPWM8_HALT<br>EN_CR5B1 | EPWM8_HALT<br>EN_CR5A1 | EPWM8_HALT<br>EN_CR5B0 | EPWM8_HALT<br>EN_CR5A0 |
| NONE     |    |    |    | R/W                    | R/W                    | R/W                    | R/W                    |
| 0h       |    |    |    | 0h                     | 0h                     | 0h                     | 0h                     |

**Table 2-3760. CONTROLSS\_CTRL\_EPWM8\_HALTEN Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                         |
|------|--------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED           | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM8_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM8_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM8_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM8_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.195 CONTROLSS\_CTRL\_EPWM9 HALTEN Register

### 1 CONTROLSS\_CTRL\_EPWM9 HALTEN Register (Offset = 524h) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3761. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0524h       |

**Figure 2-1252. CONTROLSS\_CTRL\_EPWM9 HALTEN Name Register**

|          |    |    |    |                        |                        |                        |                        |
|----------|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 31       | 30 | 29 | 28 | 27                     | 26                     | 25                     | 24                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 23       | 22 | 21 | 20 | 19                     | 18                     | 17                     | 16                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 15       | 14 | 13 | 12 | 11                     | 10                     | 9                      | 8                      |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 7        | 6  | 5  | 4  | 3                      | 2                      | 1                      | 0                      |
| RESERVED |    |    |    | EPWM9_HALT<br>EN_CR5B1 | EPWM9_HALT<br>EN_CR5A1 | EPWM9_HALT<br>EN_CR5B0 | EPWM9_HALT<br>EN_CR5A0 |
| NONE     |    |    |    | R/W                    | R/W                    | R/W                    | R/W                    |
| 0h       |    |    |    | 0h                     | 0h                     | 0h                     | 0h                     |

**Table 2-3763. CONTROLSS\_CTRL\_EPWM9 HALTEN Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                         |
|------|--------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED           | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM9_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM9_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM9_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM9_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.196 CONTROLSS\_CTRL\_EPWM10 HALTEN Register

### 1 CONTROLSS\_CTRL\_EPWM10 HALTEN Register (Offset = 528h) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3764. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0528h       |

**Figure 2-1253. CONTROLSS\_CTRL\_EPWM10 HALTEN Name Register**

|          |    |    |    |                         |                         |                         |                         |
|----------|----|----|----|-------------------------|-------------------------|-------------------------|-------------------------|
| 31       | 30 | 29 | 28 | 27                      | 26                      | 25                      | 24                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 23       | 22 | 21 | 20 | 19                      | 18                      | 17                      | 16                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 15       | 14 | 13 | 12 | 11                      | 10                      | 9                       | 8                       |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 7        | 6  | 5  | 4  | 3                       | 2                       | 1                       | 0                       |
| RESERVED |    |    |    | EPWM10_HAL<br>TEN_CR5B1 | EPWM10_HAL<br>TEN_CR5A1 | EPWM10_HAL<br>TEN_CR5B0 | EPWM10_HAL<br>TEN_CR5A0 |
| NONE     |    |    |    | R/W                     | R/W                     | R/W                     | R/W                     |
| 0h       |    |    |    | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 2-3766. CONTROLSS\_CTRL\_EPWM10 HALTEN Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                                                                                         |
|------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM10_HALTEN_CR5B<br>1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM10_HALTEN_CR5A<br>1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM10_HALTEN_CR5B<br>0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM10_HALTEN_CR5A<br>0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

### 2.7.2.197 CONTROLSS\_CTRL\_EPWM11\_HALTEN Register

#### 1 CONTROLSS\_CTRL\_EPWM11\_HALTEN Register (Offset = 52Ch) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3767. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 052Ch       |

**Figure 2-1254. CONTROLSS\_CTRL\_EPWM11\_HALTEN Name Register**

|          |    |    |    |                         |                         |                         |                         |
|----------|----|----|----|-------------------------|-------------------------|-------------------------|-------------------------|
| 31       | 30 | 29 | 28 | 27                      | 26                      | 25                      | 24                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 23       | 22 | 21 | 20 | 19                      | 18                      | 17                      | 16                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 15       | 14 | 13 | 12 | 11                      | 10                      | 9                       | 8                       |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 7        | 6  | 5  | 4  | 3                       | 2                       | 1                       | 0                       |
| RESERVED |    |    |    | EPWM11_HALT<br>EN_CR5B1 | EPWM11_HALT<br>EN_CR5A1 | EPWM11_HALT<br>EN_CR5B0 | EPWM11_HALT<br>EN_CR5A0 |
| NONE     |    |    |    | R/W                     | R/W                     | R/W                     | R/W                     |
| 0h       |    |    |    | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 2-3769. CONTROLSS\_CTRL\_EPWM11\_HALTEN Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                         |
|------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED            | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM11_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM11_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM11_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM11_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.198 CONTROLSS\_CTRL\_EPWM12\_HALTEN Register

### 1 CONTROLSS\_CTRL\_EPWM12\_HALTEN Register (Offset = 530h) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3770. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0530h       |

**Figure 2-1255. CONTROLSS\_CTRL\_EPWM12\_HALTEN Name Register**

|          |    |    |    |                         |                         |                         |                         |
|----------|----|----|----|-------------------------|-------------------------|-------------------------|-------------------------|
| 31       | 30 | 29 | 28 | 27                      | 26                      | 25                      | 24                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 23       | 22 | 21 | 20 | 19                      | 18                      | 17                      | 16                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 15       | 14 | 13 | 12 | 11                      | 10                      | 9                       | 8                       |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 7        | 6  | 5  | 4  | 3                       | 2                       | 1                       | 0                       |
| RESERVED |    |    |    | EPWM12_HAL<br>TEN_CR5B1 | EPWM12_HAL<br>TEN_CR5A1 | EPWM12_HAL<br>TEN_CR5B0 | EPWM12_HAL<br>TEN_CR5A0 |
| NONE     |    |    |    | R/W                     | R/W                     | R/W                     | R/W                     |
| 0h       |    |    |    | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 2-3772. CONTROLSS\_CTRL\_EPWM12\_HALTEN Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                                                                                         |
|------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM12_HALTEN_CR5B<br>1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM12_HALTEN_CR5A<br>1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM12_HALTEN_CR5B<br>0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM12_HALTEN_CR5A<br>0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

### 2.7.2.199 CONTROLSS\_CTRL\_EPWM13 HALTEN Register

#### 1 CONTROLSS\_CTRL\_EPWM13 HALTEN Register (Offset = 534h) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3773. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0534h       |

**Figure 2-1256. CONTROLSS\_CTRL\_EPWM13 HALTEN Name Register**

|          |    |    |    |                         |                         |                         |                         |
|----------|----|----|----|-------------------------|-------------------------|-------------------------|-------------------------|
| 31       | 30 | 29 | 28 | 27                      | 26                      | 25                      | 24                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 23       | 22 | 21 | 20 | 19                      | 18                      | 17                      | 16                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 15       | 14 | 13 | 12 | 11                      | 10                      | 9                       | 8                       |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 7        | 6  | 5  | 4  | 3                       | 2                       | 1                       | 0                       |
| RESERVED |    |    |    | EPWM13_HAL<br>TEN_CR5B1 | EPWM13_HAL<br>TEN_CR5A1 | EPWM13_HAL<br>TEN_CR5B0 | EPWM13_HAL<br>TEN_CR5A0 |
| NONE     |    |    |    | R/W                     | R/W                     | R/W                     | R/W                     |
| 0h       |    |    |    | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 2-3775. CONTROLSS\_CTRL\_EPWM13 HALTEN Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                                                                                         |
|------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM13_HALTEN_CR5B<br>1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM13_HALTEN_CR5A<br>1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM13_HALTEN_CR5B<br>0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM13_HALTEN_CR5A<br>0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.200 CONTROLSS\_CTRL\_EPWM14 HALTEN Register

### 1 CONTROLSS\_CTRL\_EPWM14 HALTEN Register (Offset = 538h) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3776. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0538h       |

**Figure 2-1257. CONTROLSS\_CTRL\_EPWM14 HALTEN Name Register**

|          |    |    |    |                         |                         |                         |                         |
|----------|----|----|----|-------------------------|-------------------------|-------------------------|-------------------------|
| 31       | 30 | 29 | 28 | 27                      | 26                      | 25                      | 24                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 23       | 22 | 21 | 20 | 19                      | 18                      | 17                      | 16                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 15       | 14 | 13 | 12 | 11                      | 10                      | 9                       | 8                       |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 7        | 6  | 5  | 4  | 3                       | 2                       | 1                       | 0                       |
| RESERVED |    |    |    | EPWM14_HAL<br>TEN_CR5B1 | EPWM14_HAL<br>TEN_CR5A1 | EPWM14_HAL<br>TEN_CR5B0 | EPWM14_HAL<br>TEN_CR5A0 |
| NONE     |    |    |    | R/W                     | R/W                     | R/W                     | R/W                     |
| 0h       |    |    |    | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 2-3778. CONTROLSS\_CTRL\_EPWM14 HALTEN Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                         |
|------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED            | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM14_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM14_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM14_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM14_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |



### 2.7.2.201 CONTROLSS\_CTRL\_EPWM15\_HALTEN Register

#### 1 CONTROLSS\_CTRL\_EPWM15\_HALTEN Register (Offset = 53Ch) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3779. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 053Ch       |

**Figure 2-1258. CONTROLSS\_CTRL\_EPWM15\_HALTEN Name Register**

|          |    |    |    |                         |                         |                         |                         |
|----------|----|----|----|-------------------------|-------------------------|-------------------------|-------------------------|
| 31       | 30 | 29 | 28 | 27                      | 26                      | 25                      | 24                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 23       | 22 | 21 | 20 | 19                      | 18                      | 17                      | 16                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 15       | 14 | 13 | 12 | 11                      | 10                      | 9                       | 8                       |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 7        | 6  | 5  | 4  | 3                       | 2                       | 1                       | 0                       |
| RESERVED |    |    |    | EPWM15_HAL<br>TEN_CR5B1 | EPWM15_HAL<br>TEN_CR5A1 | EPWM15_HAL<br>TEN_CR5B0 | EPWM15_HAL<br>TEN_CR5A0 |
| NONE     |    |    |    | R/W                     | R/W                     | R/W                     | R/W                     |
| 0h       |    |    |    | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 2-3781. CONTROLSS\_CTRL\_EPWM15\_HALTEN Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                                                                                         |
|------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM15_HALTEN_CR5B<br>1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM15_HALTEN_CR5A<br>1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM15_HALTEN_CR5B<br>0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM15_HALTEN_CR5A<br>0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.202 CONTROLSS\_CTRL\_EPWM16 HALTEN Register

### 1 CONTROLSS\_CTRL\_EPWM16 HALTEN Register (Offset = 540h) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3782. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0540h       |

**Figure 2-1259. CONTROLSS\_CTRL\_EPWM16 HALTEN Name Register**

|          |    |    |    |                         |                         |                         |                         |
|----------|----|----|----|-------------------------|-------------------------|-------------------------|-------------------------|
| 31       | 30 | 29 | 28 | 27                      | 26                      | 25                      | 24                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 23       | 22 | 21 | 20 | 19                      | 18                      | 17                      | 16                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 15       | 14 | 13 | 12 | 11                      | 10                      | 9                       | 8                       |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 7        | 6  | 5  | 4  | 3                       | 2                       | 1                       | 0                       |
| RESERVED |    |    |    | EPWM16_HAL<br>TEN_CR5B1 | EPWM16_HAL<br>TEN_CR5A1 | EPWM16_HAL<br>TEN_CR5B0 | EPWM16_HAL<br>TEN_CR5A0 |
| NONE     |    |    |    | R/W                     | R/W                     | R/W                     | R/W                     |
| 0h       |    |    |    | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 2-3784. CONTROLSS\_CTRL\_EPWM16 HALTEN Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                         |
|------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED            | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM16_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM16_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM16_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM16_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

### 2.7.2.203 CONTROLSS\_CTRL\_EPWM17\_HALTEN Register

#### 1 CONTROLSS\_CTRL\_EPWM17\_HALTEN Register (Offset = 544h) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3785. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0544h       |

**Figure 2-1260. CONTROLSS\_CTRL\_EPWM17\_HALTEN Name Register**

|          |    |    |    |                         |                         |                         |                         |
|----------|----|----|----|-------------------------|-------------------------|-------------------------|-------------------------|
| 31       | 30 | 29 | 28 | 27                      | 26                      | 25                      | 24                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 23       | 22 | 21 | 20 | 19                      | 18                      | 17                      | 16                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 15       | 14 | 13 | 12 | 11                      | 10                      | 9                       | 8                       |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 7        | 6  | 5  | 4  | 3                       | 2                       | 1                       | 0                       |
| RESERVED |    |    |    | EPWM17_HAL<br>TEN_CR5B1 | EPWM17_HAL<br>TEN_CR5A1 | EPWM17_HAL<br>TEN_CR5B0 | EPWM17_HAL<br>TEN_CR5A0 |
| NONE     |    |    |    | R/W                     | R/W                     | R/W                     | R/W                     |
| 0h       |    |    |    | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 2-3787. CONTROLSS\_CTRL\_EPWM17\_HALTEN Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                         |
|------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED            | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM17_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM17_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM17_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM17_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.204 CONTROLSS\_CTRL\_EPWM18\_HALTEN Register

### 1 CONTROLSS\_CTRL\_EPWM18\_HALTEN Register (Offset = 548h) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3788. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0548h       |

**Figure 2-1261. CONTROLSS\_CTRL\_EPWM18\_HALTEN Name Register**

|          |    |    |    |                         |                         |                         |                         |
|----------|----|----|----|-------------------------|-------------------------|-------------------------|-------------------------|
| 31       | 30 | 29 | 28 | 27                      | 26                      | 25                      | 24                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 23       | 22 | 21 | 20 | 19                      | 18                      | 17                      | 16                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 15       | 14 | 13 | 12 | 11                      | 10                      | 9                       | 8                       |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 7        | 6  | 5  | 4  | 3                       | 2                       | 1                       | 0                       |
| RESERVED |    |    |    | EPWM18_HAL<br>TEN_CR5B1 | EPWM18_HAL<br>TEN_CR5A1 | EPWM18_HAL<br>TEN_CR5B0 | EPWM18_HAL<br>TEN_CR5A0 |
| NONE     |    |    |    | R/W                     | R/W                     | R/W                     | R/W                     |
| 0h       |    |    |    | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 2-3790. CONTROLSS\_CTRL\_EPWM18\_HALTEN Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                                                                                         |
|------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM18_HALTEN_CR5B<br>1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM18_HALTEN_CR5A<br>1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM18_HALTEN_CR5B<br>0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM18_HALTEN_CR5A<br>0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.205 CONTROLSS\_CTRL\_EPWM19 HALTEN Register

### 1 CONTROLSS\_CTRL\_EPWM19 HALTEN Register (Offset = 54Ch) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3791. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 054Ch       |

**Figure 2-1262. CONTROLSS\_CTRL\_EPWM19 HALTEN Name Register**

|          |    |    |    |                         |                         |                         |                         |
|----------|----|----|----|-------------------------|-------------------------|-------------------------|-------------------------|
| 31       | 30 | 29 | 28 | 27                      | 26                      | 25                      | 24                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 23       | 22 | 21 | 20 | 19                      | 18                      | 17                      | 16                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 15       | 14 | 13 | 12 | 11                      | 10                      | 9                       | 8                       |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 7        | 6  | 5  | 4  | 3                       | 2                       | 1                       | 0                       |
| RESERVED |    |    |    | EPWM19_HAL<br>TEN_CR5B1 | EPWM19_HAL<br>TEN_CR5A1 | EPWM19_HAL<br>TEN_CR5B0 | EPWM19_HAL<br>TEN_CR5A0 |
| NONE     |    |    |    | R/W                     | R/W                     | R/W                     | R/W                     |
| 0h       |    |    |    | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 2-3793. CONTROLSS\_CTRL\_EPWM19 HALTEN Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                         |
|------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED            | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM19_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM19_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM19_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM19_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.206 CONTROLSS\_CTRL\_EPWM20 HALTEN Register

### 1 CONTROLSS\_CTRL\_EPWM20 HALTEN Register (Offset = 550h) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3794. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0550h       |

**Figure 2-1263. CONTROLSS\_CTRL\_EPWM20 HALTEN Name Register**

|          |    |    |    |                         |                         |                         |                         |
|----------|----|----|----|-------------------------|-------------------------|-------------------------|-------------------------|
| 31       | 30 | 29 | 28 | 27                      | 26                      | 25                      | 24                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 23       | 22 | 21 | 20 | 19                      | 18                      | 17                      | 16                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 15       | 14 | 13 | 12 | 11                      | 10                      | 9                       | 8                       |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 7        | 6  | 5  | 4  | 3                       | 2                       | 1                       | 0                       |
| RESERVED |    |    |    | EPWM20_HAL<br>TEN_CR5B1 | EPWM20_HAL<br>TEN_CR5A1 | EPWM20_HAL<br>TEN_CR5B0 | EPWM20_HAL<br>TEN_CR5A0 |
| NONE     |    |    |    | R/W                     | R/W                     | R/W                     | R/W                     |
| 0h       |    |    |    | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 2-3796. CONTROLSS\_CTRL\_EPWM20 HALTEN Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                         |
|------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED            | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM20_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM20_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM20_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM20_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.207 CONTROLSS\_CTRL\_EPWM21\_HALTEN Register

### 1 CONTROLSS\_CTRL\_EPWM21\_HALTEN Register (Offset = 554h) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3797. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0554h       |

**Figure 2-1264. CONTROLSS\_CTRL\_EPWM21\_HALTEN Name Register**

|          |    |    |    |                         |                         |                         |                         |
|----------|----|----|----|-------------------------|-------------------------|-------------------------|-------------------------|
| 31       | 30 | 29 | 28 | 27                      | 26                      | 25                      | 24                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 23       | 22 | 21 | 20 | 19                      | 18                      | 17                      | 16                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 15       | 14 | 13 | 12 | 11                      | 10                      | 9                       | 8                       |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 7        | 6  | 5  | 4  | 3                       | 2                       | 1                       | 0                       |
| RESERVED |    |    |    | EPWM21_HAL<br>TEN_CR5B1 | EPWM21_HAL<br>TEN_CR5A1 | EPWM21_HAL<br>TEN_CR5B0 | EPWM21_HAL<br>TEN_CR5A0 |
| NONE     |    |    |    | R/W                     | R/W                     | R/W                     | R/W                     |
| 0h       |    |    |    | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 2-3799. CONTROLSS\_CTRL\_EPWM21\_HALTEN Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                         |
|------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED            | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM21_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM21_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM21_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM21_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

### 2.7.2.208 CONTROLSS\_CTRL\_EPWM22\_HALTEN Register

#### 1 CONTROLSS\_CTRL\_EPWM22\_HALTEN Register (Offset = 558h) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3800. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0558h       |

**Figure 2-1265. CONTROLSS\_CTRL\_EPWM22\_HALTEN Name Register**

|          |    |    |    |                         |                         |                         |                         |
|----------|----|----|----|-------------------------|-------------------------|-------------------------|-------------------------|
| 31       | 30 | 29 | 28 | 27                      | 26                      | 25                      | 24                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 23       | 22 | 21 | 20 | 19                      | 18                      | 17                      | 16                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 15       | 14 | 13 | 12 | 11                      | 10                      | 9                       | 8                       |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 7        | 6  | 5  | 4  | 3                       | 2                       | 1                       | 0                       |
| RESERVED |    |    |    | EPWM22_HAL<br>TEN_CR5B1 | EPWM22_HAL<br>TEN_CR5A1 | EPWM22_HAL<br>TEN_CR5B0 | EPWM22_HAL<br>TEN_CR5A0 |
| NONE     |    |    |    | R/W                     | R/W                     | R/W                     | R/W                     |
| 0h       |    |    |    | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 2-3802. CONTROLSS\_CTRL\_EPWM22\_HALTEN Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                                                                                         |
|------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM22_HALTEN_CR5B<br>1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM22_HALTEN_CR5A<br>1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM22_HALTEN_CR5B<br>0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM22_HALTEN_CR5A<br>0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |



### 2.7.2.209 CONTROLSS\_CTRL\_EPWM23\_HALTEN Register

#### 1 CONTROLSS\_CTRL\_EPWM23\_HALTEN Register (Offset = 55Ch) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3803. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 055Ch       |

**Figure 2-1266. CONTROLSS\_CTRL\_EPWM23\_HALTEN Name Register**

|          |    |    |    |                         |                         |                         |                         |
|----------|----|----|----|-------------------------|-------------------------|-------------------------|-------------------------|
| 31       | 30 | 29 | 28 | 27                      | 26                      | 25                      | 24                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 23       | 22 | 21 | 20 | 19                      | 18                      | 17                      | 16                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 15       | 14 | 13 | 12 | 11                      | 10                      | 9                       | 8                       |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 7        | 6  | 5  | 4  | 3                       | 2                       | 1                       | 0                       |
| RESERVED |    |    |    | EPWM23_HAL<br>TEN_CR5B1 | EPWM23_HAL<br>TEN_CR5A1 | EPWM23_HAL<br>TEN_CR5B0 | EPWM23_HAL<br>TEN_CR5A0 |
| NONE     |    |    |    | R/W                     | R/W                     | R/W                     | R/W                     |
| 0h       |    |    |    | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 2-3805. CONTROLSS\_CTRL\_EPWM23\_HALTEN Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                                                                                         |
|------|-------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED                | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM23_HALTEN_CR5B<br>1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM23_HALTEN_CR5A<br>1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM23_HALTEN_CR5B<br>0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM23_HALTEN_CR5A<br>0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

### 2.7.2.210 CONTROLSS\_CTRL\_EPWM24 HALTEN Register

#### 1 CONTROLSS\_CTRL\_EPWM24 HALTEN Register (Offset = 560h) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3806. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0560h       |

**Figure 2-1267. CONTROLSS\_CTRL\_EPWM24 HALTEN Name Register**

|          |    |    |    |                         |                         |                         |                         |
|----------|----|----|----|-------------------------|-------------------------|-------------------------|-------------------------|
| 31       | 30 | 29 | 28 | 27                      | 26                      | 25                      | 24                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 23       | 22 | 21 | 20 | 19                      | 18                      | 17                      | 16                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 15       | 14 | 13 | 12 | 11                      | 10                      | 9                       | 8                       |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 7        | 6  | 5  | 4  | 3                       | 2                       | 1                       | 0                       |
| RESERVED |    |    |    | EPWM24_HAL<br>TEN_CR5B1 | EPWM24_HAL<br>TEN_CR5A1 | EPWM24_HAL<br>TEN_CR5B0 | EPWM24_HAL<br>TEN_CR5A0 |
| NONE     |    |    |    | R/W                     | R/W                     | R/W                     | R/W                     |
| 0h       |    |    |    | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 2-3808. CONTROLSS\_CTRL\_EPWM24 HALTEN Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                         |
|------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED            | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM24_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM24_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM24_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM24_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

### 2.7.2.211 CONTROLSS\_CTRL\_EPWM25 HALTEN Register

#### 1 CONTROLSS\_CTRL\_EPWM25 HALTEN Register (Offset = 564h) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3809. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0564h       |

**Figure 2-1268. CONTROLSS\_CTRL\_EPWM25 HALTEN Name Register**

|          |    |    |    |                         |                         |                         |                         |
|----------|----|----|----|-------------------------|-------------------------|-------------------------|-------------------------|
| 31       | 30 | 29 | 28 | 27                      | 26                      | 25                      | 24                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 23       | 22 | 21 | 20 | 19                      | 18                      | 17                      | 16                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 15       | 14 | 13 | 12 | 11                      | 10                      | 9                       | 8                       |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 7        | 6  | 5  | 4  | 3                       | 2                       | 1                       | 0                       |
| RESERVED |    |    |    | EPWM25_HAL<br>TEN_CR5B1 | EPWM25_HAL<br>TEN_CR5A1 | EPWM25_HAL<br>TEN_CR5B0 | EPWM25_HAL<br>TEN_CR5A0 |
| NONE     |    |    |    | R/W                     | R/W                     | R/W                     | R/W                     |
| 0h       |    |    |    | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 2-3811. CONTROLSS\_CTRL\_EPWM25 HALTEN Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                         |
|------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED            | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM25_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM25_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM25_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM25_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.212 CONTROLSS\_CTRL\_EPWM26 HALTEN Register

### 1 CONTROLSS\_CTRL\_EPWM26 HALTEN Register (Offset = 568h) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3812. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0568h       |

**Figure 2-1269. CONTROLSS\_CTRL\_EPWM26 HALTEN Name Register**

|          |    |    |    |                         |                         |                         |                         |
|----------|----|----|----|-------------------------|-------------------------|-------------------------|-------------------------|
| 31       | 30 | 29 | 28 | 27                      | 26                      | 25                      | 24                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 23       | 22 | 21 | 20 | 19                      | 18                      | 17                      | 16                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 15       | 14 | 13 | 12 | 11                      | 10                      | 9                       | 8                       |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 7        | 6  | 5  | 4  | 3                       | 2                       | 1                       | 0                       |
| RESERVED |    |    |    | EPWM26_HAL<br>TEN_CR5B1 | EPWM26_HAL<br>TEN_CR5A1 | EPWM26_HAL<br>TEN_CR5B0 | EPWM26_HAL<br>TEN_CR5A0 |
| NONE     |    |    |    | R/W                     | R/W                     | R/W                     | R/W                     |
| 0h       |    |    |    | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 2-3814. CONTROLSS\_CTRL\_EPWM26 HALTEN Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                         |
|------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED            | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM26_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM26_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM26_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM26_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

### 2.7.2.213 CONTROLSS\_CTRL\_EPWM27\_HALTEN Register

#### 1 CONTROLSS\_CTRL\_EPWM27\_HALTEN Register (Offset = 56Ch) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3815. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 056Ch       |

**Figure 2-1270. CONTROLSS\_CTRL\_EPWM27\_HALTEN Name Register**

|          |    |    |    |                         |                         |                         |                         |
|----------|----|----|----|-------------------------|-------------------------|-------------------------|-------------------------|
| 31       | 30 | 29 | 28 | 27                      | 26                      | 25                      | 24                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 23       | 22 | 21 | 20 | 19                      | 18                      | 17                      | 16                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 15       | 14 | 13 | 12 | 11                      | 10                      | 9                       | 8                       |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 7        | 6  | 5  | 4  | 3                       | 2                       | 1                       | 0                       |
| RESERVED |    |    |    | EPWM27_HAL<br>TEN_CR5B1 | EPWM27_HAL<br>TEN_CR5A1 | EPWM27_HAL<br>TEN_CR5B0 | EPWM27_HAL<br>TEN_CR5A0 |
| NONE     |    |    |    | R/W                     | R/W                     | R/W                     | R/W                     |
| 0h       |    |    |    | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 2-3817. CONTROLSS\_CTRL\_EPWM27\_HALTEN Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                         |
|------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED            | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM27_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM27_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM27_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM27_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

### 2.7.2.214 CONTROLSS\_CTRL\_EPWM28\_HALTEN Register

#### 1 CONTROLSS\_CTRL\_EPWM28\_HALTEN Register (Offset = 570h) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3818. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0570h       |

**Figure 2-1271. CONTROLSS\_CTRL\_EPWM28\_HALTEN Name Register**

|          |    |    |    |                         |                         |                         |                         |
|----------|----|----|----|-------------------------|-------------------------|-------------------------|-------------------------|
| 31       | 30 | 29 | 28 | 27                      | 26                      | 25                      | 24                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 23       | 22 | 21 | 20 | 19                      | 18                      | 17                      | 16                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 15       | 14 | 13 | 12 | 11                      | 10                      | 9                       | 8                       |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 7        | 6  | 5  | 4  | 3                       | 2                       | 1                       | 0                       |
| RESERVED |    |    |    | EPWM28_HAL<br>TEN_CR5B1 | EPWM28_HAL<br>TEN_CR5A1 | EPWM28_HAL<br>TEN_CR5B0 | EPWM28_HAL<br>TEN_CR5A0 |
| NONE     |    |    |    | R/W                     | R/W                     | R/W                     | R/W                     |
| 0h       |    |    |    | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 2-3820. CONTROLSS\_CTRL\_EPWM28\_HALTEN Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                         |
|------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED            | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM28_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM28_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM28_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM28_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

### 2.7.2.215 CONTROLSS\_CTRL\_EPWM29 HALTEN Register

#### 1 CONTROLSS\_CTRL\_EPWM29 HALTEN Register (Offset = 574h) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3821. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0574h       |

**Figure 2-1272. CONTROLSS\_CTRL\_EPWM29 HALTEN Name Register**

|          |    |    |    |                         |                         |                         |                         |
|----------|----|----|----|-------------------------|-------------------------|-------------------------|-------------------------|
| 31       | 30 | 29 | 28 | 27                      | 26                      | 25                      | 24                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 23       | 22 | 21 | 20 | 19                      | 18                      | 17                      | 16                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 15       | 14 | 13 | 12 | 11                      | 10                      | 9                       | 8                       |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 7        | 6  | 5  | 4  | 3                       | 2                       | 1                       | 0                       |
| RESERVED |    |    |    | EPWM29_HAL<br>TEN_CR5B1 | EPWM29_HAL<br>TEN_CR5A1 | EPWM29_HAL<br>TEN_CR5B0 | EPWM29_HAL<br>TEN_CR5A0 |
| NONE     |    |    |    | R/W                     | R/W                     | R/W                     | R/W                     |
| 0h       |    |    |    | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 2-3823. CONTROLSS\_CTRL\_EPWM29 HALTEN Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                         |
|------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED            | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM29_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM29_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM29_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM29_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.216 CONTROLSS\_CTRL\_EPWM30 HALTEN Register

### 1 CONTROLSS\_CTRL\_EPWM30 HALTEN Register (Offset = 578h) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3824. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0578h       |

**Figure 2-1273. CONTROLSS\_CTRL\_EPWM30 HALTEN Name Register**

|          |    |    |    |                         |                         |                         |                         |
|----------|----|----|----|-------------------------|-------------------------|-------------------------|-------------------------|
| 31       | 30 | 29 | 28 | 27                      | 26                      | 25                      | 24                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 23       | 22 | 21 | 20 | 19                      | 18                      | 17                      | 16                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 15       | 14 | 13 | 12 | 11                      | 10                      | 9                       | 8                       |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 7        | 6  | 5  | 4  | 3                       | 2                       | 1                       | 0                       |
| RESERVED |    |    |    | EPWM30_HAL<br>TEN_CR5B1 | EPWM30_HAL<br>TEN_CR5A1 | EPWM30_HAL<br>TEN_CR5B0 | EPWM30_HAL<br>TEN_CR5A0 |
| NONE     |    |    |    | R/W                     | R/W                     | R/W                     | R/W                     |
| 0h       |    |    |    | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 2-3826. CONTROLSS\_CTRL\_EPWM30 HALTEN Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                         |
|------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED            | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM30_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM30_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM30_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM30_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |



## 2.7.2.217 CONTROLSS\_CTRL\_EPWM31\_HALTEN Register

### 1 CONTROLSS\_CTRL\_EPWM31\_HALTEN Register (Offset = 57Ch) [reset = 0h]

Epwm halt enable.

Return to [Summary Table](#)

**Table 2-3827. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 057Ch       |

**Figure 2-1274. CONTROLSS\_CTRL\_EPWM31\_HALTEN Name Register**

|          |    |    |    |                         |                         |                         |                         |
|----------|----|----|----|-------------------------|-------------------------|-------------------------|-------------------------|
| 31       | 30 | 29 | 28 | 27                      | 26                      | 25                      | 24                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 23       | 22 | 21 | 20 | 19                      | 18                      | 17                      | 16                      |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 15       | 14 | 13 | 12 | 11                      | 10                      | 9                       | 8                       |
| RESERVED |    |    |    |                         |                         |                         |                         |
| NONE     |    |    |    |                         |                         |                         |                         |
| 0h       |    |    |    |                         |                         |                         |                         |
| 7        | 6  | 5  | 4  | 3                       | 2                       | 1                       | 0                       |
| RESERVED |    |    |    | EPWM31_HAL<br>TEN_CR5B1 | EPWM31_HAL<br>TEN_CR5A1 | EPWM31_HAL<br>TEN_CR5B0 | EPWM31_HAL<br>TEN_CR5A0 |
| NONE     |    |    |    | R/W                     | R/W                     | R/W                     | R/W                     |
| 0h       |    |    |    | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 2-3829. CONTROLSS\_CTRL\_EPWM31\_HALTEN Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                         |
|------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED            | NONE | 0h    | Reserved                                                                                                            |
| 3    | EPWM31_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EPWM31_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EPWM31_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EPWM31_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.218 CONTROLSS\_CTRL\_CMPSSA0 HALTEN Register

### 1 CONTROLSS\_CTRL\_CMPSSA0 HALTEN Register (Offset = 580h) [reset = 0h]

cmpssa halt enable.

Return to [Summary Table](#)

**Table 2-3830. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0580h       |

**Figure 2-1275. CONTROLSS\_CTRL\_CMPSSA0 HALTEN Name Register**

|          |    |    |    |                      |                      |                      |                      |
|----------|----|----|----|----------------------|----------------------|----------------------|----------------------|
| 31       | 30 | 29 | 28 | 27                   | 26                   | 25                   | 24                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 23       | 22 | 21 | 20 | 19                   | 18                   | 17                   | 16                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 15       | 14 | 13 | 12 | 11                   | 10                   | 9                    | 8                    |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 7        | 6  | 5  | 4  | 3                    | 2                    | 1                    | 0                    |
| RESERVED |    |    |    | CMPSSA0_HALTEN_CR5B1 | CMPSSA0_HALTEN_CR5A1 | CMPSSA0_HALTEN_CR5B0 | CMPSSA0_HALTEN_CR5A0 |
| NONE     |    |    |    | R/W                  | R/W                  | R/W                  | R/W                  |
| 0h       |    |    |    | 0h                   | 0h                   | 0h                   | 0h                   |

**Table 2-3832. CONTROLSS\_CTRL\_CMPSSA0 HALTEN Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                                                                         |
|------|----------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED             | NONE | 0h    | Reserved                                                                                                            |
| 3    | CMPSSA0_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | CMPSSA0_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | CMPSSA0_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | CMPSSA0_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

### 2.7.2.219 CONTROLSS\_CTRL\_CMPSSA1\_HALTEN Register

#### 1 CONTROLSS\_CTRL\_CMPSSA1\_HALTEN Register (Offset = 584h) [reset = 0h]

cmpssa halt enable.

Return to [Summary Table](#)

**Table 2-3833. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0584h       |

**Figure 2-1276. CONTROLSS\_CTRL\_CMPSSA1\_HALTEN Name Register**

|          |    |    |    |                      |                      |                      |                      |
|----------|----|----|----|----------------------|----------------------|----------------------|----------------------|
| 31       | 30 | 29 | 28 | 27                   | 26                   | 25                   | 24                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 23       | 22 | 21 | 20 | 19                   | 18                   | 17                   | 16                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 15       | 14 | 13 | 12 | 11                   | 10                   | 9                    | 8                    |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 7        | 6  | 5  | 4  | 3                    | 2                    | 1                    | 0                    |
| RESERVED |    |    |    | CMPSSA1_HALTEN_CR5B1 | CMPSSA1_HALTEN_CR5A1 | CMPSSA1_HALTEN_CR5B0 | CMPSSA1_HALTEN_CR5A0 |
| NONE     |    |    |    | R/W                  | R/W                  | R/W                  | R/W                  |
| 0h       |    |    |    | 0h                   | 0h                   | 0h                   | 0h                   |

**Table 2-3835. CONTROLSS\_CTRL\_CMPSSA1\_HALTEN Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                                                                         |
|------|----------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED             | NONE | 0h    | Reserved                                                                                                            |
| 3    | CMPSSA1_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | CMPSSA1_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | CMPSSA1_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | CMPSSA1_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.220 CONTROLSS\_CTRL\_CMPSSA2\_HALTEN Register

### 1 CONTROLSS\_CTRL\_CMPSSA2\_HALTEN Register (Offset = 588h) [reset = 0h]

cmpssa halt enable.

Return to [Summary Table](#)

**Table 2-3836. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0588h       |

**Figure 2-1277. CONTROLSS\_CTRL\_CMPSSA2\_HALTEN Name Register**

|          |    |    |    |                      |                      |                      |                      |
|----------|----|----|----|----------------------|----------------------|----------------------|----------------------|
| 31       | 30 | 29 | 28 | 27                   | 26                   | 25                   | 24                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 23       | 22 | 21 | 20 | 19                   | 18                   | 17                   | 16                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 15       | 14 | 13 | 12 | 11                   | 10                   | 9                    | 8                    |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 7        | 6  | 5  | 4  | 3                    | 2                    | 1                    | 0                    |
| RESERVED |    |    |    | CMPSSA2_HALTEN_CR5B1 | CMPSSA2_HALTEN_CR5A1 | CMPSSA2_HALTEN_CR5B0 | CMPSSA2_HALTEN_CR5A0 |
| NONE     |    |    |    | R/W                  | R/W                  | R/W                  | R/W                  |
| 0h       |    |    |    | 0h                   | 0h                   | 0h                   | 0h                   |

**Table 2-3838. CONTROLSS\_CTRL\_CMPSSA2\_HALTEN Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                                                                         |
|------|----------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED             | NONE | 0h    | Reserved                                                                                                            |
| 3    | CMPSSA2_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | CMPSSA2_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | CMPSSA2_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | CMPSSA2_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.221 CONTROLSS\_CTRL\_CMPSSA3\_HALTEN Register

### 1 CONTROLSS\_CTRL\_CMPSSA3\_HALTEN Register (Offset = 58Ch) [reset = 0h]

cmpssa halt enable.

Return to [Summary Table](#)

**Table 2-3839. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 058Ch       |

**Figure 2-1278. CONTROLSS\_CTRL\_CMPSSA3\_HALTEN Name Register**

|          |    |    |    |                      |                      |                      |                      |
|----------|----|----|----|----------------------|----------------------|----------------------|----------------------|
| 31       | 30 | 29 | 28 | 27                   | 26                   | 25                   | 24                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 23       | 22 | 21 | 20 | 19                   | 18                   | 17                   | 16                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 15       | 14 | 13 | 12 | 11                   | 10                   | 9                    | 8                    |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 7        | 6  | 5  | 4  | 3                    | 2                    | 1                    | 0                    |
| RESERVED |    |    |    | CMPSSA3_HALTEN_CR5B1 | CMPSSA3_HALTEN_CR5A1 | CMPSSA3_HALTEN_CR5B0 | CMPSSA3_HALTEN_CR5A0 |
| NONE     |    |    |    | R/W                  | R/W                  | R/W                  | R/W                  |
| 0h       |    |    |    | 0h                   | 0h                   | 0h                   | 0h                   |

**Table 2-3841. CONTROLSS\_CTRL\_CMPSSA3\_HALTEN Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                                                                         |
|------|----------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED             | NONE | 0h    | Reserved                                                                                                            |
| 3    | CMPSSA3_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | CMPSSA3_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | CMPSSA3_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | CMPSSA3_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.222 CONTROLSS\_CTRL\_CMPSSA4\_HALTEN Register

### 1 CONTROLSS\_CTRL\_CMPSSA4\_HALTEN Register (Offset = 590h) [reset = 0h]

cmpssa halt enable.

Return to [Summary Table](#)

**Table 2-3842. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0590h       |

**Figure 2-1279. CONTROLSS\_CTRL\_CMPSSA4\_HALTEN Name Register**

|          |    |    |    |                      |                      |                      |                      |
|----------|----|----|----|----------------------|----------------------|----------------------|----------------------|
| 31       | 30 | 29 | 28 | 27                   | 26                   | 25                   | 24                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 23       | 22 | 21 | 20 | 19                   | 18                   | 17                   | 16                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 15       | 14 | 13 | 12 | 11                   | 10                   | 9                    | 8                    |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 7        | 6  | 5  | 4  | 3                    | 2                    | 1                    | 0                    |
| RESERVED |    |    |    | CMPSSA4_HALTEN_CR5B1 | CMPSSA4_HALTEN_CR5A1 | CMPSSA4_HALTEN_CR5B0 | CMPSSA4_HALTEN_CR5A0 |
| NONE     |    |    |    | R/W                  | R/W                  | R/W                  | R/W                  |
| 0h       |    |    |    | 0h                   | 0h                   | 0h                   | 0h                   |

**Table 2-3844. CONTROLSS\_CTRL\_CMPSSA4\_HALTEN Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                                                                         |
|------|----------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED             | NONE | 0h    | Reserved                                                                                                            |
| 3    | CMPSSA4_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | CMPSSA4_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | CMPSSA4_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | CMPSSA4_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

### 2.7.2.223 CONTROLSS\_CTRL\_CMPSSA5\_HALTEN Register

#### 1 CONTROLSS\_CTRL\_CMPSSA5\_HALTEN Register (Offset = 594h) [reset = 0h]

cmpssa halt enable.

Return to [Summary Table](#)

**Table 2-3845. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0594h       |

**Figure 2-1280. CONTROLSS\_CTRL\_CMPSSA5\_HALTEN Name Register**

|          |    |    |    |                      |                      |                      |                      |
|----------|----|----|----|----------------------|----------------------|----------------------|----------------------|
| 31       | 30 | 29 | 28 | 27                   | 26                   | 25                   | 24                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 23       | 22 | 21 | 20 | 19                   | 18                   | 17                   | 16                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 15       | 14 | 13 | 12 | 11                   | 10                   | 9                    | 8                    |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 7        | 6  | 5  | 4  | 3                    | 2                    | 1                    | 0                    |
| RESERVED |    |    |    | CMPSSA5_HALTEN_CR5B1 | CMPSSA5_HALTEN_CR5A1 | CMPSSA5_HALTEN_CR5B0 | CMPSSA5_HALTEN_CR5A0 |
| NONE     |    |    |    | R/W                  | R/W                  | R/W                  | R/W                  |
| 0h       |    |    |    | 0h                   | 0h                   | 0h                   | 0h                   |

**Table 2-3847. CONTROLSS\_CTRL\_CMPSSA5\_HALTEN Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                                                                         |
|------|----------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED             | NONE | 0h    | Reserved                                                                                                            |
| 3    | CMPSSA5_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | CMPSSA5_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | CMPSSA5_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | CMPSSA5_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.224 CONTROLSS\_CTRL\_CMPSSA6 HALTEN Register

### 1 CONTROLSS\_CTRL\_CMPSSA6 HALTEN Register (Offset = 598h) [reset = 0h]

cmpssa halt enable.

Return to [Summary Table](#)

**Table 2-3848. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0598h       |

**Figure 2-1281. CONTROLSS\_CTRL\_CMPSSA6 HALTEN Name Register**

|          |    |    |    |                      |                      |                      |                      |
|----------|----|----|----|----------------------|----------------------|----------------------|----------------------|
| 31       | 30 | 29 | 28 | 27                   | 26                   | 25                   | 24                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 23       | 22 | 21 | 20 | 19                   | 18                   | 17                   | 16                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 15       | 14 | 13 | 12 | 11                   | 10                   | 9                    | 8                    |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 7        | 6  | 5  | 4  | 3                    | 2                    | 1                    | 0                    |
| RESERVED |    |    |    | CMPSSA6_HALTEN_CR5B1 | CMPSSA6_HALTEN_CR5A1 | CMPSSA6_HALTEN_CR5B0 | CMPSSA6_HALTEN_CR5A0 |
| NONE     |    |    |    | R/W                  | R/W                  | R/W                  | R/W                  |
| 0h       |    |    |    | 0h                   | 0h                   | 0h                   | 0h                   |

**Table 2-3850. CONTROLSS\_CTRL\_CMPSSA6 HALTEN Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                                                                         |
|------|----------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED             | NONE | 0h    | Reserved                                                                                                            |
| 3    | CMPSSA6_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | CMPSSA6_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | CMPSSA6_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | CMPSSA6_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |



## 2.7.2.225 CONTROLSS\_CTRL\_CMPSSA7\_HALTEN Register

### 1 CONTROLSS\_CTRL\_CMPSSA7\_HALTEN Register (Offset = 59Ch) [reset = 0h]

cmpssa halt enable.

Return to [Summary Table](#)

**Table 2-3851. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 059Ch       |

**Figure 2-1282. CONTROLSS\_CTRL\_CMPSSA7\_HALTEN Name Register**

|          |    |    |    |                      |                      |                      |                      |
|----------|----|----|----|----------------------|----------------------|----------------------|----------------------|
| 31       | 30 | 29 | 28 | 27                   | 26                   | 25                   | 24                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 23       | 22 | 21 | 20 | 19                   | 18                   | 17                   | 16                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 15       | 14 | 13 | 12 | 11                   | 10                   | 9                    | 8                    |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 7        | 6  | 5  | 4  | 3                    | 2                    | 1                    | 0                    |
| RESERVED |    |    |    | CMPSSA7_HALTEN_CR5B1 | CMPSSA7_HALTEN_CR5A1 | CMPSSA7_HALTEN_CR5B0 | CMPSSA7_HALTEN_CR5A0 |
| NONE     |    |    |    | R/W                  | R/W                  | R/W                  | R/W                  |
| 0h       |    |    |    | 0h                   | 0h                   | 0h                   | 0h                   |

**Table 2-3853. CONTROLSS\_CTRL\_CMPSSA7\_HALTEN Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                                                                         |
|------|----------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED             | NONE | 0h    | Reserved                                                                                                            |
| 3    | CMPSSA7_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | CMPSSA7_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | CMPSSA7_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | CMPSSA7_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.226 CONTROLSS\_CTRL\_CMPSSA8\_HALTEN Register

### 1 CONTROLSS\_CTRL\_CMPSSA8\_HALTEN Register (Offset = 5A0h) [reset = 0h]

cmpssa halt enable.

Return to [Summary Table](#)

**Table 2-3854. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 05A0h       |

**Figure 2-1283. CONTROLSS\_CTRL\_CMPSSA8\_HALTEN Name Register**

|          |    |    |    |                      |                      |                      |                      |
|----------|----|----|----|----------------------|----------------------|----------------------|----------------------|
| 31       | 30 | 29 | 28 | 27                   | 26                   | 25                   | 24                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 23       | 22 | 21 | 20 | 19                   | 18                   | 17                   | 16                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 15       | 14 | 13 | 12 | 11                   | 10                   | 9                    | 8                    |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 7        | 6  | 5  | 4  | 3                    | 2                    | 1                    | 0                    |
| RESERVED |    |    |    | CMPSSA8_HALTEN_CR5B1 | CMPSSA8_HALTEN_CR5A1 | CMPSSA8_HALTEN_CR5B0 | CMPSSA8_HALTEN_CR5A0 |
| NONE     |    |    |    | R/W                  | R/W                  | R/W                  | R/W                  |
| 0h       |    |    |    | 0h                   | 0h                   | 0h                   | 0h                   |

**Table 2-3856. CONTROLSS\_CTRL\_CMPSSA8\_HALTEN Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                                                                         |
|------|----------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED             | NONE | 0h    | Reserved                                                                                                            |
| 3    | CMPSSA8_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | CMPSSA8_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | CMPSSA8_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | CMPSSA8_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.227 CONTROLSS\_CTRL\_CMPSSA9\_HALTEN Register

### 1 CONTROLSS\_CTRL\_CMPSSA9\_HALTEN Register (Offset = 5A4h) [reset = 0h]

cmpssa halt enable.

Return to [Summary Table](#)

**Table 2-3857. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 05A4h       |

**Figure 2-1284. CONTROLSS\_CTRL\_CMPSSA9\_HALTEN Name Register**

|          |    |    |    |                      |                      |                      |                      |
|----------|----|----|----|----------------------|----------------------|----------------------|----------------------|
| 31       | 30 | 29 | 28 | 27                   | 26                   | 25                   | 24                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 23       | 22 | 21 | 20 | 19                   | 18                   | 17                   | 16                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 15       | 14 | 13 | 12 | 11                   | 10                   | 9                    | 8                    |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 7        | 6  | 5  | 4  | 3                    | 2                    | 1                    | 0                    |
| RESERVED |    |    |    | CMPSSA9_HALTEN_CR5B1 | CMPSSA9_HALTEN_CR5A1 | CMPSSA9_HALTEN_CR5B0 | CMPSSA9_HALTEN_CR5A0 |
| NONE     |    |    |    | R/W                  | R/W                  | R/W                  | R/W                  |
| 0h       |    |    |    | 0h                   | 0h                   | 0h                   | 0h                   |

**Table 2-3859. CONTROLSS\_CTRL\_CMPSSA9\_HALTEN Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                                                                         |
|------|----------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED             | NONE | 0h    | Reserved                                                                                                            |
| 3    | CMPSSA9_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | CMPSSA9_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | CMPSSA9_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | CMPSSA9_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.228 CONTROLSS\_CTRL\_CMPSSB0\_HALTEN Register

### 1 CONTROLSS\_CTRL\_CMPSSB0\_HALTEN Register (Offset = 5A8h) [reset = 0h]

cmpssb halt enable.

Return to [Summary Table](#)

**Table 2-3860. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 05A8h       |

**Figure 2-1285. CONTROLSS\_CTRL\_CMPSSB0\_HALTEN Name Register**

|          |    |    |    |                      |                      |                      |                      |
|----------|----|----|----|----------------------|----------------------|----------------------|----------------------|
| 31       | 30 | 29 | 28 | 27                   | 26                   | 25                   | 24                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 23       | 22 | 21 | 20 | 19                   | 18                   | 17                   | 16                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 15       | 14 | 13 | 12 | 11                   | 10                   | 9                    | 8                    |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 7        | 6  | 5  | 4  | 3                    | 2                    | 1                    | 0                    |
| RESERVED |    |    |    | CMPSSB0_HALTEN_CR5B1 | CMPSSB0_HALTEN_CR5A1 | CMPSSB0_HALTEN_CR5B0 | CMPSSB0_HALTEN_CR5A0 |
| NONE     |    |    |    | R/W                  | R/W                  | R/W                  | R/W                  |
| 0h       |    |    |    | 0h                   | 0h                   | 0h                   | 0h                   |

**Table 2-3862. CONTROLSS\_CTRL\_CMPSSB0\_HALTEN Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                                                                         |
|------|----------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED             | NONE | 0h    | Reserved                                                                                                            |
| 3    | CMPSSB0_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | CMPSSB0_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | CMPSSB0_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | CMPSSB0_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.229 CONTROLSS\_CTRL\_CMPSSB1\_HALTEN Register

### 1 CONTROLSS\_CTRL\_CMPSSB1\_HALTEN Register (Offset = 5ACh) [reset = 0h]

cmpssb halt enable.

Return to [Summary Table](#)

**Table 2-3863. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 05ACh       |

**Figure 2-1286. CONTROLSS\_CTRL\_CMPSSB1\_HALTEN Name Register**

|          |    |    |    |                      |                      |                      |                      |
|----------|----|----|----|----------------------|----------------------|----------------------|----------------------|
| 31       | 30 | 29 | 28 | 27                   | 26                   | 25                   | 24                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 23       | 22 | 21 | 20 | 19                   | 18                   | 17                   | 16                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 15       | 14 | 13 | 12 | 11                   | 10                   | 9                    | 8                    |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 7        | 6  | 5  | 4  | 3                    | 2                    | 1                    | 0                    |
| RESERVED |    |    |    | CMPSSB1_HALTEN_CR5B1 | CMPSSB1_HALTEN_CR5A1 | CMPSSB1_HALTEN_CR5B0 | CMPSSB1_HALTEN_CR5A0 |
| NONE     |    |    |    | R/W                  | R/W                  | R/W                  | R/W                  |
| 0h       |    |    |    | 0h                   | 0h                   | 0h                   | 0h                   |

**Table 2-3865. CONTROLSS\_CTRL\_CMPSSB1\_HALTEN Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                                                                         |
|------|----------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED             | NONE | 0h    | Reserved                                                                                                            |
| 3    | CMPSSB1_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | CMPSSB1_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | CMPSSB1_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | CMPSSB1_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

### 2.7.2.230 CONTROLSS\_CTRL\_CMPSSB2\_HALTEN Register

#### 1 CONTROLSS\_CTRL\_CMPSSB2\_HALTEN Register (Offset = 5B0h) [reset = 0h]

cmpssb halt enable.

Return to [Summary Table](#)

**Table 2-3866. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 05B0h       |

**Figure 2-1287. CONTROLSS\_CTRL\_CMPSSB2\_HALTEN Name Register**

|          |    |    |    |                      |                      |                      |                      |
|----------|----|----|----|----------------------|----------------------|----------------------|----------------------|
| 31       | 30 | 29 | 28 | 27                   | 26                   | 25                   | 24                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 23       | 22 | 21 | 20 | 19                   | 18                   | 17                   | 16                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 15       | 14 | 13 | 12 | 11                   | 10                   | 9                    | 8                    |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 7        | 6  | 5  | 4  | 3                    | 2                    | 1                    | 0                    |
| RESERVED |    |    |    | CMPSSB2_HALTEN_CR5B1 | CMPSSB2_HALTEN_CR5A1 | CMPSSB2_HALTEN_CR5B0 | CMPSSB2_HALTEN_CR5A0 |
| NONE     |    |    |    | R/W                  | R/W                  | R/W                  | R/W                  |
| 0h       |    |    |    | 0h                   | 0h                   | 0h                   | 0h                   |

**Table 2-3868. CONTROLSS\_CTRL\_CMPSSB2\_HALTEN Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                                                                         |
|------|----------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED             | NONE | 0h    | Reserved                                                                                                            |
| 3    | CMPSSB2_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | CMPSSB2_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | CMPSSB2_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | CMPSSB2_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.231 CONTROLSS\_CTRL\_CMPSSB3\_HALTEN Register

### 1 CONTROLSS\_CTRL\_CMPSSB3\_HALTEN Register (Offset = 5B4h) [reset = 0h]

cmpssb halt enable.

Return to [Summary Table](#)

**Table 2-3869. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 05B4h       |

**Figure 2-1288. CONTROLSS\_CTRL\_CMPSSB3\_HALTEN Name Register**

|          |    |    |    |                      |                      |                      |                      |
|----------|----|----|----|----------------------|----------------------|----------------------|----------------------|
| 31       | 30 | 29 | 28 | 27                   | 26                   | 25                   | 24                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 23       | 22 | 21 | 20 | 19                   | 18                   | 17                   | 16                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 15       | 14 | 13 | 12 | 11                   | 10                   | 9                    | 8                    |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 7        | 6  | 5  | 4  | 3                    | 2                    | 1                    | 0                    |
| RESERVED |    |    |    | CMPSSB3_HALTEN_CR5B1 | CMPSSB3_HALTEN_CR5A1 | CMPSSB3_HALTEN_CR5B0 | CMPSSB3_HALTEN_CR5A0 |
| NONE     |    |    |    | R/W                  | R/W                  | R/W                  | R/W                  |
| 0h       |    |    |    | 0h                   | 0h                   | 0h                   | 0h                   |

**Table 2-3871. CONTROLSS\_CTRL\_CMPSSB3\_HALTEN Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                                                                         |
|------|----------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED             | NONE | 0h    | Reserved                                                                                                            |
| 3    | CMPSSB3_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | CMPSSB3_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | CMPSSB3_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | CMPSSB3_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.232 CONTROLSS\_CTRL\_CMPSSB4\_HALTEN Register

### 1 CONTROLSS\_CTRL\_CMPSSB4\_HALTEN Register (Offset = 5B8h) [reset = 0h]

cmpssb halt enable.

Return to [Summary Table](#)

**Table 2-3872. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 05B8h       |

**Figure 2-1289. CONTROLSS\_CTRL\_CMPSSB4\_HALTEN Name Register**

|          |    |    |    |                      |                      |                      |                      |
|----------|----|----|----|----------------------|----------------------|----------------------|----------------------|
| 31       | 30 | 29 | 28 | 27                   | 26                   | 25                   | 24                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 23       | 22 | 21 | 20 | 19                   | 18                   | 17                   | 16                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 15       | 14 | 13 | 12 | 11                   | 10                   | 9                    | 8                    |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 7        | 6  | 5  | 4  | 3                    | 2                    | 1                    | 0                    |
| RESERVED |    |    |    | CMPSSB4_HALTEN_CR5B1 | CMPSSB4_HALTEN_CR5A1 | CMPSSB4_HALTEN_CR5B0 | CMPSSB4_HALTEN_CR5A0 |
| NONE     |    |    |    | R/W                  | R/W                  | R/W                  | R/W                  |
| 0h       |    |    |    | 0h                   | 0h                   | 0h                   | 0h                   |

**Table 2-3874. CONTROLSS\_CTRL\_CMPSSB4\_HALTEN Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                                                                         |
|------|----------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED             | NONE | 0h    | Reserved                                                                                                            |
| 3    | CMPSSB4_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | CMPSSB4_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | CMPSSB4_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | CMPSSB4_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |



### 2.7.2.233 CONTROLSS\_CTRL\_CMPSSB5\_HALTEN Register

#### 1 CONTROLSS\_CTRL\_CMPSSB5\_HALTEN Register (Offset = 5BCh) [reset = 0h]

cmpssb halt enable.

Return to [Summary Table](#)

**Table 2-3875. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 05BCh       |

**Figure 2-1290. CONTROLSS\_CTRL\_CMPSSB5\_HALTEN Name Register**

|          |    |    |    |                      |                      |                      |                      |
|----------|----|----|----|----------------------|----------------------|----------------------|----------------------|
| 31       | 30 | 29 | 28 | 27                   | 26                   | 25                   | 24                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 23       | 22 | 21 | 20 | 19                   | 18                   | 17                   | 16                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 15       | 14 | 13 | 12 | 11                   | 10                   | 9                    | 8                    |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 7        | 6  | 5  | 4  | 3                    | 2                    | 1                    | 0                    |
| RESERVED |    |    |    | CMPSSB5_HALTEN_CR5B1 | CMPSSB5_HALTEN_CR5A1 | CMPSSB5_HALTEN_CR5B0 | CMPSSB5_HALTEN_CR5A0 |
| NONE     |    |    |    | R/W                  | R/W                  | R/W                  | R/W                  |
| 0h       |    |    |    | 0h                   | 0h                   | 0h                   | 0h                   |

**Table 2-3877. CONTROLSS\_CTRL\_CMPSSB5\_HALTEN Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                                                                         |
|------|----------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED             | NONE | 0h    | Reserved                                                                                                            |
| 3    | CMPSSB5_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | CMPSSB5_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | CMPSSB5_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | CMPSSB5_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.234 CONTROLSS\_CTRL\_CMPSSB6\_HALTEN Register

### 1 CONTROLSS\_CTRL\_CMPSSB6\_HALTEN Register (Offset = 5C0h) [reset = 0h]

cmpssb halt enable.

Return to [Summary Table](#)

**Table 2-3878. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 05C0h       |

**Figure 2-1291. CONTROLSS\_CTRL\_CMPSSB6\_HALTEN Name Register**

|          |    |    |    |                      |                      |                      |                      |
|----------|----|----|----|----------------------|----------------------|----------------------|----------------------|
| 31       | 30 | 29 | 28 | 27                   | 26                   | 25                   | 24                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 23       | 22 | 21 | 20 | 19                   | 18                   | 17                   | 16                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 15       | 14 | 13 | 12 | 11                   | 10                   | 9                    | 8                    |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 7        | 6  | 5  | 4  | 3                    | 2                    | 1                    | 0                    |
| RESERVED |    |    |    | CMPSSB6_HALTEN_CR5B1 | CMPSSB6_HALTEN_CR5A1 | CMPSSB6_HALTEN_CR5B0 | CMPSSB6_HALTEN_CR5A0 |
| NONE     |    |    |    | R/W                  | R/W                  | R/W                  | R/W                  |
| 0h       |    |    |    | 0h                   | 0h                   | 0h                   | 0h                   |

**Table 2-3880. CONTROLSS\_CTRL\_CMPSSB6\_HALTEN Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                                                                         |
|------|----------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED             | NONE | 0h    | Reserved                                                                                                            |
| 3    | CMPSSB6_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | CMPSSB6_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | CMPSSB6_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | CMPSSB6_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.235 CONTROLSS\_CTRL\_CMPSSB7\_HALTEN Register

### 1 CONTROLSS\_CTRL\_CMPSSB7\_HALTEN Register (Offset = 5C4h) [reset = 0h]

cmpssb halt enable.

Return to [Summary Table](#)

**Table 2-3881. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 05C4h       |

**Figure 2-1292. CONTROLSS\_CTRL\_CMPSSB7\_HALTEN Name Register**

|          |    |    |    |                      |                      |                      |                      |
|----------|----|----|----|----------------------|----------------------|----------------------|----------------------|
| 31       | 30 | 29 | 28 | 27                   | 26                   | 25                   | 24                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 23       | 22 | 21 | 20 | 19                   | 18                   | 17                   | 16                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 15       | 14 | 13 | 12 | 11                   | 10                   | 9                    | 8                    |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 7        | 6  | 5  | 4  | 3                    | 2                    | 1                    | 0                    |
| RESERVED |    |    |    | CMPSSB7_HALTEN_CR5B1 | CMPSSB7_HALTEN_CR5A1 | CMPSSB7_HALTEN_CR5B0 | CMPSSB7_HALTEN_CR5A0 |
| NONE     |    |    |    | R/W                  | R/W                  | R/W                  | R/W                  |
| 0h       |    |    |    | 0h                   | 0h                   | 0h                   | 0h                   |

**Table 2-3883. CONTROLSS\_CTRL\_CMPSSB7\_HALTEN Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                                                                         |
|------|----------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED             | NONE | 0h    | Reserved                                                                                                            |
| 3    | CMPSSB7_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | CMPSSB7_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | CMPSSB7_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | CMPSSB7_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.236 CONTROLSS\_CTRL\_CMPSSB8\_HALTEN Register

### 1 CONTROLSS\_CTRL\_CMPSSB8\_HALTEN Register (Offset = 5C8h) [reset = 0h]

cmpssb halt enable.

Return to [Summary Table](#)

**Table 2-3884. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 05C8h       |

**Figure 2-1293. CONTROLSS\_CTRL\_CMPSSB8\_HALTEN Name Register**

|          |    |    |    |                      |                      |                      |                      |
|----------|----|----|----|----------------------|----------------------|----------------------|----------------------|
| 31       | 30 | 29 | 28 | 27                   | 26                   | 25                   | 24                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 23       | 22 | 21 | 20 | 19                   | 18                   | 17                   | 16                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 15       | 14 | 13 | 12 | 11                   | 10                   | 9                    | 8                    |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 7        | 6  | 5  | 4  | 3                    | 2                    | 1                    | 0                    |
| RESERVED |    |    |    | CMPSSB8_HALTEN_CR5B1 | CMPSSB8_HALTEN_CR5A1 | CMPSSB8_HALTEN_CR5B0 | CMPSSB8_HALTEN_CR5A0 |
| NONE     |    |    |    | R/W                  | R/W                  | R/W                  | R/W                  |
| 0h       |    |    |    | 0h                   | 0h                   | 0h                   | 0h                   |

**Table 2-3886. CONTROLSS\_CTRL\_CMPSSB8\_HALTEN Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                                                                         |
|------|----------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED             | NONE | 0h    | Reserved                                                                                                            |
| 3    | CMPSSB8_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | CMPSSB8_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | CMPSSB8_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | CMPSSB8_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

### 2.7.2.237 CONTROLSS\_CTRL\_CMPSSB9\_HALTEN Register

#### 1 CONTROLSS\_CTRL\_CMPSSB9\_HALTEN Register (Offset = 5CCh) [reset = 0h]

cmpssb halt enable.

Return to [Summary Table](#)

**Table 2-3887. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 05CCh       |

**Figure 2-1294. CONTROLSS\_CTRL\_CMPSSB9\_HALTEN Name Register**

|          |    |    |    |                      |                      |                      |                      |
|----------|----|----|----|----------------------|----------------------|----------------------|----------------------|
| 31       | 30 | 29 | 28 | 27                   | 26                   | 25                   | 24                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 23       | 22 | 21 | 20 | 19                   | 18                   | 17                   | 16                   |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 15       | 14 | 13 | 12 | 11                   | 10                   | 9                    | 8                    |
| RESERVED |    |    |    |                      |                      |                      |                      |
| NONE     |    |    |    |                      |                      |                      |                      |
| 0h       |    |    |    |                      |                      |                      |                      |
| 7        | 6  | 5  | 4  | 3                    | 2                    | 1                    | 0                    |
| RESERVED |    |    |    | CMPSSB9_HALTEN_CR5B1 | CMPSSB9_HALTEN_CR5A1 | CMPSSB9_HALTEN_CR5B0 | CMPSSB9_HALTEN_CR5A0 |
| NONE     |    |    |    | R/W                  | R/W                  | R/W                  | R/W                  |
| 0h       |    |    |    | 0h                   | 0h                   | 0h                   | 0h                   |

**Table 2-3889. CONTROLSS\_CTRL\_CMPSSB9\_HALTEN Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                                                                         |
|------|----------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED             | NONE | 0h    | Reserved                                                                                                            |
| 3    | CMPSSB9_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | CMPSSB9_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | CMPSSB9_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | CMPSSB9_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.238 CONTROLSS\_CTRL\_ECAP0 HALTEN Register

### 1 CONTROLSS\_CTRL\_ECAP0 HALTEN Register (Offset = 5D0h) [reset = 0h]

Ecap halt enable.

Return to [Summary Table](#)

**Table 2-3890. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 05D0h       |

**Figure 2-1295. CONTROLSS\_CTRL\_ECAP0 HALTEN Name Register**

|          |    |    |    |                        |                        |                        |                        |
|----------|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 31       | 30 | 29 | 28 | 27                     | 26                     | 25                     | 24                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 23       | 22 | 21 | 20 | 19                     | 18                     | 17                     | 16                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 15       | 14 | 13 | 12 | 11                     | 10                     | 9                      | 8                      |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 7        | 6  | 5  | 4  | 3                      | 2                      | 1                      | 0                      |
| RESERVED |    |    |    | ECAP0_HALTE<br>N_CR5B1 | ECAP0_HALTE<br>N_CR5A1 | ECAP0_HALTE<br>N_CR5B0 | ECAP0_HALTE<br>N_CR5A0 |
| NONE     |    |    |    | R/W                    | R/W                    | R/W                    | R/W                    |
| 0h       |    |    |    | 0h                     | 0h                     | 0h                     | 0h                     |

**Table 2-3892. CONTROLSS\_CTRL\_ECAP0 HALTEN Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                         |
|------|--------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED           | NONE | 0h    | Reserved                                                                                                            |
| 3    | ECAP0_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | ECAP0_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | ECAP0_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | ECAP0_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

### 2.7.2.239 CONTROLSS\_CTRL\_ECAP1 HALTEN Register

#### 1 CONTROLSS\_CTRL\_ECAP1 HALTEN Register (Offset = 5D4h) [reset = 0h]

Ecaphalt enable.

Return to [Summary Table](#)

**Table 2-3893. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 05D4h       |

**Figure 2-1296. CONTROLSS\_CTRL\_ECAP1 HALTEN Name Register**

|          |    |    |    |                        |                        |                        |                        |
|----------|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 31       | 30 | 29 | 28 | 27                     | 26                     | 25                     | 24                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 23       | 22 | 21 | 20 | 19                     | 18                     | 17                     | 16                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 15       | 14 | 13 | 12 | 11                     | 10                     | 9                      | 8                      |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 7        | 6  | 5  | 4  | 3                      | 2                      | 1                      | 0                      |
| RESERVED |    |    |    | ECAP1_HALTE<br>N_CR5B1 | ECAP1_HALTE<br>N_CR5A1 | ECAP1_HALTE<br>N_CR5B0 | ECAP1_HALTE<br>N_CR5A0 |
| NONE     |    |    |    | R/W                    | R/W                    | R/W                    | R/W                    |
| 0h       |    |    |    | 0h                     | 0h                     | 0h                     | 0h                     |

**Table 2-3895. CONTROLSS\_CTRL\_ECAP1 HALTEN Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                         |
|------|--------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED           | NONE | 0h    | Reserved                                                                                                            |
| 3    | ECAP1_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | ECAP1_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | ECAP1_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | ECAP1_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.240 CONTROLSS\_CTRL\_ECAP2\_HALTEN Register

### 1 CONTROLSS\_CTRL\_ECAP2\_HALTEN Register (Offset = 5D8h) [reset = 0h]

Ecapi halt enable.

Return to [Summary Table](#)

**Table 2-3896. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 05D8h       |

**Figure 2-1297. CONTROLSS\_CTRL\_ECAP2\_HALTEN Name Register**

|          |    |    |    |                        |                        |                        |                        |
|----------|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 31       | 30 | 29 | 28 | 27                     | 26                     | 25                     | 24                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 23       | 22 | 21 | 20 | 19                     | 18                     | 17                     | 16                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 15       | 14 | 13 | 12 | 11                     | 10                     | 9                      | 8                      |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 7        | 6  | 5  | 4  | 3                      | 2                      | 1                      | 0                      |
| RESERVED |    |    |    | ECAP2_HALTE<br>N_CR5B1 | ECAP2_HALTE<br>N_CR5A1 | ECAP2_HALTE<br>N_CR5B0 | ECAP2_HALTE<br>N_CR5A0 |
| NONE     |    |    |    | R/W                    | R/W                    | R/W                    | R/W                    |
| 0h       |    |    |    | 0h                     | 0h                     | 0h                     | 0h                     |

**Table 2-3898. CONTROLSS\_CTRL\_ECAP2\_HALTEN Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                         |
|------|--------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED           | NONE | 0h    | Reserved                                                                                                            |
| 3    | ECAP2_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | ECAP2_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | ECAP2_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | ECAP2_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |



## 2.7.2.241 CONTROLSS\_CTRL\_ECAP3 HALTEN Register

### 1 CONTROLSS\_CTRL\_ECAP3 HALTEN Register (Offset = 5DCh) [reset = 0h]

Ecaphalt enable.

Return to [Summary Table](#)

**Table 2-3899. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 05DCh       |

**Figure 2-1298. CONTROLSS\_CTRL\_ECAP3 HALTEN Name Register**

|          |    |    |    |                        |                        |                        |                        |
|----------|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 31       | 30 | 29 | 28 | 27                     | 26                     | 25                     | 24                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 23       | 22 | 21 | 20 | 19                     | 18                     | 17                     | 16                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 15       | 14 | 13 | 12 | 11                     | 10                     | 9                      | 8                      |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 7        | 6  | 5  | 4  | 3                      | 2                      | 1                      | 0                      |
| RESERVED |    |    |    | ECAP3_HALTE<br>N_CR5B1 | ECAP3_HALTE<br>N_CR5A1 | ECAP3_HALTE<br>N_CR5B0 | ECAP3_HALTE<br>N_CR5A0 |
| NONE     |    |    |    | R/W                    | R/W                    | R/W                    | R/W                    |
| 0h       |    |    |    | 0h                     | 0h                     | 0h                     | 0h                     |

**Table 2-3901. CONTROLSS\_CTRL\_ECAP3 HALTEN Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                         |
|------|--------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED           | NONE | 0h    | Reserved                                                                                                            |
| 3    | ECAP3_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | ECAP3_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | ECAP3_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | ECAP3_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.242 CONTROLSS\_CTRL\_ECAP4 HALTEN Register

### 1 CONTROLSS\_CTRL\_ECAP4 HALTEN Register (Offset = 5E0h) [reset = 0h]

Ecaphalt enable.

Return to [Summary Table](#)

**Table 2-3902. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 05E0h       |

**Figure 2-1299. CONTROLSS\_CTRL\_ECAP4 HALTEN Name Register**

|          |    |    |    |                        |                        |                        |                        |
|----------|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 31       | 30 | 29 | 28 | 27                     | 26                     | 25                     | 24                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 23       | 22 | 21 | 20 | 19                     | 18                     | 17                     | 16                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 15       | 14 | 13 | 12 | 11                     | 10                     | 9                      | 8                      |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 7        | 6  | 5  | 4  | 3                      | 2                      | 1                      | 0                      |
| RESERVED |    |    |    | ECAP4_HALTE<br>N_CR5B1 | ECAP4_HALTE<br>N_CR5A1 | ECAP4_HALTE<br>N_CR5B0 | ECAP4_HALTE<br>N_CR5A0 |
| NONE     |    |    |    | R/W                    | R/W                    | R/W                    | R/W                    |
| 0h       |    |    |    | 0h                     | 0h                     | 0h                     | 0h                     |

**Table 2-3904. CONTROLSS\_CTRL\_ECAP4 HALTEN Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                         |
|------|--------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED           | NONE | 0h    | Reserved                                                                                                            |
| 3    | ECAP4_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | ECAP4_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | ECAP4_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | ECAP4_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

### 2.7.2.243 CONTROLSS\_CTRL\_ECAP5 HALTEN Register

#### 1 CONTROLSS\_CTRL\_ECAP5 HALTEN Register (Offset = 5E4h) [reset = 0h]

Ecaphalt enable.

Return to [Summary Table](#)

**Table 2-3905. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 05E4h       |

**Figure 2-1300. CONTROLSS\_CTRL\_ECAP5 HALTEN Name Register**

|          |    |    |    |                        |                        |                        |                        |
|----------|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 31       | 30 | 29 | 28 | 27                     | 26                     | 25                     | 24                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 23       | 22 | 21 | 20 | 19                     | 18                     | 17                     | 16                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 15       | 14 | 13 | 12 | 11                     | 10                     | 9                      | 8                      |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 7        | 6  | 5  | 4  | 3                      | 2                      | 1                      | 0                      |
| RESERVED |    |    |    | ECAP5_HALTE<br>N_CR5B1 | ECAP5_HALTE<br>N_CR5A1 | ECAP5_HALTE<br>N_CR5B0 | ECAP5_HALTE<br>N_CR5A0 |
| NONE     |    |    |    | R/W                    | R/W                    | R/W                    | R/W                    |
| 0h       |    |    |    | 0h                     | 0h                     | 0h                     | 0h                     |

**Table 2-3907. CONTROLSS\_CTRL\_ECAP5 HALTEN Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                         |
|------|--------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED           | NONE | 0h    | Reserved                                                                                                            |
| 3    | ECAP5_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | ECAP5_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | ECAP5_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | ECAP5_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

### 2.7.2.244 CONTROLSS\_CTRL\_ECAP6 HALTEN Register

#### 1 CONTROLSS\_CTRL\_ECAP6 HALTEN Register (Offset = 5E8h) [reset = 0h]

Ecaphalt enable.

Return to [Summary Table](#)

**Table 2-3908. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 05E8h       |

**Figure 2-1301. CONTROLSS\_CTRL\_ECAP6 HALTEN Name Register**

|          |    |    |    |                        |                        |                        |                        |
|----------|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 31       | 30 | 29 | 28 | 27                     | 26                     | 25                     | 24                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 23       | 22 | 21 | 20 | 19                     | 18                     | 17                     | 16                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 15       | 14 | 13 | 12 | 11                     | 10                     | 9                      | 8                      |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 7        | 6  | 5  | 4  | 3                      | 2                      | 1                      | 0                      |
| RESERVED |    |    |    | ECAP6_HALTE<br>N_CR5B1 | ECAP6_HALTE<br>N_CR5A1 | ECAP6_HALTE<br>N_CR5B0 | ECAP6_HALTE<br>N_CR5A0 |
| NONE     |    |    |    | R/W                    | R/W                    | R/W                    | R/W                    |
| 0h       |    |    |    | 0h                     | 0h                     | 0h                     | 0h                     |

**Table 2-3910. CONTROLSS\_CTRL\_ECAP6 HALTEN Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                         |
|------|--------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED           | NONE | 0h    | Reserved                                                                                                            |
| 3    | ECAP6_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | ECAP6_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | ECAP6_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | ECAP6_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

### 2.7.2.245 CONTROLSS\_CTRL\_ECAP7 HALTEN Register

#### 1 CONTROLSS\_CTRL\_ECAP7 HALTEN Register (Offset = 5ECh) [reset = 0h]

Ecaphalt enable.

Return to [Summary Table](#)

**Table 2-3911. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 05ECh       |

**Figure 2-1302. CONTROLSS\_CTRL\_ECAP7 HALTEN Name Register**

|          |    |    |    |                        |                        |                        |                        |
|----------|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 31       | 30 | 29 | 28 | 27                     | 26                     | 25                     | 24                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 23       | 22 | 21 | 20 | 19                     | 18                     | 17                     | 16                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 15       | 14 | 13 | 12 | 11                     | 10                     | 9                      | 8                      |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 7        | 6  | 5  | 4  | 3                      | 2                      | 1                      | 0                      |
| RESERVED |    |    |    | ECAP7_HALTE<br>N_CR5B1 | ECAP7_HALTE<br>N_CR5A1 | ECAP7_HALTE<br>N_CR5B0 | ECAP7_HALTE<br>N_CR5A0 |
| NONE     |    |    |    | R/W                    | R/W                    | R/W                    | R/W                    |
| 0h       |    |    |    | 0h                     | 0h                     | 0h                     | 0h                     |

**Table 2-3913. CONTROLSS\_CTRL\_ECAP7 HALTEN Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                         |
|------|--------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED           | NONE | 0h    | Reserved                                                                                                            |
| 3    | ECAP7_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | ECAP7_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | ECAP7_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | ECAP7_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.246 CONTROLSS\_CTRL\_ECAP8 HALTEN Register

### 1 CONTROLSS\_CTRL\_ECAP8 HALTEN Register (Offset = 5F0h) [reset = 0h]

Ecaphalt enable.

Return to [Summary Table](#)

**Table 2-3914. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 05F0h       |

**Figure 2-1303. CONTROLSS\_CTRL\_ECAP8 HALTEN Name Register**

|          |    |    |    |                        |                        |                        |                        |
|----------|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 31       | 30 | 29 | 28 | 27                     | 26                     | 25                     | 24                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 23       | 22 | 21 | 20 | 19                     | 18                     | 17                     | 16                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 15       | 14 | 13 | 12 | 11                     | 10                     | 9                      | 8                      |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 7        | 6  | 5  | 4  | 3                      | 2                      | 1                      | 0                      |
| RESERVED |    |    |    | ECAP8_HALTE<br>N_CR5B1 | ECAP8_HALTE<br>N_CR5A1 | ECAP8_HALTE<br>N_CR5B0 | ECAP8_HALTE<br>N_CR5A0 |
| NONE     |    |    |    | R/W                    | R/W                    | R/W                    | R/W                    |
| 0h       |    |    |    | 0h                     | 0h                     | 0h                     | 0h                     |

**Table 2-3916. CONTROLSS\_CTRL\_ECAP8 HALTEN Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                         |
|------|--------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED           | NONE | 0h    | Reserved                                                                                                            |
| 3    | ECAP8_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | ECAP8_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | ECAP8_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | ECAP8_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

### 2.7.2.247 CONTROLSS\_CTRL\_ECAP9 HALTEN Register

#### 1 CONTROLSS\_CTRL\_ECAP9 HALTEN Register (Offset = 5F4h) [reset = 0h]

Ecapi halt enable.

Return to [Summary Table](#)

**Table 2-3917. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 05F4h       |

**Figure 2-1304. CONTROLSS\_CTRL\_ECAP9 HALTEN Name Register**

|          |    |    |    |                        |                        |                        |                        |
|----------|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 31       | 30 | 29 | 28 | 27                     | 26                     | 25                     | 24                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 23       | 22 | 21 | 20 | 19                     | 18                     | 17                     | 16                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 15       | 14 | 13 | 12 | 11                     | 10                     | 9                      | 8                      |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 7        | 6  | 5  | 4  | 3                      | 2                      | 1                      | 0                      |
| RESERVED |    |    |    | ECAP9 HALTE<br>N_CR5B1 | ECAP9 HALTE<br>N_CR5A1 | ECAP9 HALTE<br>N_CR5B0 | ECAP9 HALTE<br>N_CR5A0 |
| NONE     |    |    |    | R/W                    | R/W                    | R/W                    | R/W                    |
| 0h       |    |    |    | 0h                     | 0h                     | 0h                     | 0h                     |

**Table 2-3919. CONTROLSS\_CTRL\_ECAP9 HALTEN Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                         |
|------|--------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED           | NONE | 0h    | Reserved                                                                                                            |
| 3    | ECAP9_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | ECAP9_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | ECAP9_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | ECAP9_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

## 2.7.2.248 CONTROLSS\_CTRL\_EQEP0 HALTEN Register

### 1 CONTROLSS\_CTRL\_EQEP0 HALTEN Register (Offset = 5F8h) [reset = 0h]

Eqep halt enable.

Return to [Summary Table](#)

**Table 2-3920. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 05F8h       |

**Figure 2-1305. CONTROLSS\_CTRL\_EQEP0 HALTEN Name Register**

|          |    |    |    |                        |                        |                        |                        |
|----------|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 31       | 30 | 29 | 28 | 27                     | 26                     | 25                     | 24                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 23       | 22 | 21 | 20 | 19                     | 18                     | 17                     | 16                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 15       | 14 | 13 | 12 | 11                     | 10                     | 9                      | 8                      |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 7        | 6  | 5  | 4  | 3                      | 2                      | 1                      | 0                      |
| RESERVED |    |    |    | EQEP0_HALTE<br>N_CR5B1 | EQEP0_HALTE<br>N_CR5A1 | EQEP0_HALTE<br>N_CR5B0 | EQEP0_HALTE<br>N_CR5A0 |
| NONE     |    |    |    | R/W                    | R/W                    | R/W                    | R/W                    |
| 0h       |    |    |    | 0h                     | 0h                     | 0h                     | 0h                     |

**Table 2-3922. CONTROLSS\_CTRL\_EQEP0 HALTEN Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                         |
|------|--------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED           | NONE | 0h    | Reserved                                                                                                            |
| 3    | EQEP0_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EQEP0_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EQEP0_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EQEP0_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |



## 2.7.2.249 CONTROLSS\_CTRL\_EQEP1\_HALTEN Register

### 1 CONTROLSS\_CTRL\_EQEP1\_HALTEN Register (Offset = 5FCh) [reset = 0h]

Eqep halt enable.

Return to [Summary Table](#)

**Table 2-3923. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 05FCh       |

**Figure 2-1306. CONTROLSS\_CTRL\_EQEP1\_HALTEN Name Register**

|          |    |    |    |                        |                        |                        |                        |
|----------|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 31       | 30 | 29 | 28 | 27                     | 26                     | 25                     | 24                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 23       | 22 | 21 | 20 | 19                     | 18                     | 17                     | 16                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 15       | 14 | 13 | 12 | 11                     | 10                     | 9                      | 8                      |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 7        | 6  | 5  | 4  | 3                      | 2                      | 1                      | 0                      |
| RESERVED |    |    |    | EQEP1_HALTE<br>N_CR5B1 | EQEP1_HALTE<br>N_CR5A1 | EQEP1_HALTE<br>N_CR5B0 | EQEP1_HALTE<br>N_CR5A0 |
| NONE     |    |    |    | R/W                    | R/W                    | R/W                    | R/W                    |
| 0h       |    |    |    | 0h                     | 0h                     | 0h                     | 0h                     |

**Table 2-3925. CONTROLSS\_CTRL\_EQEP1\_HALTEN Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                         |
|------|--------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED           | NONE | 0h    | Reserved                                                                                                            |
| 3    | EQEP1_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EQEP1_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EQEP1_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EQEP1_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

### 2.7.2.250 CONTROLSS\_CTRL\_EQEP2\_HALTEN Register

#### 1 CONTROLSS\_CTRL\_EQEP2\_HALTEN Register (Offset = 600h) [reset = 0h]

Eqep halt enable.

Return to [Summary Table](#)

**Table 2-3926. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 0600h       |

**Figure 2-1307. CONTROLSS\_CTRL\_EQEP2\_HALTEN Name Register**

|          |    |    |    |                        |                        |                        |                        |
|----------|----|----|----|------------------------|------------------------|------------------------|------------------------|
| 31       | 30 | 29 | 28 | 27                     | 26                     | 25                     | 24                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 23       | 22 | 21 | 20 | 19                     | 18                     | 17                     | 16                     |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 15       | 14 | 13 | 12 | 11                     | 10                     | 9                      | 8                      |
| RESERVED |    |    |    |                        |                        |                        |                        |
| NONE     |    |    |    |                        |                        |                        |                        |
| 0h       |    |    |    |                        |                        |                        |                        |
| 7        | 6  | 5  | 4  | 3                      | 2                      | 1                      | 0                      |
| RESERVED |    |    |    | EQEP2_HALTE<br>N_CR5B1 | EQEP2_HALTE<br>N_CR5A1 | EQEP2_HALTE<br>N_CR5B0 | EQEP2_HALTE<br>N_CR5A0 |
| NONE     |    |    |    | R/W                    | R/W                    | R/W                    | R/W                    |
| 0h       |    |    |    | 0h                     | 0h                     | 0h                     | 0h                     |

**Table 2-3928. CONTROLSS\_CTRL\_EQEP2\_HALTEN Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                         |
|------|--------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED           | NONE | 0h    | Reserved                                                                                                            |
| 3    | EQEP2_HALTEN_CR5B1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 2    | EQEP2_HALTEN_CR5A1 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 1    | EQEP2_HALTEN_CR5B0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |
| 0    | EQEP2_HALTEN_CR5A0 | R/W  | 0h    | Write 1'b0: IP Halt disabled with corresponding CPU halt<br>Write 1'b1: IP Halt enabled with corresponding CPU halt |

### 2.7.2.251 CONTROLSS\_CTRL\_LOCK0\_KICK0 Register

#### 1 CONTROLSS\_CTRL\_LOCK0\_KICK0 Register (Offset = 1008h) [reset = 0h]

- KICK0 component.

Return to [Summary Table](#)

**Table 2-3929. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 1008h       |

**Figure 2-1308. CONTROLSS\_CTRL\_LOCK0\_KICK0 Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| LOCK0_KICK0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LOCK0_KICK0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| LOCK0_KICK0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LOCK0_KICK0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 2-3931. CONTROLSS\_CTRL\_LOCK0\_KICK0 Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description       |
|------|-------------|------|-------|-------------------|
| 31:0 | LOCK0_KICK0 | R/W  | 0h    | - KICK0 component |

### 2.7.2.252 CONTROLSS\_CTRL\_LOCK0\_KICK1 Register

#### 1 CONTROLSS\_CTRL\_LOCK0\_KICK1 Register (Offset = 100Ch) [reset = 0h]

- KICK1 component.

Return to [Summary Table](#)

**Table 2-3932. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 100Ch       |

**Figure 2-1309. CONTROLSS\_CTRL\_LOCK0\_KICK1 Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| LOCK0_KICK1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LOCK0_KICK1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| LOCK0_KICK1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LOCK0_KICK1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 2-3934. CONTROLSS\_CTRL\_LOCK0\_KICK1 Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description       |
|------|-------------|------|-------|-------------------|
| 31:0 | LOCK0_KICK1 | R/W  | 0h    | - KICK1 component |

### 2.7.2.253 CONTROLSS\_CTRL\_INTR\_RAW\_STATUS Register

#### 1 CONTROLSS\_CTRL\_INTR\_RAW\_STATUS Register (Offset = 1010h) [reset = 0h]

Interrupt Raw Status/Set Register.

Return to [Summary Table](#)

**Table 2-3935. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 1010h       |

**Figure 2-1310. CONTROLSS\_CTRL\_INTR\_RAW\_STATUS Name Register**

|          |    |    |    |           |          |          |          |
|----------|----|----|----|-----------|----------|----------|----------|
| 31       | 30 | 29 | 28 | 27        | 26       | 25       | 24       |
| RESERVED |    |    |    |           |          |          |          |
| NONE     |    |    |    |           |          |          |          |
| 0h       |    |    |    |           |          |          |          |
| 23       | 22 | 21 | 20 | 19        | 18       | 17       | 16       |
| RESERVED |    |    |    |           |          |          |          |
| NONE     |    |    |    |           |          |          |          |
| 0h       |    |    |    |           |          |          |          |
| 15       | 14 | 13 | 12 | 11        | 10       | 9        | 8        |
| RESERVED |    |    |    |           |          |          |          |
| NONE     |    |    |    |           |          |          |          |
| 0h       |    |    |    |           |          |          |          |
| 7        | 6  | 5  | 4  | 3         | 2        | 1        | 0        |
| RESERVED |    |    |    | PROXY_ERR | KICK_ERR | ADDR_ERR | PROT_ERR |
| NONE     |    |    |    | R/W1TS    | R/W1TS   | R/W1TS   | R/W1TS   |
| 0h       |    |    |    | 0h        | 0h       | 0h       | 0h       |

**Table 2-3937. CONTROLSS\_CTRL\_INTR\_RAW\_STATUS Register Field Descriptions**

| Bit  | Field     | Type   | Reset | Description                                                                                                |
|------|-----------|--------|-------|------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED  | NONE   | 0h    | Reserved                                                                                                   |
| 3    | PROXY_ERR | R/W1TS | 0h    | Proxy0 access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. |
| 2    | KICK_ERR  | R/W1TS | 0h    | Kick access violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.   |
| 1    | ADDR_ERR  | R/W1TS | 0h    | Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.    |
| 0    | PROT_ERR  | R/W1TS | 0h    | Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect.    |

## 2.7.2.254 CONTROLSS\_CTRL\_INTR\_ENABLED\_STATUS\_CLEAR Register

### 1 CONTROLSS\_CTRL\_INTR\_ENABLED\_STATUS\_CLEAR Register (Offset = 1014h) [reset = 0h]

Interrupt Enabled Status/Clear register.

Return to [Summary Table](#)

**Table 2-3938. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 1014h       |

**Figure 2-1311. CONTROLSS\_CTRL\_INTR\_ENABLED\_STATUS\_CLEAR Name Register**

|          |    |    |    |                   |                  |                  |                  |
|----------|----|----|----|-------------------|------------------|------------------|------------------|
| 31       | 30 | 29 | 28 | 27                | 26               | 25               | 24               |
| RESERVED |    |    |    |                   |                  |                  |                  |
| NONE     |    |    |    |                   |                  |                  |                  |
| 0h       |    |    |    |                   |                  |                  |                  |
| 23       | 22 | 21 | 20 | 19                | 18               | 17               | 16               |
| RESERVED |    |    |    |                   |                  |                  |                  |
| NONE     |    |    |    |                   |                  |                  |                  |
| 0h       |    |    |    |                   |                  |                  |                  |
| 15       | 14 | 13 | 12 | 11                | 10               | 9                | 8                |
| RESERVED |    |    |    |                   |                  |                  |                  |
| NONE     |    |    |    |                   |                  |                  |                  |
| 0h       |    |    |    |                   |                  |                  |                  |
| 7        | 6  | 5  | 4  | 3                 | 2                | 1                | 0                |
| RESERVED |    |    |    | ENABLED_PROXY_ERR | ENABLED_KICK_ERR | ENABLED_ADDR_ERR | ENABLED_PROT_ERR |
| NONE     |    |    |    | R/W1TC            | R/W1TC           | R/W1TC           | R/W1TC           |
| 0h       |    |    |    | 0h                | 0h               | 0h               | 0h               |

**Table 2-3940. CONTROLSS\_CTRL\_INTR\_ENABLED\_STATUS\_CLEAR Register Field Descriptions**

| Bit  | Field             | Type   | Reset | Description                                                                                                      |
|------|-------------------|--------|-------|------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED          | NONE   | 0h    | Reserved                                                                                                         |
| 3    | ENABLED_PROXY_ERR | R/W1TC | 0h    | Proxy0 access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. |
| 2    | ENABLED_KICK_ERR  | R/W1TC | 0h    | Kick access violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.   |
| 1    | ENABLED_ADDR_ERR  | R/W1TC | 0h    | Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.    |
| 0    | ENABLED_PROT_ERR  | R/W1TC | 0h    | Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect.    |

## 2.7.2.255 CONTROLSS\_CTRL\_INTR\_ENABLE Register

### 1 CONTROLSS\_CTRL\_INTR\_ENABLE Register (Offset = 1018h) [reset = 0h]

Interrupt Enable register.

Return to [Summary Table](#)

**Table 2-3941. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 1018h       |

**Figure 2-1312. CONTROLSS\_CTRL\_INTR\_ENABLE Name Register**

|          |    |    |    |              |             |             |             |
|----------|----|----|----|--------------|-------------|-------------|-------------|
| 31       | 30 | 29 | 28 | 27           | 26          | 25          | 24          |
| RESERVED |    |    |    |              |             |             |             |
| NONE     |    |    |    |              |             |             |             |
| 0h       |    |    |    |              |             |             |             |
| 23       | 22 | 21 | 20 | 19           | 18          | 17          | 16          |
| RESERVED |    |    |    |              |             |             |             |
| NONE     |    |    |    |              |             |             |             |
| 0h       |    |    |    |              |             |             |             |
| 15       | 14 | 13 | 12 | 11           | 10          | 9           | 8           |
| RESERVED |    |    |    |              |             |             |             |
| NONE     |    |    |    |              |             |             |             |
| 0h       |    |    |    |              |             |             |             |
| 7        | 6  | 5  | 4  | 3            | 2           | 1           | 0           |
| RESERVED |    |    |    | PROXY_ERR_EN | KICK_ERR_EN | ADDR_ERR_EN | PROT_ERR_EN |
| NONE     |    |    |    | R/W1TS       | R/W1TS      | R/W1TS      | R/W1TS      |
| 0h       |    |    |    | 0h           | 0h          | 0h          | 0h          |

**Table 2-3943. CONTROLSS\_CTRL\_INTR\_ENABLE Register Field Descriptions**

| Bit  | Field        | Type   | Reset | Description                                                                                   |
|------|--------------|--------|-------|-----------------------------------------------------------------------------------------------|
| 31:4 | RESERVED     | NONE   | 0h    | Reserved                                                                                      |
| 3    | PROXY_ERR_EN | R/W1TS | 0h    | Proxy0 access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. |
| 2    | KICK_ERR_EN  | R/W1TS | 0h    | Kick access violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.   |
| 1    | ADDR_ERR_EN  | R/W1TS | 0h    | Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.    |
| 0    | PROT_ERR_EN  | R/W1TS | 0h    | Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect.    |

## 2.7.2.256 CONTROLSS\_CTRL\_INTR\_ENABLE\_CLEAR Register

### 1 CONTROLSS\_CTRL\_INTR\_ENABLE\_CLEAR Register (Offset = 101Ch) [reset = 0h]

Interrupt Enable Clear register.

Return to [Summary Table](#)

**Table 2-3944. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 101Ch       |

**Figure 2-1313. CONTROLSS\_CTRL\_INTR\_ENABLE\_CLEAR Name Register**

|          |    |    |    |                  |                 |                 |                 |
|----------|----|----|----|------------------|-----------------|-----------------|-----------------|
| 31       | 30 | 29 | 28 | 27               | 26              | 25              | 24              |
| RESERVED |    |    |    |                  |                 |                 |                 |
| NONE     |    |    |    |                  |                 |                 |                 |
| 0h       |    |    |    |                  |                 |                 |                 |
| 23       | 22 | 21 | 20 | 19               | 18              | 17              | 16              |
| RESERVED |    |    |    |                  |                 |                 |                 |
| NONE     |    |    |    |                  |                 |                 |                 |
| 0h       |    |    |    |                  |                 |                 |                 |
| 15       | 14 | 13 | 12 | 11               | 10              | 9               | 8               |
| RESERVED |    |    |    |                  |                 |                 |                 |
| NONE     |    |    |    |                  |                 |                 |                 |
| 0h       |    |    |    |                  |                 |                 |                 |
| 7        | 6  | 5  | 4  | 3                | 2               | 1               | 0               |
| RESERVED |    |    |    | PROXY_ERR_EN_CLR | KICK_ERR_EN_CLR | ADDR_ERR_EN_CLR | PROT_ERR_EN_CLR |
| NONE     |    |    |    | R/W1TC           | R/W1TC          | R/W1TC          | R/W1TC          |
| 0h       |    |    |    | 0h               | 0h              | 0h              | 0h              |

**Table 2-3946. CONTROLSS\_CTRL\_INTR\_ENABLE\_CLEAR Register Field Descriptions**

| Bit  | Field            | Type   | Reset | Description                                                                                           |
|------|------------------|--------|-------|-------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED         | NONE   | 0h    | Reserved                                                                                              |
| 3    | PROXY_ERR_EN_CLR | R/W1TC | 0h    | Proxy0 access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect. |
| 2    | KICK_ERR_EN_CLR  | R/W1TC | 0h    | Kick access violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.   |
| 1    | ADDR_ERR_EN_CLR  | R/W1TC | 0h    | Addressing violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.    |
| 0    | PROT_ERR_EN_CLR  | R/W1TC | 0h    | Protection violation error enable clear. Write a 1 to clear the enable. Writing a 0 has no effect.    |



### 2.7.2.257 CONTROLSS\_CTRL\_EOI Register

#### 1 CONTROLSS\_CTRL\_EOI Register (Offset = 1020h) [reset = 0h]

EOI register.

Return to [Summary Table](#)

**Table 2-3947. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 1020h       |

**Figure 2-1314. CONTROLSS\_CTRL\_EOI Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| EOI_VECTOR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 2-3949. CONTROLSS\_CTRL\_EOI Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                 |
|------|------------|------|-------|-----------------------------------------------------------------------------|
| 31:8 | RESERVED   | NONE | 0h    | Reserved                                                                    |
| 7:0  | EOI_VECTOR | R/W  | 0h    | EOI vector value. Write this with interrupt distribution value in the chip. |

## 2.7.2.258 CONTROLSS\_CTRL\_FAULT\_ADDRESS Register

### 1 CONTROLSS\_CTRL\_FAULT\_ADDRESS Register (Offset = 1024h) [reset = 0h]

Fault Address register.

Return to [Summary Table](#)

**Table 2-3950. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 1024h       |

**Figure 2-1315. CONTROLSS\_CTRL\_FAULT\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 2-3952. CONTROLSS\_CTRL\_FAULT\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description    |
|------|------------|------|-------|----------------|
| 31:0 | FAULT_ADDR | R    | 0h    | Fault Address. |

## 2.7.2.259 CONTROLSS\_CTRL\_FAULT\_TYPE\_STATUS Register

### 1 CONTROLSS\_CTRL\_FAULT\_TYPE\_STATUS Register (Offset = 1028h) [reset = 0h]

Fault Type Status register.

Return to [Summary Table](#)

**Table 2-3953. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 1028h       |

**Figure 2-1316. CONTROLSS\_CTRL\_FAULT\_TYPE\_STATUS Name Register**

|          |          |            |    |    |    |    |    |
|----------|----------|------------|----|----|----|----|----|
| 31       | 30       | 29         | 28 | 27 | 26 | 25 | 24 |
| RESERVED |          |            |    |    |    |    |    |
| NONE     |          |            |    |    |    |    |    |
| 0h       |          |            |    |    |    |    |    |
| 23       | 22       | 21         | 20 | 19 | 18 | 17 | 16 |
| RESERVED |          |            |    |    |    |    |    |
| NONE     |          |            |    |    |    |    |    |
| 0h       |          |            |    |    |    |    |    |
| 15       | 14       | 13         | 12 | 11 | 10 | 9  | 8  |
| RESERVED |          |            |    |    |    |    |    |
| NONE     |          |            |    |    |    |    |    |
| 0h       |          |            |    |    |    |    |    |
| 7        | 6        | 5          | 4  | 3  | 2  | 1  | 0  |
| RESERVED | FAULT_NS | FAULT_TYPE |    |    |    |    |    |
| NONE     | R        | R          |    |    |    |    |    |
| 0h       | 0h       | 0h         |    |    |    |    |    |

**Table 2-3955. CONTROLSS\_CTRL\_FAULT\_TYPE\_STATUS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                         |
|------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                            |
| 6    | FAULT_NS   | R    | 0h    | Non-secure access.                                                                                                                                                                                                                                                                                                                                                                                  |
| 5:0  | FAULT_TYPE | R    | 0h    | Fault Type<br>10_0000 = Supervisor read fault - priv = 1 dir = 1 dtype != 1<br>01_0000 = Supervisor write fault - priv = 1 dir = 0<br>00_1000 = Supervisor execute fault - priv = 1 dir = 1 dtype = 1<br>00_0100 = User read fault - priv = 0 dir = 1 dtype = 1<br>00_0010 = User write fault - priv = 0 dir = 0<br>00_0001 = User execute fault - priv = 0 dir = 1 dtype = 1<br>00_0000 = No fault |

## 2.7.2.260 CONTROLSS\_CTRL\_FAULT\_ATTR\_STATUS Register

### 1 CONTROLSS\_CTRL\_FAULT\_ATTR\_STATUS Register (Offset = 102Ch) [reset = 0h]

Fault Attribute Status register.

Return to [Summary Table](#)

**Table 2-3956. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 102Ch       |

**Figure 2-1317. CONTROLSS\_CTRL\_FAULT\_ATTR\_STATUS Name Register**

|               |    |    |    |               |    |    |    |
|---------------|----|----|----|---------------|----|----|----|
| 31            | 30 | 29 | 28 | 27            | 26 | 25 | 24 |
| FAULT_XID     |    |    |    |               |    |    |    |
| R             |    |    |    |               |    |    |    |
| 0h            |    |    |    |               |    |    |    |
| 23            | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
| FAULT_XID     |    |    |    | FAULT_ROUTEID |    |    |    |
| R             |    |    |    | R             |    |    |    |
| 0h            |    |    |    | 0h            |    |    |    |
| 15            | 14 | 13 | 12 | 11            | 10 | 9  | 8  |
| FAULT_ROUTEID |    |    |    |               |    |    |    |
| R             |    |    |    |               |    |    |    |
| 0h            |    |    |    |               |    |    |    |
| 7             | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| FAULT_PRIVID  |    |    |    |               |    |    |    |
| R             |    |    |    |               |    |    |    |
| 0h            |    |    |    |               |    |    |    |

**Table 2-3958. CONTROLSS\_CTRL\_FAULT\_ATTR\_STATUS Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description   |
|-------|---------------|------|-------|---------------|
| 31:20 | FAULT_XID     | R    | 0h    | XID.          |
| 19:8  | FAULT_ROUTEID | R    | 0h    | Route ID.     |
| 7:0   | FAULT_PRIVID  | R    | 0h    | Privilege ID. |

## 2.7.2.261 CONTROLSS\_CTRL\_FAULT\_CLEAR Register

### 1 CONTROLSS\_CTRL\_FAULT\_CLEAR Register (Offset = 1030h) [reset = 0h]

Fault Clear register.

Return to [Summary Table](#)

**Table 2-3959. Instance Table**

| Instance Name         | Physical Address |
|-----------------------|------------------|
| CONTROLSS_GLOBAL_CTRL | 502F 1030h       |

**Figure 2-1318. CONTROLSS\_CTRL\_FAULT\_CLEAR Name Register**

|          |    |    |    |    |    |    |           |
|----------|----|----|----|----|----|----|-----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24        |
| RESERVED |    |    |    |    |    |    |           |
| NONE     |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16        |
| RESERVED |    |    |    |    |    |    |           |
| NONE     |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8         |
| RESERVED |    |    |    |    |    |    |           |
| NONE     |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0         |
| RESERVED |    |    |    |    |    |    | FAULT_CLR |
| NONE     |    |    |    |    |    |    | W         |
| 0h       |    |    |    |    |    |    | 0h        |

**Table 2-3961. CONTROLSS\_CTRL\_FAULT\_CLEAR Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                   |
|------|-----------|------|-------|-------------------------------------------------------------------------------|
| 31:1 | RESERVED  | NONE | 0h    | Reserved                                                                      |
| 0    | FAULT_CLR | W    | 0h    | Fault clear. Writing a 1 clears the current fault. Writing a 0 has no effect. |

## Real-time Control Subsystem (CONTROLSS) Registers

---



The Real-time Control Subsystem (CONTROLSS) registers are described in the following sections.

---

**Note**

All images except ADC images uses hexadecimal. ADC uses binary due to legacy documentation.

---

### 3.1 CONTROLSS 16-bit Register Access Note

---

**Note**

8-bit wide register access is **not allowed** for ADC, EPWM, DAC, CMPSS, EQEP, SDFM, and FSI MMR regions. 16-bit access must be used instead.

---

## 3.2 ADC

### ADC

#### 3.2.1 ADC Summaries

#### ADC Summaries

**Table 3-1. ADC\_RESULTS Registers, Base Address=5010 0000h, Length=256**

| Offset | Length | Register Name                             | ADC0_G0_G5 Physical Address | ADC1_G0_G5 Physical Address | ADC2_G0_G5 Physical Address |
|--------|--------|-------------------------------------------|-----------------------------|-----------------------------|-----------------------------|
| 0h     | 16     | <a href="#">ADC_RESULTS_ADCRESULT0</a>    | 5010 0000h                  | 5010 1000h                  | 5010 2000h                  |
| 2h     | 16     | <a href="#">ADC_RESULTS_ADCRESULT1</a>    | 5010 0002h                  | 5010 1002h                  | 5010 2002h                  |
| 4h     | 16     | <a href="#">ADC_RESULTS_ADCRESULT2</a>    | 5010 0004h                  | 5010 1004h                  | 5010 2004h                  |
| 6h     | 16     | <a href="#">ADC_RESULTS_ADCRESULT3</a>    | 5010 0006h                  | 5010 1006h                  | 5010 2006h                  |
| 8h     | 16     | <a href="#">ADC_RESULTS_ADCRESULT4</a>    | 5010 0008h                  | 5010 1008h                  | 5010 2008h                  |
| Ah     | 16     | <a href="#">ADC_RESULTS_ADCRESULT5</a>    | 5010 000Ah                  | 5010 100Ah                  | 5010 200Ah                  |
| Ch     | 16     | <a href="#">ADC_RESULTS_ADCRESULT6</a>    | 5010 000Ch                  | 5010 100Ch                  | 5010 200Ch                  |
| Eh     | 16     | <a href="#">ADC_RESULTS_ADCRESULT7</a>    | 5010 000Eh                  | 5010 100Eh                  | 5010 200Eh                  |
| 10h    | 16     | <a href="#">ADC_RESULTS_ADCRESULT8</a>    | 5010 0010h                  | 5010 1010h                  | 5010 2010h                  |
| 12h    | 16     | <a href="#">ADC_RESULTS_ADCRESULT9</a>    | 5010 0012h                  | 5010 1012h                  | 5010 2012h                  |
| 14h    | 16     | <a href="#">ADC_RESULTS_ADCRESULT10</a>   | 5010 0014h                  | 5010 1014h                  | 5010 2014h                  |
| 16h    | 16     | <a href="#">ADC_RESULTS_ADCRESULT11</a>   | 5010 0016h                  | 5010 1016h                  | 5010 2016h                  |
| 18h    | 16     | <a href="#">ADC_RESULTS_ADCRESULT12</a>   | 5010 0018h                  | 5010 1018h                  | 5010 2018h                  |
| 1Ah    | 16     | <a href="#">ADC_RESULTS_ADCRESULT13</a>   | 5010 001Ah                  | 5010 101Ah                  | 5010 201Ah                  |
| 1Ch    | 16     | <a href="#">ADC_RESULTS_ADCRESULT14</a>   | 5010 001Ch                  | 5010 101Ch                  | 5010 201Ch                  |
| 1Eh    | 16     | <a href="#">ADC_RESULTS_ADCRESULT15</a>   | 5010 001Eh                  | 5010 101Eh                  | 5010 201Eh                  |
| 20h    | 32     | <a href="#">ADC_RESULTS_ADCPPB1RESULT</a> | 5010 0020h                  | 5010 1020h                  | 5010 2020h                  |
| 24h    | 32     | <a href="#">ADC_RESULTS_ADCPPB2RESULT</a> | 5010 0024h                  | 5010 1024h                  | 5010 2024h                  |
| 28h    | 32     | <a href="#">ADC_RESULTS_ADCPPB3RESULT</a> | 5010 0028h                  | 5010 1028h                  | 5010 2028h                  |
| 2Ch    | 32     | <a href="#">ADC_RESULTS_ADCPPB4RESULT</a> | 5010 002Ch                  | 5010 102Ch                  | 5010 202Ch                  |
| 30h    | 32     | <a href="#">ADC_RESULTS_ADCPPB1SUM</a>    | 5010 0030h                  | 5010 1030h                  | 5010 2030h                  |
| 34h    | 16     | <a href="#">ADC_RESULTS_ADCPPB1COUNT</a>  | 5010 0034h                  | 5010 1034h                  | 5010 2034h                  |
| 38h    | 32     | <a href="#">ADC_RESULTS_ADCPPB2SUM</a>    | 5010 0038h                  | 5010 1038h                  | 5010 2038h                  |
| 3Ch    | 16     | <a href="#">ADC_RESULTS_ADCPPB2COUNT</a>  | 5010 003Ch                  | 5010 103Ch                  | 5010 203Ch                  |
| 40h    | 32     | <a href="#">ADC_RESULTS_ADCPPB3SUM</a>    | 5010 0040h                  | 5010 1040h                  | 5010 2040h                  |
| 44h    | 16     | <a href="#">ADC_RESULTS_ADCPPB3COUNT</a>  | 5010 0044h                  | 5010 1044h                  | 5010 2044h                  |
| 48h    | 32     | <a href="#">ADC_RESULTS_ADCPPB4SUM</a>    | 5010 0048h                  | 5010 1048h                  | 5010 2048h                  |
| 4Ch    | 16     | <a href="#">ADC_RESULTS_ADCPPB4COUNT</a>  | 5010 004Ch                  | 5010 104Ch                  | 5010 204Ch                  |
| 50h    | 32     | <a href="#">ADC_RESULTS_ADCPPB1MAX</a>    | 5010 0050h                  | 5010 1050h                  | 5010 2050h                  |
| 54h    | 16     | <a href="#">ADC_RESULTS_ADCPPB1MAXINT</a> | 5010 0054h                  | 5010 1054h                  | 5010 2054h                  |
| 58h    | 32     | <a href="#">ADC_RESULTS_ADCPPB1MIN</a>    | 5010 0058h                  | 5010 1058h                  | 5010 2058h                  |
| 5Ch    | 16     | <a href="#">ADC_RESULTS_ADCPPB1MININT</a> | 5010 005Ch                  | 5010 105Ch                  | 5010 205Ch                  |

**Table 3-1. ADC\_RESULTS Registers, Base Address=5010 0000h, Length=256 (continued)**

| Offset | Length | Register Name                           | ADC0_G0_G5 Physical Address | ADC1_G0_G5 Physical Address | ADC2_G0_G5 Physical Address |
|--------|--------|-----------------------------------------|-----------------------------|-----------------------------|-----------------------------|
| 60h    | 32     | <a href="#">ADC_RESULTS_ADCPPB2MAX</a>  | 5010 0060h                  | 5010 1060h                  | 5010 2060h                  |
| 64h    | 16     | <a href="#">ADC_RESULTS_ADCPPB2MAXI</a> | 5010 0064h                  | 5010 1064h                  | 5010 2064h                  |
| 68h    | 32     | <a href="#">ADC_RESULTS_ADCPPB2MIN</a>  | 5010 0068h                  | 5010 1068h                  | 5010 2068h                  |
| 6Ch    | 16     | <a href="#">ADC_RESULTS_ADCPPB2MINI</a> | 5010 006Ch                  | 5010 106Ch                  | 5010 206Ch                  |
| 70h    | 32     | <a href="#">ADC_RESULTS_ADCPPB3MAX</a>  | 5010 0070h                  | 5010 1070h                  | 5010 2070h                  |
| 74h    | 16     | <a href="#">ADC_RESULTS_ADCPPB3MAXI</a> | 5010 0074h                  | 5010 1074h                  | 5010 2074h                  |
| 78h    | 32     | <a href="#">ADC_RESULTS_ADCPPB3MIN</a>  | 5010 0078h                  | 5010 1078h                  | 5010 2078h                  |
| 7Ch    | 16     | <a href="#">ADC_RESULTS_ADCPPB3MINI</a> | 5010 007Ch                  | 5010 107Ch                  | 5010 207Ch                  |
| 80h    | 32     | <a href="#">ADC_RESULTS_ADCPPB4MAX</a>  | 5010 0080h                  | 5010 1080h                  | 5010 2080h                  |
| 84h    | 16     | <a href="#">ADC_RESULTS_ADCPPB4MAXI</a> | 5010 0084h                  | 5010 1084h                  | 5010 2084h                  |
| 88h    | 32     | <a href="#">ADC_RESULTS_ADCPPB4MIN</a>  | 5010 0088h                  | 5010 1088h                  | 5010 2088h                  |
| 8Ch    | 16     | <a href="#">ADC_RESULTS_ADCPPB4MINI</a> | 5010 008Ch                  | 5010 108Ch                  | 5010 208Ch                  |

**Table 3-2. ADC\_RESULTS Registers, Base Address=5010 0000h, Length=256**

| Offset | Length | Register Name                             | ADC3_G0_G5 Physical Address | ADC4_G0_G5 Physical Address |
|--------|--------|-------------------------------------------|-----------------------------|-----------------------------|
| 0h     | 16     | <a href="#">ADC_RESULTS_ADCRESULT0</a>    | 5010 3000h                  | 5010 4000h                  |
| 2h     | 16     | <a href="#">ADC_RESULTS_ADCRESULT1</a>    | 5010 3002h                  | 5010 4002h                  |
| 4h     | 16     | <a href="#">ADC_RESULTS_ADCRESULT2</a>    | 5010 3004h                  | 5010 4004h                  |
| 6h     | 16     | <a href="#">ADC_RESULTS_ADCRESULT3</a>    | 5010 3006h                  | 5010 4006h                  |
| 8h     | 16     | <a href="#">ADC_RESULTS_ADCRESULT4</a>    | 5010 3008h                  | 5010 4008h                  |
| Ah     | 16     | <a href="#">ADC_RESULTS_ADCRESULT5</a>    | 5010 300Ah                  | 5010 400Ah                  |
| Ch     | 16     | <a href="#">ADC_RESULTS_ADCRESULT6</a>    | 5010 300Ch                  | 5010 400Ch                  |
| Eh     | 16     | <a href="#">ADC_RESULTS_ADCRESULT7</a>    | 5010 300Eh                  | 5010 400Eh                  |
| 10h    | 16     | <a href="#">ADC_RESULTS_ADCRESULT8</a>    | 5010 3010h                  | 5010 4010h                  |
| 12h    | 16     | <a href="#">ADC_RESULTS_ADCRESULT9</a>    | 5010 3012h                  | 5010 4012h                  |
| 14h    | 16     | <a href="#">ADC_RESULTS_ADCRESULT10</a>   | 5010 3014h                  | 5010 4014h                  |
| 16h    | 16     | <a href="#">ADC_RESULTS_ADCRESULT11</a>   | 5010 3016h                  | 5010 4016h                  |
| 18h    | 16     | <a href="#">ADC_RESULTS_ADCRESULT12</a>   | 5010 3018h                  | 5010 4018h                  |
| 1Ah    | 16     | <a href="#">ADC_RESULTS_ADCRESULT13</a>   | 5010 301Ah                  | 5010 401Ah                  |
| 1Ch    | 16     | <a href="#">ADC_RESULTS_ADCRESULT14</a>   | 5010 301Ch                  | 5010 401Ch                  |
| 1Eh    | 16     | <a href="#">ADC_RESULTS_ADCRESULT15</a>   | 5010 301Eh                  | 5010 401Eh                  |
| 20h    | 32     | <a href="#">ADC_RESULTS_ADCPPB1RESULT</a> | 5010 3020h                  | 5010 4020h                  |
| 24h    | 32     | <a href="#">ADC_RESULTS_ADCPPB2RESULT</a> | 5010 3024h                  | 5010 4024h                  |
| 28h    | 32     | <a href="#">ADC_RESULTS_ADCPPB3RESULT</a> | 5010 3028h                  | 5010 4028h                  |
| 2Ch    | 32     | <a href="#">ADC_RESULTS_ADCPPB4RESULT</a> | 5010 302Ch                  | 5010 402Ch                  |
| 30h    | 32     | <a href="#">ADC_RESULTS_ADCPPB1SUM</a>    | 5010 3030h                  | 5010 4030h                  |
| 34h    | 16     | <a href="#">ADC_RESULTS_ADCPPB1COUNT</a>  | 5010 3034h                  | 5010 4034h                  |
| 38h    | 32     | <a href="#">ADC_RESULTS_ADCPPB2SUM</a>    | 5010 3038h                  | 5010 4038h                  |
| 3Ch    | 16     | <a href="#">ADC_RESULTS_ADCPPB2COUNT</a>  | 5010 303Ch                  | 5010 403Ch                  |
| 40h    | 32     | <a href="#">ADC_RESULTS_ADCPPB3SUM</a>    | 5010 3040h                  | 5010 4040h                  |
| 44h    | 16     | <a href="#">ADC_RESULTS_ADCPPB3COUNT</a>  | 5010 3044h                  | 5010 4044h                  |
| 48h    | 32     | <a href="#">ADC_RESULTS_ADCPPB4SUM</a>    | 5010 3048h                  | 5010 4048h                  |
| 4Ch    | 16     | <a href="#">ADC_RESULTS_ADCPPB4COUNT</a>  | 5010 304Ch                  | 5010 404Ch                  |



**Table 3-2. ADC\_RESULTS Registers, Base Address=5010 0000h, Length=256 (continued)**

| Offset | Length | Register Name                           | ADC3_G0_G5 Physical Address | ADC4_G0_G5 Physical Address |
|--------|--------|-----------------------------------------|-----------------------------|-----------------------------|
| 50h    | 32     | <a href="#">ADC_RESULTS_ADCPPB1MAX</a>  | 5010 3050h                  | 5010 4050h                  |
| 54h    | 16     | <a href="#">ADC_RESULTS_ADCPPB1MAXI</a> | 5010 3054h                  | 5010 4054h                  |
| 58h    | 32     | <a href="#">ADC_RESULTS_ADCPPB1MIN</a>  | 5010 3058h                  | 5010 4058h                  |
| 5Ch    | 16     | <a href="#">ADC_RESULTS_ADCPPB1MINI</a> | 5010 305Ch                  | 5010 405Ch                  |
| 60h    | 32     | <a href="#">ADC_RESULTS_ADCPPB2MAX</a>  | 5010 3060h                  | 5010 4060h                  |
| 64h    | 16     | <a href="#">ADC_RESULTS_ADCPPB2MAXI</a> | 5010 3064h                  | 5010 4064h                  |
| 68h    | 32     | <a href="#">ADC_RESULTS_ADCPPB2MIN</a>  | 5010 3068h                  | 5010 4068h                  |
| 6Ch    | 16     | <a href="#">ADC_RESULTS_ADCPPB2MINI</a> | 5010 306Ch                  | 5010 406Ch                  |
| 70h    | 32     | <a href="#">ADC_RESULTS_ADCPPB3MAX</a>  | 5010 3070h                  | 5010 4070h                  |
| 74h    | 16     | <a href="#">ADC_RESULTS_ADCPPB3MAXI</a> | 5010 3074h                  | 5010 4074h                  |
| 78h    | 32     | <a href="#">ADC_RESULTS_ADCPPB3MIN</a>  | 5010 3078h                  | 5010 4078h                  |
| 7Ch    | 16     | <a href="#">ADC_RESULTS_ADCPPB3MINI</a> | 5010 307Ch                  | 5010 407Ch                  |
| 80h    | 32     | <a href="#">ADC_RESULTS_ADCPPB4MAX</a>  | 5010 3080h                  | 5010 4080h                  |
| 84h    | 16     | <a href="#">ADC_RESULTS_ADCPPB4MAXI</a> | 5010 3084h                  | 5010 4084h                  |
| 88h    | 32     | <a href="#">ADC_RESULTS_ADCPPB4MIN</a>  | 5010 3088h                  | 5010 4088h                  |
| 8Ch    | 16     | <a href="#">ADC_RESULTS_ADCPPB4MINI</a> | 5010 308Ch                  | 5010 408Ch                  |

**Table 3-3. ADC\_CFG Registers, Base Address=502C 0000h, Length=256**

| Offset | Length | Register Name                         | ADC0_G0_G5 Physical Address | ADC1_G0_G5 Physical Address | ADC2_G0_G5 Physical Address |
|--------|--------|---------------------------------------|-----------------------------|-----------------------------|-----------------------------|
| 0h     | 16     | <a href="#">ADC_CFG_ADCCTL1</a>       | 502C 0000h                  | 502C 1000h                  | 502C 2000h                  |
| 2h     | 16     | <a href="#">ADC_CFG_ADCCTL2</a>       | 502C 0002h                  | 502C 1002h                  | 502C 2002h                  |
| 4h     | 16     | <a href="#">ADC_CFG_ADCBURSTCTL</a>   | 502C 0004h                  | 502C 1004h                  | 502C 2004h                  |
| 6h     | 16     | <a href="#">ADC_CFG_ADCINTFLG</a>     | 502C 0006h                  | 502C 1006h                  | 502C 2006h                  |
| 8h     | 16     | <a href="#">ADC_CFG_ADCINTFLGCLR</a>  | 502C 0008h                  | 502C 1008h                  | 502C 2008h                  |
| Ah     | 16     | <a href="#">ADC_CFG_ADCINTOVF</a>     | 502C 000Ah                  | 502C 100Ah                  | 502C 200Ah                  |
| Ch     | 16     | <a href="#">ADC_CFG_ADCINTOVFCLR</a>  | 502C 000Ch                  | 502C 100Ch                  | 502C 200Ch                  |
| Eh     | 16     | <a href="#">ADC_CFG_ADCINTSEL1N2</a>  | 502C 000Eh                  | 502C 100Eh                  | 502C 200Eh                  |
| 10h    | 16     | <a href="#">ADC_CFG_ADCINTSEL3N4</a>  | 502C 0010h                  | 502C 1010h                  | 502C 2010h                  |
| 12h    | 16     | <a href="#">ADC_CFG_ADCSOCPRCTL</a>   | 502C 0012h                  | 502C 1012h                  | 502C 2012h                  |
| 14h    | 16     | <a href="#">ADC_CFG_ADCINTSOCSEL1</a> | 502C 0014h                  | 502C 1014h                  | 502C 2014h                  |
| 16h    | 16     | <a href="#">ADC_CFG_ADCINTSOCSEL2</a> | 502C 0016h                  | 502C 1016h                  | 502C 2016h                  |
| 18h    | 16     | <a href="#">ADC_CFG_ADCSOCFLG1</a>    | 502C 0018h                  | 502C 1018h                  | 502C 2018h                  |
| 1Ah    | 16     | <a href="#">ADC_CFG_ADCSOCFRC1</a>    | 502C 001Ah                  | 502C 101Ah                  | 502C 201Ah                  |
| 1Ch    | 16     | <a href="#">ADC_CFG_ADCSOCOVF1</a>    | 502C 001Ch                  | 502C 101Ch                  | 502C 201Ch                  |
| 1Eh    | 16     | <a href="#">ADC_CFG_ADCSOCOVFCLR1</a> | 502C 001Eh                  | 502C 101Eh                  | 502C 201Eh                  |
| 20h    | 32     | <a href="#">ADC_CFG_ADCSOC0CTL</a>    | 502C 0020h                  | 502C 1020h                  | 502C 2020h                  |
| 24h    | 32     | <a href="#">ADC_CFG_ADCSOC1CTL</a>    | 502C 0024h                  | 502C 1024h                  | 502C 2024h                  |
| 28h    | 32     | <a href="#">ADC_CFG_ADCSOC2CTL</a>    | 502C 0028h                  | 502C 1028h                  | 502C 2028h                  |
| 2Ch    | 32     | <a href="#">ADC_CFG_ADCSOC3CTL</a>    | 502C 002Ch                  | 502C 102Ch                  | 502C 202Ch                  |
| 30h    | 32     | <a href="#">ADC_CFG_ADCSOC4CTL</a>    | 502C 0030h                  | 502C 1030h                  | 502C 2030h                  |
| 34h    | 32     | <a href="#">ADC_CFG_ADCSOC5CTL</a>    | 502C 0034h                  | 502C 1034h                  | 502C 2034h                  |
| 38h    | 32     | <a href="#">ADC_CFG_ADCSOC6CTL</a>    | 502C 0038h                  | 502C 1038h                  | 502C 2038h                  |
| 3Ch    | 32     | <a href="#">ADC_CFG_ADCSOC7CTL</a>    | 502C 003Ch                  | 502C 103Ch                  | 502C 203Ch                  |

**Table 3-3. ADC\_CFG Registers, Base Address=502C 0000h, Length=256 (continued)**

| Offset | Length | Register Name                                  | ADC0_G0_G5 Physical Address | ADC1_G0_G5 Physical Address | ADC2_G0_G5 Physical Address |
|--------|--------|------------------------------------------------|-----------------------------|-----------------------------|-----------------------------|
| 40h    | 32     | <a href="#">ADC_CFG_ADCSOC8CTL</a>             | 502C 0040h                  | 502C 1040h                  | 502C 2040h                  |
| 44h    | 32     | <a href="#">ADC_CFG_ADCSOC9CTL</a>             | 502C 0044h                  | 502C 1044h                  | 502C 2044h                  |
| 48h    | 32     | <a href="#">ADC_CFG_ADCSOC10CTL</a>            | 502C 0048h                  | 502C 1048h                  | 502C 2048h                  |
| 4Ch    | 32     | <a href="#">ADC_CFG_ADCSOC11CTL</a>            | 502C 004Ch                  | 502C 104Ch                  | 502C 204Ch                  |
| 50h    | 32     | <a href="#">ADC_CFG_ADCSOC12CTL</a>            | 502C 0050h                  | 502C 1050h                  | 502C 2050h                  |
| 54h    | 32     | <a href="#">ADC_CFG_ADCSOC13CTL</a>            | 502C 0054h                  | 502C 1054h                  | 502C 2054h                  |
| 58h    | 32     | <a href="#">ADC_CFG_ADCSOC14CTL</a>            | 502C 0058h                  | 502C 1058h                  | 502C 2058h                  |
| 5Ch    | 32     | <a href="#">ADC_CFG_ADCSOC15CTL</a>            | 502C 005Ch                  | 502C 105Ch                  | 502C 205Ch                  |
| 60h    | 16     | <a href="#">ADC_CFG_ADCEVTSTAT</a>             | 502C 0060h                  | 502C 1060h                  | 502C 2060h                  |
| 64h    | 16     | <a href="#">ADC_CFG_ADCEVTCLR</a>              | 502C 0064h                  | 502C 1064h                  | 502C 2064h                  |
| 68h    | 16     | <a href="#">ADC_CFG_ADCEVTSEL</a>              | 502C 0068h                  | 502C 1068h                  | 502C 2068h                  |
| 6Ch    | 16     | <a href="#">ADC_CFG_ADCEVTINTSEL</a>           | 502C 006Ch                  | 502C 106Ch                  | 502C 206Ch                  |
| 70h    | 16     | <a href="#">ADC_CFG_ADCOSDETECT</a>            | 502C 0070h                  | 502C 1070h                  | 502C 2070h                  |
| 72h    | 16     | <a href="#">ADC_CFG_ADCCOUNTER</a>             | 502C 0072h                  | 502C 1072h                  | 502C 2072h                  |
| 74h    | 16     | <a href="#">ADC_CFG_ADCREV</a>                 | 502C 0074h                  | 502C 1074h                  | 502C 2074h                  |
| 76h    | 16     | <a href="#">ADC_CFG_ADCOFFTRIM</a>             | 502C 0076h                  | 502C 1076h                  | 502C 2076h                  |
| 7Ah    | 16     | <a href="#">ADC_CFG_ADCOFFTRIM3</a>            | 502C 007Ah                  | 502C 107Ah                  | 502C 207Ah                  |
| 80h    | 16     | <a href="#">ADC_CFG_ADCPPB1CONFIG</a>          | 502C 0080h                  | 502C 1080h                  | 502C 2080h                  |
| 82h    | 16     | <a href="#">ADC_CFG_ADCPPB1STAMP</a>           | 502C 0082h                  | 502C 1082h                  | 502C 2082h                  |
| 84h    | 16     | <a href="#">ADC_CFG_ADCPPB1OFFCAL</a>          | 502C 0084h                  | 502C 1084h                  | 502C 2084h                  |
| 86h    | 16     | <a href="#">ADC_CFG_ADCPPB1OFFREF</a>          | 502C 0086h                  | 502C 1086h                  | 502C 2086h                  |
| 88h    | 32     | <a href="#">ADC_CFG_ADCPPB1TRIPHI</a>          | 502C 0088h                  | 502C 1088h                  | 502C 2088h                  |
| 8Ch    | 32     | <a href="#">ADC_CFG_ADCPPB1TRIPLO</a>          | 502C 008Ch                  | 502C 108Ch                  | 502C 208Ch                  |
| 90h    | 16     | <a href="#">ADC_CFG_ADCPPB2CONFIG</a>          | 502C 0090h                  | 502C 1090h                  | 502C 2090h                  |
| 92h    | 16     | <a href="#">ADC_CFG_ADCPPB2STAMP</a>           | 502C 0092h                  | 502C 1092h                  | 502C 2092h                  |
| 94h    | 16     | <a href="#">ADC_CFG_ADCPPB2OFFCAL</a>          | 502C 0094h                  | 502C 1094h                  | 502C 2094h                  |
| 96h    | 16     | <a href="#">ADC_CFG_ADCPPB2OFFREF</a>          | 502C 0096h                  | 502C 1096h                  | 502C 2096h                  |
| 98h    | 32     | <a href="#">ADC_CFG_ADCPPB2TRIPHI</a>          | 502C 0098h                  | 502C 1098h                  | 502C 2098h                  |
| 9Ch    | 32     | <a href="#">ADC_CFG_ADCPPB2TRIPLO</a>          | 502C 009Ch                  | 502C 109Ch                  | 502C 209Ch                  |
| A0h    | 16     | <a href="#">ADC_CFG_ADCPPB3CONFIG</a>          | 502C 00A0h                  | 502C 10A0h                  | 502C 20A0h                  |
| A2h    | 16     | <a href="#">ADC_CFG_ADCPPB3STAMP</a>           | 502C 00A2h                  | 502C 10A2h                  | 502C 20A2h                  |
| A4h    | 16     | <a href="#">ADC_CFG_ADCPPB3OFFCAL</a>          | 502C 00A4h                  | 502C 10A4h                  | 502C 20A4h                  |
| A6h    | 16     | <a href="#">ADC_CFG_ADCPPB3OFFREF</a>          | 502C 00A6h                  | 502C 10A6h                  | 502C 20A6h                  |
| A8h    | 32     | <a href="#">ADC_CFG_ADCPPB3TRIPHI</a>          | 502C 00A8h                  | 502C 10A8h                  | 502C 20A8h                  |
| ACh    | 32     | <a href="#">ADC_CFG_ADCPPB3TRIPLO</a>          | 502C 00ACh                  | 502C 10ACh                  | 502C 20ACh                  |
| B0h    | 16     | <a href="#">ADC_CFG_ADCPPB4CONFIG</a>          | 502C 00B0h                  | 502C 10B0h                  | 502C 20B0h                  |
| B2h    | 16     | <a href="#">ADC_CFG_ADCPPB4STAMP</a>           | 502C 00B2h                  | 502C 10B2h                  | 502C 20B2h                  |
| B4h    | 16     | <a href="#">ADC_CFG_ADCPPB4OFFCAL</a>          | 502C 00B4h                  | 502C 10B4h                  | 502C 20B4h                  |
| B6h    | 16     | <a href="#">ADC_CFG_ADCPPB4OFFREF</a>          | 502C 00B6h                  | 502C 10B6h                  | 502C 20B6h                  |
| B8h    | 32     | <a href="#">ADC_CFG_ADCPPB4TRIPHI</a>          | 502C 00B8h                  | 502C 10B8h                  | 502C 20B8h                  |
| BCh    | 32     | <a href="#">ADC_CFG_ADCPPB4TRIPLO</a>          | 502C 00BCh                  | 502C 10BCh                  | 502C 20BCh                  |
| C0h    | 32     | <a href="#">ADC_CFG_ADCSAFECHECKRES<br/>EN</a> | 502C 00C0h                  | 502C 10C0h                  | 502C 20C0h                  |
| DEh    | 16     | <a href="#">ADC_CFG_ADCINTCYCLE</a>            | 502C 00DEh                  | 502C 10DEh                  | 502C 20DEh                  |
| E0h    | 32     | <a href="#">ADC_CFG_ADCINLTRIM1</a>            | 502C 00E0h                  | 502C 10E0h                  | 502C 20E0h                  |

**Table 3-3. ADC\_CFG Registers, Base Address=502C 0000h, Length=256 (continued)**

| Offset | Length | Register Name                          | ADC0_G0_G5 Physical Address | ADC1_G0_G5 Physical Address | ADC2_G0_G5 Physical Address |
|--------|--------|----------------------------------------|-----------------------------|-----------------------------|-----------------------------|
| E4h    | 32     | <a href="#">ADC_CFG_ADCINLTRIM2</a>    | 502C 00E4h                  | 502C 10E4h                  | 502C 20E4h                  |
| E8h    | 32     | <a href="#">ADC_CFG_ADCINLTRIM3</a>    | 502C 00E8h                  | 502C 10E8h                  | 502C 20E8h                  |
| ECh    | 32     | <a href="#">ADC_CFG_ADCINLTRIM4</a>    | 502C 00ECh                  | 502C 10ECh                  | 502C 20ECh                  |
| F0h    | 32     | <a href="#">ADC_CFG_ADCINLTRIM5</a>    | 502C 00F0h                  | 502C 10F0h                  | 502C 20F0h                  |
| F4h    | 32     | <a href="#">ADC_CFG_ADCINLTRIM6</a>    | 502C 00F4h                  | 502C 10F4h                  | 502C 20F4h                  |
| FAh    | 16     | <a href="#">ADC_CFG_ADCREV2</a>        | 502C 00FAh                  | 502C 10FAh                  | 502C 20FAh                  |
| FCh    | 32     | <a href="#">ADC_CFG_ADCINLTRIMCTL</a>  | 502C 00FCh                  | 502C 10FCh                  | 502C 20FCh                  |
| 100h   | 32     | <a href="#">ADC_CFG_REP1CTL</a>        | 502C 0100h                  | 502C 1100h                  | 502C 2100h                  |
| 104h   | 32     | <a href="#">ADC_CFG_REP1N</a>          | 502C 0104h                  | 502C 1104h                  | 502C 2104h                  |
| 108h   | 32     | <a href="#">ADC_CFG_REP1PHASE</a>      | 502C 0108h                  | 502C 1108h                  | 502C 2108h                  |
| 10Ch   | 32     | <a href="#">ADC_CFG_REP1SPREAD</a>     | 502C 010Ch                  | 502C 110Ch                  | 502C 210Ch                  |
| 110h   | 16     | <a href="#">ADC_CFG_REP1FRC</a>        | 502C 0110h                  | 502C 1110h                  | 502C 2110h                  |
| 120h   | 32     | <a href="#">ADC_CFG_REP2CTL</a>        | 502C 0120h                  | 502C 1120h                  | 502C 2120h                  |
| 124h   | 32     | <a href="#">ADC_CFG_REP2N</a>          | 502C 0124h                  | 502C 1124h                  | 502C 2124h                  |
| 128h   | 32     | <a href="#">ADC_CFG_REP2PHASE</a>      | 502C 0128h                  | 502C 1128h                  | 502C 2128h                  |
| 12Ch   | 32     | <a href="#">ADC_CFG_REP2SPREAD</a>     | 502C 012Ch                  | 502C 112Ch                  | 502C 212Ch                  |
| 130h   | 16     | <a href="#">ADC_CFG_REP2FRC</a>        | 502C 0130h                  | 502C 1130h                  | 502C 2130h                  |
| 140h   | 16     | <a href="#">ADC_CFG_ADCPPB1LIMIT</a>   | 502C 0140h                  | 502C 1140h                  | 502C 2140h                  |
| 144h   | 16     | <a href="#">ADC_CFG_ADCPPBP1PCOUNT</a> | 502C 0144h                  | 502C 1144h                  | 502C 2144h                  |
| 148h   | 16     | <a href="#">ADC_CFG_ADCPPB1CONFIG2</a> | 502C 0148h                  | 502C 1148h                  | 502C 2148h                  |
| 14Ch   | 32     | <a href="#">ADC_CFG_ADCPPB1PSUM</a>    | 502C 014Ch                  | 502C 114Ch                  | 502C 214Ch                  |
| 150h   | 32     | <a href="#">ADC_CFG_ADCPPB1PMAX</a>    | 502C 0150h                  | 502C 1150h                  | 502C 2150h                  |
| 154h   | 16     | <a href="#">ADC_CFG_ADCPPB1PMAXI</a>   | 502C 0154h                  | 502C 1154h                  | 502C 2154h                  |
| 158h   | 32     | <a href="#">ADC_CFG_ADCPPB1PMIN</a>    | 502C 0158h                  | 502C 1158h                  | 502C 2158h                  |
| 15Ch   | 16     | <a href="#">ADC_CFG_ADCPPB1PMINI</a>   | 502C 015Ch                  | 502C 115Ch                  | 502C 215Ch                  |
| 160h   | 32     | <a href="#">ADC_CFG_ADCPPB1TRIPLO2</a> | 502C 0160h                  | 502C 1160h                  | 502C 2160h                  |
| 174h   | 16     | <a href="#">ADC_CFG_ADCPPB2LIMIT</a>   | 502C 0174h                  | 502C 1174h                  | 502C 2174h                  |
| 178h   | 16     | <a href="#">ADC_CFG_ADCPPBP2PCOUNT</a> | 502C 0178h                  | 502C 1178h                  | 502C 2178h                  |
| 17Ch   | 16     | <a href="#">ADC_CFG_ADCPPB2CONFIG2</a> | 502C 017Ch                  | 502C 117Ch                  | 502C 217Ch                  |
| 180h   | 32     | <a href="#">ADC_CFG_ADCPPB2PSUM</a>    | 502C 0180h                  | 502C 1180h                  | 502C 2180h                  |
| 184h   | 32     | <a href="#">ADC_CFG_ADCPPB2PMAX</a>    | 502C 0184h                  | 502C 1184h                  | 502C 2184h                  |
| 188h   | 16     | <a href="#">ADC_CFG_ADCPPB2PMAXI</a>   | 502C 0188h                  | 502C 1188h                  | 502C 2188h                  |
| 18Ch   | 32     | <a href="#">ADC_CFG_ADCPPB2PMIN</a>    | 502C 018Ch                  | 502C 118Ch                  | 502C 218Ch                  |
| 190h   | 16     | <a href="#">ADC_CFG_ADCPPB2PMINI</a>   | 502C 0190h                  | 502C 1190h                  | 502C 2190h                  |
| 194h   | 32     | <a href="#">ADC_CFG_ADCPPB2TRIPLO2</a> | 502C 0194h                  | 502C 1194h                  | 502C 2194h                  |
| 1A8h   | 16     | <a href="#">ADC_CFG_ADCPPB3LIMIT</a>   | 502C 01A8h                  | 502C 11A8h                  | 502C 21A8h                  |
| 1ACh   | 16     | <a href="#">ADC_CFG_ADCPPBP3PCOUNT</a> | 502C 01ACh                  | 502C 11ACh                  | 502C 21ACh                  |
| 1B0h   | 16     | <a href="#">ADC_CFG_ADCPPB3CONFIG2</a> | 502C 01B0h                  | 502C 11B0h                  | 502C 21B0h                  |
| 1B4h   | 32     | <a href="#">ADC_CFG_ADCPPB3PSUM</a>    | 502C 01B4h                  | 502C 11B4h                  | 502C 21B4h                  |
| 1B8h   | 32     | <a href="#">ADC_CFG_ADCPPB3PMAX</a>    | 502C 01B8h                  | 502C 11B8h                  | 502C 21B8h                  |
| 1BCh   | 16     | <a href="#">ADC_CFG_ADCPPB3PMAXI</a>   | 502C 01BCh                  | 502C 11BCh                  | 502C 21BCh                  |
| 1C0h   | 32     | <a href="#">ADC_CFG_ADCPPB3PMIN</a>    | 502C 01C0h                  | 502C 11C0h                  | 502C 21C0h                  |
| 1C4h   | 16     | <a href="#">ADC_CFG_ADCPPB3PMINI</a>   | 502C 01C4h                  | 502C 11C4h                  | 502C 21C4h                  |
| 1C8h   | 32     | <a href="#">ADC_CFG_ADCPPB3TRIPLO2</a> | 502C 01C8h                  | 502C 11C8h                  | 502C 21C8h                  |

**Table 3-3. ADC\_CFG Registers, Base Address=502C 0000h, Length=256 (continued)**

| Offset | Length | Register Name                          | ADC0_G0_G5 Physical Address | ADC1_G0_G5 Physical Address | ADC2_G0_G5 Physical Address |
|--------|--------|----------------------------------------|-----------------------------|-----------------------------|-----------------------------|
| 1DCh   | 16     | <a href="#">ADC_CFG_ADCPPB4LIMIT</a>   | 502C 01DCh                  | 502C 11DCh                  | 502C 21DCh                  |
| 1E0h   | 16     | <a href="#">ADC_CFG_ADCPPB4PCOUNT</a>  | 502C 01E0h                  | 502C 11E0h                  | 502C 21E0h                  |
| 1E4h   | 16     | <a href="#">ADC_CFG_ADCPPB4CONFIG2</a> | 502C 01E4h                  | 502C 11E4h                  | 502C 21E4h                  |
| 1E8h   | 32     | <a href="#">ADC_CFG_ADCPPB4PSUM</a>    | 502C 01E8h                  | 502C 11E8h                  | 502C 21E8h                  |
| 1ECh   | 32     | <a href="#">ADC_CFG_ADCPPB4PMAX</a>    | 502C 01ECh                  | 502C 11ECh                  | 502C 21ECh                  |
| 1F0h   | 16     | <a href="#">ADC_CFG_ADCPPB4PMAXI</a>   | 502C 01F0h                  | 502C 11F0h                  | 502C 21F0h                  |
| 1F4h   | 32     | <a href="#">ADC_CFG_ADCPPB4PMIN</a>    | 502C 01F4h                  | 502C 11F4h                  | 502C 21F4h                  |
| 1F8h   | 16     | <a href="#">ADC_CFG_ADCPPB4PMINI</a>   | 502C 01F8h                  | 502C 11F8h                  | 502C 21F8h                  |
| 1FCh   | 32     | <a href="#">ADC_CFG_ADCPPB4TRIPLO2</a> | 502C 01FCh                  | 502C 11FCh                  | 502C 21FCh                  |

**Table 3-4. ADC\_CFG Registers, Base Address=502C 0000h, Length=256**

| Offset | Length | Register Name                         | ADC3_G0_G5 Physical Address | ADC4_G0_G5 Physical Address |
|--------|--------|---------------------------------------|-----------------------------|-----------------------------|
| 0h     | 16     | <a href="#">ADC_CFG_ADCCTL1</a>       | 502C 3000h                  | 502C 4000h                  |
| 2h     | 16     | <a href="#">ADC_CFG_ADCCTL2</a>       | 502C 3002h                  | 502C 4002h                  |
| 4h     | 16     | <a href="#">ADC_CFG_ADCBURSTCTL</a>   | 502C 3004h                  | 502C 4004h                  |
| 6h     | 16     | <a href="#">ADC_CFG_ADCINTFLG</a>     | 502C 3006h                  | 502C 4006h                  |
| 8h     | 16     | <a href="#">ADC_CFG_ADCINTFLGCLR</a>  | 502C 3008h                  | 502C 4008h                  |
| Ah     | 16     | <a href="#">ADC_CFG_ADCINTOVF</a>     | 502C 300Ah                  | 502C 400Ah                  |
| Ch     | 16     | <a href="#">ADC_CFG_ADCINTOVFCLR</a>  | 502C 300Ch                  | 502C 400Ch                  |
| Eh     | 16     | <a href="#">ADC_CFG_ADCINTSEL1N2</a>  | 502C 300Eh                  | 502C 400Eh                  |
| 10h    | 16     | <a href="#">ADC_CFG_ADCINTSEL3N4</a>  | 502C 3010h                  | 502C 4010h                  |
| 12h    | 16     | <a href="#">ADC_CFG_ADCSOPRCTL</a>    | 502C 3012h                  | 502C 4012h                  |
| 14h    | 16     | <a href="#">ADC_CFG_ADCINTSOCSEL1</a> | 502C 3014h                  | 502C 4014h                  |
| 16h    | 16     | <a href="#">ADC_CFG_ADCINTSOCSEL2</a> | 502C 3016h                  | 502C 4016h                  |
| 18h    | 16     | <a href="#">ADC_CFG_ADCSOCFLG1</a>    | 502C 3018h                  | 502C 4018h                  |
| 1Ah    | 16     | <a href="#">ADC_CFG_ADCSOCFRC1</a>    | 502C 301Ah                  | 502C 401Ah                  |
| 1Ch    | 16     | <a href="#">ADC_CFG_ADCSOCOVF1</a>    | 502C 301Ch                  | 502C 401Ch                  |
| 1Eh    | 16     | <a href="#">ADC_CFG_ADCSOCOVFCLR1</a> | 502C 301Eh                  | 502C 401Eh                  |
| 20h    | 32     | <a href="#">ADC_CFG_ADCSOC0CTL</a>    | 502C 3020h                  | 502C 4020h                  |
| 24h    | 32     | <a href="#">ADC_CFG_ADCSOC1CTL</a>    | 502C 3024h                  | 502C 4024h                  |
| 28h    | 32     | <a href="#">ADC_CFG_ADCSOC2CTL</a>    | 502C 3028h                  | 502C 4028h                  |
| 2Ch    | 32     | <a href="#">ADC_CFG_ADCSOC3CTL</a>    | 502C 302Ch                  | 502C 402Ch                  |
| 30h    | 32     | <a href="#">ADC_CFG_ADCSOC4CTL</a>    | 502C 3030h                  | 502C 4030h                  |
| 34h    | 32     | <a href="#">ADC_CFG_ADCSOC5CTL</a>    | 502C 3034h                  | 502C 4034h                  |
| 38h    | 32     | <a href="#">ADC_CFG_ADCSOC6CTL</a>    | 502C 3038h                  | 502C 4038h                  |
| 3Ch    | 32     | <a href="#">ADC_CFG_ADCSOC7CTL</a>    | 502C 303Ch                  | 502C 403Ch                  |
| 40h    | 32     | <a href="#">ADC_CFG_ADCSOC8CTL</a>    | 502C 3040h                  | 502C 4040h                  |
| 44h    | 32     | <a href="#">ADC_CFG_ADCSOC9CTL</a>    | 502C 3044h                  | 502C 4044h                  |
| 48h    | 32     | <a href="#">ADC_CFG_ADCSOC10CTL</a>   | 502C 3048h                  | 502C 4048h                  |
| 4Ch    | 32     | <a href="#">ADC_CFG_ADCSOC11CTL</a>   | 502C 304Ch                  | 502C 404Ch                  |
| 50h    | 32     | <a href="#">ADC_CFG_ADCSOC12CTL</a>   | 502C 3050h                  | 502C 4050h                  |
| 54h    | 32     | <a href="#">ADC_CFG_ADCSOC13CTL</a>   | 502C 3054h                  | 502C 4054h                  |
| 58h    | 32     | <a href="#">ADC_CFG_ADCSOC14CTL</a>   | 502C 3058h                  | 502C 4058h                  |

**Table 3-4. ADC\_CFG Registers, Base Address=502C 0000h, Length=256 (continued)**

| Offset | Length | Register Name                             | ADC3_G0_G5 Physical Address | ADC4_G0_G5 Physical Address |
|--------|--------|-------------------------------------------|-----------------------------|-----------------------------|
| 5Ch    | 32     | <a href="#">ADC_CFG_ADCSOC15CTL</a>       | 502C 305Ch                  | 502C 405Ch                  |
| 60h    | 16     | <a href="#">ADC_CFG_ADCEVTSTAT</a>        | 502C 3060h                  | 502C 4060h                  |
| 64h    | 16     | <a href="#">ADC_CFG_ADCEVTCLR</a>         | 502C 3064h                  | 502C 4064h                  |
| 68h    | 16     | <a href="#">ADC_CFG_ADCEVTSEL</a>         | 502C 3068h                  | 502C 4068h                  |
| 6Ch    | 16     | <a href="#">ADC_CFG_ADCEVTINTSEL</a>      | 502C 306Ch                  | 502C 406Ch                  |
| 70h    | 16     | <a href="#">ADC_CFG_ADCOSDETECT</a>       | 502C 3070h                  | 502C 4070h                  |
| 72h    | 16     | <a href="#">ADC_CFG_ADCCOUNTER</a>        | 502C 3072h                  | 502C 4072h                  |
| 74h    | 16     | <a href="#">ADC_CFG_ADCREV</a>            | 502C 3074h                  | 502C 4074h                  |
| 76h    | 16     | <a href="#">ADC_CFG_ADCOFFTRIM</a>        | 502C 3076h                  | 502C 4076h                  |
| 7Ah    | 16     | <a href="#">ADC_CFG_ADCOFFTRIM3</a>       | 502C 307Ah                  | 502C 407Ah                  |
| 80h    | 16     | <a href="#">ADC_CFG_ADCPPB1CONFIG</a>     | 502C 3080h                  | 502C 4080h                  |
| 82h    | 16     | <a href="#">ADC_CFG_ADCPPB1STAMP</a>      | 502C 3082h                  | 502C 4082h                  |
| 84h    | 16     | <a href="#">ADC_CFG_ADCPPB1OFFCAL</a>     | 502C 3084h                  | 502C 4084h                  |
| 86h    | 16     | <a href="#">ADC_CFG_ADCPPB1OFFREF</a>     | 502C 3086h                  | 502C 4086h                  |
| 88h    | 32     | <a href="#">ADC_CFG_ADCPPB1TRIPHI</a>     | 502C 3088h                  | 502C 4088h                  |
| 8Ch    | 32     | <a href="#">ADC_CFG_ADCPPB1TRIPLO</a>     | 502C 308Ch                  | 502C 408Ch                  |
| 90h    | 16     | <a href="#">ADC_CFG_ADCPPB2CONFIG</a>     | 502C 3090h                  | 502C 4090h                  |
| 92h    | 16     | <a href="#">ADC_CFG_ADCPPB2STAMP</a>      | 502C 3092h                  | 502C 4092h                  |
| 94h    | 16     | <a href="#">ADC_CFG_ADCPPB2OFFCAL</a>     | 502C 3094h                  | 502C 4094h                  |
| 96h    | 16     | <a href="#">ADC_CFG_ADCPPB2OFFREF</a>     | 502C 3096h                  | 502C 4096h                  |
| 98h    | 32     | <a href="#">ADC_CFG_ADCPPB2TRIPHI</a>     | 502C 3098h                  | 502C 4098h                  |
| 9Ch    | 32     | <a href="#">ADC_CFG_ADCPPB2TRIPLO</a>     | 502C 309Ch                  | 502C 409Ch                  |
| A0h    | 16     | <a href="#">ADC_CFG_ADCPPB3CONFIG</a>     | 502C 30A0h                  | 502C 40A0h                  |
| A2h    | 16     | <a href="#">ADC_CFG_ADCPPB3STAMP</a>      | 502C 30A2h                  | 502C 40A2h                  |
| A4h    | 16     | <a href="#">ADC_CFG_ADCPPB3OFFCAL</a>     | 502C 30A4h                  | 502C 40A4h                  |
| A6h    | 16     | <a href="#">ADC_CFG_ADCPPB3OFFREF</a>     | 502C 30A6h                  | 502C 40A6h                  |
| A8h    | 32     | <a href="#">ADC_CFG_ADCPPB3TRIPHI</a>     | 502C 30A8h                  | 502C 40A8h                  |
| ACh    | 32     | <a href="#">ADC_CFG_ADCPPB3TRIPLO</a>     | 502C 30ACh                  | 502C 40ACh                  |
| B0h    | 16     | <a href="#">ADC_CFG_ADCPPB4CONFIG</a>     | 502C 30B0h                  | 502C 40B0h                  |
| B2h    | 16     | <a href="#">ADC_CFG_ADCPPB4STAMP</a>      | 502C 30B2h                  | 502C 40B2h                  |
| B4h    | 16     | <a href="#">ADC_CFG_ADCPPB4OFFCAL</a>     | 502C 30B4h                  | 502C 40B4h                  |
| B6h    | 16     | <a href="#">ADC_CFG_ADCPPB4OFFREF</a>     | 502C 30B6h                  | 502C 40B6h                  |
| B8h    | 32     | <a href="#">ADC_CFG_ADCPPB4TRIPHI</a>     | 502C 30B8h                  | 502C 40B8h                  |
| BCh    | 32     | <a href="#">ADC_CFG_ADCPPB4TRIPLO</a>     | 502C 30BCh                  | 502C 40BCh                  |
| C0h    | 32     | <a href="#">ADC_CFG_ADCSAFECHECKRESEN</a> | 502C 30C0h                  | 502C 40C0h                  |
| DEh    | 16     | <a href="#">ADC_CFG_ADCINTCYCLE</a>       | 502C 30DEh                  | 502C 40DEh                  |
| E0h    | 32     | <a href="#">ADC_CFG_ADCINLTRIM1</a>       | 502C 30E0h                  | 502C 40E0h                  |
| E4h    | 32     | <a href="#">ADC_CFG_ADCINLTRIM2</a>       | 502C 30E4h                  | 502C 40E4h                  |
| E8h    | 32     | <a href="#">ADC_CFG_ADCINLTRIM3</a>       | 502C 30E8h                  | 502C 40E8h                  |
| ECh    | 32     | <a href="#">ADC_CFG_ADCINLTRIM4</a>       | 502C 30ECh                  | 502C 40ECh                  |
| F0h    | 32     | <a href="#">ADC_CFG_ADCINLTRIM5</a>       | 502C 30F0h                  | 502C 40F0h                  |
| F4h    | 32     | <a href="#">ADC_CFG_ADCINLTRIM6</a>       | 502C 30F4h                  | 502C 40F4h                  |
| FAh    | 16     | <a href="#">ADC_CFG_ADCREV2</a>           | 502C 30FAh                  | 502C 40FAh                  |
| FCh    | 32     | <a href="#">ADC_CFG_ADCINLTRIMCTL</a>     | 502C 30FCh                  | 502C 40FCh                  |

**Table 3-4. ADC\_CFG Registers, Base Address=502C 0000h, Length=256 (continued)**

| Offset | Length | Register Name                          | ADC3_G0_G5 Physical Address | ADC4_G0_G5 Physical Address |
|--------|--------|----------------------------------------|-----------------------------|-----------------------------|
| 100h   | 32     | <a href="#">ADC_CFG_REP1CTL</a>        | 502C 3100h                  | 502C 4100h                  |
| 104h   | 32     | <a href="#">ADC_CFG_REP1N</a>          | 502C 3104h                  | 502C 4104h                  |
| 108h   | 32     | <a href="#">ADC_CFG_REP1PHASE</a>      | 502C 3108h                  | 502C 4108h                  |
| 10Ch   | 32     | <a href="#">ADC_CFG_REP1SPREAD</a>     | 502C 310Ch                  | 502C 410Ch                  |
| 110h   | 16     | <a href="#">ADC_CFG_REP1FRC</a>        | 502C 3110h                  | 502C 4110h                  |
| 120h   | 32     | <a href="#">ADC_CFG_REP2CTL</a>        | 502C 3120h                  | 502C 4120h                  |
| 124h   | 32     | <a href="#">ADC_CFG_REP2N</a>          | 502C 3124h                  | 502C 4124h                  |
| 128h   | 32     | <a href="#">ADC_CFG_REP2PHASE</a>      | 502C 3128h                  | 502C 4128h                  |
| 12Ch   | 32     | <a href="#">ADC_CFG_REP2SPREAD</a>     | 502C 312Ch                  | 502C 412Ch                  |
| 130h   | 16     | <a href="#">ADC_CFG_REP2FRC</a>        | 502C 3130h                  | 502C 4130h                  |
| 140h   | 16     | <a href="#">ADC_CFG_ADCPPB1LIMIT</a>   | 502C 3140h                  | 502C 4140h                  |
| 144h   | 16     | <a href="#">ADC_CFG_ADCPPB1PCOUNT</a>  | 502C 3144h                  | 502C 4144h                  |
| 148h   | 16     | <a href="#">ADC_CFG_ADCPPB1CONFIG2</a> | 502C 3148h                  | 502C 4148h                  |
| 14Ch   | 32     | <a href="#">ADC_CFG_ADCPPB1PSUM</a>    | 502C 314Ch                  | 502C 414Ch                  |
| 150h   | 32     | <a href="#">ADC_CFG_ADCPPB1PMAX</a>    | 502C 3150h                  | 502C 4150h                  |
| 154h   | 16     | <a href="#">ADC_CFG_ADCPPB1PMAXI</a>   | 502C 3154h                  | 502C 4154h                  |
| 158h   | 32     | <a href="#">ADC_CFG_ADCPPB1PMIN</a>    | 502C 3158h                  | 502C 4158h                  |
| 15Ch   | 16     | <a href="#">ADC_CFG_ADCPPB1PMINI</a>   | 502C 315Ch                  | 502C 415Ch                  |
| 160h   | 32     | <a href="#">ADC_CFG_ADCPPB1TRIPLO2</a> | 502C 3160h                  | 502C 4160h                  |
| 174h   | 16     | <a href="#">ADC_CFG_ADCPPB2LIMIT</a>   | 502C 3174h                  | 502C 4174h                  |
| 178h   | 16     | <a href="#">ADC_CFG_ADCPPB2PCOUNT</a>  | 502C 3178h                  | 502C 4178h                  |
| 17Ch   | 16     | <a href="#">ADC_CFG_ADCPPB2CONFIG2</a> | 502C 317Ch                  | 502C 417Ch                  |
| 180h   | 32     | <a href="#">ADC_CFG_ADCPPB2PSUM</a>    | 502C 3180h                  | 502C 4180h                  |
| 184h   | 32     | <a href="#">ADC_CFG_ADCPPB2PMAX</a>    | 502C 3184h                  | 502C 4184h                  |
| 188h   | 16     | <a href="#">ADC_CFG_ADCPPB2PMAXI</a>   | 502C 3188h                  | 502C 4188h                  |
| 18Ch   | 32     | <a href="#">ADC_CFG_ADCPPB2PMIN</a>    | 502C 318Ch                  | 502C 418Ch                  |
| 190h   | 16     | <a href="#">ADC_CFG_ADCPPB2PMINI</a>   | 502C 3190h                  | 502C 4190h                  |
| 194h   | 32     | <a href="#">ADC_CFG_ADCPPB2TRIPLO2</a> | 502C 3194h                  | 502C 4194h                  |
| 1A8h   | 16     | <a href="#">ADC_CFG_ADCPPB3LIMIT</a>   | 502C 31A8h                  | 502C 41A8h                  |
| 1ACh   | 16     | <a href="#">ADC_CFG_ADCPPB3PCOUNT</a>  | 502C 31ACh                  | 502C 41ACh                  |
| 1B0h   | 16     | <a href="#">ADC_CFG_ADCPPB3CONFIG2</a> | 502C 31B0h                  | 502C 41B0h                  |
| 1B4h   | 32     | <a href="#">ADC_CFG_ADCPPB3PSUM</a>    | 502C 31B4h                  | 502C 41B4h                  |
| 1B8h   | 32     | <a href="#">ADC_CFG_ADCPPB3PMAX</a>    | 502C 31B8h                  | 502C 41B8h                  |
| 1BCh   | 16     | <a href="#">ADC_CFG_ADCPPB3PMAXI</a>   | 502C 31BCh                  | 502C 41BCh                  |
| 1C0h   | 32     | <a href="#">ADC_CFG_ADCPPB3PMIN</a>    | 502C 31C0h                  | 502C 41C0h                  |
| 1C4h   | 16     | <a href="#">ADC_CFG_ADCPPB3PMINI</a>   | 502C 31C4h                  | 502C 41C4h                  |
| 1C8h   | 32     | <a href="#">ADC_CFG_ADCPPB3TRIPLO2</a> | 502C 31C8h                  | 502C 41C8h                  |
| 1DCh   | 16     | <a href="#">ADC_CFG_ADCPPB4LIMIT</a>   | 502C 31DCh                  | 502C 41DCh                  |
| 1E0h   | 16     | <a href="#">ADC_CFG_ADCPPB4PCOUNT</a>  | 502C 31E0h                  | 502C 41E0h                  |
| 1E4h   | 16     | <a href="#">ADC_CFG_ADCPPB4CONFIG2</a> | 502C 31E4h                  | 502C 41E4h                  |
| 1E8h   | 32     | <a href="#">ADC_CFG_ADCPPB4PSUM</a>    | 502C 31E8h                  | 502C 41E8h                  |
| 1ECh   | 32     | <a href="#">ADC_CFG_ADCPPB4PMAX</a>    | 502C 31ECh                  | 502C 41ECh                  |
| 1F0h   | 16     | <a href="#">ADC_CFG_ADCPPB4PMAXI</a>   | 502C 31F0h                  | 502C 41F0h                  |
| 1F4h   | 32     | <a href="#">ADC_CFG_ADCPPB4PMIN</a>    | 502C 31F4h                  | 502C 41F4h                  |

**Table 3-4. ADC\_CFG Registers, Base Address=502C 0000h, Length=256 (continued)**

| Offset | Length | Register Name                          | ADC3_G0_G5 Physical Address | ADC4_G0_G5 Physical Address |
|--------|--------|----------------------------------------|-----------------------------|-----------------------------|
| 1F8h   | 16     | <a href="#">ADC_CFG_ADCPPB4PMINI</a>   | 502C 31F8h                  | 502C 41F8h                  |
| 1FCh   | 32     | <a href="#">ADC_CFG_ADCPPB4TRIPLO2</a> | 502C 31FCh                  | 502C 41FCh                  |

### 3.2.2 ADC Registers

#### ADC Registers

### 3.2.2.1 ADC\_RESULTS\_ADCRESULT0 Register

#### 1 ADC\_RESULTS\_ADCRESULT0 Register (Offset = 0h) [reset = 0h]

ADC Result 0 Register.

Return to [Summary Table](#)

**Table 3-5. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0000h       |
| ADC1_G0_G5    | 5010 1000h       |
| ADC2_G0_G5    | 5010 2000h       |
| ADC3_G0_G5    | 5010 3000h       |
| ADC4_G0_G5    | 5010 4000h       |

**Figure 3-1. ADC\_RESULTS\_ADCRESULT0 Name Register**

|        |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |
| 7      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |

**Table 3-7. ADC\_RESULTS\_ADCRESULT0 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                      |
|------|--------|------|-------|----------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | RESULT | R    | 0h    | ADC Result 0<br>12-bit ADC result. After the ADC completes a conversion of SOC0, the digital result is placed in this bit field. |



### 3.2.2.2 ADC\_RESULTS\_ADCRESULT1 Register

#### 1 ADC\_RESULTS\_ADCRESULT1 Register (Offset = 2h) [reset = 0h]

ADC Result 1 Register.

Return to [Summary Table](#)

**Table 3-8. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0002h       |
| ADC1_G0_G5    | 5010 1002h       |
| ADC2_G0_G5    | 5010 2002h       |
| ADC3_G0_G5    | 5010 3002h       |
| ADC4_G0_G5    | 5010 4002h       |

**Figure 3-2. ADC\_RESULTS\_ADCRESULT1 Name Register**

|        |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |
| 7      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |

**Table 3-10. ADC\_RESULTS\_ADCRESULT1 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                      |
|------|--------|------|-------|----------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | RESULT | R    | 0h    | ADC Result 1<br>12-bit ADC result. After the ADC completes a conversion of SOC1, the digital result is placed in this bit field. |

### 3.2.2.3 ADC\_RESULTS\_ADCRESULT2 Register

#### 1 ADC\_RESULTS\_ADCRESULT2 Register (Offset = 4h) [reset = 0h]

ADC Result 2 Register.

Return to [Summary Table](#)

**Table 3-11. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0004h       |
| ADC1_G0_G5    | 5010 1004h       |
| ADC2_G0_G5    | 5010 2004h       |
| ADC3_G0_G5    | 5010 3004h       |
| ADC4_G0_G5    | 5010 4004h       |

**Figure 3-3. ADC\_RESULTS\_ADCRESULT2 Name Register**

|        |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |
| 7      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |

**Table 3-13. ADC\_RESULTS\_ADCRESULT2 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                      |
|------|--------|------|-------|----------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | RESULT | R    | 0h    | ADC Result 2<br>12-bit ADC result. After the ADC completes a conversion of SOC2, the digital result is placed in this bit field. |

### 3.2.2.4 ADC\_RESULTS\_ADCRESULT3 Register

#### 1 ADC\_RESULTS\_ADCRESULT3 Register (Offset = 6h) [reset = 0h]

ADC Result 3 Register.

Return to [Summary Table](#)

**Table 3-14. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0006h       |
| ADC1_G0_G5    | 5010 1006h       |
| ADC2_G0_G5    | 5010 2006h       |
| ADC3_G0_G5    | 5010 3006h       |
| ADC4_G0_G5    | 5010 4006h       |

**Figure 3-4. ADC\_RESULTS\_ADCRESULT3 Name Register**

|        |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |
| 7      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |

**Table 3-16. ADC\_RESULTS\_ADCRESULT3 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                      |
|------|--------|------|-------|----------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | RESULT | R    | 0h    | ADC Result 3<br>12-bit ADC result. After the ADC completes a conversion of SOC3, the digital result is placed in this bit field. |

### 3.2.2.5 ADC\_RESULTS\_ADCRESULT4 Register

#### 1 ADC\_RESULTS\_ADCRESULT4 Register (Offset = 8h) [reset = 0h]

ADC Result 4 Register.

Return to [Summary Table](#)

**Table 3-17. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0008h       |
| ADC1_G0_G5    | 5010 1008h       |
| ADC2_G0_G5    | 5010 2008h       |
| ADC3_G0_G5    | 5010 3008h       |
| ADC4_G0_G5    | 5010 4008h       |

**Figure 3-5. ADC\_RESULTS\_ADCRESULT4 Name Register**

|        |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |
| 7      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |

**Table 3-19. ADC\_RESULTS\_ADCRESULT4 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                      |
|------|--------|------|-------|----------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | RESULT | R    | 0h    | ADC Result 4<br>12-bit ADC result. After the ADC completes a conversion of SOC4, the digital result is placed in this bit field. |

### 3.2.2.6 ADC\_RESULTS\_ADCRESULT5 Register

#### 1 ADC\_RESULTS\_ADCRESULT5 Register (Offset = Ah) [reset = 0h]

ADC Result 5 Register.

Return to [Summary Table](#)

**Table 3-20. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 000Ah       |
| ADC1_G0_G5    | 5010 100Ah       |
| ADC2_G0_G5    | 5010 200Ah       |
| ADC3_G0_G5    | 5010 300Ah       |
| ADC4_G0_G5    | 5010 400Ah       |

**Figure 3-6. ADC\_RESULTS\_ADCRESULT5 Name Register**

|        |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |
| 7      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |

**Table 3-22. ADC\_RESULTS\_ADCRESULT5 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                      |
|------|--------|------|-------|----------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | RESULT | R    | 0h    | ADC Result 5<br>12-bit ADC result. After the ADC completes a conversion of SOC5, the digital result is placed in this bit field. |

### 3.2.2.7 ADC\_RESULTS\_ADCRESULT6 Register

#### 1 ADC\_RESULTS\_ADCRESULT6 Register (Offset = Ch) [reset = 0h]

ADC Result 6 Register.

Return to [Summary Table](#)

**Table 3-23. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 000Ch       |
| ADC1_G0_G5    | 5010 100Ch       |
| ADC2_G0_G5    | 5010 200Ch       |
| ADC3_G0_G5    | 5010 300Ch       |
| ADC4_G0_G5    | 5010 400Ch       |

**Figure 3-7. ADC\_RESULTS\_ADCRESULT6 Name Register**

|        |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |
| 7      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |

**Table 3-25. ADC\_RESULTS\_ADCRESULT6 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                      |
|------|--------|------|-------|----------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | RESULT | R    | 0h    | ADC Result 6<br>12-bit ADC result. After the ADC completes a conversion of SOC6, the digital result is placed in this bit field. |

### 3.2.2.8 ADC\_RESULTS\_ADCRESULT7 Register

#### 1 ADC\_RESULTS\_ADCRESULT7 Register (Offset = Eh) [reset = 0h]

ADC Result 7 Register.

Return to [Summary Table](#)

**Table 3-26. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 000Eh       |
| ADC1_G0_G5    | 5010 100Eh       |
| ADC2_G0_G5    | 5010 200Eh       |
| ADC3_G0_G5    | 5010 300Eh       |
| ADC4_G0_G5    | 5010 400Eh       |

**Figure 3-8. ADC\_RESULTS\_ADCRESULT7 Name Register**

|        |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |
| 7      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |

**Table 3-28. ADC\_RESULTS\_ADCRESULT7 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                      |
|------|--------|------|-------|----------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | RESULT | R    | 0h    | ADC Result 7<br>12-bit ADC result. After the ADC completes a conversion of SOC7, the digital result is placed in this bit field. |

### 3.2.2.9 ADC\_RESULTS\_ADCRESULT8 Register

#### 1 ADC\_RESULTS\_ADCRESULT8 Register (Offset = 10h) [reset = 0h]

ADC Result 8 Register.

Return to [Summary Table](#)

**Table 3-29. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0010h       |
| ADC1_G0_G5    | 5010 1010h       |
| ADC2_G0_G5    | 5010 2010h       |
| ADC3_G0_G5    | 5010 3010h       |
| ADC4_G0_G5    | 5010 4010h       |

**Figure 3-9. ADC\_RESULTS\_ADCRESULT8 Name Register**

|        |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |
| 7      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |

**Table 3-31. ADC\_RESULTS\_ADCRESULT8 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                      |
|------|--------|------|-------|----------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | RESULT | R    | 0h    | ADC Result 8<br>12-bit ADC result. After the ADC completes a conversion of SOC8, the digital result is placed in this bit field. |



### 3.2.2.10 ADC\_RESULTS\_ADCRESULT9 Register

#### 1 ADC\_RESULTS\_ADCRESULT9 Register (Offset = 12h) [reset = 0h]

ADC Result 9 Register.

Return to [Summary Table](#)

**Table 3-32. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0012h       |
| ADC1_G0_G5    | 5010 1012h       |
| ADC2_G0_G5    | 5010 2012h       |
| ADC3_G0_G5    | 5010 3012h       |
| ADC4_G0_G5    | 5010 4012h       |

**Figure 3-10. ADC\_RESULTS\_ADCRESULT9 Name Register**

|        |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |
| 7      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |

**Table 3-34. ADC\_RESULTS\_ADCRESULT9 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                      |
|------|--------|------|-------|----------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | RESULT | R    | 0h    | ADC Result 9<br>12-bit ADC result. After the ADC completes a conversion of SOC9, the digital result is placed in this bit field. |

### 3.2.2.11 ADC\_RESULTS\_ADCRESULT10 Register

#### 1 ADC\_RESULTS\_ADCRESULT10 Register (Offset = 14h) [reset = 0h]

ADC Result 10 Register.

Return to [Summary Table](#)

**Table 3-35. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0014h       |
| ADC1_G0_G5    | 5010 1014h       |
| ADC2_G0_G5    | 5010 2014h       |
| ADC3_G0_G5    | 5010 3014h       |
| ADC4_G0_G5    | 5010 4014h       |

**Figure 3-11. ADC\_RESULTS\_ADCRESULT10 Name Register**

|        |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |
| 7      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |

**Table 3-37. ADC\_RESULTS\_ADCRESULT10 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                        |
|------|--------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | RESULT | R    | 0h    | ADC Result 10<br>12-bit ADC result. After the ADC completes a conversion of SOC10, the digital result is placed in this bit field. |

### 3.2.2.12 ADC\_RESULTS\_ADCRESULT11 Register

#### 1 ADC\_RESULTS\_ADCRESULT11 Register (Offset = 16h) [reset = 0h]

ADC Result 11 Register.

Return to [Summary Table](#)

**Table 3-38. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0016h       |
| ADC1_G0_G5    | 5010 1016h       |
| ADC2_G0_G5    | 5010 2016h       |
| ADC3_G0_G5    | 5010 3016h       |
| ADC4_G0_G5    | 5010 4016h       |

**Figure 3-12. ADC\_RESULTS\_ADCRESULT11 Name Register**

|        |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |
| 7      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |

**Table 3-40. ADC\_RESULTS\_ADCRESULT11 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                        |
|------|--------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | RESULT | R    | 0h    | ADC Result 11<br>12-bit ADC result. After the ADC completes a conversion of SOC11, the digital result is placed in this bit field. |

### 3.2.2.13 ADC\_RESULTS\_ADCRESULT12 Register

#### 1 ADC\_RESULTS\_ADCRESULT12 Register (Offset = 18h) [reset = 0h]

ADC Result 12 Register.

Return to [Summary Table](#)

**Table 3-41. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0018h       |
| ADC1_G0_G5    | 5010 1018h       |
| ADC2_G0_G5    | 5010 2018h       |
| ADC3_G0_G5    | 5010 3018h       |
| ADC4_G0_G5    | 5010 4018h       |

**Figure 3-13. ADC\_RESULTS\_ADCRESULT12 Name Register**

|        |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |
| 7      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |

**Table 3-43. ADC\_RESULTS\_ADCRESULT12 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                        |
|------|--------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | RESULT | R    | 0h    | ADC Result 12<br>12-bit ADC result. After the ADC completes a conversion of SOC12, the digital result is placed in this bit field. |

### 3.2.2.14 ADC\_RESULTS\_ADCRESULT13 Register

#### 1 ADC\_RESULTS\_ADCRESULT13 Register (Offset = 1Ah) [reset = 0h]

ADC Result 13 Register.

Return to [Summary Table](#)

**Table 3-44. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 001Ah       |
| ADC1_G0_G5    | 5010 101Ah       |
| ADC2_G0_G5    | 5010 201Ah       |
| ADC3_G0_G5    | 5010 301Ah       |
| ADC4_G0_G5    | 5010 401Ah       |

**Figure 3-14. ADC\_RESULTS\_ADCRESULT13 Name Register**

|        |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |
| 7      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |

**Table 3-46. ADC\_RESULTS\_ADCRESULT13 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                        |
|------|--------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | RESULT | R    | 0h    | ADC Result 13<br>12-bit ADC result. After the ADC completes a conversion of SOC13, the digital result is placed in this bit field. |

### 3.2.2.15 ADC\_RESULTS\_ADCRESULT14 Register

#### 1 ADC\_RESULTS\_ADCRESULT14 Register (Offset = 1Ch) [reset = 0h]

ADC Result 14 Register.

Return to [Summary Table](#)

**Table 3-47. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 001Ch       |
| ADC1_G0_G5    | 5010 101Ch       |
| ADC2_G0_G5    | 5010 201Ch       |
| ADC3_G0_G5    | 5010 301Ch       |
| ADC4_G0_G5    | 5010 401Ch       |

**Figure 3-15. ADC\_RESULTS\_ADCRESULT14 Name Register**

|        |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |
| 7      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |

**Table 3-49. ADC\_RESULTS\_ADCRESULT14 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                        |
|------|--------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | RESULT | R    | 0h    | ADC Result 14<br>12-bit ADC result. After the ADC completes a conversion of SOC14, the digital result is placed in this bit field. |

### 3.2.2.16 ADC\_RESULTS\_ADCRESULT15 Register

#### 1 ADC\_RESULTS\_ADCRESULT15 Register (Offset = 1Eh) [reset = 0h]

ADC Result 15 Register.

Return to [Summary Table](#)

**Table 3-50. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 001Eh       |
| ADC1_G0_G5    | 5010 101Eh       |
| ADC2_G0_G5    | 5010 201Eh       |
| ADC3_G0_G5    | 5010 301Eh       |
| ADC4_G0_G5    | 5010 401Eh       |

**Figure 3-16. ADC\_RESULTS\_ADCRESULT15 Name Register**

|        |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |
| 7      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| RESULT |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |

**Table 3-52. ADC\_RESULTS\_ADCRESULT15 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                        |
|------|--------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | RESULT | R    | 0h    | ADC Result 15<br>12-bit ADC result. After the ADC completes a conversion of SOC15, the digital result is placed in this bit field. |

### 3.2.2.17 ADC\_RESULTS\_ADCPPB1RESULT Register

#### 1 ADC\_RESULTS\_ADCPPB1RESULT Register (Offset = 20h) [reset = 0h]

ADC Post Processing Block 1 Result Register.

Return to [Summary Table](#)

**Table 3-53. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0020h       |
| ADC1_G0_G5    | 5010 1020h       |
| ADC2_G0_G5    | 5010 2020h       |
| ADC3_G0_G5    | 5010 3020h       |
| ADC4_G0_G5    | 5010 4020h       |

**Figure 3-17. ADC\_RESULTS\_ADCPPB1RESULT Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SIGN      |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SIGN      |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PPBRESULT |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PPBRESULT |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 3-55. ADC\_RESULTS\_ADCPPB1RESULT Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                   |
|-------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 16.<br>NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12. |



**Table 3-55. ADC\_RESULTS\_ADCPPB1RESULT Register Field Descriptions (continued)**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------|-----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | PPBRESULT | R    | 0h    | <p>ADC Post Processing Block Result 1</p> <p>The result of the offset/reference subtraction post conversion processing is stored in this register.</p> <p>This result is available 1 SYSCLK cycle after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be available 1 SYSCLK cycle after the associated ADCRESULT and subsequent results [in order from lowest numbered PPB to highest] will each become available every 2-3 SYSCLK cycles [refer to the TRM for more detailed timing information].</p> <p>If ADCINTFLG is polled to determine when to read the PPBRESULT, it may be necessary to add one or more NOP instructions to ensure that the updated post conversion processing result has posted to the register.</p> <p>NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.</p> |

### 3.2.2.18 ADC\_RESULTS\_ADCPPB2RESULT Register

#### 1 ADC\_RESULTS\_ADCPPB2RESULT Register (Offset = 24h) [reset = 0h]

ADC Post Processing Block 2 Result Register.

Return to [Summary Table](#)

**Table 3-56. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0024h       |
| ADC1_G0_G5    | 5010 1024h       |
| ADC2_G0_G5    | 5010 2024h       |
| ADC3_G0_G5    | 5010 3024h       |
| ADC4_G0_G5    | 5010 4024h       |

**Figure 3-18. ADC\_RESULTS\_ADCPPB2RESULT Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SIGN      |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SIGN      |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PPBRESULT |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PPBRESULT |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 3-58. ADC\_RESULTS\_ADCPPB2RESULT Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                   |
|-------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 16.<br>NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12. |

**Table 3-58. ADC\_RESULTS\_ADCPPB2RESULT Register Field Descriptions (continued)**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------|-----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | PPBRESULT | R    | 0h    | <p>ADC Post Processing Block Result 2</p> <p>The result of the offset/reference subtraction post conversion processing is stored in this register.</p> <p>This result is available 1 SYSCLK cycle after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be available 1 SYSCLK cycle after the associated ADCRESULT and subsequent results [in order from lowest numbered PPB to highest] will each become available every 2-3 SYSCLK cycles [refer to the TRM for more detailed timing information].</p> <p>If ADCINTFLG is polled to determine when to read the PPBRESULT, it may be necessary to add one or more NOP instructions to ensure that the updated post conversion processing result has posted to the register.</p> <p>NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.</p> |

### 3.2.2.19 ADC\_RESULTS\_ADCPPB3RESULT Register

#### 1 ADC\_RESULTS\_ADCPPB3RESULT Register (Offset = 28h) [reset = 0h]

ADC Post Processing Block 3 Result Register.

Return to [Summary Table](#)

**Table 3-59. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0028h       |
| ADC1_G0_G5    | 5010 1028h       |
| ADC2_G0_G5    | 5010 2028h       |
| ADC3_G0_G5    | 5010 3028h       |
| ADC4_G0_G5    | 5010 4028h       |

**Figure 3-19. ADC\_RESULTS\_ADCPPB3RESULT Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SIGN      |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SIGN      |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PPBRESULT |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PPBRESULT |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 3-61. ADC\_RESULTS\_ADCPPB3RESULT Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                   |
|-------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 16.<br>NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12. |

**Table 3-61. ADC\_RESULTS\_ADCPPB3RESULT Register Field Descriptions (continued)**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------|-----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | PPBRESULT | R    | 0h    | <p>ADC Post Processing Block Result 3</p> <p>The result of the offset/reference subtraction post conversion processing is stored in this register.</p> <p>This result is available 1 SYSCLK cycle after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be available 1 SYSCLK cycle after the associated ADCRESULT and subsequent results [in order from lowest numbered PPB to highest] will each become available every 2-3 SYSCLK cycles [refer to the TRM for more detailed timing information].</p> <p>If ADCINTFLG is polled to determine when to read the PPBRESULT, it may be necessary to add one or more NOP instructions to ensure that the updated post conversion processing result has posted to the register.</p> <p>NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.</p> |

### 3.2.2.20 ADC\_RESULTS\_ADCPPB4RESULT Register

#### 1 ADC\_RESULTS\_ADCPPB4RESULT Register (Offset = 2Ch) [reset = 0h]

ADC Post Processing Block 4 Result Register.

Return to [Summary Table](#)

**Table 3-62. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 002Ch       |
| ADC1_G0_G5    | 5010 102Ch       |
| ADC2_G0_G5    | 5010 202Ch       |
| ADC3_G0_G5    | 5010 302Ch       |
| ADC4_G0_G5    | 5010 402Ch       |

**Figure 3-20. ADC\_RESULTS\_ADCPPB4RESULT Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SIGN      |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SIGN      |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PPBRESULT |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PPBRESULT |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 3-64. ADC\_RESULTS\_ADCPPB4RESULT Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                   |
|-------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 16.<br>NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the SIGN bits extend down to bit 12, and all reflect the same value as bit 12. |

**Table 3-64. ADC\_RESULTS\_ADCPPB4RESULT Register Field Descriptions (continued)**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------|-----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | PPBRESULT | R    | 0h    | <p>ADC Post Processing Block Result 4</p> <p>The result of the offset/reference subtraction post conversion processing is stored in this register.</p> <p>This result is available 1 SYSCLK cycle after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be available 1 SYSCLK cycle after the associated ADCRESULT and subsequent results [in order from lowest numbered PPB to highest] will each become available every 2-3 SYSCLK cycles [refer to the TRM for more detailed timing information].</p> <p>If ADCINTFLG is polled to determine when to read the PPBRESULT, it may be necessary to add one or more NOP instructions to ensure that the updated post conversion processing result has posted to the register.</p> <p>NOTE: If the conversion associated with this Post Processing Block is a 12-bit conversion, the PPBRESULT bits are limited to bits 12:0.</p> |

### 3.2.2.21 ADC\_RESULTS\_ADCPPB1SUM Register

#### 1 ADC\_RESULTS\_ADCPPB1SUM Register (Offset = 30h) [reset = 0h]

ADC PPB 1 Final Sum Result Register.

Return to [Summary Table](#)

**Table 3-65. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0030h       |
| ADC1_G0_G5    | 5010 1030h       |
| ADC2_G0_G5    | 5010 2030h       |
| ADC3_G0_G5    | 5010 3030h       |
| ADC4_G0_G5    | 5010 4030h       |

**Figure 3-21. ADC\_RESULTS\_ADCPPB1SUM Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SIGN |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SUM  |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SUM  |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SUM  |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 3-67. ADC\_RESULTS\_ADCPPB1SUM Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 23.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 23:0  | SUM   | R    | 0h    | Post Processing Block 1 Oversampling Final Sum. When either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event, the value of PSUM is loaded into this register. In the case of a count-match event, the sum loaded into this register includes the value from the most recent conversion.<br>The value from PSUM will be right shifted by the amount specified in the SHIFT register before being loaded into the final SUM result register.<br>This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information]. |



### 3.2.2.22 ADC\_RESULTS\_ADCPPB1COUNT Register

#### 1 ADC\_RESULTS\_ADCPPB1COUNT Register (Offset = 34h) [reset = 0h]

ADC PPB1 Final Conversion Count Register.

Return to [Summary Table](#)

**Table 3-68. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0034h       |
| ADC1_G0_G5    | 5010 1034h       |
| ADC2_G0_G5    | 5010 2034h       |
| ADC3_G0_G5    | 5010 3034h       |
| ADC4_G0_G5    | 5010 4034h       |

**Figure 3-22. ADC\_RESULTS\_ADCPPB1COUNT Name Register**

|            |    |    |    |    |    |       |   |
|------------|----|----|----|----|----|-------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9     | 8 |
| RESERVED_1 |    |    |    |    |    | COUNT |   |
| R          |    |    |    |    |    | R     |   |
| 0h         |    |    |    |    |    | 0h    |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1     | 0 |
| COUNT      |    |    |    |    |    |       |   |
| R          |    |    |    |    |    |       |   |
| 0h         |    |    |    |    |    |       |   |

**Table 3-70. ADC\_RESULTS\_ADCPPB1COUNT Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 9:0   | COUNT      | R    | 0h    | Post Processing Block 1 Oversampling Final Count. When either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event, the value of PCOUNT is loaded into this register. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information]. |

### 3.2.2.23 ADC\_RESULTS\_ADCPPB2SUM Register

#### 1 ADC\_RESULTS\_ADCPPB2SUM Register (Offset = 38h) [reset = 0h]

ADC PPB 2 Final Sum Result Register.

Return to [Summary Table](#)

**Table 3-71. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0038h       |
| ADC1_G0_G5    | 5010 1038h       |
| ADC2_G0_G5    | 5010 2038h       |
| ADC3_G0_G5    | 5010 3038h       |
| ADC4_G0_G5    | 5010 4038h       |

**Figure 3-23. ADC\_RESULTS\_ADCPPB2SUM Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SIGN |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SUM  |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SUM  |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SUM  |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 3-73. ADC\_RESULTS\_ADCPPB2SUM Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 23.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 23:0  | SUM   | R    | 0h    | Post Processing Block 2 Oversampling Final Sum. When either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event, the value of PSUM is loaded into this register. In the case of a count-match event, the sum loaded into this register includes the value from the most recent conversion.<br>The value from PSUM will be right shifted by the amount specified in the SHIFT register before being loaded into the final SUM result register.<br>This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information]. |

### 3.2.2.24 ADC\_RESULTS\_ADCPPB2COUNT Register

#### 1 ADC\_RESULTS\_ADCPPB2COUNT Register (Offset = 3Ch) [reset = 0h]

ADC PPB2 Final Conversion Count Register.

Return to [Summary Table](#)

**Table 3-74. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 003Ch       |
| ADC1_G0_G5    | 5010 103Ch       |
| ADC2_G0_G5    | 5010 203Ch       |
| ADC3_G0_G5    | 5010 303Ch       |
| ADC4_G0_G5    | 5010 403Ch       |

**Figure 3-24. ADC\_RESULTS\_ADCPPB2COUNT Name Register**

|            |    |    |    |    |    |       |   |
|------------|----|----|----|----|----|-------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9     | 8 |
| RESERVED_1 |    |    |    |    |    | COUNT |   |
| R          |    |    |    |    |    | R     |   |
| 0h         |    |    |    |    |    | 0h    |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1     | 0 |
| COUNT      |    |    |    |    |    |       |   |
| R          |    |    |    |    |    |       |   |
| 0h         |    |    |    |    |    |       |   |

**Table 3-76. ADC\_RESULTS\_ADCPPB2COUNT Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 9:0   | COUNT      | R    | 0h    | Post Processing Block 2 Oversampling Final Count. When either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event, the value of PCOUNT is loaded into this register. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information]. |

### 3.2.2.25 ADC\_RESULTS\_ADCPPB3SUM Register

#### 1 ADC\_RESULTS\_ADCPPB3SUM Register (Offset = 40h) [reset = 0h]

ADC PPB 3 Final Sum Result Register.

Return to [Summary Table](#)

**Table 3-77. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0040h       |
| ADC1_G0_G5    | 5010 1040h       |
| ADC2_G0_G5    | 5010 2040h       |
| ADC3_G0_G5    | 5010 3040h       |
| ADC4_G0_G5    | 5010 4040h       |

**Figure 3-25. ADC\_RESULTS\_ADCPPB3SUM Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SIGN |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SUM  |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SUM  |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SUM  |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 3-79. ADC\_RESULTS\_ADCPPB3SUM Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 23.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 23:0  | SUM   | R    | 0h    | <p>Post Processing Block 3 Oversampling Final Sum. When either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event, the value of PSUM is loaded into this register. In the case of a count-match event, the sum loaded into this register includes the value from the most recent conversion.</p> <p>The value from PSUM will be right shifted by the amount specified in the SHIFT register before being loaded into the final SUM result register.</p> <p>This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information].</p> |

### 3.2.2.26 ADC\_RESULTS\_ADCPPB3COUNT Register

#### 1 ADC\_RESULTS\_ADCPPB3COUNT Register (Offset = 44h) [reset = 0h]

ADC PPB3 Final Conversion Count Register.

Return to [Summary Table](#)

**Table 3-80. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0044h       |
| ADC1_G0_G5    | 5010 1044h       |
| ADC2_G0_G5    | 5010 2044h       |
| ADC3_G0_G5    | 5010 3044h       |
| ADC4_G0_G5    | 5010 4044h       |

**Figure 3-26. ADC\_RESULTS\_ADCPPB3COUNT Name Register**

|            |    |    |    |    |    |       |   |
|------------|----|----|----|----|----|-------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9     | 8 |
| RESERVED_1 |    |    |    |    |    | COUNT |   |
| R          |    |    |    |    |    | R     |   |
| 0h         |    |    |    |    |    | 0h    |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1     | 0 |
| COUNT      |    |    |    |    |    |       |   |
| R          |    |    |    |    |    |       |   |
| 0h         |    |    |    |    |    |       |   |

**Table 3-82. ADC\_RESULTS\_ADCPPB3COUNT Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 9:0   | COUNT      | R    | 0h    | Post Processing Block 3 Oversampling Final Count. When either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event, the value of PCOUNT is loaded into this register. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information]. |

### 3.2.2.27 ADC\_RESULTS\_ADCPPB4SUM Register

#### 1 ADC\_RESULTS\_ADCPPB4SUM Register (Offset = 48h) [reset = 0h]

ADC PPB 4 Final Sum Result Register.

Return to [Summary Table](#)

**Table 3-83. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0048h       |
| ADC1_G0_G5    | 5010 1048h       |
| ADC2_G0_G5    | 5010 2048h       |
| ADC3_G0_G5    | 5010 3048h       |
| ADC4_G0_G5    | 5010 4048h       |

**Figure 3-27. ADC\_RESULTS\_ADCPPB4SUM Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SIGN |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SUM  |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SUM  |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SUM  |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 3-85. ADC\_RESULTS\_ADCPPB4SUM Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 23.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 23:0  | SUM   | R    | 0h    | Post Processing Block 4 Oversampling Final Sum. When either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event, the value of PSUM is loaded into this register. In the case of a count-match event, the sum loaded into this register includes the value from the most recent conversion.<br>The value from PSUM will be right shifted by the amount specified in the SHIFT register before being loaded into the final SUM result register.<br>This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information]. |

### 3.2.2.28 ADC\_RESULTS\_ADCPPB4COUNT Register

#### 1 ADC\_RESULTS\_ADCPPB4COUNT Register (Offset = 4Ch) [reset = 0h]

ADC PPB4 Final Conversion Count Register.

Return to [Summary Table](#)

**Table 3-86. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 004Ch       |
| ADC1_G0_G5    | 5010 104Ch       |
| ADC2_G0_G5    | 5010 204Ch       |
| ADC3_G0_G5    | 5010 304Ch       |
| ADC4_G0_G5    | 5010 404Ch       |

**Figure 3-28. ADC\_RESULTS\_ADCPPB4COUNT Name Register**

|            |    |    |    |    |    |       |   |
|------------|----|----|----|----|----|-------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9     | 8 |
| RESERVED_1 |    |    |    |    |    | COUNT |   |
| R          |    |    |    |    |    | R     |   |
| 0h         |    |    |    |    |    | 0h    |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1     | 0 |
| COUNT      |    |    |    |    |    |       |   |
| R          |    |    |    |    |    |       |   |
| 0h         |    |    |    |    |    |       |   |

**Table 3-88. ADC\_RESULTS\_ADCPPB4COUNT Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 9:0   | COUNT      | R    | 0h    | Post Processing Block 4 Oversampling Final Count. When either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event, the value of PCOUNT is loaded into this register. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information]. |

### 3.2.2.29 ADC\_RESULTS\_ADCPPB1MAX Register

#### 1 ADC\_RESULTS\_ADCPPB1MAX Register (Offset = 50h) [reset = 0h]

ADC PPB 1 Final Max Result Register.

Return to [Summary Table](#)

**Table 3-89. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0050h       |
| ADC1_G0_G5    | 5010 1050h       |
| ADC2_G0_G5    | 5010 2050h       |
| ADC3_G0_G5    | 5010 3050h       |
| ADC4_G0_G5    | 5010 4050h       |

**Figure 3-29. ADC\_RESULTS\_ADCPPB1MAX Name Register**

|      |    |    |    |    |    |    |     |
|------|----|----|----|----|----|----|-----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24  |
| SIGN |    |    |    |    |    |    |     |
| R    |    |    |    |    |    |    |     |
| 0h   |    |    |    |    |    |    |     |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16  |
| SIGN |    |    |    |    |    |    | MAX |
| R    |    |    |    |    |    |    | R   |
| 0h   |    |    |    |    |    |    | 0h  |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8   |
| MAX  |    |    |    |    |    |    |     |
| R    |    |    |    |    |    |    |     |
| 0h   |    |    |    |    |    |    |     |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0   |
| MAX  |    |    |    |    |    |    |     |
| R    |    |    |    |    |    |    |     |
| 0h   |    |    |    |    |    |    |     |

**Table 3-91. ADC\_RESULTS\_ADCPPB1MAX Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 16.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 16:0  | MAX   | R    | 0h    | Post Processing Block 1 Oversampling Final Max. When either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event, the value of PMAX is loaded into this register. In the case of a count-match event, the max loaded into this register includes the value from the most recent conversion.<br>This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available [only when a count-match event occurs]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information]. |



### 3.2.2.30 ADC\_RESULTS\_ADCPPB1MAXI Register

#### 1 ADC\_RESULTS\_ADCPPB1MAXI Register (Offset = 54h) [reset = 0h]

ADC PPB 1 Final Max Index Result Register.

Return to [Summary Table](#)

**Table 3-92. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0054h       |
| ADC1_G0_G5    | 5010 1054h       |
| ADC2_G0_G5    | 5010 2054h       |
| ADC3_G0_G5    | 5010 3054h       |
| ADC4_G0_G5    | 5010 4054h       |

**Figure 3-30. ADC\_RESULTS\_ADCPPB1MAXI Name Register**

|            |    |    |    |    |    |      |   |
|------------|----|----|----|----|----|------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9    | 8 |
| RESERVED_1 |    |    |    |    |    | MAXI |   |
| R          |    |    |    |    |    | R    |   |
| 0h         |    |    |    |    |    | 0h   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1    | 0 |
| MAXI       |    |    |    |    |    |      |   |
| R          |    |    |    |    |    |      |   |
| 0h         |    |    |    |    |    |      |   |

**Table 3-94. ADC\_RESULTS\_ADCPPB1MAXI Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 9:0   | MAXI       | R    | 0h    | Post Processing Block 1 Oversampling Final Index of the Max. When either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event, the value of PMAXI is loaded into this register. In the case of a count-match event, the max index loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information]. |

### 3.2.2.31 ADC\_RESULTS\_ADCPPB1MIN Register

#### 1 ADC\_RESULTS\_ADCPPB1MIN Register (Offset = 58h) [reset = 0h]

ADC PPB 1 Final Min Result Register.

Return to [Summary Table](#)

**Table 3-95. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0058h       |
| ADC1_G0_G5    | 5010 1058h       |
| ADC2_G0_G5    | 5010 2058h       |
| ADC3_G0_G5    | 5010 3058h       |
| ADC4_G0_G5    | 5010 4058h       |

**Figure 3-31. ADC\_RESULTS\_ADCPPB1MIN Name Register**

|      |    |    |    |    |    |    |     |
|------|----|----|----|----|----|----|-----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24  |
| SIGN |    |    |    |    |    |    |     |
| R    |    |    |    |    |    |    |     |
| 0h   |    |    |    |    |    |    |     |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16  |
| SIGN |    |    |    |    |    |    | MIN |
| R    |    |    |    |    |    |    | R   |
| 0h   |    |    |    |    |    |    | 0h  |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8   |
| MIN  |    |    |    |    |    |    |     |
| R    |    |    |    |    |    |    |     |
| 0h   |    |    |    |    |    |    |     |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0   |
| MIN  |    |    |    |    |    |    |     |
| R    |    |    |    |    |    |    |     |
| 0h   |    |    |    |    |    |    |     |

**Table 3-97. ADC\_RESULTS\_ADCPPB1MIN Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 16.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 16:0  | MIN   | R    | 0h    | Post Processing Block 1 Oversampling Final Min. When either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event, the value of PMIN is loaded into this register. In the case of a count-match event, the max loaded into this register includes the value from the most recent conversion.<br>This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information]. |

### 3.2.2.32 ADC\_RESULTS\_ADCPPB1MINI Register

#### 1 ADC\_RESULTS\_ADCPPB1MINI Register (Offset = 5Ch) [reset = 0h]

ADC PPB 1 Final Min Index Result Register.

Return to [Summary Table](#)

**Table 3-98. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 005Ch       |
| ADC1_G0_G5    | 5010 105Ch       |
| ADC2_G0_G5    | 5010 205Ch       |
| ADC3_G0_G5    | 5010 305Ch       |
| ADC4_G0_G5    | 5010 405Ch       |

**Figure 3-32. ADC\_RESULTS\_ADCPPB1MINI Name Register**

|            |    |    |    |    |    |      |   |
|------------|----|----|----|----|----|------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9    | 8 |
| RESERVED_1 |    |    |    |    |    | MINI |   |
| R          |    |    |    |    |    | R    |   |
| 0h         |    |    |    |    |    | 0h   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1    | 0 |
| MINI       |    |    |    |    |    |      |   |
| R          |    |    |    |    |    |      |   |
| 0h         |    |    |    |    |    |      |   |

**Table 3-100. ADC\_RESULTS\_ADCPPB1MINI Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 9:0   | MINI       | R    | 0h    | Post Processing Block 1 Oversampling Final Index of the Min. When either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event, the value of PMINI is loaded into this register. In the case of a count-match event, the min index loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information]. |

### 3.2.2.33 ADC\_RESULTS\_ADCPPB2MAX Register

#### 1 ADC\_RESULTS\_ADCPPB2MAX Register (Offset = 60h) [reset = 0h]

ADC PPB 2 Final Max Result Register.

Return to [Summary Table](#)

**Table 3-101. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0060h       |
| ADC1_G0_G5    | 5010 1060h       |
| ADC2_G0_G5    | 5010 2060h       |
| ADC3_G0_G5    | 5010 3060h       |
| ADC4_G0_G5    | 5010 4060h       |

**Figure 3-33. ADC\_RESULTS\_ADCPPB2MAX Name Register**

|      |    |    |    |    |    |    |     |
|------|----|----|----|----|----|----|-----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24  |
| SIGN |    |    |    |    |    |    |     |
| R    |    |    |    |    |    |    |     |
| 0h   |    |    |    |    |    |    |     |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16  |
| SIGN |    |    |    |    |    |    | MAX |
| R    |    |    |    |    |    |    | R   |
| 0h   |    |    |    |    |    |    | 0h  |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8   |
| MAX  |    |    |    |    |    |    |     |
| R    |    |    |    |    |    |    |     |
| 0h   |    |    |    |    |    |    |     |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0   |
| MAX  |    |    |    |    |    |    |     |
| R    |    |    |    |    |    |    |     |
| 0h   |    |    |    |    |    |    |     |

**Table 3-103. ADC\_RESULTS\_ADCPPB2MAX Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 16.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 16:0  | MAX   | R    | 0h    | Post Processing Block 2 Oversampling Final Max. When either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event, the value of PMAX is loaded into this register. In the case of a count-match event, the max loaded into this register includes the value from the most recent conversion.<br>This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available [only when a count-match event occurs]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information]. |

### 3.2.2.34 ADC\_RESULTS\_ADCPPB2MAXI Register

#### 1 ADC\_RESULTS\_ADCPPB2MAXI Register (Offset = 64h) [reset = 0h]

ADC PPB 2 Final Max Index Result Register.

Return to [Summary Table](#)

**Table 3-104. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0064h       |
| ADC1_G0_G5    | 5010 1064h       |
| ADC2_G0_G5    | 5010 2064h       |
| ADC3_G0_G5    | 5010 3064h       |
| ADC4_G0_G5    | 5010 4064h       |

**Figure 3-34. ADC\_RESULTS\_ADCPPB2MAXI Name Register**

|            |    |    |    |    |    |      |   |
|------------|----|----|----|----|----|------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9    | 8 |
| RESERVED_1 |    |    |    |    |    | MAXI |   |
| R          |    |    |    |    |    | R    |   |
| 0h         |    |    |    |    |    | 0h   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1    | 0 |
| MAXI       |    |    |    |    |    |      |   |
| R          |    |    |    |    |    |      |   |
| 0h         |    |    |    |    |    |      |   |

**Table 3-106. ADC\_RESULTS\_ADCPPB2MAXI Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 9:0   | MAXI       | R    | 0h    | Post Processing Block 2 Oversampling Final Index of the Max. When either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event, the value of PMAI is loaded into this register. In the case of a count-match event, the max index loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information]. |

### 3.2.2.35 ADC\_RESULTS\_ADCPPB2MIN Register

#### 1 ADC\_RESULTS\_ADCPPB2MIN Register (Offset = 68h) [reset = 0h]

ADC PPB 2 Final Min Result Register.

Return to [Summary Table](#)

**Table 3-107. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0068h       |
| ADC1_G0_G5    | 5010 1068h       |
| ADC2_G0_G5    | 5010 2068h       |
| ADC3_G0_G5    | 5010 3068h       |
| ADC4_G0_G5    | 5010 4068h       |

**Figure 3-35. ADC\_RESULTS\_ADCPPB2MIN Name Register**

|      |    |    |    |    |    |    |     |
|------|----|----|----|----|----|----|-----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24  |
| SIGN |    |    |    |    |    |    |     |
| R    |    |    |    |    |    |    |     |
| 0h   |    |    |    |    |    |    |     |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16  |
| SIGN |    |    |    |    |    |    | MIN |
| R    |    |    |    |    |    |    | R   |
| 0h   |    |    |    |    |    |    | 0h  |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8   |
| MIN  |    |    |    |    |    |    |     |
| R    |    |    |    |    |    |    |     |
| 0h   |    |    |    |    |    |    |     |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0   |
| MIN  |    |    |    |    |    |    |     |
| R    |    |    |    |    |    |    |     |
| 0h   |    |    |    |    |    |    |     |

**Table 3-109. ADC\_RESULTS\_ADCPPB2MIN Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 16.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 16:0  | MIN   | R    | 0h    | Post Processing Block 2 Oversampling Final Min. When either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event, the value of PMIN is loaded into this register. In the case of a count-match event, the max loaded into this register includes the value from the most recent conversion.<br><br>This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information]. |

### 3.2.2.36 ADC\_RESULTS\_ADCPPB2MINI Register

#### 1 ADC\_RESULTS\_ADCPPB2MINI Register (Offset = 6Ch) [reset = 0h]

ADC PPB 2 Final Min Index Result Register.

Return to [Summary Table](#)

**Table 3-110. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 006Ch       |
| ADC1_G0_G5    | 5010 106Ch       |
| ADC2_G0_G5    | 5010 206Ch       |
| ADC3_G0_G5    | 5010 306Ch       |
| ADC4_G0_G5    | 5010 406Ch       |

**Figure 3-36. ADC\_RESULTS\_ADCPPB2MINI Name Register**

|            |    |    |    |    |    |      |   |
|------------|----|----|----|----|----|------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9    | 8 |
| RESERVED_1 |    |    |    |    |    | MINI |   |
| R          |    |    |    |    |    | R    |   |
| 0h         |    |    |    |    |    | 0h   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1    | 0 |
| MINI       |    |    |    |    |    |      |   |
| R          |    |    |    |    |    |      |   |
| 0h         |    |    |    |    |    |      |   |

**Table 3-112. ADC\_RESULTS\_ADCPPB2MINI Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 9:0   | MINI       | R    | 0h    | Post Processing Block 2 Oversampling Final Index of the Min. When either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event, the value of PMINI is loaded into this register. In the case of a count-match event, the min index loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information]. |

### 3.2.2.37 ADC\_RESULTS\_ADCPPB3MAX Register

#### 1 ADC\_RESULTS\_ADCPPB3MAX Register (Offset = 70h) [reset = 0h]

ADC PPB 3 Final Max Result Register.

Return to [Summary Table](#)

**Table 3-113. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0070h       |
| ADC1_G0_G5    | 5010 1070h       |
| ADC2_G0_G5    | 5010 2070h       |
| ADC3_G0_G5    | 5010 3070h       |
| ADC4_G0_G5    | 5010 4070h       |

**Figure 3-37. ADC\_RESULTS\_ADCPPB3MAX Name Register**

|      |    |    |    |    |    |    |     |
|------|----|----|----|----|----|----|-----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24  |
| SIGN |    |    |    |    |    |    |     |
| R    |    |    |    |    |    |    |     |
| 0h   |    |    |    |    |    |    |     |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16  |
| SIGN |    |    |    |    |    |    | MAX |
| R    |    |    |    |    |    |    | R   |
| 0h   |    |    |    |    |    |    | 0h  |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8   |
| MAX  |    |    |    |    |    |    |     |
| R    |    |    |    |    |    |    |     |
| 0h   |    |    |    |    |    |    |     |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0   |
| MAX  |    |    |    |    |    |    |     |
| R    |    |    |    |    |    |    |     |
| 0h   |    |    |    |    |    |    |     |

**Table 3-115. ADC\_RESULTS\_ADCPPB3MAX Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 16.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 16:0  | MAX   | R    | 0h    | Post Processing Block 3 Oversampling Final Max. When either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event, the value of PMAX is loaded into this register. In the case of a count-match event, the max loaded into this register includes the value from the most recent conversion.<br>This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available [only when a count-match event occurs]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information]. |



### 3.2.2.38 ADC\_RESULTS\_ADCPPB3MAXI Register

#### 1 ADC\_RESULTS\_ADCPPB3MAXI Register (Offset = 74h) [reset = 0h]

ADC PPB 3 Final Max Index Result Register.

Return to [Summary Table](#)

**Table 3-116. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0074h       |
| ADC1_G0_G5    | 5010 1074h       |
| ADC2_G0_G5    | 5010 2074h       |
| ADC3_G0_G5    | 5010 3074h       |
| ADC4_G0_G5    | 5010 4074h       |

**Figure 3-38. ADC\_RESULTS\_ADCPPB3MAXI Name Register**

|            |    |    |    |    |    |      |   |
|------------|----|----|----|----|----|------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9    | 8 |
| RESERVED_1 |    |    |    |    |    | MAXI |   |
| R          |    |    |    |    |    | R    |   |
| 0h         |    |    |    |    |    | 0h   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1    | 0 |
| MAXI       |    |    |    |    |    |      |   |
| R          |    |    |    |    |    |      |   |
| 0h         |    |    |    |    |    |      |   |

**Table 3-118. ADC\_RESULTS\_ADCPPB3MAXI Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 9:0   | MAXI       | R    | 0h    | Post Processing Block 3 Oversampling Final Index of the Max. When either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event, the value of PMAI is loaded into this register. In the case of a count-match event, the max index loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information]. |

### 3.2.2.39 ADC\_RESULTS\_ADCPPB3MIN Register

#### 1 ADC\_RESULTS\_ADCPPB3MIN Register (Offset = 78h) [reset = 0h]

ADC PPB 3 Final Min Result Register.

Return to [Summary Table](#)

**Table 3-119. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0078h       |
| ADC1_G0_G5    | 5010 1078h       |
| ADC2_G0_G5    | 5010 2078h       |
| ADC3_G0_G5    | 5010 3078h       |
| ADC4_G0_G5    | 5010 4078h       |

**Figure 3-39. ADC\_RESULTS\_ADCPPB3MIN Name Register**

|      |    |    |    |    |    |    |     |
|------|----|----|----|----|----|----|-----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24  |
| SIGN |    |    |    |    |    |    |     |
| R    |    |    |    |    |    |    |     |
| 0h   |    |    |    |    |    |    |     |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16  |
| SIGN |    |    |    |    |    |    | MIN |
| R    |    |    |    |    |    |    | R   |
| 0h   |    |    |    |    |    |    | 0h  |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8   |
| MIN  |    |    |    |    |    |    |     |
| R    |    |    |    |    |    |    |     |
| 0h   |    |    |    |    |    |    |     |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0   |
| MIN  |    |    |    |    |    |    |     |
| R    |    |    |    |    |    |    |     |
| 0h   |    |    |    |    |    |    |     |

**Table 3-121. ADC\_RESULTS\_ADCPPB3MIN Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 16.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 16:0  | MIN   | R    | 0h    | Post Processing Block 3 Oversampling Final Min. When either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event, the value of PMIN is loaded into this register. In the case of a count-match event, the max loaded into this register includes the value from the most recent conversion.<br>This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information]. |

### 3.2.2.40 ADC\_RESULTS\_ADCPPB3MINI Register

#### 1 ADC\_RESULTS\_ADCPPB3MINI Register (Offset = 7Ch) [reset = 0h]

ADC PPB 3 Final Min Index Result Register.

Return to [Summary Table](#)

**Table 3-122. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 007Ch       |
| ADC1_G0_G5    | 5010 107Ch       |
| ADC2_G0_G5    | 5010 207Ch       |
| ADC3_G0_G5    | 5010 307Ch       |
| ADC4_G0_G5    | 5010 407Ch       |

**Figure 3-40. ADC\_RESULTS\_ADCPPB3MINI Name Register**

|            |    |    |    |    |    |      |   |
|------------|----|----|----|----|----|------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9    | 8 |
| RESERVED_1 |    |    |    |    |    | MINI |   |
| R          |    |    |    |    |    | R    |   |
| 0h         |    |    |    |    |    | 0h   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1    | 0 |
| MINI       |    |    |    |    |    |      |   |
| R          |    |    |    |    |    |      |   |
| 0h         |    |    |    |    |    |      |   |

**Table 3-124. ADC\_RESULTS\_ADCPPB3MINI Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 9:0   | MINI       | R    | 0h    | Post Processing Block 3 Oversampling Final Index of the Min. When either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event, the value of PMINI is loaded into this register. In the case of a count-match event, the min index loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information]. |

### 3.2.2.41 ADC\_RESULTS\_ADCPPB4MAX Register

#### 1 ADC\_RESULTS\_ADCPPB4MAX Register (Offset = 80h) [reset = 0h]

ADC PPB 4 Final Max Result Register.

Return to [Summary Table](#)

**Table 3-125. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0080h       |
| ADC1_G0_G5    | 5010 1080h       |
| ADC2_G0_G5    | 5010 2080h       |
| ADC3_G0_G5    | 5010 3080h       |
| ADC4_G0_G5    | 5010 4080h       |

**Figure 3-41. ADC\_RESULTS\_ADCPPB4MAX Name Register**

|      |    |    |    |    |    |    |     |
|------|----|----|----|----|----|----|-----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24  |
| SIGN |    |    |    |    |    |    |     |
| R    |    |    |    |    |    |    |     |
| 0h   |    |    |    |    |    |    |     |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16  |
| SIGN |    |    |    |    |    |    | MAX |
| R    |    |    |    |    |    |    | R   |
| 0h   |    |    |    |    |    |    | 0h  |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8   |
| MAX  |    |    |    |    |    |    |     |
| R    |    |    |    |    |    |    |     |
| 0h   |    |    |    |    |    |    |     |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0   |
| MAX  |    |    |    |    |    |    |     |
| R    |    |    |    |    |    |    |     |
| 0h   |    |    |    |    |    |    |     |

**Table 3-127. ADC\_RESULTS\_ADCPPB4MAX Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 16.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 16:0  | MAX   | R    | 0h    | Post Processing Block 4 Oversampling Final Max. When either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event, the value of PMAX is loaded into this register. In the case of a count-match event, the max loaded into this register includes the value from the most recent conversion.<br>This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available [only when a count-match event occurs]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information]. |

### 3.2.2.42 ADC\_RESULTS\_ADCPPB4MAXI Register

#### 1 ADC\_RESULTS\_ADCPPB4MAXI Register (Offset = 84h) [reset = 0h]

ADC PPB 4 Final Max Index Result Register.

Return to [Summary Table](#)

**Table 3-128. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0084h       |
| ADC1_G0_G5    | 5010 1084h       |
| ADC2_G0_G5    | 5010 2084h       |
| ADC3_G0_G5    | 5010 3084h       |
| ADC4_G0_G5    | 5010 4084h       |

**Figure 3-42. ADC\_RESULTS\_ADCPPB4MAXI Name Register**

|            |    |    |    |    |    |      |   |
|------------|----|----|----|----|----|------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9    | 8 |
| RESERVED_1 |    |    |    |    |    | MAXI |   |
| R          |    |    |    |    |    | R    |   |
| 0h         |    |    |    |    |    | 0h   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1    | 0 |
| MAXI       |    |    |    |    |    |      |   |
| R          |    |    |    |    |    |      |   |
| 0h         |    |    |    |    |    |      |   |

**Table 3-130. ADC\_RESULTS\_ADCPPB4MAXI Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 9:0   | MAXI       | R    | 0h    | Post Processing Block 4 Oversampling Final Index of the Max. When either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event, the value of PMAI is loaded into this register. In the case of a count-match event, the max index loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information]. |

### 3.2.2.43 ADC\_RESULTS\_ADCPPB4MIN Register

#### 1 ADC\_RESULTS\_ADCPPB4MIN Register (Offset = 88h) [reset = 0h]

ADC PPB 4 Final Min Result Register.

Return to [Summary Table](#)

**Table 3-131. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 0088h       |
| ADC1_G0_G5    | 5010 1088h       |
| ADC2_G0_G5    | 5010 2088h       |
| ADC3_G0_G5    | 5010 3088h       |
| ADC4_G0_G5    | 5010 4088h       |

**Figure 3-43. ADC\_RESULTS\_ADCPPB4MIN Name Register**

|      |    |    |    |    |    |    |     |
|------|----|----|----|----|----|----|-----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24  |
| SIGN |    |    |    |    |    |    |     |
| R    |    |    |    |    |    |    |     |
| 0h   |    |    |    |    |    |    |     |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16  |
| SIGN |    |    |    |    |    |    | MIN |
| R    |    |    |    |    |    |    | R   |
| 0h   |    |    |    |    |    |    | 0h  |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8   |
| MIN  |    |    |    |    |    |    |     |
| R    |    |    |    |    |    |    |     |
| 0h   |    |    |    |    |    |    |     |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0   |
| MIN  |    |    |    |    |    |    |     |
| R    |    |    |    |    |    |    |     |
| 0h   |    |    |    |    |    |    |     |

**Table 3-133. ADC\_RESULTS\_ADCPPB4MIN Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 16.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 16:0  | MIN   | R    | 0h    | Post Processing Block 4 Oversampling Final Min. When either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event, the value of PMIN is loaded into this register. In the case of a count-match event, the max loaded into this register includes the value from the most recent conversion.<br>This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information]. |

### 3.2.2.44 ADC\_RESULTS\_ADCPPB4MINI Register

#### 1 ADC\_RESULTS\_ADCPPB4MINI Register (Offset = 8Ch) [reset = 0h]

ADC PPB 4 Final Min Index Result Register.

Return to [Summary Table](#)

**Table 3-134. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 5010 008Ch       |
| ADC1_G0_G5    | 5010 108Ch       |
| ADC2_G0_G5    | 5010 208Ch       |
| ADC3_G0_G5    | 5010 308Ch       |
| ADC4_G0_G5    | 5010 408Ch       |

**Figure 3-44. ADC\_RESULTS\_ADCPPB4MINI Name Register**

|            |    |    |    |    |    |      |   |
|------------|----|----|----|----|----|------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9    | 8 |
| RESERVED_1 |    |    |    |    |    | MINI |   |
| R          |    |    |    |    |    | R    |   |
| 0h         |    |    |    |    |    | 0h   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1    | 0 |
| MINI       |    |    |    |    |    |      |   |
| R          |    |    |    |    |    |      |   |
| 0h         |    |    |    |    |    |      |   |

**Table 3-136. ADC\_RESULTS\_ADCPPB4MINI Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 9:0   | MINI       | R    | 0h    | Post Processing Block 4 Oversampling Final Index of the Min. When either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event, the value of PMINI is loaded into this register. In the case of a count-match event, the min index loaded into this register includes the value from the most recent conversion. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available [only in case of a count-match event]. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information]. |

### 3.2.2.45 ADC\_CFG\_ADCCTL1 Register

#### 1 ADC\_CFG\_ADCCTL1 Register (Offset = 0h) [reset = 0h]

ADC Control 1 Register.

Return to [Summary Table](#)

**Table 3-137. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0000h       |
| ADC1_G0_G5    | 502C 1000h       |
| ADC2_G0_G5    | 502C 2000h       |
| ADC3_G0_G5    | 502C 3000h       |
| ADC4_G0_G5    | 502C 4000h       |

**Figure 3-45. ADC\_CFG\_ADCCTL1 Name Register**

| 15       | 14                | 13     | 12         | 11        | 10          | 9          | 8 |
|----------|-------------------|--------|------------|-----------|-------------|------------|---|
| TDMAEN   | EXTMUXPRESELECTEN | ADCBSY | RESERVED_3 | ADCBSYCHN |             |            |   |
| R/W      | R/W               | R      | R          | R         |             |            |   |
| 0h       | 0h                | 0h     | 0h         | 0h        |             |            |   |
| 7        | 6                 | 5      | 4          | 3         | 2           | 1          | 0 |
| ADCPWDNZ | RESERVED_2        |        |            |           | INTPULSEPOS | RESERVED_1 |   |
| R/W      | R                 |        |            |           | R/W         | R          |   |
| 0h       | 0h                |        |            |           | 0h          | 0h         |   |

**Table 3-139. ADC\_CFG\_ADCCTL1 Register Field Descriptions**

| Bit | Field             | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-----|-------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | TDMAEN            | R/W  | 0h    | Enable Alternate DMA Timings. This bit controls when the DMA is triggered.<br>0 DMA is triggered at the same time as the CPU interrupt<br>1 DMA is always triggered at tDMA regardless of whether the ADC is in early interrupt mode or late interrupt mode                                                                                                                                                                                                                                                                                                              |
| 14  | EXTMUXPRESELECTEN | R/W  | 0h    | If the ADC SOC sequence is deterministic, the ADCEXTMUX pins can be set earlier: at the end of the S+H window of the previous conversion instead of the beginning of the S+H window of the current conversion. This allows some of the external mux settling time to be pipelined with the previous conversion's conversion time. However, this will not work in the case where high-priority SOC's can arrive asynchronously.<br>0 ADCEXTMUX pins only change at beginning of S+H window<br>1 ADCEXTMUX pins are set after the end of S+H window based on pending SOC's |
| 13  | ADCBSY            | R    | 0h    | ADC Busy. Set when ADC SOC is generated, cleared by hardware four ADC clocks after negative edge of S/H pulse. Used by the ADC state machine to determine if ADC is available to sample.<br>0 ADC is available to sample next channel<br>1 ADC is busy and cannot sample another channel                                                                                                                                                                                                                                                                                 |
| 12  | RESERVED_3        | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |



**Table 3-139. ADC\_CFG\_ADCCTL1 Register Field Descriptions (continued)**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|-------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11:8 | ADCB SYCHN  | R    | 0h    | ADC Busy Channel. Set when an ADC Start of Conversion [SOC] is generated.<br>When ADCBSY<br>0:holds the value of the last converted SOC<br>When ADCBSY<br>1:reflects the SOC currently being processed<br>0h SOC0 is currently processing or was last SOC converted<br>1h SOC1 is currently processing or was last SOC converted<br>2h SOC2 is currently processing or was last SOC converted<br>3h SOC3 is currently processing or was last SOC converted<br>4h SOC4 is currently processing or was last SOC converted<br>5h SOC5 is currently processing or was last SOC converted<br>6h SOC6 is currently processing or was last SOC converted<br>7h SOC7 is currently processing or was last SOC converted<br>8h SOC8 is currently processing or was last SOC converted<br>9h SOC9 is currently processing or was last SOC converted<br>Ah SOC10 is currently processing or was last SOC converted<br>Bh SOC11 is currently processing or was last SOC converted<br>Ch SOC12 is currently processing or was last SOC converted<br>Dh SOC13 is currently processing or was last SOC converted<br>Eh SOC14 is currently processing or was last SOC converted<br>Fh SOC15 is currently processing or was last SOC converted |
| 7    | ADCPWDNZ    | R/W  | 0h    | ADC Power Down [active low]. This bit controls the power up and power down of all the analog circuitry inside the analog core.<br>0 All analog circuitry inside the core is powered down<br>1 All analog circuitry inside the core is powered up                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 6:3  | RESERVED_2  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 2    | INTPULSEPOS | R/W  | 0h    | ADC Interrupt Pulse Position.<br>0 Interrupt pulse generation occurs when ADC begins conversion [at the end of the acquisition window] plus a number of SYSCLK cycles as specified in the ADCINTCYCLE.OFFSET register.<br>1 Interrupt pulse generation occurs at the end of the conversion, 1 cycle prior to the ADC result latching into its result register                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 1:0  | RESERVED_1  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

### 3.2.2.46 ADC\_CFG\_ADCCTL2 Register

#### 1 ADC\_CFG\_ADCCTL2 Register (Offset = 2h) [reset = 0h]

ADC Control 2 Register.

Return to [Summary Table](#)

**Table 3-140. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0002h       |
| ADC1_G0_G5    | 502C 1002h       |
| ADC2_G0_G5    | 502C 2002h       |
| ADC3_G0_G5    | 502C 3002h       |
| ADC4_G0_G5    | 502C 4002h       |

**Figure 3-46. ADC\_CFG\_ADCCTL2 Name Register**

| 15         | 14         | 13         | 12 | 11         | 10 | 9 | 8           |
|------------|------------|------------|----|------------|----|---|-------------|
| RESERVED_3 |            |            |    | RESERVED_2 |    |   | OFFTRIMMODE |
| R          |            |            |    | R          |    |   | R/W         |
| 0h         |            |            |    | 0h         |    |   | 0h          |
| 7          | 6          | 5          | 4  | 3          | 2  | 1 | 0           |
| SIGNALMODE | RESOLUTION | RESERVED_1 |    | PRESCALE   |    |   |             |
| R/W        | R/W        | R          |    | R/W        |    |   |             |
| 0h         | 0h         | 0h         |    | 0h         |    |   |             |

**Table 3-142. ADC\_CFG\_ADCCTL2 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                    |
|-------|-------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | RESERVED_3  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                       |
| 12:9  | RESERVED_2  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                       |
| 8     | OFFTRIMMODE | R/W  | 0h    | ADC offset trim mode.<br>0 = Offset trim supplied by ADCOFFTRIM.OFFTRIM regardless of resolution or signal mode<br>1 = Offset trim for each combination of resolution, signalmode, and even or odd is supplied by a different field in ADCOFFTRIM, ADCOFFTRIM2, or ADCOFFTRIM3 |
| 7     | SIGNALMODE  | R/W  | 0h    | SOC Signaling Mode. Selects the input mode of the converter. Use the AdcSetMode function to change the signal mode.<br>0 Single-ended<br>1 Differential                                                                                                                        |
| 6     | RESOLUTION  | R/W  | 0h    | SOC Conversion Resolution. Selects the resolution of the converter. Use the AdcSetMode function to change the resolution.<br>0 12-bit resolution                                                                                                                               |
| 5:4   | RESERVED_1  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                       |

**Table 3-142. ADC\_CFG\_ADCCTL2 Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-----|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0 | PRESCALE | R/W  | 0h    | ADC Clock Prescaler.<br>0000 ADCCLK = Input Clock / 1.0<br>0001 Invalid<br>0010 ADCCLK = Input Clock / 2.0<br>0011 ADCCLK = Input Clock / 2.5<br>0100 ADCCLK = Input Clock / 3.0<br>0101 ADCCLK = Input Clock / 3.5<br>0110 ADCCLK = Input Clock / 4.0<br>0111 ADCCLK = Input Clock / 4.5<br>1000 ADCCLK = Input Clock / 5.0<br>1001 ADCCLK = Input Clock / 5.5<br>1010 ADCCLK = Input Clock / 6.0<br>1011 ADCCLK = Input Clock / 6.5<br>1100 ADCCLK = Input Clock / 7.0<br>1101 ADCCLK = Input Clock / 7.5<br>1110 ADCCLK = Input Clock / 8.0<br>1111 ADCCLK = Input Clock / 8.5 |

### 3.2.2.47 ADC\_CFG\_ADCBURSTCTL Register

#### 1 ADC\_CFG\_ADCBURSTCTL Register (Offset = 4h) [reset = 0h]

ADC Burst Control Register.

Return to [Summary Table](#)

**Table 3-143. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0004h       |
| ADC1_G0_G5    | 502C 1004h       |
| ADC2_G0_G5    | 502C 2004h       |
| ADC3_G0_G5    | 502C 3004h       |
| ADC4_G0_G5    | 502C 4004h       |

**Figure 3-47. ADC\_CFG\_ADCBURSTCTL Name Register**

| 15         | 14           | 13 | 12 | 11        | 10 | 9 | 8 |
|------------|--------------|----|----|-----------|----|---|---|
| BURSTEN    | RESERVED_2   |    |    | BURSTSIZE |    |   |   |
| R/W        | R            |    |    | R/W       |    |   |   |
| 0h         | 0h           |    |    | 0h        |    |   |   |
| 7          | 6            | 5  | 4  | 3         | 2  | 1 | 0 |
| RESERVED_1 | BURSTTRIGSEL |    |    |           |    |   |   |
| R          | R/W          |    |    |           |    |   |   |
| 0h         | 0h           |    |    |           |    |   |   |

**Table 3-145. ADC\_CFG\_ADCBURSTCTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | BURSTEN    | R/W  | 0h    | SOC Burst Mode Enable. This bit enables the SOC Burst Mode of operation.<br>0 Burst mode is disabled.<br>1 Burst mode is enabled.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 14:12 | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 11:8  | BURSTSIZE  | R/W  | 0h    | SOC Burst Size Select. This bit field determines how many SOC's are converted when a burst conversion sequence is started. The first SOC converted is defined by the round robin pointer, which is advanced as each SOC is converted.<br>0h 1 SOC converted<br>1h 2 SOC's converted<br>2h 3 SOC's converted<br>3h 4 SOC's converted<br>4h 5 SOC's converted<br>5h 6 SOC's converted<br>6h 7 SOC's converted<br>7h 8 SOC's converted<br>8h 9 SOC's converted<br>9h 10 SOC's converted<br>Ah 11 SOC's converted<br>Bh 12 SOC's converted<br>Ch 13 SOC's converted<br>Dh 14 SOC's converted<br>Eh 15 SOC's converted<br>Fh 16 SOC's converted<br>Note: If the burst causes SOC's to be set for conversion that were already pending, the corresponding bits in the ADCSOCOVF register will be set. |
| 7     | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

**Table 3-145. ADC\_CFG\_ADGBURSTCTL Register Field Descriptions (continued)**

| Bit | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-----|--------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6:0 | BURSTTRIGSEL | R/W  | 0h    | <p>SOC Burst Trigger Source Select. Configures which trigger will start a burst conversion sequence.</p> <p>Note: SOCFRC1 register can always be used to software trigger SOC's in addition to any hardware trigger configuration.</p> <p>00h BURSTTRIG0 - Software only<br/> 01h BURSTTRIG1 - RTI0 Timer<br/> 02h BURSTTRIG2 - RTI1 Timer<br/> 03h BURSTTRIG3 - RTI2 Timer<br/> 04h BURSTTRIG4 - RTI3 Timer<br/> 05h BURSTTRIG5 - InputXBAR.Out[5]<br/> 06h BURSTTRIG6 - spare<br/> 07h BURSTTRIG7 - spare<br/> 08h BURSTTRIG8 - EPWM0, ADCSOCA<br/> 09h BURSTTRIG9 - EPWM0, ADCSOCA<br/> 0Ah BURSTTRIG10 - EPWM1, ADCSOCA<br/> 0Bh BURSTTRIG11 - EPWM1, ADCSOCA<br/> 0Ch BURSTTRIG12 - EPWM2, ADCSOCA<br/> 0Dh BURSTTRIG13 - EPWM2, ADCSOCA<br/> 0Eh BURSTTRIG14 - EPWM3, ADCSOCA<br/> 0Fh BURSTTRIG15 - EPWM3, ADCSOCA<br/> .... EPWM4 to EPWM27<br/> 40h BURSTTRIG64 - EPWM28, ADCSOCA<br/> 41h BURSTTRIG65 - EPWM28, ADCSOCA<br/> 42h BURSTTRIG66 - EPWM29, ADCSOCA<br/> 43h BURSTTRIG67 - EPWM29, ADCSOCA<br/> 44h BURSTTRIG68 - EPWM30, ADCSOCA<br/> 45h BURSTTRIG69 - EPWM30, ADCSOCA<br/> 46h BURSTTRIG70 - EPWM31, ADCSOCA<br/> 47h BURSTTRIG71 - EPWM31, ADCSOCA<br/> 48h BURSTTRIG72 - ECAP0, TRIGOUT<br/> .... ECAP1 to ECAP8<br/> 51h BURSTTRIG81 - ECAP9, TRIGOUT<br/> 52h BURSTTRIG82 - ECAP10, TRIGOUT<br/> ....<br/> 57h BURSTTRIG73 - ECAP15, TRIGOUT<br/> 58h BURSTTRIG1 - RTI4 Timer<br/> 59h BURSTTRIG1 - RTI5 Timer<br/> 5Ah BURSTTRIG1 - RTI6 Timer<br/> 5Bh BURSTTRIG1 - RTI7 Timer</p> |

### 3.2.2.48 ADC\_CFG\_ADCINTFLG Register

#### 1 ADC\_CFG\_ADCINTFLG Register (Offset = 6h) [reset = 0h]

ADC Interrupt Flag Register.

Return to [Summary Table](#)

**Table 3-146. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0006h       |
| ADC1_G0_G5    | 502C 1006h       |
| ADC2_G0_G5    | 502C 2006h       |
| ADC3_G0_G5    | 502C 3006h       |
| ADC4_G0_G5    | 502C 4006h       |

**Figure 3-48. ADC\_CFG\_ADCINTFLG Name Register**

|                   |                   |                   |                   |         |         |         |         |
|-------------------|-------------------|-------------------|-------------------|---------|---------|---------|---------|
| 15                | 14                | 13                | 12                | 11      | 10      | 9       | 8       |
| RESERVED_1        |                   |                   |                   |         |         |         |         |
| R                 |                   |                   |                   |         |         |         |         |
| 0h                |                   |                   |                   |         |         |         |         |
| 7                 | 6                 | 5                 | 4                 | 3       | 2       | 1       | 0       |
| ADCINT4RESU<br>LT | ADCINT3RESU<br>LT | ADCINT2RESU<br>LT | ADCINT1RESU<br>LT | ADCINT4 | ADCINT3 | ADCINT2 | ADCINT1 |
| R                 | R                 | R                 | R                 | R       | R       | R       | R       |
| 0h                | 0h                | 0h                | 0h                | 0h      | 0h      | 0h      | 0h      |

**Table 3-148. ADC\_CFG\_ADCINTFLG Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|------|---------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED_1    | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 7    | ADCINT4RESULT | R    | 0h    | <p>ADC Interrupt 4 Results Ready Flag. This flag is set when the conversions results associated with ADCINT4 latch into the corresponding results register.</p> <p>0 Conversion results have not latched<br/>1 Conversion results have latched</p> <p>This flag can be used in an ISR that is entered in early interrupt mode to ensure that the corresponding results are ready before proceeding to read the result register.</p> <p>This flag can be cleared via the ACK bit in the ADCINTFLGCLR that also clears the ADCINT4 flag.</p> <p>In case results latch and this flag is already set, the corresponding flag in ADCINTOVF is NOT set. This flag does NOT have to be cleared in order for ADCINT ISRs to propagate to the PIE.</p> <p>In case the associated SOC is associated with a PPB or PPBs, the flag will not be set until all associated PPB results latch.</p> |

**Table 3-148. ADC\_CFG\_ADCINTFLG Register Field Descriptions (continued)**

| Bit | Field         | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-----|---------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6   | ADCINT3RESULT | R    | 0h    | <p>ADC Interrupt 3 Results Ready Flag. This flag is set when the conversions results associated with ADCINT3 latch into the corresponding results register.</p> <p>0 Conversion results have not latched<br/>1 Conversion results have latched</p> <p>This flag can be used in an ISR that is entered in early interrupt mode to ensure that the corresponding results are ready before proceeding to read the result register.</p> <p>This flag can be cleared via the ACK bit in the ADCINTFLGCLR that also clears the ADCINT3 flag.</p> <p>In case results latch and this flag is already set, the corresponding flag in ADCINTOVF is NOT set. This flag does NOT have to be cleared in order for ADCINT ISRs to propagate to the PIE.</p> <p>In case the associated SOC is associated with a PPB or PPBs, the flag will not be set until all associated PPB results latch.</p> |
| 5   | ADCINT2RESULT | R    | 0h    | <p>ADC Interrupt 2 Results Ready Flag. This flag is set when the conversions results associated with ADCINT2 latch into the corresponding results register.</p> <p>0 Conversion results have not latched<br/>1 Conversion results have latched</p> <p>This flag can be used in an ISR that is entered in early interrupt mode to ensure that the corresponding results are ready before proceeding to read the result register.</p> <p>This flag can be cleared via the ACK bit in the ADCINTFLGCLR that also clears the ADCINT2 flag.</p> <p>In case results latch and this flag is already set, the corresponding flag in ADCINTOVF is NOT set. This flag does NOT have to be cleared in order for ADCINT ISRs to propagate to the PIE.</p> <p>In case the associated SOC is associated with a PPB or PPBs, the flag will not be set until all associated PPB results latch.</p> |
| 4   | ADCINT1RESULT | R    | 0h    | <p>ADC Interrupt 1 Results Ready Flag. This flag is set when the conversions results associated with ADCINT1 latch into the corresponding results register.</p> <p>0 Conversion results have not latched<br/>1 Conversion results have latched</p> <p>This flag can be used in an ISR that is entered in early interrupt mode to ensure that the corresponding results are ready before proceeding to read the result register.</p> <p>This flag can be cleared via the ACK bit in the ADCINTFLGCLR that also clears the ADCINT1 flag.</p> <p>In case results latch and this flag is already set, the corresponding flag in ADCINTOVF is NOT set. This flag does NOT have to be cleared in order for ADCINT ISRs to propagate to the PIE.</p> <p>In case the associated SOC is associated with a PPB or PPBs, the flag will not be set until all associated PPB results latch.</p> |
| 3   | ADCINT4       | R    | 0h    | <p>ADC Interrupt 4 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear.</p> <p>0 No ADC interrupt pulse generated<br/>1 ADC interrupt pulse generated</p> <p>If the ADC interrupt is placed in continue to interrupt mode [INTSELxNy register] then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set.</p> <p>If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.</p>                                                                                                                                                                                                                      |

**Table 3-148. ADC\_CFG\_ADCINTFLG Register Field Descriptions (continued)**

| Bit | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-----|---------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | ADCINT3 | R    | 0h    | <p>ADC Interrupt 3 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear.</p> <p>0 No ADC interrupt pulse generated<br/>1 ADC interrupt pulse generated</p> <p>If the ADC interrupt is placed in continue to interrupt mode [INTSELxNy register] then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.</p> |
| 1   | ADCINT2 | R    | 0h    | <p>ADC Interrupt 2 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear.</p> <p>0 No ADC interrupt pulse generated<br/>1 ADC interrupt pulse generated</p> <p>If the ADC interrupt is placed in continue to interrupt mode [INTSELxNy register] then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.</p> |
| 0   | ADCINT1 | R    | 0h    | <p>ADC Interrupt 1 Flag. Reading these flags indicates if the associated ADCINT pulse was generated since the last clear.</p> <p>0 No ADC interrupt pulse generated<br/>1 ADC interrupt pulse generated</p> <p>If the ADC interrupt is placed in continue to interrupt mode [INTSELxNy register] then further interrupt pulses are generated whenever a selected EOC event occurs even if the flag bit is set. If the continuous mode is not enabled, then no further interrupt pulses are generated until the user clears this flag bit using the ADCINTFLGCLR register. Rather, an ADC interrupt overflow event occurs in the ADCINTOVF register.</p> |



### 3.2.2.49 ADC\_CFG\_ADCINTFLGCLR Register

#### 1 ADC\_CFG\_ADCINTFLGCLR Register (Offset = 8h) [reset = 0h]

ADC Interrupt Flag Clear Register.

Return to [Summary Table](#)

**Table 3-149. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0008h       |
| ADC1_G0_G5    | 502C 1008h       |
| ADC2_G0_G5    | 502C 2008h       |
| ADC3_G0_G5    | 502C 3008h       |
| ADC4_G0_G5    | 502C 4008h       |

**Figure 3-49. ADC\_CFG\_ADCINTFLGCLR Name Register**

|            |    |    |    |         |         |         |         |
|------------|----|----|----|---------|---------|---------|---------|
| 15         | 14 | 13 | 12 | 11      | 10      | 9       | 8       |
| RESERVED_1 |    |    |    |         |         |         |         |
| R          |    |    |    |         |         |         |         |
| 0h         |    |    |    |         |         |         |         |
| 7          | 6  | 5  | 4  | 3       | 2       | 1       | 0       |
| RESERVED_1 |    |    |    | ADCINT4 | ADCINT3 | ADCINT2 | ADCINT1 |
| R          |    |    |    | R/W1TS  | R/W1TS  | R/W1TS  | R/W1TS  |
| 0h         |    |    |    | 0h      | 0h      | 0h      | 0h      |

**Table 3-151. ADC\_CFG\_ADCINTFLGCLR Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                                         |
|------|------------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:4 | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                            |
| 3    | ADCINT4    | R/W1TS | 0h    | ADC Interrupt 4 Flag Clear. Reads return 0.<br>0 No action<br>1 Clears respective flag bit in the ADCINTFLG register. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set |
| 2    | ADCINT3    | R/W1TS | 0h    | ADC Interrupt 3 Flag Clear. Reads return 0.<br>0 No action<br>1 Clears respective flag bit in the ADCINTFLG register. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set |
| 1    | ADCINT2    | R/W1TS | 0h    | ADC Interrupt 2 Flag Clear. Reads return 0.<br>0 No action<br>1 Clears respective flag bit in the ADCINTFLG register. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set |
| 0    | ADCINT1    | R/W1TS | 0h    | ADC Interrupt 1 Flag Clear. Reads return 0.<br>0 No action<br>1 Clears respective flag bit in the ADCINTFLG register. If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set |

### 3.2.2.50 ADC\_CFG\_ADCINTOVF Register

#### 1 ADC\_CFG\_ADCINTOVF Register (Offset = Ah) [reset = 0h]

ADC Interrupt Overflow Register.

Return to [Summary Table](#)

**Table 3-152. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 000Ah       |
| ADC1_G0_G5    | 502C 100Ah       |
| ADC2_G0_G5    | 502C 200Ah       |
| ADC3_G0_G5    | 502C 300Ah       |
| ADC4_G0_G5    | 502C 400Ah       |

**Figure 3-50. ADC\_CFG\_ADCINTOVF Name Register**

|            |    |    |    |         |         |         |         |
|------------|----|----|----|---------|---------|---------|---------|
| 15         | 14 | 13 | 12 | 11      | 10      | 9       | 8       |
| RESERVED_1 |    |    |    |         |         |         |         |
| R          |    |    |    |         |         |         |         |
| 0h         |    |    |    |         |         |         |         |
| 7          | 6  | 5  | 4  | 3       | 2       | 1       | 0       |
| RESERVED_1 |    |    |    | ADCINT4 | ADCINT3 | ADCINT2 | ADCINT1 |
| R          |    |    |    | R       | R       | R       | R       |
| 0h         |    |    |    | 0h      | 0h      | 0h      | 0h      |

**Table 3-154. ADC\_CFG\_ADCINTOVF Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:4 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 3    | ADCINT4    | R    | 0h    | ADC Interrupt 4 Overflow Flags<br>Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs.<br>0 No ADC interrupt overflow event detected.<br>1 ADC Interrupt overflow event detected.<br>The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection. |
| 2    | ADCINT3    | R    | 0h    | ADC Interrupt 3 Overflow Flags<br>Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs.<br>0 No ADC interrupt overflow event detected.<br>1 ADC Interrupt overflow event detected.<br>The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection. |
| 1    | ADCINT2    | R    | 0h    | ADC Interrupt 2 Overflow Flags<br>Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs.<br>0 No ADC interrupt overflow event detected.<br>1 ADC Interrupt overflow event detected.<br>The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection. |

**Table 3-154. ADC\_CFG\_ADCINTOVF Register Field Descriptions (continued)**

| Bit | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-----|---------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | ADCINT1 | R    | 0h    | <p>ADC Interrupt 1 Overflow Flags</p> <p>Indicates if an overflow occurred when generating ADCINT pulses. If the respective ADCINTFLG bit is set and a selected additional EOC trigger is generated, then an overflow condition occurs.</p> <p>0 No ADC interrupt overflow event detected.</p> <p>1 ADC Interrupt overflow event detected.</p> <p>The overflow bit does not care about the continuous mode bit state. An overflow condition is generated irrespective of this mode selection.</p> |

### 3.2.2.51 ADC\_CFG\_ADCINTOVFCLR Register

#### 1 ADC\_CFG\_ADCINTOVFCLR Register (Offset = Ch) [reset = 0h]

ADC Interrupt Overflow Clear Register.

Return to [Summary Table](#)

**Table 3-155. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 000Ch       |
| ADC1_G0_G5    | 502C 100Ch       |
| ADC2_G0_G5    | 502C 200Ch       |
| ADC3_G0_G5    | 502C 300Ch       |
| ADC4_G0_G5    | 502C 400Ch       |

**Figure 3-51. ADC\_CFG\_ADCINTOVFCLR Name Register**

|            |    |    |    |         |         |         |         |
|------------|----|----|----|---------|---------|---------|---------|
| 15         | 14 | 13 | 12 | 11      | 10      | 9       | 8       |
| RESERVED_1 |    |    |    |         |         |         |         |
| R          |    |    |    |         |         |         |         |
| 0h         |    |    |    |         |         |         |         |
| 7          | 6  | 5  | 4  | 3       | 2       | 1       | 0       |
| RESERVED_1 |    |    |    | ADCINT4 | ADCINT3 | ADCINT2 | ADCINT1 |
| R          |    |    |    | R/W1TS  | R/W1TS  | R/W1TS  | R/W1TS  |
| 0h         |    |    |    | 0h      | 0h      | 0h      | 0h      |

**Table 3-157. ADC\_CFG\_ADCINTOVFCLR Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                                                                           |
|------|------------|--------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:4 | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                              |
| 3    | ADCINT4    | R/W1TS | 0h    | ADC Interrupt 4 Overflow Clear Bits<br>0 No action.<br>1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set. |
| 2    | ADCINT3    | R/W1TS | 0h    | ADC Interrupt 3 Overflow Clear Bits<br>0 No action.<br>1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set. |
| 1    | ADCINT2    | R/W1TS | 0h    | ADC Interrupt 2 Overflow Clear Bits<br>0 No action.<br>1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set. |
| 0    | ADCINT1    | R/W1TS | 0h    | ADC Interrupt 1 Overflow Clear Bits<br>0 No action.<br>1 Clears the respective overflow bit in the ADCINTOVF register. If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCINTOVF register, then hardware has priority and the ADCINTOVF bit will be set. |

### 3.2.2.52 ADC\_CFG\_ADCINTSEL1N2 Register

#### 1 ADC\_CFG\_ADCINTSEL1N2 Register (Offset = Eh) [reset = 0h]

ADC Interrupt 1 and 2 Selection Register.

Return to [Summary Table](#)

**Table 3-158. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 000Eh       |
| ADC1_G0_G5    | 502C 100Eh       |
| ADC2_G0_G5    | 502C 200Eh       |
| ADC3_G0_G5    | 502C 300Eh       |
| ADC4_G0_G5    | 502C 400Eh       |

**Figure 3-52. ADC\_CFG\_ADCINTSEL1N2 Name Register**

| 15         | 14       | 13    | 12      | 11 | 10 | 9 | 8 |
|------------|----------|-------|---------|----|----|---|---|
| RESERVED_2 | INT2CONT | INT2E | INT2SEL |    |    |   |   |
| R          | R/W      | R/W   | R/W     |    |    |   |   |
| 0h         | 0h       | 0h    | 0h      |    |    |   |   |
| 7          | 6        | 5     | 4       | 3  | 2  | 1 | 0 |
| RESERVED_1 | INT1CONT | INT1E | INT1SEL |    |    |   |   |
| R          | R/W      | R/W   | R/W     |    |    |   |   |
| 0h         | 0h       | 0h    | 0h      |    |    |   |   |

**Table 3-160. ADC\_CFG\_ADCINTSEL1N2 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 14   | INT2CONT   | R/W  | 0h    | ADCINT2 Continue to Interrupt Mode<br>0 No further ADCINT2 pulses are generated until ADCINT2 flag [in ADCINTFLG register] is cleared by user.<br>1 ADCINT2 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 13   | INT2E      | R/W  | 0h    | ADCINT2 Interrupt Enable<br>0 ADCINT2 is disabled<br>1 ADCINT2 is enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 12:8 | INT2SEL    | R/W  | 0h    | ADCINT2 EOC Source Select<br>00h EOC0 is trigger for ADCINT2<br>01h EOC1 is trigger for ADCINT2<br>02h EOC2 is trigger for ADCINT2<br>03h EOC3 is trigger for ADCINT2<br>04h EOC4 is trigger for ADCINT2<br>05h EOC5 is trigger for ADCINT2<br>06h EOC6 is trigger for ADCINT2<br>07h EOC7 is trigger for ADCINT2<br>08h EOC8 is trigger for ADCINT2<br>09h EOC9 is trigger for ADCINT2<br>0Ah EOC10 is trigger for ADCINT2<br>0Bh EOC11 is trigger for ADCINT2<br>0Ch EOC12 is trigger for ADCINT2<br>0Dh EOC13 is trigger for ADCINT2<br>0Eh EOC14 is trigger for ADCINT2<br>0Fh EOC15 is trigger for ADCINT2<br>10h OSINT1 is trigger for ADCINT2<br>11h OSINT2 is trigger for ADCINT2<br>12h OSINT3 is trigger for ADCINT2<br>13h OSINT4 is trigger for ADCINT2 |

**Table 3-160. ADC\_CFG\_ADCINTSEL1N2 Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 6   | INT1CONT   | R/W  | 0h    | ADCINT1 Continue to Interrupt Mode<br>0 No further ADCINT1 pulses are generated until ADCINT1 flag [in ADCINTFLG register] is cleared by user.<br>1 ADCINT1 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 5   | INT1E      | R/W  | 0h    | ADCINT1 Interrupt Enable<br>0 ADCINT1 is disabled<br>1 ADCINT1 is enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 4:0 | INT1SEL    | R/W  | 0h    | ADCINT1 EOC Source Select<br>00h EOC0 is trigger for ADCINT1<br>01h EOC1 is trigger for ADCINT1<br>02h EOC2 is trigger for ADCINT1<br>03h EOC3 is trigger for ADCINT1<br>04h EOC4 is trigger for ADCINT1<br>05h EOC5 is trigger for ADCINT1<br>06h EOC6 is trigger for ADCINT1<br>07h EOC7 is trigger for ADCINT1<br>08h EOC8 is trigger for ADCINT1<br>09h EOC9 is trigger for ADCINT1<br>0Ah EOC10 is trigger for ADCINT1<br>0Bh EOC11 is trigger for ADCINT1<br>0Ch EOC12 is trigger for ADCINT1<br>0Dh EOC13 is trigger for ADCINT1<br>0Eh EOC14 is trigger for ADCINT1<br>0Fh EOC15 is trigger for ADCINT1<br>10h OSINT1 is trigger for ADCINT1<br>11h OSINT2 is trigger for ADCINT1<br>12h OSINT3 is trigger for ADCINT1<br>13h OSINT4 is trigger for ADCINT1 |

### 3.2.2.53 ADC\_CFG\_ADCINTSEL3N4 Register

#### 1 ADC\_CFG\_ADCINTSEL3N4 Register (Offset = 10h) [reset = 0h]

ADC Interrupt 3 and 4 Selection Register.

Return to [Summary Table](#)

**Table 3-161. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0010h       |
| ADC1_G0_G5    | 502C 1010h       |
| ADC2_G0_G5    | 502C 2010h       |
| ADC3_G0_G5    | 502C 3010h       |
| ADC4_G0_G5    | 502C 4010h       |

**Figure 3-53. ADC\_CFG\_ADCINTSEL3N4 Name Register**

| 15         | 14       | 13    | 12      | 11 | 10 | 9 | 8 |
|------------|----------|-------|---------|----|----|---|---|
| RESERVED_2 | INT4CONT | INT4E | INT4SEL |    |    |   |   |
| R          | R/W      | R/W   | R/W     |    |    |   |   |
| 0h         | 0h       | 0h    | 0h      |    |    |   |   |
| 7          | 6        | 5     | 4       | 3  | 2  | 1 | 0 |
| RESERVED_1 | INT3CONT | INT3E | INT3SEL |    |    |   |   |
| R          | R/W      | R/W   | R/W     |    |    |   |   |
| 0h         | 0h       | 0h    | 0h      |    |    |   |   |

**Table 3-163. ADC\_CFG\_ADCINTSEL3N4 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 14   | INT4CONT   | R/W  | 0h    | ADCINT4 Continue to Interrupt Mode<br>0 No further ADCINT4 pulses are generated until ADCINT4 flag [in ADCINTFLG register] is cleared by user.<br>1 ADCINT4 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 13   | INT4E      | R/W  | 0h    | ADCINT4 Interrupt Enable<br>0 ADCINT4 is disabled<br>1 ADCINT4 is enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 12:8 | INT4SEL    | R/W  | 0h    | ADCINT4 EOC Source Select<br>00h EOC0 is trigger for ADCINT4<br>01h EOC1 is trigger for ADCINT4<br>02h EOC2 is trigger for ADCINT4<br>03h EOC3 is trigger for ADCINT4<br>04h EOC4 is trigger for ADCINT4<br>05h EOC5 is trigger for ADCINT4<br>06h EOC6 is trigger for ADCINT4<br>07h EOC7 is trigger for ADCINT4<br>08h EOC8 is trigger for ADCINT4<br>09h EOC9 is trigger for ADCINT4<br>0Ah EOC10 is trigger for ADCINT4<br>0Bh EOC11 is trigger for ADCINT4<br>0Ch EOC12 is trigger for ADCINT4<br>0Dh EOC13 is trigger for ADCINT4<br>0Eh EOC14 is trigger for ADCINT4<br>0Fh EOC15 is trigger for ADCINT4<br>10hOSINT1 is trigger for ADCINT4<br>11hOSINT2 is trigger for ADCINT4<br>12hOSINT3 is trigger for ADCINT4<br>13hOSINT4 is trigger for ADCINT4 |

**Table 3-163. ADC\_CFG\_ADCINTSEL3N4 Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 6   | INT3CONT   | R/W  | 0h    | ADCINT3 Continue to Interrupt Mode<br>0 No further ADCINT3 pulses are generated until ADCINT3 flag [in ADCINTFLG register] is cleared by user.<br>1 ADCINT3 pulses are generated whenever an EOC pulse is generated irrespective of whether the flag bit is cleared or not.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 5   | INT3E      | R/W  | 0h    | ADCINT3 Interrupt Enable<br>0 ADCINT3 is disabled<br>1 ADCINT3 is enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 4:0 | INT3SEL    | R/W  | 0h    | ADCINT3 EOC Source Select<br>00h EOC0 is trigger for ADCINT3<br>01h EOC1 is trigger for ADCINT3<br>02h EOC2 is trigger for ADCINT3<br>03h EOC3 is trigger for ADCINT3<br>04h EOC4 is trigger for ADCINT3<br>05h EOC5 is trigger for ADCINT3<br>06h EOC6 is trigger for ADCINT3<br>07h EOC7 is trigger for ADCINT3<br>08h EOC8 is trigger for ADCINT3<br>09h EOC9 is trigger for ADCINT3<br>0Ah EOC10 is trigger for ADCINT3<br>0Bh EOC11 is trigger for ADCINT3<br>0Ch EOC12 is trigger for ADCINT3<br>0Dh EOC13 is trigger for ADCINT3<br>0Eh EOC14 is trigger for ADCINT3<br>0Fh EOC15 is trigger for ADCINT3<br>10h OSINT1 is trigger for ADCINT3<br>11h OSINT2 is trigger for ADCINT3<br>12h OSINT3 is trigger for ADCINT3<br>13h OSINT4 is trigger for ADCINT3 |



### 3.2.2.54 ADC\_CFG\_ADCSOCPRCTL Register

#### 1 ADC\_CFG\_ADCSOCPRCTL Register (Offset = 12h) [reset = 200h]

ADC SOC Priority Control Register.

Return to [Summary Table](#)

**Table 3-164. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0012h       |
| ADC1_G0_G5    | 502C 1012h       |
| ADC2_G0_G5    | 502C 2012h       |
| ADC3_G0_G5    | 502C 3012h       |
| ADC4_G0_G5    | 502C 4012h       |

**Figure 3-54. ADC\_CFG\_ADCSOCPRCTL Name Register**

|            |    |    |             |    |    |           |   |
|------------|----|----|-------------|----|----|-----------|---|
| 15         | 14 | 13 | 12          | 11 | 10 | 9         | 8 |
| RESERVED_1 |    |    |             |    |    | RRPOINTER |   |
| R          |    |    |             |    |    | R         |   |
| 0h         |    |    |             |    |    | 10h       |   |
| 7          | 6  | 5  | 4           | 3  | 2  | 1         | 0 |
| RRPOINTER  |    |    | SOCPRIORITY |    |    |           |   |
| R          |    |    | R/W         |    |    |           |   |
| 10h        |    |    | 0h          |    |    |           |   |

**Table 3-166. ADC\_CFG\_ADCSOCPRCTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description |
|-------|------------|------|-------|-------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved    |

**Table 3-166. ADC\_CFG\_ADCSOCPRCTL Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9:5 | RRPOINTER | R    | 10h   | <p>Round Robin Pointer. Holds the value of the last converted round robin SOCx to be used by the round robin scheme to determine order of conversions.</p> <p>00h SOC0 was last round robin SOC to convert, SOC1 is highest round robin priority.</p> <p>01h SOC1 was last round robin SOC to convert, SOC2 is highest round robin priority.</p> <p>02h SOC2 was last round robin SOC to convert, SOC3 is highest round robin priority.</p> <p>03h SOC3 was last round robin SOC to convert, SOC4 is highest round robin priority.</p> <p>04h SOC4 was last round robin SOC to convert, SOC5 is highest round robin priority.</p> <p>05h SOC5 was last round robin SOC to convert, SOC6 is highest round robin priority.</p> <p>06h SOC6 was last round robin SOC to convert, SOC7 is highest round robin priority.</p> <p>07h SOC7 was last round robin SOC to convert, SOC8 is highest round robin priority.</p> <p>08h SOC8 was last round robin SOC to convert, SOC9 is highest round robin priority.</p> <p>09h SOC9 was last round robin SOC to convert, SOC10 is highest round robin priority.</p> <p>0Ah SOC10 was last round robin SOC to convert, SOC11 is highest round robin priority.</p> <p>0Bh SOC11 was last round robin SOC to convert, SOC12 is highest round robin priority.</p> <p>0Ch SOC12 was last round robin SOC to convert, SOC13 is highest round robin priority.</p> <p>0Dh SOC13 was last round robin SOC to convert, SOC14 is highest round robin priority.</p> <p>0Eh SOC14 was last round robin SOC to convert, SOC15 is highest round robin priority.</p> <p>0Fh SOC15 was last round robin SOC to convert, SOC0 is highest round robin priority.</p> <p>10h Reset value to indicate no SOC has been converted. SOC0 is highest round robin priority. Set to this value when the ADC module is reset by SOFTPRES or when the ADCSOCPRCTL register is written. In the latter case, if a conversion is currently in progress, it will complete and then the new priority will take effect.</p> <p>Others Invalid value.</p> |

**Table 3-166. ADC\_CFG\_ADCSOCPRCTL Register Field Descriptions (continued)**

| Bit | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-----|-------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | SOCPRIORITY | R/W  | 0h    | <p>SOC Priority</p> <p>Determines the cutoff point for priority mode and round robin arbitration for SOCx</p> <p>00h SOC priority is handled in round robin mode for all channels.</p> <p>01h SOC0 is high priority, rest of channels are in round robin mode.</p> <p>02h SOC0-SOC1 are high priority, SOC2-SOC15 are in round robin mode.</p> <p>03h SOC0-SOC2 are high priority, SOC3-SOC15 are in round robin mode.</p> <p>04h SOC0-SOC3 are high priority, SOC4-SOC15 are in round robin mode.</p> <p>05h SOC0-SOC4 are high priority, SOC5-SOC15 are in round robin mode.</p> <p>06h SOC0-SOC5 are high priority, SOC6-SOC15 are in round robin mode.</p> <p>07h SOC0-SOC6 are high priority, SOC7-SOC15 are in round robin mode.</p> <p>08h SOC0-SOC7 are high priority, SOC8-SOC15 are in round robin mode.</p> <p>09h SOC0-SOC8 are high priority, SOC9-SOC15 are in round robin mode.</p> <p>0Ah SOC0-SOC9 are high priority, SOC10-SOC15 are in round robin mode.</p> <p>0Bh SOC0-SOC10 are high priority, SOC11-SOC15 are in round robin mode.</p> <p>0Ch SOC0-SOC11 are high priority, SOC12-SOC15 are in round robin mode.</p> <p>0Dh SOC0-SOC12 are high priority, SOC13-SOC15 are in round robin mode.</p> <p>0Eh SOC0-SOC13 are high priority, SOC14-SOC15 are in round robin mode.</p> <p>0Fh SOC0-SOC14 are high priority, SOC15 is in round robin mode.</p> <p>10h All SOCx are in high priority mode, arbitrated by SOC number.</p> <p>Others Invalid selection.</p> |

### 3.2.2.55 ADC\_CFG\_ADCINTSOCSEL1 Register

#### 1 ADC\_CFG\_ADCINTSOCSEL1 Register (Offset = 14h) [reset = 0h]

ADC Interrupt SOC Selection 1 Register.

Return to [Summary Table](#)

**Table 3-167. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0014h       |
| ADC1_G0_G5    | 502C 1014h       |
| ADC2_G0_G5    | 502C 2014h       |
| ADC3_G0_G5    | 502C 3014h       |
| ADC4_G0_G5    | 502C 4014h       |

**Figure 3-55. ADC\_CFG\_ADCINTSOCSEL1 Name Register**

| 15   | 14 | 13   | 12 | 11   | 10 | 9    | 8 |
|------|----|------|----|------|----|------|---|
| SOC7 |    | SOC6 |    | SOC5 |    | SOC4 |   |
| R/W  |    | R/W  |    | R/W  |    | R/W  |   |
| 0h   |    | 0h   |    | 0h   |    | 0h   |   |
| 7    | 6  | 5    | 4  | 3    | 2  | 1    | 0 |
| SOC3 |    | SOC2 |    | SOC1 |    | SOC0 |   |
| R/W  |    | R/W  |    | R/W  |    | R/W  |   |
| 0h   |    | 0h   |    | 0h   |    | 0h   |   |

**Table 3-169. ADC\_CFG\_ADCINTSOCSEL1 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                   |
|-------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | SOC7  | R/W  | 0h    | SOC7 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC7. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register.<br>00 No ADCINT will trigger SOC7. TRIGSEL field alone determines SOC0 trigger.<br>01 ADCINT1 will trigger SOC7.<br>10 ADCINT2 will trigger SOC7.<br>11 Invalid selection. |
| 13:12 | SOC6  | R/W  | 0h    | SOC6 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC6. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register.<br>00 No ADCINT will trigger SOC6. TRIGSEL field alone determines SOC0 trigger.<br>01 ADCINT1 will trigger SOC6.<br>10 ADCINT2 will trigger SOC6.<br>11 Invalid selection. |
| 11:10 | SOC5  | R/W  | 0h    | SOC5 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC5. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register.<br>00 No ADCINT will trigger SOC5. TRIGSEL field alone determines SOC0 trigger.<br>01 ADCINT1 will trigger SOC5.<br>10 ADCINT2 will trigger SOC5.<br>11 Invalid selection. |

**Table 3-169. ADC\_CFG\_ADCINTSOCSEL1 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                   |
|-----|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9:8 | SOC4  | R/W  | 0h    | SOC4 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC4. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register.<br>00 No ADCINT will trigger SOC4. TRIGSEL field alone determines SOC0 trigger.<br>01 ADCINT1 will trigger SOC4.<br>10 ADCINT2 will trigger SOC4.<br>11 Invalid selection. |
| 7:6 | SOC3  | R/W  | 0h    | SOC3 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC3. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register.<br>00 No ADCINT will trigger SOC3. TRIGSEL field alone determines SOC0 trigger.<br>01 ADCINT1 will trigger SOC3.<br>10 ADCINT2 will trigger SOC3.<br>11 Invalid selection. |
| 5:4 | SOC2  | R/W  | 0h    | SOC2 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC2. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register.<br>00 No ADCINT will trigger SOC2. TRIGSEL field alone determines SOC0 trigger.<br>01 ADCINT1 will trigger SOC2.<br>10 ADCINT2 will trigger SOC2.<br>11 Invalid selection. |
| 3:2 | SOC1  | R/W  | 0h    | SOC1 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC1. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register.<br>00 No ADCINT will trigger SOC1. TRIGSEL field alone determines SOC0 trigger.<br>01 ADCINT1 will trigger SOC1.<br>10 ADCINT2 will trigger SOC1.<br>11 Invalid selection. |
| 1:0 | SOC0  | R/W  | 0h    | SOC0 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC0. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register.<br>00 No ADCINT will trigger SOC0. TRIGSEL field alone determines SOC0 trigger.<br>01 ADCINT1 will trigger SOC0.<br>10 ADCINT2 will trigger SOC0.<br>11 Invalid selection. |

### 3.2.2.56 ADC\_CFG\_ADCINTSOCSEL2 Register

#### 1 ADC\_CFG\_ADCINTSOCSEL2 Register (Offset = 16h) [reset = 0h]

ADC Interrupt SOC Selection 2 Register.

Return to [Summary Table](#)

**Table 3-170. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0016h       |
| ADC1_G0_G5    | 502C 1016h       |
| ADC2_G0_G5    | 502C 2016h       |
| ADC3_G0_G5    | 502C 3016h       |
| ADC4_G0_G5    | 502C 4016h       |

**Figure 3-56. ADC\_CFG\_ADCINTSOCSEL2 Name Register**

| 15    | 14 | 13    | 12 | 11    | 10 | 9     | 8 |
|-------|----|-------|----|-------|----|-------|---|
| SOC15 |    | SOC14 |    | SOC13 |    | SOC12 |   |
| R/W   |    | R/W   |    | R/W   |    | R/W   |   |
| 0h    |    | 0h    |    | 0h    |    | 0h    |   |
| 7     | 6  | 5     | 4  | 3     | 2  | 1     | 0 |
| SOC11 |    | SOC10 |    | SOC9  |    | SOC8  |   |
| R/W   |    | R/W   |    | R/W   |    | R/W   |   |
| 0h    |    | 0h    |    | 0h    |    | 0h    |   |

**Table 3-172. ADC\_CFG\_ADCINTSOCSEL2 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                        |
|-------|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | SOC15 | R/W  | 0h    | SOC15 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC15. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register.<br>00 No ADCINT will trigger SOC15. TRIGSEL field alone determines SOC0 trigger.<br>01 ADCINT1 will trigger SOC15.<br>10 ADCINT2 will trigger SOC15.<br>11 Invalid selection. |
| 13:12 | SOC14 | R/W  | 0h    | SOC14 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC14. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register.<br>00 No ADCINT will trigger SOC14. TRIGSEL field alone determines SOC0 trigger.<br>01 ADCINT1 will trigger SOC14.<br>10 ADCINT2 will trigger SOC14.<br>11 Invalid selection. |
| 11:10 | SOC13 | R/W  | 0h    | SOC13 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC13. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register.<br>00 No ADCINT will trigger SOC13. TRIGSEL field alone determines SOC0 trigger.<br>01 ADCINT1 will trigger SOC13.<br>10 ADCINT2 will trigger SOC13.<br>11 Invalid selection. |

**Table 3-172. ADC\_CFG\_ADCINTSOCSEL2 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                        |
|-----|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9:8 | SOC12 | R/W  | 0h    | SOC12 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC12. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register.<br>00 No ADCINT will trigger SOC12. TRIGSEL field alone determines SOC0 trigger.<br>01 ADCINT1 will trigger SOC12.<br>10 ADCINT2 will trigger SOC12.<br>11 Invalid selection. |
| 7:6 | SOC11 | R/W  | 0h    | SOC11 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC11. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register.<br>00 No ADCINT will trigger SOC11. TRIGSEL field alone determines SOC0 trigger.<br>01 ADCINT1 will trigger SOC11.<br>10 ADCINT2 will trigger SOC11.<br>11 Invalid selection. |
| 5:4 | SOC10 | R/W  | 0h    | SOC10 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC10. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register.<br>00 No ADCINT will trigger SOC10. TRIGSEL field alone determines SOC0 trigger.<br>01 ADCINT1 will trigger SOC10.<br>10 ADCINT2 will trigger SOC10.<br>11 Invalid selection. |
| 3:2 | SOC9  | R/W  | 0h    | SOC9 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC9. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register.<br>00 No ADCINT will trigger SOC9. TRIGSEL field alone determines SOC0 trigger.<br>01 ADCINT1 will trigger SOC9.<br>10 ADCINT2 will trigger SOC9.<br>11 Invalid selection.      |
| 1:0 | SOC8  | R/W  | 0h    | SOC8 ADC Interrupt Trigger Select. Selects which, if any, ADCINT triggers SOC8. The trigger selected in this field is in addition to the TRIGSEL field in the ADCSOCxCTL register.<br>00 No ADCINT will trigger SOC8. TRIGSEL field alone determines SOC0 trigger.<br>01 ADCINT1 will trigger SOC8.<br>10 ADCINT2 will trigger SOC8.<br>11 Invalid selection.      |

### 3.2.2.57 ADC\_CFG\_ADCSOCFLG1 Register

#### 1 ADC\_CFG\_ADCSOCFLG1 Register (Offset = 18h) [reset = 0h]

ADC SOC Flag 1 Register.

Return to [Summary Table](#)

**Table 3-173. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0018h       |
| ADC1_G0_G5    | 502C 1018h       |
| ADC2_G0_G5    | 502C 2018h       |
| ADC3_G0_G5    | 502C 3018h       |
| ADC4_G0_G5    | 502C 4018h       |

**Figure 3-57. ADC\_CFG\_ADCSOCFLG1 Name Register**

| 15    | 14    | 13    | 12    | 11    | 10    | 9    | 8    |
|-------|-------|-------|-------|-------|-------|------|------|
| SOC15 | SOC14 | SOC13 | SOC12 | SOC11 | SOC10 | SOC9 | SOC8 |
| R     | R     | R     | R     | R     | R     | R    | R    |
| 0h    | 0h    | 0h    | 0h    | 0h    | 0h    | 0h   | 0h   |
| 7     | 6     | 5     | 4     | 3     | 2     | 1    | 0    |
| SOC7  | SOC6  | SOC5  | SOC4  | SOC3  | SOC2  | SOC1 | SOC0 |
| R     | R     | R     | R     | R     | R     | R    | R    |
| 0h    | 0h    | 0h    | 0h    | 0h    | 0h    | 0h   | 0h   |

**Table 3-175. ADC\_CFG\_ADCSOCFLG1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | SOC15 | R    | 0h    | SOC15 Start of Conversion Flag. Indicates the state of SOC15 conversions.<br>0 No sample pending for SOC15.<br>1 Trigger has been received and sample is pending for SOC15.<br>This bit will be automatically cleared when the SOC15 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not. |
| 14  | SOC14 | R    | 0h    | SOC14 Start of Conversion Flag. Indicates the state of SOC14 conversions.<br>0 No sample pending for SOC14.<br>1 Trigger has been received and sample is pending for SOC14.<br>This bit will be automatically cleared when the SOC14 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not. |



**Table 3-175. ADC\_CFG\_ADCSOCFLG1 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 13  | SOC13 | R    | 0h    | SOC13 Start of Conversion Flag. Indicates the state of SOC13 conversions.<br>0 No sample pending for SOC13.<br>1 Trigger has been received and sample is pending for SOC13.<br>This bit will be automatically cleared when the SOC13 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not. |
| 12  | SOC12 | R    | 0h    | SOC12 Start of Conversion Flag. Indicates the state of SOC12 conversions.<br>0 No sample pending for SOC12.<br>1 Trigger has been received and sample is pending for SOC12.<br>This bit will be automatically cleared when the SOC12 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not. |
| 11  | SOC11 | R    | 0h    | SOC11 Start of Conversion Flag. Indicates the state of SOC11 conversions.<br>0 No sample pending for SOC11.<br>1 Trigger has been received and sample is pending for SOC11.<br>This bit will be automatically cleared when the SOC11 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not. |
| 10  | SOC10 | R    | 0h    | SOC10 Start of Conversion Flag. Indicates the state of SOC10 conversions.<br>0 No sample pending for SOC10.<br>1 Trigger has been received and sample is pending for SOC10.<br>This bit will be automatically cleared when the SOC10 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not. |
| 9   | SOC9  | R    | 0h    | SOC9 Start of Conversion Flag. Indicates the state of SOC9 conversions.<br>0 No sample pending for SOC9.<br>1 Trigger has been received and sample is pending for SOC9.<br>This bit will be automatically cleared when the SOC9 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.      |

**Table 3-175. ADC\_CFG\_ADCSOCFLG1 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-----|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8   | SOC8  | R    | 0h    | <p>SOC8 Start of Conversion Flag. Indicates the state of SOC8 conversions.</p> <p>0 No sample pending for SOC8.</p> <p>1 Trigger has been received and sample is pending for SOC8.</p> <p>This bit will be automatically cleared when the SOC8 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.</p> |
| 7   | SOC7  | R    | 0h    | <p>SOC7 Start of Conversion Flag. Indicates the state of SOC7 conversions.</p> <p>0 No sample pending for SOC7.</p> <p>1 Trigger has been received and sample is pending for SOC7.</p> <p>This bit will be automatically cleared when the SOC7 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.</p> |
| 6   | SOC6  | R    | 0h    | <p>SOC6 Start of Conversion Flag. Indicates the state of SOC6 conversions.</p> <p>0 No sample pending for SOC6.</p> <p>1 Trigger has been received and sample is pending for SOC6.</p> <p>This bit will be automatically cleared when the SOC6 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.</p> |
| 5   | SOC5  | R    | 0h    | <p>SOC5 Start of Conversion Flag. Indicates the state of SOC5 conversions.</p> <p>0 No sample pending for SOC5.</p> <p>1 Trigger has been received and sample is pending for SOC5.</p> <p>This bit will be automatically cleared when the SOC5 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.</p> |
| 4   | SOC4  | R    | 0h    | <p>SOC4 Start of Conversion Flag. Indicates the state of SOC4 conversions.</p> <p>0 No sample pending for SOC4.</p> <p>1 Trigger has been received and sample is pending for SOC4.</p> <p>This bit will be automatically cleared when the SOC4 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.</p> |

**Table 3-175. ADC\_CFG\_ADCSOCFLG1 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-----|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3   | SOC3  | R    | 0h    | <p>SOC3 Start of Conversion Flag. Indicates the state of SOC3 conversions.</p> <p>0 No sample pending for SOC3.</p> <p>1 Trigger has been received and sample is pending for SOC3.</p> <p>This bit will be automatically cleared when the SOC3 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.</p> |
| 2   | SOC2  | R    | 0h    | <p>SOC2 Start of Conversion Flag. Indicates the state of SOC2 conversions.</p> <p>0 No sample pending for SOC2.</p> <p>1 Trigger has been received and sample is pending for SOC2.</p> <p>This bit will be automatically cleared when the SOC2 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.</p> |
| 1   | SOC1  | R    | 0h    | <p>SOC1 Start of Conversion Flag. Indicates the state of SOC1 conversions.</p> <p>0 No sample pending for SOC1.</p> <p>1 Trigger has been received and sample is pending for SOC1.</p> <p>This bit will be automatically cleared when the SOC1 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.</p> |
| 0   | SOC0  | R    | 0h    | <p>SOC0 Start of Conversion Flag. Indicates the state of SOC0 conversions.</p> <p>0 No sample pending for SOC0.</p> <p>1 Trigger has been received and sample is pending for SOC0.</p> <p>This bit will be automatically cleared when the SOC0 conversion is started. If contention exists where this bit receives both a request to set and a request to clear on the same cycle, regardless of the source of either, this bit will be set and the request to clear will be ignored. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether this bit was previously set or not.</p> |

### 3.2.2.58 ADC\_CFG\_ADCSOCFRC1 Register

#### 1 ADC\_CFG\_ADCSOCFRC1 Register (Offset = 1Ah) [reset = 0h]

ADC SOC Force 1 Register.

Return to [Summary Table](#)

**Table 3-176. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 001Ah       |
| ADC1_G0_G5    | 502C 101Ah       |
| ADC2_G0_G5    | 502C 201Ah       |
| ADC3_G0_G5    | 502C 301Ah       |
| ADC4_G0_G5    | 502C 401Ah       |

**Figure 3-58. ADC\_CFG\_ADCSOCFRC1 Name Register**

| 15     | 14     | 13     | 12     | 11     | 10     | 9      | 8      |
|--------|--------|--------|--------|--------|--------|--------|--------|
| SOC15  | SOC14  | SOC13  | SOC12  | SOC11  | SOC10  | SOC9   | SOC8   |
| R/W1TS | R/W1TS | R/W1TS | R/W1TS | R/W1TS | R/W1TS | R/W1TS | R/W1TS |
| 0h     | 0h     | 0h     | 0h     | 0h     | 0h     | 0h     | 0h     |
| 7      | 6      | 5      | 4      | 3      | 2      | 1      | 0      |
| SOC7   | SOC6   | SOC5   | SOC4   | SOC3   | SOC2   | SOC1   | SOC0   |
| R/W1TS | R/W1TS | R/W1TS | R/W1TS | R/W1TS | R/W1TS | R/W1TS | R/W1TS |
| 0h     | 0h     | 0h     | 0h     | 0h     | 0h     | 0h     | 0h     |

**Table 3-178. ADC\_CFG\_ADCSOCFRC1 Register Field Descriptions**

| Bit | Field | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-----|-------|--------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | SOC15 | R/W1TS | 0h    | SOC15 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC15 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.<br>0 No action.<br>1 Force SOC15 flag bit to 1. This will cause a conversion to start once priority is given to SOC15.<br>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC15 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not. |
| 14  | SOC14 | R/W1TS | 0h    | SOC14 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC14 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.<br>0 No action.<br>1 Force SOC14 flag bit to 1. This will cause a conversion to start once priority is given to SOC14.<br>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC14 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not. |

**Table 3-178. ADC\_CFG\_ADCSOCFRC1 Register Field Descriptions (continued)**

| Bit | Field | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|-------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 13  | SOC13 | R/W1TS | 0h    | <p>SOC13 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC13 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC13 flag bit to 1. This will cause a conversion to start once priority is given to SOC13.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC13 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p> |
| 12  | SOC12 | R/W1TS | 0h    | <p>SOC12 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC12 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC12 flag bit to 1. This will cause a conversion to start once priority is given to SOC12.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC12 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p> |
| 11  | SOC11 | R/W1TS | 0h    | <p>SOC11 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC11 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC11 flag bit to 1. This will cause a conversion to start once priority is given to SOC11.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC11 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p> |
| 10  | SOC10 | R/W1TS | 0h    | <p>SOC10 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC10 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC10 flag bit to 1. This will cause a conversion to start once priority is given to SOC10.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC10 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p> |

**Table 3-178. ADC\_CFG\_ADCSOCFRC1 Register Field Descriptions (continued)**

| Bit | Field | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|-------|--------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9   | SOC9  | R/W1TS | 0h    | <p>SOC9 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC9 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC9 flag bit to 1. This will cause a conversion to start once priority is given to SOC9.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC9 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p> |
| 8   | SOC8  | R/W1TS | 0h    | <p>SOC8 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC8 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC8 flag bit to 1. This will cause a conversion to start once priority is given to SOC8.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC8 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p> |
| 7   | SOC7  | R/W1TS | 0h    | <p>SOC7 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC7 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC7 flag bit to 1. This will cause a conversion to start once priority is given to SOC7.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC7 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p> |
| 6   | SOC6  | R/W1TS | 0h    | <p>SOC6 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC6 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC6 flag bit to 1. This will cause a conversion to start once priority is given to SOC6.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC6 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p> |

**Table 3-178. ADC\_CFG\_ADCSOCFRC1 Register Field Descriptions (continued)**

| Bit | Field | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|-------|--------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | SOC5  | R/W1TS | 0h    | <p>SOC5 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC5 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC5 flag bit to 1. This will cause a conversion to start once priority is given to SOC5.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC5 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p> |
| 4   | SOC4  | R/W1TS | 0h    | <p>SOC4 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC4 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC4 flag bit to 1. This will cause a conversion to start once priority is given to SOC4.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC4 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p> |
| 3   | SOC3  | R/W1TS | 0h    | <p>SOC3 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC3 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC3 flag bit to 1. This will cause a conversion to start once priority is given to SOC3.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC3 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p> |
| 2   | SOC2  | R/W1TS | 0h    | <p>SOC2 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC2 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC2 flag bit to 1. This will cause a conversion to start once priority is given to SOC2.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC2 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p> |

**Table 3-178. ADC\_CFG\_ADCSOCFRC1 Register Field Descriptions (continued)**

| Bit | Field | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|-------|--------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | SOC1  | R/W1TS | 0h    | <p>SOC1 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC1 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC1 flag bit to 1. This will cause a conversion to start once priority is given to SOC1.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC1 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p> |
| 0   | SOC0  | R/W1TS | 0h    | <p>SOC0 Force Start of Conversion Bit. Writing a 1 will force to 1 the SOC0 flag in the ADCSOCFLG1 register. This can be used to initiate a software initiated conversion. Writes of 0 are ignored. This bit will always read as a 0.</p> <p>0 No action.</p> <p>1 Force SOC0 flag bit to 1. This will cause a conversion to start once priority is given to SOC0.</p> <p>If software tries to set this bit on the same clock cycle that hardware tries to clear the SOC0 bit in the ADCSOCFLG1 register, then software has priority and the ADCSOCFLG1 bit will be set. In this case the overflow bit in the ADCSOCOVF1 register will not be affected regardless of whether the ADCSOCFLG1 bit was previously set or not.</p> |



### 3.2.2.59 ADC\_CFG\_ADCSOCOVF1 Register

#### 1 ADC\_CFG\_ADCSOCOVF1 Register (Offset = 1Ch) [reset = 0h]

ADC SOC Overflow 1 Register.

Return to [Summary Table](#)

**Table 3-179. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 001Ch       |
| ADC1_G0_G5    | 502C 101Ch       |
| ADC2_G0_G5    | 502C 201Ch       |
| ADC3_G0_G5    | 502C 301Ch       |
| ADC4_G0_G5    | 502C 401Ch       |

**Figure 3-59. ADC\_CFG\_ADCSOCOVF1 Name Register**

| 15    | 14    | 13    | 12    | 11    | 10    | 9    | 8    |
|-------|-------|-------|-------|-------|-------|------|------|
| SOC15 | SOC14 | SOC13 | SOC12 | SOC11 | SOC10 | SOC9 | SOC8 |
| R     | R     | R     | R     | R     | R     | R    | R    |
| 0h    | 0h    | 0h    | 0h    | 0h    | 0h    | 0h   | 0h   |
| 7     | 6     | 5     | 4     | 3     | 2     | 1    | 0    |
| SOC7  | SOC6  | SOC5  | SOC4  | SOC3  | SOC2  | SOC1 | SOC0 |
| R     | R     | R     | R     | R     | R     | R    | R    |
| 0h    | 0h    | 0h    | 0h    | 0h    | 0h    | 0h   | 0h   |

**Table 3-181. ADC\_CFG\_ADCSOCOVF1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                   |
|-----|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | SOC15 | R    | 0h    | SOC15 Start of Conversion Overflow Flag. Indicates an SOC15 event was generated in hardware while an existing SOC15 event was already pending.<br>0 No SOC15 event overflow.<br>1 SOC15 event overflow.<br>An overflow condition does not stop SOC15 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit. |
| 14  | SOC14 | R    | 0h    | SOC14 Start of Conversion Overflow Flag. Indicates an SOC14 event was generated in hardware while an existing SOC14 event was already pending.<br>0 No SOC14 event overflow.<br>1 SOC14 event overflow.<br>An overflow condition does not stop SOC14 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit. |
| 13  | SOC13 | R    | 0h    | SOC13 Start of Conversion Overflow Flag. Indicates an SOC13 event was generated in hardware while an existing SOC13 event was already pending.<br>0 No SOC13 event overflow.<br>1 SOC13 event overflow.<br>An overflow condition does not stop SOC13 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit. |

**Table 3-181. ADC\_CFG\_ADCSOCOVF1 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                   |
|-----|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12  | SOC12 | R    | 0h    | SOC12 Start of Conversion Overflow Flag. Indicates an SOC12 event was generated in hardware while an existing SOC12 event was already pending.<br>0 No SOC12 event overflow.<br>1 SOC12 event overflow.<br>An overflow condition does not stop SOC12 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit. |
| 11  | SOC11 | R    | 0h    | SOC11 Start of Conversion Overflow Flag. Indicates an SOC11 event was generated in hardware while an existing SOC11 event was already pending.<br>0 No SOC11 event overflow.<br>1 SOC11 event overflow.<br>An overflow condition does not stop SOC11 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit. |
| 10  | SOC10 | R    | 0h    | SOC10 Start of Conversion Overflow Flag. Indicates an SOC10 event was generated in hardware while an existing SOC10 event was already pending.<br>0 No SOC10 event overflow.<br>1 SOC10 event overflow.<br>An overflow condition does not stop SOC10 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit. |
| 9   | SOC9  | R    | 0h    | SOC9 Start of Conversion Overflow Flag. Indicates an SOC9 event was generated in hardware while an existing SOC9 event was already pending.<br>0 No SOC9 event overflow.<br>1 SOC9 event overflow.<br>An overflow condition does not stop SOC9 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.       |
| 8   | SOC8  | R    | 0h    | SOC8 Start of Conversion Overflow Flag. Indicates an SOC8 event was generated in hardware while an existing SOC8 event was already pending.<br>0 No SOC8 event overflow.<br>1 SOC8 event overflow.<br>An overflow condition does not stop SOC8 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.       |
| 7   | SOC7  | R    | 0h    | SOC7 Start of Conversion Overflow Flag. Indicates an SOC7 event was generated in hardware while an existing SOC7 event was already pending.<br>0 No SOC7 event overflow.<br>1 SOC7 event overflow.<br>An overflow condition does not stop SOC7 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.       |
| 6   | SOC6  | R    | 0h    | SOC6 Start of Conversion Overflow Flag. Indicates an SOC6 event was generated in hardware while an existing SOC6 event was already pending.<br>0 No SOC6 event overflow.<br>1 SOC6 event overflow.<br>An overflow condition does not stop SOC6 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit.       |

**Table 3-181. ADC\_CFG\_ADCSOCOVF1 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                             |
|-----|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | SOC5  | R    | 0h    | SOC5 Start of Conversion Overflow Flag. Indicates an SOC5 event was generated in hardware while an existing SOC5 event was already pending.<br>0 No SOC5 event overflow.<br>1 SOC5 event overflow.<br>An overflow condition does not stop SOC5 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit. |
| 4   | SOC4  | R    | 0h    | SOC4 Start of Conversion Overflow Flag. Indicates an SOC4 event was generated in hardware while an existing SOC4 event was already pending.<br>0 No SOC4 event overflow.<br>1 SOC4 event overflow.<br>An overflow condition does not stop SOC4 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit. |
| 3   | SOC3  | R    | 0h    | SOC3 Start of Conversion Overflow Flag. Indicates an SOC3 event was generated in hardware while an existing SOC3 event was already pending.<br>0 No SOC3 event overflow.<br>1 SOC3 event overflow.<br>An overflow condition does not stop SOC3 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit. |
| 2   | SOC2  | R    | 0h    | SOC2 Start of Conversion Overflow Flag. Indicates an SOC2 event was generated in hardware while an existing SOC2 event was already pending.<br>0 No SOC2 event overflow.<br>1 SOC2 event overflow.<br>An overflow condition does not stop SOC2 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit. |
| 1   | SOC1  | R    | 0h    | SOC1 Start of Conversion Overflow Flag. Indicates an SOC1 event was generated in hardware while an existing SOC1 event was already pending.<br>0 No SOC1 event overflow.<br>1 SOC1 event overflow.<br>An overflow condition does not stop SOC1 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit. |
| 0   | SOC0  | R    | 0h    | SOC0 Start of Conversion Overflow Flag. Indicates an SOC0 event was generated in hardware while an existing SOC0 event was already pending.<br>0 No SOC0 event overflow.<br>1 SOC0 event overflow.<br>An overflow condition does not stop SOC0 events from being processed. It simply is an indication that a hardware trigger was missed. A write to the ADCSOCFRC1 register does not effect this bit. |

### 3.2.2.60 ADC\_CFG\_ADCSOCOVFCLR1 Register

#### 1 ADC\_CFG\_ADCSOCOVFCLR1 Register (Offset = 1Eh) [reset = 0h]

ADC SOC Overflow Clear 1 Register.

Return to [Summary Table](#)

**Table 3-182. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 001Eh       |
| ADC1_G0_G5    | 502C 101Eh       |
| ADC2_G0_G5    | 502C 201Eh       |
| ADC3_G0_G5    | 502C 301Eh       |
| ADC4_G0_G5    | 502C 401Eh       |

**Figure 3-60. ADC\_CFG\_ADCSOCOVFCLR1 Name Register**

| 15     | 14     | 13     | 12     | 11     | 10     | 9      | 8      |
|--------|--------|--------|--------|--------|--------|--------|--------|
| SOC15  | SOC14  | SOC13  | SOC12  | SOC11  | SOC10  | SOC9   | SOC8   |
| R/W1TS | R/W1TS | R/W1TS | R/W1TS | R/W1TS | R/W1TS | R/W1TS | R/W1TS |
| 0h     | 0h     | 0h     | 0h     | 0h     | 0h     | 0h     | 0h     |
| 7      | 6      | 5      | 4      | 3      | 2      | 1      | 0      |
| SOC7   | SOC6   | SOC5   | SOC4   | SOC3   | SOC2   | SOC1   | SOC0   |
| R/W1TS | R/W1TS | R/W1TS | R/W1TS | R/W1TS | R/W1TS | R/W1TS | R/W1TS |
| 0h     | 0h     | 0h     | 0h     | 0h     | 0h     | 0h     | 0h     |

**Table 3-184. ADC\_CFG\_ADCSOCOVFCLR1 Register Field Descriptions**

| Bit | Field | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|-------|--------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | SOC15 | R/W1TS | 0h    | SOC15 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC15 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0.<br>0 No action.<br>1 Clear SOC15 overflow flag.<br>If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. |
| 14  | SOC14 | R/W1TS | 0h    | SOC14 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC14 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0.<br>0 No action.<br>1 Clear SOC14 overflow flag.<br>If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. |
| 13  | SOC13 | R/W1TS | 0h    | SOC13 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC13 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0.<br>0 No action.<br>1 Clear SOC13 overflow flag.<br>If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. |

**Table 3-184. ADC\_CFG\_ADCSOCOVFCLR1 Register Field Descriptions (continued)**

| Bit | Field | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|-------|--------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12  | SOC12 | R/W1TS | 0h    | SOC12 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC12 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0.<br>0 No action.<br>1 Clear SOC12 overflow flag.<br>If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. |
| 11  | SOC11 | R/W1TS | 0h    | SOC11 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC11 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0.<br>0 No action.<br>1 Clear SOC11 overflow flag.<br>If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. |
| 10  | SOC10 | R/W1TS | 0h    | SOC10 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC10 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0.<br>0 No action.<br>1 Clear SOC10 overflow flag.<br>If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. |
| 9   | SOC9  | R/W1TS | 0h    | SOC9 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC9 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0.<br>0 No action.<br>1 Clear SOC9 overflow flag.<br>If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..    |
| 8   | SOC8  | R/W1TS | 0h    | SOC8 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC8 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0.<br>0 No action.<br>1 Clear SOC8 overflow flag.<br>If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..    |
| 7   | SOC7  | R/W1TS | 0h    | SOC7 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC7 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0.<br>0 No action.<br>1 Clear SOC7 overflow flag.<br>If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..    |
| 6   | SOC6  | R/W1TS | 0h    | SOC6 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC6 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0.<br>0 No action.<br>1 Clear SOC6 overflow flag.<br>If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set..    |

**Table 3-184. ADC\_CFG\_ADCSOCOVFCLR1 Register Field Descriptions (continued)**

| Bit | Field | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-----|-------|--------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | SOC5  | R/W1TS | 0h    | SOC5 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC5 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0.<br>0 No action.<br>1 Clear SOC5 overflow flag.<br>If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. |
| 4   | SOC4  | R/W1TS | 0h    | SOC4 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC4 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0.<br>0 No action.<br>1 Clear SOC4 overflow flag.<br>If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. |
| 3   | SOC3  | R/W1TS | 0h    | SOC3 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC3 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0.<br>0 No action.<br>1 Clear SOC3 overflow flag.<br>If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. |
| 2   | SOC2  | R/W1TS | 0h    | SOC2 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC2 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0.<br>0 No action.<br>1 Clear SOC2 overflow flag.<br>If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. |
| 1   | SOC1  | R/W1TS | 0h    | SOC1 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC1 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0.<br>0 No action.<br>1 Clear SOC1 overflow flag.<br>If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. |
| 0   | SOC0  | R/W1TS | 0h    | SOC0 Clear Start of Conversion Overflow Bit. Writing a 1 will clear the SOC0 overflow flag in the ADCSOCOVF1 register. Writes of 0 are ignored. Reads will always return a 0.<br>0 No action.<br>1 Clear SOC0 overflow flag.<br>If software tries to set this bit on the same clock cycle that hardware tries to set the overflow bit in the ADCSOCOVF1 register, then hardware has priority and the ADCSOCOVF1 bit will be set.. |

### 3.2.2.61 ADC\_CFG\_ADCSOC0CTL Register

#### 1 ADC\_CFG\_ADCSOC0CTL Register (Offset = 20h) [reset = 0h]

ADC SOC0 Control Register.

Return to [Summary Table](#)

**Table 3-185. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0020h       |
| ADC1_G0_G5    | 502C 1020h       |
| ADC2_G0_G5    | 502C 2020h       |
| ADC3_G0_G5    | 502C 3020h       |
| ADC4_G0_G5    | 502C 4020h       |

**Figure 3-61. ADC\_CFG\_ADCSOC0CTL Name Register**

|          |            |    |    |            |         |            |       |
|----------|------------|----|----|------------|---------|------------|-------|
| 31       | 30         | 29 | 28 | 27         | 26      | 25         | 24    |
| EXTCHSEL |            |    |    | RESERVED_2 | TRIGSEL |            |       |
| R/W      |            |    |    | R          | R/W     |            |       |
| 0h       |            |    |    | 0h         | 0h      |            |       |
| 23       | 22         | 21 | 20 | 19         | 18      | 17         | 16    |
| TRIGSEL  |            |    |    | CHSEL      |         |            |       |
| R/W      |            |    |    | R/W        |         |            |       |
| 0h       |            |    |    | 0h         |         |            |       |
| 15       | 14         | 13 | 12 | 11         | 10      | 9          | 8     |
| CHSEL    | RESOLUTION |    |    | SIGNALMODE |         | RESERVED_1 | ACQPS |
| R/W      | R          |    |    | R          |         | R          | R/W   |
| 0h       | 0h         |    |    | 0h         |         | 0h         | 0h    |
| 7        | 6          | 5  | 4  | 3          | 2       | 1          | 0     |
| ACQPS    |            |    |    |            |         |            |       |
| R/W      |            |    |    |            |         |            |       |
| 0h       |            |    |    |            |         |            |       |

**Table 3-187. ADC\_CFG\_ADCSOC0CTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                     |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28 | EXTCHSEL   | R/W  | 0h    | SOC0 External Channel Mux Select. Selects the external mux combination to output when SOC0 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. |
| 27    | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                        |

**Table 3-187. ADC\_CFG\_ADCSOC0CTL Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:20 | TRIGSEL    | R/W  | 0h    | <p>SOC0 Trigger Source Select. Along with the SOC0 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC0 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it.</p> <p>Note: SOCFRC1 register can always be used to software trigger SOC0s in addition to any hardware trigger configuration.</p> <p>00h ADCTRIG0 - Software only<br/> 01h ADCTRIG1 - RTI0 Timer<br/> 02h ADCTRIG2 - RTI1 Timer<br/> 03h ADCTRIG3 - RTI2 Timer<br/> 04h ADCTRIG4 - RTI3 Timer<br/> 05h ADCTRIG5 - InputXBAR.Out[5]<br/> 06h ADCTRIG6 - spare<br/> 07h ADCTRIG7 - spare<br/> 08h ADCTRIG8 - EPWM0, ADCSOCA<br/> 09h ADCTRIG9 - EPWM0, ADCSOCA<br/> 0Ah ADCTRIG10 - EPWM1, ADCSOCA<br/> 0Bh ADCTRIG11 - EPWM1, ADCSOCA<br/> 0Ch ADCTRIG12 - EPWM2, ADCSOCA<br/> 0Dh ADCTRIG13 - EPWM2, ADCSOCA<br/> 0Eh ADCTRIG14 - EPWM3, ADCSOCA<br/> 0Fh ADCTRIG15 - EPWM3, ADCSOCA<br/> .... EPWM4 to EPWM27<br/> 40h ADCTRIG64 - EPWM28, ADCSOCA<br/> 41h ADCTRIG65 - EPWM28, ADCSOCA<br/> 42h ADCTRIG66 - EPWM29, ADCSOCA<br/> 43h ADCTRIG67 - EPWM29, ADCSOCA<br/> 44h ADCTRIG68 - EPWM30, ADCSOCA<br/> 45h ADCTRIG69 - EPWM30, ADCSOCA<br/> 46h ADCTRIG70 - EPWM31, ADCSOCA<br/> 47h ADCTRIG71 - EPWM31, ADCSOCA<br/> 48h ADCTRIG72 - ECAP0, TRIGOUT<br/> .... ECAP1 to ECAP8<br/> 51h ADCTRIG81 - ECAP9, TRIGOUT<br/> 52h ADCTRIG82 - ECAP10, TRIGOUT<br/> ....<br/> 57h ADCTRIG87 - ECAP15, TRIGOUT<br/> 58h ADCTRIG88 - RTI4 Timer<br/> 59h ADCTRIG89 - RTI5 Timer<br/> 5Ah ADCTRIG90 - RTI6 Timer<br/> 5Bh ADCTRIG91 - RTI7 Timer<br/> ....<br/> 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.</p> |
| 19:15 | CHSEL      | R/W  | 0h    | <p>SOC0 Channel Select. Selects the channel to be converted when SOC0 is received by the ADC.</p> <p>Single-ended Signaling Mode [SIGNALMODE = 0]:<br/> 00h ADCIN0<br/> 01h ADCIN1<br/> 02h ADCIN2<br/> 03h ADCIN3<br/> 04h ADCIN4<br/> 05h ADCIN5<br/> Differential Signaling Mode [SIGNALMODE = 1]:<br/> 00h ADCIN0 [non-inverting] and ADCIN1 [inverting]<br/> 01h ADCIN0 [non-inverting] and ADCIN1 [inverting]<br/> 02h ADCIN2 [non-inverting] and ADCIN3 [inverting]<br/> 03h ADCIN2 [non-inverting] and ADCIN3 [inverting]<br/> 04h ADCIN4 [non-inverting] and ADCIN5 [inverting]<br/> 05h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 14:12 | RESOLUTION | R    | 0h    | Placeholder for per-SOC resolution                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 11:10 | SIGNALMODE | R    | 0h    | Placeholder for per-SOC signal mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |



**Table 3-187. ADC\_CFG\_ADCSOC0CTL Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-----|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9   | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 8:0 | ACQPS      | R/W  | 0h    | <p>SOC0 Acquisition Prescale. Controls the sample and hold window for this SOC.</p> <p>000h Reserved</p> <p>001h Reserved</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>003h Sample window is 4 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p> <p>The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.</p> |

### 3.2.2.62 ADC\_CFG\_ADCSOC1CTL Register

#### 1 ADC\_CFG\_ADCSOC1CTL Register (Offset = 24h) [reset = 0h]

ADC SOC1 Control Register.

Return to [Summary Table](#)

**Table 3-188. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0024h       |
| ADC1_G0_G5    | 502C 1024h       |
| ADC2_G0_G5    | 502C 2024h       |
| ADC3_G0_G5    | 502C 3024h       |
| ADC4_G0_G5    | 502C 4024h       |

**Figure 3-62. ADC\_CFG\_ADCSOC1CTL Name Register**

|          |            |    |    |            |         |            |       |
|----------|------------|----|----|------------|---------|------------|-------|
| 31       | 30         | 29 | 28 | 27         | 26      | 25         | 24    |
| EXTCHSEL |            |    |    | RESERVED_2 | TRIGSEL |            |       |
| R/W      |            |    |    | R          | R/W     |            |       |
| 0h       |            |    |    | 0h         | 0h      |            |       |
| 23       | 22         | 21 | 20 | 19         | 18      | 17         | 16    |
| TRIGSEL  |            |    |    | CHSEL      |         |            |       |
| R/W      |            |    |    | R/W        |         |            |       |
| 0h       |            |    |    | 0h         |         |            |       |
| 15       | 14         | 13 | 12 | 11         | 10      | 9          | 8     |
| CHSEL    | RESOLUTION |    |    | SIGNALMODE |         | RESERVED_1 | ACQPS |
| R/W      | R          |    |    | R          |         | R          | R/W   |
| 0h       | 0h         |    |    | 0h         |         | 0h         | 0h    |
| 7        | 6          | 5  | 4  | 3          | 2       | 1          | 0     |
| ACQPS    |            |    |    |            |         |            |       |
| R/W      |            |    |    |            |         |            |       |
| 0h       |            |    |    |            |         |            |       |

**Table 3-190. ADC\_CFG\_ADCSOC1CTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                     |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28 | EXTCHSEL   | R/W  | 0h    | SOC1 External Channel Mux Select. Selects the external mux combination to output when SOC1 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. |
| 27    | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                        |

**Table 3-190. ADC\_CFG\_ADCSOC1CTL Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:20 | TRIGSEL    | R/W  | 0h    | <p>SOC1 Trigger Source Select. Along with the SOC1 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC1 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it.</p> <p>Note: SOCFRC1 register can always be used to software trigger SOC1s in addition to any hardware trigger configuration.</p> <p>00h ADCTRIG0 - Software only<br/> 01h ADCTRIG1 - RTI0 Timer<br/> 02h ADCTRIG2 - RTI1 Timer<br/> 03h ADCTRIG3 - RTI2 Timer<br/> 04h ADCTRIG4 - RTI3 Timer<br/> 05h ADCTRIG5 - InputXBAR.Out[5]<br/> 06h ADCTRIG6 - spare<br/> 07h ADCTRIG7 - spare<br/> 08h ADCTRIG8 - EPWM0, ADCSOCA<br/> 09h ADCTRIG9 - EPWM0, ADCSOCB<br/> 0Ah ADCTRIG10 - EPWM1, ADCSOCA<br/> 0Bh ADCTRIG11 - EPWM1, ADCSOCB<br/> 0Ch ADCTRIG12 - EPWM2, ADCSOCA<br/> 0Dh ADCTRIG13 - EPWM2, ADCSOCB<br/> 0Eh ADCTRIG14 - EPWM3, ADCSOCA<br/> 0Fh ADCTRIG15 - EPWM3, ADCSOCB<br/> .... EPWM4 to EPWM27<br/> 40h ADCTRIG64 - EPWM28, ADCSOCA<br/> 41h ADCTRIG65 - EPWM28, ADCSOCB<br/> 42h ADCTRIG66 - EPWM29, ADCSOCA<br/> 43h ADCTRIG67 - EPWM29, ADCSOCB<br/> 44h ADCTRIG68 - EPWM30, ADCSOCA<br/> 45h ADCTRIG69 - EPWM30, ADCSOCB<br/> 46h ADCTRIG70 - EPWM31, ADCSOCA<br/> 47h ADCTRIG71 - EPWM31, ADCSOCB<br/> 48h ADCTRIG72 - ECAP0, TRIGOUT<br/> .... ECAP1 to ECAP8<br/> 51h ADCTRIG81 - ECAP9, TRIGOUT<br/> 52h ADCTRIG82 - ECAP10, TRIGOUT<br/> ....<br/> 57h ADCTRIG87 - ECAP15, TRIGOUT<br/> 58h ADCTRIG88 - RTI4 Timer<br/> 59h ADCTRIG89 - RTI5 Timer<br/> 5Ah ADCTRIG90 - RTI6 Timer<br/> 5Bh ADCTRIG91 - RTI7 Timer<br/> ....<br/> 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.</p> |
| 19:15 | CHSEL      | R/W  | 0h    | <p>SOC1 Channel Select. Selects the channel to be converted when SOC1 is received by the ADC.</p> <p>Single-ended Signaling Mode [SIGNALMODE = 0]:<br/> 00h: ADCIN0<br/> 01h: ADCIN1<br/> 02h: ADCIN2<br/> 03h: ADCIN3<br/> 04h: ADCIN4<br/> 05h: ADCIN5<br/> Differential Signaling Mode [SIGNALMODE = 1]:<br/> 00h: ADCIN0 [non-inverting] and ADCIN1 [inverting]<br/> 01h: ADCIN0 [non-inverting] and ADCIN1 [inverting]<br/> 02h: ADCIN2 [non-inverting] and ADCIN3 [inverting]<br/> 03h: ADCIN2 [non-inverting] and ADCIN3 [inverting]<br/> 04h: ADCIN4 [non-inverting] and ADCIN5 [inverting]<br/> 05h: ADCIN4 [non-inverting] and ADCIN5 [inverting]</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 14:12 | RESOLUTION | R    | 0h    | Placeholder for per-SOC resolution                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 11:10 | SIGNALMODE | R    | 0h    | Placeholder for per-SOC signal mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

**Table 3-190. ADC\_CFG\_ADCSOC1CTL Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-----|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9   | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 8:0 | ACQPS      | R/W  | 0h    | <p>SOC1 Acquisition Prescale. Controls the sample and hold window for this SOC.</p> <p>000h Reserved</p> <p>001h Reserved</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>003h Sample window is 4 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p> <p>The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.</p> |

### 3.2.2.63 ADC\_CFG\_ADCSOC2CTL Register

#### 1 ADC\_CFG\_ADCSOC2CTL Register (Offset = 28h) [reset = 0h]

ADC SOC2 Control Register.

Return to [Summary Table](#)

**Table 3-191. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0028h       |
| ADC1_G0_G5    | 502C 1028h       |
| ADC2_G0_G5    | 502C 2028h       |
| ADC3_G0_G5    | 502C 3028h       |
| ADC4_G0_G5    | 502C 4028h       |

**Figure 3-63. ADC\_CFG\_ADCSOC2CTL Name Register**

|          |            |    |    |            |         |            |       |
|----------|------------|----|----|------------|---------|------------|-------|
| 31       | 30         | 29 | 28 | 27         | 26      | 25         | 24    |
| EXTCHSEL |            |    |    | RESERVED_2 | TRIGSEL |            |       |
| R/W      |            |    |    | R          | R/W     |            |       |
| 0h       |            |    |    | 0h         | 0h      |            |       |
| 23       | 22         | 21 | 20 | 19         | 18      | 17         | 16    |
| TRIGSEL  |            |    |    | CHSEL      |         |            |       |
| R/W      |            |    |    | R/W        |         |            |       |
| 0h       |            |    |    | 0h         |         |            |       |
| 15       | 14         | 13 | 12 | 11         | 10      | 9          | 8     |
| CHSEL    | RESOLUTION |    |    | SIGNALMODE |         | RESERVED_1 | ACQPS |
| R/W      | R          |    |    | R          |         | R          | R/W   |
| 0h       | 0h         |    |    | 0h         |         | 0h         | 0h    |
| 7        | 6          | 5  | 4  | 3          | 2       | 1          | 0     |
| ACQPS    |            |    |    |            |         |            |       |
| R/W      |            |    |    |            |         |            |       |
| 0h       |            |    |    |            |         |            |       |

**Table 3-193. ADC\_CFG\_ADCSOC2CTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                     |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28 | EXTCHSEL   | R/W  | 0h    | SOC2 External Channel Mux Select. Selects the external mux combination to output when SOC2 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. |
| 27    | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                        |

**Table 3-193. ADC\_CFG\_ADCSOC2CTL Register Field Descriptions (continued)**

| Bit   | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|---------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:20 | TRIGSEL | R/W  | 0h    | <p>SOC2 Trigger Source Select. Along with the SOC2 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC2 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it.</p> <p>Note: SOCFRC1 register can always be used to software trigger SOC2s in addition to any hardware trigger configuration.</p> <p>00h ADCTRIG0 - Software only<br/> 01h ADCTRIG1 - RTI0 Timer<br/> 02h ADCTRIG2 - RTI1 Timer<br/> 03h ADCTRIG3 - RTI2 Timer<br/> 04h ADCTRIG4 - RTI3 Timer<br/> 05h ADCTRIG5 - InputXBAR.Out[5]<br/> 06h ADCTRIG6 - spare<br/> 07h ADCTRIG7 - spare<br/> 08h ADCTRIG8 - EPWM0, ADCSOCA<br/> 09h ADCTRIG9 - EPWM0, ADCSOCB<br/> 0Ah ADCTRIG10 - EPWM1, ADCSOCA<br/> 0Bh ADCTRIG11 - EPWM1, ADCSOCB<br/> 0Ch ADCTRIG12 - EPWM2, ADCSOCA<br/> 0Dh ADCTRIG13 - EPWM2, ADCSOCB<br/> 0Eh ADCTRIG14 - EPWM3, ADCSOCA<br/> 0Fh ADCTRIG15 - EPWM3, ADCSOCB<br/> .... EPWM4 to EPWM27<br/> 40h ADCTRIG64 - EPWM28, ADCSOCA<br/> 41h ADCTRIG65 - EPWM28, ADCSOCB<br/> 42h ADCTRIG66 - EPWM29, ADCSOCA<br/> 43h ADCTRIG67 - EPWM29, ADCSOCB<br/> 44h ADCTRIG68 - EPWM30, ADCSOCA<br/> 45h ADCTRIG69 - EPWM30, ADCSOCB<br/> 46h ADCTRIG70 - EPWM31, ADCSOCA<br/> 47h ADCTRIG71 - EPWM31, ADCSOCB<br/> 48h ADCTRIG72 - ECAP0, TRIGOUT<br/> .... ECAP1 to ECAP8<br/> 51h ADCTRIG81 - ECAP9, TRIGOUT<br/> 52h ADCTRIG82 - ECAP10, TRIGOUT<br/> ....<br/> 57h ADCTRIG87 - ECAP15, TRIGOUT<br/> 58h ADCTRIG88 - RTI4 Timer<br/> 59h ADCTRIG89 - RTI5 Timer<br/> 5Ah ADCTRIG90 - RTI6 Timer<br/> 5Bh ADCTRIG91 - RTI7 Timer<br/> ....<br/> 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.</p> |

**Table 3-193. ADC\_CFG\_ADCSOC2CTL Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19:15 | CHSEL      | R/W  | 0h    | <p>SOC2 Channel Select. Selects the channel to be converted when SOC2 is received by the ADC.</p> <p>Single-ended Signaling Mode [SIGNALMODE = 0]:</p> <p>00h ADCIN0</p> <p>01h ADCIN1</p> <p>02h ADCIN2</p> <p>03h ADCIN3</p> <p>...</p> <p>1Dh ADCIN29</p> <p>1Eh ADCIN30</p> <p>1Fh ADCIN31</p> <p>Differential Signaling Mode [SIGNALMODE = 1]:</p> <p>00h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>01h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>02h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>03h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>04h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>05h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>...</p> <p>0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>10h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>11h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> <p>1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> |
| 14:12 | RESOLUTION | R    | 0h    | Placeholder for per-SOC resolution                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 11:10 | SIGNALMODE | R    | 0h    | Placeholder for per-SOC signal mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 9     | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 8:0   | ACQPS      | R/W  | 0h    | <p>SOC2 Acquisition Prescale. Controls the sample and hold window for this SOC.</p> <p>000h Reserved</p> <p>001h Reserved</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>003h Sample window is 4 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p> <p>The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

### 3.2.2.64 ADC\_CFG\_ADCSOC3CTL Register

#### 1 ADC\_CFG\_ADCSOC3CTL Register (Offset = 2Ch) [reset = 0h]

ADC SOC3 Control Register.

Return to [Summary Table](#)

**Table 3-194. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 002Ch       |
| ADC1_G0_G5    | 502C 102Ch       |
| ADC2_G0_G5    | 502C 202Ch       |
| ADC3_G0_G5    | 502C 302Ch       |
| ADC4_G0_G5    | 502C 402Ch       |

**Figure 3-64. ADC\_CFG\_ADCSOC3CTL Name Register**

|          |            |    |    |            |         |            |       |
|----------|------------|----|----|------------|---------|------------|-------|
| 31       | 30         | 29 | 28 | 27         | 26      | 25         | 24    |
| EXTCHSEL |            |    |    | RESERVED_2 | TRIGSEL |            |       |
| R/W      |            |    |    | R          | R/W     |            |       |
| 0h       |            |    |    | 0h         | 0h      |            |       |
| 23       | 22         | 21 | 20 | 19         | 18      | 17         | 16    |
| TRIGSEL  |            |    |    | CHSEL      |         |            |       |
| R/W      |            |    |    | R/W        |         |            |       |
| 0h       |            |    |    | 0h         |         |            |       |
| 15       | 14         | 13 | 12 | 11         | 10      | 9          | 8     |
| CHSEL    | RESOLUTION |    |    | SIGNALMODE |         | RESERVED_1 | ACQPS |
| R/W      | R          |    |    | R          |         | R          | R/W   |
| 0h       | 0h         |    |    | 0h         |         | 0h         | 0h    |
| 7        | 6          | 5  | 4  | 3          | 2       | 1          | 0     |
| ACQPS    |            |    |    |            |         |            |       |
| R/W      |            |    |    |            |         |            |       |
| 0h       |            |    |    |            |         |            |       |

**Table 3-196. ADC\_CFG\_ADCSOC3CTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                     |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28 | EXTCHSEL   | R/W  | 0h    | SOC3 External Channel Mux Select. Selects the external mux combination to output when SOC3 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. |
| 27    | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                        |



**Table 3-196. ADC\_CFG\_ADCSOC3CTL Register Field Descriptions (continued)**

| Bit   | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|---------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:20 | TRIGSEL | R/W  | 0h    | <p>SOC3 Trigger Source Select. Along with the SOC3 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC3 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it.</p> <p>Note: SOCFRC1 register can always be used to software trigger SOC3 in addition to any hardware trigger configuration.</p> <p>00h ADCTRIG0 - Software only<br/> 01h ADCTRIG1 - RTI0 Timer<br/> 02h ADCTRIG2 - RTI1 Timer<br/> 03h ADCTRIG3 - RTI2 Timer<br/> 04h ADCTRIG4 - RTI3 Timer<br/> 05h ADCTRIG5 - InputXBAR.Out[5]<br/> 06h ADCTRIG6 - spare<br/> 07h ADCTRIG7 - spare<br/> 08h ADCTRIG8 - EPWM0, ADCSOCA<br/> 09h ADCTRIG9 - EPWM0, ADCSOCB<br/> 0Ah ADCTRIG10 - EPWM1, ADCSOCA<br/> 0Bh ADCTRIG11 - EPWM1, ADCSOCB<br/> 0Ch ADCTRIG12 - EPWM2, ADCSOCA<br/> 0Dh ADCTRIG13 - EPWM2, ADCSOCB<br/> 0Eh ADCTRIG14 - EPWM3, ADCSOCA<br/> 0Fh ADCTRIG15 - EPWM3, ADCSOCB<br/> .... EPWM4 to EPWM27<br/> 40h ADCTRIG64 - EPWM28, ADCSOCA<br/> 41h ADCTRIG65 - EPWM28, ADCSOCB<br/> 42h ADCTRIG66 - EPWM29, ADCSOCA<br/> 43h ADCTRIG67 - EPWM29, ADCSOCB<br/> 44h ADCTRIG68 - EPWM30, ADCSOCA<br/> 45h ADCTRIG69 - EPWM30, ADCSOCB<br/> 46h ADCTRIG70 - EPWM31, ADCSOCA<br/> 47h ADCTRIG71 - EPWM31, ADCSOCB<br/> 48h ADCTRIG72 - ECAP0, TRIGOUT<br/> .... ECAP1 to ECAP8<br/> 51h ADCTRIG81 - ECAP9, TRIGOUT<br/> 52h ADCTRIG82 - ECAP10, TRIGOUT<br/> ....<br/> 57h ADCTRIG87 - ECAP15, TRIGOUT<br/> 58h ADCTRIG88 - RTI4 Timer<br/> 59h ADCTRIG89 - RTI5 Timer<br/> 5Ah ADCTRIG90 - RTI6 Timer<br/> 5Bh ADCTRIG91 - RTI7 Timer<br/> ....<br/> 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.</p> |

**Table 3-196. ADC\_CFG\_ADCSOC3CTL Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19:15 | CHSEL      | R/W  | 0h    | <p>SOC3 Channel Select. Selects the channel to be converted when SOC3 is received by the ADC.</p> <p>Single-ended Signaling Mode [SIGNALMODE = 0]:</p> <p>00h ADCIN0</p> <p>01h ADCIN1</p> <p>02h ADCIN2</p> <p>03h ADCIN3</p> <p>...</p> <p>1Dh ADCIN29</p> <p>1Eh ADCIN30</p> <p>1Fh ADCIN31</p> <p>Differential Signaling Mode [SIGNALMODE = 1]:</p> <p>00h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>01h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>02h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>03h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>04h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>05h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>...</p> <p>0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>10h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>11h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> <p>1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> |
| 14:12 | RESOLUTION | R    | 0h    | Placeholder for per-SOC resolution                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 11:10 | SIGNALMODE | R    | 0h    | Placeholder for per-SOC signal mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 9     | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 8:0   | ACQPS      | R/W  | 0h    | <p>SOC3 Acquisition Prescale. Controls the sample and hold window for this SOC.</p> <p>000h Reserved</p> <p>001h Reserved</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>003h Sample window is 4 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p> <p>The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

### 3.2.2.65 ADC\_CFG\_ADCSOC4CTL Register

#### 1 ADC\_CFG\_ADCSOC4CTL Register (Offset = 30h) [reset = 0h]

ADC SOC4 Control Register.

Return to [Summary Table](#)

**Table 3-197. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0030h       |
| ADC1_G0_G5    | 502C 1030h       |
| ADC2_G0_G5    | 502C 2030h       |
| ADC3_G0_G5    | 502C 3030h       |
| ADC4_G0_G5    | 502C 4030h       |

**Figure 3-65. ADC\_CFG\_ADCSOC4CTL Name Register**

|          |            |    |    |            |         |            |       |
|----------|------------|----|----|------------|---------|------------|-------|
| 31       | 30         | 29 | 28 | 27         | 26      | 25         | 24    |
| EXTCHSEL |            |    |    | RESERVED_2 | TRIGSEL |            |       |
| R/W      |            |    |    | R          | R/W     |            |       |
| 0h       |            |    |    | 0h         | 0h      |            |       |
| 23       | 22         | 21 | 20 | 19         | 18      | 17         | 16    |
| TRIGSEL  |            |    |    | CHSEL      |         |            |       |
| R/W      |            |    |    | R/W        |         |            |       |
| 0h       |            |    |    | 0h         |         |            |       |
| 15       | 14         | 13 | 12 | 11         | 10      | 9          | 8     |
| CHSEL    | RESOLUTION |    |    | SIGNALMODE |         | RESERVED_1 | ACQPS |
| R/W      | R          |    |    | R          |         | R          | R/W   |
| 0h       | 0h         |    |    | 0h         |         | 0h         | 0h    |
| 7        | 6          | 5  | 4  | 3          | 2       | 1          | 0     |
| ACQPS    |            |    |    |            |         |            |       |
| R/W      |            |    |    |            |         |            |       |
| 0h       |            |    |    |            |         |            |       |

**Table 3-199. ADC\_CFG\_ADCSOC4CTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                     |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28 | EXTCHSEL   | R/W  | 0h    | SOC4 External Channel Mux Select. Selects the external mux combination to output when SOC4 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. |
| 27    | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                        |

**Table 3-199. ADC\_CFG\_ADCSOC4CTL Register Field Descriptions (continued)**

| Bit   | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|---------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:20 | TRIGSEL | R/W  | 0h    | <p>SOC4 Trigger Source Select. Along with the SOC4 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC4 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it.</p> <p>Note: SOCFRC1 register can always be used to software trigger SOC4s in addition to any hardware trigger configuration.</p> <p>00h ADCTRIG0 - Software only<br/> 01h ADCTRIG1 - RTI0 Timer<br/> 02h ADCTRIG2 - RTI1 Timer<br/> 03h ADCTRIG3 - RTI2 Timer<br/> 04h ADCTRIG4 - RTI3 Timer<br/> 05h ADCTRIG5 - InputXBAR.Out[5]<br/> 06h ADCTRIG6 - spare<br/> 07h ADCTRIG7 - spare<br/> 08h ADCTRIG8 - EPWM0, ADCSOCA<br/> 09h ADCTRIG9 - EPWM0, ADCSOCB<br/> 0Ah ADCTRIG10 - EPWM1, ADCSOCA<br/> 0Bh ADCTRIG11 - EPWM1, ADCSOCB<br/> 0Ch ADCTRIG12 - EPWM2, ADCSOCA<br/> 0Dh ADCTRIG13 - EPWM2, ADCSOCB<br/> 0Eh ADCTRIG14 - EPWM3, ADCSOCA<br/> 0Fh ADCTRIG15 - EPWM3, ADCSOCB<br/> .... EPWM4 to EPWM27<br/> 40h ADCTRIG64 - EPWM28, ADCSOCA<br/> 41h ADCTRIG65 - EPWM28, ADCSOCB<br/> 42h ADCTRIG66 - EPWM29, ADCSOCA<br/> 43h ADCTRIG67 - EPWM29, ADCSOCB<br/> 44h ADCTRIG68 - EPWM30, ADCSOCA<br/> 45h ADCTRIG69 - EPWM30, ADCSOCB<br/> 46h ADCTRIG70 - EPWM31, ADCSOCA<br/> 47h ADCTRIG71 - EPWM31, ADCSOCB<br/> 48h ADCTRIG72 - ECAP0, TRIGOUT<br/> .... ECAP1 to ECAP8<br/> 51h ADCTRIG81 - ECAP9, TRIGOUT<br/> 52h ADCTRIG82 - ECAP10, TRIGOUT<br/> ....<br/> 57h ADCTRIG87 - ECAP15, TRIGOUT<br/> 58h ADCTRIG88 - RTI4 Timer<br/> 59h ADCTRIG89 - RTI5 Timer<br/> 5Ah ADCTRIG90 - RTI6 Timer<br/> 5Bh ADCTRIG91 - RTI7 Timer<br/> ....<br/> 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.</p> |

**Table 3-199. ADC\_CFG\_ADCSOC4CTL Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19:15 | CHSEL      | R/W  | 0h    | <p>SOC4 Channel Select. Selects the channel to be converted when SOC4 is received by the ADC.</p> <p>Single-ended Signaling Mode [SIGNALMODE = 0]:</p> <p>00h ADCIN0</p> <p>01h ADCIN1</p> <p>02h ADCIN2</p> <p>03h ADCIN3</p> <p>...</p> <p>1Dh ADCIN29</p> <p>1Eh ADCIN30</p> <p>1Fh ADCIN31</p> <p>Differential Signaling Mode [SIGNALMODE = 1]:</p> <p>00h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>01h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>02h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>03h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>04h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>05h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>...</p> <p>0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>10h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>11h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> <p>1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> |
| 14:12 | RESOLUTION | R    | 0h    | Placeholder for per-SOC resolution                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 11:10 | SIGNALMODE | R    | 0h    | Placeholder for per-SOC signal mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 9     | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 8:0   | ACQPS      | R/W  | 0h    | <p>SOC4 Acquisition Prescale. Controls the sample and hold window for this SOC.</p> <p>000h Reserved</p> <p>001h Reserved</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>003h Sample window is 4 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p> <p>The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

### 3.2.2.66 ADC\_CFG\_ADCSOC5CTL Register

#### 1 ADC\_CFG\_ADCSOC5CTL Register (Offset = 34h) [reset = 0h]

ADC SOC5 Control Register.

Return to [Summary Table](#)

**Table 3-200. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0034h       |
| ADC1_G0_G5    | 502C 1034h       |
| ADC2_G0_G5    | 502C 2034h       |
| ADC3_G0_G5    | 502C 3034h       |
| ADC4_G0_G5    | 502C 4034h       |

**Figure 3-66. ADC\_CFG\_ADCSOC5CTL Name Register**

|          |            |    |    |            |         |            |       |
|----------|------------|----|----|------------|---------|------------|-------|
| 31       | 30         | 29 | 28 | 27         | 26      | 25         | 24    |
| EXTCHSEL |            |    |    | RESERVED_2 | TRIGSEL |            |       |
| R/W      |            |    |    | R          | R/W     |            |       |
| 0h       |            |    |    | 0h         | 0h      |            |       |
| 23       | 22         | 21 | 20 | 19         | 18      | 17         | 16    |
| TRIGSEL  |            |    |    | CHSEL      |         |            |       |
| R/W      |            |    |    | R/W        |         |            |       |
| 0h       |            |    |    | 0h         |         |            |       |
| 15       | 14         | 13 | 12 | 11         | 10      | 9          | 8     |
| CHSEL    | RESOLUTION |    |    | SIGNALMODE |         | RESERVED_1 | ACQPS |
| R/W      | R          |    |    | R          |         | R          | R/W   |
| 0h       | 0h         |    |    | 0h         |         | 0h         | 0h    |
| 7        | 6          | 5  | 4  | 3          | 2       | 1          | 0     |
| ACQPS    |            |    |    |            |         |            |       |
| R/W      |            |    |    |            |         |            |       |
| 0h       |            |    |    |            |         |            |       |

**Table 3-202. ADC\_CFG\_ADCSOC5CTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                     |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28 | EXTCHSEL   | R/W  | 0h    | SOC5 External Channel Mux Select. Selects the external mux combination to output when SOC5 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. |
| 27    | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                        |

**Table 3-202. ADC\_CFG\_ADCSOC5CTL Register Field Descriptions (continued)**

| Bit   | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|---------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:20 | TRIGSEL | R/W  | 0h    | <p>SOC5 Trigger Source Select. Along with the SOC5 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC5 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it.</p> <p>Note: SOCFRC1 register can always be used to software trigger SOC5s in addition to any hardware trigger configuration.</p> <p>00h ADCTRIG0 - Software only<br/> 01h ADCTRIG1 - RTI0 Timer<br/> 02h ADCTRIG2 - RTI1 Timer<br/> 03h ADCTRIG3 - RTI2 Timer<br/> 04h ADCTRIG4 - RTI3 Timer<br/> 05h ADCTRIG5 - InputXBAR.Out[5]<br/> 06h ADCTRIG6 - spare<br/> 07h ADCTRIG7 - spare<br/> 08h ADCTRIG8 - EPWM0, ADCSOCA<br/> 09h ADCTRIG9 - EPWM0, ADCSOCB<br/> 0Ah ADCTRIG10 - EPWM1, ADCSOCA<br/> 0Bh ADCTRIG11 - EPWM1, ADCSOCB<br/> 0Ch ADCTRIG12 - EPWM2, ADCSOCA<br/> 0Dh ADCTRIG13 - EPWM2, ADCSOCB<br/> 0Eh ADCTRIG14 - EPWM3, ADCSOCA<br/> 0Fh ADCTRIG15 - EPWM3, ADCSOCB<br/> .... EPWM4 to EPWM27<br/> 40h ADCTRIG64 - EPWM28, ADCSOCA<br/> 41h ADCTRIG65 - EPWM28, ADCSOCB<br/> 42h ADCTRIG66 - EPWM29, ADCSOCA<br/> 43h ADCTRIG67 - EPWM29, ADCSOCB<br/> 44h ADCTRIG68 - EPWM30, ADCSOCA<br/> 45h ADCTRIG69 - EPWM30, ADCSOCB<br/> 46h ADCTRIG70 - EPWM31, ADCSOCA<br/> 47h ADCTRIG71 - EPWM31, ADCSOCB<br/> 48h ADCTRIG72 - ECAP0, TRIGOUT<br/> .... ECAP1 to ECAP8<br/> 51h ADCTRIG81 - ECAP9, TRIGOUT<br/> 52h ADCTRIG82 - ECAP10, TRIGOUT<br/> ....<br/> 57h ADCTRIG87 - ECAP15, TRIGOUT<br/> 58h ADCTRIG88 - RTI4 Timer<br/> 59h ADCTRIG89 - RTI5 Timer<br/> 5Ah ADCTRIG90 - RTI6 Timer<br/> 5Bh ADCTRIG91 - RTI7 Timer<br/> ....<br/> 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.</p> |

**Table 3-202. ADC\_CFG\_ADCSOC5CTL Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19:15 | CHSEL      | R/W  | 0h    | <p>SOC5 Channel Select. Selects the channel to be converted when SOC5 is received by the ADC.</p> <p>Single-ended Signaling Mode [SIGNALMODE = 0]:</p> <p>00h ADCIN0</p> <p>01h ADCIN1</p> <p>02h ADCIN2</p> <p>03h ADCIN3</p> <p>...</p> <p>1Dh ADCIN29</p> <p>1Eh ADCIN30</p> <p>1Fh ADCIN31</p> <p>Differential Signaling Mode [SIGNALMODE = 1]:</p> <p>00h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>01h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>02h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>03h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>04h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>05h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>...</p> <p>0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>10h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>11h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> <p>1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> |
| 14:12 | RESOLUTION | R    | 0h    | Placeholder for per-SOC resolution                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 11:10 | SIGNALMODE | R    | 0h    | Placeholder for per-SOC signal mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 9     | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 8:0   | ACQPS      | R/W  | 0h    | <p>SOC5 Acquisition Prescale. Controls the sample and hold window for this SOC.</p> <p>000h Reserved</p> <p>001h Reserved</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>003h Sample window is 4 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p> <p>The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |



### 3.2.2.67 ADC\_CFG\_ADCSOC6CTL Register

#### 1 ADC\_CFG\_ADCSOC6CTL Register (Offset = 38h) [reset = 0h]

ADC SOC6 Control Register.

Return to [Summary Table](#)

**Table 3-203. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0038h       |
| ADC1_G0_G5    | 502C 1038h       |
| ADC2_G0_G5    | 502C 2038h       |
| ADC3_G0_G5    | 502C 3038h       |
| ADC4_G0_G5    | 502C 4038h       |

**Figure 3-67. ADC\_CFG\_ADCSOC6CTL Name Register**

|          |            |    |    |            |         |            |       |
|----------|------------|----|----|------------|---------|------------|-------|
| 31       | 30         | 29 | 28 | 27         | 26      | 25         | 24    |
| EXTCHSEL |            |    |    | RESERVED_2 | TRIGSEL |            |       |
| R/W      |            |    |    | R          | R/W     |            |       |
| 0h       |            |    |    | 0h         | 0h      |            |       |
| 23       | 22         | 21 | 20 | 19         | 18      | 17         | 16    |
| TRIGSEL  |            |    |    | CHSEL      |         |            |       |
| R/W      |            |    |    | R/W        |         |            |       |
| 0h       |            |    |    | 0h         |         |            |       |
| 15       | 14         | 13 | 12 | 11         | 10      | 9          | 8     |
| CHSEL    | RESOLUTION |    |    | SIGNALMODE |         | RESERVED_1 | ACQPS |
| R/W      | R          |    |    | R          |         | R          | R/W   |
| 0h       | 0h         |    |    | 0h         |         | 0h         | 0h    |
| 7        | 6          | 5  | 4  | 3          | 2       | 1          | 0     |
| ACQPS    |            |    |    |            |         |            |       |
| R/W      |            |    |    |            |         |            |       |
| 0h       |            |    |    |            |         |            |       |

**Table 3-205. ADC\_CFG\_ADCSOC6CTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                     |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28 | EXTCHSEL   | R/W  | 0h    | SOC6 External Channel Mux Select. Selects the external mux combination to output when SOC6 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. |
| 27    | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                        |

**Table 3-205. ADC\_CFG\_ADCSOC6CTL Register Field Descriptions (continued)**

| Bit   | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|---------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:20 | TRIGSEL | R/W  | 0h    | <p>SOC6 Trigger Source Select. Along with the SOC6 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC6 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it.</p> <p>Note: SOCFRC1 register can always be used to software trigger SOC6 in addition to any hardware trigger configuration.</p> <p>00h ADCTRIG0 - Software only<br/> 01h ADCTRIG1 - RTI0 Timer<br/> 02h ADCTRIG2 - RTI1 Timer<br/> 03h ADCTRIG3 - RTI2 Timer<br/> 04h ADCTRIG4 - RTI3 Timer<br/> 05h ADCTRIG5 - InputXBAR.Out[5]<br/> 06h ADCTRIG6 - spare<br/> 07h ADCTRIG7 - spare<br/> 08h ADCTRIG8 - EPWM0, ADCSOCA<br/> 09h ADCTRIG9 - EPWM0, ADCSOCB<br/> 0Ah ADCTRIG10 - EPWM1, ADCSOCA<br/> 0Bh ADCTRIG11 - EPWM1, ADCSOCB<br/> 0Ch ADCTRIG12 - EPWM2, ADCSOCA<br/> 0Dh ADCTRIG13 - EPWM2, ADCSOCB<br/> 0Eh ADCTRIG14 - EPWM3, ADCSOCA<br/> 0Fh ADCTRIG15 - EPWM3, ADCSOCB<br/> .... EPWM4 to EPWM27<br/> 40h ADCTRIG64 - EPWM28, ADCSOCA<br/> 41h ADCTRIG65 - EPWM28, ADCSOCB<br/> 42h ADCTRIG66 - EPWM29, ADCSOCA<br/> 43h ADCTRIG67 - EPWM29, ADCSOCB<br/> 44h ADCTRIG68 - EPWM30, ADCSOCA<br/> 45h ADCTRIG69 - EPWM30, ADCSOCB<br/> 46h ADCTRIG70 - EPWM31, ADCSOCA<br/> 47h ADCTRIG71 - EPWM31, ADCSOCB<br/> 48h ADCTRIG72 - ECAP0, TRIGOUT<br/> .... ECAP1 to ECAP8<br/> 51h ADCTRIG81 - ECAP9, TRIGOUT<br/> 52h ADCTRIG82 - ECAP10, TRIGOUT<br/> ....<br/> 57h ADCTRIG87 - ECAP15, TRIGOUT<br/> 58h ADCTRIG88 - RTI4 Timer<br/> 59h ADCTRIG89 - RTI5 Timer<br/> 5Ah ADCTRIG90 - RTI6 Timer<br/> 5Bh ADCTRIG91 - RTI7 Timer<br/> ....<br/> 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.</p> |

**Table 3-205. ADC\_CFG\_ADCSOC6CTL Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19:15 | CHSEL      | R/W  | 0h    | <p>SOC6 Channel Select. Selects the channel to be converted when SOC6 is received by the ADC.</p> <p>Single-ended Signaling Mode [SIGNALMODE = 0]:</p> <p>00h ADCIN0</p> <p>01h ADCIN1</p> <p>02h ADCIN2</p> <p>03h ADCIN3</p> <p>...</p> <p>1Dh ADCIN29</p> <p>1Eh ADCIN30</p> <p>1Fh ADCIN31</p> <p>Differential Signaling Mode [SIGNALMODE = 1]:</p> <p>00h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>01h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>02h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>03h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>04h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>05h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>...</p> <p>0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>10h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>11h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> <p>1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> |
| 14:12 | RESOLUTION | R    | 0h    | Placeholder for per-SOC resolution                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 11:10 | SIGNALMODE | R    | 0h    | Placeholder for per-SOC signal mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 9     | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 8:0   | ACQPS      | R/W  | 0h    | <p>SOC6 Acquisition Prescale. Controls the sample and hold window for this SOC.</p> <p>000h Reserved</p> <p>001h Reserved</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>003h Sample window is 4 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p> <p>The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

### 3.2.2.68 ADC\_CFG\_ADCSOC7CTL Register

#### 1 ADC\_CFG\_ADCSOC7CTL Register (Offset = 3Ch) [reset = 0h]

ADC SOC7 Control Register.

Return to [Summary Table](#)

**Table 3-206. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 003Ch       |
| ADC1_G0_G5    | 502C 103Ch       |
| ADC2_G0_G5    | 502C 203Ch       |
| ADC3_G0_G5    | 502C 303Ch       |
| ADC4_G0_G5    | 502C 403Ch       |

**Figure 3-68. ADC\_CFG\_ADCSOC7CTL Name Register**

|          |            |    |    |            |         |            |       |
|----------|------------|----|----|------------|---------|------------|-------|
| 31       | 30         | 29 | 28 | 27         | 26      | 25         | 24    |
| EXTCHSEL |            |    |    | RESERVED_2 | TRIGSEL |            |       |
| R/W      |            |    |    | R          | R/W     |            |       |
| 0h       |            |    |    | 0h         | 0h      |            |       |
| 23       | 22         | 21 | 20 | 19         | 18      | 17         | 16    |
| TRIGSEL  |            |    |    | CHSEL      |         |            |       |
| R/W      |            |    |    | R/W        |         |            |       |
| 0h       |            |    |    | 0h         |         |            |       |
| 15       | 14         | 13 | 12 | 11         | 10      | 9          | 8     |
| CHSEL    | RESOLUTION |    |    | SIGNALMODE |         | RESERVED_1 | ACQPS |
| R/W      | R          |    |    | R          |         | R          | R/W   |
| 0h       | 0h         |    |    | 0h         |         | 0h         | 0h    |
| 7        | 6          | 5  | 4  | 3          | 2       | 1          | 0     |
| ACQPS    |            |    |    |            |         |            |       |
| R/W      |            |    |    |            |         |            |       |
| 0h       |            |    |    |            |         |            |       |

**Table 3-208. ADC\_CFG\_ADCSOC7CTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                     |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28 | EXTCHSEL   | R/W  | 0h    | SOC7 External Channel Mux Select. Selects the external mux combination to output when SOC7 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. |
| 27    | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                        |

**Table 3-208. ADC\_CFG\_ADCSOC7CTL Register Field Descriptions (continued)**

| Bit   | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|---------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:20 | TRIGSEL | R/W  | 0h    | <p>SOC7 Trigger Source Select. Along with the SOC7 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC7 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it.</p> <p>Note: SOCFRC1 register can always be used to software trigger SOC7s in addition to any hardware trigger configuration.</p> <p>00h ADCTRIG0 - Software only<br/> 01h ADCTRIG1 - RTI0 Timer<br/> 02h ADCTRIG2 - RTI1 Timer<br/> 03h ADCTRIG3 - RTI2 Timer<br/> 04h ADCTRIG4 - RTI3 Timer<br/> 05h ADCTRIG5 - InputXBAR.Out[5]<br/> 06h ADCTRIG6 - spare<br/> 07h ADCTRIG7 - spare<br/> 08h ADCTRIG8 - EPWM0, ADCSOCA<br/> 09h ADCTRIG9 - EPWM0, ADCSOCA<br/> 0Ah ADCTRIG10 - EPWM1, ADCSOCA<br/> 0Bh ADCTRIG11 - EPWM1, ADCSOCA<br/> 0Ch ADCTRIG12 - EPWM2, ADCSOCA<br/> 0Dh ADCTRIG13 - EPWM2, ADCSOCA<br/> 0Eh ADCTRIG14 - EPWM3, ADCSOCA<br/> 0Fh ADCTRIG15 - EPWM3, ADCSOCA<br/> .... EPWM4 to EPWM27<br/> 40h ADCTRIG64 - EPWM28, ADCSOCA<br/> 41h ADCTRIG65 - EPWM28, ADCSOCA<br/> 42h ADCTRIG66 - EPWM29, ADCSOCA<br/> 43h ADCTRIG67 - EPWM29, ADCSOCA<br/> 44h ADCTRIG68 - EPWM30, ADCSOCA<br/> 45h ADCTRIG69 - EPWM30, ADCSOCA<br/> 46h ADCTRIG70 - EPWM31, ADCSOCA<br/> 47h ADCTRIG71 - EPWM31, ADCSOCA<br/> 48h ADCTRIG72 - ECAP0, TRIGOUT<br/> .... ECAP1 to ECAP8<br/> 51h ADCTRIG81 - ECAP9, TRIGOUT<br/> 52h ADCTRIG82 - ECAP10, TRIGOUT<br/> ....<br/> 57h ADCTRIG87 - ECAP15, TRIGOUT<br/> 58h ADCTRIG88 - RTI4 Timer<br/> 59h ADCTRIG89 - RTI5 Timer<br/> 5Ah ADCTRIG90 - RTI6 Timer<br/> 5Bh ADCTRIG91 - RTI7 Timer<br/> ....<br/> 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.</p> |

**Table 3-208. ADC\_CFG\_ADCSOC7CTL Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19:15 | CHSEL      | R/W  | 0h    | <p>SOC7 Channel Select. Selects the channel to be converted when SOC7 is received by the ADC.</p> <p>Single-ended Signaling Mode [SIGNALMODE = 0]:</p> <p>00h ADCIN0</p> <p>01h ADCIN1</p> <p>02h ADCIN2</p> <p>03h ADCIN3</p> <p>...</p> <p>1Dh ADCIN29</p> <p>1Eh ADCIN30</p> <p>1Fh ADCIN31</p> <p>Differential Signaling Mode [SIGNALMODE = 1]:</p> <p>00h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>01h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>02h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>03h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>04h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>05h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>...</p> <p>0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>10h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>11h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> <p>1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> |
| 14:12 | RESOLUTION | R    | 0h    | Placeholder for per-SOC resolution                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 11:10 | SIGNALMODE | R    | 0h    | Placeholder for per-SOC signal mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 9     | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 8:0   | ACQPS      | R/W  | 0h    | <p>SOC7 Acquisition Prescale. Controls the sample and hold window for this SOC.</p> <p>000h Reserved</p> <p>001h Reserved</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>003h Sample window is 4 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p> <p>The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

### 3.2.2.69 ADC\_CFG\_ADCSOC8CTL Register

#### 1 ADC\_CFG\_ADCSOC8CTL Register (Offset = 40h) [reset = 0h]

ADC SOC8 Control Register.

Return to [Summary Table](#)

**Table 3-209. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0040h       |
| ADC1_G0_G5    | 502C 1040h       |
| ADC2_G0_G5    | 502C 2040h       |
| ADC3_G0_G5    | 502C 3040h       |
| ADC4_G0_G5    | 502C 4040h       |

**Figure 3-69. ADC\_CFG\_ADCSOC8CTL Name Register**

|          |            |    |    |            |         |            |       |
|----------|------------|----|----|------------|---------|------------|-------|
| 31       | 30         | 29 | 28 | 27         | 26      | 25         | 24    |
| EXTCHSEL |            |    |    | RESERVED_2 | TRIGSEL |            |       |
| R/W      |            |    |    | R          | R/W     |            |       |
| 0h       |            |    |    | 0h         | 0h      |            |       |
| 23       | 22         | 21 | 20 | 19         | 18      | 17         | 16    |
| TRIGSEL  |            |    |    | CHSEL      |         |            |       |
| R/W      |            |    |    | R/W        |         |            |       |
| 0h       |            |    |    | 0h         |         |            |       |
| 15       | 14         | 13 | 12 | 11         | 10      | 9          | 8     |
| CHSEL    | RESOLUTION |    |    | SIGNALMODE |         | RESERVED_1 | ACQPS |
| R/W      | R          |    |    | R          |         | R          | R/W   |
| 0h       | 0h         |    |    | 0h         |         | 0h         | 0h    |
| 7        | 6          | 5  | 4  | 3          | 2       | 1          | 0     |
| ACQPS    |            |    |    |            |         |            |       |
| R/W      |            |    |    |            |         |            |       |
| 0h       |            |    |    |            |         |            |       |

**Table 3-211. ADC\_CFG\_ADCSOC8CTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                     |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28 | EXTCHSEL   | R/W  | 0h    | SOC8 External Channel Mux Select. Selects the external mux combination to output when SOC8 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. |
| 27    | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                        |

**Table 3-211. ADC\_CFG\_ADCSOC8CTL Register Field Descriptions (continued)**

| Bit   | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|---------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:20 | TRIGSEL | R/W  | 0h    | <p>SOC8 Trigger Source Select. Along with the SOC8 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC8 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it.</p> <p>Note: SOCFRC1 register can always be used to software trigger SOC8s in addition to any hardware trigger configuration.</p> <p>00h ADCTRIG0 - Software only<br/> 01h ADCTRIG1 - RTI0 Timer<br/> 02h ADCTRIG2 - RTI1 Timer<br/> 03h ADCTRIG3 - RTI2 Timer<br/> 04h ADCTRIG4 - RTI3 Timer<br/> 05h ADCTRIG5 - InputXBAR.Out[5]<br/> 06h ADCTRIG6 - spare<br/> 07h ADCTRIG7 - spare<br/> 08h ADCTRIG8 - EPWM0, ADCSOCA<br/> 09h ADCTRIG9 - EPWM0, ADCSOCB<br/> 0Ah ADCTRIG10 - EPWM1, ADCSOCA<br/> 0Bh ADCTRIG11 - EPWM1, ADCSOCB<br/> 0Ch ADCTRIG12 - EPWM2, ADCSOCA<br/> 0Dh ADCTRIG13 - EPWM2, ADCSOCB<br/> 0Eh ADCTRIG14 - EPWM3, ADCSOCA<br/> 0Fh ADCTRIG15 - EPWM3, ADCSOCB<br/> .... EPWM4 to EPWM27<br/> 40h ADCTRIG64 - EPWM28, ADCSOCA<br/> 41h ADCTRIG65 - EPWM28, ADCSOCB<br/> 42h ADCTRIG66 - EPWM29, ADCSOCA<br/> 43h ADCTRIG67 - EPWM29, ADCSOCB<br/> 44h ADCTRIG68 - EPWM30, ADCSOCA<br/> 45h ADCTRIG69 - EPWM30, ADCSOCB<br/> 46h ADCTRIG70 - EPWM31, ADCSOCA<br/> 47h ADCTRIG71 - EPWM31, ADCSOCB<br/> 48h ADCTRIG72 - ECAP0, TRIGOUT<br/> .... ECAP1 to ECAP8<br/> 51h ADCTRIG81 - ECAP9, TRIGOUT<br/> 52h ADCTRIG82 - ECAP10, TRIGOUT<br/> ....<br/> 57h ADCTRIG87 - ECAP15, TRIGOUT<br/> 58h ADCTRIG88 - RTI4 Timer<br/> 59h ADCTRIG89 - RTI5 Timer<br/> 5Ah ADCTRIG90 - RTI6 Timer<br/> 5Bh ADCTRIG91 - RTI7 Timer<br/> ....<br/> 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.</p> |



**Table 3-211. ADC\_CFG\_ADCSOC8CTL Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19:15 | CHSEL      | R/W  | 0h    | <p>SOC8 Channel Select. Selects the channel to be converted when SOC8 is received by the ADC.</p> <p>Single-ended Signaling Mode [SIGNALMODE = 0]:</p> <p>00h ADCIN0</p> <p>01h ADCIN1</p> <p>02h ADCIN2</p> <p>03h ADCIN3</p> <p>...</p> <p>1Dh ADCIN29</p> <p>1Eh ADCIN30</p> <p>1Fh ADCIN31</p> <p>Differential Signaling Mode [SIGNALMODE = 1]:</p> <p>00h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>01h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>02h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>03h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>04h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>05h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>...</p> <p>0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>10h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>11h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> <p>1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> |
| 14:12 | RESOLUTION | R    | 0h    | Placeholder for per-SOC resolution                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 11:10 | SIGNALMODE | R    | 0h    | Placeholder for per-SOC signal mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 9     | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 8:0   | ACQPS      | R/W  | 0h    | <p>SOC8 Acquisition Prescale. Controls the sample and hold window for this SOC.</p> <p>000h Reserved</p> <p>001h Reserved</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>003h Sample window is 4 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p> <p>The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

### 3.2.2.70 ADC\_CFG\_ADCSOC9CTL Register

#### 1 ADC\_CFG\_ADCSOC9CTL Register (Offset = 44h) [reset = 0h]

ADC SOC9 Control Register.

Return to [Summary Table](#)

**Table 3-212. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0044h       |
| ADC1_G0_G5    | 502C 1044h       |
| ADC2_G0_G5    | 502C 2044h       |
| ADC3_G0_G5    | 502C 3044h       |
| ADC4_G0_G5    | 502C 4044h       |

**Figure 3-70. ADC\_CFG\_ADCSOC9CTL Name Register**

|          |            |    |    |            |         |            |       |
|----------|------------|----|----|------------|---------|------------|-------|
| 31       | 30         | 29 | 28 | 27         | 26      | 25         | 24    |
| EXTCHSEL |            |    |    | RESERVED_2 | TRIGSEL |            |       |
| R/W      |            |    |    | R          | R/W     |            |       |
| 0h       |            |    |    | 0h         | 0h      |            |       |
| 23       | 22         | 21 | 20 | 19         | 18      | 17         | 16    |
| TRIGSEL  |            |    |    | CHSEL      |         |            |       |
| R/W      |            |    |    | R/W        |         |            |       |
| 0h       |            |    |    | 0h         |         |            |       |
| 15       | 14         | 13 | 12 | 11         | 10      | 9          | 8     |
| CHSEL    | RESOLUTION |    |    | SIGNALMODE |         | RESERVED_1 | ACQPS |
| R/W      | R          |    |    | R          |         | R          | R/W   |
| 0h       | 0h         |    |    | 0h         |         | 0h         | 0h    |
| 7        | 6          | 5  | 4  | 3          | 2       | 1          | 0     |
| ACQPS    |            |    |    |            |         |            |       |
| R/W      |            |    |    |            |         |            |       |
| 0h       |            |    |    |            |         |            |       |

**Table 3-214. ADC\_CFG\_ADCSOC9CTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                     |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28 | EXTCHSEL   | R/W  | 0h    | SOC9 External Channel Mux Select. Selects the external mux combination to output when SOC9 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. |
| 27    | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                        |

**Table 3-214. ADC\_CFG\_ADCSOC9CTL Register Field Descriptions (continued)**

| Bit   | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|---------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:20 | TRIGSEL | R/W  | 0h    | <p>SOC9 Trigger Source Select. Along with the SOC9 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC9 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it.</p> <p>Note: SOCFRC1 register can always be used to software trigger SOC9s in addition to any hardware trigger configuration.</p> <p>00h ADCTRIG0 - Software only<br/> 01h ADCTRIG1 - RTI0 Timer<br/> 02h ADCTRIG2 - RTI1 Timer<br/> 03h ADCTRIG3 - RTI2 Timer<br/> 04h ADCTRIG4 - RTI3 Timer<br/> 05h ADCTRIG5 - InputXBAR.Out[5]<br/> 06h ADCTRIG6 - spare<br/> 07h ADCTRIG7 - spare<br/> 08h ADCTRIG8 - EPWM0, ADCSOCA<br/> 09h ADCTRIG9 - EPWM0, ADCSOCB<br/> 0Ah ADCTRIG10 - EPWM1, ADCSOCA<br/> 0Bh ADCTRIG11 - EPWM1, ADCSOCB<br/> 0Ch ADCTRIG12 - EPWM2, ADCSOCA<br/> 0Dh ADCTRIG13 - EPWM2, ADCSOCB<br/> 0Eh ADCTRIG14 - EPWM3, ADCSOCA<br/> 0Fh ADCTRIG15 - EPWM3, ADCSOCB<br/> .... EPWM4 to EPWM27<br/> 40h ADCTRIG64 - EPWM28, ADCSOCA<br/> 41h ADCTRIG65 - EPWM28, ADCSOCB<br/> 42h ADCTRIG66 - EPWM29, ADCSOCA<br/> 43h ADCTRIG67 - EPWM29, ADCSOCB<br/> 44h ADCTRIG68 - EPWM30, ADCSOCA<br/> 45h ADCTRIG69 - EPWM30, ADCSOCB<br/> 46h ADCTRIG70 - EPWM31, ADCSOCA<br/> 47h ADCTRIG71 - EPWM31, ADCSOCB<br/> 48h ADCTRIG72 - ECAP0, TRIGOUT<br/> .... ECAP1 to ECAP8<br/> 51h ADCTRIG81 - ECAP9, TRIGOUT<br/> 52h ADCTRIG82 - ECAP10, TRIGOUT<br/> ....<br/> 57h ADCTRIG87 - ECAP15, TRIGOUT<br/> 58h ADCTRIG88 - RTI4 Timer<br/> 59h ADCTRIG89 - RTI5 Timer<br/> 5Ah ADCTRIG90 - RTI6 Timer<br/> 5Bh ADCTRIG91 - RTI7 Timer<br/> ....<br/> 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.</p> |

**Table 3-214. ADC\_CFG\_ADCSOC9CTL Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19:15 | CHSEL      | R/W  | 0h    | <p>SOC9 Channel Select. Selects the channel to be converted when SOC9 is received by the ADC.</p> <p>Single-ended Signaling Mode [SIGNALMODE = 0]:</p> <p>00h ADCIN0</p> <p>01h ADCIN1</p> <p>02h ADCIN2</p> <p>03h ADCIN3</p> <p>...</p> <p>1Dh ADCIN29</p> <p>1Eh ADCIN30</p> <p>1Fh ADCIN31</p> <p>Differential Signaling Mode [SIGNALMODE = 1]:</p> <p>00h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>01h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>02h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>03h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>04h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>05h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>...</p> <p>0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>10h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>11h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> <p>1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> |
| 14:12 | RESOLUTION | R    | 0h    | Placeholder for per-SOC resolution                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 11:10 | SIGNALMODE | R    | 0h    | Placeholder for per-SOC signal mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 9     | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 8:0   | ACQPS      | R/W  | 0h    | <p>SOC9 Acquisition Prescale. Controls the sample and hold window for this SOC.</p> <p>000h Reserved</p> <p>001h Reserved</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>003h Sample window is 4 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p> <p>The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

### 3.2.2.71 ADC\_CFG\_ADCSOC10CTL Register

#### 1 ADC\_CFG\_ADCSOC10CTL Register (Offset = 48h) [reset = 0h]

ADC SOC10 Control Register.

Return to [Summary Table](#)

**Table 3-215. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0048h       |
| ADC1_G0_G5    | 502C 1048h       |
| ADC2_G0_G5    | 502C 2048h       |
| ADC3_G0_G5    | 502C 3048h       |
| ADC4_G0_G5    | 502C 4048h       |

**Figure 3-71. ADC\_CFG\_ADCSOC10CTL Name Register**

|          |            |    |    |            |         |            |       |
|----------|------------|----|----|------------|---------|------------|-------|
| 31       | 30         | 29 | 28 | 27         | 26      | 25         | 24    |
| EXTCHSEL |            |    |    | RESERVED_2 | TRIGSEL |            |       |
| R/W      |            |    |    | R          | R/W     |            |       |
| 0h       |            |    |    | 0h         | 0h      |            |       |
| 23       | 22         | 21 | 20 | 19         | 18      | 17         | 16    |
| TRIGSEL  |            |    |    | CHSEL      |         |            |       |
| R/W      |            |    |    | R/W        |         |            |       |
| 0h       |            |    |    | 0h         |         |            |       |
| 15       | 14         | 13 | 12 | 11         | 10      | 9          | 8     |
| CHSEL    | RESOLUTION |    |    | SIGNALMODE |         | RESERVED_1 | ACQPS |
| R/W      | R          |    |    | R          |         | R          | R/W   |
| 0h       | 0h         |    |    | 0h         |         | 0h         | 0h    |
| 7        | 6          | 5  | 4  | 3          | 2       | 1          | 0     |
| ACQPS    |            |    |    |            |         |            |       |
| R/W      |            |    |    |            |         |            |       |
| 0h       |            |    |    |            |         |            |       |

**Table 3-217. ADC\_CFG\_ADCSOC10CTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                       |
|-------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28 | EXTCHSEL   | R/W  | 0h    | SOC10 External Channel Mux Select. Selects the external mux combination to output when SOC10 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. |
| 27    | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                          |

**Table 3-217. ADC\_CFG\_ADCSOC10CTL Register Field Descriptions (continued)**

| Bit   | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|---------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:20 | TRIGSEL | R/W  | 0h    | <p>SOC10 Trigger Source Select. Along with the SOC10 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC10 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it.</p> <p>Note: SOCFRC1 register can always be used to software trigger SOC10s in addition to any hardware trigger configuration.</p> <p>00h ADCTRIG0 - Software only<br/> 01h ADCTRIG1 - RTI0 Timer<br/> 02h ADCTRIG2 - RTI1 Timer<br/> 03h ADCTRIG3 - RTI2 Timer<br/> 04h ADCTRIG4 - RTI3 Timer<br/> 05h ADCTRIG5 - InputXBAR.Out[5]<br/> 06h ADCTRIG6 - spare<br/> 07h ADCTRIG7 - spare<br/> 08h ADCTRIG8 - EPWM0, ADCSOCA<br/> 09h ADCTRIG9 - EPWM0, ADCSOCB<br/> 0Ah ADCTRIG10 - EPWM1, ADCSOCA<br/> 0Bh ADCTRIG11 - EPWM1, ADCSOCB<br/> 0Ch ADCTRIG12 - EPWM2, ADCSOCA<br/> 0Dh ADCTRIG13 - EPWM2, ADCSOCB<br/> 0Eh ADCTRIG14 - EPWM3, ADCSOCA<br/> 0Fh ADCTRIG15 - EPWM3, ADCSOCB<br/> .... EPWM4 to EPWM27<br/> 40h ADCTRIG64 - EPWM28, ADCSOCA<br/> 41h ADCTRIG65 - EPWM28, ADCSOCB<br/> 42h ADCTRIG66 - EPWM29, ADCSOCA<br/> 43h ADCTRIG67 - EPWM29, ADCSOCB<br/> 44h ADCTRIG68 - EPWM30, ADCSOCA<br/> 45h ADCTRIG69 - EPWM30, ADCSOCB<br/> 46h ADCTRIG70 - EPWM31, ADCSOCA<br/> 47h ADCTRIG71 - EPWM31, ADCSOCB<br/> 48h ADCTRIG72 - ECAP0, TRIGOUT<br/> .... ECAP1 to ECAP8<br/> 51h ADCTRIG81 - ECAP9, TRIGOUT<br/> 52h ADCTRIG82 - ECAP10, TRIGOUT<br/> ....<br/> 57h ADCTRIG87 - ECAP15, TRIGOUT<br/> 58h ADCTRIG88 - RTI4 Timer<br/> 59h ADCTRIG89 - RTI5 Timer<br/> 5Ah ADCTRIG90 - RTI6 Timer<br/> 5Bh ADCTRIG91 - RTI7 Timer<br/> ....<br/> 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.</p> |

**Table 3-217. ADC\_CFG\_ADCSOC10CTL Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19:15 | CHSEL      | R/W  | 0h    | <p>SOC10 Channel Select. Selects the channel to be converted when SOC10 is received by the ADC.</p> <p>Single-ended Signaling Mode [SIGNALMODE = 0]:</p> <p>00h ADCIN0</p> <p>01h ADCIN1</p> <p>02h ADCIN2</p> <p>03h ADCIN3</p> <p>...</p> <p>1Dh ADCIN29</p> <p>1Eh ADCIN30</p> <p>1Fh ADCIN31</p> <p>Differential Signaling Mode [SIGNALMODE = 1]:</p> <p>00h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>01h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>02h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>03h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>04h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>05h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>...</p> <p>0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>10h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>11h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> <p>1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> |
| 14:12 | RESOLUTION | R    | 0h    | Placeholder for per-SOC resolution                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 11:10 | SIGNALMODE | R    | 0h    | Placeholder for per-SOC signal mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 9     | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 8:0   | ACQPS      | R/W  | 0h    | <p>SOC10 Acquisition Prescale. Controls the sample and hold window for this SOC.</p> <p>000h Reserved</p> <p>001h Reserved</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>003h Sample window is 4 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p> <p>The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

### 3.2.2.72 ADC\_CFG\_ADCSOC11CTL Register

#### 1 ADC\_CFG\_ADCSOC11CTL Register (Offset = 4Ch) [reset = 0h]

ADC SOC11 Control Register.

Return to [Summary Table](#)

**Table 3-218. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 004Ch       |
| ADC1_G0_G5    | 502C 104Ch       |
| ADC2_G0_G5    | 502C 204Ch       |
| ADC3_G0_G5    | 502C 304Ch       |
| ADC4_G0_G5    | 502C 404Ch       |

**Figure 3-72. ADC\_CFG\_ADCSOC11CTL Name Register**

|          |            |    |    |            |         |            |       |
|----------|------------|----|----|------------|---------|------------|-------|
| 31       | 30         | 29 | 28 | 27         | 26      | 25         | 24    |
| EXTCHSEL |            |    |    | RESERVED_2 | TRIGSEL |            |       |
| R/W      |            |    |    | R          | R/W     |            |       |
| 0h       |            |    |    | 0h         | 0h      |            |       |
| 23       | 22         | 21 | 20 | 19         | 18      | 17         | 16    |
| TRIGSEL  |            |    |    | CHSEL      |         |            |       |
| R/W      |            |    |    | R/W        |         |            |       |
| 0h       |            |    |    | 0h         |         |            |       |
| 15       | 14         | 13 | 12 | 11         | 10      | 9          | 8     |
| CHSEL    | RESOLUTION |    |    | SIGNALMODE |         | RESERVED_1 | ACQPS |
| R/W      | R          |    |    | R          |         | R          | R/W   |
| 0h       | 0h         |    |    | 0h         |         | 0h         | 0h    |
| 7        | 6          | 5  | 4  | 3          | 2       | 1          | 0     |
| ACQPS    |            |    |    |            |         |            |       |
| R/W      |            |    |    |            |         |            |       |
| 0h       |            |    |    |            |         |            |       |

**Table 3-220. ADC\_CFG\_ADCSOC11CTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                       |
|-------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28 | EXTCHSEL   | R/W  | 0h    | SOC11 External Channel Mux Select. Selects the external mux combination to output when SOC11 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. |
| 27    | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                          |



**Table 3-220. ADC\_CFG\_ADCSOC11CTL Register Field Descriptions (continued)**

| Bit   | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|---------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:20 | TRIGSEL | R/W  | 0h    | <p>SOC11 Trigger Source Select. Along with the SOC11 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC11 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it.</p> <p>Note: SOCFRC1 register can always be used to software trigger SOC11 in addition to any hardware trigger configuration.</p> <p>00h ADCTRIG0 - Software only<br/> 01h ADCTRIG1 - RTI0 Timer<br/> 02h ADCTRIG2 - RTI1 Timer<br/> 03h ADCTRIG3 - RTI2 Timer<br/> 04h ADCTRIG4 - RTI3 Timer<br/> 05h ADCTRIG5 - InputXBAR.Out[5]<br/> 06h ADCTRIG6 - spare<br/> 07h ADCTRIG7 - spare<br/> 08h ADCTRIG8 - EPWM0, ADCSOCA<br/> 09h ADCTRIG9 - EPWM0, ADCSOCB<br/> 0Ah ADCTRIG10 - EPWM1, ADCSOCA<br/> 0Bh ADCTRIG11 - EPWM1, ADCSOCB<br/> 0Ch ADCTRIG12 - EPWM2, ADCSOCA<br/> 0Dh ADCTRIG13 - EPWM2, ADCSOCB<br/> 0Eh ADCTRIG14 - EPWM3, ADCSOCA<br/> 0Fh ADCTRIG15 - EPWM3, ADCSOCB<br/> .... EPWM4 to EPWM27<br/> 40h ADCTRIG64 - EPWM28, ADCSOCA<br/> 41h ADCTRIG65 - EPWM28, ADCSOCB<br/> 42h ADCTRIG66 - EPWM29, ADCSOCA<br/> 43h ADCTRIG67 - EPWM29, ADCSOCB<br/> 44h ADCTRIG68 - EPWM30, ADCSOCA<br/> 45h ADCTRIG69 - EPWM30, ADCSOCB<br/> 46h ADCTRIG70 - EPWM31, ADCSOCA<br/> 47h ADCTRIG71 - EPWM31, ADCSOCB<br/> 48h ADCTRIG72 - ECAP0, TRIGOUT<br/> .... ECAP1 to ECAP8<br/> 51h ADCTRIG81 - ECAP9, TRIGOUT<br/> 52h ADCTRIG82 - ECAP10, TRIGOUT<br/> ....<br/> 57h ADCTRIG87 - ECAP15, TRIGOUT<br/> 58h ADCTRIG88 - RTI4 Timer<br/> 59h ADCTRIG89 - RTI5 Timer<br/> 5Ah ADCTRIG90 - RTI6 Timer<br/> 5Bh ADCTRIG91 - RTI7 Timer<br/> ....<br/> 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.</p> |

**Table 3-220. ADC\_CFG\_ADCSOC11CTL Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19:15 | CHSEL      | R/W  | 0h    | <p>SOC11 Channel Select. Selects the channel to be converted when SOC11 is received by the ADC.</p> <p>Single-ended Signaling Mode [SIGNALMODE = 0]:</p> <p>00h ADCIN0</p> <p>01h ADCIN1</p> <p>02h ADCIN2</p> <p>03h ADCIN3</p> <p>...</p> <p>1Dh ADCIN29</p> <p>1Eh ADCIN30</p> <p>1Fh ADCIN31</p> <p>Differential Signaling Mode [SIGNALMODE = 1]:</p> <p>00h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>01h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>02h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>03h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>04h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>05h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>...</p> <p>0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>10h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>11h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> <p>1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> |
| 14:12 | RESOLUTION | R    | 0h    | Placeholder for per-SOC resolution                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 11:10 | SIGNALMODE | R    | 0h    | Placeholder for per-SOC signal mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 9     | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 8:0   | ACQPS      | R/W  | 0h    | <p>SOC11 Acquisition Prescale. Controls the sample and hold window for this SOC.</p> <p>000h Reserved</p> <p>001h Reserved</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>003h Sample window is 4 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p> <p>The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

### 3.2.2.73 ADC\_CFG\_ADCSOC12CTL Register

#### 1 ADC\_CFG\_ADCSOC12CTL Register (Offset = 50h) [reset = 0h]

ADC SOC12 Control Register.

Return to [Summary Table](#)

**Table 3-221. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0050h       |
| ADC1_G0_G5    | 502C 1050h       |
| ADC2_G0_G5    | 502C 2050h       |
| ADC3_G0_G5    | 502C 3050h       |
| ADC4_G0_G5    | 502C 4050h       |

**Figure 3-73. ADC\_CFG\_ADCSOC12CTL Name Register**

|          |            |    |    |            |         |            |       |
|----------|------------|----|----|------------|---------|------------|-------|
| 31       | 30         | 29 | 28 | 27         | 26      | 25         | 24    |
| EXTCHSEL |            |    |    | RESERVED_2 | TRIGSEL |            |       |
| R/W      |            |    |    | R          | R/W     |            |       |
| 0h       |            |    |    | 0h         | 0h      |            |       |
| 23       | 22         | 21 | 20 | 19         | 18      | 17         | 16    |
| TRIGSEL  |            |    |    | CHSEL      |         |            |       |
| R/W      |            |    |    | R/W        |         |            |       |
| 0h       |            |    |    | 0h         |         |            |       |
| 15       | 14         | 13 | 12 | 11         | 10      | 9          | 8     |
| CHSEL    | RESOLUTION |    |    | SIGNALMODE |         | RESERVED_1 | ACQPS |
| R/W      | R          |    |    | R          |         | R          | R/W   |
| 0h       | 0h         |    |    | 0h         |         | 0h         | 0h    |
| 7        | 6          | 5  | 4  | 3          | 2       | 1          | 0     |
| ACQPS    |            |    |    |            |         |            |       |
| R/W      |            |    |    |            |         |            |       |
| 0h       |            |    |    |            |         |            |       |

**Table 3-223. ADC\_CFG\_ADCSOC12CTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                       |
|-------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28 | EXTCHSEL   | R/W  | 0h    | SOC12 External Channel Mux Select. Selects the external mux combination to output when SOC12 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. |
| 27    | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                          |

**Table 3-223. ADC\_CFG\_ADCSOC12CTL Register Field Descriptions (continued)**

| Bit   | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|---------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:20 | TRIGSEL | R/W  | 0h    | <p>SOC12 Trigger Source Select. Along with the SOC12 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC12 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it.</p> <p>Note: SOCFRC1 register can always be used to software trigger SOC12s in addition to any hardware trigger configuration.</p> <p>00h ADCTRIG0 - Software only<br/> 01h ADCTRIG1 - RTI0 Timer<br/> 02h ADCTRIG2 - RTI1 Timer<br/> 03h ADCTRIG3 - RTI2 Timer<br/> 04h ADCTRIG4 - RTI3 Timer<br/> 05h ADCTRIG5 - InputXBAR.Out[5]<br/> 06h ADCTRIG6 - spare<br/> 07h ADCTRIG7 - spare<br/> 08h ADCTRIG8 - EPWM0, ADCSOCA<br/> 09h ADCTRIG9 - EPWM0, ADCSOCB<br/> 0Ah ADCTRIG10 - EPWM1, ADCSOCA<br/> 0Bh ADCTRIG11 - EPWM1, ADCSOCB<br/> 0Ch ADCTRIG12 - EPWM2, ADCSOCA<br/> 0Dh ADCTRIG13 - EPWM2, ADCSOCB<br/> 0Eh ADCTRIG14 - EPWM3, ADCSOCA<br/> 0Fh ADCTRIG15 - EPWM3, ADCSOCB<br/> .... EPWM4 to EPWM27<br/> 40h ADCTRIG64 - EPWM28, ADCSOCA<br/> 41h ADCTRIG65 - EPWM28, ADCSOCB<br/> 42h ADCTRIG66 - EPWM29, ADCSOCA<br/> 43h ADCTRIG67 - EPWM29, ADCSOCB<br/> 44h ADCTRIG68 - EPWM30, ADCSOCA<br/> 45h ADCTRIG69 - EPWM30, ADCSOCB<br/> 46h ADCTRIG70 - EPWM31, ADCSOCA<br/> 47h ADCTRIG71 - EPWM31, ADCSOCB<br/> 48h ADCTRIG72 - ECAP0, TRIGOUT<br/> .... ECAP1 to ECAP8<br/> 51h ADCTRIG81 - ECAP9, TRIGOUT<br/> 52h ADCTRIG82 - ECAP10, TRIGOUT<br/> ....<br/> 57h ADCTRIG87 - ECAP15, TRIGOUT<br/> 58h ADCTRIG88 - RTI4 Timer<br/> 59h ADCTRIG89 - RTI5 Timer<br/> 5Ah ADCTRIG90 - RTI6 Timer<br/> 5Bh ADCTRIG91 - RTI7 Timer<br/> ....<br/> 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.</p> |

**Table 3-223. ADC\_CFG\_ADCSOC12CTL Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19:15 | CHSEL      | R/W  | 0h    | <p>SOC12 Channel Select. Selects the channel to be converted when SOC12 is received by the ADC.</p> <p>Single-ended Signaling Mode [SIGNALMODE = 0]:</p> <p>00h ADCIN0</p> <p>01h ADCIN1</p> <p>02h ADCIN2</p> <p>03h ADCIN3</p> <p>...</p> <p>1Dh ADCIN29</p> <p>1Eh ADCIN30</p> <p>1Fh ADCIN31</p> <p>Differential Signaling Mode [SIGNALMODE = 1]:</p> <p>00h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>01h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>02h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>03h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>04h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>05h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>...</p> <p>0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>10h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>11h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> <p>1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> |
| 14:12 | RESOLUTION | R    | 0h    | Placeholder for per-SOC resolution                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 11:10 | SIGNALMODE | R    | 0h    | Placeholder for per-SOC signal mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 9     | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 8:0   | ACQPS      | R/W  | 0h    | <p>SOC12 Acquisition Prescale. Controls the sample and hold window for this SOC.</p> <p>000h Reserved</p> <p>001h Reserved</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>003h Sample window is 4 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p> <p>The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

### 3.2.2.74 ADC\_CFG\_ADCSOC13CTL Register

#### 1 ADC\_CFG\_ADCSOC13CTL Register (Offset = 54h) [reset = 0h]

ADC SOC13 Control Register.

Return to [Summary Table](#)

**Table 3-224. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0054h       |
| ADC1_G0_G5    | 502C 1054h       |
| ADC2_G0_G5    | 502C 2054h       |
| ADC3_G0_G5    | 502C 3054h       |
| ADC4_G0_G5    | 502C 4054h       |

**Figure 3-74. ADC\_CFG\_ADCSOC13CTL Name Register**

|          |            |    |    |            |         |            |       |
|----------|------------|----|----|------------|---------|------------|-------|
| 31       | 30         | 29 | 28 | 27         | 26      | 25         | 24    |
| EXTCHSEL |            |    |    | RESERVED_2 | TRIGSEL |            |       |
| R/W      |            |    |    | R          | R/W     |            |       |
| 0h       |            |    |    | 0h         | 0h      |            |       |
| 23       | 22         | 21 | 20 | 19         | 18      | 17         | 16    |
| TRIGSEL  |            |    |    | CHSEL      |         |            |       |
| R/W      |            |    |    | R/W        |         |            |       |
| 0h       |            |    |    | 0h         |         |            |       |
| 15       | 14         | 13 | 12 | 11         | 10      | 9          | 8     |
| CHSEL    | RESOLUTION |    |    | SIGNALMODE |         | RESERVED_1 | ACQPS |
| R/W      | R          |    |    | R          |         | R          | R/W   |
| 0h       | 0h         |    |    | 0h         |         | 0h         | 0h    |
| 7        | 6          | 5  | 4  | 3          | 2       | 1          | 0     |
| ACQPS    |            |    |    |            |         |            |       |
| R/W      |            |    |    |            |         |            |       |
| 0h       |            |    |    |            |         |            |       |

**Table 3-226. ADC\_CFG\_ADCSOC13CTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                          |
|-------|------------|------|-------|------------------------------------------------------|
| 31:28 | EXTCHSEL   | R/W  | 0h    | SOC13 External Channel Mux Select. Selects the exter |
| 27    | RESERVED_2 | R    | 0h    | Reserved                                             |

**Table 3-226. ADC\_CFG\_ADCSOC13CTL Register Field Descriptions (continued)**

| Bit   | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|---------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:20 | TRIGSEL | R/W  | 0h    | <p>SOC13 Trigger Source Select. Along with the SOC13 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC13 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it.</p> <p>Note: SOCFRC1 register can always be used to software trigger SOC13 in addition to any hardware trigger configuration.</p> <p>00h ADCTRIG0 - Software only<br/> 01h ADCTRIG1 - RTI0 Timer<br/> 02h ADCTRIG2 - RTI1 Timer<br/> 03h ADCTRIG3 - RTI2 Timer<br/> 04h ADCTRIG4 - RTI3 Timer<br/> 05h ADCTRIG5 - InputXBAR.Out[5]<br/> 06h ADCTRIG6 - spare<br/> 07h ADCTRIG7 - spare<br/> 08h ADCTRIG8 - EPWM0, ADCSOCA<br/> 09h ADCTRIG9 - EPWM0, ADCSOCB<br/> 0Ah ADCTRIG10 - EPWM1, ADCSOCA<br/> 0Bh ADCTRIG11 - EPWM1, ADCSOCB<br/> 0Ch ADCTRIG12 - EPWM2, ADCSOCA<br/> 0Dh ADCTRIG13 - EPWM2, ADCSOCB<br/> 0Eh ADCTRIG14 - EPWM3, ADCSOCA<br/> 0Fh ADCTRIG15 - EPWM3, ADCSOCB<br/> .... EPWM4 to EPWM27<br/> 40h ADCTRIG64 - EPWM28, ADCSOCA<br/> 41h ADCTRIG65 - EPWM28, ADCSOCB<br/> 42h ADCTRIG66 - EPWM29, ADCSOCA<br/> 43h ADCTRIG67 - EPWM29, ADCSOCB<br/> 44h ADCTRIG68 - EPWM30, ADCSOCA<br/> 45h ADCTRIG69 - EPWM30, ADCSOCB<br/> 46h ADCTRIG70 - EPWM31, ADCSOCA<br/> 47h ADCTRIG71 - EPWM31, ADCSOCB<br/> 48h ADCTRIG72 - ECAP0, TRIGOUT<br/> .... ECAP1 to ECAP8<br/> 51h ADCTRIG81 - ECAP9, TRIGOUT<br/> 52h ADCTRIG82 - ECAP10, TRIGOUT<br/> ....<br/> 57h ADCTRIG87 - ECAP15, TRIGOUT<br/> 58h ADCTRIG88 - RTI4 Timer<br/> 59h ADCTRIG89 - RTI5 Timer<br/> 5Ah ADCTRIG90 - RTI6 Timer<br/> 5Bh ADCTRIG91 - RTI7 Timer<br/> ....<br/> 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.</p> |

**Table 3-226. ADC\_CFG\_ADCSOC13CTL Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19:15 | CHSEL      | R/W  | 0h    | <p>SOC13 Channel Select. Selects the channel to be converted when SOC13 is received by the ADC.</p> <p>Single-ended Signaling Mode [SIGNALMODE = 0]:</p> <p>00h ADCIN0</p> <p>01h ADCIN1</p> <p>02h ADCIN2</p> <p>03h ADCIN3</p> <p>...</p> <p>1Dh ADCIN29</p> <p>1Eh ADCIN30</p> <p>1Fh ADCIN31</p> <p>Differential Signaling Mode [SIGNALMODE = 1]:</p> <p>00h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>01h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>02h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>03h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>04h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>05h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>...</p> <p>0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>10h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>11h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> <p>1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> |
| 14:12 | RESOLUTION | R    | 0h    | Placeholder for per-SOC resolution                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 11:10 | SIGNALMODE | R    | 0h    | Placeholder for per-SOC signal mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 9     | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 8:0   | ACQPS      | R/W  | 0h    | <p>SOC13 Acquisition Prescale. Controls the sample and hold window for this SOC.</p> <p>000h Reserved</p> <p>001h Reserved</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>003h Sample window is 4 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p> <p>The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |



### 3.2.2.75 ADC\_CFG\_ADCSOC14CTL Register

#### 1 ADC\_CFG\_ADCSOC14CTL Register (Offset = 58h) [reset = 0h]

ADC SOC14 Control Register.

Return to [Summary Table](#)

**Table 3-227. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0058h       |
| ADC1_G0_G5    | 502C 1058h       |
| ADC2_G0_G5    | 502C 2058h       |
| ADC3_G0_G5    | 502C 3058h       |
| ADC4_G0_G5    | 502C 4058h       |

**Figure 3-75. ADC\_CFG\_ADCSOC14CTL Name Register**

|          |            |    |    |            |         |            |       |
|----------|------------|----|----|------------|---------|------------|-------|
| 31       | 30         | 29 | 28 | 27         | 26      | 25         | 24    |
| EXTCHSEL |            |    |    | RESERVED_2 | TRIGSEL |            |       |
| R/W      |            |    |    | R          | R/W     |            |       |
| 0h       |            |    |    | 0h         | 0h      |            |       |
| 23       | 22         | 21 | 20 | 19         | 18      | 17         | 16    |
| TRIGSEL  |            |    |    | CHSEL      |         |            |       |
| R/W      |            |    |    | R/W        |         |            |       |
| 0h       |            |    |    | 0h         |         |            |       |
| 15       | 14         | 13 | 12 | 11         | 10      | 9          | 8     |
| CHSEL    | RESOLUTION |    |    | SIGNALMODE |         | RESERVED_1 | ACQPS |
| R/W      | R          |    |    | R          |         | R          | R/W   |
| 0h       | 0h         |    |    | 0h         |         | 0h         | 0h    |
| 7        | 6          | 5  | 4  | 3          | 2       | 1          | 0     |
| ACQPS    |            |    |    |            |         |            |       |
| R/W      |            |    |    |            |         |            |       |
| 0h       |            |    |    |            |         |            |       |

**Table 3-229. ADC\_CFG\_ADCSOC14CTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                       |
|-------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28 | EXTCHSEL   | R/W  | 0h    | SOC14 External Channel Mux Select. Selects the external mux combination to output when SOC14 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. |
| 27    | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                          |

**Table 3-229. ADC\_CFG\_ADCSOC14CTL Register Field Descriptions (continued)**

| Bit   | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|---------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:20 | TRIGSEL | R/W  | 0h    | <p>SOC14 Trigger Source Select. Along with the SOC14 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC14 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it.</p> <p>Note: SOCFRC1 register can always be used to software trigger SOC14 in addition to any hardware trigger configuration.</p> <p>00h ADCTRIG0 - Software only<br/> 01h ADCTRIG1 - RTI0 Timer<br/> 02h ADCTRIG2 - RTI1 Timer<br/> 03h ADCTRIG3 - RTI2 Timer<br/> 04h ADCTRIG4 - RTI3 Timer<br/> 05h ADCTRIG5 - InputXBAR.Out[5]<br/> 06h ADCTRIG6 - spare<br/> 07h ADCTRIG7 - spare<br/> 08h ADCTRIG8 - EPWM0, ADCSOCA<br/> 09h ADCTRIG9 - EPWM0, ADCSOCB<br/> 0Ah ADCTRIG10 - EPWM1, ADCSOCA<br/> 0Bh ADCTRIG11 - EPWM1, ADCSOCB<br/> 0Ch ADCTRIG12 - EPWM2, ADCSOCA<br/> 0Dh ADCTRIG13 - EPWM2, ADCSOCB<br/> 0Eh ADCTRIG14 - EPWM3, ADCSOCA<br/> 0Fh ADCTRIG15 - EPWM3, ADCSOCB<br/> .... EPWM4 to EPWM27<br/> 40h ADCTRIG64 - EPWM28, ADCSOCA<br/> 41h ADCTRIG65 - EPWM28, ADCSOCB<br/> 42h ADCTRIG66 - EPWM29, ADCSOCA<br/> 43h ADCTRIG67 - EPWM29, ADCSOCB<br/> 44h ADCTRIG68 - EPWM30, ADCSOCA<br/> 45h ADCTRIG69 - EPWM30, ADCSOCB<br/> 46h ADCTRIG70 - EPWM31, ADCSOCA<br/> 47h ADCTRIG71 - EPWM31, ADCSOCB<br/> 48h ADCTRIG72 - ECAP0, TRIGOUT<br/> .... ECAP1 to ECAP8<br/> 51h ADCTRIG81 - ECAP9, TRIGOUT<br/> 52h ADCTRIG82 - ECAP10, TRIGOUT<br/> ....<br/> 57h ADCTRIG87 - ECAP15, TRIGOUT<br/> 58h ADCTRIG88 - RTI4 Timer<br/> 59h ADCTRIG89 - RTI5 Timer<br/> 5Ah ADCTRIG90 - RTI6 Timer<br/> 5Bh ADCTRIG91 - RTI7 Timer<br/> ....<br/> 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.</p> |

**Table 3-229. ADC\_CFG\_ADCSOC14CTL Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19:15 | CHSEL      | R/W  | 0h    | <p>SOC14 Channel Select. Selects the channel to be converted when SOC14 is received by the ADC.</p> <p>Single-ended Signaling Mode [SIGNALMODE = 0]:</p> <p>00h ADCIN0</p> <p>01h ADCIN1</p> <p>02h ADCIN2</p> <p>03h ADCIN3</p> <p>...</p> <p>1Dh ADCIN29</p> <p>1Eh ADCIN30</p> <p>1Fh ADCIN31</p> <p>Differential Signaling Mode [SIGNALMODE = 1]:</p> <p>00h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>01h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>02h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>03h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>04h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>05h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>...</p> <p>0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>10h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>11h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> <p>1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> |
| 14:12 | RESOLUTION | R    | 0h    | Placeholder for per-SOC resolution                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 11:10 | SIGNALMODE | R    | 0h    | Placeholder for per-SOC signal mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 9     | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 8:0   | ACQPS      | R/W  | 0h    | <p>SOC14 Acquisition Prescale. Controls the sample and hold window for this SOC.</p> <p>000h Reserved</p> <p>001h Reserved</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>003h Sample window is 4 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p> <p>The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

### 3.2.2.76 ADC\_CFG\_ADCSOC15CTL Register

#### 1 ADC\_CFG\_ADCSOC15CTL Register (Offset = 5Ch) [reset = 0h]

ADC SOC15 Control Register.

Return to [Summary Table](#)

**Table 3-230. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 005Ch       |
| ADC1_G0_G5    | 502C 105Ch       |
| ADC2_G0_G5    | 502C 205Ch       |
| ADC3_G0_G5    | 502C 305Ch       |
| ADC4_G0_G5    | 502C 405Ch       |

**Figure 3-76. ADC\_CFG\_ADCSOC15CTL Name Register**

|          |            |    |    |            |         |            |       |
|----------|------------|----|----|------------|---------|------------|-------|
| 31       | 30         | 29 | 28 | 27         | 26      | 25         | 24    |
| EXTCHSEL |            |    |    | RESERVED_2 | TRIGSEL |            |       |
| R/W      |            |    |    | R          | R/W     |            |       |
| 0h       |            |    |    | 0h         | 0h      |            |       |
| 23       | 22         | 21 | 20 | 19         | 18      | 17         | 16    |
| TRIGSEL  |            |    |    | CHSEL      |         |            |       |
| R/W      |            |    |    | R/W        |         |            |       |
| 0h       |            |    |    | 0h         |         |            |       |
| 15       | 14         | 13 | 12 | 11         | 10      | 9          | 8     |
| CHSEL    | RESOLUTION |    |    | SIGNALMODE |         | RESERVED_1 | ACQPS |
| R/W      | R          |    |    | R          |         | R          | R/W   |
| 0h       | 0h         |    |    | 0h         |         | 0h         | 0h    |
| 7        | 6          | 5  | 4  | 3          | 2       | 1          | 0     |
| ACQPS    |            |    |    |            |         |            |       |
| R/W      |            |    |    |            |         |            |       |
| 0h       |            |    |    |            |         |            |       |

**Table 3-232. ADC\_CFG\_ADCSOC15CTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                       |
|-------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28 | EXTCHSEL   | R/W  | 0h    | SOC15 External Channel Mux Select. Selects the external mux combination to output when SOC15 is received by the ADC. Some or all of the ADCEXTMUX lines can be enabled via the device GPIO mux to control an external analog mux. |
| 27    | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                          |

**Table 3-232. ADC\_CFG\_ADCSOC15CTL Register Field Descriptions (continued)**

| Bit   | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|---------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:20 | TRIGSEL | R/W  | 0h    | <p>SOC15 Trigger Source Select. Along with the SOC15 field in the ADCINTSOCSEL1 register, this bit field configures which trigger will set the SOC15 flag in the ADCSOCFLG1 register to initiate a conversion to start once priority is given to it.</p> <p>Note: SOCFRC1 register can always be used to software trigger SOC15 in addition to any hardware trigger configuration.</p> <p>00h ADCTRIG0 - Software only<br/> 01h ADCTRIG1 - RTI0 Timer<br/> 02h ADCTRIG2 - RTI1 Timer<br/> 03h ADCTRIG3 - RTI2 Timer<br/> 04h ADCTRIG4 - RTI3 Timer<br/> 05h ADCTRIG5 - InputXBAR.Out[5]<br/> 06h ADCTRIG6 - spare<br/> 07h ADCTRIG7 - spare<br/> 08h ADCTRIG8 - EPWM0, ADCSOCA<br/> 09h ADCTRIG9 - EPWM0, ADCSOCB<br/> 0Ah ADCTRIG10 - EPWM1, ADCSOCA<br/> 0Bh ADCTRIG11 - EPWM1, ADCSOCB<br/> 0Ch ADCTRIG12 - EPWM2, ADCSOCA<br/> 0Dh ADCTRIG13 - EPWM2, ADCSOCB<br/> 0Eh ADCTRIG14 - EPWM3, ADCSOCA<br/> 0Fh ADCTRIG15 - EPWM3, ADCSOCB<br/> .... EPWM4 to EPWM27<br/> 40h ADCTRIG64 - EPWM28, ADCSOCA<br/> 41h ADCTRIG65 - EPWM28, ADCSOCB<br/> 42h ADCTRIG66 - EPWM29, ADCSOCA<br/> 43h ADCTRIG67 - EPWM29, ADCSOCB<br/> 44h ADCTRIG68 - EPWM30, ADCSOCA<br/> 45h ADCTRIG69 - EPWM30, ADCSOCB<br/> 46h ADCTRIG70 - EPWM31, ADCSOCA<br/> 47h ADCTRIG71 - EPWM31, ADCSOCB<br/> 48h ADCTRIG72 - ECAP0, TRIGOUT<br/> .... ECAP1 to ECAP8<br/> 51h ADCTRIG81 - ECAP9, TRIGOUT<br/> 52h ADCTRIG82 - ECAP10, TRIGOUT<br/> ....<br/> 57h ADCTRIG87 - ECAP15, TRIGOUT<br/> 58h ADCTRIG88 - RTI4 Timer<br/> 59h ADCTRIG89 - RTI5 Timer<br/> 5Ah ADCTRIG90 - RTI6 Timer<br/> 5Bh ADCTRIG91 - RTI7 Timer<br/> ....<br/> 7Fh ADCTRIG127 - REP2TRIG - these are not external trigger signals on the ADC IP port. We need to configure them for internal selection of repeater triggers.</p> |

**Table 3-232. ADC\_CFG\_ADCSOC15CTL Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19:15 | CHSEL      | R/W  | 0h    | <p>SOC15 Channel Select. Selects the channel to be converted when SOC15 is received by the ADC.</p> <p>Single-ended Signaling Mode [SIGNALMODE = 0]:</p> <p>00h ADCIN0</p> <p>01h ADCIN1</p> <p>02h ADCIN2</p> <p>03h ADCIN3</p> <p>...</p> <p>1Dh ADCIN29</p> <p>1Eh ADCIN30</p> <p>1Fh ADCIN31</p> <p>Differential Signaling Mode [SIGNALMODE = 1]:</p> <p>00h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>01h ADCIN0 [non-inverting] and ADCIN1 [inverting]</p> <p>02h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>03h ADCIN2 [non-inverting] and ADCIN3 [inverting]</p> <p>04h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>05h ADCIN4 [non-inverting] and ADCIN5 [inverting]</p> <p>...</p> <p>0Eh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>0Fh ADCIN26 [non-inverting] and ADCIN27 [inverting]</p> <p>10h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>11h ADCIN28 [non-inverting] and ADCIN29 [inverting]</p> <p>1Eh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> <p>1Fh ADCIN30 [non-inverting] and ADCIN31 [inverting]</p> |
| 14:12 | RESOLUTION | R    | 0h    | Placeholder for per-SOC resolution                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 11:10 | SIGNALMODE | R    | 0h    | Placeholder for per-SOC signal mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 9     | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 8:0   | ACQPS      | R/W  | 0h    | <p>SOC15 Acquisition Prescale. Controls the sample and hold window for this SOC.</p> <p>000h Reserved</p> <p>001h Reserved</p> <p>002h Sample window is 3 system clock cycles wide</p> <p>003h Sample window is 4 system clock cycles wide</p> <p>...</p> <p>1FFh Sample window is 512 system clock cycles wide</p> <p>The configured acquisition time must be at least as long as one ADCCLK cycle for correct ADC operation. The configured acquisition time must also be at least 3 SYSCLK cycles long. The device datasheet will also specify a minimum sample and hold window duration.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

### 3.2.2.77 ADC\_CFG\_ADCEVTSTAT Register

#### 1 ADC\_CFG\_ADCEVTSTAT Register (Offset = 60h) [reset = 0h]

ADC Event Status Register.

Return to [Summary Table](#)

**Table 3-233. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0060h       |
| ADC1_G0_G5    | 502C 1060h       |
| ADC2_G0_G5    | 502C 2060h       |
| ADC3_G0_G5    | 502C 3060h       |
| ADC4_G0_G5    | 502C 4060h       |

**Figure 3-77. ADC\_CFG\_ADCEVTSTAT Name Register**

| 15         | 14       | 13         | 12         | 11         | 10       | 9          | 8          |
|------------|----------|------------|------------|------------|----------|------------|------------|
| RESERVED_4 | PPB4ZERO | PPB4TRIPLO | PPB4TRIPHI | RESERVED_3 | PPB3ZERO | PPB3TRIPLO | PPB3TRIPHI |
| R          | R        | R          | R          | R          | R        | R          | R          |
| 0h         | 0h       | 0h         | 0h         | 0h         | 0h       | 0h         | 0h         |
| 7          | 6        | 5          | 4          | 3          | 2        | 1          | 0          |
| RESERVED_2 | PPB2ZERO | PPB2TRIPLO | PPB2TRIPHI | RESERVED_1 | PPB1ZERO | PPB1TRIPLO | PPB1TRIPHI |
| R          | R        | R          | R          | R          | R        | R          | R          |
| 0h         | 0h       | 0h         | 0h         | 0h         | 0h       | 0h         | 0h         |

**Table 3-235. ADC\_CFG\_ADCEVTSTAT Register Field Descriptions**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | RESERVED_4 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 14  | PPB4ZERO   | R    | 0h    | Post Processing Block 4 Zero Crossing Flag. When set indicates the ADCPPB4RESULT register has changed sign. This bit is gated by EOC signal.<br>Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt.<br>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority |
| 13  | PPB4TRIPLO | R    | 0h    | Post Processing Block 4 Trip Low Flag. When set indicates a digital compare trip low event has occurred.<br>Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt.<br>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority                                     |
| 12  | PPB4TRIPHI | R    | 0h    | Post Processing Block 4 Trip High Flag. When set indicates a digital compare trip high event has occurred.<br>Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt.<br>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority                                   |
| 11  | RESERVED_3 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

**Table 3-235. ADC\_CFG\_ADCEVTSTAT Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | PPB3ZERO   | R    | 0h    | Post Processing Block 3 Zero Crossing Flag. When set indicates the ADCPPB3RESULT register has changed sign. This bit is gated by EOC signal.<br>Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt.<br>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority |
| 9   | PPB3TRIPLO | R    | 0h    | Post Processing Block 3 Trip Low Flag. When set indicates a digital compare trip low event has occurred.<br>Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt.<br>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority                                     |
| 8   | PPB3TRIPHI | R    | 0h    | Post Processing Block 3 Trip High Flag. When set indicates a digital compare trip high event has occurred.<br>Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt.<br>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority                                   |
| 7   | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 6   | PPB2ZERO   | R    | 0h    | Post Processing Block 2 Zero Crossing Flag. When set indicates the ADCPPB2RESULT register has changed sign. This bit is gated by EOC signal.<br>Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt.<br>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority |
| 5   | PPB2TRIPLO | R    | 0h    | Post Processing Block 2 Trip Low Flag. When set indicates a digital compare trip low event has occurred.<br>Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt.<br>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority                                     |
| 4   | PPB2TRIPHI | R    | 0h    | Post Processing Block 2 Trip High Flag. When set indicates a digital compare trip high event has occurred.<br>Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt.<br>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority                                   |
| 3   | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 2   | PPB1ZERO   | R    | 0h    | Post Processing Block 1 Zero Crossing Flag. When set indicates the ADCPPB1RESULT register has changed sign. This bit is gated by EOC signal.<br>Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt.<br>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority |



**Table 3-235. ADC\_CFG\_ADCEVTSTAT Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-----|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | PPB1TRIPLO | R    | 0h    | <p>Post Processing Block 1 Trip Low Flag. When set indicates a digital compare trip low event has occurred.</p> <p>Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt.</p> <p>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority</p>   |
| 0   | PPB1TRIPHI | R    | 0h    | <p>Post Processing Block 1 Trip High Flag. When set indicates a digital compare trip high event has occurred.</p> <p>Note: these bits are set even when the corresponding enable in ADCEVTINTSEL is not set. Because of this, an ISR may need to examine both the ADCEVTSTAT and ADCEVTINTSEL registers to determine the source of the interrupt.</p> <p>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority</p> |

### 3.2.2.78 ADC\_CFG\_ADCEVTCLR Register

#### 1 ADC\_CFG\_ADCEVTCLR Register (Offset = 64h) [reset = 0h]

ADC Event Clear Register.

Return to [Summary Table](#)

**Table 3-236. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0064h       |
| ADC1_G0_G5    | 502C 1064h       |
| ADC2_G0_G5    | 502C 2064h       |
| ADC3_G0_G5    | 502C 3064h       |
| ADC4_G0_G5    | 502C 4064h       |

**Figure 3-78. ADC\_CFG\_ADCEVTCLR Name Register**

| 15         | 14       | 13         | 12         | 11         | 10       | 9          | 8          |
|------------|----------|------------|------------|------------|----------|------------|------------|
| RESERVED_4 | PPB4ZERO | PPB4TRIPLO | PPB4TRIPHI | RESERVED_3 | PPB3ZERO | PPB3TRIPLO | PPB3TRIPHI |
| R          | R/W1TS   | R/W1TS     | R/W1TS     | R          | R/W1TS   | R/W1TS     | R/W1TS     |
| 0h         | 0h       | 0h         | 0h         | 0h         | 0h       | 0h         | 0h         |
| 7          | 6        | 5          | 4          | 3          | 2        | 1          | 0          |
| RESERVED_2 | PPB2ZERO | PPB2TRIPLO | PPB2TRIPHI | RESERVED_1 | PPB1ZERO | PPB1TRIPLO | PPB1TRIPHI |
| R          | R/W1TS   | R/W1TS     | R/W1TS     | R          | R/W1TS   | R/W1TS     | R/W1TS     |
| 0h         | 0h       | 0h         | 0h         | 0h         | 0h       | 0h         | 0h         |

**Table 3-238. ADC\_CFG\_ADCEVTCLR Register Field Descriptions**

| Bit | Field      | Type   | Reset | Description                                                                                                                                                                                                                                            |
|-----|------------|--------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | RESERVED_4 | R      | 0h    | Reserved                                                                                                                                                                                                                                               |
| 14  | PPB4ZERO   | R/W1TS | 0h    | Post Processing Block 4 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register.<br>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority |
| 13  | PPB4TRIPLO | R/W1TS | 0h    | Post Processing Block 4 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register.<br>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority           |
| 12  | PPB4TRIPHI | R/W1TS | 0h    | Post Processing Block 4 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register.<br>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority         |
| 11  | RESERVED_3 | R      | 0h    | Reserved                                                                                                                                                                                                                                               |
| 10  | PPB3ZERO   | R/W1TS | 0h    | Post Processing Block 3 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register.<br>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority |
| 9   | PPB3TRIPLO | R/W1TS | 0h    | Post Processing Block 3 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register.<br>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority           |
| 8   | PPB3TRIPHI | R/W1TS | 0h    | Post Processing Block 3 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register.<br>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority         |
| 7   | RESERVED_2 | R      | 0h    | Reserved                                                                                                                                                                                                                                               |

**Table 3-238. ADC\_CFG\_ADCEVTCLR Register Field Descriptions (continued)**

| Bit | Field      | Type   | Reset | Description                                                                                                                                                                                                                                            |
|-----|------------|--------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6   | PPB2ZERO   | R/W1TS | 0h    | Post Processing Block 2 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register.<br>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority |
| 5   | PPB2TRIPLO | R/W1TS | 0h    | Post Processing Block 2 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register.<br>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority           |
| 4   | PPB2TRIPHI | R/W1TS | 0h    | Post Processing Block 2 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register.<br>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority         |
| 3   | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                                                                               |
| 2   | PPB1ZERO   | R/W1TS | 0h    | Post Processing Block 1 Zero Crossing Clear. Clears the corresponding zero crossing flag in the ADCEVTSTAT register.<br>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority |
| 1   | PPB1TRIPLO | R/W1TS | 0h    | Post Processing Block 1 Trip Low Clear. Clears the corresponding trip low flag in the ADCEVTSTAT register.<br>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority           |
| 0   | PPB1TRIPHI | R/W1TS | 0h    | Post Processing Block 1 Trip High Clear. Clears the corresponding trip high flag in the ADCEVTSTAT register.<br>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority         |

### 3.2.2.79 ADC\_CFG\_ADCEVTSEL Register

#### 1 ADC\_CFG\_ADCEVTSEL Register (Offset = 68h) [reset = 0h]

ADC Event Selection Register.

Return to [Summary Table](#)

**Table 3-239. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0068h       |
| ADC1_G0_G5    | 502C 1068h       |
| ADC2_G0_G5    | 502C 2068h       |
| ADC3_G0_G5    | 502C 3068h       |
| ADC4_G0_G5    | 502C 4068h       |

**Figure 3-79. ADC\_CFG\_ADCEVTSEL Name Register**

| 15         | 14       | 13         | 12         | 11         | 10       | 9          | 8          |
|------------|----------|------------|------------|------------|----------|------------|------------|
| RESERVED_4 | PPB4ZERO | PPB4TRIPLO | PPB4TRIPHI | RESERVED_3 | PPB3ZERO | PPB3TRIPLO | PPB3TRIPHI |
| R          | R/W      | R/W        | R/W        | R          | R/W      | R/W        | R/W        |
| 0h         | 0h       | 0h         | 0h         | 0h         | 0h       | 0h         | 0h         |
| 7          | 6        | 5          | 4          | 3          | 2        | 1          | 0          |
| RESERVED_2 | PPB2ZERO | PPB2TRIPLO | PPB2TRIPHI | RESERVED_1 | PPB1ZERO | PPB1TRIPLO | PPB1TRIPHI |
| R          | R/W      | R/W        | R/W        | R          | R/W      | R/W        | R/W        |
| 0h         | 0h       | 0h         | 0h         | 0h         | 0h       | 0h         | 0h         |

**Table 3-241. ADC\_CFG\_ADCEVTSEL Register Field Descriptions**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                 |
|-----|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | RESERVED_4 | R    | 0h    | Reserved                                                                                                                                                                                                                                                    |
| 14  | PPB4ZERO   | R/W  | 0h    | Post Processing Block 4 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks. |
| 13  | PPB4TRIPLO | R/W  | 0h    | Post Processing Block 4 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.           |
| 12  | PPB4TRIPHI | R/W  | 0h    | Post Processing Block 4 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.         |
| 11  | RESERVED_3 | R    | 0h    | Reserved                                                                                                                                                                                                                                                    |
| 10  | PPB3ZERO   | R/W  | 0h    | Post Processing Block 3 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks. |
| 9   | PPB3TRIPLO | R/W  | 0h    | Post Processing Block 3 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.           |
| 8   | PPB3TRIPHI | R/W  | 0h    | Post Processing Block 3 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.         |
| 7   | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                    |

**Table 3-241. ADC\_CFG\_ADCEVTSEL Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                 |
|-----|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6   | PPB2ZERO   | R/W  | 0h    | Post Processing Block 2 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks. |
| 5   | PPB2TRIPLO | R/W  | 0h    | Post Processing Block 2 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.           |
| 4   | PPB2TRIPHI | R/W  | 0h    | Post Processing Block 2 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.         |
| 3   | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                    |
| 2   | PPB1ZERO   | R/W  | 0h    | Post Processing Block 1 Zero Crossing Event Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks. |
| 1   | PPB1TRIPLO | R/W  | 0h    | Post Processing Block 1 Trip Low Event Enable. Setting this bit allows the corresponding rising trip low flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.           |
| 0   | PPB1TRIPHI | R/W  | 0h    | Post Processing Block 1 Trip High Event Enable. Setting this bit allows the corresponding rising trip high flag to activate the event signal to the PWM blocks. The flag must be cleared before it can produce additional events to the PWM blocks.         |

### 3.2.2.80 ADC\_CFG\_ADCEVTINTSEL Register

#### 1 ADC\_CFG\_ADCEVTINTSEL Register (Offset = 6Ch) [reset = 0h]

ADC Event Interrupt Selection Register.

Return to [Summary Table](#)

**Table 3-242. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 006Ch       |
| ADC1_G0_G5    | 502C 106Ch       |
| ADC2_G0_G5    | 502C 206Ch       |
| ADC3_G0_G5    | 502C 306Ch       |
| ADC4_G0_G5    | 502C 406Ch       |

**Figure 3-80. ADC\_CFG\_ADCEVTINTSEL Name Register**

| 15         | 14       | 13         | 12         | 11         | 10       | 9          | 8          |
|------------|----------|------------|------------|------------|----------|------------|------------|
| RESERVED_4 | PPB4ZERO | PPB4TRIPLO | PPB4TRIPHI | RESERVED_3 | PPB3ZERO | PPB3TRIPLO | PPB3TRIPHI |
| R          | R/W      | R/W        | R/W        | R          | R/W      | R/W        | R/W        |
| 0h         | 0h       | 0h         | 0h         | 0h         | 0h       | 0h         | 0h         |
| 7          | 6        | 5          | 4          | 3          | 2        | 1          | 0          |
| RESERVED_2 | PPB2ZERO | PPB2TRIPLO | PPB2TRIPHI | RESERVED_1 | PPB1ZERO | PPB1TRIPLO | PPB1TRIPHI |
| R          | R/W      | R/W        | R/W        | R          | R/W      | R/W        | R/W        |
| 0h         | 0h       | 0h         | 0h         | 0h         | 0h       | 0h         | 0h         |

**Table 3-244. ADC\_CFG\_ADCEVTINTSEL Register Field Descriptions**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                     |
|-----|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | RESERVED_4 | R    | 0h    | Reserved                                                                                                                                                                                                                                                        |
| 14  | PPB4ZERO   | R/W  | 0h    | Post Processing Block 4 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE. |
| 13  | PPB4TRIPLO | R/W  | 0h    | Post Processing Block 4 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.           |
| 12  | PPB4TRIPHI | R/W  | 0h    | Post Processing Block 4 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.         |
| 11  | RESERVED_3 | R    | 0h    | Reserved                                                                                                                                                                                                                                                        |
| 10  | PPB3ZERO   | R/W  | 0h    | Post Processing Block 3 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE. |
| 9   | PPB3TRIPLO | R/W  | 0h    | Post Processing Block 3 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.           |
| 8   | PPB3TRIPHI | R/W  | 0h    | Post Processing Block 3 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.         |
| 7   | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                        |

**Table 3-244. ADC\_CFG\_ADCEVTINTSEL Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                     |
|-----|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6   | PPB2ZERO   | R/W  | 0h    | Post Processing Block 2 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE. |
| 5   | PPB2TRIPLO | R/W  | 0h    | Post Processing Block 2 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.           |
| 4   | PPB2TRIPHI | R/W  | 0h    | Post Processing Block 2 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.         |
| 3   | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                        |
| 2   | PPB1ZERO   | R/W  | 0h    | Post Processing Block 1 Zero Crossing Interrupt Enable. Setting this bit allows the corresponding rising zero crossing flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE. |
| 1   | PPB1TRIPLO | R/W  | 0h    | Post Processing Block 1 Trip Low Interrupt Enable. Setting this bit allows the corresponding rising trip low flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.           |
| 0   | PPB1TRIPHI | R/W  | 0h    | Post Processing Block 1 Trip High Interrupt Enable. Setting this bit allows the corresponding rising trip high flag to activate the event interrupt signal to the PIE. The flag must be cleared before it can produce additional interrupts to the PIE.         |

### 3.2.2.81 ADC\_CFG\_ADCOSDETECT Register

#### 1 ADC\_CFG\_ADCOSDETECT Register (Offset = 70h) [reset = 0h]

ADC Open and Shorts Detect Register.

Return to [Summary Table](#)

**Table 3-245. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0070h       |
| ADC1_G0_G5    | 502C 1070h       |
| ADC2_G0_G5    | 502C 2070h       |
| ADC3_G0_G5    | 502C 3070h       |
| ADC4_G0_G5    | 502C 4070h       |

**Figure 3-81. ADC\_CFG\_ADCOSDETECT Name Register**

|            |    |    |    |           |    |   |   |
|------------|----|----|----|-----------|----|---|---|
| 15         | 14 | 13 | 12 | 11        | 10 | 9 | 8 |
| RESERVED_1 |    |    |    |           |    |   |   |
| R          |    |    |    |           |    |   |   |
| 0h         |    |    |    |           |    |   |   |
| 7          | 6  | 5  | 4  | 3         | 2  | 1 | 0 |
| RESERVED_1 |    |    |    | DETECTCFG |    |   |   |
| R          |    |    |    | R/W       |    |   |   |
| 0h         |    |    |    | 0h        |    |   |   |

**Table 3-247. ADC\_CFG\_ADCOSDETECT Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:3 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 2:0  | DETECTCFG  | R/W  | 0h    | ADC Opens and Shorts Detect Configuration. This bit field defines the open/shorts detection circuit state.<br>0h Open/Shorts detection circuit is disabled.<br>1h Open/Shorts detection circuit is enabled at zero scale.<br>2h Open/Shorts detection circuit is enabled at full scale.<br>3h Open/Shorts detection circuit is enabled at [nominal] 5/12 scale.<br>4h Open/Shorts detection circuit is enabled at [nominal] 7/12 scale.<br>5h Open/Shorts detection circuit is enabled with a [nominal] 5K pulldown to VSSA.<br>6h Open/Shorts detection circuit is enabled with a [nominal] 5K pullup to VDPA.<br>7h Open/Shorts detection circuit is enabled with a [nominal] 7K pulldown to VSSA. |



### 3.2.2.82 ADC\_CFG\_ADCCOUNTER Register

#### 1 ADC\_CFG\_ADCCOUNTER Register (Offset = 72h) [reset = 0h]

ADC Counter Register.

Return to [Summary Table](#)

**Table 3-248. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0072h       |
| ADC1_G0_G5    | 502C 1072h       |
| ADC2_G0_G5    | 502C 2072h       |
| ADC3_G0_G5    | 502C 3072h       |
| ADC4_G0_G5    | 502C 4072h       |

**Figure 3-82. ADC\_CFG\_ADCCOUNTER Name Register**

|            |    |    |    |           |    |   |   |
|------------|----|----|----|-----------|----|---|---|
| 15         | 14 | 13 | 12 | 11        | 10 | 9 | 8 |
| RESERVED_1 |    |    |    | FREECOUNT |    |   |   |
| R          |    |    |    | R         |    |   |   |
| 0h         |    |    |    | 0h        |    |   |   |
| 7          | 6  | 5  | 4  | 3         | 2  | 1 | 0 |
| FREECOUNT  |    |    |    |           |    |   |   |
| R          |    |    |    |           |    |   |   |
| 0h         |    |    |    |           |    |   |   |

**Table 3-250. ADC\_CFG\_ADCCOUNTER Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                         |
|-------|------------|------|-------|-----------------------------------------------------------------------------------------------------|
| 15:12 | RESERVED_1 | R    | 0h    | Reserved                                                                                            |
| 11:0  | FREECOUNT  | R    | 0h    | ADC Free Running Counter Value. This bit field reflects the status of the free running ADC counter. |

### 3.2.2.83 ADC\_CFG\_ADCREV Register

#### 1 ADC\_CFG\_ADCREV Register (Offset = 74h) [reset = 105h]

ADC Revision Register.

Return to [Summary Table](#)

**Table 3-251. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0074h       |
| ADC1_G0_G5    | 502C 1074h       |
| ADC2_G0_G5    | 502C 2074h       |
| ADC3_G0_G5    | 502C 3074h       |
| ADC4_G0_G5    | 502C 4074h       |

**Figure 3-83. ADC\_CFG\_ADCREV Name Register**

|      |    |    |    |    |    |   |   |
|------|----|----|----|----|----|---|---|
| 15   | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| REV  |    |    |    |    |    |   |   |
| R    |    |    |    |    |    |   |   |
| 1h   |    |    |    |    |    |   |   |
| 7    | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| TYPE |    |    |    |    |    |   |   |
| R    |    |    |    |    |    |   |   |
| 5h   |    |    |    |    |    |   |   |

**Table 3-253. ADC\_CFG\_ADCREV Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                            |
|------|-------|------|-------|--------------------------------------------------------------------------------------------------------|
| 15:8 | REV   | R    | 1h    | ADC Revision. To allow documentation of differences between revisions. First version is labeled as 00h |
| 7:0  | TYPE  | R    | 5h    | ADC Type. Always set to 5 for this ADC.                                                                |

### 3.2.2.84 ADC\_CFG\_ADCCOFFTRIM Register

#### 1 ADC\_CFG\_ADCCOFFTRIM Register (Offset = 76h) [reset = 0h]

ADC Offset Trim Register.

Return to [Summary Table](#)

**Table 3-254. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0076h       |
| ADC1_G0_G5    | 502C 1076h       |
| ADC2_G0_G5    | 502C 2076h       |
| ADC3_G0_G5    | 502C 3076h       |
| ADC4_G0_G5    | 502C 4076h       |

**Figure 3-84. ADC\_CFG\_ADCCOFFTRIM Name Register**

|                 |    |    |    |    |    |   |   |
|-----------------|----|----|----|----|----|---|---|
| 15              | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| OFFTRIM12BSEODD |    |    |    |    |    |   |   |
| R/W             |    |    |    |    |    |   |   |
| 0h              |    |    |    |    |    |   |   |
| 7               | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| OFFTRIM         |    |    |    |    |    |   |   |
| R/W             |    |    |    |    |    |   |   |
| 0h              |    |    |    |    |    |   |   |

**Table 3-256. ADC\_CFG\_ADCCOFFTRIM Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------|-----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | OFFTRIM12BSEODD | R/W  | 0h    | If ADCCLT2.OFFTRIMMODE = 1, then this register will supply offset trim when the ADC is in 12-bit single-ended mode for odd channels. Range is +127 steps to -128 steps [2's compliment format]. Regardless of the converter resolution, the size of each trim step is [VREFHI-VREFLO]/65536.                                                                                                                                                                                                                                                                                                                                                                                                        |
| 7:0  | OFFTRIM         | R/W  | 0h    | ADC Offset Trim. Adjusts the conversion results of the converter up or down to account for offset error in the ADC. A different offset trim is required for each combination of resolution and signal mode. If ADCCLT2.OFFTRIMMODE = 0, then using the AdcSetMode function to set the resolution and signal mode will ensure that the correct offset trim is loaded into this register. If ADCCLT2.OFFTRIMMODE = 1, then this register will supply offset trim only when the ADC is in 12-bit single-ended mode and only for even channels. Range is +127 steps to -128 steps [2's compliment format]. Regardless of the converter resolution, the size of each trim step is [VREFHI-VREFLO]/65536. |

### 3.2.2.85 ADC\_CFG\_ADCOFFTRIM3 Register

#### 1 ADC\_CFG\_ADCOFFTRIM3 Register (Offset = 7Ah) [reset = 0h]

ADC Offset Trim Register.

Return to [Summary Table](#)

**Table 3-257. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 007Ah       |
| ADC1_G0_G5    | 502C 107Ah       |
| ADC2_G0_G5    | 502C 207Ah       |
| ADC3_G0_G5    | 502C 307Ah       |
| ADC4_G0_G5    | 502C 407Ah       |

**Figure 3-85. ADC\_CFG\_ADCOFFTRIM3 Name Register**

|              |    |    |    |    |    |   |   |
|--------------|----|----|----|----|----|---|---|
| 15           | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RSVD         |    |    |    |    |    |   |   |
| 0h           |    |    |    |    |    |   |   |
| 7            | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| OFFTRIM12BDE |    |    |    |    |    |   |   |
| R/W          |    |    |    |    |    |   |   |
| 0h           |    |    |    |    |    |   |   |

**Table 3-259. ADC\_CFG\_ADCOFFTRIM3 Register Field Descriptions**

| Bit | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                       |
|-----|--------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | OFFTRIM12BDE | R/W  | 0h    | If ADCCLT2.OFFTRIMMODE = 1, then this register will supply offset trim when the ADC is in 12-bit differential mode.<br>Range is +127 steps to -128 steps [2's compliment format].<br>Regardless of the converter resolution, the size of each trim step is [VREFHI-VREFLO]/65536. |

### 3.2.2.86 ADC\_CFG\_ADCPPB1CONFIG Register

#### 1 ADC\_CFG\_ADCPPB1CONFIG Register (Offset = 80h) [reset = 0h]

ADC PPB1 Config Register.

Return to [Summary Table](#)

**Table 3-260. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0080h       |
| ADC1_G0_G5    | 502C 1080h       |
| ADC2_G0_G5    | 502C 2080h       |
| ADC3_G0_G5    | 502C 3080h       |
| ADC4_G0_G5    | 502C 4080h       |

**Figure 3-86. ADC\_CFG\_ADCPPB1CONFIG Name Register**

|            |       |       |            |        |    |   |   |
|------------|-------|-------|------------|--------|----|---|---|
| 15         | 14    | 13    | 12         | 11     | 10 | 9 | 8 |
| RESERVED_1 |       |       |            |        |    |   |   |
| R          |       |       |            |        |    |   |   |
| 0h         |       |       |            |        |    |   |   |
| 7          | 6     | 5     | 4          | 3      | 2  | 1 | 0 |
| RESERVED_1 | ABSEN | CBCEN | TWOSCOMPEN | CONFIG |    |   |   |
| R          | R/W   | R/W   | R/W        | R/W    |    |   |   |
| 0h         | 0h    | 0h    | 0h         | 0h     |    |   |   |

**Table 3-262. ADC\_CFG\_ADCPPB1CONFIG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:7 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                               |
| 6    | ABSEN      | R/W  | 0h    | ADC Post Processing Block 1 Absolute Value Enable. When set this bit enables absolute value calculation on the ADCRESULTx associated with ADCPPB1.<br>This occurs before the TWOSCOMPEN logic is evaluated [so enabling both TWOSCOMPEN and ABSEN will always result in a negative value stored in ADCPPBxRESULT]<br>0 ADCPPB1RESULT = ADCRESULTx - ADCPPB1OFFREF<br>1 ADCPPB1RESULT = abs[ADCRESULTx - ADCPPB1OFFREF] |
| 5    | CBCEN      | R/W  | 0h    | ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present.                                                                                                                                                                                         |
| 4    | TWOSCOMPEN | R/W  | 0h    | ADC Post Processing Block 1 Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the ADCPPB1RESULT register.<br>0 ADCPPB1RESULT = ADCRESULTx - ADCPPB1OFFREF<br>1 ADCPPB1RESULT = ADCPPB1OFFREF - ADCRESULTx                                        |

**Table 3-262. ADC\_CFG\_ADCPPB1CONFIG Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|--------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0 | CONFIG | R/W  | 0h    | <p>ADC Post Processing Block 1 Configuration. This bit field defines which SOC/EOC/RESULT is associated with this post processing block.</p> <p>0000 SOC0/EOC0/RESULT0 is associated with post processing block 1</p> <p>0001 SOC1/EOC1/RESULT1 is associated with post processing block 1</p> <p>0010 SOC2/EOC2/RESULT2 is associated with post processing block 1</p> <p>0011 SOC3/EOC3/RESULT3 is associated with post processing block 1</p> <p>0100 SOC4/EOC4/RESULT4 is associated with post processing block 1</p> <p>0101 SOC5/EOC5/RESULT5 is associated with post processing block 1</p> <p>0110 SOC6/EOC6/RESULT6 is associated with post processing block 1</p> <p>0111 SOC7/EOC7/RESULT7 is associated with post processing block 1</p> <p>1000 SOC8/EOC8/RESULT8 is associated with post processing block 1</p> <p>1001 SOC9/EOC9/RESULT9 is associated with post processing block 1</p> <p>1010 SOC10/EOC10/RESULT10 is associated with post processing block 1</p> <p>1011 SOC11/EOC11/RESULT11 is associated with post processing block 1</p> <p>1100 SOC12/EOC12/RESULT12 is associated with post processing block 1</p> <p>1101 SOC13/EOC13/RESULT13 is associated with post processing block 1</p> <p>1110 SOC14/EOC14/RESULT14 is associated with post processing block 1</p> <p>1111 SOC15/EOC15/RESULT15 is associated with post processing block 1</p> |

### 3.2.2.87 ADC\_CFG\_ADCPPB1STAMP Register

#### 1 ADC\_CFG\_ADCPPB1STAMP Register (Offset = 82h) [reset = 0h]

ADC PPB1 Sample Delay Time Stamp Register.

Return to [Summary Table](#)

**Table 3-263. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0082h       |
| ADC1_G0_G5    | 502C 1082h       |
| ADC2_G0_G5    | 502C 2082h       |
| ADC3_G0_G5    | 502C 3082h       |
| ADC4_G0_G5    | 502C 4082h       |

**Figure 3-87. ADC\_CFG\_ADCPPB1STAMP Name Register**

|            |    |    |    |          |    |   |   |
|------------|----|----|----|----------|----|---|---|
| 15         | 14 | 13 | 12 | 11       | 10 | 9 | 8 |
| RESERVED_1 |    |    |    | DLYSTAMP |    |   |   |
| R          |    |    |    | R        |    |   |   |
| 0h         |    |    |    | 0h       |    |   |   |
| 7          | 6  | 5  | 4  | 3        | 2  | 1 | 0 |
| DLYSTAMP   |    |    |    |          |    |   |   |
| R          |    |    |    |          |    |   |   |
| 0h         |    |    |    |          |    |   |   |

**Table 3-265. ADC\_CFG\_ADCPPB1STAMP Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                       |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                          |
| 11:0  | DLYSTAMP   | R    | 0h    | ADC Post Processing Block 1 Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample. |

### 3.2.2.88 ADC\_CFG\_ADCPPB1OFFCAL Register

#### 1 ADC\_CFG\_ADCPPB1OFFCAL Register (Offset = 84h) [reset = 0h]

ADC PPB1 Offset Calibration Register.

Return to [Summary Table](#)

**Table 3-266. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0084h       |
| ADC1_G0_G5    | 502C 1084h       |
| ADC2_G0_G5    | 502C 2084h       |
| ADC3_G0_G5    | 502C 3084h       |
| ADC4_G0_G5    | 502C 4084h       |

**Figure 3-88. ADC\_CFG\_ADCPPB1OFFCAL Name Register**

|            |    |    |    |    |    |        |   |
|------------|----|----|----|----|----|--------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9      | 8 |
| RESERVED_1 |    |    |    |    |    | OFFCAL |   |
| R          |    |    |    |    |    | R/W    |   |
| 0h         |    |    |    |    |    | 0h     |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1      | 0 |
| OFFCAL     |    |    |    |    |    |        |   |
| R/W        |    |    |    |    |    |        |   |
| 0h         |    |    |    |    |    |        |   |

**Table 3-268. ADC\_CFG\_ADCPPB1OFFCAL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 9:0   | OFFCAL     | R/W  | 0h    | <p>ADC Post Processing Block 1 Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register.</p> <p>000h No change. The ADC output is stored directly into ADCRESULT.</p> <p>001h ADC output - 1 is stored into ADCRESULT.</p> <p>002h ADC output - 2 is stored into ADCRESULT.</p> <p>...</p> <p>200h ADC output + 512 is stored into ADCRESULT.</p> <p>...</p> <p>3FFh ADC output + 1 is stored into ADCRESULT.</p> <p>NOTE: In 16-bit mode, the subtraction will saturate at 0000h and FFFFh before being stored into the ADCRESULT register.</p> <p>In 12-bit mode, the subtraction will saturate at 0000h and 0FFFh before being stored into the ADCRESULT register.</p> <p>Note: in the case that multiple PPBs point to the same SOC, only the OFFCAL of the lowest numbered PPB will be applied.</p> |



### 3.2.2.89 ADC\_CFG\_ADCPPB1OFFREF Register

#### 1 ADC\_CFG\_ADCPPB1OFFREF Register (Offset = 86h) [reset = 0h]

ADC PPB1 Offset Reference Register.

Return to [Summary Table](#)

**Table 3-269. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0086h       |
| ADC1_G0_G5    | 502C 1086h       |
| ADC2_G0_G5    | 502C 2086h       |
| ADC3_G0_G5    | 502C 3086h       |
| ADC4_G0_G5    | 502C 4086h       |

**Figure 3-89. ADC\_CFG\_ADCPPB1OFFREF Name Register**

|        |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| OFFREF |    |    |    |    |    |   |   |
| R/W    |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |
| 7      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| OFFREF |    |    |    |    |    |   |   |
| R/W    |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |

**Table 3-271. ADC\_CFG\_ADCPPB1OFFREF Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|--------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | OFFREF | R/W  | 0h    | <p>ADC Post Processing Block 1 Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB1RESULT register. This subtraction is not saturated.</p> <p>0000h No change. The ADCRESULT value is passed on.<br/> 0001h ADCRESULT - 1 is passed on.<br/> 0002h ADCRESULT - 2 is passed on.<br/> ...<br/> 8000h ADCRESULT - 32,768 is passed on.<br/> ...<br/> FFFFh ADCRESULT - 65,535 is passed on.</p> <p>NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.</p> |

### 3.2.2.90 ADC\_CFG\_ADCPPB1TRIPHI Register

#### 1 ADC\_CFG\_ADCPPB1TRIPHI Register (Offset = 88h) [reset = 0h]

ADC PPB1 Trip High Register.

Return to [Summary Table](#)

**Table 3-272. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0088h       |
| ADC1_G0_G5    | 502C 1088h       |
| ADC2_G0_G5    | 502C 2088h       |
| ADC3_G0_G5    | 502C 3088h       |
| ADC4_G0_G5    | 502C 4088h       |

**Figure 3-90. ADC\_CFG\_ADCPPB1TRIPHI Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_1 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LIMITHI    |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| LIMITHI    |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LIMITHI    |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 3-274. ADC\_CFG\_ADCPPB1TRIPHI Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                              |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                 |
| 23:0  | LIMITHI    | R/W  | 0h    | ADC Post Processing Block 1 Trip High Limit. This value sets the digital comparator trip high limit.<br>When comparing to an ADCPPBxRESULT register, the upper bits will be ignored:<br>- TRIPHI[23:17] will be ignored in 16 bit mode<br>- TRIPHI[23:13] will be ignored in 12 bit mode |

### 3.2.2.91 ADC\_CFG\_ADCPPB1TRIPLO Register

#### 1 ADC\_CFG\_ADCPPB1TRIPLO Register (Offset = 8Ch) [reset = 0h]

ADC PPB1 Trip Low/Trigger Time Stamp Register.

Return to [Summary Table](#)

**Table 3-275. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 008Ch       |
| ADC1_G0_G5    | 502C 108Ch       |
| ADC2_G0_G5    | 502C 208Ch       |
| ADC3_G0_G5    | 502C 308Ch       |
| ADC4_G0_G5    | 502C 408Ch       |

**Figure 3-91. ADC\_CFG\_ADCPPB1TRIPLO Name Register**

|          |    |    |    |            |            |    |       |
|----------|----|----|----|------------|------------|----|-------|
| 31       | 30 | 29 | 28 | 27         | 26         | 25 | 24    |
| REQSTAMP |    |    |    |            |            |    |       |
| R        |    |    |    |            |            |    |       |
| 0h       |    |    |    |            |            |    |       |
| 23       | 22 | 21 | 20 | 19         | 18         | 17 | 16    |
| REQSTAMP |    |    |    | LIMITLO2EN | RESERVED_1 |    | LSIGN |
| R        |    |    |    | R/W        | R          |    | R/W   |
| 0h       |    |    |    | 0h         | 0h         |    | 0h    |
| 15       | 14 | 13 | 12 | 11         | 10         | 9  | 8     |
| LIMITLO  |    |    |    |            |            |    |       |
| R/W      |    |    |    |            |            |    |       |
| 0h       |    |    |    |            |            |    |       |
| 7        | 6  | 5  | 4  | 3          | 2          | 1  | 0     |
| LIMITLO  |    |    |    |            |            |    |       |
| R/W      |    |    |    |            |            |    |       |
| 0h       |    |    |    |            |            |    |       |

**Table 3-277. ADC\_CFG\_ADCPPB1TRIPLO Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                        |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | REQSTAMP   | R    | 0h    | ADC Post Processing Block 1 Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.                                                                                                                                                            |
| 19    | LIMITLO2EN | R/W  | 0h    | Extended Low Limit 2 Enable.<br>0 = Low limit set by ADCPPB1TRIPLO register. Not compatible with comparison with ADCPPB1PSUM or ADCPPB1SUM<br>1 = Low limit set by ADCPPB1TRIPLO2 register                                                                                                                                                         |
| 18:17 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                           |
| 16    | LSIGN      | R/W  | 0h    | Low Limit Sign Bit. This is the sign bit [17th bit] to the LIMITLO bit field when in 16-bit ADC mode.                                                                                                                                                                                                                                              |
| 15:0  | LIMITLO    | R/W  | 0h    | ADC Post Processing Block 1 Trip Low Limit. This value sets the digital comparator trip low limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB1RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRESULT bit field of the ADCPPB1RESULT register. |

### 3.2.2.92 ADC\_CFG\_ADCPPB2CONFIG Register

#### 1 ADC\_CFG\_ADCPPB2CONFIG Register (Offset = 90h) [reset = 1h]

ADC PPB2 Config Register.

Return to [Summary Table](#)

**Table 3-278. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0090h       |
| ADC1_G0_G5    | 502C 1090h       |
| ADC2_G0_G5    | 502C 2090h       |
| ADC3_G0_G5    | 502C 3090h       |
| ADC4_G0_G5    | 502C 4090h       |

**Figure 3-92. ADC\_CFG\_ADCPPB2CONFIG Name Register**

|            |       |       |            |        |    |   |   |
|------------|-------|-------|------------|--------|----|---|---|
| 15         | 14    | 13    | 12         | 11     | 10 | 9 | 8 |
| RESERVED_1 |       |       |            |        |    |   |   |
| R          |       |       |            |        |    |   |   |
| 0h         |       |       |            |        |    |   |   |
| 7          | 6     | 5     | 4          | 3      | 2  | 1 | 0 |
| RESERVED_1 | ABSEN | CBCEN | TWOSCOMPEN | CONFIG |    |   |   |
| R          | R/W   | R/W   | R/W        | R/W    |    |   |   |
| 0h         | 0h    | 0h    | 0h         | 1h     |    |   |   |

**Table 3-280. ADC\_CFG\_ADCPPB2CONFIG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:7 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                               |
| 6    | ABSEN      | R/W  | 0h    | ADC Post Processing Block 2 Absolute Value Enable. When set this bit enables absolute value calculation on the ADCRESULTx associated with ADCPPB2.<br>This occurs before the TWOSCOMPEN logic is evaluated [so enabling both TWOSCOMPEN and ABSEN will always result in a negative value stored in ADCPPBxRESULT]<br>0 ADCPPB2RESULT = ADCRESULTx - ADCPPB2OFFREF<br>1 ADCPPB2RESULT = abs[ADCRESULTx - ADCPPB2OFFREF] |
| 5    | CBCEN      | R/W  | 0h    | ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present.                                                                                                                                                                                         |
| 4    | TWOSCOMPEN | R/W  | 0h    | ADC Post Processing Block 2 Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the ADCPPB2RESULT register.<br>0 ADCPPB2RESULT = ADCRESULTx - ADCPPB2OFFREF<br>1 ADCPPB2RESULT = ADCPPB2OFFREF - ADCRESULTx                                        |

**Table 3-280. ADC\_CFG\_ADCPPB2CONFIG Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|--------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0 | CONFIG | R/W  | 1h    | <p>ADC Post Processing Block 2 Configuration. This bit field defines which SOC/EOC/RESULT is associated with this post processing block.</p> <p>0000 SOC0/EOC0/RESULT0 is associated with post processing block 2</p> <p>0001 SOC1/EOC1/RESULT1 is associated with post processing block 2</p> <p>0010 SOC2/EOC2/RESULT2 is associated with post processing block 2</p> <p>0011 SOC3/EOC3/RESULT3 is associated with post processing block 2</p> <p>0100 SOC4/EOC4/RESULT4 is associated with post processing block 2</p> <p>0101 SOC5/EOC5/RESULT5 is associated with post processing block 2</p> <p>0110 SOC6/EOC6/RESULT6 is associated with post processing block 2</p> <p>0111 SOC7/EOC7/RESULT7 is associated with post processing block 2</p> <p>1000 SOC8/EOC8/RESULT8 is associated with post processing block 2</p> <p>1001 SOC9/EOC9/RESULT9 is associated with post processing block 2</p> <p>1010 SOC10/EOC10/RESULT10 is associated with post processing block 2</p> <p>1011 SOC11/EOC11/RESULT11 is associated with post processing block 2</p> <p>1100 SOC12/EOC12/RESULT12 is associated with post processing block 2</p> <p>1101 SOC13/EOC13/RESULT13 is associated with post processing block 2</p> <p>1110 SOC14/EOC14/RESULT14 is associated with post processing block 2</p> <p>1111 SOC15/EOC15/RESULT15 is associated with post processing block 2</p> |

### 3.2.2.93 ADC\_CFG\_ADCPPB2STAMP Register

#### 1 ADC\_CFG\_ADCPPB2STAMP Register (Offset = 92h) [reset = 0h]

ADC PPB2 Sample Delay Time Stamp Register.

Return to [Summary Table](#)

**Table 3-281. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0092h       |
| ADC1_G0_G5    | 502C 1092h       |
| ADC2_G0_G5    | 502C 2092h       |
| ADC3_G0_G5    | 502C 3092h       |
| ADC4_G0_G5    | 502C 4092h       |

**Figure 3-93. ADC\_CFG\_ADCPPB2STAMP Name Register**

|            |    |    |    |          |    |   |   |
|------------|----|----|----|----------|----|---|---|
| 15         | 14 | 13 | 12 | 11       | 10 | 9 | 8 |
| RESERVED_1 |    |    |    | DLYSTAMP |    |   |   |
| R          |    |    |    | R        |    |   |   |
| 0h         |    |    |    | 0h       |    |   |   |
| 7          | 6  | 5  | 4  | 3        | 2  | 1 | 0 |
| DLYSTAMP   |    |    |    |          |    |   |   |
| R          |    |    |    |          |    |   |   |
| 0h         |    |    |    |          |    |   |   |

**Table 3-283. ADC\_CFG\_ADCPPB2STAMP Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                       |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                          |
| 11:0  | DLYSTAMP   | R    | 0h    | ADC Post Processing Block 2 Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample. |

### 3.2.2.94 ADC\_CFG\_ADCPPB2OFFCAL Register

#### 1 ADC\_CFG\_ADCPPB2OFFCAL Register (Offset = 94h) [reset = 0h]

ADC PPB2 Offset Calibration Register.

Return to [Summary Table](#)

**Table 3-284. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0094h       |
| ADC1_G0_G5    | 502C 1094h       |
| ADC2_G0_G5    | 502C 2094h       |
| ADC3_G0_G5    | 502C 3094h       |
| ADC4_G0_G5    | 502C 4094h       |

**Figure 3-94. ADC\_CFG\_ADCPPB2OFFCAL Name Register**

|            |    |    |    |    |    |        |   |
|------------|----|----|----|----|----|--------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9      | 8 |
| RESERVED_1 |    |    |    |    |    | OFFCAL |   |
| R          |    |    |    |    |    | R/W    |   |
| 0h         |    |    |    |    |    | 0h     |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1      | 0 |
| OFFCAL     |    |    |    |    |    |        |   |
| R/W        |    |    |    |    |    |        |   |
| 0h         |    |    |    |    |    |        |   |

**Table 3-286. ADC\_CFG\_ADCPPB2OFFCAL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 9:0   | OFFCAL     | R/W  | 0h    | <p>ADC Post Processing Block 2 Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register.</p> <p>000h No change. The ADC output is stored directly into ADCRESULT.</p> <p>001h ADC output - 1 is stored into ADCRESULT.</p> <p>002h ADC output - 2 is stored into ADCRESULT.</p> <p>...</p> <p>200h ADC output + 512 is stored into ADCRESULT.</p> <p>...</p> <p>3FFh ADC output + 1 is stored into ADCRESULT.</p> <p>NOTE: In 16-bit mode, the subtraction will saturate at 0000h and FFFFh before being stored into the ADCRESULT register.</p> <p>In 12-bit mode, the subtraction will saturate at 0000h and 0FFFh before being stored into the ADCRESULT register.</p> <p>Note: in the case that multiple PPBs point to the same SOC, only the OFFCAL of the lowest numbered PPB will be applied.</p> |

### 3.2.2.95 ADC\_CFG\_ADCPPB2OFFREF Register

#### 1 ADC\_CFG\_ADCPPB2OFFREF Register (Offset = 96h) [reset = 0h]

ADC PPB2 Offset Reference Register.

Return to [Summary Table](#)

**Table 3-287. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0096h       |
| ADC1_G0_G5    | 502C 1096h       |
| ADC2_G0_G5    | 502C 2096h       |
| ADC3_G0_G5    | 502C 3096h       |
| ADC4_G0_G5    | 502C 4096h       |

**Figure 3-95. ADC\_CFG\_ADCPPB2OFFREF Name Register**

|        |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| OFFREF |    |    |    |    |    |   |   |
| R/W    |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |
| 7      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| OFFREF |    |    |    |    |    |   |   |
| R/W    |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |

**Table 3-289. ADC\_CFG\_ADCPPB2OFFREF Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|--------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | OFFREF | R/W  | 0h    | <p>ADC Post Processing Block 2 Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB2RESULT register. This subtraction is not saturated.</p> <p>0000h No change. The ADCRESULT value is passed on.<br/> 0001h ADCRESULT - 1 is passed on.<br/> 0002h ADCRESULT - 2 is passed on.<br/> ...<br/> 8000h ADCRESULT - 32,768 is passed on.<br/> ...<br/> FFFFh ADCRESULT - 65,535 is passed on.</p> <p>NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.</p> |



### 3.2.2.96 ADC\_CFG\_ADCPPB2TRIPHI Register

#### 1 ADC\_CFG\_ADCPPB2TRIPHI Register (Offset = 98h) [reset = 0h]

ADC PPB2 Trip High Register.

Return to [Summary Table](#)

**Table 3-290. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0098h       |
| ADC1_G0_G5    | 502C 1098h       |
| ADC2_G0_G5    | 502C 2098h       |
| ADC3_G0_G5    | 502C 3098h       |
| ADC4_G0_G5    | 502C 4098h       |

**Figure 3-96. ADC\_CFG\_ADCPPB2TRIPHI Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_1 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LIMITHI    |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| LIMITHI    |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LIMITHI    |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 3-292. ADC\_CFG\_ADCPPB2TRIPHI Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                           |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                              |
| 23:0  | LIMITHI    | R/W  | 0h    | ADC Post Processing Block 2 Trip High Limit. This value sets the digital comparator trip high limit. When comparing to an ADCPPBxRESULT register, the upper bits will be ignored:<br>- TRIPHI[23:17] will be ignored in 16 bit mode<br>- TRIPHI[23:13] will be ignored in 12 bit mode |

### 3.2.2.97 ADC\_CFG\_ADCPPB2TRIPLO Register

#### 1 ADC\_CFG\_ADCPPB2TRIPLO Register (Offset = 9Ch) [reset = 0h]

ADC PPB2 Trip Low/Trigger Time Stamp Register.

Return to [Summary Table](#)

**Table 3-293. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 009Ch       |
| ADC1_G0_G5    | 502C 109Ch       |
| ADC2_G0_G5    | 502C 209Ch       |
| ADC3_G0_G5    | 502C 309Ch       |
| ADC4_G0_G5    | 502C 409Ch       |

**Figure 3-97. ADC\_CFG\_ADCPPB2TRIPLO Name Register**

|          |    |    |    |            |            |    |       |
|----------|----|----|----|------------|------------|----|-------|
| 31       | 30 | 29 | 28 | 27         | 26         | 25 | 24    |
| REQSTAMP |    |    |    |            |            |    |       |
| R        |    |    |    |            |            |    |       |
| 0h       |    |    |    |            |            |    |       |
| 23       | 22 | 21 | 20 | 19         | 18         | 17 | 16    |
| REQSTAMP |    |    |    | LIMITLO2EN | RESERVED_1 |    | LSIGN |
| R        |    |    |    | R/W        | R          |    | R/W   |
| 0h       |    |    |    | 0h         | 0h         |    | 0h    |
| 15       | 14 | 13 | 12 | 11         | 10         | 9  | 8     |
| LIMITLO  |    |    |    |            |            |    |       |
| R/W      |    |    |    |            |            |    |       |
| 0h       |    |    |    |            |            |    |       |
| 7        | 6  | 5  | 4  | 3          | 2          | 1  | 0     |
| LIMITLO  |    |    |    |            |            |    |       |
| R/W      |    |    |    |            |            |    |       |
| 0h       |    |    |    |            |            |    |       |

**Table 3-295. ADC\_CFG\_ADCPPB2TRIPLO Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                        |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | REQSTAMP   | R    | 0h    | ADC Post Processing Block 2 Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.                                                                                                                                                            |
| 19    | LIMITLO2EN | R/W  | 0h    | Extended Low Limit 2 Enable.<br>0 = Low limit set by ADCPPB2TRIPLO register. Not compatible with comparison with ADCPPB2PSUM or ADCPPB2SUM<br>1 = Low limit set by ADCPPB2TRIPLO2 register                                                                                                                                                         |
| 18:17 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                           |
| 16    | LSIGN      | R/W  | 0h    | Low Limit Sign Bit. This is the sign bit [17th bit] to the LIMITLO bit field when in 16-bit ADC mode.                                                                                                                                                                                                                                              |
| 15:0  | LIMITLO    | R/W  | 0h    | ADC Post Processing Block 2 Trip Low Limit. This value sets the digital comparator trip low limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB2RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRESULT bit field of the ADCPPB2RESULT register. |

### 3.2.2.98 ADC\_CFG\_ADCPPB3CONFIG Register

#### 1 ADC\_CFG\_ADCPPB3CONFIG Register (Offset = A0h) [reset = 2h]

ADC PPB3 Config Register.

Return to [Summary Table](#)

**Table 3-296. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 00A0h       |
| ADC1_G0_G5    | 502C 10A0h       |
| ADC2_G0_G5    | 502C 20A0h       |
| ADC3_G0_G5    | 502C 30A0h       |
| ADC4_G0_G5    | 502C 40A0h       |

**Figure 3-98. ADC\_CFG\_ADCPPB3CONFIG Name Register**

|            |       |       |            |        |    |   |   |
|------------|-------|-------|------------|--------|----|---|---|
| 15         | 14    | 13    | 12         | 11     | 10 | 9 | 8 |
| RESERVED_1 |       |       |            |        |    |   |   |
| R          |       |       |            |        |    |   |   |
| 0h         |       |       |            |        |    |   |   |
| 7          | 6     | 5     | 4          | 3      | 2  | 1 | 0 |
| RESERVED_1 | ABSEN | CBCEN | TWOSCOMPEN | CONFIG |    |   |   |
| R          | R/W   | R/W   | R/W        | R/W    |    |   |   |
| 0h         | 0h    | 0h    | 0h         | 2h     |    |   |   |

**Table 3-298. ADC\_CFG\_ADCPPB3CONFIG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:7 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                               |
| 6    | ABSEN      | R/W  | 0h    | ADC Post Processing Block 3 Absolute Value Enable. When set this bit enables absolute value calculation on the ADCRESULTx associated with ADCPPB3.<br>This occurs before the TWOSCOMPEN logic is evaluated [so enabling both TWOSCOMPEN and ABSEN will always result in a negative value stored in ADCPPBxRESULT]<br>0 ADCPPB3RESULT = ADCRESULTx - ADCPPB3OFFREF<br>1 ADCPPB3RESULT = abs[ADCRESULTx - ADCPPB3OFFREF] |
| 5    | CBCEN      | R/W  | 0h    | ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present.                                                                                                                                                                                         |
| 4    | TWOSCOMPEN | R/W  | 0h    | ADC Post Processing Block 3 Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the ADCPPB3RESULT register.<br>0 ADCPPB3RESULT = ADCRESULTx - ADCPPB3OFFREF<br>1 ADCPPB3RESULT = ADCPPB3OFFREF - ADCRESULTx                                        |

**Table 3-298. ADC\_CFG\_ADCPPB3CONFIG Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|--------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0 | CONFIG | R/W  | 2h    | <p>ADC Post Processing Block 3 Configuration. This bit field defines which SOC/EOC/RESULT is associated with this post processing block.</p> <p>0000 SOC0/EOC0/RESULT0 is associated with post processing block 3</p> <p>0001 SOC1/EOC1/RESULT1 is associated with post processing block 3</p> <p>0010 SOC2/EOC2/RESULT2 is associated with post processing block 3</p> <p>0011 SOC3/EOC3/RESULT3 is associated with post processing block 3</p> <p>0100 SOC4/EOC4/RESULT4 is associated with post processing block 3</p> <p>0101 SOC5/EOC5/RESULT5 is associated with post processing block 3</p> <p>0110 SOC6/EOC6/RESULT6 is associated with post processing block 3</p> <p>0111 SOC7/EOC7/RESULT7 is associated with post processing block 3</p> <p>1000 SOC8/EOC8/RESULT8 is associated with post processing block 3</p> <p>1001 SOC9/EOC9/RESULT9 is associated with post processing block 3</p> <p>1010 SOC10/EOC10/RESULT10 is associated with post processing block 3</p> <p>1011 SOC11/EOC11/RESULT11 is associated with post processing block 3</p> <p>1100 SOC12/EOC12/RESULT12 is associated with post processing block 3</p> <p>1101 SOC13/EOC13/RESULT13 is associated with post processing block 3</p> <p>1110 SOC14/EOC14/RESULT14 is associated with post processing block 3</p> <p>1111 SOC15/EOC15/RESULT15 is associated with post processing block 3</p> |

### 3.2.2.99 ADC\_CFG\_ADCPPB3STAMP Register

#### 1 ADC\_CFG\_ADCPPB3STAMP Register (Offset = A2h) [reset = 0h]

ADC PPB3 Sample Delay Time Stamp Register.

Return to [Summary Table](#)

**Table 3-299. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 00A2h       |
| ADC1_G0_G5    | 502C 10A2h       |
| ADC2_G0_G5    | 502C 20A2h       |
| ADC3_G0_G5    | 502C 30A2h       |
| ADC4_G0_G5    | 502C 40A2h       |

**Figure 3-99. ADC\_CFG\_ADCPPB3STAMP Name Register**

|            |    |    |    |          |    |   |   |
|------------|----|----|----|----------|----|---|---|
| 15         | 14 | 13 | 12 | 11       | 10 | 9 | 8 |
| RESERVED_1 |    |    |    | DLYSTAMP |    |   |   |
| R          |    |    |    | R        |    |   |   |
| 0h         |    |    |    | 0h       |    |   |   |
| 7          | 6  | 5  | 4  | 3        | 2  | 1 | 0 |
| DLYSTAMP   |    |    |    |          |    |   |   |
| R          |    |    |    |          |    |   |   |
| 0h         |    |    |    |          |    |   |   |

**Table 3-301. ADC\_CFG\_ADCPPB3STAMP Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                       |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                          |
| 11:0  | DLYSTAMP   | R    | 0h    | ADC Post Processing Block 3 Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample. |

### 3.2.2.100 ADC\_CFG\_ADCPPB3OFFCAL Register

#### 1 ADC\_CFG\_ADCPPB3OFFCAL Register (Offset = A4h) [reset = 0h]

ADC PPB3 Offset Calibration Register.

Return to [Summary Table](#)

**Table 3-302. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 00A4h       |
| ADC1_G0_G5    | 502C 10A4h       |
| ADC2_G0_G5    | 502C 20A4h       |
| ADC3_G0_G5    | 502C 30A4h       |
| ADC4_G0_G5    | 502C 40A4h       |

**Figure 3-100. ADC\_CFG\_ADCPPB3OFFCAL Name Register**

|            |    |    |    |    |    |        |   |
|------------|----|----|----|----|----|--------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9      | 8 |
| RESERVED_1 |    |    |    |    |    | OFFCAL |   |
| R          |    |    |    |    |    | R/W    |   |
| 0h         |    |    |    |    |    | 0h     |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1      | 0 |
| OFFCAL     |    |    |    |    |    |        |   |
| R/W        |    |    |    |    |    |        |   |
| 0h         |    |    |    |    |    |        |   |

**Table 3-304. ADC\_CFG\_ADCPPB3OFFCAL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 9:0   | OFFCAL     | R/W  | 0h    | <p>ADC Post Processing Block 3 Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register.</p> <p>000h No change. The ADC output is stored directly into ADCRESULT.</p> <p>001h ADC output - 1 is stored into ADCRESULT.</p> <p>002h ADC output - 2 is stored into ADCRESULT.</p> <p>...</p> <p>200h ADC output + 512 is stored into ADCRESULT.</p> <p>...</p> <p>3FFh ADC output + 1 is stored into ADCRESULT.</p> <p>NOTE: In 16-bit mode, the subtraction will saturate at 0000h and FFFFh before being stored into the ADCRESULT register.</p> <p>In 12-bit mode, the subtraction will saturate at 0000h and 0FFFh before being stored into the ADCRESULT register.</p> <p>Note: in the case that multiple PPBs point to the same SOC, only the OFFCAL of the lowest numbered PPB will be applied.</p> |

### 3.2.2.101 ADC\_CFG\_ADCPPB3OFFREF Register

#### 1 ADC\_CFG\_ADCPPB3OFFREF Register (Offset = A6h) [reset = 0h]

ADC PPB3 Offset Reference Register.

Return to [Summary Table](#)

**Table 3-305. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 00A6h       |
| ADC1_G0_G5    | 502C 10A6h       |
| ADC2_G0_G5    | 502C 20A6h       |
| ADC3_G0_G5    | 502C 30A6h       |
| ADC4_G0_G5    | 502C 40A6h       |

**Figure 3-101. ADC\_CFG\_ADCPPB3OFFREF Name Register**

|        |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| OFFREF |    |    |    |    |    |   |   |
| R/W    |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |
| 7      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| OFFREF |    |    |    |    |    |   |   |
| R/W    |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |

**Table 3-307. ADC\_CFG\_ADCPPB3OFFREF Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|--------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | OFFREF | R/W  | 0h    | <p>ADC Post Processing Block 3 Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB3RESULT register. This subtraction is not saturated.</p> <p>0000h No change. The ADCRESULT value is passed on.<br/> 0001h ADCRESULT - 1 is passed on.<br/> 0002h ADCRESULT - 2 is passed on.<br/> ...<br/> 8000h ADCRESULT - 32,768 is passed on.<br/> ...<br/> FFFFh ADCRESULT - 65,535 is passed on.</p> <p>NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.</p> |

### 3.2.2.102 ADC\_CFG\_ADCPPB3TRIPHI Register

#### 1 ADC\_CFG\_ADCPPB3TRIPHI Register (Offset = A8h) [reset = 0h]

ADC PPB3 Trip High Register.

Return to [Summary Table](#)

**Table 3-308. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 00A8h       |
| ADC1_G0_G5    | 502C 10A8h       |
| ADC2_G0_G5    | 502C 20A8h       |
| ADC3_G0_G5    | 502C 30A8h       |
| ADC4_G0_G5    | 502C 40A8h       |

**Figure 3-102. ADC\_CFG\_ADCPPB3TRIPHI Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_1 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LIMITHI    |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| LIMITHI    |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LIMITHI    |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 3-310. ADC\_CFG\_ADCPPB3TRIPHI Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                           |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                              |
| 23:0  | LIMITHI    | R/W  | 0h    | ADC Post Processing Block 3 Trip High Limit. This value sets the digital comparator trip high limit. When comparing to an ADCPPBxRESULT register, the upper bits will be ignored:<br>- TRIPHI[23:17] will be ignored in 16 bit mode<br>- TRIPHI[23:13] will be ignored in 12 bit mode |



### 3.2.2.103 ADC\_CFG\_ADCPPB3TRIPLO Register

#### 1 ADC\_CFG\_ADCPPB3TRIPLO Register (Offset = ACh) [reset = 0h]

ADC PPB3 Trip Low/Trigger Time Stamp Register.

Return to [Summary Table](#)

**Table 3-311. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 00ACh       |
| ADC1_G0_G5    | 502C 10ACh       |
| ADC2_G0_G5    | 502C 20ACh       |
| ADC3_G0_G5    | 502C 30ACh       |
| ADC4_G0_G5    | 502C 40ACh       |

**Figure 3-103. ADC\_CFG\_ADCPPB3TRIPLO Name Register**

|          |    |    |    |            |            |    |       |
|----------|----|----|----|------------|------------|----|-------|
| 31       | 30 | 29 | 28 | 27         | 26         | 25 | 24    |
| REQSTAMP |    |    |    |            |            |    |       |
| R        |    |    |    |            |            |    |       |
| 0h       |    |    |    |            |            |    |       |
| 23       | 22 | 21 | 20 | 19         | 18         | 17 | 16    |
| REQSTAMP |    |    |    | LIMITLO2EN | RESERVED_1 |    | LSIGN |
| R        |    |    |    | R/W        | R          |    | R/W   |
| 0h       |    |    |    | 0h         | 0h         |    | 0h    |
| 15       | 14 | 13 | 12 | 11         | 10         | 9  | 8     |
| LIMITLO  |    |    |    |            |            |    |       |
| R/W      |    |    |    |            |            |    |       |
| 0h       |    |    |    |            |            |    |       |
| 7        | 6  | 5  | 4  | 3          | 2          | 1  | 0     |
| LIMITLO  |    |    |    |            |            |    |       |
| R/W      |    |    |    |            |            |    |       |
| 0h       |    |    |    |            |            |    |       |

**Table 3-313. ADC\_CFG\_ADCPPB3TRIPLO Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                        |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | REQSTAMP   | R    | 0h    | ADC Post Processing Block 3 Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.                                                                                                                                                            |
| 19    | LIMITLO2EN | R/W  | 0h    | Extended Low Limit 2 Enable.<br>0 = Low limit set by ADCPPB3TRIPLO register. Not compatible with comparison with ADCPPB3PSUM or ADCPPB3SUM<br>1 = Low limit set by ADCPPB3TRIPLO2 register                                                                                                                                                         |
| 18:17 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                           |
| 16    | LSIGN      | R/W  | 0h    | Low Limit Sign Bit. This is the sign bit [17th bit] to the LIMITLO bit field when in 16-bit ADC mode.                                                                                                                                                                                                                                              |
| 15:0  | LIMITLO    | R/W  | 0h    | ADC Post Processing Block 3 Trip Low Limit. This value sets the digital comparator trip low limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB3RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRESULT bit field of the ADCPPB3RESULT register. |

### 3.2.2.104 ADC\_CFG\_ADCPPB4CONFIG Register

#### 1 ADC\_CFG\_ADCPPB4CONFIG Register (Offset = B0h) [reset = 3h]

ADC PPB4 Config Register.

Return to [Summary Table](#)

**Table 3-314. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 00B0h       |
| ADC1_G0_G5    | 502C 10B0h       |
| ADC2_G0_G5    | 502C 20B0h       |
| ADC3_G0_G5    | 502C 30B0h       |
| ADC4_G0_G5    | 502C 40B0h       |

**Figure 3-104. ADC\_CFG\_ADCPPB4CONFIG Name Register**

|            |       |       |            |        |    |   |   |
|------------|-------|-------|------------|--------|----|---|---|
| 15         | 14    | 13    | 12         | 11     | 10 | 9 | 8 |
| RESERVED_1 |       |       |            |        |    |   |   |
| R          |       |       |            |        |    |   |   |
| 0h         |       |       |            |        |    |   |   |
| 7          | 6     | 5     | 4          | 3      | 2  | 1 | 0 |
| RESERVED_1 | ABSEN | CBCEN | TWOSCOMPEN | CONFIG |    |   |   |
| R          | R/W   | R/W   | R/W        | R/W    |    |   |   |
| 0h         | 0h    | 0h    | 0h         | 3h     |    |   |   |

**Table 3-316. ADC\_CFG\_ADCPPB4CONFIG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:7 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                               |
| 6    | ABSEN      | R/W  | 0h    | ADC Post Processing Block 4 Absolute Value Enable. When set this bit enables absolute value calculation on the ADCRESULTx associated with ADCPPB4.<br>This occurs before the TWOSCOMPEN logic is evaluated [so enabling both TWOSCOMPEN and ABSEN will always result in a negative value stored in ADCPPBxRESULT]<br>0 ADCPPB4RESULT = ADCRESULTx - ADCPPB4OFFREF<br>1 ADCPPB4RESULT = abs[ADCRESULTx - ADCPPB4OFFREF] |
| 5    | CBCEN      | R/W  | 0h    | ADC Post Processing Block Cycle By Cycle Enable. When set, this bit enables the post conversion hardware processing circuit to automatically clear the ADCEVTSTAT on a conversion if the event condition is no longer present.                                                                                                                                                                                         |
| 4    | TWOSCOMPEN | R/W  | 0h    | ADC Post Processing Block 4 Two's Complement Enable. When set this bit enables the post conversion hardware processing circuit that performs a two's complement on the output of the offset/reference subtraction unit before storing the result in the ADCPPB4RESULT register.<br>0 ADCPPB4RESULT = ADCRESULTx - ADCPPB4OFFREF<br>1 ADCPPB4RESULT = ADCPPB4OFFREF - ADCRESULTx                                        |

**Table 3-316. ADC\_CFG\_ADCPPB4CONFIG Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|--------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0 | CONFIG | R/W  | 3h    | <p>ADC Post Processing Block 4 Configuration. This bit field defines which SOC/EOC/RESULT is associated with this post processing block.</p> <p>0000 SOC0/EOC0/RESULT0 is associated with post processing block 4</p> <p>0001 SOC1/EOC1/RESULT1 is associated with post processing block 4</p> <p>0010 SOC2/EOC2/RESULT2 is associated with post processing block 4</p> <p>0011 SOC3/EOC3/RESULT3 is associated with post processing block 4</p> <p>0100 SOC4/EOC4/RESULT4 is associated with post processing block 4</p> <p>0101 SOC5/EOC5/RESULT5 is associated with post processing block 4</p> <p>0110 SOC6/EOC6/RESULT6 is associated with post processing block 4</p> <p>0111 SOC7/EOC7/RESULT7 is associated with post processing block 4</p> <p>1000 SOC8/EOC8/RESULT8 is associated with post processing block 4</p> <p>1001 SOC9/EOC9/RESULT9 is associated with post processing block 4</p> <p>1010 SOC10/EOC10/RESULT10 is associated with post processing block 4</p> <p>1011 SOC11/EOC11/RESULT11 is associated with post processing block 4</p> <p>1100 SOC12/EOC12/RESULT12 is associated with post processing block 4</p> <p>1101 SOC13/EOC13/RESULT13 is associated with post processing block 4</p> <p>1110 SOC14/EOC14/RESULT14 is associated with post processing block 4</p> <p>1111 SOC15/EOC15/RESULT15 is associated with post processing block 4</p> |

### 3.2.2.105 ADC\_CFG\_ADCPPB4STAMP Register

#### 1 ADC\_CFG\_ADCPPB4STAMP Register (Offset = B2h) [reset = 0h]

ADC PPB4 Sample Delay Time Stamp Register.

Return to [Summary Table](#)

**Table 3-317. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 00B2h       |
| ADC1_G0_G5    | 502C 10B2h       |
| ADC2_G0_G5    | 502C 20B2h       |
| ADC3_G0_G5    | 502C 30B2h       |
| ADC4_G0_G5    | 502C 40B2h       |

**Figure 3-105. ADC\_CFG\_ADCPPB4STAMP Name Register**

|            |    |    |    |          |    |   |   |
|------------|----|----|----|----------|----|---|---|
| 15         | 14 | 13 | 12 | 11       | 10 | 9 | 8 |
| RESERVED_1 |    |    |    | DLYSTAMP |    |   |   |
| R          |    |    |    | R        |    |   |   |
| 0h         |    |    |    | 0h       |    |   |   |
| 7          | 6  | 5  | 4  | 3        | 2  | 1 | 0 |
| DLYSTAMP   |    |    |    |          |    |   |   |
| R          |    |    |    |          |    |   |   |
| 0h         |    |    |    |          |    |   |   |

**Table 3-319. ADC\_CFG\_ADCPPB4STAMP Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                       |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                          |
| 11:0  | DLYSTAMP   | R    | 0h    | ADC Post Processing Block 4 Delay Time Stamp. When an SOC starts sampling the value contained in REQSTAMP is subtracted from the value in ADCCOUNTER.FREECOUNT and loaded into this bit field, thereby giving the number of system clock cycles delay between the SOC trigger and the actual start of the sample. |

### 3.2.2.106 ADC\_CFG\_ADCPPB4OFFCAL Register

#### 1 ADC\_CFG\_ADCPPB4OFFCAL Register (Offset = B4h) [reset = 0h]

ADC PPB4 Offset Calibration Register.

Return to [Summary Table](#)

**Table 3-320. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 00B4h       |
| ADC1_G0_G5    | 502C 10B4h       |
| ADC2_G0_G5    | 502C 20B4h       |
| ADC3_G0_G5    | 502C 30B4h       |
| ADC4_G0_G5    | 502C 40B4h       |

**Figure 3-106. ADC\_CFG\_ADCPPB4OFFCAL Name Register**

|            |    |    |    |    |    |        |   |
|------------|----|----|----|----|----|--------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9      | 8 |
| RESERVED_1 |    |    |    |    |    | OFFCAL |   |
| R          |    |    |    |    |    | R/W    |   |
| 0h         |    |    |    |    |    | 0h     |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1      | 0 |
| OFFCAL     |    |    |    |    |    |        |   |
| R/W        |    |    |    |    |    |        |   |
| 0h         |    |    |    |    |    |        |   |

**Table 3-322. ADC\_CFG\_ADCPPB4OFFCAL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 9:0   | OFFCAL     | R/W  | 0h    | <p>ADC Post Processing Block 4 Offset Correction. This bit field can be used to digitally remove any system level offset inherent in the ADCIN circuit. This 10-bit signed value is subtracted from the ADC output before being stored in the ADCRESULT register.</p> <p>000h No change. The ADC output is stored directly into ADCRESULT.</p> <p>001h ADC output - 1 is stored into ADCRESULT.</p> <p>002h ADC output - 2 is stored into ADCRESULT.</p> <p>...</p> <p>200h ADC output + 512 is stored into ADCRESULT.</p> <p>...</p> <p>3FFh ADC output + 1 is stored into ADCRESULT.</p> <p>NOTE: In 16-bit mode, the subtraction will saturate at 0000h and FFFFh before being stored into the ADCRESULT register.</p> <p>In 12-bit mode, the subtraction will saturate at 0000h and 0FFFh before being stored into the ADCRESULT register.</p> <p>Note: in the case that multiple PPBs point to the same SOC, only the OFFCAL of the lowest numbered PPB will be applied.</p> |

### 3.2.2.107 ADC\_CFG\_ADCPPB4OFFREF Register

#### 1 ADC\_CFG\_ADCPPB4OFFREF Register (Offset = B6h) [reset = 0h]

ADC PPB4 Offset Reference Register.

Return to [Summary Table](#)

**Table 3-323. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 00B6h       |
| ADC1_G0_G5    | 502C 10B6h       |
| ADC2_G0_G5    | 502C 20B6h       |
| ADC3_G0_G5    | 502C 30B6h       |
| ADC4_G0_G5    | 502C 40B6h       |

**Figure 3-107. ADC\_CFG\_ADCPPB4OFFREF Name Register**

|        |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| OFFREF |    |    |    |    |    |   |   |
| R/W    |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |
| 7      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| OFFREF |    |    |    |    |    |   |   |
| R/W    |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |

**Table 3-325. ADC\_CFG\_ADCPPB4OFFREF Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|--------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | OFFREF | R/W  | 0h    | <p>ADC Post Processing Block 4 Offset Correction. This bit field can be used to either calculate the feedback error or convert a unipolar signal to bipolar by subtracting a reference value. This 16-bit unsigned value is subtracted from the ADCRESULT register before being passed through an optional two's complement function and stored in the ADCPPB4RESULT register. This subtraction is not saturated.</p> <p>0000h No change. The ADCRESULT value is passed on.<br/> 0001h ADCRESULT - 1 is passed on.<br/> 0002h ADCRESULT - 2 is passed on.<br/> ...<br/> 8000h ADCRESULT - 32,768 is passed on.<br/> ...<br/> FFFFh ADCRESULT - 65,535 is passed on.</p> <p>NOTE: In 12-bit mode the size of this register does not change from 16-bits. It is the user's responsibility to ensure that only a 12-bit value is written to this register when in 12-bit mode.</p> |

### 3.2.2.108 ADC\_CFG\_ADCPPB4TRIPHI Register

#### 1 ADC\_CFG\_ADCPPB4TRIPHI Register (Offset = B8h) [reset = 0h]

ADC PPB4 Trip High Register.

Return to [Summary Table](#)

**Table 3-326. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 00B8h       |
| ADC1_G0_G5    | 502C 10B8h       |
| ADC2_G0_G5    | 502C 20B8h       |
| ADC3_G0_G5    | 502C 30B8h       |
| ADC4_G0_G5    | 502C 40B8h       |

**Figure 3-108. ADC\_CFG\_ADCPPB4TRIPHI Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_1 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LIMITHI    |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| LIMITHI    |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LIMITHI    |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 3-328. ADC\_CFG\_ADCPPB4TRIPHI Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                           |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                              |
| 23:0  | LIMITHI    | R/W  | 0h    | ADC Post Processing Block 4 Trip High Limit. This value sets the digital comparator trip high limit. When comparing to an ADCPPBxRESULT register, the upper bits will be ignored:<br>- TRIPHI[23:17] will be ignored in 16 bit mode<br>- TRIPHI[23:13] will be ignored in 12 bit mode |

### 3.2.2.109 ADC\_CFG\_ADCPPB4TRIPLO Register

#### 1 ADC\_CFG\_ADCPPB4TRIPLO Register (Offset = BCh) [reset = 0h]

ADC PPB4 Trip Low/Trigger Time Stamp Register.

Return to [Summary Table](#)

**Table 3-329. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 00BCh       |
| ADC1_G0_G5    | 502C 10BCh       |
| ADC2_G0_G5    | 502C 20BCh       |
| ADC3_G0_G5    | 502C 30BCh       |
| ADC4_G0_G5    | 502C 40BCh       |

**Figure 3-109. ADC\_CFG\_ADCPPB4TRIPLO Name Register**

|          |    |    |    |            |            |    |       |
|----------|----|----|----|------------|------------|----|-------|
| 31       | 30 | 29 | 28 | 27         | 26         | 25 | 24    |
| REQSTAMP |    |    |    |            |            |    |       |
| R        |    |    |    |            |            |    |       |
| 0h       |    |    |    |            |            |    |       |
| 23       | 22 | 21 | 20 | 19         | 18         | 17 | 16    |
| REQSTAMP |    |    |    | LIMITLO2EN | RESERVED_1 |    | LSIGN |
| R        |    |    |    | R/W        | R          |    | R/W   |
| 0h       |    |    |    | 0h         | 0h         |    | 0h    |
| 15       | 14 | 13 | 12 | 11         | 10         | 9  | 8     |
| LIMITLO  |    |    |    |            |            |    |       |
| R/W      |    |    |    |            |            |    |       |
| 0h       |    |    |    |            |            |    |       |
| 7        | 6  | 5  | 4  | 3          | 2          | 1  | 0     |
| LIMITLO  |    |    |    |            |            |    |       |
| R/W      |    |    |    |            |            |    |       |
| 0h       |    |    |    |            |            |    |       |

**Table 3-331. ADC\_CFG\_ADCPPB4TRIPLO Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                       |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | REQSTAMP   | R    | 0h    | ADC Post Processing Block 4 Request Time Stamp. When a trigger sets the associated SOC flag in the ADCSOCFLG1 register the value of ADCCOUNTER.FREECOUNT is loaded into this bit field.                                                                                                                                                           |
| 19    | LIMITLO2EN | R/W  | 0h    | Extended Low Limit 2 Enable.<br>0 = Low limit set by ADCPPB4TRIPLO register. Not compatible with comparison with ADCPPB4PSUM or ADCPPB4SUM<br>1 = Low limit set by ADCPPB4TRIPLO2 register                                                                                                                                                        |
| 18:17 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                          |
| 16    | LSIGN      | R/W  | 0h    | Low Limit Sign Bit. This is the sign bit [17th bit] to the LIMITLO bit field when in 16-bit ADC mode.                                                                                                                                                                                                                                             |
| 15:0  | LIMITLO    | R/W  | 0h    | ADC Post Processing Block 4 Trip Low Limit. This value sets the digital comparator trip low limit. In 16-bit mode all 17 bits will be compared against the 17 bits of the PPBRESULT bit field of the ADCPPB4RESULT register. In 12-bit mode bits 12:0 will be compared against bits 12:0 of the PPBRSULT bit field of the ADCPPB4RESULT register. |



### 3.2.2.110 ADC\_CFG\_ADCSAFECHECKRESEN Register

#### 1 ADC\_CFG\_ADCSAFECHECKRESEN Register (Offset = C0h) [reset = 0h]

ADC Safe Check Result Enable Register.

Return to [Summary Table](#)

**Table 3-332. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 00C0h       |
| ADC1_G0_G5    | 502C 10C0h       |
| ADC2_G0_G5    | 502C 20C0h       |
| ADC3_G0_G5    | 502C 30C0h       |
| ADC4_G0_G5    | 502C 40C0h       |

**Figure 3-110. ADC\_CFG\_ADCSAFECHECKRESEN Name Register**

|            |    |            |    |            |    |            |    |
|------------|----|------------|----|------------|----|------------|----|
| 31         | 30 | 29         | 28 | 27         | 26 | 25         | 24 |
| SOC15CHKEN |    | SOC14CHKEN |    | SOC13CHKEN |    | SOC12CHKEN |    |
| R/W        |    | R/W        |    | R/W        |    | R/W        |    |
| 0h         |    | 0h         |    | 0h         |    | 0h         |    |
| 23         | 22 | 21         | 20 | 19         | 18 | 17         | 16 |
| SOC11CHKEN |    | SOC10CHKEN |    | SOC9CHKEN  |    | SOC8CHKEN  |    |
| R/W        |    | R/W        |    | R/W        |    | R/W        |    |
| 0h         |    | 0h         |    | 0h         |    | 0h         |    |
| 15         | 14 | 13         | 12 | 11         | 10 | 9          | 8  |
| SOC7CHKEN  |    | SOC6CHKEN  |    | SOC5CHKEN  |    | SOC4CHKEN  |    |
| R/W        |    | R/W        |    | R/W        |    | R/W        |    |
| 0h         |    | 0h         |    | 0h         |    | 0h         |    |
| 7          | 6  | 5          | 4  | 3          | 2  | 1          | 0  |
| SOC3CHKEN  |    | SOC2CHKEN  |    | SOC1CHKEN  |    | SOC0CHKEN  |    |
| R/W        |    | R/W        |    | R/W        |    | R/W        |    |
| 0h         |    | 0h         |    | 0h         |    | 0h         |    |

**Table 3-334. ADC\_CFG\_ADCSAFECHECKRESEN Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | SOC15CHKEN | R/W  | 0h    | Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion.<br>00 No result passed to safety checker<br>01 ADCRESULT15 passed to safety checker<br>10 PPB Result associated with SOC15 passed to safety checker<br>11 PPB Sum associated with SOC15 passed to safety checker<br>Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker |
| 29:28 | SOC14CHKEN | R/W  | 0h    | Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion.<br>00 No result passed to safety checker<br>01 ADCRESULT14 passed to safety checker<br>10 PPB Result associated with SOC14 passed to safety checker<br>11 PPB Sum associated with SOC14 passed to safety checker<br>Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker |

**Table 3-334. ADC\_CFG\_ADCSAFECHECKRESEN Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 27:26 | SOC13CHKEN | R/W  | 0h    | Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion.<br>00 No result passed to safety checker<br>01 ADCRESULT13 passed to safety checker<br>10 PPB Result associated with SOC13 passed to safety checker<br>11 PPB Sum associated with SOC13 passed to safety checker<br>Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker |
| 25:24 | SOC12CHKEN | R/W  | 0h    | Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion.<br>00 No result passed to safety checker<br>01 ADCRESULT12 passed to safety checker<br>10 PPB Result associated with SOC12 passed to safety checker<br>11 PPB Sum associated with SOC12 passed to safety checker<br>Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker |
| 23:22 | SOC11CHKEN | R/W  | 0h    | Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion.<br>00 No result passed to safety checker<br>01 ADCRESULT11 passed to safety checker<br>10 PPB Result associated with SOC11 passed to safety checker<br>11 PPB Sum associated with SOC11 passed to safety checker<br>Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker |
| 21:20 | SOC10CHKEN | R/W  | 0h    | Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion.<br>00 No result passed to safety checker<br>01 ADCRESULT10 passed to safety checker<br>10 PPB Result associated with SOC10 passed to safety checker<br>11 PPB Sum associated with SOC10 passed to safety checker<br>Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker |
| 19:18 | SOC9CHKEN  | R/W  | 0h    | Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion.<br>00 No result passed to safety checker<br>01 ADCRESULT9 passed to safety checker<br>10 PPB Result associated with SOC9 passed to safety checker<br>11 PPB Sum associated with SOC9 passed to safety checker<br>Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker    |
| 17:16 | SOC8CHKEN  | R/W  | 0h    | Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion.<br>00 No result passed to safety checker<br>01 ADCRESULT8 passed to safety checker<br>10 PPB Result associated with SOC8 passed to safety checker<br>11 PPB Sum associated with SOC8 passed to safety checker<br>Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker    |

**Table 3-334. ADC\_CFG\_ADCSAFECHECKRESEN Register Field Descriptions (continued)**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|-----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | SOC7CHKEN | R/W  | 0h    | Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion.<br>00 No result passed to safety checker<br>01 ADCRESULT7 passed to safety checker<br>10 PPB Result associated with SOC7 passed to safety checker<br>11 PPB Sum associated with SOC7 passed to safety checker<br>Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker |
| 13:12 | SOC6CHKEN | R/W  | 0h    | Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion.<br>00 No result passed to safety checker<br>01 ADCRESULT6 passed to safety checker<br>10 PPB Result associated with SOC6 passed to safety checker<br>11 PPB Sum associated with SOC6 passed to safety checker<br>Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker |
| 11:10 | SOC5CHKEN | R/W  | 0h    | Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion.<br>00 No result passed to safety checker<br>01 ADCRESULT5 passed to safety checker<br>10 PPB Result associated with SOC5 passed to safety checker<br>11 PPB Sum associated with SOC5 passed to safety checker<br>Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker |
| 9:8   | SOC4CHKEN | R/W  | 0h    | Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion.<br>00 No result passed to safety checker<br>01 ADCRESULT4 passed to safety checker<br>10 PPB Result associated with SOC4 passed to safety checker<br>11 PPB Sum associated with SOC4 passed to safety checker<br>Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker |
| 7:6   | SOC3CHKEN | R/W  | 0h    | Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion.<br>00 No result passed to safety checker<br>01 ADCRESULT3 passed to safety checker<br>10 PPB Result associated with SOC3 passed to safety checker<br>11 PPB Sum associated with SOC3 passed to safety checker<br>Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker |
| 5:4   | SOC2CHKEN | R/W  | 0h    | Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion.<br>00 No result passed to safety checker<br>01 ADCRESULT2 passed to safety checker<br>10 PPB Result associated with SOC2 passed to safety checker<br>11 PPB Sum associated with SOC2 passed to safety checker<br>Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker |

**Table 3-334. ADC\_CFG\_ADCSAFECHECKRESEN Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-----|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:2 | SOC1CHKEN | R/W  | 0h    | <p>Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion.</p> <p>00 No result passed to safety checker<br/> 01 ADCRESULT1 passed to safety checker<br/> 10 PPB Result associated with SOC1 passed to safety checker<br/> 11 PPB Sum associated with SOC1 passed to safety checker</p> <p>Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker</p> |
| 1:0 | SOC0CHKEN | R/W  | 0h    | <p>Determine which result will be passed to the safety result checker. Only one of the raw ADC result, the PPB result, or the final PPB accumulated SUM can be passed on to the checker for each conversion.</p> <p>00 No result passed to safety checker<br/> 01 ADCRESULT0 passed to safety checker<br/> 10 PPB Result associated with SOC0 passed to safety checker<br/> 11 PPB Sum associated with SOC0 passed to safety checker</p> <p>Note: if multiple PPBs point to the same SOC, the highest numbered PPB will have priority to pass its result to the safety checker</p> |

### 3.2.2.111 ADC\_CFG\_ADCINTCYCLE Register

#### 1 ADC\_CFG\_ADCINTCYCLE Register (Offset = DEh) [reset = 0h]

ADC Early Interrupt Generation Cycle.

Return to [Summary Table](#)

**Table 3-335. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 00DEh       |
| ADC1_G0_G5    | 502C 10DEh       |
| ADC2_G0_G5    | 502C 20DEh       |
| ADC3_G0_G5    | 502C 30DEh       |
| ADC4_G0_G5    | 502C 40DEh       |

**Figure 3-111. ADC\_CFG\_ADCINTCYCLE Name Register**

|       |    |    |    |    |    |   |   |
|-------|----|----|----|----|----|---|---|
| 15    | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DELAY |    |    |    |    |    |   |   |
| R/W   |    |    |    |    |    |   |   |
| 0h    |    |    |    |    |    |   |   |
| 7     | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| DELAY |    |    |    |    |    |   |   |
| R/W   |    |    |    |    |    |   |   |
| 0h    |    |    |    |    |    |   |   |

**Table 3-337. ADC\_CFG\_ADCINTCYCLE Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                    |
|------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | DELAY | R/W  | 0h    | ADC Early Interrupt Generation Cycle Delay: Defines the delay from the fall edge of ADCSOC in terms of system clock cycles, for the interrupt to be generated. |

### 3.2.2.112 ADC\_CFG\_ADCINLTRIM1 Register

#### 1 ADC\_CFG\_ADCINLTRIM1 Register (Offset = E0h) [reset = 0h]

ADC Linearity Trim 1 Register.

Return to [Summary Table](#)

**Table 3-338. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 00E0h       |
| ADC1_G0_G5    | 502C 10E0h       |
| ADC2_G0_G5    | 502C 20E0h       |
| ADC3_G0_G5    | 502C 30E0h       |
| ADC4_G0_G5    | 502C 40E0h       |

**Figure 3-112. ADC\_CFG\_ADCINLTRIM1 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INLTRIM31TO0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INLTRIM31TO0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INLTRIM31TO0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INLTRIM31TO0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 3-340. ADC\_CFG\_ADCINLTRIM1 Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                                                                                                                                                                              |
|------|--------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | INLTRIM31TO0 | R/W  | 0h    | ADC Linearity Trim Bits 31-0.<br>This register should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the contents of this register could cause this module to operate outside of datasheet specifications. |

### 3.2.2.113 ADC\_CFG\_ADCINLTRIM2 Register

#### 1 ADC\_CFG\_ADCINLTRIM2 Register (Offset = E4h) [reset = 0h]

ADC Linearity Trim 2 Register.

Return to [Summary Table](#)

**Table 3-341. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 00E4h       |
| ADC1_G0_G5    | 502C 10E4h       |
| ADC2_G0_G5    | 502C 20E4h       |
| ADC3_G0_G5    | 502C 30E4h       |
| ADC4_G0_G5    | 502C 40E4h       |

**Figure 3-113. ADC\_CFG\_ADCINLTRIM2 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INLTRIM63TO32 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INLTRIM63TO32 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INLTRIM63TO32 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INLTRIM63TO32 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 3-343. ADC\_CFG\_ADCINLTRIM2 Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                                                                                                                                                                                                                               |
|------|---------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | INLTRIM63TO32 | R/W  | 0h    | ADC Linearity Trim Bits 63-32.<br>This register should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the contents of this register could cause this module to operate outside of datasheet specifications. |

### 3.2.2.114 ADC\_CFG\_ADCINLTRIM3 Register

#### 1 ADC\_CFG\_ADCINLTRIM3 Register (Offset = E8h) [reset = 0h]

ADC Linearity Trim 3 Register.

Return to [Summary Table](#)

**Table 3-344. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 00E8h       |
| ADC1_G0_G5    | 502C 10E8h       |
| ADC2_G0_G5    | 502C 20E8h       |
| ADC3_G0_G5    | 502C 30E8h       |
| ADC4_G0_G5    | 502C 40E8h       |

**Figure 3-114. ADC\_CFG\_ADCINLTRIM3 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INLTRIM95TO64 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INLTRIM95TO64 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INLTRIM95TO64 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INLTRIM95TO64 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 3-346. ADC\_CFG\_ADCINLTRIM3 Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                                                                                                                                                                                                                               |
|------|---------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | INLTRIM95TO64 | R/W  | 0h    | ADC Linearity Trim Bits 95-64.<br>This register should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the contents of this register could cause this module to operate outside of datasheet specifications. |



### 3.2.2.115 ADC\_CFG\_ADCINLTRIM4 Register

#### 1 ADC\_CFG\_ADCINLTRIM4 Register (Offset = ECh) [reset = 0h]

ADC Linearity Trim 4 Register.

Return to [Summary Table](#)

**Table 3-347. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 00ECh       |
| ADC1_G0_G5    | 502C 10ECh       |
| ADC2_G0_G5    | 502C 20ECh       |
| ADC3_G0_G5    | 502C 30ECh       |
| ADC4_G0_G5    | 502C 40ECh       |

**Figure 3-115. ADC\_CFG\_ADCINLTRIM4 Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INLTRIM127TO96 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INLTRIM127TO96 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INLTRIM127TO96 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INLTRIM127TO96 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 3-349. ADC\_CFG\_ADCINLTRIM4 Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                                                                                                                                                                                |
|------|----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | INLTRIM127TO96 | R/W  | 0h    | ADC Linearity Trim Bits 127-96.<br>This register should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the contents of this register could cause this module to operate outside of datasheet specifications. |

### 3.2.2.116 ADC\_CFG\_ADCINLTRIM5 Register

#### 1 ADC\_CFG\_ADCINLTRIM5 Register (Offset = F0h) [reset = 0h]

ADC Linearity Trim 5 Register.

Return to [Summary Table](#)

**Table 3-350. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 00F0h       |
| ADC1_G0_G5    | 502C 10F0h       |
| ADC2_G0_G5    | 502C 20F0h       |
| ADC3_G0_G5    | 502C 30F0h       |
| ADC4_G0_G5    | 502C 40F0h       |

**Figure 3-116. ADC\_CFG\_ADCINLTRIM5 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INLTRIM159TO128 |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INLTRIM159TO128 |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INLTRIM159TO128 |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INLTRIM159TO128 |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-352. ADC\_CFG\_ADCINLTRIM5 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | INLTRIM159TO128 | R/W  | 0h    | ADC Linearity Trim Bits 159-128.<br>This register should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the contents of this register could cause this module to operate outside of datasheet specifications. |

### 3.2.2.117 ADC\_CFG\_ADCINLTRIM6 Register

#### 1 ADC\_CFG\_ADCINLTRIM6 Register (Offset = F4h) [reset = 0h]

ADC Linearity Trim 6 Register.

Return to [Summary Table](#)

**Table 3-353. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 00F4h       |
| ADC1_G0_G5    | 502C 10F4h       |
| ADC2_G0_G5    | 502C 20F4h       |
| ADC3_G0_G5    | 502C 30F4h       |
| ADC4_G0_G5    | 502C 40F4h       |

**Figure 3-117. ADC\_CFG\_ADCINLTRIM6 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INLTRIM191TO160 |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INLTRIM191TO160 |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INLTRIM191TO160 |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INLTRIM191TO160 |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-355. ADC\_CFG\_ADCINLTRIM6 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                 |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | INLTRIM191TO160 | R/W  | 0h    | ADC Linearity Trim Bits 191-160.<br>This register should not be modified unless specifically indicated by TI Errata or other documentation. Modifying the contents of this register could cause this module to operate outside of datasheet specifications. |

### 3.2.2.118 ADC\_CFG\_ADCREV2 Register

#### 1 ADC\_CFG\_ADCREV2 Register (Offset = FAh) [reset = 4h]

ADC Wrapper Revision Register.

Return to [Summary Table](#)

**Table 3-356. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 00FAh       |
| ADC1_G0_G5    | 502C 10FAh       |
| ADC2_G0_G5    | 502C 20FAh       |
| ADC3_G0_G5    | 502C 30FAh       |
| ADC4_G0_G5    | 502C 40FAh       |

**Figure 3-118. ADC\_CFG\_ADCREV2 Name Register**

|             |    |    |    |    |    |   |   |
|-------------|----|----|----|----|----|---|---|
| 15          | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| WRAPPERREV  |    |    |    |    |    |   |   |
| R           |    |    |    |    |    |   |   |
| 0h          |    |    |    |    |    |   |   |
| 7           | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| WRAPPERTYPE |    |    |    |    |    |   |   |
| R           |    |    |    |    |    |   |   |
| 4h          |    |    |    |    |    |   |   |

**Table 3-358. ADC\_CFG\_ADCREV2 Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                            |
|------|-------------|------|-------|--------------------------------------------------------------------------------------------------------|
| 15:8 | WRAPPERREV  | R    | 0h    | ADC Revision. To allow documentation of differences between revisions. First version is labeled as 00h |
| 7:0  | WRAPPERTYPE | R    | 4h    | ADC Wrapper Type. Always set to 4 for this ADC.                                                        |

### 3.2.2.119 ADC\_CFG\_ADCINLTRIMCTL Register

#### 1 ADC\_CFG\_ADCINLTRIMCTL Register (Offset = FCh) [reset = 0h]

ADC Linearity Trim Control Register.

Return to [Summary Table](#)

**Table 3-359. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 00FCh       |
| ADC1_G0_G5    | 502C 10FCh       |
| ADC2_G0_G5    | 502C 20FCh       |
| ADC3_G0_G5    | 502C 30FCh       |
| ADC4_G0_G5    | 502C 40FCh       |

**Figure 3-119. ADC\_CFG\_ADCINLTRIMCTL Name Register**

|            |    |           |    |    |    |    |           |
|------------|----|-----------|----|----|----|----|-----------|
| 31         | 30 | 29        | 28 | 27 | 26 | 25 | 24        |
| KEY        |    |           |    |    |    |    |           |
| R/W        |    |           |    |    |    |    |           |
| 0h         |    |           |    |    |    |    |           |
| 23         | 22 | 21        | 20 | 19 | 18 | 17 | 16        |
| KEY        |    |           |    |    |    |    |           |
| R/W        |    |           |    |    |    |    |           |
| 0h         |    |           |    |    |    |    |           |
| 15         | 14 | 13        | 12 | 11 | 10 | 9  | 8         |
| RESERVED_1 |    |           |    |    |    |    |           |
| R          |    |           |    |    |    |    |           |
| 0h         |    |           |    |    |    |    |           |
| 7          | 6  | 5         | 4  | 3  | 2  | 1  | 0         |
| RESERVED_1 |    | CALIBSTEP |    |    |    |    | CALIBMODE |
| R          |    | R/W       |    |    |    |    | R/W       |
| 0h         |    | 0h        |    |    |    |    | 0h        |

**Table 3-361. ADC\_CFG\_ADCINLTRIMCTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                   |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | KEY        | R/W  | 0h    | ADC Linearity Trim Control Write Key. Any write to this register must contain the value 0xA5A5 in these bit locations. If a write request attempts to load any other value into these bits, the write for the entire register is ignored. These bits always read back a zero. |
| 15:6  | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                      |
| 5:1   | CALIBSTEP  | R/W  | 0h    | ADC Linearity Calibration Step. Defines which of the 24 steps of calibration is to be executed. Never set this bit field while the ADC SELFTRIM is in progress. The R-M-W operation could unintentionally set the CALIBMODE bit again.                                        |
| 0     | CALIBMODE  | R/W  | 0h    | ADC Linearity Calibration Mode.                                                                                                                                                                                                                                               |

### 3.2.2.120 ADC\_CFG\_REP1CTL Register

#### 1 ADC\_CFG\_REP1CTL Register (Offset = 100h) [reset = 0h]

ADC Trigger Repeater 1 Control Register.

Return to [Summary Table](#)

**Table 3-362. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0100h       |
| ADC1_G0_G5    | 502C 1100h       |
| ADC2_G0_G5    | 502C 2100h       |
| ADC3_G0_G5    | 502C 3100h       |
| ADC4_G0_G5    | 502C 4100h       |

**Figure 3-120. ADC\_CFG\_REP1CTL Name Register**

|            |            |            |         |            |            |            |      |
|------------|------------|------------|---------|------------|------------|------------|------|
| 31         | 30         | 29         | 28      | 27         | 26         | 25         | 24   |
| RESERVED_5 |            |            |         |            |            |            |      |
| R          |            |            |         |            |            |            |      |
| 0h         |            |            |         |            |            |            |      |
| 23         | 22         | 21         | 20      | 19         | 18         | 17         | 16   |
| SWSYNC     | RESERVED_4 | SYNCINSEL  |         |            |            |            |      |
| R/W1TS     | R          | R/W        |         |            |            |            |      |
| 0h         | 0h         | 0h         |         |            |            |            |      |
| 15         | 14         | 13         | 12      | 11         | 10         | 9          | 8    |
| RESERVED_3 | TRIGGER    |            |         |            |            |            |      |
| R          | R/W        |            |         |            |            |            |      |
| 0h         | 0h         |            |         |            |            |            |      |
| 7          | 6          | 5          | 4       | 3          | 2          | 1          | 0    |
| TRIGGEROVF | PHASEOVF   | RESERVED_2 | SOCBUSY | MODULEBUSY | RESERVED_1 | ACTIVEMODE | MODE |
| R/W1TC     | R/W1TC     | R          | R       | R          | R          | R          | R/W  |
| 0h         | 0h         | 0h         | 0h      | 0h         | 0h         | 0h         | 0h   |

**Table 3-364. ADC\_CFG\_REP1CTL Register Field Descriptions**

| Bit   | Field      | Type   | Reset | Description                                                                                                                                                                                                                             |
|-------|------------|--------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED_5 | R      | 0h    | Reserved                                                                                                                                                                                                                                |
| 23    | SWSYNC     | R/W1TS | 0h    | Trigger repeater 1 software force sync. On a sync. event, all registers in repeater 1 are reset to a ready and waiting state. Values of NSEL, PHASE, and MODE are preserved.<br>Note: SOC's associated with repeater 1 are not cleared. |
| 22    | RESERVED_4 | R      | 0h    | Reserved                                                                                                                                                                                                                                |
| 21:16 | SYNCINSEL  | R/W    | 0h    | Trigger repeater 1 sync. input select. On a sync. event, all registers in repeater 1 are reset to a ready and waiting state. Values of NSEL, PHASE, and MODE are preserved.<br>Note: SOC's associated with repeater 1 are not cleared.  |
| 15    | RESERVED_3 | R      | 0h    | Reserved                                                                                                                                                                                                                                |

**Table 3-364. ADC\_CFG\_REP1CTL Register Field Descriptions (continued)**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------|------------|--------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14:8 | TRIGGER    | R/W    | 0h    | <p>ADC Trigger Repeater 1 Trigger Select. Selects the trigger to modify via oversampling or undersampling.</p> <p>00h REPTRIG0 - Software only</p> <p>01h REPTRIG1 - RTI0 Timer</p> <p>02h REPTRIG2 - RTI1 Timer</p> <p>03h REPTRIG3 - RTI2 Timer</p> <p>04h REPTRIG4 - RTI3 Timer</p> <p>05h REPTRIG5 - InputXBAR.Out[5]</p> <p>06h REPTRIG6 - spare</p> <p>07h REPTRIG7 - spare</p> <p>08h REPTRIG8 - EPWM0, ADCSOCA</p> <p>09h REPTRIG9 - EPWM0, ADCSOCA</p> <p>0Ah REPTRIG10 - EPWM1, ADCSOCA</p> <p>0Bh REPTRIG11 - EPWM1, ADCSOCA</p> <p>0Ch REPTRIG12 - EPWM2, ADCSOCA</p> <p>0Dh REPTRIG13 - EPWM2, ADCSOCA</p> <p>0Eh REPTRIG14 - EPWM3, ADCSOCA</p> <p>0Fh REPTRIG15 - EPWM3, ADCSOCA</p> <p>.... EPWM4 to EPWM27</p> <p>40h REPTRIG64 - EPWM28, ADCSOCA</p> <p>41h REPTRIG65 - EPWM28, ADCSOCA</p> <p>42h REPTRIG66 - EPWM29, ADCSOCA</p> <p>43h REPTRIG67 - EPWM29, ADCSOCA</p> <p>44h REPTRIG68 - EPWM30, ADCSOCA</p> <p>45h REPTRIG69 - EPWM30, ADCSOCA</p> <p>46h REPTRIG70 - EPWM31, ADCSOCA</p> <p>47h REPTRIG71 - EPWM31, ADCSOCA</p> <p>48h REPTRIG72 - ECAP0, TRIGOUT</p> <p>.... ECAP1 to ECAP8</p> <p>51h REPTRIG81 - ECAP9, TRIGOUT</p> <p>52h REPTRIG82 - ECAP10, TRIGOUT</p> <p>....</p> <p>57h REPTRIG73 - ECAP15, TRIGOUT</p> <p>58h REPTRIG1 - RTI4 Timer</p> <p>59h REPTRIG1 - RTI5 Timer</p> <p>5Ah REPTRIG1 - RTI6 Timer</p> <p>5Bh REPTRIG1 - RTI7 Timer</p> <p>....</p> <p>7Fh - Reserved</p> |
| 7    | TRIGGEROVF | R/W1TC | 0h    | <p>ADC Trigger Repeater 1 Oversampled Trigger Overflow. Indicates that a trigger was dropped because a trigger arrived while the repeater was still generating repeated oversampled triggers [NCOUNT was not 0 or SOC's associated with Repeater 1 were still pending].</p> <p>Writing a 1 will clear this flag.</p> <p>Note: This flag won't be set in undersampling mode or when NSEL = 0; if a trigger arrives before the previous SOC's have completed, the trigger will be passed and the overflow flags of the SOC's that were still pending will be set.</p> <p>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 6    | PHASEOVF   | R/W1TC | 0h    | <p>ADC Trigger Repeater 1 Phase Delay Overflow. Indicates that a trigger was dropped because a trigger arrived when the phase delay logic was still waiting to send the delayed trigger [PHASECOUNT was not 0].</p> <p>Writing a 1 will clear this flag.</p> <p>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 5    | RESERVED_2 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

**Table 3-364. ADC\_CFG\_REP1CTL Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-----|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | SOCBUSY    | R    | 0h    | ADC Trigger Repeater 1 Associated SOC's Busy indicator. In oversampling mode:<br>0 = no SOC's associated with this repeater are pending<br>1 = SOC's associated with this repeater are still pending<br>The next repeated trigger to the ADC in oversampling mode will not occur until SPREADCOUNT is 0 [minimum time is complete] and REP1CTL.BUSY = 0 [SOC's associated with trigger repeater 1 are no longer pending].<br>Note: If the ADC is in burstmode and the BURSTTRIG is Repeater 1, then all round-robin SOC's are considered associated with this repeater and the repeater will not re-trigger until there are no pending round-robin SOC's [in addition to any associated pending high-priority SOC's]. |
| 3   | MODULEBUSY | R    | 0h    | ADC Trigger Repeater 1 Module Busy indicator. In oversampling mode:<br>0 = Repeater 1 is idle and can accept a new repeated trigger in oversampling mode<br>1 = Repeater 1 still has repeated triggers remaining [NCOUNT ' 0] or associated SOC's are still pending [SOCBUSY is 1]<br>If a new oversampled trigger is received while the module is still busy, the TRIGGEROVF bit will be set and the trigger will be ignored.                                                                                                                                                                                                                                                                                        |
| 2   | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 1   | ACTIVEMODE | R    | 0h    | When a trigger is received in oversampling or undersampling mode the value of MODE is copied to ACTIVEMODE. ACTIVEMODE determines if the repeater will repeat of filter triggers. Changes to MODE while the repeater is working therefore won't cause any changes in functionality until the module becomes idle and then a new trigger is received.<br>0 = module is oversampling<br>1 = module is undersampling                                                                                                                                                                                                                                                                                                     |
| 0   | MODE       | R/W  | 0h    | ADC trigger repeater 1 mode selection. Select either oversampling or undersampling mode.<br>In oversampling mode, when the trigger selected by REP1CTL.TRIGSEL is received, the repeater will repeat the trigger REP1N.NSEL + 1 times.<br>In undersampling mode, when the trigger selected by REP1CTL.TRIGSEL is received the first time, the repeater will pass the trigger through. The next REP1N.NSEL triggers will be ignored.<br>0 = oversampling<br>1 = undersampling                                                                                                                                                                                                                                          |



### 3.2.2.121 ADC\_CFG\_REP1N Register

#### 1 ADC\_CFG\_REP1N Register (Offset = 104h) [reset = 0h]

ADC Trigger Repeater 1 N Select Register.

Return to [Summary Table](#)

**Table 3-365. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0104h       |
| ADC1_G0_G5    | 502C 1104h       |
| ADC2_G0_G5    | 502C 2104h       |
| ADC3_G0_G5    | 502C 3104h       |
| ADC4_G0_G5    | 502C 4104h       |

**Figure 3-121. ADC\_CFG\_REP1N Name Register**

|            |        |    |    |    |    |    |    |
|------------|--------|----|----|----|----|----|----|
| 31         | 30     | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_2 |        |    |    |    |    |    |    |
| R          |        |    |    |    |    |    |    |
| 0h         |        |    |    |    |    |    |    |
| 23         | 22     | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_2 | NCOUNT |    |    |    |    |    |    |
| R          | R      |    |    |    |    |    |    |
| 0h         | 0h     |    |    |    |    |    |    |
| 15         | 14     | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_1 |        |    |    |    |    |    |    |
| R          |        |    |    |    |    |    |    |
| 0h         |        |    |    |    |    |    |    |
| 7          | 6      | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED_1 | NSEL   |    |    |    |    |    |    |
| R          | R/W    |    |    |    |    |    |    |
| 0h         | 0h     |    |    |    |    |    |    |

**Table 3-367. ADC\_CFG\_REP1N Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:23 | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 22:16 | NCOUNT     | R    | 0h    | ADC trigger repeater 1 trigger count.<br>In oversampling mode, indicates the number of triggers remaining to be generated. If a trigger is received corresponding to REP1CTL.TRIGSEL while NCOUNT is not 0 [the repeater is still busy generating the repeated triggers] then the trigger will be ignored and REP1CTL.TRIGOVF will be set to 1.<br>In undersampling mode, indicates the number of triggers remaining to be suppressed. |
| 15:7  | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                               |

**Table 3-367. ADC\_CFG\_REP1N Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6:0 | NSEL  | R/W  | 0h    | <p>ADC Trigger Repeater 1 selection of number of triggers.</p> <p>In oversampling mode, selects the number of repeated triggers. For each trigger received corresponding to REP1CTL.TRIGSEL, NSEL + 1 triggers will be generated.</p> <p>0 = 1 trigger is generated [pass-through]<br/> 1 = 2 triggers are generated<br/> 2 = 3 triggers are generated<br/> ...<br/> 127 = 128 triggers are generated</p> <p>In undersampling mode, selects the number triggers to be suppressed. 1 out NSEL + 1 triggers received corresponding to REP1CTL.TRIGSEL will be passed through [the first trigger will be passed through and the subsequent NSEL triggers will be suppressed].</p> <p>0 = all triggers are passed<br/> 1 = 1 out of 2 triggers are passed<br/> 2 = 1 out of 3 triggers are passed<br/> ...<br/> 127 = 1 out of 128 triggers are passed</p> |

### 3.2.2.122 ADC\_CFG\_REP1PHASE Register

#### 1 ADC\_CFG\_REP1PHASE Register (Offset = 108h) [reset = 0h]

ADC Trigger Repeater 1 Phase Select Register.

Return to [Summary Table](#)

**Table 3-368. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0108h       |
| ADC1_G0_G5    | 502C 1108h       |
| ADC2_G0_G5    | 502C 2108h       |
| ADC3_G0_G5    | 502C 3108h       |
| ADC4_G0_G5    | 502C 4108h       |

**Figure 3-122. ADC\_CFG\_REP1PHASE Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PHASECOUNT |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PHASECOUNT |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PHASE      |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PHASE      |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 3-370. ADC\_CFG\_REP1PHASE Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | PHASECOUNT | R    | 0h    | ADC trigger repeater 1 phase delay status. When the trigger selected by REP1CTL.TRIGSEL is received, this register will start counting down from PHASECOUNT until the counter reaches 0, at which point the trigger will be passed on to the repeater re-trigger logic.<br>If the trigger selected by REP1CTL.TRIGSEL is received when PHASECOUNT is not 0 [the phase delay logic is busy from the previous trigger] then the new trigger will be ignored and REP1CTL.PHASEOVF will be set to 1. |
| 15:0  | PHASE      | R/W  | 0h    | ADC trigger repeater 1 phase delay configuration. Defines the number of SYSCLKs to delay the selected trigger before passing it on to the re-triggering logic.<br>0 = trigger is passed through without delay<br>1 = trigger is delayed by 1 SYSCLK<br>2 = trigger is delayed by 2 SYSCLKs<br>...<br>65535 = trigger is delayed by 65535 SYSCLKs                                                                                                                                                 |

### 3.2.2.123 ADC\_CFG\_REP1SPREAD Register

#### 1 ADC\_CFG\_REP1SPREAD Register (Offset = 10Ch) [reset = 0h]

ADC Trigger Repeater 1 Spread Select Register.

Return to [Summary Table](#)

**Table 3-371. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 010Ch       |
| ADC1_G0_G5    | 502C 110Ch       |
| ADC2_G0_G5    | 502C 210Ch       |
| ADC3_G0_G5    | 502C 310Ch       |
| ADC4_G0_G5    | 502C 410Ch       |

**Figure 3-123. ADC\_CFG\_REP1SPREAD Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SPREADCOUNT |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SPREADCOUNT |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SPREAD      |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SPREAD      |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 3-373. ADC\_CFG\_REP1SPREAD Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|-------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | SPREADCOUNT | R    | 0h    | ADC trigger repeater 1 spread status. When a trigger is sent to the ADC in oversampling mode, this register will start counting down from SPREAD until SPREADCOUNT equals 0.<br>The next repeated trigger to the ADC in oversampling mode will not occur until SPREADCOUNT is 0 [minimum time is complete] and REP1CTL.BUSY = 0 [SOCs associated with trigger repeater 1 are no longer pending]. |

**Table 3-373. ADC\_CFG\_REP1SPREAD Register Field Descriptions (continued)**

| Bit  | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------|--------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | SPREAD | R/W  | 0h    | <p>ADC trigger repeater 1 spread delay configuration. In oversampling mode, defines the minimum number of SYSCLKs to wait before creating the next repeated trigger to the ADC.</p> <p>If SPREAD is less than the time needed for all SOC's associated with repeater 1 to sample and convert, then the repeater will generate triggers as fast as the ADC can convert the associated conversions.</p> <p>If SPREAD is greater than the time needed for all SOC's associated with repeater 1 to sample and convert, then repeated triggers to the ADC will be SPREAD SYSCLK cycles apart.</p> <p>0 = oversampled repeated triggers occur as fast as the ADC can sample and convert associated SOC's</p> <p>1 = time between repeated triggers is at least 1 SYSCLKs</p> <p>2 = time between repeated triggers is at least 2 SYSCLKs</p> <p>...</p> <p>65535 = time between repeated triggers is at least 65535 SYSCLKs</p> |

### 3.2.2.124 ADC\_CFG\_REP1FRC Register

#### 1 ADC\_CFG\_REP1FRC Register (Offset = 110h) [reset = 0h]

ADC Trigger Repeater 1 Software Force Register.

Return to [Summary Table](#)

**Table 3-374. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0110h       |
| ADC1_G0_G5    | 502C 1110h       |
| ADC2_G0_G5    | 502C 2110h       |
| ADC3_G0_G5    | 502C 3110h       |
| ADC4_G0_G5    | 502C 4110h       |

**Figure 3-124. ADC\_CFG\_REP1FRC Name Register**

|            |    |    |    |    |    |   |        |
|------------|----|----|----|----|----|---|--------|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8      |
| RESERVED_1 |    |    |    |    |    |   |        |
| R          |    |    |    |    |    |   |        |
| 0h         |    |    |    |    |    |   |        |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0      |
| RESERVED_1 |    |    |    |    |    |   | SWFRC  |
| R          |    |    |    |    |    |   | R/W1TS |
| 0h         |    |    |    |    |    |   | 0h     |

**Table 3-376. ADC\_CFG\_REP1FRC Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                               |
|------|------------|--------|-------|-----------------------------------------------------------------------------------------------------------|
| 15:1 | RESERVED_1 | R      | 0h    | Reserved                                                                                                  |
| 0    | SWFRC      | R/W1TS | 0h    | Write 1 to force a trigger to repeat block 1 input regardless of the value of TRIGGER.<br>Always reads 0. |

### 3.2.2.125 ADC\_CFG\_REP2CTL Register

#### 1 ADC\_CFG\_REP2CTL Register (Offset = 120h) [reset = 0h]

ADC Trigger Repeater 2 Control Register.

Return to [Summary Table](#)

**Table 3-377. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0120h       |
| ADC1_G0_G5    | 502C 1120h       |
| ADC2_G0_G5    | 502C 2120h       |
| ADC3_G0_G5    | 502C 3120h       |
| ADC4_G0_G5    | 502C 4120h       |

**Figure 3-125. ADC\_CFG\_REP2CTL Name Register**

|            |            |            |         |            |            |            |      |
|------------|------------|------------|---------|------------|------------|------------|------|
| 31         | 30         | 29         | 28      | 27         | 26         | 25         | 24   |
| RESERVED_5 |            |            |         |            |            |            |      |
| R          |            |            |         |            |            |            |      |
| 0h         |            |            |         |            |            |            |      |
| 23         | 22         | 21         | 20      | 19         | 18         | 17         | 16   |
| SWSYNC     | RESERVED_4 | SYNCINSEL  |         |            |            |            |      |
| R/W1TS     | R          | R/W        |         |            |            |            |      |
| 0h         | 0h         | 0h         |         |            |            |            |      |
| 15         | 14         | 13         | 12      | 11         | 10         | 9          | 8    |
| RESERVED_3 | TRIGGER    |            |         |            |            |            |      |
| R          | R/W        |            |         |            |            |            |      |
| 0h         | 0h         |            |         |            |            |            |      |
| 7          | 6          | 5          | 4       | 3          | 2          | 1          | 0    |
| TRIGGEROVF | PHASEOVF   | RESERVED_2 | SOCBUSY | MODULEBUSY | RESERVED_1 | ACTIVEMODE | MODE |
| R/W1TC     | R/W1TC     | R          | R       | R          | R          | R          | R/W  |
| 0h         | 0h         | 0h         | 0h      | 0h         | 0h         | 0h         | 0h   |

**Table 3-379. ADC\_CFG\_REP2CTL Register Field Descriptions**

| Bit   | Field      | Type   | Reset | Description                                                                                                                                                                                                                             |
|-------|------------|--------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED_5 | R      | 0h    | Reserved                                                                                                                                                                                                                                |
| 23    | SWSYNC     | R/W1TS | 0h    | Trigger repeater 2 software force sync. On a sync. event, all registers in repeater 2 are reset to a ready and waiting state. Values of NSEL, PHASE, and MODE are preserved.<br>Note: SOC's associated with repeater 2 are not cleared. |
| 22    | RESERVED_4 | R      | 0h    | Reserved                                                                                                                                                                                                                                |
| 21:16 | SYNCINSEL  | R/W    | 0h    | Trigger repeater 2 sync. input select. On a sync. event, all registers in repeater 2 are reset to a ready and waiting state. Values of NSEL, PHASE, and MODE are preserved.<br>Note: SOC's associated with repeater 2 are not cleared.  |
| 15    | RESERVED_3 | R      | 0h    | Reserved                                                                                                                                                                                                                                |

**Table 3-379. ADC\_CFG\_REP2CTL Register Field Descriptions (continued)**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------|------------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14:8 | TRIGGER    | R/W    | 0h    | <p>ADC Trigger Repeater 2 Trigger Select. Selects the trigger to modify via oversampling or undersampling.</p> <p>00h REPTRIG0 - Software only</p> <p>01h REPTRIG1 - RTI0 Timer</p> <p>02h REPTRIG2 - RTI1 Timer</p> <p>03h REPTRIG3 - RTI2 Timer</p> <p>04h REPTRIG4 - RTI3 Timer</p> <p>05h REPTRIG5 - InputXBAR.Out[5]</p> <p>06h REPTRIG6 - spare</p> <p>07h REPTRIG7 - spare</p> <p>08h REPTRIG8 - EPWM0, ADCSOCA</p> <p>09h REPTRIG9 - EPWM0, ADCSOCA</p> <p>0Ah REPTRIG10 - EPWM1, ADCSOCA</p> <p>0Bh REPTRIG11 - EPWM1, ADCSOCA</p> <p>0Ch REPTRIG12 - EPWM2, ADCSOCA</p> <p>0Dh REPTRIG13 - EPWM2, ADCSOCA</p> <p>0Eh REPTRIG14 - EPWM3, ADCSOCA</p> <p>0Fh REPTRIG15 - EPWM3, ADCSOCA</p> <p>.... EPWM4 to EPWM27</p> <p>40h REPTRIG64 - EPWM28, ADCSOCA</p> <p>41h REPTRIG65 - EPWM28, ADCSOCA</p> <p>42h REPTRIG66 - EPWM29, ADCSOCA</p> <p>43h REPTRIG67 - EPWM29, ADCSOCA</p> <p>44h REPTRIG68 - EPWM30, ADCSOCA</p> <p>45h REPTRIG69 - EPWM30, ADCSOCA</p> <p>46h REPTRIG70 - EPWM31, ADCSOCA</p> <p>47h REPTRIG71 - EPWM31, ADCSOCA</p> <p>48h REPTRIG72 - ECAP0, TRIGOUT</p> <p>.... ECAP1 to ECAP8</p> <p>51h REPTRIG81 - ECAP9, TRIGOUT</p> <p>52h REPTRIG82 - ECAP10, TRIGOUT</p> <p>....</p> <p>57h REPTRIG73 - ECAP15, TRIGOUT</p> <p>58h REPTRIG1 - RTI4 Timer</p> <p>59h REPTRIG1 - RTI5 Timer</p> <p>5Ah REPTRIG1 - RTI6 Timer</p> <p>5Bh REPTRIG1 - RTI7 Timer</p> <p>....</p> <p>64h- 7Fh - Reserved</p> |
| 7    | TRIGGEROVF | R/W1TC | 0h    | <p>ADC Trigger Repeater 2 Oversampled Trigger Overflow. Indicates that a trigger was dropped because a trigger arrived while the repeater was still generating repeated oversampled triggers [NCOUNT was not 0 or SOC's associated with Repeater 2 were still pending].</p> <p>Writing a 1 will clear this flag.</p> <p>Note: This flag won't be set in undersampling mode or when NSEL = 0; if a trigger arrives before the previous SOC's have completed, the trigger will be passed and the overflow flags of the SOC's that were still pending will be set.</p> <p>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 6    | PHASEOVF   | R/W1TC | 0h    | <p>ADC Trigger Repeater 2 Phase Delay Overflow. Indicates that a trigger was dropped because a trigger arrived when the phase delay logic was still waiting to send the delayed trigger [PHASECOUNT was not 0].</p> <p>Writing a 1 will clear this flag.</p> <p>Note: If software sets the clear bit on the same cycle that hardware is trying to set the flag bit, then hardware has priority and the overflow bit will not be set</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 5    | RESERVED_2 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |



**Table 3-379. ADC\_CFG\_REP2CTL Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-----|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | SOCBUSY    | R    | 0h    | ADC Trigger Repeater 2 Associated SOC's Busy indicator. In oversampling mode:<br>0 = no SOC's associated with this repeater are pending<br>1 = SOC's associated with this repeater are still pending<br>The next repeated trigger to the ADC in oversampling mode will not occur until SPREADCOUNT is 0 [minimum time is complete] and REP2CTL.BUSY = 0 [SOC's associated with trigger repeater 2 are no longer pending].<br>Note: If the ADC is in burstmode and the BURSTTRIG is Repeater 2, then all round-robin SOC's are considered associated with this repeater and the repeater will not re-trigger until there are no pending round-robin SOC's [in addition to any associated pending high-priority SOC's]. |
| 3   | MODULEBUSY | R    | 0h    | ADC Trigger Repeater 2 Module Busy indicator. In oversampling mode:<br>0 = Repeater 2 is idle and can accept a new repeated trigger in oversampling mode<br>1 = Repeater 2 still has repeated triggers remaining [NCOUNT ' 0] or associated SOC's are still pending [SOCBUSY is 1]<br>If a new oversampled trigger is received while the module is still busy, the TRIGGEROVF bit will be set and the trigger will be ignored.                                                                                                                                                                                                                                                                                        |
| 2   | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 1   | ACTIVEMODE | R    | 0h    | When a trigger is received in oversampling or undersampling mode the value of MODE is copied to ACTIVEMODE. ACTIVEMODE determines if the repeater will repeat of filter triggers. Changes to MODE while the repeater is working therefore won't cause any changes in functionality until the module becomes idle and then a new trigger is received.<br>0 = module is oversampling<br>1 = module is undersampling                                                                                                                                                                                                                                                                                                     |
| 0   | MODE       | R/W  | 0h    | ADC trigger repeater 2 mode selection. Select either oversampling or undersampling mode.<br>In oversampling mode, when the trigger selected by REP2CTL.TRIGSEL is received, the repeater will repeat the trigger REP2N.NSEL + 1 times.<br>In undersampling mode, when the trigger selected by REP2CTL.TRIGSEL is received the first time, the repeater will pass the trigger through. The next REP2N.NSEL triggers will be ignored.<br>0 = oversampling<br>1 = undersampling                                                                                                                                                                                                                                          |

### 3.2.2.126 ADC\_CFG\_REP2N Register

#### 1 ADC\_CFG\_REP2N Register (Offset = 124h) [reset = 0h]

ADC Trigger Repeater 2 N Select Register.

Return to [Summary Table](#)

**Table 3-380. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0124h       |
| ADC1_G0_G5    | 502C 1124h       |
| ADC2_G0_G5    | 502C 2124h       |
| ADC3_G0_G5    | 502C 3124h       |
| ADC4_G0_G5    | 502C 4124h       |

**Figure 3-126. ADC\_CFG\_REP2N Name Register**

|            |        |    |    |    |    |    |    |
|------------|--------|----|----|----|----|----|----|
| 31         | 30     | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_2 |        |    |    |    |    |    |    |
| R          |        |    |    |    |    |    |    |
| 0h         |        |    |    |    |    |    |    |
| 23         | 22     | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_2 | NCOUNT |    |    |    |    |    |    |
| R          | R      |    |    |    |    |    |    |
| 0h         | 0h     |    |    |    |    |    |    |
| 15         | 14     | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_1 |        |    |    |    |    |    |    |
| R          |        |    |    |    |    |    |    |
| 0h         |        |    |    |    |    |    |    |
| 7          | 6      | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED_1 | NSEL   |    |    |    |    |    |    |
| R          | R/W    |    |    |    |    |    |    |
| 0h         | 0h     |    |    |    |    |    |    |

**Table 3-382. ADC\_CFG\_REP2N Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:23 | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 22:16 | NCOUNT     | R    | 0h    | ADC trigger repeater 2 trigger count.<br>In oversampling mode, indicates the number of triggers remaining to be generated. If a trigger is received corresponding to REP2CTL.TRIGSEL while NCOUNT is not 0 [the repeater is still busy generating the repeated triggers] then the trigger will be ignored and REP2CTL.TRIGOVF will be set to 1.<br>In undersampling mode, indicates the number of triggers remaining to be suppressed. |
| 15:7  | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                               |

**Table 3-382. ADC\_CFG\_REP2N Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6:0 | NSEL  | R/W  | 0h    | <p>ADC Trigger Repeater 2 selection of number of triggers.</p> <p>In oversampling mode, selects the number of repeated triggers. For each trigger received corresponding to REP2CTL.TRIGSEL, NSEL + 1 triggers will be generated.</p> <p>0 = 1 trigger is generated [pass-through]<br/> 1 = 2 triggers are generated<br/> 2 = 3 triggers are generated<br/> ...<br/> 127 = 128 triggers are generated</p> <p>In undersampling mode, selects the number triggers to be suppressed. 1 out NSEL + 1 triggers received corresponding to REP2CTL.TRIGSEL will be passed through [the first trigger will be passed through and the subsequent NSEL triggers will be suppressed].</p> <p>0 = all triggers are passed<br/> 1 = 1 out of 2 triggers are passed<br/> 2 = 1 out of 3 triggers are passed<br/> ...<br/> 127 = 1 out of 128 triggers are passed</p> |

### 3.2.2.127 ADC\_CFG\_REP2PHASE Register

#### 1 ADC\_CFG\_REP2PHASE Register (Offset = 128h) [reset = 0h]

ADC Trigger Repeater 2 Phase Select Register.

Return to [Summary Table](#)

**Table 3-383. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0128h       |
| ADC1_G0_G5    | 502C 1128h       |
| ADC2_G0_G5    | 502C 2128h       |
| ADC3_G0_G5    | 502C 3128h       |
| ADC4_G0_G5    | 502C 4128h       |

**Figure 3-127. ADC\_CFG\_REP2PHASE Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PHASECOUNT |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PHASECOUNT |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PHASE      |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PHASE      |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 3-385. ADC\_CFG\_REP2PHASE Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | PHASECOUNT | R    | 0h    | ADC trigger repeater 2 phase delay status. When the trigger selected by REP2CTL.TRIGSEL is received, this register will start counting down from PHASECOUNT until the counter reaches 0, at which point the trigger will be passed on to the repeater re-trigger logic.<br>If the trigger selected by REP2CTL.TRIGSEL is received when PHASECOUNT is not 0 [the phase delay logic is busy from the previous trigger] then the new trigger will be ignored and REP2CTL.PHASEOVF will be set to 1. |
| 15:0  | PHASE      | R/W  | 0h    | ADC trigger repeater 2 phase delay configuration. Defines the number of SYSCLKs to delay the selected trigger before passing it on to the re-triggering logic.<br>0 = trigger is passed through without delay<br>1 = trigger is delayed by 1 SYSCLK<br>2 = trigger is delayed by 2 SYSCLKs<br>...<br>65535 = trigger is delayed by 65535 SYSCLKs                                                                                                                                                 |

### 3.2.2.128 ADC\_CFG\_REP2SPREAD Register

#### 1 ADC\_CFG\_REP2SPREAD Register (Offset = 12Ch) [reset = 0h]

ADC Trigger Repeater 2 Spread Select Register.

Return to [Summary Table](#)

**Table 3-386. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 012Ch       |
| ADC1_G0_G5    | 502C 112Ch       |
| ADC2_G0_G5    | 502C 212Ch       |
| ADC3_G0_G5    | 502C 312Ch       |
| ADC4_G0_G5    | 502C 412Ch       |

**Figure 3-128. ADC\_CFG\_REP2SPREAD Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SPREADCOUNT |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SPREADCOUNT |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SPREAD      |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SPREAD      |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 3-388. ADC\_CFG\_REP2SPREAD Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|-------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | SPREADCOUNT | R    | 0h    | ADC trigger repeater 2 spread status. When a trigger is sent to the ADC in oversampling mode, this register will start counting down from SPREAD until SPREADCOUNT equals 0.<br>The next repeated trigger to the ADC in oversampling mode will not occur until SPREADCOUNT is 0 [minimum time is complete] and REP2CTL.BUSY = 0 [SOCs associated with trigger repeater 2 are no longer pending]. |

**Table 3-388. ADC\_CFG\_REP2SPREAD Register Field Descriptions (continued)**

| Bit  | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------|--------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | SPREAD | R/W  | 0h    | <p>ADC trigger repeater 2 spread delay configuration. In oversampling mode, defines the minimum number of SYSCLKs to wait before creating the next repeated trigger to the ADC.</p> <p>If SPREAD is less than the time needed for all SOC's associated with repeater 2 to sample and convert, then the repeater will generate triggers as fast as the ADC can convert the associated conversions.</p> <p>If SPREAD is greater than the time needed for all SOC's associated with repeater 2 to sample and convert, then repeated triggers to the ADC will be SPREAD SYSCLK cycles apart.</p> <p>0 = oversampled repeated triggers occur as fast as the ADC can sample and convert associated SOC's</p> <p>1 = time between repeated triggers is at least 1 SYSCLKs</p> <p>2 = time between repeated triggers is at least 2 SYSCLKs</p> <p>...</p> <p>65535 = time between repeated triggers is at least 65535 SYSCLKs</p> |

### 3.2.2.129 ADC\_CFG\_REP2FRC Register

#### 1 ADC\_CFG\_REP2FRC Register (Offset = 130h) [reset = 0h]

ADC Trigger Repeater 2 Software Force Register.

Return to [Summary Table](#)

**Table 3-389. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0130h       |
| ADC1_G0_G5    | 502C 1130h       |
| ADC2_G0_G5    | 502C 2130h       |
| ADC3_G0_G5    | 502C 3130h       |
| ADC4_G0_G5    | 502C 4130h       |

**Figure 3-129. ADC\_CFG\_REP2FRC Name Register**

|            |    |    |    |    |    |   |        |
|------------|----|----|----|----|----|---|--------|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8      |
| RESERVED_1 |    |    |    |    |    |   |        |
| R          |    |    |    |    |    |   |        |
| 0h         |    |    |    |    |    |   |        |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0      |
| RESERVED_1 |    |    |    |    |    |   | SWFRC  |
| R          |    |    |    |    |    |   | R/W1TS |
| 0h         |    |    |    |    |    |   | 0h     |

**Table 3-391. ADC\_CFG\_REP2FRC Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                               |
|------|------------|--------|-------|-----------------------------------------------------------------------------------------------------------|
| 15:1 | RESERVED_1 | R      | 0h    | Reserved                                                                                                  |
| 0    | SWFRC      | R/W1TS | 0h    | Write 1 to force a trigger to repeat block 2 input regardless of the value of TRIGGER.<br>Always reads 0. |

### 3.2.2.130 ADC\_CFG\_ADCPPB1LIMIT Register

#### 1 ADC\_CFG\_ADCPPB1LIMIT Register (Offset = 140h) [reset = 0h]

ADC PPB1Conversion Count Limit Register.

Return to [Summary Table](#)

**Table 3-392. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0140h       |
| ADC1_G0_G5    | 502C 1140h       |
| ADC2_G0_G5    | 502C 2140h       |
| ADC3_G0_G5    | 502C 3140h       |
| ADC4_G0_G5    | 502C 4140h       |

**Figure 3-130. ADC\_CFG\_ADCPPB1LIMIT Name Register**

|            |    |    |    |    |    |       |   |
|------------|----|----|----|----|----|-------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9     | 8 |
| RESERVED_1 |    |    |    |    |    | LIMIT |   |
| R          |    |    |    |    |    | R/W   |   |
| 0h         |    |    |    |    |    | 0h    |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1     | 0 |
| LIMIT      |    |    |    |    |    |       |   |
| R/W        |    |    |    |    |    |       |   |
| 0h         |    |    |    |    |    |       |   |

**Table 3-394. ADC\_CFG\_ADCPPB1LIMIT Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                               |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                  |
| 9:0   | LIMIT      | R/W  | 0h    | Post Processing Block 1 Oversampling Limit. Defines the number of conversions to accumulate before PSUM is automatically loaded into SUM. |



### 3.2.2.131 ADC\_CFG\_ADCPPBP1PCOUNT Register

#### 1 ADC\_CFG\_ADCPPBP1PCOUNT Register (Offset = 144h) [reset = 0h]

ADC PPB1 Partial Conversion Count Register.

Return to [Summary Table](#)

**Table 3-395. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0144h       |
| ADC1_G0_G5    | 502C 1144h       |
| ADC2_G0_G5    | 502C 2144h       |
| ADC3_G0_G5    | 502C 3144h       |
| ADC4_G0_G5    | 502C 4144h       |

**Figure 3-131. ADC\_CFG\_ADCPPBP1PCOUNT Name Register**

|            |    |    |    |    |    |        |   |
|------------|----|----|----|----|----|--------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9      | 8 |
| RESERVED_1 |    |    |    |    |    | PCOUNT |   |
| R          |    |    |    |    |    | R      |   |
| 0h         |    |    |    |    |    | 0h     |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1      | 0 |
| PCOUNT     |    |    |    |    |    |        |   |
| R          |    |    |    |    |    |        |   |
| 0h         |    |    |    |    |    |        |   |

**Table 3-397. ADC\_CFG\_ADCPPBP1PCOUNT Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 9:0   | PCOUNT     | R    | 0h    | Post Processing Block 1 Oversampling Partial Count. Each time a new result propagates through the PPB signal chain and accumulates into ADCPPBP1PSUM this register is incremented by 1. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPBP1RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPBP1RESULT timing information]. |

### 3.2.2.132 ADC\_CFG\_ADCPPB1CONFIG2 Register

#### 1 ADC\_CFG\_ADCPPB1CONFIG2 Register (Offset = 148h) [reset = 0h]

ADC PPB1 Sum Shift Register.

Return to [Summary Table](#)

**Table 3-398. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0148h       |
| ADC1_G0_G5    | 502C 1148h       |
| ADC2_G0_G5    | 502C 2148h       |
| ADC3_G0_G5    | 502C 3148h       |
| ADC4_G0_G5    | 502C 4148h       |

**Figure 3-132. ADC\_CFG\_ADCPPB1CONFIG2 Name Register**

| 15        | 14 | 13         | 12       | 11     | 10         | 9         | 8 |
|-----------|----|------------|----------|--------|------------|-----------|---|
| COMPSEL   |    | RESERVED_2 | OSINTSEL | SWSYNC | RESERVED_1 | SYNCINSEL |   |
| R/W       |    | R          | R/W      | R/W1TS | R          | R/W       |   |
| 0h        |    | 0h         | 0h       | 0h     | 0h         | 0h        |   |
| 7         | 6  | 5          | 4        | 3      | 2          | 1         | 0 |
| SYNCINSEL |    |            |          | SHIFT  |            |           |   |
| R/W       |    |            |          | R/W    |            |           |   |
| 0h        |    |            |          | 0h     |            |           |   |

**Table 3-400. ADC\_CFG\_ADCPPB1CONFIG2 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | COMPSEL    | R/W  | 0h    | Post Processing Block 1 Compare Source Select. This field determines whether ADCPPB1RESULT, ADCPPB1PSUM, or ADCPPB1SUM is used for the zero-crossing detect logic and threshold compare.<br>00 = ADCPPB1RESULT is used for compare logic<br>01 = ADCPPB1PSUM is used for compare logic<br>10 = ADCPPB1SUM is used for compare logic<br>11 = Reserved<br>Note: when ADCPPB1PSUM is selected as the compare source and when a LIMIT match occurs [ADCPB1LIMIT equals ADCPPB1COUNT] the ADCPPB1PSUM register will be cleared and the final sum will be loaded into ADCPPB1SUM. For this sample, the final sum, ADCPPB1SUM will be used for the comparision instead of ADCPPB1PSUM. |
| 13    | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 12    | OSINTSEL   | R/W  | 0h    | Post Processing Block 1 Interrupt Source Select.<br>OSINT1 can be used to trigger an ADC interrupt [ADCINT1 through ADCINT4] via selection in the ADCINT1N2 or ADCINT3N4. This selection determines if a sync. event can trigger OSINT1 in addition to a PCOUNT = LIMIT event.<br>0 = OSINT1 will be generated from PCOUNT = LIMIT only<br>1 = OSTIN1 will be generated form PCOUNT = LIMIT or a sync. event.<br>Note: If a SYNC event would cause an OSINT one cycle after OSINT would have been cause by PCOUNT = LIMIT match, then the second OSINT is ignored.                                                                                                              |

**Table 3-400. ADC\_CFG\_ADCPPB1CONFIG2 Register Field Descriptions (continued)**

| Bit | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                         |
|-----|------------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11  | SWSYNC     | R/W1TS | 0h    | PPB 1 software force sync. On a sync. event, all partial registers transfer to the final registers and are then reset.<br>Note: In the case where the software force occurs at the same time that a new sample is added to the PSUM and the PSUM is being used for a high or low limit compare, then the comparison will not occur. |
| 10  | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                            |
| 9:4 | SYNCINSEL  | R/W    | 0h    | PPB 1 sync. input select. On a sync. event, all partial registers transfer to the final registers and are then reset.                                                                                                                                                                                                               |
| 3:0 | SHIFT      | R/W    | 0h    | Post Processing Block 1 right shift. Defines the number of bits to right shift PSUM before loading into the final SUM.<br>0 : no right shift<br>1 : SUM = PSUM " 1<br>2 : SUM = PSUM " 2<br>...<br>10 : SUM = PSUM " 10<br>11 -<br>15 : Reserved                                                                                    |

### 3.2.2.133 ADC\_CFG\_ADCPPB1PSUM Register

#### 1 ADC\_CFG\_ADCPPB1PSUM Register (Offset = 14Ch) [reset = 0h]

ADC PPB1 Partial Sum Register.

Return to [Summary Table](#)

**Table 3-401. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 014Ch       |
| ADC1_G0_G5    | 502C 114Ch       |
| ADC2_G0_G5    | 502C 214Ch       |
| ADC3_G0_G5    | 502C 314Ch       |
| ADC4_G0_G5    | 502C 414Ch       |

**Figure 3-133. ADC\_CFG\_ADCPPB1PSUM Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SIGN |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PSUM |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PSUM |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PSUM |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 3-403. ADC\_CFG\_ADCPPB1PSUM Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 23.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 23:0  | PSUM  | R    | 0h    | Post Processing Block 1 Oversampling Partial Sum. Each time a new result propagates through the PPB signal chain and latches into ADCPPB1RESULT the result is subsequently accumulated into this register.<br>This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event.<br>This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be available 2 SYSCLK cycle after the associated ADCRESULT and subsequent results [in order from lowest numbered PPB to highest] will each become available every 2-3 SYSCLK cycles [refer to the TRM for detailed timing information]. |

### 3.2.2.134 ADC\_CFG\_ADCPPB1PMAX Register

#### 1 ADC\_CFG\_ADCPPB1PMAX Register (Offset = 150h) [reset = 0h]

ADC PPB1 Partial Max Register.

Return to [Summary Table](#)

**Table 3-404. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0150h       |
| ADC1_G0_G5    | 502C 1150h       |
| ADC2_G0_G5    | 502C 2150h       |
| ADC3_G0_G5    | 502C 3150h       |
| ADC4_G0_G5    | 502C 4150h       |

**Figure 3-134. ADC\_CFG\_ADCPPB1PMAX Name Register**

|      |    |    |    |    |    |    |      |
|------|----|----|----|----|----|----|------|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24   |
| SIGN |    |    |    |    |    |    |      |
| R    |    |    |    |    |    |    |      |
| 0h   |    |    |    |    |    |    |      |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16   |
| SIGN |    |    |    |    |    |    | PMAX |
| R    |    |    |    |    |    |    | R    |
| 0h   |    |    |    |    |    |    | 0h   |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8    |
| PMAX |    |    |    |    |    |    |      |
| R    |    |    |    |    |    |    |      |
| 0h   |    |    |    |    |    |    |      |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0    |
| PMAX |    |    |    |    |    |    |      |
| R    |    |    |    |    |    |    |      |
| 0h   |    |    |    |    |    |    |      |

**Table 3-406. ADC\_CFG\_ADCPPB1PMAX Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 16.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 16:0  | PMAX  | R    | 0h    | Post Processing Block 1 Oversampling Partial Max. Each time a new result propagates through the PPB signal chain and latches into ADCPPB1RESULT the result replaces this register if it is larger. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information]. |

### 3.2.2.135 ADC\_CFG\_ADCPPB1PMAXI Register

#### 1 ADC\_CFG\_ADCPPB1PMAXI Register (Offset = 154h) [reset = 0h]

ADC PPB1 Partial Max Index Register.

Return to [Summary Table](#)

**Table 3-407. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0154h       |
| ADC1_G0_G5    | 502C 1154h       |
| ADC2_G0_G5    | 502C 2154h       |
| ADC3_G0_G5    | 502C 3154h       |
| ADC4_G0_G5    | 502C 4154h       |

**Figure 3-135. ADC\_CFG\_ADCPPB1PMAXI Name Register**

|            |    |    |    |    |    |       |   |
|------------|----|----|----|----|----|-------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9     | 8 |
| RESERVED_1 |    |    |    |    |    | PMAXI |   |
| R          |    |    |    |    |    | R     |   |
| 0h         |    |    |    |    |    | 0h    |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1     | 0 |
| PMAXI      |    |    |    |    |    |       |   |
| R          |    |    |    |    |    |       |   |
| 0h         |    |    |    |    |    |       |   |

**Table 3-409. ADC\_CFG\_ADCPPB1PMAXI Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 9:0   | PMAXI      | R    | 0h    | Post Processing Block 1 Oversampling Partial Index of Max. Each time a new result propagates through the PPB signal chain and latches into ADCPPB1RESULT if the result replaces PMAX this register is loaded with the current value of PCOUNT.<br>This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event.<br>This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information]. |

### 3.2.2.136 ADC\_CFG\_ADCPPB1PMIN Register

#### 1 ADC\_CFG\_ADCPPB1PMIN Register (Offset = 158h) [reset = 0h]

ADC PPB1 Partial MIN Register.

Return to [Summary Table](#)

**Table 3-410. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0158h       |
| ADC1_G0_G5    | 502C 1158h       |
| ADC2_G0_G5    | 502C 2158h       |
| ADC3_G0_G5    | 502C 3158h       |
| ADC4_G0_G5    | 502C 4158h       |

**Figure 3-136. ADC\_CFG\_ADCPPB1PMIN Name Register**

|      |    |    |    |    |    |    |      |
|------|----|----|----|----|----|----|------|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24   |
| SIGN |    |    |    |    |    |    |      |
| R    |    |    |    |    |    |    |      |
| 0h   |    |    |    |    |    |    |      |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16   |
| SIGN |    |    |    |    |    |    | PMIN |
| R    |    |    |    |    |    |    | R    |
| 0h   |    |    |    |    |    |    | 0h   |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8    |
| PMIN |    |    |    |    |    |    |      |
| R    |    |    |    |    |    |    |      |
| 0h   |    |    |    |    |    |    |      |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0    |
| PMIN |    |    |    |    |    |    |      |
| R    |    |    |    |    |    |    |      |
| 0h   |    |    |    |    |    |    |      |

**Table 3-412. ADC\_CFG\_ADCPPB1PMIN Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 16.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 16:0  | PMIN  | R    | 0h    | Post Processing Block 1 Oversampling Partial Min. Each time a new result propagates through the PPB signal chain and latches into ADCPPB1RESULT the result replaces this register if it is smaller. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information]. |

### 3.2.2.137 ADC\_CFG\_ADCPPB1PMINI Register

#### 1 ADC\_CFG\_ADCPPB1PMINI Register (Offset = 15Ch) [reset = 0h]

ADC PPB1 Partial Min Index Register.

Return to [Summary Table](#)

**Table 3-413. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 015Ch       |
| ADC1_G0_G5    | 502C 115Ch       |
| ADC2_G0_G5    | 502C 215Ch       |
| ADC3_G0_G5    | 502C 315Ch       |
| ADC4_G0_G5    | 502C 415Ch       |

**Figure 3-137. ADC\_CFG\_ADCPPB1PMINI Name Register**

|            |    |    |    |    |    |       |   |
|------------|----|----|----|----|----|-------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9     | 8 |
| RESERVED_1 |    |    |    |    |    | PMINI |   |
| R          |    |    |    |    |    | R     |   |
| 0h         |    |    |    |    |    | 0h    |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1     | 0 |
| PMINI      |    |    |    |    |    |       |   |
| R          |    |    |    |    |    |       |   |
| 0h         |    |    |    |    |    |       |   |

**Table 3-415. ADC\_CFG\_ADCPPB1PMINI Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 9:0   | PMINI      | R    | 0h    | Post Processing Block 1 Oversampling Partial Index of Min. Each time a new result propagates through the PPB signal chain and latches into ADCPPB1RESULT if the result replaces PMIN this register is loaded with the current value of PCOUNT.<br>This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB1 receives a sync. event.<br>This result is available 1 SYSCLK cycle after the associated ADCPPB1RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB1RESULT timing information]. |



### 3.2.2.138 ADC\_CFG\_ADCPPB1TRIPLO2 Register

#### 1 ADC\_CFG\_ADCPPB1TRIPLO2 Register (Offset = 160h) [reset = 0h]

ADC PPB1 Extended Trip Low Register.

Return to [Summary Table](#)

**Table 3-416. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0160h       |
| ADC1_G0_G5    | 502C 1160h       |
| ADC2_G0_G5    | 502C 2160h       |
| ADC3_G0_G5    | 502C 3160h       |
| ADC4_G0_G5    | 502C 4160h       |

**Figure 3-138. ADC\_CFG\_ADCPPB1TRIPLO2 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_1 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LIMITLO    |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| LIMITLO    |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LIMITLO    |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 3-418. ADC\_CFG\_ADCPPB1TRIPLO2 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                   |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                      |
| 23:0  | LIMITLO    | R/W  | 0h    | ADC Post Processing Block 1 Trip High Low Limit. This value sets the digital comparator trip low limit if ADCPPB1TRIPLO.LIMITLO2EN = 1.<br>When comparing to an ADCPPBxRESULT register, the upper bits will be ignored:<br>- TRIPLO2[23:17] will be ignored in 16 bit mode<br>- TRIPLO2[23:13] will be ignored in 12 bit mode |

### 3.2.2.139 ADC\_CFG\_ADCPPB2LIMIT Register

#### 1 ADC\_CFG\_ADCPPB2LIMIT Register (Offset = 174h) [reset = 0h]

ADC PPB2Conversion Count Limit Register.

Return to [Summary Table](#)

**Table 3-419. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0174h       |
| ADC1_G0_G5    | 502C 1174h       |
| ADC2_G0_G5    | 502C 2174h       |
| ADC3_G0_G5    | 502C 3174h       |
| ADC4_G0_G5    | 502C 4174h       |

**Figure 3-139. ADC\_CFG\_ADCPPB2LIMIT Name Register**

|            |    |    |    |    |    |       |   |
|------------|----|----|----|----|----|-------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9     | 8 |
| RESERVED_1 |    |    |    |    |    | LIMIT |   |
| R          |    |    |    |    |    | R/W   |   |
| 0h         |    |    |    |    |    | 0h    |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1     | 0 |
| LIMIT      |    |    |    |    |    |       |   |
| R/W        |    |    |    |    |    |       |   |
| 0h         |    |    |    |    |    |       |   |

**Table 3-421. ADC\_CFG\_ADCPPB2LIMIT Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                               |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                  |
| 9:0   | LIMIT      | R/W  | 0h    | Post Processing Block 2 Oversampling Limit. Defines the number of conversions to accumulate before PSUM is automatically loaded into SUM. |

### 3.2.2.140 ADC\_CFG\_ADCPPBP2PCOUNT Register

#### 1 ADC\_CFG\_ADCPPBP2PCOUNT Register (Offset = 178h) [reset = 0h]

ADC PPB2 Partial Conversion Count Register.

Return to [Summary Table](#)

**Table 3-422. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0178h       |
| ADC1_G0_G5    | 502C 1178h       |
| ADC2_G0_G5    | 502C 2178h       |
| ADC3_G0_G5    | 502C 3178h       |
| ADC4_G0_G5    | 502C 4178h       |

**Figure 3-140. ADC\_CFG\_ADCPPBP2PCOUNT Name Register**

|            |    |    |    |    |    |        |   |
|------------|----|----|----|----|----|--------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9      | 8 |
| RESERVED_1 |    |    |    |    |    | PCOUNT |   |
| R          |    |    |    |    |    | R      |   |
| 0h         |    |    |    |    |    | 0h     |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1      | 0 |
| PCOUNT     |    |    |    |    |    |        |   |
| R          |    |    |    |    |    |        |   |
| 0h         |    |    |    |    |    |        |   |

**Table 3-424. ADC\_CFG\_ADCPPBP2PCOUNT Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 9:0   | PCOUNT     | R    | 0h    | Post Processing Block 2 Oversampling Partial Count. Each time a new result propagates through the PPB signal chain and accumulates into ADCPPB2PSUM this register is incremented by 1. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information]. |

### 3.2.2.141 ADC\_CFG\_ADCPPB2CONFIG2 Register

#### 1 ADC\_CFG\_ADCPPB2CONFIG2 Register (Offset = 17Ch) [reset = 0h]

ADC PPB2 Sum Shift Register.

Return to [Summary Table](#)

**Table 3-425. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 017Ch       |
| ADC1_G0_G5    | 502C 117Ch       |
| ADC2_G0_G5    | 502C 217Ch       |
| ADC3_G0_G5    | 502C 317Ch       |
| ADC4_G0_G5    | 502C 417Ch       |

**Figure 3-141. ADC\_CFG\_ADCPPB2CONFIG2 Name Register**

| 15        | 14         | 13       | 12     | 11         | 10        | 9     | 8 |
|-----------|------------|----------|--------|------------|-----------|-------|---|
| COMPSEL   | RESERVED_2 | OSINTSEL | SWSYNC | RESERVED_1 | SYNCINSEL |       |   |
| R/W       | R          | R/W      | R/W1TS | R          | R/W       |       |   |
| 0h        | 0h         | 0h       | 0h     | 0h         | 0h        |       |   |
| 7         | 6          | 5        | 4      | 3          | 2         | 1     | 0 |
| SYNCINSEL |            |          |        |            |           | SHIFT |   |
| R/W       |            |          |        |            |           | R/W   |   |
| 0h        |            |          |        |            |           | 0h    |   |

**Table 3-427. ADC\_CFG\_ADCPPB2CONFIG2 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | COMPSEL    | R/W  | 0h    | Post Processing Block 2 Compare Source Select. This field determines whether ADCPPB2RESULT, ADCPPB2PSUM, or ADCPPB2SUM is used for the zero-crossing detect logic and threshold compare.<br>00 = ADCPPB2RESULT is used for compare logic<br>01 = ADCPPB2PSUM is used for compare logic<br>10 = ADCPPB2SUM is used for compare logic<br>11 = Reserved<br>Note: when ADCPPB2PSUM is selected as the compare source and when a LIMIT match occurs [ADCPB2LIMIT equals ADCPPB2COUNT] the ADCPPB2PSUM register will be cleared and the final sum will be loaded into ADCPPB2SUM. For this sample, the final sum, ADCPPB2SUM will be used for the comparision instead of ADCPPB2PSUM. |
| 13    | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 12    | OSINTSEL   | R/W  | 0h    | Post Processing Block 2 Interrupt Source Select. OSINT2 can be used to trigger an ADC interrupt [ADCINT1 through ADCINT4] via selection in the ADCINT1N2 or ADCINT3N4. This selection determines if a sync. event can trigger OSINT2 in addition to a PCOUNT = LIMIT event.<br>0 = OSINT2 will be generated from PCOUNT = LIMIT only<br>1 = OSTIN2 will be generated form PCOUNT = LIMIT or a sync. event.<br>Note: If a SYNC event would cause an OSINT one cycle after OSINT would have been cause by PCOUNT = LIMIT match, then the second OSINT is ignored.                                                                                                                 |

**Table 3-427. ADC\_CFG\_ADCPPB2CONFIG2 Register Field Descriptions (continued)**

| Bit | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                         |
|-----|------------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11  | SWSYNC     | R/W1TS | 0h    | PPB 2 software force sync. On a sync. event, all partial registers transfer to the final registers and are then reset.<br>Note: In the case where the software force occurs at the same time that a new sample is added to the PSUM and the PSUM is being used for a high or low limit compare, then the comparison will not occur. |
| 10  | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                            |
| 9:4 | SYNCINSEL  | R/W    | 0h    | PPB 2 sync. input select. On a sync. event, all partial registers transfer to the final registers and are then reset.                                                                                                                                                                                                               |
| 3:0 | SHIFT      | R/W    | 0h    | Post Processing Block 2 right shift. Defines the number of bits to right shift PSUM before loading into the final SUM.<br>0 : no right shift<br>1 : SUM = PSUM " 1<br>2 : SUM = PSUM " 2<br>...<br>10 : SUM = PSUM " 10<br>11 -<br>15 : Reserved                                                                                    |

### 3.2.2.142 ADC\_CFG\_ADCPPB2PSUM Register

#### 1 ADC\_CFG\_ADCPPB2PSUM Register (Offset = 180h) [reset = 0h]

ADC PPB2 Partial Sum Register.

Return to [Summary Table](#)

**Table 3-428. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0180h       |
| ADC1_G0_G5    | 502C 1180h       |
| ADC2_G0_G5    | 502C 2180h       |
| ADC3_G0_G5    | 502C 3180h       |
| ADC4_G0_G5    | 502C 4180h       |

**Figure 3-142. ADC\_CFG\_ADCPPB2PSUM Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SIGN |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PSUM |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PSUM |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PSUM |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 3-430. ADC\_CFG\_ADCPPB2PSUM Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 23.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 23:0  | PSUM  | R    | 0h    | Post Processing Block 2 Oversampling Partial Sum. Each time a new result propagates through the PPB signal chain and latches into ADCPPB2RESULT the result is subsequently accumulated into this register.<br>This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event.<br>This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be available 2 SYSCLK cycle after the associated ADCRESULT and subsequent results [in order from lowest numbered PPB to highest] will each become available every 2-3 SYSCLK cycles [refer to the TRM for detailed timing information]. |

### 3.2.2.143 ADC\_CFG\_ADCPPB2PMAX Register

#### 1 ADC\_CFG\_ADCPPB2PMAX Register (Offset = 184h) [reset = 0h]

ADC PPB2 Partial Max Register.

Return to [Summary Table](#)

**Table 3-431. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0184h       |
| ADC1_G0_G5    | 502C 1184h       |
| ADC2_G0_G5    | 502C 2184h       |
| ADC3_G0_G5    | 502C 3184h       |
| ADC4_G0_G5    | 502C 4184h       |

**Figure 3-143. ADC\_CFG\_ADCPPB2PMAX Name Register**

|      |    |    |    |    |    |    |      |
|------|----|----|----|----|----|----|------|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24   |
| SIGN |    |    |    |    |    |    |      |
| R    |    |    |    |    |    |    |      |
| 0h   |    |    |    |    |    |    |      |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16   |
| SIGN |    |    |    |    |    |    | PMAX |
| R    |    |    |    |    |    |    | R    |
| 0h   |    |    |    |    |    |    | 0h   |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8    |
| PMAX |    |    |    |    |    |    |      |
| R    |    |    |    |    |    |    |      |
| 0h   |    |    |    |    |    |    |      |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0    |
| PMAX |    |    |    |    |    |    |      |
| R    |    |    |    |    |    |    |      |
| 0h   |    |    |    |    |    |    |      |

**Table 3-433. ADC\_CFG\_ADCPPB2PMAX Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 16.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 16:0  | PMAX  | R    | 0h    | Post Processing Block 2 Oversampling Partial Max. Each time a new result propagates through the PPB signal chain and latches into ADCPPB2RESULT the result replaces this register if it is larger. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information]. |

### 3.2.2.144 ADC\_CFG\_ADCPPB2PMAXI Register

#### 1 ADC\_CFG\_ADCPPB2PMAXI Register (Offset = 188h) [reset = 0h]

ADC PPB2 Partial Max Index Register.

Return to [Summary Table](#)

**Table 3-434. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0188h       |
| ADC1_G0_G5    | 502C 1188h       |
| ADC2_G0_G5    | 502C 2188h       |
| ADC3_G0_G5    | 502C 3188h       |
| ADC4_G0_G5    | 502C 4188h       |

**Figure 3-144. ADC\_CFG\_ADCPPB2PMAXI Name Register**

|            |    |    |    |    |    |       |   |
|------------|----|----|----|----|----|-------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9     | 8 |
| RESERVED_1 |    |    |    |    |    | PMAXI |   |
| R          |    |    |    |    |    | R     |   |
| 0h         |    |    |    |    |    | 0h    |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1     | 0 |
| PMAXI      |    |    |    |    |    |       |   |
| R          |    |    |    |    |    |       |   |
| 0h         |    |    |    |    |    |       |   |

**Table 3-436. ADC\_CFG\_ADCPPB2PMAXI Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 9:0   | PMAXI      | R    | 0h    | Post Processing Block 2 Oversampling Partial Index of Max. Each time a new result propagates through the PPB signal chain and latches into ADCPPB2RESULT if the result replaces PMAX this register is loaded with the current value of PCOUNT.<br>This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event.<br>This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information]. |



### 3.2.2.145 ADC\_CFG\_ADCPPB2PMIN Register

#### 1 ADC\_CFG\_ADCPPB2PMIN Register (Offset = 18Ch) [reset = 0h]

ADC PPB2 Partial MIN Register.

Return to [Summary Table](#)

**Table 3-437. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 018Ch       |
| ADC1_G0_G5    | 502C 118Ch       |
| ADC2_G0_G5    | 502C 218Ch       |
| ADC3_G0_G5    | 502C 318Ch       |
| ADC4_G0_G5    | 502C 418Ch       |

**Figure 3-145. ADC\_CFG\_ADCPPB2PMIN Name Register**

|      |    |    |    |    |    |    |      |
|------|----|----|----|----|----|----|------|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24   |
| SIGN |    |    |    |    |    |    |      |
| R    |    |    |    |    |    |    |      |
| 0h   |    |    |    |    |    |    |      |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16   |
| SIGN |    |    |    |    |    |    | PMIN |
| R    |    |    |    |    |    |    | R    |
| 0h   |    |    |    |    |    |    | 0h   |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8    |
| PMIN |    |    |    |    |    |    |      |
| R    |    |    |    |    |    |    |      |
| 0h   |    |    |    |    |    |    |      |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0    |
| PMIN |    |    |    |    |    |    |      |
| R    |    |    |    |    |    |    |      |
| 0h   |    |    |    |    |    |    |      |

**Table 3-439. ADC\_CFG\_ADCPPB2PMIN Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 16.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 16:0  | PMIN  | R    | 0h    | Post Processing Block 2 Oversampling Partial Min. Each time a new result propagates through the PPB signal chain and latches into ADCPPB2RESULT the result replaces this register if it is smaller. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information]. |

### 3.2.2.146 ADC\_CFG\_ADCPPB2PMINI Register

#### 1 ADC\_CFG\_ADCPPB2PMINI Register (Offset = 190h) [reset = 0h]

ADC PPB2 Partial Min Index Register.

Return to [Summary Table](#)

**Table 3-440. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0190h       |
| ADC1_G0_G5    | 502C 1190h       |
| ADC2_G0_G5    | 502C 2190h       |
| ADC3_G0_G5    | 502C 3190h       |
| ADC4_G0_G5    | 502C 4190h       |

**Figure 3-146. ADC\_CFG\_ADCPPB2PMINI Name Register**

|            |    |    |    |    |    |       |   |
|------------|----|----|----|----|----|-------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9     | 8 |
| RESERVED_1 |    |    |    |    |    | PMINI |   |
| R          |    |    |    |    |    | R     |   |
| 0h         |    |    |    |    |    | 0h    |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1     | 0 |
| PMINI      |    |    |    |    |    |       |   |
| R          |    |    |    |    |    |       |   |
| 0h         |    |    |    |    |    |       |   |

**Table 3-442. ADC\_CFG\_ADCPPB2PMINI Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 9:0   | PMINI      | R    | 0h    | Post Processing Block 2 Oversampling Partial Index of Min. Each time a new result propagates through the PPB signal chain and latches into ADCPPB2RESULT if the result replaces PMIN this register is loaded with the current value of PCOUNT.<br>This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB2 receives a sync. event.<br>This result is available 1 SYSCLK cycle after the associated ADCPPB2RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB2RESULT timing information]. |

### 3.2.2.147 ADC\_CFG\_ADCPPB2TRIPLO2 Register

#### 1 ADC\_CFG\_ADCPPB2TRIPLO2 Register (Offset = 194h) [reset = 0h]

ADC PPB2 Extended Trip Low Register.

Return to [Summary Table](#)

**Table 3-443. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 0194h       |
| ADC1_G0_G5    | 502C 1194h       |
| ADC2_G0_G5    | 502C 2194h       |
| ADC3_G0_G5    | 502C 3194h       |
| ADC4_G0_G5    | 502C 4194h       |

**Figure 3-147. ADC\_CFG\_ADCPPB2TRIPLO2 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_1 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LIMITLO    |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| LIMITLO    |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LIMITLO    |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 3-445. ADC\_CFG\_ADCPPB2TRIPLO2 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                   |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                      |
| 23:0  | LIMITLO    | R/W  | 0h    | ADC Post Processing Block 2 Trip High Low Limit. This value sets the digital comparator trip low limit if ADCPPB2TRIPLO.LIMITLO2EN = 1.<br>When comparing to an ADCPPBxRESULT register, the upper bits will be ignored:<br>- TRIPLO2[23:17] will be ignored in 16 bit mode<br>- TRIPLO2[23:13] will be ignored in 12 bit mode |

### 3.2.2.148 ADC\_CFG\_ADCPPB3LIMIT Register

#### 1 ADC\_CFG\_ADCPPB3LIMIT Register (Offset = 1A8h) [reset = 0h]

ADC PPB3Conversion Count Limit Register.

Return to [Summary Table](#)

**Table 3-446. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 01A8h       |
| ADC1_G0_G5    | 502C 11A8h       |
| ADC2_G0_G5    | 502C 21A8h       |
| ADC3_G0_G5    | 502C 31A8h       |
| ADC4_G0_G5    | 502C 41A8h       |

**Figure 3-148. ADC\_CFG\_ADCPPB3LIMIT Name Register**

|            |    |    |    |    |    |       |   |
|------------|----|----|----|----|----|-------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9     | 8 |
| RESERVED_1 |    |    |    |    |    | LIMIT |   |
| R          |    |    |    |    |    | R/W   |   |
| 0h         |    |    |    |    |    | 0h    |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1     | 0 |
| LIMIT      |    |    |    |    |    |       |   |
| R/W        |    |    |    |    |    |       |   |
| 0h         |    |    |    |    |    |       |   |

**Table 3-448. ADC\_CFG\_ADCPPB3LIMIT Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                               |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                  |
| 9:0   | LIMIT      | R/W  | 0h    | Post Processing Block 3 Oversampling Limit. Defines the number of conversions to accumulate before PSUM is automatically loaded into SUM. |

### 3.2.2.149 ADC\_CFG\_ADCPPBP3PCOUNT Register

#### 1 ADC\_CFG\_ADCPPBP3PCOUNT Register (Offset = 1ACh) [reset = 0h]

ADC PPB3 Partial Conversion Count Register.

Return to [Summary Table](#)

**Table 3-449. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 01ACh       |
| ADC1_G0_G5    | 502C 11ACh       |
| ADC2_G0_G5    | 502C 21ACh       |
| ADC3_G0_G5    | 502C 31ACh       |
| ADC4_G0_G5    | 502C 41ACh       |

**Figure 3-149. ADC\_CFG\_ADCPPBP3PCOUNT Name Register**

|            |    |    |    |    |    |        |   |
|------------|----|----|----|----|----|--------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9      | 8 |
| RESERVED_1 |    |    |    |    |    | PCOUNT |   |
| R          |    |    |    |    |    | R      |   |
| 0h         |    |    |    |    |    | 0h     |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1      | 0 |
| PCOUNT     |    |    |    |    |    |        |   |
| R          |    |    |    |    |    |        |   |
| 0h         |    |    |    |    |    |        |   |

**Table 3-451. ADC\_CFG\_ADCPPBP3PCOUNT Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 9:0   | PCOUNT     | R    | 0h    | Post Processing Block 3 Oversampling Partial Count. Each time a new result propagates through the PPB signal chain and accumulates into ADCPPB3PSUM this register is incremented by 1. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information]. |

### 3.2.2.150 ADC\_CFG\_ADCPPB3CONFIG2 Register

#### 1 ADC\_CFG\_ADCPPB3CONFIG2 Register (Offset = 1B0h) [reset = 0h]

ADC PPB3 Sum Shift Register.

Return to [Summary Table](#)

**Table 3-452. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 01B0h       |
| ADC1_G0_G5    | 502C 11B0h       |
| ADC2_G0_G5    | 502C 21B0h       |
| ADC3_G0_G5    | 502C 31B0h       |
| ADC4_G0_G5    | 502C 41B0h       |

**Figure 3-150. ADC\_CFG\_ADCPPB3CONFIG2 Name Register**

| 15        | 14         | 13       | 12     | 11         | 10        | 9     | 8 |
|-----------|------------|----------|--------|------------|-----------|-------|---|
| COMPSEL   | RESERVED_2 | OSINTSEL | SWSYNC | RESERVED_1 | SYNCINSEL |       |   |
| R/W       | R          | R/W      | R/W1TS | R          | R/W       |       |   |
| 0h        | 0h         | 0h       | 0h     | 0h         | 0h        |       |   |
| 7         | 6          | 5        | 4      | 3          | 2         | 1     | 0 |
| SYNCINSEL |            |          |        |            |           | SHIFT |   |
| R/W       |            |          |        |            |           | R/W   |   |
| 0h        |            |          |        |            |           | 0h    |   |

**Table 3-454. ADC\_CFG\_ADCPPB3CONFIG2 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | COMPSEL    | R/W  | 0h    | Post Processing Block 3 Compare Source Select. This field determines whether ADCPPB3RESULT, ADCPPB3PSUM, or ADCPPB3SUM is used for the zero-crossing detect logic and threshold compare.<br>00 = ADCPPB3RESULT is used for compare logic<br>01 = ADCPPB3PSUM is used for compare logic<br>10 = ADCPPB3SUM is used for compare logic<br>11 = Reserved<br>Note: when ADCPPB3PSUM is selected as the compare source and when a LIMIT match occurs [ADCPB3LIMIT equals ADCPPB3COUNT] the ADCPPB3PSUM register will be cleared and the final sum will be loaded into ADCPPB3SUM. For this sample, the final sum, ADCPPB3SUM will be used for the comparision instead of ADCPPB3PSUM. |
| 13    | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 12    | OSINTSEL   | R/W  | 0h    | Post Processing Block 3 Interrupt Source Select. OSINT3 can be used to trigger an ADC interrupt [ADCINT1 through ADCINT4] via selection in the ADCINT1N2 or ADCINT3N4. This selection determines if a sync. event can trigger OSINT3 in addition to a PCOUNT = LIMIT event.<br>0 = OSINT3 will be generated from PCOUNT = LIMIT only<br>1 = OSTIN3 will be generated form PCOUNT = LIMIT or a sync. event.<br>Note: If a SYNC event would cause an OSINT one cycle after OSINT would have been cause by PCOUNT = LIMIT match, then the second OSINT is ignored.                                                                                                                 |

**Table 3-454. ADC\_CFG\_ADCPPB3CONFIG2 Register Field Descriptions (continued)**

| Bit | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                         |
|-----|------------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11  | SWSYNC     | R/W1TS | 0h    | PPB 3 software force sync. On a sync. event, all partial registers transfer to the final registers and are then reset.<br>Note: In the case where the software force occurs at the same time that a new sample is added to the PSUM and the PSUM is being used for a high or low limit compare, then the comparison will not occur. |
| 10  | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                            |
| 9:4 | SYNCINSEL  | R/W    | 0h    | PPB 3 sync. input select. On a sync. event, all partial registers transfer to the final registers and are then reset.                                                                                                                                                                                                               |
| 3:0 | SHIFT      | R/W    | 0h    | Post Processing Block 3 right shift. Defines the number of bits to right shift PSUM before loading into the final SUM.<br>0 : no right shift<br>1 : SUM = PSUM " 1<br>2 : SUM = PSUM " 2<br>...<br>10 : SUM = PSUM " 10<br>11 -<br>15 : Reserved                                                                                    |

### 3.2.2.151 ADC\_CFG\_ADCPPB3PSUM Register

#### 1 ADC\_CFG\_ADCPPB3PSUM Register (Offset = 1B4h) [reset = 0h]

ADC PPB3 Partial Sum Register.

Return to [Summary Table](#)

**Table 3-455. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 01B4h       |
| ADC1_G0_G5    | 502C 11B4h       |
| ADC2_G0_G5    | 502C 21B4h       |
| ADC3_G0_G5    | 502C 31B4h       |
| ADC4_G0_G5    | 502C 41B4h       |

**Figure 3-151. ADC\_CFG\_ADCPPB3PSUM Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SIGN |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PSUM |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PSUM |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PSUM |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 3-457. ADC\_CFG\_ADCPPB3PSUM Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 23.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 23:0  | PSUM  | R    | 0h    | Post Processing Block 3 Oversampling Partial Sum. Each time a new result propagates through the PPB signal chain and latches into ADCPPB3RESULT the result is subsequently accumulated into this register.<br>This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event.<br>This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be available 2 SYSCLK cycle after the associated ADCRESULT and subsequent results [in order from lowest numbered PPB to highest] will each become available every 2-3 SYSCLK cycles [refer to the TRM for detailed timing information]. |



### 3.2.2.152 ADC\_CFG\_ADCPPB3PMAX Register

#### 1 ADC\_CFG\_ADCPPB3PMAX Register (Offset = 1B8h) [reset = 0h]

ADC PPB3 Partial Max Register.

Return to [Summary Table](#)

**Table 3-458. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 01B8h       |
| ADC1_G0_G5    | 502C 11B8h       |
| ADC2_G0_G5    | 502C 21B8h       |
| ADC3_G0_G5    | 502C 31B8h       |
| ADC4_G0_G5    | 502C 41B8h       |

**Figure 3-152. ADC\_CFG\_ADCPPB3PMAX Name Register**

|      |    |    |    |    |    |    |      |
|------|----|----|----|----|----|----|------|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24   |
| SIGN |    |    |    |    |    |    |      |
| R    |    |    |    |    |    |    |      |
| 0h   |    |    |    |    |    |    |      |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16   |
| SIGN |    |    |    |    |    |    | PMAX |
| R    |    |    |    |    |    |    | R    |
| 0h   |    |    |    |    |    |    | 0h   |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8    |
| PMAX |    |    |    |    |    |    |      |
| R    |    |    |    |    |    |    |      |
| 0h   |    |    |    |    |    |    |      |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0    |
| PMAX |    |    |    |    |    |    |      |
| R    |    |    |    |    |    |    |      |
| 0h   |    |    |    |    |    |    |      |

**Table 3-460. ADC\_CFG\_ADCPPB3PMAX Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 16.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 16:0  | PMAX  | R    | 0h    | Post Processing Block 3 Oversampling Partial Max. Each time a new result propagates through the PPB signal chain and latches into ADCPPB3RESULT the result replaces this register if it is larger. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information]. |

### 3.2.2.153 ADC\_CFG\_ADCPPB3PMAXI Register

#### 1 ADC\_CFG\_ADCPPB3PMAXI Register (Offset = 1BCh) [reset = 0h]

ADC PPB3 Partial Max Index Register.

Return to [Summary Table](#)

**Table 3-461. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 01BCh       |
| ADC1_G0_G5    | 502C 11BCh       |
| ADC2_G0_G5    | 502C 21BCh       |
| ADC3_G0_G5    | 502C 31BCh       |
| ADC4_G0_G5    | 502C 41BCh       |

**Figure 3-153. ADC\_CFG\_ADCPPB3PMAXI Name Register**

|            |    |    |    |    |    |       |   |
|------------|----|----|----|----|----|-------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9     | 8 |
| RESERVED_1 |    |    |    |    |    | PMAXI |   |
| R          |    |    |    |    |    | R     |   |
| 0h         |    |    |    |    |    | 0h    |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1     | 0 |
| PMAXI      |    |    |    |    |    |       |   |
| R          |    |    |    |    |    |       |   |
| 0h         |    |    |    |    |    |       |   |

**Table 3-463. ADC\_CFG\_ADCPPB3PMAXI Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 9:0   | PMAXI      | R    | 0h    | Post Processing Block 3 Oversampling Partial Index of Max. Each time a new result propagates through the PPB signal chain and latches into ADCPPB3RESULT if the result replaces PMAX this register is loaded with the current value of PCOUNT.<br>This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event.<br>This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information]. |

### 3.2.2.154 ADC\_CFG\_ADCPPB3PMIN Register

#### 1 ADC\_CFG\_ADCPPB3PMIN Register (Offset = 1C0h) [reset = 0h]

ADC PPB3 Partial MIN Register.

Return to [Summary Table](#)

**Table 3-464. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 01C0h       |
| ADC1_G0_G5    | 502C 11C0h       |
| ADC2_G0_G5    | 502C 21C0h       |
| ADC3_G0_G5    | 502C 31C0h       |
| ADC4_G0_G5    | 502C 41C0h       |

**Figure 3-154. ADC\_CFG\_ADCPPB3PMIN Name Register**

|      |    |    |    |    |    |    |      |
|------|----|----|----|----|----|----|------|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24   |
| SIGN |    |    |    |    |    |    |      |
| R    |    |    |    |    |    |    |      |
| 0h   |    |    |    |    |    |    |      |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16   |
| SIGN |    |    |    |    |    |    | PMIN |
| R    |    |    |    |    |    |    | R    |
| 0h   |    |    |    |    |    |    | 0h   |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8    |
| PMIN |    |    |    |    |    |    |      |
| R    |    |    |    |    |    |    |      |
| 0h   |    |    |    |    |    |    |      |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0    |
| PMIN |    |    |    |    |    |    |      |
| R    |    |    |    |    |    |    |      |
| 0h   |    |    |    |    |    |    |      |

**Table 3-466. ADC\_CFG\_ADCPPB3PMIN Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 16.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 16:0  | PMIN  | R    | 0h    | Post Processing Block 3 Oversampling Partial Min. Each time a new result propagates through the PPB signal chain and latches into ADCPPB3RESULT the result replaces this register if it is smaller. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information]. |

### 3.2.2.155 ADC\_CFG\_ADCPPB3PMINI Register

#### 1 ADC\_CFG\_ADCPPB3PMINI Register (Offset = 1C4h) [reset = 0h]

ADC PPB3 Partial Min Index Register.

Return to [Summary Table](#)

**Table 3-467. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 01C4h       |
| ADC1_G0_G5    | 502C 11C4h       |
| ADC2_G0_G5    | 502C 21C4h       |
| ADC3_G0_G5    | 502C 31C4h       |
| ADC4_G0_G5    | 502C 41C4h       |

**Figure 3-155. ADC\_CFG\_ADCPPB3PMINI Name Register**

|            |    |    |    |    |    |       |   |
|------------|----|----|----|----|----|-------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9     | 8 |
| RESERVED_1 |    |    |    |    |    | PMINI |   |
| R          |    |    |    |    |    | R     |   |
| 0h         |    |    |    |    |    | 0h    |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1     | 0 |
| PMINI      |    |    |    |    |    |       |   |
| R          |    |    |    |    |    |       |   |
| 0h         |    |    |    |    |    |       |   |

**Table 3-469. ADC\_CFG\_ADCPPB3PMINI Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 9:0   | PMINI      | R    | 0h    | Post Processing Block 3 Oversampling Partial Index of Min. Each time a new result propagates through the PPB signal chain and latches into ADCPPB3RESULT if the result replaces PMIN this register is loaded with the current value of PCOUNT.<br>This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB3 receives a sync. event.<br>This result is available 1 SYSCLK cycle after the associated ADCPPB3RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB3RESULT timing information]. |

### 3.2.2.156 ADC\_CFG\_ADCPPB3TRIPLO2 Register

#### 1 ADC\_CFG\_ADCPPB3TRIPLO2 Register (Offset = 1C8h) [reset = 0h]

ADC PPB3 Extended Trip Low Register.

Return to [Summary Table](#)

**Table 3-470. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 01C8h       |
| ADC1_G0_G5    | 502C 11C8h       |
| ADC2_G0_G5    | 502C 21C8h       |
| ADC3_G0_G5    | 502C 31C8h       |
| ADC4_G0_G5    | 502C 41C8h       |

**Figure 3-156. ADC\_CFG\_ADCPPB3TRIPLO2 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_1 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LIMITLO    |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| LIMITLO    |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LIMITLO    |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 3-472. ADC\_CFG\_ADCPPB3TRIPLO2 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                   |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                      |
| 23:0  | LIMITLO    | R/W  | 0h    | ADC Post Processing Block 3 Trip High Low Limit. This value sets the digital comparator trip low limit if ADCPPB3TRIPLO.LIMITLO2EN = 1.<br>When comparing to an ADCPPBxRESULT register, the upper bits will be ignored:<br>- TRIPLO2[23:17] will be ignored in 16 bit mode<br>- TRIPLO2[23:13] will be ignored in 12 bit mode |

### 3.2.2.157 ADC\_CFG\_ADCPPB4LIMIT Register

#### 1 ADC\_CFG\_ADCPPB4LIMIT Register (Offset = 1DCh) [reset = 0h]

ADC PPB4Conversion Count Limit Register.

Return to [Summary Table](#)

**Table 3-473. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 01DCh       |
| ADC1_G0_G5    | 502C 11DCh       |
| ADC2_G0_G5    | 502C 21DCh       |
| ADC3_G0_G5    | 502C 31DCh       |
| ADC4_G0_G5    | 502C 41DCh       |

**Figure 3-157. ADC\_CFG\_ADCPPB4LIMIT Name Register**

|            |    |    |    |    |    |       |   |
|------------|----|----|----|----|----|-------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9     | 8 |
| RESERVED_1 |    |    |    |    |    | LIMIT |   |
| R          |    |    |    |    |    | R/W   |   |
| 0h         |    |    |    |    |    | 0h    |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1     | 0 |
| LIMIT      |    |    |    |    |    |       |   |
| R/W        |    |    |    |    |    |       |   |
| 0h         |    |    |    |    |    |       |   |

**Table 3-475. ADC\_CFG\_ADCPPB4LIMIT Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                               |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                  |
| 9:0   | LIMIT      | R/W  | 0h    | Post Processing Block 4 Oversampling Limit. Defines the number of conversions to accumulate before PSUM is automatically loaded into SUM. |

### 3.2.2.158 ADC\_CFG\_ADCPPBP4PCOUNT Register

#### 1 ADC\_CFG\_ADCPPBP4PCOUNT Register (Offset = 1E0h) [reset = 0h]

ADC PPB4 Partial Conversion Count Register.

Return to [Summary Table](#)

**Table 3-476. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 01E0h       |
| ADC1_G0_G5    | 502C 11E0h       |
| ADC2_G0_G5    | 502C 21E0h       |
| ADC3_G0_G5    | 502C 31E0h       |
| ADC4_G0_G5    | 502C 41E0h       |

**Figure 3-158. ADC\_CFG\_ADCPPBP4PCOUNT Name Register**

|            |    |    |    |    |    |        |   |
|------------|----|----|----|----|----|--------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9      | 8 |
| RESERVED_1 |    |    |    |    |    | PCOUNT |   |
| R          |    |    |    |    |    | R      |   |
| 0h         |    |    |    |    |    | 0h     |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1      | 0 |
| PCOUNT     |    |    |    |    |    |        |   |
| R          |    |    |    |    |    |        |   |
| 0h         |    |    |    |    |    |        |   |

**Table 3-478. ADC\_CFG\_ADCPPBP4PCOUNT Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 9:0   | PCOUNT     | R    | 0h    | Post Processing Block 4 Oversampling Partial Count. Each time a new result propagates through the PPB signal chain and accumulates into ADCPPB4PSUM this register is incremented by 1. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information]. |

### 3.2.2.159 ADC\_CFG\_ADCPPB4CONFIG2 Register

#### 1 ADC\_CFG\_ADCPPB4CONFIG2 Register (Offset = 1E4h) [reset = 0h]

ADC PPB4 Sum Shift Register.

Return to [Summary Table](#)

**Table 3-479. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 01E4h       |
| ADC1_G0_G5    | 502C 11E4h       |
| ADC2_G0_G5    | 502C 21E4h       |
| ADC3_G0_G5    | 502C 31E4h       |
| ADC4_G0_G5    | 502C 41E4h       |

**Figure 3-159. ADC\_CFG\_ADCPPB4CONFIG2 Name Register**

| 15        | 14 | 13         | 12       | 11     | 10         | 9         | 8 |
|-----------|----|------------|----------|--------|------------|-----------|---|
| COMPSEL   |    | RESERVED_2 | OSINTSEL | SWSYNC | RESERVED_1 | SYNCINSEL |   |
| R/W       |    | R          | R/W      | R/W1TS | R          | R/W       |   |
| 0h        |    | 0h         | 0h       | 0h     | 0h         | 0h        |   |
| 7         | 6  | 5          | 4        | 3      | 2          | 1         | 0 |
| SYNCINSEL |    |            |          | SHIFT  |            |           |   |
| R/W       |    |            |          | R/W    |            |           |   |
| 0h        |    |            |          | 0h     |            |           |   |

**Table 3-481. ADC\_CFG\_ADCPPB4CONFIG2 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | COMPSEL    | R/W  | 0h    | Post Processing Block 4 Compare Source Select. This field determines whether ADCPPB4RESULT, ADCPPB4PSUM, or ADCPPB4SUM is used for the zero-crossing detect logic and threshold compare.<br>00 = ADCPPB4RESULT is used for compare logic<br>01 = ADCPPB4PSUM is used for compare logic<br>10 = ADCPPB4SUM is used for compare logic<br>11 = Reserved<br>Note: when ADCPPB4PSUM is selected as the compare source and when a LIMIT match occurs [ADCPB4LIMIT equals ADCPPB4COUNT] the ADCPPB4PSUM register will be cleared and the final sum will be loaded into ADCPPB4SUM. For this sample, the final sum, ADCPPB4SUM will be used for the comparision instead of ADCPPB4PSUM. |
| 13    | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 12    | OSINTSEL   | R/W  | 0h    | Post Processing Block 4 Interrupt Source Select. OSINT4 can be used to trigger an ADC interrupt [ADCINT1 through ADCINT4] via selection in the ADCINT1N2 or ADCINT3N4. This selection determines if a sync. event can trigger OSINT4 in addition to a PCOUNT = LIMIT event.<br>0 = OSINT4 will be generated from PCOUNT = LIMIT only<br>1 = OSTIN4 will be generated form PCOUNT = LIMIT or a sync. event.<br>Note: If a SYNC event would cause an OSINT one cycle after OSINT would have been cause by PCOUNT = LIMIT match, then the second OSINT is ignored.                                                                                                                 |



**Table 3-481. ADC\_CFG\_ADCPPB4CONFIG2 Register Field Descriptions (continued)**

| Bit | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                         |
|-----|------------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11  | SWSYNC     | R/W1TS | 0h    | PPB 4 software force sync. On a sync. event, all partial registers transfer to the final registers and are then reset.<br>Note: In the case where the software force occurs at the same time that a new sample is added to the PSUM and the PSUM is being used for a high or low limit compare, then the comparison will not occur. |
| 10  | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                            |
| 9:4 | SYNCINSEL  | R/W    | 0h    | PPB 4 sync. input select. On a sync. event, all partial registers transfer to the final registers and are then reset.                                                                                                                                                                                                               |
| 3:0 | SHIFT      | R/W    | 0h    | Post Processing Block 4 right shift. Defines the number of bits to right shift PSUM before loading into the final SUM.<br>0 : no right shift<br>1 : SUM = PSUM " 1<br>2 : SUM = PSUM " 2<br>...<br>10 : SUM = PSUM " 10<br>11 -<br>15 : Reserved                                                                                    |

### 3.2.2.160 ADC\_CFG\_ADCPPB4PSUM Register

#### 1 ADC\_CFG\_ADCPPB4PSUM Register (Offset = 1E8h) [reset = 0h]

ADC PPB4 Partial Sum Register.

Return to [Summary Table](#)

**Table 3-482. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 01E8h       |
| ADC1_G0_G5    | 502C 11E8h       |
| ADC2_G0_G5    | 502C 21E8h       |
| ADC3_G0_G5    | 502C 31E8h       |
| ADC4_G0_G5    | 502C 41E8h       |

**Figure 3-160. ADC\_CFG\_ADCPPB4PSUM Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SIGN |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PSUM |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PSUM |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PSUM |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 3-484. ADC\_CFG\_ADCPPB4PSUM Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 23.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 23:0  | PSUM  | R    | 0h    | Post Processing Block 4 Oversampling Partial Sum. Each time a new result propagates through the PPB signal chain and latches into ADCPPB4RESULT the result is subsequently accumulated into this register.<br>This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event.<br>This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC. In the case of multiple PPBs associated with the same SOC, the lowest numbered PPB's result will be available 2 SYSCLK cycle after the associated ADCRESULT and subsequent results [in order from lowest numbered PPB to highest] will each become available every 2-3 SYSCLK cycles [refer to the TRM for detailed timing information]. |

### 3.2.2.161 ADC\_CFG\_ADCPPB4PMAX Register

#### 1 ADC\_CFG\_ADCPPB4PMAX Register (Offset = 1ECh) [reset = 0h]

ADC PPB4 Partial Max Register.

Return to [Summary Table](#)

**Table 3-485. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 01ECh       |
| ADC1_G0_G5    | 502C 11ECh       |
| ADC2_G0_G5    | 502C 21ECh       |
| ADC3_G0_G5    | 502C 31ECh       |
| ADC4_G0_G5    | 502C 41ECh       |

**Figure 3-161. ADC\_CFG\_ADCPPB4PMAX Name Register**

|      |    |    |    |    |    |    |      |
|------|----|----|----|----|----|----|------|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24   |
| SIGN |    |    |    |    |    |    |      |
| R    |    |    |    |    |    |    |      |
| 0h   |    |    |    |    |    |    |      |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16   |
| SIGN |    |    |    |    |    |    | PMAX |
| R    |    |    |    |    |    |    | R    |
| 0h   |    |    |    |    |    |    | 0h   |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8    |
| PMAX |    |    |    |    |    |    |      |
| R    |    |    |    |    |    |    |      |
| 0h   |    |    |    |    |    |    |      |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0    |
| PMAX |    |    |    |    |    |    |      |
| R    |    |    |    |    |    |    |      |
| 0h   |    |    |    |    |    |    |      |

**Table 3-487. ADC\_CFG\_ADCPPB4PMAX Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 16.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 16:0  | PMAX  | R    | 0h    | Post Processing Block 4 Oversampling Partial Max. Each time a new result propagates through the PPB signal chain and latches into ADCPPB4RESULT the result replaces this register if it is larger. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information]. |

### 3.2.2.162 ADC\_CFG\_ADCPPB4PMAXI Register

#### 1 ADC\_CFG\_ADCPPB4PMAXI Register (Offset = 1F0h) [reset = 0h]

ADC PPB4 Partial Max Index Register.

Return to [Summary Table](#)

**Table 3-488. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 01F0h       |
| ADC1_G0_G5    | 502C 11F0h       |
| ADC2_G0_G5    | 502C 21F0h       |
| ADC3_G0_G5    | 502C 31F0h       |
| ADC4_G0_G5    | 502C 41F0h       |

**Figure 3-162. ADC\_CFG\_ADCPPB4PMAXI Name Register**

|            |    |    |    |    |    |       |   |
|------------|----|----|----|----|----|-------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9     | 8 |
| RESERVED_1 |    |    |    |    |    | PMAXI |   |
| R          |    |    |    |    |    | R     |   |
| 0h         |    |    |    |    |    | 0h    |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1     | 0 |
| PMAXI      |    |    |    |    |    |       |   |
| R          |    |    |    |    |    |       |   |
| 0h         |    |    |    |    |    |       |   |

**Table 3-490. ADC\_CFG\_ADCPPB4PMAXI Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 9:0   | PMAXI      | R    | 0h    | Post Processing Block 4 Oversampling Partial Index of Max. Each time a new result propagates through the PPB signal chain and latches into ADCPPB4RESULT if the result replaces PMAX this register is loaded with the current value of PCOUNT.<br>This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event.<br>This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information]. |

### 3.2.2.163 ADC\_CFG\_ADCPPB4PMIN Register

#### 1 ADC\_CFG\_ADCPPB4PMIN Register (Offset = 1F4h) [reset = 0h]

ADC PPB4 Partial MIN Register.

Return to [Summary Table](#)

**Table 3-491. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 01F4h       |
| ADC1_G0_G5    | 502C 11F4h       |
| ADC2_G0_G5    | 502C 21F4h       |
| ADC3_G0_G5    | 502C 31F4h       |
| ADC4_G0_G5    | 502C 41F4h       |

**Figure 3-163. ADC\_CFG\_ADCPPB4PMIN Name Register**

|      |    |    |    |    |    |    |      |
|------|----|----|----|----|----|----|------|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24   |
| SIGN |    |    |    |    |    |    |      |
| R    |    |    |    |    |    |    |      |
| 0h   |    |    |    |    |    |    |      |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16   |
| SIGN |    |    |    |    |    |    | PMIN |
| R    |    |    |    |    |    |    | R    |
| 0h   |    |    |    |    |    |    | 0h   |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8    |
| PMIN |    |    |    |    |    |    |      |
| R    |    |    |    |    |    |    |      |
| 0h   |    |    |    |    |    |    |      |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0    |
| PMIN |    |    |    |    |    |    |      |
| R    |    |    |    |    |    |    |      |
| 0h   |    |    |    |    |    |    |      |

**Table 3-493. ADC\_CFG\_ADCPPB4PMIN Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | SIGN  | R    | 0h    | Sign Extended Bits. These bits reflect the same value as bit 16.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 16:0  | PMIN  | R    | 0h    | Post Processing Block 4 Oversampling Partial Min. Each time a new result propagates through the PPB signal chain and latches into ADCPPB4RESULT the result replaces this register if it is smaller. This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event. This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information]. |

### 3.2.2.164 ADC\_CFG\_ADCPPB4PMINI Register

#### 1 ADC\_CFG\_ADCPPB4PMINI Register (Offset = 1F8h) [reset = 0h]

ADC PPB4 Partial Min Index Register.

Return to [Summary Table](#)

**Table 3-494. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 01F8h       |
| ADC1_G0_G5    | 502C 11F8h       |
| ADC2_G0_G5    | 502C 21F8h       |
| ADC3_G0_G5    | 502C 31F8h       |
| ADC4_G0_G5    | 502C 41F8h       |

**Figure 3-164. ADC\_CFG\_ADCPPB4PMINI Name Register**

|            |    |    |    |    |    |       |   |
|------------|----|----|----|----|----|-------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9     | 8 |
| RESERVED_1 |    |    |    |    |    | PMINI |   |
| R          |    |    |    |    |    | R     |   |
| 0h         |    |    |    |    |    | 0h    |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1     | 0 |
| PMINI      |    |    |    |    |    |       |   |
| R          |    |    |    |    |    |       |   |
| 0h         |    |    |    |    |    |       |   |

**Table 3-496. ADC\_CFG\_ADCPPB4PMINI Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 9:0   | PMINI      | R    | 0h    | Post Processing Block 4 Oversampling Partial Index of Min. Each time a new result propagates through the PPB signal chain and latches into ADCPPB4RESULT if the result replaces PMIN this register is loaded with the current value of PCOUNT.<br>This register is reset when either a count-match event occurs [PCOUNT = LIMIT] or PPB4 receives a sync. event.<br>This result is available 1 SYSCLK cycle after the associated ADCPPB4RESULT is available. This will be 2 SYSCLK cycles after the associated ADCRESULT is available, unless multiple PPBs point to the same SOC [refer to the ADCPPB4RESULT timing information]. |

### 3.2.2.165 ADC\_CFG\_ADCPPB4TRIPLO2 Register

#### 1 ADC\_CFG\_ADCPPB4TRIPLO2 Register (Offset = 1FCh) [reset = 0h]

ADC PPB4 Extended Trip Low Register.

Return to [Summary Table](#)

**Table 3-497. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ADC0_G0_G5    | 502C 01FCh       |
| ADC1_G0_G5    | 502C 11FCh       |
| ADC2_G0_G5    | 502C 21FCh       |
| ADC3_G0_G5    | 502C 31FCh       |
| ADC4_G0_G5    | 502C 41FCh       |

**Figure 3-165. ADC\_CFG\_ADCPPB4TRIPLO2 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_1 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LIMITLO    |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| LIMITLO    |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LIMITLO    |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 3-499. ADC\_CFG\_ADCPPB4TRIPLO2 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                   |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                      |
| 23:0  | LIMITLO    | R/W  | 0h    | ADC Post Processing Block 4 Trip High Low Limit. This value sets the digital comparator trip low limit if ADCPPB4TRIPLO.LIMITLO2EN = 1.<br>When comparing to an ADCPPBxRESULT register, the upper bits will be ignored:<br>- TRIPLO2[23:17] will be ignored in 16 bit mode<br>- TRIPLO2[23:13] will be ignored in 12 bit mode |

### 3.3 CMPSSA

#### CMPSSA

##### 3.3.1 CMPSSA Summaries

#### CMPSSA Summaries

**Table 3-500. CMPSSA Registers, Base Address=5020 0000h, Length=4096**

| Offset | Length | Register Name                          | CMPSSA0 Physical Address | CMPSSA1 Physical Address | CMPSSA2 Physical Address |
|--------|--------|----------------------------------------|--------------------------|--------------------------|--------------------------|
| 0h     | 16     | <a href="#">CMPSSA_COMPCTL</a>         | 5020 0000h               | 5020 1000h               | 5020 2000h               |
| 4h     | 16     | <a href="#">CMPSSA_COMPSTS</a>         | 5020 0004h               | 5020 1004h               | 5020 2004h               |
| 6h     | 16     | <a href="#">CMPSSA_COMPSTSCLR</a>      | 5020 0006h               | 5020 1006h               | 5020 2006h               |
| 8h     | 16     | <a href="#">CMPSSA_COMPDACCTL</a>      | 5020 0008h               | 5020 1008h               | 5020 2008h               |
| Ah     | 16     | <a href="#">CMPSSA_COMPDACCTL2</a>     | 5020 000Ah               | 5020 100Ah               | 5020 200Ah               |
| Ch     | 16     | <a href="#">CMPSSA_DACHVALS</a>        | 5020 000Ch               | 5020 100Ch               | 5020 200Ch               |
| Eh     | 16     | <a href="#">CMPSSA_DACHVALA</a>        | 5020 000Eh               | 5020 100Eh               | 5020 200Eh               |
| 10h    | 16     | <a href="#">CMPSSA_RAMPMAXREFA</a>     | 5020 0010h               | 5020 1010h               | 5020 2010h               |
| 14h    | 16     | <a href="#">CMPSSA_RAMPMAXREFS</a>     | 5020 0014h               | 5020 1014h               | 5020 2014h               |
| 18h    | 16     | <a href="#">CMPSSA_RAMPDECVALA</a>     | 5020 0018h               | 5020 1018h               | 5020 2018h               |
| 1Ch    | 16     | <a href="#">CMPSSA_RAMPDECVALS</a>     | 5020 001Ch               | 5020 101Ch               | 5020 201Ch               |
| 20h    | 16     | <a href="#">CMPSSA_RAMPSTS</a>         | 5020 0020h               | 5020 1020h               | 5020 2020h               |
| 24h    | 16     | <a href="#">CMPSSA_DACLVALS</a>        | 5020 0024h               | 5020 1024h               | 5020 2024h               |
| 26h    | 16     | <a href="#">CMPSSA_DACLVALA</a>        | 5020 0026h               | 5020 1026h               | 5020 2026h               |
| 28h    | 16     | <a href="#">CMPSSA_RAMPDLYA</a>        | 5020 0028h               | 5020 1028h               | 5020 2028h               |
| 2Ah    | 16     | <a href="#">CMPSSA_RAMPDLYS</a>        | 5020 002Ah               | 5020 102Ah               | 5020 202Ah               |
| 2Ch    | 16     | <a href="#">CMPSSA_CTRIPFILCTL</a>     | 5020 002Ch               | 5020 102Ch               | 5020 202Ch               |
| 2Eh    | 16     | <a href="#">CMPSSA_CTRIPFILCLKCTL</a>  | 5020 002Eh               | 5020 102Eh               | 5020 202Eh               |
| 30h    | 16     | <a href="#">CMPSSA_CTRIPHFILCTL</a>    | 5020 0030h               | 5020 1030h               | 5020 2030h               |
| 32h    | 16     | <a href="#">CMPSSA_CTRIPHFILCLKCTL</a> | 5020 0032h               | 5020 1032h               | 5020 2032h               |
| 34h    | 16     | <a href="#">CMPSSA_COMPLOCK</a>        | 5020 0034h               | 5020 1034h               | 5020 2034h               |
| 38h    | 16     | <a href="#">CMPSSA_DACHVALS2</a>       | 5020 0038h               | 5020 1038h               | 5020 2038h               |
| 3Ah    | 16     | <a href="#">CMPSSA_DACLVALS2</a>       | 5020 003Ah               | 5020 103Ah               | 5020 203Ah               |
| 3Ch    | 16     | <a href="#">CMPSSA_CONFIG1</a>         | 5020 003Ch               | 5020 103Ch               | 5020 203Ch               |

**Table 3-501. CMPSSA Registers, Base Address=5020 0000h, Length=4096**

| Offset | Length | Register Name                      | CMPSSA3 Physical Address | CMPSSA4 Physical Address | CMPSSA5 Physical Address |
|--------|--------|------------------------------------|--------------------------|--------------------------|--------------------------|
| 0h     | 16     | <a href="#">CMPSSA_COMPCTL</a>     | 5020 3000h               | 5020 4000h               | 5020 5000h               |
| 4h     | 16     | <a href="#">CMPSSA_COMPSTS</a>     | 5020 3004h               | 5020 4004h               | 5020 5004h               |
| 6h     | 16     | <a href="#">CMPSSA_COMPSTSCLR</a>  | 5020 3006h               | 5020 4006h               | 5020 5006h               |
| 8h     | 16     | <a href="#">CMPSSA_COMPDACCTL</a>  | 5020 3008h               | 5020 4008h               | 5020 5008h               |
| Ah     | 16     | <a href="#">CMPSSA_COMPDACCTL2</a> | 5020 300Ah               | 5020 400Ah               | 5020 500Ah               |
| Ch     | 16     | <a href="#">CMPSSA_DACHVALS</a>    | 5020 300Ch               | 5020 400Ch               | 5020 500Ch               |
| Eh     | 16     | <a href="#">CMPSSA_DACHVALA</a>    | 5020 300Eh               | 5020 400Eh               | 5020 500Eh               |
| 10h    | 16     | <a href="#">CMPSSA_RAMPMAXREFA</a> | 5020 3010h               | 5020 4010h               | 5020 5010h               |
| 14h    | 16     | <a href="#">CMPSSA_RAMPMAXREFS</a> | 5020 3014h               | 5020 4014h               | 5020 5014h               |



**Table 3-501. CMPSSA Registers, Base Address=5020 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                          | CMPSSA3 Physical Address | CMPSSA4 Physical Address | CMPSSA5 Physical Address |
|--------|--------|----------------------------------------|--------------------------|--------------------------|--------------------------|
| 18h    | 16     | <a href="#">CMPSSA_RAMPDECVALA</a>     | 5020 3018h               | 5020 4018h               | 5020 5018h               |
| 1Ch    | 16     | <a href="#">CMPSSA_RAMPDECVALS</a>     | 5020 301Ch               | 5020 401Ch               | 5020 501Ch               |
| 20h    | 16     | <a href="#">CMPSSA_RAMPSTS</a>         | 5020 3020h               | 5020 4020h               | 5020 5020h               |
| 24h    | 16     | <a href="#">CMPSSA_DACLVALS</a>        | 5020 3024h               | 5020 4024h               | 5020 5024h               |
| 26h    | 16     | <a href="#">CMPSSA_DACLVALA</a>        | 5020 3026h               | 5020 4026h               | 5020 5026h               |
| 28h    | 16     | <a href="#">CMPSSA_RAMPDLYA</a>        | 5020 3028h               | 5020 4028h               | 5020 5028h               |
| 2Ah    | 16     | <a href="#">CMPSSA_RAMPDLYS</a>        | 5020 302Ah               | 5020 402Ah               | 5020 502Ah               |
| 2Ch    | 16     | <a href="#">CMPSSA_CTRIPLFILCTL</a>    | 5020 302Ch               | 5020 402Ch               | 5020 502Ch               |
| 2Eh    | 16     | <a href="#">CMPSSA_CTRIPLFILCLKCTL</a> | 5020 302Eh               | 5020 402Eh               | 5020 502Eh               |
| 30h    | 16     | <a href="#">CMPSSA_CTRIPHFILCTL</a>    | 5020 3030h               | 5020 4030h               | 5020 5030h               |
| 32h    | 16     | <a href="#">CMPSSA_CTRIPHFILCLKCTL</a> | 5020 3032h               | 5020 4032h               | 5020 5032h               |
| 34h    | 16     | <a href="#">CMPSSA_COMPLOCK</a>        | 5020 3034h               | 5020 4034h               | 5020 5034h               |
| 38h    | 16     | <a href="#">CMPSSA_DACHVALS2</a>       | 5020 3038h               | 5020 4038h               | 5020 5038h               |
| 3Ah    | 16     | <a href="#">CMPSSA_DACLVALS2</a>       | 5020 303Ah               | 5020 403Ah               | 5020 503Ah               |
| 3Ch    | 16     | <a href="#">CMPSSA_CONFIG1</a>         | 5020 303Ch               | 5020 403Ch               | 5020 503Ch               |

**Table 3-502. CMPSSA Registers, Base Address=5020 0000h, Length=4096**

| Offset | Length | Register Name                          | CMPSSA6 Physical Address | CMPSSA7 Physical Address | CMPSSA8 Physical Address |
|--------|--------|----------------------------------------|--------------------------|--------------------------|--------------------------|
| 0h     | 16     | <a href="#">CMPSSA_COMPCTL</a>         | 5020 6000h               | 5020 7000h               | 5020 8000h               |
| 4h     | 16     | <a href="#">CMPSSA_COMPSTS</a>         | 5020 6004h               | 5020 7004h               | 5020 8004h               |
| 6h     | 16     | <a href="#">CMPSSA_COMPSTSCLR</a>      | 5020 6006h               | 5020 7006h               | 5020 8006h               |
| 8h     | 16     | <a href="#">CMPSSA_COMPDACCTL</a>      | 5020 6008h               | 5020 7008h               | 5020 8008h               |
| Ah     | 16     | <a href="#">CMPSSA_COMPDACCTL2</a>     | 5020 600Ah               | 5020 700Ah               | 5020 800Ah               |
| Ch     | 16     | <a href="#">CMPSSA_DACHVALS</a>        | 5020 600Ch               | 5020 700Ch               | 5020 800Ch               |
| Eh     | 16     | <a href="#">CMPSSA_DACHVALA</a>        | 5020 600Eh               | 5020 700Eh               | 5020 800Eh               |
| 10h    | 16     | <a href="#">CMPSSA_RAMPMAXREFA</a>     | 5020 6010h               | 5020 7010h               | 5020 8010h               |
| 14h    | 16     | <a href="#">CMPSSA_RAMPMAXREFS</a>     | 5020 6014h               | 5020 7014h               | 5020 8014h               |
| 18h    | 16     | <a href="#">CMPSSA_RAMPDECVALA</a>     | 5020 6018h               | 5020 7018h               | 5020 8018h               |
| 1Ch    | 16     | <a href="#">CMPSSA_RAMPDECVALS</a>     | 5020 601Ch               | 5020 701Ch               | 5020 801Ch               |
| 20h    | 16     | <a href="#">CMPSSA_RAMPSTS</a>         | 5020 6020h               | 5020 7020h               | 5020 8020h               |
| 24h    | 16     | <a href="#">CMPSSA_DACLVALS</a>        | 5020 6024h               | 5020 7024h               | 5020 8024h               |
| 26h    | 16     | <a href="#">CMPSSA_DACLVALA</a>        | 5020 6026h               | 5020 7026h               | 5020 8026h               |
| 28h    | 16     | <a href="#">CMPSSA_RAMPDLYA</a>        | 5020 6028h               | 5020 7028h               | 5020 8028h               |
| 2Ah    | 16     | <a href="#">CMPSSA_RAMPDLYS</a>        | 5020 602Ah               | 5020 702Ah               | 5020 802Ah               |
| 2Ch    | 16     | <a href="#">CMPSSA_CTRIPLFILCTL</a>    | 5020 602Ch               | 5020 702Ch               | 5020 802Ch               |
| 2Eh    | 16     | <a href="#">CMPSSA_CTRIPLFILCLKCTL</a> | 5020 602Eh               | 5020 702Eh               | 5020 802Eh               |
| 30h    | 16     | <a href="#">CMPSSA_CTRIPHFILCTL</a>    | 5020 6030h               | 5020 7030h               | 5020 8030h               |
| 32h    | 16     | <a href="#">CMPSSA_CTRIPHFILCLKCTL</a> | 5020 6032h               | 5020 7032h               | 5020 8032h               |
| 34h    | 16     | <a href="#">CMPSSA_COMPLOCK</a>        | 5020 6034h               | 5020 7034h               | 5020 8034h               |
| 38h    | 16     | <a href="#">CMPSSA_DACHVALS2</a>       | 5020 6038h               | 5020 7038h               | 5020 8038h               |
| 3Ah    | 16     | <a href="#">CMPSSA_DACLVALS2</a>       | 5020 603Ah               | 5020 703Ah               | 5020 803Ah               |
| 3Ch    | 16     | <a href="#">CMPSSA_CONFIG1</a>         | 5020 603Ch               | 5020 703Ch               | 5020 803Ch               |

**Table 3-503. CMPSSA Registers, Base Address=5020 0000h, Length=4096**

| Offset | Length | Register Name                          | CMPSSA9 Physical Address |
|--------|--------|----------------------------------------|--------------------------|
| 0h     | 16     | <a href="#">CMPSSA_COMPCTL</a>         | 5020 9000h               |
| 4h     | 16     | <a href="#">CMPSSA_COMPSTS</a>         | 5020 9004h               |
| 6h     | 16     | <a href="#">CMPSSA_COMPSTSCCLR</a>     | 5020 9006h               |
| 8h     | 16     | <a href="#">CMPSSA_COMPDACCTL</a>      | 5020 9008h               |
| Ah     | 16     | <a href="#">CMPSSA_COMPDACCTL2</a>     | 5020 900Ah               |
| Ch     | 16     | <a href="#">CMPSSA_DACHVALS</a>        | 5020 900Ch               |
| Eh     | 16     | <a href="#">CMPSSA_DACHVALA</a>        | 5020 900Eh               |
| 10h    | 16     | <a href="#">CMPSSA_RAMPMAXREFA</a>     | 5020 9010h               |
| 14h    | 16     | <a href="#">CMPSSA_RAMPMAXREFS</a>     | 5020 9014h               |
| 18h    | 16     | <a href="#">CMPSSA_RAMPDECVALA</a>     | 5020 9018h               |
| 1Ch    | 16     | <a href="#">CMPSSA_RAMPDECVALS</a>     | 5020 901Ch               |
| 20h    | 16     | <a href="#">CMPSSA_RAMPSTS</a>         | 5020 9020h               |
| 24h    | 16     | <a href="#">CMPSSA_DACLVALS</a>        | 5020 9024h               |
| 26h    | 16     | <a href="#">CMPSSA_DACLVALA</a>        | 5020 9026h               |
| 28h    | 16     | <a href="#">CMPSSA_RAMPDLYA</a>        | 5020 9028h               |
| 2Ah    | 16     | <a href="#">CMPSSA_RAMPDLYS</a>        | 5020 902Ah               |
| 2Ch    | 16     | <a href="#">CMPSSA_CTRIPLFILCTL</a>    | 5020 902Ch               |
| 2Eh    | 16     | <a href="#">CMPSSA_CTRIPLFILCLKCTL</a> | 5020 902Eh               |
| 30h    | 16     | <a href="#">CMPSSA_CTRIPHFILCTL</a>    | 5020 9030h               |
| 32h    | 16     | <a href="#">CMPSSA_CTRIPHFILCLKCTL</a> | 5020 9032h               |
| 34h    | 16     | <a href="#">CMPSSA_COMPLOCK</a>        | 5020 9034h               |
| 38h    | 16     | <a href="#">CMPSSA_DACHVALS2</a>       | 5020 9038h               |
| 3Ah    | 16     | <a href="#">CMPSSA_DACLVALS2</a>       | 5020 903Ah               |
| 3Ch    | 16     | <a href="#">CMPSSA_CONFIG1</a>         | 5020 903Ch               |

### 3.3.2 CMPSSA Registers

#### CMPSSA Registers

### 3.3.2.1 CMPSSA\_COMPCTL Register

#### 1 CMPSSA\_COMPCTL Register (Offset = 0h) [reset = 0h]

CMPSS Comparator Control Register.

Return to [Summary Table](#)

**Table 3-504. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSA0       | 5020 0000h       |
| CMPSSA1       | 5020 1000h       |
| CMPSSA2       | 5020 2000h       |
| CMPSSA3       | 5020 3000h       |
| CMPSSA4       | 5020 4000h       |
| CMPSSA5       | 5020 5000h       |
| CMPSSA6       | 5020 6000h       |
| CMPSSA7       | 5020 7000h       |
| CMPSSA8       | 5020 8000h       |
| CMPSSA9       | 5020 9000h       |

**Figure 3-166. CMPSSA\_COMPCTL Name Register**

| 15         | 14      | 13           | 12        | 11       | 10              | 9   | 8   |
|------------|---------|--------------|-----------|----------|-----------------|-----|-----|
| COMPDAE    | ASYNCLN | CTRIPOUTLSEL | CTRIPLSEL | COMPLINV | COMPLSOURC<br>E |     |     |
| R/W        | R/W     | R/W          | R/W       | R/W      | R/W             | R/W | R/W |
| 0h         | 0h      | 0h           | 0h        | 0h       | 0h              | 0h  | 0h  |
| 7          | 6       | 5            | 4         | 3        | 2               | 1   | 0   |
| RESERVED_1 | ASYNCHN | CTRIPOUTHSEL | CTRIPHSEL | COMPHINV | COMPHSOUR<br>CE |     |     |
| R          | R/W     | R/W          | R/W       | R/W      | R/W             | R/W | R/W |
| 0h         | 0h      | 0h           | 0h        | 0h       | 0h              | 0h  | 0h  |

**Table 3-506. CMPSSA\_COMPCTL Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | COMPDAE      | R/W  | 0h    | Comparator/DAC enable.<br>0 Comparator/DAC disabled<br>1 Comparator/DAC enabled                                                                                                                                                                                                                                                                                        |
| 14    | ASYNCLN      | R/W  | 0h    | Low comparator asynchronous path enable. Allows asynchronous comparator output to feed into OR gate with latched digital filter signal when CTRIPLSEL=3 or CTRIPOUTLSEL=3.<br>0 Asynchronous comparator output does not feed into OR gate with latched digital filter output<br>1 Asynchronous comparator output feeds into OR gate with latched digital filter output |
| 13:12 | CTRIPOUTLSEL | R/W  | 0h    | Low comparator CTRIPOUTL source select.<br>0 Asynchronous comparator output drives CTRIPOUTL<br>1 Synchronous comparator output drives CTRIPOUTL<br>2 Output of digital filter drives CTRIPOUTL<br>3 Latched output of digital filter drives CTRIPOUTL                                                                                                                 |
| 11:10 | CTRIPLSEL    | R/W  | 0h    | Low comparator CTRIPL source select.<br>0 Asynchronous comparator output drives CTRIPL<br>1 Synchronous comparator output drives CTRIPL<br>2 Output of digital filter drives CTRIPL<br>3 Latched output of digital filter drives CTRIPL                                                                                                                                |

**Table 3-506. CMPSSA\_COMPCTL Register Field Descriptions (continued)**

| Bit | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                             |
|-----|--------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9   | COMPLINV     | R/W  | 0h    | Low comparator output invert.<br>0 Output of comparator is not inverted<br>1 Output of comparator is inverted                                                                                                                                                                                                                                                           |
| 8   | COMPLSOURCE  | R/W  | 0h    | CompL Pos Mux Select<br>0 positive mux selects INL_3p3v voltage [default]<br>1 positive mux selects INH_3p3v                                                                                                                                                                                                                                                            |
| 7   | RESERVED_1   | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                |
| 6   | ASYNCHEN     | R/W  | 0h    | High comparator asynchronous path enable. Allows asynchronous comparator output to feed into OR gate with latched digital filter signal when CTRIPHSEL=3 or CTRIPOUTHSEL=3.<br>0 Asynchronous comparator output does not feed into OR gate with latched digital filter output<br>1 Asynchronous comparator output feeds into OR gate with latched digital filter output |
| 5:4 | CTRIPOUTHSEL | R/W  | 0h    | High comparator CTRIPOUTH source select.<br>0 Asynchronous comparator output drives CTRIPOUTH<br>1 Synchronous comparator output drives CTRIPOUTH<br>2 Output of digital filter drives CTRIPOUTH<br>3 Latched output of digital filter drives CTRIPOUTH                                                                                                                 |
| 3:2 | CTRIPHSEL    | R/W  | 0h    | High comparator CTRIPH source select.<br>0 Asynchronous comparator output drives CTRIPH<br>1 Synchronous comparator output drives CTRIPH<br>2 Output of digital filter drives CTRIPH<br>3 Latched output of digital filter drives CTRIPH                                                                                                                                |
| 1   | COMPHINV     | R/W  | 0h    | High comparator output invert.<br>0 Output of comparator is not inverted<br>1 Output of comparator is inverted                                                                                                                                                                                                                                                          |
| 0   | COMPHSOURCE  | R/W  | 0h    | CompH neg Mux select<br>0 negative mux selects DAC voltage [default]<br>1 negative mux selects INL_3p3v                                                                                                                                                                                                                                                                 |

### 3.3.2.2 CMPSSA\_COMPSTS Register

#### 1 CMPSSA\_COMPSTS Register (Offset = 4h) [reset = 0h]

CMPSS Comparator Status Register.

Return to [Summary Table](#)

**Table 3-507. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSA0       | 5020 0004h       |
| CMPSSA1       | 5020 1004h       |
| CMPSSA2       | 5020 2004h       |
| CMPSSA3       | 5020 3004h       |
| CMPSSA4       | 5020 4004h       |
| CMPSSA5       | 5020 5004h       |
| CMPSSA6       | 5020 6004h       |
| CMPSSA7       | 5020 7004h       |
| CMPSSA8       | 5020 8004h       |
| CMPSSA9       | 5020 9004h       |

**Figure 3-167. CMPSSA\_COMPSTS Name Register**

| 15         | 14 | 13 | 12 | 11 | 10 | 9          | 8        |
|------------|----|----|----|----|----|------------|----------|
| RESERVED_2 |    |    |    |    |    | COMPLLATCH | COMPLSTS |
| R          |    |    |    |    |    | R          | R        |
| 0h         |    |    |    |    |    | 0h         | 0h       |
| 7          | 6  | 5  | 4  | 3  | 2  | 1          | 0        |
| RESERVED_1 |    |    |    |    |    | COMPHLATCH | COMPHSTS |
| R          |    |    |    |    |    | R          | R        |
| 0h         |    |    |    |    |    | 0h         | 0h       |

**Table 3-509. CMPSSA\_COMPSTS Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                            |
|-------|------------|------|-------|--------------------------------------------------------|
| 15:10 | RESERVED_2 | R    | 0h    | Reserved                                               |
| 9     | COMPLLATCH | R    | 0h    | Latched value of low comparator digital filter output  |
| 8     | COMPLSTS   | R    | 0h    | Low comparator digital filter output                   |
| 7:2   | RESERVED_1 | R    | 0h    | Reserved                                               |
| 1     | COMPHLATCH | R    | 0h    | Latched value of high comparator digital filter output |
| 0     | COMPHSTS   | R    | 0h    | High comparator digital filter output                  |

### 3.3.2.3 CMPSSA\_COMPSTSLR Register

#### 1 CMPSSA\_COMPSTSLR Register (Offset = 6h) [reset = 0h]

CMPSS Comparator Status Clear Register.

Return to [Summary Table](#)

**Table 3-510. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSA0       | 5020 0006h       |
| CMPSSA1       | 5020 1006h       |
| CMPSSA2       | 5020 2006h       |
| CMPSSA3       | 5020 3006h       |
| CMPSSA4       | 5020 4006h       |
| CMPSSA5       | 5020 5006h       |
| CMPSSA6       | 5020 6006h       |
| CMPSSA7       | 5020 7006h       |
| CMPSSA8       | 5020 8006h       |
| CMPSSA9       | 5020 9006h       |

**Figure 3-168. CMPSSA\_COMPSTSLR Name Register**

| 15         | 14 | 13 | 12 | 11 | 10         | 9         | 8          |
|------------|----|----|----|----|------------|-----------|------------|
| RESERVED_3 |    |    |    |    | LSYNCCLREN | LLATCHCLR | RESERVED_2 |
| R          |    |    |    |    | R/W        | R/W1TS    | R          |
| 0h         |    |    |    |    | 0h         | 0h        | 0h         |
| 7          | 6  | 5  | 4  | 3  | 2          | 1         | 0          |
| RESERVED_2 |    |    |    |    | HSYNCCLREN | HLATCHCLR | RESERVED_1 |
| R          |    |    |    |    | R/W        | R/W1TS    | R          |
| 0h         |    |    |    |    | 0h         | 0h        | 0h         |

**Table 3-512. CMPSSA\_COMPSTSLR Register Field Descriptions**

| Bit   | Field      | Type   | Reset | Description                                                                                                                                                                                                                                     |
|-------|------------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | RESERVED_3 | R      | 0h    | Reserved                                                                                                                                                                                                                                        |
| 10    | LSYNCCLREN | R/W    | 0h    | Low comparator latch EPWMSYNCPER clear. Enable EPWMSYNCPER reset of low comparator digital filter output latch COMPSTS[COMPLLATCH].<br>0 EPWMSYNCPER will not reset latch<br>1 EPWMSYNCPER will reset latch                                     |
| 9     | LLATCHCLR  | R/W1TS | 0h    | Low comparator latch software clear. Perform software reset of low comparator digital filter output latch COMPSTS[COMPLLATCH]. Reads always return 0.<br>0 No effect<br>1 Generate a single pulse of latch reset signal for COMPSTS[COMPLLATCH] |
| 8:3   | RESERVED_2 | R      | 0h    | Reserved                                                                                                                                                                                                                                        |
| 2     | HSYNCCLREN | R/W    | 0h    | High comparator latch EPWMSYNCPER clear. Enable EPWMSYNCPER reset of high comparator digital filter output latch COMPSTS[COMPHLATCH].<br>0 EPWMSYNCPER will not reset latch<br>1 EPWMSYNCPER will reset latch                                   |

**Table 3-512. CMPSSA\_COMPSTSCLR Register Field Descriptions (continued)**

| Bit | Field      | Type   | Reset | Description                                                                                                                                                                                                                                       |
|-----|------------|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | HLATCHCLR  | R/W1TS | 0h    | High comparator latch software clear. Perform software reset of high comparator digital filter output latch COMPSTS[COMPHLATCH]. Reads always return 0.<br>0 No effect<br>1 Generate a single pulse of latch reset signal for COMPSTS[COMPHLATCH] |
| 0   | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                                                                          |

### 3.3.2.4 CMPSSA\_COMPDACCTL Register

#### 1 CMPSSA\_COMPDACCTL Register (Offset = 8h) [reset = 0h]

CMPSS DAC Control Register.

Return to [Summary Table](#)

**Table 3-513. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSA0       | 5020 0008h       |
| CMPSSA1       | 5020 1008h       |
| CMPSSA2       | 5020 2008h       |
| CMPSSA3       | 5020 3008h       |
| CMPSSA4       | 5020 4008h       |
| CMPSSA5       | 5020 5008h       |
| CMPSSA6       | 5020 6008h       |
| CMPSSA7       | 5020 7008h       |
| CMPSSA8       | 5020 8008h       |
| CMPSSA9       | 5020 9008h       |

**Figure 3-169. CMPSSA\_COMPDACCTL Name Register**

| 15        | 14          | 13         | 12         | 11          | 10 | 9         | 8 |
|-----------|-------------|------------|------------|-------------|----|-----------|---|
| FREESOFT  |             | RESERVED_1 | BLANKEN    | BLANKSOURCE |    |           |   |
| R/W       |             | R          | R/W        | R/W         |    |           |   |
| 0h        |             | 0h         | 0h         | 0h          |    |           |   |
| 7         | 6           | 5          | 4          | 3           | 2  | 1         | 0 |
| SWLOADSEL | RAMPLOADSEL | SELREF     | RAMPSOURCE |             |    | DACSOURCE |   |
| R/W       | R/W         | R/W        | R/W        |             |    | R/W       |   |
| 0h        | 0h          | 0h         | 0h         |             |    | 0h        |   |

**Table 3-515. CMPSSA\_COMPDACCTL Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                  |
|-------|-------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | FREESOFT    | R/W  | 0h    | Free-run or software-run emulation behavior. Behavior of the ramp generator during emulation suspend.<br>00b Ramp generator stops immediately during emulation suspend<br>01b Ramp generator completes current ramp and stops at next EPWMSYNCPER during emulation suspend<br>1Xb Ramp generator runs freely |
| 13    | RESERVED_1  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                     |
| 12    | BLANKEN     | R/W  | 0h    | EPWMBLANK enable. This bit enables the EPWMBLANK signal.<br>0 EPWMBLANK signal is disabled.<br>1 EPWMBLANK signal is enabled.                                                                                                                                                                                |
| 11:8  | BLANKSOURCE | R/W  | 0h    | EPWMBLANK source select. This bit field determines which EPWMnBLANK is passed on as the EPWMBLANK signal.<br>Where n represents the maximum number of EPWMBLANK signals available on the device:<br>0 EPWM0BLANK<br>1 EPWM1BLANK<br>2 EPWM2BLANK<br>...<br>n-1 EPWM(n-1)BLANK                                |



**Table 3-515. CMPSSA\_COMPDACCTL Register Field Descriptions (continued)**

| Bit | Field       | Type | Reset | Description                                                                                                                                                                                                                                                             |
|-----|-------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | SWLOADSEL   | R/W  | 0h    | Software load select. Determines whether DACxVALA is updated from DACxVALS on SYSCLK or EPWMSYNCPER.<br>0 DACxVALA is updated from DACxVALS on SYSCLK<br>1 DACxVALA is updated from DACxVALS on EPWMSYNCPER                                                             |
| 6   | RAMPLOADSEL | R/W  | 0h    | Ramp load select. Determines whether RAMPSTS is updated from RAMPMAXREFA or RAMPMAXREFS when COMPSTS[COMPHSTS] is triggered.<br>0 RAMPSTS is loaded from RAMPMAXREFA<br>1 RAMPSTS is loaded from RAMPMAXREFS                                                            |
| 5   | SELREF      | R/W  | 0h    | CMPSS reference select<br>0 vref_1p8v as reference voltage [default]<br>1 vdd_1p8v as reference voltage                                                                                                                                                                 |
| 4:1 | RAMPSOURCE  | R/W  | 0h    | EPWMSYNCPER source select. Determines which EPWMnSYNCPER signal is used within the CMPSS module. Where n represents the maximum number of EPWMSYNCPER signals available on the device:<br>0 EPWM1SYNCPER<br>1 EPWM2SYNCPER<br>2 EPWM3SYNCPER<br>...<br>n-1 EPWMnSYNCPER |
| 0   | DACSOURCE   | R/W  | 0h    | DAC source select. Determines whether DACHVALA is updated from DACHVALS or from the ramp generator.<br>0 DACHVALA is updated from DACHVALS<br>1 DACHVALA is updated from the ramp generator                                                                             |

### 3.3.2.5 CMPSSA\_COMPDACCTL2 Register

#### 1 CMPSSA\_COMPDACCTL2 Register (Offset = Ah) [reset = 0h]

CMPSS DAC Control Register 2

Return to [Summary Table](#)

**Table 3-516. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSA0       | 5020 000Ah       |
| CMPSSA1       | 5020 100Ah       |
| CMPSSA2       | 5020 200Ah       |
| CMPSSA3       | 5020 300Ah       |
| CMPSSA4       | 5020 400Ah       |
| CMPSSA5       | 5020 500Ah       |
| CMPSSA6       | 5020 600Ah       |
| CMPSSA7       | 5020 700Ah       |
| CMPSSA8       | 5020 800Ah       |
| CMPSSA9       | 5020 900Ah       |

**Figure 3-170. CMPSSA\_COMPDACCTL2 Name Register**

| 15         | 14 | 13          | 12 | 11 | 10                 | 9          | 8                    |
|------------|----|-------------|----|----|--------------------|------------|----------------------|
| RESERVED_3 |    |             |    |    | RAMPSOURCE<br>USEL | RESERVED_2 | BLANKSOURCE<br>EUSEL |
| R          |    |             |    |    | R/W                | R          | R/W                  |
| 0h         |    |             |    |    | 0h                 | 0h         | 0h                   |
| 7          | 6  | 5           | 4  | 3  | 2                  | 1          | 0                    |
| RESERVED_1 |    | DEACTIVESEL |    |    |                    |            | DEENABLE             |
| R          |    | R/W         |    |    |                    |            | R/W                  |
| 0h         |    | 0h          |    |    |                    |            | 0h                   |

**Table 3-518. CMPSSA\_COMPDACCTL2 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                       |
|-------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | RESERVED_3      | R    | 0h    | Reserved                                                                                                                                          |
| 10    | RAMPSOURCEUSEL  | R/W  | 0h    | 0: Selects EPWM0 to 15 as RAMP source<br>1: Selects EPWM16 to 31 as RAMP source                                                                   |
| 9     | RESERVED_2      | R    | 0h    | Reserved                                                                                                                                          |
| 8     | BLANKSOURCEUSEL | R/W  | 0h    | 0: Selects EPWM0 to 15 as blank source<br>1: Selects EPWM16 to 31 as blank source                                                                 |
| 7:6   | RESERVED_1      | R    | 0h    | Reserved                                                                                                                                          |
| 5:1   | DEACTIVESEL     | R/W  | 0h    | DEACTIVE source select:<br>0 : EPWM0.DEACTIVE<br>1 : EPWM1.DEACTIVE<br>2 : EPWM2.DEACTIVE<br>3 : EPWM3.DEACTIVE<br>.<br>.<br>31 : EPWM31.DEACTIVE |
| 0     | DEENABLE        | R/W  | 0h    | DE mode enable.<br>0 DE mode features disabled.<br>1 DE mode features enabled.                                                                    |

### 3.3.2.6 CMPSSA\_DACHVALS Register

#### 1 CMPSSA\_DACHVALS Register (Offset = Ch) [reset = 0h]

CMPSS High DAC Value Shadow Register.

Return to [Summary Table](#)

**Table 3-519. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSA0       | 5020 000Ch       |
| CMPSSA1       | 5020 100Ch       |
| CMPSSA2       | 5020 200Ch       |
| CMPSSA3       | 5020 300Ch       |
| CMPSSA4       | 5020 400Ch       |
| CMPSSA5       | 5020 500Ch       |
| CMPSSA6       | 5020 600Ch       |
| CMPSSA7       | 5020 700Ch       |
| CMPSSA8       | 5020 800Ch       |
| CMPSSA9       | 5020 900Ch       |

**Figure 3-171. CMPSSA\_DACHVALS Name Register**

|            |    |    |    |        |    |   |   |
|------------|----|----|----|--------|----|---|---|
| 15         | 14 | 13 | 12 | 11     | 10 | 9 | 8 |
| RESERVED_1 |    |    |    | DACVAL |    |   |   |
| R          |    |    |    | R/W    |    |   |   |
| 0h         |    |    |    | 0h     |    |   |   |
| 7          | 6  | 5  | 4  | 3      | 2  | 1 | 0 |
| DACVAL     |    |    |    |        |    |   |   |
| R/W        |    |    |    |        |    |   |   |
| 0h         |    |    |    |        |    |   |   |

**Table 3-521. CMPSSA\_DACHVALS Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                 |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                    |
| 11:0  | DACVAL     | R/W  | 0h    | High DAC shadow value. When COMPDACCTL[DACSOURCE]=0, the value of DACHVALS is loaded into DACHVALA on the trigger signal selected by COMPDACCTL[SWLOADSEL]. |

### 3.3.2.7 CMPSSA\_DACHVALA Register

#### 1 CMPSSA\_DACHVALA Register (Offset = Eh) [reset = 0h]

CMPSS High DAC Value Active Register.

Return to [Summary Table](#)

**Table 3-522. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSA0       | 5020 000Eh       |
| CMPSSA1       | 5020 100Eh       |
| CMPSSA2       | 5020 200Eh       |
| CMPSSA3       | 5020 300Eh       |
| CMPSSA4       | 5020 400Eh       |
| CMPSSA5       | 5020 500Eh       |
| CMPSSA6       | 5020 600Eh       |
| CMPSSA7       | 5020 700Eh       |
| CMPSSA8       | 5020 800Eh       |
| CMPSSA9       | 5020 900Eh       |

**Figure 3-172. CMPSSA\_DACHVALA Name Register**

|            |    |    |    |        |    |   |   |
|------------|----|----|----|--------|----|---|---|
| 15         | 14 | 13 | 12 | 11     | 10 | 9 | 8 |
| RESERVED_1 |    |    |    | DACVAL |    |   |   |
| R          |    |    |    | R      |    |   |   |
| 0h         |    |    |    | 0h     |    |   |   |
| 7          | 6  | 5  | 4  | 3      | 2  | 1 | 0 |
| DACVAL     |    |    |    |        |    |   |   |
| R          |    |    |    |        |    |   |   |
| 0h         |    |    |    |        |    |   |   |

**Table 3-524. CMPSSA\_DACHVALA Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                           |
|-------|------------|------|-------|-----------------------------------------------------------------------|
| 15:12 | RESERVED_1 | R    | 0h    | Reserved                                                              |
| 11:0  | DACVAL     | R    | 0h    | High DAC active value. Value that is actively driven by the high DAC. |

### 3.3.2.8 CMPSSA\_RAMPMAXREFA Register

#### 1 CMPSSA\_RAMPMAXREFA Register (Offset = 10h) [reset = 0h]

CMPSS Ramp Max Reference Active Register.

Return to [Summary Table](#)

**Table 3-525. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSA0       | 5020 0010h       |
| CMPSSA1       | 5020 1010h       |
| CMPSSA2       | 5020 2010h       |
| CMPSSA3       | 5020 3010h       |
| CMPSSA4       | 5020 4010h       |
| CMPSSA5       | 5020 5010h       |
| CMPSSA6       | 5020 6010h       |
| CMPSSA7       | 5020 7010h       |
| CMPSSA8       | 5020 8010h       |
| CMPSSA9       | 5020 9010h       |

**Figure 3-173. CMPSSA\_RAMPMAXREFA Name Register**

|            |    |    |    |    |    |   |   |
|------------|----|----|----|----|----|---|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAMPMAXREF |    |    |    |    |    |   |   |
| R          |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| RAMPMAXREF |    |    |    |    |    |   |   |
| R          |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |

**Table 3-527. CMPSSA\_RAMPMAXREFA Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                  |
|------|------------|------|-------|----------------------------------------------------------------------------------------------|
| 15:0 | RAMPMAXREF | R    | 0h    | Ramp maximum reference active value. Latched value to be loaded into ramp generator RAMPSTS. |

### 3.3.2.9 CMPSSA\_RAMPMAXREFS Register

#### 1 CMPSSA\_RAMPMAXREFS Register (Offset = 14h) [reset = 0h]

CMPSS Ramp Max Reference Shadow Register.

Return to [Summary Table](#)

**Table 3-528. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSA0       | 5020 0014h       |
| CMPSSA1       | 5020 1014h       |
| CMPSSA2       | 5020 2014h       |
| CMPSSA3       | 5020 3014h       |
| CMPSSA4       | 5020 4014h       |
| CMPSSA5       | 5020 5014h       |
| CMPSSA6       | 5020 6014h       |
| CMPSSA7       | 5020 7014h       |
| CMPSSA8       | 5020 8014h       |
| CMPSSA9       | 5020 9014h       |

**Figure 3-174. CMPSSA\_RAMPMAXREFS Name Register**

|            |    |    |    |    |    |   |   |
|------------|----|----|----|----|----|---|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAMPMAXREF |    |    |    |    |    |   |   |
| R/W        |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| RAMPMAXREF |    |    |    |    |    |   |   |
| R/W        |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |

**Table 3-530. CMPSSA\_RAMPMAXREFS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                              |
|------|------------|------|-------|------------------------------------------------------------------------------------------|
| 15:0 | RAMPMAXREF | R/W  | 0h    | Ramp maximum reference shadow. Unlatched value to be loaded into ramp generator RAMPSTS. |

### 3.3.2.10 CMPSSA\_RAMPDECVALA Register

#### 1 CMPSSA\_RAMPDECVALA Register (Offset = 18h) [reset = 0h]

CMPSS Ramp Decrement Value Active Register.

Return to [Summary Table](#)

**Table 3-531. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSA0       | 5020 0018h       |
| CMPSSA1       | 5020 1018h       |
| CMPSSA2       | 5020 2018h       |
| CMPSSA3       | 5020 3018h       |
| CMPSSA4       | 5020 4018h       |
| CMPSSA5       | 5020 5018h       |
| CMPSSA6       | 5020 6018h       |
| CMPSSA7       | 5020 7018h       |
| CMPSSA8       | 5020 8018h       |
| CMPSSA9       | 5020 9018h       |

**Figure 3-175. CMPSSA\_RAMPDECVALA Name Register**

|            |    |    |    |    |    |   |   |
|------------|----|----|----|----|----|---|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAMPDECVAL |    |    |    |    |    |   |   |
| R          |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| RAMPDECVAL |    |    |    |    |    |   |   |
| R          |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |

**Table 3-533. CMPSSA\_RAMPDECVALA Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                      |
|------|------------|------|-------|----------------------------------------------------------------------------------|
| 15:0 | RAMPDECVAL | R    | 0h    | Ramp decrement value active. Latched value that will be subtracted from RAMPSTS. |

### 3.3.2.11 CMPSSA\_RAMPDECVALS Register

#### 1 CMPSSA\_RAMPDECVALS Register (Offset = 1Ch) [reset = 0h]

CMPSS Ramp Decrement Value Shadow Register.

Return to [Summary Table](#)

**Table 3-534. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSA0       | 5020 001Ch       |
| CMPSSA1       | 5020 101Ch       |
| CMPSSA2       | 5020 201Ch       |
| CMPSSA3       | 5020 301Ch       |
| CMPSSA4       | 5020 401Ch       |
| CMPSSA5       | 5020 501Ch       |
| CMPSSA6       | 5020 601Ch       |
| CMPSSA7       | 5020 701Ch       |
| CMPSSA8       | 5020 801Ch       |
| CMPSSA9       | 5020 901Ch       |

**Figure 3-176. CMPSSA\_RAMPDECVALS Name Register**

|            |    |    |    |    |    |   |   |
|------------|----|----|----|----|----|---|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAMPDECVAL |    |    |    |    |    |   |   |
| R/W        |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| RAMPDECVAL |    |    |    |    |    |   |   |
| R/W        |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |

**Table 3-536. CMPSSA\_RAMPDECVALS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                 |
|------|------------|------|-------|-----------------------------------------------------------------------------|
| 15:0 | RAMPDECVAL | R/W  | 0h    | Ramp decrement value shadow. Unlatched value to be loaded into RAMPDECVALA. |



### 3.3.2.12 CMPSSA\_RAMPSTS Register

#### 1 CMPSSA\_RAMPSTS Register (Offset = 20h) [reset = 0h]

CMPSS Ramp Status Register.

Return to [Summary Table](#)

**Table 3-537. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSA0       | 5020 0020h       |
| CMPSSA1       | 5020 1020h       |
| CMPSSA2       | 5020 2020h       |
| CMPSSA3       | 5020 3020h       |
| CMPSSA4       | 5020 4020h       |
| CMPSSA5       | 5020 5020h       |
| CMPSSA6       | 5020 6020h       |
| CMPSSA7       | 5020 7020h       |
| CMPSSA8       | 5020 8020h       |
| CMPSSA9       | 5020 9020h       |

**Figure 3-177. CMPSSA\_RAMPSTS Name Register**

|           |    |    |    |    |    |   |   |
|-----------|----|----|----|----|----|---|---|
| 15        | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAMPVALUE |    |    |    |    |    |   |   |
| R         |    |    |    |    |    |   |   |
| 0h        |    |    |    |    |    |   |   |
| 7         | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| RAMPVALUE |    |    |    |    |    |   |   |
| R         |    |    |    |    |    |   |   |
| 0h        |    |    |    |    |    |   |   |

**Table 3-539. CMPSSA\_RAMPSTS Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                  |
|------|-----------|------|-------|----------------------------------------------|
| 15:0 | RAMPVALUE | R    | 0h    | Ramp value. Present value of ramp generator. |

### 3.3.2.13 CMPSSA\_DACLVALS Register

#### 1 CMPSSA\_DACLVALS Register (Offset = 24h) [reset = 0h]

CMPSS Low DAC Value Shadow Register.

Return to [Summary Table](#)

**Table 3-540. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSA0       | 5020 0024h       |
| CMPSSA1       | 5020 1024h       |
| CMPSSA2       | 5020 2024h       |
| CMPSSA3       | 5020 3024h       |
| CMPSSA4       | 5020 4024h       |
| CMPSSA5       | 5020 5024h       |
| CMPSSA6       | 5020 6024h       |
| CMPSSA7       | 5020 7024h       |
| CMPSSA8       | 5020 8024h       |
| CMPSSA9       | 5020 9024h       |

**Figure 3-178. CMPSSA\_DACLVALS Name Register**

|            |    |    |    |        |    |   |   |
|------------|----|----|----|--------|----|---|---|
| 15         | 14 | 13 | 12 | 11     | 10 | 9 | 8 |
| RESERVED_1 |    |    |    | DACVAL |    |   |   |
| R          |    |    |    | R/W    |    |   |   |
| 0h         |    |    |    | 0h     |    |   |   |
| 7          | 6  | 5  | 4  | 3      | 2  | 1 | 0 |
| DACVAL     |    |    |    |        |    |   |   |
| R/W        |    |    |    |        |    |   |   |
| 0h         |    |    |    |        |    |   |   |

**Table 3-542. CMPSSA\_DACLVALS Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                    |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------|
| 15:12 | RESERVED_1 | R    | 0h    | Reserved                                                                                                       |
| 11:0  | DACVAL     | R/W  | 0h    | Low DAC shadow value. value to be loaded into DACVALA on the trigger signal selected by COMPDACCTL[SWLOADSEL]. |

### 3.3.2.14 CMPSSA\_DACLVALA Register

#### 1 CMPSSA\_DACLVALA Register (Offset = 26h) [reset = 0h]

CMPSS Low DAC Value Active Register.

Return to [Summary Table](#)

**Table 3-543. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSA0       | 5020 0026h       |
| CMPSSA1       | 5020 1026h       |
| CMPSSA2       | 5020 2026h       |
| CMPSSA3       | 5020 3026h       |
| CMPSSA4       | 5020 4026h       |
| CMPSSA5       | 5020 5026h       |
| CMPSSA6       | 5020 6026h       |
| CMPSSA7       | 5020 7026h       |
| CMPSSA8       | 5020 8026h       |
| CMPSSA9       | 5020 9026h       |

**Figure 3-179. CMPSSA\_DACLVALA Name Register**

|            |    |    |    |        |    |   |   |
|------------|----|----|----|--------|----|---|---|
| 15         | 14 | 13 | 12 | 11     | 10 | 9 | 8 |
| RESERVED_1 |    |    |    | DACVAL |    |   |   |
| R          |    |    |    | R      |    |   |   |
| 0h         |    |    |    | 0h     |    |   |   |
| 7          | 6  | 5  | 4  | 3      | 2  | 1 | 0 |
| DACVAL     |    |    |    |        |    |   |   |
| R          |    |    |    |        |    |   |   |
| 0h         |    |    |    |        |    |   |   |

**Table 3-545. CMPSSA\_DACLVALA Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                         |
|-------|------------|------|-------|---------------------------------------------------------------------|
| 15:12 | RESERVED_1 | R    | 0h    | Reserved                                                            |
| 11:0  | DACVAL     | R    | 0h    | Low DAC active value. Value that is actively driven by the low DAC. |

### 3.3.2.15 CMPSSA\_RAMPDLYA Register

#### 1 CMPSSA\_RAMPDLYA Register (Offset = 28h) [reset = 0h]

CMPSS Ramp Delay Active Register.

Return to [Summary Table](#)

**Table 3-546. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSA0       | 5020 0028h       |
| CMPSSA1       | 5020 1028h       |
| CMPSSA2       | 5020 2028h       |
| CMPSSA3       | 5020 3028h       |
| CMPSSA4       | 5020 4028h       |
| CMPSSA5       | 5020 5028h       |
| CMPSSA6       | 5020 6028h       |
| CMPSSA7       | 5020 7028h       |
| CMPSSA8       | 5020 8028h       |
| CMPSSA9       | 5020 9028h       |

**Figure 3-180. CMPSSA\_RAMPDLYA Name Register**

| 15         | 14 | 13 | 12 | 11    | 10 | 9 | 8 |
|------------|----|----|----|-------|----|---|---|
| RESERVED_1 |    |    |    | DELAY |    |   |   |
| R          |    |    |    | R     |    |   |   |
| 0h         |    |    |    | 0h    |    |   |   |
| 7          | 6  | 5  | 4  | 3     | 2  | 1 | 0 |
| DELAY      |    |    |    |       |    |   |   |
| R          |    |    |    |       |    |   |   |
| 0h         |    |    |    |       |    |   |   |

**Table 3-548. CMPSSA\_RAMPDLYA Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                          |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                             |
| 12:0  | DELAY      | R    | 0h    | Ramp delay active value. Latched value of the number of cycles to delay the start of the ramp generator decrementer after a EPWMSYNCPER is received. |

### 3.3.2.16 CMPSSA\_RAMPDLYS Register

#### 1 CMPSSA\_RAMPDLYS Register (Offset = 2Ah) [reset = 0h]

CMPSS Ramp Delay Shadow Register.

Return to [Summary Table](#)

**Table 3-549. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSA0       | 5020 002Ah       |
| CMPSSA1       | 5020 102Ah       |
| CMPSSA2       | 5020 202Ah       |
| CMPSSA3       | 5020 302Ah       |
| CMPSSA4       | 5020 402Ah       |
| CMPSSA5       | 5020 502Ah       |
| CMPSSA6       | 5020 602Ah       |
| CMPSSA7       | 5020 702Ah       |
| CMPSSA8       | 5020 802Ah       |
| CMPSSA9       | 5020 902Ah       |

**Figure 3-181. CMPSSA\_RAMPDLYS Name Register**

|            |    |    |    |       |    |   |   |
|------------|----|----|----|-------|----|---|---|
| 15         | 14 | 13 | 12 | 11    | 10 | 9 | 8 |
| RESERVED_1 |    |    |    | DELAY |    |   |   |
| R          |    |    |    | R/W   |    |   |   |
| 0h         |    |    |    | 0h    |    |   |   |
| 7          | 6  | 5  | 4  | 3     | 2  | 1 | 0 |
| DELAY      |    |    |    |       |    |   |   |
| R/W        |    |    |    |       |    |   |   |
| 0h         |    |    |    |       |    |   |   |

**Table 3-551. CMPSSA\_RAMPDLYS Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                          |
|-------|------------|------|-------|----------------------------------------------------------------------|
| 15:13 | RESERVED_1 | R    | 0h    | Reserved                                                             |
| 12:0  | DELAY      | R/W  | 0h    | Ramp delay shadow value. Unlatched value to be loaded into RAMPDLYA. |

### 3.3.2.17 CMPSSA\_CTRIPLFILCTL Register

#### 1 CMPSSA\_CTRIPLFILCTL Register (Offset = 2Ch) [reset = 0h]

CTRIPL Filter Control Register.

Return to [Summary Table](#)

**Table 3-552. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSA0       | 5020 002Ch       |
| CMPSSA1       | 5020 102Ch       |
| CMPSSA2       | 5020 202Ch       |
| CMPSSA3       | 5020 302Ch       |
| CMPSSA4       | 5020 402Ch       |
| CMPSSA5       | 5020 502Ch       |
| CMPSSA6       | 5020 602Ch       |
| CMPSSA7       | 5020 702Ch       |
| CMPSSA8       | 5020 802Ch       |
| CMPSSA9       | 5020 902Ch       |

**Figure 3-182. CMPSSA\_CTRIPLFILCTL Name Register**

| 15      | 14         | 13     | 12 | 11         | 10 | 9 | 8       |
|---------|------------|--------|----|------------|----|---|---------|
| FILINIT | RESERVED_2 | THRESH |    |            |    |   | SAMPWIN |
| R/W1TS  | R          | R/W    |    |            |    |   | R/W     |
| 0h      | 0h         | 0h     |    |            |    |   | 0h      |
| 7       | 6          | 5      | 4  | 3          | 2  | 1 | 0       |
| SAMPWIN |            |        |    | RESERVED_1 |    |   |         |
| R/W     |            |        |    | R          |    |   |         |
| 0h      |            |        |    | 0h         |    |   |         |

**Table 3-554. CMPSSA\_CTRIPLFILCTL Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                                                   |
|------|------------|--------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | FILINIT    | R/W1TS | 0h    | Low filter initialization.<br>0 No effect<br>1 Initialize all samples to the filter input value                                                                                               |
| 14   | RESERVED_2 | R      | 0h    | Reserved                                                                                                                                                                                      |
| 13:9 | THRESH     | R/W    | 0h    | Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Threshold used is THRESH+1. |
| 8:4  | SAMPWIN    | R/W    | 0h    | Low filter sample window size. Number of samples to monitor is SAMPWIN+1.                                                                                                                     |
| 3:0  | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                      |

### 3.3.2.18 CMPSSA\_CTRIPLFILCLKCTL Register

#### 1 CMPSSA\_CTRIPLFILCLKCTL Register (Offset = 2Eh) [reset = 0h]

CTRIPL Filter Clock Control Register.

Return to [Summary Table](#)

**Table 3-555. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSA0       | 5020 002Eh       |
| CMPSSA1       | 5020 102Eh       |
| CMPSSA2       | 5020 202Eh       |
| CMPSSA3       | 5020 302Eh       |
| CMPSSA4       | 5020 402Eh       |
| CMPSSA5       | 5020 502Eh       |
| CMPSSA6       | 5020 602Eh       |
| CMPSSA7       | 5020 702Eh       |
| CMPSSA8       | 5020 802Eh       |
| CMPSSA9       | 5020 902Eh       |

**Figure 3-183. CMPSSA\_CTRIPLFILCLKCTL Name Register**

|             |    |    |    |    |    |   |   |
|-------------|----|----|----|----|----|---|---|
| 15          | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CLKPRESCALE |    |    |    |    |    |   |   |
| R/W         |    |    |    |    |    |   |   |
| 0h          |    |    |    |    |    |   |   |
| 7           | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| CLKPRESCALE |    |    |    |    |    |   |   |
| R/W         |    |    |    |    |    |   |   |
| 0h          |    |    |    |    |    |   |   |

**Table 3-557. CMPSSA\_CTRIPLFILCLKCTL Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                 |
|------|-------------|------|-------|---------------------------------------------------------------------------------------------|
| 15:0 | CLKPRESCALE | R/W  | 0h    | Low filter sample clock prescale. Number of system clocks between samples is CLKPRESCALE+1. |

### 3.3.2.19 CMPSSA\_CTRIPHFILCTL Register

#### 1 CMPSSA\_CTRIPHFILCTL Register (Offset = 30h) [reset = 0h]

CTRIPH Filter Control Register.

Return to [Summary Table](#)

**Table 3-558. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSA0       | 5020 0030h       |
| CMPSSA1       | 5020 1030h       |
| CMPSSA2       | 5020 2030h       |
| CMPSSA3       | 5020 3030h       |
| CMPSSA4       | 5020 4030h       |
| CMPSSA5       | 5020 5030h       |
| CMPSSA6       | 5020 6030h       |
| CMPSSA7       | 5020 7030h       |
| CMPSSA8       | 5020 8030h       |
| CMPSSA9       | 5020 9030h       |

**Figure 3-184. CMPSSA\_CTRIPHFILCTL Name Register**

| 15      | 14         | 13     | 12 | 11         | 10 | 9 | 8       |
|---------|------------|--------|----|------------|----|---|---------|
| FILINIT | RESERVED_2 | THRESH |    |            |    |   | SAMPWIN |
| R/W1TS  | R          | R/W    |    |            |    |   | R/W     |
| 0h      | 0h         | 0h     |    |            |    |   | 0h      |
| 7       | 6          | 5      | 4  | 3          | 2  | 1 | 0       |
| SAMPWIN |            |        |    | RESERVED_1 |    |   |         |
| R/W     |            |        |    | R          |    |   |         |
| 0h      |            |        |    | 0h         |    |   |         |

**Table 3-560. CMPSSA\_CTRIPHFILCTL Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                                                    |
|------|------------|--------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | FILINIT    | R/W1TS | 0h    | High filter initialization.<br>0 No effect<br>1 Initialize all samples to the filter input value                                                                                               |
| 14   | RESERVED_2 | R      | 0h    | Reserved                                                                                                                                                                                       |
| 13:9 | THRESH     | R/W    | 0h    | High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Threshold used is THRESH+1. |
| 8:4  | SAMPWIN    | R/W    | 0h    | High filter sample window size. Number of samples to monitor is SAMPWIN+1.                                                                                                                     |
| 3:0  | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                       |



### 3.3.2.20 CMPSSA\_CTRIPHFILCLKCTL Register

#### 1 CMPSSA\_CTRIPHFILCLKCTL Register (Offset = 32h) [reset = 0h]

CTRIPH Filter Clock Control Register.

Return to [Summary Table](#)

**Table 3-561. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSA0       | 5020 0032h       |
| CMPSSA1       | 5020 1032h       |
| CMPSSA2       | 5020 2032h       |
| CMPSSA3       | 5020 3032h       |
| CMPSSA4       | 5020 4032h       |
| CMPSSA5       | 5020 5032h       |
| CMPSSA6       | 5020 6032h       |
| CMPSSA7       | 5020 7032h       |
| CMPSSA8       | 5020 8032h       |
| CMPSSA9       | 5020 9032h       |

**Figure 3-185. CMPSSA\_CTRIPHFILCLKCTL Name Register**

|             |    |    |    |    |    |   |   |
|-------------|----|----|----|----|----|---|---|
| 15          | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CLKPRESCALE |    |    |    |    |    |   |   |
| R/W         |    |    |    |    |    |   |   |
| 0h          |    |    |    |    |    |   |   |
| 7           | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| CLKPRESCALE |    |    |    |    |    |   |   |
| R/W         |    |    |    |    |    |   |   |
| 0h          |    |    |    |    |    |   |   |

**Table 3-563. CMPSSA\_CTRIPHFILCLKCTL Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                  |
|------|-------------|------|-------|----------------------------------------------------------------------------------------------|
| 15:0 | CLKPRESCALE | R/W  | 0h    | High filter sample clock prescale. Number of system clocks between samples is CLKPRESCALE+1. |

### 3.3.2.21 CMPSSA\_COMPLOCK Register

#### 1 CMPSSA\_COMPLOCK Register (Offset = 34h) [reset = 0h]

CMPSS Lock Register.

Return to [Summary Table](#)

**Table 3-564. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSA0       | 5020 0034h       |
| CMPSSA1       | 5020 1034h       |
| CMPSSA2       | 5020 2034h       |
| CMPSSA3       | 5020 3034h       |
| CMPSSA4       | 5020 4034h       |
| CMPSSA5       | 5020 5034h       |
| CMPSSA6       | 5020 6034h       |
| CMPSSA7       | 5020 7034h       |
| CMPSSA8       | 5020 8034h       |
| CMPSSA9       | 5020 9034h       |

**Figure 3-186. CMPSSA\_COMPLOCK Name Register**

|            |    |    |        |        |        |            |         |
|------------|----|----|--------|--------|--------|------------|---------|
| 15         | 14 | 13 | 12     | 11     | 10     | 9          | 8       |
| RESERVED_1 |    |    |        |        |        |            |         |
| R          |    |    |        |        |        |            |         |
| 0h         |    |    |        |        |        |            |         |
| 7          | 6  | 5  | 4      | 3      | 2      | 1          | 0       |
| RESERVED_1 |    |    | TEST   | CTRIIP | DACCTL | COMPHYSCTL | COMPCTL |
| R          |    |    | R/W1TS | R/W1TS | R/W1TS | R/W1TS     | R/W1TS  |
| 0h         |    |    | 0h     | 0h     | 0h     | 0h         | 0h      |

**Table 3-566. CMPSSA\_COMPLOCK Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                                       |
|------|------------|--------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:5 | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                          |
| 4    | TEST       | R/W1TS | 0h    | TEST Lock. This bit, when set, will prevent any further writes to the any undocumented registers that may effect the performance/ behavior of this block. Once set this bit can only be cleared by a reset.                                                                       |
| 3    | CTRIIP     | R/W1TS | 0h    | Lock write-access to the CTRIIPxFILCTL and CTRIIPxFILCLKCTL registers.<br>0 CTRIIPxFILCTL and CTRIIPxFILCLKCTL registers are not locked. Write 0 to this bit has no effect.<br>1 CTRIIPxFILCTL and CTRIIPxFILCLKCTL registers are locked. Only a system reset can clear this bit. |
| 2    | DACCTL     | R/W1TS | 0h    | Lock write-access to the DACCTL register.<br>0 DACCTL register is not locked. Write 0 to this bit has no effect.<br>1 DACCTL register is locked. Only a system reset can clear this bit.                                                                                          |
| 1    | COMPHYSCTL | R/W1TS | 0h    | Lock write-access to the COMPHYSCTL register.<br>0 COMPHYSCTL register is not locked. Write 0 to this bit has no effect.<br>1 COMPHYSCTL register is locked. Only a system reset can clear this bit.                                                                              |

**Table 3-566. CMPSSA\_COMPLOCK Register Field Descriptions (continued)**

| Bit | Field   | Type   | Reset | Description                                                                                                                                                                                 |
|-----|---------|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | COMPCTL | R/W1TS | 0h    | Lock write-access to the COMPCTL register.<br>0 COMPCTL register is not locked. Write 0 to this bit has no effect.<br>1 COMPCTL register is locked. Only a system reset can clear this bit. |

### 3.3.2.22 CMPSSA\_DACHVALS2 Register

#### 1 CMPSSA\_DACHVALS2 Register (Offset = 38h) [reset = 0h]

CMPSS High DAC Value Shadow Register 2

Return to [Summary Table](#)

**Table 3-567. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSA0       | 5020 0038h       |
| CMPSSA1       | 5020 1038h       |
| CMPSSA2       | 5020 2038h       |
| CMPSSA3       | 5020 3038h       |
| CMPSSA4       | 5020 4038h       |
| CMPSSA5       | 5020 5038h       |
| CMPSSA6       | 5020 6038h       |
| CMPSSA7       | 5020 7038h       |
| CMPSSA8       | 5020 8038h       |
| CMPSSA9       | 5020 9038h       |

**Figure 3-187. CMPSSA\_DACHVALS2 Name Register**

|            |    |    |    |        |    |   |   |
|------------|----|----|----|--------|----|---|---|
| 15         | 14 | 13 | 12 | 11     | 10 | 9 | 8 |
| RESERVED_1 |    |    |    | DACVAL |    |   |   |
| R          |    |    |    | R/W    |    |   |   |
| 0h         |    |    |    | 0h     |    |   |   |
| 7          | 6  | 5  | 4  | 3      | 2  | 1 | 0 |
| DACVAL     |    |    |    |        |    |   |   |
| R/W        |    |    |    |        |    |   |   |
| 0h         |    |    |    |        |    |   |   |

**Table 3-569. CMPSSA\_DACHVALS2 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                    |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                       |
| 11:0  | DACVAL     | R/W  | 0h    | High DAC shadow register2 value. When COMPDACCTL[DACSOURCE]=0, the value of DACHVALS2 is loaded into DACHVALA when DE mode is enabled and selected DEACTIVE input is asserted. |

### 3.3.2.23 CMPSSA\_DACLVALS2 Register

#### 1 CMPSSA\_DACLVALS2 Register (Offset = 3Ah) [reset = 0h]

CMPSS Low DAC Value Shadow Register 2

Return to [Summary Table](#)

**Table 3-570. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSA0       | 5020 003Ah       |
| CMPSSA1       | 5020 103Ah       |
| CMPSSA2       | 5020 203Ah       |
| CMPSSA3       | 5020 303Ah       |
| CMPSSA4       | 5020 403Ah       |
| CMPSSA5       | 5020 503Ah       |
| CMPSSA6       | 5020 603Ah       |
| CMPSSA7       | 5020 703Ah       |
| CMPSSA8       | 5020 803Ah       |
| CMPSSA9       | 5020 903Ah       |

**Figure 3-188. CMPSSA\_DACLVALS2 Name Register**

|            |    |    |    |        |    |   |   |
|------------|----|----|----|--------|----|---|---|
| 15         | 14 | 13 | 12 | 11     | 10 | 9 | 8 |
| RESERVED_1 |    |    |    | DACVAL |    |   |   |
| R          |    |    |    | R/W    |    |   |   |
| 0h         |    |    |    | 0h     |    |   |   |
| 7          | 6  | 5  | 4  | 3      | 2  | 1 | 0 |
| DACVAL     |    |    |    |        |    |   |   |
| R/W        |    |    |    |        |    |   |   |
| 0h         |    |    |    |        |    |   |   |

**Table 3-572. CMPSSA\_DACLVALS2 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                 |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                    |
| 11:0  | DACVAL     | R/W  | 0h    | Low DAC shadow register2 value. Value of DACHVALS2 is loaded into DACHVALA when DE mode is enabled and selected DEACTIVE input is asserted. |

### 3.3.2.24 CMPSSA\_CONFIG1 Register

#### 1 CMPSSA\_CONFIG1 Register (Offset = 3Ch) [reset = 0h]

CMPSS Config1 Register.

Return to [Summary Table](#)

**Table 3-573. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSA0       | 5020 003Ch       |
| CMPSSA1       | 5020 103Ch       |
| CMPSSA2       | 5020 203Ch       |
| CMPSSA3       | 5020 303Ch       |
| CMPSSA4       | 5020 403Ch       |
| CMPSSA5       | 5020 503Ch       |
| CMPSSA6       | 5020 603Ch       |
| CMPSSA7       | 5020 703Ch       |
| CMPSSA8       | 5020 803Ch       |
| CMPSSA9       | 5020 903Ch       |

**Figure 3-189. CMPSSA\_CONFIG1 Name Register**

|          |    |    |    |          |    |   |   |
|----------|----|----|----|----------|----|---|---|
| 15       | 14 | 13 | 12 | 11       | 10 | 9 | 8 |
| SPARE    |    |    |    |          |    |   |   |
| R/W      |    |    |    |          |    |   |   |
| 0h       |    |    |    |          |    |   |   |
| 7        | 6  | 5  | 4  | 3        | 2  | 1 | 0 |
| COMPLHYS |    |    |    | COMPHHYS |    |   |   |
| R/W      |    |    |    | R/W      |    |   |   |
| 0h       |    |    |    | 0h       |    |   |   |

**Table 3-575. CMPSSA\_CONFIG1 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                       |
|------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | SPARE    | R/W  | 0h    | SPARE                                                                                                                                                                                                                                                                                                                                                                             |
| 7:4  | COMPLHYS | R/W  | 0h    | CompL Hysteresis<br>COMPLHYS[3] : reserved<br>COMPLHYS[2] : Controls which comparator output value hysteresis is applied to.<br>1'b0 : Hysteresis is applied when the comparator output is 1'b1<br>1'b1 : Hysteresis is applied when the comparator output is 1'b0<br>COMPLHYS[1:0] = hysteresis value<br>2'b00 : 0 LSB<br>2'b01 : 17.5 LSB<br>2'b10 : 35 LSB<br>2'b11 : 52.5 LSB |
| 3:0  | COMPHHYS | R/W  | 0h    | CompH Hysteresis<br>COMPHHYS[3] : reserved<br>COMPHHYS[2] : Controls which comparator output value hysteresis is applied to.<br>1'b0 : Hysteresis is applied when the comparator output is 1'b1<br>1'b1 : Hysteresis is applied when the comparator output is 1'b0<br>COMPHHYS[1:0] = hysteresis value<br>2'b00 : 0 LSB<br>2'b01 : 17.5 LSB<br>2'b10 : 35 LSB<br>2'b11 : 52.5 LSB |

### 3.4 CMPSSB

#### CMPSSB

##### 3.4.1 CMPSSB Summaries

#### CMPSSB Summaries

**Table 3-576. CMPSSB Registers, Base Address=5022 0000h, Length=4096**

| Offset | Length | Register Name                          | CMPSSB0 Physical Address | CMPSSB1 Physical Address | CMPSSB2 Physical Address |
|--------|--------|----------------------------------------|--------------------------|--------------------------|--------------------------|
| 0h     | 16     | <a href="#">CMPSSB_COMPCTL</a>         | 5022 0000h               | 5022 1000h               | 5022 2000h               |
| 4h     | 16     | <a href="#">CMPSSB_COMPSTS</a>         | 5022 0004h               | 5022 1004h               | 5022 2004h               |
| 6h     | 16     | <a href="#">CMPSSB_COMPSTSCLR</a>      | 5022 0006h               | 5022 1006h               | 5022 2006h               |
| 8h     | 16     | <a href="#">CMPSSB_COMPDACCTL</a>      | 5022 0008h               | 5022 1008h               | 5022 2008h               |
| Ah     | 16     | <a href="#">CMPSSB_COMPDACCTL2</a>     | 5022 000Ah               | 5022 100Ah               | 5022 200Ah               |
| Ch     | 16     | <a href="#">CMPSSB_DACHVALS</a>        | 5022 000Ch               | 5022 100Ch               | 5022 200Ch               |
| Eh     | 16     | <a href="#">CMPSSB_DACHVALA</a>        | 5022 000Eh               | 5022 100Eh               | 5022 200Eh               |
| 10h    | 16     | <a href="#">CMPSSB_RAMPMAXREFA</a>     | 5022 0010h               | 5022 1010h               | 5022 2010h               |
| 14h    | 16     | <a href="#">CMPSSB_RAMPMAXREFS</a>     | 5022 0014h               | 5022 1014h               | 5022 2014h               |
| 18h    | 16     | <a href="#">CMPSSB_RAMPDECVALA</a>     | 5022 0018h               | 5022 1018h               | 5022 2018h               |
| 1Ch    | 16     | <a href="#">CMPSSB_RAMPDECVALS</a>     | 5022 001Ch               | 5022 101Ch               | 5022 201Ch               |
| 20h    | 16     | <a href="#">CMPSSB_RAMPSTS</a>         | 5022 0020h               | 5022 1020h               | 5022 2020h               |
| 24h    | 16     | <a href="#">CMPSSB_DACLVALS</a>        | 5022 0024h               | 5022 1024h               | 5022 2024h               |
| 26h    | 16     | <a href="#">CMPSSB_DACLVALA</a>        | 5022 0026h               | 5022 1026h               | 5022 2026h               |
| 28h    | 16     | <a href="#">CMPSSB_RAMPDLYA</a>        | 5022 0028h               | 5022 1028h               | 5022 2028h               |
| 2Ah    | 16     | <a href="#">CMPSSB_RAMPDLYS</a>        | 5022 002Ah               | 5022 102Ah               | 5022 202Ah               |
| 2Ch    | 16     | <a href="#">CMPSSB_CTRIPFILCTL</a>     | 5022 002Ch               | 5022 102Ch               | 5022 202Ch               |
| 2Eh    | 16     | <a href="#">CMPSSB_CTRIPFILCLKCTL</a>  | 5022 002Eh               | 5022 102Eh               | 5022 202Eh               |
| 30h    | 16     | <a href="#">CMPSSB_CTRIPHFILCTL</a>    | 5022 0030h               | 5022 1030h               | 5022 2030h               |
| 32h    | 16     | <a href="#">CMPSSB_CTRIPHFILCLKCTL</a> | 5022 0032h               | 5022 1032h               | 5022 2032h               |
| 34h    | 16     | <a href="#">CMPSSB_COMBLOCK</a>        | 5022 0034h               | 5022 1034h               | 5022 2034h               |
| 38h    | 16     | <a href="#">CMPSSB_DACHVALS2</a>       | 5022 0038h               | 5022 1038h               | 5022 2038h               |
| 3Ah    | 16     | <a href="#">CMPSSB_DACLVALS2</a>       | 5022 003Ah               | 5022 103Ah               | 5022 203Ah               |
| 3Ch    | 16     | <a href="#">CMPSSB_CONFIG1</a>         | 5022 003Ch               | 5022 103Ch               | 5022 203Ch               |

**Table 3-577. CMPSSB Registers, Base Address=5022 0000h, Length=4096**

| Offset | Length | Register Name                      | CMPSSB3 Physical Address | CMPSSB4 Physical Address | CMPSSB5 Physical Address |
|--------|--------|------------------------------------|--------------------------|--------------------------|--------------------------|
| 0h     | 16     | <a href="#">CMPSSB_COMPCTL</a>     | 5022 3000h               | 5022 4000h               | 5022 5000h               |
| 4h     | 16     | <a href="#">CMPSSB_COMPSTS</a>     | 5022 3004h               | 5022 4004h               | 5022 5004h               |
| 6h     | 16     | <a href="#">CMPSSB_COMPSTSCLR</a>  | 5022 3006h               | 5022 4006h               | 5022 5006h               |
| 8h     | 16     | <a href="#">CMPSSB_COMPDACCTL</a>  | 5022 3008h               | 5022 4008h               | 5022 5008h               |
| Ah     | 16     | <a href="#">CMPSSB_COMPDACCTL2</a> | 5022 300Ah               | 5022 400Ah               | 5022 500Ah               |
| Ch     | 16     | <a href="#">CMPSSB_DACHVALS</a>    | 5022 300Ch               | 5022 400Ch               | 5022 500Ch               |
| Eh     | 16     | <a href="#">CMPSSB_DACHVALA</a>    | 5022 300Eh               | 5022 400Eh               | 5022 500Eh               |
| 10h    | 16     | <a href="#">CMPSSB_RAMPMAXREFA</a> | 5022 3010h               | 5022 4010h               | 5022 5010h               |
| 14h    | 16     | <a href="#">CMPSSB_RAMPMAXREFS</a> | 5022 3014h               | 5022 4014h               | 5022 5014h               |

**Table 3-577. CMPSSB Registers, Base Address=5022 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                          | CMPSSB3 Physical Address | CMPSSB4 Physical Address | CMPSSB5 Physical Address |
|--------|--------|----------------------------------------|--------------------------|--------------------------|--------------------------|
| 18h    | 16     | <a href="#">CMPSSB_RAMPDECVALA</a>     | 5022 3018h               | 5022 4018h               | 5022 5018h               |
| 1Ch    | 16     | <a href="#">CMPSSB_RAMPDECVALS</a>     | 5022 301Ch               | 5022 401Ch               | 5022 501Ch               |
| 20h    | 16     | <a href="#">CMPSSB_RAMPSTS</a>         | 5022 3020h               | 5022 4020h               | 5022 5020h               |
| 24h    | 16     | <a href="#">CMPSSB_DACLVALS</a>        | 5022 3024h               | 5022 4024h               | 5022 5024h               |
| 26h    | 16     | <a href="#">CMPSSB_DACLVALA</a>        | 5022 3026h               | 5022 4026h               | 5022 5026h               |
| 28h    | 16     | <a href="#">CMPSSB_RAMPDLYA</a>        | 5022 3028h               | 5022 4028h               | 5022 5028h               |
| 2Ah    | 16     | <a href="#">CMPSSB_RAMPDLYS</a>        | 5022 302Ah               | 5022 402Ah               | 5022 502Ah               |
| 2Ch    | 16     | <a href="#">CMPSSB_CTRIPLFILCTL</a>    | 5022 302Ch               | 5022 402Ch               | 5022 502Ch               |
| 2Eh    | 16     | <a href="#">CMPSSB_CTRIPLFILCLKCTL</a> | 5022 302Eh               | 5022 402Eh               | 5022 502Eh               |
| 30h    | 16     | <a href="#">CMPSSB_CTRIPHFILCTL</a>    | 5022 3030h               | 5022 4030h               | 5022 5030h               |
| 32h    | 16     | <a href="#">CMPSSB_CTRIPHFILCLKCTL</a> | 5022 3032h               | 5022 4032h               | 5022 5032h               |
| 34h    | 16     | <a href="#">CMPSSB_COMPLOCK</a>        | 5022 3034h               | 5022 4034h               | 5022 5034h               |
| 38h    | 16     | <a href="#">CMPSSB_DACHVALS2</a>       | 5022 3038h               | 5022 4038h               | 5022 5038h               |
| 3Ah    | 16     | <a href="#">CMPSSB_DACLVALS2</a>       | 5022 303Ah               | 5022 403Ah               | 5022 503Ah               |
| 3Ch    | 16     | <a href="#">CMPSSB_CONFIG1</a>         | 5022 303Ch               | 5022 403Ch               | 5022 503Ch               |

**Table 3-578. CMPSSB Registers, Base Address=5022 0000h, Length=4096**

| Offset | Length | Register Name                          | CMPSSB6 Physical Address | CMPSSB7 Physical Address | CMPSSB8 Physical Address |
|--------|--------|----------------------------------------|--------------------------|--------------------------|--------------------------|
| 0h     | 16     | <a href="#">CMPSSB_COMPCTL</a>         | 5022 6000h               | 5022 7000h               | 5022 8000h               |
| 4h     | 16     | <a href="#">CMPSSB_COMPSTS</a>         | 5022 6004h               | 5022 7004h               | 5022 8004h               |
| 6h     | 16     | <a href="#">CMPSSB_COMPSTSLR</a>       | 5022 6006h               | 5022 7006h               | 5022 8006h               |
| 8h     | 16     | <a href="#">CMPSSB_COMPDACCTL</a>      | 5022 6008h               | 5022 7008h               | 5022 8008h               |
| Ah     | 16     | <a href="#">CMPSSB_COMPDACCTL2</a>     | 5022 600Ah               | 5022 700Ah               | 5022 800Ah               |
| Ch     | 16     | <a href="#">CMPSSB_DACHVALS</a>        | 5022 600Ch               | 5022 700Ch               | 5022 800Ch               |
| Eh     | 16     | <a href="#">CMPSSB_DACHVALA</a>        | 5022 600Eh               | 5022 700Eh               | 5022 800Eh               |
| 10h    | 16     | <a href="#">CMPSSB_RAMPMAXREFA</a>     | 5022 6010h               | 5022 7010h               | 5022 8010h               |
| 14h    | 16     | <a href="#">CMPSSB_RAMPMAXREFS</a>     | 5022 6014h               | 5022 7014h               | 5022 8014h               |
| 18h    | 16     | <a href="#">CMPSSB_RAMPDECVALA</a>     | 5022 6018h               | 5022 7018h               | 5022 8018h               |
| 1Ch    | 16     | <a href="#">CMPSSB_RAMPDECVALS</a>     | 5022 601Ch               | 5022 701Ch               | 5022 801Ch               |
| 20h    | 16     | <a href="#">CMPSSB_RAMPSTS</a>         | 5022 6020h               | 5022 7020h               | 5022 8020h               |
| 24h    | 16     | <a href="#">CMPSSB_DACLVALS</a>        | 5022 6024h               | 5022 7024h               | 5022 8024h               |
| 26h    | 16     | <a href="#">CMPSSB_DACLVALA</a>        | 5022 6026h               | 5022 7026h               | 5022 8026h               |
| 28h    | 16     | <a href="#">CMPSSB_RAMPDLYA</a>        | 5022 6028h               | 5022 7028h               | 5022 8028h               |
| 2Ah    | 16     | <a href="#">CMPSSB_RAMPDLYS</a>        | 5022 602Ah               | 5022 702Ah               | 5022 802Ah               |
| 2Ch    | 16     | <a href="#">CMPSSB_CTRIPLFILCTL</a>    | 5022 602Ch               | 5022 702Ch               | 5022 802Ch               |
| 2Eh    | 16     | <a href="#">CMPSSB_CTRIPLFILCLKCTL</a> | 5022 602Eh               | 5022 702Eh               | 5022 802Eh               |
| 30h    | 16     | <a href="#">CMPSSB_CTRIPHFILCTL</a>    | 5022 6030h               | 5022 7030h               | 5022 8030h               |
| 32h    | 16     | <a href="#">CMPSSB_CTRIPHFILCLKCTL</a> | 5022 6032h               | 5022 7032h               | 5022 8032h               |
| 34h    | 16     | <a href="#">CMPSSB_COMPLOCK</a>        | 5022 6034h               | 5022 7034h               | 5022 8034h               |
| 38h    | 16     | <a href="#">CMPSSB_DACHVALS2</a>       | 5022 6038h               | 5022 7038h               | 5022 8038h               |
| 3Ah    | 16     | <a href="#">CMPSSB_DACLVALS2</a>       | 5022 603Ah               | 5022 703Ah               | 5022 803Ah               |
| 3Ch    | 16     | <a href="#">CMPSSB_CONFIG1</a>         | 5022 603Ch               | 5022 703Ch               | 5022 803Ch               |



**Table 3-579. CMPSSB Registers, Base Address=5022 0000h, Length=4096**

| Offset | Length | Register Name                          | CMPSSB9 Physical Address |
|--------|--------|----------------------------------------|--------------------------|
| 0h     | 16     | <a href="#">CMPSSB_COMPCTL</a>         | 5022 9000h               |
| 4h     | 16     | <a href="#">CMPSSB_COMPSTS</a>         | 5022 9004h               |
| 6h     | 16     | <a href="#">CMPSSB_COMPSTSCLR</a>      | 5022 9006h               |
| 8h     | 16     | <a href="#">CMPSSB_COMPDACCTL</a>      | 5022 9008h               |
| Ah     | 16     | <a href="#">CMPSSB_COMPDACCTL2</a>     | 5022 900Ah               |
| Ch     | 16     | <a href="#">CMPSSB_DACHVALS</a>        | 5022 900Ch               |
| Eh     | 16     | <a href="#">CMPSSB_DACHVALA</a>        | 5022 900Eh               |
| 10h    | 16     | <a href="#">CMPSSB_RAMPMAXREFA</a>     | 5022 9010h               |
| 14h    | 16     | <a href="#">CMPSSB_RAMPMAXREFS</a>     | 5022 9014h               |
| 18h    | 16     | <a href="#">CMPSSB_RAMPDECVALA</a>     | 5022 9018h               |
| 1Ch    | 16     | <a href="#">CMPSSB_RAMPDECVALS</a>     | 5022 901Ch               |
| 20h    | 16     | <a href="#">CMPSSB_RAMPSTS</a>         | 5022 9020h               |
| 24h    | 16     | <a href="#">CMPSSB_DACLVALS</a>        | 5022 9024h               |
| 26h    | 16     | <a href="#">CMPSSB_DACLVALA</a>        | 5022 9026h               |
| 28h    | 16     | <a href="#">CMPSSB_RAMPDLYA</a>        | 5022 9028h               |
| 2Ah    | 16     | <a href="#">CMPSSB_RAMPDLYS</a>        | 5022 902Ah               |
| 2Ch    | 16     | <a href="#">CMPSSB_CTRIPLFILCTL</a>    | 5022 902Ch               |
| 2Eh    | 16     | <a href="#">CMPSSB_CTRIPLFILCLKCTL</a> | 5022 902Eh               |
| 30h    | 16     | <a href="#">CMPSSB_CTRIPHFILCTL</a>    | 5022 9030h               |
| 32h    | 16     | <a href="#">CMPSSB_CTRIPHFILCLKCTL</a> | 5022 9032h               |
| 34h    | 16     | <a href="#">CMPSSB_COMPLOCK</a>        | 5022 9034h               |
| 38h    | 16     | <a href="#">CMPSSB_DACHVALS2</a>       | 5022 9038h               |
| 3Ah    | 16     | <a href="#">CMPSSB_DACLVALS2</a>       | 5022 903Ah               |
| 3Ch    | 16     | <a href="#">CMPSSB_CONFIG1</a>         | 5022 903Ch               |

### 3.4.2 CMPSSB Registers

#### CMPSSB Registers

### 3.4.2.1 CMPSSB\_COMPCTL Register

#### 1 CMPSSB\_COMPCTL Register (Offset = 0h) [reset = 0h]

CMPSS Comparator Control Register.

Return to [Summary Table](#)

**Table 3-580. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSB0       | 5022 0000h       |
| CMPSSB1       | 5022 1000h       |
| CMPSSB2       | 5022 2000h       |
| CMPSSB3       | 5022 3000h       |
| CMPSSB4       | 5022 4000h       |
| CMPSSB5       | 5022 5000h       |
| CMPSSB6       | 5022 6000h       |
| CMPSSB7       | 5022 7000h       |
| CMPSSB8       | 5022 8000h       |
| CMPSSB9       | 5022 9000h       |

**Figure 3-190. CMPSSB\_COMPCTL Name Register**

| 15         | 14       | 13          | 12        | 11       | 10         | 9 | 8 |
|------------|----------|-------------|-----------|----------|------------|---|---|
| COMPDAE    | ASYNLEN  | CTRIOUTLSEL | CTRIPLSEL | COMPLINV | RESERVED_3 |   |   |
| R/W        | R/W      | R/W         | R/W       | R/W      | R/W        |   |   |
| 0h         | 0h       | 0h          | 0h        | 0h       | 0h         |   |   |
| 7          | 6        | 5           | 4         | 3        | 2          | 1 | 0 |
| RESERVED_2 | ASYNCHEN | CTRIOUTHSEL | CTRIHSEL  | COMPHINV | RESERVED_1 |   |   |
| R          | R/W      | R/W         | R/W       | R/W      | R/W        |   |   |
| 0h         | 0h       | 0h          | 0h        | 0h       | 0h         |   |   |

**Table 3-582. CMPSSB\_COMPCTL Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                           |
|-------|-------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | COMPDAE     | R/W  | 0h    | Comparator/DAC enable.<br>0 Comparator/DAC disabled<br>1 Comparator/DAC enabled                                                                                                                                                                                                                                                                                       |
| 14    | ASYNLEN     | R/W  | 0h    | Low comparator asynchronous path enable. Allows asynchronous comparator output to feed into OR gate with latched digital filter signal when CTRIPLSEL=3 or CTRIOUTLSEL=3.<br>0 Asynchronous comparator output does not feed into OR gate with latched digital filter output<br>1 Asynchronous comparator output feeds into OR gate with latched digital filter output |
| 13:12 | CTRIOUTLSEL | R/W  | 0h    | Low comparator CTRIOUTL source select.<br>0 Asynchronous comparator output drives CTRIOUTL<br>1 Synchronous comparator output drives CTRIOUTL<br>2 Output of digital filter drives CTRIOUTL<br>3 Latched output of digital filter drives CTRIOUTL                                                                                                                     |
| 11:10 | CTRIPLSEL   | R/W  | 0h    | Low comparator CTRIPL source select.<br>0 Asynchronous comparator output drives CTRIPL<br>1 Synchronous comparator output drives CTRIPL<br>2 Output of digital filter drives CTRIPL<br>3 Latched output of digital filter drives CTRIPL                                                                                                                               |
| 9     | COMPLINV    | R/W  | 0h    | Low comparator output invert.<br>0 Output of comparator is not inverted<br>1 Output of comparator is inverted                                                                                                                                                                                                                                                         |

**Table 3-582. CMPSSB\_COMPCTL Register Field Descriptions (continued)**

| Bit | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                             |
|-----|--------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8   | RESERVED_3   | R/W  | 0h    | Reserved for CMPSSB                                                                                                                                                                                                                                                                                                                                                     |
| 7   | RESERVED_2   | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                |
| 6   | ASYNCHEN     | R/W  | 0h    | High comparator asynchronous path enable. Allows asynchronous comparator output to feed into OR gate with latched digital filter signal when CTRIPHSEL=3 or CTRIPOUTHSEL=3.<br>0 Asynchronous comparator output does not feed into OR gate with latched digital filter output<br>1 Asynchronous comparator output feeds into OR gate with latched digital filter output |
| 5:4 | CTRIPOUTHSEL | R/W  | 0h    | High comparator CTRIPOUTH source select.<br>0 Asynchronous comparator output drives CTRIPOUTH<br>1 Synchronous comparator output drives CTRIPOUTH<br>2 Output of digital filter drives CTRIPOUTH<br>3 Latched output of digital filter drives CTRIPOUTH                                                                                                                 |
| 3:2 | CTRIPHSEL    | R/W  | 0h    | High comparator CTRIPH source select.<br>0 Asynchronous comparator output drives CTRIPH<br>1 Synchronous comparator output drives CTRIPH<br>2 Output of digital filter drives CTRIPH<br>3 Latched output of digital filter drives CTRIPH                                                                                                                                |
| 1   | COMPHINV     | R/W  | 0h    | High comparator output invert.<br>0 Output of comparator is not inverted<br>1 Output of comparator is inverted                                                                                                                                                                                                                                                          |
| 0   | RESERVED_1   | R/W  | 0h    | Reserved for CMPSSB                                                                                                                                                                                                                                                                                                                                                     |

### 3.4.2.2 CMPSSB\_COMPSTS Register

#### 1 CMPSSB\_COMPSTS Register (Offset = 4h) [reset = 0h]

CMPSS Comparator Status Register.

Return to [Summary Table](#)

**Table 3-583. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSB0       | 5022 0004h       |
| CMPSSB1       | 5022 1004h       |
| CMPSSB2       | 5022 2004h       |
| CMPSSB3       | 5022 3004h       |
| CMPSSB4       | 5022 4004h       |
| CMPSSB5       | 5022 5004h       |
| CMPSSB6       | 5022 6004h       |
| CMPSSB7       | 5022 7004h       |
| CMPSSB8       | 5022 8004h       |
| CMPSSB9       | 5022 9004h       |

**Figure 3-191. CMPSSB\_COMPSTS Name Register**

| 15         | 14 | 13 | 12 | 11 | 10 | 9          | 8        |
|------------|----|----|----|----|----|------------|----------|
| RESERVED_2 |    |    |    |    |    | COMPLLATCH | COMPLSTS |
| R          |    |    |    |    |    | R          | R        |
| 0h         |    |    |    |    |    | 0h         | 0h       |
| 7          | 6  | 5  | 4  | 3  | 2  | 1          | 0        |
| RESERVED_1 |    |    |    |    |    | COMPHLATCH | COMPHSTS |
| R          |    |    |    |    |    | R          | R        |
| 0h         |    |    |    |    |    | 0h         | 0h       |

**Table 3-585. CMPSSB\_COMPSTS Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                            |
|-------|------------|------|-------|--------------------------------------------------------|
| 15:10 | RESERVED_2 | R    | 0h    | Reserved                                               |
| 9     | COMPLLATCH | R    | 0h    | Latched value of low comparator digital filter output  |
| 8     | COMPLSTS   | R    | 0h    | Low comparator digital filter output                   |
| 7:2   | RESERVED_1 | R    | 0h    | Reserved                                               |
| 1     | COMPHLATCH | R    | 0h    | Latched value of high comparator digital filter output |
| 0     | COMPHSTS   | R    | 0h    | High comparator digital filter output                  |

### 3.4.2.3 CMPSSB\_COMPSTSLR Register

#### 1 CMPSSB\_COMPSTSLR Register (Offset = 6h) [reset = 0h]

CMPSS Comparator Status Clear Register.

Return to [Summary Table](#)

**Table 3-586. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSB0       | 5022 0006h       |
| CMPSSB1       | 5022 1006h       |
| CMPSSB2       | 5022 2006h       |
| CMPSSB3       | 5022 3006h       |
| CMPSSB4       | 5022 4006h       |
| CMPSSB5       | 5022 5006h       |
| CMPSSB6       | 5022 6006h       |
| CMPSSB7       | 5022 7006h       |
| CMPSSB8       | 5022 8006h       |
| CMPSSB9       | 5022 9006h       |

**Figure 3-192. CMPSSB\_COMPSTSLR Name Register**

| 15         | 14 | 13 | 12 | 11 | 10         | 9         | 8          |
|------------|----|----|----|----|------------|-----------|------------|
| RESERVED_3 |    |    |    |    | LSYNCCLREN | LLATCHCLR | RESERVED_2 |
| R          |    |    |    |    | R/W        | R/W1TS    | R          |
| 0h         |    |    |    |    | 0h         | 0h        | 0h         |
| 7          | 6  | 5  | 4  | 3  | 2          | 1         | 0          |
| RESERVED_2 |    |    |    |    | HSYNCCLREN | HLATCHCLR | RESERVED_1 |
| R          |    |    |    |    | R/W        | R/W1TS    | R          |
| 0h         |    |    |    |    | 0h         | 0h        | 0h         |

**Table 3-588. CMPSSB\_COMPSTSLR Register Field Descriptions**

| Bit   | Field      | Type   | Reset | Description                                                                                                                                                                                                                                     |
|-------|------------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | RESERVED_3 | R      | 0h    | Reserved                                                                                                                                                                                                                                        |
| 10    | LSYNCCLREN | R/W    | 0h    | Low comparator latch EPWMSYNCPER clear. Enable EPWMSYNCPER reset of low comparator digital filter output latch COMPSTS[COMPLLATCH].<br>0 EPWMSYNCPER will not reset latch<br>1 EPWMSYNCPER will reset latch                                     |
| 9     | LLATCHCLR  | R/W1TS | 0h    | Low comparator latch software clear. Perform software reset of low comparator digital filter output latch COMPSTS[COMPLLATCH]. Reads always return 0.<br>0 No effect<br>1 Generate a single pulse of latch reset signal for COMPSTS[COMPLLATCH] |
| 8:3   | RESERVED_2 | R      | 0h    | Reserved                                                                                                                                                                                                                                        |
| 2     | HSYNCCLREN | R/W    | 0h    | High comparator latch EPWMSYNCPER clear. Enable EPWMSYNCPER reset of high comparator digital filter output latch COMPSTS[COMPHLATCH].<br>0 EPWMSYNCPER will not reset latch<br>1 EPWMSYNCPER will reset latch                                   |

**Table 3-588. CMPSSB\_COMPSTSCLR Register Field Descriptions (continued)**

| Bit | Field      | Type   | Reset | Description                                                                                                                                                                                                                                       |
|-----|------------|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | HLATCHCLR  | R/W1TS | 0h    | High comparator latch software clear. Perform software reset of high comparator digital filter output latch COMPSTS[COMPHLATCH]. Reads always return 0.<br>0 No effect<br>1 Generate a single pulse of latch reset signal for COMPSTS[COMPHLATCH] |
| 0   | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                                                                          |

### 3.4.2.4 CMPSSB\_COMPDACCTL Register

#### 1 CMPSSB\_COMPDACCTL Register (Offset = 8h) [reset = 0h]

CMPSS DAC Control Register.

Return to [Summary Table](#)

**Table 3-589. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSB0       | 5022 0008h       |
| CMPSSB1       | 5022 1008h       |
| CMPSSB2       | 5022 2008h       |
| CMPSSB3       | 5022 3008h       |
| CMPSSB4       | 5022 4008h       |
| CMPSSB5       | 5022 5008h       |
| CMPSSB6       | 5022 6008h       |
| CMPSSB7       | 5022 7008h       |
| CMPSSB8       | 5022 8008h       |
| CMPSSB9       | 5022 9008h       |

**Figure 3-193. CMPSSB\_COMPDACCTL Name Register**

| 15        | 14          | 13         | 12         | 11          | 10 | 9         | 8 |
|-----------|-------------|------------|------------|-------------|----|-----------|---|
| FREESOFT  |             | RESERVED_1 | BLANKEN    | BLANKSOURCE |    |           |   |
| R/W       |             | R          | R/W        | R/W         |    |           |   |
| 0h        |             | 0h         | 0h         | 0h          |    |           |   |
| 7         | 6           | 5          | 4          | 3           | 2  | 1         | 0 |
| SWLOADSEL | RAMPLOADSEL | SELREF     | RAMPSOURCE |             |    | DACSOURCE |   |
| R/W       | R/W         | R/W        | R/W        |             |    | R/W       |   |
| 0h        | 0h          | 0h         | 0h         |             |    | 0h        |   |

**Table 3-591. CMPSSB\_COMPDACCTL Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                  |
|-------|-------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | FREESOFT    | R/W  | 0h    | Free-run or software-run emulation behavior. Behavior of the ramp generator during emulation suspend.<br>00b Ramp generator stops immediately during emulation suspend<br>01b Ramp generator completes current ramp and stops at next EPWMSYNCPER during emulation suspend<br>1Xb Ramp generator runs freely |
| 13    | RESERVED_1  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                     |
| 12    | BLANKEN     | R/W  | 0h    | EPWMBLANK enable. This bit enables the EPWMBLANK signal.<br>0 EPWMBLANK signal is disabled.<br>1 EPWMBLANK signal is enabled.                                                                                                                                                                                |
| 11:8  | BLANKSOURCE | R/W  | 0h    | EPWMBLANK source select. This bit field determines which EPWMnBLANK is passed on as the EPWMBLANK signal.<br>Where n represents the maximum number of EPWMBLANK signals available on the device:<br>0 EPWM1BLANK<br>1 EPWM2BLANK<br>2 EPWM3BLANK<br>...<br>n-1 EPWMnBLANK                                    |

**Table 3-591. CMPSSB\_COMPDACCTL Register Field Descriptions (continued)**

| Bit | Field       | Type | Reset | Description                                                                                                                                                                                                                                                             |
|-----|-------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | SWLOADSEL   | R/W  | 0h    | Software load select. Determines whether DACxVALA is updated from DACxVALS on SYSCLK or EPWMSYNCPER.<br>0 DACxVALA is updated from DACxVALS on SYSCLK<br>1 DACxVALA is updated from DACxVALS on EPWMSYNCPER                                                             |
| 6   | RAMPLOADSEL | R/W  | 0h    | Ramp load select. Determines whether RAMPSTS is updated from RAMPMAXREFA or RAMPMAXREFS when COMPSTS[COMPHSTS] is triggered.<br>0 RAMPSTS is loaded from RAMPMAXREFA<br>1 RAMPSTS is loaded from RAMPMAXREFS                                                            |
| 5   | SELREF      | R/W  | 0h    | CMPSS reference select<br>0 vref_1p8v as reference voltage [default]<br>1 vdd_1p8v as reference voltage                                                                                                                                                                 |
| 4:1 | RAMPSOURCE  | R/W  | 0h    | EPWMSYNCPER source select. Determines which EPWMnSYNCPER signal is used within the CMPSS module. Where n represents the maximum number of EPWMSYNCPER signals available on the device:<br>0 EPWM1SYNCPER<br>1 EPWM2SYNCPER<br>2 EPWM3SYNCPER<br>...<br>n-1 EPWMnSYNCPER |
| 0   | DACSOURCE   | R/W  | 0h    | DAC source select. Determines whether DACHVALA is updated from DACHVALS or from the ramp generator.<br>0 DACHVALA is updated from DACHVALS<br>1 DACHVALA is updated from the ramp generator                                                                             |



### 3.4.2.5 CMPSSB\_COMPDACCTL2 Register

#### 1 CMPSSB\_COMPDACCTL2 Register (Offset = Ah) [reset = 0h]

CMPSS DAC Control Register 2

Return to [Summary Table](#)

**Table 3-592. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSB0       | 5022 000Ah       |
| CMPSSB1       | 5022 100Ah       |
| CMPSSB2       | 5022 200Ah       |
| CMPSSB3       | 5022 300Ah       |
| CMPSSB4       | 5022 400Ah       |
| CMPSSB5       | 5022 500Ah       |
| CMPSSB6       | 5022 600Ah       |
| CMPSSB7       | 5022 700Ah       |
| CMPSSB8       | 5022 800Ah       |
| CMPSSB9       | 5022 900Ah       |

**Figure 3-194. CMPSSB\_COMPDACCTL2 Name Register**

| 15         | 14 | 13          | 12 | 11 | 10                 | 9          | 8                    |
|------------|----|-------------|----|----|--------------------|------------|----------------------|
| RESERVED_3 |    |             |    |    | RAMPSOURCE<br>USEL | RESERVED_2 | BLANKSOURCE<br>EUSEL |
| R          |    |             |    |    | R/W                | R          | R/W                  |
| 0h         |    |             |    |    | 0h                 | 0h         | 0h                   |
| 7          | 6  | 5           | 4  | 3  | 2                  | 1          | 0                    |
| RESERVED_1 |    | DEACTIVESEL |    |    |                    |            | DEENABLE             |
| R          |    | R/W         |    |    |                    |            | R/W                  |
| 0h         |    | 0h          |    |    |                    |            | 0h                   |

**Table 3-594. CMPSSB\_COMPDACCTL2 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                 |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | RESERVED_3      | R    | 0h    | Reserved                                                                                                                                                    |
| 10    | RAMPSOURCEUSEL  | R/W  | 0h    | 0: Selects EPWM0 to 15 as RAMP source<br>1: Selects EPWM16 to 31 as RAMP source                                                                             |
| 9     | RESERVED_2      | R    | 0h    | Reserved                                                                                                                                                    |
| 8     | BLANKSOURCEUSEL | R/W  | 0h    | 0: Selects EPWM0 to 15 as blank source<br>1: Selects EPWM16 to 31 as blank source                                                                           |
| 7:6   | RESERVED_1      | R    | 0h    | Reserved                                                                                                                                                    |
| 5:1   | DEACTIVESEL     | R/W  | 0h    | DEACTIVE source select:<br>0x0 : EPWM0.DEACTIVE<br>0x1 : EPWM1.DEACTIVE<br>0x2 : EPWM2.DEACTIVE<br>0x3 : EPWM3.DEACTIVE<br>.<br>.<br>0x31 : EPWM31.DEACTIVE |
| 0     | DEENABLE        | R/W  | 0h    | DE mode enable.<br>0 DE mode features disabled.<br>1 DE mode features enabled.                                                                              |

### 3.4.2.6 CMPSSB\_DACHVALS Register

#### 1 CMPSSB\_DACHVALS Register (Offset = Ch) [reset = 0h]

CMPSS High DAC Value Shadow Register.

Return to [Summary Table](#)

**Table 3-595. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSB0       | 5022 000Ch       |
| CMPSSB1       | 5022 100Ch       |
| CMPSSB2       | 5022 200Ch       |
| CMPSSB3       | 5022 300Ch       |
| CMPSSB4       | 5022 400Ch       |
| CMPSSB5       | 5022 500Ch       |
| CMPSSB6       | 5022 600Ch       |
| CMPSSB7       | 5022 700Ch       |
| CMPSSB8       | 5022 800Ch       |
| CMPSSB9       | 5022 900Ch       |

**Figure 3-195. CMPSSB\_DACHVALS Name Register**

|            |    |    |    |        |    |   |   |
|------------|----|----|----|--------|----|---|---|
| 15         | 14 | 13 | 12 | 11     | 10 | 9 | 8 |
| RESERVED_1 |    |    |    | DACVAL |    |   |   |
| R          |    |    |    | R/W    |    |   |   |
| 0h         |    |    |    | 0h     |    |   |   |
| 7          | 6  | 5  | 4  | 3      | 2  | 1 | 0 |
| DACVAL     |    |    |    |        |    |   |   |
| R/W        |    |    |    |        |    |   |   |
| 0h         |    |    |    |        |    |   |   |

**Table 3-597. CMPSSB\_DACHVALS Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                 |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                    |
| 11:0  | DACVAL     | R/W  | 0h    | High DAC shadow value. When COMPDACCTL[DACSOURCE]=0, the value of DACHVALS is loaded into DACHVALA on the trigger signal selected by COMPDACCTL[SWLOADSEL]. |

### 3.4.2.7 CMPSSB\_DACHVALA Register

#### 1 CMPSSB\_DACHVALA Register (Offset = Eh) [reset = 0h]

CMPSS High DAC Value Active Register.

Return to [Summary Table](#)

**Table 3-598. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSB0       | 5022 000Eh       |
| CMPSSB1       | 5022 100Eh       |
| CMPSSB2       | 5022 200Eh       |
| CMPSSB3       | 5022 300Eh       |
| CMPSSB4       | 5022 400Eh       |
| CMPSSB5       | 5022 500Eh       |
| CMPSSB6       | 5022 600Eh       |
| CMPSSB7       | 5022 700Eh       |
| CMPSSB8       | 5022 800Eh       |
| CMPSSB9       | 5022 900Eh       |

**Figure 3-196. CMPSSB\_DACHVALA Name Register**

|            |    |    |    |        |    |   |   |
|------------|----|----|----|--------|----|---|---|
| 15         | 14 | 13 | 12 | 11     | 10 | 9 | 8 |
| RESERVED_1 |    |    |    | DACVAL |    |   |   |
| R          |    |    |    | R      |    |   |   |
| 0h         |    |    |    | 0h     |    |   |   |
| 7          | 6  | 5  | 4  | 3      | 2  | 1 | 0 |
| DACVAL     |    |    |    |        |    |   |   |
| R          |    |    |    |        |    |   |   |
| 0h         |    |    |    |        |    |   |   |

**Table 3-600. CMPSSB\_DACHVALA Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                           |
|-------|------------|------|-------|-----------------------------------------------------------------------|
| 15:12 | RESERVED_1 | R    | 0h    | Reserved                                                              |
| 11:0  | DACVAL     | R    | 0h    | High DAC active value. Value that is actively driven by the high DAC. |

### 3.4.2.8 CMPSSB\_RAMPMAXREFA Register

#### 1 CMPSSB\_RAMPMAXREFA Register (Offset = 10h) [reset = 0h]

CMPSS Ramp Max Reference Active Register.

Return to [Summary Table](#)

**Table 3-601. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSB0       | 5022 0010h       |
| CMPSSB1       | 5022 1010h       |
| CMPSSB2       | 5022 2010h       |
| CMPSSB3       | 5022 3010h       |
| CMPSSB4       | 5022 4010h       |
| CMPSSB5       | 5022 5010h       |
| CMPSSB6       | 5022 6010h       |
| CMPSSB7       | 5022 7010h       |
| CMPSSB8       | 5022 8010h       |
| CMPSSB9       | 5022 9010h       |

**Figure 3-197. CMPSSB\_RAMPMAXREFA Name Register**

|            |    |    |    |    |    |   |   |
|------------|----|----|----|----|----|---|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAMPMAXREF |    |    |    |    |    |   |   |
| R          |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| RAMPMAXREF |    |    |    |    |    |   |   |
| R          |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |

**Table 3-603. CMPSSB\_RAMPMAXREFA Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                  |
|------|------------|------|-------|----------------------------------------------------------------------------------------------|
| 15:0 | RAMPMAXREF | R    | 0h    | Ramp maximum reference active value. Latched value to be loaded into ramp generator RAMPSTS. |

### 3.4.2.9 CMPSSB\_RAMPMAXREFS Register

#### 1 CMPSSB\_RAMPMAXREFS Register (Offset = 14h) [reset = 0h]

CMPSS Ramp Max Reference Shadow Register.

Return to [Summary Table](#)

**Table 3-604. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSB0       | 5022 0014h       |
| CMPSSB1       | 5022 1014h       |
| CMPSSB2       | 5022 2014h       |
| CMPSSB3       | 5022 3014h       |
| CMPSSB4       | 5022 4014h       |
| CMPSSB5       | 5022 5014h       |
| CMPSSB6       | 5022 6014h       |
| CMPSSB7       | 5022 7014h       |
| CMPSSB8       | 5022 8014h       |
| CMPSSB9       | 5022 9014h       |

**Figure 3-198. CMPSSB\_RAMPMAXREFS Name Register**

|            |    |    |    |    |    |   |   |
|------------|----|----|----|----|----|---|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAMPMAXREF |    |    |    |    |    |   |   |
| R/W        |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| RAMPMAXREF |    |    |    |    |    |   |   |
| R/W        |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |

**Table 3-606. CMPSSB\_RAMPMAXREFS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                              |
|------|------------|------|-------|------------------------------------------------------------------------------------------|
| 15:0 | RAMPMAXREF | R/W  | 0h    | Ramp maximum reference shadow. Unlatched value to be loaded into ramp generator RAMPSTS. |

### 3.4.2.10 CMPSSB\_RAMPDECVALA Register

#### 1 CMPSSB\_RAMPDECVALA Register (Offset = 18h) [reset = 0h]

CMPSS Ramp Decrement Value Active Register.

Return to [Summary Table](#)

**Table 3-607. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSB0       | 5022 0018h       |
| CMPSSB1       | 5022 1018h       |
| CMPSSB2       | 5022 2018h       |
| CMPSSB3       | 5022 3018h       |
| CMPSSB4       | 5022 4018h       |
| CMPSSB5       | 5022 5018h       |
| CMPSSB6       | 5022 6018h       |
| CMPSSB7       | 5022 7018h       |
| CMPSSB8       | 5022 8018h       |
| CMPSSB9       | 5022 9018h       |

**Figure 3-199. CMPSSB\_RAMPDECVALA Name Register**

|            |    |    |    |    |    |   |   |
|------------|----|----|----|----|----|---|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAMPDECVAL |    |    |    |    |    |   |   |
| R          |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| RAMPDECVAL |    |    |    |    |    |   |   |
| R          |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |

**Table 3-609. CMPSSB\_RAMPDECVALA Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                      |
|------|------------|------|-------|----------------------------------------------------------------------------------|
| 15:0 | RAMPDECVAL | R    | 0h    | Ramp decrement value active. Latched value that will be subtracted from RAMPSTS. |

### 3.4.2.11 CMPSSB\_RAMPDECVALS Register

#### 1 CMPSSB\_RAMPDECVALS Register (Offset = 1Ch) [reset = 0h]

CMPSS Ramp Decrement Value Shadow Register.

Return to [Summary Table](#)

**Table 3-610. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSB0       | 5022 001Ch       |
| CMPSSB1       | 5022 101Ch       |
| CMPSSB2       | 5022 201Ch       |
| CMPSSB3       | 5022 301Ch       |
| CMPSSB4       | 5022 401Ch       |
| CMPSSB5       | 5022 501Ch       |
| CMPSSB6       | 5022 601Ch       |
| CMPSSB7       | 5022 701Ch       |
| CMPSSB8       | 5022 801Ch       |
| CMPSSB9       | 5022 901Ch       |

**Figure 3-200. CMPSSB\_RAMPDECVALS Name Register**

|            |    |    |    |    |    |   |   |
|------------|----|----|----|----|----|---|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAMPDECVAL |    |    |    |    |    |   |   |
| R/W        |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| RAMPDECVAL |    |    |    |    |    |   |   |
| R/W        |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |

**Table 3-612. CMPSSB\_RAMPDECVALS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                 |
|------|------------|------|-------|-----------------------------------------------------------------------------|
| 15:0 | RAMPDECVAL | R/W  | 0h    | Ramp decrement value shadow. Unlatched value to be loaded into RAMPDECVALA. |

### 3.4.2.12 CMPSSB\_RAMPSTS Register

#### 1 CMPSSB\_RAMPSTS Register (Offset = 20h) [reset = 0h]

CMPSS Ramp Status Register.

Return to [Summary Table](#)

**Table 3-613. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSB0       | 5022 0020h       |
| CMPSSB1       | 5022 1020h       |
| CMPSSB2       | 5022 2020h       |
| CMPSSB3       | 5022 3020h       |
| CMPSSB4       | 5022 4020h       |
| CMPSSB5       | 5022 5020h       |
| CMPSSB6       | 5022 6020h       |
| CMPSSB7       | 5022 7020h       |
| CMPSSB8       | 5022 8020h       |
| CMPSSB9       | 5022 9020h       |

**Figure 3-201. CMPSSB\_RAMPSTS Name Register**

|           |    |    |    |    |    |   |   |
|-----------|----|----|----|----|----|---|---|
| 15        | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RAMPVALUE |    |    |    |    |    |   |   |
| R         |    |    |    |    |    |   |   |
| 0h        |    |    |    |    |    |   |   |
| 7         | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| RAMPVALUE |    |    |    |    |    |   |   |
| R         |    |    |    |    |    |   |   |
| 0h        |    |    |    |    |    |   |   |

**Table 3-615. CMPSSB\_RAMPSTS Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                  |
|------|-----------|------|-------|----------------------------------------------|
| 15:0 | RAMPVALUE | R    | 0h    | Ramp value. Present value of ramp generator. |



### 3.4.2.13 CMPSSB\_DACLVALS Register

#### 1 CMPSSB\_DACLVALS Register (Offset = 24h) [reset = 0h]

CMPSS Low DAC Value Shadow Register.

Return to [Summary Table](#)

**Table 3-616. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSB0       | 5022 0024h       |
| CMPSSB1       | 5022 1024h       |
| CMPSSB2       | 5022 2024h       |
| CMPSSB3       | 5022 3024h       |
| CMPSSB4       | 5022 4024h       |
| CMPSSB5       | 5022 5024h       |
| CMPSSB6       | 5022 6024h       |
| CMPSSB7       | 5022 7024h       |
| CMPSSB8       | 5022 8024h       |
| CMPSSB9       | 5022 9024h       |

**Figure 3-202. CMPSSB\_DACLVALS Name Register**

|            |    |    |    |        |    |   |   |
|------------|----|----|----|--------|----|---|---|
| 15         | 14 | 13 | 12 | 11     | 10 | 9 | 8 |
| RESERVED_1 |    |    |    | DACVAL |    |   |   |
| R          |    |    |    | R/W    |    |   |   |
| 0h         |    |    |    | 0h     |    |   |   |
| 7          | 6  | 5  | 4  | 3      | 2  | 1 | 0 |
| DACVAL     |    |    |    |        |    |   |   |
| R/W        |    |    |    |        |    |   |   |
| 0h         |    |    |    |        |    |   |   |

**Table 3-618. CMPSSB\_DACLVALS Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                    |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------|
| 15:12 | RESERVED_1 | R    | 0h    | Reserved                                                                                                       |
| 11:0  | DACVAL     | R/W  | 0h    | Low DAC shadow value. value to be loaded into DACVALA on the trigger signal selected by COMPDACCTL[SWLOADSEL]. |

### 3.4.2.14 CMPSSB\_DACLVALA Register

#### 1 CMPSSB\_DACLVALA Register (Offset = 26h) [reset = 0h]

CMPSS Low DAC Value Active Register.

Return to [Summary Table](#)

**Table 3-619. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSB0       | 5022 0026h       |
| CMPSSB1       | 5022 1026h       |
| CMPSSB2       | 5022 2026h       |
| CMPSSB3       | 5022 3026h       |
| CMPSSB4       | 5022 4026h       |
| CMPSSB5       | 5022 5026h       |
| CMPSSB6       | 5022 6026h       |
| CMPSSB7       | 5022 7026h       |
| CMPSSB8       | 5022 8026h       |
| CMPSSB9       | 5022 9026h       |

**Figure 3-203. CMPSSB\_DACLVALA Name Register**

|            |    |    |    |        |    |   |   |
|------------|----|----|----|--------|----|---|---|
| 15         | 14 | 13 | 12 | 11     | 10 | 9 | 8 |
| RESERVED_1 |    |    |    | DACVAL |    |   |   |
| R          |    |    |    | R      |    |   |   |
| 0h         |    |    |    | 0h     |    |   |   |
| 7          | 6  | 5  | 4  | 3      | 2  | 1 | 0 |
| DACVAL     |    |    |    |        |    |   |   |
| R          |    |    |    |        |    |   |   |
| 0h         |    |    |    |        |    |   |   |

**Table 3-621. CMPSSB\_DACLVALA Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                         |
|-------|------------|------|-------|---------------------------------------------------------------------|
| 15:12 | RESERVED_1 | R    | 0h    | Reserved                                                            |
| 11:0  | DACVAL     | R    | 0h    | Low DAC active value. Value that is actively driven by the low DAC. |

### 3.4.2.15 CMPSSB\_RAMPDLYA Register

#### 1 CMPSSB\_RAMPDLYA Register (Offset = 28h) [reset = 0h]

CMPSS Ramp Delay Active Register.

Return to [Summary Table](#)

**Table 3-622. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSB0       | 5022 0028h       |
| CMPSSB1       | 5022 1028h       |
| CMPSSB2       | 5022 2028h       |
| CMPSSB3       | 5022 3028h       |
| CMPSSB4       | 5022 4028h       |
| CMPSSB5       | 5022 5028h       |
| CMPSSB6       | 5022 6028h       |
| CMPSSB7       | 5022 7028h       |
| CMPSSB8       | 5022 8028h       |
| CMPSSB9       | 5022 9028h       |

**Figure 3-204. CMPSSB\_RAMPDLYA Name Register**

| 15         | 14 | 13 | 12 | 11    | 10 | 9 | 8 |
|------------|----|----|----|-------|----|---|---|
| RESERVED_1 |    |    |    | DELAY |    |   |   |
| R          |    |    |    | R     |    |   |   |
| 0h         |    |    |    | 0h    |    |   |   |
| 7          | 6  | 5  | 4  | 3     | 2  | 1 | 0 |
| DELAY      |    |    |    |       |    |   |   |
| R          |    |    |    |       |    |   |   |
| 0h         |    |    |    |       |    |   |   |

**Table 3-624. CMPSSB\_RAMPDLYA Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                          |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                             |
| 12:0  | DELAY      | R    | 0h    | Ramp delay active value. Latched value of the number of cycles to delay the start of the ramp generator decrementer after a EPWMSYNCPER is received. |

### 3.4.2.16 CMPSSB\_RAMPDLYS Register

#### 1 CMPSSB\_RAMPDLYS Register (Offset = 2Ah) [reset = 0h]

CMPSS Ramp Delay Shadow Register.

Return to [Summary Table](#)

**Table 3-625. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSB0       | 5022 002Ah       |
| CMPSSB1       | 5022 102Ah       |
| CMPSSB2       | 5022 202Ah       |
| CMPSSB3       | 5022 302Ah       |
| CMPSSB4       | 5022 402Ah       |
| CMPSSB5       | 5022 502Ah       |
| CMPSSB6       | 5022 602Ah       |
| CMPSSB7       | 5022 702Ah       |
| CMPSSB8       | 5022 802Ah       |
| CMPSSB9       | 5022 902Ah       |

**Figure 3-205. CMPSSB\_RAMPDLYS Name Register**

|            |    |    |    |       |    |   |   |
|------------|----|----|----|-------|----|---|---|
| 15         | 14 | 13 | 12 | 11    | 10 | 9 | 8 |
| RESERVED_1 |    |    |    | DELAY |    |   |   |
| R          |    |    |    | R/W   |    |   |   |
| 0h         |    |    |    | 0h    |    |   |   |
| 7          | 6  | 5  | 4  | 3     | 2  | 1 | 0 |
| DELAY      |    |    |    |       |    |   |   |
| R/W        |    |    |    |       |    |   |   |
| 0h         |    |    |    |       |    |   |   |

**Table 3-627. CMPSSB\_RAMPDLYS Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                          |
|-------|------------|------|-------|----------------------------------------------------------------------|
| 15:13 | RESERVED_1 | R    | 0h    | Reserved                                                             |
| 12:0  | DELAY      | R/W  | 0h    | Ramp delay shadow value. Unlatched value to be loaded into RAMPDLYA. |

### 3.4.2.17 CMPSSB\_CTRIPLFILCTL Register

#### 1 CMPSSB\_CTRIPLFILCTL Register (Offset = 2Ch) [reset = 0h]

CTRIPL Filter Control Register.

Return to [Summary Table](#)

**Table 3-628. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSB0       | 5022 002Ch       |
| CMPSSB1       | 5022 102Ch       |
| CMPSSB2       | 5022 202Ch       |
| CMPSSB3       | 5022 302Ch       |
| CMPSSB4       | 5022 402Ch       |
| CMPSSB5       | 5022 502Ch       |
| CMPSSB6       | 5022 602Ch       |
| CMPSSB7       | 5022 702Ch       |
| CMPSSB8       | 5022 802Ch       |
| CMPSSB9       | 5022 902Ch       |

**Figure 3-206. CMPSSB\_CTRIPLFILCTL Name Register**

| 15      | 14         | 13     | 12 | 11         | 10 | 9 | 8       |
|---------|------------|--------|----|------------|----|---|---------|
| FILINIT | RESERVED_2 | THRESH |    |            |    |   | SAMPWIN |
| R/W1TS  | R          | R/W    |    |            |    |   | R/W     |
| 0h      | 0h         | 0h     |    |            |    |   | 0h      |
| 7       | 6          | 5      | 4  | 3          | 2  | 1 | 0       |
| SAMPWIN |            |        |    | RESERVED_1 |    |   |         |
| R/W     |            |        |    | R          |    |   |         |
| 0h      |            |        |    | 0h         |    |   |         |

**Table 3-630. CMPSSB\_CTRIPLFILCTL Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                                                   |
|------|------------|--------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | FILINIT    | R/W1TS | 0h    | Low filter initialization.<br>0 No effect<br>1 Initialize all samples to the filter input value                                                                                               |
| 14   | RESERVED_2 | R      | 0h    | Reserved                                                                                                                                                                                      |
| 13:9 | THRESH     | R/W    | 0h    | Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Threshold used is THRESH+1. |
| 8:4  | SAMPWIN    | R/W    | 0h    | Low filter sample window size. Number of samples to monitor is SAMPWIN+1.                                                                                                                     |
| 3:0  | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                      |

### 3.4.2.18 CMPSSB\_CTRIPLFILCLKCTL Register

#### 1 CMPSSB\_CTRIPLFILCLKCTL Register (Offset = 2Eh) [reset = 0h]

CTRIPL Filter Clock Control Register.

Return to [Summary Table](#)

**Table 3-631. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSB0       | 5022 002Eh       |
| CMPSSB1       | 5022 102Eh       |
| CMPSSB2       | 5022 202Eh       |
| CMPSSB3       | 5022 302Eh       |
| CMPSSB4       | 5022 402Eh       |
| CMPSSB5       | 5022 502Eh       |
| CMPSSB6       | 5022 602Eh       |
| CMPSSB7       | 5022 702Eh       |
| CMPSSB8       | 5022 802Eh       |
| CMPSSB9       | 5022 902Eh       |

**Figure 3-207. CMPSSB\_CTRIPLFILCLKCTL Name Register**

|             |    |    |    |    |    |   |   |
|-------------|----|----|----|----|----|---|---|
| 15          | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CLKPRESCALE |    |    |    |    |    |   |   |
| R/W         |    |    |    |    |    |   |   |
| 0h          |    |    |    |    |    |   |   |
| 7           | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| CLKPRESCALE |    |    |    |    |    |   |   |
| R/W         |    |    |    |    |    |   |   |
| 0h          |    |    |    |    |    |   |   |

**Table 3-633. CMPSSB\_CTRIPLFILCLKCTL Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                 |
|------|-------------|------|-------|---------------------------------------------------------------------------------------------|
| 15:0 | CLKPRESCALE | R/W  | 0h    | Low filter sample clock prescale. Number of system clocks between samples is CLKPRESCALE+1. |

### 3.4.2.19 CMPSSB\_CTRIPHFILCTL Register

#### 1 CMPSSB\_CTRIPHFILCTL Register (Offset = 30h) [reset = 0h]

CTRIPH Filter Control Register.

Return to [Summary Table](#)

**Table 3-634. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSB0       | 5022 0030h       |
| CMPSSB1       | 5022 1030h       |
| CMPSSB2       | 5022 2030h       |
| CMPSSB3       | 5022 3030h       |
| CMPSSB4       | 5022 4030h       |
| CMPSSB5       | 5022 5030h       |
| CMPSSB6       | 5022 6030h       |
| CMPSSB7       | 5022 7030h       |
| CMPSSB8       | 5022 8030h       |
| CMPSSB9       | 5022 9030h       |

**Figure 3-208. CMPSSB\_CTRIPHFILCTL Name Register**

| 15      | 14         | 13     | 12 | 11         | 10 | 9 | 8       |
|---------|------------|--------|----|------------|----|---|---------|
| FILINIT | RESERVED_2 | THRESH |    |            |    |   | SAMPWIN |
| R/W1TS  | R          | R/W    |    |            |    |   | R/W     |
| 0h      | 0h         | 0h     |    |            |    |   | 0h      |
| 7       | 6          | 5      | 4  | 3          | 2  | 1 | 0       |
| SAMPWIN |            |        |    | RESERVED_1 |    |   |         |
| R/W     |            |        |    | R          |    |   |         |
| 0h      |            |        |    | 0h         |    |   |         |

**Table 3-636. CMPSSB\_CTRIPHFILCTL Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                                                    |
|------|------------|--------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | FILINIT    | R/W1TS | 0h    | High filter initialization.<br>0 No effect<br>1 Initialize all samples to the filter input value                                                                                               |
| 14   | RESERVED_2 | R      | 0h    | Reserved                                                                                                                                                                                       |
| 13:9 | THRESH     | R/W    | 0h    | High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. Threshold used is THRESH+1. |
| 8:4  | SAMPWIN    | R/W    | 0h    | High filter sample window size. Number of samples to monitor is SAMPWIN+1.                                                                                                                     |
| 3:0  | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                       |

### 3.4.2.20 CMPSSB\_CTRIPHFILCLKCTL Register

#### 1 CMPSSB\_CTRIPHFILCLKCTL Register (Offset = 32h) [reset = 0h]

CTRIPH Filter Clock Control Register.

Return to [Summary Table](#)

**Table 3-637. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSB0       | 5022 0032h       |
| CMPSSB1       | 5022 1032h       |
| CMPSSB2       | 5022 2032h       |
| CMPSSB3       | 5022 3032h       |
| CMPSSB4       | 5022 4032h       |
| CMPSSB5       | 5022 5032h       |
| CMPSSB6       | 5022 6032h       |
| CMPSSB7       | 5022 7032h       |
| CMPSSB8       | 5022 8032h       |
| CMPSSB9       | 5022 9032h       |

**Figure 3-209. CMPSSB\_CTRIPHFILCLKCTL Name Register**

|             |    |    |    |    |    |   |   |
|-------------|----|----|----|----|----|---|---|
| 15          | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CLKPRESCALE |    |    |    |    |    |   |   |
| R/W         |    |    |    |    |    |   |   |
| 0h          |    |    |    |    |    |   |   |
| 7           | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| CLKPRESCALE |    |    |    |    |    |   |   |
| R/W         |    |    |    |    |    |   |   |
| 0h          |    |    |    |    |    |   |   |

**Table 3-639. CMPSSB\_CTRIPHFILCLKCTL Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                  |
|------|-------------|------|-------|----------------------------------------------------------------------------------------------|
| 15:0 | CLKPRESCALE | R/W  | 0h    | High filter sample clock prescale. Number of system clocks between samples is CLKPRESCALE+1. |



### 3.4.2.21 CMPSSB\_COMPLOCK Register

#### 1 CMPSSB\_COMPLOCK Register (Offset = 34h) [reset = 0h]

CMPSS Lock Register.

Return to [Summary Table](#)

**Table 3-640. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSB0       | 5022 0034h       |
| CMPSSB1       | 5022 1034h       |
| CMPSSB2       | 5022 2034h       |
| CMPSSB3       | 5022 3034h       |
| CMPSSB4       | 5022 4034h       |
| CMPSSB5       | 5022 5034h       |
| CMPSSB6       | 5022 6034h       |
| CMPSSB7       | 5022 7034h       |
| CMPSSB8       | 5022 8034h       |
| CMPSSB9       | 5022 9034h       |

**Figure 3-210. CMPSSB\_COMPLOCK Name Register**

|            |    |    |        |        |        |             |         |
|------------|----|----|--------|--------|--------|-------------|---------|
| 15         | 14 | 13 | 12     | 11     | 10     | 9           | 8       |
| RESERVED_1 |    |    |        |        |        |             |         |
| R          |    |    |        |        |        |             |         |
| 0h         |    |    |        |        |        |             |         |
| 7          | 6  | 5  | 4      | 3      | 2      | 1           | 0       |
| RESERVED_1 |    |    | TEST   | CTRIIP | DACCTL | COMPHYSCCTL | COMPCTL |
| R          |    |    | R/W1TS | R/W1TS | R/W1TS | R/W1TS      | R/W1TS  |
| 0h         |    |    | 0h     | 0h     | 0h     | 0h          | 0h      |

**Table 3-642. CMPSSB\_COMPLOCK Register Field Descriptions**

| Bit  | Field       | Type   | Reset | Description                                                                                                                                                                                                                                                                       |
|------|-------------|--------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:5 | RESERVED_1  | R      | 0h    | Reserved                                                                                                                                                                                                                                                                          |
| 4    | TEST        | R/W1TS | 0h    | TEST Lock. This bit, when set, will prevent any further writes to the any undocumented registers that may effect the performance/ behavior of this block. Once set this bit can only be cleared by a reset.                                                                       |
| 3    | CTRIIP      | R/W1TS | 0h    | Lock write-access to the CTRIIPxFILCTL and CTRIIPxFILCLKCTL registers.<br>0 CTRIIPxFILCTL and CTRIIPxFILCLKCTL registers are not locked. Write 0 to this bit has no effect.<br>1 CTRIIPxFILCTL and CTRIIPxFILCLKCTL registers are locked. Only a system reset can clear this bit. |
| 2    | DACCTL      | R/W1TS | 0h    | Lock write-access to the DACCTL register.<br>0 DACCTL register is not locked. Write 0 to this bit has no effect.<br>1 DACCTL register is locked. Only a system reset can clear this bit.                                                                                          |
| 1    | COMPHYSCCTL | R/W1TS | 0h    | Lock write-access to the COMPHYSCCTL register.<br>0 COMPHYSCCTL register is not locked. Write 0 to this bit has no effect.<br>1 COMPHYSCCTL register is locked. Only a system reset can clear this bit.                                                                           |

**Table 3-642. CMPSSB\_COMPLOCK Register Field Descriptions (continued)**

| Bit | Field   | Type   | Reset | Description                                                                                                                                                                                 |
|-----|---------|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | COMPCTL | R/W1TS | 0h    | Lock write-access to the COMPCTL register.<br>0 COMPCTL register is not locked. Write 0 to this bit has no effect.<br>1 COMPCTL register is locked. Only a system reset can clear this bit. |

### 3.4.2.22 CMPSSB\_DACHVALS2 Register

#### 1 CMPSSB\_DACHVALS2 Register (Offset = 38h) [reset = 0h]

CMPSS High DAC Value Shadow Register 2

Return to [Summary Table](#)

**Table 3-643. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSB0       | 5022 0038h       |
| CMPSSB1       | 5022 1038h       |
| CMPSSB2       | 5022 2038h       |
| CMPSSB3       | 5022 3038h       |
| CMPSSB4       | 5022 4038h       |
| CMPSSB5       | 5022 5038h       |
| CMPSSB6       | 5022 6038h       |
| CMPSSB7       | 5022 7038h       |
| CMPSSB8       | 5022 8038h       |
| CMPSSB9       | 5022 9038h       |

**Figure 3-211. CMPSSB\_DACHVALS2 Name Register**

|            |    |    |    |        |    |   |   |
|------------|----|----|----|--------|----|---|---|
| 15         | 14 | 13 | 12 | 11     | 10 | 9 | 8 |
| RESERVED_1 |    |    |    | DACVAL |    |   |   |
| R          |    |    |    | R/W    |    |   |   |
| 0h         |    |    |    | 0h     |    |   |   |
| 7          | 6  | 5  | 4  | 3      | 2  | 1 | 0 |
| DACVAL     |    |    |    |        |    |   |   |
| R/W        |    |    |    |        |    |   |   |
| 0h         |    |    |    |        |    |   |   |

**Table 3-645. CMPSSB\_DACHVALS2 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                    |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                       |
| 11:0  | DACVAL     | R/W  | 0h    | High DAC shadow register2 value. When COMPDACCTL[DACSOURCE]=0, the value of DACHVALS2 is loaded into DACHVALA when DE mode is enabled and selected DEACTIVE input is asserted. |

### 3.4.2.23 CMPSSB\_DACLVALS2 Register

#### 1 CMPSSB\_DACLVALS2 Register (Offset = 3Ah) [reset = 0h]

CMPSS Low DAC Value Shadow Register 2

Return to [Summary Table](#)

**Table 3-646. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSB0       | 5022 003Ah       |
| CMPSSB1       | 5022 103Ah       |
| CMPSSB2       | 5022 203Ah       |
| CMPSSB3       | 5022 303Ah       |
| CMPSSB4       | 5022 403Ah       |
| CMPSSB5       | 5022 503Ah       |
| CMPSSB6       | 5022 603Ah       |
| CMPSSB7       | 5022 703Ah       |
| CMPSSB8       | 5022 803Ah       |
| CMPSSB9       | 5022 903Ah       |

**Figure 3-212. CMPSSB\_DACLVALS2 Name Register**

|            |    |    |    |        |    |   |   |
|------------|----|----|----|--------|----|---|---|
| 15         | 14 | 13 | 12 | 11     | 10 | 9 | 8 |
| RESERVED_1 |    |    |    | DACVAL |    |   |   |
| R          |    |    |    | R/W    |    |   |   |
| 0h         |    |    |    | 0h     |    |   |   |
| 7          | 6  | 5  | 4  | 3      | 2  | 1 | 0 |
| DACVAL     |    |    |    |        |    |   |   |
| R/W        |    |    |    |        |    |   |   |
| 0h         |    |    |    |        |    |   |   |

**Table 3-648. CMPSSB\_DACLVALS2 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                 |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                    |
| 11:0  | DACVAL     | R/W  | 0h    | Low DAC shadow register2 value. Value of DACHVALS2 is loaded into DACHVALA when DE mode is enabled and selected DEACTIVE input is asserted. |

### 3.4.2.24 CMPSSB\_CONFIG1 Register

#### 1 CMPSSB\_CONFIG1 Register (Offset = 3Ch) [reset = 0h]

CMPSS Config1 Register.

Return to [Summary Table](#)

**Table 3-649. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CMPSSB0       | 5022 003Ch       |
| CMPSSB1       | 5022 103Ch       |
| CMPSSB2       | 5022 203Ch       |
| CMPSSB3       | 5022 303Ch       |
| CMPSSB4       | 5022 403Ch       |
| CMPSSB5       | 5022 503Ch       |
| CMPSSB6       | 5022 603Ch       |
| CMPSSB7       | 5022 703Ch       |
| CMPSSB8       | 5022 803Ch       |
| CMPSSB9       | 5022 903Ch       |

**Figure 3-213. CMPSSB\_CONFIG1 Name Register**

|          |    |    |    |          |    |   |   |
|----------|----|----|----|----------|----|---|---|
| 15       | 14 | 13 | 12 | 11       | 10 | 9 | 8 |
| SPARE    |    |    |    |          |    |   |   |
| R/W      |    |    |    |          |    |   |   |
| 0h       |    |    |    |          |    |   |   |
| 7        | 6  | 5  | 4  | 3        | 2  | 1 | 0 |
| COMPLHYS |    |    |    | COMPHHYS |    |   |   |
| R/W      |    |    |    | R/W      |    |   |   |
| 0h       |    |    |    | 0h       |    |   |   |

**Table 3-651. CMPSSB\_CONFIG1 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                       |
|------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | SPARE    | R/W  | 0h    | SPARE                                                                                                                                                                                                                                                                                                                                                                             |
| 7:4  | COMPLHYS | R/W  | 0h    | CompL Hysteresis<br>COMPLHYS[3] : reserved<br>COMPLHYS[2] : Controls which comparator output value hysteresis is applied to.<br>1'b0 : Hysteresis is applied when the comparator output is 1'b1<br>1'b1 : Hysteresis is applied when the comparator output is 1'b0<br>COMPLHYS[1:0] = hysteresis value<br>2'b00 : 0 LSB<br>2'b01 : 17.5 LSB<br>2'b10 : 35 LSB<br>2'b11 : 52.5 LSB |
| 3:0  | COMPHHYS | R/W  | 0h    | CompH Hysteresis<br>COMPHHYS[3] : reserved<br>COMPHHYS[2] : Controls which comparator output value hysteresis is applied to.<br>1'b0 : Hysteresis is applied when the comparator output is 1'b1<br>1'b1 : Hysteresis is applied when the comparator output is 1'b0<br>COMPHHYS[1:0] = hysteresis value<br>2'b00 : 0 LSB<br>2'b01 : 17.5 LSB<br>2'b10 : 35 LSB<br>2'b11 : 52.5 LSB |

## 3.5 DAC

### DAC

#### 3.5.1 DAC Summaries

#### DAC Summaries

**Table 3-652. DAC Registers, Base Address=5026 0000h, Length=4096**

| Offset | Length | Register Name                    | DAC0 Physical Address |
|--------|--------|----------------------------------|-----------------------|
| 0h     | 16     | <a href="#">DAC_DACREV</a>       | 5026 0000h            |
| 2h     | 16     | <a href="#">DAC_DACCTL_ALT2_</a> | 5026 0002h            |
| 4h     | 16     | <a href="#">DAC_DACVALA</a>      | 5026 0004h            |
| 6h     | 16     | <a href="#">DAC_DACVALS</a>      | 5026 0006h            |
| 8h     | 16     | <a href="#">DAC_DACOUTEN</a>     | 5026 0008h            |
| Ah     | 16     | <a href="#">DAC_DACLOCK</a>      | 5026 000Ah            |
| Eh     | 16     | <a href="#">DAC_DACCONFIG</a>    | 5026 000Eh            |

#### 3.5.2 DAC Registers

#### DAC Registers

### 3.5.2.1 DAC\_DACREV Register

#### 1 DAC\_DACREV Register (Offset = 0h) [reset = 0h]

DAC Revision Register.

Return to [Summary Table](#)

**Table 3-653. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| DAC0          | 5026 0000h       |

**Figure 3-214. DAC\_DACREV Name Register**

|            |    |    |    |    |    |   |   |
|------------|----|----|----|----|----|---|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED_1 |    |    |    |    |    |   |   |
| R          |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| REV        |    |    |    |    |    |   |   |
| R          |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |

**Table 3-655. DAC\_DACREV Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description  |
|------|------------|------|-------|--------------|
| 15:8 | RESERVED_1 | R    | 0h    | Reserved     |
| 7:0  | REV        | R    | 0h    | DAC Revision |

### 3.5.2.2 DAC\_DACCTL\_ALT2\_ Register

#### 1 DAC\_DACCTL\_ALT2\_ Register (Offset = 2h) [reset = 0h]

DAC Control Register.

Return to [Summary Table](#)

**Table 3-656. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| DAC0          | 5026 0002h       |

**Figure 3-215. DAC\_DACCTL\_ALT2\_ Name Register**

| 15         | 14 | 13 | 12 | 11         | 10       | 9    | 8         |
|------------|----|----|----|------------|----------|------|-----------|
| RESERVED_2 |    |    |    |            |          |      | SYNCSEL   |
| R          |    |    |    |            |          |      | R/W       |
| 0h         |    |    |    |            |          |      | 0h        |
| 7          | 6  | 5  | 4  | 3          | 2        | 1    | 0         |
| SYNCSEL    |    |    |    | RESERVED_1 | LOADMODE | MODE | DACREFSEL |
| R/W        |    |    |    | R          | R/W      | R/W  | R/W       |
| 0h         |    |    |    | 0h         | 0h       | 0h   | 0h        |

**Table 3-658. DAC\_DACCTL\_ALT2\_ Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                             |
|------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:9 | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                |
| 8:4  | SYNCSEL    | R/W  | 0h    | DAC EPWMSYNCPER select. Determines which EPWMSYNCPER signal will update the DACVALA register.<br>Where n represents the maximum number of EPWMSYNCPER signals available on the device:<br>0 EPWM1SYNCPER<br>1 EPWM2SYNCPER<br>2 EPWM3SYNCPER<br>...<br>n-1 EPWMnSYNCPER |
| 3    | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                |
| 2    | LOADMODE   | R/W  | 0h    | DACVALA load mode. Determines when the DACVALA register is updated with the value from DACVALS.<br>0 Load on next SYSCLK<br>1 Load on next EPWMSYNCPER specified by SYNCSEL                                                                                             |
| 1    | MODE       | R/W  | 0h    | DAC gain mode select. Selects the gain mode for the buffered output. The MODE value is only used when DACREFSEL=1 and internal ADC reference mode is selected.<br>0 Gain is 1<br>1 Gain is 2                                                                            |
| 0    | DACREFSEL  | R/W  | 0h    | DAC reference select. Selects which voltage references are used by the DAC.<br>0 VDAC/VSSA are the reference voltages<br>1 ADC VREFHI/VSSA are the reference voltages                                                                                                   |



### 3.5.2.3 DAC\_DACVALA Register

#### 1 DAC\_DACVALA Register (Offset = 4h) [reset = 0h]

DAC Value Register - Active.

Return to [Summary Table](#)

**Table 3-659. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| DAC0          | 5026 0004h       |

**Figure 3-216. DAC\_DACVALA Name Register**

|            |    |    |    |         |    |   |   |
|------------|----|----|----|---------|----|---|---|
| 15         | 14 | 13 | 12 | 11      | 10 | 9 | 8 |
| RESERVED_1 |    |    |    | DACVALA |    |   |   |
| R          |    |    |    | R       |    |   |   |
| 0h         |    |    |    | 0h      |    |   |   |
| 7          | 6  | 5  | 4  | 3       | 2  | 1 | 0 |
| DACVALA    |    |    |    |         |    |   |   |
| R          |    |    |    |         |    |   |   |
| 0h         |    |    |    |         |    |   |   |

**Table 3-661. DAC\_DACVALA Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                    |
|-------|------------|------|-------|------------------------------------------------|
| 15:12 | RESERVED_1 | R    | 0h    | Reserved                                       |
| 11:0  | DACVALA    | R    | 0h    | Active output code currently driven by the DAC |

### 3.5.2.4 DAC\_DACVALS Register

#### 1 DAC\_DACVALS Register (Offset = 6h) [reset = 0h]

DAC Value Register - Shadow.

Return to [Summary Table](#)

**Table 3-662. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| DAC0          | 5026 0006h       |

**Figure 3-217. DAC\_DACVALS Name Register**

| 15         | 14 | 13 | 12 | 11      | 10 | 9 | 8 |
|------------|----|----|----|---------|----|---|---|
| RESERVED_1 |    |    |    | DACVALS |    |   |   |
| R          |    |    |    | R/W     |    |   |   |
| 0h         |    |    |    | 0h      |    |   |   |
| 7          | 6  | 5  | 4  | 3       | 2  | 1 | 0 |
| DACVALS    |    |    |    |         |    |   |   |
| R/W        |    |    |    |         |    |   |   |
| 0h         |    |    |    |         |    |   |   |

**Table 3-664. DAC\_DACVALS Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                  |
|-------|------------|------|-------|----------------------------------------------|
| 15:12 | RESERVED_1 | R    | 0h    | Reserved                                     |
| 11:0  | DACVALS    | R/W  | 0h    | Shadow output code to be loaded into DACVALA |

### 3.5.2.5 DAC\_DACOUTEN Register

#### 1 DAC\_DACOUTEN Register (Offset = 8h) [reset = 0h]

DAC Output Enable Register.

Return to [Summary Table](#)

**Table 3-665. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| DAC0          | 5026 0008h       |

**Figure 3-218. DAC\_DACOUTEN Name Register**

|            |    |    |    |    |    |   |          |
|------------|----|----|----|----|----|---|----------|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8        |
| RESERVED_1 |    |    |    |    |    |   |          |
| R          |    |    |    |    |    |   |          |
| 0h         |    |    |    |    |    |   |          |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0        |
| RESERVED_1 |    |    |    |    |    |   | DACOUTEN |
| R          |    |    |    |    |    |   | R/W      |
| 0h         |    |    |    |    |    |   | 0h       |

**Table 3-667. DAC\_DACOUTEN Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                              |
|------|------------|------|-------|--------------------------------------------------------------------------|
| 15:1 | RESERVED_1 | R    | 0h    | Reserved                                                                 |
| 0    | DACOUTEN   | R/W  | 0h    | DAC output enable<br>0 DAC output is disabled<br>1 DAC output is enabled |

### 3.5.2.6 DAC\_DACLOCK Register

#### 1 DAC\_DACLOCK Register (Offset = Ah) [reset = 0h]

DAC Lock Register.

Return to [Summary Table](#)

**Table 3-668. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| DAC0          | 5026 000Ah       |

**Figure 3-219. DAC\_DACLOCK Name Register**

| 15         | 14 | 13 | 12 | 11         | 10     | 9      | 8 |
|------------|----|----|----|------------|--------|--------|---|
| KEY        |    |    |    | RESERVED_1 |        |        |   |
| R/W        |    |    |    | R          |        |        |   |
| 0h         |    |    |    | 0h         |        |        |   |
| 7          | 6  | 5  | 4  | 3          | 2      | 1      | 0 |
| RESERVED_1 |    |    |    | DACOUTEN   | DACVAL | DACCTL |   |
| R          |    |    |    | R/W1TS     | R/W1TS | R/W1TS |   |
| 0h         |    |    |    | 0h         | 0h     | 0h     |   |

**Table 3-670. DAC\_DACLOCK Register Field Descriptions**

| Bit   | Field      | Type   | Reset | Description                                                                                                                                                                                                               |
|-------|------------|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | KEY        | R/W    | 0h    | Writes to this register succeed only if this field is written with a value of 0xA.<br>Only 16-bit writes will succeed [provided the KEY matches]. Read-modify-writes to individual bits in this register will be ignored. |
| 11:3  | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                                                  |
| 2     | DACOUTEN   | R/W1TS | 0h    | Lock write-access to the DACOUTEN register.<br>0 DACOUTEN register is not locked. Write 0 to this bit has no effect.<br>1 DACOUTEN register is locked. Only a system reset can clear this bit.                            |
| 1     | DACVAL     | R/W1TS | 0h    | Lock write-access to the DACVALS register.<br>0 DACVALS register is not locked. Write 0 to this bit has no effect.<br>1 DACVALS register is locked. Only a system reset can clear this bit.                               |
| 0     | DACCTL     | R/W1TS | 0h    | Lock write-access to the DACCTL register.<br>0 DACCTL register is not locked. Write 0 to this bit has no effect.<br>1 DACCTL register is locked. Only a system reset can clear this bit.                                  |

### 3.5.2.7 DAC\_DACCONFIG Register

#### 1 DAC\_DACCONFIG Register (Offset = Eh) [reset = 0h]

DAC Configuration Register.

Return to [Summary Table](#)

**Table 3-671. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| DAC0          | 5026 000Eh       |

**Figure 3-220. DAC\_DACCONFIG Name Register**

|        |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CONFIG |    |    |    |    |    |   |   |
| R/W    |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |
| 7      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| CONFIG |    |    |    |    |    |   |   |
| R/W    |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |

**Table 3-673. DAC\_DACCONFIG Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                  |
|------|--------|------|-------|------------------------------------------------------------------------------|
| 15:0 | CONFIG | R/W  | 0h    | DAC Configuration. This bit field is used for TI internal testing/debugging. |

## 3.6 ECAP

### ECAP

#### 3.6.1 ECAP Summaries

#### ECAP Summaries

**Table 3-674. ECAP Registers, Base Address=5024 0000h, Length=4096**

| Offset | Length | Register Name                                | ECAP0 Physical Address | ECAP1 Physical Address | ECAP2 Physical Address |
|--------|--------|----------------------------------------------|------------------------|------------------------|------------------------|
| 0h     | 32     | <a href="#">ECAP_TSCTR</a>                   | 5024 0000h             | 5024 1000h             | 5024 2000h             |
| 4h     | 32     | <a href="#">ECAP_CTRPHS</a>                  | 5024 0004h             | 5024 1004h             | 5024 2004h             |
| 8h     | 32     | <a href="#">ECAP_CAP1</a>                    | 5024 0008h             | 5024 1008h             | 5024 2008h             |
| Ch     | 32     | <a href="#">ECAP_CAP2</a>                    | 5024 000Ch             | 5024 100Ch             | 5024 200Ch             |
| 10h    | 32     | <a href="#">ECAP_CAP3</a>                    | 5024 0010h             | 5024 1010h             | 5024 2010h             |
| 14h    | 32     | <a href="#">ECAP_CAP4</a>                    | 5024 0014h             | 5024 1014h             | 5024 2014h             |
| 24h    | 32     | <a href="#">ECAP_ECCTL0</a>                  | 5024 0024h             | 5024 1024h             | 5024 2024h             |
| 28h    | 16     | <a href="#">ECAP_ECCTL1</a>                  | 5024 0028h             | 5024 1028h             | 5024 2028h             |
| 2Ah    | 16     | <a href="#">ECAP_ECCTL2</a>                  | 5024 002Ah             | 5024 102Ah             | 5024 202Ah             |
| 2Ch    | 16     | <a href="#">ECAP_ECEINT</a>                  | 5024 002Ch             | 5024 102Ch             | 5024 202Ch             |
| 2Eh    | 16     | <a href="#">ECAP_ECFLG</a>                   | 5024 002Eh             | 5024 102Eh             | 5024 202Eh             |
| 30h    | 16     | <a href="#">ECAP_ECCLR</a>                   | 5024 0030h             | 5024 1030h             | 5024 2030h             |
| 32h    | 16     | <a href="#">ECAP_ECFRC</a>                   | 5024 0032h             | 5024 1032h             | 5024 2032h             |
| 3Ch    | 32     | <a href="#">ECAP_ECAPSYNCINSEL</a>           | 5024 003Ch             | 5024 103Ch             | 5024 203Ch             |
| 80h    | 32     | <a href="#">ECAP_MUNIT_COMMON_CTL</a>        | 5024 0080h             | 5024 1080h             | 5024 2080h             |
| C0h    | 32     | <a href="#">ECAP_MUNIT_1_CTL</a>             | 5024 00C0h             | 5024 10C0h             | 5024 20C0h             |
| C4h    | 32     | <a href="#">ECAP_MUNIT_1_SHADOW_CTL</a>      | 5024 00C4h             | 5024 10C4h             | 5024 20C4h             |
| D0h    | 32     | <a href="#">ECAP_MUNIT_1_MIN</a>             | 5024 00D0h             | 5024 10D0h             | 5024 20D0h             |
| D4h    | 32     | <a href="#">ECAP_MUNIT_1_MAX</a>             | 5024 00D4h             | 5024 10D4h             | 5024 20D4h             |
| D8h    | 32     | <a href="#">ECAP_MUNIT_1_MIN_SHADOW</a>      | 5024 00D8h             | 5024 10D8h             | 5024 20D8h             |
| DCh    | 32     | <a href="#">ECAP_MUNIT_1_MAX_SHADOW</a>      | 5024 00DCh             | 5024 10DCh             | 5024 20DCh             |
| E0h    | 32     | <a href="#">ECAP_MUNIT_1_DEBUG_RANGE_MIN</a> | 5024 00E0h             | 5024 10E0h             | 5024 20E0h             |
| E4h    | 32     | <a href="#">ECAP_MUNIT_1_DEBUG_RANGE_MAX</a> | 5024 00E4h             | 5024 10E4h             | 5024 20E4h             |
| 100h   | 32     | <a href="#">ECAP_MUNIT_2_CTL</a>             | 5024 0100h             | 5024 1100h             | 5024 2100h             |
| 104h   | 32     | <a href="#">ECAP_MUNIT_2_SHADOW_CTL</a>      | 5024 0104h             | 5024 1104h             | 5024 2104h             |
| 110h   | 32     | <a href="#">ECAP_MUNIT_2_MIN</a>             | 5024 0110h             | 5024 1110h             | 5024 2110h             |
| 114h   | 32     | <a href="#">ECAP_MUNIT_2_MAX</a>             | 5024 0114h             | 5024 1114h             | 5024 2114h             |
| 118h   | 32     | <a href="#">ECAP_MUNIT_2_MIN_SHADOW</a>      | 5024 0118h             | 5024 1118h             | 5024 2118h             |
| 11Ch   | 32     | <a href="#">ECAP_MUNIT_2_MAX_SHADOW</a>      | 5024 011Ch             | 5024 111Ch             | 5024 211Ch             |
| 120h   | 32     | <a href="#">ECAP_MUNIT_2_DEBUG_RANGE_MIN</a> | 5024 0120h             | 5024 1120h             | 5024 2120h             |
| 124h   | 32     | <a href="#">ECAP_MUNIT_2_DEBUG_RANGE_MAX</a> | 5024 0124h             | 5024 1124h             | 5024 2124h             |

**Table 3-675. ECAP Registers, Base Address=5024 0000h, Length=4096**

| Offset | Length | Register Name                                | ECAP3 Physical Address | ECAP4 Physical Address | ECAP5 Physical Address |
|--------|--------|----------------------------------------------|------------------------|------------------------|------------------------|
| 0h     | 32     | <a href="#">ECAP_TSCTR</a>                   | 5024 3000h             | 5024 4000h             | 5024 5000h             |
| 4h     | 32     | <a href="#">ECAP_CTRPHS</a>                  | 5024 3004h             | 5024 4004h             | 5024 5004h             |
| 8h     | 32     | <a href="#">ECAP_CAP1</a>                    | 5024 3008h             | 5024 4008h             | 5024 5008h             |
| Ch     | 32     | <a href="#">ECAP_CAP2</a>                    | 5024 300Ch             | 5024 400Ch             | 5024 500Ch             |
| 10h    | 32     | <a href="#">ECAP_CAP3</a>                    | 5024 3010h             | 5024 4010h             | 5024 5010h             |
| 14h    | 32     | <a href="#">ECAP_CAP4</a>                    | 5024 3014h             | 5024 4014h             | 5024 5014h             |
| 24h    | 32     | <a href="#">ECAP_ECCTL0</a>                  | 5024 3024h             | 5024 4024h             | 5024 5024h             |
| 28h    | 16     | <a href="#">ECAP_ECCTL1</a>                  | 5024 3028h             | 5024 4028h             | 5024 5028h             |
| 2Ah    | 16     | <a href="#">ECAP_ECCTL2</a>                  | 5024 302Ah             | 5024 402Ah             | 5024 502Ah             |
| 2Ch    | 16     | <a href="#">ECAP_ECEINT</a>                  | 5024 302Ch             | 5024 402Ch             | 5024 502Ch             |
| 2Eh    | 16     | <a href="#">ECAP_ECFLG</a>                   | 5024 302Eh             | 5024 402Eh             | 5024 502Eh             |
| 30h    | 16     | <a href="#">ECAP_ECCLR</a>                   | 5024 3030h             | 5024 4030h             | 5024 5030h             |
| 32h    | 16     | <a href="#">ECAP_ECFRC</a>                   | 5024 3032h             | 5024 4032h             | 5024 5032h             |
| 3Ch    | 32     | <a href="#">ECAP_ECAPSYNCINSEL</a>           | 5024 303Ch             | 5024 403Ch             | 5024 503Ch             |
| 80h    | 32     | <a href="#">ECAP_MUNIT_COMMON_CTL</a>        | 5024 3080h             | 5024 4080h             | 5024 5080h             |
| C0h    | 32     | <a href="#">ECAP_MUNIT_1_CTL</a>             | 5024 30C0h             | 5024 40C0h             | 5024 50C0h             |
| C4h    | 32     | <a href="#">ECAP_MUNIT_1_SHADOW_CTL</a>      | 5024 30C4h             | 5024 40C4h             | 5024 50C4h             |
| D0h    | 32     | <a href="#">ECAP_MUNIT_1_MIN</a>             | 5024 30D0h             | 5024 40D0h             | 5024 50D0h             |
| D4h    | 32     | <a href="#">ECAP_MUNIT_1_MAX</a>             | 5024 30D4h             | 5024 40D4h             | 5024 50D4h             |
| D8h    | 32     | <a href="#">ECAP_MUNIT_1_MIN_SHADOW</a>      | 5024 30D8h             | 5024 40D8h             | 5024 50D8h             |
| DCh    | 32     | <a href="#">ECAP_MUNIT_1_MAX_SHADOW</a>      | 5024 30DCh             | 5024 40DCh             | 5024 50DCh             |
| E0h    | 32     | <a href="#">ECAP_MUNIT_1_DEBUG_RANGE_MIN</a> | 5024 30E0h             | 5024 40E0h             | 5024 50E0h             |
| E4h    | 32     | <a href="#">ECAP_MUNIT_1_DEBUG_RANGE_MAX</a> | 5024 30E4h             | 5024 40E4h             | 5024 50E4h             |
| 100h   | 32     | <a href="#">ECAP_MUNIT_2_CTL</a>             | 5024 3100h             | 5024 4100h             | 5024 5100h             |
| 104h   | 32     | <a href="#">ECAP_MUNIT_2_SHADOW_CTL</a>      | 5024 3104h             | 5024 4104h             | 5024 5104h             |
| 110h   | 32     | <a href="#">ECAP_MUNIT_2_MIN</a>             | 5024 3110h             | 5024 4110h             | 5024 5110h             |
| 114h   | 32     | <a href="#">ECAP_MUNIT_2_MAX</a>             | 5024 3114h             | 5024 4114h             | 5024 5114h             |
| 118h   | 32     | <a href="#">ECAP_MUNIT_2_MIN_SHADOW</a>      | 5024 3118h             | 5024 4118h             | 5024 5118h             |
| 11Ch   | 32     | <a href="#">ECAP_MUNIT_2_MAX_SHADOW</a>      | 5024 311Ch             | 5024 411Ch             | 5024 511Ch             |
| 120h   | 32     | <a href="#">ECAP_MUNIT_2_DEBUG_RANGE_MIN</a> | 5024 3120h             | 5024 4120h             | 5024 5120h             |
| 124h   | 32     | <a href="#">ECAP_MUNIT_2_DEBUG_RANGE_MAX</a> | 5024 3124h             | 5024 4124h             | 5024 5124h             |

**Table 3-676. ECAP Registers, Base Address=5024 0000h, Length=4096**

| Offset | Length | Register Name               | ECAP6 Physical Address | ECAP7 Physical Address | ECAP8 Physical Address |
|--------|--------|-----------------------------|------------------------|------------------------|------------------------|
| 0h     | 32     | <a href="#">ECAP_TSCTR</a>  | 5024 6000h             | 5024 7000h             | 5024 8000h             |
| 4h     | 32     | <a href="#">ECAP_CTRPHS</a> | 5024 6004h             | 5024 7004h             | 5024 8004h             |
| 8h     | 32     | <a href="#">ECAP_CAP1</a>   | 5024 6008h             | 5024 7008h             | 5024 8008h             |
| Ch     | 32     | <a href="#">ECAP_CAP2</a>   | 5024 600Ch             | 5024 700Ch             | 5024 800Ch             |
| 10h    | 32     | <a href="#">ECAP_CAP3</a>   | 5024 6010h             | 5024 7010h             | 5024 8010h             |
| 14h    | 32     | <a href="#">ECAP_CAP4</a>   | 5024 6014h             | 5024 7014h             | 5024 8014h             |

**Table 3-676. ECAP Registers, Base Address=5024 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                                | ECAP6 Physical Address | ECAP7 Physical Address | ECAP8 Physical Address |
|--------|--------|----------------------------------------------|------------------------|------------------------|------------------------|
| 24h    | 32     | <a href="#">ECAP_ECCTL0</a>                  | 5024 6024h             | 5024 7024h             | 5024 8024h             |
| 28h    | 16     | <a href="#">ECAP_ECCTL1</a>                  | 5024 6028h             | 5024 7028h             | 5024 8028h             |
| 2Ah    | 16     | <a href="#">ECAP_ECCTL2</a>                  | 5024 602Ah             | 5024 702Ah             | 5024 802Ah             |
| 2Ch    | 16     | <a href="#">ECAP_ECEINT</a>                  | 5024 602Ch             | 5024 702Ch             | 5024 802Ch             |
| 2Eh    | 16     | <a href="#">ECAP_ECFLG</a>                   | 5024 602Eh             | 5024 702Eh             | 5024 802Eh             |
| 30h    | 16     | <a href="#">ECAP_ECCLR</a>                   | 5024 6030h             | 5024 7030h             | 5024 8030h             |
| 32h    | 16     | <a href="#">ECAP_ECFRC</a>                   | 5024 6032h             | 5024 7032h             | 5024 8032h             |
| 3Ch    | 32     | <a href="#">ECAP_ECAPSYNCINSEL</a>           | 5024 603Ch             | 5024 703Ch             | 5024 803Ch             |
| 80h    | 32     | <a href="#">ECAP_MUNIT_COMMON_CTL</a>        | 5024 6080h             | 5024 7080h             | 5024 8080h             |
| C0h    | 32     | <a href="#">ECAP_MUNIT_1_CTL</a>             | 5024 60C0h             | 5024 70C0h             | 5024 80C0h             |
| C4h    | 32     | <a href="#">ECAP_MUNIT_1_SHADOW_CTL</a>      | 5024 60C4h             | 5024 70C4h             | 5024 80C4h             |
| D0h    | 32     | <a href="#">ECAP_MUNIT_1_MIN</a>             | 5024 60D0h             | 5024 70D0h             | 5024 80D0h             |
| D4h    | 32     | <a href="#">ECAP_MUNIT_1_MAX</a>             | 5024 60D4h             | 5024 70D4h             | 5024 80D4h             |
| D8h    | 32     | <a href="#">ECAP_MUNIT_1_MIN_SHADOW</a>      | 5024 60D8h             | 5024 70D8h             | 5024 80D8h             |
| DCh    | 32     | <a href="#">ECAP_MUNIT_1_MAX_SHADOW</a>      | 5024 60DCh             | 5024 70DCh             | 5024 80DCh             |
| E0h    | 32     | <a href="#">ECAP_MUNIT_1_DEBUG_RANGE_MIN</a> | 5024 60E0h             | 5024 70E0h             | 5024 80E0h             |
| E4h    | 32     | <a href="#">ECAP_MUNIT_1_DEBUG_RANGE_MAX</a> | 5024 60E4h             | 5024 70E4h             | 5024 80E4h             |
| 100h   | 32     | <a href="#">ECAP_MUNIT_2_CTL</a>             | 5024 6100h             | 5024 7100h             | 5024 8100h             |
| 104h   | 32     | <a href="#">ECAP_MUNIT_2_SHADOW_CTL</a>      | 5024 6104h             | 5024 7104h             | 5024 8104h             |
| 110h   | 32     | <a href="#">ECAP_MUNIT_2_MIN</a>             | 5024 6110h             | 5024 7110h             | 5024 8110h             |
| 114h   | 32     | <a href="#">ECAP_MUNIT_2_MAX</a>             | 5024 6114h             | 5024 7114h             | 5024 8114h             |
| 118h   | 32     | <a href="#">ECAP_MUNIT_2_MIN_SHADOW</a>      | 5024 6118h             | 5024 7118h             | 5024 8118h             |
| 11Ch   | 32     | <a href="#">ECAP_MUNIT_2_MAX_SHADOW</a>      | 5024 611Ch             | 5024 711Ch             | 5024 811Ch             |
| 120h   | 32     | <a href="#">ECAP_MUNIT_2_DEBUG_RANGE_MIN</a> | 5024 6120h             | 5024 7120h             | 5024 8120h             |
| 124h   | 32     | <a href="#">ECAP_MUNIT_2_DEBUG_RANGE_MAX</a> | 5024 6124h             | 5024 7124h             | 5024 8124h             |

**Table 3-677. ECAP Registers, Base Address=5024 0000h, Length=4096**

| Offset | Length | Register Name               | ECAP9 Physical Address |
|--------|--------|-----------------------------|------------------------|
| 0h     | 32     | <a href="#">ECAP_TSCTR</a>  | 5024 9000h             |
| 4h     | 32     | <a href="#">ECAP_CTRPHS</a> | 5024 9004h             |
| 8h     | 32     | <a href="#">ECAP_CAP1</a>   | 5024 9008h             |
| Ch     | 32     | <a href="#">ECAP_CAP2</a>   | 5024 900Ch             |
| 10h    | 32     | <a href="#">ECAP_CAP3</a>   | 5024 9010h             |
| 14h    | 32     | <a href="#">ECAP_CAP4</a>   | 5024 9014h             |
| 24h    | 32     | <a href="#">ECAP_ECCTL0</a> | 5024 9024h             |
| 28h    | 16     | <a href="#">ECAP_ECCTL1</a> | 5024 9028h             |
| 2Ah    | 16     | <a href="#">ECAP_ECCTL2</a> | 5024 902Ah             |
| 2Ch    | 16     | <a href="#">ECAP_ECEINT</a> | 5024 902Ch             |
| 2Eh    | 16     | <a href="#">ECAP_ECFLG</a>  | 5024 902Eh             |
| 30h    | 16     | <a href="#">ECAP_ECCLR</a>  | 5024 9030h             |
| 32h    | 16     | <a href="#">ECAP_ECFRC</a>  | 5024 9032h             |



**Table 3-677. ECAP Registers, Base Address=5024 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                                | ECAP9 Physical Address |
|--------|--------|----------------------------------------------|------------------------|
| 3Ch    | 32     | <a href="#">ECAP_ECAPSYNCINSEL</a>           | 5024 903Ch             |
| 80h    | 32     | <a href="#">ECAP_MUNIT_COMMON_CTL</a>        | 5024 9080h             |
| C0h    | 32     | <a href="#">ECAP_MUNIT_1_CTL</a>             | 5024 90C0h             |
| C4h    | 32     | <a href="#">ECAP_MUNIT_1_SHADOW_CTL</a>      | 5024 90C4h             |
| D0h    | 32     | <a href="#">ECAP_MUNIT_1_MIN</a>             | 5024 90D0h             |
| D4h    | 32     | <a href="#">ECAP_MUNIT_1_MAX</a>             | 5024 90D4h             |
| D8h    | 32     | <a href="#">ECAP_MUNIT_1_MIN_SHADOW</a>      | 5024 90D8h             |
| DCh    | 32     | <a href="#">ECAP_MUNIT_1_MAX_SHADOW</a>      | 5024 90DCh             |
| E0h    | 32     | <a href="#">ECAP_MUNIT_1_DEBUG_RANGE_MIN</a> | 5024 90E0h             |
| E4h    | 32     | <a href="#">ECAP_MUNIT_1_DEBUG_RANGE_MAX</a> | 5024 90E4h             |
| 100h   | 32     | <a href="#">ECAP_MUNIT_2_CTL</a>             | 5024 9100h             |
| 104h   | 32     | <a href="#">ECAP_MUNIT_2_SHADOW_CTL</a>      | 5024 9104h             |
| 110h   | 32     | <a href="#">ECAP_MUNIT_2_MIN</a>             | 5024 9110h             |
| 114h   | 32     | <a href="#">ECAP_MUNIT_2_MAX</a>             | 5024 9114h             |
| 118h   | 32     | <a href="#">ECAP_MUNIT_2_MIN_SHADOW</a>      | 5024 9118h             |
| 11Ch   | 32     | <a href="#">ECAP_MUNIT_2_MAX_SHADOW</a>      | 5024 911Ch             |
| 120h   | 32     | <a href="#">ECAP_MUNIT_2_DEBUG_RANGE_MIN</a> | 5024 9120h             |
| 124h   | 32     | <a href="#">ECAP_MUNIT_2_DEBUG_RANGE_MAX</a> | 5024 9124h             |

### 3.6.2 ECAP Registers

#### ECAP Registers

### 3.6.2.1 ECAP\_TSCTR Register

#### 1 ECAP\_TSCTR Register (Offset = 0h) [reset = 0h]

Time-Stamp Counter.

Return to [Summary Table](#)

**Table 3-678. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 0000h       |
| ECAP1         | 5024 1000h       |
| ECAP2         | 5024 2000h       |
| ECAP3         | 5024 3000h       |
| ECAP4         | 5024 4000h       |
| ECAP5         | 5024 5000h       |
| ECAP6         | 5024 6000h       |
| ECAP7         | 5024 7000h       |
| ECAP8         | 5024 8000h       |
| ECAP9         | 5024 9000h       |

**Figure 3-221. ECAP\_TSCTR Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TSCTR |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TSCTR |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TSCTR |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TSCTR |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 3-680. ECAP\_TSCTR Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                 |
|------|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | TSCTR | R/W  | 0h    | Active 32-bit counter register that is used as the capture time-base HR mode :<br>1] This register reads HRCOUNTER value and is not writable<br>2] can be reset using CTRFILTRESET<br>3] Its not synchronized to SYSCLK domain so reads may not be accurate |

### 3.6.2.2 ECAP\_CTRPHS Register

#### 1 ECAP\_CTRPHS Register (Offset = 4h) [reset = 0h]

Counter Phase Offset Value Register.

Return to [Summary Table](#)

**Table 3-681. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 0004h       |
| ECAP1         | 5024 1004h       |
| ECAP2         | 5024 2004h       |
| ECAP3         | 5024 3004h       |
| ECAP4         | 5024 4004h       |
| ECAP5         | 5024 5004h       |
| ECAP6         | 5024 6004h       |
| ECAP7         | 5024 7004h       |
| ECAP8         | 5024 8004h       |
| ECAP9         | 5024 9004h       |

**Figure 3-222. ECAP\_CTRPHS Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CTRPHS |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CTRPHS |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CTRPHS |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CTRPHS |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 3-683. ECAP\_CTRPHS Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                              |
|------|--------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CTRPHS | R/W  | 0h    | Counter phase value register that can be programmed for phase lag/lead. This register CTRPHS is loaded into TSCTR upon either a SYNCI event or S/W force via a control bit. Used to achieve phase control synchronization with respect to other eCAP and EPWM time-bases.<br>This register is not applicable in HR mode. |

### 3.6.2.3 ECAP\_CAP1 Register

#### 1 ECAP\_CAP1 Register (Offset = 8h) [reset = 0h]

Capture 1 Register.

Return to [Summary Table](#)

**Table 3-684. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 0008h       |
| ECAP1         | 5024 1008h       |
| ECAP2         | 5024 2008h       |
| ECAP3         | 5024 3008h       |
| ECAP4         | 5024 4008h       |
| ECAP5         | 5024 5008h       |
| ECAP6         | 5024 6008h       |
| ECAP7         | 5024 7008h       |
| ECAP8         | 5024 8008h       |
| ECAP9         | 5024 9008h       |

**Figure 3-223. ECAP\_CAP1 Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAP1 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAP1 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAP1 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAP1 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 3-686. ECAP\_CAP1 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                        |
|------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CAP1  | R/W  | 0h    | This register can be loaded (written) by:<br>1. Time-Stamp (counter value) during a capture event.<br>2. Software - may be useful for test purposes/initialization.<br>3. APRD shadow register (ECAP_CAP3) when used in APWM mode. |

### 3.6.2.4 ECAP\_CAP2 Register

#### 1 ECAP\_CAP2 Register (Offset = Ch) [reset = 0h]

Capture 2 Register.

Return to [Summary Table](#)

**Table 3-687. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 000Ch       |
| ECAP1         | 5024 100Ch       |
| ECAP2         | 5024 200Ch       |
| ECAP3         | 5024 300Ch       |
| ECAP4         | 5024 400Ch       |
| ECAP5         | 5024 500Ch       |
| ECAP6         | 5024 600Ch       |
| ECAP7         | 5024 700Ch       |
| ECAP8         | 5024 800Ch       |
| ECAP9         | 5024 900Ch       |

**Figure 3-224. ECAP\_CAP2 Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAP2 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAP2 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAP2 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAP2 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 3-689. ECAP\_CAP2 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                         |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CAP2  | R/W  | 0h    | This register can be loaded (written) by:<br>1. Time-Stamp (counter value) during a capture event.<br>2. Software - may be useful for test purposes.<br>3. ACMP shadow register (ECAP_CAP4) when used in APWM mode. |

### 3.6.2.5 ECAP\_CAP3 Register

#### 1 ECAP\_CAP3 Register (Offset = 10h) [reset = 0h]

Capture 3 Register.

Return to [Summary Table](#)

**Table 3-690. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 0010h       |
| ECAP1         | 5024 1010h       |
| ECAP2         | 5024 2010h       |
| ECAP3         | 5024 3010h       |
| ECAP4         | 5024 4010h       |
| ECAP5         | 5024 5010h       |
| ECAP6         | 5024 6010h       |
| ECAP7         | 5024 7010h       |
| ECAP8         | 5024 8010h       |
| ECAP9         | 5024 9010h       |

**Figure 3-225. ECAP\_CAP3 Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAP3 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAP3 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAP3 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAP3 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 3-692. ECAP\_CAP3 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                         |
|------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CAP3  | R/W  | 0h    | In CMP mode this is a time-stamp capture register.<br>In APMW mode this is the period shadow (APER) register.<br>User updates the PWM period value via this register.<br>In this mode the ECAP_CAP3 (APRD) register shadows the ECAP_CAP1 register. |

### 3.6.2.6 ECAP\_CAP4 Register

#### 1 ECAP\_CAP4 Register (Offset = 14h) [reset = 0h]

Capture 4 Register.

Return to [Summary Table](#)

**Table 3-693. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 0014h       |
| ECAP1         | 5024 1014h       |
| ECAP2         | 5024 2014h       |
| ECAP3         | 5024 3014h       |
| ECAP4         | 5024 4014h       |
| ECAP5         | 5024 5014h       |
| ECAP6         | 5024 6014h       |
| ECAP7         | 5024 7014h       |
| ECAP8         | 5024 8014h       |
| ECAP9         | 5024 9014h       |

**Figure 3-226. ECAP\_CAP4 Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAP4 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAP4 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAP4 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAP4 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 3-695. ECAP\_CAP4 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                           |
|------|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CAP4  | R/W  | 0h    | In CMP mode this is a time-stamp capture register.<br>In APMW mode this is the compare shadow (ACMP) register.<br>User updates the PWM Compare value via this register.<br>In this mode the ECAP_CAP4 (ACMP) register shadows the ECAP_CAP2 register. |

### 3.6.2.7 ECAP\_ECCTL0 Register

#### 1 ECAP\_ECCTL0 Register (Offset = 24h) [reset = FFh]

Capture Control Register 0

Return to [Summary Table](#)

**Table 3-696. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 0024h       |
| ECAP1         | 5024 1024h       |
| ECAP2         | 5024 2024h       |
| ECAP3         | 5024 3024h       |
| ECAP4         | 5024 4024h       |
| ECAP5         | 5024 5024h       |
| ECAP6         | 5024 6024h       |
| ECAP7         | 5024 7024h       |
| ECAP8         | 5024 8024h       |
| ECAP9         | 5024 9024h       |

**Figure 3-227. ECAP\_ECCTL0 Name Register**

|            |    |    |    |            |    |           |    |
|------------|----|----|----|------------|----|-----------|----|
| 31         | 30 | 29 | 28 | 27         | 26 | 25        | 24 |
| RESERVED_2 |    |    |    |            |    |           |    |
| R          |    |    |    |            |    |           |    |
| 0h         |    |    |    |            |    |           |    |
| 23         | 22 | 21 | 20 | 19         | 18 | 17        | 16 |
| RESERVED_2 |    |    |    |            |    | SOCEVTSEL |    |
| R          |    |    |    |            |    | R/W       |    |
| 0h         |    |    |    |            |    | 0h        |    |
| 15         | 14 | 13 | 12 | 11         | 10 | 9         | 8  |
| QUALPRD    |    |    |    | RESERVED_1 |    |           |    |
| R/W        |    |    |    | R          |    |           |    |
| 0h         |    |    |    | 0h         |    |           |    |
| 7          | 6  | 5  | 4  | 3          | 2  | 1         | 0  |
| INPUTSEL   |    |    |    |            |    |           |    |
| R/W        |    |    |    |            |    |           |    |
| FFh        |    |    |    |            |    |           |    |

**Table 3-698. ECAP\_ECCTL0 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description |
|-------|------------|------|-------|-------------|
| 31:18 | RESERVED_2 | R    | 0h    | Reserved    |



**Table 3-698. ECAP\_ECCTL0 Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 17:16 | SOCEVTSEL  | R/W  | 0h    | ADC SOC event select<br>Capture Mode:<br>00b[R/W] = SOC trigger source is CEVT1<br>01b[R/W] = SOC trigger source is CEVT2<br>10b[R/W] = SOC trigger source is CEVT3<br>11b[R/W] = SOC trigger source is CEVT4<br>APWM Mode:<br>00b[R/W] = SOC trigger interrupt source is period match<br>01b[R/W] = SOC trigger interrupt source is compare match<br>10b[R/W] = SOC trigger interrupt source is period match or compare match<br>11b[R/W] = Disabled |
| 15:12 | QUALPRD    | R/W  | 0h    | Qual period to filter out noise on input signals being monitored, Not applicable for HR mode.<br>0x0 : Bypass<br>0x1 : pulses of with 1 cycle or less will be filtered out<br>0x2 : pulses of with 2 cycles or less will be filtered out<br>....<br>0xF : pulses of with 15 cycles or less will be filtered out                                                                                                                                       |
| 11:8  | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 7:0   | INPUTSEL   | R/W  | FFh   | Capture input source select bits<br>0x0 capture input is ECAPxINPUT[0]<br>0x1 capture input is ECAPxINPUT[1]<br>0x2 capture input is ECAPxINPUT[2]<br>...<br>0xFF capture input is ECAPxINPUT[256]                                                                                                                                                                                                                                                    |

### 3.6.2.8 ECAP\_ECCTL1 Register

#### 1 ECAP\_ECCTL1 Register (Offset = 28h) [reset = 0h]

Capture Control Register 1

Return to [Summary Table](#)

**Table 3-699. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 0028h       |
| ECAP1         | 5024 1028h       |
| ECAP2         | 5024 2028h       |
| ECAP3         | 5024 3028h       |
| ECAP4         | 5024 4028h       |
| ECAP5         | 5024 5028h       |
| ECAP6         | 5024 6028h       |
| ECAP7         | 5024 7028h       |
| ECAP8         | 5024 8028h       |
| ECAP9         | 5024 9028h       |

**Figure 3-228. ECAP\_ECCTL1 Name Register**

|           |         |          |         |         |         |         |         |
|-----------|---------|----------|---------|---------|---------|---------|---------|
| 15        | 14      | 13       | 12      | 11      | 10      | 9       | 8       |
| FREE_SOFT |         | PRESCALE |         |         |         |         | CAPLDEN |
| R/W       |         | R/W      |         |         |         |         | R/W     |
| 0h        |         | 0h       |         |         |         |         | 0h      |
| 7         | 6       | 5        | 4       | 3       | 2       | 1       | 0       |
| CTRRST4   | CAP4POL | CTRRST3  | CAP3POL | CTRRST2 | CAP2POL | CTRRST1 | CAP1POL |
| R/W       | R/W     | R/W      | R/W     | R/W     | R/W     | R/W     | R/W     |
| 0h        | 0h      | 0h       | 0h      | 0h      | 0h      | 0h      | 0h      |

**Table 3-701. ECAP\_ECCTL1 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                      |
|-------|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | FREE_SOFT | R/W  | 0h    | Emulation Control<br>0 TSCTR counter stops immediately on emulation suspend<br>1 TSCTR counter runs until = 0<br>2 TSCTR counter is unaffected by emulation suspend (Run Free)<br>3 TSCTR counter is unaffected by emulation suspend (Run Free)  |
| 13:9  | PRESCALE  | R/W  | 0h    | Event Filter prescale select<br>0 Divide by 1 (i.e., no prescale, by-pass the prescaler)<br>1 Divide by 2<br>2 Divide by 4<br>3 Divide by 6<br>4 Divide by 8<br>5 Divide by 10<br>30 Divide by 60<br>31 Divide by 62                             |
| 8     | CAPLDEN   | R/W  | 0h    | Enable Loading of CAP1-4 registers on a capture event. Note that this bit does not disable CEVTn events from being generated.<br>0 Disable CAP1-4 register loads at capture event time.<br>1 Enable CAP1-4 register loads at capture event time. |

**Table 3-701. ECAP\_ECCTL1 Register Field Descriptions (continued)**

| Bit | Field   | Type | Reset | Description                                                                                                                                                                                                             |
|-----|---------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | CTRRST4 | R/W  | 0h    | Counter Reset on Capture Event 4<br>0 Do not reset counter on Capture Event 4 (absolute time stamp operation)<br>1 Reset counter after Capture Event 4 time-stamp has been captured (used in difference mode operation) |
| 6   | CAP4POL | R/W  | 0h    | Capture Event 4 Polarity select<br>0 Capture Event 4 triggered on a rising edge (RE)<br>1 Capture Event 4 triggered on a falling edge (FE)                                                                              |
| 5   | CTRRST3 | R/W  | 0h    | Counter Reset on Capture Event 3<br>0 Do not reset counter on Capture Event 3 (absolute time stamp)<br>1 Reset counter after Event 3 time-stamp has been captured (used in difference mode operation)                   |
| 4   | CAP3POL | R/W  | 0h    | Capture Event 3 Polarity select<br>0 Capture Event 3 triggered on a rising edge (RE)<br>1 Capture Event 3 triggered on a falling edge (FE)                                                                              |
| 3   | CTRRST2 | R/W  | 0h    | Counter Reset on Capture Event 2<br>0 Do not reset counter on Capture Event 2 (absolute time stamp)<br>1 Reset counter after Event 2 time-stamp has been captured (used in difference mode operation)                   |
| 2   | CAP2POL | R/W  | 0h    | Capture Event 2 Polarity select<br>0 Capture Event 2 triggered on a rising edge (RE)<br>1 Capture Event 2 triggered on a falling edge (FE)                                                                              |
| 1   | CTRRST1 | R/W  | 0h    | Counter Reset on Capture Event 1<br>0 Do not reset counter on Capture Event 1 (absolute time stamp)<br>1 Reset counter after Event 1 time-stamp has been captured (used in difference mode operation)                   |
| 0   | CAP1POL | R/W  | 0h    | Capture Event 1 Polarity select<br>0 Capture Event 1 triggered on a rising edge (RE)<br>1 Capture Event 1 triggered on a falling edge (FE)                                                                              |

### 3.6.2.9 ECAP\_ECCTL2 Register

#### 1 ECAP\_ECCTL2 Register (Offset = 2Ah) [reset = 6h]

Capture Control Register 2

Return to [Summary Table](#)

**Table 3-702. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 002Ah       |
| ECAP1         | 5024 102Ah       |
| ECAP2         | 5024 202Ah       |
| ECAP3         | 5024 302Ah       |
| ECAP4         | 5024 402Ah       |
| ECAP5         | 5024 502Ah       |
| ECAP6         | 5024 602Ah       |
| ECAP7         | 5024 702Ah       |
| ECAP8         | 5024 802Ah       |
| ECAP9         | 5024 902Ah       |

**Figure 3-229. ECAP\_ECCTL2 Name Register**

| 15         | 14 | 13        | 12        | 11           | 10        | 9        | 8            |
|------------|----|-----------|-----------|--------------|-----------|----------|--------------|
| MODCNTRSTS |    | DMAEVTSEL |           | CTRFILTRESET | APWMPOL   | CAP_APWM | SWSYNC       |
| R/W        |    | R/W       |           | R/W1TC       | R/W       | R/W      | R/W1TS       |
| 0h         |    | 0h        |           | 0h           | 0h        | 0h       | 0h           |
| 7          | 6  | 5         | 4         | 3            | 2         | 1        | 0            |
| SYNCO_SEL  |    | SYNCL_EN  | TSCTRSTOP | REARM        | STOP_WRAP |          | CONT_ONESHOT |
| R/W        |    | R/W       | R/W       | R/W1TS       | R/W       |          | R/W          |
| 0h         |    | 0h        | 0h        | 0h           | 3h        |          | 0h           |

**Table 3-704. ECAP\_ECCTL2 Register Field Descriptions**

| Bit   | Field        | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|--------------|--------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | MODCNTRSTS   | R/W    | 0h    | This bit field reads current status on modulo counter<br>00b[R] = CAP1 register gets loaded on next capture event.<br>01b[R] = CAP2 register gets loaded on next capture event.<br>10b[R] = CAP3 register gets loaded on next capture event.<br>11b[R] = CAP4 register gets loaded on next capture event.                                                                                                                         |
| 13:12 | DMAEVTSEL    | R/W    | 0h    | DMA event select<br>Capture Mode:<br>00b[R/W] = DMA interrupt source is CEVT1<br>01b[R/W] = DMA interrupt source is CEVT2<br>10b[R/W] = DMA interrupt source is CEVT3<br>11b[R/W] = DMA interrupt source is CEVT4<br>APWM Mode:<br>00b[R/W] = DMA interrupt source is period match<br>01b[R/W] = DMA interrupt source is compare match<br>10b[R/W] = DMA interrupt source is period match or compare match<br>11b[R/W] = Disabled |
| 11    | CTRFILTRESET | R/W1TC | 0h    | Reset Bit<br>0h[R] = No effect<br>1h[W] = Resets event filter, counter, modulo counter and CEVT[1,2,3,4] and CNTOVF , HRERROR flags<br>Note: This provides an ability start capture module from known state in case spurious inputs are captured while ECAP is configured.                                                                                                                                                        |

**Table 3-704. ECAP\_ECCTL2 Register Field Descriptions (continued)**

| Bit | Field     | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|-----------|--------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | APWMPOL   | R/W    | 0h    | APWM output polarity select. This is applicable only in APWM operating mode.<br>0 Output is active high (Compare value defines high time)<br>1 Output is active low (Compare value defines low time)                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 9   | CAP_APWM  | R/W    | 0h    | CAP/APWM operating mode select<br>0 ECAP module operates in capture mode. This mode forces the following configuration: - Inhibits TSCTR resets via CTR = PRD event - Inhibits shadow loads on CAP1 and 2 registers - Permits user to enable CAP1-4 register load - CAPx/APWMx pin operates as a capture input<br>1 ECAP module operates in APWM mode. This mode forces the following configuration: - Resets TSCTR on CTR = PRD event (period boundary) - Permits shadow loading on CAP1 and 2 registers - Disables loading of time-stamps into CAP1-4 registers - CAPx/APWMx pin operates as a APWM output         |
| 8   | SWSYNC    | R/W1TS | 0h    | Software-forced Counter [TSCTR] Synchronizer. This provides the user a method to generate a synchronization pulse through software. In APWM mode, the synchronization pulse can also be sourced from the CTR = PRD event.<br>0 Writing a zero has no effect. Reading always returns a zero<br>1 Writing a one forces a TSCTR shadow load of current ECAP module and any ECAP modules down-stream providing the SYNC0_SEL bits are 0,0. After writing a 1, this bit returns to a zero. Note: Selection CTR = PRD is meaningful only in APWM mode; however, you can choose it in CAP mode if you find doing so useful. |
| 7:6 | SYNC0_SEL | R/W    | 0h    | Sync-Out Select<br>0 sync out signal is SWSYNC<br>1 Select CTR = PRD event to be the sync-out signal<br>3 Disable sync out signal                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 5   | SYNCl_EN  | R/W    | 0h    | Counter [TSCTR] Sync-In select mode<br>0 Disable sync-in option<br>1 Enable counter (TSCTR) to be loaded from CTRPHS register upon either a SYNCl signal or a S/W force event.                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 4   | TSCTRSTOP | R/W    | 0h    | Time Stamp [TSCTR] Counter Stop [freeze] Control<br>0 TSCTR stopped<br>1 TSCTR free-running                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 3   | REARM     | R/W1TS | 0h    | Re-Arming Control. Note: The re-arm function is valid in one shot or continuous mode<br>0 Has no effect (reading always returns a 0)<br>1 Arms the one-shot sequence as follows: (1) Resets the Mod4 counter to zero (2) Unfreezes the Mod4 counter (3) Enables capture register loads                                                                                                                                                                                                                                                                                                                               |

**Table 3-704. ECAP\_ECCTL2 Register Field Descriptions (continued)**

| Bit | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|-------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:1 | STOP_WRAP   | R/W  | 3h    | <p>Stop value for one-shot mode. This is the number [between 1-4] of captures allowed to occur before the CAP[1-4] registers are frozen, that is, capture sequence is stopped.</p> <p>Wrap value for continuous mode. This is the number [between 1-4] of the capture register in which the circular buffer wraps around and starts again.</p> <p>Notes: STOP_WRAP is compared to Mod4 counter and, when equal, 2 actions occur:</p> <ul style="list-style-type: none"> <li>- Mod4 counter is stopped [frozen]</li> <li>- Capture register loads are inhibited</li> </ul> <p>In one-shot mode, further interrupt events are blocked until re-armed.</p> <p>0      Stop after Capture Event 1 in one-shot mode<br/>                  wrap after Capture Event 1 in continuous mode.</p> <p>1      Stop after Capture Event 2 in one-shot mode<br/>                  wrap after Capture Event 2 in continuous mode.</p> <p>2      Stop after Capture Event 3 in one-shot mode<br/>                  wrap after Capture Event 3 in continuous mode.</p> <p>3      Stop after Capture Event 4 in one-shot mode<br/>                  wrap after Capture Event 4 in continuous mode.</p> |
| 0   | CONT_ONESHT | R/W  | 0h    | <p>Continuous or one-shot mode control [applicable only in capture mode]</p> <p>0      Operate in continuous mode</p> <p>1      Operate in one-Shot mode</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

### 3.6.2.10 ECAP\_ECEINT Register

#### 1 ECAP\_ECEINT Register (Offset = 2Ch) [reset = 0h]

The interrupt enable bits (CEVT1, ...) block any of the selected events from generating an interrupt. Events will still be latched into the flag bit (ECFLG register) and can be forced/cleared via the ECFRC/ECCLR registers. The proper procedure for configuring peripheral modes and interrupts is as follows:

- Disable global interrupts
- Stop eCAP counter
- Disable eCAP interrupts
- Configure peripheral registers
- Clear spurious eCAP interrupt flags
- Enable eCAP interrupts
- Start eCAP counter
- Enable global interrupts.

Return to [Summary Table](#)

**Table 3-705. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 002Ch       |
| ECAP1         | 5024 102Ch       |
| ECAP2         | 5024 202Ch       |
| ECAP3         | 5024 302Ch       |
| ECAP4         | 5024 402Ch       |
| ECAP5         | 5024 502Ch       |
| ECAP6         | 5024 602Ch       |
| ECAP7         | 5024 702Ch       |
| ECAP8         | 5024 802Ch       |
| ECAP9         | 5024 902Ch       |

**Figure 3-230. ECAP\_ECEINT Name Register**

| 15         | 14         | 13     | 12                     | 11                     | 10                     | 9                      | 8          |
|------------|------------|--------|------------------------|------------------------|------------------------|------------------------|------------|
| RESERVED_2 |            |        | MUNIT_2_ERR<br>OR_EVT2 | MUNIT_2_ERR<br>OR_EVT1 | MUNIT_1_ERR<br>OR_EVT2 | MUNIT_1_ERR<br>OR_EVT1 | HRERROR    |
| R          |            |        | R/W                    | R/W                    | R/W                    | R/W                    | R/W        |
| 0h         |            |        | 0h                     | 0h                     | 0h                     | 0h                     | 0h         |
| 7          | 6          | 5      | 4                      | 3                      | 2                      | 1                      | 0          |
| CTR_EQ_CMP | CTR_EQ_PRD | CTROVF | CEVT4                  | CEVT3                  | CEVT2                  | CEVT1                  | RESERVED_1 |
| R/W        | R/W        | R/W    | R/W                    | R/W                    | R/W                    | R/W                    | R          |
| 0h         | 0h         | 0h     | 0h                     | 0h                     | 0h                     | 0h                     | 0h         |

**Table 3-707. ECAP\_ECEINT Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                       |
|-------|--------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | RESERVED_2         | R    | 0h    | Reserved                                                                                                                                                          |
| 12    | MUNIT_2_ERROR_EVT2 | R/W  | 0h    | Monitoring unit 2 error event 2 interrupt enable<br>0 : Disable Monitoring unit 2 error event 2 interrupt<br>1 : Enable Monitoring unit 2 error event 2 interrupt |
| 11    | MUNIT_2_ERROR_EVT1 | R/W  | 0h    | Monitoring unit 2 error event 2 interrupt enable<br>0 : Disable Monitoring unit 2 error event 1 interrupt<br>1 : Enable Monitoring unit 2 error event 1 interrupt |
| 10    | MUNIT_1_ERROR_EVT2 | R/W  | 0h    | Monitoring unit 1 error event 1 interrupt enable<br>0 : Disable Monitoring unit 1 error event 2 interrupt<br>1 : Enable Monitoring unit 1 error event 2 interrupt |

**Table 3-707. ECAP\_ECEINT Register Field Descriptions (continued)**

| Bit | Field              | Type | Reset | Description                                                                                                                                                         |
|-----|--------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9   | MUNIT_1_ERROR_EVT1 | R/W  | 0h    | Monitoring unit 1 error event 1 interrupt enable<br>0 : Disable Monitoring unit 1 error event 1 interrupt<br>1 : Enable Monitoring unit 1 error event 1 interrupt   |
| 8   | HRERROR            | R/W  | 0h    | High resolution error interrupt enable<br>0      Disable High Resolution Error as an Interrupt source<br>1      Enable High Resolution Error as an Interrupt source |
| 7   | CTR_EQ_CMP         | R/W  | 0h    | Counter Equal Compare Interrupt Enable<br>0      Disable Compare Equal as an Interrupt source<br>1      Enable Compare Equal as an Interrupt source                 |
| 6   | CTR_EQ_PRD         | R/W  | 0h    | Counter Equal Period Interrupt Enable<br>0      Disable Period Equal as an Interrupt source<br>1      Enable Period Equal as an Interrupt source                    |
| 5   | CTROVF             | R/W  | 0h    | Counter Overflow Interrupt Enable<br>0      Disabled counter overflow as an Interrupt source<br>1      Enable counter overflow as an Interrupt source               |
| 4   | CEVT4              | R/W  | 0h    | Capture Event 4 Interrupt Enable<br>0      Disable Capture Event 4 as an Interrupt source<br>1      Capture Event 4 Interrupt Enable                                |
| 3   | CEVT3              | R/W  | 0h    | Capture Event 3 Interrupt Enable<br>0      Disable Capture Event 3 as an Interrupt source<br>1      Enable Capture Event 3 as an Interrupt source                   |
| 2   | CEVT2              | R/W  | 0h    | Capture Event 2 Interrupt Enable<br>0      Disable Capture Event 2 as an Interrupt source<br>1      Enable Capture Event 2 as an Interrupt source                   |
| 1   | CEVT1              | R/W  | 0h    | Capture Event 1 Interrupt Enable<br>0      Disable Capture Event 1 as an Interrupt source<br>1      Enable Capture Event 1 as an Interrupt source                   |
| 0   | RESERVED_1         | R    | 0h    | Reserved                                                                                                                                                            |



### 3.6.2.11 ECAP\_ECFLG Register

#### 1 ECAP\_ECFLG Register (Offset = 2Eh) [reset = 0h]

Capture Interrupt Flag Register.

Return to [Summary Table](#)

**Table 3-708. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 002Eh       |
| ECAP1         | 5024 102Eh       |
| ECAP2         | 5024 202Eh       |
| ECAP3         | 5024 302Eh       |
| ECAP4         | 5024 402Eh       |
| ECAP5         | 5024 502Eh       |
| ECAP6         | 5024 602Eh       |
| ECAP7         | 5024 702Eh       |
| ECAP8         | 5024 802Eh       |
| ECAP9         | 5024 902Eh       |

**Figure 3-231. ECAP\_ECFLG Name Register**

| 15         | 14      | 13     | 12                     | 11                     | 10                     | 9                      | 8       |
|------------|---------|--------|------------------------|------------------------|------------------------|------------------------|---------|
| RESERVED_1 |         |        | MUNIT_2_ERR<br>OR_EVT2 | MUNIT_2_ERR<br>OR_EVT1 | MUNIT_1_ERR<br>OR_EVT2 | MUNIT_1_ERR<br>OR_EVT1 | HRERROR |
| R          |         |        | R                      | R                      | R                      | R                      | R       |
| 0h         |         |        | 0h                     | 0h                     | 0h                     | 0h                     | 0h      |
| 7          | 6       | 5      | 4                      | 3                      | 2                      | 1                      | 0       |
| CTR_CMP    | CTR_PRD | CTROVF | CEVT4                  | CEVT3                  | CEVT2                  | CEVT1                  | INT     |
| R          | R       | R      | R                      | R                      | R                      | R                      | R       |
| 0h         | 0h      | 0h     | 0h                     | 0h                     | 0h                     | 0h                     | 0h      |

**Table 3-710. ECAP\_ECFLG Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                          |
|-------|--------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | RESERVED_1         | R    | 0h    | Reserved                                                                                                                                                                                             |
| 12    | MUNIT_2_ERROR_EVT2 | R    | 0h    | Error event 2 Interrupt Flag from monitoring unit 2                                                                                                                                                  |
| 11    | MUNIT_2_ERROR_EVT1 | R    | 0h    | Error event 2 Interrupt Flag from monitoring unit 2                                                                                                                                                  |
| 10    | MUNIT_1_ERROR_EVT2 | R    | 0h    | Error event 2 Interrupt Flag from monitoring unit 1                                                                                                                                                  |
| 9     | MUNIT_1_ERROR_EVT1 | R    | 0h    | Error event 2 Interrupt Flag from monitoring unit 1                                                                                                                                                  |
| 8     | HRERROR            | R    | 0h    | High resolution error status flag<br>0 Indicates no event occurred<br>1 Indicates the High resolution Error occurred                                                                                 |
| 7     | CTR_CMP            | R    | 0h    | Compare Equal Compare Status Flag. This flag is active only in APWM mode.<br>0 Indicates no event occurred<br>1 Indicates the counter (TSCTR) reached the compare register value (ACMP)              |
| 6     | CTR_PRD            | R    | 0h    | Counter Equal Period Status Flag. This flag is only active in APWM mode.<br>0 Indicates no event occurred<br>1 Indicates the counter (TSCTR) reached the period register value (APRD) and was reset. |

**Table 3-710. ECAP\_ECFLG Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                   |
|-----|--------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | CTROVF | R    | 0h    | Counter Overflow Status Flag. This flag is active in CAP and APWM mode.<br>0 Indicates no event occurred<br>1 Indicates the counter (TSCTR) has made the transition from FFFFFFFF to 00000000 |
| 4   | CEVT4  | R    | 0h    | Capture Event 4 Status Flag This flag is only active in CAP mode.<br>0 Indicates no event occurred<br>1 Indicates the fourth event occurred at ECAPx pin                                      |
| 3   | CEVT3  | R    | 0h    | Capture Event 3 Status Flag. This flag is active only in CAP mode.<br>0 Indicates no event occurred<br>1 Indicates the third event occurred at ECAPx pin.                                     |
| 2   | CEVT2  | R    | 0h    | Capture Event 2 Status Flag. This flag is only active in CAP mode.<br>0 Indicates no event occurred<br>1 Indicates the second event occurred at ECAPx pin.                                    |
| 1   | CEVT1  | R    | 0h    | Capture Event 1 Status Flag. This flag is only active in CAP mode.<br>0 Indicates no event occurred<br>1 Indicates the first event occurred at ECAPx pin.                                     |
| 0   | INT    | R    | 0h    | Global Interrupt Status Flag<br>0 Indicates no event occurred<br>1 Indicates that an interrupt was generated.                                                                                 |

### 3.6.2.12 ECAP\_ECCLR Register

#### 1 ECAP\_ECCLR Register (Offset = 30h) [reset = 0h]

Capture Interrupt Clear Register.

Return to [Summary Table](#)

**Table 3-711. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 0030h       |
| ECAP1         | 5024 1030h       |
| ECAP2         | 5024 2030h       |
| ECAP3         | 5024 3030h       |
| ECAP4         | 5024 4030h       |
| ECAP5         | 5024 5030h       |
| ECAP6         | 5024 6030h       |
| ECAP7         | 5024 7030h       |
| ECAP8         | 5024 8030h       |
| ECAP9         | 5024 9030h       |

**Figure 3-232. ECAP\_ECCLR Name Register**

| 15         | 14      | 13     | 12                     | 11                     | 10                     | 9                      | 8       |
|------------|---------|--------|------------------------|------------------------|------------------------|------------------------|---------|
| RESERVED_1 |         |        | MUNIT_2_ERR<br>OR_EVT2 | MUNIT_2_ERR<br>OR_EVT1 | MUNIT_1_ERR<br>OR_EVT2 | MUNIT_1_ERR<br>OR_EVT1 | HRERROR |
| R          |         |        | R/W1TC                 | R/W1TC                 | R/W1TC                 | R/W1TC                 | R/W1TC  |
| 0h         |         |        | 0h                     | 0h                     | 0h                     | 0h                     | 0h      |
| 7          | 6       | 5      | 4                      | 3                      | 2                      | 1                      | 0       |
| CTR_CMP    | CTR_PRD | CTROVF | CEVT4                  | CEVT3                  | CEVT2                  | CEVT1                  | INT     |
| R/W1TC     | R/W1TC  | R/W1TC | R/W1TC                 | R/W1TC                 | R/W1TC                 | R/W1TC                 | R/W1TC  |
| 0h         | 0h      | 0h     | 0h                     | 0h                     | 0h                     | 0h                     | 0h      |

**Table 3-713. ECAP\_ECCLR Register Field Descriptions**

| Bit   | Field              | Type   | Reset | Description                                                                                                                         |
|-------|--------------------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | RESERVED_1         | R      | 0h    | Reserved                                                                                                                            |
| 12    | MUNIT_2_ERROR_EVT2 | R/W1TC | 0h    | Writing '1' clears MUNIT_2_ERROR_EVT2 interrupt flag                                                                                |
| 11    | MUNIT_2_ERROR_EVT1 | R/W1TC | 0h    | Writing '1' clears MUNIT_2_ERROR_EVT1 interrupt flag                                                                                |
| 10    | MUNIT_1_ERROR_EVT2 | R/W1TC | 0h    | Writing '1' clears MUNIT_1_ERROR_EVT2 interrupt flag                                                                                |
| 9     | MUNIT_1_ERROR_EVT1 | R/W1TC | 0h    | Writing '1' clears MUNIT_1_ERROR_EVT1 interrupt flag                                                                                |
| 8     | HRERROR            | R/W1TC | 0h    | High resolution error status Clear<br>0 writing a 0 has no effect. Always reads back a 0<br>1 writing a 1 clears the HRERROR flag.  |
| 7     | CTR_CMP            | R/W1TC | 0h    | Counter Equal Compare Status Clear<br>0 writing a 0 has no effect. Always reads back a 0<br>1 writing a 1 clears the CTR=COMP flag. |
| 6     | CTR_PRD            | R/W1TC | 0h    | Counter Equal Period Status Clear<br>0 writing a 0 has no effect. Always reads back a 0<br>1 writing a 1 clears the CTR=PRD flag.   |

**Table 3-713. ECAP\_ECCLR Register Field Descriptions (continued)**

| Bit | Field  | Type   | Reset | Description                                                                                                                                                                                                        |
|-----|--------|--------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | CTROVF | R/W1TC | 0h    | Counter Overflow Status Clear<br>0 writing a 0 has no effect. Always reads back a 0<br>1 writing a 1 clears the CTROVF flag.                                                                                       |
| 4   | CEVT4  | R/W1TC | 0h    | Capture Event 4 Status Clear<br>0 writing a 0 has no effect. Always reads back a 0<br>1 writing a 1 clears the CEVT4 flag.                                                                                         |
| 3   | CEVT3  | R/W1TC | 0h    | Capture Event 3 Status Clear<br>0 writing a 0 has no effect. Always reads back a 0<br>1 writing a 1 clears the CEVT3 flag.                                                                                         |
| 2   | CEVT2  | R/W1TC | 0h    | Capture Event 2 Status Clear<br>0 writing a 0 has no effect. Always reads back a 0<br>1 writing a 1 clears the CEVT2 flag.                                                                                         |
| 1   | CEVT1  | R/W1TC | 0h    | Capture Event 1 Status Clear<br>0 writing a 0 has no effect. Always reads back a 0<br>1 writing a 1 clears the CEVT1 flag.                                                                                         |
| 0   | INT    | R/W1TC | 0h    | ECAP Global Interrupt Status Clear<br>0 writing a 0 has no effect. Always reads back a 0<br>1 writing a 1 clears the INT flag and enable further interrupts to be generated if any of the event flags are set to 1 |

### 3.6.2.13 ECAP\_ECFRC Register

#### 1 ECAP\_ECFRC Register (Offset = 32h) [reset = 0h]

Capture Interrupt Force Register.

Return to [Summary Table](#)

**Table 3-714. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 0032h       |
| ECAP1         | 5024 1032h       |
| ECAP2         | 5024 2032h       |
| ECAP3         | 5024 3032h       |
| ECAP4         | 5024 4032h       |
| ECAP5         | 5024 5032h       |
| ECAP6         | 5024 6032h       |
| ECAP7         | 5024 7032h       |
| ECAP8         | 5024 8032h       |
| ECAP9         | 5024 9032h       |

**Figure 3-233. ECAP\_ECFRC Name Register**

| 15         | 14      | 13     | 12                     | 11                     | 10                     | 9                      | 8          |
|------------|---------|--------|------------------------|------------------------|------------------------|------------------------|------------|
| RESERVED_2 |         |        | MUNIT_2_ERR<br>OR_EVT2 | MUNIT_2_ERR<br>OR_EVT1 | MUNIT_1_ERR<br>OR_EVT2 | MUNIT_1_ERR<br>OR_EVT1 | HRERROR    |
| R          |         |        | R/W1TS                 | R/W1TS                 | R/W1TS                 | R/W1TS                 | R/W1TS     |
| 0h         |         |        | 0h                     | 0h                     | 0h                     | 0h                     | 0h         |
| 7          | 6       | 5      | 4                      | 3                      | 2                      | 1                      | 0          |
| CTR_CMP    | CTR_PRD | CTROVF | CEVT4                  | CEVT3                  | CEVT2                  | CEVT1                  | RESERVED_1 |
| R/W1TS     | R/W1TS  | R/W1TS | R/W1TS                 | R/W1TS                 | R/W1TS                 | R/W1TS                 | R          |
| 0h         | 0h      | 0h     | 0h                     | 0h                     | 0h                     | 0h                     | 0h         |

**Table 3-716. ECAP\_ECFRC Register Field Descriptions**

| Bit   | Field              | Type   | Reset | Description                                                                                                                                                   |
|-------|--------------------|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | RESERVED_2         | R      | 0h    | Reserved                                                                                                                                                      |
| 12    | MUNIT_2_ERROR_EVT2 | R/W1TS | 0h    | Writing '1' sets MUNIT_2_ERROR_EVT2 interrupt flag                                                                                                            |
| 11    | MUNIT_2_ERROR_EVT1 | R/W1TS | 0h    | Writing '1' sets MUNIT_2_ERROR_EVT1 interrupt flag                                                                                                            |
| 10    | MUNIT_1_ERROR_EVT2 | R/W1TS | 0h    | Writing '1' sets MUNIT_1_ERROR_EVT2 interrupt flag                                                                                                            |
| 9     | MUNIT_1_ERROR_EVT1 | R/W1TS | 0h    | Writing '1' sets MUNIT_1_ERROR_EVT1 interrupt flag                                                                                                            |
| 8     | HRERROR            | R/W1TS | 0h    | High resolution error Force interrupt<br>0 No effect. Always reads back a 0.<br>1 Writing a 1 sets the CTR_CMP flag.                                          |
| 7     | CTR_CMP            | R/W1TS | 0h    | Force Counter Equal Compare Interrupt. This event is only active in APWM mode.<br>0 No effect. Always reads back a 0.<br>1 Writing a 1 sets the CTR_CMP flag. |
| 6     | CTR_PRD            | R/W1TS | 0h    | Force Counter Equal Period Interrupt. This event is only active in APWM mode.<br>0 No effect. Always reads back a 0.<br>1 Writing a 1 sets the CTR_PRD flag.  |

**Table 3-716. ECAP\_ECFRC Register Field Descriptions (continued)**

| Bit | Field      | Type   | Reset | Description                                                                                                                                |
|-----|------------|--------|-------|--------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | CTROVF     | R/W1TS | 0h    | Force Counter Overflow<br>0 No effect. Always reads back a 0.<br>1 Writing a 1 to this bit sets the CTROVF flag.                           |
| 4   | CEVT4      | R/W1TS | 0h    | Force Capture Event 4. This event is only active in CAP mode.<br>0 No effect. Always reads back a 0.<br>1 Writing a 1 sets the CEVT4 flag. |
| 3   | CEVT3      | R/W1TS | 0h    | Force Capture Event 3. This event is only active in CAP mode.<br>0 No effect. Always reads back a 0.<br>1 Writing a 1 sets the CEVT3 flag. |
| 2   | CEVT2      | R/W1TS | 0h    | Force Capture Event 2. This event is only active in CAP mode.<br>0 No effect. Always reads back a 0.<br>1 Writing a 1 sets the CEVT2 flag. |
| 1   | CEVT1      | R/W1TS | 0h    | Force Capture Event 1. This event is only active in CAP mode.<br>0 No effect. Always reads back a 0.<br>1 Sets the CEVT1 flag.             |
| 0   | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                   |

### 3.6.2.14 ECAP\_ECAPSYNCINSEL Register

#### 1 ECAP\_ECAPSYNCINSEL Register (Offset = 3Ch) [reset = 1h]

SYNC source select register.

Return to [Summary Table](#)

**Table 3-717. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 003Ch       |
| ECAP1         | 5024 103Ch       |
| ECAP2         | 5024 203Ch       |
| ECAP3         | 5024 303Ch       |
| ECAP4         | 5024 403Ch       |
| ECAP5         | 5024 503Ch       |
| ECAP6         | 5024 603Ch       |
| ECAP7         | 5024 703Ch       |
| ECAP8         | 5024 803Ch       |
| ECAP9         | 5024 903Ch       |

**Figure 3-234. ECAP\_ECAPSYNCINSEL Name Register**

|            |     |    |    |    |    |    |    |
|------------|-----|----|----|----|----|----|----|
| 31         | 30  | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_1 |     |    |    |    |    |    |    |
| R          |     |    |    |    |    |    |    |
| 0h         |     |    |    |    |    |    |    |
| 23         | 22  | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_1 |     |    |    |    |    |    |    |
| R          |     |    |    |    |    |    |    |
| 0h         |     |    |    |    |    |    |    |
| 15         | 14  | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_1 |     |    |    |    |    |    |    |
| R          |     |    |    |    |    |    |    |
| 0h         |     |    |    |    |    |    |    |
| 7          | 6   | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED_1 | SEL |    |    |    |    |    |    |
| R          | R/W |    |    |    |    |    |    |
| 0h         | 1h  |    |    |    |    |    |    |

**Table 3-719. ECAP\_ECAPSYNCINSEL Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                               |
|------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                  |
| 6:0  | SEL        | R/W  | 1h    | These bits determine the source of SYNCIN signal.<br>0x0 : Reserved.<br>0x1: EPWM0.SYNCOU<br>0x1: EPWM1.SYNCOU<br>0x3: EPWM2.SYNCOU<br>...<br>0x32: EPWM31.SYNCOU<br>0x33-0x128: Reserved |

### 3.6.2.15 ECAP\_MUNIT\_COMMON\_CTL Register

#### 1 ECAP\_MUNIT\_COMMON\_CTL Register (Offset = 80h) [reset = 0h]

Control registers for monitoring unit {#}

Return to [Summary Table](#)

**Table 3-720. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 0080h       |
| ECAP1         | 5024 1080h       |
| ECAP2         | 5024 2080h       |
| ECAP3         | 5024 3080h       |
| ECAP4         | 5024 4080h       |
| ECAP5         | 5024 5080h       |
| ECAP6         | 5024 6080h       |
| ECAP7         | 5024 7080h       |
| ECAP8         | 5024 8080h       |
| ECAP9         | 5024 9080h       |

**Figure 3-235. ECAP\_MUNIT\_COMMON\_CTL Name Register**

|            |            |    |    |    |    |    |    |
|------------|------------|----|----|----|----|----|----|
| 31         | 30         | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_3 |            |    |    |    |    |    |    |
| R          |            |    |    |    |    |    |    |
| 0h         |            |    |    |    |    |    |    |
| 23         | 22         | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_3 |            |    |    |    |    |    |    |
| R          |            |    |    |    |    |    |    |
| 0h         |            |    |    |    |    |    |    |
| 15         | 14         | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_2 | GLDSTRBSEL |    |    |    |    |    |    |
| R          | R/W        |    |    |    |    |    |    |
| 0h         | 0h         |    |    |    |    |    |    |
| 7          | 6          | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED_1 | TRIPSEL    |    |    |    |    |    |    |
| R          | R/W        |    |    |    |    |    |    |
| 0h         | 0h         |    |    |    |    |    |    |

**Table 3-722. ECAP\_MUNIT\_COMMON\_CTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                            |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED_3 | R    | 0h    | Reserved                                                                                                                                                               |
| 15    | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                               |
| 14:8  | GLDSTRBSEL | R/W  | 0h    | Global load strobe select to enable shadow to active loading<br>0x0 : Reserved.<br>0x1 to 0x7F : Global load strobe from SOC level including EPWM global load strobes. |
| 7     | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                               |



**Table 3-722. ECAP\_MUNIT\_COMMON\_CTL Register Field Descriptions (continued)**

| Bit | Field   | Type | Reset | Description                                                                                                                                                                                                                                       |
|-----|---------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6:0 | TRIPSEL | R/W  | 0h    | Trip signal select to disable and enable signal monitoring automatically<br>0x0 : Disabled, Trip signals does not effect signal monitoring.<br>0x1 to 0x7F : Signal monioring is disabled when selected signal is high and enabled when it is low |

### 3.6.2.16 ECAP\_MUNIT\_1\_CTL Register

#### 1 ECAP\_MUNIT\_1\_CTL Register (Offset = C0h) [reset = 0h]

Control registers for monitoring unit 1

Return to [Summary Table](#)

**Table 3-723. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 00C0h       |
| ECAP1         | 5024 10C0h       |
| ECAP2         | 5024 20C0h       |
| ECAP3         | 5024 30C0h       |
| ECAP4         | 5024 40C0h       |
| ECAP5         | 5024 50C0h       |
| ECAP6         | 5024 60C0h       |
| ECAP7         | 5024 70C0h       |
| ECAP8         | 5024 80C0h       |
| ECAP9         | 5024 90C0h       |

**Figure 3-236. ECAP\_MUNIT\_1\_CTL Name Register**

|            |    |    |    |         |    |                    |     |
|------------|----|----|----|---------|----|--------------------|-----|
| 31         | 30 | 29 | 28 | 27      | 26 | 25                 | 24  |
| RESERVED_3 |    |    |    |         |    |                    |     |
| R          |    |    |    |         |    |                    |     |
| 0h         |    |    |    |         |    |                    |     |
| 23         | 22 | 21 | 20 | 19      | 18 | 17                 | 16  |
| RESERVED_3 |    |    |    |         |    |                    |     |
| R          |    |    |    |         |    |                    |     |
| 0h         |    |    |    |         |    |                    |     |
| 15         | 14 | 13 | 12 | 11      | 10 | 9                  | 8   |
| RESERVED_2 |    |    |    | MON_SEL |    |                    |     |
| R          |    |    |    | R/W     |    |                    |     |
| 0h         |    |    |    | 0h      |    |                    |     |
| 7          | 6  | 5  | 4  | 3       | 2  | 1                  | 0   |
| RESERVED_1 |    |    |    |         |    | DEBUG_RANG<br>E_EN | EN  |
| R          |    |    |    |         |    | R/W                | R/W |
| 0h         |    |    |    |         |    | 0h                 | 0h  |

**Table 3-725. ECAP\_MUNIT\_1\_CTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED_3 | R    | 0h    | Reserved                                                                                                                                                                                                                                 |
| 15:12 | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                 |
| 11:8  | MON_SEL    | R/W  | 0h    | Type of monitoring<br>0 : High Pulse width<br>1 : Low Pulse width<br>2 : Period width from Rise to Rise<br>3 : Period width from fall to fall<br>4 : Monitor rise edge<br>5 : Monitor fall edge<br>6<br>15 : Reserved [High Pulse width] |

**Table 3-725. ECAP\_MUNIT\_1\_CTL Register Field Descriptions (continued)**

| Bit | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                |
|-----|----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:2 | RESERVED_1     | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                   |
| 1   | DEBUG_RANGE_EN | R/W  | 0h    | Debug mode enable.<br>0 : Debug mode is disabled.<br>1 : Debug mode of monitoring unit 1 is enabled to obtain the variation seen in the system for debug purpose. Range is captured in MUNIT_1_DEBUG_RANGE_MIN and MUNIT_1_DEBUG_RANGE_MAX registers<br>Toggle DEBUG_RANGE_EN to restart this process, this will initialize MUNIT_1_DEBUG_RANGE_MIN and MUNIT_1_DEBUG_RANGE_MAX registers. |
| 0   | EN             | R/W  | 0h    | 0 : Monitoring unit 1 is disabled<br>1 : Monitoring unit 1 is enabled                                                                                                                                                                                                                                                                                                                      |

### 3.6.2.17 ECAP\_MUNIT\_1\_SHADOW\_CTL Register

#### 1 ECAP\_MUNIT\_1\_SHADOW\_CTL Register (Offset = C4h) [reset = 0h]

Shadow control registers for monitoring unit 1

Return to [Summary Table](#)

**Table 3-726. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 00C4h       |
| ECAP1         | 5024 10C4h       |
| ECAP2         | 5024 20C4h       |
| ECAP3         | 5024 30C4h       |
| ECAP4         | 5024 40C4h       |
| ECAP5         | 5024 50C4h       |
| ECAP6         | 5024 60C4h       |
| ECAP7         | 5024 70C4h       |
| ECAP8         | 5024 80C4h       |
| ECAP9         | 5024 90C4h       |

**Figure 3-237. ECAP\_MUNIT\_1\_SHADOW\_CTL Name Register**

|            |    |    |    |    |          |        |          |
|------------|----|----|----|----|----------|--------|----------|
| 31         | 30 | 29 | 28 | 27 | 26       | 25     | 24       |
| RESERVED_1 |    |    |    |    |          |        |          |
| R          |    |    |    |    |          |        |          |
| 0h         |    |    |    |    |          |        |          |
| 23         | 22 | 21 | 20 | 19 | 18       | 17     | 16       |
| RESERVED_1 |    |    |    |    |          |        |          |
| R          |    |    |    |    |          |        |          |
| 0h         |    |    |    |    |          |        |          |
| 15         | 14 | 13 | 12 | 11 | 10       | 9      | 8        |
| RESERVED_1 |    |    |    |    |          |        |          |
| R          |    |    |    |    |          |        |          |
| 0h         |    |    |    |    |          |        |          |
| 7          | 6  | 5  | 4  | 3  | 2        | 1      | 0        |
| RESERVED_1 |    |    |    |    | LOADMODE | SWSYNC | SYNCl_EN |
| R          |    |    |    |    | R/W      | R/W1TS | R/W      |
| 0h         |    |    |    |    | 0h       | 0h     | 0h       |

**Table 3-728. ECAP\_MUNIT\_1\_SHADOW\_CTL Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                         |
|------|------------|--------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                            |
| 2    | LOADMODE   | R/W    | 0h    | Load mode<br>0 : Active registers are loaded with shadow on next sync event<br>1 : Active registers are loaded with shadow on EPWMx.GLDLCSTRB event |
| 1    | SWSYNC     | R/W1TS | 0h    | Copies Min and Max values from shadow to active registers immediately if MUNIT_1_SHADOW_CTL.SYNCl_EN is set.                                        |
| 0    | SYNCl_EN   | R/W    | 0h    | Shadow Enable<br>0 : Disabled<br>1 : Enabled                                                                                                        |

### 3.6.2.18 ECAP\_MUNIT\_1\_MIN Register

#### 1 ECAP\_MUNIT\_1\_MIN Register (Offset = D0h) [reset = 0h]

Min value for monitoring unit 1

Return to [Summary Table](#)

**Table 3-729. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 00D0h       |
| ECAP1         | 5024 10D0h       |
| ECAP2         | 5024 20D0h       |
| ECAP3         | 5024 30D0h       |
| ECAP4         | 5024 40D0h       |
| ECAP5         | 5024 50D0h       |
| ECAP6         | 5024 60D0h       |
| ECAP7         | 5024 70D0h       |
| ECAP8         | 5024 80D0h       |
| ECAP9         | 5024 90D0h       |

**Figure 3-238. ECAP\_MUNIT\_1\_MIN Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MIN_VALUE |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MIN_VALUE |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MIN_VALUE |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MIN_VALUE |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 3-731. ECAP\_MUNIT\_1\_MIN Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                  |
|------|-----------|------|-------|------------------------------|
| 31:0 | MIN_VALUE | R/W  | 0h    | Minimum value for monitoring |

### 3.6.2.19 ECAP\_MUNIT\_1\_MAX Register

#### 1 ECAP\_MUNIT\_1\_MAX Register (Offset = D4h) [reset = 0h]

Max value for monitoring unit 1

Return to [Summary Table](#)

**Table 3-732. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 00D4h       |
| ECAP1         | 5024 10D4h       |
| ECAP2         | 5024 20D4h       |
| ECAP3         | 5024 30D4h       |
| ECAP4         | 5024 40D4h       |
| ECAP5         | 5024 50D4h       |
| ECAP6         | 5024 60D4h       |
| ECAP7         | 5024 70D4h       |
| ECAP8         | 5024 80D4h       |
| ECAP9         | 5024 90D4h       |

**Figure 3-239. ECAP\_MUNIT\_1\_MAX Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MAX_VALUE |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MAX_VALUE |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MAX_VALUE |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MAX_VALUE |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 3-734. ECAP\_MUNIT\_1\_MAX Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                  |
|------|-----------|------|-------|------------------------------|
| 31:0 | MAX_VALUE | R/W  | 0h    | Maximum value for monitoring |

### 3.6.2.20 ECAP\_MUNIT\_1\_MIN\_SHADOW Register

#### 1 ECAP\_MUNIT\_1\_MIN\_SHADOW Register (Offset = D8h) [reset = 0h]

Shadow register for Min value of monitoring unit 1

Return to [Summary Table](#)

**Table 3-735. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 00D8h       |
| ECAP1         | 5024 10D8h       |
| ECAP2         | 5024 20D8h       |
| ECAP3         | 5024 30D8h       |
| ECAP4         | 5024 40D8h       |
| ECAP5         | 5024 50D8h       |
| ECAP6         | 5024 60D8h       |
| ECAP7         | 5024 70D8h       |
| ECAP8         | 5024 80D8h       |
| ECAP9         | 5024 90D8h       |

**Figure 3-240. ECAP\_MUNIT\_1\_MIN\_SHADOW Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MIN_VALUE_SHADOW |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MIN_VALUE_SHADOW |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MIN_VALUE_SHADOW |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MIN_VALUE_SHADOW |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-737. ECAP\_MUNIT\_1\_MIN\_SHADOW Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                         |
|------|------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:0 | MIN_VALUE_SHADOW | R/W  | 0h    | Shadow minimum value for monitoring. Shadow value is loaded to active register on Sync event or global load strobe. |

### 3.6.2.21 ECAP\_MUNIT\_1\_MAX\_SHADOW Register

#### 1 ECAP\_MUNIT\_1\_MAX\_SHADOW Register (Offset = DCh) [reset = 0h]

Shadow register for Max value of monitoring unit 1

Return to [Summary Table](#)

**Table 3-738. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 00DCh       |
| ECAP1         | 5024 10DCh       |
| ECAP2         | 5024 20DCh       |
| ECAP3         | 5024 30DCh       |
| ECAP4         | 5024 40DCh       |
| ECAP5         | 5024 50DCh       |
| ECAP6         | 5024 60DCh       |
| ECAP7         | 5024 70DCh       |
| ECAP8         | 5024 80DCh       |
| ECAP9         | 5024 90DCh       |

**Figure 3-241. ECAP\_MUNIT\_1\_MAX\_SHADOW Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MAX_VALUE_SHADOW |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MAX_VALUE_SHADOW |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MAX_VALUE_SHADOW |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MAX_VALUE_SHADOW |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-740. ECAP\_MUNIT\_1\_MAX\_SHADOW Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                         |
|------|------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:0 | MAX_VALUE_SHADOW | R/W  | 0h    | Shadow maximum value for monitoring. Shadow value is loaded to active register on Sync event or global load strobe. |



### 3.6.2.22 ECAP\_MUNIT\_1\_DEBUG\_RANGE\_MIN Register

#### 1 ECAP\_MUNIT\_1\_DEBUG\_RANGE\_MIN Register (Offset = E0h) [reset = FFFFFFFFh]

Observed Min value of check being enabled on minotoring unit 1

Return to [Summary Table](#)

**Table 3-741. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 00E0h       |
| ECAP1         | 5024 10E0h       |
| ECAP2         | 5024 20E0h       |
| ECAP3         | 5024 30E0h       |
| ECAP4         | 5024 40E0h       |
| ECAP5         | 5024 50E0h       |
| ECAP6         | 5024 60E0h       |
| ECAP7         | 5024 70E0h       |
| ECAP8         | 5024 80E0h       |
| ECAP9         | 5024 90E0h       |

**Figure 3-242. ECAP\_MUNIT\_1\_DEBUG\_RANGE\_MIN Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MIN_VALUE |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| FFFFFFFh  |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MIN_VALUE |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| FFFFFFFh  |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MIN_VALUE |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| FFFFFFFh  |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MIN_VALUE |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| FFFFFFFh  |    |    |    |    |    |    |    |

**Table 3-743. ECAP\_MUNIT\_1\_DEBUG\_RANGE\_MIN Register Field Descriptions**

| Bit  | Field     | Type | Reset    | Description                                                                                                              |
|------|-----------|------|----------|--------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MIN_VALUE | R    | FFFFFFFh | Observed Min value of check being enabled on minotoring unit 1. Is updated when MUNIT_1_CTL.DEBUG_RANGE_EN is set to '1' |

### 3.6.2.23 ECAP\_MUNIT\_1\_DEBUG\_RANGE\_MAX Register

#### 1 ECAP\_MUNIT\_1\_DEBUG\_RANGE\_MAX Register (Offset = E4h) [reset = 0h]

Observed Max value of check being enabled on minotoring unit 1

Return to [Summary Table](#)

**Table 3-744. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 00E4h       |
| ECAP1         | 5024 10E4h       |
| ECAP2         | 5024 20E4h       |
| ECAP3         | 5024 30E4h       |
| ECAP4         | 5024 40E4h       |
| ECAP5         | 5024 50E4h       |
| ECAP6         | 5024 60E4h       |
| ECAP7         | 5024 70E4h       |
| ECAP8         | 5024 80E4h       |
| ECAP9         | 5024 90E4h       |

**Figure 3-243. ECAP\_MUNIT\_1\_DEBUG\_RANGE\_MAX Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MAX_VALUE |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MAX_VALUE |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MAX_VALUE |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MAX_VALUE |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 3-746. ECAP\_MUNIT\_1\_DEBUG\_RANGE\_MAX Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                              |
|------|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MAX_VALUE | R    | 0h    | Observed Min value of check being enabled on minotoring unit 1. Is updated when MUNIT_1_CTL.DEBUG_RANGE_EN is set to '1' |

### 3.6.2.24 ECAP\_MUNIT\_2\_CTL Register

#### 1 ECAP\_MUNIT\_2\_CTL Register (Offset = 100h) [reset = 0h]

Control registers for monitoring unit 2

Return to [Summary Table](#)

**Table 3-747. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 0100h       |
| ECAP1         | 5024 1100h       |
| ECAP2         | 5024 2100h       |
| ECAP3         | 5024 3100h       |
| ECAP4         | 5024 4100h       |
| ECAP5         | 5024 5100h       |
| ECAP6         | 5024 6100h       |
| ECAP7         | 5024 7100h       |
| ECAP8         | 5024 8100h       |
| ECAP9         | 5024 9100h       |

**Figure 3-244. ECAP\_MUNIT\_2\_CTL Name Register**

|            |    |    |    |         |    |                    |     |
|------------|----|----|----|---------|----|--------------------|-----|
| 31         | 30 | 29 | 28 | 27      | 26 | 25                 | 24  |
| RESERVED_3 |    |    |    |         |    |                    |     |
| R          |    |    |    |         |    |                    |     |
| 0h         |    |    |    |         |    |                    |     |
| 23         | 22 | 21 | 20 | 19      | 18 | 17                 | 16  |
| RESERVED_3 |    |    |    |         |    |                    |     |
| R          |    |    |    |         |    |                    |     |
| 0h         |    |    |    |         |    |                    |     |
| 15         | 14 | 13 | 12 | 11      | 10 | 9                  | 8   |
| RESERVED_2 |    |    |    | MON_SEL |    |                    |     |
| R          |    |    |    | R/W     |    |                    |     |
| 0h         |    |    |    | 0h      |    |                    |     |
| 7          | 6  | 5  | 4  | 3       | 2  | 1                  | 0   |
| RESERVED_1 |    |    |    |         |    | DEBUG_RANG<br>E_EN | EN  |
| R          |    |    |    |         |    | R/W                | R/W |
| 0h         |    |    |    |         |    | 0h                 | 0h  |

**Table 3-749. ECAP\_MUNIT\_2\_CTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED_3 | R    | 0h    | Reserved                                                                                                                                                                                                                                 |
| 15:12 | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                 |
| 11:8  | MON_SEL    | R/W  | 0h    | Type of monitoring<br>0 : High Pulse width<br>1 : Low Pulse width<br>2 : Period width from Rise to Rise<br>3 : Period width from fall to fall<br>4 : Monitor rise edge<br>5 : Monitor fall edge<br>6<br>15 : Reserved [High Pulse width] |

**Table 3-749. ECAP\_MUNIT\_2\_CTL Register Field Descriptions (continued)**

| Bit | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                |
|-----|----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:2 | RESERVED_1     | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                   |
| 1   | DEBUG_RANGE_EN | R/W  | 0h    | Debug mode enable.<br>0 : Debug mode is disabled.<br>1 : Debug mode of monitoring unit 2 is enabled to obtain the variation seen in the system for debug purpose. Range is captured in MUNIT_2_DEBUG_RANGE_MIN and MUNIT_2_DEBUG_RANGE_MAX registers<br>Toggle DEBUG_RANGE_EN to restart this process, this will initialize MUNIT_2_DEBUG_RANGE_MIN and MUNIT_2_DEBUG_RANGE_MAX registers. |
| 0   | EN             | R/W  | 0h    | 0 : Monitoring unit 2 is disabled<br>1 : Monitoring unit 2 is enabled                                                                                                                                                                                                                                                                                                                      |

### 3.6.2.25 ECAP\_MUNIT\_2\_SHADOW\_CTL Register

#### 1 ECAP\_MUNIT\_2\_SHADOW\_CTL Register (Offset = 104h) [reset = 0h]

Shadow control registers for monitoring unit 2

Return to [Summary Table](#)

**Table 3-750. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 0104h       |
| ECAP1         | 5024 1104h       |
| ECAP2         | 5024 2104h       |
| ECAP3         | 5024 3104h       |
| ECAP4         | 5024 4104h       |
| ECAP5         | 5024 5104h       |
| ECAP6         | 5024 6104h       |
| ECAP7         | 5024 7104h       |
| ECAP8         | 5024 8104h       |
| ECAP9         | 5024 9104h       |

**Figure 3-245. ECAP\_MUNIT\_2\_SHADOW\_CTL Name Register**

|            |    |    |    |    |          |        |          |
|------------|----|----|----|----|----------|--------|----------|
| 31         | 30 | 29 | 28 | 27 | 26       | 25     | 24       |
| RESERVED_1 |    |    |    |    |          |        |          |
| R          |    |    |    |    |          |        |          |
| 0h         |    |    |    |    |          |        |          |
| 23         | 22 | 21 | 20 | 19 | 18       | 17     | 16       |
| RESERVED_1 |    |    |    |    |          |        |          |
| R          |    |    |    |    |          |        |          |
| 0h         |    |    |    |    |          |        |          |
| 15         | 14 | 13 | 12 | 11 | 10       | 9      | 8        |
| RESERVED_1 |    |    |    |    |          |        |          |
| R          |    |    |    |    |          |        |          |
| 0h         |    |    |    |    |          |        |          |
| 7          | 6  | 5  | 4  | 3  | 2        | 1      | 0        |
| RESERVED_1 |    |    |    |    | LOADMODE | SWSYNC | SYNCl_EN |
| R          |    |    |    |    | R/W      | R/W1TS | R/W      |
| 0h         |    |    |    |    | 0h       | 0h     | 0h       |

**Table 3-752. ECAP\_MUNIT\_2\_SHADOW\_CTL Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                         |
|------|------------|--------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                            |
| 2    | LOADMODE   | R/W    | 0h    | Load mode<br>0 : Active registers are loaded with shadow on next sync event<br>1 : Active registers are loaded with shadow on EPWMx.GLDLCSTRB event |
| 1    | SWSYNC     | R/W1TS | 0h    | Copies Min and Max values from shadow to active registers immediately if MUNIT_2_SHADOW_CTL.SYNCl_EN is set.                                        |
| 0    | SYNCl_EN   | R/W    | 0h    | Shadow Enable<br>0 : Disabled<br>1 : Enabled                                                                                                        |

### 3.6.2.26 ECAP\_MUNIT\_2\_MIN Register

#### 1 ECAP\_MUNIT\_2\_MIN Register (Offset = 110h) [reset = 0h]

Min value for monitoring unit 2

Return to [Summary Table](#)

**Table 3-753. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 0110h       |
| ECAP1         | 5024 1110h       |
| ECAP2         | 5024 2110h       |
| ECAP3         | 5024 3110h       |
| ECAP4         | 5024 4110h       |
| ECAP5         | 5024 5110h       |
| ECAP6         | 5024 6110h       |
| ECAP7         | 5024 7110h       |
| ECAP8         | 5024 8110h       |
| ECAP9         | 5024 9110h       |

**Figure 3-246. ECAP\_MUNIT\_2\_MIN Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MIN_VALUE |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MIN_VALUE |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MIN_VALUE |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MIN_VALUE |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 3-755. ECAP\_MUNIT\_2\_MIN Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                  |
|------|-----------|------|-------|------------------------------|
| 31:0 | MIN_VALUE | R/W  | 0h    | Minimum value for monitoring |

### 3.6.2.27 ECAP\_MUNIT\_2\_MAX Register

#### 1 ECAP\_MUNIT\_2\_MAX Register (Offset = 114h) [reset = 0h]

Max value for monitoring unit 2

Return to [Summary Table](#)

**Table 3-756. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 0114h       |
| ECAP1         | 5024 1114h       |
| ECAP2         | 5024 2114h       |
| ECAP3         | 5024 3114h       |
| ECAP4         | 5024 4114h       |
| ECAP5         | 5024 5114h       |
| ECAP6         | 5024 6114h       |
| ECAP7         | 5024 7114h       |
| ECAP8         | 5024 8114h       |
| ECAP9         | 5024 9114h       |

**Figure 3-247. ECAP\_MUNIT\_2\_MAX Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MAX_VALUE |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MAX_VALUE |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MAX_VALUE |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MAX_VALUE |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 3-758. ECAP\_MUNIT\_2\_MAX Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                  |
|------|-----------|------|-------|------------------------------|
| 31:0 | MAX_VALUE | R/W  | 0h    | Maximum value for monitoring |

### 3.6.2.28 ECAP\_MUNIT\_2\_MIN\_SHADOW Register

#### 1 ECAP\_MUNIT\_2\_MIN\_SHADOW Register (Offset = 118h) [reset = 0h]

Shadow register for Min value of monitoring unit 2

Return to [Summary Table](#)

**Table 3-759. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 0118h       |
| ECAP1         | 5024 1118h       |
| ECAP2         | 5024 2118h       |
| ECAP3         | 5024 3118h       |
| ECAP4         | 5024 4118h       |
| ECAP5         | 5024 5118h       |
| ECAP6         | 5024 6118h       |
| ECAP7         | 5024 7118h       |
| ECAP8         | 5024 8118h       |
| ECAP9         | 5024 9118h       |

**Figure 3-248. ECAP\_MUNIT\_2\_MIN\_SHADOW Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MIN_VALUE_SHADOW |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MIN_VALUE_SHADOW |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MIN_VALUE_SHADOW |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MIN_VALUE_SHADOW |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-761. ECAP\_MUNIT\_2\_MIN\_SHADOW Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                         |
|------|------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:0 | MIN_VALUE_SHADOW | R/W  | 0h    | Shadow minimum value for monitoring. Shadow value is loaded to active register on Sync event or global load strobe. |



### 3.6.2.29 ECAP\_MUNIT\_2\_MAX\_SHADOW Register

#### 1 ECAP\_MUNIT\_2\_MAX\_SHADOW Register (Offset = 11Ch) [reset = 0h]

Shadow register for Max value of monitoring unit 2

Return to [Summary Table](#)

**Table 3-762. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 011Ch       |
| ECAP1         | 5024 111Ch       |
| ECAP2         | 5024 211Ch       |
| ECAP3         | 5024 311Ch       |
| ECAP4         | 5024 411Ch       |
| ECAP5         | 5024 511Ch       |
| ECAP6         | 5024 611Ch       |
| ECAP7         | 5024 711Ch       |
| ECAP8         | 5024 811Ch       |
| ECAP9         | 5024 911Ch       |

**Figure 3-249. ECAP\_MUNIT\_2\_MAX\_SHADOW Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MAX_VALUE_SHADOW |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MAX_VALUE_SHADOW |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MAX_VALUE_SHADOW |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MAX_VALUE_SHADOW |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-764. ECAP\_MUNIT\_2\_MAX\_SHADOW Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                         |
|------|------------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:0 | MAX_VALUE_SHADOW | R/W  | 0h    | Shadow maximum value for monitoring. Shadow value is loaded to active register on Sync event or global load strobe. |

### 3.6.2.30 ECAP\_MUNIT\_2\_DEBUG\_RANGE\_MIN Register

#### 1 ECAP\_MUNIT\_2\_DEBUG\_RANGE\_MIN Register (Offset = 120h) [reset = FFFFFFFFh]

Observed Min value of check being enabled on minotoring unit 2

Return to [Summary Table](#)

**Table 3-765. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 0120h       |
| ECAP1         | 5024 1120h       |
| ECAP2         | 5024 2120h       |
| ECAP3         | 5024 3120h       |
| ECAP4         | 5024 4120h       |
| ECAP5         | 5024 5120h       |
| ECAP6         | 5024 6120h       |
| ECAP7         | 5024 7120h       |
| ECAP8         | 5024 8120h       |
| ECAP9         | 5024 9120h       |

**Figure 3-250. ECAP\_MUNIT\_2\_DEBUG\_RANGE\_MIN Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MIN_VALUE |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| FFFFFFFh  |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MIN_VALUE |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| FFFFFFFh  |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MIN_VALUE |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| FFFFFFFh  |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MIN_VALUE |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| FFFFFFFh  |    |    |    |    |    |    |    |

**Table 3-767. ECAP\_MUNIT\_2\_DEBUG\_RANGE\_MIN Register Field Descriptions**

| Bit  | Field     | Type | Reset    | Description                                                                                                              |
|------|-----------|------|----------|--------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MIN_VALUE | R    | FFFFFFFh | Observed Min value of check being enabled on minotoring unit 2. Is updated when MUNIT_2_CTL.DEBUG_RANGE_EN is set to '1' |

### 3.6.2.31 ECAP\_MUNIT\_2\_DEBUG\_RANGE\_MAX Register

#### 1 ECAP\_MUNIT\_2\_DEBUG\_RANGE\_MAX Register (Offset = 124h) [reset = 0h]

Observed Max value of check being enabled on minotoring unit 2

Return to [Summary Table](#)

**Table 3-768. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECAP0         | 5024 0124h       |
| ECAP1         | 5024 1124h       |
| ECAP2         | 5024 2124h       |
| ECAP3         | 5024 3124h       |
| ECAP4         | 5024 4124h       |
| ECAP5         | 5024 5124h       |
| ECAP6         | 5024 6124h       |
| ECAP7         | 5024 7124h       |
| ECAP8         | 5024 8124h       |
| ECAP9         | 5024 9124h       |

**Figure 3-251. ECAP\_MUNIT\_2\_DEBUG\_RANGE\_MAX Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MAX_VALUE |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MAX_VALUE |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MAX_VALUE |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MAX_VALUE |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 3-770. ECAP\_MUNIT\_2\_DEBUG\_RANGE\_MAX Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                              |
|------|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MAX_VALUE | R    | 0h    | Observed Min value of check being enabled on minotoring unit 2. Is updated when MUNIT_2_CTL.DEBUG_RANGE_EN is set to '1' |

## 3.7 EPWM

### EPWM

#### 3.7.1 EPWM Summaries

#### EPWM Summaries

**Table 3-771. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM0_G0 Physical Address | EPWM1_G0 Physical Address | EPWM10_G0 Physical Address |
|--------|--------|------------------------------------|---------------------------|---------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5000 0000h                | 5004 0000h                | 5008 0000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5000 0002h                | 5004 0002h                | 5008 0002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5000 0006h                | 5004 0006h                | 5008 0006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5000 0008h                | 5004 0008h                | 5008 0008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5000 000Ah                | 5004 000Ah                | 5008 000Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 5000 000Ch                | 5004 000Ch                | 5008 000Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5000 000Eh                | 5004 000Eh                | 5008 000Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5000 0010h                | 5004 0010h                | 5008 0010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5000 0012h                | 5004 0012h                | 5008 0012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 5000 0018h                | 5004 0018h                | 5008 0018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 5000 001Ah                | 5004 001Ah                | 5008 001Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 5000 0020h                | 5004 0020h                | 5008 0020h                 |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 5000 0022h                | 5004 0022h                | 5008 0022h                 |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 5000 0028h                | 5004 0028h                | 5008 0028h                 |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 5000 0030h                | 5004 0030h                | 5008 0030h                 |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 5000 0032h                | 5004 0032h                | 5008 0032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 5000 0040h                | 5004 0040h                | 5008 0040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 5000 004Eh                | 5004 004Eh                | 5008 004Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>        | 5000 005Ah                | 5004 005Ah                | 5008 005Ah                 |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>         | 5000 005Ch                | 5004 005Ch                | 5008 005Ch                 |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>        | 5000 0068h                | 5004 0068h                | 5008 0068h                 |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>        | 5000 006Ah                | 5004 006Ah                | 5008 006Ah                 |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>     | 5000 0070h                | 5004 0070h                | 5008 0070h                 |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>    | 5000 0074h                | 5004 0074h                | 5008 0074h                 |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>         | 5000 007Ah                | 5004 007Ah                | 5008 007Ah                 |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>       | 5000 007Ch                | 5004 007Ch                | 5008 007Ch                 |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>      | 5000 007Eh                | 5004 007Eh                | 5008 007Eh                 |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>        | 5000 0080h                | 5004 0080h                | 5008 0080h                 |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>       | 5000 0082h                | 5004 0082h                | 5008 0082h                 |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>        | 5000 0084h                | 5004 0084h                | 5008 0084h                 |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>       | 5000 0086h                | 5004 0086h                | 5008 0086h                 |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>        | 5000 008Eh                | 5004 008Eh                | 5008 008Eh                 |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>       | 5000 0092h                | 5004 0092h                | 5008 0092h                 |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>       | 5000 00A0h                | 5004 00A0h                | 5008 00A0h                 |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>         | 5000 00A2h                | 5004 00A2h                | 5008 00A2h                 |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>       | 5000 00A4h                | 5004 00A4h                | 5008 00A4h                 |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>         | 5000 00A6h                | 5004 00A6h                | 5008 00A6h                 |

**Table 3-771. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                     | EPWM0_G0 Physical Address | EPWM1_G0 Physical Address | EPWM10_G0 Physical Address |
|--------|--------|-----------------------------------|---------------------------|---------------------------|----------------------------|
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>        | 5000 00C0h                | 5004 00C0h                | 5008 00C0h                 |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>      | 5000 00C4h                | 5004 00C4h                | 5008 00C4h                 |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>        | 5000 00C6h                | 5004 00C6h                | 5008 00C6h                 |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>     | 5000 00C8h                | 5004 00C8h                | 5008 00C8h                 |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>         | 5000 00D4h                | 5004 00D4h                | 5008 00D4h                 |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>         | 5000 00D8h                | 5004 00D8h                | 5008 00D8h                 |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>         | 5000 00DEh                | 5004 00DEh                | 5008 00DEh                 |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>         | 5000 00E2h                | 5004 00E2h                | 5008 00E2h                 |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>      | 5000 00E8h                | 5004 00E8h                | 5008 00E8h                 |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>    | 5000 00EEh                | 5004 00EEh                | 5008 00EEh                 |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>        | 5000 0100h                | 5004 0100h                | 5008 0100h                 |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>       | 5000 0102h                | 5004 0102h                | 5008 0102h                 |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>      | 5000 0104h                | 5004 0104h                | 5008 0104h                 |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>        | 5000 0108h                | 5004 0108h                | 5008 0108h                 |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>       | 5000 010Ah                | 5004 010Ah                | 5008 010Ah                 |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>     | 5000 010Ch                | 5004 010Ch                | 5008 010Ch                 |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>     | 5000 010Eh                | 5004 010Eh                | 5008 010Eh                 |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>       | 5000 011Ah                | 5004 011Ah                | 5008 011Ah                 |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>        | 5000 0126h                | 5004 0126h                | 5008 0126h                 |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>     | 5000 0128h                | 5004 0128h                | 5008 0128h                 |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>     | 5000 012Ah                | 5004 012Ah                | 5008 012Ah                 |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>        | 5000 012Eh                | 5004 012Eh                | 5008 012Eh                 |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>     | 5000 0130h                | 5004 0130h                | 5008 0130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>     | 5000 0132h                | 5004 0132h                | 5008 0132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>        | 5000 0136h                | 5004 0136h                | 5008 0136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a> | 5000 013Ah                | 5004 013Ah                | 5008 013Ah                 |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>        | 5000 0148h                | 5004 0148h                | 5008 0148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>         | 5000 014Ch                | 5004 014Ch                | 5008 014Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>        | 5000 0150h                | 5004 0150h                | 5008 0150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>        | 5000 0154h                | 5004 0154h                | 5008 0154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>        | 5000 0158h                | 5004 0158h                | 5008 0158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>      | 5000 015Ch                | 5004 015Ch                | 5008 015Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>      | 5000 0160h                | 5004 0160h                | 5008 0160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a> | 5000 0164h                | 5004 0164h                | 5008 0164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>    | 5000 0168h                | 5004 0168h                | 5008 0168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>   | 5000 016Ch                | 5004 016Ch                | 5008 016Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>  | 5000 0170h                | 5004 0170h                | 5008 0170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>  | 5000 0174h                | 5004 0174h                | 5008 0174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>    | 5000 0180h                | 5004 0180h                | 5008 0180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>       | 5000 0186h                | 5004 0186h                | 5008 0186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>       | 5000 0188h                | 5004 0188h                | 5008 0188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>       | 5000 018Eh                | 5004 018Eh                | 5008 018Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>     | 5000 0190h                | 5004 0190h                | 5008 0190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>    | 5000 0192h                | 5004 0192h                | 5008 0192h                 |

**Table 3-771. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM0_G0 Physical Address | EPWM1_G0 Physical Address | EPWM10_G0 Physical Address |
|--------|--------|---------------------------------------|---------------------------|---------------------------|----------------------------|
| 194h   | 16     | <a href="#">EPWM_DCFFSETCNT</a>       | 5000 0194h                | 5004 0194h                | 5008 0194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5000 0196h                | 5004 0196h                | 5008 0196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5000 0198h                | 5004 0198h                | 5008 0198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5000 019Ah                | 5004 019Ah                | 5008 019Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5000 019Ch                | 5004 019Ch                | 5008 019Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5000 019Eh                | 5004 019Eh                | 5008 019Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5000 01A4h                | 5004 01A4h                | 5008 01A4h                 |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5000 01A6h                | 5004 01A6h                | 5008 01A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 5000 01A8h                | 5004 01A8h                | 5008 01A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 5000 01AAh                | 5004 01AAh                | 5008 01AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 5000 01ACh                | 5004 01ACh                | 5008 01ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 5000 01AEh                | 5004 01AEh                | 5008 01AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 5000 01B0h                | 5004 01B0h                | 5008 01B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 5000 01B2h                | 5004 01B2h                | 5008 01B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 5000 01F4h                | 5004 01F4h                | 5008 01F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 5000 01FAh                | 5004 01FAh                | 5008 01FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 5000 01FCh                | 5004 01FCh                | 5008 01FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>         | 5000 0400h                | 5004 0400h                | 5008 0400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>         | 5000 0410h                | 5004 0410h                | 5008 0410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>            | 5000 0418h                | 5004 0418h                | 5008 0418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a>   | 5000 041Ch                | 5004 041Ch                | 5008 041Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>     | 5000 0420h                | 5004 0420h                | 5008 0420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>     | 5000 0428h                | 5004 0428h                | 5008 0428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>     | 5000 0430h                | 5004 0430h                | 5008 0430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>     | 5000 0600h                | 5004 0600h                | 5008 0600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>     | 5000 0604h                | 5004 0604h                | 5008 0604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>     | 5000 0608h                | 5004 0608h                | 5008 0608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>     | 5000 060Ch                | 5004 060Ch                | 5008 060Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>     | 5000 0610h                | 5004 0610h                | 5008 0610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>     | 5000 0614h                | 5004 0614h                | 5008 0614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>     | 5000 0618h                | 5004 0618h                | 5008 0618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>     | 5000 061Ch                | 5004 061Ch                | 5008 061Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>    | 5000 0620h                | 5004 0620h                | 5008 0620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a>   | 5000 0630h                | 5004 0630h                | 5008 0630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a>   | 5000 0632h                | 5004 0632h                | 5008 0632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a>   | 5000 0644h                | 5004 0644h                | 5008 0644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>      | 5000 0680h                | 5004 0680h                | 5008 0680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>      | 5000 0684h                | 5004 0684h                | 5008 0684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>      | 5000 0688h                | 5004 0688h                | 5008 0688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>      | 5000 068Ch                | 5004 068Ch                | 5008 068Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>      | 5000 0690h                | 5004 0690h                | 5008 0690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>      | 5000 0694h                | 5004 0694h                | 5008 0694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>      | 5000 0698h                | 5004 0698h                | 5008 0698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>      | 5000 069Ch                | 5004 069Ch                | 5008 069Ch                 |

**Table 3-771. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM0_G0 Physical Address | EPWM1_G0 Physical Address | EPWM10_G0 Physical Address |
|--------|--------|------------------------------------|---------------------------|---------------------------|----------------------------|
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>  | 5000 06A0h                | 5004 06A0h                | 5008 06A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a> | 5000 06B0h                | 5004 06B0h                | 5008 06B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a> | 5000 06B2h                | 5004 06B2h                | 5008 06B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>    | 5000 06BAh                | 5004 06BAh                | 5008 06BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>    | 5000 06BEh                | 5004 06BEh                | 5008 06BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a> | 5000 06C4h                | 5004 06C4h                | 5008 06C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>   | 5000 0700h                | 5004 0700h                | 5008 0700h                 |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>   | 5000 0704h                | 5004 0704h                | 5008 0704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>   | 5000 0708h                | 5004 0708h                | 5008 0708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>   | 5000 070Ch                | 5004 070Ch                | 5008 070Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>   | 5000 0710h                | 5004 0710h                | 5008 0710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>   | 5000 0714h                | 5004 0714h                | 5008 0714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>   | 5000 0718h                | 5004 0718h                | 5008 0718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>   | 5000 071Ch                | 5004 071Ch                | 5008 071Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>  | 5000 0720h                | 5004 0720h                | 5008 0720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a> | 5000 0730h                | 5004 0730h                | 5008 0730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a> | 5000 0732h                | 5004 0732h                | 5008 0732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>    | 5000 073Ah                | 5004 073Ah                | 5008 073Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>    | 5000 073Eh                | 5004 073Eh                | 5008 073Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a> | 5000 0744h                | 5004 0744h                | 5008 0744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 5000 0780h                | 5004 0780h                | 5008 0780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 5000 0784h                | 5004 0784h                | 5008 0784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 5000 0788h                | 5004 0788h                | 5008 0788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 5000 078Ch                | 5004 078Ch                | 5008 078Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 5000 0790h                | 5004 0790h                | 5008 0790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 5000 0794h                | 5004 0794h                | 5008 0794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 5000 0798h                | 5004 0798h                | 5008 0798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 5000 079Ch                | 5004 079Ch                | 5008 079Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 5000 07A0h                | 5004 07A0h                | 5008 07A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5000 07B0h                | 5004 07B0h                | 5008 07B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5000 07B2h                | 5004 07B2h                | 5008 07B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5000 07BAh                | 5004 07BAh                | 5008 07BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5000 07BEh                | 5004 07BEh                | 5008 07BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5000 07C4h                | 5004 07C4h                | 5008 07C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5000 0800h                | 5004 0800h                | 5008 0800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5000 0804h                | 5004 0804h                | 5008 0804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5000 0808h                | 5004 0808h                | 5008 0808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5000 080Ch                | 5004 080Ch                | 5008 080Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 5000 0810h                | 5004 0810h                | 5008 0810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5000 0814h                | 5004 0814h                | 5008 0814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 5000 0820h                | 5004 0820h                | 5008 0820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 5000 0824h                | 5004 0824h                | 5008 0824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 5000 0828h                | 5004 0828h                | 5008 0828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 5000 082Ch                | 5004 082Ch                | 5008 082Ch                 |

**Table 3-771. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                  | EPWM0_G0 Physical Address | EPWM1_G0 Physical Address | EPWM10_G0 Physical Address |
|--------|--------|--------------------------------|---------------------------|---------------------------|----------------------------|
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a> | 5000 0C00h                | 5004 0C00h                | 5008 0C00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>  | 5000 0C04h                | 5004 0C04h                | 5008 0C04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>   | 5000 0C20h                | 5004 0C20h                | 5008 0C20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>   | 5000 0C24h                | 5004 0C24h                | 5008 0C24h                 |

**Table 3-772. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM11_G0 Physical Address | EPWM12_G0 Physical Address | EPWM13_G0 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 500C 0000h                 | 5000 1000h                 | 5004 1000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 500C 0002h                 | 5000 1002h                 | 5004 1002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 500C 0006h                 | 5000 1006h                 | 5004 1006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 500C 0008h                 | 5000 1008h                 | 5004 1008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 500C 000Ah                 | 5000 100Ah                 | 5004 100Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 500C 000Ch                 | 5000 100Ch                 | 5004 100Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 500C 000Eh                 | 5000 100Eh                 | 5004 100Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 500C 0010h                 | 5000 1010h                 | 5004 1010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 500C 0012h                 | 5000 1012h                 | 5004 1012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 500C 0018h                 | 5000 1018h                 | 5004 1018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 500C 001Ah                 | 5000 101Ah                 | 5004 101Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 500C 0020h                 | 5000 1020h                 | 5004 1020h                 |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 500C 0022h                 | 5000 1022h                 | 5004 1022h                 |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 500C 0028h                 | 5000 1028h                 | 5004 1028h                 |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 500C 0030h                 | 5000 1030h                 | 5004 1030h                 |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 500C 0032h                 | 5000 1032h                 | 5004 1032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 500C 0040h                 | 5000 1040h                 | 5004 1040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 500C 004Eh                 | 5000 104Eh                 | 5004 104Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>        | 500C 005Ah                 | 5000 105Ah                 | 5004 105Ah                 |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>         | 500C 005Ch                 | 5000 105Ch                 | 5004 105Ch                 |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>        | 500C 0068h                 | 5000 1068h                 | 5004 1068h                 |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>        | 500C 006Ah                 | 5000 106Ah                 | 5004 106Ah                 |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>     | 500C 0070h                 | 5000 1070h                 | 5004 1070h                 |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>    | 500C 0074h                 | 5000 1074h                 | 5004 1074h                 |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>         | 500C 007Ah                 | 5000 107Ah                 | 5004 107Ah                 |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>       | 500C 007Ch                 | 5000 107Ch                 | 5004 107Ch                 |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>      | 500C 007Eh                 | 5000 107Eh                 | 5004 107Eh                 |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>        | 500C 0080h                 | 5000 1080h                 | 5004 1080h                 |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>       | 500C 0082h                 | 5000 1082h                 | 5004 1082h                 |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>        | 500C 0084h                 | 5000 1084h                 | 5004 1084h                 |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>       | 500C 0086h                 | 5000 1086h                 | 5004 1086h                 |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>        | 500C 008Eh                 | 5000 108Eh                 | 5004 108Eh                 |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>       | 500C 0092h                 | 5000 1092h                 | 5004 1092h                 |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>       | 500C 00A0h                 | 5000 10A0h                 | 5004 10A0h                 |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>         | 500C 00A2h                 | 5000 10A2h                 | 5004 10A2h                 |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>       | 500C 00A4h                 | 5000 10A4h                 | 5004 10A4h                 |



**Table 3-772. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                     | EPWM11_G0 Physical Address | EPWM12_G0 Physical Address | EPWM13_G0 Physical Address |
|--------|--------|-----------------------------------|----------------------------|----------------------------|----------------------------|
| A6h    | 16     | <a href="#">EPWM_DBFED</a>        | 500C 00A6h                 | 5000 10A6h                 | 5004 10A6h                 |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>        | 500C 00C0h                 | 5000 10C0h                 | 5004 10C0h                 |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>      | 500C 00C4h                 | 5000 10C4h                 | 5004 10C4h                 |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>        | 500C 00C6h                 | 5000 10C6h                 | 5004 10C6h                 |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>     | 500C 00C8h                 | 5000 10C8h                 | 5004 10C8h                 |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>         | 500C 00D4h                 | 5000 10D4h                 | 5004 10D4h                 |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>         | 500C 00D8h                 | 5000 10D8h                 | 5004 10D8h                 |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>         | 500C 00DEh                 | 5000 10DEh                 | 5004 10DEh                 |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>         | 500C 00E2h                 | 5000 10E2h                 | 5004 10E2h                 |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>      | 500C 00E8h                 | 5000 10E8h                 | 5004 10E8h                 |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>    | 500C 00EEh                 | 5000 10EEh                 | 5004 10EEh                 |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>        | 500C 0100h                 | 5000 1100h                 | 5004 1100h                 |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>       | 500C 0102h                 | 5000 1102h                 | 5004 1102h                 |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>      | 500C 0104h                 | 5000 1104h                 | 5004 1104h                 |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>        | 500C 0108h                 | 5000 1108h                 | 5004 1108h                 |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>       | 500C 010Ah                 | 5000 110Ah                 | 5004 110Ah                 |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>     | 500C 010Ch                 | 5000 110Ch                 | 5004 110Ch                 |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>     | 500C 010Eh                 | 5000 110Eh                 | 5004 110Eh                 |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>       | 500C 011Ah                 | 5000 111Ah                 | 5004 111Ah                 |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>        | 500C 0126h                 | 5000 1126h                 | 5004 1126h                 |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>     | 500C 0128h                 | 5000 1128h                 | 5004 1128h                 |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>     | 500C 012Ah                 | 5000 112Ah                 | 5004 112Ah                 |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>        | 500C 012Eh                 | 5000 112Eh                 | 5004 112Eh                 |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>     | 500C 0130h                 | 5000 1130h                 | 5004 1130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>     | 500C 0132h                 | 5000 1132h                 | 5004 1132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>        | 500C 0136h                 | 5000 1136h                 | 5004 1136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a> | 500C 013Ah                 | 5000 113Ah                 | 5004 113Ah                 |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>        | 500C 0148h                 | 5000 1148h                 | 5004 1148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>         | 500C 014Ch                 | 5000 114Ch                 | 5004 114Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>        | 500C 0150h                 | 5000 1150h                 | 5004 1150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>        | 500C 0154h                 | 5000 1154h                 | 5004 1154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>        | 500C 0158h                 | 5000 1158h                 | 5004 1158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>      | 500C 015Ch                 | 5000 115Ch                 | 5004 115Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>      | 500C 0160h                 | 5000 1160h                 | 5004 1160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a> | 500C 0164h                 | 5000 1164h                 | 5004 1164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>    | 500C 0168h                 | 5000 1168h                 | 5004 1168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>   | 500C 016Ch                 | 5000 116Ch                 | 5004 116Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>  | 500C 0170h                 | 5000 1170h                 | 5004 1170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>  | 500C 0174h                 | 5000 1174h                 | 5004 1174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>    | 500C 0180h                 | 5000 1180h                 | 5004 1180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>       | 500C 0186h                 | 5000 1186h                 | 5004 1186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>       | 500C 0188h                 | 5000 1188h                 | 5004 1188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>       | 500C 018Eh                 | 5000 118Eh                 | 5004 118Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>     | 500C 0190h                 | 5000 1190h                 | 5004 1190h                 |

**Table 3-772. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM11_G0 Physical Address | EPWM12_G0 Physical Address | EPWM13_G0 Physical Address |
|--------|--------|---------------------------------------|----------------------------|----------------------------|----------------------------|
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 500C 0192h                 | 5000 1192h                 | 5004 1192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 500C 0194h                 | 5000 1194h                 | 5004 1194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 500C 0196h                 | 5000 1196h                 | 5004 1196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 500C 0198h                 | 5000 1198h                 | 5004 1198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 500C 019Ah                 | 5000 119Ah                 | 5004 119Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 500C 019Ch                 | 5000 119Ch                 | 5004 119Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 500C 019Eh                 | 5000 119Eh                 | 5004 119Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 500C 01A4h                 | 5000 11A4h                 | 5004 11A4h                 |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 500C 01A6h                 | 5000 11A6h                 | 5004 11A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 500C 01A8h                 | 5000 11A8h                 | 5004 11A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 500C 01AAh                 | 5000 11AAh                 | 5004 11AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 500C 01ACh                 | 5000 11ACh                 | 5004 11ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 500C 01AEh                 | 5000 11AEh                 | 5004 11AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 500C 01B0h                 | 5000 11B0h                 | 5004 11B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 500C 01B2h                 | 5000 11B2h                 | 5004 11B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 500C 01F4h                 | 5000 11F4h                 | 5004 11F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 500C 01FAh                 | 5000 11FAh                 | 5004 11FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 500C 01FCh                 | 5000 11FCh                 | 5004 11FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>         | 500C 0400h                 | 5000 1400h                 | 5004 1400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>         | 500C 0410h                 | 5000 1410h                 | 5004 1410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>            | 500C 0418h                 | 5000 1418h                 | 5004 1418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a>   | 500C 041Ch                 | 5000 141Ch                 | 5004 141Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>     | 500C 0420h                 | 5000 1420h                 | 5004 1420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>     | 500C 0428h                 | 5000 1428h                 | 5004 1428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>     | 500C 0430h                 | 5000 1430h                 | 5004 1430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>     | 500C 0600h                 | 5000 1600h                 | 5004 1600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>     | 500C 0604h                 | 5000 1604h                 | 5004 1604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>     | 500C 0608h                 | 5000 1608h                 | 5004 1608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>     | 500C 060Ch                 | 5000 160Ch                 | 5004 160Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>     | 500C 0610h                 | 5000 1610h                 | 5004 1610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>     | 500C 0614h                 | 5000 1614h                 | 5004 1614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>     | 500C 0618h                 | 5000 1618h                 | 5004 1618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>     | 500C 061Ch                 | 5000 161Ch                 | 5004 161Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>    | 500C 0620h                 | 5000 1620h                 | 5004 1620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a>   | 500C 0630h                 | 5000 1630h                 | 5004 1630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a>   | 500C 0632h                 | 5000 1632h                 | 5004 1632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a>   | 500C 0644h                 | 5000 1644h                 | 5004 1644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>      | 500C 0680h                 | 5000 1680h                 | 5004 1680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>      | 500C 0684h                 | 5000 1684h                 | 5004 1684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>      | 500C 0688h                 | 5000 1688h                 | 5004 1688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>      | 500C 068Ch                 | 5000 168Ch                 | 5004 168Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>      | 500C 0690h                 | 5000 1690h                 | 5004 1690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>      | 500C 0694h                 | 5000 1694h                 | 5004 1694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>      | 500C 0698h                 | 5000 1698h                 | 5004 1698h                 |

**Table 3-772. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM11_G0 Physical Address | EPWM12_G0 Physical Address | EPWM13_G0 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>   | 500C 069Ch                 | 5000 169Ch                 | 5004 169Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>  | 500C 06A0h                 | 5000 16A0h                 | 5004 16A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a> | 500C 06B0h                 | 5000 16B0h                 | 5004 16B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a> | 500C 06B2h                 | 5000 16B2h                 | 5004 16B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>    | 500C 06BAh                 | 5000 16BAh                 | 5004 16BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>    | 500C 06BEh                 | 5000 16BEh                 | 5004 16BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a> | 500C 06C4h                 | 5000 16C4h                 | 5004 16C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>   | 500C 0700h                 | 5000 1700h                 | 5004 1700h                 |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>   | 500C 0704h                 | 5000 1704h                 | 5004 1704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>   | 500C 0708h                 | 5000 1708h                 | 5004 1708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>   | 500C 070Ch                 | 5000 170Ch                 | 5004 170Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>   | 500C 0710h                 | 5000 1710h                 | 5004 1710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>   | 500C 0714h                 | 5000 1714h                 | 5004 1714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>   | 500C 0718h                 | 5000 1718h                 | 5004 1718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>   | 500C 071Ch                 | 5000 171Ch                 | 5004 171Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>  | 500C 0720h                 | 5000 1720h                 | 5004 1720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a> | 500C 0730h                 | 5000 1730h                 | 5004 1730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a> | 500C 0732h                 | 5000 1732h                 | 5004 1732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>    | 500C 073Ah                 | 5000 173Ah                 | 5004 173Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>    | 500C 073Eh                 | 5000 173Eh                 | 5004 173Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a> | 500C 0744h                 | 5000 1744h                 | 5004 1744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 500C 0780h                 | 5000 1780h                 | 5004 1780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 500C 0784h                 | 5000 1784h                 | 5004 1784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 500C 0788h                 | 5000 1788h                 | 5004 1788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 500C 078Ch                 | 5000 178Ch                 | 5004 178Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 500C 0790h                 | 5000 1790h                 | 5004 1790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 500C 0794h                 | 5000 1794h                 | 5004 1794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 500C 0798h                 | 5000 1798h                 | 5004 1798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 500C 079Ch                 | 5000 179Ch                 | 5004 179Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 500C 07A0h                 | 5000 17A0h                 | 5004 17A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 500C 07B0h                 | 5000 17B0h                 | 5004 17B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 500C 07B2h                 | 5000 17B2h                 | 5004 17B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 500C 07BAh                 | 5000 17BAh                 | 5004 17BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 500C 07BEh                 | 5000 17BEh                 | 5004 17BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 500C 07C4h                 | 5000 17C4h                 | 5004 17C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 500C 0800h                 | 5000 1800h                 | 5004 1800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 500C 0804h                 | 5000 1804h                 | 5004 1804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 500C 0808h                 | 5000 1808h                 | 5004 1808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 500C 080Ch                 | 5000 180Ch                 | 5004 180Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 500C 0810h                 | 5000 1810h                 | 5004 1810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 500C 0814h                 | 5000 1814h                 | 5004 1814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 500C 0820h                 | 5000 1820h                 | 5004 1820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 500C 0824h                 | 5000 1824h                 | 5004 1824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 500C 0828h                 | 5000 1828h                 | 5004 1828h                 |

**Table 3-772. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                   | EPWM11_G0 Physical Address | EPWM12_G0 Physical Address | EPWM13_G0 Physical Address |
|--------|--------|---------------------------------|----------------------------|----------------------------|----------------------------|
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a> | 500C 082Ch                 | 5000 182Ch                 | 5004 182Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>  | 500C 0C00h                 | 5000 1C00h                 | 5004 1C00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>   | 500C 0C04h                 | 5000 1C04h                 | 5004 1C04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>    | 500C 0C20h                 | 5000 1C20h                 | 5004 1C20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>    | 500C 0C24h                 | 5000 1C24h                 | 5004 1C24h                 |

**Table 3-773. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM14_G0 Physical Address | EPWM15_G0 Physical Address | EPWM16_G0 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5008 1000h                 | 500C 1000h                 | 5000 2000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5008 1002h                 | 500C 1002h                 | 5000 2002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5008 1006h                 | 500C 1006h                 | 5000 2006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5008 1008h                 | 500C 1008h                 | 5000 2008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5008 100Ah                 | 500C 100Ah                 | 5000 200Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 5008 100Ch                 | 500C 100Ch                 | 5000 200Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5008 100Eh                 | 500C 100Eh                 | 5000 200Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5008 1010h                 | 500C 1010h                 | 5000 2010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5008 1012h                 | 500C 1012h                 | 5000 2012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 5008 1018h                 | 500C 1018h                 | 5000 2018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 5008 101Ah                 | 500C 101Ah                 | 5000 201Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 5008 1020h                 | 500C 1020h                 | 5000 2020h                 |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 5008 1022h                 | 500C 1022h                 | 5000 2022h                 |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 5008 1028h                 | 500C 1028h                 | 5000 2028h                 |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 5008 1030h                 | 500C 1030h                 | 5000 2030h                 |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 5008 1032h                 | 500C 1032h                 | 5000 2032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 5008 1040h                 | 500C 1040h                 | 5000 2040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 5008 104Eh                 | 500C 104Eh                 | 5000 204Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>        | 5008 105Ah                 | 500C 105Ah                 | 5000 205Ah                 |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>         | 5008 105Ch                 | 500C 105Ch                 | 5000 205Ch                 |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>        | 5008 1068h                 | 500C 1068h                 | 5000 2068h                 |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>        | 5008 106Ah                 | 500C 106Ah                 | 5000 206Ah                 |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>     | 5008 1070h                 | 500C 1070h                 | 5000 2070h                 |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>    | 5008 1074h                 | 500C 1074h                 | 5000 2074h                 |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>         | 5008 107Ah                 | 500C 107Ah                 | 5000 207Ah                 |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>       | 5008 107Ch                 | 500C 107Ch                 | 5000 207Ch                 |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>      | 5008 107Eh                 | 500C 107Eh                 | 5000 207Eh                 |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>        | 5008 1080h                 | 500C 1080h                 | 5000 2080h                 |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>       | 5008 1082h                 | 500C 1082h                 | 5000 2082h                 |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>        | 5008 1084h                 | 500C 1084h                 | 5000 2084h                 |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>       | 5008 1086h                 | 500C 1086h                 | 5000 2086h                 |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRFC</a>       | 5008 108Eh                 | 500C 108Eh                 | 5000 208Eh                 |
| 92h    | 16     | <a href="#">EPWM_AQCSFRFC</a>      | 5008 1092h                 | 500C 1092h                 | 5000 2092h                 |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>       | 5008 10A0h                 | 500C 10A0h                 | 5000 20A0h                 |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>         | 5008 10A2h                 | 500C 10A2h                 | 5000 20A2h                 |

**Table 3-773. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                     | EPWM14_G0 Physical Address | EPWM15_G0 Physical Address | EPWM16_G0 Physical Address |
|--------|--------|-----------------------------------|----------------------------|----------------------------|----------------------------|
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>      | 5008 10A4h                 | 500C 10A4h                 | 5000 20A4h                 |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>        | 5008 10A6h                 | 500C 10A6h                 | 5000 20A6h                 |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>        | 5008 10C0h                 | 500C 10C0h                 | 5000 20C0h                 |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>      | 5008 10C4h                 | 500C 10C4h                 | 5000 20C4h                 |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>        | 5008 10C6h                 | 500C 10C6h                 | 5000 20C6h                 |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>     | 5008 10C8h                 | 500C 10C8h                 | 5000 20C8h                 |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>         | 5008 10D4h                 | 500C 10D4h                 | 5000 20D4h                 |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>         | 5008 10D8h                 | 500C 10D8h                 | 5000 20D8h                 |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>         | 5008 10DEh                 | 500C 10DEh                 | 5000 20DEh                 |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>         | 5008 10E2h                 | 500C 10E2h                 | 5000 20E2h                 |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>      | 5008 10E8h                 | 500C 10E8h                 | 5000 20E8h                 |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>    | 5008 10EEh                 | 500C 10EEh                 | 5000 20EEh                 |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>        | 5008 1100h                 | 500C 1100h                 | 5000 2100h                 |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>       | 5008 1102h                 | 500C 1102h                 | 5000 2102h                 |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>      | 5008 1104h                 | 500C 1104h                 | 5000 2104h                 |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>        | 5008 1108h                 | 500C 1108h                 | 5000 2108h                 |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>       | 5008 110Ah                 | 500C 110Ah                 | 5000 210Ah                 |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>     | 5008 110Ch                 | 500C 110Ch                 | 5000 210Ch                 |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>     | 5008 110Eh                 | 500C 110Eh                 | 5000 210Eh                 |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>       | 5008 111Ah                 | 500C 111Ah                 | 5000 211Ah                 |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>        | 5008 1126h                 | 500C 1126h                 | 5000 2126h                 |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>     | 5008 1128h                 | 500C 1128h                 | 5000 2128h                 |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>     | 5008 112Ah                 | 500C 112Ah                 | 5000 212Ah                 |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>        | 5008 112Eh                 | 500C 112Eh                 | 5000 212Eh                 |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>     | 5008 1130h                 | 500C 1130h                 | 5000 2130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>     | 5008 1132h                 | 500C 1132h                 | 5000 2132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>        | 5008 1136h                 | 500C 1136h                 | 5000 2136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a> | 5008 113Ah                 | 500C 113Ah                 | 5000 213Ah                 |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>        | 5008 1148h                 | 500C 1148h                 | 5000 2148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>         | 5008 114Ch                 | 500C 114Ch                 | 5000 214Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>        | 5008 1150h                 | 500C 1150h                 | 5000 2150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>        | 5008 1154h                 | 500C 1154h                 | 5000 2154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>        | 5008 1158h                 | 500C 1158h                 | 5000 2158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>      | 5008 115Ch                 | 500C 115Ch                 | 5000 215Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>      | 5008 1160h                 | 500C 1160h                 | 5000 2160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a> | 5008 1164h                 | 500C 1164h                 | 5000 2164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>    | 5008 1168h                 | 500C 1168h                 | 5000 2168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>   | 5008 116Ch                 | 500C 116Ch                 | 5000 216Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>  | 5008 1170h                 | 500C 1170h                 | 5000 2170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>  | 5008 1174h                 | 500C 1174h                 | 5000 2174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>    | 5008 1180h                 | 500C 1180h                 | 5000 2180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>       | 5008 1186h                 | 500C 1186h                 | 5000 2186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>       | 5008 1188h                 | 500C 1188h                 | 5000 2188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>       | 5008 118Eh                 | 500C 118Eh                 | 5000 218Eh                 |

**Table 3-773. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM14_G0 Physical Address | EPWM15_G0 Physical Address | EPWM16_G0 Physical Address |
|--------|--------|---------------------------------------|----------------------------|----------------------------|----------------------------|
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5008 1190h                 | 500C 1190h                 | 5000 2190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5008 1192h                 | 500C 1192h                 | 5000 2192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5008 1194h                 | 500C 1194h                 | 5000 2194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5008 1196h                 | 500C 1196h                 | 5000 2196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5008 1198h                 | 500C 1198h                 | 5000 2198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5008 119Ah                 | 500C 119Ah                 | 5000 219Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5008 119Ch                 | 500C 119Ch                 | 5000 219Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5008 119Eh                 | 500C 119Eh                 | 5000 219Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5008 11A4h                 | 500C 11A4h                 | 5000 21A4h                 |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5008 11A6h                 | 500C 11A6h                 | 5000 21A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 5008 11A8h                 | 500C 11A8h                 | 5000 21A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 5008 11AAh                 | 500C 11AAh                 | 5000 21AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 5008 11ACh                 | 500C 11ACh                 | 5000 21ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 5008 11AEh                 | 500C 11AEh                 | 5000 21AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 5008 11B0h                 | 500C 11B0h                 | 5000 21B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 5008 11B2h                 | 500C 11B2h                 | 5000 21B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 5008 11F4h                 | 500C 11F4h                 | 5000 21F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 5008 11FAh                 | 500C 11FAh                 | 5000 21FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 5008 11FCh                 | 500C 11FCh                 | 5000 21FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>         | 5008 1400h                 | 500C 1400h                 | 5000 2400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>         | 5008 1410h                 | 500C 1410h                 | 5000 2410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>            | 5008 1418h                 | 500C 1418h                 | 5000 2418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a>   | 5008 141Ch                 | 500C 141Ch                 | 5000 241Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>     | 5008 1420h                 | 500C 1420h                 | 5000 2420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>     | 5008 1428h                 | 500C 1428h                 | 5000 2428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>     | 5008 1430h                 | 500C 1430h                 | 5000 2430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>     | 5008 1600h                 | 500C 1600h                 | 5000 2600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>     | 5008 1604h                 | 500C 1604h                 | 5000 2604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>     | 5008 1608h                 | 500C 1608h                 | 5000 2608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>     | 5008 160Ch                 | 500C 160Ch                 | 5000 260Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>     | 5008 1610h                 | 500C 1610h                 | 5000 2610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>     | 5008 1614h                 | 500C 1614h                 | 5000 2614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>     | 5008 1618h                 | 500C 1618h                 | 5000 2618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>     | 5008 161Ch                 | 500C 161Ch                 | 5000 261Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>    | 5008 1620h                 | 500C 1620h                 | 5000 2620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a>   | 5008 1630h                 | 500C 1630h                 | 5000 2630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a>   | 5008 1632h                 | 500C 1632h                 | 5000 2632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a>   | 5008 1644h                 | 500C 1644h                 | 5000 2644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>      | 5008 1680h                 | 500C 1680h                 | 5000 2680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>      | 5008 1684h                 | 500C 1684h                 | 5000 2684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>      | 5008 1688h                 | 500C 1688h                 | 5000 2688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>      | 5008 168Ch                 | 500C 168Ch                 | 5000 268Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>      | 5008 1690h                 | 500C 1690h                 | 5000 2690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>      | 5008 1694h                 | 500C 1694h                 | 5000 2694h                 |

**Table 3-773. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM14_G0 Physical Address | EPWM15_G0 Physical Address | EPWM16_G0 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>   | 5008 1698h                 | 500C 1698h                 | 5000 2698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>   | 5008 169Ch                 | 500C 169Ch                 | 5000 269Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>  | 5008 16A0h                 | 500C 16A0h                 | 5000 26A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a> | 5008 16B0h                 | 500C 16B0h                 | 5000 26B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a> | 5008 16B2h                 | 500C 16B2h                 | 5000 26B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>    | 5008 16BAh                 | 500C 16BAh                 | 5000 26BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>    | 5008 16BEh                 | 500C 16BEh                 | 5000 26BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a> | 5008 16C4h                 | 500C 16C4h                 | 5000 26C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>   | 5008 1700h                 | 500C 1700h                 | 5000 2700h                 |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>   | 5008 1704h                 | 500C 1704h                 | 5000 2704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>   | 5008 1708h                 | 500C 1708h                 | 5000 2708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>   | 5008 170Ch                 | 500C 170Ch                 | 5000 270Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>   | 5008 1710h                 | 500C 1710h                 | 5000 2710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>   | 5008 1714h                 | 500C 1714h                 | 5000 2714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>   | 5008 1718h                 | 500C 1718h                 | 5000 2718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>   | 5008 171Ch                 | 500C 171Ch                 | 5000 271Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>  | 5008 1720h                 | 500C 1720h                 | 5000 2720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a> | 5008 1730h                 | 500C 1730h                 | 5000 2730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a> | 5008 1732h                 | 500C 1732h                 | 5000 2732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>    | 5008 173Ah                 | 500C 173Ah                 | 5000 273Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>    | 5008 173Eh                 | 500C 173Eh                 | 5000 273Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a> | 5008 1744h                 | 500C 1744h                 | 5000 2744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 5008 1780h                 | 500C 1780h                 | 5000 2780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 5008 1784h                 | 500C 1784h                 | 5000 2784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 5008 1788h                 | 500C 1788h                 | 5000 2788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 5008 178Ch                 | 500C 178Ch                 | 5000 278Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 5008 1790h                 | 500C 1790h                 | 5000 2790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 5008 1794h                 | 500C 1794h                 | 5000 2794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 5008 1798h                 | 500C 1798h                 | 5000 2798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 5008 179Ch                 | 500C 179Ch                 | 5000 279Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 5008 17A0h                 | 500C 17A0h                 | 5000 27A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5008 17B0h                 | 500C 17B0h                 | 5000 27B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5008 17B2h                 | 500C 17B2h                 | 5000 27B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5008 17BAh                 | 500C 17BAh                 | 5000 27BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5008 17BEh                 | 500C 17BEh                 | 5000 27BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5008 17C4h                 | 500C 17C4h                 | 5000 27C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5008 1800h                 | 500C 1800h                 | 5000 2800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5008 1804h                 | 500C 1804h                 | 5000 2804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5008 1808h                 | 500C 1808h                 | 5000 2808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5008 180Ch                 | 500C 180Ch                 | 5000 280Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 5008 1810h                 | 500C 1810h                 | 5000 2810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5008 1814h                 | 500C 1814h                 | 5000 2814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 5008 1820h                 | 500C 1820h                 | 5000 2820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 5008 1824h                 | 500C 1824h                 | 5000 2824h                 |



**Table 3-773. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                   | EPWM14_G0 Physical Address | EPWM15_G0 Physical Address | EPWM16_G0 Physical Address |
|--------|--------|---------------------------------|----------------------------|----------------------------|----------------------------|
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>  | 5008 1828h                 | 500C 1828h                 | 5000 2828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a> | 5008 182Ch                 | 500C 182Ch                 | 5000 282Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>  | 5008 1C00h                 | 500C 1C00h                 | 5000 2C00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>   | 5008 1C04h                 | 500C 1C04h                 | 5000 2C04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>    | 5008 1C20h                 | 500C 1C20h                 | 5000 2C20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>    | 5008 1C24h                 | 500C 1C24h                 | 5000 2C24h                 |

**Table 3-774. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM17_G0 Physical Address | EPWM18_G0 Physical Address | EPWM19_G0 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5004 2000h                 | 5008 2000h                 | 500C 2000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5004 2002h                 | 5008 2002h                 | 500C 2002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5004 2006h                 | 5008 2006h                 | 500C 2006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5004 2008h                 | 5008 2008h                 | 500C 2008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5004 200Ah                 | 5008 200Ah                 | 500C 200Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 5004 200Ch                 | 5008 200Ch                 | 500C 200Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5004 200Eh                 | 5008 200Eh                 | 500C 200Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5004 2010h                 | 5008 2010h                 | 500C 2010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5004 2012h                 | 5008 2012h                 | 500C 2012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 5004 2018h                 | 5008 2018h                 | 500C 2018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 5004 201Ah                 | 5008 201Ah                 | 500C 201Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 5004 2020h                 | 5008 2020h                 | 500C 2020h                 |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 5004 2022h                 | 5008 2022h                 | 500C 2022h                 |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 5004 2028h                 | 5008 2028h                 | 500C 2028h                 |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 5004 2030h                 | 5008 2030h                 | 500C 2030h                 |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 5004 2032h                 | 5008 2032h                 | 500C 2032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 5004 2040h                 | 5008 2040h                 | 500C 2040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 5004 204Eh                 | 5008 204Eh                 | 500C 204Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>        | 5004 205Ah                 | 5008 205Ah                 | 500C 205Ah                 |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>         | 5004 205Ch                 | 5008 205Ch                 | 500C 205Ch                 |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>        | 5004 2068h                 | 5008 2068h                 | 500C 2068h                 |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>        | 5004 206Ah                 | 5008 206Ah                 | 500C 206Ah                 |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>     | 5004 2070h                 | 5008 2070h                 | 500C 2070h                 |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>    | 5004 2074h                 | 5008 2074h                 | 500C 2074h                 |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>         | 5004 207Ah                 | 5008 207Ah                 | 500C 207Ah                 |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>       | 5004 207Ch                 | 5008 207Ch                 | 500C 207Ch                 |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>      | 5004 207Eh                 | 5008 207Eh                 | 500C 207Eh                 |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>        | 5004 2080h                 | 5008 2080h                 | 500C 2080h                 |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>       | 5004 2082h                 | 5008 2082h                 | 500C 2082h                 |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>        | 5004 2084h                 | 5008 2084h                 | 500C 2084h                 |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>       | 5004 2086h                 | 5008 2086h                 | 500C 2086h                 |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>        | 5004 208Eh                 | 5008 208Eh                 | 500C 208Eh                 |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>       | 5004 2092h                 | 5008 2092h                 | 500C 2092h                 |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>       | 5004 20A0h                 | 5008 20A0h                 | 500C 20A0h                 |



**Table 3-774. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                     | EPWM17_G0 Physical Address | EPWM18_G0 Physical Address | EPWM19_G0 Physical Address |
|--------|--------|-----------------------------------|----------------------------|----------------------------|----------------------------|
| A2h    | 16     | <a href="#">EPWM_DBRED</a>        | 5004 20A2h                 | 5008 20A2h                 | 500C 20A2h                 |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>      | 5004 20A4h                 | 5008 20A4h                 | 500C 20A4h                 |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>        | 5004 20A6h                 | 5008 20A6h                 | 500C 20A6h                 |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>        | 5004 20C0h                 | 5008 20C0h                 | 500C 20C0h                 |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>      | 5004 20C4h                 | 5008 20C4h                 | 500C 20C4h                 |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>        | 5004 20C6h                 | 5008 20C6h                 | 500C 20C6h                 |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>     | 5004 20C8h                 | 5008 20C8h                 | 500C 20C8h                 |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>         | 5004 20D4h                 | 5008 20D4h                 | 500C 20D4h                 |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>         | 5004 20D8h                 | 5008 20D8h                 | 500C 20D8h                 |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>         | 5004 20DEh                 | 5008 20DEh                 | 500C 20DEh                 |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>         | 5004 20E2h                 | 5008 20E2h                 | 500C 20E2h                 |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>      | 5004 20E8h                 | 5008 20E8h                 | 500C 20E8h                 |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>    | 5004 20EEh                 | 5008 20EEh                 | 500C 20EEh                 |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>        | 5004 2100h                 | 5008 2100h                 | 500C 2100h                 |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>       | 5004 2102h                 | 5008 2102h                 | 500C 2102h                 |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>      | 5004 2104h                 | 5008 2104h                 | 500C 2104h                 |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>        | 5004 2108h                 | 5008 2108h                 | 500C 2108h                 |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>       | 5004 210Ah                 | 5008 210Ah                 | 500C 210Ah                 |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>     | 5004 210Ch                 | 5008 210Ch                 | 500C 210Ch                 |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>     | 5004 210Eh                 | 5008 210Eh                 | 500C 210Eh                 |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>       | 5004 211Ah                 | 5008 211Ah                 | 500C 211Ah                 |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>        | 5004 2126h                 | 5008 2126h                 | 500C 2126h                 |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>     | 5004 2128h                 | 5008 2128h                 | 500C 2128h                 |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>     | 5004 212Ah                 | 5008 212Ah                 | 500C 212Ah                 |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>        | 5004 212Eh                 | 5008 212Eh                 | 500C 212Eh                 |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>     | 5004 2130h                 | 5008 2130h                 | 500C 2130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>     | 5004 2132h                 | 5008 2132h                 | 500C 2132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>        | 5004 2136h                 | 5008 2136h                 | 500C 2136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a> | 5004 213Ah                 | 5008 213Ah                 | 500C 213Ah                 |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>        | 5004 2148h                 | 5008 2148h                 | 500C 2148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>         | 5004 214Ch                 | 5008 214Ch                 | 500C 214Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>        | 5004 2150h                 | 5008 2150h                 | 500C 2150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>        | 5004 2154h                 | 5008 2154h                 | 500C 2154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>        | 5004 2158h                 | 5008 2158h                 | 500C 2158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>      | 5004 215Ch                 | 5008 215Ch                 | 500C 215Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>      | 5004 2160h                 | 5008 2160h                 | 500C 2160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a> | 5004 2164h                 | 5008 2164h                 | 500C 2164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>    | 5004 2168h                 | 5008 2168h                 | 500C 2168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>   | 5004 216Ch                 | 5008 216Ch                 | 500C 216Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>  | 5004 2170h                 | 5008 2170h                 | 500C 2170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>  | 5004 2174h                 | 5008 2174h                 | 500C 2174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>    | 5004 2180h                 | 5008 2180h                 | 500C 2180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>       | 5004 2186h                 | 5008 2186h                 | 500C 2186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>       | 5004 2188h                 | 5008 2188h                 | 500C 2188h                 |

**Table 3-774. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM17_G0 Physical Address | EPWM18_G0 Physical Address | EPWM19_G0 Physical Address |
|--------|--------|---------------------------------------|----------------------------|----------------------------|----------------------------|
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5004 218Eh                 | 5008 218Eh                 | 500C 218Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5004 2190h                 | 5008 2190h                 | 500C 2190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5004 2192h                 | 5008 2192h                 | 500C 2192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5004 2194h                 | 5008 2194h                 | 500C 2194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5004 2196h                 | 5008 2196h                 | 500C 2196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5004 2198h                 | 5008 2198h                 | 500C 2198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5004 219Ah                 | 5008 219Ah                 | 500C 219Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5004 219Ch                 | 5008 219Ch                 | 500C 219Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5004 219Eh                 | 5008 219Eh                 | 500C 219Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5004 21A4h                 | 5008 21A4h                 | 500C 21A4h                 |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5004 21A6h                 | 5008 21A6h                 | 500C 21A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 5004 21A8h                 | 5008 21A8h                 | 500C 21A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 5004 21AAh                 | 5008 21AAh                 | 500C 21AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 5004 21ACh                 | 5008 21ACh                 | 500C 21ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 5004 21AEh                 | 5008 21AEh                 | 500C 21AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 5004 21B0h                 | 5008 21B0h                 | 500C 21B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 5004 21B2h                 | 5008 21B2h                 | 500C 21B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 5004 21F4h                 | 5008 21F4h                 | 500C 21F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 5004 21FAh                 | 5008 21FAh                 | 500C 21FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 5004 21FCh                 | 5008 21FCh                 | 500C 21FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>         | 5004 2400h                 | 5008 2400h                 | 500C 2400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>         | 5004 2410h                 | 5008 2410h                 | 500C 2410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>            | 5004 2418h                 | 5008 2418h                 | 500C 2418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a>   | 5004 241Ch                 | 5008 241Ch                 | 500C 241Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>     | 5004 2420h                 | 5008 2420h                 | 500C 2420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>     | 5004 2428h                 | 5008 2428h                 | 500C 2428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>     | 5004 2430h                 | 5008 2430h                 | 500C 2430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>     | 5004 2600h                 | 5008 2600h                 | 500C 2600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>     | 5004 2604h                 | 5008 2604h                 | 500C 2604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>     | 5004 2608h                 | 5008 2608h                 | 500C 2608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>     | 5004 260Ch                 | 5008 260Ch                 | 500C 260Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>     | 5004 2610h                 | 5008 2610h                 | 500C 2610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>     | 5004 2614h                 | 5008 2614h                 | 500C 2614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>     | 5004 2618h                 | 5008 2618h                 | 500C 2618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>     | 5004 261Ch                 | 5008 261Ch                 | 500C 261Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>    | 5004 2620h                 | 5008 2620h                 | 500C 2620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a>   | 5004 2630h                 | 5008 2630h                 | 500C 2630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a>   | 5004 2632h                 | 5008 2632h                 | 500C 2632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a>   | 5004 2644h                 | 5008 2644h                 | 500C 2644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>      | 5004 2680h                 | 5008 2680h                 | 500C 2680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>      | 5004 2684h                 | 5008 2684h                 | 500C 2684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>      | 5004 2688h                 | 5008 2688h                 | 500C 2688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>      | 5004 268Ch                 | 5008 268Ch                 | 500C 268Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>      | 5004 2690h                 | 5008 2690h                 | 500C 2690h                 |

**Table 3-774. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM17_G0 Physical Address | EPWM18_G0 Physical Address | EPWM19_G0 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>   | 5004 2694h                 | 5008 2694h                 | 500C 2694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>   | 5004 2698h                 | 5008 2698h                 | 500C 2698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>   | 5004 269Ch                 | 5008 269Ch                 | 500C 269Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>  | 5004 26A0h                 | 5008 26A0h                 | 500C 26A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a> | 5004 26B0h                 | 5008 26B0h                 | 500C 26B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a> | 5004 26B2h                 | 5008 26B2h                 | 500C 26B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>    | 5004 26BAh                 | 5008 26BAh                 | 500C 26BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>    | 5004 26BEh                 | 5008 26BEh                 | 500C 26BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a> | 5004 26C4h                 | 5008 26C4h                 | 500C 26C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>   | 5004 2700h                 | 5008 2700h                 | 500C 2700h                 |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>   | 5004 2704h                 | 5008 2704h                 | 500C 2704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>   | 5004 2708h                 | 5008 2708h                 | 500C 2708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>   | 5004 270Ch                 | 5008 270Ch                 | 500C 270Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>   | 5004 2710h                 | 5008 2710h                 | 500C 2710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>   | 5004 2714h                 | 5008 2714h                 | 500C 2714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>   | 5004 2718h                 | 5008 2718h                 | 500C 2718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>   | 5004 271Ch                 | 5008 271Ch                 | 500C 271Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>  | 5004 2720h                 | 5008 2720h                 | 500C 2720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a> | 5004 2730h                 | 5008 2730h                 | 500C 2730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a> | 5004 2732h                 | 5008 2732h                 | 500C 2732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>    | 5004 273Ah                 | 5008 273Ah                 | 500C 273Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>    | 5004 273Eh                 | 5008 273Eh                 | 500C 273Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a> | 5004 2744h                 | 5008 2744h                 | 500C 2744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 5004 2780h                 | 5008 2780h                 | 500C 2780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 5004 2784h                 | 5008 2784h                 | 500C 2784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 5004 2788h                 | 5008 2788h                 | 500C 2788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 5004 278Ch                 | 5008 278Ch                 | 500C 278Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 5004 2790h                 | 5008 2790h                 | 500C 2790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 5004 2794h                 | 5008 2794h                 | 500C 2794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 5004 2798h                 | 5008 2798h                 | 500C 2798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 5004 279Ch                 | 5008 279Ch                 | 500C 279Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 5004 27A0h                 | 5008 27A0h                 | 500C 27A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5004 27B0h                 | 5008 27B0h                 | 500C 27B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5004 27B2h                 | 5008 27B2h                 | 500C 27B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5004 27BAh                 | 5008 27BAh                 | 500C 27BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5004 27BEh                 | 5008 27BEh                 | 500C 27BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5004 27C4h                 | 5008 27C4h                 | 500C 27C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5004 2800h                 | 5008 2800h                 | 500C 2800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5004 2804h                 | 5008 2804h                 | 500C 2804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5004 2808h                 | 5008 2808h                 | 500C 2808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5004 280Ch                 | 5008 280Ch                 | 500C 280Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 5004 2810h                 | 5008 2810h                 | 500C 2810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5004 2814h                 | 5008 2814h                 | 500C 2814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 5004 2820h                 | 5008 2820h                 | 500C 2820h                 |

**Table 3-774. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                   | EPWM17_G0 Physical Address | EPWM18_G0 Physical Address | EPWM19_G0 Physical Address |
|--------|--------|---------------------------------|----------------------------|----------------------------|----------------------------|
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>   | 5004 2824h                 | 5008 2824h                 | 500C 2824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>  | 5004 2828h                 | 5008 2828h                 | 500C 2828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a> | 5004 282Ch                 | 5008 282Ch                 | 500C 282Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>  | 5004 2C00h                 | 5008 2C00h                 | 500C 2C00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>   | 5004 2C04h                 | 5008 2C04h                 | 500C 2C04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>    | 5004 2C20h                 | 5008 2C20h                 | 500C 2C20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>    | 5004 2C24h                 | 5008 2C24h                 | 500C 2C24h                 |

**Table 3-775. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM2_G0 Physical Address | EPWM20_G0 Physical Address | EPWM21_G0 Physical Address |
|--------|--------|------------------------------------|---------------------------|----------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5000 3000h                | 5004 3000h                 | 5008 3000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5000 3002h                | 5004 3002h                 | 5008 3002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5000 3006h                | 5004 3006h                 | 5008 3006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5000 3008h                | 5004 3008h                 | 5008 3008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5000 300Ah                | 5004 300Ah                 | 5008 300Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 5000 300Ch                | 5004 300Ch                 | 5008 300Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5000 300Eh                | 5004 300Eh                 | 5008 300Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5000 3010h                | 5004 3010h                 | 5008 3010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5000 3012h                | 5004 3012h                 | 5008 3012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 5000 3018h                | 5004 3018h                 | 5008 3018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 5000 301Ah                | 5004 301Ah                 | 5008 301Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 5000 3020h                | 5004 3020h                 | 5008 3020h                 |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 5000 3022h                | 5004 3022h                 | 5008 3022h                 |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 5000 3028h                | 5004 3028h                 | 5008 3028h                 |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 5000 3030h                | 5004 3030h                 | 5008 3030h                 |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 5000 3032h                | 5004 3032h                 | 5008 3032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 5000 3040h                | 5004 3040h                 | 5008 3040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 5000 304Eh                | 5004 304Eh                 | 5008 304Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>        | 5000 305Ah                | 5004 305Ah                 | 5008 305Ah                 |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>         | 5000 305Ch                | 5004 305Ch                 | 5008 305Ch                 |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>        | 5000 3068h                | 5004 3068h                 | 5008 3068h                 |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>        | 5000 306Ah                | 5004 306Ah                 | 5008 306Ah                 |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>     | 5000 3070h                | 5004 3070h                 | 5008 3070h                 |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>    | 5000 3074h                | 5004 3074h                 | 5008 3074h                 |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>         | 5000 307Ah                | 5004 307Ah                 | 5008 307Ah                 |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>       | 5000 307Ch                | 5004 307Ch                 | 5008 307Ch                 |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>      | 5000 307Eh                | 5004 307Eh                 | 5008 307Eh                 |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>        | 5000 3080h                | 5004 3080h                 | 5008 3080h                 |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>       | 5000 3082h                | 5004 3082h                 | 5008 3082h                 |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>        | 5000 3084h                | 5004 3084h                 | 5008 3084h                 |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>       | 5000 3086h                | 5004 3086h                 | 5008 3086h                 |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>        | 5000 308Eh                | 5004 308Eh                 | 5008 308Eh                 |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>       | 5000 3092h                | 5004 3092h                 | 5008 3092h                 |

**Table 3-775. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                     | EPWM2_G0 Physical Address | EPWM20_G0 Physical Address | EPWM21_G0 Physical Address |
|--------|--------|-----------------------------------|---------------------------|----------------------------|----------------------------|
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>      | 5000 30A0h                | 5004 30A0h                 | 5008 30A0h                 |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>        | 5000 30A2h                | 5004 30A2h                 | 5008 30A2h                 |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>      | 5000 30A4h                | 5004 30A4h                 | 5008 30A4h                 |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>        | 5000 30A6h                | 5004 30A6h                 | 5008 30A6h                 |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>        | 5000 30C0h                | 5004 30C0h                 | 5008 30C0h                 |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>      | 5000 30C4h                | 5004 30C4h                 | 5008 30C4h                 |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>        | 5000 30C6h                | 5004 30C6h                 | 5008 30C6h                 |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>     | 5000 30C8h                | 5004 30C8h                 | 5008 30C8h                 |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>         | 5000 30D4h                | 5004 30D4h                 | 5008 30D4h                 |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>         | 5000 30D8h                | 5004 30D8h                 | 5008 30D8h                 |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>         | 5000 30DEh                | 5004 30DEh                 | 5008 30DEh                 |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>         | 5000 30E2h                | 5004 30E2h                 | 5008 30E2h                 |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>      | 5000 30E8h                | 5004 30E8h                 | 5008 30E8h                 |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>    | 5000 30EEh                | 5004 30EEh                 | 5008 30EEh                 |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>        | 5000 3100h                | 5004 3100h                 | 5008 3100h                 |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>       | 5000 3102h                | 5004 3102h                 | 5008 3102h                 |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>      | 5000 3104h                | 5004 3104h                 | 5008 3104h                 |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>        | 5000 3108h                | 5004 3108h                 | 5008 3108h                 |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>       | 5000 310Ah                | 5004 310Ah                 | 5008 310Ah                 |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>     | 5000 310Ch                | 5004 310Ch                 | 5008 310Ch                 |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>     | 5000 310Eh                | 5004 310Eh                 | 5008 310Eh                 |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>       | 5000 311Ah                | 5004 311Ah                 | 5008 311Ah                 |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>        | 5000 3126h                | 5004 3126h                 | 5008 3126h                 |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>     | 5000 3128h                | 5004 3128h                 | 5008 3128h                 |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>     | 5000 312Ah                | 5004 312Ah                 | 5008 312Ah                 |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>        | 5000 312Eh                | 5004 312Eh                 | 5008 312Eh                 |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>     | 5000 3130h                | 5004 3130h                 | 5008 3130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>     | 5000 3132h                | 5004 3132h                 | 5008 3132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRFC</a>       | 5000 3136h                | 5004 3136h                 | 5008 3136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a> | 5000 313Ah                | 5004 313Ah                 | 5008 313Ah                 |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>        | 5000 3148h                | 5004 3148h                 | 5008 3148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>         | 5000 314Ch                | 5004 314Ch                 | 5008 314Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>        | 5000 3150h                | 5004 3150h                 | 5008 3150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>        | 5000 3154h                | 5004 3154h                 | 5008 3154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>        | 5000 3158h                | 5004 3158h                 | 5008 3158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>      | 5000 315Ch                | 5004 315Ch                 | 5008 315Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>      | 5000 3160h                | 5004 3160h                 | 5008 3160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a> | 5000 3164h                | 5004 3164h                 | 5008 3164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>    | 5000 3168h                | 5004 3168h                 | 5008 3168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>   | 5000 316Ch                | 5004 316Ch                 | 5008 316Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>  | 5000 3170h                | 5004 3170h                 | 5008 3170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>  | 5000 3174h                | 5004 3174h                 | 5008 3174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>    | 5000 3180h                | 5004 3180h                 | 5008 3180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>       | 5000 3186h                | 5004 3186h                 | 5008 3186h                 |

**Table 3-775. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM2_G0 Physical Address | EPWM20_G0 Physical Address | EPWM21_G0 Physical Address |
|--------|--------|---------------------------------------|---------------------------|----------------------------|----------------------------|
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5000 3188h                | 5004 3188h                 | 5008 3188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5000 318Eh                | 5004 318Eh                 | 5008 318Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5000 3190h                | 5004 3190h                 | 5008 3190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5000 3192h                | 5004 3192h                 | 5008 3192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5000 3194h                | 5004 3194h                 | 5008 3194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5000 3196h                | 5004 3196h                 | 5008 3196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5000 3198h                | 5004 3198h                 | 5008 3198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5000 319Ah                | 5004 319Ah                 | 5008 319Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5000 319Ch                | 5004 319Ch                 | 5008 319Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5000 319Eh                | 5004 319Eh                 | 5008 319Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5000 31A4h                | 5004 31A4h                 | 5008 31A4h                 |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5000 31A6h                | 5004 31A6h                 | 5008 31A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 5000 31A8h                | 5004 31A8h                 | 5008 31A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 5000 31AAh                | 5004 31AAh                 | 5008 31AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 5000 31ACh                | 5004 31ACh                 | 5008 31ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 5000 31AEh                | 5004 31AEh                 | 5008 31AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 5000 31B0h                | 5004 31B0h                 | 5008 31B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 5000 31B2h                | 5004 31B2h                 | 5008 31B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 5000 31F4h                | 5004 31F4h                 | 5008 31F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 5000 31FAh                | 5004 31FAh                 | 5008 31FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 5000 31FCh                | 5004 31FCh                 | 5008 31FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>         | 5000 3400h                | 5004 3400h                 | 5008 3400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>         | 5000 3410h                | 5004 3410h                 | 5008 3410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>            | 5000 3418h                | 5004 3418h                 | 5008 3418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a>   | 5000 341Ch                | 5004 341Ch                 | 5008 341Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>     | 5000 3420h                | 5004 3420h                 | 5008 3420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>     | 5000 3428h                | 5004 3428h                 | 5008 3428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>     | 5000 3430h                | 5004 3430h                 | 5008 3430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>     | 5000 3600h                | 5004 3600h                 | 5008 3600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>     | 5000 3604h                | 5004 3604h                 | 5008 3604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>     | 5000 3608h                | 5004 3608h                 | 5008 3608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>     | 5000 360Ch                | 5004 360Ch                 | 5008 360Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>     | 5000 3610h                | 5004 3610h                 | 5008 3610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>     | 5000 3614h                | 5004 3614h                 | 5008 3614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>     | 5000 3618h                | 5004 3618h                 | 5008 3618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>     | 5000 361Ch                | 5004 361Ch                 | 5008 361Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>    | 5000 3620h                | 5004 3620h                 | 5008 3620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a>   | 5000 3630h                | 5004 3630h                 | 5008 3630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a>   | 5000 3632h                | 5004 3632h                 | 5008 3632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a>   | 5000 3644h                | 5004 3644h                 | 5008 3644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>      | 5000 3680h                | 5004 3680h                 | 5008 3680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>      | 5000 3684h                | 5004 3684h                 | 5008 3684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>      | 5000 3688h                | 5004 3688h                 | 5008 3688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>      | 5000 368Ch                | 5004 368Ch                 | 5008 368Ch                 |



**Table 3-775. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM2_G0 Physical Address | EPWM20_G0 Physical Address | EPWM21_G0 Physical Address |
|--------|--------|------------------------------------|---------------------------|----------------------------|----------------------------|
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>   | 5000 3690h                | 5004 3690h                 | 5008 3690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>   | 5000 3694h                | 5004 3694h                 | 5008 3694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>   | 5000 3698h                | 5004 3698h                 | 5008 3698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>   | 5000 369Ch                | 5004 369Ch                 | 5008 369Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>  | 5000 36A0h                | 5004 36A0h                 | 5008 36A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a> | 5000 36B0h                | 5004 36B0h                 | 5008 36B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a> | 5000 36B2h                | 5004 36B2h                 | 5008 36B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>    | 5000 36BAh                | 5004 36BAh                 | 5008 36BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>    | 5000 36BEh                | 5004 36BEh                 | 5008 36BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a> | 5000 36C4h                | 5004 36C4h                 | 5008 36C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>   | 5000 3700h                | 5004 3700h                 | 5008 3700h                 |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>   | 5000 3704h                | 5004 3704h                 | 5008 3704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>   | 5000 3708h                | 5004 3708h                 | 5008 3708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>   | 5000 370Ch                | 5004 370Ch                 | 5008 370Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>   | 5000 3710h                | 5004 3710h                 | 5008 3710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>   | 5000 3714h                | 5004 3714h                 | 5008 3714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>   | 5000 3718h                | 5004 3718h                 | 5008 3718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>   | 5000 371Ch                | 5004 371Ch                 | 5008 371Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>  | 5000 3720h                | 5004 3720h                 | 5008 3720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a> | 5000 3730h                | 5004 3730h                 | 5008 3730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a> | 5000 3732h                | 5004 3732h                 | 5008 3732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>    | 5000 373Ah                | 5004 373Ah                 | 5008 373Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>    | 5000 373Eh                | 5004 373Eh                 | 5008 373Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a> | 5000 3744h                | 5004 3744h                 | 5008 3744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 5000 3780h                | 5004 3780h                 | 5008 3780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 5000 3784h                | 5004 3784h                 | 5008 3784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 5000 3788h                | 5004 3788h                 | 5008 3788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 5000 378Ch                | 5004 378Ch                 | 5008 378Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 5000 3790h                | 5004 3790h                 | 5008 3790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 5000 3794h                | 5004 3794h                 | 5008 3794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 5000 3798h                | 5004 3798h                 | 5008 3798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 5000 379Ch                | 5004 379Ch                 | 5008 379Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 5000 37A0h                | 5004 37A0h                 | 5008 37A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5000 37B0h                | 5004 37B0h                 | 5008 37B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5000 37B2h                | 5004 37B2h                 | 5008 37B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5000 37BAh                | 5004 37BAh                 | 5008 37BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5000 37BEh                | 5004 37BEh                 | 5008 37BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5000 37C4h                | 5004 37C4h                 | 5008 37C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5000 3800h                | 5004 3800h                 | 5008 3800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5000 3804h                | 5004 3804h                 | 5008 3804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5000 3808h                | 5004 3808h                 | 5008 3808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5000 380Ch                | 5004 380Ch                 | 5008 380Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 5000 3810h                | 5004 3810h                 | 5008 3810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5000 3814h                | 5004 3814h                 | 5008 3814h                 |

**Table 3-775. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                   | EPWM2_G0 Physical Address | EPWM20_G0 Physical Address | EPWM21_G0 Physical Address |
|--------|--------|---------------------------------|---------------------------|----------------------------|----------------------------|
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>   | 5000 3820h                | 5004 3820h                 | 5008 3820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>   | 5000 3824h                | 5004 3824h                 | 5008 3824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>  | 5000 3828h                | 5004 3828h                 | 5008 3828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a> | 5000 382Ch                | 5004 382Ch                 | 5008 382Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>  | 5000 3C00h                | 5004 3C00h                 | 5008 3C00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>   | 5000 3C04h                | 5004 3C04h                 | 5008 3C04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>    | 5000 3C20h                | 5004 3C20h                 | 5008 3C20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>    | 5000 3C24h                | 5004 3C24h                 | 5008 3C24h                 |

**Table 3-776. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM22_G0 Physical Address | EPWM23_G0 Physical Address | EPWM24_G0 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 500C 3000h                 | 5000 4000h                 | 5004 4000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 500C 3002h                 | 5000 4002h                 | 5004 4002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 500C 3006h                 | 5000 4006h                 | 5004 4006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 500C 3008h                 | 5000 4008h                 | 5004 4008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 500C 300Ah                 | 5000 400Ah                 | 5004 400Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNOUTEN</a>  | 500C 300Ch                 | 5000 400Ch                 | 5004 400Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 500C 300Eh                 | 5000 400Eh                 | 5004 400Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 500C 3010h                 | 5000 4010h                 | 5004 4010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 500C 3012h                 | 5000 4012h                 | 5004 4012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 500C 3018h                 | 5000 4018h                 | 5004 4018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 500C 301Ah                 | 5000 401Ah                 | 5004 401Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 500C 3020h                 | 5000 4020h                 | 5004 4020h                 |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 500C 3022h                 | 5000 4022h                 | 5004 4022h                 |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 500C 3028h                 | 5000 4028h                 | 5004 4028h                 |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 500C 3030h                 | 5000 4030h                 | 5004 4030h                 |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 500C 3032h                 | 5000 4032h                 | 5004 4032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 500C 3040h                 | 5000 4040h                 | 5004 4040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 500C 304Eh                 | 5000 404Eh                 | 5004 404Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>        | 500C 305Ah                 | 5000 405Ah                 | 5004 405Ah                 |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>         | 500C 305Ch                 | 5000 405Ch                 | 5004 405Ch                 |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>        | 500C 3068h                 | 5000 4068h                 | 5004 4068h                 |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>        | 500C 306Ah                 | 5000 406Ah                 | 5004 406Ah                 |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>     | 500C 3070h                 | 5000 4070h                 | 5004 4070h                 |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>    | 500C 3074h                 | 5000 4074h                 | 5004 4074h                 |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>         | 500C 307Ah                 | 5000 407Ah                 | 5004 407Ah                 |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>       | 500C 307Ch                 | 5000 407Ch                 | 5004 407Ch                 |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>      | 500C 307Eh                 | 5000 407Eh                 | 5004 407Eh                 |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>        | 500C 3080h                 | 5000 4080h                 | 5004 4080h                 |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>       | 500C 3082h                 | 5000 4082h                 | 5004 4082h                 |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>        | 500C 3084h                 | 5000 4084h                 | 5004 4084h                 |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>       | 500C 3086h                 | 5000 4086h                 | 5004 4086h                 |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>        | 500C 308Eh                 | 5000 408Eh                 | 5004 408Eh                 |



**Table 3-776. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                     | EPWM22_G0 Physical Address | EPWM23_G0 Physical Address | EPWM24_G0 Physical Address |
|--------|--------|-----------------------------------|----------------------------|----------------------------|----------------------------|
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>      | 500C 3092h                 | 5000 4092h                 | 5004 4092h                 |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>      | 500C 30A0h                 | 5000 40A0h                 | 5004 40A0h                 |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>        | 500C 30A2h                 | 5000 40A2h                 | 5004 40A2h                 |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>      | 500C 30A4h                 | 5000 40A4h                 | 5004 40A4h                 |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>        | 500C 30A6h                 | 5000 40A6h                 | 5004 40A6h                 |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>        | 500C 30C0h                 | 5000 40C0h                 | 5004 40C0h                 |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>      | 500C 30C4h                 | 5000 40C4h                 | 5004 40C4h                 |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>        | 500C 30C6h                 | 5000 40C6h                 | 5004 40C6h                 |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>     | 500C 30C8h                 | 5000 40C8h                 | 5004 40C8h                 |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>         | 500C 30D4h                 | 5000 40D4h                 | 5004 40D4h                 |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>         | 500C 30D8h                 | 5000 40D8h                 | 5004 40D8h                 |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>         | 500C 30DEh                 | 5000 40DEh                 | 5004 40DEh                 |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>         | 500C 30E2h                 | 5000 40E2h                 | 5004 40E2h                 |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>      | 500C 30E8h                 | 5000 40E8h                 | 5004 40E8h                 |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>    | 500C 30EEh                 | 5000 40EEh                 | 5004 40EEh                 |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>        | 500C 3100h                 | 5000 4100h                 | 5004 4100h                 |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>       | 500C 3102h                 | 5000 4102h                 | 5004 4102h                 |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>      | 500C 3104h                 | 5000 4104h                 | 5004 4104h                 |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>        | 500C 3108h                 | 5000 4108h                 | 5004 4108h                 |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>       | 500C 310Ah                 | 5000 410Ah                 | 5004 410Ah                 |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>     | 500C 310Ch                 | 5000 410Ch                 | 5004 410Ch                 |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>     | 500C 310Eh                 | 5000 410Eh                 | 5004 410Eh                 |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>       | 500C 311Ah                 | 5000 411Ah                 | 5004 411Ah                 |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>        | 500C 3126h                 | 5000 4126h                 | 5004 4126h                 |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>     | 500C 3128h                 | 5000 4128h                 | 5004 4128h                 |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>     | 500C 312Ah                 | 5000 412Ah                 | 5004 412Ah                 |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>        | 500C 312Eh                 | 5000 412Eh                 | 5004 412Eh                 |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>     | 500C 3130h                 | 5000 4130h                 | 5004 4130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>     | 500C 3132h                 | 5000 4132h                 | 5004 4132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>        | 500C 3136h                 | 5000 4136h                 | 5004 4136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a> | 500C 313Ah                 | 5000 413Ah                 | 5004 413Ah                 |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>        | 500C 3148h                 | 5000 4148h                 | 5004 4148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>         | 500C 314Ch                 | 5000 414Ch                 | 5004 414Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>        | 500C 3150h                 | 5000 4150h                 | 5004 4150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>        | 500C 3154h                 | 5000 4154h                 | 5004 4154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>        | 500C 3158h                 | 5000 4158h                 | 5004 4158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>      | 500C 315Ch                 | 5000 415Ch                 | 5004 415Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>      | 500C 3160h                 | 5000 4160h                 | 5004 4160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a> | 500C 3164h                 | 5000 4164h                 | 5004 4164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>    | 500C 3168h                 | 5000 4168h                 | 5004 4168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>   | 500C 316Ch                 | 5000 416Ch                 | 5004 416Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>  | 500C 3170h                 | 5000 4170h                 | 5004 4170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>  | 500C 3174h                 | 5000 4174h                 | 5004 4174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRISEL</a>     | 500C 3180h                 | 5000 4180h                 | 5004 4180h                 |

**Table 3-776. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM22_G0 Physical Address | EPWM23_G0 Physical Address | EPWM24_G0 Physical Address |
|--------|--------|---------------------------------------|----------------------------|----------------------------|----------------------------|
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 500C 3186h                 | 5000 4186h                 | 5004 4186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 500C 3188h                 | 5000 4188h                 | 5004 4188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 500C 318Eh                 | 5000 418Eh                 | 5004 418Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 500C 3190h                 | 5000 4190h                 | 5004 4190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 500C 3192h                 | 5000 4192h                 | 5004 4192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 500C 3194h                 | 5000 4194h                 | 5004 4194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 500C 3196h                 | 5000 4196h                 | 5004 4196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 500C 3198h                 | 5000 4198h                 | 5004 4198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 500C 319Ah                 | 5000 419Ah                 | 5004 419Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 500C 319Ch                 | 5000 419Ch                 | 5004 419Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 500C 319Eh                 | 5000 419Eh                 | 5004 419Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 500C 31A4h                 | 5000 41A4h                 | 5004 41A4h                 |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 500C 31A6h                 | 5000 41A6h                 | 5004 41A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 500C 31A8h                 | 5000 41A8h                 | 5004 41A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 500C 31AAh                 | 5000 41AAh                 | 5004 41AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 500C 31ACh                 | 5000 41ACh                 | 5004 41ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 500C 31AEh                 | 5000 41AEh                 | 5004 41AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 500C 31B0h                 | 5000 41B0h                 | 5004 41B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 500C 31B2h                 | 5000 41B2h                 | 5004 41B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 500C 31F4h                 | 5000 41F4h                 | 5004 41F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 500C 31FAh                 | 5000 41FAh                 | 5004 41FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 500C 31FCh                 | 5000 41FCh                 | 5004 41FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>         | 500C 3400h                 | 5000 4400h                 | 5004 4400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>         | 500C 3410h                 | 5000 4410h                 | 5004 4410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>            | 500C 3418h                 | 5000 4418h                 | 5004 4418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a>   | 500C 341Ch                 | 5000 441Ch                 | 5004 441Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>     | 500C 3420h                 | 5000 4420h                 | 5004 4420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>     | 500C 3428h                 | 5000 4428h                 | 5004 4428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>     | 500C 3430h                 | 5000 4430h                 | 5004 4430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>     | 500C 3600h                 | 5000 4600h                 | 5004 4600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>     | 500C 3604h                 | 5000 4604h                 | 5004 4604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>     | 500C 3608h                 | 5000 4608h                 | 5004 4608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>     | 500C 360Ch                 | 5000 460Ch                 | 5004 460Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>     | 500C 3610h                 | 5000 4610h                 | 5004 4610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>     | 500C 3614h                 | 5000 4614h                 | 5004 4614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>     | 500C 3618h                 | 5000 4618h                 | 5004 4618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>     | 500C 361Ch                 | 5000 461Ch                 | 5004 461Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>    | 500C 3620h                 | 5000 4620h                 | 5004 4620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a>   | 500C 3630h                 | 5000 4630h                 | 5004 4630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a>   | 500C 3632h                 | 5000 4632h                 | 5004 4632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a>   | 500C 3644h                 | 5000 4644h                 | 5004 4644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>      | 500C 3680h                 | 5000 4680h                 | 5004 4680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>      | 500C 3684h                 | 5000 4684h                 | 5004 4684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>      | 500C 3688h                 | 5000 4688h                 | 5004 4688h                 |

**Table 3-776. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM22_G0 Physical Address | EPWM23_G0 Physical Address | EPWM24_G0 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>   | 500C 368Ch                 | 5000 468Ch                 | 5004 468Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>   | 500C 3690h                 | 5000 4690h                 | 5004 4690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>   | 500C 3694h                 | 5000 4694h                 | 5004 4694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>   | 500C 3698h                 | 5000 4698h                 | 5004 4698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>   | 500C 369Ch                 | 5000 469Ch                 | 5004 469Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>  | 500C 36A0h                 | 5000 46A0h                 | 5004 46A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a> | 500C 36B0h                 | 5000 46B0h                 | 5004 46B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a> | 500C 36B2h                 | 5000 46B2h                 | 5004 46B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>    | 500C 36BAh                 | 5000 46BAh                 | 5004 46BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>    | 500C 36BEh                 | 5000 46BEh                 | 5004 46BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a> | 500C 36C4h                 | 5000 46C4h                 | 5004 46C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>   | 500C 3700h                 | 5000 4700h                 | 5004 4700h                 |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>   | 500C 3704h                 | 5000 4704h                 | 5004 4704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>   | 500C 3708h                 | 5000 4708h                 | 5004 4708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>   | 500C 370Ch                 | 5000 470Ch                 | 5004 470Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>   | 500C 3710h                 | 5000 4710h                 | 5004 4710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>   | 500C 3714h                 | 5000 4714h                 | 5004 4714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>   | 500C 3718h                 | 5000 4718h                 | 5004 4718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>   | 500C 371Ch                 | 5000 471Ch                 | 5004 471Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>  | 500C 3720h                 | 5000 4720h                 | 5004 4720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a> | 500C 3730h                 | 5000 4730h                 | 5004 4730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a> | 500C 3732h                 | 5000 4732h                 | 5004 4732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>    | 500C 373Ah                 | 5000 473Ah                 | 5004 473Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>    | 500C 373Eh                 | 5000 473Eh                 | 5004 473Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a> | 500C 3744h                 | 5000 4744h                 | 5004 4744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 500C 3780h                 | 5000 4780h                 | 5004 4780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 500C 3784h                 | 5000 4784h                 | 5004 4784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 500C 3788h                 | 5000 4788h                 | 5004 4788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 500C 378Ch                 | 5000 478Ch                 | 5004 478Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 500C 3790h                 | 5000 4790h                 | 5004 4790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 500C 3794h                 | 5000 4794h                 | 5004 4794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 500C 3798h                 | 5000 4798h                 | 5004 4798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 500C 379Ch                 | 5000 479Ch                 | 5004 479Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 500C 37A0h                 | 5000 47A0h                 | 5004 47A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 500C 37B0h                 | 5000 47B0h                 | 5004 47B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 500C 37B2h                 | 5000 47B2h                 | 5004 47B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 500C 37BAh                 | 5000 47BAh                 | 5004 47BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 500C 37BEh                 | 5000 47BEh                 | 5004 47BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 500C 37C4h                 | 5000 47C4h                 | 5004 47C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 500C 3800h                 | 5000 4800h                 | 5004 4800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 500C 3804h                 | 5000 4804h                 | 5004 4804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 500C 3808h                 | 5000 4808h                 | 5004 4808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 500C 380Ch                 | 5000 480Ch                 | 5004 480Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRG</a>         | 500C 3810h                 | 5000 4810h                 | 5004 4810h                 |

**Table 3-776. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                   | EPWM22_G0 Physical Address | EPWM23_G0 Physical Address | EPWM24_G0 Physical Address |
|--------|--------|---------------------------------|----------------------------|----------------------------|----------------------------|
| 814h   | 32     | <a href="#">EPWM_DECLR</a>      | 500C 3814h                 | 5000 4814h                 | 5004 4814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>   | 500C 3820h                 | 5000 4820h                 | 5004 4820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>   | 500C 3824h                 | 5000 4824h                 | 5004 4824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>  | 500C 3828h                 | 5000 4828h                 | 5004 4828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a> | 500C 382Ch                 | 5000 482Ch                 | 5004 482Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFG</a>   | 500C 3C00h                 | 5000 4C00h                 | 5004 4C00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>   | 500C 3C04h                 | 5000 4C04h                 | 5004 4C04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>    | 500C 3C20h                 | 5000 4C20h                 | 5004 4C20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>    | 500C 3C24h                 | 5000 4C24h                 | 5004 4C24h                 |

**Table 3-777. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM25_G0 Physical Address | EPWM26_G0 Physical Address | EPWM27_G0 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5008 4000h                 | 500C 4000h                 | 5000 5000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5008 4002h                 | 500C 4002h                 | 5000 5002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5008 4006h                 | 500C 4006h                 | 5000 5006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5008 4008h                 | 500C 4008h                 | 5000 5008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5008 400Ah                 | 500C 400Ah                 | 5000 500Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUEN</a>  | 5008 400Ch                 | 500C 400Ch                 | 5000 500Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5008 400Eh                 | 500C 400Eh                 | 5000 500Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5008 4010h                 | 500C 4010h                 | 5000 5010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5008 4012h                 | 500C 4012h                 | 5000 5012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 5008 4018h                 | 500C 4018h                 | 5000 5018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 5008 401Ah                 | 500C 401Ah                 | 5000 501Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 5008 4020h                 | 500C 4020h                 | 5000 5020h                 |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 5008 4022h                 | 500C 4022h                 | 5000 5022h                 |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 5008 4028h                 | 500C 4028h                 | 5000 5028h                 |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 5008 4030h                 | 500C 4030h                 | 5000 5030h                 |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 5008 4032h                 | 500C 4032h                 | 5000 5032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 5008 4040h                 | 500C 4040h                 | 5000 5040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 5008 404Eh                 | 500C 404Eh                 | 5000 504Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>        | 5008 405Ah                 | 500C 405Ah                 | 5000 505Ah                 |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>         | 5008 405Ch                 | 500C 405Ch                 | 5000 505Ch                 |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>        | 5008 4068h                 | 500C 4068h                 | 5000 5068h                 |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>        | 5008 406Ah                 | 500C 406Ah                 | 5000 506Ah                 |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>     | 5008 4070h                 | 500C 4070h                 | 5000 5070h                 |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>    | 5008 4074h                 | 500C 4074h                 | 5000 5074h                 |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>         | 5008 407Ah                 | 500C 407Ah                 | 5000 507Ah                 |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>       | 5008 407Ch                 | 500C 407Ch                 | 5000 507Ch                 |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>      | 5008 407Eh                 | 500C 407Eh                 | 5000 507Eh                 |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>        | 5008 4080h                 | 500C 4080h                 | 5000 5080h                 |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>       | 5008 4082h                 | 500C 4082h                 | 5000 5082h                 |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>        | 5008 4084h                 | 500C 4084h                 | 5000 5084h                 |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>       | 5008 4086h                 | 500C 4086h                 | 5000 5086h                 |

**Table 3-777. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                     | EPWM25_G0 Physical Address | EPWM26_G0 Physical Address | EPWM27_G0 Physical Address |
|--------|--------|-----------------------------------|----------------------------|----------------------------|----------------------------|
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>       | 5008 408Eh                 | 500C 408Eh                 | 5000 508Eh                 |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>      | 5008 4092h                 | 500C 4092h                 | 5000 5092h                 |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>      | 5008 40A0h                 | 500C 40A0h                 | 5000 50A0h                 |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>        | 5008 40A2h                 | 500C 40A2h                 | 5000 50A2h                 |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>      | 5008 40A4h                 | 500C 40A4h                 | 5000 50A4h                 |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>        | 5008 40A6h                 | 500C 40A6h                 | 5000 50A6h                 |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>        | 5008 40C0h                 | 500C 40C0h                 | 5000 50C0h                 |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>      | 5008 40C4h                 | 500C 40C4h                 | 5000 50C4h                 |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>        | 5008 40C6h                 | 500C 40C6h                 | 5000 50C6h                 |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>     | 5008 40C8h                 | 500C 40C8h                 | 5000 50C8h                 |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>         | 5008 40D4h                 | 500C 40D4h                 | 5000 50D4h                 |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>         | 5008 40D8h                 | 500C 40D8h                 | 5000 50D8h                 |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>         | 5008 40DEh                 | 500C 40DEh                 | 5000 50DEh                 |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>         | 5008 40E2h                 | 500C 40E2h                 | 5000 50E2h                 |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>      | 5008 40E8h                 | 500C 40E8h                 | 5000 50E8h                 |
| EEh    | 16     | <a href="#">EPWM_SWDELVAL</a>     | 5008 40EEh                 | 500C 40EEh                 | 5000 50EEh                 |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>        | 5008 4100h                 | 500C 4100h                 | 5000 5100h                 |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>       | 5008 4102h                 | 500C 4102h                 | 5000 5102h                 |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>      | 5008 4104h                 | 500C 4104h                 | 5000 5104h                 |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>        | 5008 4108h                 | 500C 4108h                 | 5000 5108h                 |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>       | 5008 410Ah                 | 500C 410Ah                 | 5000 510Ah                 |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>     | 5008 410Ch                 | 500C 410Ch                 | 5000 510Ch                 |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>     | 5008 410Eh                 | 500C 410Eh                 | 5000 510Eh                 |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>       | 5008 411Ah                 | 500C 411Ah                 | 5000 511Ah                 |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>        | 5008 4126h                 | 500C 4126h                 | 5000 5126h                 |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>     | 5008 4128h                 | 500C 4128h                 | 5000 5128h                 |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>     | 5008 412Ah                 | 500C 412Ah                 | 5000 512Ah                 |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>        | 5008 412Eh                 | 500C 412Eh                 | 5000 512Eh                 |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>     | 5008 4130h                 | 500C 4130h                 | 5000 5130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>     | 5008 4132h                 | 500C 4132h                 | 5000 5132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>        | 5008 4136h                 | 500C 4136h                 | 5000 5136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a> | 5008 413Ah                 | 500C 413Ah                 | 5000 513Ah                 |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>        | 5008 4148h                 | 500C 4148h                 | 5000 5148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>         | 5008 414Ch                 | 500C 414Ch                 | 5000 514Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>        | 5008 4150h                 | 500C 4150h                 | 5000 5150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>        | 5008 4154h                 | 500C 4154h                 | 5000 5154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>        | 5008 4158h                 | 500C 4158h                 | 5000 5158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>      | 5008 415Ch                 | 500C 415Ch                 | 5000 515Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>      | 5008 4160h                 | 500C 4160h                 | 5000 5160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a> | 5008 4164h                 | 500C 4164h                 | 5000 5164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>    | 5008 4168h                 | 500C 4168h                 | 5000 5168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>   | 5008 416Ch                 | 500C 416Ch                 | 5000 516Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>  | 5008 4170h                 | 500C 4170h                 | 5000 5170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>  | 5008 4174h                 | 500C 4174h                 | 5000 5174h                 |

**Table 3-777. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM25_G0 Physical Address | EPWM26_G0 Physical Address | EPWM27_G0 Physical Address |
|--------|--------|---------------------------------------|----------------------------|----------------------------|----------------------------|
| 180h   | 16     | <a href="#">EPWM_DCTRISEL</a>         | 5008 4180h                 | 500C 4180h                 | 5000 5180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 5008 4186h                 | 500C 4186h                 | 5000 5186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5008 4188h                 | 500C 4188h                 | 5000 5188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5008 418Eh                 | 500C 418Eh                 | 5000 518Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5008 4190h                 | 500C 4190h                 | 5000 5190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5008 4192h                 | 500C 4192h                 | 5000 5192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5008 4194h                 | 500C 4194h                 | 5000 5194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5008 4196h                 | 500C 4196h                 | 5000 5196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5008 4198h                 | 500C 4198h                 | 5000 5198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5008 419Ah                 | 500C 419Ah                 | 5000 519Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5008 419Ch                 | 500C 419Ch                 | 5000 519Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5008 419Eh                 | 500C 419Eh                 | 5000 519Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5008 41A4h                 | 500C 41A4h                 | 5000 51A4h                 |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5008 41A6h                 | 500C 41A6h                 | 5000 51A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 5008 41A8h                 | 500C 41A8h                 | 5000 51A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 5008 41AAh                 | 500C 41AAh                 | 5000 51AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 5008 41ACh                 | 500C 41ACh                 | 5000 51ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRISEL</a>    | 5008 41AEh                 | 500C 41AEh                 | 5000 51AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 5008 41B0h                 | 500C 41B0h                 | 5000 51B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 5008 41B2h                 | 500C 41B2h                 | 5000 51B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 5008 41F4h                 | 500C 41F4h                 | 5000 51F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 5008 41FAh                 | 500C 41FAh                 | 5000 51FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 5008 41FCh                 | 500C 41FCh                 | 5000 51FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>         | 5008 4400h                 | 500C 4400h                 | 5000 5400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>         | 5008 4410h                 | 500C 4410h                 | 5000 5410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>            | 5008 4418h                 | 500C 4418h                 | 5000 5418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a>   | 5008 441Ch                 | 500C 441Ch                 | 5000 541Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>     | 5008 4420h                 | 500C 4420h                 | 5000 5420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>     | 5008 4428h                 | 500C 4428h                 | 5000 5428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>     | 5008 4430h                 | 500C 4430h                 | 5000 5430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>     | 5008 4600h                 | 500C 4600h                 | 5000 5600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>     | 5008 4604h                 | 500C 4604h                 | 5000 5604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>     | 5008 4608h                 | 500C 4608h                 | 5000 5608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>     | 5008 460Ch                 | 500C 460Ch                 | 5000 560Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>     | 5008 4610h                 | 500C 4610h                 | 5000 5610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>     | 5008 4614h                 | 500C 4614h                 | 5000 5614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>     | 5008 4618h                 | 500C 4618h                 | 5000 5618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>     | 5008 461Ch                 | 500C 461Ch                 | 5000 561Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>    | 5008 4620h                 | 500C 4620h                 | 5000 5620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a>   | 5008 4630h                 | 500C 4630h                 | 5000 5630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a>   | 5008 4632h                 | 500C 4632h                 | 5000 5632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a>   | 5008 4644h                 | 500C 4644h                 | 5000 5644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>      | 5008 4680h                 | 500C 4680h                 | 5000 5680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>      | 5008 4684h                 | 500C 4684h                 | 5000 5684h                 |

**Table 3-777. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM25_G0 Physical Address | EPWM26_G0 Physical Address | EPWM27_G0 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>   | 5008 4688h                 | 500C 4688h                 | 5000 5688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>   | 5008 468Ch                 | 500C 468Ch                 | 5000 568Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>   | 5008 4690h                 | 500C 4690h                 | 5000 5690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>   | 5008 4694h                 | 500C 4694h                 | 5000 5694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>   | 5008 4698h                 | 500C 4698h                 | 5000 5698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>   | 5008 469Ch                 | 500C 469Ch                 | 5000 569Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>  | 5008 46A0h                 | 500C 46A0h                 | 5000 56A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a> | 5008 46B0h                 | 500C 46B0h                 | 5000 56B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a> | 5008 46B2h                 | 500C 46B2h                 | 5000 56B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>    | 5008 46BAh                 | 500C 46BAh                 | 5000 56BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>    | 5008 46BEh                 | 500C 46BEh                 | 5000 56BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a> | 5008 46C4h                 | 500C 46C4h                 | 5000 56C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>   | 5008 4700h                 | 500C 4700h                 | 5000 5700h                 |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>   | 5008 4704h                 | 500C 4704h                 | 5000 5704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>   | 5008 4708h                 | 500C 4708h                 | 5000 5708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>   | 5008 470Ch                 | 500C 470Ch                 | 5000 570Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>   | 5008 4710h                 | 500C 4710h                 | 5000 5710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>   | 5008 4714h                 | 500C 4714h                 | 5000 5714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>   | 5008 4718h                 | 500C 4718h                 | 5000 5718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>   | 5008 471Ch                 | 500C 471Ch                 | 5000 571Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>  | 5008 4720h                 | 500C 4720h                 | 5000 5720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a> | 5008 4730h                 | 500C 4730h                 | 5000 5730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a> | 5008 4732h                 | 500C 4732h                 | 5000 5732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>    | 5008 473Ah                 | 500C 473Ah                 | 5000 573Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>    | 5008 473Eh                 | 500C 473Eh                 | 5000 573Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a> | 5008 4744h                 | 500C 4744h                 | 5000 5744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 5008 4780h                 | 500C 4780h                 | 5000 5780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 5008 4784h                 | 500C 4784h                 | 5000 5784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 5008 4788h                 | 500C 4788h                 | 5000 5788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 5008 478Ch                 | 500C 478Ch                 | 5000 578Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 5008 4790h                 | 500C 4790h                 | 5000 5790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 5008 4794h                 | 500C 4794h                 | 5000 5794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 5008 4798h                 | 500C 4798h                 | 5000 5798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 5008 479Ch                 | 500C 479Ch                 | 5000 579Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 5008 47A0h                 | 500C 47A0h                 | 5000 57A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5008 47B0h                 | 500C 47B0h                 | 5000 57B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5008 47B2h                 | 500C 47B2h                 | 5000 57B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5008 47BAh                 | 500C 47BAh                 | 5000 57BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5008 47BEh                 | 500C 47BEh                 | 5000 57BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5008 47C4h                 | 500C 47C4h                 | 5000 57C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5008 4800h                 | 500C 4800h                 | 5000 5800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5008 4804h                 | 500C 4804h                 | 5000 5804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5008 4808h                 | 500C 4808h                 | 5000 5808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5008 480Ch                 | 500C 480Ch                 | 5000 580Ch                 |



**Table 3-777. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                   | EPWM25_G0 Physical Address | EPWM26_G0 Physical Address | EPWM27_G0 Physical Address |
|--------|--------|---------------------------------|----------------------------|----------------------------|----------------------------|
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>      | 5008 4810h                 | 500C 4810h                 | 5000 5810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>      | 5008 4814h                 | 500C 4814h                 | 5000 5814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>   | 5008 4820h                 | 500C 4820h                 | 5000 5820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>   | 5008 4824h                 | 500C 4824h                 | 5000 5824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>  | 5008 4828h                 | 500C 4828h                 | 5000 5828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a> | 5008 482Ch                 | 500C 482Ch                 | 5000 582Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFG</a>   | 5008 4C00h                 | 500C 4C00h                 | 5000 5C00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>   | 5008 4C04h                 | 500C 4C04h                 | 5000 5C04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>    | 5008 4C20h                 | 500C 4C20h                 | 5000 5C20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>    | 5008 4C24h                 | 500C 4C24h                 | 5000 5C24h                 |

**Table 3-778. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM28_G0 Physical Address | EPWM29_G0 Physical Address | EPWM3_G0 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|---------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5004 5000h                 | 5008 5000h                 | 500C 5000h                |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5004 5002h                 | 5008 5002h                 | 500C 5002h                |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5004 5006h                 | 5008 5006h                 | 500C 5006h                |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5004 5008h                 | 5008 5008h                 | 500C 5008h                |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5004 500Ah                 | 5008 500Ah                 | 500C 500Ah                |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 5004 500Ch                 | 5008 500Ch                 | 500C 500Ch                |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5004 500Eh                 | 5008 500Eh                 | 500C 500Eh                |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5004 5010h                 | 5008 5010h                 | 500C 5010h                |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5004 5012h                 | 5008 5012h                 | 500C 5012h                |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 5004 5018h                 | 5008 5018h                 | 500C 5018h                |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 5004 501Ah                 | 5008 501Ah                 | 500C 501Ah                |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 5004 5020h                 | 5008 5020h                 | 500C 5020h                |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 5004 5022h                 | 5008 5022h                 | 500C 5022h                |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 5004 5028h                 | 5008 5028h                 | 500C 5028h                |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 5004 5030h                 | 5008 5030h                 | 500C 5030h                |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 5004 5032h                 | 5008 5032h                 | 500C 5032h                |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 5004 5040h                 | 5008 5040h                 | 500C 5040h                |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 5004 504Eh                 | 5008 504Eh                 | 500C 504Eh                |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>        | 5004 505Ah                 | 5008 505Ah                 | 500C 505Ah                |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>         | 5004 505Ch                 | 5008 505Ch                 | 500C 505Ch                |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>        | 5004 5068h                 | 5008 5068h                 | 500C 5068h                |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>        | 5004 506Ah                 | 5008 506Ah                 | 500C 506Ah                |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>     | 5004 5070h                 | 5008 5070h                 | 500C 5070h                |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>    | 5004 5074h                 | 5008 5074h                 | 500C 5074h                |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>         | 5004 507Ah                 | 5008 507Ah                 | 500C 507Ah                |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>       | 5004 507Ch                 | 5008 507Ch                 | 500C 507Ch                |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>      | 5004 507Eh                 | 5008 507Eh                 | 500C 507Eh                |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>        | 5004 5080h                 | 5008 5080h                 | 500C 5080h                |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>       | 5004 5082h                 | 5008 5082h                 | 500C 5082h                |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>        | 5004 5084h                 | 5008 5084h                 | 500C 5084h                |



**Table 3-778. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                     | EPWM28_G0 Physical Address | EPWM29_G0 Physical Address | EPWM3_G0 Physical Address |
|--------|--------|-----------------------------------|----------------------------|----------------------------|---------------------------|
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>      | 5004 5086h                 | 5008 5086h                 | 500C 5086h                |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>       | 5004 508Eh                 | 5008 508Eh                 | 500C 508Eh                |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>      | 5004 5092h                 | 5008 5092h                 | 500C 5092h                |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>      | 5004 50A0h                 | 5008 50A0h                 | 500C 50A0h                |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>        | 5004 50A2h                 | 5008 50A2h                 | 500C 50A2h                |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>      | 5004 50A4h                 | 5008 50A4h                 | 500C 50A4h                |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>        | 5004 50A6h                 | 5008 50A6h                 | 500C 50A6h                |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>        | 5004 50C0h                 | 5008 50C0h                 | 500C 50C0h                |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>      | 5004 50C4h                 | 5008 50C4h                 | 500C 50C4h                |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>        | 5004 50C6h                 | 5008 50C6h                 | 500C 50C6h                |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>     | 5004 50C8h                 | 5008 50C8h                 | 500C 50C8h                |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>         | 5004 50D4h                 | 5008 50D4h                 | 500C 50D4h                |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>         | 5004 50D8h                 | 5008 50D8h                 | 500C 50D8h                |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>         | 5004 50DEh                 | 5008 50DEh                 | 500C 50DEh                |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>         | 5004 50E2h                 | 5008 50E2h                 | 500C 50E2h                |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>      | 5004 50E8h                 | 5008 50E8h                 | 500C 50E8h                |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>    | 5004 50EEh                 | 5008 50EEh                 | 500C 50EEh                |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>        | 5004 5100h                 | 5008 5100h                 | 500C 5100h                |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>       | 5004 5102h                 | 5008 5102h                 | 500C 5102h                |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>      | 5004 5104h                 | 5008 5104h                 | 500C 5104h                |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>        | 5004 5108h                 | 5008 5108h                 | 500C 5108h                |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>       | 5004 510Ah                 | 5008 510Ah                 | 500C 510Ah                |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>     | 5004 510Ch                 | 5008 510Ch                 | 500C 510Ch                |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>     | 5004 510Eh                 | 5008 510Eh                 | 500C 510Eh                |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>       | 5004 511Ah                 | 5008 511Ah                 | 500C 511Ah                |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>        | 5004 5126h                 | 5008 5126h                 | 500C 5126h                |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>     | 5004 5128h                 | 5008 5128h                 | 500C 5128h                |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>     | 5004 512Ah                 | 5008 512Ah                 | 500C 512Ah                |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>        | 5004 512Eh                 | 5008 512Eh                 | 500C 512Eh                |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>     | 5004 5130h                 | 5008 5130h                 | 500C 5130h                |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>     | 5004 5132h                 | 5008 5132h                 | 500C 5132h                |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>        | 5004 5136h                 | 5008 5136h                 | 500C 5136h                |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a> | 5004 513Ah                 | 5008 513Ah                 | 500C 513Ah                |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>        | 5004 5148h                 | 5008 5148h                 | 500C 5148h                |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>         | 5004 514Ch                 | 5008 514Ch                 | 500C 514Ch                |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>        | 5004 5150h                 | 5008 5150h                 | 500C 5150h                |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>        | 5004 5154h                 | 5008 5154h                 | 500C 5154h                |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>        | 5004 5158h                 | 5008 5158h                 | 500C 5158h                |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>      | 5004 515Ch                 | 5008 515Ch                 | 500C 515Ch                |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>      | 5004 5160h                 | 5008 5160h                 | 500C 5160h                |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a> | 5004 5164h                 | 5008 5164h                 | 500C 5164h                |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>    | 5004 5168h                 | 5008 5168h                 | 500C 5168h                |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>   | 5004 516Ch                 | 5008 516Ch                 | 500C 516Ch                |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>  | 5004 5170h                 | 5008 5170h                 | 500C 5170h                |

**Table 3-778. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM28_G0 Physical Address | EPWM29_G0 Physical Address | EPWM3_G0 Physical Address |
|--------|--------|---------------------------------------|----------------------------|----------------------------|---------------------------|
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 5004 5174h                 | 5008 5174h                 | 500C 5174h                |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 5004 5180h                 | 5008 5180h                 | 500C 5180h                |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 5004 5186h                 | 5008 5186h                 | 500C 5186h                |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5004 5188h                 | 5008 5188h                 | 500C 5188h                |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5004 518Eh                 | 5008 518Eh                 | 500C 518Eh                |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5004 5190h                 | 5008 5190h                 | 500C 5190h                |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5004 5192h                 | 5008 5192h                 | 500C 5192h                |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5004 5194h                 | 5008 5194h                 | 500C 5194h                |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5004 5196h                 | 5008 5196h                 | 500C 5196h                |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5004 5198h                 | 5008 5198h                 | 500C 5198h                |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5004 519Ah                 | 5008 519Ah                 | 500C 519Ah                |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5004 519Ch                 | 5008 519Ch                 | 500C 519Ch                |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5004 519Eh                 | 5008 519Eh                 | 500C 519Eh                |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5004 51A4h                 | 5008 51A4h                 | 500C 51A4h                |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5004 51A6h                 | 5008 51A6h                 | 500C 51A6h                |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 5004 51A8h                 | 5008 51A8h                 | 500C 51A8h                |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 5004 51AAh                 | 5008 51AAh                 | 500C 51AAh                |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 5004 51ACh                 | 5008 51ACh                 | 500C 51ACh                |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 5004 51AEh                 | 5008 51AEh                 | 500C 51AEh                |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 5004 51B0h                 | 5008 51B0h                 | 500C 51B0h                |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 5004 51B2h                 | 5008 51B2h                 | 500C 51B2h                |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 5004 51F4h                 | 5008 51F4h                 | 500C 51F4h                |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 5004 51FAh                 | 5008 51FAh                 | 500C 51FAh                |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 5004 51FCh                 | 5008 51FCh                 | 500C 51FCh                |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>         | 5004 5400h                 | 5008 5400h                 | 500C 5400h                |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>         | 5004 5410h                 | 5008 5410h                 | 500C 5410h                |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>            | 5004 5418h                 | 5008 5418h                 | 500C 5418h                |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a>   | 5004 541Ch                 | 5008 541Ch                 | 500C 541Ch                |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>     | 5004 5420h                 | 5008 5420h                 | 500C 5420h                |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>     | 5004 5428h                 | 5008 5428h                 | 500C 5428h                |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>     | 5004 5430h                 | 5008 5430h                 | 500C 5430h                |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>     | 5004 5600h                 | 5008 5600h                 | 500C 5600h                |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>     | 5004 5604h                 | 5008 5604h                 | 500C 5604h                |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>     | 5004 5608h                 | 5008 5608h                 | 500C 5608h                |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>     | 5004 560Ch                 | 5008 560Ch                 | 500C 560Ch                |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>     | 5004 5610h                 | 5008 5610h                 | 500C 5610h                |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>     | 5004 5614h                 | 5008 5614h                 | 500C 5614h                |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>     | 5004 5618h                 | 5008 5618h                 | 500C 5618h                |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>     | 5004 561Ch                 | 5008 561Ch                 | 500C 561Ch                |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>    | 5004 5620h                 | 5008 5620h                 | 500C 5620h                |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a>   | 5004 5630h                 | 5008 5630h                 | 500C 5630h                |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a>   | 5004 5632h                 | 5008 5632h                 | 500C 5632h                |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a>   | 5004 5644h                 | 5008 5644h                 | 500C 5644h                |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>      | 5004 5680h                 | 5008 5680h                 | 500C 5680h                |

**Table 3-778. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM28_G0 Physical Address | EPWM29_G0 Physical Address | EPWM3_G0 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|---------------------------|
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>   | 5004 5684h                 | 5008 5684h                 | 500C 5684h                |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>   | 5004 5688h                 | 5008 5688h                 | 500C 5688h                |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>   | 5004 568Ch                 | 5008 568Ch                 | 500C 568Ch                |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>   | 5004 5690h                 | 5008 5690h                 | 500C 5690h                |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>   | 5004 5694h                 | 5008 5694h                 | 500C 5694h                |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>   | 5004 5698h                 | 5008 5698h                 | 500C 5698h                |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>   | 5004 569Ch                 | 5008 569Ch                 | 500C 569Ch                |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>  | 5004 56A0h                 | 5008 56A0h                 | 500C 56A0h                |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a> | 5004 56B0h                 | 5008 56B0h                 | 500C 56B0h                |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a> | 5004 56B2h                 | 5008 56B2h                 | 500C 56B2h                |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>    | 5004 56BAh                 | 5008 56BAh                 | 500C 56BAh                |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>    | 5004 56BEh                 | 5008 56BEh                 | 500C 56BEh                |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a> | 5004 56C4h                 | 5008 56C4h                 | 500C 56C4h                |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>   | 5004 5700h                 | 5008 5700h                 | 500C 5700h                |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>   | 5004 5704h                 | 5008 5704h                 | 500C 5704h                |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>   | 5004 5708h                 | 5008 5708h                 | 500C 5708h                |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>   | 5004 570Ch                 | 5008 570Ch                 | 500C 570Ch                |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>   | 5004 5710h                 | 5008 5710h                 | 500C 5710h                |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>   | 5004 5714h                 | 5008 5714h                 | 500C 5714h                |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>   | 5004 5718h                 | 5008 5718h                 | 500C 5718h                |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>   | 5004 571Ch                 | 5008 571Ch                 | 500C 571Ch                |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>  | 5004 5720h                 | 5008 5720h                 | 500C 5720h                |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a> | 5004 5730h                 | 5008 5730h                 | 500C 5730h                |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a> | 5004 5732h                 | 5008 5732h                 | 500C 5732h                |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>    | 5004 573Ah                 | 5008 573Ah                 | 500C 573Ah                |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>    | 5004 573Eh                 | 5008 573Eh                 | 500C 573Eh                |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a> | 5004 5744h                 | 5008 5744h                 | 500C 5744h                |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 5004 5780h                 | 5008 5780h                 | 500C 5780h                |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 5004 5784h                 | 5008 5784h                 | 500C 5784h                |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 5004 5788h                 | 5008 5788h                 | 500C 5788h                |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 5004 578Ch                 | 5008 578Ch                 | 500C 578Ch                |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 5004 5790h                 | 5008 5790h                 | 500C 5790h                |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 5004 5794h                 | 5008 5794h                 | 500C 5794h                |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 5004 5798h                 | 5008 5798h                 | 500C 5798h                |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 5004 579Ch                 | 5008 579Ch                 | 500C 579Ch                |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 5004 57A0h                 | 5008 57A0h                 | 500C 57A0h                |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5004 57B0h                 | 5008 57B0h                 | 500C 57B0h                |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5004 57B2h                 | 5008 57B2h                 | 500C 57B2h                |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5004 57BAh                 | 5008 57BAh                 | 500C 57BAh                |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5004 57BEh                 | 5008 57BEh                 | 500C 57BEh                |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5004 57C4h                 | 5008 57C4h                 | 500C 57C4h                |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5004 5800h                 | 5008 5800h                 | 500C 5800h                |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5004 5804h                 | 5008 5804h                 | 500C 5804h                |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5004 5808h                 | 5008 5808h                 | 500C 5808h                |

**Table 3-778. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                   | EPWM28_G0 Physical Address | EPWM29_G0 Physical Address | EPWM3_G0 Physical Address |
|--------|--------|---------------------------------|----------------------------|----------------------------|---------------------------|
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>      | 5004 580Ch                 | 5008 580Ch                 | 500C 580Ch                |
| 810h   | 32     | <a href="#">EPWM_DEFRFC</a>     | 5004 5810h                 | 5008 5810h                 | 500C 5810h                |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>      | 5004 5814h                 | 5008 5814h                 | 500C 5814h                |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>   | 5004 5820h                 | 5008 5820h                 | 500C 5820h                |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>   | 5004 5824h                 | 5008 5824h                 | 500C 5824h                |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>  | 5004 5828h                 | 5008 5828h                 | 500C 5828h                |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a> | 5004 582Ch                 | 5008 582Ch                 | 500C 582Ch                |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>  | 5004 5C00h                 | 5008 5C00h                 | 500C 5C00h                |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>   | 5004 5C04h                 | 5008 5C04h                 | 500C 5C04h                |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>    | 5004 5C20h                 | 5008 5C20h                 | 500C 5C20h                |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>    | 5004 5C24h                 | 5008 5C24h                 | 500C 5C24h                |

**Table 3-779. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM30_G0 Physical Address | EPWM31_G0 Physical Address | EPWM4_G0 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|---------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5000 6000h                 | 5004 6000h                 | 5008 6000h                |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5000 6002h                 | 5004 6002h                 | 5008 6002h                |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5000 6006h                 | 5004 6006h                 | 5008 6006h                |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5000 6008h                 | 5004 6008h                 | 5008 6008h                |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5000 600Ah                 | 5004 600Ah                 | 5008 600Ah                |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 5000 600Ch                 | 5004 600Ch                 | 5008 600Ch                |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5000 600Eh                 | 5004 600Eh                 | 5008 600Eh                |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5000 6010h                 | 5004 6010h                 | 5008 6010h                |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5000 6012h                 | 5004 6012h                 | 5008 6012h                |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 5000 6018h                 | 5004 6018h                 | 5008 6018h                |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 5000 601Ah                 | 5004 601Ah                 | 5008 601Ah                |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 5000 6020h                 | 5004 6020h                 | 5008 6020h                |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 5000 6022h                 | 5004 6022h                 | 5008 6022h                |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 5000 6028h                 | 5004 6028h                 | 5008 6028h                |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 5000 6030h                 | 5004 6030h                 | 5008 6030h                |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 5000 6032h                 | 5004 6032h                 | 5008 6032h                |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 5000 6040h                 | 5004 6040h                 | 5008 6040h                |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 5000 604Eh                 | 5004 604Eh                 | 5008 604Eh                |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>        | 5000 605Ah                 | 5004 605Ah                 | 5008 605Ah                |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>         | 5000 605Ch                 | 5004 605Ch                 | 5008 605Ch                |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>        | 5000 6068h                 | 5004 6068h                 | 5008 6068h                |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>        | 5000 606Ah                 | 5004 606Ah                 | 5008 606Ah                |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>     | 5000 6070h                 | 5004 6070h                 | 5008 6070h                |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>    | 5000 6074h                 | 5004 6074h                 | 5008 6074h                |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>         | 5000 607Ah                 | 5004 607Ah                 | 5008 607Ah                |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>       | 5000 607Ch                 | 5004 607Ch                 | 5008 607Ch                |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>      | 5000 607Eh                 | 5004 607Eh                 | 5008 607Eh                |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>        | 5000 6080h                 | 5004 6080h                 | 5008 6080h                |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>       | 5000 6082h                 | 5004 6082h                 | 5008 6082h                |

**Table 3-779. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                     | EPWM30_G0 Physical Address | EPWM31_G0 Physical Address | EPWM4_G0 Physical Address |
|--------|--------|-----------------------------------|----------------------------|----------------------------|---------------------------|
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>       | 5000 6084h                 | 5004 6084h                 | 5008 6084h                |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>      | 5000 6086h                 | 5004 6086h                 | 5008 6086h                |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>       | 5000 608Eh                 | 5004 608Eh                 | 5008 608Eh                |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>      | 5000 6092h                 | 5004 6092h                 | 5008 6092h                |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>      | 5000 60A0h                 | 5004 60A0h                 | 5008 60A0h                |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>        | 5000 60A2h                 | 5004 60A2h                 | 5008 60A2h                |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>      | 5000 60A4h                 | 5004 60A4h                 | 5008 60A4h                |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>        | 5000 60A6h                 | 5004 60A6h                 | 5008 60A6h                |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>        | 5000 60C0h                 | 5004 60C0h                 | 5008 60C0h                |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>      | 5000 60C4h                 | 5004 60C4h                 | 5008 60C4h                |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>        | 5000 60C6h                 | 5004 60C6h                 | 5008 60C6h                |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>     | 5000 60C8h                 | 5004 60C8h                 | 5008 60C8h                |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>         | 5000 60D4h                 | 5004 60D4h                 | 5008 60D4h                |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>         | 5000 60D8h                 | 5004 60D8h                 | 5008 60D8h                |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>         | 5000 60DEh                 | 5004 60DEh                 | 5008 60DEh                |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>         | 5000 60E2h                 | 5004 60E2h                 | 5008 60E2h                |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>      | 5000 60E8h                 | 5004 60E8h                 | 5008 60E8h                |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>    | 5000 60EEh                 | 5004 60EEh                 | 5008 60EEh                |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>        | 5000 6100h                 | 5004 6100h                 | 5008 6100h                |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>       | 5000 6102h                 | 5004 6102h                 | 5008 6102h                |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>      | 5000 6104h                 | 5004 6104h                 | 5008 6104h                |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>        | 5000 6108h                 | 5004 6108h                 | 5008 6108h                |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>       | 5000 610Ah                 | 5004 610Ah                 | 5008 610Ah                |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>     | 5000 610Ch                 | 5004 610Ch                 | 5008 610Ch                |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>     | 5000 610Eh                 | 5004 610Eh                 | 5008 610Eh                |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>       | 5000 611Ah                 | 5004 611Ah                 | 5008 611Ah                |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>        | 5000 6126h                 | 5004 6126h                 | 5008 6126h                |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>     | 5000 6128h                 | 5004 6128h                 | 5008 6128h                |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>     | 5000 612Ah                 | 5004 612Ah                 | 5008 612Ah                |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>        | 5000 612Eh                 | 5004 612Eh                 | 5008 612Eh                |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>     | 5000 6130h                 | 5004 6130h                 | 5008 6130h                |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>     | 5000 6132h                 | 5004 6132h                 | 5008 6132h                |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>        | 5000 6136h                 | 5004 6136h                 | 5008 6136h                |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a> | 5000 613Ah                 | 5004 613Ah                 | 5008 613Ah                |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>        | 5000 6148h                 | 5004 6148h                 | 5008 6148h                |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>         | 5000 614Ch                 | 5004 614Ch                 | 5008 614Ch                |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>        | 5000 6150h                 | 5004 6150h                 | 5008 6150h                |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>        | 5000 6154h                 | 5004 6154h                 | 5008 6154h                |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>        | 5000 6158h                 | 5004 6158h                 | 5008 6158h                |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>      | 5000 615Ch                 | 5004 615Ch                 | 5008 615Ch                |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>      | 5000 6160h                 | 5004 6160h                 | 5008 6160h                |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a> | 5000 6164h                 | 5004 6164h                 | 5008 6164h                |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>    | 5000 6168h                 | 5004 6168h                 | 5008 6168h                |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>   | 5000 616Ch                 | 5004 616Ch                 | 5008 616Ch                |

**Table 3-779. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM30_G0 Physical Address | EPWM31_G0 Physical Address | EPWM4_G0 Physical Address |
|--------|--------|---------------------------------------|----------------------------|----------------------------|---------------------------|
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 5000 6170h                 | 5004 6170h                 | 5008 6170h                |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 5000 6174h                 | 5004 6174h                 | 5008 6174h                |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 5000 6180h                 | 5004 6180h                 | 5008 6180h                |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 5000 6186h                 | 5004 6186h                 | 5008 6186h                |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5000 6188h                 | 5004 6188h                 | 5008 6188h                |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5000 618Eh                 | 5004 618Eh                 | 5008 618Eh                |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5000 6190h                 | 5004 6190h                 | 5008 6190h                |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5000 6192h                 | 5004 6192h                 | 5008 6192h                |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5000 6194h                 | 5004 6194h                 | 5008 6194h                |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5000 6196h                 | 5004 6196h                 | 5008 6196h                |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5000 6198h                 | 5004 6198h                 | 5008 6198h                |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5000 619Ah                 | 5004 619Ah                 | 5008 619Ah                |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5000 619Ch                 | 5004 619Ch                 | 5008 619Ch                |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5000 619Eh                 | 5004 619Eh                 | 5008 619Eh                |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5000 61A4h                 | 5004 61A4h                 | 5008 61A4h                |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5000 61A6h                 | 5004 61A6h                 | 5008 61A6h                |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 5000 61A8h                 | 5004 61A8h                 | 5008 61A8h                |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 5000 61AAh                 | 5004 61AAh                 | 5008 61AAh                |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 5000 61ACh                 | 5004 61ACh                 | 5008 61ACh                |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 5000 61AEh                 | 5004 61AEh                 | 5008 61AEh                |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 5000 61B0h                 | 5004 61B0h                 | 5008 61B0h                |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 5000 61B2h                 | 5004 61B2h                 | 5008 61B2h                |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 5000 61F4h                 | 5004 61F4h                 | 5008 61F4h                |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 5000 61FAh                 | 5004 61FAh                 | 5008 61FAh                |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 5000 61FCh                 | 5004 61FCh                 | 5008 61FCh                |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>         | 5000 6400h                 | 5004 6400h                 | 5008 6400h                |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>         | 5000 6410h                 | 5004 6410h                 | 5008 6410h                |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>            | 5000 6418h                 | 5004 6418h                 | 5008 6418h                |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a>   | 5000 641Ch                 | 5004 641Ch                 | 5008 641Ch                |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>     | 5000 6420h                 | 5004 6420h                 | 5008 6420h                |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>     | 5000 6428h                 | 5004 6428h                 | 5008 6428h                |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>     | 5000 6430h                 | 5004 6430h                 | 5008 6430h                |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>     | 5000 6600h                 | 5004 6600h                 | 5008 6600h                |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>     | 5000 6604h                 | 5004 6604h                 | 5008 6604h                |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>     | 5000 6608h                 | 5004 6608h                 | 5008 6608h                |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>     | 5000 660Ch                 | 5004 660Ch                 | 5008 660Ch                |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>     | 5000 6610h                 | 5004 6610h                 | 5008 6610h                |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>     | 5000 6614h                 | 5004 6614h                 | 5008 6614h                |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>     | 5000 6618h                 | 5004 6618h                 | 5008 6618h                |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>     | 5000 661Ch                 | 5004 661Ch                 | 5008 661Ch                |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>    | 5000 6620h                 | 5004 6620h                 | 5008 6620h                |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a>   | 5000 6630h                 | 5004 6630h                 | 5008 6630h                |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a>   | 5000 6632h                 | 5004 6632h                 | 5008 6632h                |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a>   | 5000 6644h                 | 5004 6644h                 | 5008 6644h                |



**Table 3-779. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM30_G0 Physical Address | EPWM31_G0 Physical Address | EPWM4_G0 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|---------------------------|
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>   | 5000 6680h                 | 5004 6680h                 | 5008 6680h                |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>   | 5000 6684h                 | 5004 6684h                 | 5008 6684h                |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>   | 5000 6688h                 | 5004 6688h                 | 5008 6688h                |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>   | 5000 668Ch                 | 5004 668Ch                 | 5008 668Ch                |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>   | 5000 6690h                 | 5004 6690h                 | 5008 6690h                |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>   | 5000 6694h                 | 5004 6694h                 | 5008 6694h                |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>   | 5000 6698h                 | 5004 6698h                 | 5008 6698h                |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>   | 5000 669Ch                 | 5004 669Ch                 | 5008 669Ch                |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>  | 5000 66A0h                 | 5004 66A0h                 | 5008 66A0h                |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a> | 5000 66B0h                 | 5004 66B0h                 | 5008 66B0h                |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a> | 5000 66B2h                 | 5004 66B2h                 | 5008 66B2h                |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>    | 5000 66BAh                 | 5004 66BAh                 | 5008 66BAh                |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>    | 5000 66BEh                 | 5004 66BEh                 | 5008 66BEh                |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a> | 5000 66C4h                 | 5004 66C4h                 | 5008 66C4h                |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>   | 5000 6700h                 | 5004 6700h                 | 5008 6700h                |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>   | 5000 6704h                 | 5004 6704h                 | 5008 6704h                |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>   | 5000 6708h                 | 5004 6708h                 | 5008 6708h                |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>   | 5000 670Ch                 | 5004 670Ch                 | 5008 670Ch                |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>   | 5000 6710h                 | 5004 6710h                 | 5008 6710h                |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>   | 5000 6714h                 | 5004 6714h                 | 5008 6714h                |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>   | 5000 6718h                 | 5004 6718h                 | 5008 6718h                |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>   | 5000 671Ch                 | 5004 671Ch                 | 5008 671Ch                |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>  | 5000 6720h                 | 5004 6720h                 | 5008 6720h                |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a> | 5000 6730h                 | 5004 6730h                 | 5008 6730h                |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a> | 5000 6732h                 | 5004 6732h                 | 5008 6732h                |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>    | 5000 673Ah                 | 5004 673Ah                 | 5008 673Ah                |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>    | 5000 673Eh                 | 5004 673Eh                 | 5008 673Eh                |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a> | 5000 6744h                 | 5004 6744h                 | 5008 6744h                |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 5000 6780h                 | 5004 6780h                 | 5008 6780h                |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 5000 6784h                 | 5004 6784h                 | 5008 6784h                |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 5000 6788h                 | 5004 6788h                 | 5008 6788h                |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 5000 678Ch                 | 5004 678Ch                 | 5008 678Ch                |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 5000 6790h                 | 5004 6790h                 | 5008 6790h                |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 5000 6794h                 | 5004 6794h                 | 5008 6794h                |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 5000 6798h                 | 5004 6798h                 | 5008 6798h                |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 5000 679Ch                 | 5004 679Ch                 | 5008 679Ch                |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 5000 67A0h                 | 5004 67A0h                 | 5008 67A0h                |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5000 67B0h                 | 5004 67B0h                 | 5008 67B0h                |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5000 67B2h                 | 5004 67B2h                 | 5008 67B2h                |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5000 67BAh                 | 5004 67BAh                 | 5008 67BAh                |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5000 67BEh                 | 5004 67BEh                 | 5008 67BEh                |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5000 67C4h                 | 5004 67C4h                 | 5008 67C4h                |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5000 6800h                 | 5004 6800h                 | 5008 6800h                |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5000 6804h                 | 5004 6804h                 | 5008 6804h                |

**Table 3-779. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                   | EPWM30_G0 Physical Address | EPWM31_G0 Physical Address | EPWM4_G0 Physical Address |
|--------|--------|---------------------------------|----------------------------|----------------------------|---------------------------|
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>   | 5000 6808h                 | 5004 6808h                 | 5008 6808h                |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>      | 5000 680Ch                 | 5004 680Ch                 | 5008 680Ch                |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>      | 5000 6810h                 | 5004 6810h                 | 5008 6810h                |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>      | 5000 6814h                 | 5004 6814h                 | 5008 6814h                |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>   | 5000 6820h                 | 5004 6820h                 | 5008 6820h                |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>   | 5000 6824h                 | 5004 6824h                 | 5008 6824h                |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>  | 5000 6828h                 | 5004 6828h                 | 5008 6828h                |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a> | 5000 682Ch                 | 5004 682Ch                 | 5008 682Ch                |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>  | 5000 6C00h                 | 5004 6C00h                 | 5008 6C00h                |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>   | 5000 6C04h                 | 5004 6C04h                 | 5008 6C04h                |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>    | 5000 6C20h                 | 5004 6C20h                 | 5008 6C20h                |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>    | 5000 6C24h                 | 5004 6C24h                 | 5008 6C24h                |

**Table 3-780. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM5_G0 Physical Address | EPWM6_G0 Physical Address | EPWM7_G0 Physical Address |
|--------|--------|------------------------------------|---------------------------|---------------------------|---------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 500C 6000h                | 5000 7000h                | 5004 7000h                |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 500C 6002h                | 5000 7002h                | 5004 7002h                |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 500C 6006h                | 5000 7006h                | 5004 7006h                |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 500C 6008h                | 5000 7008h                | 5004 7008h                |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 500C 600Ah                | 5000 700Ah                | 5004 700Ah                |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 500C 600Ch                | 5000 700Ch                | 5004 700Ch                |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 500C 600Eh                | 5000 700Eh                | 5004 700Eh                |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 500C 6010h                | 5000 7010h                | 5004 7010h                |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 500C 6012h                | 5000 7012h                | 5004 7012h                |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 500C 6018h                | 5000 7018h                | 5004 7018h                |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 500C 601Ah                | 5000 701Ah                | 5004 701Ah                |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 500C 6020h                | 5000 7020h                | 5004 7020h                |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 500C 6022h                | 5000 7022h                | 5004 7022h                |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 500C 6028h                | 5000 7028h                | 5004 7028h                |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 500C 6030h                | 5000 7030h                | 5004 7030h                |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 500C 6032h                | 5000 7032h                | 5004 7032h                |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 500C 6040h                | 5000 7040h                | 5004 7040h                |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 500C 604Eh                | 5000 704Eh                | 5004 704Eh                |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>        | 500C 605Ah                | 5000 705Ah                | 5004 705Ah                |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>         | 500C 605Ch                | 5000 705Ch                | 5004 705Ch                |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>        | 500C 6068h                | 5000 7068h                | 5004 7068h                |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>        | 500C 606Ah                | 5000 706Ah                | 5004 706Ah                |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>     | 500C 6070h                | 5000 7070h                | 5004 7070h                |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>    | 500C 6074h                | 5000 7074h                | 5004 7074h                |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>         | 500C 607Ah                | 5000 707Ah                | 5004 707Ah                |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>       | 500C 607Ch                | 5000 707Ch                | 5004 707Ch                |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>      | 500C 607Eh                | 5000 707Eh                | 5004 707Eh                |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>        | 500C 6080h                | 5000 7080h                | 5004 7080h                |



**Table 3-780. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                     | EPWM5_G0 Physical Address | EPWM6_G0 Physical Address | EPWM7_G0 Physical Address |
|--------|--------|-----------------------------------|---------------------------|---------------------------|---------------------------|
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>      | 500C 6082h                | 5000 7082h                | 5004 7082h                |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>       | 500C 6084h                | 5000 7084h                | 5004 7084h                |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>      | 500C 6086h                | 5000 7086h                | 5004 7086h                |
| 8Eh    | 16     | <a href="#">EPWM_AQSFR</a>        | 500C 608Eh                | 5000 708Eh                | 5004 708Eh                |
| 92h    | 16     | <a href="#">EPWM_AQCSFR</a>       | 500C 6092h                | 5000 7092h                | 5004 7092h                |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>      | 500C 60A0h                | 5000 70A0h                | 5004 70A0h                |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>        | 500C 60A2h                | 5000 70A2h                | 5004 70A2h                |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>      | 500C 60A4h                | 5000 70A4h                | 5004 70A4h                |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>        | 500C 60A6h                | 5000 70A6h                | 5004 70A6h                |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>        | 500C 60C0h                | 5000 70C0h                | 5004 70C0h                |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>      | 500C 60C4h                | 5000 70C4h                | 5004 70C4h                |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>        | 500C 60C6h                | 5000 70C6h                | 5004 70C6h                |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>     | 500C 60C8h                | 5000 70C8h                | 5004 70C8h                |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>         | 500C 60D4h                | 5000 70D4h                | 5004 70D4h                |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>         | 500C 60D8h                | 5000 70D8h                | 5004 70D8h                |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>         | 500C 60DEh                | 5000 70DEh                | 5004 70DEh                |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>         | 500C 60E2h                | 5000 70E2h                | 5004 70E2h                |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>      | 500C 60E8h                | 5000 70E8h                | 5004 70E8h                |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>    | 500C 60EEh                | 5000 70EEh                | 5004 70EEh                |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>        | 500C 6100h                | 5000 7100h                | 5004 7100h                |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>       | 500C 6102h                | 5000 7102h                | 5004 7102h                |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>      | 500C 6104h                | 5000 7104h                | 5004 7104h                |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>        | 500C 6108h                | 5000 7108h                | 5004 7108h                |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>       | 500C 610Ah                | 5000 710Ah                | 5004 710Ah                |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>     | 500C 610Ch                | 5000 710Ch                | 5004 710Ch                |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>     | 500C 610Eh                | 5000 710Eh                | 5004 710Eh                |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>       | 500C 611Ah                | 5000 711Ah                | 5004 711Ah                |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>        | 500C 6126h                | 5000 7126h                | 5004 7126h                |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>     | 500C 6128h                | 5000 7128h                | 5004 7128h                |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>     | 500C 612Ah                | 5000 712Ah                | 5004 712Ah                |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>        | 500C 612Eh                | 5000 712Eh                | 5004 712Eh                |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>     | 500C 6130h                | 5000 7130h                | 5004 7130h                |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>     | 500C 6132h                | 5000 7132h                | 5004 7132h                |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>        | 500C 6136h                | 5000 7136h                | 5004 7136h                |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a> | 500C 613Ah                | 5000 713Ah                | 5004 713Ah                |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>        | 500C 6148h                | 5000 7148h                | 5004 7148h                |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>         | 500C 614Ch                | 5000 714Ch                | 5004 714Ch                |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>        | 500C 6150h                | 5000 7150h                | 5004 7150h                |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>        | 500C 6154h                | 5000 7154h                | 5004 7154h                |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>        | 500C 6158h                | 5000 7158h                | 5004 7158h                |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>      | 500C 615Ch                | 5000 715Ch                | 5004 715Ch                |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>      | 500C 6160h                | 5000 7160h                | 5004 7160h                |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a> | 500C 6164h                | 5000 7164h                | 5004 7164h                |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>    | 500C 6168h                | 5000 7168h                | 5004 7168h                |

**Table 3-780. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM5_G0 Physical Address | EPWM6_G0 Physical Address | EPWM7_G0 Physical Address |
|--------|--------|---------------------------------------|---------------------------|---------------------------|---------------------------|
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 500C 616Ch                | 5000 716Ch                | 5004 716Ch                |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 500C 6170h                | 5000 7170h                | 5004 7170h                |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 500C 6174h                | 5000 7174h                | 5004 7174h                |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 500C 6180h                | 5000 7180h                | 5004 7180h                |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 500C 6186h                | 5000 7186h                | 5004 7186h                |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 500C 6188h                | 5000 7188h                | 5004 7188h                |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 500C 618Eh                | 5000 718Eh                | 5004 718Eh                |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 500C 6190h                | 5000 7190h                | 5004 7190h                |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 500C 6192h                | 5000 7192h                | 5004 7192h                |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 500C 6194h                | 5000 7194h                | 5004 7194h                |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 500C 6196h                | 5000 7196h                | 5004 7196h                |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 500C 6198h                | 5000 7198h                | 5004 7198h                |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 500C 619Ah                | 5000 719Ah                | 5004 719Ah                |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 500C 619Ch                | 5000 719Ch                | 5004 719Ch                |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 500C 619Eh                | 5000 719Eh                | 5004 719Eh                |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 500C 61A4h                | 5000 71A4h                | 5004 71A4h                |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 500C 61A6h                | 5000 71A6h                | 5004 71A6h                |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 500C 61A8h                | 5000 71A8h                | 5004 71A8h                |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 500C 61AAh                | 5000 71AAh                | 5004 71AAh                |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 500C 61ACh                | 5000 71ACh                | 5004 71ACh                |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 500C 61AEh                | 5000 71AEh                | 5004 71AEh                |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 500C 61B0h                | 5000 71B0h                | 5004 71B0h                |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 500C 61B2h                | 5000 71B2h                | 5004 71B2h                |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 500C 61F4h                | 5000 71F4h                | 5004 71F4h                |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 500C 61FAh                | 5000 71FAh                | 5004 71FAh                |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 500C 61FCh                | 5000 71FCh                | 5004 71FCh                |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>         | 500C 6400h                | 5000 7400h                | 5004 7400h                |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>         | 500C 6410h                | 5000 7410h                | 5004 7410h                |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>            | 500C 6418h                | 5000 7418h                | 5004 7418h                |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a>   | 500C 641Ch                | 5000 741Ch                | 5004 741Ch                |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>     | 500C 6420h                | 5000 7420h                | 5004 7420h                |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>     | 500C 6428h                | 5000 7428h                | 5004 7428h                |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>     | 500C 6430h                | 5000 7430h                | 5004 7430h                |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>     | 500C 6600h                | 5000 7600h                | 5004 7600h                |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>     | 500C 6604h                | 5000 7604h                | 5004 7604h                |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>     | 500C 6608h                | 5000 7608h                | 5004 7608h                |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>     | 500C 660Ch                | 5000 760Ch                | 5004 760Ch                |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>     | 500C 6610h                | 5000 7610h                | 5004 7610h                |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>     | 500C 6614h                | 5000 7614h                | 5004 7614h                |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>     | 500C 6618h                | 5000 7618h                | 5004 7618h                |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>     | 500C 661Ch                | 5000 761Ch                | 5004 761Ch                |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>    | 500C 6620h                | 5000 7620h                | 5004 7620h                |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a>   | 500C 6630h                | 5000 7630h                | 5004 7630h                |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a>   | 500C 6632h                | 5000 7632h                | 5004 7632h                |

**Table 3-780. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM5_G0 Physical Address | EPWM6_G0 Physical Address | EPWM7_G0 Physical Address |
|--------|--------|-------------------------------------|---------------------------|---------------------------|---------------------------|
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 500C 6644h                | 5000 7644h                | 5004 7644h                |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 500C 6680h                | 5000 7680h                | 5004 7680h                |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 500C 6684h                | 5000 7684h                | 5004 7684h                |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 500C 6688h                | 5000 7688h                | 5004 7688h                |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 500C 668Ch                | 5000 768Ch                | 5004 768Ch                |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 500C 6690h                | 5000 7690h                | 5004 7690h                |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 500C 6694h                | 5000 7694h                | 5004 7694h                |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 500C 6698h                | 5000 7698h                | 5004 7698h                |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 500C 669Ch                | 5000 769Ch                | 5004 769Ch                |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 500C 66A0h                | 5000 76A0h                | 5004 76A0h                |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 500C 66B0h                | 5000 76B0h                | 5004 76B0h                |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 500C 66B2h                | 5000 76B2h                | 5004 76B2h                |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 500C 66BAh                | 5000 76BAh                | 5004 76BAh                |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 500C 66BEh                | 5000 76BEh                | 5004 76BEh                |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 500C 66C4h                | 5000 76C4h                | 5004 76C4h                |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 500C 6700h                | 5000 7700h                | 5004 7700h                |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 500C 6704h                | 5000 7704h                | 5004 7704h                |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 500C 6708h                | 5000 7708h                | 5004 7708h                |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>    | 500C 670Ch                | 5000 770Ch                | 5004 770Ch                |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>    | 500C 6710h                | 5000 7710h                | 5004 7710h                |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>    | 500C 6714h                | 5000 7714h                | 5004 7714h                |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>    | 500C 6718h                | 5000 7718h                | 5004 7718h                |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>    | 500C 671Ch                | 5000 771Ch                | 5004 771Ch                |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>   | 500C 6720h                | 5000 7720h                | 5004 7720h                |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a>  | 500C 6730h                | 5000 7730h                | 5004 7730h                |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a>  | 500C 6732h                | 5000 7732h                | 5004 7732h                |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>     | 500C 673Ah                | 5000 773Ah                | 5004 773Ah                |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>     | 500C 673Eh                | 5000 773Eh                | 5004 773Eh                |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a>  | 500C 6744h                | 5000 7744h                | 5004 7744h                |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>    | 500C 6780h                | 5000 7780h                | 5004 7780h                |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>    | 500C 6784h                | 5000 7784h                | 5004 7784h                |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>    | 500C 6788h                | 5000 7788h                | 5004 7788h                |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>    | 500C 678Ch                | 5000 778Ch                | 5004 778Ch                |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>    | 500C 6790h                | 5000 7790h                | 5004 7790h                |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>    | 500C 6794h                | 5000 7794h                | 5004 7794h                |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>    | 500C 6798h                | 5000 7798h                | 5004 7798h                |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>    | 500C 679Ch                | 5000 779Ch                | 5004 779Ch                |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>   | 500C 67A0h                | 5000 77A0h                | 5004 77A0h                |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a>  | 500C 67B0h                | 5000 77B0h                | 5004 77B0h                |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a>  | 500C 67B2h                | 5000 77B2h                | 5004 77B2h                |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>     | 500C 67BAh                | 5000 77BAh                | 5004 77BAh                |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>     | 500C 67BEh                | 5000 77BEh                | 5004 77BEh                |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a>  | 500C 67C4h                | 5000 77C4h                | 5004 77C4h                |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>          | 500C 6800h                | 5000 7800h                | 5004 7800h                |

**Table 3-780. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                   | EPWM5_G0 Physical Address | EPWM6_G0 Physical Address | EPWM7_G0 Physical Address |
|--------|--------|---------------------------------|---------------------------|---------------------------|---------------------------|
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>  | 500C 6804h                | 5000 7804h                | 5004 7804h                |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>   | 500C 6808h                | 5000 7808h                | 5004 7808h                |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>      | 500C 680Ch                | 5000 780Ch                | 5004 780Ch                |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>      | 500C 6810h                | 5000 7810h                | 5004 7810h                |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>      | 500C 6814h                | 5000 7814h                | 5004 7814h                |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>   | 500C 6820h                | 5000 7820h                | 5004 7820h                |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>   | 500C 6824h                | 5000 7824h                | 5004 7824h                |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>  | 500C 6828h                | 5000 7828h                | 5004 7828h                |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a> | 500C 682Ch                | 5000 782Ch                | 5004 782Ch                |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>  | 500C 6C00h                | 5000 7C00h                | 5004 7C00h                |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>   | 500C 6C04h                | 5000 7C04h                | 5004 7C04h                |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>    | 500C 6C20h                | 5000 7C20h                | 5004 7C20h                |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>    | 500C 6C24h                | 5000 7C24h                | 5004 7C24h                |

**Table 3-781. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM8_G0 Physical Address | EPWM9_G0 Physical Address | EPWM0_G1 Physical Address |
|--------|--------|------------------------------------|---------------------------|---------------------------|---------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5008 7000h                | 500C 7000h                | 5000 8000h                |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5008 7002h                | 500C 7002h                | 5000 8002h                |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5008 7006h                | 500C 7006h                | 5000 8006h                |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5008 7008h                | 500C 7008h                | 5000 8008h                |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5008 700Ah                | 500C 700Ah                | 5000 800Ah                |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 5008 700Ch                | 500C 700Ch                | 5000 800Ch                |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5008 700Eh                | 500C 700Eh                | 5000 800Eh                |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5008 7010h                | 500C 7010h                | 5000 8010h                |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5008 7012h                | 500C 7012h                | 5000 8012h                |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 5008 7018h                | 500C 7018h                | 5000 8018h                |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 5008 701Ah                | 500C 701Ah                | 5000 801Ah                |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 5008 7020h                | 500C 7020h                | 5000 8020h                |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 5008 7022h                | 500C 7022h                | 5000 8022h                |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 5008 7028h                | 500C 7028h                | 5000 8028h                |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 5008 7030h                | 500C 7030h                | 5000 8030h                |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 5008 7032h                | 500C 7032h                | 5000 8032h                |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 5008 7040h                | 500C 7040h                | 5000 8040h                |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 5008 704Eh                | 500C 704Eh                | 5000 804Eh                |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>        | 5008 705Ah                | 500C 705Ah                | 5000 805Ah                |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>         | 5008 705Ch                | 500C 705Ch                | 5000 805Ch                |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>        | 5008 7068h                | 500C 7068h                | 5000 8068h                |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>        | 5008 706Ah                | 500C 706Ah                | 5000 806Ah                |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>     | 5008 7070h                | 500C 7070h                | 5000 8070h                |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>    | 5008 7074h                | 500C 7074h                | 5000 8074h                |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>         | 5008 707Ah                | 500C 707Ah                | 5000 807Ah                |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>       | 5008 707Ch                | 500C 707Ch                | 5000 807Ch                |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>      | 5008 707Eh                | 500C 707Eh                | 5000 807Eh                |

**Table 3-781. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                     | EPWM8_G0 Physical Address | EPWM9_G0 Physical Address | EPWM0_G1 Physical Address |
|--------|--------|-----------------------------------|---------------------------|---------------------------|---------------------------|
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>       | 5008 7080h                | 500C 7080h                | 5000 8080h                |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>      | 5008 7082h                | 500C 7082h                | 5000 8082h                |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>       | 5008 7084h                | 500C 7084h                | 5000 8084h                |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>      | 5008 7086h                | 500C 7086h                | 5000 8086h                |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>       | 5008 708Eh                | 500C 708Eh                | 5000 808Eh                |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>      | 5008 7092h                | 500C 7092h                | 5000 8092h                |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>      | 5008 70A0h                | 500C 70A0h                | 5000 80A0h                |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>        | 5008 70A2h                | 500C 70A2h                | 5000 80A2h                |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>      | 5008 70A4h                | 500C 70A4h                | 5000 80A4h                |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>        | 5008 70A6h                | 500C 70A6h                | 5000 80A6h                |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>        | 5008 70C0h                | 500C 70C0h                | 5000 80C0h                |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>      | 5008 70C4h                | 500C 70C4h                | 5000 80C4h                |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>        | 5008 70C6h                | 500C 70C6h                | 5000 80C6h                |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>     | 5008 70C8h                | 500C 70C8h                | 5000 80C8h                |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>         | 5008 70D4h                | 500C 70D4h                | 5000 80D4h                |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>         | 5008 70D8h                | 500C 70D8h                | 5000 80D8h                |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>         | 5008 70DEh                | 500C 70DEh                | 5000 80DEh                |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>         | 5008 70E2h                | 500C 70E2h                | 5000 80E2h                |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>      | 5008 70E8h                | 500C 70E8h                | 5000 80E8h                |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>    | 5008 70EEh                | 500C 70EEh                | 5000 80EEh                |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>        | 5008 7100h                | 500C 7100h                | 5000 8100h                |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>       | 5008 7102h                | 500C 7102h                | 5000 8102h                |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>      | 5008 7104h                | 500C 7104h                | 5000 8104h                |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>        | 5008 7108h                | 500C 7108h                | 5000 8108h                |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>       | 5008 710Ah                | 500C 710Ah                | 5000 810Ah                |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>     | 5008 710Ch                | 500C 710Ch                | 5000 810Ch                |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>     | 5008 710Eh                | 500C 710Eh                | 5000 810Eh                |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>       | 5008 711Ah                | 500C 711Ah                | 5000 811Ah                |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>        | 5008 7126h                | 500C 7126h                | 5000 8126h                |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>     | 5008 7128h                | 500C 7128h                | 5000 8128h                |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>     | 5008 712Ah                | 500C 712Ah                | 5000 812Ah                |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>        | 5008 712Eh                | 500C 712Eh                | 5000 812Eh                |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>     | 5008 7130h                | 500C 7130h                | 5000 8130h                |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>     | 5008 7132h                | 500C 7132h                | 5000 8132h                |
| 136h   | 16     | <a href="#">EPWM_TZFRFC</a>       | 5008 7136h                | 500C 7136h                | 5000 8136h                |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a> | 5008 713Ah                | 500C 713Ah                | 5000 813Ah                |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>        | 5008 7148h                | 500C 7148h                | 5000 8148h                |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>         | 5008 714Ch                | 500C 714Ch                | 5000 814Ch                |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>        | 5008 7150h                | 500C 7150h                | 5000 8150h                |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>        | 5008 7154h                | 500C 7154h                | 5000 8154h                |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>        | 5008 7158h                | 500C 7158h                | 5000 8158h                |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>      | 5008 715Ch                | 500C 715Ch                | 5000 815Ch                |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>      | 5008 7160h                | 500C 7160h                | 5000 8160h                |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a> | 5008 7164h                | 500C 7164h                | 5000 8164h                |

**Table 3-781. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM8_G0 Physical Address | EPWM9_G0 Physical Address | EPWM0_G1 Physical Address |
|--------|--------|---------------------------------------|---------------------------|---------------------------|---------------------------|
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 5008 7168h                | 500C 7168h                | 5000 8168h                |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 5008 716Ch                | 500C 716Ch                | 5000 816Ch                |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 5008 7170h                | 500C 7170h                | 5000 8170h                |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 5008 7174h                | 500C 7174h                | 5000 8174h                |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 5008 7180h                | 500C 7180h                | 5000 8180h                |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 5008 7186h                | 500C 7186h                | 5000 8186h                |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5008 7188h                | 500C 7188h                | 5000 8188h                |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5008 718Eh                | 500C 718Eh                | 5000 818Eh                |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5008 7190h                | 500C 7190h                | 5000 8190h                |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5008 7192h                | 500C 7192h                | 5000 8192h                |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5008 7194h                | 500C 7194h                | 5000 8194h                |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5008 7196h                | 500C 7196h                | 5000 8196h                |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5008 7198h                | 500C 7198h                | 5000 8198h                |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5008 719Ah                | 500C 719Ah                | 5000 819Ah                |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5008 719Ch                | 500C 719Ch                | 5000 819Ch                |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5008 719Eh                | 500C 719Eh                | 5000 819Eh                |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5008 71A4h                | 500C 71A4h                | 5000 81A4h                |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5008 71A6h                | 500C 71A6h                | 5000 81A6h                |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 5008 71A8h                | 500C 71A8h                | 5000 81A8h                |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 5008 71AAh                | 500C 71AAh                | 5000 81AAh                |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 5008 71ACh                | 500C 71ACh                | 5000 81ACh                |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 5008 71AEh                | 500C 71AEh                | 5000 81AEh                |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 5008 71B0h                | 500C 71B0h                | 5000 81B0h                |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 5008 71B2h                | 500C 71B2h                | 5000 81B2h                |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 5008 71F4h                | 500C 71F4h                | 5000 81F4h                |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 5008 71FAh                | 500C 71FAh                | 5000 81FAh                |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 5008 71FCh                | 500C 71FCh                | 5000 81FCh                |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>         | 5008 7400h                | 500C 7400h                | 5000 8400h                |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>         | 5008 7410h                | 500C 7410h                | 5000 8410h                |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>            | 5008 7418h                | 500C 7418h                | 5000 8418h                |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a>   | 5008 741Ch                | 500C 741Ch                | 5000 841Ch                |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>     | 5008 7420h                | 500C 7420h                | 5000 8420h                |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>     | 5008 7428h                | 500C 7428h                | 5000 8428h                |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>     | 5008 7430h                | 500C 7430h                | 5000 8430h                |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>     | 5008 7600h                | 500C 7600h                | 5000 8600h                |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>     | 5008 7604h                | 500C 7604h                | 5000 8604h                |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>     | 5008 7608h                | 500C 7608h                | 5000 8608h                |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>     | 5008 760Ch                | 500C 760Ch                | 5000 860Ch                |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>     | 5008 7610h                | 500C 7610h                | 5000 8610h                |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>     | 5008 7614h                | 500C 7614h                | 5000 8614h                |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>     | 5008 7618h                | 500C 7618h                | 5000 8618h                |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>     | 5008 761Ch                | 500C 761Ch                | 5000 861Ch                |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>    | 5008 7620h                | 500C 7620h                | 5000 8620h                |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a>   | 5008 7630h                | 500C 7630h                | 5000 8630h                |

**Table 3-781. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM8_G0 Physical Address | EPWM9_G0 Physical Address | EPWM0_G1 Physical Address |
|--------|--------|-------------------------------------|---------------------------|---------------------------|---------------------------|
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 5008 7632h                | 500C 7632h                | 5000 8632h                |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 5008 7644h                | 500C 7644h                | 5000 8644h                |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 5008 7680h                | 500C 7680h                | 5000 8680h                |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 5008 7684h                | 500C 7684h                | 5000 8684h                |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 5008 7688h                | 500C 7688h                | 5000 8688h                |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 5008 768Ch                | 500C 768Ch                | 5000 868Ch                |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 5008 7690h                | 500C 7690h                | 5000 8690h                |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 5008 7694h                | 500C 7694h                | 5000 8694h                |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 5008 7698h                | 500C 7698h                | 5000 8698h                |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 5008 769Ch                | 500C 769Ch                | 5000 869Ch                |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 5008 76A0h                | 500C 76A0h                | 5000 86A0h                |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 5008 76B0h                | 500C 76B0h                | 5000 86B0h                |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 5008 76B2h                | 500C 76B2h                | 5000 86B2h                |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 5008 76BAh                | 500C 76BAh                | 5000 86BAh                |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 5008 76BEh                | 500C 76BEh                | 5000 86BEh                |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 5008 76C4h                | 500C 76C4h                | 5000 86C4h                |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 5008 7700h                | 500C 7700h                | 5000 8700h                |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 5008 7704h                | 500C 7704h                | 5000 8704h                |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 5008 7708h                | 500C 7708h                | 5000 8708h                |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>    | 5008 770Ch                | 500C 770Ch                | 5000 870Ch                |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>    | 5008 7710h                | 500C 7710h                | 5000 8710h                |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>    | 5008 7714h                | 500C 7714h                | 5000 8714h                |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>    | 5008 7718h                | 500C 7718h                | 5000 8718h                |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>    | 5008 771Ch                | 500C 771Ch                | 5000 871Ch                |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>   | 5008 7720h                | 500C 7720h                | 5000 8720h                |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a>  | 5008 7730h                | 500C 7730h                | 5000 8730h                |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a>  | 5008 7732h                | 500C 7732h                | 5000 8732h                |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>     | 5008 773Ah                | 500C 773Ah                | 5000 873Ah                |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>     | 5008 773Eh                | 500C 773Eh                | 5000 873Eh                |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a>  | 5008 7744h                | 500C 7744h                | 5000 8744h                |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>    | 5008 7780h                | 500C 7780h                | 5000 8780h                |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>    | 5008 7784h                | 500C 7784h                | 5000 8784h                |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>    | 5008 7788h                | 500C 7788h                | 5000 8788h                |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>    | 5008 778Ch                | 500C 778Ch                | 5000 878Ch                |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>    | 5008 7790h                | 500C 7790h                | 5000 8790h                |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>    | 5008 7794h                | 500C 7794h                | 5000 8794h                |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>    | 5008 7798h                | 500C 7798h                | 5000 8798h                |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>    | 5008 779Ch                | 500C 779Ch                | 5000 879Ch                |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>   | 5008 77A0h                | 500C 77A0h                | 5000 87A0h                |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a>  | 5008 77B0h                | 500C 77B0h                | 5000 87B0h                |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a>  | 5008 77B2h                | 500C 77B2h                | 5000 87B2h                |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>     | 5008 77BAh                | 500C 77BAh                | 5000 87BAh                |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>     | 5008 77BEh                | 500C 77BEh                | 5000 87BEh                |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a>  | 5008 77C4h                | 500C 77C4h                | 5000 87C4h                |



**Table 3-781. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                   | EPWM8_G0 Physical Address | EPWM9_G0 Physical Address | EPWM0_G1 Physical Address |
|--------|--------|---------------------------------|---------------------------|---------------------------|---------------------------|
| 800h   | 32     | <a href="#">EPWM_DECTL</a>      | 5008 7800h                | 500C 7800h                | 5000 8800h                |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>  | 5008 7804h                | 500C 7804h                | 5000 8804h                |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>   | 5008 7808h                | 500C 7808h                | 5000 8808h                |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>      | 5008 780Ch                | 500C 780Ch                | 5000 880Ch                |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>      | 5008 7810h                | 500C 7810h                | 5000 8810h                |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>      | 5008 7814h                | 500C 7814h                | 5000 8814h                |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>   | 5008 7820h                | 500C 7820h                | 5000 8820h                |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>   | 5008 7824h                | 500C 7824h                | 5000 8824h                |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>  | 5008 7828h                | 500C 7828h                | 5000 8828h                |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a> | 5008 782Ch                | 500C 782Ch                | 5000 882Ch                |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>  | 5008 7C00h                | 500C 7C00h                | 5000 8C00h                |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>   | 5008 7C04h                | 500C 7C04h                | 5000 8C04h                |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>    | 5008 7C20h                | 500C 7C20h                | 5000 8C20h                |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>    | 5008 7C24h                | 500C 7C24h                | 5000 8C24h                |

**Table 3-782. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM1_G1 Physical Address | EPWM10_G1 Physical Address | EPWM11_G1 Physical Address |
|--------|--------|------------------------------------|---------------------------|----------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5004 8000h                | 5008 8000h                 | 500C 8000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5004 8002h                | 5008 8002h                 | 500C 8002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5004 8006h                | 5008 8006h                 | 500C 8006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5004 8008h                | 5008 8008h                 | 500C 8008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5004 800Ah                | 5008 800Ah                 | 500C 800Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUEN</a>  | 5004 800Ch                | 5008 800Ch                 | 500C 800Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5004 800Eh                | 5008 800Eh                 | 500C 800Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5004 8010h                | 5008 8010h                 | 500C 8010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5004 8012h                | 5008 8012h                 | 500C 8012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 5004 8018h                | 5008 8018h                 | 500C 8018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 5004 801Ah                | 5008 801Ah                 | 500C 801Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 5004 8020h                | 5008 8020h                 | 500C 8020h                 |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 5004 8022h                | 5008 8022h                 | 500C 8022h                 |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 5004 8028h                | 5008 8028h                 | 500C 8028h                 |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 5004 8030h                | 5008 8030h                 | 500C 8030h                 |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 5004 8032h                | 5008 8032h                 | 500C 8032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 5004 8040h                | 5008 8040h                 | 500C 8040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 5004 804Eh                | 5008 804Eh                 | 500C 804Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>        | 5004 805Ah                | 5008 805Ah                 | 500C 805Ah                 |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>         | 5004 805Ch                | 5008 805Ch                 | 500C 805Ch                 |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>        | 5004 8068h                | 5008 8068h                 | 500C 8068h                 |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>        | 5004 806Ah                | 5008 806Ah                 | 500C 806Ah                 |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>     | 5004 8070h                | 5008 8070h                 | 500C 8070h                 |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>    | 5004 8074h                | 5008 8074h                 | 500C 8074h                 |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>         | 5004 807Ah                | 5008 807Ah                 | 500C 807Ah                 |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>       | 5004 807Ch                | 5008 807Ch                 | 500C 807Ch                 |



**Table 3-782. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                     | EPWM1_G1 Physical Address | EPWM10_G1 Physical Address | EPWM11_G1 Physical Address |
|--------|--------|-----------------------------------|---------------------------|----------------------------|----------------------------|
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>     | 5004 807Eh                | 5008 807Eh                 | 500C 807Eh                 |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>       | 5004 8080h                | 5008 8080h                 | 500C 8080h                 |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>      | 5004 8082h                | 5008 8082h                 | 500C 8082h                 |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>       | 5004 8084h                | 5008 8084h                 | 500C 8084h                 |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>      | 5004 8086h                | 5008 8086h                 | 500C 8086h                 |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>       | 5004 808Eh                | 5008 808Eh                 | 500C 808Eh                 |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>      | 5004 8092h                | 5008 8092h                 | 500C 8092h                 |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>      | 5004 80A0h                | 5008 80A0h                 | 500C 80A0h                 |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>        | 5004 80A2h                | 5008 80A2h                 | 500C 80A2h                 |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>      | 5004 80A4h                | 5008 80A4h                 | 500C 80A4h                 |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>        | 5004 80A6h                | 5008 80A6h                 | 500C 80A6h                 |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>        | 5004 80C0h                | 5008 80C0h                 | 500C 80C0h                 |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>      | 5004 80C4h                | 5008 80C4h                 | 500C 80C4h                 |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>        | 5004 80C6h                | 5008 80C6h                 | 500C 80C6h                 |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>     | 5004 80C8h                | 5008 80C8h                 | 500C 80C8h                 |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>         | 5004 80D4h                | 5008 80D4h                 | 500C 80D4h                 |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>         | 5004 80D8h                | 5008 80D8h                 | 500C 80D8h                 |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>         | 5004 80DEh                | 5008 80DEh                 | 500C 80DEh                 |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>         | 5004 80E2h                | 5008 80E2h                 | 500C 80E2h                 |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>      | 5004 80E8h                | 5008 80E8h                 | 500C 80E8h                 |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>    | 5004 80EEh                | 5008 80EEh                 | 500C 80EEh                 |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>        | 5004 8100h                | 5008 8100h                 | 500C 8100h                 |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>       | 5004 8102h                | 5008 8102h                 | 500C 8102h                 |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>      | 5004 8104h                | 5008 8104h                 | 500C 8104h                 |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>        | 5004 8108h                | 5008 8108h                 | 500C 8108h                 |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>       | 5004 810Ah                | 5008 810Ah                 | 500C 810Ah                 |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>     | 5004 810Ch                | 5008 810Ch                 | 500C 810Ch                 |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>     | 5004 810Eh                | 5008 810Eh                 | 500C 810Eh                 |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>       | 5004 811Ah                | 5008 811Ah                 | 500C 811Ah                 |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>        | 5004 8126h                | 5008 8126h                 | 500C 8126h                 |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>     | 5004 8128h                | 5008 8128h                 | 500C 8128h                 |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>     | 5004 812Ah                | 5008 812Ah                 | 500C 812Ah                 |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>        | 5004 812Eh                | 5008 812Eh                 | 500C 812Eh                 |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>     | 5004 8130h                | 5008 8130h                 | 500C 8130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>     | 5004 8132h                | 5008 8132h                 | 500C 8132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>        | 5004 8136h                | 5008 8136h                 | 500C 8136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a> | 5004 813Ah                | 5008 813Ah                 | 500C 813Ah                 |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>        | 5004 8148h                | 5008 8148h                 | 500C 8148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>         | 5004 814Ch                | 5008 814Ch                 | 500C 814Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>        | 5004 8150h                | 5008 8150h                 | 500C 8150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>        | 5004 8154h                | 5008 8154h                 | 500C 8154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>        | 5004 8158h                | 5008 8158h                 | 500C 8158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>      | 5004 815Ch                | 5008 815Ch                 | 500C 815Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>      | 5004 8160h                | 5008 8160h                 | 500C 8160h                 |

**Table 3-782. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM1_G1 Physical Address | EPWM10_G1 Physical Address | EPWM11_G1 Physical Address |
|--------|--------|---------------------------------------|---------------------------|----------------------------|----------------------------|
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 5004 8164h                | 5008 8164h                 | 500C 8164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 5004 8168h                | 5008 8168h                 | 500C 8168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 5004 816Ch                | 5008 816Ch                 | 500C 816Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 5004 8170h                | 5008 8170h                 | 500C 8170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 5004 8174h                | 5008 8174h                 | 500C 8174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 5004 8180h                | 5008 8180h                 | 500C 8180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 5004 8186h                | 5008 8186h                 | 500C 8186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5004 8188h                | 5008 8188h                 | 500C 8188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5004 818Eh                | 5008 818Eh                 | 500C 818Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5004 8190h                | 5008 8190h                 | 500C 8190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5004 8192h                | 5008 8192h                 | 500C 8192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5004 8194h                | 5008 8194h                 | 500C 8194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5004 8196h                | 5008 8196h                 | 500C 8196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5004 8198h                | 5008 8198h                 | 500C 8198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5004 819Ah                | 5008 819Ah                 | 500C 819Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5004 819Ch                | 5008 819Ch                 | 500C 819Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5004 819Eh                | 5008 819Eh                 | 500C 819Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5004 81A4h                | 5008 81A4h                 | 500C 81A4h                 |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5004 81A6h                | 5008 81A6h                 | 500C 81A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 5004 81A8h                | 5008 81A8h                 | 500C 81A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 5004 81AAh                | 5008 81AAh                 | 500C 81AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 5004 81ACh                | 5008 81ACh                 | 500C 81ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 5004 81AEh                | 5008 81AEh                 | 500C 81AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 5004 81B0h                | 5008 81B0h                 | 500C 81B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 5004 81B2h                | 5008 81B2h                 | 500C 81B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 5004 81F4h                | 5008 81F4h                 | 500C 81F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 5004 81FAh                | 5008 81FAh                 | 500C 81FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 5004 81FCh                | 5008 81FCh                 | 500C 81FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>         | 5004 8400h                | 5008 8400h                 | 500C 8400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>         | 5004 8410h                | 5008 8410h                 | 500C 8410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>            | 5004 8418h                | 5008 8418h                 | 500C 8418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a>   | 5004 841Ch                | 5008 841Ch                 | 500C 841Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>     | 5004 8420h                | 5008 8420h                 | 500C 8420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>     | 5004 8428h                | 5008 8428h                 | 500C 8428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>     | 5004 8430h                | 5008 8430h                 | 500C 8430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>     | 5004 8600h                | 5008 8600h                 | 500C 8600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>     | 5004 8604h                | 5008 8604h                 | 500C 8604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>     | 5004 8608h                | 5008 8608h                 | 500C 8608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>     | 5004 860Ch                | 5008 860Ch                 | 500C 860Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>     | 5004 8610h                | 5008 8610h                 | 500C 8610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>     | 5004 8614h                | 5008 8614h                 | 500C 8614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>     | 5004 8618h                | 5008 8618h                 | 500C 8618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>     | 5004 861Ch                | 5008 861Ch                 | 500C 861Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>    | 5004 8620h                | 5008 8620h                 | 500C 8620h                 |

**Table 3-782. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM1_G1 Physical Address | EPWM10_G1 Physical Address | EPWM11_G1 Physical Address |
|--------|--------|-------------------------------------|---------------------------|----------------------------|----------------------------|
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 5004 8630h                | 5008 8630h                 | 500C 8630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 5004 8632h                | 5008 8632h                 | 500C 8632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 5004 8644h                | 5008 8644h                 | 500C 8644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 5004 8680h                | 5008 8680h                 | 500C 8680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 5004 8684h                | 5008 8684h                 | 500C 8684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 5004 8688h                | 5008 8688h                 | 500C 8688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 5004 868Ch                | 5008 868Ch                 | 500C 868Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 5004 8690h                | 5008 8690h                 | 500C 8690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 5004 8694h                | 5008 8694h                 | 500C 8694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 5004 8698h                | 5008 8698h                 | 500C 8698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 5004 869Ch                | 5008 869Ch                 | 500C 869Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 5004 86A0h                | 5008 86A0h                 | 500C 86A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 5004 86B0h                | 5008 86B0h                 | 500C 86B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 5004 86B2h                | 5008 86B2h                 | 500C 86B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 5004 86BAh                | 5008 86BAh                 | 500C 86BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 5004 86BEh                | 5008 86BEh                 | 500C 86BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 5004 86C4h                | 5008 86C4h                 | 500C 86C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 5004 8700h                | 5008 8700h                 | 500C 8700h                 |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 5004 8704h                | 5008 8704h                 | 500C 8704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 5004 8708h                | 5008 8708h                 | 500C 8708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>    | 5004 870Ch                | 5008 870Ch                 | 500C 870Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>    | 5004 8710h                | 5008 8710h                 | 500C 8710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>    | 5004 8714h                | 5008 8714h                 | 500C 8714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>    | 5004 8718h                | 5008 8718h                 | 500C 8718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>    | 5004 871Ch                | 5008 871Ch                 | 500C 871Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>   | 5004 8720h                | 5008 8720h                 | 500C 8720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a>  | 5004 8730h                | 5008 8730h                 | 500C 8730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a>  | 5004 8732h                | 5008 8732h                 | 500C 8732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>     | 5004 873Ah                | 5008 873Ah                 | 500C 873Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>     | 5004 873Eh                | 5008 873Eh                 | 500C 873Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a>  | 5004 8744h                | 5008 8744h                 | 500C 8744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>    | 5004 8780h                | 5008 8780h                 | 500C 8780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>    | 5004 8784h                | 5008 8784h                 | 500C 8784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>    | 5004 8788h                | 5008 8788h                 | 500C 8788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>    | 5004 878Ch                | 5008 878Ch                 | 500C 878Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>    | 5004 8790h                | 5008 8790h                 | 500C 8790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>    | 5004 8794h                | 5008 8794h                 | 500C 8794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>    | 5004 8798h                | 5008 8798h                 | 500C 8798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>    | 5004 879Ch                | 5008 879Ch                 | 500C 879Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>   | 5004 87A0h                | 5008 87A0h                 | 500C 87A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a>  | 5004 87B0h                | 5008 87B0h                 | 500C 87B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a>  | 5004 87B2h                | 5008 87B2h                 | 500C 87B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>     | 5004 87BAh                | 5008 87BAh                 | 500C 87BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>     | 5004 87BEh                | 5008 87BEh                 | 500C 87BEh                 |

**Table 3-782. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM1_G1 Physical Address | EPWM10_G1 Physical Address | EPWM11_G1 Physical Address |
|--------|--------|------------------------------------|---------------------------|----------------------------|----------------------------|
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5004 87C4h                | 5008 87C4h                 | 500C 87C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5004 8800h                | 5008 8800h                 | 500C 8800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5004 8804h                | 5008 8804h                 | 500C 8804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5004 8808h                | 5008 8808h                 | 500C 8808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5004 880Ch                | 5008 880Ch                 | 500C 880Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 5004 8810h                | 5008 8810h                 | 500C 8810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5004 8814h                | 5008 8814h                 | 500C 8814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 5004 8820h                | 5008 8820h                 | 500C 8820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 5004 8824h                | 5008 8824h                 | 500C 8824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 5004 8828h                | 5008 8828h                 | 500C 8828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 5004 882Ch                | 5008 882Ch                 | 500C 882Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFG</a>      | 5004 8C00h                | 5008 8C00h                 | 500C 8C00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 5004 8C04h                | 5008 8C04h                 | 500C 8C04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 5004 8C20h                | 5008 8C20h                 | 500C 8C20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 5004 8C24h                | 5008 8C24h                 | 500C 8C24h                 |

**Table 3-783. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM12_G1 Physical Address | EPWM13_G1 Physical Address | EPWM14_G1 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5000 9000h                 | 5004 9000h                 | 5008 9000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5000 9002h                 | 5004 9002h                 | 5008 9002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5000 9006h                 | 5004 9006h                 | 5008 9006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5000 9008h                 | 5004 9008h                 | 5008 9008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5000 900Ah                 | 5004 900Ah                 | 5008 900Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNOUTEN</a>  | 5000 900Ch                 | 5004 900Ch                 | 5008 900Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5000 900Eh                 | 5004 900Eh                 | 5008 900Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5000 9010h                 | 5004 9010h                 | 5008 9010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5000 9012h                 | 5004 9012h                 | 5008 9012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 5000 9018h                 | 5004 9018h                 | 5008 9018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 5000 901Ah                 | 5004 901Ah                 | 5008 901Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 5000 9020h                 | 5004 9020h                 | 5008 9020h                 |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 5000 9022h                 | 5004 9022h                 | 5008 9022h                 |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 5000 9028h                 | 5004 9028h                 | 5008 9028h                 |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 5000 9030h                 | 5004 9030h                 | 5008 9030h                 |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 5000 9032h                 | 5004 9032h                 | 5008 9032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 5000 9040h                 | 5004 9040h                 | 5008 9040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 5000 904Eh                 | 5004 904Eh                 | 5008 904Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>        | 5000 905Ah                 | 5004 905Ah                 | 5008 905Ah                 |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>         | 5000 905Ch                 | 5004 905Ch                 | 5008 905Ch                 |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>        | 5000 9068h                 | 5004 9068h                 | 5008 9068h                 |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>        | 5000 906Ah                 | 5004 906Ah                 | 5008 906Ah                 |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>     | 5000 9070h                 | 5004 9070h                 | 5008 9070h                 |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>    | 5000 9074h                 | 5004 9074h                 | 5008 9074h                 |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>         | 5000 907Ah                 | 5004 907Ah                 | 5008 907Ah                 |

**Table 3-783. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                     | EPWM12_G1 Physical Address | EPWM13_G1 Physical Address | EPWM14_G1 Physical Address |
|--------|--------|-----------------------------------|----------------------------|----------------------------|----------------------------|
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>      | 5000 907Ch                 | 5004 907Ch                 | 5008 907Ch                 |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>     | 5000 907Eh                 | 5004 907Eh                 | 5008 907Eh                 |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>       | 5000 9080h                 | 5004 9080h                 | 5008 9080h                 |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>      | 5000 9082h                 | 5004 9082h                 | 5008 9082h                 |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>       | 5000 9084h                 | 5004 9084h                 | 5008 9084h                 |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>      | 5000 9086h                 | 5004 9086h                 | 5008 9086h                 |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>       | 5000 908Eh                 | 5004 908Eh                 | 5008 908Eh                 |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>      | 5000 9092h                 | 5004 9092h                 | 5008 9092h                 |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>      | 5000 90A0h                 | 5004 90A0h                 | 5008 90A0h                 |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>        | 5000 90A2h                 | 5004 90A2h                 | 5008 90A2h                 |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>      | 5000 90A4h                 | 5004 90A4h                 | 5008 90A4h                 |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>        | 5000 90A6h                 | 5004 90A6h                 | 5008 90A6h                 |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>        | 5000 90C0h                 | 5004 90C0h                 | 5008 90C0h                 |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>      | 5000 90C4h                 | 5004 90C4h                 | 5008 90C4h                 |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>        | 5000 90C6h                 | 5004 90C6h                 | 5008 90C6h                 |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>     | 5000 90C8h                 | 5004 90C8h                 | 5008 90C8h                 |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>         | 5000 90D4h                 | 5004 90D4h                 | 5008 90D4h                 |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>         | 5000 90D8h                 | 5004 90D8h                 | 5008 90D8h                 |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>         | 5000 90DEh                 | 5004 90DEh                 | 5008 90DEh                 |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>         | 5000 90E2h                 | 5004 90E2h                 | 5008 90E2h                 |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>      | 5000 90E8h                 | 5004 90E8h                 | 5008 90E8h                 |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>    | 5000 90EEh                 | 5004 90EEh                 | 5008 90EEh                 |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>        | 5000 9100h                 | 5004 9100h                 | 5008 9100h                 |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>       | 5000 9102h                 | 5004 9102h                 | 5008 9102h                 |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>      | 5000 9104h                 | 5004 9104h                 | 5008 9104h                 |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>        | 5000 9108h                 | 5004 9108h                 | 5008 9108h                 |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>       | 5000 910Ah                 | 5004 910Ah                 | 5008 910Ah                 |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>     | 5000 910Ch                 | 5004 910Ch                 | 5008 910Ch                 |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>     | 5000 910Eh                 | 5004 910Eh                 | 5008 910Eh                 |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>       | 5000 911Ah                 | 5004 911Ah                 | 5008 911Ah                 |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>        | 5000 9126h                 | 5004 9126h                 | 5008 9126h                 |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>     | 5000 9128h                 | 5004 9128h                 | 5008 9128h                 |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>     | 5000 912Ah                 | 5004 912Ah                 | 5008 912Ah                 |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>        | 5000 912Eh                 | 5004 912Eh                 | 5008 912Eh                 |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>     | 5000 9130h                 | 5004 9130h                 | 5008 9130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>     | 5000 9132h                 | 5004 9132h                 | 5008 9132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>        | 5000 9136h                 | 5004 9136h                 | 5008 9136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a> | 5000 913Ah                 | 5004 913Ah                 | 5008 913Ah                 |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>        | 5000 9148h                 | 5004 9148h                 | 5008 9148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>         | 5000 914Ch                 | 5004 914Ch                 | 5008 914Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>        | 5000 9150h                 | 5004 9150h                 | 5008 9150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>        | 5000 9154h                 | 5004 9154h                 | 5008 9154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>        | 5000 9158h                 | 5004 9158h                 | 5008 9158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>      | 5000 915Ch                 | 5004 915Ch                 | 5008 915Ch                 |

**Table 3-783. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM12_G1 Physical Address | EPWM13_G1 Physical Address | EPWM14_G1 Physical Address |
|--------|--------|---------------------------------------|----------------------------|----------------------------|----------------------------|
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 5000 9160h                 | 5004 9160h                 | 5008 9160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 5000 9164h                 | 5004 9164h                 | 5008 9164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 5000 9168h                 | 5004 9168h                 | 5008 9168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 5000 916Ch                 | 5004 916Ch                 | 5008 916Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 5000 9170h                 | 5004 9170h                 | 5008 9170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 5000 9174h                 | 5004 9174h                 | 5008 9174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 5000 9180h                 | 5004 9180h                 | 5008 9180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 5000 9186h                 | 5004 9186h                 | 5008 9186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5000 9188h                 | 5004 9188h                 | 5008 9188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5000 918Eh                 | 5004 918Eh                 | 5008 918Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5000 9190h                 | 5004 9190h                 | 5008 9190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5000 9192h                 | 5004 9192h                 | 5008 9192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5000 9194h                 | 5004 9194h                 | 5008 9194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5000 9196h                 | 5004 9196h                 | 5008 9196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5000 9198h                 | 5004 9198h                 | 5008 9198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5000 919Ah                 | 5004 919Ah                 | 5008 919Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5000 919Ch                 | 5004 919Ch                 | 5008 919Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5000 919Eh                 | 5004 919Eh                 | 5008 919Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5000 91A4h                 | 5004 91A4h                 | 5008 91A4h                 |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5000 91A6h                 | 5004 91A6h                 | 5008 91A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 5000 91A8h                 | 5004 91A8h                 | 5008 91A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 5000 91AAh                 | 5004 91AAh                 | 5008 91AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 5000 91ACh                 | 5004 91ACh                 | 5008 91ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 5000 91AEh                 | 5004 91AEh                 | 5008 91AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 5000 91B0h                 | 5004 91B0h                 | 5008 91B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 5000 91B2h                 | 5004 91B2h                 | 5008 91B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 5000 91F4h                 | 5004 91F4h                 | 5008 91F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 5000 91FAh                 | 5004 91FAh                 | 5008 91FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 5000 91FCh                 | 5004 91FCh                 | 5008 91FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>         | 5000 9400h                 | 5004 9400h                 | 5008 9400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>         | 5000 9410h                 | 5004 9410h                 | 5008 9410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>            | 5000 9418h                 | 5004 9418h                 | 5008 9418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a>   | 5000 941Ch                 | 5004 941Ch                 | 5008 941Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>     | 5000 9420h                 | 5004 9420h                 | 5008 9420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>     | 5000 9428h                 | 5004 9428h                 | 5008 9428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>     | 5000 9430h                 | 5004 9430h                 | 5008 9430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>     | 5000 9600h                 | 5004 9600h                 | 5008 9600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>     | 5000 9604h                 | 5004 9604h                 | 5008 9604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>     | 5000 9608h                 | 5004 9608h                 | 5008 9608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>     | 5000 960Ch                 | 5004 960Ch                 | 5008 960Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>     | 5000 9610h                 | 5004 9610h                 | 5008 9610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>     | 5000 9614h                 | 5004 9614h                 | 5008 9614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>     | 5000 9618h                 | 5004 9618h                 | 5008 9618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>     | 5000 961Ch                 | 5004 961Ch                 | 5008 961Ch                 |



**Table 3-783. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM12_G1 Physical Address | EPWM13_G1 Physical Address | EPWM14_G1 Physical Address |
|--------|--------|-------------------------------------|----------------------------|----------------------------|----------------------------|
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 5000 9620h                 | 5004 9620h                 | 5008 9620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 5000 9630h                 | 5004 9630h                 | 5008 9630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 5000 9632h                 | 5004 9632h                 | 5008 9632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 5000 9644h                 | 5004 9644h                 | 5008 9644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 5000 9680h                 | 5004 9680h                 | 5008 9680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 5000 9684h                 | 5004 9684h                 | 5008 9684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 5000 9688h                 | 5004 9688h                 | 5008 9688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 5000 968Ch                 | 5004 968Ch                 | 5008 968Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 5000 9690h                 | 5004 9690h                 | 5008 9690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 5000 9694h                 | 5004 9694h                 | 5008 9694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 5000 9698h                 | 5004 9698h                 | 5008 9698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 5000 969Ch                 | 5004 969Ch                 | 5008 969Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 5000 96A0h                 | 5004 96A0h                 | 5008 96A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 5000 96B0h                 | 5004 96B0h                 | 5008 96B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 5000 96B2h                 | 5004 96B2h                 | 5008 96B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 5000 96BAh                 | 5004 96BAh                 | 5008 96BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 5000 96BEh                 | 5004 96BEh                 | 5008 96BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 5000 96C4h                 | 5004 96C4h                 | 5008 96C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 5000 9700h                 | 5004 9700h                 | 5008 9700h                 |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 5000 9704h                 | 5004 9704h                 | 5008 9704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 5000 9708h                 | 5004 9708h                 | 5008 9708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>    | 5000 970Ch                 | 5004 970Ch                 | 5008 970Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>    | 5000 9710h                 | 5004 9710h                 | 5008 9710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>    | 5000 9714h                 | 5004 9714h                 | 5008 9714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>    | 5000 9718h                 | 5004 9718h                 | 5008 9718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>    | 5000 971Ch                 | 5004 971Ch                 | 5008 971Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>   | 5000 9720h                 | 5004 9720h                 | 5008 9720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a>  | 5000 9730h                 | 5004 9730h                 | 5008 9730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a>  | 5000 9732h                 | 5004 9732h                 | 5008 9732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>     | 5000 973Ah                 | 5004 973Ah                 | 5008 973Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>     | 5000 973Eh                 | 5004 973Eh                 | 5008 973Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a>  | 5000 9744h                 | 5004 9744h                 | 5008 9744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>    | 5000 9780h                 | 5004 9780h                 | 5008 9780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>    | 5000 9784h                 | 5004 9784h                 | 5008 9784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>    | 5000 9788h                 | 5004 9788h                 | 5008 9788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>    | 5000 978Ch                 | 5004 978Ch                 | 5008 978Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>    | 5000 9790h                 | 5004 9790h                 | 5008 9790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>    | 5000 9794h                 | 5004 9794h                 | 5008 9794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>    | 5000 9798h                 | 5004 9798h                 | 5008 9798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>    | 5000 979Ch                 | 5004 979Ch                 | 5008 979Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>   | 5000 97A0h                 | 5004 97A0h                 | 5008 97A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a>  | 5000 97B0h                 | 5004 97B0h                 | 5008 97B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a>  | 5000 97B2h                 | 5004 97B2h                 | 5008 97B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>     | 5000 97BAh                 | 5004 97BAh                 | 5008 97BAh                 |

**Table 3-783. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM12_G1 Physical Address | EPWM13_G1 Physical Address | EPWM14_G1 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5000 97BEh                 | 5004 97BEh                 | 5008 97BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5000 97C4h                 | 5004 97C4h                 | 5008 97C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5000 9800h                 | 5004 9800h                 | 5008 9800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5000 9804h                 | 5004 9804h                 | 5008 9804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5000 9808h                 | 5004 9808h                 | 5008 9808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5000 980Ch                 | 5004 980Ch                 | 5008 980Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 5000 9810h                 | 5004 9810h                 | 5008 9810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5000 9814h                 | 5004 9814h                 | 5008 9814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 5000 9820h                 | 5004 9820h                 | 5008 9820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 5000 9824h                 | 5004 9824h                 | 5008 9824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 5000 9828h                 | 5004 9828h                 | 5008 9828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 5000 982Ch                 | 5004 982Ch                 | 5008 982Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFG</a>      | 5000 9C00h                 | 5004 9C00h                 | 5008 9C00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 5000 9C04h                 | 5004 9C04h                 | 5008 9C04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 5000 9C20h                 | 5004 9C20h                 | 5008 9C20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 5000 9C24h                 | 5004 9C24h                 | 5008 9C24h                 |

**Table 3-784. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM15_G1 Physical Address | EPWM16_G1 Physical Address | EPWM17_G1 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 500C 9000h                 | 5000 A000h                 | 5004 A000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 500C 9002h                 | 5000 A002h                 | 5004 A002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 500C 9006h                 | 5000 A006h                 | 5004 A006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 500C 9008h                 | 5000 A008h                 | 5004 A008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 500C 900Ah                 | 5000 A00Ah                 | 5004 A00Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 500C 900Ch                 | 5000 A00Ch                 | 5004 A00Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 500C 900Eh                 | 5000 A00Eh                 | 5004 A00Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 500C 9010h                 | 5000 A010h                 | 5004 A010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 500C 9012h                 | 5000 A012h                 | 5004 A012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 500C 9018h                 | 5000 A018h                 | 5004 A018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 500C 901Ah                 | 5000 A01Ah                 | 5004 A01Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 500C 9020h                 | 5000 A020h                 | 5004 A020h                 |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 500C 9022h                 | 5000 A022h                 | 5004 A022h                 |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 500C 9028h                 | 5000 A028h                 | 5004 A028h                 |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 500C 9030h                 | 5000 A030h                 | 5004 A030h                 |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 500C 9032h                 | 5000 A032h                 | 5004 A032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 500C 9040h                 | 5000 A040h                 | 5004 A040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 500C 904Eh                 | 5000 A04Eh                 | 5004 A04Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>        | 500C 905Ah                 | 5000 A05Ah                 | 5004 A05Ah                 |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>         | 500C 905Ch                 | 5000 A05Ch                 | 5004 A05Ch                 |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>        | 500C 9068h                 | 5000 A068h                 | 5004 A068h                 |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>        | 500C 906Ah                 | 5000 A06Ah                 | 5004 A06Ah                 |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>     | 500C 9070h                 | 5000 A070h                 | 5004 A070h                 |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>    | 500C 9074h                 | 5000 A074h                 | 5004 A074h                 |



**Table 3-784. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                     | EPWM15_G1 Physical Address | EPWM16_G1 Physical Address | EPWM17_G1 Physical Address |
|--------|--------|-----------------------------------|----------------------------|----------------------------|----------------------------|
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>        | 500C 907Ah                 | 5000 A07Ah                 | 5004 A07Ah                 |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>      | 500C 907Ch                 | 5000 A07Ch                 | 5004 A07Ch                 |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>     | 500C 907Eh                 | 5000 A07Eh                 | 5004 A07Eh                 |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>       | 500C 9080h                 | 5000 A080h                 | 5004 A080h                 |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>      | 500C 9082h                 | 5000 A082h                 | 5004 A082h                 |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>       | 500C 9084h                 | 5000 A084h                 | 5004 A084h                 |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>      | 500C 9086h                 | 5000 A086h                 | 5004 A086h                 |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>       | 500C 908Eh                 | 5000 A08Eh                 | 5004 A08Eh                 |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>      | 500C 9092h                 | 5000 A092h                 | 5004 A092h                 |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>      | 500C 90A0h                 | 5000 A0A0h                 | 5004 A0A0h                 |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>        | 500C 90A2h                 | 5000 A0A2h                 | 5004 A0A2h                 |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>      | 500C 90A4h                 | 5000 A0A4h                 | 5004 A0A4h                 |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>        | 500C 90A6h                 | 5000 A0A6h                 | 5004 A0A6h                 |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>        | 500C 90C0h                 | 5000 A0C0h                 | 5004 A0C0h                 |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>      | 500C 90C4h                 | 5000 A0C4h                 | 5004 A0C4h                 |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>        | 500C 90C6h                 | 5000 A0C6h                 | 5004 A0C6h                 |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>     | 500C 90C8h                 | 5000 A0C8h                 | 5004 A0C8h                 |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>         | 500C 90D4h                 | 5000 A0D4h                 | 5004 A0D4h                 |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>         | 500C 90D8h                 | 5000 A0D8h                 | 5004 A0D8h                 |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>         | 500C 90DEh                 | 5000 A0DEh                 | 5004 A0DEh                 |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>         | 500C 90E2h                 | 5000 A0E2h                 | 5004 A0E2h                 |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>      | 500C 90E8h                 | 5000 A0E8h                 | 5004 A0E8h                 |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>    | 500C 90EEh                 | 5000 A0EEh                 | 5004 A0EEh                 |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>        | 500C 9100h                 | 5000 A100h                 | 5004 A100h                 |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>       | 500C 9102h                 | 5000 A102h                 | 5004 A102h                 |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>      | 500C 9104h                 | 5000 A104h                 | 5004 A104h                 |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>        | 500C 9108h                 | 5000 A108h                 | 5004 A108h                 |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>       | 500C 910Ah                 | 5000 A10Ah                 | 5004 A10Ah                 |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>     | 500C 910Ch                 | 5000 A10Ch                 | 5004 A10Ch                 |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>     | 500C 910Eh                 | 5000 A10Eh                 | 5004 A10Eh                 |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>       | 500C 911Ah                 | 5000 A11Ah                 | 5004 A11Ah                 |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>        | 500C 9126h                 | 5000 A126h                 | 5004 A126h                 |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>     | 500C 9128h                 | 5000 A128h                 | 5004 A128h                 |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>     | 500C 912Ah                 | 5000 A12Ah                 | 5004 A12Ah                 |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>        | 500C 912Eh                 | 5000 A12Eh                 | 5004 A12Eh                 |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>     | 500C 9130h                 | 5000 A130h                 | 5004 A130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>     | 500C 9132h                 | 5000 A132h                 | 5004 A132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>        | 500C 9136h                 | 5000 A136h                 | 5004 A136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a> | 500C 913Ah                 | 5000 A13Ah                 | 5004 A13Ah                 |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>        | 500C 9148h                 | 5000 A148h                 | 5004 A148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>         | 500C 914Ch                 | 5000 A14Ch                 | 5004 A14Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>        | 500C 9150h                 | 5000 A150h                 | 5004 A150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>        | 500C 9154h                 | 5000 A154h                 | 5004 A154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>        | 500C 9158h                 | 5000 A158h                 | 5004 A158h                 |

**Table 3-784. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM15_G1 Physical Address | EPWM16_G1 Physical Address | EPWM17_G1 Physical Address |
|--------|--------|---------------------------------------|----------------------------|----------------------------|----------------------------|
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 500C 915Ch                 | 5000 A15Ch                 | 5004 A15Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 500C 9160h                 | 5000 A160h                 | 5004 A160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 500C 9164h                 | 5000 A164h                 | 5004 A164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 500C 9168h                 | 5000 A168h                 | 5004 A168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 500C 916Ch                 | 5000 A16Ch                 | 5004 A16Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 500C 9170h                 | 5000 A170h                 | 5004 A170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 500C 9174h                 | 5000 A174h                 | 5004 A174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 500C 9180h                 | 5000 A180h                 | 5004 A180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 500C 9186h                 | 5000 A186h                 | 5004 A186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 500C 9188h                 | 5000 A188h                 | 5004 A188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 500C 918Eh                 | 5000 A18Eh                 | 5004 A18Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 500C 9190h                 | 5000 A190h                 | 5004 A190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 500C 9192h                 | 5000 A192h                 | 5004 A192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 500C 9194h                 | 5000 A194h                 | 5004 A194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 500C 9196h                 | 5000 A196h                 | 5004 A196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 500C 9198h                 | 5000 A198h                 | 5004 A198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 500C 919Ah                 | 5000 A19Ah                 | 5004 A19Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 500C 919Ch                 | 5000 A19Ch                 | 5004 A19Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 500C 919Eh                 | 5000 A19Eh                 | 5004 A19Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 500C 91A4h                 | 5000 A1A4h                 | 5004 A1A4h                 |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 500C 91A6h                 | 5000 A1A6h                 | 5004 A1A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 500C 91A8h                 | 5000 A1A8h                 | 5004 A1A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 500C 91AAh                 | 5000 A1AAh                 | 5004 A1AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 500C 91ACh                 | 5000 A1ACh                 | 5004 A1ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 500C 91AEh                 | 5000 A1AEh                 | 5004 A1AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 500C 91B0h                 | 5000 A1B0h                 | 5004 A1B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 500C 91B2h                 | 5000 A1B2h                 | 5004 A1B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 500C 91F4h                 | 5000 A1F4h                 | 5004 A1F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 500C 91FAh                 | 5000 A1FAh                 | 5004 A1FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 500C 91FCh                 | 5000 A1FCh                 | 5004 A1FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>         | 500C 9400h                 | 5000 A400h                 | 5004 A400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>         | 500C 9410h                 | 5000 A410h                 | 5004 A410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>            | 500C 9418h                 | 5000 A418h                 | 5004 A418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a>   | 500C 941Ch                 | 5000 A41Ch                 | 5004 A41Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>     | 500C 9420h                 | 5000 A420h                 | 5004 A420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>     | 500C 9428h                 | 5000 A428h                 | 5004 A428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>     | 500C 9430h                 | 5000 A430h                 | 5004 A430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>     | 500C 9600h                 | 5000 A600h                 | 5004 A600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>     | 500C 9604h                 | 5000 A604h                 | 5004 A604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>     | 500C 9608h                 | 5000 A608h                 | 5004 A608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>     | 500C 960Ch                 | 5000 A60Ch                 | 5004 A60Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>     | 500C 9610h                 | 5000 A610h                 | 5004 A610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>     | 500C 9614h                 | 5000 A614h                 | 5004 A614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>     | 500C 9618h                 | 5000 A618h                 | 5004 A618h                 |

**Table 3-784. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM15_G1 Physical Address | EPWM16_G1 Physical Address | EPWM17_G1 Physical Address |
|--------|--------|-------------------------------------|----------------------------|----------------------------|----------------------------|
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 500C 961Ch                 | 5000 A61Ch                 | 5004 A61Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 500C 9620h                 | 5000 A620h                 | 5004 A620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 500C 9630h                 | 5000 A630h                 | 5004 A630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 500C 9632h                 | 5000 A632h                 | 5004 A632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 500C 9644h                 | 5000 A644h                 | 5004 A644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 500C 9680h                 | 5000 A680h                 | 5004 A680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 500C 9684h                 | 5000 A684h                 | 5004 A684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 500C 9688h                 | 5000 A688h                 | 5004 A688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 500C 968Ch                 | 5000 A68Ch                 | 5004 A68Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 500C 9690h                 | 5000 A690h                 | 5004 A690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 500C 9694h                 | 5000 A694h                 | 5004 A694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 500C 9698h                 | 5000 A698h                 | 5004 A698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 500C 969Ch                 | 5000 A69Ch                 | 5004 A69Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 500C 96A0h                 | 5000 A6A0h                 | 5004 A6A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 500C 96B0h                 | 5000 A6B0h                 | 5004 A6B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 500C 96B2h                 | 5000 A6B2h                 | 5004 A6B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 500C 96BAh                 | 5000 A6BAh                 | 5004 A6BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 500C 96BEh                 | 5000 A6BEh                 | 5004 A6BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 500C 96C4h                 | 5000 A6C4h                 | 5004 A6C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 500C 9700h                 | 5000 A700h                 | 5004 A700h                 |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 500C 9704h                 | 5000 A704h                 | 5004 A704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 500C 9708h                 | 5000 A708h                 | 5004 A708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>    | 500C 970Ch                 | 5000 A70Ch                 | 5004 A70Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>    | 500C 9710h                 | 5000 A710h                 | 5004 A710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>    | 500C 9714h                 | 5000 A714h                 | 5004 A714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>    | 500C 9718h                 | 5000 A718h                 | 5004 A718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>    | 500C 971Ch                 | 5000 A71Ch                 | 5004 A71Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>   | 500C 9720h                 | 5000 A720h                 | 5004 A720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a>  | 500C 9730h                 | 5000 A730h                 | 5004 A730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a>  | 500C 9732h                 | 5000 A732h                 | 5004 A732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>     | 500C 973Ah                 | 5000 A73Ah                 | 5004 A73Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>     | 500C 973Eh                 | 5000 A73Eh                 | 5004 A73Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a>  | 500C 9744h                 | 5000 A744h                 | 5004 A744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>    | 500C 9780h                 | 5000 A780h                 | 5004 A780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>    | 500C 9784h                 | 5000 A784h                 | 5004 A784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>    | 500C 9788h                 | 5000 A788h                 | 5004 A788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>    | 500C 978Ch                 | 5000 A78Ch                 | 5004 A78Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>    | 500C 9790h                 | 5000 A790h                 | 5004 A790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>    | 500C 9794h                 | 5000 A794h                 | 5004 A794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>    | 500C 9798h                 | 5000 A798h                 | 5004 A798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>    | 500C 979Ch                 | 5000 A79Ch                 | 5004 A79Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>   | 500C 97A0h                 | 5000 A7A0h                 | 5004 A7A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a>  | 500C 97B0h                 | 5000 A7B0h                 | 5004 A7B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a>  | 500C 97B2h                 | 5000 A7B2h                 | 5004 A7B2h                 |

**Table 3-784. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM15_G1 Physical Address | EPWM16_G1 Physical Address | EPWM17_G1 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 500C 97BAh                 | 5000 A7BAh                 | 5004 A7BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 500C 97BEh                 | 5000 A7BEh                 | 5004 A7BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 500C 97C4h                 | 5000 A7C4h                 | 5004 A7C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 500C 9800h                 | 5000 A800h                 | 5004 A800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 500C 9804h                 | 5000 A804h                 | 5004 A804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 500C 9808h                 | 5000 A808h                 | 5004 A808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 500C 980Ch                 | 5000 A80Ch                 | 5004 A80Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 500C 9810h                 | 5000 A810h                 | 5004 A810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 500C 9814h                 | 5000 A814h                 | 5004 A814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 500C 9820h                 | 5000 A820h                 | 5004 A820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 500C 9824h                 | 5000 A824h                 | 5004 A824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 500C 9828h                 | 5000 A828h                 | 5004 A828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 500C 982Ch                 | 5000 A82Ch                 | 5004 A82Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFG</a>      | 500C 9C00h                 | 5000 AC00h                 | 5004 AC00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 500C 9C04h                 | 5000 AC04h                 | 5004 AC04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 500C 9C20h                 | 5000 AC20h                 | 5004 AC20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 500C 9C24h                 | 5000 AC24h                 | 5004 AC24h                 |

**Table 3-785. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM18_G1 Physical Address | EPWM19_G1 Physical Address | EPWM2_G1 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|---------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5008 A000h                 | 500C A000h                 | 5000 B000h                |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5008 A002h                 | 500C A002h                 | 5000 B002h                |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5008 A006h                 | 500C A006h                 | 5000 B006h                |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5008 A008h                 | 500C A008h                 | 5000 B008h                |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5008 A00Ah                 | 500C A00Ah                 | 5000 B00Ah                |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 5008 A00Ch                 | 500C A00Ch                 | 5000 B00Ch                |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5008 A00Eh                 | 500C A00Eh                 | 5000 B00Eh                |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5008 A010h                 | 500C A010h                 | 5000 B010h                |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5008 A012h                 | 500C A012h                 | 5000 B012h                |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 5008 A018h                 | 500C A018h                 | 5000 B018h                |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 5008 A01Ah                 | 500C A01Ah                 | 5000 B01Ah                |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 5008 A020h                 | 500C A020h                 | 5000 B020h                |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 5008 A022h                 | 500C A022h                 | 5000 B022h                |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 5008 A028h                 | 500C A028h                 | 5000 B028h                |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 5008 A030h                 | 500C A030h                 | 5000 B030h                |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 5008 A032h                 | 500C A032h                 | 5000 B032h                |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 5008 A040h                 | 500C A040h                 | 5000 B040h                |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 5008 A04Eh                 | 500C A04Eh                 | 5000 B04Eh                |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>        | 5008 A05Ah                 | 500C A05Ah                 | 5000 B05Ah                |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>         | 5008 A05Ch                 | 500C A05Ch                 | 5000 B05Ch                |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>        | 5008 A068h                 | 500C A068h                 | 5000 B068h                |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>        | 5008 A06Ah                 | 500C A06Ah                 | 5000 B06Ah                |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>     | 5008 A070h                 | 500C A070h                 | 5000 B070h                |

**Table 3-785. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                     | EPWM18_G1 Physical Address | EPWM19_G1 Physical Address | EPWM2_G1 Physical Address |
|--------|--------|-----------------------------------|----------------------------|----------------------------|---------------------------|
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>   | 5008 A074h                 | 500C A074h                 | 5000 B074h                |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>        | 5008 A07Ah                 | 500C A07Ah                 | 5000 B07Ah                |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>      | 5008 A07Ch                 | 500C A07Ch                 | 5000 B07Ch                |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>     | 5008 A07Eh                 | 500C A07Eh                 | 5000 B07Eh                |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>       | 5008 A080h                 | 500C A080h                 | 5000 B080h                |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>      | 5008 A082h                 | 500C A082h                 | 5000 B082h                |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>       | 5008 A084h                 | 500C A084h                 | 5000 B084h                |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>      | 5008 A086h                 | 500C A086h                 | 5000 B086h                |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>       | 5008 A08Eh                 | 500C A08Eh                 | 5000 B08Eh                |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>      | 5008 A092h                 | 500C A092h                 | 5000 B092h                |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>      | 5008 A0A0h                 | 500C A0A0h                 | 5000 B0A0h                |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>        | 5008 A0A2h                 | 500C A0A2h                 | 5000 B0A2h                |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>      | 5008 A0A4h                 | 500C A0A4h                 | 5000 B0A4h                |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>        | 5008 A0A6h                 | 500C A0A6h                 | 5000 B0A6h                |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>        | 5008 A0C0h                 | 500C A0C0h                 | 5000 B0C0h                |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>      | 5008 A0C4h                 | 500C A0C4h                 | 5000 B0C4h                |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>        | 5008 A0C6h                 | 500C A0C6h                 | 5000 B0C6h                |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>     | 5008 A0C8h                 | 500C A0C8h                 | 5000 B0C8h                |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>         | 5008 A0D4h                 | 500C A0D4h                 | 5000 B0D4h                |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>         | 5008 A0D8h                 | 500C A0D8h                 | 5000 B0D8h                |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>         | 5008 A0DEh                 | 500C A0DEh                 | 5000 B0DEh                |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>         | 5008 A0E2h                 | 500C A0E2h                 | 5000 B0E2h                |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>      | 5008 A0E8h                 | 500C A0E8h                 | 5000 B0E8h                |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>    | 5008 A0EEh                 | 500C A0EEh                 | 5000 B0EEh                |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>        | 5008 A100h                 | 500C A100h                 | 5000 B100h                |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>       | 5008 A102h                 | 500C A102h                 | 5000 B102h                |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>      | 5008 A104h                 | 500C A104h                 | 5000 B104h                |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>        | 5008 A108h                 | 500C A108h                 | 5000 B108h                |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>       | 5008 A10Ah                 | 500C A10Ah                 | 5000 B10Ah                |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>     | 5008 A10Ch                 | 500C A10Ch                 | 5000 B10Ch                |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLCB</a>      | 5008 A10Eh                 | 500C A10Eh                 | 5000 B10Eh                |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>       | 5008 A11Ah                 | 500C A11Ah                 | 5000 B11Ah                |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>        | 5008 A126h                 | 500C A126h                 | 5000 B126h                |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>     | 5008 A128h                 | 500C A128h                 | 5000 B128h                |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>     | 5008 A12Ah                 | 500C A12Ah                 | 5000 B12Ah                |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>        | 5008 A12Eh                 | 500C A12Eh                 | 5000 B12Eh                |
| 130h   | 16     | <a href="#">EPWM_TZCBCLR</a>      | 5008 A130h                 | 500C A130h                 | 5000 B130h                |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>     | 5008 A132h                 | 500C A132h                 | 5000 B132h                |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>        | 5008 A136h                 | 500C A136h                 | 5000 B136h                |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a> | 5008 A13Ah                 | 500C A13Ah                 | 5000 B13Ah                |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>        | 5008 A148h                 | 500C A148h                 | 5000 B148h                |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>         | 5008 A14Ch                 | 500C A14Ch                 | 5000 B14Ch                |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>        | 5008 A150h                 | 500C A150h                 | 5000 B150h                |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>        | 5008 A154h                 | 500C A154h                 | 5000 B154h                |

**Table 3-785. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM18_G1 Physical Address | EPWM19_G1 Physical Address | EPWM2_G1 Physical Address |
|--------|--------|---------------------------------------|----------------------------|----------------------------|---------------------------|
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 5008 A158h                 | 500C A158h                 | 5000 B158h                |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 5008 A15Ch                 | 500C A15Ch                 | 5000 B15Ch                |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 5008 A160h                 | 500C A160h                 | 5000 B160h                |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 5008 A164h                 | 500C A164h                 | 5000 B164h                |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 5008 A168h                 | 500C A168h                 | 5000 B168h                |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 5008 A16Ch                 | 500C A16Ch                 | 5000 B16Ch                |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 5008 A170h                 | 500C A170h                 | 5000 B170h                |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 5008 A174h                 | 500C A174h                 | 5000 B174h                |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 5008 A180h                 | 500C A180h                 | 5000 B180h                |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 5008 A186h                 | 500C A186h                 | 5000 B186h                |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5008 A188h                 | 500C A188h                 | 5000 B188h                |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5008 A18Eh                 | 500C A18Eh                 | 5000 B18Eh                |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5008 A190h                 | 500C A190h                 | 5000 B190h                |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5008 A192h                 | 500C A192h                 | 5000 B192h                |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5008 A194h                 | 500C A194h                 | 5000 B194h                |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5008 A196h                 | 500C A196h                 | 5000 B196h                |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5008 A198h                 | 500C A198h                 | 5000 B198h                |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5008 A19Ah                 | 500C A19Ah                 | 5000 B19Ah                |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5008 A19Ch                 | 500C A19Ch                 | 5000 B19Ch                |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5008 A19Eh                 | 500C A19Eh                 | 5000 B19Eh                |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5008 A1A4h                 | 500C A1A4h                 | 5000 B1A4h                |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5008 A1A6h                 | 500C A1A6h                 | 5000 B1A6h                |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 5008 A1A8h                 | 500C A1A8h                 | 5000 B1A8h                |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 5008 A1AAh                 | 500C A1AAh                 | 5000 B1AAh                |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 5008 A1ACh                 | 500C A1ACh                 | 5000 B1ACh                |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 5008 A1AEh                 | 500C A1AEh                 | 5000 B1AEh                |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 5008 A1B0h                 | 500C A1B0h                 | 5000 B1B0h                |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 5008 A1B2h                 | 500C A1B2h                 | 5000 B1B2h                |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 5008 A1F4h                 | 500C A1F4h                 | 5000 B1F4h                |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 5008 A1FAh                 | 500C A1FAh                 | 5000 B1FAh                |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 5008 A1FCh                 | 500C A1FCh                 | 5000 B1FCh                |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>         | 5008 A400h                 | 500C A400h                 | 5000 B400h                |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>         | 5008 A410h                 | 500C A410h                 | 5000 B410h                |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>            | 5008 A418h                 | 500C A418h                 | 5000 B418h                |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a>   | 5008 A41Ch                 | 500C A41Ch                 | 5000 B41Ch                |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>     | 5008 A420h                 | 500C A420h                 | 5000 B420h                |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>     | 5008 A428h                 | 500C A428h                 | 5000 B428h                |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>     | 5008 A430h                 | 500C A430h                 | 5000 B430h                |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>     | 5008 A600h                 | 500C A600h                 | 5000 B600h                |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>     | 5008 A604h                 | 500C A604h                 | 5000 B604h                |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>     | 5008 A608h                 | 500C A608h                 | 5000 B608h                |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>     | 5008 A60Ch                 | 500C A60Ch                 | 5000 B60Ch                |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>     | 5008 A610h                 | 500C A610h                 | 5000 B610h                |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>     | 5008 A614h                 | 500C A614h                 | 5000 B614h                |



**Table 3-785. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM18_G1 Physical Address | EPWM19_G1 Physical Address | EPWM2_G1 Physical Address |
|--------|--------|-------------------------------------|----------------------------|----------------------------|---------------------------|
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 5008 A618h                 | 500C A618h                 | 5000 B618h                |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 5008 A61Ch                 | 500C A61Ch                 | 5000 B61Ch                |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 5008 A620h                 | 500C A620h                 | 5000 B620h                |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 5008 A630h                 | 500C A630h                 | 5000 B630h                |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 5008 A632h                 | 500C A632h                 | 5000 B632h                |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 5008 A644h                 | 500C A644h                 | 5000 B644h                |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 5008 A680h                 | 500C A680h                 | 5000 B680h                |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 5008 A684h                 | 500C A684h                 | 5000 B684h                |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 5008 A688h                 | 500C A688h                 | 5000 B688h                |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 5008 A68Ch                 | 500C A68Ch                 | 5000 B68Ch                |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 5008 A690h                 | 500C A690h                 | 5000 B690h                |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 5008 A694h                 | 500C A694h                 | 5000 B694h                |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 5008 A698h                 | 500C A698h                 | 5000 B698h                |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 5008 A69Ch                 | 500C A69Ch                 | 5000 B69Ch                |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 5008 A6A0h                 | 500C A6A0h                 | 5000 B6A0h                |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 5008 A6B0h                 | 500C A6B0h                 | 5000 B6B0h                |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 5008 A6B2h                 | 500C A6B2h                 | 5000 B6B2h                |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 5008 A6BAh                 | 500C A6BAh                 | 5000 B6BAh                |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 5008 A6BEh                 | 500C A6BEh                 | 5000 B6BEh                |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 5008 A6C4h                 | 500C A6C4h                 | 5000 B6C4h                |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 5008 A700h                 | 500C A700h                 | 5000 B700h                |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 5008 A704h                 | 500C A704h                 | 5000 B704h                |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 5008 A708h                 | 500C A708h                 | 5000 B708h                |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>    | 5008 A70Ch                 | 500C A70Ch                 | 5000 B70Ch                |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>    | 5008 A710h                 | 500C A710h                 | 5000 B710h                |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>    | 5008 A714h                 | 500C A714h                 | 5000 B714h                |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>    | 5008 A718h                 | 500C A718h                 | 5000 B718h                |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>    | 5008 A71Ch                 | 500C A71Ch                 | 5000 B71Ch                |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>   | 5008 A720h                 | 500C A720h                 | 5000 B720h                |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a>  | 5008 A730h                 | 500C A730h                 | 5000 B730h                |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a>  | 5008 A732h                 | 500C A732h                 | 5000 B732h                |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>     | 5008 A73Ah                 | 500C A73Ah                 | 5000 B73Ah                |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>     | 5008 A73Eh                 | 500C A73Eh                 | 5000 B73Eh                |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a>  | 5008 A744h                 | 500C A744h                 | 5000 B744h                |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>    | 5008 A780h                 | 500C A780h                 | 5000 B780h                |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>    | 5008 A784h                 | 500C A784h                 | 5000 B784h                |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>    | 5008 A788h                 | 500C A788h                 | 5000 B788h                |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>    | 5008 A78Ch                 | 500C A78Ch                 | 5000 B78Ch                |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>    | 5008 A790h                 | 500C A790h                 | 5000 B790h                |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>    | 5008 A794h                 | 500C A794h                 | 5000 B794h                |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>    | 5008 A798h                 | 500C A798h                 | 5000 B798h                |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>    | 5008 A79Ch                 | 500C A79Ch                 | 5000 B79Ch                |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>   | 5008 A7A0h                 | 500C A7A0h                 | 5000 B7A0h                |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a>  | 5008 A7B0h                 | 500C A7B0h                 | 5000 B7B0h                |

**Table 3-785. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM18_G1 Physical Address | EPWM19_G1 Physical Address | EPWM2_G1 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|---------------------------|
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5008 A7B2h                 | 500C A7B2h                 | 5000 B7B2h                |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5008 A7BAh                 | 500C A7BAh                 | 5000 B7BAh                |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5008 A7BEh                 | 500C A7BEh                 | 5000 B7BEh                |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5008 A7C4h                 | 500C A7C4h                 | 5000 B7C4h                |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5008 A800h                 | 500C A800h                 | 5000 B800h                |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5008 A804h                 | 500C A804h                 | 5000 B804h                |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5008 A808h                 | 500C A808h                 | 5000 B808h                |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5008 A80Ch                 | 500C A80Ch                 | 5000 B80Ch                |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 5008 A810h                 | 500C A810h                 | 5000 B810h                |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5008 A814h                 | 500C A814h                 | 5000 B814h                |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 5008 A820h                 | 500C A820h                 | 5000 B820h                |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 5008 A824h                 | 500C A824h                 | 5000 B824h                |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 5008 A828h                 | 500C A828h                 | 5000 B828h                |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 5008 A82Ch                 | 500C A82Ch                 | 5000 B82Ch                |
| C00h   | 32     | <a href="#">EPWM_MINDBCFG</a>      | 5008 AC00h                 | 500C AC00h                 | 5000 BC00h                |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 5008 AC04h                 | 500C AC04h                 | 5000 BC04h                |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 5008 AC20h                 | 500C AC20h                 | 5000 BC20h                |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 5008 AC24h                 | 500C AC24h                 | 5000 BC24h                |

**Table 3-786. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM20_G1 Physical Address | EPWM21_G1 Physical Address | EPWM22_G1 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5004 B000h                 | 5008 B000h                 | 500C B000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5004 B002h                 | 5008 B002h                 | 500C B002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5004 B006h                 | 5008 B006h                 | 500C B006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5004 B008h                 | 5008 B008h                 | 500C B008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5004 B00Ah                 | 5008 B00Ah                 | 500C B00Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 5004 B00Ch                 | 5008 B00Ch                 | 500C B00Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5004 B00Eh                 | 5008 B00Eh                 | 500C B00Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5004 B010h                 | 5008 B010h                 | 500C B010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5004 B012h                 | 5008 B012h                 | 500C B012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 5004 B018h                 | 5008 B018h                 | 500C B018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 5004 B01Ah                 | 5008 B01Ah                 | 500C B01Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 5004 B020h                 | 5008 B020h                 | 500C B020h                 |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 5004 B022h                 | 5008 B022h                 | 500C B022h                 |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 5004 B028h                 | 5008 B028h                 | 500C B028h                 |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 5004 B030h                 | 5008 B030h                 | 500C B030h                 |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 5004 B032h                 | 5008 B032h                 | 500C B032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 5004 B040h                 | 5008 B040h                 | 500C B040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 5004 B04Eh                 | 5008 B04Eh                 | 500C B04Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>        | 5004 B05Ah                 | 5008 B05Ah                 | 500C B05Ah                 |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>         | 5004 B05Ch                 | 5008 B05Ch                 | 500C B05Ch                 |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>        | 5004 B068h                 | 5008 B068h                 | 500C B068h                 |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>        | 5004 B06Ah                 | 5008 B06Ah                 | 500C B06Ah                 |



**Table 3-786. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                     | EPWM20_G1 Physical Address | EPWM21_G1 Physical Address | EPWM22_G1 Physical Address |
|--------|--------|-----------------------------------|----------------------------|----------------------------|----------------------------|
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>    | 5004 B070h                 | 5008 B070h                 | 500C B070h                 |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>   | 5004 B074h                 | 5008 B074h                 | 500C B074h                 |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>        | 5004 B07Ah                 | 5008 B07Ah                 | 500C B07Ah                 |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>      | 5004 B07Ch                 | 5008 B07Ch                 | 500C B07Ch                 |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>     | 5004 B07Eh                 | 5008 B07Eh                 | 500C B07Eh                 |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>       | 5004 B080h                 | 5008 B080h                 | 500C B080h                 |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>      | 5004 B082h                 | 5008 B082h                 | 500C B082h                 |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>       | 5004 B084h                 | 5008 B084h                 | 500C B084h                 |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>      | 5004 B086h                 | 5008 B086h                 | 500C B086h                 |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>       | 5004 B08Eh                 | 5008 B08Eh                 | 500C B08Eh                 |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>      | 5004 B092h                 | 5008 B092h                 | 500C B092h                 |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>      | 5004 B0A0h                 | 5008 B0A0h                 | 500C B0A0h                 |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>        | 5004 B0A2h                 | 5008 B0A2h                 | 500C B0A2h                 |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>      | 5004 B0A4h                 | 5008 B0A4h                 | 500C B0A4h                 |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>        | 5004 B0A6h                 | 5008 B0A6h                 | 500C B0A6h                 |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>        | 5004 B0C0h                 | 5008 B0C0h                 | 500C B0C0h                 |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>      | 5004 B0C4h                 | 5008 B0C4h                 | 500C B0C4h                 |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>        | 5004 B0C6h                 | 5008 B0C6h                 | 500C B0C6h                 |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>     | 5004 B0C8h                 | 5008 B0C8h                 | 500C B0C8h                 |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>         | 5004 B0D4h                 | 5008 B0D4h                 | 500C B0D4h                 |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>         | 5004 B0D8h                 | 5008 B0D8h                 | 500C B0D8h                 |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>         | 5004 B0DEh                 | 5008 B0DEh                 | 500C B0DEh                 |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>         | 5004 B0E2h                 | 5008 B0E2h                 | 500C B0E2h                 |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>      | 5004 B0E8h                 | 5008 B0E8h                 | 500C B0E8h                 |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>    | 5004 B0EEh                 | 5008 B0EEh                 | 500C B0EEh                 |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>        | 5004 B100h                 | 5008 B100h                 | 500C B100h                 |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>       | 5004 B102h                 | 5008 B102h                 | 500C B102h                 |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>      | 5004 B104h                 | 5008 B104h                 | 500C B104h                 |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>        | 5004 B108h                 | 5008 B108h                 | 500C B108h                 |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>       | 5004 B10Ah                 | 5008 B10Ah                 | 500C B10Ah                 |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>     | 5004 B10Ch                 | 5008 B10Ch                 | 500C B10Ch                 |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>     | 5004 B10Eh                 | 5008 B10Eh                 | 500C B10Eh                 |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>       | 5004 B11Ah                 | 5008 B11Ah                 | 500C B11Ah                 |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>        | 5004 B126h                 | 5008 B126h                 | 500C B126h                 |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>     | 5004 B128h                 | 5008 B128h                 | 500C B128h                 |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>     | 5004 B12Ah                 | 5008 B12Ah                 | 500C B12Ah                 |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>        | 5004 B12Eh                 | 5008 B12Eh                 | 500C B12Eh                 |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>     | 5004 B130h                 | 5008 B130h                 | 500C B130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>     | 5004 B132h                 | 5008 B132h                 | 500C B132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>        | 5004 B136h                 | 5008 B136h                 | 500C B136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a> | 5004 B13Ah                 | 5008 B13Ah                 | 500C B13Ah                 |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>        | 5004 B148h                 | 5008 B148h                 | 500C B148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>         | 5004 B14Ch                 | 5008 B14Ch                 | 500C B14Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>        | 5004 B150h                 | 5008 B150h                 | 500C B150h                 |

**Table 3-786. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM20_G1 Physical Address | EPWM21_G1 Physical Address | EPWM22_G1 Physical Address |
|--------|--------|---------------------------------------|----------------------------|----------------------------|----------------------------|
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>            | 5004 B154h                 | 5008 B154h                 | 500C B154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 5004 B158h                 | 5008 B158h                 | 500C B158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 5004 B15Ch                 | 5008 B15Ch                 | 500C B15Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 5004 B160h                 | 5008 B160h                 | 500C B160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 5004 B164h                 | 5008 B164h                 | 500C B164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 5004 B168h                 | 5008 B168h                 | 500C B168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 5004 B16Ch                 | 5008 B16Ch                 | 500C B16Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 5004 B170h                 | 5008 B170h                 | 500C B170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 5004 B174h                 | 5008 B174h                 | 500C B174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 5004 B180h                 | 5008 B180h                 | 500C B180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 5004 B186h                 | 5008 B186h                 | 500C B186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5004 B188h                 | 5008 B188h                 | 500C B188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5004 B18Eh                 | 5008 B18Eh                 | 500C B18Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5004 B190h                 | 5008 B190h                 | 500C B190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5004 B192h                 | 5008 B192h                 | 500C B192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5004 B194h                 | 5008 B194h                 | 500C B194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5004 B196h                 | 5008 B196h                 | 500C B196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5004 B198h                 | 5008 B198h                 | 500C B198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5004 B19Ah                 | 5008 B19Ah                 | 500C B19Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5004 B19Ch                 | 5008 B19Ch                 | 500C B19Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5004 B19Eh                 | 5008 B19Eh                 | 500C B19Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5004 B1A4h                 | 5008 B1A4h                 | 500C B1A4h                 |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5004 B1A6h                 | 5008 B1A6h                 | 500C B1A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 5004 B1A8h                 | 5008 B1A8h                 | 500C B1A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 5004 B1AAh                 | 5008 B1AAh                 | 500C B1AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 5004 B1ACh                 | 5008 B1ACh                 | 500C B1ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 5004 B1AEh                 | 5008 B1AEh                 | 500C B1AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 5004 B1B0h                 | 5008 B1B0h                 | 500C B1B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 5004 B1B2h                 | 5008 B1B2h                 | 500C B1B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 5004 B1F4h                 | 5008 B1F4h                 | 500C B1F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 5004 B1FAh                 | 5008 B1FAh                 | 500C B1FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 5004 B1FCh                 | 5008 B1FCh                 | 500C B1FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>         | 5004 B400h                 | 5008 B400h                 | 500C B400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>         | 5004 B410h                 | 5008 B410h                 | 500C B410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>            | 5004 B418h                 | 5008 B418h                 | 500C B418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a>   | 5004 B41Ch                 | 5008 B41Ch                 | 500C B41Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>     | 5004 B420h                 | 5008 B420h                 | 500C B420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>     | 5004 B428h                 | 5008 B428h                 | 500C B428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>     | 5004 B430h                 | 5008 B430h                 | 500C B430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>     | 5004 B600h                 | 5008 B600h                 | 500C B600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>     | 5004 B604h                 | 5008 B604h                 | 500C B604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>     | 5004 B608h                 | 5008 B608h                 | 500C B608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>     | 5004 B60Ch                 | 5008 B60Ch                 | 500C B60Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>     | 5004 B610h                 | 5008 B610h                 | 500C B610h                 |

**Table 3-786. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM20_G1 Physical Address | EPWM21_G1 Physical Address | EPWM22_G1 Physical Address |
|--------|--------|-------------------------------------|----------------------------|----------------------------|----------------------------|
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 5004 B614h                 | 5008 B614h                 | 500C B614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 5004 B618h                 | 5008 B618h                 | 500C B618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 5004 B61Ch                 | 5008 B61Ch                 | 500C B61Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 5004 B620h                 | 5008 B620h                 | 500C B620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 5004 B630h                 | 5008 B630h                 | 500C B630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 5004 B632h                 | 5008 B632h                 | 500C B632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 5004 B644h                 | 5008 B644h                 | 500C B644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 5004 B680h                 | 5008 B680h                 | 500C B680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 5004 B684h                 | 5008 B684h                 | 500C B684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 5004 B688h                 | 5008 B688h                 | 500C B688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 5004 B68Ch                 | 5008 B68Ch                 | 500C B68Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 5004 B690h                 | 5008 B690h                 | 500C B690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 5004 B694h                 | 5008 B694h                 | 500C B694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 5004 B698h                 | 5008 B698h                 | 500C B698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 5004 B69Ch                 | 5008 B69Ch                 | 500C B69Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 5004 B6A0h                 | 5008 B6A0h                 | 500C B6A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 5004 B6B0h                 | 5008 B6B0h                 | 500C B6B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 5004 B6B2h                 | 5008 B6B2h                 | 500C B6B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 5004 B6BAh                 | 5008 B6BAh                 | 500C B6BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 5004 B6BEh                 | 5008 B6BEh                 | 500C B6BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 5004 B6C4h                 | 5008 B6C4h                 | 500C B6C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 5004 B700h                 | 5008 B700h                 | 500C B700h                 |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 5004 B704h                 | 5008 B704h                 | 500C B704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 5004 B708h                 | 5008 B708h                 | 500C B708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>    | 5004 B70Ch                 | 5008 B70Ch                 | 500C B70Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>    | 5004 B710h                 | 5008 B710h                 | 500C B710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>    | 5004 B714h                 | 5008 B714h                 | 500C B714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>    | 5004 B718h                 | 5008 B718h                 | 500C B718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>    | 5004 B71Ch                 | 5008 B71Ch                 | 500C B71Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>   | 5004 B720h                 | 5008 B720h                 | 500C B720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a>  | 5004 B730h                 | 5008 B730h                 | 500C B730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a>  | 5004 B732h                 | 5008 B732h                 | 500C B732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>     | 5004 B73Ah                 | 5008 B73Ah                 | 500C B73Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>     | 5004 B73Eh                 | 5008 B73Eh                 | 500C B73Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a>  | 5004 B744h                 | 5008 B744h                 | 500C B744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>    | 5004 B780h                 | 5008 B780h                 | 500C B780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>    | 5004 B784h                 | 5008 B784h                 | 500C B784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>    | 5004 B788h                 | 5008 B788h                 | 500C B788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>    | 5004 B78Ch                 | 5008 B78Ch                 | 500C B78Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>    | 5004 B790h                 | 5008 B790h                 | 500C B790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>    | 5004 B794h                 | 5008 B794h                 | 500C B794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>    | 5004 B798h                 | 5008 B798h                 | 500C B798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>    | 5004 B79Ch                 | 5008 B79Ch                 | 500C B79Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>   | 5004 B7A0h                 | 5008 B7A0h                 | 500C B7A0h                 |

**Table 3-786. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM20_G1 Physical Address | EPWM21_G1 Physical Address | EPWM22_G1 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5004 B7B0h                 | 5008 B7B0h                 | 500C B7B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5004 B7B2h                 | 5008 B7B2h                 | 500C B7B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5004 B7BAh                 | 5008 B7BAh                 | 500C B7BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5004 B7BEh                 | 5008 B7BEh                 | 500C B7BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5004 B7C4h                 | 5008 B7C4h                 | 500C B7C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5004 B800h                 | 5008 B800h                 | 500C B800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5004 B804h                 | 5008 B804h                 | 500C B804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5004 B808h                 | 5008 B808h                 | 500C B808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5004 B80Ch                 | 5008 B80Ch                 | 500C B80Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 5004 B810h                 | 5008 B810h                 | 500C B810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5004 B814h                 | 5008 B814h                 | 500C B814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 5004 B820h                 | 5008 B820h                 | 500C B820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 5004 B824h                 | 5008 B824h                 | 500C B824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 5004 B828h                 | 5008 B828h                 | 500C B828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 5004 B82Ch                 | 5008 B82Ch                 | 500C B82Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>     | 5004 BC00h                 | 5008 BC00h                 | 500C BC00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 5004 BC04h                 | 5008 BC04h                 | 500C BC04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 5004 BC20h                 | 5008 BC20h                 | 500C BC20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 5004 BC24h                 | 5008 BC24h                 | 500C BC24h                 |

**Table 3-787. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM23_G1 Physical Address | EPWM24_G1 Physical Address | EPWM25_G1 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5000 C000h                 | 5004 C000h                 | 5008 C000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5000 C002h                 | 5004 C002h                 | 5008 C002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5000 C006h                 | 5004 C006h                 | 5008 C006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5000 C008h                 | 5004 C008h                 | 5008 C008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5000 C00Ah                 | 5004 C00Ah                 | 5008 C00Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 5000 C00Ch                 | 5004 C00Ch                 | 5008 C00Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5000 C00Eh                 | 5004 C00Eh                 | 5008 C00Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5000 C010h                 | 5004 C010h                 | 5008 C010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5000 C012h                 | 5004 C012h                 | 5008 C012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 5000 C018h                 | 5004 C018h                 | 5008 C018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 5000 C01Ah                 | 5004 C01Ah                 | 5008 C01Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 5000 C020h                 | 5004 C020h                 | 5008 C020h                 |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 5000 C022h                 | 5004 C022h                 | 5008 C022h                 |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 5000 C028h                 | 5004 C028h                 | 5008 C028h                 |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 5000 C030h                 | 5004 C030h                 | 5008 C030h                 |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 5000 C032h                 | 5004 C032h                 | 5008 C032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 5000 C040h                 | 5004 C040h                 | 5008 C040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 5000 C04Eh                 | 5004 C04Eh                 | 5008 C04Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>        | 5000 C05Ah                 | 5004 C05Ah                 | 5008 C05Ah                 |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>         | 5000 C05Ch                 | 5004 C05Ch                 | 5008 C05Ch                 |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>        | 5000 C068h                 | 5004 C068h                 | 5008 C068h                 |

**Table 3-787. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                     | EPWM23_G1 Physical Address | EPWM24_G1 Physical Address | EPWM25_G1 Physical Address |
|--------|--------|-----------------------------------|----------------------------|----------------------------|----------------------------|
| 6Ah    | 16     | <a href="#">EPWM_GLD CFG</a>      | 5000 C06Ah                 | 5004 C06Ah                 | 5008 C06Ah                 |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>    | 5000 C070h                 | 5004 C070h                 | 5008 C070h                 |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>   | 5000 C074h                 | 5004 C074h                 | 5008 C074h                 |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>        | 5000 C07Ah                 | 5004 C07Ah                 | 5008 C07Ah                 |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>      | 5000 C07Ch                 | 5004 C07Ch                 | 5008 C07Ch                 |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>     | 5000 C07Eh                 | 5004 C07Eh                 | 5008 C07Eh                 |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>       | 5000 C080h                 | 5004 C080h                 | 5008 C080h                 |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>      | 5000 C082h                 | 5004 C082h                 | 5008 C082h                 |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>       | 5000 C084h                 | 5004 C084h                 | 5008 C084h                 |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>      | 5000 C086h                 | 5004 C086h                 | 5008 C086h                 |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>       | 5000 C08Eh                 | 5004 C08Eh                 | 5008 C08Eh                 |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>      | 5000 C092h                 | 5004 C092h                 | 5008 C092h                 |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>      | 5000 C0A0h                 | 5004 C0A0h                 | 5008 C0A0h                 |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>        | 5000 C0A2h                 | 5004 C0A2h                 | 5008 C0A2h                 |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>      | 5000 C0A4h                 | 5004 C0A4h                 | 5008 C0A4h                 |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>        | 5000 C0A6h                 | 5004 C0A6h                 | 5008 C0A6h                 |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>        | 5000 C0C0h                 | 5004 C0C0h                 | 5008 C0C0h                 |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>      | 5000 C0C4h                 | 5004 C0C4h                 | 5008 C0C4h                 |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>        | 5000 C0C6h                 | 5004 C0C6h                 | 5008 C0C6h                 |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>     | 5000 C0C8h                 | 5004 C0C8h                 | 5008 C0C8h                 |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>         | 5000 C0D4h                 | 5004 C0D4h                 | 5008 C0D4h                 |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>         | 5000 C0D8h                 | 5004 C0D8h                 | 5008 C0D8h                 |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>         | 5000 C0DEh                 | 5004 C0DEh                 | 5008 C0DEh                 |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>         | 5000 C0E2h                 | 5004 C0E2h                 | 5008 C0E2h                 |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>      | 5000 C0E8h                 | 5004 C0E8h                 | 5008 C0E8h                 |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>    | 5000 C0EEh                 | 5004 C0EEh                 | 5008 C0EEh                 |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>        | 5000 C100h                 | 5004 C100h                 | 5008 C100h                 |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>       | 5000 C102h                 | 5004 C102h                 | 5008 C102h                 |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>      | 5000 C104h                 | 5004 C104h                 | 5008 C104h                 |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>        | 5000 C108h                 | 5004 C108h                 | 5008 C108h                 |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>       | 5000 C10Ah                 | 5004 C10Ah                 | 5008 C10Ah                 |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>     | 5000 C10Ch                 | 5004 C10Ch                 | 5008 C10Ch                 |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>     | 5000 C10Eh                 | 5004 C10Eh                 | 5008 C10Eh                 |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>       | 5000 C11Ah                 | 5004 C11Ah                 | 5008 C11Ah                 |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>        | 5000 C126h                 | 5004 C126h                 | 5008 C126h                 |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>     | 5000 C128h                 | 5004 C128h                 | 5008 C128h                 |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>     | 5000 C12Ah                 | 5004 C12Ah                 | 5008 C12Ah                 |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>        | 5000 C12Eh                 | 5004 C12Eh                 | 5008 C12Eh                 |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>     | 5000 C130h                 | 5004 C130h                 | 5008 C130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>     | 5000 C132h                 | 5004 C132h                 | 5008 C132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>        | 5000 C136h                 | 5004 C136h                 | 5008 C136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a> | 5000 C13Ah                 | 5004 C13Ah                 | 5008 C13Ah                 |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>        | 5000 C148h                 | 5004 C148h                 | 5008 C148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>         | 5000 C14Ch                 | 5004 C14Ch                 | 5008 C14Ch                 |

**Table 3-787. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM23_G1 Physical Address | EPWM24_G1 Physical Address | EPWM25_G1 Physical Address |
|--------|--------|---------------------------------------|----------------------------|----------------------------|----------------------------|
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>            | 5000 C150h                 | 5004 C150h                 | 5008 C150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>            | 5000 C154h                 | 5004 C154h                 | 5008 C154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 5000 C158h                 | 5004 C158h                 | 5008 C158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 5000 C15Ch                 | 5004 C15Ch                 | 5008 C15Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 5000 C160h                 | 5004 C160h                 | 5008 C160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 5000 C164h                 | 5004 C164h                 | 5008 C164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 5000 C168h                 | 5004 C168h                 | 5008 C168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 5000 C16Ch                 | 5004 C16Ch                 | 5008 C16Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 5000 C170h                 | 5004 C170h                 | 5008 C170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 5000 C174h                 | 5004 C174h                 | 5008 C174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 5000 C180h                 | 5004 C180h                 | 5008 C180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 5000 C186h                 | 5004 C186h                 | 5008 C186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5000 C188h                 | 5004 C188h                 | 5008 C188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5000 C18Eh                 | 5004 C18Eh                 | 5008 C18Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5000 C190h                 | 5004 C190h                 | 5008 C190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5000 C192h                 | 5004 C192h                 | 5008 C192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5000 C194h                 | 5004 C194h                 | 5008 C194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5000 C196h                 | 5004 C196h                 | 5008 C196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5000 C198h                 | 5004 C198h                 | 5008 C198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5000 C19Ah                 | 5004 C19Ah                 | 5008 C19Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5000 C19Ch                 | 5004 C19Ch                 | 5008 C19Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5000 C19Eh                 | 5004 C19Eh                 | 5008 C19Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5000 C1A4h                 | 5004 C1A4h                 | 5008 C1A4h                 |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5000 C1A6h                 | 5004 C1A6h                 | 5008 C1A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 5000 C1A8h                 | 5004 C1A8h                 | 5008 C1A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 5000 C1AAh                 | 5004 C1AAh                 | 5008 C1AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 5000 C1ACh                 | 5004 C1ACh                 | 5008 C1ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 5000 C1AEh                 | 5004 C1AEh                 | 5008 C1AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 5000 C1B0h                 | 5004 C1B0h                 | 5008 C1B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 5000 C1B2h                 | 5004 C1B2h                 | 5008 C1B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 5000 C1F4h                 | 5004 C1F4h                 | 5008 C1F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 5000 C1FAh                 | 5004 C1FAh                 | 5008 C1FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 5000 C1FCh                 | 5004 C1FCh                 | 5008 C1FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>         | 5000 C400h                 | 5004 C400h                 | 5008 C400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>         | 5000 C410h                 | 5004 C410h                 | 5008 C410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>            | 5000 C418h                 | 5004 C418h                 | 5008 C418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a>   | 5000 C41Ch                 | 5004 C41Ch                 | 5008 C41Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>     | 5000 C420h                 | 5004 C420h                 | 5008 C420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>     | 5000 C428h                 | 5004 C428h                 | 5008 C428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>     | 5000 C430h                 | 5004 C430h                 | 5008 C430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>     | 5000 C600h                 | 5004 C600h                 | 5008 C600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>     | 5000 C604h                 | 5004 C604h                 | 5008 C604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>     | 5000 C608h                 | 5004 C608h                 | 5008 C608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>     | 5000 C60Ch                 | 5004 C60Ch                 | 5008 C60Ch                 |



**Table 3-787. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM23_G1 Physical Address | EPWM24_G1 Physical Address | EPWM25_G1 Physical Address |
|--------|--------|-------------------------------------|----------------------------|----------------------------|----------------------------|
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>   | 5000 C610h                 | 5004 C610h                 | 5008 C610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 5000 C614h                 | 5004 C614h                 | 5008 C614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 5000 C618h                 | 5004 C618h                 | 5008 C618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 5000 C61Ch                 | 5004 C61Ch                 | 5008 C61Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 5000 C620h                 | 5004 C620h                 | 5008 C620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 5000 C630h                 | 5004 C630h                 | 5008 C630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 5000 C632h                 | 5004 C632h                 | 5008 C632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 5000 C644h                 | 5004 C644h                 | 5008 C644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 5000 C680h                 | 5004 C680h                 | 5008 C680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 5000 C684h                 | 5004 C684h                 | 5008 C684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 5000 C688h                 | 5004 C688h                 | 5008 C688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 5000 C68Ch                 | 5004 C68Ch                 | 5008 C68Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 5000 C690h                 | 5004 C690h                 | 5008 C690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 5000 C694h                 | 5004 C694h                 | 5008 C694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 5000 C698h                 | 5004 C698h                 | 5008 C698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 5000 C69Ch                 | 5004 C69Ch                 | 5008 C69Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 5000 C6A0h                 | 5004 C6A0h                 | 5008 C6A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 5000 C6B0h                 | 5004 C6B0h                 | 5008 C6B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 5000 C6B2h                 | 5004 C6B2h                 | 5008 C6B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 5000 C6BAh                 | 5004 C6BAh                 | 5008 C6BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 5000 C6BEh                 | 5004 C6BEh                 | 5008 C6BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 5000 C6C4h                 | 5004 C6C4h                 | 5008 C6C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 5000 C700h                 | 5004 C700h                 | 5008 C700h                 |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 5000 C704h                 | 5004 C704h                 | 5008 C704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 5000 C708h                 | 5004 C708h                 | 5008 C708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>    | 5000 C70Ch                 | 5004 C70Ch                 | 5008 C70Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>    | 5000 C710h                 | 5004 C710h                 | 5008 C710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>    | 5000 C714h                 | 5004 C714h                 | 5008 C714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>    | 5000 C718h                 | 5004 C718h                 | 5008 C718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>    | 5000 C71Ch                 | 5004 C71Ch                 | 5008 C71Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>   | 5000 C720h                 | 5004 C720h                 | 5008 C720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a>  | 5000 C730h                 | 5004 C730h                 | 5008 C730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a>  | 5000 C732h                 | 5004 C732h                 | 5008 C732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>     | 5000 C73Ah                 | 5004 C73Ah                 | 5008 C73Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>     | 5000 C73Eh                 | 5004 C73Eh                 | 5008 C73Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a>  | 5000 C744h                 | 5004 C744h                 | 5008 C744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>    | 5000 C780h                 | 5004 C780h                 | 5008 C780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>    | 5000 C784h                 | 5004 C784h                 | 5008 C784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>    | 5000 C788h                 | 5004 C788h                 | 5008 C788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>    | 5000 C78Ch                 | 5004 C78Ch                 | 5008 C78Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>    | 5000 C790h                 | 5004 C790h                 | 5008 C790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>    | 5000 C794h                 | 5004 C794h                 | 5008 C794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>    | 5000 C798h                 | 5004 C798h                 | 5008 C798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>    | 5000 C79Ch                 | 5004 C79Ch                 | 5008 C79Ch                 |

**Table 3-787. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM23_G1 Physical Address | EPWM24_G1 Physical Address | EPWM25_G1 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 5000 C7A0h                 | 5004 C7A0h                 | 5008 C7A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5000 C7B0h                 | 5004 C7B0h                 | 5008 C7B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5000 C7B2h                 | 5004 C7B2h                 | 5008 C7B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5000 C7BAh                 | 5004 C7BAh                 | 5008 C7BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5000 C7BEh                 | 5004 C7BEh                 | 5008 C7BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5000 C7C4h                 | 5004 C7C4h                 | 5008 C7C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5000 C800h                 | 5004 C800h                 | 5008 C800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5000 C804h                 | 5004 C804h                 | 5008 C804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5000 C808h                 | 5004 C808h                 | 5008 C808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5000 C80Ch                 | 5004 C80Ch                 | 5008 C80Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 5000 C810h                 | 5004 C810h                 | 5008 C810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5000 C814h                 | 5004 C814h                 | 5008 C814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 5000 C820h                 | 5004 C820h                 | 5008 C820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 5000 C824h                 | 5004 C824h                 | 5008 C824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 5000 C828h                 | 5004 C828h                 | 5008 C828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 5000 C82Ch                 | 5004 C82Ch                 | 5008 C82Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>     | 5000 CC00h                 | 5004 CC00h                 | 5008 CC00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 5000 CC04h                 | 5004 CC04h                 | 5008 CC04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 5000 CC20h                 | 5004 CC20h                 | 5008 CC20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 5000 CC24h                 | 5004 CC24h                 | 5008 CC24h                 |

**Table 3-788. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM26_G1 Physical Address | EPWM27_G1 Physical Address | EPWM28_G1 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 500C C000h                 | 5000 D000h                 | 5004 D000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 500C C002h                 | 5000 D002h                 | 5004 D002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 500C C006h                 | 5000 D006h                 | 5004 D006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 500C C008h                 | 5000 D008h                 | 5004 D008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 500C C00Ah                 | 5000 D00Ah                 | 5004 D00Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUEN</a>  | 500C C00Ch                 | 5000 D00Ch                 | 5004 D00Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 500C C00Eh                 | 5000 D00Eh                 | 5004 D00Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 500C C010h                 | 5000 D010h                 | 5004 D010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 500C C012h                 | 5000 D012h                 | 5004 D012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 500C C018h                 | 5000 D018h                 | 5004 D018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 500C C01Ah                 | 5000 D01Ah                 | 5004 D01Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 500C C020h                 | 5000 D020h                 | 5004 D020h                 |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 500C C022h                 | 5000 D022h                 | 5004 D022h                 |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 500C C028h                 | 5000 D028h                 | 5004 D028h                 |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 500C C030h                 | 5000 D030h                 | 5004 D030h                 |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 500C C032h                 | 5000 D032h                 | 5004 D032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 500C C040h                 | 5000 D040h                 | 5004 D040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 500C C04Eh                 | 5000 D04Eh                 | 5004 D04Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>        | 500C C05Ah                 | 5000 D05Ah                 | 5004 D05Ah                 |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>         | 500C C05Ch                 | 5000 D05Ch                 | 5004 D05Ch                 |



**Table 3-788. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name     | EPWM26_G1 Physical Address | EPWM27_G1 Physical Address | EPWM28_G1 Physical Address |
|--------|--------|-------------------|----------------------------|----------------------------|----------------------------|
| 68h    | 16     | EPWM_GLDCTL       | 500C C068h                 | 5000 D068h                 | 5004 D068h                 |
| 6Ah    | 16     | EPWM_GLDCFG       | 500C C06Ah                 | 5000 D06Ah                 | 5004 D06Ah                 |
| 70h    | 32     | EPWM_EPWMXLINK    | 500C C070h                 | 5000 D070h                 | 5004 D070h                 |
| 74h    | 32     | EPWM_EPWMXLINK2   | 500C C074h                 | 5000 D074h                 | 5004 D074h                 |
| 7Ah    | 16     | EPWM_ETEST        | 500C C07Ah                 | 5000 D07Ah                 | 5004 D07Ah                 |
| 7Ch    | 16     | EPWM_EPWMREV      | 500C C07Ch                 | 5000 D07Ch                 | 5004 D07Ch                 |
| 7Eh    | 16     | EPWM_HRPWMREV     | 500C C07Eh                 | 5000 D07Eh                 | 5004 D07Eh                 |
| 80h    | 16     | EPWM_AQCTLA       | 500C C080h                 | 5000 D080h                 | 5004 D080h                 |
| 82h    | 16     | EPWM_AQCTLA2      | 500C C082h                 | 5000 D082h                 | 5004 D082h                 |
| 84h    | 16     | EPWM_AQCTLB       | 500C C084h                 | 5000 D084h                 | 5004 D084h                 |
| 86h    | 16     | EPWM_AQCTLB2      | 500C C086h                 | 5000 D086h                 | 5004 D086h                 |
| 8Eh    | 16     | EPWM_AQSFRC       | 500C C08Eh                 | 5000 D08Eh                 | 5004 D08Eh                 |
| 92h    | 16     | EPWM_AQCSFRC      | 500C C092h                 | 5000 D092h                 | 5004 D092h                 |
| A0h    | 16     | EPWM_DBREDHR      | 500C C0A0h                 | 5000 D0A0h                 | 5004 D0A0h                 |
| A2h    | 16     | EPWM_DBRED        | 500C C0A2h                 | 5000 D0A2h                 | 5004 D0A2h                 |
| A4h    | 16     | EPWM_DBFEDHR      | 500C C0A4h                 | 5000 D0A4h                 | 5004 D0A4h                 |
| A6h    | 16     | EPWM_DBFED        | 500C C0A6h                 | 5000 D0A6h                 | 5004 D0A6h                 |
| C0h    | 32     | EPWM_TBPHS        | 500C C0C0h                 | 5000 D0C0h                 | 5004 D0C0h                 |
| C4h    | 16     | EPWM_TBPRDHR      | 500C C0C4h                 | 5000 D0C4h                 | 5004 D0C4h                 |
| C6h    | 16     | EPWM_TBPRD        | 500C C0C6h                 | 5000 D0C6h                 | 5004 D0C6h                 |
| C8h    | 16     | EPWM_TBPRDHRB     | 500C C0C8h                 | 5000 D0C8h                 | 5004 D0C8h                 |
| D4h    | 32     | EPWM_CMPA         | 500C C0D4h                 | 5000 D0D4h                 | 5004 D0D4h                 |
| D8h    | 32     | EPWM_CMPB         | 500C C0D8h                 | 5000 D0D8h                 | 5004 D0D8h                 |
| DEh    | 16     | EPWM_CMPC         | 500C C0DEh                 | 5000 D0DEh                 | 5004 D0DEh                 |
| E2h    | 16     | EPWM_CMPD         | 500C C0E2h                 | 5000 D0E2h                 | 5004 D0E2h                 |
| E8h    | 16     | EPWM_GLDCTL2      | 500C C0E8h                 | 5000 D0E8h                 | 5004 D0E8h                 |
| EEh    | 16     | EPWM_SWVDELVAL    | 500C C0EEh                 | 5000 D0EEh                 | 5004 D0EEh                 |
| 100h   | 16     | EPWM_TZSEL        | 500C C100h                 | 5000 D100h                 | 5004 D100h                 |
| 102h   | 16     | EPWM_TZSEL2       | 500C C102h                 | 5000 D102h                 | 5004 D102h                 |
| 104h   | 16     | EPWM_TZDCSEL      | 500C C104h                 | 5000 D104h                 | 5004 D104h                 |
| 108h   | 16     | EPWM_TZCTL        | 500C C108h                 | 5000 D108h                 | 5004 D108h                 |
| 10Ah   | 16     | EPWM_TZCTL2       | 500C C10Ah                 | 5000 D10Ah                 | 5004 D10Ah                 |
| 10Ch   | 16     | EPWM_TZCTLDCA     | 500C C10Ch                 | 5000 D10Ch                 | 5004 D10Ch                 |
| 10Eh   | 16     | EPWM_TZCTLDCB     | 500C C10Eh                 | 5000 D10Eh                 | 5004 D10Eh                 |
| 11Ah   | 16     | EPWM_TZEINT       | 500C C11Ah                 | 5000 D11Ah                 | 5004 D11Ah                 |
| 126h   | 16     | EPWM_TZFLG        | 500C C126h                 | 5000 D126h                 | 5004 D126h                 |
| 128h   | 16     | EPWM_TZCBCFLG     | 500C C128h                 | 5000 D128h                 | 5004 D128h                 |
| 12Ah   | 16     | EPWM_TZOSTFLG     | 500C C12Ah                 | 5000 D12Ah                 | 5004 D12Ah                 |
| 12Eh   | 16     | EPWM_TZCLR        | 500C C12Eh                 | 5000 D12Eh                 | 5004 D12Eh                 |
| 130h   | 16     | EPWM_TZCBCCLR     | 500C C130h                 | 5000 D130h                 | 5004 D130h                 |
| 132h   | 16     | EPWM_TZOSTCLR     | 500C C132h                 | 5000 D132h                 | 5004 D132h                 |
| 136h   | 16     | EPWM_TZFRC        | 500C C136h                 | 5000 D136h                 | 5004 D136h                 |
| 13Ah   | 16     | EPWM_TZTRIPOUTSEL | 500C C13Ah                 | 5000 D13Ah                 | 5004 D13Ah                 |
| 148h   | 16     | EPWM_ETSEL        | 500C C148h                 | 5000 D148h                 | 5004 D148h                 |

**Table 3-788. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM26_G1 Physical Address | EPWM27_G1 Physical Address | EPWM28_G1 Physical Address |
|--------|--------|---------------------------------------|----------------------------|----------------------------|----------------------------|
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>             | 500C C14Ch                 | 5000 D14Ch                 | 5004 D14Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>            | 500C C150h                 | 5000 D150h                 | 5004 D150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>            | 500C C154h                 | 5000 D154h                 | 5004 D154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 500C C158h                 | 5000 D158h                 | 5004 D158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 500C C15Ch                 | 5000 D15Ch                 | 5004 D15Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 500C C160h                 | 5000 D160h                 | 5004 D160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 500C C164h                 | 5000 D164h                 | 5004 D164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 500C C168h                 | 5000 D168h                 | 5004 D168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 500C C16Ch                 | 5000 D16Ch                 | 5004 D16Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 500C C170h                 | 5000 D170h                 | 5004 D170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 500C C174h                 | 5000 D174h                 | 5004 D174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 500C C180h                 | 5000 D180h                 | 5004 D180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 500C C186h                 | 5000 D186h                 | 5004 D186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 500C C188h                 | 5000 D188h                 | 5004 D188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 500C C18Eh                 | 5000 D18Eh                 | 5004 D18Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 500C C190h                 | 5000 D190h                 | 5004 D190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 500C C192h                 | 5000 D192h                 | 5004 D192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 500C C194h                 | 5000 D194h                 | 5004 D194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 500C C196h                 | 5000 D196h                 | 5004 D196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 500C C198h                 | 5000 D198h                 | 5004 D198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 500C C19Ah                 | 5000 D19Ah                 | 5004 D19Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 500C C19Ch                 | 5000 D19Ch                 | 5004 D19Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 500C C19Eh                 | 5000 D19Eh                 | 5004 D19Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 500C C1A4h                 | 5000 D1A4h                 | 5004 D1A4h                 |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 500C C1A6h                 | 5000 D1A6h                 | 5004 D1A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 500C C1A8h                 | 5000 D1A8h                 | 5004 D1A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 500C C1AAh                 | 5000 D1AAh                 | 5004 D1AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 500C C1ACh                 | 5000 D1ACh                 | 5004 D1ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 500C C1AEh                 | 5000 D1AEh                 | 5004 D1AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 500C C1B0h                 | 5000 D1B0h                 | 5004 D1B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 500C C1B2h                 | 5000 D1B2h                 | 5004 D1B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 500C C1F4h                 | 5000 D1F4h                 | 5004 D1F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 500C C1FAh                 | 5000 D1FAh                 | 5004 D1FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 500C C1FCh                 | 5000 D1FCh                 | 5004 D1FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>         | 500C C400h                 | 5000 D400h                 | 5004 D400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>         | 500C C410h                 | 5000 D410h                 | 5004 D410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>            | 500C C418h                 | 5000 D418h                 | 5004 D418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a>   | 500C C41Ch                 | 5000 D41Ch                 | 5004 D41Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>     | 500C C420h                 | 5000 D420h                 | 5004 D420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>     | 500C C428h                 | 5000 D428h                 | 5004 D428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>     | 500C C430h                 | 5000 D430h                 | 5004 D430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>     | 500C C600h                 | 5000 D600h                 | 5004 D600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>     | 500C C604h                 | 5000 D604h                 | 5004 D604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>     | 500C C608h                 | 5000 D608h                 | 5004 D608h                 |

**Table 3-788. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM26_G1 Physical Address | EPWM27_G1 Physical Address | EPWM28_G1 Physical Address |
|--------|--------|-------------------------------------|----------------------------|----------------------------|----------------------------|
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>   | 500C C60Ch                 | 5000 D60Ch                 | 5004 D60Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>   | 500C C610h                 | 5000 D610h                 | 5004 D610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 500C C614h                 | 5000 D614h                 | 5004 D614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 500C C618h                 | 5000 D618h                 | 5004 D618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 500C C61Ch                 | 5000 D61Ch                 | 5004 D61Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 500C C620h                 | 5000 D620h                 | 5004 D620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 500C C630h                 | 5000 D630h                 | 5004 D630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 500C C632h                 | 5000 D632h                 | 5004 D632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 500C C644h                 | 5000 D644h                 | 5004 D644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 500C C680h                 | 5000 D680h                 | 5004 D680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 500C C684h                 | 5000 D684h                 | 5004 D684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 500C C688h                 | 5000 D688h                 | 5004 D688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 500C C68Ch                 | 5000 D68Ch                 | 5004 D68Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 500C C690h                 | 5000 D690h                 | 5004 D690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 500C C694h                 | 5000 D694h                 | 5004 D694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 500C C698h                 | 5000 D698h                 | 5004 D698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 500C C69Ch                 | 5000 D69Ch                 | 5004 D69Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 500C C6A0h                 | 5000 D6A0h                 | 5004 D6A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 500C C6B0h                 | 5000 D6B0h                 | 5004 D6B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 500C C6B2h                 | 5000 D6B2h                 | 5004 D6B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 500C C6BAh                 | 5000 D6BAh                 | 5004 D6BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 500C C6BEh                 | 5000 D6BEh                 | 5004 D6BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 500C C6C4h                 | 5000 D6C4h                 | 5004 D6C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 500C C700h                 | 5000 D700h                 | 5004 D700h                 |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 500C C704h                 | 5000 D704h                 | 5004 D704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 500C C708h                 | 5000 D708h                 | 5004 D708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>    | 500C C70Ch                 | 5000 D70Ch                 | 5004 D70Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>    | 500C C710h                 | 5000 D710h                 | 5004 D710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>    | 500C C714h                 | 5000 D714h                 | 5004 D714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>    | 500C C718h                 | 5000 D718h                 | 5004 D718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>    | 500C C71Ch                 | 5000 D71Ch                 | 5004 D71Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>   | 500C C720h                 | 5000 D720h                 | 5004 D720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a>  | 500C C730h                 | 5000 D730h                 | 5004 D730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a>  | 500C C732h                 | 5000 D732h                 | 5004 D732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>     | 500C C73Ah                 | 5000 D73Ah                 | 5004 D73Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>     | 500C C73Eh                 | 5000 D73Eh                 | 5004 D73Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a>  | 500C C744h                 | 5000 D744h                 | 5004 D744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>    | 500C C780h                 | 5000 D780h                 | 5004 D780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>    | 500C C784h                 | 5000 D784h                 | 5004 D784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>    | 500C C788h                 | 5000 D788h                 | 5004 D788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>    | 500C C78Ch                 | 5000 D78Ch                 | 5004 D78Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>    | 500C C790h                 | 5000 D790h                 | 5004 D790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>    | 500C C794h                 | 5000 D794h                 | 5004 D794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>    | 500C C798h                 | 5000 D798h                 | 5004 D798h                 |

**Table 3-788. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM26_G1 Physical Address | EPWM27_G1 Physical Address | EPWM28_G1 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 500C C79Ch                 | 5000 D79Ch                 | 5004 D79Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 500C C7A0h                 | 5000 D7A0h                 | 5004 D7A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 500C C7B0h                 | 5000 D7B0h                 | 5004 D7B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 500C C7B2h                 | 5000 D7B2h                 | 5004 D7B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 500C C7BAh                 | 5000 D7BAh                 | 5004 D7BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 500C C7BEh                 | 5000 D7BEh                 | 5004 D7BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 500C C7C4h                 | 5000 D7C4h                 | 5004 D7C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 500C C800h                 | 5000 D800h                 | 5004 D800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 500C C804h                 | 5000 D804h                 | 5004 D804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 500C C808h                 | 5000 D808h                 | 5004 D808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 500C C80Ch                 | 5000 D80Ch                 | 5004 D80Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 500C C810h                 | 5000 D810h                 | 5004 D810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 500C C814h                 | 5000 D814h                 | 5004 D814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 500C C820h                 | 5000 D820h                 | 5004 D820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 500C C824h                 | 5000 D824h                 | 5004 D824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 500C C828h                 | 5000 D828h                 | 5004 D828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 500C C82Ch                 | 5000 D82Ch                 | 5004 D82Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFG</a>      | 500C CC00h                 | 5000 DC00h                 | 5004 DC00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 500C CC04h                 | 5000 DC04h                 | 5004 DC04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 500C CC20h                 | 5000 DC20h                 | 5004 DC20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 500C CC24h                 | 5000 DC24h                 | 5004 DC24h                 |

**Table 3-789. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM29_G1 Physical Address | EPWM3_G1 Physical Address | EPWM30_G1 Physical Address |
|--------|--------|------------------------------------|----------------------------|---------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5008 D000h                 | 500C D000h                | 5000 E000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5008 D002h                 | 500C D002h                | 5000 E002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5008 D006h                 | 500C D006h                | 5000 E006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5008 D008h                 | 500C D008h                | 5000 E008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5008 D00Ah                 | 500C D00Ah                | 5000 E00Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 5008 D00Ch                 | 500C D00Ch                | 5000 E00Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5008 D00Eh                 | 500C D00Eh                | 5000 E00Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5008 D010h                 | 500C D010h                | 5000 E010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5008 D012h                 | 500C D012h                | 5000 E012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 5008 D018h                 | 500C D018h                | 5000 E018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 5008 D01Ah                 | 500C D01Ah                | 5000 E01Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 5008 D020h                 | 500C D020h                | 5000 E020h                 |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 5008 D022h                 | 500C D022h                | 5000 E022h                 |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 5008 D028h                 | 500C D028h                | 5000 E028h                 |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 5008 D030h                 | 500C D030h                | 5000 E030h                 |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 5008 D032h                 | 500C D032h                | 5000 E032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 5008 D040h                 | 500C D040h                | 5000 E040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 5008 D04Eh                 | 500C D04Eh                | 5000 E04Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>        | 5008 D05Ah                 | 500C D05Ah                | 5000 E05Ah                 |

**Table 3-789. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                     | EPWM29_G1 Physical Address | EPWM3_G1 Physical Address | EPWM30_G1 Physical Address |
|--------|--------|-----------------------------------|----------------------------|---------------------------|----------------------------|
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>        | 5008 D05Ch                 | 500C D05Ch                | 5000 E05Ch                 |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>       | 5008 D068h                 | 500C D068h                | 5000 E068h                 |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>       | 5008 D06Ah                 | 500C D06Ah                | 5000 E06Ah                 |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>    | 5008 D070h                 | 500C D070h                | 5000 E070h                 |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>   | 5008 D074h                 | 500C D074h                | 5000 E074h                 |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>        | 5008 D07Ah                 | 500C D07Ah                | 5000 E07Ah                 |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>      | 5008 D07Ch                 | 500C D07Ch                | 5000 E07Ch                 |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>     | 5008 D07Eh                 | 500C D07Eh                | 5000 E07Eh                 |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>       | 5008 D080h                 | 500C D080h                | 5000 E080h                 |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>      | 5008 D082h                 | 500C D082h                | 5000 E082h                 |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>       | 5008 D084h                 | 500C D084h                | 5000 E084h                 |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>      | 5008 D086h                 | 500C D086h                | 5000 E086h                 |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>       | 5008 D08Eh                 | 500C D08Eh                | 5000 E08Eh                 |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>      | 5008 D092h                 | 500C D092h                | 5000 E092h                 |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>      | 5008 D0A0h                 | 500C D0A0h                | 5000 E0A0h                 |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>        | 5008 D0A2h                 | 500C D0A2h                | 5000 E0A2h                 |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>      | 5008 D0A4h                 | 500C D0A4h                | 5000 E0A4h                 |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>        | 5008 D0A6h                 | 500C D0A6h                | 5000 E0A6h                 |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>        | 5008 D0C0h                 | 500C D0C0h                | 5000 E0C0h                 |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>      | 5008 D0C4h                 | 500C D0C4h                | 5000 E0C4h                 |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>        | 5008 D0C6h                 | 500C D0C6h                | 5000 E0C6h                 |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>     | 5008 D0C8h                 | 500C D0C8h                | 5000 E0C8h                 |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>         | 5008 D0D4h                 | 500C D0D4h                | 5000 E0D4h                 |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>         | 5008 D0D8h                 | 500C D0D8h                | 5000 E0D8h                 |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>         | 5008 D0DEh                 | 500C D0DEh                | 5000 E0DEh                 |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>         | 5008 D0E2h                 | 500C D0E2h                | 5000 E0E2h                 |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>      | 5008 D0E8h                 | 500C D0E8h                | 5000 E0E8h                 |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>    | 5008 D0EEh                 | 500C D0EEh                | 5000 E0EEh                 |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>        | 5008 D100h                 | 500C D100h                | 5000 E100h                 |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>       | 5008 D102h                 | 500C D102h                | 5000 E102h                 |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>      | 5008 D104h                 | 500C D104h                | 5000 E104h                 |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>        | 5008 D108h                 | 500C D108h                | 5000 E108h                 |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>       | 5008 D10Ah                 | 500C D10Ah                | 5000 E10Ah                 |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>     | 5008 D10Ch                 | 500C D10Ch                | 5000 E10Ch                 |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>     | 5008 D10Eh                 | 500C D10Eh                | 5000 E10Eh                 |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>       | 5008 D11Ah                 | 500C D11Ah                | 5000 E11Ah                 |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>        | 5008 D126h                 | 500C D126h                | 5000 E126h                 |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>     | 5008 D128h                 | 500C D128h                | 5000 E128h                 |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>     | 5008 D12Ah                 | 500C D12Ah                | 5000 E12Ah                 |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>        | 5008 D12Eh                 | 500C D12Eh                | 5000 E12Eh                 |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>     | 5008 D130h                 | 500C D130h                | 5000 E130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>     | 5008 D132h                 | 500C D132h                | 5000 E132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>        | 5008 D136h                 | 500C D136h                | 5000 E136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a> | 5008 D13Ah                 | 500C D13Ah                | 5000 E13Ah                 |

**Table 3-789. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM29_G1 Physical Address | EPWM3_G1 Physical Address | EPWM30_G1 Physical Address |
|--------|--------|---------------------------------------|----------------------------|---------------------------|----------------------------|
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>            | 5008 D148h                 | 500C D148h                | 5000 E148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>             | 5008 D14Ch                 | 500C D14Ch                | 5000 E14Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>            | 5008 D150h                 | 500C D150h                | 5000 E150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>            | 5008 D154h                 | 500C D154h                | 5000 E154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 5008 D158h                 | 500C D158h                | 5000 E158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 5008 D15Ch                 | 500C D15Ch                | 5000 E15Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 5008 D160h                 | 500C D160h                | 5000 E160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 5008 D164h                 | 500C D164h                | 5000 E164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 5008 D168h                 | 500C D168h                | 5000 E168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 5008 D16Ch                 | 500C D16Ch                | 5000 E16Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 5008 D170h                 | 500C D170h                | 5000 E170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 5008 D174h                 | 500C D174h                | 5000 E174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 5008 D180h                 | 500C D180h                | 5000 E180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 5008 D186h                 | 500C D186h                | 5000 E186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5008 D188h                 | 500C D188h                | 5000 E188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5008 D18Eh                 | 500C D18Eh                | 5000 E18Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5008 D190h                 | 500C D190h                | 5000 E190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5008 D192h                 | 500C D192h                | 5000 E192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5008 D194h                 | 500C D194h                | 5000 E194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5008 D196h                 | 500C D196h                | 5000 E196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5008 D198h                 | 500C D198h                | 5000 E198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5008 D19Ah                 | 500C D19Ah                | 5000 E19Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5008 D19Ch                 | 500C D19Ch                | 5000 E19Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5008 D19Eh                 | 500C D19Eh                | 5000 E19Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5008 D1A4h                 | 500C D1A4h                | 5000 E1A4h                 |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5008 D1A6h                 | 500C D1A6h                | 5000 E1A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 5008 D1A8h                 | 500C D1A8h                | 5000 E1A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 5008 D1AAh                 | 500C D1AAh                | 5000 E1AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 5008 D1ACh                 | 500C D1ACh                | 5000 E1ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 5008 D1AEh                 | 500C D1AEh                | 5000 E1AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 5008 D1B0h                 | 500C D1B0h                | 5000 E1B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 5008 D1B2h                 | 500C D1B2h                | 5000 E1B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 5008 D1F4h                 | 500C D1F4h                | 5000 E1F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 5008 D1FAh                 | 500C D1FAh                | 5000 E1FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 5008 D1FCh                 | 500C D1FCh                | 5000 E1FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>         | 5008 D400h                 | 500C D400h                | 5000 E400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>         | 5008 D410h                 | 500C D410h                | 5000 E410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>            | 5008 D418h                 | 500C D418h                | 5000 E418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a>   | 5008 D41Ch                 | 500C D41Ch                | 5000 E41Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>     | 5008 D420h                 | 500C D420h                | 5000 E420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>     | 5008 D428h                 | 500C D428h                | 5000 E428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>     | 5008 D430h                 | 500C D430h                | 5000 E430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>     | 5008 D600h                 | 500C D600h                | 5000 E600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>     | 5008 D604h                 | 500C D604h                | 5000 E604h                 |

**Table 3-789. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM29_G1 Physical Address | EPWM3_G1 Physical Address | EPWM30_G1 Physical Address |
|--------|--------|-------------------------------------|----------------------------|---------------------------|----------------------------|
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>   | 5008 D608h                 | 500C D608h                | 5000 E608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>   | 5008 D60Ch                 | 500C D60Ch                | 5000 E60Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>   | 5008 D610h                 | 500C D610h                | 5000 E610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 5008 D614h                 | 500C D614h                | 5000 E614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 5008 D618h                 | 500C D618h                | 5000 E618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 5008 D61Ch                 | 500C D61Ch                | 5000 E61Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 5008 D620h                 | 500C D620h                | 5000 E620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 5008 D630h                 | 500C D630h                | 5000 E630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 5008 D632h                 | 500C D632h                | 5000 E632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 5008 D644h                 | 500C D644h                | 5000 E644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 5008 D680h                 | 500C D680h                | 5000 E680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 5008 D684h                 | 500C D684h                | 5000 E684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 5008 D688h                 | 500C D688h                | 5000 E688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 5008 D68Ch                 | 500C D68Ch                | 5000 E68Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 5008 D690h                 | 500C D690h                | 5000 E690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 5008 D694h                 | 500C D694h                | 5000 E694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 5008 D698h                 | 500C D698h                | 5000 E698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 5008 D69Ch                 | 500C D69Ch                | 5000 E69Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 5008 D6A0h                 | 500C D6A0h                | 5000 E6A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 5008 D6B0h                 | 500C D6B0h                | 5000 E6B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 5008 D6B2h                 | 500C D6B2h                | 5000 E6B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 5008 D6BAh                 | 500C D6BAh                | 5000 E6BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 5008 D6BEh                 | 500C D6BEh                | 5000 E6BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 5008 D6C4h                 | 500C D6C4h                | 5000 E6C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 5008 D700h                 | 500C D700h                | 5000 E700h                 |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 5008 D704h                 | 500C D704h                | 5000 E704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 5008 D708h                 | 500C D708h                | 5000 E708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>    | 5008 D70Ch                 | 500C D70Ch                | 5000 E70Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>    | 5008 D710h                 | 500C D710h                | 5000 E710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>    | 5008 D714h                 | 500C D714h                | 5000 E714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>    | 5008 D718h                 | 500C D718h                | 5000 E718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>    | 5008 D71Ch                 | 500C D71Ch                | 5000 E71Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>   | 5008 D720h                 | 500C D720h                | 5000 E720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a>  | 5008 D730h                 | 500C D730h                | 5000 E730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a>  | 5008 D732h                 | 500C D732h                | 5000 E732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>     | 5008 D73Ah                 | 500C D73Ah                | 5000 E73Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>     | 5008 D73Eh                 | 500C D73Eh                | 5000 E73Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a>  | 5008 D744h                 | 500C D744h                | 5000 E744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>    | 5008 D780h                 | 500C D780h                | 5000 E780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>    | 5008 D784h                 | 500C D784h                | 5000 E784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>    | 5008 D788h                 | 500C D788h                | 5000 E788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>    | 5008 D78Ch                 | 500C D78Ch                | 5000 E78Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>    | 5008 D790h                 | 500C D790h                | 5000 E790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>    | 5008 D794h                 | 500C D794h                | 5000 E794h                 |



**Table 3-789. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM29_G1 Physical Address | EPWM3_G1 Physical Address | EPWM30_G1 Physical Address |
|--------|--------|------------------------------------|----------------------------|---------------------------|----------------------------|
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 5008 D798h                 | 500C D798h                | 5000 E798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 5008 D79Ch                 | 500C D79Ch                | 5000 E79Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 5008 D7A0h                 | 500C D7A0h                | 5000 E7A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5008 D7B0h                 | 500C D7B0h                | 5000 E7B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5008 D7B2h                 | 500C D7B2h                | 5000 E7B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5008 D7BAh                 | 500C D7BAh                | 5000 E7BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5008 D7BEh                 | 500C D7BEh                | 5000 E7BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5008 D7C4h                 | 500C D7C4h                | 5000 E7C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5008 D800h                 | 500C D800h                | 5000 E800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5008 D804h                 | 500C D804h                | 5000 E804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5008 D808h                 | 500C D808h                | 5000 E808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5008 D80Ch                 | 500C D80Ch                | 5000 E80Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 5008 D810h                 | 500C D810h                | 5000 E810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5008 D814h                 | 500C D814h                | 5000 E814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 5008 D820h                 | 500C D820h                | 5000 E820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 5008 D824h                 | 500C D824h                | 5000 E824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 5008 D828h                 | 500C D828h                | 5000 E828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 5008 D82Ch                 | 500C D82Ch                | 5000 E82Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>     | 5008 DC00h                 | 500C DC00h                | 5000 EC00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 5008 DC04h                 | 500C DC04h                | 5000 EC04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 5008 DC20h                 | 500C DC20h                | 5000 EC20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 5008 DC24h                 | 500C DC24h                | 5000 EC24h                 |

**Table 3-790. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM31_G1 Physical Address | EPWM4_G1 Physical Address | EPWM5_G1 Physical Address |
|--------|--------|------------------------------------|----------------------------|---------------------------|---------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5004 E000h                 | 5008 E000h                | 500C E000h                |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5004 E002h                 | 5008 E002h                | 500C E002h                |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5004 E006h                 | 5008 E006h                | 500C E006h                |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5004 E008h                 | 5008 E008h                | 500C E008h                |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5004 E00Ah                 | 5008 E00Ah                | 500C E00Ah                |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 5004 E00Ch                 | 5008 E00Ch                | 500C E00Ch                |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5004 E00Eh                 | 5008 E00Eh                | 500C E00Eh                |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5004 E010h                 | 5008 E010h                | 500C E010h                |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5004 E012h                 | 5008 E012h                | 500C E012h                |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 5004 E018h                 | 5008 E018h                | 500C E018h                |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 5004 E01Ah                 | 5008 E01Ah                | 500C E01Ah                |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 5004 E020h                 | 5008 E020h                | 500C E020h                |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 5004 E022h                 | 5008 E022h                | 500C E022h                |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 5004 E028h                 | 5008 E028h                | 500C E028h                |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 5004 E030h                 | 5008 E030h                | 500C E030h                |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 5004 E032h                 | 5008 E032h                | 500C E032h                |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 5004 E040h                 | 5008 E040h                | 500C E040h                |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 5004 E04Eh                 | 5008 E04Eh                | 500C E04Eh                |



**Table 3-790. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                   | EPWM31_G1 Physical Address | EPWM4_G1 Physical Address | EPWM5_G1 Physical Address |
|--------|--------|---------------------------------|----------------------------|---------------------------|---------------------------|
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>     | 5004 E05Ah                 | 5008 E05Ah                | 500C E05Ah                |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>      | 5004 E05Ch                 | 5008 E05Ch                | 500C E05Ch                |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>     | 5004 E068h                 | 5008 E068h                | 500C E068h                |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>     | 5004 E06Ah                 | 5008 E06Ah                | 500C E06Ah                |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>  | 5004 E070h                 | 5008 E070h                | 500C E070h                |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a> | 5004 E074h                 | 5008 E074h                | 500C E074h                |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>      | 5004 E07Ah                 | 5008 E07Ah                | 500C E07Ah                |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>    | 5004 E07Ch                 | 5008 E07Ch                | 500C E07Ch                |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>   | 5004 E07Eh                 | 5008 E07Eh                | 500C E07Eh                |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>     | 5004 E080h                 | 5008 E080h                | 500C E080h                |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>    | 5004 E082h                 | 5008 E082h                | 500C E082h                |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>     | 5004 E084h                 | 5008 E084h                | 500C E084h                |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>    | 5004 E086h                 | 5008 E086h                | 500C E086h                |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>     | 5004 E08Eh                 | 5008 E08Eh                | 500C E08Eh                |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>    | 5004 E092h                 | 5008 E092h                | 500C E092h                |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>    | 5004 E0A0h                 | 5008 E0A0h                | 500C E0A0h                |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>      | 5004 E0A2h                 | 5008 E0A2h                | 500C E0A2h                |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>    | 5004 E0A4h                 | 5008 E0A4h                | 500C E0A4h                |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>      | 5004 E0A6h                 | 5008 E0A6h                | 500C E0A6h                |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>      | 5004 E0C0h                 | 5008 E0C0h                | 500C E0C0h                |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>    | 5004 E0C4h                 | 5008 E0C4h                | 500C E0C4h                |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>      | 5004 E0C6h                 | 5008 E0C6h                | 500C E0C6h                |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>   | 5004 E0C8h                 | 5008 E0C8h                | 500C E0C8h                |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>       | 5004 E0D4h                 | 5008 E0D4h                | 500C E0D4h                |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>       | 5004 E0D8h                 | 5008 E0D8h                | 500C E0D8h                |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>       | 5004 E0DEh                 | 5008 E0DEh                | 500C E0DEh                |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>       | 5004 E0E2h                 | 5008 E0E2h                | 500C E0E2h                |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>    | 5004 E0E8h                 | 5008 E0E8h                | 500C E0E8h                |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>  | 5004 E0EEh                 | 5008 E0EEh                | 500C E0EEh                |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>      | 5004 E100h                 | 5008 E100h                | 500C E100h                |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>     | 5004 E102h                 | 5008 E102h                | 500C E102h                |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>    | 5004 E104h                 | 5008 E104h                | 500C E104h                |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>      | 5004 E108h                 | 5008 E108h                | 500C E108h                |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>     | 5004 E10Ah                 | 5008 E10Ah                | 500C E10Ah                |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>   | 5004 E10Ch                 | 5008 E10Ch                | 500C E10Ch                |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>   | 5004 E10Eh                 | 5008 E10Eh                | 500C E10Eh                |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>     | 5004 E11Ah                 | 5008 E11Ah                | 500C E11Ah                |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>      | 5004 E126h                 | 5008 E126h                | 500C E126h                |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>   | 5004 E128h                 | 5008 E128h                | 500C E128h                |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>   | 5004 E12Ah                 | 5008 E12Ah                | 500C E12Ah                |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>      | 5004 E12Eh                 | 5008 E12Eh                | 500C E12Eh                |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>   | 5004 E130h                 | 5008 E130h                | 500C E130h                |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>   | 5004 E132h                 | 5008 E132h                | 500C E132h                |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>      | 5004 E136h                 | 5008 E136h                | 500C E136h                |

**Table 3-790. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM31_G1 Physical Address | EPWM4_G1 Physical Address | EPWM5_G1 Physical Address |
|--------|--------|---------------------------------------|----------------------------|---------------------------|---------------------------|
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a>     | 5004 E13Ah                 | 5008 E13Ah                | 500C E13Ah                |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>            | 5004 E148h                 | 5008 E148h                | 500C E148h                |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>             | 5004 E14Ch                 | 5008 E14Ch                | 500C E14Ch                |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>            | 5004 E150h                 | 5008 E150h                | 500C E150h                |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>            | 5004 E154h                 | 5008 E154h                | 500C E154h                |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 5004 E158h                 | 5008 E158h                | 500C E158h                |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 5004 E15Ch                 | 5008 E15Ch                | 500C E15Ch                |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 5004 E160h                 | 5008 E160h                | 500C E160h                |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 5004 E164h                 | 5008 E164h                | 500C E164h                |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 5004 E168h                 | 5008 E168h                | 500C E168h                |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 5004 E16Ch                 | 5008 E16Ch                | 500C E16Ch                |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 5004 E170h                 | 5008 E170h                | 500C E170h                |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 5004 E174h                 | 5008 E174h                | 500C E174h                |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 5004 E180h                 | 5008 E180h                | 500C E180h                |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 5004 E186h                 | 5008 E186h                | 500C E186h                |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5004 E188h                 | 5008 E188h                | 500C E188h                |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5004 E18Eh                 | 5008 E18Eh                | 500C E18Eh                |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5004 E190h                 | 5008 E190h                | 500C E190h                |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5004 E192h                 | 5008 E192h                | 500C E192h                |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5004 E194h                 | 5008 E194h                | 500C E194h                |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5004 E196h                 | 5008 E196h                | 500C E196h                |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5004 E198h                 | 5008 E198h                | 500C E198h                |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5004 E19Ah                 | 5008 E19Ah                | 500C E19Ah                |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5004 E19Ch                 | 5008 E19Ch                | 500C E19Ch                |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5004 E19Eh                 | 5008 E19Eh                | 500C E19Eh                |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5004 E1A4h                 | 5008 E1A4h                | 500C E1A4h                |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5004 E1A6h                 | 5008 E1A6h                | 500C E1A6h                |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 5004 E1A8h                 | 5008 E1A8h                | 500C E1A8h                |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 5004 E1AAh                 | 5008 E1AAh                | 500C E1AAh                |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 5004 E1ACh                 | 5008 E1ACh                | 500C E1ACh                |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 5004 E1AEh                 | 5008 E1AEh                | 500C E1AEh                |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 5004 E1B0h                 | 5008 E1B0h                | 500C E1B0h                |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 5004 E1B2h                 | 5008 E1B2h                | 500C E1B2h                |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 5004 E1F4h                 | 5008 E1F4h                | 500C E1F4h                |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 5004 E1FAh                 | 5008 E1FAh                | 500C E1FAh                |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 5004 E1FCh                 | 5008 E1FCh                | 500C E1FCh                |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>         | 5004 E400h                 | 5008 E400h                | 500C E400h                |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>         | 5004 E410h                 | 5008 E410h                | 500C E410h                |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>            | 5004 E418h                 | 5008 E418h                | 500C E418h                |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a>   | 5004 E41Ch                 | 5008 E41Ch                | 500C E41Ch                |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>     | 5004 E420h                 | 5008 E420h                | 500C E420h                |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>     | 5004 E428h                 | 5008 E428h                | 500C E428h                |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>     | 5004 E430h                 | 5008 E430h                | 500C E430h                |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>     | 5004 E600h                 | 5008 E600h                | 500C E600h                |

**Table 3-790. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM31_G1 Physical Address | EPWM4_G1 Physical Address | EPWM5_G1 Physical Address |
|--------|--------|-------------------------------------|----------------------------|---------------------------|---------------------------|
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>   | 5004 E604h                 | 5008 E604h                | 500C E604h                |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>   | 5004 E608h                 | 5008 E608h                | 500C E608h                |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>   | 5004 E60Ch                 | 5008 E60Ch                | 500C E60Ch                |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>   | 5004 E610h                 | 5008 E610h                | 500C E610h                |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 5004 E614h                 | 5008 E614h                | 500C E614h                |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 5004 E618h                 | 5008 E618h                | 500C E618h                |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 5004 E61Ch                 | 5008 E61Ch                | 500C E61Ch                |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 5004 E620h                 | 5008 E620h                | 500C E620h                |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 5004 E630h                 | 5008 E630h                | 500C E630h                |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 5004 E632h                 | 5008 E632h                | 500C E632h                |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 5004 E644h                 | 5008 E644h                | 500C E644h                |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 5004 E680h                 | 5008 E680h                | 500C E680h                |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 5004 E684h                 | 5008 E684h                | 500C E684h                |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 5004 E688h                 | 5008 E688h                | 500C E688h                |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 5004 E68Ch                 | 5008 E68Ch                | 500C E68Ch                |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 5004 E690h                 | 5008 E690h                | 500C E690h                |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 5004 E694h                 | 5008 E694h                | 500C E694h                |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 5004 E698h                 | 5008 E698h                | 500C E698h                |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 5004 E69Ch                 | 5008 E69Ch                | 500C E69Ch                |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 5004 E6A0h                 | 5008 E6A0h                | 500C E6A0h                |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 5004 E6B0h                 | 5008 E6B0h                | 500C E6B0h                |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 5004 E6B2h                 | 5008 E6B2h                | 500C E6B2h                |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 5004 E6BAh                 | 5008 E6BAh                | 500C E6BAh                |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 5004 E6BEh                 | 5008 E6BEh                | 500C E6BEh                |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 5004 E6C4h                 | 5008 E6C4h                | 500C E6C4h                |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 5004 E700h                 | 5008 E700h                | 500C E700h                |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 5004 E704h                 | 5008 E704h                | 500C E704h                |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 5004 E708h                 | 5008 E708h                | 500C E708h                |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>    | 5004 E70Ch                 | 5008 E70Ch                | 500C E70Ch                |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>    | 5004 E710h                 | 5008 E710h                | 500C E710h                |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>    | 5004 E714h                 | 5008 E714h                | 500C E714h                |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>    | 5004 E718h                 | 5008 E718h                | 500C E718h                |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>    | 5004 E71Ch                 | 5008 E71Ch                | 500C E71Ch                |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>   | 5004 E720h                 | 5008 E720h                | 500C E720h                |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a>  | 5004 E730h                 | 5008 E730h                | 500C E730h                |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a>  | 5004 E732h                 | 5008 E732h                | 500C E732h                |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>     | 5004 E73Ah                 | 5008 E73Ah                | 500C E73Ah                |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>     | 5004 E73Eh                 | 5008 E73Eh                | 500C E73Eh                |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a>  | 5004 E744h                 | 5008 E744h                | 500C E744h                |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>    | 5004 E780h                 | 5008 E780h                | 500C E780h                |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>    | 5004 E784h                 | 5008 E784h                | 500C E784h                |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>    | 5004 E788h                 | 5008 E788h                | 500C E788h                |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>    | 5004 E78Ch                 | 5008 E78Ch                | 500C E78Ch                |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>    | 5004 E790h                 | 5008 E790h                | 500C E790h                |

**Table 3-790. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM31_G1 Physical Address | EPWM4_G1 Physical Address | EPWM5_G1 Physical Address |
|--------|--------|------------------------------------|----------------------------|---------------------------|---------------------------|
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 5004 E794h                 | 5008 E794h                | 500C E794h                |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 5004 E798h                 | 5008 E798h                | 500C E798h                |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 5004 E79Ch                 | 5008 E79Ch                | 500C E79Ch                |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 5004 E7A0h                 | 5008 E7A0h                | 500C E7A0h                |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5004 E7B0h                 | 5008 E7B0h                | 500C E7B0h                |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5004 E7B2h                 | 5008 E7B2h                | 500C E7B2h                |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5004 E7BAh                 | 5008 E7BAh                | 500C E7BAh                |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5004 E7BEh                 | 5008 E7BEh                | 500C E7BEh                |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5004 E7C4h                 | 5008 E7C4h                | 500C E7C4h                |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5004 E800h                 | 5008 E800h                | 500C E800h                |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5004 E804h                 | 5008 E804h                | 500C E804h                |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5004 E808h                 | 5008 E808h                | 500C E808h                |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5004 E80Ch                 | 5008 E80Ch                | 500C E80Ch                |
| 810h   | 32     | <a href="#">EPWM_DEFRFC</a>        | 5004 E810h                 | 5008 E810h                | 500C E810h                |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5004 E814h                 | 5008 E814h                | 500C E814h                |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 5004 E820h                 | 5008 E820h                | 500C E820h                |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 5004 E824h                 | 5008 E824h                | 500C E824h                |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 5004 E828h                 | 5008 E828h                | 500C E828h                |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 5004 E82Ch                 | 5008 E82Ch                | 500C E82Ch                |
| C00h   | 32     | <a href="#">EPWM_MINDBCFG</a>      | 5004 EC00h                 | 5008 EC00h                | 500C EC00h                |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 5004 EC04h                 | 5008 EC04h                | 500C EC04h                |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 5004 EC20h                 | 5008 EC20h                | 500C EC20h                |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 5004 EC24h                 | 5008 EC24h                | 500C EC24h                |

**Table 3-791. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM6_G1 Physical Address | EPWM7_G1 Physical Address | EPWM8_G1 Physical Address |
|--------|--------|------------------------------------|---------------------------|---------------------------|---------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5000 F000h                | 5004 F000h                | 5008 F000h                |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5000 F002h                | 5004 F002h                | 5008 F002h                |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5000 F006h                | 5004 F006h                | 5008 F006h                |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5000 F008h                | 5004 F008h                | 5008 F008h                |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5000 F00Ah                | 5004 F00Ah                | 5008 F00Ah                |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 5000 F00Ch                | 5004 F00Ch                | 5008 F00Ch                |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5000 F00Eh                | 5004 F00Eh                | 5008 F00Eh                |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5000 F010h                | 5004 F010h                | 5008 F010h                |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5000 F012h                | 5004 F012h                | 5008 F012h                |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 5000 F018h                | 5004 F018h                | 5008 F018h                |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 5000 F01Ah                | 5004 F01Ah                | 5008 F01Ah                |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 5000 F020h                | 5004 F020h                | 5008 F020h                |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 5000 F022h                | 5004 F022h                | 5008 F022h                |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 5000 F028h                | 5004 F028h                | 5008 F028h                |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 5000 F030h                | 5004 F030h                | 5008 F030h                |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 5000 F032h                | 5004 F032h                | 5008 F032h                |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 5000 F040h                | 5004 F040h                | 5008 F040h                |

**Table 3-791. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                   | EPWM6_G1 Physical Address | EPWM7_G1 Physical Address | EPWM8_G1 Physical Address |
|--------|--------|---------------------------------|---------------------------|---------------------------|---------------------------|
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>    | 5000 F04Eh                | 5004 F04Eh                | 5008 F04Eh                |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>     | 5000 F05Ah                | 5004 F05Ah                | 5008 F05Ah                |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>      | 5000 F05Ch                | 5004 F05Ch                | 5008 F05Ch                |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>     | 5000 F068h                | 5004 F068h                | 5008 F068h                |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>     | 5000 F06Ah                | 5004 F06Ah                | 5008 F06Ah                |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>  | 5000 F070h                | 5004 F070h                | 5008 F070h                |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a> | 5000 F074h                | 5004 F074h                | 5008 F074h                |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>      | 5000 F07Ah                | 5004 F07Ah                | 5008 F07Ah                |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>    | 5000 F07Ch                | 5004 F07Ch                | 5008 F07Ch                |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>   | 5000 F07Eh                | 5004 F07Eh                | 5008 F07Eh                |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>     | 5000 F080h                | 5004 F080h                | 5008 F080h                |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>    | 5000 F082h                | 5004 F082h                | 5008 F082h                |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>     | 5000 F084h                | 5004 F084h                | 5008 F084h                |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>    | 5000 F086h                | 5004 F086h                | 5008 F086h                |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>     | 5000 F08Eh                | 5004 F08Eh                | 5008 F08Eh                |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>    | 5000 F092h                | 5004 F092h                | 5008 F092h                |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>    | 5000 F0A0h                | 5004 F0A0h                | 5008 F0A0h                |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>      | 5000 F0A2h                | 5004 F0A2h                | 5008 F0A2h                |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>    | 5000 F0A4h                | 5004 F0A4h                | 5008 F0A4h                |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>      | 5000 F0A6h                | 5004 F0A6h                | 5008 F0A6h                |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>      | 5000 F0C0h                | 5004 F0C0h                | 5008 F0C0h                |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>    | 5000 F0C4h                | 5004 F0C4h                | 5008 F0C4h                |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>      | 5000 F0C6h                | 5004 F0C6h                | 5008 F0C6h                |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>   | 5000 F0C8h                | 5004 F0C8h                | 5008 F0C8h                |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>       | 5000 F0D4h                | 5004 F0D4h                | 5008 F0D4h                |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>       | 5000 F0D8h                | 5004 F0D8h                | 5008 F0D8h                |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>       | 5000 F0DEh                | 5004 F0DEh                | 5008 F0DEh                |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>       | 5000 F0E2h                | 5004 F0E2h                | 5008 F0E2h                |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>    | 5000 F0E8h                | 5004 F0E8h                | 5008 F0E8h                |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>  | 5000 F0EEh                | 5004 F0EEh                | 5008 F0EEh                |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>      | 5000 F100h                | 5004 F100h                | 5008 F100h                |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>     | 5000 F102h                | 5004 F102h                | 5008 F102h                |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>    | 5000 F104h                | 5004 F104h                | 5008 F104h                |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>      | 5000 F108h                | 5004 F108h                | 5008 F108h                |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>     | 5000 F10Ah                | 5004 F10Ah                | 5008 F10Ah                |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>   | 5000 F10Ch                | 5004 F10Ch                | 5008 F10Ch                |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>   | 5000 F10Eh                | 5004 F10Eh                | 5008 F10Eh                |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>     | 5000 F11Ah                | 5004 F11Ah                | 5008 F11Ah                |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>      | 5000 F126h                | 5004 F126h                | 5008 F126h                |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>   | 5000 F128h                | 5004 F128h                | 5008 F128h                |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>   | 5000 F12Ah                | 5004 F12Ah                | 5008 F12Ah                |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>      | 5000 F12Eh                | 5004 F12Eh                | 5008 F12Eh                |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>   | 5000 F130h                | 5004 F130h                | 5008 F130h                |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>   | 5000 F132h                | 5004 F132h                | 5008 F132h                |

**Table 3-791. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM6_G1 Physical Address | EPWM7_G1 Physical Address | EPWM8_G1 Physical Address |
|--------|--------|---------------------------------------|---------------------------|---------------------------|---------------------------|
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>            | 5000 F136h                | 5004 F136h                | 5008 F136h                |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a>     | 5000 F13Ah                | 5004 F13Ah                | 5008 F13Ah                |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>            | 5000 F148h                | 5004 F148h                | 5008 F148h                |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>             | 5000 F14Ch                | 5004 F14Ch                | 5008 F14Ch                |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>            | 5000 F150h                | 5004 F150h                | 5008 F150h                |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>            | 5000 F154h                | 5004 F154h                | 5008 F154h                |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 5000 F158h                | 5004 F158h                | 5008 F158h                |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 5000 F15Ch                | 5004 F15Ch                | 5008 F15Ch                |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 5000 F160h                | 5004 F160h                | 5008 F160h                |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 5000 F164h                | 5004 F164h                | 5008 F164h                |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 5000 F168h                | 5004 F168h                | 5008 F168h                |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 5000 F16Ch                | 5004 F16Ch                | 5008 F16Ch                |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 5000 F170h                | 5004 F170h                | 5008 F170h                |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 5000 F174h                | 5004 F174h                | 5008 F174h                |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 5000 F180h                | 5004 F180h                | 5008 F180h                |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 5000 F186h                | 5004 F186h                | 5008 F186h                |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5000 F188h                | 5004 F188h                | 5008 F188h                |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5000 F18Eh                | 5004 F18Eh                | 5008 F18Eh                |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5000 F190h                | 5004 F190h                | 5008 F190h                |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5000 F192h                | 5004 F192h                | 5008 F192h                |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5000 F194h                | 5004 F194h                | 5008 F194h                |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5000 F196h                | 5004 F196h                | 5008 F196h                |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5000 F198h                | 5004 F198h                | 5008 F198h                |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5000 F19Ah                | 5004 F19Ah                | 5008 F19Ah                |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5000 F19Ch                | 5004 F19Ch                | 5008 F19Ch                |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5000 F19Eh                | 5004 F19Eh                | 5008 F19Eh                |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5000 F1A4h                | 5004 F1A4h                | 5008 F1A4h                |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5000 F1A6h                | 5004 F1A6h                | 5008 F1A6h                |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 5000 F1A8h                | 5004 F1A8h                | 5008 F1A8h                |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 5000 F1AAh                | 5004 F1AAh                | 5008 F1AAh                |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 5000 F1ACh                | 5004 F1ACh                | 5008 F1ACh                |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 5000 F1AEh                | 5004 F1AEh                | 5008 F1AEh                |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 5000 F1B0h                | 5004 F1B0h                | 5008 F1B0h                |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 5000 F1B2h                | 5004 F1B2h                | 5008 F1B2h                |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 5000 F1F4h                | 5004 F1F4h                | 5008 F1F4h                |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 5000 F1FAh                | 5004 F1FAh                | 5008 F1FAh                |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 5000 F1FCh                | 5004 F1FCh                | 5008 F1FCh                |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>         | 5000 F400h                | 5004 F400h                | 5008 F400h                |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>         | 5000 F410h                | 5004 F410h                | 5008 F410h                |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>            | 5000 F418h                | 5004 F418h                | 5008 F418h                |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a>   | 5000 F41Ch                | 5004 F41Ch                | 5008 F41Ch                |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>     | 5000 F420h                | 5004 F420h                | 5008 F420h                |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>     | 5000 F428h                | 5004 F428h                | 5008 F428h                |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>     | 5000 F430h                | 5004 F430h                | 5008 F430h                |

**Table 3-791. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM6_G1 Physical Address | EPWM7_G1 Physical Address | EPWM8_G1 Physical Address |
|--------|--------|-------------------------------------|---------------------------|---------------------------|---------------------------|
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>   | 5000 F600h                | 5004 F600h                | 5008 F600h                |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>   | 5000 F604h                | 5004 F604h                | 5008 F604h                |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>   | 5000 F608h                | 5004 F608h                | 5008 F608h                |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>   | 5000 F60Ch                | 5004 F60Ch                | 5008 F60Ch                |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>   | 5000 F610h                | 5004 F610h                | 5008 F610h                |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 5000 F614h                | 5004 F614h                | 5008 F614h                |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 5000 F618h                | 5004 F618h                | 5008 F618h                |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 5000 F61Ch                | 5004 F61Ch                | 5008 F61Ch                |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 5000 F620h                | 5004 F620h                | 5008 F620h                |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 5000 F630h                | 5004 F630h                | 5008 F630h                |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 5000 F632h                | 5004 F632h                | 5008 F632h                |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 5000 F644h                | 5004 F644h                | 5008 F644h                |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 5000 F680h                | 5004 F680h                | 5008 F680h                |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 5000 F684h                | 5004 F684h                | 5008 F684h                |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 5000 F688h                | 5004 F688h                | 5008 F688h                |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 5000 F68Ch                | 5004 F68Ch                | 5008 F68Ch                |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 5000 F690h                | 5004 F690h                | 5008 F690h                |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 5000 F694h                | 5004 F694h                | 5008 F694h                |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 5000 F698h                | 5004 F698h                | 5008 F698h                |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 5000 F69Ch                | 5004 F69Ch                | 5008 F69Ch                |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 5000 F6A0h                | 5004 F6A0h                | 5008 F6A0h                |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 5000 F6B0h                | 5004 F6B0h                | 5008 F6B0h                |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 5000 F6B2h                | 5004 F6B2h                | 5008 F6B2h                |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 5000 F6BAh                | 5004 F6BAh                | 5008 F6BAh                |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 5000 F6BEh                | 5004 F6BEh                | 5008 F6BEh                |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 5000 F6C4h                | 5004 F6C4h                | 5008 F6C4h                |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 5000 F700h                | 5004 F700h                | 5008 F700h                |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 5000 F704h                | 5004 F704h                | 5008 F704h                |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 5000 F708h                | 5004 F708h                | 5008 F708h                |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>    | 5000 F70Ch                | 5004 F70Ch                | 5008 F70Ch                |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>    | 5000 F710h                | 5004 F710h                | 5008 F710h                |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>    | 5000 F714h                | 5004 F714h                | 5008 F714h                |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>    | 5000 F718h                | 5004 F718h                | 5008 F718h                |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>    | 5000 F71Ch                | 5004 F71Ch                | 5008 F71Ch                |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>   | 5000 F720h                | 5004 F720h                | 5008 F720h                |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a>  | 5000 F730h                | 5004 F730h                | 5008 F730h                |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a>  | 5000 F732h                | 5004 F732h                | 5008 F732h                |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>     | 5000 F73Ah                | 5004 F73Ah                | 5008 F73Ah                |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>     | 5000 F73Eh                | 5004 F73Eh                | 5008 F73Eh                |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a>  | 5000 F744h                | 5004 F744h                | 5008 F744h                |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>    | 5000 F780h                | 5004 F780h                | 5008 F780h                |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>    | 5000 F784h                | 5004 F784h                | 5008 F784h                |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>    | 5000 F788h                | 5004 F788h                | 5008 F788h                |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>    | 5000 F78Ch                | 5004 F78Ch                | 5008 F78Ch                |



**Table 3-791. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM6_G1 Physical Address | EPWM7_G1 Physical Address | EPWM8_G1 Physical Address |
|--------|--------|------------------------------------|---------------------------|---------------------------|---------------------------|
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 5000 F790h                | 5004 F790h                | 5008 F790h                |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 5000 F794h                | 5004 F794h                | 5008 F794h                |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 5000 F798h                | 5004 F798h                | 5008 F798h                |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 5000 F79Ch                | 5004 F79Ch                | 5008 F79Ch                |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 5000 F7A0h                | 5004 F7A0h                | 5008 F7A0h                |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5000 F7B0h                | 5004 F7B0h                | 5008 F7B0h                |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5000 F7B2h                | 5004 F7B2h                | 5008 F7B2h                |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5000 F7BAh                | 5004 F7BAh                | 5008 F7BAh                |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5000 F7BEh                | 5004 F7BEh                | 5008 F7BEh                |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5000 F7C4h                | 5004 F7C4h                | 5008 F7C4h                |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5000 F800h                | 5004 F800h                | 5008 F800h                |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5000 F804h                | 5004 F804h                | 5008 F804h                |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5000 F808h                | 5004 F808h                | 5008 F808h                |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5000 F80Ch                | 5004 F80Ch                | 5008 F80Ch                |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 5000 F810h                | 5004 F810h                | 5008 F810h                |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5000 F814h                | 5004 F814h                | 5008 F814h                |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 5000 F820h                | 5004 F820h                | 5008 F820h                |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 5000 F824h                | 5004 F824h                | 5008 F824h                |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 5000 F828h                | 5004 F828h                | 5008 F828h                |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 5000 F82Ch                | 5004 F82Ch                | 5008 F82Ch                |
| C00h   | 32     | <a href="#">EPWM_MINDBCFG</a>      | 5000 FC00h                | 5004 FC00h                | 5008 FC00h                |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 5000 FC04h                | 5004 FC04h                | 5008 FC04h                |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 5000 FC20h                | 5004 FC20h                | 5008 FC20h                |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 5000 FC24h                | 5004 FC24h                | 5008 FC24h                |

**Table 3-792. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM9_G1 Physical Address | EPWM0_G2 Physical Address | EPWM1_G2 Physical Address |
|--------|--------|------------------------------------|---------------------------|---------------------------|---------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 500C F000h                | 5001 0000h                | 5005 0000h                |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 500C F002h                | 5001 0002h                | 5005 0002h                |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 500C F006h                | 5001 0006h                | 5005 0006h                |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 500C F008h                | 5001 0008h                | 5005 0008h                |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 500C F00Ah                | 5001 000Ah                | 5005 000Ah                |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 500C F00Ch                | 5001 000Ch                | 5005 000Ch                |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 500C F00Eh                | 5001 000Eh                | 5005 000Eh                |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 500C F010h                | 5001 0010h                | 5005 0010h                |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 500C F012h                | 5001 0012h                | 5005 0012h                |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 500C F018h                | 5001 0018h                | 5005 0018h                |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 500C F01Ah                | 5001 001Ah                | 5005 001Ah                |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 500C F020h                | 5001 0020h                | 5005 0020h                |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 500C F022h                | 5001 0022h                | 5005 0022h                |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 500C F028h                | 5001 0028h                | 5005 0028h                |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 500C F030h                | 5001 0030h                | 5005 0030h                |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 500C F032h                | 5001 0032h                | 5005 0032h                |



**Table 3-792. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                   | EPWM9_G1 Physical Address | EPWM0_G2 Physical Address | EPWM1_G2 Physical Address |
|--------|--------|---------------------------------|---------------------------|---------------------------|---------------------------|
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>     | 500C F040h                | 5001 0040h                | 5005 0040h                |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>    | 500C F04Eh                | 5001 004Eh                | 5005 004Eh                |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>     | 500C F05Ah                | 5001 005Ah                | 5005 005Ah                |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>      | 500C F05Ch                | 5001 005Ch                | 5005 005Ch                |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>     | 500C F068h                | 5001 0068h                | 5005 0068h                |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>     | 500C F06Ah                | 5001 006Ah                | 5005 006Ah                |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>  | 500C F070h                | 5001 0070h                | 5005 0070h                |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a> | 500C F074h                | 5001 0074h                | 5005 0074h                |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>      | 500C F07Ah                | 5001 007Ah                | 5005 007Ah                |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>    | 500C F07Ch                | 5001 007Ch                | 5005 007Ch                |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>   | 500C F07Eh                | 5001 007Eh                | 5005 007Eh                |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>     | 500C F080h                | 5001 0080h                | 5005 0080h                |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>    | 500C F082h                | 5001 0082h                | 5005 0082h                |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>     | 500C F084h                | 5001 0084h                | 5005 0084h                |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>    | 500C F086h                | 5001 0086h                | 5005 0086h                |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>     | 500C F08Eh                | 5001 008Eh                | 5005 008Eh                |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>    | 500C F092h                | 5001 0092h                | 5005 0092h                |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>    | 500C F0A0h                | 5001 00A0h                | 5005 00A0h                |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>      | 500C F0A2h                | 5001 00A2h                | 5005 00A2h                |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>    | 500C F0A4h                | 5001 00A4h                | 5005 00A4h                |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>      | 500C F0A6h                | 5001 00A6h                | 5005 00A6h                |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>      | 500C F0C0h                | 5001 00C0h                | 5005 00C0h                |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>    | 500C F0C4h                | 5001 00C4h                | 5005 00C4h                |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>      | 500C F0C6h                | 5001 00C6h                | 5005 00C6h                |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>   | 500C F0C8h                | 5001 00C8h                | 5005 00C8h                |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>       | 500C F0D4h                | 5001 00D4h                | 5005 00D4h                |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>       | 500C F0D8h                | 5001 00D8h                | 5005 00D8h                |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>       | 500C F0DEh                | 5001 00DEh                | 5005 00DEh                |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>       | 500C F0E2h                | 5001 00E2h                | 5005 00E2h                |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>    | 500C F0E8h                | 5001 00E8h                | 5005 00E8h                |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>  | 500C F0EEh                | 5001 00EEh                | 5005 00EEh                |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>      | 500C F100h                | 5001 0100h                | 5005 0100h                |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>     | 500C F102h                | 5001 0102h                | 5005 0102h                |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>    | 500C F104h                | 5001 0104h                | 5005 0104h                |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>      | 500C F108h                | 5001 0108h                | 5005 0108h                |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>     | 500C F10Ah                | 5001 010Ah                | 5005 010Ah                |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>   | 500C F10Ch                | 5001 010Ch                | 5005 010Ch                |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>   | 500C F10Eh                | 5001 010Eh                | 5005 010Eh                |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>     | 500C F11Ah                | 5001 011Ah                | 5005 011Ah                |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>      | 500C F126h                | 5001 0126h                | 5005 0126h                |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>   | 500C F128h                | 5001 0128h                | 5005 0128h                |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>   | 500C F12Ah                | 5001 012Ah                | 5005 012Ah                |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>      | 500C F12Eh                | 5001 012Eh                | 5005 012Eh                |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>   | 500C F130h                | 5001 0130h                | 5005 0130h                |

**Table 3-792. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM9_G1 Physical Address | EPWM0_G2 Physical Address | EPWM1_G2 Physical Address |
|--------|--------|---------------------------------------|---------------------------|---------------------------|---------------------------|
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>         | 500C F132h                | 5001 0132h                | 5005 0132h                |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>            | 500C F136h                | 5001 0136h                | 5005 0136h                |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a>     | 500C F13Ah                | 5001 013Ah                | 5005 013Ah                |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>            | 500C F148h                | 5001 0148h                | 5005 0148h                |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>             | 500C F14Ch                | 5001 014Ch                | 5005 014Ch                |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>            | 500C F150h                | 5001 0150h                | 5005 0150h                |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>            | 500C F154h                | 5001 0154h                | 5005 0154h                |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 500C F158h                | 5001 0158h                | 5005 0158h                |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 500C F15Ch                | 5001 015Ch                | 5005 015Ch                |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 500C F160h                | 5001 0160h                | 5005 0160h                |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 500C F164h                | 5001 0164h                | 5005 0164h                |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 500C F168h                | 5001 0168h                | 5005 0168h                |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 500C F16Ch                | 5001 016Ch                | 5005 016Ch                |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 500C F170h                | 5001 0170h                | 5005 0170h                |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 500C F174h                | 5001 0174h                | 5005 0174h                |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 500C F180h                | 5001 0180h                | 5005 0180h                |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 500C F186h                | 5001 0186h                | 5005 0186h                |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 500C F188h                | 5001 0188h                | 5005 0188h                |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 500C F18Eh                | 5001 018Eh                | 5005 018Eh                |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 500C F190h                | 5001 0190h                | 5005 0190h                |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 500C F192h                | 5001 0192h                | 5005 0192h                |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 500C F194h                | 5001 0194h                | 5005 0194h                |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 500C F196h                | 5001 0196h                | 5005 0196h                |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 500C F198h                | 5001 0198h                | 5005 0198h                |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 500C F19Ah                | 5001 019Ah                | 5005 019Ah                |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 500C F19Ch                | 5001 019Ch                | 5005 019Ch                |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 500C F19Eh                | 5001 019Eh                | 5005 019Eh                |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 500C F1A4h                | 5001 01A4h                | 5005 01A4h                |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 500C F1A6h                | 5001 01A6h                | 5005 01A6h                |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 500C F1A8h                | 5001 01A8h                | 5005 01A8h                |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 500C F1AAh                | 5001 01AAh                | 5005 01AAh                |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 500C F1ACh                | 5001 01ACh                | 5005 01ACh                |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 500C F1AEh                | 5001 01AEh                | 5005 01AEh                |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 500C F1B0h                | 5001 01B0h                | 5005 01B0h                |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 500C F1B2h                | 5001 01B2h                | 5005 01B2h                |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 500C F1F4h                | 5001 01F4h                | 5005 01F4h                |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 500C F1FAh                | 5001 01FAh                | 5005 01FAh                |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 500C F1FCh                | 5001 01FCh                | 5005 01FCh                |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>         | 500C F400h                | 5001 0400h                | 5005 0400h                |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>         | 500C F410h                | 5001 0410h                | 5005 0410h                |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>            | 500C F418h                | 5001 0418h                | 5005 0418h                |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a>   | 500C F41Ch                | 5001 041Ch                | 5005 041Ch                |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>     | 500C F420h                | 5001 0420h                | 5005 0420h                |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>     | 500C F428h                | 5001 0428h                | 5005 0428h                |

**Table 3-792. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM9_G1 Physical Address | EPWM0_G2 Physical Address | EPWM1_G2 Physical Address |
|--------|--------|-------------------------------------|---------------------------|---------------------------|---------------------------|
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>   | 500C F430h                | 5001 0430h                | 5005 0430h                |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>   | 500C F600h                | 5001 0600h                | 5005 0600h                |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>   | 500C F604h                | 5001 0604h                | 5005 0604h                |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>   | 500C F608h                | 5001 0608h                | 5005 0608h                |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>   | 500C F60Ch                | 5001 060Ch                | 5005 060Ch                |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>   | 500C F610h                | 5001 0610h                | 5005 0610h                |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 500C F614h                | 5001 0614h                | 5005 0614h                |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 500C F618h                | 5001 0618h                | 5005 0618h                |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 500C F61Ch                | 5001 061Ch                | 5005 061Ch                |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 500C F620h                | 5001 0620h                | 5005 0620h                |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 500C F630h                | 5001 0630h                | 5005 0630h                |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 500C F632h                | 5001 0632h                | 5005 0632h                |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 500C F644h                | 5001 0644h                | 5005 0644h                |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 500C F680h                | 5001 0680h                | 5005 0680h                |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 500C F684h                | 5001 0684h                | 5005 0684h                |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 500C F688h                | 5001 0688h                | 5005 0688h                |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 500C F68Ch                | 5001 068Ch                | 5005 068Ch                |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 500C F690h                | 5001 0690h                | 5005 0690h                |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 500C F694h                | 5001 0694h                | 5005 0694h                |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 500C F698h                | 5001 0698h                | 5005 0698h                |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 500C F69Ch                | 5001 069Ch                | 5005 069Ch                |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 500C F6A0h                | 5001 06A0h                | 5005 06A0h                |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 500C F6B0h                | 5001 06B0h                | 5005 06B0h                |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 500C F6B2h                | 5001 06B2h                | 5005 06B2h                |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 500C F6BAh                | 5001 06BAh                | 5005 06BAh                |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 500C F6BEh                | 5001 06BEh                | 5005 06BEh                |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 500C F6C4h                | 5001 06C4h                | 5005 06C4h                |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 500C F700h                | 5001 0700h                | 5005 0700h                |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 500C F704h                | 5001 0704h                | 5005 0704h                |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 500C F708h                | 5001 0708h                | 5005 0708h                |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>    | 500C F70Ch                | 5001 070Ch                | 5005 070Ch                |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>    | 500C F710h                | 5001 0710h                | 5005 0710h                |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>    | 500C F714h                | 5001 0714h                | 5005 0714h                |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>    | 500C F718h                | 5001 0718h                | 5005 0718h                |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>    | 500C F71Ch                | 5001 071Ch                | 5005 071Ch                |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>   | 500C F720h                | 5001 0720h                | 5005 0720h                |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a>  | 500C F730h                | 5001 0730h                | 5005 0730h                |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a>  | 500C F732h                | 5001 0732h                | 5005 0732h                |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>     | 500C F73Ah                | 5001 073Ah                | 5005 073Ah                |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>     | 500C F73Eh                | 5001 073Eh                | 5005 073Eh                |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a>  | 500C F744h                | 5001 0744h                | 5005 0744h                |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>    | 500C F780h                | 5001 0780h                | 5005 0780h                |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>    | 500C F784h                | 5001 0784h                | 5005 0784h                |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>    | 500C F788h                | 5001 0788h                | 5005 0788h                |

**Table 3-792. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM9_G1 Physical Address | EPWM0_G2 Physical Address | EPWM1_G2 Physical Address |
|--------|--------|------------------------------------|---------------------------|---------------------------|---------------------------|
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 500C F78Ch                | 5001 078Ch                | 5005 078Ch                |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 500C F790h                | 5001 0790h                | 5005 0790h                |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 500C F794h                | 5001 0794h                | 5005 0794h                |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 500C F798h                | 5001 0798h                | 5005 0798h                |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 500C F79Ch                | 5001 079Ch                | 5005 079Ch                |
| 7A0h   | 32     | <a href="#">EPWM_XTBRD_SHDW3</a>   | 500C F7A0h                | 5001 07A0h                | 5005 07A0h                |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 500C F7B0h                | 5001 07B0h                | 5005 07B0h                |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 500C F7B2h                | 5001 07B2h                | 5005 07B2h                |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 500C F7BAh                | 5001 07BAh                | 5005 07BAh                |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 500C F7BEh                | 5001 07BEh                | 5005 07BEh                |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 500C F7C4h                | 5001 07C4h                | 5005 07C4h                |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 500C F800h                | 5001 0800h                | 5005 0800h                |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 500C F804h                | 5001 0804h                | 5005 0804h                |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 500C F808h                | 5001 0808h                | 5005 0808h                |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 500C F80Ch                | 5001 080Ch                | 5005 080Ch                |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 500C F810h                | 5001 0810h                | 5005 0810h                |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 500C F814h                | 5001 0814h                | 5005 0814h                |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 500C F820h                | 5001 0820h                | 5005 0820h                |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 500C F824h                | 5001 0824h                | 5005 0824h                |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 500C F828h                | 5001 0828h                | 5005 0828h                |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 500C F82Ch                | 5001 082Ch                | 5005 082Ch                |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>     | 500C FC00h                | 5001 0C00h                | 5005 0C00h                |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 500C FC04h                | 5001 0C04h                | 5005 0C04h                |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 500C FC20h                | 5001 0C20h                | 5005 0C20h                |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 500C FC24h                | 5001 0C24h                | 5005 0C24h                |

**Table 3-793. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM10_G2 Physical Address | EPWM11_G2 Physical Address | EPWM12_G2 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5009 0000h                 | 500D 0000h                 | 5001 1000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5009 0002h                 | 500D 0002h                 | 5001 1002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5009 0006h                 | 500D 0006h                 | 5001 1006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5009 0008h                 | 500D 0008h                 | 5001 1008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5009 000Ah                 | 500D 000Ah                 | 5001 100Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 5009 000Ch                 | 500D 000Ch                 | 5001 100Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5009 000Eh                 | 500D 000Eh                 | 5001 100Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5009 0010h                 | 500D 0010h                 | 5001 1010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5009 0012h                 | 500D 0012h                 | 5001 1012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 5009 0018h                 | 500D 0018h                 | 5001 1018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 5009 001Ah                 | 500D 001Ah                 | 5001 101Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 5009 0020h                 | 500D 0020h                 | 5001 1020h                 |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 5009 0022h                 | 500D 0022h                 | 5001 1022h                 |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 5009 0028h                 | 500D 0028h                 | 5001 1028h                 |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 5009 0030h                 | 500D 0030h                 | 5001 1030h                 |

**Table 3-793. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                   | EPWM10_G2 Physical Address | EPWM11_G2 Physical Address | EPWM12_G2 Physical Address |
|--------|--------|---------------------------------|----------------------------|----------------------------|----------------------------|
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>    | 5009 0032h                 | 500D 0032h                 | 5001 1032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>     | 5009 0040h                 | 500D 0040h                 | 5001 1040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>    | 5009 004Eh                 | 500D 004Eh                 | 5001 104Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>     | 5009 005Ah                 | 500D 005Ah                 | 5001 105Ah                 |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>      | 5009 005Ch                 | 500D 005Ch                 | 5001 105Ch                 |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>     | 5009 0068h                 | 500D 0068h                 | 5001 1068h                 |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>     | 5009 006Ah                 | 500D 006Ah                 | 5001 106Ah                 |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>  | 5009 0070h                 | 500D 0070h                 | 5001 1070h                 |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a> | 5009 0074h                 | 500D 0074h                 | 5001 1074h                 |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>      | 5009 007Ah                 | 500D 007Ah                 | 5001 107Ah                 |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>    | 5009 007Ch                 | 500D 007Ch                 | 5001 107Ch                 |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>   | 5009 007Eh                 | 500D 007Eh                 | 5001 107Eh                 |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>     | 5009 0080h                 | 500D 0080h                 | 5001 1080h                 |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>    | 5009 0082h                 | 500D 0082h                 | 5001 1082h                 |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>     | 5009 0084h                 | 500D 0084h                 | 5001 1084h                 |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>    | 5009 0086h                 | 500D 0086h                 | 5001 1086h                 |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>     | 5009 008Eh                 | 500D 008Eh                 | 5001 108Eh                 |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>    | 5009 0092h                 | 500D 0092h                 | 5001 1092h                 |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>    | 5009 00A0h                 | 500D 00A0h                 | 5001 10A0h                 |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>      | 5009 00A2h                 | 500D 00A2h                 | 5001 10A2h                 |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>    | 5009 00A4h                 | 500D 00A4h                 | 5001 10A4h                 |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>      | 5009 00A6h                 | 500D 00A6h                 | 5001 10A6h                 |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>      | 5009 00C0h                 | 500D 00C0h                 | 5001 10C0h                 |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>    | 5009 00C4h                 | 500D 00C4h                 | 5001 10C4h                 |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>      | 5009 00C6h                 | 500D 00C6h                 | 5001 10C6h                 |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>   | 5009 00C8h                 | 500D 00C8h                 | 5001 10C8h                 |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>       | 5009 00D4h                 | 500D 00D4h                 | 5001 10D4h                 |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>       | 5009 00D8h                 | 500D 00D8h                 | 5001 10D8h                 |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>       | 5009 00DEh                 | 500D 00DEh                 | 5001 10DEh                 |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>       | 5009 00E2h                 | 500D 00E2h                 | 5001 10E2h                 |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>    | 5009 00E8h                 | 500D 00E8h                 | 5001 10E8h                 |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>  | 5009 00EEh                 | 500D 00EEh                 | 5001 10EEh                 |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>      | 5009 0100h                 | 500D 0100h                 | 5001 1100h                 |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>     | 5009 0102h                 | 500D 0102h                 | 5001 1102h                 |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>    | 5009 0104h                 | 500D 0104h                 | 5001 1104h                 |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>      | 5009 0108h                 | 500D 0108h                 | 5001 1108h                 |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>     | 5009 010Ah                 | 500D 010Ah                 | 5001 110Ah                 |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>   | 5009 010Ch                 | 500D 010Ch                 | 5001 110Ch                 |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>   | 5009 010Eh                 | 500D 010Eh                 | 5001 110Eh                 |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>     | 5009 011Ah                 | 500D 011Ah                 | 5001 111Ah                 |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>      | 5009 0126h                 | 500D 0126h                 | 5001 1126h                 |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>   | 5009 0128h                 | 500D 0128h                 | 5001 1128h                 |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>   | 5009 012Ah                 | 500D 012Ah                 | 5001 112Ah                 |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>      | 5009 012Eh                 | 500D 012Eh                 | 5001 112Eh                 |

**Table 3-793. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM10_G2 Physical Address | EPWM11_G2 Physical Address | EPWM12_G2 Physical Address |
|--------|--------|---------------------------------------|----------------------------|----------------------------|----------------------------|
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>         | 5009 0130h                 | 500D 0130h                 | 5001 1130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>         | 5009 0132h                 | 500D 0132h                 | 5001 1132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>            | 5009 0136h                 | 500D 0136h                 | 5001 1136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a>     | 5009 013Ah                 | 500D 013Ah                 | 5001 113Ah                 |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>            | 5009 0148h                 | 500D 0148h                 | 5001 1148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>             | 5009 014Ch                 | 500D 014Ch                 | 5001 114Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>            | 5009 0150h                 | 500D 0150h                 | 5001 1150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>            | 5009 0154h                 | 500D 0154h                 | 5001 1154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 5009 0158h                 | 500D 0158h                 | 5001 1158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 5009 015Ch                 | 500D 015Ch                 | 5001 115Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 5009 0160h                 | 500D 0160h                 | 5001 1160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 5009 0164h                 | 500D 0164h                 | 5001 1164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 5009 0168h                 | 500D 0168h                 | 5001 1168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 5009 016Ch                 | 500D 016Ch                 | 5001 116Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 5009 0170h                 | 500D 0170h                 | 5001 1170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 5009 0174h                 | 500D 0174h                 | 5001 1174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 5009 0180h                 | 500D 0180h                 | 5001 1180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 5009 0186h                 | 500D 0186h                 | 5001 1186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5009 0188h                 | 500D 0188h                 | 5001 1188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5009 018Eh                 | 500D 018Eh                 | 5001 118Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5009 0190h                 | 500D 0190h                 | 5001 1190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5009 0192h                 | 500D 0192h                 | 5001 1192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5009 0194h                 | 500D 0194h                 | 5001 1194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5009 0196h                 | 500D 0196h                 | 5001 1196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5009 0198h                 | 500D 0198h                 | 5001 1198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5009 019Ah                 | 500D 019Ah                 | 5001 119Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5009 019Ch                 | 500D 019Ch                 | 5001 119Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5009 019Eh                 | 500D 019Eh                 | 5001 119Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5009 01A4h                 | 500D 01A4h                 | 5001 11A4h                 |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5009 01A6h                 | 500D 01A6h                 | 5001 11A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 5009 01A8h                 | 500D 01A8h                 | 5001 11A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 5009 01AAh                 | 500D 01AAh                 | 5001 11AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 5009 01ACh                 | 500D 01ACh                 | 5001 11ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 5009 01AEh                 | 500D 01AEh                 | 5001 11AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 5009 01B0h                 | 500D 01B0h                 | 5001 11B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 5009 01B2h                 | 500D 01B2h                 | 5001 11B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 5009 01F4h                 | 500D 01F4h                 | 5001 11F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 5009 01FAh                 | 500D 01FAh                 | 5001 11FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 5009 01FCh                 | 500D 01FCh                 | 5001 11FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>         | 5009 0400h                 | 500D 0400h                 | 5001 1400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>         | 5009 0410h                 | 500D 0410h                 | 5001 1410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>            | 5009 0418h                 | 500D 0418h                 | 5001 1418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a>   | 5009 041Ch                 | 500D 041Ch                 | 5001 141Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>     | 5009 0420h                 | 500D 0420h                 | 5001 1420h                 |

**Table 3-793. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM10_G2 Physical Address | EPWM11_G2 Physical Address | EPWM12_G2 Physical Address |
|--------|--------|-------------------------------------|----------------------------|----------------------------|----------------------------|
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>   | 5009 0428h                 | 500D 0428h                 | 5001 1428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>   | 5009 0430h                 | 500D 0430h                 | 5001 1430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>   | 5009 0600h                 | 500D 0600h                 | 5001 1600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>   | 5009 0604h                 | 500D 0604h                 | 5001 1604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>   | 5009 0608h                 | 500D 0608h                 | 5001 1608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>   | 5009 060Ch                 | 500D 060Ch                 | 5001 160Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>   | 5009 0610h                 | 500D 0610h                 | 5001 1610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 5009 0614h                 | 500D 0614h                 | 5001 1614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 5009 0618h                 | 500D 0618h                 | 5001 1618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 5009 061Ch                 | 500D 061Ch                 | 5001 161Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 5009 0620h                 | 500D 0620h                 | 5001 1620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 5009 0630h                 | 500D 0630h                 | 5001 1630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 5009 0632h                 | 500D 0632h                 | 5001 1632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 5009 0644h                 | 500D 0644h                 | 5001 1644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 5009 0680h                 | 500D 0680h                 | 5001 1680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 5009 0684h                 | 500D 0684h                 | 5001 1684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 5009 0688h                 | 500D 0688h                 | 5001 1688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 5009 068Ch                 | 500D 068Ch                 | 5001 168Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 5009 0690h                 | 500D 0690h                 | 5001 1690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 5009 0694h                 | 500D 0694h                 | 5001 1694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 5009 0698h                 | 500D 0698h                 | 5001 1698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 5009 069Ch                 | 500D 069Ch                 | 5001 169Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 5009 06A0h                 | 500D 06A0h                 | 5001 16A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 5009 06B0h                 | 500D 06B0h                 | 5001 16B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 5009 06B2h                 | 500D 06B2h                 | 5001 16B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 5009 06BAh                 | 500D 06BAh                 | 5001 16BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 5009 06BEh                 | 500D 06BEh                 | 5001 16BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 5009 06C4h                 | 500D 06C4h                 | 5001 16C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 5009 0700h                 | 500D 0700h                 | 5001 1700h                 |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 5009 0704h                 | 500D 0704h                 | 5001 1704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 5009 0708h                 | 500D 0708h                 | 5001 1708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>    | 5009 070Ch                 | 500D 070Ch                 | 5001 170Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>    | 5009 0710h                 | 500D 0710h                 | 5001 1710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>    | 5009 0714h                 | 500D 0714h                 | 5001 1714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>    | 5009 0718h                 | 500D 0718h                 | 5001 1718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>    | 5009 071Ch                 | 500D 071Ch                 | 5001 171Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>   | 5009 0720h                 | 500D 0720h                 | 5001 1720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a>  | 5009 0730h                 | 500D 0730h                 | 5001 1730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a>  | 5009 0732h                 | 500D 0732h                 | 5001 1732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>     | 5009 073Ah                 | 500D 073Ah                 | 5001 173Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>     | 5009 073Eh                 | 500D 073Eh                 | 5001 173Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a>  | 5009 0744h                 | 500D 0744h                 | 5001 1744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>    | 5009 0780h                 | 500D 0780h                 | 5001 1780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>    | 5009 0784h                 | 500D 0784h                 | 5001 1784h                 |



**Table 3-793. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM10_G2 Physical Address | EPWM11_G2 Physical Address | EPWM12_G2 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 5009 0788h                 | 500D 0788h                 | 5001 1788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 5009 078Ch                 | 500D 078Ch                 | 5001 178Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 5009 0790h                 | 500D 0790h                 | 5001 1790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 5009 0794h                 | 500D 0794h                 | 5001 1794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 5009 0798h                 | 500D 0798h                 | 5001 1798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 5009 079Ch                 | 500D 079Ch                 | 5001 179Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 5009 07A0h                 | 500D 07A0h                 | 5001 17A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5009 07B0h                 | 500D 07B0h                 | 5001 17B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5009 07B2h                 | 500D 07B2h                 | 5001 17B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5009 07BAh                 | 500D 07BAh                 | 5001 17BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5009 07BEh                 | 500D 07BEh                 | 5001 17BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5009 07C4h                 | 500D 07C4h                 | 5001 17C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5009 0800h                 | 500D 0800h                 | 5001 1800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5009 0804h                 | 500D 0804h                 | 5001 1804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5009 0808h                 | 500D 0808h                 | 5001 1808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5009 080Ch                 | 500D 080Ch                 | 5001 180Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 5009 0810h                 | 500D 0810h                 | 5001 1810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5009 0814h                 | 500D 0814h                 | 5001 1814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 5009 0820h                 | 500D 0820h                 | 5001 1820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 5009 0824h                 | 500D 0824h                 | 5001 1824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 5009 0828h                 | 500D 0828h                 | 5001 1828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 5009 082Ch                 | 500D 082Ch                 | 5001 182Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFC</a>      | 5009 0C00h                 | 500D 0C00h                 | 5001 1C00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 5009 0C04h                 | 500D 0C04h                 | 5001 1C04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 5009 0C20h                 | 500D 0C20h                 | 5001 1C20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 5009 0C24h                 | 500D 0C24h                 | 5001 1C24h                 |

**Table 3-794. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM13_G2 Physical Address | EPWM14_G2 Physical Address | EPWM15_G2 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5005 1000h                 | 5009 1000h                 | 500D 1000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5005 1002h                 | 5009 1002h                 | 500D 1002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5005 1006h                 | 5009 1006h                 | 500D 1006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5005 1008h                 | 5009 1008h                 | 500D 1008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5005 100Ah                 | 5009 100Ah                 | 500D 100Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 5005 100Ch                 | 5009 100Ch                 | 500D 100Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5005 100Eh                 | 5009 100Eh                 | 500D 100Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5005 1010h                 | 5009 1010h                 | 500D 1010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5005 1012h                 | 5009 1012h                 | 500D 1012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 5005 1018h                 | 5009 1018h                 | 500D 1018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 5005 101Ah                 | 5009 101Ah                 | 500D 101Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 5005 1020h                 | 5009 1020h                 | 500D 1020h                 |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 5005 1022h                 | 5009 1022h                 | 500D 1022h                 |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 5005 1028h                 | 5009 1028h                 | 500D 1028h                 |



**Table 3-794. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                   | EPWM13_G2 Physical Address | EPWM14_G2 Physical Address | EPWM15_G2 Physical Address |
|--------|--------|---------------------------------|----------------------------|----------------------------|----------------------------|
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>    | 5005 1030h                 | 5009 1030h                 | 500D 1030h                 |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>    | 5005 1032h                 | 5009 1032h                 | 500D 1032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>     | 5005 1040h                 | 5009 1040h                 | 500D 1040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>    | 5005 104Eh                 | 5009 104Eh                 | 500D 104Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>     | 5005 105Ah                 | 5009 105Ah                 | 500D 105Ah                 |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>      | 5005 105Ch                 | 5009 105Ch                 | 500D 105Ch                 |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>     | 5005 1068h                 | 5009 1068h                 | 500D 1068h                 |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>     | 5005 106Ah                 | 5009 106Ah                 | 500D 106Ah                 |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>  | 5005 1070h                 | 5009 1070h                 | 500D 1070h                 |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a> | 5005 1074h                 | 5009 1074h                 | 500D 1074h                 |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>      | 5005 107Ah                 | 5009 107Ah                 | 500D 107Ah                 |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>    | 5005 107Ch                 | 5009 107Ch                 | 500D 107Ch                 |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>   | 5005 107Eh                 | 5009 107Eh                 | 500D 107Eh                 |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>     | 5005 1080h                 | 5009 1080h                 | 500D 1080h                 |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>    | 5005 1082h                 | 5009 1082h                 | 500D 1082h                 |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>     | 5005 1084h                 | 5009 1084h                 | 500D 1084h                 |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>    | 5005 1086h                 | 5009 1086h                 | 500D 1086h                 |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>     | 5005 108Eh                 | 5009 108Eh                 | 500D 108Eh                 |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>    | 5005 1092h                 | 5009 1092h                 | 500D 1092h                 |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>    | 5005 10A0h                 | 5009 10A0h                 | 500D 10A0h                 |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>      | 5005 10A2h                 | 5009 10A2h                 | 500D 10A2h                 |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>    | 5005 10A4h                 | 5009 10A4h                 | 500D 10A4h                 |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>      | 5005 10A6h                 | 5009 10A6h                 | 500D 10A6h                 |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>      | 5005 10C0h                 | 5009 10C0h                 | 500D 10C0h                 |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>    | 5005 10C4h                 | 5009 10C4h                 | 500D 10C4h                 |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>      | 5005 10C6h                 | 5009 10C6h                 | 500D 10C6h                 |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>   | 5005 10C8h                 | 5009 10C8h                 | 500D 10C8h                 |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>       | 5005 10D4h                 | 5009 10D4h                 | 500D 10D4h                 |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>       | 5005 10D8h                 | 5009 10D8h                 | 500D 10D8h                 |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>       | 5005 10DEh                 | 5009 10DEh                 | 500D 10DEh                 |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>       | 5005 10E2h                 | 5009 10E2h                 | 500D 10E2h                 |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>    | 5005 10E8h                 | 5009 10E8h                 | 500D 10E8h                 |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>  | 5005 10EEh                 | 5009 10EEh                 | 500D 10EEh                 |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>      | 5005 1100h                 | 5009 1100h                 | 500D 1100h                 |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>     | 5005 1102h                 | 5009 1102h                 | 500D 1102h                 |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>    | 5005 1104h                 | 5009 1104h                 | 500D 1104h                 |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>      | 5005 1108h                 | 5009 1108h                 | 500D 1108h                 |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>     | 5005 110Ah                 | 5009 110Ah                 | 500D 110Ah                 |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>   | 5005 110Ch                 | 5009 110Ch                 | 500D 110Ch                 |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>   | 5005 110Eh                 | 5009 110Eh                 | 500D 110Eh                 |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>     | 5005 111Ah                 | 5009 111Ah                 | 500D 111Ah                 |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>      | 5005 1126h                 | 5009 1126h                 | 500D 1126h                 |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>   | 5005 1128h                 | 5009 1128h                 | 500D 1128h                 |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>   | 5005 112Ah                 | 5009 112Ah                 | 500D 112Ah                 |

**Table 3-794. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM13_G2 Physical Address | EPWM14_G2 Physical Address | EPWM15_G2 Physical Address |
|--------|--------|---------------------------------------|----------------------------|----------------------------|----------------------------|
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>            | 5005 112Eh                 | 5009 112Eh                 | 500D 112Eh                 |
| 130h   | 16     | <a href="#">EPWM_TZCBCLR</a>          | 5005 1130h                 | 5009 1130h                 | 500D 1130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>         | 5005 1132h                 | 5009 1132h                 | 500D 1132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRFC</a>           | 5005 1136h                 | 5009 1136h                 | 500D 1136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a>     | 5005 113Ah                 | 5009 113Ah                 | 500D 113Ah                 |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>            | 5005 1148h                 | 5009 1148h                 | 500D 1148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>             | 5005 114Ch                 | 5009 114Ch                 | 500D 114Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>            | 5005 1150h                 | 5009 1150h                 | 500D 1150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>            | 5005 1154h                 | 5009 1154h                 | 500D 1154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 5005 1158h                 | 5009 1158h                 | 500D 1158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 5005 115Ch                 | 5009 115Ch                 | 500D 115Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 5005 1160h                 | 5009 1160h                 | 500D 1160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 5005 1164h                 | 5009 1164h                 | 500D 1164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 5005 1168h                 | 5009 1168h                 | 500D 1168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 5005 116Ch                 | 5009 116Ch                 | 500D 116Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 5005 1170h                 | 5009 1170h                 | 500D 1170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 5005 1174h                 | 5009 1174h                 | 500D 1174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRISEL</a>         | 5005 1180h                 | 5009 1180h                 | 500D 1180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 5005 1186h                 | 5009 1186h                 | 500D 1186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5005 1188h                 | 5009 1188h                 | 500D 1188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5005 118Eh                 | 5009 118Eh                 | 500D 118Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5005 1190h                 | 5009 1190h                 | 500D 1190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5005 1192h                 | 5009 1192h                 | 500D 1192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5005 1194h                 | 5009 1194h                 | 500D 1194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5005 1196h                 | 5009 1196h                 | 500D 1196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5005 1198h                 | 5009 1198h                 | 500D 1198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5005 119Ah                 | 5009 119Ah                 | 500D 119Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5005 119Ch                 | 5009 119Ch                 | 500D 119Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5005 119Eh                 | 5009 119Eh                 | 500D 119Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5005 11A4h                 | 5009 11A4h                 | 500D 11A4h                 |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5005 11A6h                 | 5009 11A6h                 | 500D 11A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 5005 11A8h                 | 5009 11A8h                 | 500D 11A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 5005 11AAh                 | 5009 11AAh                 | 500D 11AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 5005 11ACh                 | 5009 11ACh                 | 500D 11ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 5005 11AEh                 | 5009 11AEh                 | 500D 11AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 5005 11B0h                 | 5009 11B0h                 | 500D 11B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 5005 11B2h                 | 5009 11B2h                 | 500D 11B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 5005 11F4h                 | 5009 11F4h                 | 500D 11F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 5005 11FAh                 | 5009 11FAh                 | 500D 11FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 5005 11FCh                 | 5009 11FCh                 | 500D 11FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>         | 5005 1400h                 | 5009 1400h                 | 500D 1400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>         | 5005 1410h                 | 5009 1410h                 | 500D 1410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>            | 5005 1418h                 | 5009 1418h                 | 500D 1418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a>   | 5005 141Ch                 | 5009 141Ch                 | 500D 141Ch                 |

**Table 3-794. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM13_G2 Physical Address | EPWM14_G2 Physical Address | EPWM15_G2 Physical Address |
|--------|--------|-------------------------------------|----------------------------|----------------------------|----------------------------|
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>   | 5005 1420h                 | 5009 1420h                 | 500D 1420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>   | 5005 1428h                 | 5009 1428h                 | 500D 1428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>   | 5005 1430h                 | 5009 1430h                 | 500D 1430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>   | 5005 1600h                 | 5009 1600h                 | 500D 1600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>   | 5005 1604h                 | 5009 1604h                 | 500D 1604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>   | 5005 1608h                 | 5009 1608h                 | 500D 1608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>   | 5005 160Ch                 | 5009 160Ch                 | 500D 160Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>   | 5005 1610h                 | 5009 1610h                 | 500D 1610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 5005 1614h                 | 5009 1614h                 | 500D 1614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 5005 1618h                 | 5009 1618h                 | 500D 1618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 5005 161Ch                 | 5009 161Ch                 | 500D 161Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 5005 1620h                 | 5009 1620h                 | 500D 1620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 5005 1630h                 | 5009 1630h                 | 500D 1630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 5005 1632h                 | 5009 1632h                 | 500D 1632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 5005 1644h                 | 5009 1644h                 | 500D 1644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 5005 1680h                 | 5009 1680h                 | 500D 1680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 5005 1684h                 | 5009 1684h                 | 500D 1684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 5005 1688h                 | 5009 1688h                 | 500D 1688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 5005 168Ch                 | 5009 168Ch                 | 500D 168Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 5005 1690h                 | 5009 1690h                 | 500D 1690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 5005 1694h                 | 5009 1694h                 | 500D 1694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 5005 1698h                 | 5009 1698h                 | 500D 1698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 5005 169Ch                 | 5009 169Ch                 | 500D 169Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 5005 16A0h                 | 5009 16A0h                 | 500D 16A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 5005 16B0h                 | 5009 16B0h                 | 500D 16B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 5005 16B2h                 | 5009 16B2h                 | 500D 16B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 5005 16BAh                 | 5009 16BAh                 | 500D 16BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 5005 16BEh                 | 5009 16BEh                 | 500D 16BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 5005 16C4h                 | 5009 16C4h                 | 500D 16C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 5005 1700h                 | 5009 1700h                 | 500D 1700h                 |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 5005 1704h                 | 5009 1704h                 | 500D 1704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 5005 1708h                 | 5009 1708h                 | 500D 1708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>    | 5005 170Ch                 | 5009 170Ch                 | 500D 170Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>    | 5005 1710h                 | 5009 1710h                 | 500D 1710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>    | 5005 1714h                 | 5009 1714h                 | 500D 1714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>    | 5005 1718h                 | 5009 1718h                 | 500D 1718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>    | 5005 171Ch                 | 5009 171Ch                 | 500D 171Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>   | 5005 1720h                 | 5009 1720h                 | 500D 1720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a>  | 5005 1730h                 | 5009 1730h                 | 500D 1730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a>  | 5005 1732h                 | 5009 1732h                 | 500D 1732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>     | 5005 173Ah                 | 5009 173Ah                 | 500D 173Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>     | 5005 173Eh                 | 5009 173Eh                 | 500D 173Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a>  | 5005 1744h                 | 5009 1744h                 | 500D 1744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>    | 5005 1780h                 | 5009 1780h                 | 500D 1780h                 |

**Table 3-794. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM13_G2 Physical Address | EPWM14_G2 Physical Address | EPWM15_G2 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 5005 1784h                 | 5009 1784h                 | 500D 1784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 5005 1788h                 | 5009 1788h                 | 500D 1788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 5005 178Ch                 | 5009 178Ch                 | 500D 178Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 5005 1790h                 | 5009 1790h                 | 500D 1790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 5005 1794h                 | 5009 1794h                 | 500D 1794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 5005 1798h                 | 5009 1798h                 | 500D 1798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 5005 179Ch                 | 5009 179Ch                 | 500D 179Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBRD_SHDW3</a>   | 5005 17A0h                 | 5009 17A0h                 | 500D 17A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5005 17B0h                 | 5009 17B0h                 | 500D 17B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5005 17B2h                 | 5009 17B2h                 | 500D 17B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5005 17BAh                 | 5009 17BAh                 | 500D 17BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5005 17BEh                 | 5009 17BEh                 | 500D 17BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5005 17C4h                 | 5009 17C4h                 | 500D 17C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5005 1800h                 | 5009 1800h                 | 500D 1800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5005 1804h                 | 5009 1804h                 | 500D 1804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5005 1808h                 | 5009 1808h                 | 500D 1808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5005 180Ch                 | 5009 180Ch                 | 500D 180Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 5005 1810h                 | 5009 1810h                 | 500D 1810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5005 1814h                 | 5009 1814h                 | 500D 1814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 5005 1820h                 | 5009 1820h                 | 500D 1820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 5005 1824h                 | 5009 1824h                 | 500D 1824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 5005 1828h                 | 5009 1828h                 | 500D 1828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 5005 182Ch                 | 5009 182Ch                 | 500D 182Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>     | 5005 1C00h                 | 5009 1C00h                 | 500D 1C00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 5005 1C04h                 | 5009 1C04h                 | 500D 1C04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 5005 1C20h                 | 5009 1C20h                 | 500D 1C20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 5005 1C24h                 | 5009 1C24h                 | 500D 1C24h                 |

**Table 3-795. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM16_G2 Physical Address | EPWM17_G2 Physical Address | EPWM18_G2 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5001 2000h                 | 5005 2000h                 | 5009 2000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5001 2002h                 | 5005 2002h                 | 5009 2002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5001 2006h                 | 5005 2006h                 | 5009 2006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5001 2008h                 | 5005 2008h                 | 5009 2008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5001 200Ah                 | 5005 200Ah                 | 5009 200Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUEN</a>  | 5001 200Ch                 | 5005 200Ch                 | 5009 200Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5001 200Eh                 | 5005 200Eh                 | 5009 200Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5001 2010h                 | 5005 2010h                 | 5009 2010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5001 2012h                 | 5005 2012h                 | 5009 2012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 5001 2018h                 | 5005 2018h                 | 5009 2018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 5001 201Ah                 | 5005 201Ah                 | 5009 201Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 5001 2020h                 | 5005 2020h                 | 5009 2020h                 |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 5001 2022h                 | 5005 2022h                 | 5009 2022h                 |

**Table 3-795. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                   | EPWM16_G2 Physical Address | EPWM17_G2 Physical Address | EPWM18_G2 Physical Address |
|--------|--------|---------------------------------|----------------------------|----------------------------|----------------------------|
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>      | 5001 2028h                 | 5005 2028h                 | 5009 2028h                 |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>    | 5001 2030h                 | 5005 2030h                 | 5009 2030h                 |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>    | 5001 2032h                 | 5005 2032h                 | 5009 2032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>     | 5001 2040h                 | 5005 2040h                 | 5009 2040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>    | 5001 204Eh                 | 5005 204Eh                 | 5009 204Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>     | 5001 205Ah                 | 5005 205Ah                 | 5009 205Ah                 |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>      | 5001 205Ch                 | 5005 205Ch                 | 5009 205Ch                 |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>     | 5001 2068h                 | 5005 2068h                 | 5009 2068h                 |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>     | 5001 206Ah                 | 5005 206Ah                 | 5009 206Ah                 |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>  | 5001 2070h                 | 5005 2070h                 | 5009 2070h                 |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a> | 5001 2074h                 | 5005 2074h                 | 5009 2074h                 |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>      | 5001 207Ah                 | 5005 207Ah                 | 5009 207Ah                 |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>    | 5001 207Ch                 | 5005 207Ch                 | 5009 207Ch                 |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>   | 5001 207Eh                 | 5005 207Eh                 | 5009 207Eh                 |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>     | 5001 2080h                 | 5005 2080h                 | 5009 2080h                 |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>    | 5001 2082h                 | 5005 2082h                 | 5009 2082h                 |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>     | 5001 2084h                 | 5005 2084h                 | 5009 2084h                 |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>    | 5001 2086h                 | 5005 2086h                 | 5009 2086h                 |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>     | 5001 208Eh                 | 5005 208Eh                 | 5009 208Eh                 |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>    | 5001 2092h                 | 5005 2092h                 | 5009 2092h                 |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>    | 5001 20A0h                 | 5005 20A0h                 | 5009 20A0h                 |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>      | 5001 20A2h                 | 5005 20A2h                 | 5009 20A2h                 |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>    | 5001 20A4h                 | 5005 20A4h                 | 5009 20A4h                 |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>      | 5001 20A6h                 | 5005 20A6h                 | 5009 20A6h                 |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>      | 5001 20C0h                 | 5005 20C0h                 | 5009 20C0h                 |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>    | 5001 20C4h                 | 5005 20C4h                 | 5009 20C4h                 |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>      | 5001 20C6h                 | 5005 20C6h                 | 5009 20C6h                 |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>   | 5001 20C8h                 | 5005 20C8h                 | 5009 20C8h                 |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>       | 5001 20D4h                 | 5005 20D4h                 | 5009 20D4h                 |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>       | 5001 20D8h                 | 5005 20D8h                 | 5009 20D8h                 |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>       | 5001 20DEh                 | 5005 20DEh                 | 5009 20DEh                 |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>       | 5001 20E2h                 | 5005 20E2h                 | 5009 20E2h                 |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>    | 5001 20E8h                 | 5005 20E8h                 | 5009 20E8h                 |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>  | 5001 20EEh                 | 5005 20EEh                 | 5009 20EEh                 |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>      | 5001 2100h                 | 5005 2100h                 | 5009 2100h                 |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>     | 5001 2102h                 | 5005 2102h                 | 5009 2102h                 |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>    | 5001 2104h                 | 5005 2104h                 | 5009 2104h                 |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>      | 5001 2108h                 | 5005 2108h                 | 5009 2108h                 |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>     | 5001 210Ah                 | 5005 210Ah                 | 5009 210Ah                 |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>   | 5001 210Ch                 | 5005 210Ch                 | 5009 210Ch                 |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>   | 5001 210Eh                 | 5005 210Eh                 | 5009 210Eh                 |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>     | 5001 211Ah                 | 5005 211Ah                 | 5009 211Ah                 |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>      | 5001 2126h                 | 5005 2126h                 | 5009 2126h                 |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>   | 5001 2128h                 | 5005 2128h                 | 5009 2128h                 |

**Table 3-795. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM16_G2 Physical Address | EPWM17_G2 Physical Address | EPWM18_G2 Physical Address |
|--------|--------|---------------------------------------|----------------------------|----------------------------|----------------------------|
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>         | 5001 212Ah                 | 5005 212Ah                 | 5009 212Ah                 |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>            | 5001 212Eh                 | 5005 212Eh                 | 5009 212Eh                 |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>         | 5001 2130h                 | 5005 2130h                 | 5009 2130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>         | 5001 2132h                 | 5005 2132h                 | 5009 2132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>            | 5001 2136h                 | 5005 2136h                 | 5009 2136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a>     | 5001 213Ah                 | 5005 213Ah                 | 5009 213Ah                 |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>            | 5001 2148h                 | 5005 2148h                 | 5009 2148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>             | 5001 214Ch                 | 5005 214Ch                 | 5009 214Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>            | 5001 2150h                 | 5005 2150h                 | 5009 2150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>            | 5001 2154h                 | 5005 2154h                 | 5009 2154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 5001 2158h                 | 5005 2158h                 | 5009 2158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 5001 215Ch                 | 5005 215Ch                 | 5009 215Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 5001 2160h                 | 5005 2160h                 | 5009 2160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 5001 2164h                 | 5005 2164h                 | 5009 2164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 5001 2168h                 | 5005 2168h                 | 5009 2168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 5001 216Ch                 | 5005 216Ch                 | 5009 216Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 5001 2170h                 | 5005 2170h                 | 5009 2170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 5001 2174h                 | 5005 2174h                 | 5009 2174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 5001 2180h                 | 5005 2180h                 | 5009 2180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 5001 2186h                 | 5005 2186h                 | 5009 2186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5001 2188h                 | 5005 2188h                 | 5009 2188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5001 218Eh                 | 5005 218Eh                 | 5009 218Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5001 2190h                 | 5005 2190h                 | 5009 2190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5001 2192h                 | 5005 2192h                 | 5009 2192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5001 2194h                 | 5005 2194h                 | 5009 2194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5001 2196h                 | 5005 2196h                 | 5009 2196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5001 2198h                 | 5005 2198h                 | 5009 2198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5001 219Ah                 | 5005 219Ah                 | 5009 219Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5001 219Ch                 | 5005 219Ch                 | 5009 219Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5001 219Eh                 | 5005 219Eh                 | 5009 219Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5001 21A4h                 | 5005 21A4h                 | 5009 21A4h                 |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5001 21A6h                 | 5005 21A6h                 | 5009 21A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 5001 21A8h                 | 5005 21A8h                 | 5009 21A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 5001 21AAh                 | 5005 21AAh                 | 5009 21AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 5001 21ACh                 | 5005 21ACh                 | 5009 21ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 5001 21AEh                 | 5005 21AEh                 | 5009 21AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 5001 21B0h                 | 5005 21B0h                 | 5009 21B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 5001 21B2h                 | 5005 21B2h                 | 5009 21B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 5001 21F4h                 | 5005 21F4h                 | 5009 21F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 5001 21FAh                 | 5005 21FAh                 | 5009 21FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 5001 21FCh                 | 5005 21FCh                 | 5009 21FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>         | 5001 2400h                 | 5005 2400h                 | 5009 2400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>         | 5001 2410h                 | 5005 2410h                 | 5009 2410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>            | 5001 2418h                 | 5005 2418h                 | 5009 2418h                 |

**Table 3-795. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM16_G2 Physical Address | EPWM17_G2 Physical Address | EPWM18_G2 Physical Address |
|--------|--------|-------------------------------------|----------------------------|----------------------------|----------------------------|
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a> | 5001 241Ch                 | 5005 241Ch                 | 5009 241Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>   | 5001 2420h                 | 5005 2420h                 | 5009 2420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>   | 5001 2428h                 | 5005 2428h                 | 5009 2428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>   | 5001 2430h                 | 5005 2430h                 | 5009 2430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>   | 5001 2600h                 | 5005 2600h                 | 5009 2600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>   | 5001 2604h                 | 5005 2604h                 | 5009 2604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>   | 5001 2608h                 | 5005 2608h                 | 5009 2608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>   | 5001 260Ch                 | 5005 260Ch                 | 5009 260Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>   | 5001 2610h                 | 5005 2610h                 | 5009 2610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 5001 2614h                 | 5005 2614h                 | 5009 2614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 5001 2618h                 | 5005 2618h                 | 5009 2618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 5001 261Ch                 | 5005 261Ch                 | 5009 261Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 5001 2620h                 | 5005 2620h                 | 5009 2620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 5001 2630h                 | 5005 2630h                 | 5009 2630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 5001 2632h                 | 5005 2632h                 | 5009 2632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 5001 2644h                 | 5005 2644h                 | 5009 2644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 5001 2680h                 | 5005 2680h                 | 5009 2680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 5001 2684h                 | 5005 2684h                 | 5009 2684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 5001 2688h                 | 5005 2688h                 | 5009 2688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 5001 268Ch                 | 5005 268Ch                 | 5009 268Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 5001 2690h                 | 5005 2690h                 | 5009 2690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 5001 2694h                 | 5005 2694h                 | 5009 2694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 5001 2698h                 | 5005 2698h                 | 5009 2698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 5001 269Ch                 | 5005 269Ch                 | 5009 269Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 5001 26A0h                 | 5005 26A0h                 | 5009 26A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 5001 26B0h                 | 5005 26B0h                 | 5009 26B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 5001 26B2h                 | 5005 26B2h                 | 5009 26B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 5001 26BAh                 | 5005 26BAh                 | 5009 26BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 5001 26BEh                 | 5005 26BEh                 | 5009 26BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 5001 26C4h                 | 5005 26C4h                 | 5009 26C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 5001 2700h                 | 5005 2700h                 | 5009 2700h                 |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 5001 2704h                 | 5005 2704h                 | 5009 2704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 5001 2708h                 | 5005 2708h                 | 5009 2708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>    | 5001 270Ch                 | 5005 270Ch                 | 5009 270Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>    | 5001 2710h                 | 5005 2710h                 | 5009 2710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>    | 5001 2714h                 | 5005 2714h                 | 5009 2714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>    | 5001 2718h                 | 5005 2718h                 | 5009 2718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>    | 5001 271Ch                 | 5005 271Ch                 | 5009 271Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>   | 5001 2720h                 | 5005 2720h                 | 5009 2720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a>  | 5001 2730h                 | 5005 2730h                 | 5009 2730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a>  | 5001 2732h                 | 5005 2732h                 | 5009 2732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>     | 5001 273Ah                 | 5005 273Ah                 | 5009 273Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>     | 5001 273Eh                 | 5005 273Eh                 | 5009 273Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a>  | 5001 2744h                 | 5005 2744h                 | 5009 2744h                 |



**Table 3-795. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM16_G2 Physical Address | EPWM17_G2 Physical Address | EPWM18_G2 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 5001 2780h                 | 5005 2780h                 | 5009 2780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 5001 2784h                 | 5005 2784h                 | 5009 2784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 5001 2788h                 | 5005 2788h                 | 5009 2788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 5001 278Ch                 | 5005 278Ch                 | 5009 278Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 5001 2790h                 | 5005 2790h                 | 5009 2790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 5001 2794h                 | 5005 2794h                 | 5009 2794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 5001 2798h                 | 5005 2798h                 | 5009 2798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 5001 279Ch                 | 5005 279Ch                 | 5009 279Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBRD_SHDW3</a>   | 5001 27A0h                 | 5005 27A0h                 | 5009 27A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5001 27B0h                 | 5005 27B0h                 | 5009 27B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5001 27B2h                 | 5005 27B2h                 | 5009 27B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5001 27BAh                 | 5005 27BAh                 | 5009 27BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5001 27BEh                 | 5005 27BEh                 | 5009 27BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5001 27C4h                 | 5005 27C4h                 | 5009 27C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5001 2800h                 | 5005 2800h                 | 5009 2800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5001 2804h                 | 5005 2804h                 | 5009 2804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5001 2808h                 | 5005 2808h                 | 5009 2808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5001 280Ch                 | 5005 280Ch                 | 5009 280Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 5001 2810h                 | 5005 2810h                 | 5009 2810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5001 2814h                 | 5005 2814h                 | 5009 2814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 5001 2820h                 | 5005 2820h                 | 5009 2820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 5001 2824h                 | 5005 2824h                 | 5009 2824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 5001 2828h                 | 5005 2828h                 | 5009 2828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 5001 282Ch                 | 5005 282Ch                 | 5009 282Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>     | 5001 2C00h                 | 5005 2C00h                 | 5009 2C00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 5001 2C04h                 | 5005 2C04h                 | 5009 2C04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 5001 2C20h                 | 5005 2C20h                 | 5009 2C20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 5001 2C24h                 | 5005 2C24h                 | 5009 2C24h                 |

**Table 3-796. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM19_G2 Physical Address | EPWM20_G2 Physical Address | EPWM21_G2 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 500D 2000h                 | 5001 3000h                 | 5005 3000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 500D 2002h                 | 5001 3002h                 | 5005 3002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 500D 2006h                 | 5001 3006h                 | 5005 3006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 500D 2008h                 | 5001 3008h                 | 5005 3008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 500D 200Ah                 | 5001 300Ah                 | 5005 300Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 500D 200Ch                 | 5001 300Ch                 | 5005 300Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 500D 200Eh                 | 5001 300Eh                 | 5005 300Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 500D 2010h                 | 5001 3010h                 | 5005 3010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 500D 2012h                 | 5001 3012h                 | 5005 3012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 500D 2018h                 | 5001 3018h                 | 5005 3018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 500D 201Ah                 | 5001 301Ah                 | 5005 301Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 500D 2020h                 | 5001 3020h                 | 5005 3020h                 |



**Table 3-796. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                   | EPWM19_G2 Physical Address | EPWM2_G2 Physical Address | EPWM20_G2 Physical Address |
|--------|--------|---------------------------------|----------------------------|---------------------------|----------------------------|
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>  | 500D 2022h                 | 5001 3022h                | 5005 3022h                 |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>      | 500D 2028h                 | 5001 3028h                | 5005 3028h                 |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>    | 500D 2030h                 | 5001 3030h                | 5005 3030h                 |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>    | 500D 2032h                 | 5001 3032h                | 5005 3032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>     | 500D 2040h                 | 5001 3040h                | 5005 3040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>    | 500D 204Eh                 | 5001 304Eh                | 5005 304Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>     | 500D 205Ah                 | 5001 305Ah                | 5005 305Ah                 |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>      | 500D 205Ch                 | 5001 305Ch                | 5005 305Ch                 |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>     | 500D 2068h                 | 5001 3068h                | 5005 3068h                 |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>     | 500D 206Ah                 | 5001 306Ah                | 5005 306Ah                 |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>  | 500D 2070h                 | 5001 3070h                | 5005 3070h                 |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a> | 500D 2074h                 | 5001 3074h                | 5005 3074h                 |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>      | 500D 207Ah                 | 5001 307Ah                | 5005 307Ah                 |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>    | 500D 207Ch                 | 5001 307Ch                | 5005 307Ch                 |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>   | 500D 207Eh                 | 5001 307Eh                | 5005 307Eh                 |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>     | 500D 2080h                 | 5001 3080h                | 5005 3080h                 |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>    | 500D 2082h                 | 5001 3082h                | 5005 3082h                 |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>     | 500D 2084h                 | 5001 3084h                | 5005 3084h                 |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>    | 500D 2086h                 | 5001 3086h                | 5005 3086h                 |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>     | 500D 208Eh                 | 5001 308Eh                | 5005 308Eh                 |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>    | 500D 2092h                 | 5001 3092h                | 5005 3092h                 |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>    | 500D 20A0h                 | 5001 30A0h                | 5005 30A0h                 |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>      | 500D 20A2h                 | 5001 30A2h                | 5005 30A2h                 |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>    | 500D 20A4h                 | 5001 30A4h                | 5005 30A4h                 |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>      | 500D 20A6h                 | 5001 30A6h                | 5005 30A6h                 |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>      | 500D 20C0h                 | 5001 30C0h                | 5005 30C0h                 |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>    | 500D 20C4h                 | 5001 30C4h                | 5005 30C4h                 |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>      | 500D 20C6h                 | 5001 30C6h                | 5005 30C6h                 |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>   | 500D 20C8h                 | 5001 30C8h                | 5005 30C8h                 |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>       | 500D 20D4h                 | 5001 30D4h                | 5005 30D4h                 |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>       | 500D 20D8h                 | 5001 30D8h                | 5005 30D8h                 |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>       | 500D 20DEh                 | 5001 30DEh                | 5005 30DEh                 |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>       | 500D 20E2h                 | 5001 30E2h                | 5005 30E2h                 |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>    | 500D 20E8h                 | 5001 30E8h                | 5005 30E8h                 |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>  | 500D 20EEh                 | 5001 30EEh                | 5005 30EEh                 |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>      | 500D 2100h                 | 5001 3100h                | 5005 3100h                 |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>     | 500D 2102h                 | 5001 3102h                | 5005 3102h                 |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>    | 500D 2104h                 | 5001 3104h                | 5005 3104h                 |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>      | 500D 2108h                 | 5001 3108h                | 5005 3108h                 |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>     | 500D 210Ah                 | 5001 310Ah                | 5005 310Ah                 |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>   | 500D 210Ch                 | 5001 310Ch                | 5005 310Ch                 |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>   | 500D 210Eh                 | 5001 310Eh                | 5005 310Eh                 |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>     | 500D 211Ah                 | 5001 311Ah                | 5005 311Ah                 |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>      | 500D 2126h                 | 5001 3126h                | 5005 3126h                 |

**Table 3-796. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM19_G2 Physical Address | EPWM2_G2 Physical Address | EPWM20_G2 Physical Address |
|--------|--------|---------------------------------------|----------------------------|---------------------------|----------------------------|
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>         | 500D 2128h                 | 5001 3128h                | 5005 3128h                 |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>         | 500D 212Ah                 | 5001 312Ah                | 5005 312Ah                 |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>            | 500D 212Eh                 | 5001 312Eh                | 5005 312Eh                 |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>         | 500D 2130h                 | 5001 3130h                | 5005 3130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>         | 500D 2132h                 | 5001 3132h                | 5005 3132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>            | 500D 2136h                 | 5001 3136h                | 5005 3136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a>     | 500D 213Ah                 | 5001 313Ah                | 5005 313Ah                 |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>            | 500D 2148h                 | 5001 3148h                | 5005 3148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>             | 500D 214Ch                 | 5001 314Ch                | 5005 314Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>            | 500D 2150h                 | 5001 3150h                | 5005 3150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>            | 500D 2154h                 | 5001 3154h                | 5005 3154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 500D 2158h                 | 5001 3158h                | 5005 3158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 500D 215Ch                 | 5001 315Ch                | 5005 315Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 500D 2160h                 | 5001 3160h                | 5005 3160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 500D 2164h                 | 5001 3164h                | 5005 3164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 500D 2168h                 | 5001 3168h                | 5005 3168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 500D 216Ch                 | 5001 316Ch                | 5005 316Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 500D 2170h                 | 5001 3170h                | 5005 3170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 500D 2174h                 | 5001 3174h                | 5005 3174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRISEL</a>         | 500D 2180h                 | 5001 3180h                | 5005 3180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 500D 2186h                 | 5001 3186h                | 5005 3186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 500D 2188h                 | 5001 3188h                | 5005 3188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 500D 218Eh                 | 5001 318Eh                | 5005 318Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 500D 2190h                 | 5001 3190h                | 5005 3190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 500D 2192h                 | 5001 3192h                | 5005 3192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 500D 2194h                 | 5001 3194h                | 5005 3194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 500D 2196h                 | 5001 3196h                | 5005 3196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 500D 2198h                 | 5001 3198h                | 5005 3198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 500D 219Ah                 | 5001 319Ah                | 5005 319Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 500D 219Ch                 | 5001 319Ch                | 5005 319Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 500D 219Eh                 | 5001 319Eh                | 5005 319Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 500D 21A4h                 | 5001 31A4h                | 5005 31A4h                 |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 500D 21A6h                 | 5001 31A6h                | 5005 31A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 500D 21A8h                 | 5001 31A8h                | 5005 31A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 500D 21AAh                 | 5001 31AAh                | 5005 31AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 500D 21ACh                 | 5001 31ACh                | 5005 31ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 500D 21AEh                 | 5001 31AEh                | 5005 31AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 500D 21B0h                 | 5001 31B0h                | 5005 31B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 500D 21B2h                 | 5001 31B2h                | 5005 31B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 500D 21F4h                 | 5001 31F4h                | 5005 31F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 500D 21FAh                 | 5001 31FAh                | 5005 31FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 500D 21FCh                 | 5001 31FCh                | 5005 31FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>         | 500D 2400h                 | 5001 3400h                | 5005 3400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>         | 500D 2410h                 | 5001 3410h                | 5005 3410h                 |

**Table 3-796. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM19_G2 Physical Address | EPWM2_G2 Physical Address | EPWM20_G2 Physical Address |
|--------|--------|-------------------------------------|----------------------------|---------------------------|----------------------------|
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>          | 500D 2418h                 | 5001 3418h                | 5005 3418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a> | 500D 241Ch                 | 5001 341Ch                | 5005 341Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>   | 500D 2420h                 | 5001 3420h                | 5005 3420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>   | 500D 2428h                 | 5001 3428h                | 5005 3428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>   | 500D 2430h                 | 5001 3430h                | 5005 3430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>   | 500D 2600h                 | 5001 3600h                | 5005 3600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>   | 500D 2604h                 | 5001 3604h                | 5005 3604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>   | 500D 2608h                 | 5001 3608h                | 5005 3608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>   | 500D 260Ch                 | 5001 360Ch                | 5005 360Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>   | 500D 2610h                 | 5001 3610h                | 5005 3610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 500D 2614h                 | 5001 3614h                | 5005 3614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 500D 2618h                 | 5001 3618h                | 5005 3618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 500D 261Ch                 | 5001 361Ch                | 5005 361Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 500D 2620h                 | 5001 3620h                | 5005 3620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 500D 2630h                 | 5001 3630h                | 5005 3630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 500D 2632h                 | 5001 3632h                | 5005 3632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 500D 2644h                 | 5001 3644h                | 5005 3644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 500D 2680h                 | 5001 3680h                | 5005 3680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 500D 2684h                 | 5001 3684h                | 5005 3684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 500D 2688h                 | 5001 3688h                | 5005 3688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 500D 268Ch                 | 5001 368Ch                | 5005 368Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 500D 2690h                 | 5001 3690h                | 5005 3690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 500D 2694h                 | 5001 3694h                | 5005 3694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 500D 2698h                 | 5001 3698h                | 5005 3698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 500D 269Ch                 | 5001 369Ch                | 5005 369Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 500D 26A0h                 | 5001 36A0h                | 5005 36A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 500D 26B0h                 | 5001 36B0h                | 5005 36B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 500D 26B2h                 | 5001 36B2h                | 5005 36B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 500D 26BAh                 | 5001 36BAh                | 5005 36BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 500D 26BEh                 | 5001 36BEh                | 5005 36BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 500D 26C4h                 | 5001 36C4h                | 5005 36C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 500D 2700h                 | 5001 3700h                | 5005 3700h                 |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 500D 2704h                 | 5001 3704h                | 5005 3704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 500D 2708h                 | 5001 3708h                | 5005 3708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>    | 500D 270Ch                 | 5001 370Ch                | 5005 370Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>    | 500D 2710h                 | 5001 3710h                | 5005 3710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>    | 500D 2714h                 | 5001 3714h                | 5005 3714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>    | 500D 2718h                 | 5001 3718h                | 5005 3718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>    | 500D 271Ch                 | 5001 371Ch                | 5005 371Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>   | 500D 2720h                 | 5001 3720h                | 5005 3720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a>  | 500D 2730h                 | 5001 3730h                | 5005 3730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a>  | 500D 2732h                 | 5001 3732h                | 5005 3732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>     | 500D 273Ah                 | 5001 373Ah                | 5005 373Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>     | 500D 273Eh                 | 5001 373Eh                | 5005 373Eh                 |

**Table 3-796. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM19_G2 Physical Address | EPWM2_G2 Physical Address | EPWM20_G2 Physical Address |
|--------|--------|------------------------------------|----------------------------|---------------------------|----------------------------|
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a> | 500D 2744h                 | 5001 3744h                | 5005 3744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 500D 2780h                 | 5001 3780h                | 5005 3780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 500D 2784h                 | 5001 3784h                | 5005 3784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 500D 2788h                 | 5001 3788h                | 5005 3788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 500D 278Ch                 | 5001 378Ch                | 5005 378Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 500D 2790h                 | 5001 3790h                | 5005 3790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 500D 2794h                 | 5001 3794h                | 5005 3794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 500D 2798h                 | 5001 3798h                | 5005 3798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 500D 279Ch                 | 5001 379Ch                | 5005 379Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 500D 27A0h                 | 5001 37A0h                | 5005 37A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 500D 27B0h                 | 5001 37B0h                | 5005 37B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 500D 27B2h                 | 5001 37B2h                | 5005 37B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 500D 27BAh                 | 5001 37BAh                | 5005 37BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 500D 27BEh                 | 5001 37BEh                | 5005 37BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 500D 27C4h                 | 5001 37C4h                | 5005 37C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 500D 2800h                 | 5001 3800h                | 5005 3800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 500D 2804h                 | 5001 3804h                | 5005 3804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 500D 2808h                 | 5001 3808h                | 5005 3808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 500D 280Ch                 | 5001 380Ch                | 5005 380Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRFC</a>        | 500D 2810h                 | 5001 3810h                | 5005 3810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 500D 2814h                 | 5001 3814h                | 5005 3814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 500D 2820h                 | 5001 3820h                | 5005 3820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 500D 2824h                 | 5001 3824h                | 5005 3824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 500D 2828h                 | 5001 3828h                | 5005 3828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 500D 282Ch                 | 5001 382Ch                | 5005 382Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>     | 500D 2C00h                 | 5001 3C00h                | 5005 3C00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 500D 2C04h                 | 5001 3C04h                | 5005 3C04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 500D 2C20h                 | 5001 3C20h                | 5005 3C20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 500D 2C24h                 | 5001 3C24h                | 5005 3C24h                 |

**Table 3-797. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM21_G2 Physical Address | EPWM22_G2 Physical Address | EPWM23_G2 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5009 3000h                 | 500D 3000h                 | 5001 4000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5009 3002h                 | 500D 3002h                 | 5001 4002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5009 3006h                 | 500D 3006h                 | 5001 4006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5009 3008h                 | 500D 3008h                 | 5001 4008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5009 300Ah                 | 500D 300Ah                 | 5001 400Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 5009 300Ch                 | 500D 300Ch                 | 5001 400Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5009 300Eh                 | 500D 300Eh                 | 5001 400Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5009 3010h                 | 500D 3010h                 | 5001 4010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5009 3012h                 | 500D 3012h                 | 5001 4012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 5009 3018h                 | 500D 3018h                 | 5001 4018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 5009 301Ah                 | 500D 301Ah                 | 5001 401Ah                 |

**Table 3-797. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name   | EPWM21_G2 Physical Address | EPWM22_G2 Physical Address | EPWM23_G2 Physical Address |
|--------|--------|-----------------|----------------------------|----------------------------|----------------------------|
| 20h    | 16     | EPWM_AQCTL      | 5009 3020h                 | 500D 3020h                 | 5001 4020h                 |
| 22h    | 16     | EPWM_AQTSRCSEL  | 5009 3022h                 | 500D 3022h                 | 5001 4022h                 |
| 28h    | 16     | EPWM_PCCTL      | 5009 3028h                 | 500D 3028h                 | 5001 4028h                 |
| 30h    | 16     | EPWM_VCAPCTL    | 5009 3030h                 | 500D 3030h                 | 5001 4030h                 |
| 32h    | 16     | EPWM_VCNTCFG    | 5009 3032h                 | 500D 3032h                 | 5001 4032h                 |
| 40h    | 16     | EPWM_HRCNFG     | 5009 3040h                 | 500D 3040h                 | 5001 4040h                 |
| 4Eh    | 16     | EPWM_HRCNFG2    | 5009 304Eh                 | 500D 304Eh                 | 5001 404Eh                 |
| 5Ah    | 16     | EPWM_HRPCTL     | 5009 305Ah                 | 500D 305Ah                 | 5001 405Ah                 |
| 5Ch    | 16     | EPWM_TRREM      | 5009 305Ch                 | 500D 305Ch                 | 5001 405Ch                 |
| 68h    | 16     | EPWM_GLDCTL     | 5009 3068h                 | 500D 3068h                 | 5001 4068h                 |
| 6Ah    | 16     | EPWM_GLDCFG     | 5009 306Ah                 | 500D 306Ah                 | 5001 406Ah                 |
| 70h    | 32     | EPWM_EPWMXLINK  | 5009 3070h                 | 500D 3070h                 | 5001 4070h                 |
| 74h    | 32     | EPWM_EPWMXLINK2 | 5009 3074h                 | 500D 3074h                 | 5001 4074h                 |
| 7Ah    | 16     | EPWM_ETEST      | 5009 307Ah                 | 500D 307Ah                 | 5001 407Ah                 |
| 7Ch    | 16     | EPWM_EPWMREV    | 5009 307Ch                 | 500D 307Ch                 | 5001 407Ch                 |
| 7Eh    | 16     | EPWM_HRPWMREV   | 5009 307Eh                 | 500D 307Eh                 | 5001 407Eh                 |
| 80h    | 16     | EPWM_AQCTLA     | 5009 3080h                 | 500D 3080h                 | 5001 4080h                 |
| 82h    | 16     | EPWM_AQCTLA2    | 5009 3082h                 | 500D 3082h                 | 5001 4082h                 |
| 84h    | 16     | EPWM_AQCTLB     | 5009 3084h                 | 500D 3084h                 | 5001 4084h                 |
| 86h    | 16     | EPWM_AQCTLB2    | 5009 3086h                 | 500D 3086h                 | 5001 4086h                 |
| 8Eh    | 16     | EPWM_AQSFRC     | 5009 308Eh                 | 500D 308Eh                 | 5001 408Eh                 |
| 92h    | 16     | EPWM_AQCSFRC    | 5009 3092h                 | 500D 3092h                 | 5001 4092h                 |
| A0h    | 16     | EPWM_DBREDHR    | 5009 30A0h                 | 500D 30A0h                 | 5001 40A0h                 |
| A2h    | 16     | EPWM_DBRED      | 5009 30A2h                 | 500D 30A2h                 | 5001 40A2h                 |
| A4h    | 16     | EPWM_DBFEDHR    | 5009 30A4h                 | 500D 30A4h                 | 5001 40A4h                 |
| A6h    | 16     | EPWM_DBFED      | 5009 30A6h                 | 500D 30A6h                 | 5001 40A6h                 |
| C0h    | 32     | EPWM_TBPHS      | 5009 30C0h                 | 500D 30C0h                 | 5001 40C0h                 |
| C4h    | 16     | EPWM_TBPRDHR    | 5009 30C4h                 | 500D 30C4h                 | 5001 40C4h                 |
| C6h    | 16     | EPWM_TBPRD      | 5009 30C6h                 | 500D 30C6h                 | 5001 40C6h                 |
| C8h    | 16     | EPWM_TBPRDHRB   | 5009 30C8h                 | 500D 30C8h                 | 5001 40C8h                 |
| D4h    | 32     | EPWM_CMPA       | 5009 30D4h                 | 500D 30D4h                 | 5001 40D4h                 |
| D8h    | 32     | EPWM_CMPB       | 5009 30D8h                 | 500D 30D8h                 | 5001 40D8h                 |
| DEh    | 16     | EPWM_CMPC       | 5009 30DEh                 | 500D 30DEh                 | 5001 40DEh                 |
| E2h    | 16     | EPWM_CMPD       | 5009 30E2h                 | 500D 30E2h                 | 5001 40E2h                 |
| E8h    | 16     | EPWM_GLDCTL2    | 5009 30E8h                 | 500D 30E8h                 | 5001 40E8h                 |
| EEh    | 16     | EPWM_SWVDELVAL  | 5009 30EEh                 | 500D 30EEh                 | 5001 40EEh                 |
| 100h   | 16     | EPWM_TZSEL      | 5009 3100h                 | 500D 3100h                 | 5001 4100h                 |
| 102h   | 16     | EPWM_TZSEL2     | 5009 3102h                 | 500D 3102h                 | 5001 4102h                 |
| 104h   | 16     | EPWM_TZDCSEL    | 5009 3104h                 | 500D 3104h                 | 5001 4104h                 |
| 108h   | 16     | EPWM_TZCTL      | 5009 3108h                 | 500D 3108h                 | 5001 4108h                 |
| 10Ah   | 16     | EPWM_TZCTL2     | 5009 310Ah                 | 500D 310Ah                 | 5001 410Ah                 |
| 10Ch   | 16     | EPWM_TZCTLDCA   | 5009 310Ch                 | 500D 310Ch                 | 5001 410Ch                 |
| 10Eh   | 16     | EPWM_TZCTLDCB   | 5009 310Eh                 | 500D 310Eh                 | 5001 410Eh                 |
| 11Ah   | 16     | EPWM_TZEINT     | 5009 311Ah                 | 500D 311Ah                 | 5001 411Ah                 |

**Table 3-797. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM21_G2 Physical Address | EPWM22_G2 Physical Address | EPWM23_G2 Physical Address |
|--------|--------|---------------------------------------|----------------------------|----------------------------|----------------------------|
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>            | 5009 3126h                 | 500D 3126h                 | 5001 4126h                 |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>         | 5009 3128h                 | 500D 3128h                 | 5001 4128h                 |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>         | 5009 312Ah                 | 500D 312Ah                 | 5001 412Ah                 |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>            | 5009 312Eh                 | 500D 312Eh                 | 5001 412Eh                 |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>         | 5009 3130h                 | 500D 3130h                 | 5001 4130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>         | 5009 3132h                 | 500D 3132h                 | 5001 4132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>            | 5009 3136h                 | 500D 3136h                 | 5001 4136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a>     | 5009 313Ah                 | 500D 313Ah                 | 5001 413Ah                 |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>            | 5009 3148h                 | 500D 3148h                 | 5001 4148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>             | 5009 314Ch                 | 500D 314Ch                 | 5001 414Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>            | 5009 3150h                 | 500D 3150h                 | 5001 4150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>            | 5009 3154h                 | 500D 3154h                 | 5001 4154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 5009 3158h                 | 500D 3158h                 | 5001 4158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 5009 315Ch                 | 500D 315Ch                 | 5001 415Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 5009 3160h                 | 500D 3160h                 | 5001 4160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 5009 3164h                 | 500D 3164h                 | 5001 4164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 5009 3168h                 | 500D 3168h                 | 5001 4168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 5009 316Ch                 | 500D 316Ch                 | 5001 416Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 5009 3170h                 | 500D 3170h                 | 5001 4170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 5009 3174h                 | 500D 3174h                 | 5001 4174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 5009 3180h                 | 500D 3180h                 | 5001 4180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 5009 3186h                 | 500D 3186h                 | 5001 4186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5009 3188h                 | 500D 3188h                 | 5001 4188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5009 318Eh                 | 500D 318Eh                 | 5001 418Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5009 3190h                 | 500D 3190h                 | 5001 4190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5009 3192h                 | 500D 3192h                 | 5001 4192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5009 3194h                 | 500D 3194h                 | 5001 4194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5009 3196h                 | 500D 3196h                 | 5001 4196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5009 3198h                 | 500D 3198h                 | 5001 4198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5009 319Ah                 | 500D 319Ah                 | 5001 419Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5009 319Ch                 | 500D 319Ch                 | 5001 419Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5009 319Eh                 | 500D 319Eh                 | 5001 419Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5009 31A4h                 | 500D 31A4h                 | 5001 41A4h                 |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5009 31A6h                 | 500D 31A6h                 | 5001 41A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 5009 31A8h                 | 500D 31A8h                 | 5001 41A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 5009 31AAh                 | 500D 31AAh                 | 5001 41AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 5009 31ACh                 | 500D 31ACh                 | 5001 41ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 5009 31AEh                 | 500D 31AEh                 | 5001 41AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 5009 31B0h                 | 500D 31B0h                 | 5001 41B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 5009 31B2h                 | 500D 31B2h                 | 5001 41B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 5009 31F4h                 | 500D 31F4h                 | 5001 41F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 5009 31FAh                 | 500D 31FAh                 | 5001 41FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 5009 31FCh                 | 500D 31FCh                 | 5001 41FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>         | 5009 3400h                 | 500D 3400h                 | 5001 4400h                 |

**Table 3-797. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM21_G2 Physical Address | EPWM22_G2 Physical Address | EPWM23_G2 Physical Address |
|--------|--------|-------------------------------------|----------------------------|----------------------------|----------------------------|
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>       | 5009 3410h                 | 500D 3410h                 | 5001 4410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>          | 5009 3418h                 | 500D 3418h                 | 5001 4418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a> | 5009 341Ch                 | 500D 341Ch                 | 5001 441Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>   | 5009 3420h                 | 500D 3420h                 | 5001 4420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>   | 5009 3428h                 | 500D 3428h                 | 5001 4428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>   | 5009 3430h                 | 500D 3430h                 | 5001 4430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>   | 5009 3600h                 | 500D 3600h                 | 5001 4600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>   | 5009 3604h                 | 500D 3604h                 | 5001 4604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>   | 5009 3608h                 | 500D 3608h                 | 5001 4608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>   | 5009 360Ch                 | 500D 360Ch                 | 5001 460Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>   | 5009 3610h                 | 500D 3610h                 | 5001 4610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 5009 3614h                 | 500D 3614h                 | 5001 4614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 5009 3618h                 | 500D 3618h                 | 5001 4618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 5009 361Ch                 | 500D 361Ch                 | 5001 461Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 5009 3620h                 | 500D 3620h                 | 5001 4620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 5009 3630h                 | 500D 3630h                 | 5001 4630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 5009 3632h                 | 500D 3632h                 | 5001 4632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 5009 3644h                 | 500D 3644h                 | 5001 4644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 5009 3680h                 | 500D 3680h                 | 5001 4680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 5009 3684h                 | 500D 3684h                 | 5001 4684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 5009 3688h                 | 500D 3688h                 | 5001 4688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 5009 368Ch                 | 500D 368Ch                 | 5001 468Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 5009 3690h                 | 500D 3690h                 | 5001 4690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 5009 3694h                 | 500D 3694h                 | 5001 4694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 5009 3698h                 | 500D 3698h                 | 5001 4698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 5009 369Ch                 | 500D 369Ch                 | 5001 469Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 5009 36A0h                 | 500D 36A0h                 | 5001 46A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 5009 36B0h                 | 500D 36B0h                 | 5001 46B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 5009 36B2h                 | 500D 36B2h                 | 5001 46B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 5009 36BAh                 | 500D 36BAh                 | 5001 46BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 5009 36BEh                 | 500D 36BEh                 | 5001 46BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 5009 36C4h                 | 500D 36C4h                 | 5001 46C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 5009 3700h                 | 500D 3700h                 | 5001 4700h                 |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 5009 3704h                 | 500D 3704h                 | 5001 4704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 5009 3708h                 | 500D 3708h                 | 5001 4708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>    | 5009 370Ch                 | 500D 370Ch                 | 5001 470Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>    | 5009 3710h                 | 500D 3710h                 | 5001 4710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>    | 5009 3714h                 | 500D 3714h                 | 5001 4714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>    | 5009 3718h                 | 500D 3718h                 | 5001 4718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>    | 5009 371Ch                 | 500D 371Ch                 | 5001 471Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>   | 5009 3720h                 | 500D 3720h                 | 5001 4720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a>  | 5009 3730h                 | 500D 3730h                 | 5001 4730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a>  | 5009 3732h                 | 500D 3732h                 | 5001 4732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>     | 5009 373Ah                 | 500D 373Ah                 | 5001 473Ah                 |



**Table 3-797. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM21_G2 Physical Address | EPWM22_G2 Physical Address | EPWM23_G2 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>    | 5009 373Eh                 | 500D 373Eh                 | 5001 473Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a> | 5009 3744h                 | 500D 3744h                 | 5001 4744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 5009 3780h                 | 500D 3780h                 | 5001 4780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 5009 3784h                 | 500D 3784h                 | 5001 4784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 5009 3788h                 | 500D 3788h                 | 5001 4788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 5009 378Ch                 | 500D 378Ch                 | 5001 478Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 5009 3790h                 | 500D 3790h                 | 5001 4790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 5009 3794h                 | 500D 3794h                 | 5001 4794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 5009 3798h                 | 500D 3798h                 | 5001 4798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 5009 379Ch                 | 500D 379Ch                 | 5001 479Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 5009 37A0h                 | 500D 37A0h                 | 5001 47A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5009 37B0h                 | 500D 37B0h                 | 5001 47B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5009 37B2h                 | 500D 37B2h                 | 5001 47B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5009 37BAh                 | 500D 37BAh                 | 5001 47BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5009 37BEh                 | 500D 37BEh                 | 5001 47BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5009 37C4h                 | 500D 37C4h                 | 5001 47C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5009 3800h                 | 500D 3800h                 | 5001 4800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5009 3804h                 | 500D 3804h                 | 5001 4804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5009 3808h                 | 500D 3808h                 | 5001 4808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5009 380Ch                 | 500D 380Ch                 | 5001 480Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 5009 3810h                 | 500D 3810h                 | 5001 4810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5009 3814h                 | 500D 3814h                 | 5001 4814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 5009 3820h                 | 500D 3820h                 | 5001 4820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 5009 3824h                 | 500D 3824h                 | 5001 4824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 5009 3828h                 | 500D 3828h                 | 5001 4828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 5009 382Ch                 | 500D 382Ch                 | 5001 482Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>     | 5009 3C00h                 | 500D 3C00h                 | 5001 4C00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 5009 3C04h                 | 500D 3C04h                 | 5001 4C04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 5009 3C20h                 | 500D 3C20h                 | 5001 4C20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 5009 3C24h                 | 500D 3C24h                 | 5001 4C24h                 |

**Table 3-798. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM24_G2 Physical Address | EPWM25_G2 Physical Address | EPWM26_G2 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5005 4000h                 | 5009 4000h                 | 500D 4000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5005 4002h                 | 5009 4002h                 | 500D 4002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5005 4006h                 | 5009 4006h                 | 500D 4006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5005 4008h                 | 5009 4008h                 | 500D 4008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5005 400Ah                 | 5009 400Ah                 | 500D 400Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 5005 400Ch                 | 5009 400Ch                 | 500D 400Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5005 400Eh                 | 5009 400Eh                 | 500D 400Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5005 4010h                 | 5009 4010h                 | 500D 4010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5005 4012h                 | 5009 4012h                 | 500D 4012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 5005 4018h                 | 5009 4018h                 | 500D 4018h                 |



**Table 3-798. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                   | EPWM24_G2 Physical Address | EPWM25_G2 Physical Address | EPWM26_G2 Physical Address |
|--------|--------|---------------------------------|----------------------------|----------------------------|----------------------------|
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>     | 5005 401Ah                 | 5009 401Ah                 | 500D 401Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>      | 5005 4020h                 | 5009 4020h                 | 500D 4020h                 |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>  | 5005 4022h                 | 5009 4022h                 | 500D 4022h                 |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>      | 5005 4028h                 | 5009 4028h                 | 500D 4028h                 |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>    | 5005 4030h                 | 5009 4030h                 | 500D 4030h                 |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>    | 5005 4032h                 | 5009 4032h                 | 500D 4032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>     | 5005 4040h                 | 5009 4040h                 | 500D 4040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>    | 5005 404Eh                 | 5009 404Eh                 | 500D 404Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>     | 5005 405Ah                 | 5009 405Ah                 | 500D 405Ah                 |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>      | 5005 405Ch                 | 5009 405Ch                 | 500D 405Ch                 |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>     | 5005 4068h                 | 5009 4068h                 | 500D 4068h                 |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>     | 5005 406Ah                 | 5009 406Ah                 | 500D 406Ah                 |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>  | 5005 4070h                 | 5009 4070h                 | 500D 4070h                 |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a> | 5005 4074h                 | 5009 4074h                 | 500D 4074h                 |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>      | 5005 407Ah                 | 5009 407Ah                 | 500D 407Ah                 |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>    | 5005 407Ch                 | 5009 407Ch                 | 500D 407Ch                 |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>   | 5005 407Eh                 | 5009 407Eh                 | 500D 407Eh                 |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>     | 5005 4080h                 | 5009 4080h                 | 500D 4080h                 |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>    | 5005 4082h                 | 5009 4082h                 | 500D 4082h                 |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>     | 5005 4084h                 | 5009 4084h                 | 500D 4084h                 |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>    | 5005 4086h                 | 5009 4086h                 | 500D 4086h                 |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>     | 5005 408Eh                 | 5009 408Eh                 | 500D 408Eh                 |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>    | 5005 4092h                 | 5009 4092h                 | 500D 4092h                 |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>    | 5005 40A0h                 | 5009 40A0h                 | 500D 40A0h                 |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>      | 5005 40A2h                 | 5009 40A2h                 | 500D 40A2h                 |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>    | 5005 40A4h                 | 5009 40A4h                 | 500D 40A4h                 |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>      | 5005 40A6h                 | 5009 40A6h                 | 500D 40A6h                 |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>      | 5005 40C0h                 | 5009 40C0h                 | 500D 40C0h                 |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>    | 5005 40C4h                 | 5009 40C4h                 | 500D 40C4h                 |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>      | 5005 40C6h                 | 5009 40C6h                 | 500D 40C6h                 |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>   | 5005 40C8h                 | 5009 40C8h                 | 500D 40C8h                 |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>       | 5005 40D4h                 | 5009 40D4h                 | 500D 40D4h                 |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>       | 5005 40D8h                 | 5009 40D8h                 | 500D 40D8h                 |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>       | 5005 40DEh                 | 5009 40DEh                 | 500D 40DEh                 |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>       | 5005 40E2h                 | 5009 40E2h                 | 500D 40E2h                 |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>    | 5005 40E8h                 | 5009 40E8h                 | 500D 40E8h                 |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>  | 5005 40EEh                 | 5009 40EEh                 | 500D 40EEh                 |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>      | 5005 4100h                 | 5009 4100h                 | 500D 4100h                 |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>     | 5005 4102h                 | 5009 4102h                 | 500D 4102h                 |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>    | 5005 4104h                 | 5009 4104h                 | 500D 4104h                 |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>      | 5005 4108h                 | 5009 4108h                 | 500D 4108h                 |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>     | 5005 410Ah                 | 5009 410Ah                 | 500D 410Ah                 |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>   | 5005 410Ch                 | 5009 410Ch                 | 500D 410Ch                 |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>   | 5005 410Eh                 | 5009 410Eh                 | 500D 410Eh                 |

**Table 3-798. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM24_G2 Physical Address | EPWM25_G2 Physical Address | EPWM26_G2 Physical Address |
|--------|--------|---------------------------------------|----------------------------|----------------------------|----------------------------|
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>           | 5005 411Ah                 | 5009 411Ah                 | 500D 411Ah                 |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>            | 5005 4126h                 | 5009 4126h                 | 500D 4126h                 |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>         | 5005 4128h                 | 5009 4128h                 | 500D 4128h                 |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>         | 5005 412Ah                 | 5009 412Ah                 | 500D 412Ah                 |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>            | 5005 412Eh                 | 5009 412Eh                 | 500D 412Eh                 |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>         | 5005 4130h                 | 5009 4130h                 | 500D 4130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>         | 5005 4132h                 | 5009 4132h                 | 500D 4132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>            | 5005 4136h                 | 5009 4136h                 | 500D 4136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a>     | 5005 413Ah                 | 5009 413Ah                 | 500D 413Ah                 |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>            | 5005 4148h                 | 5009 4148h                 | 500D 4148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>             | 5005 414Ch                 | 5009 414Ch                 | 500D 414Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>            | 5005 4150h                 | 5009 4150h                 | 500D 4150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>            | 5005 4154h                 | 5009 4154h                 | 500D 4154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 5005 4158h                 | 5009 4158h                 | 500D 4158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 5005 415Ch                 | 5009 415Ch                 | 500D 415Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 5005 4160h                 | 5009 4160h                 | 500D 4160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 5005 4164h                 | 5009 4164h                 | 500D 4164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 5005 4168h                 | 5009 4168h                 | 500D 4168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 5005 416Ch                 | 5009 416Ch                 | 500D 416Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 5005 4170h                 | 5009 4170h                 | 500D 4170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 5005 4174h                 | 5009 4174h                 | 500D 4174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 5005 4180h                 | 5009 4180h                 | 500D 4180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 5005 4186h                 | 5009 4186h                 | 500D 4186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5005 4188h                 | 5009 4188h                 | 500D 4188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5005 418Eh                 | 5009 418Eh                 | 500D 418Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5005 4190h                 | 5009 4190h                 | 500D 4190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5005 4192h                 | 5009 4192h                 | 500D 4192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5005 4194h                 | 5009 4194h                 | 500D 4194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5005 4196h                 | 5009 4196h                 | 500D 4196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5005 4198h                 | 5009 4198h                 | 500D 4198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5005 419Ah                 | 5009 419Ah                 | 500D 419Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5005 419Ch                 | 5009 419Ch                 | 500D 419Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5005 419Eh                 | 5009 419Eh                 | 500D 419Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5005 41A4h                 | 5009 41A4h                 | 500D 41A4h                 |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5005 41A6h                 | 5009 41A6h                 | 500D 41A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 5005 41A8h                 | 5009 41A8h                 | 500D 41A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 5005 41AAh                 | 5009 41AAh                 | 500D 41AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 5005 41ACh                 | 5009 41ACh                 | 500D 41ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 5005 41AEh                 | 5009 41AEh                 | 500D 41AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 5005 41B0h                 | 5009 41B0h                 | 500D 41B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 5005 41B2h                 | 5009 41B2h                 | 500D 41B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 5005 41F4h                 | 5009 41F4h                 | 500D 41F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 5005 41FAh                 | 5009 41FAh                 | 500D 41FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>          | 5005 41FCh                 | 5009 41FCh                 | 500D 41FCh                 |

**Table 3-798. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM24_G2 Physical Address | EPWM25_G2 Physical Address | EPWM26_G2 Physical Address |
|--------|--------|-------------------------------------|----------------------------|----------------------------|----------------------------|
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>       | 5005 4400h                 | 5009 4400h                 | 500D 4400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>       | 5005 4410h                 | 5009 4410h                 | 500D 4410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>          | 5005 4418h                 | 5009 4418h                 | 500D 4418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a> | 5005 441Ch                 | 5009 441Ch                 | 500D 441Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>   | 5005 4420h                 | 5009 4420h                 | 500D 4420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>   | 5005 4428h                 | 5009 4428h                 | 500D 4428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>   | 5005 4430h                 | 5009 4430h                 | 500D 4430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>   | 5005 4600h                 | 5009 4600h                 | 500D 4600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>   | 5005 4604h                 | 5009 4604h                 | 500D 4604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>   | 5005 4608h                 | 5009 4608h                 | 500D 4608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>   | 5005 460Ch                 | 5009 460Ch                 | 500D 460Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>   | 5005 4610h                 | 5009 4610h                 | 500D 4610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 5005 4614h                 | 5009 4614h                 | 500D 4614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 5005 4618h                 | 5009 4618h                 | 500D 4618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 5005 461Ch                 | 5009 461Ch                 | 500D 461Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 5005 4620h                 | 5009 4620h                 | 500D 4620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 5005 4630h                 | 5009 4630h                 | 500D 4630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 5005 4632h                 | 5009 4632h                 | 500D 4632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 5005 4644h                 | 5009 4644h                 | 500D 4644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 5005 4680h                 | 5009 4680h                 | 500D 4680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 5005 4684h                 | 5009 4684h                 | 500D 4684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 5005 4688h                 | 5009 4688h                 | 500D 4688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 5005 468Ch                 | 5009 468Ch                 | 500D 468Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 5005 4690h                 | 5009 4690h                 | 500D 4690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 5005 4694h                 | 5009 4694h                 | 500D 4694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 5005 4698h                 | 5009 4698h                 | 500D 4698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 5005 469Ch                 | 5009 469Ch                 | 500D 469Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 5005 46A0h                 | 5009 46A0h                 | 500D 46A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 5005 46B0h                 | 5009 46B0h                 | 500D 46B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 5005 46B2h                 | 5009 46B2h                 | 500D 46B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 5005 46BAh                 | 5009 46BAh                 | 500D 46BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 5005 46BEh                 | 5009 46BEh                 | 500D 46BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 5005 46C4h                 | 5009 46C4h                 | 500D 46C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 5005 4700h                 | 5009 4700h                 | 500D 4700h                 |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 5005 4704h                 | 5009 4704h                 | 500D 4704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 5005 4708h                 | 5009 4708h                 | 500D 4708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>    | 5005 470Ch                 | 5009 470Ch                 | 500D 470Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>    | 5005 4710h                 | 5009 4710h                 | 500D 4710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>    | 5005 4714h                 | 5009 4714h                 | 500D 4714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>    | 5005 4718h                 | 5009 4718h                 | 500D 4718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>    | 5005 471Ch                 | 5009 471Ch                 | 500D 471Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>   | 5005 4720h                 | 5009 4720h                 | 500D 4720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a>  | 5005 4730h                 | 5009 4730h                 | 500D 4730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a>  | 5005 4732h                 | 5009 4732h                 | 500D 4732h                 |

**Table 3-798. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM24_G2 Physical Address | EPWM25_G2 Physical Address | EPWM26_G2 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>    | 5005 473Ah                 | 5009 473Ah                 | 500D 473Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>    | 5005 473Eh                 | 5009 473Eh                 | 500D 473Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a> | 5005 4744h                 | 5009 4744h                 | 500D 4744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 5005 4780h                 | 5009 4780h                 | 500D 4780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 5005 4784h                 | 5009 4784h                 | 500D 4784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 5005 4788h                 | 5009 4788h                 | 500D 4788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 5005 478Ch                 | 5009 478Ch                 | 500D 478Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 5005 4790h                 | 5009 4790h                 | 500D 4790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 5005 4794h                 | 5009 4794h                 | 500D 4794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 5005 4798h                 | 5009 4798h                 | 500D 4798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 5005 479Ch                 | 5009 479Ch                 | 500D 479Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 5005 47A0h                 | 5009 47A0h                 | 500D 47A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5005 47B0h                 | 5009 47B0h                 | 500D 47B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5005 47B2h                 | 5009 47B2h                 | 500D 47B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5005 47BAh                 | 5009 47BAh                 | 500D 47BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5005 47BEh                 | 5009 47BEh                 | 500D 47BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5005 47C4h                 | 5009 47C4h                 | 500D 47C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5005 4800h                 | 5009 4800h                 | 500D 4800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5005 4804h                 | 5009 4804h                 | 500D 4804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5005 4808h                 | 5009 4808h                 | 500D 4808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5005 480Ch                 | 5009 480Ch                 | 500D 480Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 5005 4810h                 | 5009 4810h                 | 500D 4810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5005 4814h                 | 5009 4814h                 | 500D 4814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 5005 4820h                 | 5009 4820h                 | 500D 4820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 5005 4824h                 | 5009 4824h                 | 500D 4824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 5005 4828h                 | 5009 4828h                 | 500D 4828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 5005 482Ch                 | 5009 482Ch                 | 500D 482Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>     | 5005 4C00h                 | 5009 4C00h                 | 500D 4C00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 5005 4C04h                 | 5009 4C04h                 | 500D 4C04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 5005 4C20h                 | 5009 4C20h                 | 500D 4C20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 5005 4C24h                 | 5009 4C24h                 | 500D 4C24h                 |

**Table 3-799. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM27_G2 Physical Address | EPWM28_G2 Physical Address | EPWM29_G2 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5001 5000h                 | 5005 5000h                 | 5009 5000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5001 5002h                 | 5005 5002h                 | 5009 5002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5001 5006h                 | 5005 5006h                 | 5009 5006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5001 5008h                 | 5005 5008h                 | 5009 5008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5001 500Ah                 | 5005 500Ah                 | 5009 500Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 5001 500Ch                 | 5005 500Ch                 | 5009 500Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5001 500Eh                 | 5005 500Eh                 | 5009 500Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5001 5010h                 | 5005 5010h                 | 5009 5010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5001 5012h                 | 5005 5012h                 | 5009 5012h                 |

**Table 3-799. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                   | EPWM27_G2 Physical Address | EPWM28_G2 Physical Address | EPWM29_G2 Physical Address |
|--------|--------|---------------------------------|----------------------------|----------------------------|----------------------------|
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>      | 5001 5018h                 | 5005 5018h                 | 5009 5018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>     | 5001 501Ah                 | 5005 501Ah                 | 5009 501Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>      | 5001 5020h                 | 5005 5020h                 | 5009 5020h                 |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>  | 5001 5022h                 | 5005 5022h                 | 5009 5022h                 |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>      | 5001 5028h                 | 5005 5028h                 | 5009 5028h                 |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>    | 5001 5030h                 | 5005 5030h                 | 5009 5030h                 |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>    | 5001 5032h                 | 5005 5032h                 | 5009 5032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>     | 5001 5040h                 | 5005 5040h                 | 5009 5040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>    | 5001 504Eh                 | 5005 504Eh                 | 5009 504Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>     | 5001 505Ah                 | 5005 505Ah                 | 5009 505Ah                 |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>      | 5001 505Ch                 | 5005 505Ch                 | 5009 505Ch                 |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>     | 5001 5068h                 | 5005 5068h                 | 5009 5068h                 |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>     | 5001 506Ah                 | 5005 506Ah                 | 5009 506Ah                 |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>  | 5001 5070h                 | 5005 5070h                 | 5009 5070h                 |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a> | 5001 5074h                 | 5005 5074h                 | 5009 5074h                 |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>      | 5001 507Ah                 | 5005 507Ah                 | 5009 507Ah                 |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>    | 5001 507Ch                 | 5005 507Ch                 | 5009 507Ch                 |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>   | 5001 507Eh                 | 5005 507Eh                 | 5009 507Eh                 |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>     | 5001 5080h                 | 5005 5080h                 | 5009 5080h                 |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>    | 5001 5082h                 | 5005 5082h                 | 5009 5082h                 |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>     | 5001 5084h                 | 5005 5084h                 | 5009 5084h                 |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>    | 5001 5086h                 | 5005 5086h                 | 5009 5086h                 |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRFC</a>    | 5001 508Eh                 | 5005 508Eh                 | 5009 508Eh                 |
| 92h    | 16     | <a href="#">EPWM_AQCSFRFC</a>   | 5001 5092h                 | 5005 5092h                 | 5009 5092h                 |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>    | 5001 50A0h                 | 5005 50A0h                 | 5009 50A0h                 |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>      | 5001 50A2h                 | 5005 50A2h                 | 5009 50A2h                 |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>    | 5001 50A4h                 | 5005 50A4h                 | 5009 50A4h                 |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>      | 5001 50A6h                 | 5005 50A6h                 | 5009 50A6h                 |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>      | 5001 50C0h                 | 5005 50C0h                 | 5009 50C0h                 |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>    | 5001 50C4h                 | 5005 50C4h                 | 5009 50C4h                 |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>      | 5001 50C6h                 | 5005 50C6h                 | 5009 50C6h                 |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>   | 5001 50C8h                 | 5005 50C8h                 | 5009 50C8h                 |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>       | 5001 50D4h                 | 5005 50D4h                 | 5009 50D4h                 |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>       | 5001 50D8h                 | 5005 50D8h                 | 5009 50D8h                 |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>       | 5001 50DEh                 | 5005 50DEh                 | 5009 50DEh                 |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>       | 5001 50E2h                 | 5005 50E2h                 | 5009 50E2h                 |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>    | 5001 50E8h                 | 5005 50E8h                 | 5009 50E8h                 |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>  | 5001 50EEh                 | 5005 50EEh                 | 5009 50EEh                 |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>      | 5001 5100h                 | 5005 5100h                 | 5009 5100h                 |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>     | 5001 5102h                 | 5005 5102h                 | 5009 5102h                 |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>    | 5001 5104h                 | 5005 5104h                 | 5009 5104h                 |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>      | 5001 5108h                 | 5005 5108h                 | 5009 5108h                 |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>     | 5001 510Ah                 | 5005 510Ah                 | 5009 510Ah                 |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>   | 5001 510Ch                 | 5005 510Ch                 | 5009 510Ch                 |

**Table 3-799. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM27_G2 Physical Address | EPWM28_G2 Physical Address | EPWM29_G2 Physical Address |
|--------|--------|---------------------------------------|----------------------------|----------------------------|----------------------------|
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>         | 5001 510Eh                 | 5005 510Eh                 | 5009 510Eh                 |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>           | 5001 511Ah                 | 5005 511Ah                 | 5009 511Ah                 |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>            | 5001 5126h                 | 5005 5126h                 | 5009 5126h                 |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>         | 5001 5128h                 | 5005 5128h                 | 5009 5128h                 |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>         | 5001 512Ah                 | 5005 512Ah                 | 5009 512Ah                 |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>            | 5001 512Eh                 | 5005 512Eh                 | 5009 512Eh                 |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>         | 5001 5130h                 | 5005 5130h                 | 5009 5130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>         | 5001 5132h                 | 5005 5132h                 | 5009 5132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>            | 5001 5136h                 | 5005 5136h                 | 5009 5136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a>     | 5001 513Ah                 | 5005 513Ah                 | 5009 513Ah                 |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>            | 5001 5148h                 | 5005 5148h                 | 5009 5148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>             | 5001 514Ch                 | 5005 514Ch                 | 5009 514Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>            | 5001 5150h                 | 5005 5150h                 | 5009 5150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>            | 5001 5154h                 | 5005 5154h                 | 5009 5154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 5001 5158h                 | 5005 5158h                 | 5009 5158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 5001 515Ch                 | 5005 515Ch                 | 5009 515Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 5001 5160h                 | 5005 5160h                 | 5009 5160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 5001 5164h                 | 5005 5164h                 | 5009 5164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 5001 5168h                 | 5005 5168h                 | 5009 5168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 5001 516Ch                 | 5005 516Ch                 | 5009 516Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 5001 5170h                 | 5005 5170h                 | 5009 5170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 5001 5174h                 | 5005 5174h                 | 5009 5174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 5001 5180h                 | 5005 5180h                 | 5009 5180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 5001 5186h                 | 5005 5186h                 | 5009 5186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5001 5188h                 | 5005 5188h                 | 5009 5188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5001 518Eh                 | 5005 518Eh                 | 5009 518Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5001 5190h                 | 5005 5190h                 | 5009 5190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5001 5192h                 | 5005 5192h                 | 5009 5192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5001 5194h                 | 5005 5194h                 | 5009 5194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5001 5196h                 | 5005 5196h                 | 5009 5196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5001 5198h                 | 5005 5198h                 | 5009 5198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5001 519Ah                 | 5005 519Ah                 | 5009 519Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5001 519Ch                 | 5005 519Ch                 | 5009 519Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5001 519Eh                 | 5005 519Eh                 | 5009 519Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5001 51A4h                 | 5005 51A4h                 | 5009 51A4h                 |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5001 51A6h                 | 5005 51A6h                 | 5009 51A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 5001 51A8h                 | 5005 51A8h                 | 5009 51A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 5001 51AAh                 | 5005 51AAh                 | 5009 51AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 5001 51ACh                 | 5005 51ACh                 | 5009 51ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 5001 51AEh                 | 5005 51AEh                 | 5009 51AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 5001 51B0h                 | 5005 51B0h                 | 5009 51B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 5001 51B2h                 | 5005 51B2h                 | 5009 51B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 5001 51F4h                 | 5005 51F4h                 | 5009 51F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>        | 5001 51FAh                 | 5005 51FAh                 | 5009 51FAh                 |

**Table 3-799. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM27_G2 Physical Address | EPWM28_G2 Physical Address | EPWM29_G2 Physical Address |
|--------|--------|-------------------------------------|----------------------------|----------------------------|----------------------------|
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>        | 5001 51FCh                 | 5005 51FCh                 | 5009 51FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>       | 5001 5400h                 | 5005 5400h                 | 5009 5400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>       | 5001 5410h                 | 5005 5410h                 | 5009 5410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>          | 5001 5418h                 | 5005 5418h                 | 5009 5418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a> | 5001 541Ch                 | 5005 541Ch                 | 5009 541Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>   | 5001 5420h                 | 5005 5420h                 | 5009 5420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>   | 5001 5428h                 | 5005 5428h                 | 5009 5428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>   | 5001 5430h                 | 5005 5430h                 | 5009 5430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>   | 5001 5600h                 | 5005 5600h                 | 5009 5600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>   | 5001 5604h                 | 5005 5604h                 | 5009 5604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>   | 5001 5608h                 | 5005 5608h                 | 5009 5608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>   | 5001 560Ch                 | 5005 560Ch                 | 5009 560Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>   | 5001 5610h                 | 5005 5610h                 | 5009 5610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 5001 5614h                 | 5005 5614h                 | 5009 5614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 5001 5618h                 | 5005 5618h                 | 5009 5618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 5001 561Ch                 | 5005 561Ch                 | 5009 561Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 5001 5620h                 | 5005 5620h                 | 5009 5620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 5001 5630h                 | 5005 5630h                 | 5009 5630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 5001 5632h                 | 5005 5632h                 | 5009 5632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 5001 5644h                 | 5005 5644h                 | 5009 5644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 5001 5680h                 | 5005 5680h                 | 5009 5680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 5001 5684h                 | 5005 5684h                 | 5009 5684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 5001 5688h                 | 5005 5688h                 | 5009 5688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 5001 568Ch                 | 5005 568Ch                 | 5009 568Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 5001 5690h                 | 5005 5690h                 | 5009 5690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 5001 5694h                 | 5005 5694h                 | 5009 5694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 5001 5698h                 | 5005 5698h                 | 5009 5698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 5001 569Ch                 | 5005 569Ch                 | 5009 569Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 5001 56A0h                 | 5005 56A0h                 | 5009 56A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 5001 56B0h                 | 5005 56B0h                 | 5009 56B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 5001 56B2h                 | 5005 56B2h                 | 5009 56B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 5001 56BAh                 | 5005 56BAh                 | 5009 56BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 5001 56BEh                 | 5005 56BEh                 | 5009 56BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 5001 56C4h                 | 5005 56C4h                 | 5009 56C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 5001 5700h                 | 5005 5700h                 | 5009 5700h                 |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 5001 5704h                 | 5005 5704h                 | 5009 5704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 5001 5708h                 | 5005 5708h                 | 5009 5708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>    | 5001 570Ch                 | 5005 570Ch                 | 5009 570Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>    | 5001 5710h                 | 5005 5710h                 | 5009 5710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>    | 5001 5714h                 | 5005 5714h                 | 5009 5714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>    | 5001 5718h                 | 5005 5718h                 | 5009 5718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>    | 5001 571Ch                 | 5005 571Ch                 | 5009 571Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>   | 5001 5720h                 | 5005 5720h                 | 5009 5720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a>  | 5001 5730h                 | 5005 5730h                 | 5009 5730h                 |



**Table 3-799. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM27_G2 Physical Address | EPWM28_G2 Physical Address | EPWM29_G2 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a> | 5001 5732h                 | 5005 5732h                 | 5009 5732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>    | 5001 573Ah                 | 5005 573Ah                 | 5009 573Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>    | 5001 573Eh                 | 5005 573Eh                 | 5009 573Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a> | 5001 5744h                 | 5005 5744h                 | 5009 5744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 5001 5780h                 | 5005 5780h                 | 5009 5780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 5001 5784h                 | 5005 5784h                 | 5009 5784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 5001 5788h                 | 5005 5788h                 | 5009 5788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 5001 578Ch                 | 5005 578Ch                 | 5009 578Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 5001 5790h                 | 5005 5790h                 | 5009 5790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 5001 5794h                 | 5005 5794h                 | 5009 5794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 5001 5798h                 | 5005 5798h                 | 5009 5798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 5001 579Ch                 | 5005 579Ch                 | 5009 579Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 5001 57A0h                 | 5005 57A0h                 | 5009 57A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5001 57B0h                 | 5005 57B0h                 | 5009 57B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5001 57B2h                 | 5005 57B2h                 | 5009 57B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5001 57BAh                 | 5005 57BAh                 | 5009 57BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5001 57BEh                 | 5005 57BEh                 | 5009 57BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5001 57C4h                 | 5005 57C4h                 | 5009 57C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5001 5800h                 | 5005 5800h                 | 5009 5800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5001 5804h                 | 5005 5804h                 | 5009 5804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5001 5808h                 | 5005 5808h                 | 5009 5808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5001 580Ch                 | 5005 580Ch                 | 5009 580Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 5001 5810h                 | 5005 5810h                 | 5009 5810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5001 5814h                 | 5005 5814h                 | 5009 5814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 5001 5820h                 | 5005 5820h                 | 5009 5820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 5001 5824h                 | 5005 5824h                 | 5009 5824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 5001 5828h                 | 5005 5828h                 | 5009 5828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 5001 582Ch                 | 5005 582Ch                 | 5009 582Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>     | 5001 5C00h                 | 5005 5C00h                 | 5009 5C00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 5001 5C04h                 | 5005 5C04h                 | 5009 5C04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 5001 5C20h                 | 5005 5C20h                 | 5009 5C20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 5001 5C24h                 | 5005 5C24h                 | 5009 5C24h                 |

**Table 3-800. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM3_G2 Physical Address | EPWM30_G2 Physical Address | EPWM31_G2 Physical Address |
|--------|--------|------------------------------------|---------------------------|----------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 500D 5000h                | 5001 6000h                 | 5005 6000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 500D 5002h                | 5001 6002h                 | 5005 6002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 500D 5006h                | 5001 6006h                 | 5005 6006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 500D 5008h                | 5001 6008h                 | 5005 6008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 500D 500Ah                | 5001 600Ah                 | 5005 600Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 500D 500Ch                | 5001 600Ch                 | 5005 600Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 500D 500Eh                | 5001 600Eh                 | 5005 600Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 500D 5010h                | 5001 6010h                 | 5005 6010h                 |



**Table 3-800. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                   | EPWM3_G2 Physical Address | EPWM30_G2 Physical Address | EPWM31_G2 Physical Address |
|--------|--------|---------------------------------|---------------------------|----------------------------|----------------------------|
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>    | 500D 5012h                | 5001 6012h                 | 5005 6012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>      | 500D 5018h                | 5001 6018h                 | 5005 6018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>     | 500D 501Ah                | 5001 601Ah                 | 5005 601Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>      | 500D 5020h                | 5001 6020h                 | 5005 6020h                 |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>  | 500D 5022h                | 5001 6022h                 | 5005 6022h                 |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>      | 500D 5028h                | 5001 6028h                 | 5005 6028h                 |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>    | 500D 5030h                | 5001 6030h                 | 5005 6030h                 |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>    | 500D 5032h                | 5001 6032h                 | 5005 6032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>     | 500D 5040h                | 5001 6040h                 | 5005 6040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>    | 500D 504Eh                | 5001 604Eh                 | 5005 604Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>     | 500D 505Ah                | 5001 605Ah                 | 5005 605Ah                 |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>      | 500D 505Ch                | 5001 605Ch                 | 5005 605Ch                 |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>     | 500D 5068h                | 5001 6068h                 | 5005 6068h                 |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>     | 500D 506Ah                | 5001 606Ah                 | 5005 606Ah                 |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>  | 500D 5070h                | 5001 6070h                 | 5005 6070h                 |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a> | 500D 5074h                | 5001 6074h                 | 5005 6074h                 |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>      | 500D 507Ah                | 5001 607Ah                 | 5005 607Ah                 |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>    | 500D 507Ch                | 5001 607Ch                 | 5005 607Ch                 |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>   | 500D 507Eh                | 5001 607Eh                 | 5005 607Eh                 |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>     | 500D 5080h                | 5001 6080h                 | 5005 6080h                 |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>    | 500D 5082h                | 5001 6082h                 | 5005 6082h                 |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>     | 500D 5084h                | 5001 6084h                 | 5005 6084h                 |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>    | 500D 5086h                | 5001 6086h                 | 5005 6086h                 |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>     | 500D 508Eh                | 5001 608Eh                 | 5005 608Eh                 |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>    | 500D 5092h                | 5001 6092h                 | 5005 6092h                 |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>    | 500D 50A0h                | 5001 60A0h                 | 5005 60A0h                 |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>      | 500D 50A2h                | 5001 60A2h                 | 5005 60A2h                 |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>    | 500D 50A4h                | 5001 60A4h                 | 5005 60A4h                 |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>      | 500D 50A6h                | 5001 60A6h                 | 5005 60A6h                 |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>      | 500D 50C0h                | 5001 60C0h                 | 5005 60C0h                 |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>    | 500D 50C4h                | 5001 60C4h                 | 5005 60C4h                 |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>      | 500D 50C6h                | 5001 60C6h                 | 5005 60C6h                 |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>   | 500D 50C8h                | 5001 60C8h                 | 5005 60C8h                 |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>       | 500D 50D4h                | 5001 60D4h                 | 5005 60D4h                 |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>       | 500D 50D8h                | 5001 60D8h                 | 5005 60D8h                 |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>       | 500D 50DEh                | 5001 60DEh                 | 5005 60DEh                 |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>       | 500D 50E2h                | 5001 60E2h                 | 5005 60E2h                 |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>    | 500D 50E8h                | 5001 60E8h                 | 5005 60E8h                 |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>  | 500D 50EEh                | 5001 60EEh                 | 5005 60EEh                 |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>      | 500D 5100h                | 5001 6100h                 | 5005 6100h                 |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>     | 500D 5102h                | 5001 6102h                 | 5005 6102h                 |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>    | 500D 5104h                | 5001 6104h                 | 5005 6104h                 |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>      | 500D 5108h                | 5001 6108h                 | 5005 6108h                 |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>     | 500D 510Ah                | 5001 610Ah                 | 5005 610Ah                 |

**Table 3-800. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM3_G2 Physical Address | EPWM30_G2 Physical Address | EPWM31_G2 Physical Address |
|--------|--------|---------------------------------------|---------------------------|----------------------------|----------------------------|
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>         | 500D 510Ch                | 5001 610Ch                 | 5005 610Ch                 |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>         | 500D 510Eh                | 5001 610Eh                 | 5005 610Eh                 |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>           | 500D 511Ah                | 5001 611Ah                 | 5005 611Ah                 |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>            | 500D 5126h                | 5001 6126h                 | 5005 6126h                 |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>         | 500D 5128h                | 5001 6128h                 | 5005 6128h                 |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>         | 500D 512Ah                | 5001 612Ah                 | 5005 612Ah                 |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>            | 500D 512Eh                | 5001 612Eh                 | 5005 612Eh                 |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>         | 500D 5130h                | 5001 6130h                 | 5005 6130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>         | 500D 5132h                | 5001 6132h                 | 5005 6132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>            | 500D 5136h                | 5001 6136h                 | 5005 6136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a>     | 500D 513Ah                | 5001 613Ah                 | 5005 613Ah                 |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>            | 500D 5148h                | 5001 6148h                 | 5005 6148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>             | 500D 514Ch                | 5001 614Ch                 | 5005 614Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>            | 500D 5150h                | 5001 6150h                 | 5005 6150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>            | 500D 5154h                | 5001 6154h                 | 5005 6154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 500D 5158h                | 5001 6158h                 | 5005 6158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 500D 515Ch                | 5001 615Ch                 | 5005 615Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 500D 5160h                | 5001 6160h                 | 5005 6160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 500D 5164h                | 5001 6164h                 | 5005 6164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 500D 5168h                | 5001 6168h                 | 5005 6168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 500D 516Ch                | 5001 616Ch                 | 5005 616Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 500D 5170h                | 5001 6170h                 | 5005 6170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 500D 5174h                | 5001 6174h                 | 5005 6174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 500D 5180h                | 5001 6180h                 | 5005 6180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 500D 5186h                | 5001 6186h                 | 5005 6186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 500D 5188h                | 5001 6188h                 | 5005 6188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 500D 518Eh                | 5001 618Eh                 | 5005 618Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 500D 5190h                | 5001 6190h                 | 5005 6190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 500D 5192h                | 5001 6192h                 | 5005 6192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 500D 5194h                | 5001 6194h                 | 5005 6194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 500D 5196h                | 5001 6196h                 | 5005 6196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 500D 5198h                | 5001 6198h                 | 5005 6198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 500D 519Ah                | 5001 619Ah                 | 5005 619Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 500D 519Ch                | 5001 619Ch                 | 5005 619Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 500D 519Eh                | 5001 619Eh                 | 5005 619Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 500D 51A4h                | 5001 61A4h                 | 5005 61A4h                 |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 500D 51A6h                | 5001 61A6h                 | 5005 61A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 500D 51A8h                | 5001 61A8h                 | 5005 61A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 500D 51AAh                | 5001 61AAh                 | 5005 61AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 500D 51ACh                | 5001 61ACh                 | 5005 61ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 500D 51AEh                | 5001 61AEh                 | 5005 61AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 500D 51B0h                | 5001 61B0h                 | 5005 61B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>       | 500D 51B2h                | 5001 61B2h                 | 5005 61B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>         | 500D 51F4h                | 5001 61F4h                 | 5005 61F4h                 |

**Table 3-800. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM3_G2 Physical Address | EPWM30_G2 Physical Address | EPWM31_G2 Physical Address |
|--------|--------|-------------------------------------|---------------------------|----------------------------|----------------------------|
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>      | 500D 51FAh                | 5001 61FAh                 | 5005 61FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>        | 500D 51FCh                | 5001 61FCh                 | 5005 61FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>       | 500D 5400h                | 5001 6400h                 | 5005 6400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>       | 500D 5410h                | 5001 6410h                 | 5005 6410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>          | 500D 5418h                | 5001 6418h                 | 5005 6418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a> | 500D 541Ch                | 5001 641Ch                 | 5005 641Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>   | 500D 5420h                | 5001 6420h                 | 5005 6420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>   | 500D 5428h                | 5001 6428h                 | 5005 6428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>   | 500D 5430h                | 5001 6430h                 | 5005 6430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>   | 500D 5600h                | 5001 6600h                 | 5005 6600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>   | 500D 5604h                | 5001 6604h                 | 5005 6604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>   | 500D 5608h                | 5001 6608h                 | 5005 6608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>   | 500D 560Ch                | 5001 660Ch                 | 5005 660Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>   | 500D 5610h                | 5001 6610h                 | 5005 6610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 500D 5614h                | 5001 6614h                 | 5005 6614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 500D 5618h                | 5001 6618h                 | 5005 6618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 500D 561Ch                | 5001 661Ch                 | 5005 661Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 500D 5620h                | 5001 6620h                 | 5005 6620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 500D 5630h                | 5001 6630h                 | 5005 6630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 500D 5632h                | 5001 6632h                 | 5005 6632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 500D 5644h                | 5001 6644h                 | 5005 6644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 500D 5680h                | 5001 6680h                 | 5005 6680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 500D 5684h                | 5001 6684h                 | 5005 6684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 500D 5688h                | 5001 6688h                 | 5005 6688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 500D 568Ch                | 5001 668Ch                 | 5005 668Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 500D 5690h                | 5001 6690h                 | 5005 6690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 500D 5694h                | 5001 6694h                 | 5005 6694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 500D 5698h                | 5001 6698h                 | 5005 6698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 500D 569Ch                | 5001 669Ch                 | 5005 669Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 500D 56A0h                | 5001 66A0h                 | 5005 66A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 500D 56B0h                | 5001 66B0h                 | 5005 66B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 500D 56B2h                | 5001 66B2h                 | 5005 66B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 500D 56BAh                | 5001 66BAh                 | 5005 66BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 500D 56BEh                | 5001 66BEh                 | 5005 66BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 500D 56C4h                | 5001 66C4h                 | 5005 66C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 500D 5700h                | 5001 6700h                 | 5005 6700h                 |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 500D 5704h                | 5001 6704h                 | 5005 6704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 500D 5708h                | 5001 6708h                 | 5005 6708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>    | 500D 570Ch                | 5001 670Ch                 | 5005 670Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>    | 500D 5710h                | 5001 6710h                 | 5005 6710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>    | 500D 5714h                | 5001 6714h                 | 5005 6714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>    | 500D 5718h                | 5001 6718h                 | 5005 6718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>    | 500D 571Ch                | 5001 671Ch                 | 5005 671Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>   | 500D 5720h                | 5001 6720h                 | 5005 6720h                 |

**Table 3-800. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM3_G2 Physical Address | EPWM30_G2 Physical Address | EPWM31_G2 Physical Address |
|--------|--------|------------------------------------|---------------------------|----------------------------|----------------------------|
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a> | 500D 5730h                | 5001 6730h                 | 5005 6730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a> | 500D 5732h                | 5001 6732h                 | 5005 6732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>    | 500D 573Ah                | 5001 673Ah                 | 5005 673Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>    | 500D 573Eh                | 5001 673Eh                 | 5005 673Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a> | 500D 5744h                | 5001 6744h                 | 5005 6744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 500D 5780h                | 5001 6780h                 | 5005 6780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 500D 5784h                | 5001 6784h                 | 5005 6784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 500D 5788h                | 5001 6788h                 | 5005 6788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 500D 578Ch                | 5001 678Ch                 | 5005 678Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 500D 5790h                | 5001 6790h                 | 5005 6790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 500D 5794h                | 5001 6794h                 | 5005 6794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 500D 5798h                | 5001 6798h                 | 5005 6798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 500D 579Ch                | 5001 679Ch                 | 5005 679Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 500D 57A0h                | 5001 67A0h                 | 5005 67A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 500D 57B0h                | 5001 67B0h                 | 5005 67B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 500D 57B2h                | 5001 67B2h                 | 5005 67B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 500D 57BAh                | 5001 67BAh                 | 5005 67BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 500D 57BEh                | 5001 67BEh                 | 5005 67BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 500D 57C4h                | 5001 67C4h                 | 5005 67C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 500D 5800h                | 5001 6800h                 | 5005 6800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 500D 5804h                | 5001 6804h                 | 5005 6804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 500D 5808h                | 5001 6808h                 | 5005 6808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 500D 580Ch                | 5001 680Ch                 | 5005 680Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 500D 5810h                | 5001 6810h                 | 5005 6810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 500D 5814h                | 5001 6814h                 | 5005 6814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 500D 5820h                | 5001 6820h                 | 5005 6820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 500D 5824h                | 5001 6824h                 | 5005 6824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 500D 5828h                | 5001 6828h                 | 5005 6828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 500D 582Ch                | 5001 682Ch                 | 5005 682Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>     | 500D 5C00h                | 5001 6C00h                 | 5005 6C00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 500D 5C04h                | 5001 6C04h                 | 5005 6C04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 500D 5C20h                | 5001 6C20h                 | 5005 6C20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 500D 5C24h                | 5001 6C24h                 | 5005 6C24h                 |

**Table 3-801. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM4_G2 Physical Address | EPWM5_G2 Physical Address | EPWM6_G2 Physical Address |
|--------|--------|------------------------------------|---------------------------|---------------------------|---------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5009 6000h                | 500D 6000h                | 5001 7000h                |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5009 6002h                | 500D 6002h                | 5001 7002h                |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5009 6006h                | 500D 6006h                | 5001 7006h                |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5009 6008h                | 500D 6008h                | 5001 7008h                |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5009 600Ah                | 500D 600Ah                | 5001 700Ah                |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 5009 600Ch                | 500D 600Ch                | 5001 700Ch                |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5009 600Eh                | 500D 600Eh                | 5001 700Eh                |

**Table 3-801. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                   | EPWM4_G2 Physical Address | EPWM5_G2 Physical Address | EPWM6_G2 Physical Address |
|--------|--------|---------------------------------|---------------------------|---------------------------|---------------------------|
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>     | 5009 6010h                | 500D 6010h                | 5001 7010h                |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>    | 5009 6012h                | 500D 6012h                | 5001 7012h                |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>      | 5009 6018h                | 500D 6018h                | 5001 7018h                |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>     | 5009 601Ah                | 500D 601Ah                | 5001 701Ah                |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>      | 5009 6020h                | 500D 6020h                | 5001 7020h                |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>  | 5009 6022h                | 500D 6022h                | 5001 7022h                |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>      | 5009 6028h                | 500D 6028h                | 5001 7028h                |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>    | 5009 6030h                | 500D 6030h                | 5001 7030h                |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>    | 5009 6032h                | 500D 6032h                | 5001 7032h                |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>     | 5009 6040h                | 500D 6040h                | 5001 7040h                |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>    | 5009 604Eh                | 500D 604Eh                | 5001 704Eh                |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>     | 5009 605Ah                | 500D 605Ah                | 5001 705Ah                |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>      | 5009 605Ch                | 500D 605Ch                | 5001 705Ch                |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>     | 5009 6068h                | 500D 6068h                | 5001 7068h                |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>     | 5009 606Ah                | 500D 606Ah                | 5001 706Ah                |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>  | 5009 6070h                | 500D 6070h                | 5001 7070h                |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a> | 5009 6074h                | 500D 6074h                | 5001 7074h                |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>      | 5009 607Ah                | 500D 607Ah                | 5001 707Ah                |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>    | 5009 607Ch                | 500D 607Ch                | 5001 707Ch                |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>   | 5009 607Eh                | 500D 607Eh                | 5001 707Eh                |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>     | 5009 6080h                | 500D 6080h                | 5001 7080h                |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>    | 5009 6082h                | 500D 6082h                | 5001 7082h                |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>     | 5009 6084h                | 500D 6084h                | 5001 7084h                |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>    | 5009 6086h                | 500D 6086h                | 5001 7086h                |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>     | 5009 608Eh                | 500D 608Eh                | 5001 708Eh                |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>    | 5009 6092h                | 500D 6092h                | 5001 7092h                |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>    | 5009 60A0h                | 500D 60A0h                | 5001 70A0h                |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>      | 5009 60A2h                | 500D 60A2h                | 5001 70A2h                |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>    | 5009 60A4h                | 500D 60A4h                | 5001 70A4h                |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>      | 5009 60A6h                | 500D 60A6h                | 5001 70A6h                |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>      | 5009 60C0h                | 500D 60C0h                | 5001 70C0h                |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>    | 5009 60C4h                | 500D 60C4h                | 5001 70C4h                |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>      | 5009 60C6h                | 500D 60C6h                | 5001 70C6h                |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>   | 5009 60C8h                | 500D 60C8h                | 5001 70C8h                |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>       | 5009 60D4h                | 500D 60D4h                | 5001 70D4h                |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>       | 5009 60D8h                | 500D 60D8h                | 5001 70D8h                |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>       | 5009 60DEh                | 500D 60DEh                | 5001 70DEh                |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>       | 5009 60E2h                | 500D 60E2h                | 5001 70E2h                |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>    | 5009 60E8h                | 500D 60E8h                | 5001 70E8h                |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>  | 5009 60EEh                | 500D 60EEh                | 5001 70EEh                |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>      | 5009 6100h                | 500D 6100h                | 5001 7100h                |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>     | 5009 6102h                | 500D 6102h                | 5001 7102h                |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>    | 5009 6104h                | 500D 6104h                | 5001 7104h                |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>      | 5009 6108h                | 500D 6108h                | 5001 7108h                |

**Table 3-801. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name         | EPWM4_G2 Physical Address | EPWM5_G2 Physical Address | EPWM6_G2 Physical Address |
|--------|--------|-----------------------|---------------------------|---------------------------|---------------------------|
| 10Ah   | 16     | EPWM_TZCTL2           | 5009 610Ah                | 500D 610Ah                | 5001 710Ah                |
| 10Ch   | 16     | EPWM_TZCTLDCA         | 5009 610Ch                | 500D 610Ch                | 5001 710Ch                |
| 10Eh   | 16     | EPWM_TZCTLDCB         | 5009 610Eh                | 500D 610Eh                | 5001 710Eh                |
| 11Ah   | 16     | EPWM_TZEINT           | 5009 611Ah                | 500D 611Ah                | 5001 711Ah                |
| 126h   | 16     | EPWM_TZFLG            | 5009 6126h                | 500D 6126h                | 5001 7126h                |
| 128h   | 16     | EPWM_TZCBCFLG         | 5009 6128h                | 500D 6128h                | 5001 7128h                |
| 12Ah   | 16     | EPWM_TZOSTFLG         | 5009 612Ah                | 500D 612Ah                | 5001 712Ah                |
| 12Eh   | 16     | EPWM_TZCLR            | 5009 612Eh                | 500D 612Eh                | 5001 712Eh                |
| 130h   | 16     | EPWM_TZCBCCLR         | 5009 6130h                | 500D 6130h                | 5001 7130h                |
| 132h   | 16     | EPWM_TZOSTCLR         | 5009 6132h                | 500D 6132h                | 5001 7132h                |
| 136h   | 16     | EPWM_TZFRC            | 5009 6136h                | 500D 6136h                | 5001 7136h                |
| 13Ah   | 16     | EPWM_TZTRIPOUTSEL     | 5009 613Ah                | 500D 613Ah                | 5001 713Ah                |
| 148h   | 16     | EPWM_ETSEL            | 5009 6148h                | 500D 6148h                | 5001 7148h                |
| 14Ch   | 16     | EPWM_ETPS             | 5009 614Ch                | 500D 614Ch                | 5001 714Ch                |
| 150h   | 16     | EPWM_ETFLG            | 5009 6150h                | 500D 6150h                | 5001 7150h                |
| 154h   | 16     | EPWM_ETCLR            | 5009 6154h                | 500D 6154h                | 5001 7154h                |
| 158h   | 16     | EPWM_ETFRC            | 5009 6158h                | 500D 6158h                | 5001 7158h                |
| 15Ch   | 16     | EPWM_ETINTPS          | 5009 615Ch                | 500D 615Ch                | 5001 715Ch                |
| 160h   | 16     | EPWM_ETSOCPS          | 5009 6160h                | 500D 6160h                | 5001 7160h                |
| 164h   | 16     | EPWM_ETCNTINITCTL     | 5009 6164h                | 500D 6164h                | 5001 7164h                |
| 168h   | 16     | EPWM_ETCNTINIT        | 5009 6168h                | 500D 6168h                | 5001 7168h                |
| 16Ch   | 16     | EPWM_ETINTMIXEN       | 5009 616Ch                | 500D 616Ch                | 5001 716Ch                |
| 170h   | 16     | EPWM_ETSOCAMIXEN      | 5009 6170h                | 500D 6170h                | 5001 7170h                |
| 174h   | 16     | EPWM_ETSOCBMIXEN      | 5009 6174h                | 500D 6174h                | 5001 7174h                |
| 180h   | 16     | EPWM_DCTRIPSEL        | 5009 6180h                | 500D 6180h                | 5001 7180h                |
| 186h   | 16     | EPWM_DCACTL           | 5009 6186h                | 500D 6186h                | 5001 7186h                |
| 188h   | 16     | EPWM_DCBCTL           | 5009 6188h                | 500D 6188h                | 5001 7188h                |
| 18Eh   | 16     | EPWM_DCFCTL           | 5009 618Eh                | 500D 618Eh                | 5001 718Eh                |
| 190h   | 16     | EPWM_DCCAPCTL         | 5009 6190h                | 500D 6190h                | 5001 7190h                |
| 192h   | 16     | EPWM_DCFOFFSET        | 5009 6192h                | 500D 6192h                | 5001 7192h                |
| 194h   | 16     | EPWM_DCFOFFSETCNT     | 5009 6194h                | 500D 6194h                | 5001 7194h                |
| 196h   | 16     | EPWM_DCFWINDOW        | 5009 6196h                | 500D 6196h                | 5001 7196h                |
| 198h   | 16     | EPWM_DCFWINDOWCNT     | 5009 6198h                | 500D 6198h                | 5001 7198h                |
| 19Ah   | 16     | EPWM_BLANKPULSEMIXSEL | 5009 619Ah                | 500D 619Ah                | 5001 719Ah                |
| 19Ch   | 16     | EPWM_DCCAPMIXSEL      | 5009 619Ch                | 500D 619Ch                | 5001 719Ch                |
| 19Eh   | 16     | EPWM_DCCAP            | 5009 619Eh                | 500D 619Eh                | 5001 719Eh                |
| 1A4h   | 16     | EPWM_DCAHTRIPSEL      | 5009 61A4h                | 500D 61A4h                | 5001 71A4h                |
| 1A6h   | 16     | EPWM_DCALTRIPSEL      | 5009 61A6h                | 500D 61A6h                | 5001 71A6h                |
| 1A8h   | 16     | EPWM_DCBHTRIPSEL      | 5009 61A8h                | 500D 61A8h                | 5001 71A8h                |
| 1AAh   | 16     | EPWM_DCBLTRIPSEL      | 5009 61AAh                | 500D 61AAh                | 5001 71AAh                |
| 1ACh   | 16     | EPWM_CAPCTL           | 5009 61ACh                | 500D 61ACh                | 5001 71ACh                |
| 1AEh   | 16     | EPWM_CAPGATETRIPSEL   | 5009 61AEh                | 500D 61AEh                | 5001 71AEh                |
| 1B0h   | 16     | EPWM_CAPINTRIPSEL     | 5009 61B0h                | 500D 61B0h                | 5001 71B0h                |
| 1B2h   | 16     | EPWM_CAPTRIPSEL       | 5009 61B2h                | 500D 61B2h                | 5001 71B2h                |

**Table 3-801. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM4_G2 Physical Address | EPWM5_G2 Physical Address | EPWM6_G2 Physical Address |
|--------|--------|-------------------------------------|---------------------------|---------------------------|---------------------------|
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>       | 5009 61F4h                | 500D 61F4h                | 5001 71F4h                |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>      | 5009 61FAh                | 500D 61FAh                | 5001 71FAh                |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>        | 5009 61FCh                | 500D 61FCh                | 5001 71FCh                |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>       | 5009 6400h                | 500D 6400h                | 5001 7400h                |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>       | 5009 6410h                | 500D 6410h                | 5001 7410h                |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>          | 5009 6418h                | 500D 6418h                | 5001 7418h                |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a> | 5009 641Ch                | 500D 641Ch                | 5001 741Ch                |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>   | 5009 6420h                | 500D 6420h                | 5001 7420h                |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>   | 5009 6428h                | 500D 6428h                | 5001 7428h                |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>   | 5009 6430h                | 500D 6430h                | 5001 7430h                |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>   | 5009 6600h                | 500D 6600h                | 5001 7600h                |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>   | 5009 6604h                | 500D 6604h                | 5001 7604h                |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>   | 5009 6608h                | 500D 6608h                | 5001 7608h                |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>   | 5009 660Ch                | 500D 660Ch                | 5001 760Ch                |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>   | 5009 6610h                | 500D 6610h                | 5001 7610h                |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 5009 6614h                | 500D 6614h                | 5001 7614h                |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 5009 6618h                | 500D 6618h                | 5001 7618h                |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 5009 661Ch                | 500D 661Ch                | 5001 761Ch                |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 5009 6620h                | 500D 6620h                | 5001 7620h                |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 5009 6630h                | 500D 6630h                | 5001 7630h                |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 5009 6632h                | 500D 6632h                | 5001 7632h                |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 5009 6644h                | 500D 6644h                | 5001 7644h                |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 5009 6680h                | 500D 6680h                | 5001 7680h                |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 5009 6684h                | 500D 6684h                | 5001 7684h                |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 5009 6688h                | 500D 6688h                | 5001 7688h                |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 5009 668Ch                | 500D 668Ch                | 5001 768Ch                |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 5009 6690h                | 500D 6690h                | 5001 7690h                |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 5009 6694h                | 500D 6694h                | 5001 7694h                |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 5009 6698h                | 500D 6698h                | 5001 7698h                |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 5009 669Ch                | 500D 669Ch                | 5001 769Ch                |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 5009 66A0h                | 500D 66A0h                | 5001 76A0h                |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 5009 66B0h                | 500D 66B0h                | 5001 76B0h                |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 5009 66B2h                | 500D 66B2h                | 5001 76B2h                |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 5009 66BAh                | 500D 66BAh                | 5001 76BAh                |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 5009 66BEh                | 500D 66BEh                | 5001 76BEh                |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 5009 66C4h                | 500D 66C4h                | 5001 76C4h                |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 5009 6700h                | 500D 6700h                | 5001 7700h                |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 5009 6704h                | 500D 6704h                | 5001 7704h                |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 5009 6708h                | 500D 6708h                | 5001 7708h                |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>    | 5009 670Ch                | 500D 670Ch                | 5001 770Ch                |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>    | 5009 6710h                | 500D 6710h                | 5001 7710h                |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>    | 5009 6714h                | 500D 6714h                | 5001 7714h                |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>    | 5009 6718h                | 500D 6718h                | 5001 7718h                |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>    | 5009 671Ch                | 500D 671Ch                | 5001 771Ch                |



**Table 3-801. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM4_G2 Physical Address | EPWM5_G2 Physical Address | EPWM6_G2 Physical Address |
|--------|--------|------------------------------------|---------------------------|---------------------------|---------------------------|
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>  | 5009 6720h                | 500D 6720h                | 5001 7720h                |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a> | 5009 6730h                | 500D 6730h                | 5001 7730h                |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a> | 5009 6732h                | 500D 6732h                | 5001 7732h                |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>    | 5009 673Ah                | 500D 673Ah                | 5001 773Ah                |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>    | 5009 673Eh                | 500D 673Eh                | 5001 773Eh                |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a> | 5009 6744h                | 500D 6744h                | 5001 7744h                |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 5009 6780h                | 500D 6780h                | 5001 7780h                |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 5009 6784h                | 500D 6784h                | 5001 7784h                |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 5009 6788h                | 500D 6788h                | 5001 7788h                |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 5009 678Ch                | 500D 678Ch                | 5001 778Ch                |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 5009 6790h                | 500D 6790h                | 5001 7790h                |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 5009 6794h                | 500D 6794h                | 5001 7794h                |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 5009 6798h                | 500D 6798h                | 5001 7798h                |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 5009 679Ch                | 500D 679Ch                | 5001 779Ch                |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 5009 67A0h                | 500D 67A0h                | 5001 77A0h                |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5009 67B0h                | 500D 67B0h                | 5001 77B0h                |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5009 67B2h                | 500D 67B2h                | 5001 77B2h                |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5009 67BAh                | 500D 67BAh                | 5001 77BAh                |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5009 67BEh                | 500D 67BEh                | 5001 77BEh                |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5009 67C4h                | 500D 67C4h                | 5001 77C4h                |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5009 6800h                | 500D 6800h                | 5001 7800h                |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5009 6804h                | 500D 6804h                | 5001 7804h                |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5009 6808h                | 500D 6808h                | 5001 7808h                |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5009 680Ch                | 500D 680Ch                | 5001 780Ch                |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 5009 6810h                | 500D 6810h                | 5001 7810h                |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5009 6814h                | 500D 6814h                | 5001 7814h                |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 5009 6820h                | 500D 6820h                | 5001 7820h                |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 5009 6824h                | 500D 6824h                | 5001 7824h                |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 5009 6828h                | 500D 6828h                | 5001 7828h                |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 5009 682Ch                | 500D 682Ch                | 5001 782Ch                |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>     | 5009 6C00h                | 500D 6C00h                | 5001 7C00h                |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 5009 6C04h                | 500D 6C04h                | 5001 7C04h                |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 5009 6C20h                | 500D 6C20h                | 5001 7C20h                |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 5009 6C24h                | 500D 6C24h                | 5001 7C24h                |

**Table 3-802. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM7_G2 Physical Address | EPWM8_G2 Physical Address | EPWM9_G2 Physical Address |
|--------|--------|------------------------------------|---------------------------|---------------------------|---------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5005 7000h                | 5009 7000h                | 500D 7000h                |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5005 7002h                | 5009 7002h                | 500D 7002h                |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5005 7006h                | 5009 7006h                | 500D 7006h                |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5005 7008h                | 5009 7008h                | 500D 7008h                |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5005 700Ah                | 5009 700Ah                | 500D 700Ah                |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNOUTEN</a>  | 5005 700Ch                | 5009 700Ch                | 500D 700Ch                |



**Table 3-802. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                   | EPWM7_G2 Physical Address | EPWM8_G2 Physical Address | EPWM9_G2 Physical Address |
|--------|--------|---------------------------------|---------------------------|---------------------------|---------------------------|
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>     | 5005 700Eh                | 5009 700Eh                | 500D 700Eh                |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>     | 5005 7010h                | 5009 7010h                | 500D 7010h                |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>    | 5005 7012h                | 5009 7012h                | 500D 7012h                |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>      | 5005 7018h                | 5009 7018h                | 500D 7018h                |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>     | 5005 701Ah                | 5009 701Ah                | 500D 701Ah                |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>      | 5005 7020h                | 5009 7020h                | 500D 7020h                |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>  | 5005 7022h                | 5009 7022h                | 500D 7022h                |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>      | 5005 7028h                | 5009 7028h                | 500D 7028h                |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>    | 5005 7030h                | 5009 7030h                | 500D 7030h                |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>    | 5005 7032h                | 5009 7032h                | 500D 7032h                |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>     | 5005 7040h                | 5009 7040h                | 500D 7040h                |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>    | 5005 704Eh                | 5009 704Eh                | 500D 704Eh                |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>     | 5005 705Ah                | 5009 705Ah                | 500D 705Ah                |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>      | 5005 705Ch                | 5009 705Ch                | 500D 705Ch                |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>     | 5005 7068h                | 5009 7068h                | 500D 7068h                |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>     | 5005 706Ah                | 5009 706Ah                | 500D 706Ah                |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>  | 5005 7070h                | 5009 7070h                | 500D 7070h                |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a> | 5005 7074h                | 5009 7074h                | 500D 7074h                |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>      | 5005 707Ah                | 5009 707Ah                | 500D 707Ah                |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>    | 5005 707Ch                | 5009 707Ch                | 500D 707Ch                |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>   | 5005 707Eh                | 5009 707Eh                | 500D 707Eh                |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>     | 5005 7080h                | 5009 7080h                | 500D 7080h                |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>    | 5005 7082h                | 5009 7082h                | 500D 7082h                |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>     | 5005 7084h                | 5009 7084h                | 500D 7084h                |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>    | 5005 7086h                | 5009 7086h                | 500D 7086h                |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>     | 5005 708Eh                | 5009 708Eh                | 500D 708Eh                |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>    | 5005 7092h                | 5009 7092h                | 500D 7092h                |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>    | 5005 70A0h                | 5009 70A0h                | 500D 70A0h                |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>      | 5005 70A2h                | 5009 70A2h                | 500D 70A2h                |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>    | 5005 70A4h                | 5009 70A4h                | 500D 70A4h                |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>      | 5005 70A6h                | 5009 70A6h                | 500D 70A6h                |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>      | 5005 70C0h                | 5009 70C0h                | 500D 70C0h                |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>    | 5005 70C4h                | 5009 70C4h                | 500D 70C4h                |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>      | 5005 70C6h                | 5009 70C6h                | 500D 70C6h                |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>   | 5005 70C8h                | 5009 70C8h                | 500D 70C8h                |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>       | 5005 70D4h                | 5009 70D4h                | 500D 70D4h                |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>       | 5005 70D8h                | 5009 70D8h                | 500D 70D8h                |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>       | 5005 70DEh                | 5009 70DEh                | 500D 70DEh                |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>       | 5005 70E2h                | 5009 70E2h                | 500D 70E2h                |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>    | 5005 70E8h                | 5009 70E8h                | 500D 70E8h                |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>  | 5005 70EEh                | 5009 70EEh                | 500D 70EEh                |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>      | 5005 7100h                | 5009 7100h                | 500D 7100h                |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>     | 5005 7102h                | 5009 7102h                | 500D 7102h                |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>    | 5005 7104h                | 5009 7104h                | 500D 7104h                |

**Table 3-802. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM7_G2 Physical Address | EPWM8_G2 Physical Address | EPWM9_G2 Physical Address |
|--------|--------|---------------------------------------|---------------------------|---------------------------|---------------------------|
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>            | 5005 7108h                | 5009 7108h                | 500D 7108h                |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>           | 5005 710Ah                | 5009 710Ah                | 500D 710Ah                |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>         | 5005 710Ch                | 5009 710Ch                | 500D 710Ch                |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>         | 5005 710Eh                | 5009 710Eh                | 500D 710Eh                |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>           | 5005 711Ah                | 5009 711Ah                | 500D 711Ah                |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>            | 5005 7126h                | 5009 7126h                | 500D 7126h                |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>         | 5005 7128h                | 5009 7128h                | 500D 7128h                |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>         | 5005 712Ah                | 5009 712Ah                | 500D 712Ah                |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>            | 5005 712Eh                | 5009 712Eh                | 500D 712Eh                |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>         | 5005 7130h                | 5009 7130h                | 500D 7130h                |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>         | 5005 7132h                | 5009 7132h                | 500D 7132h                |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>            | 5005 7136h                | 5009 7136h                | 500D 7136h                |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a>     | 5005 713Ah                | 5009 713Ah                | 500D 713Ah                |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>            | 5005 7148h                | 5009 7148h                | 500D 7148h                |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>             | 5005 714Ch                | 5009 714Ch                | 500D 714Ch                |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>            | 5005 7150h                | 5009 7150h                | 500D 7150h                |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>            | 5005 7154h                | 5009 7154h                | 500D 7154h                |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 5005 7158h                | 5009 7158h                | 500D 7158h                |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 5005 715Ch                | 5009 715Ch                | 500D 715Ch                |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 5005 7160h                | 5009 7160h                | 500D 7160h                |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 5005 7164h                | 5009 7164h                | 500D 7164h                |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 5005 7168h                | 5009 7168h                | 500D 7168h                |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 5005 716Ch                | 5009 716Ch                | 500D 716Ch                |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 5005 7170h                | 5009 7170h                | 500D 7170h                |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 5005 7174h                | 5009 7174h                | 500D 7174h                |
| 180h   | 16     | <a href="#">EPWM_DCTRISEL</a>         | 5005 7180h                | 5009 7180h                | 500D 7180h                |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 5005 7186h                | 5009 7186h                | 500D 7186h                |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5005 7188h                | 5009 7188h                | 500D 7188h                |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5005 718Eh                | 5009 718Eh                | 500D 718Eh                |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5005 7190h                | 5009 7190h                | 500D 7190h                |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5005 7192h                | 5009 7192h                | 500D 7192h                |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5005 7194h                | 5009 7194h                | 500D 7194h                |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5005 7196h                | 5009 7196h                | 500D 7196h                |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5005 7198h                | 5009 7198h                | 500D 7198h                |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5005 719Ah                | 5009 719Ah                | 500D 719Ah                |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5005 719Ch                | 5009 719Ch                | 500D 719Ch                |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5005 719Eh                | 5009 719Eh                | 500D 719Eh                |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5005 71A4h                | 5009 71A4h                | 500D 71A4h                |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5005 71A6h                | 5009 71A6h                | 500D 71A6h                |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 5005 71A8h                | 5009 71A8h                | 500D 71A8h                |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 5005 71AAh                | 5009 71AAh                | 500D 71AAh                |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 5005 71ACh                | 5009 71ACh                | 500D 71ACh                |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 5005 71AEh                | 5009 71AEh                | 500D 71AEh                |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>     | 5005 71B0h                | 5009 71B0h                | 500D 71B0h                |

**Table 3-802. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM7_G2 Physical Address | EPWM8_G2 Physical Address | EPWM9_G2 Physical Address |
|--------|--------|-------------------------------------|---------------------------|---------------------------|---------------------------|
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>     | 5005 71B2h                | 5009 71B2h                | 500D 71B2h                |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>       | 5005 71F4h                | 5009 71F4h                | 500D 71F4h                |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>      | 5005 71FAh                | 5009 71FAh                | 500D 71FAh                |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>        | 5005 71FCh                | 5009 71FCh                | 500D 71FCh                |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>       | 5005 7400h                | 5009 7400h                | 500D 7400h                |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>       | 5005 7410h                | 5009 7410h                | 500D 7410h                |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>          | 5005 7418h                | 5009 7418h                | 500D 7418h                |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a> | 5005 741Ch                | 5009 741Ch                | 500D 741Ch                |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>   | 5005 7420h                | 5009 7420h                | 500D 7420h                |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>   | 5005 7428h                | 5009 7428h                | 500D 7428h                |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>   | 5005 7430h                | 5009 7430h                | 500D 7430h                |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>   | 5005 7600h                | 5009 7600h                | 500D 7600h                |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>   | 5005 7604h                | 5009 7604h                | 500D 7604h                |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>   | 5005 7608h                | 5009 7608h                | 500D 7608h                |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>   | 5005 760Ch                | 5009 760Ch                | 500D 760Ch                |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>   | 5005 7610h                | 5009 7610h                | 500D 7610h                |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 5005 7614h                | 5009 7614h                | 500D 7614h                |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 5005 7618h                | 5009 7618h                | 500D 7618h                |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 5005 761Ch                | 5009 761Ch                | 500D 761Ch                |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 5005 7620h                | 5009 7620h                | 500D 7620h                |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 5005 7630h                | 5009 7630h                | 500D 7630h                |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 5005 7632h                | 5009 7632h                | 500D 7632h                |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 5005 7644h                | 5009 7644h                | 500D 7644h                |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 5005 7680h                | 5009 7680h                | 500D 7680h                |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 5005 7684h                | 5009 7684h                | 500D 7684h                |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 5005 7688h                | 5009 7688h                | 500D 7688h                |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 5005 768Ch                | 5009 768Ch                | 500D 768Ch                |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 5005 7690h                | 5009 7690h                | 500D 7690h                |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 5005 7694h                | 5009 7694h                | 500D 7694h                |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 5005 7698h                | 5009 7698h                | 500D 7698h                |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 5005 769Ch                | 5009 769Ch                | 500D 769Ch                |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 5005 76A0h                | 5009 76A0h                | 500D 76A0h                |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 5005 76B0h                | 5009 76B0h                | 500D 76B0h                |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 5005 76B2h                | 5009 76B2h                | 500D 76B2h                |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 5005 76BAh                | 5009 76BAh                | 500D 76BAh                |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 5005 76BEh                | 5009 76BEh                | 500D 76BEh                |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 5005 76C4h                | 5009 76C4h                | 500D 76C4h                |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 5005 7700h                | 5009 7700h                | 500D 7700h                |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 5005 7704h                | 5009 7704h                | 500D 7704h                |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 5005 7708h                | 5009 7708h                | 500D 7708h                |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>    | 5005 770Ch                | 5009 770Ch                | 500D 770Ch                |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>    | 5005 7710h                | 5009 7710h                | 500D 7710h                |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>    | 5005 7714h                | 5009 7714h                | 500D 7714h                |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>    | 5005 7718h                | 5009 7718h                | 500D 7718h                |

**Table 3-802. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM7_G2 Physical Address | EPWM8_G2 Physical Address | EPWM9_G2 Physical Address |
|--------|--------|------------------------------------|---------------------------|---------------------------|---------------------------|
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>   | 5005 771Ch                | 5009 771Ch                | 500D 771Ch                |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>  | 5005 7720h                | 5009 7720h                | 500D 7720h                |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a> | 5005 7730h                | 5009 7730h                | 500D 7730h                |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a> | 5005 7732h                | 5009 7732h                | 500D 7732h                |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>    | 5005 773Ah                | 5009 773Ah                | 500D 773Ah                |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>    | 5005 773Eh                | 5009 773Eh                | 500D 773Eh                |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a> | 5005 7744h                | 5009 7744h                | 500D 7744h                |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 5005 7780h                | 5009 7780h                | 500D 7780h                |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 5005 7784h                | 5009 7784h                | 500D 7784h                |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 5005 7788h                | 5009 7788h                | 500D 7788h                |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 5005 778Ch                | 5009 778Ch                | 500D 778Ch                |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 5005 7790h                | 5009 7790h                | 500D 7790h                |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 5005 7794h                | 5009 7794h                | 500D 7794h                |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 5005 7798h                | 5009 7798h                | 500D 7798h                |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 5005 779Ch                | 5009 779Ch                | 500D 779Ch                |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 5005 77A0h                | 5009 77A0h                | 500D 77A0h                |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5005 77B0h                | 5009 77B0h                | 500D 77B0h                |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5005 77B2h                | 5009 77B2h                | 500D 77B2h                |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5005 77BAh                | 5009 77BAh                | 500D 77BAh                |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5005 77BEh                | 5009 77BEh                | 500D 77BEh                |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5005 77C4h                | 5009 77C4h                | 500D 77C4h                |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5005 7800h                | 5009 7800h                | 500D 7800h                |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5005 7804h                | 5009 7804h                | 500D 7804h                |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5005 7808h                | 5009 7808h                | 500D 7808h                |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5005 780Ch                | 5009 780Ch                | 500D 780Ch                |
| 810h   | 32     | <a href="#">EPWM_DEFRFC</a>        | 5005 7810h                | 5009 7810h                | 500D 7810h                |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5005 7814h                | 5009 7814h                | 500D 7814h                |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 5005 7820h                | 5009 7820h                | 500D 7820h                |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 5005 7824h                | 5009 7824h                | 500D 7824h                |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 5005 7828h                | 5009 7828h                | 500D 7828h                |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 5005 782Ch                | 5009 782Ch                | 500D 782Ch                |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>     | 5005 7C00h                | 5009 7C00h                | 500D 7C00h                |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 5005 7C04h                | 5009 7C04h                | 500D 7C04h                |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 5005 7C20h                | 5009 7C20h                | 500D 7C20h                |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 5005 7C24h                | 5009 7C24h                | 500D 7C24h                |

**Table 3-803. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM0_G3 Physical Address | EPWM1_G3 Physical Address | EPWM10_G3 Physical Address |
|--------|--------|------------------------------------|---------------------------|---------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5001 8000h                | 5005 8000h                | 5009 8000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5001 8002h                | 5005 8002h                | 5009 8002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5001 8006h                | 5005 8006h                | 5009 8006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5001 8008h                | 5005 8008h                | 5009 8008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5001 800Ah                | 5005 800Ah                | 5009 800Ah                 |

**Table 3-803. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                     | EPWM0_G3 Physical Address | EPWM1_G3 Physical Address | EPWM10_G3 Physical Address |
|--------|--------|-----------------------------------|---------------------------|---------------------------|----------------------------|
| Ch     | 16     | <a href="#">EPWM_EPWMSYNOUTEN</a> | 5001 800Ch                | 5005 800Ch                | 5009 800Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>       | 5001 800Eh                | 5005 800Eh                | 5009 800Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>       | 5001 8010h                | 5005 8010h                | 5009 8010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>      | 5001 8012h                | 5005 8012h                | 5009 8012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>        | 5001 8018h                | 5005 8018h                | 5009 8018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>       | 5001 801Ah                | 5005 801Ah                | 5009 801Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>        | 5001 8020h                | 5005 8020h                | 5009 8020h                 |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>    | 5001 8022h                | 5005 8022h                | 5009 8022h                 |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>        | 5001 8028h                | 5005 8028h                | 5009 8028h                 |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>      | 5001 8030h                | 5005 8030h                | 5009 8030h                 |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>      | 5001 8032h                | 5005 8032h                | 5009 8032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>       | 5001 8040h                | 5005 8040h                | 5009 8040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>      | 5001 804Eh                | 5005 804Eh                | 5009 804Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>       | 5001 805Ah                | 5005 805Ah                | 5009 805Ah                 |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>        | 5001 805Ch                | 5005 805Ch                | 5009 805Ch                 |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>       | 5001 8068h                | 5005 8068h                | 5009 8068h                 |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>       | 5001 806Ah                | 5005 806Ah                | 5009 806Ah                 |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>    | 5001 8070h                | 5005 8070h                | 5009 8070h                 |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>   | 5001 8074h                | 5005 8074h                | 5009 8074h                 |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>        | 5001 807Ah                | 5005 807Ah                | 5009 807Ah                 |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>      | 5001 807Ch                | 5005 807Ch                | 5009 807Ch                 |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>     | 5001 807Eh                | 5005 807Eh                | 5009 807Eh                 |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>       | 5001 8080h                | 5005 8080h                | 5009 8080h                 |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>      | 5001 8082h                | 5005 8082h                | 5009 8082h                 |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>       | 5001 8084h                | 5005 8084h                | 5009 8084h                 |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>      | 5001 8086h                | 5005 8086h                | 5009 8086h                 |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>       | 5001 808Eh                | 5005 808Eh                | 5009 808Eh                 |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>      | 5001 8092h                | 5005 8092h                | 5009 8092h                 |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>      | 5001 80A0h                | 5005 80A0h                | 5009 80A0h                 |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>        | 5001 80A2h                | 5005 80A2h                | 5009 80A2h                 |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>      | 5001 80A4h                | 5005 80A4h                | 5009 80A4h                 |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>        | 5001 80A6h                | 5005 80A6h                | 5009 80A6h                 |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>        | 5001 80C0h                | 5005 80C0h                | 5009 80C0h                 |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>      | 5001 80C4h                | 5005 80C4h                | 5009 80C4h                 |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>        | 5001 80C6h                | 5005 80C6h                | 5009 80C6h                 |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>     | 5001 80C8h                | 5005 80C8h                | 5009 80C8h                 |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>         | 5001 80D4h                | 5005 80D4h                | 5009 80D4h                 |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>         | 5001 80D8h                | 5005 80D8h                | 5009 80D8h                 |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>         | 5001 80DEh                | 5005 80DEh                | 5009 80DEh                 |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>         | 5001 80E2h                | 5005 80E2h                | 5009 80E2h                 |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>      | 5001 80E8h                | 5005 80E8h                | 5009 80E8h                 |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>    | 5001 80EEh                | 5005 80EEh                | 5009 80EEh                 |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>        | 5001 8100h                | 5005 8100h                | 5009 8100h                 |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>       | 5001 8102h                | 5005 8102h                | 5009 8102h                 |

**Table 3-803. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM0_G3 Physical Address | EPWM1_G3 Physical Address | EPWM10_G3 Physical Address |
|--------|--------|---------------------------------------|---------------------------|---------------------------|----------------------------|
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>          | 5001 8104h                | 5005 8104h                | 5009 8104h                 |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>            | 5001 8108h                | 5005 8108h                | 5009 8108h                 |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>           | 5001 810Ah                | 5005 810Ah                | 5009 810Ah                 |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>         | 5001 810Ch                | 5005 810Ch                | 5009 810Ch                 |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>         | 5001 810Eh                | 5005 810Eh                | 5009 810Eh                 |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>           | 5001 811Ah                | 5005 811Ah                | 5009 811Ah                 |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>            | 5001 8126h                | 5005 8126h                | 5009 8126h                 |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>         | 5001 8128h                | 5005 8128h                | 5009 8128h                 |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>         | 5001 812Ah                | 5005 812Ah                | 5009 812Ah                 |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>            | 5001 812Eh                | 5005 812Eh                | 5009 812Eh                 |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>         | 5001 8130h                | 5005 8130h                | 5009 8130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>         | 5001 8132h                | 5005 8132h                | 5009 8132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>            | 5001 8136h                | 5005 8136h                | 5009 8136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a>     | 5001 813Ah                | 5005 813Ah                | 5009 813Ah                 |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>            | 5001 8148h                | 5005 8148h                | 5009 8148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>             | 5001 814Ch                | 5005 814Ch                | 5009 814Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>            | 5001 8150h                | 5005 8150h                | 5009 8150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>            | 5001 8154h                | 5005 8154h                | 5009 8154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 5001 8158h                | 5005 8158h                | 5009 8158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 5001 815Ch                | 5005 815Ch                | 5009 815Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 5001 8160h                | 5005 8160h                | 5009 8160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 5001 8164h                | 5005 8164h                | 5009 8164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 5001 8168h                | 5005 8168h                | 5009 8168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 5001 816Ch                | 5005 816Ch                | 5009 816Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 5001 8170h                | 5005 8170h                | 5009 8170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 5001 8174h                | 5005 8174h                | 5009 8174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 5001 8180h                | 5005 8180h                | 5009 8180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 5001 8186h                | 5005 8186h                | 5009 8186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5001 8188h                | 5005 8188h                | 5009 8188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5001 818Eh                | 5005 818Eh                | 5009 818Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5001 8190h                | 5005 8190h                | 5009 8190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5001 8192h                | 5005 8192h                | 5009 8192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5001 8194h                | 5005 8194h                | 5009 8194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5001 8196h                | 5005 8196h                | 5009 8196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5001 8198h                | 5005 8198h                | 5009 8198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5001 819Ah                | 5005 819Ah                | 5009 819Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5001 819Ch                | 5005 819Ch                | 5009 819Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5001 819Eh                | 5005 819Eh                | 5009 819Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5001 81A4h                | 5005 81A4h                | 5009 81A4h                 |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5001 81A6h                | 5005 81A6h                | 5009 81A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 5001 81A8h                | 5005 81A8h                | 5009 81A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 5001 81AAh                | 5005 81AAh                | 5009 81AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 5001 81ACh                | 5005 81ACh                | 5009 81ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a>   | 5001 81AEh                | 5005 81AEh                | 5009 81AEh                 |

**Table 3-803. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM0_G3 Physical Address | EPWM1_G3 Physical Address | EPWM10_G3 Physical Address |
|--------|--------|-------------------------------------|---------------------------|---------------------------|----------------------------|
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>   | 5001 81B0h                | 5005 81B0h                | 5009 81B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>     | 5001 81B2h                | 5005 81B2h                | 5009 81B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>       | 5001 81F4h                | 5005 81F4h                | 5009 81F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>      | 5001 81FAh                | 5005 81FAh                | 5009 81FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>        | 5001 81FCh                | 5005 81FCh                | 5009 81FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>       | 5001 8400h                | 5005 8400h                | 5009 8400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>       | 5001 8410h                | 5005 8410h                | 5009 8410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>          | 5001 8418h                | 5005 8418h                | 5009 8418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a> | 5001 841Ch                | 5005 841Ch                | 5009 841Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>   | 5001 8420h                | 5005 8420h                | 5009 8420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>   | 5001 8428h                | 5005 8428h                | 5009 8428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>   | 5001 8430h                | 5005 8430h                | 5009 8430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>   | 5001 8600h                | 5005 8600h                | 5009 8600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>   | 5001 8604h                | 5005 8604h                | 5009 8604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>   | 5001 8608h                | 5005 8608h                | 5009 8608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>   | 5001 860Ch                | 5005 860Ch                | 5009 860Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>   | 5001 8610h                | 5005 8610h                | 5009 8610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 5001 8614h                | 5005 8614h                | 5009 8614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 5001 8618h                | 5005 8618h                | 5009 8618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 5001 861Ch                | 5005 861Ch                | 5009 861Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 5001 8620h                | 5005 8620h                | 5009 8620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 5001 8630h                | 5005 8630h                | 5009 8630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 5001 8632h                | 5005 8632h                | 5009 8632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 5001 8644h                | 5005 8644h                | 5009 8644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 5001 8680h                | 5005 8680h                | 5009 8680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 5001 8684h                | 5005 8684h                | 5009 8684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 5001 8688h                | 5005 8688h                | 5009 8688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 5001 868Ch                | 5005 868Ch                | 5009 868Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 5001 8690h                | 5005 8690h                | 5009 8690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 5001 8694h                | 5005 8694h                | 5009 8694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 5001 8698h                | 5005 8698h                | 5009 8698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 5001 869Ch                | 5005 869Ch                | 5009 869Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 5001 86A0h                | 5005 86A0h                | 5009 86A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 5001 86B0h                | 5005 86B0h                | 5009 86B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 5001 86B2h                | 5005 86B2h                | 5009 86B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 5001 86BAh                | 5005 86BAh                | 5009 86BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 5001 86BEh                | 5005 86BEh                | 5009 86BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 5001 86C4h                | 5005 86C4h                | 5009 86C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 5001 8700h                | 5005 8700h                | 5009 8700h                 |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 5001 8704h                | 5005 8704h                | 5009 8704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 5001 8708h                | 5005 8708h                | 5009 8708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>    | 5001 870Ch                | 5005 870Ch                | 5009 870Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>    | 5001 8710h                | 5005 8710h                | 5009 8710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>    | 5001 8714h                | 5005 8714h                | 5009 8714h                 |



**Table 3-803. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM0_G3 Physical Address | EPWM1_G3 Physical Address | EPWM10_G3 Physical Address |
|--------|--------|------------------------------------|---------------------------|---------------------------|----------------------------|
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>   | 5001 8718h                | 5005 8718h                | 5009 8718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>   | 5001 871Ch                | 5005 871Ch                | 5009 871Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>  | 5001 8720h                | 5005 8720h                | 5009 8720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a> | 5001 8730h                | 5005 8730h                | 5009 8730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a> | 5001 8732h                | 5005 8732h                | 5009 8732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>    | 5001 873Ah                | 5005 873Ah                | 5009 873Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>    | 5001 873Eh                | 5005 873Eh                | 5009 873Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a> | 5001 8744h                | 5005 8744h                | 5009 8744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 5001 8780h                | 5005 8780h                | 5009 8780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 5001 8784h                | 5005 8784h                | 5009 8784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 5001 8788h                | 5005 8788h                | 5009 8788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 5001 878Ch                | 5005 878Ch                | 5009 878Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 5001 8790h                | 5005 8790h                | 5009 8790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 5001 8794h                | 5005 8794h                | 5009 8794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 5001 8798h                | 5005 8798h                | 5009 8798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 5001 879Ch                | 5005 879Ch                | 5009 879Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 5001 87A0h                | 5005 87A0h                | 5009 87A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5001 87B0h                | 5005 87B0h                | 5009 87B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5001 87B2h                | 5005 87B2h                | 5009 87B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5001 87BAh                | 5005 87BAh                | 5009 87BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5001 87BEh                | 5005 87BEh                | 5009 87BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5001 87C4h                | 5005 87C4h                | 5009 87C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5001 8800h                | 5005 8800h                | 5009 8800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5001 8804h                | 5005 8804h                | 5009 8804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5001 8808h                | 5005 8808h                | 5009 8808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5001 880Ch                | 5005 880Ch                | 5009 880Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 5001 8810h                | 5005 8810h                | 5009 8810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5001 8814h                | 5005 8814h                | 5009 8814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 5001 8820h                | 5005 8820h                | 5009 8820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 5001 8824h                | 5005 8824h                | 5009 8824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 5001 8828h                | 5005 8828h                | 5009 8828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 5001 882Ch                | 5005 882Ch                | 5009 882Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFG</a>      | 5001 8C00h                | 5005 8C00h                | 5009 8C00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 5001 8C04h                | 5005 8C04h                | 5009 8C04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 5001 8C20h                | 5005 8C20h                | 5009 8C20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 5001 8C24h                | 5005 8C24h                | 5009 8C24h                 |

**Table 3-804. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM11_G3 Physical Address | EPWM12_G3 Physical Address | EPWM13_G3 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 500D 8000h                 | 5001 9000h                 | 5005 9000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 500D 8002h                 | 5001 9002h                 | 5005 9002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 500D 8006h                 | 5001 9006h                 | 5005 9006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 500D 8008h                 | 5001 9008h                 | 5005 9008h                 |



**Table 3-804. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                     | EPWM11_G3 Physical Address | EPWM12_G3 Physical Address | EPWM13_G3 Physical Address |
|--------|--------|-----------------------------------|----------------------------|----------------------------|----------------------------|
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>        | 500D 800Ah                 | 5001 900Ah                 | 5005 900Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUEN</a> | 500D 800Ch                 | 5001 900Ch                 | 5005 900Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>       | 500D 800Eh                 | 5001 900Eh                 | 5005 900Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>       | 500D 8010h                 | 5001 9010h                 | 5005 9010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>      | 500D 8012h                 | 5001 9012h                 | 5005 9012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>        | 500D 8018h                 | 5001 9018h                 | 5005 9018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>       | 500D 801Ah                 | 5001 901Ah                 | 5005 901Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>        | 500D 8020h                 | 5001 9020h                 | 5005 9020h                 |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>    | 500D 8022h                 | 5001 9022h                 | 5005 9022h                 |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>        | 500D 8028h                 | 5001 9028h                 | 5005 9028h                 |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>      | 500D 8030h                 | 5001 9030h                 | 5005 9030h                 |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>      | 500D 8032h                 | 5001 9032h                 | 5005 9032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>       | 500D 8040h                 | 5001 9040h                 | 5005 9040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>      | 500D 804Eh                 | 5001 904Eh                 | 5005 904Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>       | 500D 805Ah                 | 5001 905Ah                 | 5005 905Ah                 |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>        | 500D 805Ch                 | 5001 905Ch                 | 5005 905Ch                 |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>       | 500D 8068h                 | 5001 9068h                 | 5005 9068h                 |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>       | 500D 806Ah                 | 5001 906Ah                 | 5005 906Ah                 |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>    | 500D 8070h                 | 5001 9070h                 | 5005 9070h                 |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>   | 500D 8074h                 | 5001 9074h                 | 5005 9074h                 |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>        | 500D 807Ah                 | 5001 907Ah                 | 5005 907Ah                 |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>      | 500D 807Ch                 | 5001 907Ch                 | 5005 907Ch                 |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>     | 500D 807Eh                 | 5001 907Eh                 | 5005 907Eh                 |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>       | 500D 8080h                 | 5001 9080h                 | 5005 9080h                 |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>      | 500D 8082h                 | 5001 9082h                 | 5005 9082h                 |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>       | 500D 8084h                 | 5001 9084h                 | 5005 9084h                 |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>      | 500D 8086h                 | 5001 9086h                 | 5005 9086h                 |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>       | 500D 808Eh                 | 5001 908Eh                 | 5005 908Eh                 |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>      | 500D 8092h                 | 5001 9092h                 | 5005 9092h                 |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>      | 500D 80A0h                 | 5001 90A0h                 | 5005 90A0h                 |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>        | 500D 80A2h                 | 5001 90A2h                 | 5005 90A2h                 |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>      | 500D 80A4h                 | 5001 90A4h                 | 5005 90A4h                 |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>        | 500D 80A6h                 | 5001 90A6h                 | 5005 90A6h                 |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>        | 500D 80C0h                 | 5001 90C0h                 | 5005 90C0h                 |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>      | 500D 80C4h                 | 5001 90C4h                 | 5005 90C4h                 |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>        | 500D 80C6h                 | 5001 90C6h                 | 5005 90C6h                 |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>     | 500D 80C8h                 | 5001 90C8h                 | 5005 90C8h                 |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>         | 500D 80D4h                 | 5001 90D4h                 | 5005 90D4h                 |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>         | 500D 80D8h                 | 5001 90D8h                 | 5005 90D8h                 |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>         | 500D 80DEh                 | 5001 90DEh                 | 5005 90DEh                 |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>         | 500D 80E2h                 | 5001 90E2h                 | 5005 90E2h                 |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>      | 500D 80E8h                 | 5001 90E8h                 | 5005 90E8h                 |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>    | 500D 80EEh                 | 5001 90EEh                 | 5005 90EEh                 |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>        | 500D 8100h                 | 5001 9100h                 | 5005 9100h                 |

**Table 3-804. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM11_G3 Physical Address | EPWM12_G3 Physical Address | EPWM13_G3 Physical Address |
|--------|--------|---------------------------------------|----------------------------|----------------------------|----------------------------|
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>           | 500D 8102h                 | 5001 9102h                 | 5005 9102h                 |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>          | 500D 8104h                 | 5001 9104h                 | 5005 9104h                 |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>            | 500D 8108h                 | 5001 9108h                 | 5005 9108h                 |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>           | 500D 810Ah                 | 5001 910Ah                 | 5005 910Ah                 |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>         | 500D 810Ch                 | 5001 910Ch                 | 5005 910Ch                 |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>         | 500D 810Eh                 | 5001 910Eh                 | 5005 910Eh                 |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>           | 500D 811Ah                 | 5001 911Ah                 | 5005 911Ah                 |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>            | 500D 8126h                 | 5001 9126h                 | 5005 9126h                 |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>         | 500D 8128h                 | 5001 9128h                 | 5005 9128h                 |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>         | 500D 812Ah                 | 5001 912Ah                 | 5005 912Ah                 |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>            | 500D 812Eh                 | 5001 912Eh                 | 5005 912Eh                 |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>         | 500D 8130h                 | 5001 9130h                 | 5005 9130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>         | 500D 8132h                 | 5001 9132h                 | 5005 9132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>            | 500D 8136h                 | 5001 9136h                 | 5005 9136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a>     | 500D 813Ah                 | 5001 913Ah                 | 5005 913Ah                 |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>            | 500D 8148h                 | 5001 9148h                 | 5005 9148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>             | 500D 814Ch                 | 5001 914Ch                 | 5005 914Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>            | 500D 8150h                 | 5001 9150h                 | 5005 9150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>            | 500D 8154h                 | 5001 9154h                 | 5005 9154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 500D 8158h                 | 5001 9158h                 | 5005 9158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 500D 815Ch                 | 5001 915Ch                 | 5005 915Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 500D 8160h                 | 5001 9160h                 | 5005 9160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 500D 8164h                 | 5001 9164h                 | 5005 9164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 500D 8168h                 | 5001 9168h                 | 5005 9168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 500D 816Ch                 | 5001 916Ch                 | 5005 916Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 500D 8170h                 | 5001 9170h                 | 5005 9170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 500D 8174h                 | 5001 9174h                 | 5005 9174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 500D 8180h                 | 5001 9180h                 | 5005 9180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 500D 8186h                 | 5001 9186h                 | 5005 9186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 500D 8188h                 | 5001 9188h                 | 5005 9188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 500D 818Eh                 | 5001 918Eh                 | 5005 918Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 500D 8190h                 | 5001 9190h                 | 5005 9190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 500D 8192h                 | 5001 9192h                 | 5005 9192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 500D 8194h                 | 5001 9194h                 | 5005 9194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 500D 8196h                 | 5001 9196h                 | 5005 9196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 500D 8198h                 | 5001 9198h                 | 5005 9198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 500D 819Ah                 | 5001 919Ah                 | 5005 919Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 500D 819Ch                 | 5001 919Ch                 | 5005 919Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 500D 819Eh                 | 5001 919Eh                 | 5005 919Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 500D 81A4h                 | 5001 91A4h                 | 5005 91A4h                 |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 500D 81A6h                 | 5001 91A6h                 | 5005 91A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 500D 81A8h                 | 5001 91A8h                 | 5005 91A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>      | 500D 81AAh                 | 5001 91AAh                 | 5005 91AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>           | 500D 81ACh                 | 5001 91ACh                 | 5005 91ACh                 |

**Table 3-804. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM11_G3 Physical Address | EPWM12_G3 Physical Address | EPWM13_G3 Physical Address |
|--------|--------|-------------------------------------|----------------------------|----------------------------|----------------------------|
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a> | 500D 81AEh                 | 5001 91AEh                 | 5005 91AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>   | 500D 81B0h                 | 5001 91B0h                 | 5005 91B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>     | 500D 81B2h                 | 5001 91B2h                 | 5005 91B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>       | 500D 81F4h                 | 5001 91F4h                 | 5005 91F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>      | 500D 81FAh                 | 5001 91FAh                 | 5005 91FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>        | 500D 81FCh                 | 5001 91FCh                 | 5005 91FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>       | 500D 8400h                 | 5001 9400h                 | 5005 9400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>       | 500D 8410h                 | 5001 9410h                 | 5005 9410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>          | 500D 8418h                 | 5001 9418h                 | 5005 9418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a> | 500D 841Ch                 | 5001 941Ch                 | 5005 941Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>   | 500D 8420h                 | 5001 9420h                 | 5005 9420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>   | 500D 8428h                 | 5001 9428h                 | 5005 9428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>   | 500D 8430h                 | 5001 9430h                 | 5005 9430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>   | 500D 8600h                 | 5001 9600h                 | 5005 9600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>   | 500D 8604h                 | 5001 9604h                 | 5005 9604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>   | 500D 8608h                 | 5001 9608h                 | 5005 9608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>   | 500D 860Ch                 | 5001 960Ch                 | 5005 960Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>   | 500D 8610h                 | 5001 9610h                 | 5005 9610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 500D 8614h                 | 5001 9614h                 | 5005 9614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 500D 8618h                 | 5001 9618h                 | 5005 9618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 500D 861Ch                 | 5001 961Ch                 | 5005 961Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 500D 8620h                 | 5001 9620h                 | 5005 9620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 500D 8630h                 | 5001 9630h                 | 5005 9630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 500D 8632h                 | 5001 9632h                 | 5005 9632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 500D 8644h                 | 5001 9644h                 | 5005 9644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 500D 8680h                 | 5001 9680h                 | 5005 9680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 500D 8684h                 | 5001 9684h                 | 5005 9684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 500D 8688h                 | 5001 9688h                 | 5005 9688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 500D 868Ch                 | 5001 968Ch                 | 5005 968Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 500D 8690h                 | 5001 9690h                 | 5005 9690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 500D 8694h                 | 5001 9694h                 | 5005 9694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 500D 8698h                 | 5001 9698h                 | 5005 9698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 500D 869Ch                 | 5001 969Ch                 | 5005 969Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 500D 86A0h                 | 5001 96A0h                 | 5005 96A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 500D 86B0h                 | 5001 96B0h                 | 5005 96B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 500D 86B2h                 | 5001 96B2h                 | 5005 96B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 500D 86BAh                 | 5001 96BAh                 | 5005 96BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 500D 86BEh                 | 5001 96BEh                 | 5005 96BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 500D 86C4h                 | 5001 96C4h                 | 5005 96C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 500D 8700h                 | 5001 9700h                 | 5005 9700h                 |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 500D 8704h                 | 5001 9704h                 | 5005 9704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 500D 8708h                 | 5001 9708h                 | 5005 9708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>    | 500D 870Ch                 | 5001 970Ch                 | 5005 970Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>    | 500D 8710h                 | 5001 9710h                 | 5005 9710h                 |

**Table 3-804. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM11_G3 Physical Address | EPWM12_G3 Physical Address | EPWM13_G3 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>   | 500D 8714h                 | 5001 9714h                 | 5005 9714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>   | 500D 8718h                 | 5001 9718h                 | 5005 9718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>   | 500D 871Ch                 | 5001 971Ch                 | 5005 971Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>  | 500D 8720h                 | 5001 9720h                 | 5005 9720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a> | 500D 8730h                 | 5001 9730h                 | 5005 9730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a> | 500D 8732h                 | 5001 9732h                 | 5005 9732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>    | 500D 873Ah                 | 5001 973Ah                 | 5005 973Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>    | 500D 873Eh                 | 5001 973Eh                 | 5005 973Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a> | 500D 8744h                 | 5001 9744h                 | 5005 9744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 500D 8780h                 | 5001 9780h                 | 5005 9780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 500D 8784h                 | 5001 9784h                 | 5005 9784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 500D 8788h                 | 5001 9788h                 | 5005 9788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 500D 878Ch                 | 5001 978Ch                 | 5005 978Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 500D 8790h                 | 5001 9790h                 | 5005 9790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 500D 8794h                 | 5001 9794h                 | 5005 9794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 500D 8798h                 | 5001 9798h                 | 5005 9798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 500D 879Ch                 | 5001 979Ch                 | 5005 979Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 500D 87A0h                 | 5001 97A0h                 | 5005 97A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 500D 87B0h                 | 5001 97B0h                 | 5005 97B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 500D 87B2h                 | 5001 97B2h                 | 5005 97B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 500D 87BAh                 | 5001 97BAh                 | 5005 97BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 500D 87BEh                 | 5001 97BEh                 | 5005 97BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 500D 87C4h                 | 5001 97C4h                 | 5005 97C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 500D 8800h                 | 5001 9800h                 | 5005 9800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 500D 8804h                 | 5001 9804h                 | 5005 9804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 500D 8808h                 | 5001 9808h                 | 5005 9808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 500D 880Ch                 | 5001 980Ch                 | 5005 980Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 500D 8810h                 | 5001 9810h                 | 5005 9810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 500D 8814h                 | 5001 9814h                 | 5005 9814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 500D 8820h                 | 5001 9820h                 | 5005 9820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 500D 8824h                 | 5001 9824h                 | 5005 9824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 500D 8828h                 | 5001 9828h                 | 5005 9828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 500D 882Ch                 | 5001 982Ch                 | 5005 982Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>     | 500D 8C00h                 | 5001 9C00h                 | 5005 9C00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 500D 8C04h                 | 5001 9C04h                 | 5005 9C04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 500D 8C20h                 | 5001 9C20h                 | 5005 9C20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 500D 8C24h                 | 5001 9C24h                 | 5005 9C24h                 |

**Table 3-805. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM14_G3 Physical Address | EPWM15_G3 Physical Address | EPWM16_G3 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5009 9000h                 | 500D 9000h                 | 5001 A000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5009 9002h                 | 500D 9002h                 | 5001 A002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5009 9006h                 | 500D 9006h                 | 5001 A006h                 |

**Table 3-805. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                     | EPWM14_G3 Physical Address | EPWM15_G3 Physical Address | EPWM16_G3 Physical Address |
|--------|--------|-----------------------------------|----------------------------|----------------------------|----------------------------|
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>        | 5009 9008h                 | 500D 9008h                 | 5001 A008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>        | 5009 900Ah                 | 500D 900Ah                 | 5001 A00Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUEN</a> | 5009 900Ch                 | 500D 900Ch                 | 5001 A00Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>       | 5009 900Eh                 | 500D 900Eh                 | 5001 A00Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>       | 5009 9010h                 | 500D 9010h                 | 5001 A010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>      | 5009 9012h                 | 500D 9012h                 | 5001 A012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>        | 5009 9018h                 | 500D 9018h                 | 5001 A018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>       | 5009 901Ah                 | 500D 901Ah                 | 5001 A01Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>        | 5009 9020h                 | 500D 9020h                 | 5001 A020h                 |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>    | 5009 9022h                 | 500D 9022h                 | 5001 A022h                 |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>        | 5009 9028h                 | 500D 9028h                 | 5001 A028h                 |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>      | 5009 9030h                 | 500D 9030h                 | 5001 A030h                 |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>      | 5009 9032h                 | 500D 9032h                 | 5001 A032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>       | 5009 9040h                 | 500D 9040h                 | 5001 A040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>      | 5009 904Eh                 | 500D 904Eh                 | 5001 A04Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>       | 5009 905Ah                 | 500D 905Ah                 | 5001 A05Ah                 |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>        | 5009 905Ch                 | 500D 905Ch                 | 5001 A05Ch                 |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>       | 5009 9068h                 | 500D 9068h                 | 5001 A068h                 |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>       | 5009 906Ah                 | 500D 906Ah                 | 5001 A06Ah                 |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>    | 5009 9070h                 | 500D 9070h                 | 5001 A070h                 |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>   | 5009 9074h                 | 500D 9074h                 | 5001 A074h                 |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>        | 5009 907Ah                 | 500D 907Ah                 | 5001 A07Ah                 |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>      | 5009 907Ch                 | 500D 907Ch                 | 5001 A07Ch                 |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>     | 5009 907Eh                 | 500D 907Eh                 | 5001 A07Eh                 |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>       | 5009 9080h                 | 500D 9080h                 | 5001 A080h                 |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>      | 5009 9082h                 | 500D 9082h                 | 5001 A082h                 |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>       | 5009 9084h                 | 500D 9084h                 | 5001 A084h                 |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>      | 5009 9086h                 | 500D 9086h                 | 5001 A086h                 |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>       | 5009 908Eh                 | 500D 908Eh                 | 5001 A08Eh                 |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>      | 5009 9092h                 | 500D 9092h                 | 5001 A092h                 |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>      | 5009 90A0h                 | 500D 90A0h                 | 5001 A0A0h                 |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>        | 5009 90A2h                 | 500D 90A2h                 | 5001 A0A2h                 |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>      | 5009 90A4h                 | 500D 90A4h                 | 5001 A0A4h                 |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>        | 5009 90A6h                 | 500D 90A6h                 | 5001 A0A6h                 |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>        | 5009 90C0h                 | 500D 90C0h                 | 5001 A0C0h                 |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>      | 5009 90C4h                 | 500D 90C4h                 | 5001 A0C4h                 |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>        | 5009 90C6h                 | 500D 90C6h                 | 5001 A0C6h                 |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>     | 5009 90C8h                 | 500D 90C8h                 | 5001 A0C8h                 |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>         | 5009 90D4h                 | 500D 90D4h                 | 5001 A0D4h                 |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>         | 5009 90D8h                 | 500D 90D8h                 | 5001 A0D8h                 |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>         | 5009 90DEh                 | 500D 90DEh                 | 5001 A0DEh                 |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>         | 5009 90E2h                 | 500D 90E2h                 | 5001 A0E2h                 |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>      | 5009 90E8h                 | 500D 90E8h                 | 5001 A0E8h                 |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>    | 5009 90EEh                 | 500D 90EEh                 | 5001 A0EEh                 |

**Table 3-805. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM14_G3 Physical Address | EPWM15_G3 Physical Address | EPWM16_G3 Physical Address |
|--------|--------|---------------------------------------|----------------------------|----------------------------|----------------------------|
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>            | 5009 9100h                 | 500D 9100h                 | 5001 A100h                 |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>           | 5009 9102h                 | 500D 9102h                 | 5001 A102h                 |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>          | 5009 9104h                 | 500D 9104h                 | 5001 A104h                 |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>            | 5009 9108h                 | 500D 9108h                 | 5001 A108h                 |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>           | 5009 910Ah                 | 500D 910Ah                 | 5001 A10Ah                 |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>         | 5009 910Ch                 | 500D 910Ch                 | 5001 A10Ch                 |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>         | 5009 910Eh                 | 500D 910Eh                 | 5001 A10Eh                 |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>           | 5009 911Ah                 | 500D 911Ah                 | 5001 A11Ah                 |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>            | 5009 9126h                 | 500D 9126h                 | 5001 A126h                 |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>         | 5009 9128h                 | 500D 9128h                 | 5001 A128h                 |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>         | 5009 912Ah                 | 500D 912Ah                 | 5001 A12Ah                 |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>            | 5009 912Eh                 | 500D 912Eh                 | 5001 A12Eh                 |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>         | 5009 9130h                 | 500D 9130h                 | 5001 A130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>         | 5009 9132h                 | 500D 9132h                 | 5001 A132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>            | 5009 9136h                 | 500D 9136h                 | 5001 A136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a>     | 5009 913Ah                 | 500D 913Ah                 | 5001 A13Ah                 |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>            | 5009 9148h                 | 500D 9148h                 | 5001 A148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>             | 5009 914Ch                 | 500D 914Ch                 | 5001 A14Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>            | 5009 9150h                 | 500D 9150h                 | 5001 A150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>            | 5009 9154h                 | 500D 9154h                 | 5001 A154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 5009 9158h                 | 500D 9158h                 | 5001 A158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 5009 915Ch                 | 500D 915Ch                 | 5001 A15Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 5009 9160h                 | 500D 9160h                 | 5001 A160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 5009 9164h                 | 500D 9164h                 | 5001 A164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 5009 9168h                 | 500D 9168h                 | 5001 A168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 5009 916Ch                 | 500D 916Ch                 | 5001 A16Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 5009 9170h                 | 500D 9170h                 | 5001 A170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 5009 9174h                 | 500D 9174h                 | 5001 A174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 5009 9180h                 | 500D 9180h                 | 5001 A180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 5009 9186h                 | 500D 9186h                 | 5001 A186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5009 9188h                 | 500D 9188h                 | 5001 A188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5009 918Eh                 | 500D 918Eh                 | 5001 A18Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5009 9190h                 | 500D 9190h                 | 5001 A190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5009 9192h                 | 500D 9192h                 | 5001 A192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5009 9194h                 | 500D 9194h                 | 5001 A194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5009 9196h                 | 500D 9196h                 | 5001 A196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5009 9198h                 | 500D 9198h                 | 5001 A198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5009 919Ah                 | 500D 919Ah                 | 5001 A19Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5009 919Ch                 | 500D 919Ch                 | 5001 A19Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5009 919Eh                 | 500D 919Eh                 | 5001 A19Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5009 91A4h                 | 500D 91A4h                 | 5001 A1A4h                 |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5009 91A6h                 | 500D 91A6h                 | 5001 A1A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 5009 91A8h                 | 500D 91A8h                 | 5001 A1A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCNLTRIPSEL</a>      | 5009 91AAh                 | 500D 91AAh                 | 5001 A1AAh                 |

**Table 3-805. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM14_G3 Physical Address | EPWM15_G3 Physical Address | EPWM16_G3 Physical Address |
|--------|--------|-------------------------------------|----------------------------|----------------------------|----------------------------|
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>         | 5009 91ACh                 | 500D 91ACh                 | 5001 A1ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a> | 5009 91AEh                 | 500D 91AEh                 | 5001 A1AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>   | 5009 91B0h                 | 500D 91B0h                 | 5001 A1B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>     | 5009 91B2h                 | 500D 91B2h                 | 5001 A1B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>       | 5009 91F4h                 | 500D 91F4h                 | 5001 A1F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>      | 5009 91FAh                 | 500D 91FAh                 | 5001 A1FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>        | 5009 91FCh                 | 500D 91FCh                 | 5001 A1FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>       | 5009 9400h                 | 500D 9400h                 | 5001 A400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>       | 5009 9410h                 | 500D 9410h                 | 5001 A410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>          | 5009 9418h                 | 500D 9418h                 | 5001 A418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a> | 5009 941Ch                 | 500D 941Ch                 | 5001 A41Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>   | 5009 9420h                 | 500D 9420h                 | 5001 A420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>   | 5009 9428h                 | 500D 9428h                 | 5001 A428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>   | 5009 9430h                 | 500D 9430h                 | 5001 A430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>   | 5009 9600h                 | 500D 9600h                 | 5001 A600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>   | 5009 9604h                 | 500D 9604h                 | 5001 A604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>   | 5009 9608h                 | 500D 9608h                 | 5001 A608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>   | 5009 960Ch                 | 500D 960Ch                 | 5001 A60Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>   | 5009 9610h                 | 500D 9610h                 | 5001 A610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 5009 9614h                 | 500D 9614h                 | 5001 A614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 5009 9618h                 | 500D 9618h                 | 5001 A618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 5009 961Ch                 | 500D 961Ch                 | 5001 A61Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 5009 9620h                 | 500D 9620h                 | 5001 A620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 5009 9630h                 | 500D 9630h                 | 5001 A630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 5009 9632h                 | 500D 9632h                 | 5001 A632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 5009 9644h                 | 500D 9644h                 | 5001 A644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 5009 9680h                 | 500D 9680h                 | 5001 A680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 5009 9684h                 | 500D 9684h                 | 5001 A684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 5009 9688h                 | 500D 9688h                 | 5001 A688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 5009 968Ch                 | 500D 968Ch                 | 5001 A68Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 5009 9690h                 | 500D 9690h                 | 5001 A690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 5009 9694h                 | 500D 9694h                 | 5001 A694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 5009 9698h                 | 500D 9698h                 | 5001 A698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 5009 969Ch                 | 500D 969Ch                 | 5001 A69Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 5009 96A0h                 | 500D 96A0h                 | 5001 A6A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 5009 96B0h                 | 500D 96B0h                 | 5001 A6B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 5009 96B2h                 | 500D 96B2h                 | 5001 A6B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 5009 96BAh                 | 500D 96BAh                 | 5001 A6BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 5009 96BEh                 | 500D 96BEh                 | 5001 A6BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 5009 96C4h                 | 500D 96C4h                 | 5001 A6C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 5009 9700h                 | 500D 9700h                 | 5001 A700h                 |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 5009 9704h                 | 500D 9704h                 | 5001 A704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 5009 9708h                 | 500D 9708h                 | 5001 A708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>    | 5009 970Ch                 | 500D 970Ch                 | 5001 A70Ch                 |



**Table 3-805. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM14_G3 Physical Address | EPWM15_G3 Physical Address | EPWM16_G3 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>   | 5009 9710h                 | 500D 9710h                 | 5001 A710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>   | 5009 9714h                 | 500D 9714h                 | 5001 A714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>   | 5009 9718h                 | 500D 9718h                 | 5001 A718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>   | 5009 971Ch                 | 500D 971Ch                 | 5001 A71Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>  | 5009 9720h                 | 500D 9720h                 | 5001 A720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a> | 5009 9730h                 | 500D 9730h                 | 5001 A730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a> | 5009 9732h                 | 500D 9732h                 | 5001 A732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>    | 5009 973Ah                 | 500D 973Ah                 | 5001 A73Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>    | 5009 973Eh                 | 500D 973Eh                 | 5001 A73Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a> | 5009 9744h                 | 500D 9744h                 | 5001 A744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 5009 9780h                 | 500D 9780h                 | 5001 A780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 5009 9784h                 | 500D 9784h                 | 5001 A784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 5009 9788h                 | 500D 9788h                 | 5001 A788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 5009 978Ch                 | 500D 978Ch                 | 5001 A78Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 5009 9790h                 | 500D 9790h                 | 5001 A790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 5009 9794h                 | 500D 9794h                 | 5001 A794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 5009 9798h                 | 500D 9798h                 | 5001 A798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 5009 979Ch                 | 500D 979Ch                 | 5001 A79Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 5009 97A0h                 | 500D 97A0h                 | 5001 A7A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5009 97B0h                 | 500D 97B0h                 | 5001 A7B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5009 97B2h                 | 500D 97B2h                 | 5001 A7B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5009 97BAh                 | 500D 97BAh                 | 5001 A7BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5009 97BEh                 | 500D 97BEh                 | 5001 A7BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5009 97C4h                 | 500D 97C4h                 | 5001 A7C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5009 9800h                 | 500D 9800h                 | 5001 A800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5009 9804h                 | 500D 9804h                 | 5001 A804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5009 9808h                 | 500D 9808h                 | 5001 A808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5009 980Ch                 | 500D 980Ch                 | 5001 A80Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 5009 9810h                 | 500D 9810h                 | 5001 A810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5009 9814h                 | 500D 9814h                 | 5001 A814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 5009 9820h                 | 500D 9820h                 | 5001 A820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 5009 9824h                 | 500D 9824h                 | 5001 A824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 5009 9828h                 | 500D 9828h                 | 5001 A828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 5009 982Ch                 | 500D 982Ch                 | 5001 A82Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>     | 5009 9C00h                 | 500D 9C00h                 | 5001 AC00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 5009 9C04h                 | 500D 9C04h                 | 5001 AC04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 5009 9C20h                 | 500D 9C20h                 | 5001 AC20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 5009 9C24h                 | 500D 9C24h                 | 5001 AC24h                 |

**Table 3-806. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name               | EPWM17_G3 Physical Address | EPWM18_G3 Physical Address | EPWM19_G3 Physical Address |
|--------|--------|-----------------------------|----------------------------|----------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>  | 5005 A000h                 | 5009 A000h                 | 500D A000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a> | 5005 A002h                 | 5009 A002h                 | 500D A002h                 |



**Table 3-806. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM17_G3 Physical Address | EPWM18_G3 Physical Address | EPWM19_G3 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5005 A006h                 | 5009 A006h                 | 500D A006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5005 A008h                 | 5009 A008h                 | 500D A008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5005 A00Ah                 | 5009 A00Ah                 | 500D A00Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 5005 A00Ch                 | 5009 A00Ch                 | 500D A00Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5005 A00Eh                 | 5009 A00Eh                 | 500D A00Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5005 A010h                 | 5009 A010h                 | 500D A010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5005 A012h                 | 5009 A012h                 | 500D A012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 5005 A018h                 | 5009 A018h                 | 500D A018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 5005 A01Ah                 | 5009 A01Ah                 | 500D A01Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 5005 A020h                 | 5009 A020h                 | 500D A020h                 |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 5005 A022h                 | 5009 A022h                 | 500D A022h                 |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 5005 A028h                 | 5009 A028h                 | 500D A028h                 |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 5005 A030h                 | 5009 A030h                 | 500D A030h                 |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 5005 A032h                 | 5009 A032h                 | 500D A032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 5005 A040h                 | 5009 A040h                 | 500D A040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 5005 A04Eh                 | 5009 A04Eh                 | 500D A04Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>        | 5005 A05Ah                 | 5009 A05Ah                 | 500D A05Ah                 |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>         | 5005 A05Ch                 | 5009 A05Ch                 | 500D A05Ch                 |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>        | 5005 A068h                 | 5009 A068h                 | 500D A068h                 |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>        | 5005 A06Ah                 | 5009 A06Ah                 | 500D A06Ah                 |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>     | 5005 A070h                 | 5009 A070h                 | 500D A070h                 |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>    | 5005 A074h                 | 5009 A074h                 | 500D A074h                 |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>         | 5005 A07Ah                 | 5009 A07Ah                 | 500D A07Ah                 |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>       | 5005 A07Ch                 | 5009 A07Ch                 | 500D A07Ch                 |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>      | 5005 A07Eh                 | 5009 A07Eh                 | 500D A07Eh                 |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>        | 5005 A080h                 | 5009 A080h                 | 500D A080h                 |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>       | 5005 A082h                 | 5009 A082h                 | 500D A082h                 |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>        | 5005 A084h                 | 5009 A084h                 | 500D A084h                 |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>       | 5005 A086h                 | 5009 A086h                 | 500D A086h                 |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>        | 5005 A08Eh                 | 5009 A08Eh                 | 500D A08Eh                 |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>       | 5005 A092h                 | 5009 A092h                 | 500D A092h                 |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>       | 5005 A0A0h                 | 5009 A0A0h                 | 500D A0A0h                 |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>         | 5005 A0A2h                 | 5009 A0A2h                 | 500D A0A2h                 |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>       | 5005 A0A4h                 | 5009 A0A4h                 | 500D A0A4h                 |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>         | 5005 A0A6h                 | 5009 A0A6h                 | 500D A0A6h                 |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>         | 5005 A0C0h                 | 5009 A0C0h                 | 500D A0C0h                 |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>       | 5005 A0C4h                 | 5009 A0C4h                 | 500D A0C4h                 |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>         | 5005 A0C6h                 | 5009 A0C6h                 | 500D A0C6h                 |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>      | 5005 A0C8h                 | 5009 A0C8h                 | 500D A0C8h                 |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>          | 5005 A0D4h                 | 5009 A0D4h                 | 500D A0D4h                 |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>          | 5005 A0D8h                 | 5009 A0D8h                 | 500D A0D8h                 |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>          | 5005 A0DEh                 | 5009 A0DEh                 | 500D A0DEh                 |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>          | 5005 A0E2h                 | 5009 A0E2h                 | 500D A0E2h                 |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>       | 5005 A0E8h                 | 5009 A0E8h                 | 500D A0E8h                 |

**Table 3-806. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM17_G3 Physical Address | EPWM18_G3 Physical Address | EPWM19_G3 Physical Address |
|--------|--------|---------------------------------------|----------------------------|----------------------------|----------------------------|
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>        | 5005 A0EEh                 | 5009 A0EEh                 | 500D A0EEh                 |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>            | 5005 A100h                 | 5009 A100h                 | 500D A100h                 |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>           | 5005 A102h                 | 5009 A102h                 | 500D A102h                 |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>          | 5005 A104h                 | 5009 A104h                 | 500D A104h                 |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>            | 5005 A108h                 | 5009 A108h                 | 500D A108h                 |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>           | 5005 A10Ah                 | 5009 A10Ah                 | 500D A10Ah                 |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>         | 5005 A10Ch                 | 5009 A10Ch                 | 500D A10Ch                 |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>         | 5005 A10Eh                 | 5009 A10Eh                 | 500D A10Eh                 |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>           | 5005 A11Ah                 | 5009 A11Ah                 | 500D A11Ah                 |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>            | 5005 A126h                 | 5009 A126h                 | 500D A126h                 |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>         | 5005 A128h                 | 5009 A128h                 | 500D A128h                 |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>         | 5005 A12Ah                 | 5009 A12Ah                 | 500D A12Ah                 |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>            | 5005 A12Eh                 | 5009 A12Eh                 | 500D A12Eh                 |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>         | 5005 A130h                 | 5009 A130h                 | 500D A130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>         | 5005 A132h                 | 5009 A132h                 | 500D A132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>            | 5005 A136h                 | 5009 A136h                 | 500D A136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a>     | 5005 A13Ah                 | 5009 A13Ah                 | 500D A13Ah                 |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>            | 5005 A148h                 | 5009 A148h                 | 500D A148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>             | 5005 A14Ch                 | 5009 A14Ch                 | 500D A14Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>            | 5005 A150h                 | 5009 A150h                 | 500D A150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>            | 5005 A154h                 | 5009 A154h                 | 500D A154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 5005 A158h                 | 5009 A158h                 | 500D A158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 5005 A15Ch                 | 5009 A15Ch                 | 500D A15Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 5005 A160h                 | 5009 A160h                 | 500D A160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 5005 A164h                 | 5009 A164h                 | 500D A164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 5005 A168h                 | 5009 A168h                 | 500D A168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 5005 A16Ch                 | 5009 A16Ch                 | 500D A16Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 5005 A170h                 | 5009 A170h                 | 500D A170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 5005 A174h                 | 5009 A174h                 | 500D A174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 5005 A180h                 | 5009 A180h                 | 500D A180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 5005 A186h                 | 5009 A186h                 | 500D A186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5005 A188h                 | 5009 A188h                 | 500D A188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5005 A18Eh                 | 5009 A18Eh                 | 500D A18Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5005 A190h                 | 5009 A190h                 | 500D A190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5005 A192h                 | 5009 A192h                 | 500D A192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5005 A194h                 | 5009 A194h                 | 500D A194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5005 A196h                 | 5009 A196h                 | 500D A196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5005 A198h                 | 5009 A198h                 | 500D A198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5005 A19Ah                 | 5009 A19Ah                 | 500D A19Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5005 A19Ch                 | 5009 A19Ch                 | 500D A19Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5005 A19Eh                 | 5009 A19Eh                 | 500D A19Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5005 A1A4h                 | 5009 A1A4h                 | 500D A1A4h                 |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5005 A1A6h                 | 5009 A1A6h                 | 500D A1A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 5005 A1A8h                 | 5009 A1A8h                 | 500D A1A8h                 |

**Table 3-806. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM17_G3 Physical Address | EPWM18_G3 Physical Address | EPWM19_G3 Physical Address |
|--------|--------|-------------------------------------|----------------------------|----------------------------|----------------------------|
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>    | 5005 A1AAh                 | 5009 A1AAh                 | 500D A1AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>         | 5005 A1ACh                 | 5009 A1ACh                 | 500D A1ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a> | 5005 A1AEh                 | 5009 A1AEh                 | 500D A1AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>   | 5005 A1B0h                 | 5009 A1B0h                 | 500D A1B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>     | 5005 A1B2h                 | 5009 A1B2h                 | 500D A1B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>       | 5005 A1F4h                 | 5009 A1F4h                 | 500D A1F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>      | 5005 A1FAh                 | 5009 A1FAh                 | 500D A1FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>        | 5005 A1FCh                 | 5009 A1FCh                 | 500D A1FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>       | 5005 A400h                 | 5009 A400h                 | 500D A400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>       | 5005 A410h                 | 5009 A410h                 | 500D A410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>          | 5005 A418h                 | 5009 A418h                 | 500D A418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a> | 5005 A41Ch                 | 5009 A41Ch                 | 500D A41Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>   | 5005 A420h                 | 5009 A420h                 | 500D A420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>   | 5005 A428h                 | 5009 A428h                 | 500D A428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>   | 5005 A430h                 | 5009 A430h                 | 500D A430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>   | 5005 A600h                 | 5009 A600h                 | 500D A600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>   | 5005 A604h                 | 5009 A604h                 | 500D A604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>   | 5005 A608h                 | 5009 A608h                 | 500D A608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>   | 5005 A60Ch                 | 5009 A60Ch                 | 500D A60Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>   | 5005 A610h                 | 5009 A610h                 | 500D A610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 5005 A614h                 | 5009 A614h                 | 500D A614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 5005 A618h                 | 5009 A618h                 | 500D A618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 5005 A61Ch                 | 5009 A61Ch                 | 500D A61Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 5005 A620h                 | 5009 A620h                 | 500D A620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 5005 A630h                 | 5009 A630h                 | 500D A630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 5005 A632h                 | 5009 A632h                 | 500D A632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 5005 A644h                 | 5009 A644h                 | 500D A644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 5005 A680h                 | 5009 A680h                 | 500D A680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 5005 A684h                 | 5009 A684h                 | 500D A684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 5005 A688h                 | 5009 A688h                 | 500D A688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 5005 A68Ch                 | 5009 A68Ch                 | 500D A68Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 5005 A690h                 | 5009 A690h                 | 500D A690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 5005 A694h                 | 5009 A694h                 | 500D A694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 5005 A698h                 | 5009 A698h                 | 500D A698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 5005 A69Ch                 | 5009 A69Ch                 | 500D A69Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 5005 A6A0h                 | 5009 A6A0h                 | 500D A6A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 5005 A6B0h                 | 5009 A6B0h                 | 500D A6B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 5005 A6B2h                 | 5009 A6B2h                 | 500D A6B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 5005 A6BAh                 | 5009 A6BAh                 | 500D A6BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 5005 A6BEh                 | 5009 A6BEh                 | 500D A6BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 5005 A6C4h                 | 5009 A6C4h                 | 500D A6C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 5005 A700h                 | 5009 A700h                 | 500D A700h                 |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 5005 A704h                 | 5009 A704h                 | 500D A704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 5005 A708h                 | 5009 A708h                 | 500D A708h                 |

**Table 3-806. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM17_G3 Physical Address | EPWM18_G3 Physical Address | EPWM19_G3 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>   | 5005 A70Ch                 | 5009 A70Ch                 | 500D A70Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>   | 5005 A710h                 | 5009 A710h                 | 500D A710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>   | 5005 A714h                 | 5009 A714h                 | 500D A714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>   | 5005 A718h                 | 5009 A718h                 | 500D A718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>   | 5005 A71Ch                 | 5009 A71Ch                 | 500D A71Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>  | 5005 A720h                 | 5009 A720h                 | 500D A720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a> | 5005 A730h                 | 5009 A730h                 | 500D A730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a> | 5005 A732h                 | 5009 A732h                 | 500D A732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>    | 5005 A73Ah                 | 5009 A73Ah                 | 500D A73Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>    | 5005 A73Eh                 | 5009 A73Eh                 | 500D A73Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a> | 5005 A744h                 | 5009 A744h                 | 500D A744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 5005 A780h                 | 5009 A780h                 | 500D A780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 5005 A784h                 | 5009 A784h                 | 500D A784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 5005 A788h                 | 5009 A788h                 | 500D A788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 5005 A78Ch                 | 5009 A78Ch                 | 500D A78Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 5005 A790h                 | 5009 A790h                 | 500D A790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 5005 A794h                 | 5009 A794h                 | 500D A794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 5005 A798h                 | 5009 A798h                 | 500D A798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 5005 A79Ch                 | 5009 A79Ch                 | 500D A79Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 5005 A7A0h                 | 5009 A7A0h                 | 500D A7A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5005 A7B0h                 | 5009 A7B0h                 | 500D A7B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5005 A7B2h                 | 5009 A7B2h                 | 500D A7B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5005 A7BAh                 | 5009 A7BAh                 | 500D A7BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5005 A7BEh                 | 5009 A7BEh                 | 500D A7BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5005 A7C4h                 | 5009 A7C4h                 | 500D A7C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5005 A800h                 | 5009 A800h                 | 500D A800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5005 A804h                 | 5009 A804h                 | 500D A804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5005 A808h                 | 5009 A808h                 | 500D A808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5005 A80Ch                 | 5009 A80Ch                 | 500D A80Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 5005 A810h                 | 5009 A810h                 | 500D A810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5005 A814h                 | 5009 A814h                 | 500D A814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 5005 A820h                 | 5009 A820h                 | 500D A820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 5005 A824h                 | 5009 A824h                 | 500D A824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 5005 A828h                 | 5009 A828h                 | 500D A828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 5005 A82Ch                 | 5009 A82Ch                 | 500D A82Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>     | 5005 AC00h                 | 5009 AC00h                 | 500D AC00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 5005 AC04h                 | 5009 AC04h                 | 500D AC04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 5005 AC20h                 | 5009 AC20h                 | 500D AC20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 5005 AC24h                 | 5009 AC24h                 | 500D AC24h                 |

**Table 3-807. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name              | EPWM2_G3 Physical Address | EPWM20_G3 Physical Address | EPWM21_G3 Physical Address |
|--------|--------|----------------------------|---------------------------|----------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a> | 5001 B000h                | 5005 B000h                 | 5009 B000h                 |

**Table 3-807. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM2_G3 Physical Address | EPWM20_G3 Physical Address | EPWM21_G3 Physical Address |
|--------|--------|------------------------------------|---------------------------|----------------------------|----------------------------|
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5001 B002h                | 5005 B002h                 | 5009 B002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5001 B006h                | 5005 B006h                 | 5009 B006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5001 B008h                | 5005 B008h                 | 5009 B008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5001 B00Ah                | 5005 B00Ah                 | 5009 B00Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 5001 B00Ch                | 5005 B00Ch                 | 5009 B00Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5001 B00Eh                | 5005 B00Eh                 | 5009 B00Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5001 B010h                | 5005 B010h                 | 5009 B010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5001 B012h                | 5005 B012h                 | 5009 B012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 5001 B018h                | 5005 B018h                 | 5009 B018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 5001 B01Ah                | 5005 B01Ah                 | 5009 B01Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 5001 B020h                | 5005 B020h                 | 5009 B020h                 |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 5001 B022h                | 5005 B022h                 | 5009 B022h                 |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 5001 B028h                | 5005 B028h                 | 5009 B028h                 |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 5001 B030h                | 5005 B030h                 | 5009 B030h                 |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 5001 B032h                | 5005 B032h                 | 5009 B032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 5001 B040h                | 5005 B040h                 | 5009 B040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 5001 B04Eh                | 5005 B04Eh                 | 5009 B04Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>        | 5001 B05Ah                | 5005 B05Ah                 | 5009 B05Ah                 |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>         | 5001 B05Ch                | 5005 B05Ch                 | 5009 B05Ch                 |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>        | 5001 B068h                | 5005 B068h                 | 5009 B068h                 |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>        | 5001 B06Ah                | 5005 B06Ah                 | 5009 B06Ah                 |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>     | 5001 B070h                | 5005 B070h                 | 5009 B070h                 |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>    | 5001 B074h                | 5005 B074h                 | 5009 B074h                 |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>         | 5001 B07Ah                | 5005 B07Ah                 | 5009 B07Ah                 |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>       | 5001 B07Ch                | 5005 B07Ch                 | 5009 B07Ch                 |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>      | 5001 B07Eh                | 5005 B07Eh                 | 5009 B07Eh                 |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>        | 5001 B080h                | 5005 B080h                 | 5009 B080h                 |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>       | 5001 B082h                | 5005 B082h                 | 5009 B082h                 |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>        | 5001 B084h                | 5005 B084h                 | 5009 B084h                 |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>       | 5001 B086h                | 5005 B086h                 | 5009 B086h                 |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>        | 5001 B08Eh                | 5005 B08Eh                 | 5009 B08Eh                 |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>       | 5001 B092h                | 5005 B092h                 | 5009 B092h                 |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>       | 5001 B0A0h                | 5005 B0A0h                 | 5009 B0A0h                 |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>         | 5001 B0A2h                | 5005 B0A2h                 | 5009 B0A2h                 |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>       | 5001 B0A4h                | 5005 B0A4h                 | 5009 B0A4h                 |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>         | 5001 B0A6h                | 5005 B0A6h                 | 5009 B0A6h                 |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>         | 5001 B0C0h                | 5005 B0C0h                 | 5009 B0C0h                 |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>       | 5001 B0C4h                | 5005 B0C4h                 | 5009 B0C4h                 |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>         | 5001 B0C6h                | 5005 B0C6h                 | 5009 B0C6h                 |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>      | 5001 B0C8h                | 5005 B0C8h                 | 5009 B0C8h                 |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>          | 5001 B0D4h                | 5005 B0D4h                 | 5009 B0D4h                 |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>          | 5001 B0D8h                | 5005 B0D8h                 | 5009 B0D8h                 |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>          | 5001 B0DEh                | 5005 B0DEh                 | 5009 B0DEh                 |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>          | 5001 B0E2h                | 5005 B0E2h                 | 5009 B0E2h                 |

**Table 3-807. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM2_G3 Physical Address | EPWM20_G3 Physical Address | EPWM21_G3 Physical Address |
|--------|--------|---------------------------------------|---------------------------|----------------------------|----------------------------|
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>          | 5001 B0E8h                | 5005 B0E8h                 | 5009 B0E8h                 |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>        | 5001 B0EEh                | 5005 B0EEh                 | 5009 B0EEh                 |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>            | 5001 B100h                | 5005 B100h                 | 5009 B100h                 |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>           | 5001 B102h                | 5005 B102h                 | 5009 B102h                 |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>          | 5001 B104h                | 5005 B104h                 | 5009 B104h                 |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>            | 5001 B108h                | 5005 B108h                 | 5009 B108h                 |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>           | 5001 B10Ah                | 5005 B10Ah                 | 5009 B10Ah                 |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>         | 5001 B10Ch                | 5005 B10Ch                 | 5009 B10Ch                 |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>         | 5001 B10Eh                | 5005 B10Eh                 | 5009 B10Eh                 |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>           | 5001 B11Ah                | 5005 B11Ah                 | 5009 B11Ah                 |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>            | 5001 B126h                | 5005 B126h                 | 5009 B126h                 |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>         | 5001 B128h                | 5005 B128h                 | 5009 B128h                 |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>         | 5001 B12Ah                | 5005 B12Ah                 | 5009 B12Ah                 |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>            | 5001 B12Eh                | 5005 B12Eh                 | 5009 B12Eh                 |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>         | 5001 B130h                | 5005 B130h                 | 5009 B130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>         | 5001 B132h                | 5005 B132h                 | 5009 B132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>            | 5001 B136h                | 5005 B136h                 | 5009 B136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a>     | 5001 B13Ah                | 5005 B13Ah                 | 5009 B13Ah                 |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>            | 5001 B148h                | 5005 B148h                 | 5009 B148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>             | 5001 B14Ch                | 5005 B14Ch                 | 5009 B14Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>            | 5001 B150h                | 5005 B150h                 | 5009 B150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>            | 5001 B154h                | 5005 B154h                 | 5009 B154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 5001 B158h                | 5005 B158h                 | 5009 B158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 5001 B15Ch                | 5005 B15Ch                 | 5009 B15Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 5001 B160h                | 5005 B160h                 | 5009 B160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 5001 B164h                | 5005 B164h                 | 5009 B164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 5001 B168h                | 5005 B168h                 | 5009 B168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 5001 B16Ch                | 5005 B16Ch                 | 5009 B16Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 5001 B170h                | 5005 B170h                 | 5009 B170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 5001 B174h                | 5005 B174h                 | 5009 B174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRISEL</a>         | 5001 B180h                | 5005 B180h                 | 5009 B180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 5001 B186h                | 5005 B186h                 | 5009 B186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5001 B188h                | 5005 B188h                 | 5009 B188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5001 B18Eh                | 5005 B18Eh                 | 5009 B18Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5001 B190h                | 5005 B190h                 | 5009 B190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5001 B192h                | 5005 B192h                 | 5009 B192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5001 B194h                | 5005 B194h                 | 5009 B194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5001 B196h                | 5005 B196h                 | 5009 B196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5001 B198h                | 5005 B198h                 | 5009 B198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5001 B19Ah                | 5005 B19Ah                 | 5009 B19Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5001 B19Ch                | 5005 B19Ch                 | 5009 B19Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5001 B19Eh                | 5005 B19Eh                 | 5009 B19Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5001 B1A4h                | 5005 B1A4h                 | 5009 B1A4h                 |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5001 B1A6h                | 5005 B1A6h                 | 5009 B1A6h                 |



**Table 3-807. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM2_G3 Physical Address | EPWM20_G3 Physical Address | EPWM21_G3 Physical Address |
|--------|--------|-------------------------------------|---------------------------|----------------------------|----------------------------|
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>    | 5001 B1A8h                | 5005 B1A8h                 | 5009 B1A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>    | 5001 B1AAh                | 5005 B1AAh                 | 5009 B1AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>         | 5001 B1ACh                | 5005 B1ACh                 | 5009 B1ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a> | 5001 B1AEh                | 5005 B1AEh                 | 5009 B1AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>   | 5001 B1B0h                | 5005 B1B0h                 | 5009 B1B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>     | 5001 B1B2h                | 5005 B1B2h                 | 5009 B1B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>       | 5001 B1F4h                | 5005 B1F4h                 | 5009 B1F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>      | 5001 B1FAh                | 5005 B1FAh                 | 5009 B1FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>        | 5001 B1FCh                | 5005 B1FCh                 | 5009 B1FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>       | 5001 B400h                | 5005 B400h                 | 5009 B400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>       | 5001 B410h                | 5005 B410h                 | 5009 B410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>          | 5001 B418h                | 5005 B418h                 | 5009 B418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a> | 5001 B41Ch                | 5005 B41Ch                 | 5009 B41Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>   | 5001 B420h                | 5005 B420h                 | 5009 B420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>   | 5001 B428h                | 5005 B428h                 | 5009 B428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>   | 5001 B430h                | 5005 B430h                 | 5009 B430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>   | 5001 B600h                | 5005 B600h                 | 5009 B600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>   | 5001 B604h                | 5005 B604h                 | 5009 B604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>   | 5001 B608h                | 5005 B608h                 | 5009 B608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>   | 5001 B60Ch                | 5005 B60Ch                 | 5009 B60Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>   | 5001 B610h                | 5005 B610h                 | 5009 B610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 5001 B614h                | 5005 B614h                 | 5009 B614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 5001 B618h                | 5005 B618h                 | 5009 B618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 5001 B61Ch                | 5005 B61Ch                 | 5009 B61Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 5001 B620h                | 5005 B620h                 | 5009 B620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 5001 B630h                | 5005 B630h                 | 5009 B630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 5001 B632h                | 5005 B632h                 | 5009 B632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 5001 B644h                | 5005 B644h                 | 5009 B644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 5001 B680h                | 5005 B680h                 | 5009 B680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 5001 B684h                | 5005 B684h                 | 5009 B684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 5001 B688h                | 5005 B688h                 | 5009 B688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 5001 B68Ch                | 5005 B68Ch                 | 5009 B68Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 5001 B690h                | 5005 B690h                 | 5009 B690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 5001 B694h                | 5005 B694h                 | 5009 B694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 5001 B698h                | 5005 B698h                 | 5009 B698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 5001 B69Ch                | 5005 B69Ch                 | 5009 B69Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 5001 B6A0h                | 5005 B6A0h                 | 5009 B6A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 5001 B6B0h                | 5005 B6B0h                 | 5009 B6B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 5001 B6B2h                | 5005 B6B2h                 | 5009 B6B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 5001 B6BAh                | 5005 B6BAh                 | 5009 B6BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 5001 B6BEh                | 5005 B6BEh                 | 5009 B6BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 5001 B6C4h                | 5005 B6C4h                 | 5009 B6C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 5001 B700h                | 5005 B700h                 | 5009 B700h                 |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 5001 B704h                | 5005 B704h                 | 5009 B704h                 |

**Table 3-807. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM2_G3 Physical Address | EPWM20_G3 Physical Address | EPWM21_G3 Physical Address |
|--------|--------|------------------------------------|---------------------------|----------------------------|----------------------------|
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>   | 5001 B708h                | 5005 B708h                 | 5009 B708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>   | 5001 B70Ch                | 5005 B70Ch                 | 5009 B70Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>   | 5001 B710h                | 5005 B710h                 | 5009 B710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>   | 5001 B714h                | 5005 B714h                 | 5009 B714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>   | 5001 B718h                | 5005 B718h                 | 5009 B718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>   | 5001 B71Ch                | 5005 B71Ch                 | 5009 B71Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>  | 5001 B720h                | 5005 B720h                 | 5009 B720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a> | 5001 B730h                | 5005 B730h                 | 5009 B730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a> | 5001 B732h                | 5005 B732h                 | 5009 B732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>    | 5001 B73Ah                | 5005 B73Ah                 | 5009 B73Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>    | 5001 B73Eh                | 5005 B73Eh                 | 5009 B73Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a> | 5001 B744h                | 5005 B744h                 | 5009 B744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 5001 B780h                | 5005 B780h                 | 5009 B780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 5001 B784h                | 5005 B784h                 | 5009 B784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 5001 B788h                | 5005 B788h                 | 5009 B788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 5001 B78Ch                | 5005 B78Ch                 | 5009 B78Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 5001 B790h                | 5005 B790h                 | 5009 B790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 5001 B794h                | 5005 B794h                 | 5009 B794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 5001 B798h                | 5005 B798h                 | 5009 B798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 5001 B79Ch                | 5005 B79Ch                 | 5009 B79Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 5001 B7A0h                | 5005 B7A0h                 | 5009 B7A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5001 B7B0h                | 5005 B7B0h                 | 5009 B7B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5001 B7B2h                | 5005 B7B2h                 | 5009 B7B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5001 B7BAh                | 5005 B7BAh                 | 5009 B7BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5001 B7BEh                | 5005 B7BEh                 | 5009 B7BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5001 B7C4h                | 5005 B7C4h                 | 5009 B7C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5001 B800h                | 5005 B800h                 | 5009 B800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5001 B804h                | 5005 B804h                 | 5009 B804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5001 B808h                | 5005 B808h                 | 5009 B808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5001 B80Ch                | 5005 B80Ch                 | 5009 B80Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 5001 B810h                | 5005 B810h                 | 5009 B810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5001 B814h                | 5005 B814h                 | 5009 B814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 5001 B820h                | 5005 B820h                 | 5009 B820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 5001 B824h                | 5005 B824h                 | 5009 B824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 5001 B828h                | 5005 B828h                 | 5009 B828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 5001 B82Ch                | 5005 B82Ch                 | 5009 B82Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>     | 5001 BC00h                | 5005 BC00h                 | 5009 BC00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 5001 BC04h                | 5005 BC04h                 | 5009 BC04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 5001 BC20h                | 5005 BC20h                 | 5009 BC20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 5001 BC24h                | 5005 BC24h                 | 5009 BC24h                 |



**Table 3-808. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM22_G3 Physical Address | EPWM23_G3 Physical Address | EPWM24_G3 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 500D B000h                 | 5001 C000h                 | 5005 C000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 500D B002h                 | 5001 C002h                 | 5005 C002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 500D B006h                 | 5001 C006h                 | 5005 C006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 500D B008h                 | 5001 C008h                 | 5005 C008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 500D B00Ah                 | 5001 C00Ah                 | 5005 C00Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 500D B00Ch                 | 5001 C00Ch                 | 5005 C00Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 500D B00Eh                 | 5001 C00Eh                 | 5005 C00Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 500D B010h                 | 5001 C010h                 | 5005 C010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 500D B012h                 | 5001 C012h                 | 5005 C012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 500D B018h                 | 5001 C018h                 | 5005 C018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 500D B01Ah                 | 5001 C01Ah                 | 5005 C01Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 500D B020h                 | 5001 C020h                 | 5005 C020h                 |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 500D B022h                 | 5001 C022h                 | 5005 C022h                 |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 500D B028h                 | 5001 C028h                 | 5005 C028h                 |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 500D B030h                 | 5001 C030h                 | 5005 C030h                 |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 500D B032h                 | 5001 C032h                 | 5005 C032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 500D B040h                 | 5001 C040h                 | 5005 C040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 500D B04Eh                 | 5001 C04Eh                 | 5005 C04Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>        | 500D B05Ah                 | 5001 C05Ah                 | 5005 C05Ah                 |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>         | 500D B05Ch                 | 5001 C05Ch                 | 5005 C05Ch                 |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>        | 500D B068h                 | 5001 C068h                 | 5005 C068h                 |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>        | 500D B06Ah                 | 5001 C06Ah                 | 5005 C06Ah                 |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>     | 500D B070h                 | 5001 C070h                 | 5005 C070h                 |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>    | 500D B074h                 | 5001 C074h                 | 5005 C074h                 |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>         | 500D B07Ah                 | 5001 C07Ah                 | 5005 C07Ah                 |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>       | 500D B07Ch                 | 5001 C07Ch                 | 5005 C07Ch                 |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>      | 500D B07Eh                 | 5001 C07Eh                 | 5005 C07Eh                 |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>        | 500D B080h                 | 5001 C080h                 | 5005 C080h                 |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>       | 500D B082h                 | 5001 C082h                 | 5005 C082h                 |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>        | 500D B084h                 | 5001 C084h                 | 5005 C084h                 |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>       | 500D B086h                 | 5001 C086h                 | 5005 C086h                 |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>        | 500D B08Eh                 | 5001 C08Eh                 | 5005 C08Eh                 |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>       | 500D B092h                 | 5001 C092h                 | 5005 C092h                 |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>       | 500D B0A0h                 | 5001 C0A0h                 | 5005 C0A0h                 |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>         | 500D B0A2h                 | 5001 C0A2h                 | 5005 C0A2h                 |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>       | 500D B0A4h                 | 5001 C0A4h                 | 5005 C0A4h                 |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>         | 500D B0A6h                 | 5001 C0A6h                 | 5005 C0A6h                 |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>         | 500D B0C0h                 | 5001 C0C0h                 | 5005 C0C0h                 |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>       | 500D B0C4h                 | 5001 C0C4h                 | 5005 C0C4h                 |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>         | 500D B0C6h                 | 5001 C0C6h                 | 5005 C0C6h                 |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>      | 500D B0C8h                 | 5001 C0C8h                 | 5005 C0C8h                 |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>          | 500D B0D4h                 | 5001 C0D4h                 | 5005 C0D4h                 |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>          | 500D B0D8h                 | 5001 C0D8h                 | 5005 C0D8h                 |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>          | 500D B0DEh                 | 5001 C0DEh                 | 5005 C0DEh                 |

**Table 3-808. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM22_G3 Physical Address | EPWM23_G3 Physical Address | EPWM24_G3 Physical Address |
|--------|--------|---------------------------------------|----------------------------|----------------------------|----------------------------|
| E2h    | 16     | <a href="#">EPWM_CMPD</a>             | 500D B0E2h                 | 5001 C0E2h                 | 5005 C0E2h                 |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>          | 500D B0E8h                 | 5001 C0E8h                 | 5005 C0E8h                 |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>        | 500D B0EEh                 | 5001 C0EEh                 | 5005 C0EEh                 |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>            | 500D B100h                 | 5001 C100h                 | 5005 C100h                 |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>           | 500D B102h                 | 5001 C102h                 | 5005 C102h                 |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>          | 500D B104h                 | 5001 C104h                 | 5005 C104h                 |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>            | 500D B108h                 | 5001 C108h                 | 5005 C108h                 |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>           | 500D B10Ah                 | 5001 C10Ah                 | 5005 C10Ah                 |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>         | 500D B10Ch                 | 5001 C10Ch                 | 5005 C10Ch                 |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>         | 500D B10Eh                 | 5001 C10Eh                 | 5005 C10Eh                 |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>           | 500D B11Ah                 | 5001 C11Ah                 | 5005 C11Ah                 |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>            | 500D B126h                 | 5001 C126h                 | 5005 C126h                 |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>         | 500D B128h                 | 5001 C128h                 | 5005 C128h                 |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>         | 500D B12Ah                 | 5001 C12Ah                 | 5005 C12Ah                 |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>            | 500D B12Eh                 | 5001 C12Eh                 | 5005 C12Eh                 |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>         | 500D B130h                 | 5001 C130h                 | 5005 C130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>         | 500D B132h                 | 5001 C132h                 | 5005 C132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>            | 500D B136h                 | 5001 C136h                 | 5005 C136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a>     | 500D B13Ah                 | 5001 C13Ah                 | 5005 C13Ah                 |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>            | 500D B148h                 | 5001 C148h                 | 5005 C148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>             | 500D B14Ch                 | 5001 C14Ch                 | 5005 C14Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>            | 500D B150h                 | 5001 C150h                 | 5005 C150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>            | 500D B154h                 | 5001 C154h                 | 5005 C154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 500D B158h                 | 5001 C158h                 | 5005 C158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 500D B15Ch                 | 5001 C15Ch                 | 5005 C15Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 500D B160h                 | 5001 C160h                 | 5005 C160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 500D B164h                 | 5001 C164h                 | 5005 C164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 500D B168h                 | 5001 C168h                 | 5005 C168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 500D B16Ch                 | 5001 C16Ch                 | 5005 C16Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 500D B170h                 | 5001 C170h                 | 5005 C170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 500D B174h                 | 5001 C174h                 | 5005 C174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 500D B180h                 | 5001 C180h                 | 5005 C180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 500D B186h                 | 5001 C186h                 | 5005 C186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 500D B188h                 | 5001 C188h                 | 5005 C188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 500D B18Eh                 | 5001 C18Eh                 | 5005 C18Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 500D B190h                 | 5001 C190h                 | 5005 C190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 500D B192h                 | 5001 C192h                 | 5005 C192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 500D B194h                 | 5001 C194h                 | 5005 C194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 500D B196h                 | 5001 C196h                 | 5005 C196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 500D B198h                 | 5001 C198h                 | 5005 C198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 500D B19Ah                 | 5001 C19Ah                 | 5005 C19Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 500D B19Ch                 | 5001 C19Ch                 | 5005 C19Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 500D B19Eh                 | 5001 C19Eh                 | 5005 C19Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 500D B1A4h                 | 5001 C1A4h                 | 5005 C1A4h                 |

**Table 3-808. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM22_G3 Physical Address | EPWM23_G3 Physical Address | EPWM24_G3 Physical Address |
|--------|--------|-------------------------------------|----------------------------|----------------------------|----------------------------|
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>    | 500D B1A6h                 | 5001 C1A6h                 | 5005 C1A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>    | 500D B1A8h                 | 5001 C1A8h                 | 5005 C1A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>    | 500D B1AAh                 | 5001 C1AAh                 | 5005 C1AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>         | 500D B1ACh                 | 5001 C1ACh                 | 5005 C1ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a> | 500D B1AEh                 | 5001 C1AEh                 | 5005 C1AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>   | 500D B1B0h                 | 5001 C1B0h                 | 5005 C1B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>     | 500D B1B2h                 | 5001 C1B2h                 | 5005 C1B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>       | 500D B1F4h                 | 5001 C1F4h                 | 5005 C1F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>      | 500D B1FAh                 | 5001 C1FAh                 | 5005 C1FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>        | 500D B1FCh                 | 5001 C1FCh                 | 5005 C1FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>       | 500D B400h                 | 5001 C400h                 | 5005 C400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>       | 500D B410h                 | 5001 C410h                 | 5005 C410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>          | 500D B418h                 | 5001 C418h                 | 5005 C418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a> | 500D B41Ch                 | 5001 C41Ch                 | 5005 C41Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>   | 500D B420h                 | 5001 C420h                 | 5005 C420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>   | 500D B428h                 | 5001 C428h                 | 5005 C428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>   | 500D B430h                 | 5001 C430h                 | 5005 C430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>   | 500D B600h                 | 5001 C600h                 | 5005 C600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>   | 500D B604h                 | 5001 C604h                 | 5005 C604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>   | 500D B608h                 | 5001 C608h                 | 5005 C608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>   | 500D B60Ch                 | 5001 C60Ch                 | 5005 C60Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>   | 500D B610h                 | 5001 C610h                 | 5005 C610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 500D B614h                 | 5001 C614h                 | 5005 C614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 500D B618h                 | 5001 C618h                 | 5005 C618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 500D B61Ch                 | 5001 C61Ch                 | 5005 C61Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 500D B620h                 | 5001 C620h                 | 5005 C620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 500D B630h                 | 5001 C630h                 | 5005 C630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 500D B632h                 | 5001 C632h                 | 5005 C632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 500D B644h                 | 5001 C644h                 | 5005 C644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 500D B680h                 | 5001 C680h                 | 5005 C680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 500D B684h                 | 5001 C684h                 | 5005 C684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 500D B688h                 | 5001 C688h                 | 5005 C688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 500D B68Ch                 | 5001 C68Ch                 | 5005 C68Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 500D B690h                 | 5001 C690h                 | 5005 C690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 500D B694h                 | 5001 C694h                 | 5005 C694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 500D B698h                 | 5001 C698h                 | 5005 C698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 500D B69Ch                 | 5001 C69Ch                 | 5005 C69Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 500D B6A0h                 | 5001 C6A0h                 | 5005 C6A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 500D B6B0h                 | 5001 C6B0h                 | 5005 C6B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 500D B6B2h                 | 5001 C6B2h                 | 5005 C6B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 500D B6BAh                 | 5001 C6BAh                 | 5005 C6BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 500D B6BEh                 | 5001 C6BEh                 | 5005 C6BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 500D B6C4h                 | 5001 C6C4h                 | 5005 C6C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 500D B700h                 | 5001 C700h                 | 5005 C700h                 |

**Table 3-808. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM22_G3 Physical Address | EPWM23_G3 Physical Address | EPWM24_G3 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>   | 500D B704h                 | 5001 C704h                 | 5005 C704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>   | 500D B708h                 | 5001 C708h                 | 5005 C708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>   | 500D B70Ch                 | 5001 C70Ch                 | 5005 C70Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>   | 500D B710h                 | 5001 C710h                 | 5005 C710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>   | 500D B714h                 | 5001 C714h                 | 5005 C714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>   | 500D B718h                 | 5001 C718h                 | 5005 C718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>   | 500D B71Ch                 | 5001 C71Ch                 | 5005 C71Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>  | 500D B720h                 | 5001 C720h                 | 5005 C720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a> | 500D B730h                 | 5001 C730h                 | 5005 C730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a> | 500D B732h                 | 5001 C732h                 | 5005 C732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>    | 500D B73Ah                 | 5001 C73Ah                 | 5005 C73Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>    | 500D B73Eh                 | 5001 C73Eh                 | 5005 C73Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a> | 500D B744h                 | 5001 C744h                 | 5005 C744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 500D B780h                 | 5001 C780h                 | 5005 C780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 500D B784h                 | 5001 C784h                 | 5005 C784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 500D B788h                 | 5001 C788h                 | 5005 C788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 500D B78Ch                 | 5001 C78Ch                 | 5005 C78Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 500D B790h                 | 5001 C790h                 | 5005 C790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 500D B794h                 | 5001 C794h                 | 5005 C794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 500D B798h                 | 5001 C798h                 | 5005 C798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 500D B79Ch                 | 5001 C79Ch                 | 5005 C79Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 500D B7A0h                 | 5001 C7A0h                 | 5005 C7A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 500D B7B0h                 | 5001 C7B0h                 | 5005 C7B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 500D B7B2h                 | 5001 C7B2h                 | 5005 C7B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 500D B7BAh                 | 5001 C7BAh                 | 5005 C7BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 500D B7BEh                 | 5001 C7BEh                 | 5005 C7BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 500D B7C4h                 | 5001 C7C4h                 | 5005 C7C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 500D B800h                 | 5001 C800h                 | 5005 C800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 500D B804h                 | 5001 C804h                 | 5005 C804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 500D B808h                 | 5001 C808h                 | 5005 C808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 500D B80Ch                 | 5001 C80Ch                 | 5005 C80Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 500D B810h                 | 5001 C810h                 | 5005 C810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 500D B814h                 | 5001 C814h                 | 5005 C814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 500D B820h                 | 5001 C820h                 | 5005 C820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 500D B824h                 | 5001 C824h                 | 5005 C824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 500D B828h                 | 5001 C828h                 | 5005 C828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 500D B82Ch                 | 5001 C82Ch                 | 5005 C82Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>     | 500D BC00h                 | 5001 CC00h                 | 5005 CC00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 500D BC04h                 | 5001 CC04h                 | 5005 CC04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 500D BC20h                 | 5001 CC20h                 | 5005 CC20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 500D BC24h                 | 5001 CC24h                 | 5005 CC24h                 |

**Table 3-809. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM25_G3 Physical Address | EPWM26_G3 Physical Address | EPWM27_G3 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5009 C000h                 | 500D C000h                 | 5001 D000h                 |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5009 C002h                 | 500D C002h                 | 5001 D002h                 |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5009 C006h                 | 500D C006h                 | 5001 D006h                 |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5009 C008h                 | 500D C008h                 | 5001 D008h                 |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5009 C00Ah                 | 500D C00Ah                 | 5001 D00Ah                 |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 5009 C00Ch                 | 500D C00Ch                 | 5001 D00Ch                 |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5009 C00Eh                 | 500D C00Eh                 | 5001 D00Eh                 |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5009 C010h                 | 500D C010h                 | 5001 D010h                 |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5009 C012h                 | 500D C012h                 | 5001 D012h                 |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 5009 C018h                 | 500D C018h                 | 5001 D018h                 |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 5009 C01Ah                 | 500D C01Ah                 | 5001 D01Ah                 |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 5009 C020h                 | 500D C020h                 | 5001 D020h                 |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 5009 C022h                 | 500D C022h                 | 5001 D022h                 |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 5009 C028h                 | 500D C028h                 | 5001 D028h                 |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 5009 C030h                 | 500D C030h                 | 5001 D030h                 |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 5009 C032h                 | 500D C032h                 | 5001 D032h                 |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 5009 C040h                 | 500D C040h                 | 5001 D040h                 |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 5009 C04Eh                 | 500D C04Eh                 | 5001 D04Eh                 |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>        | 5009 C05Ah                 | 500D C05Ah                 | 5001 D05Ah                 |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>         | 5009 C05Ch                 | 500D C05Ch                 | 5001 D05Ch                 |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>        | 5009 C068h                 | 500D C068h                 | 5001 D068h                 |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>        | 5009 C06Ah                 | 500D C06Ah                 | 5001 D06Ah                 |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>     | 5009 C070h                 | 500D C070h                 | 5001 D070h                 |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>    | 5009 C074h                 | 500D C074h                 | 5001 D074h                 |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>         | 5009 C07Ah                 | 500D C07Ah                 | 5001 D07Ah                 |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>       | 5009 C07Ch                 | 500D C07Ch                 | 5001 D07Ch                 |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>      | 5009 C07Eh                 | 500D C07Eh                 | 5001 D07Eh                 |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>        | 5009 C080h                 | 500D C080h                 | 5001 D080h                 |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>       | 5009 C082h                 | 500D C082h                 | 5001 D082h                 |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>        | 5009 C084h                 | 500D C084h                 | 5001 D084h                 |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>       | 5009 C086h                 | 500D C086h                 | 5001 D086h                 |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>        | 5009 C08Eh                 | 500D C08Eh                 | 5001 D08Eh                 |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>       | 5009 C092h                 | 500D C092h                 | 5001 D092h                 |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>       | 5009 C0A0h                 | 500D C0A0h                 | 5001 D0A0h                 |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>         | 5009 C0A2h                 | 500D C0A2h                 | 5001 D0A2h                 |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>       | 5009 C0A4h                 | 500D C0A4h                 | 5001 D0A4h                 |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>         | 5009 C0A6h                 | 500D C0A6h                 | 5001 D0A6h                 |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>         | 5009 C0C0h                 | 500D C0C0h                 | 5001 D0C0h                 |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>       | 5009 C0C4h                 | 500D C0C4h                 | 5001 D0C4h                 |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>         | 5009 C0C6h                 | 500D C0C6h                 | 5001 D0C6h                 |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>      | 5009 C0C8h                 | 500D C0C8h                 | 5001 D0C8h                 |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>          | 5009 C0D4h                 | 500D C0D4h                 | 5001 D0D4h                 |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>          | 5009 C0D8h                 | 500D C0D8h                 | 5001 D0D8h                 |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>          | 5009 C0DEh                 | 500D C0DEh                 | 5001 D0DEh                 |

**Table 3-809. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM25_G3 Physical Address | EPWM26_G3 Physical Address | EPWM27_G3 Physical Address |
|--------|--------|---------------------------------------|----------------------------|----------------------------|----------------------------|
| E2h    | 16     | <a href="#">EPWM_CMPD</a>             | 5009 C0E2h                 | 500D C0E2h                 | 5001 D0E2h                 |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>          | 5009 C0E8h                 | 500D C0E8h                 | 5001 D0E8h                 |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>        | 5009 C0EEh                 | 500D C0EEh                 | 5001 D0EEh                 |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>            | 5009 C100h                 | 500D C100h                 | 5001 D100h                 |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>           | 5009 C102h                 | 500D C102h                 | 5001 D102h                 |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>          | 5009 C104h                 | 500D C104h                 | 5001 D104h                 |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>            | 5009 C108h                 | 500D C108h                 | 5001 D108h                 |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>           | 5009 C10Ah                 | 500D C10Ah                 | 5001 D10Ah                 |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>         | 5009 C10Ch                 | 500D C10Ch                 | 5001 D10Ch                 |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>         | 5009 C10Eh                 | 500D C10Eh                 | 5001 D10Eh                 |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>           | 5009 C11Ah                 | 500D C11Ah                 | 5001 D11Ah                 |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>            | 5009 C126h                 | 500D C126h                 | 5001 D126h                 |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>         | 5009 C128h                 | 500D C128h                 | 5001 D128h                 |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>         | 5009 C12Ah                 | 500D C12Ah                 | 5001 D12Ah                 |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>            | 5009 C12Eh                 | 500D C12Eh                 | 5001 D12Eh                 |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>         | 5009 C130h                 | 500D C130h                 | 5001 D130h                 |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>         | 5009 C132h                 | 500D C132h                 | 5001 D132h                 |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>            | 5009 C136h                 | 500D C136h                 | 5001 D136h                 |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a>     | 5009 C13Ah                 | 500D C13Ah                 | 5001 D13Ah                 |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>            | 5009 C148h                 | 500D C148h                 | 5001 D148h                 |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>             | 5009 C14Ch                 | 500D C14Ch                 | 5001 D14Ch                 |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>            | 5009 C150h                 | 500D C150h                 | 5001 D150h                 |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>            | 5009 C154h                 | 500D C154h                 | 5001 D154h                 |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 5009 C158h                 | 500D C158h                 | 5001 D158h                 |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 5009 C15Ch                 | 500D C15Ch                 | 5001 D15Ch                 |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 5009 C160h                 | 500D C160h                 | 5001 D160h                 |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 5009 C164h                 | 500D C164h                 | 5001 D164h                 |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 5009 C168h                 | 500D C168h                 | 5001 D168h                 |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 5009 C16Ch                 | 500D C16Ch                 | 5001 D16Ch                 |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 5009 C170h                 | 500D C170h                 | 5001 D170h                 |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 5009 C174h                 | 500D C174h                 | 5001 D174h                 |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 5009 C180h                 | 500D C180h                 | 5001 D180h                 |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 5009 C186h                 | 500D C186h                 | 5001 D186h                 |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5009 C188h                 | 500D C188h                 | 5001 D188h                 |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5009 C18Eh                 | 500D C18Eh                 | 5001 D18Eh                 |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5009 C190h                 | 500D C190h                 | 5001 D190h                 |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5009 C192h                 | 500D C192h                 | 5001 D192h                 |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5009 C194h                 | 500D C194h                 | 5001 D194h                 |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5009 C196h                 | 500D C196h                 | 5001 D196h                 |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5009 C198h                 | 500D C198h                 | 5001 D198h                 |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5009 C19Ah                 | 500D C19Ah                 | 5001 D19Ah                 |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5009 C19Ch                 | 500D C19Ch                 | 5001 D19Ch                 |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5009 C19Eh                 | 500D C19Eh                 | 5001 D19Eh                 |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5009 C1A4h                 | 500D C1A4h                 | 5001 D1A4h                 |

**Table 3-809. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM25_G3 Physical Address | EPWM26_G3 Physical Address | EPWM27_G3 Physical Address |
|--------|--------|-------------------------------------|----------------------------|----------------------------|----------------------------|
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>    | 5009 C1A6h                 | 500D C1A6h                 | 5001 D1A6h                 |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>    | 5009 C1A8h                 | 500D C1A8h                 | 5001 D1A8h                 |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>    | 5009 C1AAh                 | 500D C1AAh                 | 5001 D1AAh                 |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>         | 5009 C1ACh                 | 500D C1ACh                 | 5001 D1ACh                 |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a> | 5009 C1AEh                 | 500D C1AEh                 | 5001 D1AEh                 |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>   | 5009 C1B0h                 | 500D C1B0h                 | 5001 D1B0h                 |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>     | 5009 C1B2h                 | 500D C1B2h                 | 5001 D1B2h                 |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>       | 5009 C1F4h                 | 500D C1F4h                 | 5001 D1F4h                 |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>      | 5009 C1FAh                 | 500D C1FAh                 | 5001 D1FAh                 |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>        | 5009 C1FCh                 | 500D C1FCh                 | 5001 D1FCh                 |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>       | 5009 C400h                 | 500D C400h                 | 5001 D400h                 |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>       | 5009 C410h                 | 500D C410h                 | 5001 D410h                 |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>          | 5009 C418h                 | 500D C418h                 | 5001 D418h                 |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a> | 5009 C41Ch                 | 500D C41Ch                 | 5001 D41Ch                 |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>   | 5009 C420h                 | 500D C420h                 | 5001 D420h                 |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>   | 5009 C428h                 | 500D C428h                 | 5001 D428h                 |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>   | 5009 C430h                 | 500D C430h                 | 5001 D430h                 |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>   | 5009 C600h                 | 500D C600h                 | 5001 D600h                 |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>   | 5009 C604h                 | 500D C604h                 | 5001 D604h                 |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>   | 5009 C608h                 | 500D C608h                 | 5001 D608h                 |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>   | 5009 C60Ch                 | 500D C60Ch                 | 5001 D60Ch                 |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>   | 5009 C610h                 | 500D C610h                 | 5001 D610h                 |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 5009 C614h                 | 500D C614h                 | 5001 D614h                 |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 5009 C618h                 | 500D C618h                 | 5001 D618h                 |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 5009 C61Ch                 | 500D C61Ch                 | 5001 D61Ch                 |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 5009 C620h                 | 500D C620h                 | 5001 D620h                 |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 5009 C630h                 | 500D C630h                 | 5001 D630h                 |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 5009 C632h                 | 500D C632h                 | 5001 D632h                 |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 5009 C644h                 | 500D C644h                 | 5001 D644h                 |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 5009 C680h                 | 500D C680h                 | 5001 D680h                 |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 5009 C684h                 | 500D C684h                 | 5001 D684h                 |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 5009 C688h                 | 500D C688h                 | 5001 D688h                 |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 5009 C68Ch                 | 500D C68Ch                 | 5001 D68Ch                 |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 5009 C690h                 | 500D C690h                 | 5001 D690h                 |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 5009 C694h                 | 500D C694h                 | 5001 D694h                 |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 5009 C698h                 | 500D C698h                 | 5001 D698h                 |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 5009 C69Ch                 | 500D C69Ch                 | 5001 D69Ch                 |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 5009 C6A0h                 | 500D C6A0h                 | 5001 D6A0h                 |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 5009 C6B0h                 | 500D C6B0h                 | 5001 D6B0h                 |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 5009 C6B2h                 | 500D C6B2h                 | 5001 D6B2h                 |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 5009 C6BAh                 | 500D C6BAh                 | 5001 D6BAh                 |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 5009 C6BEh                 | 500D C6BEh                 | 5001 D6BEh                 |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 5009 C6C4h                 | 500D C6C4h                 | 5001 D6C4h                 |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 5009 C700h                 | 500D C700h                 | 5001 D700h                 |



**Table 3-809. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM25_G3 Physical Address | EPWM26_G3 Physical Address | EPWM27_G3 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|----------------------------|
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>   | 5009 C704h                 | 500D C704h                 | 5001 D704h                 |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>   | 5009 C708h                 | 500D C708h                 | 5001 D708h                 |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>   | 5009 C70Ch                 | 500D C70Ch                 | 5001 D70Ch                 |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>   | 5009 C710h                 | 500D C710h                 | 5001 D710h                 |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>   | 5009 C714h                 | 500D C714h                 | 5001 D714h                 |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>   | 5009 C718h                 | 500D C718h                 | 5001 D718h                 |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>   | 5009 C71Ch                 | 500D C71Ch                 | 5001 D71Ch                 |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>  | 5009 C720h                 | 500D C720h                 | 5001 D720h                 |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a> | 5009 C730h                 | 500D C730h                 | 5001 D730h                 |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a> | 5009 C732h                 | 500D C732h                 | 5001 D732h                 |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>    | 5009 C73Ah                 | 500D C73Ah                 | 5001 D73Ah                 |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>    | 5009 C73Eh                 | 500D C73Eh                 | 5001 D73Eh                 |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a> | 5009 C744h                 | 500D C744h                 | 5001 D744h                 |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 5009 C780h                 | 500D C780h                 | 5001 D780h                 |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 5009 C784h                 | 500D C784h                 | 5001 D784h                 |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 5009 C788h                 | 500D C788h                 | 5001 D788h                 |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 5009 C78Ch                 | 500D C78Ch                 | 5001 D78Ch                 |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 5009 C790h                 | 500D C790h                 | 5001 D790h                 |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 5009 C794h                 | 500D C794h                 | 5001 D794h                 |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 5009 C798h                 | 500D C798h                 | 5001 D798h                 |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 5009 C79Ch                 | 500D C79Ch                 | 5001 D79Ch                 |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 5009 C7A0h                 | 500D C7A0h                 | 5001 D7A0h                 |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5009 C7B0h                 | 500D C7B0h                 | 5001 D7B0h                 |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5009 C7B2h                 | 500D C7B2h                 | 5001 D7B2h                 |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5009 C7BAh                 | 500D C7BAh                 | 5001 D7BAh                 |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5009 C7BEh                 | 500D C7BEh                 | 5001 D7BEh                 |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5009 C7C4h                 | 500D C7C4h                 | 5001 D7C4h                 |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5009 C800h                 | 500D C800h                 | 5001 D800h                 |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5009 C804h                 | 500D C804h                 | 5001 D804h                 |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5009 C808h                 | 500D C808h                 | 5001 D808h                 |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5009 C80Ch                 | 500D C80Ch                 | 5001 D80Ch                 |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 5009 C810h                 | 500D C810h                 | 5001 D810h                 |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5009 C814h                 | 500D C814h                 | 5001 D814h                 |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 5009 C820h                 | 500D C820h                 | 5001 D820h                 |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 5009 C824h                 | 500D C824h                 | 5001 D824h                 |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 5009 C828h                 | 500D C828h                 | 5001 D828h                 |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 5009 C82Ch                 | 500D C82Ch                 | 5001 D82Ch                 |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>     | 5009 CC00h                 | 500D CC00h                 | 5001 DC00h                 |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 5009 CC04h                 | 500D CC04h                 | 5001 DC04h                 |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 5009 CC20h                 | 500D CC20h                 | 5001 DC20h                 |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 5009 CC24h                 | 500D CC24h                 | 5001 DC24h                 |



**Table 3-810. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM28_G3 Physical Address | EPWM29_G3 Physical Address | EPWM3_G3 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|---------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5005 D000h                 | 5009 D000h                 | 500D D000h                |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5005 D002h                 | 5009 D002h                 | 500D D002h                |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5005 D006h                 | 5009 D006h                 | 500D D006h                |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5005 D008h                 | 5009 D008h                 | 500D D008h                |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5005 D00Ah                 | 5009 D00Ah                 | 500D D00Ah                |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUEN</a>  | 5005 D00Ch                 | 5009 D00Ch                 | 500D D00Ch                |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5005 D00Eh                 | 5009 D00Eh                 | 500D D00Eh                |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5005 D010h                 | 5009 D010h                 | 500D D010h                |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5005 D012h                 | 5009 D012h                 | 500D D012h                |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 5005 D018h                 | 5009 D018h                 | 500D D018h                |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 5005 D01Ah                 | 5009 D01Ah                 | 500D D01Ah                |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 5005 D020h                 | 5009 D020h                 | 500D D020h                |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 5005 D022h                 | 5009 D022h                 | 500D D022h                |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 5005 D028h                 | 5009 D028h                 | 500D D028h                |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 5005 D030h                 | 5009 D030h                 | 500D D030h                |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 5005 D032h                 | 5009 D032h                 | 500D D032h                |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 5005 D040h                 | 5009 D040h                 | 500D D040h                |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 5005 D04Eh                 | 5009 D04Eh                 | 500D D04Eh                |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>        | 5005 D05Ah                 | 5009 D05Ah                 | 500D D05Ah                |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>         | 5005 D05Ch                 | 5009 D05Ch                 | 500D D05Ch                |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>        | 5005 D068h                 | 5009 D068h                 | 500D D068h                |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>        | 5005 D06Ah                 | 5009 D06Ah                 | 500D D06Ah                |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>     | 5005 D070h                 | 5009 D070h                 | 500D D070h                |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>    | 5005 D074h                 | 5009 D074h                 | 500D D074h                |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>         | 5005 D07Ah                 | 5009 D07Ah                 | 500D D07Ah                |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>       | 5005 D07Ch                 | 5009 D07Ch                 | 500D D07Ch                |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>      | 5005 D07Eh                 | 5009 D07Eh                 | 500D D07Eh                |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>        | 5005 D080h                 | 5009 D080h                 | 500D D080h                |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>       | 5005 D082h                 | 5009 D082h                 | 500D D082h                |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>        | 5005 D084h                 | 5009 D084h                 | 500D D084h                |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>       | 5005 D086h                 | 5009 D086h                 | 500D D086h                |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>        | 5005 D08Eh                 | 5009 D08Eh                 | 500D D08Eh                |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>       | 5005 D092h                 | 5009 D092h                 | 500D D092h                |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>       | 5005 D0A0h                 | 5009 D0A0h                 | 500D D0A0h                |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>         | 5005 D0A2h                 | 5009 D0A2h                 | 500D D0A2h                |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>       | 5005 D0A4h                 | 5009 D0A4h                 | 500D D0A4h                |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>         | 5005 D0A6h                 | 5009 D0A6h                 | 500D D0A6h                |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>         | 5005 D0C0h                 | 5009 D0C0h                 | 500D D0C0h                |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>       | 5005 D0C4h                 | 5009 D0C4h                 | 500D D0C4h                |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>         | 5005 D0C6h                 | 5009 D0C6h                 | 500D D0C6h                |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>      | 5005 D0C8h                 | 5009 D0C8h                 | 500D D0C8h                |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>          | 5005 D0D4h                 | 5009 D0D4h                 | 500D D0D4h                |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>          | 5005 D0D8h                 | 5009 D0D8h                 | 500D D0D8h                |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>          | 5005 D0DEh                 | 5009 D0DEh                 | 500D D0DEh                |

**Table 3-810. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM28_G3 Physical Address | EPWM29_G3 Physical Address | EPWM3_G3 Physical Address |
|--------|--------|---------------------------------------|----------------------------|----------------------------|---------------------------|
| E2h    | 16     | <a href="#">EPWM_CMPD</a>             | 5005 D0E2h                 | 5009 D0E2h                 | 500D D0E2h                |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>          | 5005 D0E8h                 | 5009 D0E8h                 | 500D D0E8h                |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>        | 5005 D0EEh                 | 5009 D0EEh                 | 500D D0EEh                |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>            | 5005 D100h                 | 5009 D100h                 | 500D D100h                |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>           | 5005 D102h                 | 5009 D102h                 | 500D D102h                |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>          | 5005 D104h                 | 5009 D104h                 | 500D D104h                |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>            | 5005 D108h                 | 5009 D108h                 | 500D D108h                |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>           | 5005 D10Ah                 | 5009 D10Ah                 | 500D D10Ah                |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>         | 5005 D10Ch                 | 5009 D10Ch                 | 500D D10Ch                |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>         | 5005 D10Eh                 | 5009 D10Eh                 | 500D D10Eh                |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>           | 5005 D11Ah                 | 5009 D11Ah                 | 500D D11Ah                |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>            | 5005 D126h                 | 5009 D126h                 | 500D D126h                |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>         | 5005 D128h                 | 5009 D128h                 | 500D D128h                |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>         | 5005 D12Ah                 | 5009 D12Ah                 | 500D D12Ah                |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>            | 5005 D12Eh                 | 5009 D12Eh                 | 500D D12Eh                |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>         | 5005 D130h                 | 5009 D130h                 | 500D D130h                |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>         | 5005 D132h                 | 5009 D132h                 | 500D D132h                |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>            | 5005 D136h                 | 5009 D136h                 | 500D D136h                |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a>     | 5005 D13Ah                 | 5009 D13Ah                 | 500D D13Ah                |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>            | 5005 D148h                 | 5009 D148h                 | 500D D148h                |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>             | 5005 D14Ch                 | 5009 D14Ch                 | 500D D14Ch                |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>            | 5005 D150h                 | 5009 D150h                 | 500D D150h                |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>            | 5005 D154h                 | 5009 D154h                 | 500D D154h                |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 5005 D158h                 | 5009 D158h                 | 500D D158h                |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 5005 D15Ch                 | 5009 D15Ch                 | 500D D15Ch                |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 5005 D160h                 | 5009 D160h                 | 500D D160h                |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 5005 D164h                 | 5009 D164h                 | 500D D164h                |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 5005 D168h                 | 5009 D168h                 | 500D D168h                |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 5005 D16Ch                 | 5009 D16Ch                 | 500D D16Ch                |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 5005 D170h                 | 5009 D170h                 | 500D D170h                |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 5005 D174h                 | 5009 D174h                 | 500D D174h                |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 5005 D180h                 | 5009 D180h                 | 500D D180h                |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 5005 D186h                 | 5009 D186h                 | 500D D186h                |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5005 D188h                 | 5009 D188h                 | 500D D188h                |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5005 D18Eh                 | 5009 D18Eh                 | 500D D18Eh                |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5005 D190h                 | 5009 D190h                 | 500D D190h                |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5005 D192h                 | 5009 D192h                 | 500D D192h                |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5005 D194h                 | 5009 D194h                 | 500D D194h                |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5005 D196h                 | 5009 D196h                 | 500D D196h                |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5005 D198h                 | 5009 D198h                 | 500D D198h                |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5005 D19Ah                 | 5009 D19Ah                 | 500D D19Ah                |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5005 D19Ch                 | 5009 D19Ch                 | 500D D19Ch                |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5005 D19Eh                 | 5009 D19Eh                 | 500D D19Eh                |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5005 D1A4h                 | 5009 D1A4h                 | 500D D1A4h                |

**Table 3-810. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM28_G3 Physical Address | EPWM29_G3 Physical Address | EPWM3_G3 Physical Address |
|--------|--------|-------------------------------------|----------------------------|----------------------------|---------------------------|
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>    | 5005 D1A6h                 | 5009 D1A6h                 | 500D D1A6h                |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>    | 5005 D1A8h                 | 5009 D1A8h                 | 500D D1A8h                |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>    | 5005 D1AAh                 | 5009 D1AAh                 | 500D D1AAh                |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>         | 5005 D1ACh                 | 5009 D1ACh                 | 500D D1ACh                |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a> | 5005 D1AEh                 | 5009 D1AEh                 | 500D D1AEh                |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>   | 5005 D1B0h                 | 5009 D1B0h                 | 500D D1B0h                |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>     | 5005 D1B2h                 | 5009 D1B2h                 | 500D D1B2h                |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>       | 5005 D1F4h                 | 5009 D1F4h                 | 500D D1F4h                |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>      | 5005 D1FAh                 | 5009 D1FAh                 | 500D D1FAh                |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>        | 5005 D1FCh                 | 5009 D1FCh                 | 500D D1FCh                |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>       | 5005 D400h                 | 5009 D400h                 | 500D D400h                |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>       | 5005 D410h                 | 5009 D410h                 | 500D D410h                |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>          | 5005 D418h                 | 5009 D418h                 | 500D D418h                |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a> | 5005 D41Ch                 | 5009 D41Ch                 | 500D D41Ch                |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>   | 5005 D420h                 | 5009 D420h                 | 500D D420h                |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>   | 5005 D428h                 | 5009 D428h                 | 500D D428h                |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>   | 5005 D430h                 | 5009 D430h                 | 500D D430h                |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>   | 5005 D600h                 | 5009 D600h                 | 500D D600h                |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>   | 5005 D604h                 | 5009 D604h                 | 500D D604h                |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>   | 5005 D608h                 | 5009 D608h                 | 500D D608h                |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>   | 5005 D60Ch                 | 5009 D60Ch                 | 500D D60Ch                |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>   | 5005 D610h                 | 5009 D610h                 | 500D D610h                |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 5005 D614h                 | 5009 D614h                 | 500D D614h                |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 5005 D618h                 | 5009 D618h                 | 500D D618h                |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 5005 D61Ch                 | 5009 D61Ch                 | 500D D61Ch                |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 5005 D620h                 | 5009 D620h                 | 500D D620h                |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 5005 D630h                 | 5009 D630h                 | 500D D630h                |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 5005 D632h                 | 5009 D632h                 | 500D D632h                |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 5005 D644h                 | 5009 D644h                 | 500D D644h                |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 5005 D680h                 | 5009 D680h                 | 500D D680h                |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 5005 D684h                 | 5009 D684h                 | 500D D684h                |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 5005 D688h                 | 5009 D688h                 | 500D D688h                |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 5005 D68Ch                 | 5009 D68Ch                 | 500D D68Ch                |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 5005 D690h                 | 5009 D690h                 | 500D D690h                |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 5005 D694h                 | 5009 D694h                 | 500D D694h                |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 5005 D698h                 | 5009 D698h                 | 500D D698h                |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 5005 D69Ch                 | 5009 D69Ch                 | 500D D69Ch                |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 5005 D6A0h                 | 5009 D6A0h                 | 500D D6A0h                |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 5005 D6B0h                 | 5009 D6B0h                 | 500D D6B0h                |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 5005 D6B2h                 | 5009 D6B2h                 | 500D D6B2h                |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 5005 D6BAh                 | 5009 D6BAh                 | 500D D6BAh                |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 5005 D6BEh                 | 5009 D6BEh                 | 500D D6BEh                |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 5005 D6C4h                 | 5009 D6C4h                 | 500D D6C4h                |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 5005 D700h                 | 5009 D700h                 | 500D D700h                |

**Table 3-810. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM28_G3 Physical Address | EPWM29_G3 Physical Address | EPWM3_G3 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|---------------------------|
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>   | 5005 D704h                 | 5009 D704h                 | 500D D704h                |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>   | 5005 D708h                 | 5009 D708h                 | 500D D708h                |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>   | 5005 D70Ch                 | 5009 D70Ch                 | 500D D70Ch                |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>   | 5005 D710h                 | 5009 D710h                 | 500D D710h                |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>   | 5005 D714h                 | 5009 D714h                 | 500D D714h                |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>   | 5005 D718h                 | 5009 D718h                 | 500D D718h                |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>   | 5005 D71Ch                 | 5009 D71Ch                 | 500D D71Ch                |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>  | 5005 D720h                 | 5009 D720h                 | 500D D720h                |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a> | 5005 D730h                 | 5009 D730h                 | 500D D730h                |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a> | 5005 D732h                 | 5009 D732h                 | 500D D732h                |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>    | 5005 D73Ah                 | 5009 D73Ah                 | 500D D73Ah                |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>    | 5005 D73Eh                 | 5009 D73Eh                 | 500D D73Eh                |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a> | 5005 D744h                 | 5009 D744h                 | 500D D744h                |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 5005 D780h                 | 5009 D780h                 | 500D D780h                |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 5005 D784h                 | 5009 D784h                 | 500D D784h                |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 5005 D788h                 | 5009 D788h                 | 500D D788h                |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 5005 D78Ch                 | 5009 D78Ch                 | 500D D78Ch                |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 5005 D790h                 | 5009 D790h                 | 500D D790h                |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 5005 D794h                 | 5009 D794h                 | 500D D794h                |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 5005 D798h                 | 5009 D798h                 | 500D D798h                |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 5005 D79Ch                 | 5009 D79Ch                 | 500D D79Ch                |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 5005 D7A0h                 | 5009 D7A0h                 | 500D D7A0h                |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5005 D7B0h                 | 5009 D7B0h                 | 500D D7B0h                |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5005 D7B2h                 | 5009 D7B2h                 | 500D D7B2h                |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5005 D7BAh                 | 5009 D7BAh                 | 500D D7BAh                |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5005 D7BEh                 | 5009 D7BEh                 | 500D D7BEh                |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5005 D7C4h                 | 5009 D7C4h                 | 500D D7C4h                |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5005 D800h                 | 5009 D800h                 | 500D D800h                |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5005 D804h                 | 5009 D804h                 | 500D D804h                |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5005 D808h                 | 5009 D808h                 | 500D D808h                |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5005 D80Ch                 | 5009 D80Ch                 | 500D D80Ch                |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 5005 D810h                 | 5009 D810h                 | 500D D810h                |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5005 D814h                 | 5009 D814h                 | 500D D814h                |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 5005 D820h                 | 5009 D820h                 | 500D D820h                |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 5005 D824h                 | 5009 D824h                 | 500D D824h                |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 5005 D828h                 | 5009 D828h                 | 500D D828h                |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 5005 D82Ch                 | 5009 D82Ch                 | 500D D82Ch                |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>     | 5005 DC00h                 | 5009 DC00h                 | 500D DC00h                |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 5005 DC04h                 | 5009 DC04h                 | 500D DC04h                |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 5005 DC20h                 | 5009 DC20h                 | 500D DC20h                |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 5005 DC24h                 | 5009 DC24h                 | 500D DC24h                |

**Table 3-811. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM30_G3 Physical Address | EPWM31_G3 Physical Address | EPWM4_G3 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|---------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5001 E000h                 | 5005 E000h                 | 5009 E000h                |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5001 E002h                 | 5005 E002h                 | 5009 E002h                |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5001 E006h                 | 5005 E006h                 | 5009 E006h                |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5001 E008h                 | 5005 E008h                 | 5009 E008h                |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5001 E00Ah                 | 5005 E00Ah                 | 5009 E00Ah                |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 5001 E00Ch                 | 5005 E00Ch                 | 5009 E00Ch                |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5001 E00Eh                 | 5005 E00Eh                 | 5009 E00Eh                |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5001 E010h                 | 5005 E010h                 | 5009 E010h                |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5001 E012h                 | 5005 E012h                 | 5009 E012h                |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 5001 E018h                 | 5005 E018h                 | 5009 E018h                |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 5001 E01Ah                 | 5005 E01Ah                 | 5009 E01Ah                |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 5001 E020h                 | 5005 E020h                 | 5009 E020h                |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 5001 E022h                 | 5005 E022h                 | 5009 E022h                |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 5001 E028h                 | 5005 E028h                 | 5009 E028h                |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 5001 E030h                 | 5005 E030h                 | 5009 E030h                |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 5001 E032h                 | 5005 E032h                 | 5009 E032h                |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 5001 E040h                 | 5005 E040h                 | 5009 E040h                |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 5001 E04Eh                 | 5005 E04Eh                 | 5009 E04Eh                |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>        | 5001 E05Ah                 | 5005 E05Ah                 | 5009 E05Ah                |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>         | 5001 E05Ch                 | 5005 E05Ch                 | 5009 E05Ch                |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>        | 5001 E068h                 | 5005 E068h                 | 5009 E068h                |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>        | 5001 E06Ah                 | 5005 E06Ah                 | 5009 E06Ah                |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>     | 5001 E070h                 | 5005 E070h                 | 5009 E070h                |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>    | 5001 E074h                 | 5005 E074h                 | 5009 E074h                |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>         | 5001 E07Ah                 | 5005 E07Ah                 | 5009 E07Ah                |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>       | 5001 E07Ch                 | 5005 E07Ch                 | 5009 E07Ch                |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>      | 5001 E07Eh                 | 5005 E07Eh                 | 5009 E07Eh                |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>        | 5001 E080h                 | 5005 E080h                 | 5009 E080h                |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>       | 5001 E082h                 | 5005 E082h                 | 5009 E082h                |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>        | 5001 E084h                 | 5005 E084h                 | 5009 E084h                |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>       | 5001 E086h                 | 5005 E086h                 | 5009 E086h                |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>        | 5001 E08Eh                 | 5005 E08Eh                 | 5009 E08Eh                |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>       | 5001 E092h                 | 5005 E092h                 | 5009 E092h                |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>       | 5001 E0A0h                 | 5005 E0A0h                 | 5009 E0A0h                |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>         | 5001 E0A2h                 | 5005 E0A2h                 | 5009 E0A2h                |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>       | 5001 E0A4h                 | 5005 E0A4h                 | 5009 E0A4h                |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>         | 5001 E0A6h                 | 5005 E0A6h                 | 5009 E0A6h                |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>         | 5001 E0C0h                 | 5005 E0C0h                 | 5009 E0C0h                |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>       | 5001 E0C4h                 | 5005 E0C4h                 | 5009 E0C4h                |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>         | 5001 E0C6h                 | 5005 E0C6h                 | 5009 E0C6h                |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>      | 5001 E0C8h                 | 5005 E0C8h                 | 5009 E0C8h                |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>          | 5001 E0D4h                 | 5005 E0D4h                 | 5009 E0D4h                |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>          | 5001 E0D8h                 | 5005 E0D8h                 | 5009 E0D8h                |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>          | 5001 E0DEh                 | 5005 E0DEh                 | 5009 E0DEh                |

**Table 3-811. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM30_G3 Physical Address | EPWM31_G3 Physical Address | EPWM4_G3 Physical Address |
|--------|--------|---------------------------------------|----------------------------|----------------------------|---------------------------|
| E2h    | 16     | <a href="#">EPWM_CMPD</a>             | 5001 E0E2h                 | 5005 E0E2h                 | 5009 E0E2h                |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>          | 5001 E0E8h                 | 5005 E0E8h                 | 5009 E0E8h                |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>        | 5001 E0EEh                 | 5005 E0EEh                 | 5009 E0EEh                |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>            | 5001 E100h                 | 5005 E100h                 | 5009 E100h                |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>           | 5001 E102h                 | 5005 E102h                 | 5009 E102h                |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>          | 5001 E104h                 | 5005 E104h                 | 5009 E104h                |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>            | 5001 E108h                 | 5005 E108h                 | 5009 E108h                |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>           | 5001 E10Ah                 | 5005 E10Ah                 | 5009 E10Ah                |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>         | 5001 E10Ch                 | 5005 E10Ch                 | 5009 E10Ch                |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>         | 5001 E10Eh                 | 5005 E10Eh                 | 5009 E10Eh                |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>           | 5001 E11Ah                 | 5005 E11Ah                 | 5009 E11Ah                |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>            | 5001 E126h                 | 5005 E126h                 | 5009 E126h                |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>         | 5001 E128h                 | 5005 E128h                 | 5009 E128h                |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>         | 5001 E12Ah                 | 5005 E12Ah                 | 5009 E12Ah                |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>            | 5001 E12Eh                 | 5005 E12Eh                 | 5009 E12Eh                |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>         | 5001 E130h                 | 5005 E130h                 | 5009 E130h                |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>         | 5001 E132h                 | 5005 E132h                 | 5009 E132h                |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>            | 5001 E136h                 | 5005 E136h                 | 5009 E136h                |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a>     | 5001 E13Ah                 | 5005 E13Ah                 | 5009 E13Ah                |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>            | 5001 E148h                 | 5005 E148h                 | 5009 E148h                |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>             | 5001 E14Ch                 | 5005 E14Ch                 | 5009 E14Ch                |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>            | 5001 E150h                 | 5005 E150h                 | 5009 E150h                |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>            | 5001 E154h                 | 5005 E154h                 | 5009 E154h                |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 5001 E158h                 | 5005 E158h                 | 5009 E158h                |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 5001 E15Ch                 | 5005 E15Ch                 | 5009 E15Ch                |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 5001 E160h                 | 5005 E160h                 | 5009 E160h                |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 5001 E164h                 | 5005 E164h                 | 5009 E164h                |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 5001 E168h                 | 5005 E168h                 | 5009 E168h                |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 5001 E16Ch                 | 5005 E16Ch                 | 5009 E16Ch                |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 5001 E170h                 | 5005 E170h                 | 5009 E170h                |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 5001 E174h                 | 5005 E174h                 | 5009 E174h                |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 5001 E180h                 | 5005 E180h                 | 5009 E180h                |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 5001 E186h                 | 5005 E186h                 | 5009 E186h                |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5001 E188h                 | 5005 E188h                 | 5009 E188h                |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5001 E18Eh                 | 5005 E18Eh                 | 5009 E18Eh                |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5001 E190h                 | 5005 E190h                 | 5009 E190h                |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5001 E192h                 | 5005 E192h                 | 5009 E192h                |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5001 E194h                 | 5005 E194h                 | 5009 E194h                |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5001 E196h                 | 5005 E196h                 | 5009 E196h                |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5001 E198h                 | 5005 E198h                 | 5009 E198h                |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5001 E19Ah                 | 5005 E19Ah                 | 5009 E19Ah                |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5001 E19Ch                 | 5005 E19Ch                 | 5009 E19Ch                |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5001 E19Eh                 | 5005 E19Eh                 | 5009 E19Eh                |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5001 E1A4h                 | 5005 E1A4h                 | 5009 E1A4h                |

**Table 3-811. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM30_G3 Physical Address | EPWM31_G3 Physical Address | EPWM4_G3 Physical Address |
|--------|--------|-------------------------------------|----------------------------|----------------------------|---------------------------|
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>    | 5001 E1A6h                 | 5005 E1A6h                 | 5009 E1A6h                |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>    | 5001 E1A8h                 | 5005 E1A8h                 | 5009 E1A8h                |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>    | 5001 E1AAh                 | 5005 E1AAh                 | 5009 E1AAh                |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>         | 5001 E1ACh                 | 5005 E1ACh                 | 5009 E1ACh                |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a> | 5001 E1AEh                 | 5005 E1AEh                 | 5009 E1AEh                |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>   | 5001 E1B0h                 | 5005 E1B0h                 | 5009 E1B0h                |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>     | 5001 E1B2h                 | 5005 E1B2h                 | 5009 E1B2h                |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>       | 5001 E1F4h                 | 5005 E1F4h                 | 5009 E1F4h                |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>      | 5001 E1FAh                 | 5005 E1FAh                 | 5009 E1FAh                |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>        | 5001 E1FCh                 | 5005 E1FCh                 | 5009 E1FCh                |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>       | 5001 E400h                 | 5005 E400h                 | 5009 E400h                |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>       | 5001 E410h                 | 5005 E410h                 | 5009 E410h                |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>          | 5001 E418h                 | 5005 E418h                 | 5009 E418h                |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a> | 5001 E41Ch                 | 5005 E41Ch                 | 5009 E41Ch                |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>   | 5001 E420h                 | 5005 E420h                 | 5009 E420h                |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>   | 5001 E428h                 | 5005 E428h                 | 5009 E428h                |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>   | 5001 E430h                 | 5005 E430h                 | 5009 E430h                |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>   | 5001 E600h                 | 5005 E600h                 | 5009 E600h                |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>   | 5001 E604h                 | 5005 E604h                 | 5009 E604h                |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>   | 5001 E608h                 | 5005 E608h                 | 5009 E608h                |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>   | 5001 E60Ch                 | 5005 E60Ch                 | 5009 E60Ch                |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>   | 5001 E610h                 | 5005 E610h                 | 5009 E610h                |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 5001 E614h                 | 5005 E614h                 | 5009 E614h                |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 5001 E618h                 | 5005 E618h                 | 5009 E618h                |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 5001 E61Ch                 | 5005 E61Ch                 | 5009 E61Ch                |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 5001 E620h                 | 5005 E620h                 | 5009 E620h                |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 5001 E630h                 | 5005 E630h                 | 5009 E630h                |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 5001 E632h                 | 5005 E632h                 | 5009 E632h                |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 5001 E644h                 | 5005 E644h                 | 5009 E644h                |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 5001 E680h                 | 5005 E680h                 | 5009 E680h                |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 5001 E684h                 | 5005 E684h                 | 5009 E684h                |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 5001 E688h                 | 5005 E688h                 | 5009 E688h                |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 5001 E68Ch                 | 5005 E68Ch                 | 5009 E68Ch                |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 5001 E690h                 | 5005 E690h                 | 5009 E690h                |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 5001 E694h                 | 5005 E694h                 | 5009 E694h                |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 5001 E698h                 | 5005 E698h                 | 5009 E698h                |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 5001 E69Ch                 | 5005 E69Ch                 | 5009 E69Ch                |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 5001 E6A0h                 | 5005 E6A0h                 | 5009 E6A0h                |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 5001 E6B0h                 | 5005 E6B0h                 | 5009 E6B0h                |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 5001 E6B2h                 | 5005 E6B2h                 | 5009 E6B2h                |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 5001 E6BAh                 | 5005 E6BAh                 | 5009 E6BAh                |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 5001 E6BEh                 | 5005 E6BEh                 | 5009 E6BEh                |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 5001 E6C4h                 | 5005 E6C4h                 | 5009 E6C4h                |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 5001 E700h                 | 5005 E700h                 | 5009 E700h                |



**Table 3-811. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM30_G3 Physical Address | EPWM31_G3 Physical Address | EPWM4_G3 Physical Address |
|--------|--------|------------------------------------|----------------------------|----------------------------|---------------------------|
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>   | 5001 E704h                 | 5005 E704h                 | 5009 E704h                |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>   | 5001 E708h                 | 5005 E708h                 | 5009 E708h                |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>   | 5001 E70Ch                 | 5005 E70Ch                 | 5009 E70Ch                |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>   | 5001 E710h                 | 5005 E710h                 | 5009 E710h                |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>   | 5001 E714h                 | 5005 E714h                 | 5009 E714h                |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>   | 5001 E718h                 | 5005 E718h                 | 5009 E718h                |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>   | 5001 E71Ch                 | 5005 E71Ch                 | 5009 E71Ch                |
| 720h   | 32     | <a href="#">EPWM_XTBP RD_SHDW2</a> | 5001 E720h                 | 5005 E720h                 | 5009 E720h                |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a> | 5001 E730h                 | 5005 E730h                 | 5009 E730h                |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a> | 5001 E732h                 | 5005 E732h                 | 5009 E732h                |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>    | 5001 E73Ah                 | 5005 E73Ah                 | 5009 E73Ah                |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>    | 5001 E73Eh                 | 5005 E73Eh                 | 5009 E73Eh                |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a> | 5001 E744h                 | 5005 E744h                 | 5009 E744h                |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 5001 E780h                 | 5005 E780h                 | 5009 E780h                |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 5001 E784h                 | 5005 E784h                 | 5009 E784h                |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 5001 E788h                 | 5005 E788h                 | 5009 E788h                |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 5001 E78Ch                 | 5005 E78Ch                 | 5009 E78Ch                |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 5001 E790h                 | 5005 E790h                 | 5009 E790h                |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 5001 E794h                 | 5005 E794h                 | 5009 E794h                |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 5001 E798h                 | 5005 E798h                 | 5009 E798h                |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 5001 E79Ch                 | 5005 E79Ch                 | 5009 E79Ch                |
| 7A0h   | 32     | <a href="#">EPWM_XTBP RD_SHDW3</a> | 5001 E7A0h                 | 5005 E7A0h                 | 5009 E7A0h                |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5001 E7B0h                 | 5005 E7B0h                 | 5009 E7B0h                |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5001 E7B2h                 | 5005 E7B2h                 | 5009 E7B2h                |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5001 E7BAh                 | 5005 E7BAh                 | 5009 E7BAh                |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5001 E7BEh                 | 5005 E7BEh                 | 5009 E7BEh                |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5001 E7C4h                 | 5005 E7C4h                 | 5009 E7C4h                |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5001 E800h                 | 5005 E800h                 | 5009 E800h                |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5001 E804h                 | 5005 E804h                 | 5009 E804h                |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5001 E808h                 | 5005 E808h                 | 5009 E808h                |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5001 E80Ch                 | 5005 E80Ch                 | 5009 E80Ch                |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 5001 E810h                 | 5005 E810h                 | 5009 E810h                |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5001 E814h                 | 5005 E814h                 | 5009 E814h                |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 5001 E820h                 | 5005 E820h                 | 5009 E820h                |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 5001 E824h                 | 5005 E824h                 | 5009 E824h                |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 5001 E828h                 | 5005 E828h                 | 5009 E828h                |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 5001 E82Ch                 | 5005 E82Ch                 | 5009 E82Ch                |
| C00h   | 32     | <a href="#">EPWM_MINDBC FG</a>     | 5001 EC00h                 | 5005 EC00h                 | 5009 EC00h                |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 5001 EC04h                 | 5005 EC04h                 | 5009 EC04h                |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 5001 EC20h                 | 5005 EC20h                 | 5009 EC20h                |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 5001 EC24h                 | 5005 EC24h                 | 5009 EC24h                |



**Table 3-812. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM5_G3 Physical Address | EPWM6_G3 Physical Address | EPWM7_G3 Physical Address |
|--------|--------|------------------------------------|---------------------------|---------------------------|---------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 500D E000h                | 5001 F000h                | 5005 F000h                |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 500D E002h                | 5001 F002h                | 5005 F002h                |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 500D E006h                | 5001 F006h                | 5005 F006h                |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 500D E008h                | 5001 F008h                | 5005 F008h                |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 500D E00Ah                | 5001 F00Ah                | 5005 F00Ah                |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUTEN</a> | 500D E00Ch                | 5001 F00Ch                | 5005 F00Ch                |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 500D E00Eh                | 5001 F00Eh                | 5005 F00Eh                |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 500D E010h                | 5001 F010h                | 5005 F010h                |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 500D E012h                | 5001 F012h                | 5005 F012h                |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 500D E018h                | 5001 F018h                | 5005 F018h                |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 500D E01Ah                | 5001 F01Ah                | 5005 F01Ah                |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 500D E020h                | 5001 F020h                | 5005 F020h                |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 500D E022h                | 5001 F022h                | 5005 F022h                |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 500D E028h                | 5001 F028h                | 5005 F028h                |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 500D E030h                | 5001 F030h                | 5005 F030h                |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 500D E032h                | 5001 F032h                | 5005 F032h                |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 500D E040h                | 5001 F040h                | 5005 F040h                |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 500D E04Eh                | 5001 F04Eh                | 5005 F04Eh                |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>        | 500D E05Ah                | 5001 F05Ah                | 5005 F05Ah                |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>         | 500D E05Ch                | 5001 F05Ch                | 5005 F05Ch                |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>        | 500D E068h                | 5001 F068h                | 5005 F068h                |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>        | 500D E06Ah                | 5001 F06Ah                | 5005 F06Ah                |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>     | 500D E070h                | 5001 F070h                | 5005 F070h                |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>    | 500D E074h                | 5001 F074h                | 5005 F074h                |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>         | 500D E07Ah                | 5001 F07Ah                | 5005 F07Ah                |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>       | 500D E07Ch                | 5001 F07Ch                | 5005 F07Ch                |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>      | 500D E07Eh                | 5001 F07Eh                | 5005 F07Eh                |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>        | 500D E080h                | 5001 F080h                | 5005 F080h                |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>       | 500D E082h                | 5001 F082h                | 5005 F082h                |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>        | 500D E084h                | 5001 F084h                | 5005 F084h                |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>       | 500D E086h                | 5001 F086h                | 5005 F086h                |
| 8Eh    | 16     | <a href="#">EPWM_AQSFRC</a>        | 500D E08Eh                | 5001 F08Eh                | 5005 F08Eh                |
| 92h    | 16     | <a href="#">EPWM_AQCSFRC</a>       | 500D E092h                | 5001 F092h                | 5005 F092h                |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>       | 500D E0A0h                | 5001 F0A0h                | 5005 F0A0h                |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>         | 500D E0A2h                | 5001 F0A2h                | 5005 F0A2h                |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>       | 500D E0A4h                | 5001 F0A4h                | 5005 F0A4h                |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>         | 500D E0A6h                | 5001 F0A6h                | 5005 F0A6h                |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>         | 500D E0C0h                | 5001 F0C0h                | 5005 F0C0h                |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>       | 500D E0C4h                | 5001 F0C4h                | 5005 F0C4h                |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>         | 500D E0C6h                | 5001 F0C6h                | 5005 F0C6h                |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>      | 500D E0C8h                | 5001 F0C8h                | 5005 F0C8h                |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>          | 500D E0D4h                | 5001 F0D4h                | 5005 F0D4h                |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>          | 500D E0D8h                | 5001 F0D8h                | 5005 F0D8h                |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>          | 500D E0DEh                | 5001 F0DEh                | 5005 F0DEh                |

**Table 3-812. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM5_G3 Physical Address | EPWM6_G3 Physical Address | EPWM7_G3 Physical Address |
|--------|--------|---------------------------------------|---------------------------|---------------------------|---------------------------|
| E2h    | 16     | <a href="#">EPWM_CMPD</a>             | 500D E0E2h                | 5001 F0E2h                | 5005 F0E2h                |
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>          | 500D E0E8h                | 5001 F0E8h                | 5005 F0E8h                |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>        | 500D E0EEh                | 5001 F0EEh                | 5005 F0EEh                |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>            | 500D E100h                | 5001 F100h                | 5005 F100h                |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>           | 500D E102h                | 5001 F102h                | 5005 F102h                |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>          | 500D E104h                | 5001 F104h                | 5005 F104h                |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>            | 500D E108h                | 5001 F108h                | 5005 F108h                |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>           | 500D E10Ah                | 5001 F10Ah                | 5005 F10Ah                |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>         | 500D E10Ch                | 5001 F10Ch                | 5005 F10Ch                |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>         | 500D E10Eh                | 5001 F10Eh                | 5005 F10Eh                |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>           | 500D E11Ah                | 5001 F11Ah                | 5005 F11Ah                |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>            | 500D E126h                | 5001 F126h                | 5005 F126h                |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>         | 500D E128h                | 5001 F128h                | 5005 F128h                |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>         | 500D E12Ah                | 5001 F12Ah                | 5005 F12Ah                |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>            | 500D E12Eh                | 5001 F12Eh                | 5005 F12Eh                |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>         | 500D E130h                | 5001 F130h                | 5005 F130h                |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>         | 500D E132h                | 5001 F132h                | 5005 F132h                |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>            | 500D E136h                | 5001 F136h                | 5005 F136h                |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a>     | 500D E13Ah                | 5001 F13Ah                | 5005 F13Ah                |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>            | 500D E148h                | 5001 F148h                | 5005 F148h                |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>             | 500D E14Ch                | 5001 F14Ch                | 5005 F14Ch                |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>            | 500D E150h                | 5001 F150h                | 5005 F150h                |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>            | 500D E154h                | 5001 F154h                | 5005 F154h                |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 500D E158h                | 5001 F158h                | 5005 F158h                |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 500D E15Ch                | 5001 F15Ch                | 5005 F15Ch                |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 500D E160h                | 5001 F160h                | 5005 F160h                |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 500D E164h                | 5001 F164h                | 5005 F164h                |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 500D E168h                | 5001 F168h                | 5005 F168h                |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 500D E16Ch                | 5001 F16Ch                | 5005 F16Ch                |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 500D E170h                | 5001 F170h                | 5005 F170h                |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 500D E174h                | 5001 F174h                | 5005 F174h                |
| 180h   | 16     | <a href="#">EPWM_DCTRIPSEL</a>        | 500D E180h                | 5001 F180h                | 5005 F180h                |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 500D E186h                | 5001 F186h                | 5005 F186h                |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 500D E188h                | 5001 F188h                | 5005 F188h                |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 500D E18Eh                | 5001 F18Eh                | 5005 F18Eh                |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 500D E190h                | 5001 F190h                | 5005 F190h                |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 500D E192h                | 5001 F192h                | 5005 F192h                |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 500D E194h                | 5001 F194h                | 5005 F194h                |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 500D E196h                | 5001 F196h                | 5005 F196h                |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 500D E198h                | 5001 F198h                | 5005 F198h                |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 500D E19Ah                | 5001 F19Ah                | 5005 F19Ah                |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 500D E19Ch                | 5001 F19Ch                | 5005 F19Ch                |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 500D E19Eh                | 5001 F19Eh                | 5005 F19Eh                |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 500D E1A4h                | 5001 F1A4h                | 5005 F1A4h                |

**Table 3-812. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM5_G3 Physical Address | EPWM6_G3 Physical Address | EPWM7_G3 Physical Address |
|--------|--------|-------------------------------------|---------------------------|---------------------------|---------------------------|
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>    | 500D E1A6h                | 5001 F1A6h                | 5005 F1A6h                |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>    | 500D E1A8h                | 5001 F1A8h                | 5005 F1A8h                |
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>    | 500D E1AAh                | 5001 F1AAh                | 5005 F1AAh                |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>         | 500D E1ACh                | 5001 F1ACh                | 5005 F1ACh                |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a> | 500D E1AEh                | 5001 F1AEh                | 5005 F1AEh                |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>   | 500D E1B0h                | 5001 F1B0h                | 5005 F1B0h                |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>     | 500D E1B2h                | 5001 F1B2h                | 5005 F1B2h                |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>       | 500D E1F4h                | 5001 F1F4h                | 5005 F1F4h                |
| 1FAh   | 16     | <a href="#">EPWM_HWVDELVAL</a>      | 500D E1FAh                | 5001 F1FAh                | 5005 F1FAh                |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>        | 500D E1FCh                | 5001 F1FCh                | 5005 F1FCh                |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>       | 500D E400h                | 5001 F400h                | 5005 F400h                |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>       | 500D E410h                | 5001 F410h                | 5005 F410h                |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>          | 500D E418h                | 5001 F418h                | 5005 F418h                |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a> | 500D E41Ch                | 5001 F41Ch                | 5005 F41Ch                |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>   | 500D E420h                | 5001 F420h                | 5005 F420h                |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>   | 500D E428h                | 5001 F428h                | 5005 F428h                |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>   | 500D E430h                | 5001 F430h                | 5005 F430h                |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>   | 500D E600h                | 5001 F600h                | 5005 F600h                |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>   | 500D E604h                | 5001 F604h                | 5005 F604h                |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>   | 500D E608h                | 5001 F608h                | 5005 F608h                |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>   | 500D E60Ch                | 5001 F60Ch                | 5005 F60Ch                |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>   | 500D E610h                | 5001 F610h                | 5005 F610h                |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 500D E614h                | 5001 F614h                | 5005 F614h                |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 500D E618h                | 5001 F618h                | 5005 F618h                |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 500D E61Ch                | 5001 F61Ch                | 5005 F61Ch                |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 500D E620h                | 5001 F620h                | 5005 F620h                |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 500D E630h                | 5001 F630h                | 5005 F630h                |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 500D E632h                | 5001 F632h                | 5005 F632h                |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 500D E644h                | 5001 F644h                | 5005 F644h                |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 500D E680h                | 5001 F680h                | 5005 F680h                |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 500D E684h                | 5001 F684h                | 5005 F684h                |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 500D E688h                | 5001 F688h                | 5005 F688h                |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 500D E68Ch                | 5001 F68Ch                | 5005 F68Ch                |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 500D E690h                | 5001 F690h                | 5005 F690h                |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 500D E694h                | 5001 F694h                | 5005 F694h                |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 500D E698h                | 5001 F698h                | 5005 F698h                |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 500D E69Ch                | 5001 F69Ch                | 5005 F69Ch                |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 500D E6A0h                | 5001 F6A0h                | 5005 F6A0h                |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 500D E6B0h                | 5001 F6B0h                | 5005 F6B0h                |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 500D E6B2h                | 5001 F6B2h                | 5005 F6B2h                |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 500D E6BAh                | 5001 F6BAh                | 5005 F6BAh                |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 500D E6BEh                | 5001 F6BEh                | 5005 F6BEh                |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 500D E6C4h                | 5001 F6C4h                | 5005 F6C4h                |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 500D E700h                | 5001 F700h                | 5005 F700h                |

**Table 3-812. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM5_G3 Physical Address | EPWM6_G3 Physical Address | EPWM7_G3 Physical Address |
|--------|--------|------------------------------------|---------------------------|---------------------------|---------------------------|
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>   | 500D E704h                | 5001 F704h                | 5005 F704h                |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>   | 500D E708h                | 5001 F708h                | 5005 F708h                |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>   | 500D E70Ch                | 5001 F70Ch                | 5005 F70Ch                |
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>   | 500D E710h                | 5001 F710h                | 5005 F710h                |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>   | 500D E714h                | 5001 F714h                | 5005 F714h                |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>   | 500D E718h                | 5001 F718h                | 5005 F718h                |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>   | 500D E71Ch                | 5001 F71Ch                | 5005 F71Ch                |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>  | 500D E720h                | 5001 F720h                | 5005 F720h                |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a> | 500D E730h                | 5001 F730h                | 5005 F730h                |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a> | 500D E732h                | 5001 F732h                | 5005 F732h                |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>    | 500D E73Ah                | 5001 F73Ah                | 5005 F73Ah                |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>    | 500D E73Eh                | 5001 F73Eh                | 5005 F73Eh                |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a> | 500D E744h                | 5001 F744h                | 5005 F744h                |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 500D E780h                | 5001 F780h                | 5005 F780h                |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 500D E784h                | 5001 F784h                | 5005 F784h                |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 500D E788h                | 5001 F788h                | 5005 F788h                |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 500D E78Ch                | 5001 F78Ch                | 5005 F78Ch                |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 500D E790h                | 5001 F790h                | 5005 F790h                |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 500D E794h                | 5001 F794h                | 5005 F794h                |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 500D E798h                | 5001 F798h                | 5005 F798h                |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 500D E79Ch                | 5001 F79Ch                | 5005 F79Ch                |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 500D E7A0h                | 5001 F7A0h                | 5005 F7A0h                |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 500D E7B0h                | 5001 F7B0h                | 5005 F7B0h                |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 500D E7B2h                | 5001 F7B2h                | 5005 F7B2h                |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 500D E7BAh                | 5001 F7BAh                | 5005 F7BAh                |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 500D E7BEh                | 5001 F7BEh                | 5005 F7BEh                |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 500D E7C4h                | 5001 F7C4h                | 5005 F7C4h                |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 500D E800h                | 5001 F800h                | 5005 F800h                |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 500D E804h                | 5001 F804h                | 5005 F804h                |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 500D E808h                | 5001 F808h                | 5005 F808h                |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 500D E80Ch                | 5001 F80Ch                | 5005 F80Ch                |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 500D E810h                | 5001 F810h                | 5005 F810h                |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 500D E814h                | 5001 F814h                | 5005 F814h                |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 500D E820h                | 5001 F820h                | 5005 F820h                |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 500D E824h                | 5001 F824h                | 5005 F824h                |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 500D E828h                | 5001 F828h                | 5005 F828h                |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 500D E82Ch                | 5001 F82Ch                | 5005 F82Ch                |
| C00h   | 32     | <a href="#">EPWM_MINDBCFCG</a>     | 500D EC00h                | 5001 FC00h                | 5005 FC00h                |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 500D EC04h                | 5001 FC04h                | 5005 FC04h                |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 500D EC20h                | 5001 FC20h                | 5005 FC20h                |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 500D EC24h                | 5001 FC24h                | 5005 FC24h                |

**Table 3-813. EPWM Registers, Base Address=5000 0000h, Length=4096**

| Offset | Length | Register Name                      | EPWM8_G3 Physical Address | EPWM9_G3 Physical Address |
|--------|--------|------------------------------------|---------------------------|---------------------------|
| 0h     | 16     | <a href="#">EPWM_TBCTL</a>         | 5009 F000h                | 500D F000h                |
| 2h     | 16     | <a href="#">EPWM_TBCTL2</a>        | 5009 F002h                | 500D F002h                |
| 6h     | 16     | <a href="#">EPWM_EPWMSYNCINSEL</a> | 5009 F006h                | 500D F006h                |
| 8h     | 16     | <a href="#">EPWM_TBCTR</a>         | 5009 F008h                | 500D F008h                |
| Ah     | 16     | <a href="#">EPWM_TBSTS</a>         | 5009 F00Ah                | 500D F00Ah                |
| Ch     | 16     | <a href="#">EPWM_EPWMSYNCOUEN</a>  | 5009 F00Ch                | 500D F00Ch                |
| Eh     | 16     | <a href="#">EPWM_TBCTL3</a>        | 5009 F00Eh                | 500D F00Eh                |
| 10h    | 16     | <a href="#">EPWM_CMPCTL</a>        | 5009 F010h                | 500D F010h                |
| 12h    | 16     | <a href="#">EPWM_CMPCTL2</a>       | 5009 F012h                | 500D F012h                |
| 18h    | 16     | <a href="#">EPWM_DBCTL</a>         | 5009 F018h                | 500D F018h                |
| 1Ah    | 16     | <a href="#">EPWM_DBCTL2</a>        | 5009 F01Ah                | 500D F01Ah                |
| 20h    | 16     | <a href="#">EPWM_AQCTL</a>         | 5009 F020h                | 500D F020h                |
| 22h    | 16     | <a href="#">EPWM_AQTSRCSEL</a>     | 5009 F022h                | 500D F022h                |
| 28h    | 16     | <a href="#">EPWM_PCCTL</a>         | 5009 F028h                | 500D F028h                |
| 30h    | 16     | <a href="#">EPWM_VCAPCTL</a>       | 5009 F030h                | 500D F030h                |
| 32h    | 16     | <a href="#">EPWM_VCNTCFG</a>       | 5009 F032h                | 500D F032h                |
| 40h    | 16     | <a href="#">EPWM_HRCNFG</a>        | 5009 F040h                | 500D F040h                |
| 4Eh    | 16     | <a href="#">EPWM_HRCNFG2</a>       | 5009 F04Eh                | 500D F04Eh                |
| 5Ah    | 16     | <a href="#">EPWM_HRPCTL</a>        | 5009 F05Ah                | 500D F05Ah                |
| 5Ch    | 16     | <a href="#">EPWM_TRREM</a>         | 5009 F05Ch                | 500D F05Ch                |
| 68h    | 16     | <a href="#">EPWM_GLDCTL</a>        | 5009 F068h                | 500D F068h                |
| 6Ah    | 16     | <a href="#">EPWM_GLDCFG</a>        | 5009 F06Ah                | 500D F06Ah                |
| 70h    | 32     | <a href="#">EPWM_EPWMXLINK</a>     | 5009 F070h                | 500D F070h                |
| 74h    | 32     | <a href="#">EPWM_EPWMXLINK2</a>    | 5009 F074h                | 500D F074h                |
| 7Ah    | 16     | <a href="#">EPWM_ETEST</a>         | 5009 F07Ah                | 500D F07Ah                |
| 7Ch    | 16     | <a href="#">EPWM_EPWMREV</a>       | 5009 F07Ch                | 500D F07Ch                |
| 7Eh    | 16     | <a href="#">EPWM_HRPWMREV</a>      | 5009 F07Eh                | 500D F07Eh                |
| 80h    | 16     | <a href="#">EPWM_AQCTLA</a>        | 5009 F080h                | 500D F080h                |
| 82h    | 16     | <a href="#">EPWM_AQCTLA2</a>       | 5009 F082h                | 500D F082h                |
| 84h    | 16     | <a href="#">EPWM_AQCTLB</a>        | 5009 F084h                | 500D F084h                |
| 86h    | 16     | <a href="#">EPWM_AQCTLB2</a>       | 5009 F086h                | 500D F086h                |
| 8Eh    | 16     | <a href="#">EPWM_AQSFR</a>         | 5009 F08Eh                | 500D F08Eh                |
| 92h    | 16     | <a href="#">EPWM_AQCSFR</a>        | 5009 F092h                | 500D F092h                |
| A0h    | 16     | <a href="#">EPWM_DBREDHR</a>       | 5009 F0A0h                | 500D F0A0h                |
| A2h    | 16     | <a href="#">EPWM_DBRED</a>         | 5009 F0A2h                | 500D F0A2h                |
| A4h    | 16     | <a href="#">EPWM_DBFEDHR</a>       | 5009 F0A4h                | 500D F0A4h                |
| A6h    | 16     | <a href="#">EPWM_DBFED</a>         | 5009 F0A6h                | 500D F0A6h                |
| C0h    | 32     | <a href="#">EPWM_TBPHS</a>         | 5009 F0C0h                | 500D F0C0h                |
| C4h    | 16     | <a href="#">EPWM_TBPRDHR</a>       | 5009 F0C4h                | 500D F0C4h                |
| C6h    | 16     | <a href="#">EPWM_TBPRD</a>         | 5009 F0C6h                | 500D F0C6h                |
| C8h    | 16     | <a href="#">EPWM_TBPRDHRB</a>      | 5009 F0C8h                | 500D F0C8h                |
| D4h    | 32     | <a href="#">EPWM_CMPA</a>          | 5009 F0D4h                | 500D F0D4h                |
| D8h    | 32     | <a href="#">EPWM_CMPB</a>          | 5009 F0D8h                | 500D F0D8h                |
| DEh    | 16     | <a href="#">EPWM_CMPC</a>          | 5009 F0DEh                | 500D F0DEh                |
| E2h    | 16     | <a href="#">EPWM_CMPD</a>          | 5009 F0E2h                | 500D F0E2h                |

**Table 3-813. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                         | EPWM8_G3 Physical Address | EPWM9_G3 Physical Address |
|--------|--------|---------------------------------------|---------------------------|---------------------------|
| E8h    | 16     | <a href="#">EPWM_GLDCTL2</a>          | 5009 F0E8h                | 500D F0E8h                |
| EEh    | 16     | <a href="#">EPWM_SWVDELVAL</a>        | 5009 F0EEh                | 500D F0EEh                |
| 100h   | 16     | <a href="#">EPWM_TZSEL</a>            | 5009 F100h                | 500D F100h                |
| 102h   | 16     | <a href="#">EPWM_TZSEL2</a>           | 5009 F102h                | 500D F102h                |
| 104h   | 16     | <a href="#">EPWM_TZDCSEL</a>          | 5009 F104h                | 500D F104h                |
| 108h   | 16     | <a href="#">EPWM_TZCTL</a>            | 5009 F108h                | 500D F108h                |
| 10Ah   | 16     | <a href="#">EPWM_TZCTL2</a>           | 5009 F10Ah                | 500D F10Ah                |
| 10Ch   | 16     | <a href="#">EPWM_TZCTLDCA</a>         | 5009 F10Ch                | 500D F10Ch                |
| 10Eh   | 16     | <a href="#">EPWM_TZCTLDCB</a>         | 5009 F10Eh                | 500D F10Eh                |
| 11Ah   | 16     | <a href="#">EPWM_TZEINT</a>           | 5009 F11Ah                | 500D F11Ah                |
| 126h   | 16     | <a href="#">EPWM_TZFLG</a>            | 5009 F126h                | 500D F126h                |
| 128h   | 16     | <a href="#">EPWM_TZCBCFLG</a>         | 5009 F128h                | 500D F128h                |
| 12Ah   | 16     | <a href="#">EPWM_TZOSTFLG</a>         | 5009 F12Ah                | 500D F12Ah                |
| 12Eh   | 16     | <a href="#">EPWM_TZCLR</a>            | 5009 F12Eh                | 500D F12Eh                |
| 130h   | 16     | <a href="#">EPWM_TZCBCCLR</a>         | 5009 F130h                | 500D F130h                |
| 132h   | 16     | <a href="#">EPWM_TZOSTCLR</a>         | 5009 F132h                | 500D F132h                |
| 136h   | 16     | <a href="#">EPWM_TZFRC</a>            | 5009 F136h                | 500D F136h                |
| 13Ah   | 16     | <a href="#">EPWM_TZTRIPOUTSEL</a>     | 5009 F13Ah                | 500D F13Ah                |
| 148h   | 16     | <a href="#">EPWM_ETSEL</a>            | 5009 F148h                | 500D F148h                |
| 14Ch   | 16     | <a href="#">EPWM_ETPS</a>             | 5009 F14Ch                | 500D F14Ch                |
| 150h   | 16     | <a href="#">EPWM_ETFLG</a>            | 5009 F150h                | 500D F150h                |
| 154h   | 16     | <a href="#">EPWM_ETCLR</a>            | 5009 F154h                | 500D F154h                |
| 158h   | 16     | <a href="#">EPWM_ETFRC</a>            | 5009 F158h                | 500D F158h                |
| 15Ch   | 16     | <a href="#">EPWM_ETINTPS</a>          | 5009 F15Ch                | 500D F15Ch                |
| 160h   | 16     | <a href="#">EPWM_ETSOCPS</a>          | 5009 F160h                | 500D F160h                |
| 164h   | 16     | <a href="#">EPWM_ETCNTINITCTL</a>     | 5009 F164h                | 500D F164h                |
| 168h   | 16     | <a href="#">EPWM_ETCNTINIT</a>        | 5009 F168h                | 500D F168h                |
| 16Ch   | 16     | <a href="#">EPWM_ETINTMIXEN</a>       | 5009 F16Ch                | 500D F16Ch                |
| 170h   | 16     | <a href="#">EPWM_ETSOCAMIXEN</a>      | 5009 F170h                | 500D F170h                |
| 174h   | 16     | <a href="#">EPWM_ETSOCBMIXEN</a>      | 5009 F174h                | 500D F174h                |
| 180h   | 16     | <a href="#">EPWM_DCTRIPISEL</a>       | 5009 F180h                | 500D F180h                |
| 186h   | 16     | <a href="#">EPWM_DCACTL</a>           | 5009 F186h                | 500D F186h                |
| 188h   | 16     | <a href="#">EPWM_DCBCTL</a>           | 5009 F188h                | 500D F188h                |
| 18Eh   | 16     | <a href="#">EPWM_DCFCTL</a>           | 5009 F18Eh                | 500D F18Eh                |
| 190h   | 16     | <a href="#">EPWM_DCCAPCTL</a>         | 5009 F190h                | 500D F190h                |
| 192h   | 16     | <a href="#">EPWM_DCFOFFSET</a>        | 5009 F192h                | 500D F192h                |
| 194h   | 16     | <a href="#">EPWM_DCFOFFSETCNT</a>     | 5009 F194h                | 500D F194h                |
| 196h   | 16     | <a href="#">EPWM_DCFWINDOW</a>        | 5009 F196h                | 500D F196h                |
| 198h   | 16     | <a href="#">EPWM_DCFWINDOWCNT</a>     | 5009 F198h                | 500D F198h                |
| 19Ah   | 16     | <a href="#">EPWM_BLANKPULSEMIXSEL</a> | 5009 F19Ah                | 500D F19Ah                |
| 19Ch   | 16     | <a href="#">EPWM_DCCAPMIXSEL</a>      | 5009 F19Ch                | 500D F19Ch                |
| 19Eh   | 16     | <a href="#">EPWM_DCCAP</a>            | 5009 F19Eh                | 500D F19Eh                |
| 1A4h   | 16     | <a href="#">EPWM_DCAHTRIPSEL</a>      | 5009 F1A4h                | 500D F1A4h                |
| 1A6h   | 16     | <a href="#">EPWM_DCALTRIPSEL</a>      | 5009 F1A6h                | 500D F1A6h                |
| 1A8h   | 16     | <a href="#">EPWM_DCBHTRIPSEL</a>      | 5009 F1A8h                | 500D F1A8h                |

**Table 3-813. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                       | EPWM8_G3 Physical Address | EPWM9_G3 Physical Address |
|--------|--------|-------------------------------------|---------------------------|---------------------------|
| 1AAh   | 16     | <a href="#">EPWM_DCBLTRIPSEL</a>    | 5009 F1AAh                | 500D F1AAh                |
| 1ACh   | 16     | <a href="#">EPWM_CAPCTL</a>         | 5009 F1ACh                | 500D F1ACh                |
| 1AEh   | 16     | <a href="#">EPWM_CAPGATETRIPSEL</a> | 5009 F1AEh                | 500D F1AEh                |
| 1B0h   | 16     | <a href="#">EPWM_CAPINTRIPSEL</a>   | 5009 F1B0h                | 500D F1B0h                |
| 1B2h   | 16     | <a href="#">EPWM_CAPTRIPSEL</a>     | 5009 F1B2h                | 500D F1B2h                |
| 1F4h   | 32     | <a href="#">EPWM_EPWMLOCK</a>       | 5009 F1F4h                | 500D F1F4h                |
| 1FAh   | 16     | <a href="#">EPWM_HWVDLVAL</a>       | 5009 F1FAh                | 500D F1FAh                |
| 1FCh   | 16     | <a href="#">EPWM_VCNTVAL</a>        | 5009 F1FCh                | 500D F1FCh                |
| 400h   | 32     | <a href="#">EPWM_XCMPCTL1</a>       | 5009 F400h                | 500D F400h                |
| 410h   | 32     | <a href="#">EPWM_XLOADCTL</a>       | 5009 F410h                | 500D F410h                |
| 418h   | 32     | <a href="#">EPWM_XLOAD</a>          | 5009 F418h                | 500D F418h                |
| 41Ch   | 32     | <a href="#">EPWM_EPWMXLINKXLOAD</a> | 5009 F41Ch                | 500D F41Ch                |
| 420h   | 32     | <a href="#">EPWM_XREGSHDW1STS</a>   | 5009 F420h                | 500D F420h                |
| 428h   | 32     | <a href="#">EPWM_XREGSHDW2STS</a>   | 5009 F428h                | 500D F428h                |
| 430h   | 32     | <a href="#">EPWM_XREGSHDW3STS</a>   | 5009 F430h                | 500D F430h                |
| 600h   | 32     | <a href="#">EPWM_XCMP1_ACTIVE</a>   | 5009 F600h                | 500D F600h                |
| 604h   | 32     | <a href="#">EPWM_XCMP2_ACTIVE</a>   | 5009 F604h                | 500D F604h                |
| 608h   | 32     | <a href="#">EPWM_XCMP3_ACTIVE</a>   | 5009 F608h                | 500D F608h                |
| 60Ch   | 32     | <a href="#">EPWM_XCMP4_ACTIVE</a>   | 5009 F60Ch                | 500D F60Ch                |
| 610h   | 32     | <a href="#">EPWM_XCMP5_ACTIVE</a>   | 5009 F610h                | 500D F610h                |
| 614h   | 32     | <a href="#">EPWM_XCMP6_ACTIVE</a>   | 5009 F614h                | 500D F614h                |
| 618h   | 32     | <a href="#">EPWM_XCMP7_ACTIVE</a>   | 5009 F618h                | 500D F618h                |
| 61Ch   | 32     | <a href="#">EPWM_XCMP8_ACTIVE</a>   | 5009 F61Ch                | 500D F61Ch                |
| 620h   | 32     | <a href="#">EPWM_XTBPRD_ACTIVE</a>  | 5009 F620h                | 500D F620h                |
| 630h   | 16     | <a href="#">EPWM_XAQCTLA_ACTIVE</a> | 5009 F630h                | 500D F630h                |
| 632h   | 16     | <a href="#">EPWM_XAQCTLB_ACTIVE</a> | 5009 F632h                | 500D F632h                |
| 644h   | 32     | <a href="#">EPWM_XMINMAX_ACTIVE</a> | 5009 F644h                | 500D F644h                |
| 680h   | 32     | <a href="#">EPWM_XCMP1_SHDW1</a>    | 5009 F680h                | 500D F680h                |
| 684h   | 32     | <a href="#">EPWM_XCMP2_SHDW1</a>    | 5009 F684h                | 500D F684h                |
| 688h   | 32     | <a href="#">EPWM_XCMP3_SHDW1</a>    | 5009 F688h                | 500D F688h                |
| 68Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW1</a>    | 5009 F68Ch                | 500D F68Ch                |
| 690h   | 32     | <a href="#">EPWM_XCMP5_SHDW1</a>    | 5009 F690h                | 500D F690h                |
| 694h   | 32     | <a href="#">EPWM_XCMP6_SHDW1</a>    | 5009 F694h                | 500D F694h                |
| 698h   | 32     | <a href="#">EPWM_XCMP7_SHDW1</a>    | 5009 F698h                | 500D F698h                |
| 69Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW1</a>    | 5009 F69Ch                | 500D F69Ch                |
| 6A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW1</a>   | 5009 F6A0h                | 500D F6A0h                |
| 6B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW1</a>  | 5009 F6B0h                | 500D F6B0h                |
| 6B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW1</a>  | 5009 F6B2h                | 500D F6B2h                |
| 6BAh   | 16     | <a href="#">EPWM_CMPC_SHDW1</a>     | 5009 F6BAh                | 500D F6BAh                |
| 6BEh   | 16     | <a href="#">EPWM_CMPD_SHDW1</a>     | 5009 F6BEh                | 500D F6BEh                |
| 6C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW1</a>  | 5009 F6C4h                | 500D F6C4h                |
| 700h   | 32     | <a href="#">EPWM_XCMP1_SHDW2</a>    | 5009 F700h                | 500D F700h                |
| 704h   | 32     | <a href="#">EPWM_XCMP2_SHDW2</a>    | 5009 F704h                | 500D F704h                |
| 708h   | 32     | <a href="#">EPWM_XCMP3_SHDW2</a>    | 5009 F708h                | 500D F708h                |
| 70Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW2</a>    | 5009 F70Ch                | 500D F70Ch                |



**Table 3-813. EPWM Registers, Base Address=5000 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                      | EPWM8_G3 Physical Address | EPWM9_G3 Physical Address |
|--------|--------|------------------------------------|---------------------------|---------------------------|
| 710h   | 32     | <a href="#">EPWM_XCMP5_SHDW2</a>   | 5009 F710h                | 500D F710h                |
| 714h   | 32     | <a href="#">EPWM_XCMP6_SHDW2</a>   | 5009 F714h                | 500D F714h                |
| 718h   | 32     | <a href="#">EPWM_XCMP7_SHDW2</a>   | 5009 F718h                | 500D F718h                |
| 71Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW2</a>   | 5009 F71Ch                | 500D F71Ch                |
| 720h   | 32     | <a href="#">EPWM_XTBPRD_SHDW2</a>  | 5009 F720h                | 500D F720h                |
| 730h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW2</a> | 5009 F730h                | 500D F730h                |
| 732h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW2</a> | 5009 F732h                | 500D F732h                |
| 73Ah   | 16     | <a href="#">EPWM_CMPC_SHDW2</a>    | 5009 F73Ah                | 500D F73Ah                |
| 73Eh   | 16     | <a href="#">EPWM_CMPD_SHDW2</a>    | 5009 F73Eh                | 500D F73Eh                |
| 744h   | 32     | <a href="#">EPWM_XMINMAX_SHDW2</a> | 5009 F744h                | 500D F744h                |
| 780h   | 32     | <a href="#">EPWM_XCMP1_SHDW3</a>   | 5009 F780h                | 500D F780h                |
| 784h   | 32     | <a href="#">EPWM_XCMP2_SHDW3</a>   | 5009 F784h                | 500D F784h                |
| 788h   | 32     | <a href="#">EPWM_XCMP3_SHDW3</a>   | 5009 F788h                | 500D F788h                |
| 78Ch   | 32     | <a href="#">EPWM_XCMP4_SHDW3</a>   | 5009 F78Ch                | 500D F78Ch                |
| 790h   | 32     | <a href="#">EPWM_XCMP5_SHDW3</a>   | 5009 F790h                | 500D F790h                |
| 794h   | 32     | <a href="#">EPWM_XCMP6_SHDW3</a>   | 5009 F794h                | 500D F794h                |
| 798h   | 32     | <a href="#">EPWM_XCMP7_SHDW3</a>   | 5009 F798h                | 500D F798h                |
| 79Ch   | 32     | <a href="#">EPWM_XCMP8_SHDW3</a>   | 5009 F79Ch                | 500D F79Ch                |
| 7A0h   | 32     | <a href="#">EPWM_XTBPRD_SHDW3</a>  | 5009 F7A0h                | 500D F7A0h                |
| 7B0h   | 16     | <a href="#">EPWM_XAQCTLA_SHDW3</a> | 5009 F7B0h                | 500D F7B0h                |
| 7B2h   | 16     | <a href="#">EPWM_XAQCTLB_SHDW3</a> | 5009 F7B2h                | 500D F7B2h                |
| 7BAh   | 16     | <a href="#">EPWM_CMPC_SHDW3</a>    | 5009 F7BAh                | 500D F7BAh                |
| 7BEh   | 16     | <a href="#">EPWM_CMPD_SHDW3</a>    | 5009 F7BEh                | 500D F7BEh                |
| 7C4h   | 32     | <a href="#">EPWM_XMINMAX_SHDW3</a> | 5009 F7C4h                | 500D F7C4h                |
| 800h   | 32     | <a href="#">EPWM_DECTL</a>         | 5009 F800h                | 500D F800h                |
| 804h   | 32     | <a href="#">EPWM_DECOMPSEL</a>     | 5009 F804h                | 500D F804h                |
| 808h   | 32     | <a href="#">EPWM_DEACTCTL</a>      | 5009 F808h                | 500D F808h                |
| 80Ch   | 32     | <a href="#">EPWM_DESTS</a>         | 5009 F80Ch                | 500D F80Ch                |
| 810h   | 32     | <a href="#">EPWM_DEFRC</a>         | 5009 F810h                | 500D F810h                |
| 814h   | 32     | <a href="#">EPWM_DECLR</a>         | 5009 F814h                | 500D F814h                |
| 820h   | 32     | <a href="#">EPWM_DEMONCNT</a>      | 5009 F820h                | 500D F820h                |
| 824h   | 32     | <a href="#">EPWM_DEMONCTL</a>      | 5009 F824h                | 500D F824h                |
| 828h   | 32     | <a href="#">EPWM_DEMONSTEP</a>     | 5009 F828h                | 500D F828h                |
| 82Ch   | 32     | <a href="#">EPWM_DEMONTHRES</a>    | 5009 F82Ch                | 500D F82Ch                |
| C00h   | 32     | <a href="#">EPWM_MINDBCFG</a>      | 5009 FC00h                | 500D FC00h                |
| C04h   | 32     | <a href="#">EPWM_MINDBDLY</a>      | 5009 FC04h                | 500D FC04h                |
| C20h   | 32     | <a href="#">EPWM_LUTCTLA</a>       | 5009 FC20h                | 500D FC20h                |
| C24h   | 32     | <a href="#">EPWM_LUTCTLB</a>       | 5009 FC24h                | 500D FC24h                |

### 3.7.2 EPWM Registers

#### EPWM Registers



### 3.7.2.1 EPWM\_TBCTL Register

#### 1 EPWM\_TBCTL Register (Offset = 0h) [reset = 83h]

Time Base Control Register.

Return to [Summary Table](#)

**Table 3-814. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0000h       |
| EPWM0_G1      | 5004 0000h       |
| EPWM0_G2      | 5008 0000h       |
| EPWM0_G3      | 500C 0000h       |
| EPWM1_G0      | 5000 1000h       |
| EPWM1_G1      | 5004 1000h       |
| EPWM1_G2      | 5008 1000h       |
| EPWM1_G3      | 500C 1000h       |
| EPWM2_G0      | 5000 2000h       |
| EPWM2_G1      | 5004 2000h       |
| EPWM2_G2      | 5008 2000h       |
| EPWM2_G3      | 500C 2000h       |
| EPWM3_G0      | 5000 3000h       |
| EPWM3_G1      | 5004 3000h       |
| EPWM3_G2      | 5008 3000h       |
| EPWM3_G3      | 500C 3000h       |
| EPWM4_G0      | 5000 4000h       |
| EPWM4_G1      | 5004 4000h       |
| EPWM4_G2      | 5008 4000h       |
| EPWM4_G3      | 500C 4000h       |
| EPWM5_G0      | 5000 5000h       |
| EPWM5_G1      | 5004 5000h       |
| EPWM5_G2      | 5008 5000h       |
| EPWM5_G3      | 500C 5000h       |
| EPWM6_G0      | 5000 6000h       |
| EPWM6_G1      | 5004 6000h       |
| EPWM6_G2      | 5008 6000h       |
| EPWM6_G3      | 500C 6000h       |
| EPWM7_G0      | 5000 7000h       |
| EPWM7_G1      | 5004 7000h       |
| EPWM7_G2      | 5008 7000h       |
| EPWM7_G3      | 500C 7000h       |
| EPWM8_G0      | 5000 8000h       |
| EPWM8_G1      | 5004 8000h       |
| EPWM8_G2      | 5008 8000h       |
| EPWM8_G3      | 500C 8000h       |
| EPWM9_G0      | 5000 9000h       |
| EPWM9_G1      | 5004 9000h       |
| EPWM9_G2      | 5008 9000h       |

**Table 3-814. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9000h       |
| EPWM10_G0     | 5000 A000h       |
| EPWM10_G1     | 5004 A000h       |
| EPWM10_G2     | 5008 A000h       |
| EPWM10_G3     | 500C A000h       |
| EPWM11_G0     | 5000 B000h       |
| EPWM11_G1     | 5004 B000h       |
| EPWM11_G2     | 5008 B000h       |
| EPWM11_G3     | 500C B000h       |
| EPWM12_G0     | 5000 C000h       |
| EPWM12_G1     | 5004 C000h       |
| EPWM12_G2     | 5008 C000h       |
| EPWM12_G3     | 500C C000h       |
| EPWM13_G0     | 5000 D000h       |
| EPWM13_G1     | 5004 D000h       |
| EPWM13_G2     | 5008 D000h       |
| EPWM13_G3     | 500C D000h       |
| EPWM14_G0     | 5000 E000h       |
| EPWM14_G1     | 5004 E000h       |
| EPWM14_G2     | 5008 E000h       |
| EPWM14_G3     | 500C E000h       |
| EPWM15_G0     | 5000 F000h       |
| EPWM15_G1     | 5004 F000h       |
| EPWM15_G2     | 5008 F000h       |
| EPWM15_G3     | 500C F000h       |
| EPWM16_G0     | 5001 0000h       |
| EPWM16_G1     | 5005 0000h       |
| EPWM16_G2     | 5009 0000h       |
| EPWM16_G3     | 500D 0000h       |
| EPWM17_G0     | 5001 1000h       |
| EPWM17_G1     | 5005 1000h       |
| EPWM17_G2     | 5009 1000h       |
| EPWM17_G3     | 500D 1000h       |
| EPWM18_G0     | 5001 2000h       |
| EPWM18_G1     | 5005 2000h       |
| EPWM18_G2     | 5009 2000h       |
| EPWM18_G3     | 500D 2000h       |
| EPWM19_G0     | 5001 3000h       |
| EPWM19_G1     | 5005 3000h       |
| EPWM19_G2     | 5009 3000h       |
| EPWM19_G3     | 500D 3000h       |
| EPWM20_G0     | 5001 4000h       |
| EPWM20_G1     | 5005 4000h       |
| EPWM20_G2     | 5009 4000h       |
| EPWM20_G3     | 500D 4000h       |

**Table 3-814. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5000h       |
| EPWM21_G1     | 5005 5000h       |
| EPWM21_G2     | 5009 5000h       |
| EPWM21_G3     | 500D 5000h       |
| EPWM22_G0     | 5001 6000h       |
| EPWM22_G1     | 5005 6000h       |
| EPWM22_G2     | 5009 6000h       |
| EPWM22_G3     | 500D 6000h       |
| EPWM23_G0     | 5001 7000h       |
| EPWM23_G1     | 5005 7000h       |
| EPWM23_G2     | 5009 7000h       |
| EPWM23_G3     | 500D 7000h       |
| EPWM24_G0     | 5001 8000h       |
| EPWM24_G1     | 5005 8000h       |
| EPWM24_G2     | 5009 8000h       |
| EPWM24_G3     | 500D 8000h       |
| EPWM25_G0     | 5001 9000h       |
| EPWM25_G1     | 5005 9000h       |
| EPWM25_G2     | 5009 9000h       |
| EPWM25_G3     | 500D 9000h       |
| EPWM26_G0     | 5001 A000h       |
| EPWM26_G1     | 5005 A000h       |
| EPWM26_G2     | 5009 A000h       |
| EPWM26_G3     | 500D A000h       |
| EPWM27_G0     | 5001 B000h       |
| EPWM27_G1     | 5005 B000h       |
| EPWM27_G2     | 5009 B000h       |
| EPWM27_G3     | 500D B000h       |
| EPWM28_G0     | 5001 C000h       |
| EPWM28_G1     | 5005 C000h       |
| EPWM28_G2     | 5009 C000h       |
| EPWM28_G3     | 500D C000h       |
| EPWM29_G0     | 5001 D000h       |
| EPWM29_G1     | 5005 D000h       |
| EPWM29_G2     | 5009 D000h       |
| EPWM29_G3     | 500D D000h       |
| EPWM30_G0     | 5001 E000h       |
| EPWM30_G1     | 5005 E000h       |
| EPWM30_G2     | 5009 E000h       |
| EPWM30_G3     | 500D E000h       |
| EPWM31_G0     | 5001 F000h       |
| EPWM31_G1     | 5005 F000h       |
| EPWM31_G2     | 5009 F000h       |
| EPWM31_G3     | 500D F000h       |

**Figure 3-252. EPWM\_TBCTL Name Register**

| 15        | 14      | 13         | 12     | 11    | 10        | 9       | 8 |
|-----------|---------|------------|--------|-------|-----------|---------|---|
| FREE_SOFT |         | PHSDIR     | CLKDIV |       | HSPCLKDIV |         |   |
| R/W       |         | R/W        | R/W    |       | R/W       |         |   |
| 0h        |         | 0h         | 0h     |       | 1h        |         |   |
| 7         | 6       | 5          | 4      | 3     | 2         | 1       | 0 |
| HSPCLKDIV | SWFSYNC | RESERVED_1 |        | PRDLD | PHSEN     | CTRMODE |   |
| R/W       | R/W1TS  | R          |        | R/W   | R/W       | R/W     |   |
| 1h        | 0h      | 0h         |        | 0h    | 0h        | 3h      |   |

**Table 3-816. EPWM\_TBCTL Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|-----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | FREE_SOFT | R/W  | 0h    | Emulation Mode Bits. These bits select the behavior of the EPWM time-base counter during emulation events<br>00: Stop after the next time-base counter increment or decrement<br>01: Stop when counter completes a whole cycle:<br>- Up-count mode: stop when the time-base counter = period [TBCTR = TBPRD]<br>- Down-count mode: stop when the time-base counter = 0x00 [TBCTR = 0x00]<br>- Up-down-count mode: stop when the time-base counter = 0x00 [TBCTR = 0x00]<br>1x: Free run                                                                       |
| 13    | PHSDIR    | R/W  | 0h    | Phase Direction Bit<br>This bit is only used when the time-base counter is configured in the up-down-count mode. The PHSDIR bit indicates the direction the time-base counter [TBCTR] will count after a synchronization event occurs and a new phase value is loaded from the phase [TBPHS] register. This is irrespective of the direction of the counter before the synchronization event..<br>In the up-count and down-count modes this bit is ignored.<br>0: Count down after the synchronization event.<br>1: Count up after the synchronization event. |
| 12:10 | CLKDIV    | R/W  | 0h    | Time Base Clock Pre-Scale Bits<br>These bits select the time base clock pre-scale value [TBCLK = EPWMCLK/[HSPCLKDIV * CLKDIV]:<br>000:/1 [default on reset]<br>001:/2<br>010:/4<br>011:/8<br>100:/16<br>101:/32<br>110:/64<br>111:/128                                                                                                                                                                                                                                                                                                                        |
| 9:7   | HSPCLKDIV | R/W  | 1h    | High Speed Time Base Clock Pre-Scale Bits<br>These bits determine part of the time-base clock prescale value. TBCLK = EPWMCLK / [HSPCLKDIV x CLKDIV]. This divisor emulates the HSPCLK in the TMS320x281x system as used on the Event Manager [EV] peripheral.<br>000:/1<br>001:/2 [default on reset]<br>010:/4<br>011:/6<br>100:/8<br>101:/10<br>110:/12<br>111:/14                                                                                                                                                                                          |

**Table 3-816. EPWM\_TBCTL Register Field Descriptions (continued)**

| Bit | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|------------|--------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6   | SWFSYNC    | R/W1TS | 0h    | Software Forced Sync Pulse<br>0:Writing a 0 has no effect and reads always return a 0.<br>1:Writing a 1 forces a one-time synchronization pulse to be generated.<br>SWFSYNC can be enabled to effect EPWMxSYNCO by setting the EPWMSYNCOOUTEN.SWEN bit.                                                                                                                                                                                                                                             |
| 5:4 | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 3   | PRDLD      | R/W    | 0h    | Active Period Reg Load from Shadow Select<br>0:The period register [TBPRD] is loaded from its shadow register when the time-base counter, TBCTR, is equal to zero and/or a sync event as determined by the TBCTL2[PRDLDSYNC] bit.<br>A write/read to the TBPRD register accesses the shadow register.<br>1: Immediate Mode [Shadow register bypassed]: A write or read to the TBPRD register accesses the active register.                                                                          |
| 2   | PHSEN      | R/W    | 0h    | Counter Reg Load from Phase Reg Enable<br>0:Do not load the time-base counter [TBCTR] from the time-base phase register [TBPHS].<br>1:Allow Counter to be loaded from the Phase register [TBPHS] and shadow to active load events when an EPWMxSYNCl input signal occurs or a software-forced sync signal, see bit 6.                                                                                                                                                                               |
| 1:0 | CTRMODE    | R/W    | 3h    | Counter Mode<br>The time-base counter mode is normally configured once and not changed during normal operation. If you change the mode of the counter, the change will take effect at the next TBCLK edge and the current counter value shall increment or decrement from the value before the mode change. These bits set the time-base counter mode of operation as follows:<br>00:Up-count mode<br>01:Down-count mode<br>10:Up-down count mode<br>11:Freeze counter operation [default on reset] |

### 3.7.2.2 EPWM\_TBCTL2 Register

#### 1 EPWM\_TBCTL2 Register (Offset = 2h) [reset = 0h]

Time Base Control Register 2

Return to [Summary Table](#)

**Table 3-817. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0002h       |
| EPWM0_G1      | 5004 0002h       |
| EPWM0_G2      | 5008 0002h       |
| EPWM0_G3      | 500C 0002h       |
| EPWM1_G0      | 5000 1002h       |
| EPWM1_G1      | 5004 1002h       |
| EPWM1_G2      | 5008 1002h       |
| EPWM1_G3      | 500C 1002h       |
| EPWM2_G0      | 5000 2002h       |
| EPWM2_G1      | 5004 2002h       |
| EPWM2_G2      | 5008 2002h       |
| EPWM2_G3      | 500C 2002h       |
| EPWM3_G0      | 5000 3002h       |
| EPWM3_G1      | 5004 3002h       |
| EPWM3_G2      | 5008 3002h       |
| EPWM3_G3      | 500C 3002h       |
| EPWM4_G0      | 5000 4002h       |
| EPWM4_G1      | 5004 4002h       |
| EPWM4_G2      | 5008 4002h       |
| EPWM4_G3      | 500C 4002h       |
| EPWM5_G0      | 5000 5002h       |
| EPWM5_G1      | 5004 5002h       |
| EPWM5_G2      | 5008 5002h       |
| EPWM5_G3      | 500C 5002h       |
| EPWM6_G0      | 5000 6002h       |
| EPWM6_G1      | 5004 6002h       |
| EPWM6_G2      | 5008 6002h       |
| EPWM6_G3      | 500C 6002h       |
| EPWM7_G0      | 5000 7002h       |
| EPWM7_G1      | 5004 7002h       |
| EPWM7_G2      | 5008 7002h       |
| EPWM7_G3      | 500C 7002h       |
| EPWM8_G0      | 5000 8002h       |
| EPWM8_G1      | 5004 8002h       |
| EPWM8_G2      | 5008 8002h       |
| EPWM8_G3      | 500C 8002h       |
| EPWM9_G0      | 5000 9002h       |
| EPWM9_G1      | 5004 9002h       |
| EPWM9_G2      | 5008 9002h       |

**Table 3-817. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9002h       |
| EPWM10_G0     | 5000 A002h       |
| EPWM10_G1     | 5004 A002h       |
| EPWM10_G2     | 5008 A002h       |
| EPWM10_G3     | 500C A002h       |
| EPWM11_G0     | 5000 B002h       |
| EPWM11_G1     | 5004 B002h       |
| EPWM11_G2     | 5008 B002h       |
| EPWM11_G3     | 500C B002h       |
| EPWM12_G0     | 5000 C002h       |
| EPWM12_G1     | 5004 C002h       |
| EPWM12_G2     | 5008 C002h       |
| EPWM12_G3     | 500C C002h       |
| EPWM13_G0     | 5000 D002h       |
| EPWM13_G1     | 5004 D002h       |
| EPWM13_G2     | 5008 D002h       |
| EPWM13_G3     | 500C D002h       |
| EPWM14_G0     | 5000 E002h       |
| EPWM14_G1     | 5004 E002h       |
| EPWM14_G2     | 5008 E002h       |
| EPWM14_G3     | 500C E002h       |
| EPWM15_G0     | 5000 F002h       |
| EPWM15_G1     | 5004 F002h       |
| EPWM15_G2     | 5008 F002h       |
| EPWM15_G3     | 500C F002h       |
| EPWM16_G0     | 5001 0002h       |
| EPWM16_G1     | 5005 0002h       |
| EPWM16_G2     | 5009 0002h       |
| EPWM16_G3     | 500D 0002h       |
| EPWM17_G0     | 5001 1002h       |
| EPWM17_G1     | 5005 1002h       |
| EPWM17_G2     | 5009 1002h       |
| EPWM17_G3     | 500D 1002h       |
| EPWM18_G0     | 5001 2002h       |
| EPWM18_G1     | 5005 2002h       |
| EPWM18_G2     | 5009 2002h       |
| EPWM18_G3     | 500D 2002h       |
| EPWM19_G0     | 5001 3002h       |
| EPWM19_G1     | 5005 3002h       |
| EPWM19_G2     | 5009 3002h       |
| EPWM19_G3     | 500D 3002h       |
| EPWM20_G0     | 5001 4002h       |
| EPWM20_G1     | 5005 4002h       |
| EPWM20_G2     | 5009 4002h       |
| EPWM20_G3     | 500D 4002h       |

**Table 3-817. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5002h       |
| EPWM21_G1     | 5005 5002h       |
| EPWM21_G2     | 5009 5002h       |
| EPWM21_G3     | 500D 5002h       |
| EPWM22_G0     | 5001 6002h       |
| EPWM22_G1     | 5005 6002h       |
| EPWM22_G2     | 5009 6002h       |
| EPWM22_G3     | 500D 6002h       |
| EPWM23_G0     | 5001 7002h       |
| EPWM23_G1     | 5005 7002h       |
| EPWM23_G2     | 5009 7002h       |
| EPWM23_G3     | 500D 7002h       |
| EPWM24_G0     | 5001 8002h       |
| EPWM24_G1     | 5005 8002h       |
| EPWM24_G2     | 5009 8002h       |
| EPWM24_G3     | 500D 8002h       |
| EPWM25_G0     | 5001 9002h       |
| EPWM25_G1     | 5005 9002h       |
| EPWM25_G2     | 5009 9002h       |
| EPWM25_G3     | 500D 9002h       |
| EPWM26_G0     | 5001 A002h       |
| EPWM26_G1     | 5005 A002h       |
| EPWM26_G2     | 5009 A002h       |
| EPWM26_G3     | 500D A002h       |
| EPWM27_G0     | 5001 B002h       |
| EPWM27_G1     | 5005 B002h       |
| EPWM27_G2     | 5009 B002h       |
| EPWM27_G3     | 500D B002h       |
| EPWM28_G0     | 5001 C002h       |
| EPWM28_G1     | 5005 C002h       |
| EPWM28_G2     | 5009 C002h       |
| EPWM28_G3     | 500D C002h       |
| EPWM29_G0     | 5001 D002h       |
| EPWM29_G1     | 5005 D002h       |
| EPWM29_G2     | 5009 D002h       |
| EPWM29_G3     | 500D D002h       |
| EPWM30_G0     | 5001 E002h       |
| EPWM30_G1     | 5005 E002h       |
| EPWM30_G2     | 5009 E002h       |
| EPWM30_G3     | 500D E002h       |
| EPWM31_G0     | 5001 F002h       |
| EPWM31_G1     | 5005 F002h       |
| EPWM31_G2     | 5009 F002h       |
| EPWM31_G3     | 500D F002h       |



**Figure 3-253. EPWM\_TBCTL2 Name Register**

| 15        | 14           | 13              | 12         | 11 | 10         | 9 | 8 |
|-----------|--------------|-----------------|------------|----|------------|---|---|
| PRDLDSYNC |              | RESERVED_3      |            |    | RESERVED_2 |   |   |
| R/W       |              | R               |            |    | R          |   |   |
| 0h        |              | 0h              |            |    | 0h         |   |   |
| 7         | 6            | 5               | 4          | 3  | 2          | 1 | 0 |
| OSHTSYNC  | OSHTSYNCMODE | SELFCLRTRE<br>M | RESERVED_1 |    |            |   |   |
| R/W1TS    | R/W          | R/W             | R          |    |            |   |   |
| 0h        | 0h           | 0h              | 0h         |    |            |   |   |

**Table 3-819. EPWM\_TBCTL2 Register Field Descriptions**

| Bit   | Field           | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                      |
|-------|-----------------|--------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | PRDLDSYNC       | R/W    | 0h    | Shadow to Active Period Register Load on SYNC event<br>00:Shadow to Active Load of TBPRD occurs only when TBCTR = 0 [same as legacy].<br>01:Shadow to Active Load of TBPRD occurs both when TBCTR = 0 and when SYNC occurs.<br>10:Shadow to Active Load of TBPRD occurs only when a SYNC is received.<br>11:Reserved<br>Note: This bit selection is valid only if TBCTL[PRDL]=0. |
| 13:12 | RESERVED_3      | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                         |
| 11:8  | RESERVED_2      | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                         |
| 7     | OSHTSYNC        | R/W1TS | 0h    | Oneshot sync bit<br>0:Writing a '0' has no effect.<br>1:Allow one sync pulse to propagate.                                                                                                                                                                                                                                                                                       |
| 6     | OSHTSYNCMODE    | R/W    | 0h    | Oneshot sync enable bit<br>0:Oneshot sync mode disabled<br>1:Oneshot sync mode enabled                                                                                                                                                                                                                                                                                           |
| 5     | SELFCLRTRE<br>M | R/W    | 0h    | Loop back sync pulse to enable self sync operation<br>0:Self clear function of TRREM disabled.<br>1:Self clear function of TRREM enabled                                                                                                                                                                                                                                         |
| 4:0   | RESERVED_1      | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                         |

### 3.7.2.3 EPWM\_EPWMSYNCINSEL Register

#### 1 EPWM\_EPWMSYNCINSEL Register (Offset = 6h) [reset = 1h]

EPWMxSYNCIN Source Select Register.

Return to [Summary Table](#)

**Table 3-820. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0006h       |
| EPWM0_G1      | 5004 0006h       |
| EPWM0_G2      | 5008 0006h       |
| EPWM0_G3      | 500C 0006h       |
| EPWM1_G0      | 5000 1006h       |
| EPWM1_G1      | 5004 1006h       |
| EPWM1_G2      | 5008 1006h       |
| EPWM1_G3      | 500C 1006h       |
| EPWM2_G0      | 5000 2006h       |
| EPWM2_G1      | 5004 2006h       |
| EPWM2_G2      | 5008 2006h       |
| EPWM2_G3      | 500C 2006h       |
| EPWM3_G0      | 5000 3006h       |
| EPWM3_G1      | 5004 3006h       |
| EPWM3_G2      | 5008 3006h       |
| EPWM3_G3      | 500C 3006h       |
| EPWM4_G0      | 5000 4006h       |
| EPWM4_G1      | 5004 4006h       |
| EPWM4_G2      | 5008 4006h       |
| EPWM4_G3      | 500C 4006h       |
| EPWM5_G0      | 5000 5006h       |
| EPWM5_G1      | 5004 5006h       |
| EPWM5_G2      | 5008 5006h       |
| EPWM5_G3      | 500C 5006h       |
| EPWM6_G0      | 5000 6006h       |
| EPWM6_G1      | 5004 6006h       |
| EPWM6_G2      | 5008 6006h       |
| EPWM6_G3      | 500C 6006h       |
| EPWM7_G0      | 5000 7006h       |
| EPWM7_G1      | 5004 7006h       |
| EPWM7_G2      | 5008 7006h       |
| EPWM7_G3      | 500C 7006h       |
| EPWM8_G0      | 5000 8006h       |
| EPWM8_G1      | 5004 8006h       |
| EPWM8_G2      | 5008 8006h       |
| EPWM8_G3      | 500C 8006h       |
| EPWM9_G0      | 5000 9006h       |
| EPWM9_G1      | 5004 9006h       |
| EPWM9_G2      | 5008 9006h       |

**Table 3-820. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9006h       |
| EPWM10_G0     | 5000 A006h       |
| EPWM10_G1     | 5004 A006h       |
| EPWM10_G2     | 5008 A006h       |
| EPWM10_G3     | 500C A006h       |
| EPWM11_G0     | 5000 B006h       |
| EPWM11_G1     | 5004 B006h       |
| EPWM11_G2     | 5008 B006h       |
| EPWM11_G3     | 500C B006h       |
| EPWM12_G0     | 5000 C006h       |
| EPWM12_G1     | 5004 C006h       |
| EPWM12_G2     | 5008 C006h       |
| EPWM12_G3     | 500C C006h       |
| EPWM13_G0     | 5000 D006h       |
| EPWM13_G1     | 5004 D006h       |
| EPWM13_G2     | 5008 D006h       |
| EPWM13_G3     | 500C D006h       |
| EPWM14_G0     | 5000 E006h       |
| EPWM14_G1     | 5004 E006h       |
| EPWM14_G2     | 5008 E006h       |
| EPWM14_G3     | 500C E006h       |
| EPWM15_G0     | 5000 F006h       |
| EPWM15_G1     | 5004 F006h       |
| EPWM15_G2     | 5008 F006h       |
| EPWM15_G3     | 500C F006h       |
| EPWM16_G0     | 5001 0006h       |
| EPWM16_G1     | 5005 0006h       |
| EPWM16_G2     | 5009 0006h       |
| EPWM16_G3     | 500D 0006h       |
| EPWM17_G0     | 5001 1006h       |
| EPWM17_G1     | 5005 1006h       |
| EPWM17_G2     | 5009 1006h       |
| EPWM17_G3     | 500D 1006h       |
| EPWM18_G0     | 5001 2006h       |
| EPWM18_G1     | 5005 2006h       |
| EPWM18_G2     | 5009 2006h       |
| EPWM18_G3     | 500D 2006h       |
| EPWM19_G0     | 5001 3006h       |
| EPWM19_G1     | 5005 3006h       |
| EPWM19_G2     | 5009 3006h       |
| EPWM19_G3     | 500D 3006h       |
| EPWM20_G0     | 5001 4006h       |
| EPWM20_G1     | 5005 4006h       |
| EPWM20_G2     | 5009 4006h       |
| EPWM20_G3     | 500D 4006h       |

**Table 3-820. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5006h       |
| EPWM21_G1     | 5005 5006h       |
| EPWM21_G2     | 5009 5006h       |
| EPWM21_G3     | 500D 5006h       |
| EPWM22_G0     | 5001 6006h       |
| EPWM22_G1     | 5005 6006h       |
| EPWM22_G2     | 5009 6006h       |
| EPWM22_G3     | 500D 6006h       |
| EPWM23_G0     | 5001 7006h       |
| EPWM23_G1     | 5005 7006h       |
| EPWM23_G2     | 5009 7006h       |
| EPWM23_G3     | 500D 7006h       |
| EPWM24_G0     | 5001 8006h       |
| EPWM24_G1     | 5005 8006h       |
| EPWM24_G2     | 5009 8006h       |
| EPWM24_G3     | 500D 8006h       |
| EPWM25_G0     | 5001 9006h       |
| EPWM25_G1     | 5005 9006h       |
| EPWM25_G2     | 5009 9006h       |
| EPWM25_G3     | 500D 9006h       |
| EPWM26_G0     | 5001 A006h       |
| EPWM26_G1     | 5005 A006h       |
| EPWM26_G2     | 5009 A006h       |
| EPWM26_G3     | 500D A006h       |
| EPWM27_G0     | 5001 B006h       |
| EPWM27_G1     | 5005 B006h       |
| EPWM27_G2     | 5009 B006h       |
| EPWM27_G3     | 500D B006h       |
| EPWM28_G0     | 5001 C006h       |
| EPWM28_G1     | 5005 C006h       |
| EPWM28_G2     | 5009 C006h       |
| EPWM28_G3     | 500D C006h       |
| EPWM29_G0     | 5001 D006h       |
| EPWM29_G1     | 5005 D006h       |
| EPWM29_G2     | 5009 D006h       |
| EPWM29_G3     | 500D D006h       |
| EPWM30_G0     | 5001 E006h       |
| EPWM30_G1     | 5005 E006h       |
| EPWM30_G2     | 5009 E006h       |
| EPWM30_G3     | 500D E006h       |
| EPWM31_G0     | 5001 F006h       |
| EPWM31_G1     | 5005 F006h       |
| EPWM31_G2     | 5009 F006h       |
| EPWM31_G3     | 500D F006h       |

**Figure 3-254. EPWM\_EPWMSYNCSINSEL Name Register**

|            |    |    |    |     |    |   |   |
|------------|----|----|----|-----|----|---|---|
| 15         | 14 | 13 | 12 | 11  | 10 | 9 | 8 |
| RESERVED_1 |    |    |    |     |    |   |   |
| R          |    |    |    |     |    |   |   |
| 0h         |    |    |    |     |    |   |   |
| 7          | 6  | 5  | 4  | 3   | 2  | 1 | 0 |
| RESERVED_1 |    |    |    | SEL |    |   |   |
| R          |    |    |    | R/W |    |   |   |
| 0h         |    |    |    | 1h  |    |   |   |

**Table 3-822. EPWM\_EPWMSYNCSINSEL Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:7 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 6:0  | SEL        | R/W  | 1h    | <p>These bits determine the source of the EPWMxSYNCSIN signal</p> <p>0x0: Disabled</p> <p>0x01: EPWM0.SYNCSIN</p> <p>...</p> <p>0x10: EPWM15.SYNCSIN</p> <p>0x11: EPWM16.SYNCSIN</p> <p>...</p> <p>0x20: EPWM31.SYNCSIN</p> <p>0x21: Reserved</p> <p>...</p> <p>0x40: ECAP0.SYNCSIN</p> <p>...</p> <p>0x49: ECAP9.SYNCSIN</p> <p>0x4A: Reserved</p> <p>...</p> <p>0x4F: Reserved</p> <p>0x50: InputXBAR.Out[4]</p> <p>0x51: InputXBAR.Out[20]</p> <p>0x52: Reserved</p> <p>...</p> <p>0x57: Reserved</p> <p>0x58: SOC_TIMESYNC_XBAR0.SYNCPWMOut0</p> <p>0x59: SOC_TIMESYNC_XBAR0.SYNCPWMOut1</p> <p>0x5A: Reserved</p> <p>0x5F: Reserved</p> <p>0x60: FSIRX0.RXTRIG[0]</p> <p>0x61: FSIRX0.RXTRIG[1]</p> <p>0x62: FSIRX0.RXTRIG[2]</p> <p>0x63: FSIRX0.RXTRIG[3]</p> <p>0x64: FSIRX1.RXTRIG[0]</p> <p>0x65: FSIRX1.RXTRIG[1]</p> <p>0x66: FSIRX1.RXTRIG[2]</p> <p>0x67: FSIRX1.RXTRIG[3]</p> <p>0x68: FSIRX2.RXTRIG[0]</p> <p>0x69: FSIRX2.RXTRIG[1]</p> <p>0x6A: FSIRX2.RXTRIG[2]</p> <p>0x6B: FSIRX2.RXTRIG[3]</p> <p>0x6C: FSIRX3.RXTRIG[0]</p> <p>0x6D: FSIRX3.RXTRIG[1]</p> <p>0x6E: FSIRX3.RXTRIG[2]</p> <p>0x6F: FSIRX3.RXTRIG[3]</p> <p>0x70: Reserved</p> <p>...</p> <p>0x7F: Reserved</p> |

### 3.7.2.4 EPWM\_TBCTR Register

#### 1 EPWM\_TBCTR Register (Offset = 8h) [reset = 0h]

Time Base Counter Register.

Return to [Summary Table](#)

**Table 3-823. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0008h       |
| EPWM0_G1      | 5004 0008h       |
| EPWM0_G2      | 5008 0008h       |
| EPWM0_G3      | 500C 0008h       |
| EPWM1_G0      | 5000 1008h       |
| EPWM1_G1      | 5004 1008h       |
| EPWM1_G2      | 5008 1008h       |
| EPWM1_G3      | 500C 1008h       |
| EPWM2_G0      | 5000 2008h       |
| EPWM2_G1      | 5004 2008h       |
| EPWM2_G2      | 5008 2008h       |
| EPWM2_G3      | 500C 2008h       |
| EPWM3_G0      | 5000 3008h       |
| EPWM3_G1      | 5004 3008h       |
| EPWM3_G2      | 5008 3008h       |
| EPWM3_G3      | 500C 3008h       |
| EPWM4_G0      | 5000 4008h       |
| EPWM4_G1      | 5004 4008h       |
| EPWM4_G2      | 5008 4008h       |
| EPWM4_G3      | 500C 4008h       |
| EPWM5_G0      | 5000 5008h       |
| EPWM5_G1      | 5004 5008h       |
| EPWM5_G2      | 5008 5008h       |
| EPWM5_G3      | 500C 5008h       |
| EPWM6_G0      | 5000 6008h       |
| EPWM6_G1      | 5004 6008h       |
| EPWM6_G2      | 5008 6008h       |
| EPWM6_G3      | 500C 6008h       |
| EPWM7_G0      | 5000 7008h       |
| EPWM7_G1      | 5004 7008h       |
| EPWM7_G2      | 5008 7008h       |
| EPWM7_G3      | 500C 7008h       |
| EPWM8_G0      | 5000 8008h       |
| EPWM8_G1      | 5004 8008h       |
| EPWM8_G2      | 5008 8008h       |
| EPWM8_G3      | 500C 8008h       |
| EPWM9_G0      | 5000 9008h       |
| EPWM9_G1      | 5004 9008h       |
| EPWM9_G2      | 5008 9008h       |

**Table 3-823. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9008h       |
| EPWM10_G0     | 5000 A008h       |
| EPWM10_G1     | 5004 A008h       |
| EPWM10_G2     | 5008 A008h       |
| EPWM10_G3     | 500C A008h       |
| EPWM11_G0     | 5000 B008h       |
| EPWM11_G1     | 5004 B008h       |
| EPWM11_G2     | 5008 B008h       |
| EPWM11_G3     | 500C B008h       |
| EPWM12_G0     | 5000 C008h       |
| EPWM12_G1     | 5004 C008h       |
| EPWM12_G2     | 5008 C008h       |
| EPWM12_G3     | 500C C008h       |
| EPWM13_G0     | 5000 D008h       |
| EPWM13_G1     | 5004 D008h       |
| EPWM13_G2     | 5008 D008h       |
| EPWM13_G3     | 500C D008h       |
| EPWM14_G0     | 5000 E008h       |
| EPWM14_G1     | 5004 E008h       |
| EPWM14_G2     | 5008 E008h       |
| EPWM14_G3     | 500C E008h       |
| EPWM15_G0     | 5000 F008h       |
| EPWM15_G1     | 5004 F008h       |
| EPWM15_G2     | 5008 F008h       |
| EPWM15_G3     | 500C F008h       |
| EPWM16_G0     | 5001 0008h       |
| EPWM16_G1     | 5005 0008h       |
| EPWM16_G2     | 5009 0008h       |
| EPWM16_G3     | 500D 0008h       |
| EPWM17_G0     | 5001 1008h       |
| EPWM17_G1     | 5005 1008h       |
| EPWM17_G2     | 5009 1008h       |
| EPWM17_G3     | 500D 1008h       |
| EPWM18_G0     | 5001 2008h       |
| EPWM18_G1     | 5005 2008h       |
| EPWM18_G2     | 5009 2008h       |
| EPWM18_G3     | 500D 2008h       |
| EPWM19_G0     | 5001 3008h       |
| EPWM19_G1     | 5005 3008h       |
| EPWM19_G2     | 5009 3008h       |
| EPWM19_G3     | 500D 3008h       |
| EPWM20_G0     | 5001 4008h       |
| EPWM20_G1     | 5005 4008h       |
| EPWM20_G2     | 5009 4008h       |
| EPWM20_G3     | 500D 4008h       |

**Table 3-823. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5008h       |
| EPWM21_G1     | 5005 5008h       |
| EPWM21_G2     | 5009 5008h       |
| EPWM21_G3     | 500D 5008h       |
| EPWM22_G0     | 5001 6008h       |
| EPWM22_G1     | 5005 6008h       |
| EPWM22_G2     | 5009 6008h       |
| EPWM22_G3     | 500D 6008h       |
| EPWM23_G0     | 5001 7008h       |
| EPWM23_G1     | 5005 7008h       |
| EPWM23_G2     | 5009 7008h       |
| EPWM23_G3     | 500D 7008h       |
| EPWM24_G0     | 5001 8008h       |
| EPWM24_G1     | 5005 8008h       |
| EPWM24_G2     | 5009 8008h       |
| EPWM24_G3     | 500D 8008h       |
| EPWM25_G0     | 5001 9008h       |
| EPWM25_G1     | 5005 9008h       |
| EPWM25_G2     | 5009 9008h       |
| EPWM25_G3     | 500D 9008h       |
| EPWM26_G0     | 5001 A008h       |
| EPWM26_G1     | 5005 A008h       |
| EPWM26_G2     | 5009 A008h       |
| EPWM26_G3     | 500D A008h       |
| EPWM27_G0     | 5001 B008h       |
| EPWM27_G1     | 5005 B008h       |
| EPWM27_G2     | 5009 B008h       |
| EPWM27_G3     | 500D B008h       |
| EPWM28_G0     | 5001 C008h       |
| EPWM28_G1     | 5005 C008h       |
| EPWM28_G2     | 5009 C008h       |
| EPWM28_G3     | 500D C008h       |
| EPWM29_G0     | 5001 D008h       |
| EPWM29_G1     | 5005 D008h       |
| EPWM29_G2     | 5009 D008h       |
| EPWM29_G3     | 500D D008h       |
| EPWM30_G0     | 5001 E008h       |
| EPWM30_G1     | 5005 E008h       |
| EPWM30_G2     | 5009 E008h       |
| EPWM30_G3     | 500D E008h       |
| EPWM31_G0     | 5001 F008h       |
| EPWM31_G1     | 5005 F008h       |
| EPWM31_G2     | 5009 F008h       |
| EPWM31_G3     | 500D F008h       |



**Figure 3-255. EPWM\_TBCTR Name Register**

|       |    |    |    |    |    |   |   |
|-------|----|----|----|----|----|---|---|
| 15    | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TBCTR |    |    |    |    |    |   |   |
| R/W   |    |    |    |    |    |   |   |
| 0h    |    |    |    |    |    |   |   |
| 7     | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| TBCTR |    |    |    |    |    |   |   |
| R/W   |    |    |    |    |    |   |   |
| 0h    |    |    |    |    |    |   |   |

**Table 3-825. EPWM\_TBCTR Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                |
|------|-------|------|-------|----------------------------|
| 15:0 | TBCTR | R/W  | 0h    | Time Base Counter Register |

### 3.7.2.5 EPWM\_TBSTS Register

#### 1 EPWM\_TBSTS Register (Offset = Ah) [reset = 1h]

Time Base Status Register.

Return to [Summary Table](#)

**Table 3-826. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 000Ah       |
| EPWM0_G1      | 5004 000Ah       |
| EPWM0_G2      | 5008 000Ah       |
| EPWM0_G3      | 500C 000Ah       |
| EPWM1_G0      | 5000 100Ah       |
| EPWM1_G1      | 5004 100Ah       |
| EPWM1_G2      | 5008 100Ah       |
| EPWM1_G3      | 500C 100Ah       |
| EPWM2_G0      | 5000 200Ah       |
| EPWM2_G1      | 5004 200Ah       |
| EPWM2_G2      | 5008 200Ah       |
| EPWM2_G3      | 500C 200Ah       |
| EPWM3_G0      | 5000 300Ah       |
| EPWM3_G1      | 5004 300Ah       |
| EPWM3_G2      | 5008 300Ah       |
| EPWM3_G3      | 500C 300Ah       |
| EPWM4_G0      | 5000 400Ah       |
| EPWM4_G1      | 5004 400Ah       |
| EPWM4_G2      | 5008 400Ah       |
| EPWM4_G3      | 500C 400Ah       |
| EPWM5_G0      | 5000 500Ah       |
| EPWM5_G1      | 5004 500Ah       |
| EPWM5_G2      | 5008 500Ah       |
| EPWM5_G3      | 500C 500Ah       |
| EPWM6_G0      | 5000 600Ah       |
| EPWM6_G1      | 5004 600Ah       |
| EPWM6_G2      | 5008 600Ah       |
| EPWM6_G3      | 500C 600Ah       |
| EPWM7_G0      | 5000 700Ah       |
| EPWM7_G1      | 5004 700Ah       |
| EPWM7_G2      | 5008 700Ah       |
| EPWM7_G3      | 500C 700Ah       |
| EPWM8_G0      | 5000 800Ah       |
| EPWM8_G1      | 5004 800Ah       |
| EPWM8_G2      | 5008 800Ah       |
| EPWM8_G3      | 500C 800Ah       |
| EPWM9_G0      | 5000 900Ah       |
| EPWM9_G1      | 5004 900Ah       |
| EPWM9_G2      | 5008 900Ah       |

**Table 3-826. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 900Ah       |
| EPWM10_G0     | 5000 A00Ah       |
| EPWM10_G1     | 5004 A00Ah       |
| EPWM10_G2     | 5008 A00Ah       |
| EPWM10_G3     | 500C A00Ah       |
| EPWM11_G0     | 5000 B00Ah       |
| EPWM11_G1     | 5004 B00Ah       |
| EPWM11_G2     | 5008 B00Ah       |
| EPWM11_G3     | 500C B00Ah       |
| EPWM12_G0     | 5000 C00Ah       |
| EPWM12_G1     | 5004 C00Ah       |
| EPWM12_G2     | 5008 C00Ah       |
| EPWM12_G3     | 500C C00Ah       |
| EPWM13_G0     | 5000 D00Ah       |
| EPWM13_G1     | 5004 D00Ah       |
| EPWM13_G2     | 5008 D00Ah       |
| EPWM13_G3     | 500C D00Ah       |
| EPWM14_G0     | 5000 E00Ah       |
| EPWM14_G1     | 5004 E00Ah       |
| EPWM14_G2     | 5008 E00Ah       |
| EPWM14_G3     | 500C E00Ah       |
| EPWM15_G0     | 5000 F00Ah       |
| EPWM15_G1     | 5004 F00Ah       |
| EPWM15_G2     | 5008 F00Ah       |
| EPWM15_G3     | 500C F00Ah       |
| EPWM16_G0     | 5001 000Ah       |
| EPWM16_G1     | 5005 000Ah       |
| EPWM16_G2     | 5009 000Ah       |
| EPWM16_G3     | 500D 000Ah       |
| EPWM17_G0     | 5001 100Ah       |
| EPWM17_G1     | 5005 100Ah       |
| EPWM17_G2     | 5009 100Ah       |
| EPWM17_G3     | 500D 100Ah       |
| EPWM18_G0     | 5001 200Ah       |
| EPWM18_G1     | 5005 200Ah       |
| EPWM18_G2     | 5009 200Ah       |
| EPWM18_G3     | 500D 200Ah       |
| EPWM19_G0     | 5001 300Ah       |
| EPWM19_G1     | 5005 300Ah       |
| EPWM19_G2     | 5009 300Ah       |
| EPWM19_G3     | 500D 300Ah       |
| EPWM20_G0     | 5001 400Ah       |
| EPWM20_G1     | 5005 400Ah       |
| EPWM20_G2     | 5009 400Ah       |
| EPWM20_G3     | 500D 400Ah       |

**Table 3-826. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 500Ah       |
| EPWM21_G1     | 5005 500Ah       |
| EPWM21_G2     | 5009 500Ah       |
| EPWM21_G3     | 500D 500Ah       |
| EPWM22_G0     | 5001 600Ah       |
| EPWM22_G1     | 5005 600Ah       |
| EPWM22_G2     | 5009 600Ah       |
| EPWM22_G3     | 500D 600Ah       |
| EPWM23_G0     | 5001 700Ah       |
| EPWM23_G1     | 5005 700Ah       |
| EPWM23_G2     | 5009 700Ah       |
| EPWM23_G3     | 500D 700Ah       |
| EPWM24_G0     | 5001 800Ah       |
| EPWM24_G1     | 5005 800Ah       |
| EPWM24_G2     | 5009 800Ah       |
| EPWM24_G3     | 500D 800Ah       |
| EPWM25_G0     | 5001 900Ah       |
| EPWM25_G1     | 5005 900Ah       |
| EPWM25_G2     | 5009 900Ah       |
| EPWM25_G3     | 500D 900Ah       |
| EPWM26_G0     | 5001 A00Ah       |
| EPWM26_G1     | 5005 A00Ah       |
| EPWM26_G2     | 5009 A00Ah       |
| EPWM26_G3     | 500D A00Ah       |
| EPWM27_G0     | 5001 B00Ah       |
| EPWM27_G1     | 5005 B00Ah       |
| EPWM27_G2     | 5009 B00Ah       |
| EPWM27_G3     | 500D B00Ah       |
| EPWM28_G0     | 5001 C00Ah       |
| EPWM28_G1     | 5005 C00Ah       |
| EPWM28_G2     | 5009 C00Ah       |
| EPWM28_G3     | 500D C00Ah       |
| EPWM29_G0     | 5001 D00Ah       |
| EPWM29_G1     | 5005 D00Ah       |
| EPWM29_G2     | 5009 D00Ah       |
| EPWM29_G3     | 500D D00Ah       |
| EPWM30_G0     | 5001 E00Ah       |
| EPWM30_G1     | 5005 E00Ah       |
| EPWM30_G2     | 5009 E00Ah       |
| EPWM30_G3     | 500D E00Ah       |
| EPWM31_G0     | 5001 F00Ah       |
| EPWM31_G1     | 5005 F00Ah       |
| EPWM31_G2     | 5009 F00Ah       |
| EPWM31_G3     | 500D F00Ah       |

**Figure 3-256. EPWM\_TBSTS Name Register**

|            |    |    |    |        |        |        |   |
|------------|----|----|----|--------|--------|--------|---|
| 15         | 14 | 13 | 12 | 11     | 10     | 9      | 8 |
| RESERVED_1 |    |    |    |        |        |        |   |
| R          |    |    |    |        |        |        |   |
| 0h         |    |    |    |        |        |        |   |
| 7          | 6  | 5  | 4  | 3      | 2      | 1      | 0 |
| RESERVED_1 |    |    |    | CTRMX  | SYNCl  | CTDRlR |   |
| R          |    |    |    | R/W1TC | R/W1TC | R      |   |
| 0h         |    |    |    | 0h     | 0h     | 1h     |   |

**Table 3-828. EPWM\_TBSTS Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                                                                         |
|------|------------|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:3 | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                            |
| 2    | CTRMX      | R/W1TC | 0h    | Time-Base Counter Max Latched Status Bit<br>0:Reading a 0 indicates the time-base counter never reached its maximum value. Writing a 0 will have no effect.<br>1:Reading a 1 on this bit indicates that the time-base counter reached the max value 0xFFFF. Writing a 1 to this bit will clear the latched event.   |
| 1    | SYNCl      | R/W1TC | 0h    | Input Synchronization Latched Status Bit<br>0:Writing a 0 will have no effect. Reading a 0 indicates no external synchronization event has occurred.<br>1:Reading a 1 on this bit indicates that an external synchronization event has occurred [EPWMxSYNCl]. Writing a 1 to this bit will clear the latched event. |
| 0    | CTDRlR     | R      | 1h    | Time Base Counter Direction Status Bit<br>0:Time-Base Counter is currently counting down.<br>1:Time-Base Counter is currently counting up.<br>Note: This bit is only valid when the counter is not frozen.                                                                                                          |

### 3.7.2.6 EPWM\_EPWMSYNCOUEN Register

#### 1 EPWM\_EPWMSYNCOUEN Register (Offset = Ch) [reset = 1h]

EPWMxSYNCOUEN Source Enable Register.

Return to [Summary Table](#)

**Table 3-829. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 000Ch       |
| EPWM0_G1      | 5004 000Ch       |
| EPWM0_G2      | 5008 000Ch       |
| EPWM0_G3      | 500C 000Ch       |
| EPWM1_G0      | 5000 100Ch       |
| EPWM1_G1      | 5004 100Ch       |
| EPWM1_G2      | 5008 100Ch       |
| EPWM1_G3      | 500C 100Ch       |
| EPWM2_G0      | 5000 200Ch       |
| EPWM2_G1      | 5004 200Ch       |
| EPWM2_G2      | 5008 200Ch       |
| EPWM2_G3      | 500C 200Ch       |
| EPWM3_G0      | 5000 300Ch       |
| EPWM3_G1      | 5004 300Ch       |
| EPWM3_G2      | 5008 300Ch       |
| EPWM3_G3      | 500C 300Ch       |
| EPWM4_G0      | 5000 400Ch       |
| EPWM4_G1      | 5004 400Ch       |
| EPWM4_G2      | 5008 400Ch       |
| EPWM4_G3      | 500C 400Ch       |
| EPWM5_G0      | 5000 500Ch       |
| EPWM5_G1      | 5004 500Ch       |
| EPWM5_G2      | 5008 500Ch       |
| EPWM5_G3      | 500C 500Ch       |
| EPWM6_G0      | 5000 600Ch       |
| EPWM6_G1      | 5004 600Ch       |
| EPWM6_G2      | 5008 600Ch       |
| EPWM6_G3      | 500C 600Ch       |
| EPWM7_G0      | 5000 700Ch       |
| EPWM7_G1      | 5004 700Ch       |
| EPWM7_G2      | 5008 700Ch       |
| EPWM7_G3      | 500C 700Ch       |
| EPWM8_G0      | 5000 800Ch       |
| EPWM8_G1      | 5004 800Ch       |
| EPWM8_G2      | 5008 800Ch       |
| EPWM8_G3      | 500C 800Ch       |
| EPWM9_G0      | 5000 900Ch       |
| EPWM9_G1      | 5004 900Ch       |
| EPWM9_G2      | 5008 900Ch       |

**Table 3-829. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 900Ch       |
| EPWM10_G0     | 5000 A00Ch       |
| EPWM10_G1     | 5004 A00Ch       |
| EPWM10_G2     | 5008 A00Ch       |
| EPWM10_G3     | 500C A00Ch       |
| EPWM11_G0     | 5000 B00Ch       |
| EPWM11_G1     | 5004 B00Ch       |
| EPWM11_G2     | 5008 B00Ch       |
| EPWM11_G3     | 500C B00Ch       |
| EPWM12_G0     | 5000 C00Ch       |
| EPWM12_G1     | 5004 C00Ch       |
| EPWM12_G2     | 5008 C00Ch       |
| EPWM12_G3     | 500C C00Ch       |
| EPWM13_G0     | 5000 D00Ch       |
| EPWM13_G1     | 5004 D00Ch       |
| EPWM13_G2     | 5008 D00Ch       |
| EPWM13_G3     | 500C D00Ch       |
| EPWM14_G0     | 5000 E00Ch       |
| EPWM14_G1     | 5004 E00Ch       |
| EPWM14_G2     | 5008 E00Ch       |
| EPWM14_G3     | 500C E00Ch       |
| EPWM15_G0     | 5000 F00Ch       |
| EPWM15_G1     | 5004 F00Ch       |
| EPWM15_G2     | 5008 F00Ch       |
| EPWM15_G3     | 500C F00Ch       |
| EPWM16_G0     | 5001 000Ch       |
| EPWM16_G1     | 5005 000Ch       |
| EPWM16_G2     | 5009 000Ch       |
| EPWM16_G3     | 500D 000Ch       |
| EPWM17_G0     | 5001 100Ch       |
| EPWM17_G1     | 5005 100Ch       |
| EPWM17_G2     | 5009 100Ch       |
| EPWM17_G3     | 500D 100Ch       |
| EPWM18_G0     | 5001 200Ch       |
| EPWM18_G1     | 5005 200Ch       |
| EPWM18_G2     | 5009 200Ch       |
| EPWM18_G3     | 500D 200Ch       |
| EPWM19_G0     | 5001 300Ch       |
| EPWM19_G1     | 5005 300Ch       |
| EPWM19_G2     | 5009 300Ch       |
| EPWM19_G3     | 500D 300Ch       |
| EPWM20_G0     | 5001 400Ch       |
| EPWM20_G1     | 5005 400Ch       |
| EPWM20_G2     | 5009 400Ch       |
| EPWM20_G3     | 500D 400Ch       |

**Table 3-829. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 500Ch       |
| EPWM21_G1     | 5005 500Ch       |
| EPWM21_G2     | 5009 500Ch       |
| EPWM21_G3     | 500D 500Ch       |
| EPWM22_G0     | 5001 600Ch       |
| EPWM22_G1     | 5005 600Ch       |
| EPWM22_G2     | 5009 600Ch       |
| EPWM22_G3     | 500D 600Ch       |
| EPWM23_G0     | 5001 700Ch       |
| EPWM23_G1     | 5005 700Ch       |
| EPWM23_G2     | 5009 700Ch       |
| EPWM23_G3     | 500D 700Ch       |
| EPWM24_G0     | 5001 800Ch       |
| EPWM24_G1     | 5005 800Ch       |
| EPWM24_G2     | 5009 800Ch       |
| EPWM24_G3     | 500D 800Ch       |
| EPWM25_G0     | 5001 900Ch       |
| EPWM25_G1     | 5005 900Ch       |
| EPWM25_G2     | 5009 900Ch       |
| EPWM25_G3     | 500D 900Ch       |
| EPWM26_G0     | 5001 A00Ch       |
| EPWM26_G1     | 5005 A00Ch       |
| EPWM26_G2     | 5009 A00Ch       |
| EPWM26_G3     | 500D A00Ch       |
| EPWM27_G0     | 5001 B00Ch       |
| EPWM27_G1     | 5005 B00Ch       |
| EPWM27_G2     | 5009 B00Ch       |
| EPWM27_G3     | 500D B00Ch       |
| EPWM28_G0     | 5001 C00Ch       |
| EPWM28_G1     | 5005 C00Ch       |
| EPWM28_G2     | 5009 C00Ch       |
| EPWM28_G3     | 500D C00Ch       |
| EPWM29_G0     | 5001 D00Ch       |
| EPWM29_G1     | 5005 D00Ch       |
| EPWM29_G2     | 5009 D00Ch       |
| EPWM29_G3     | 500D D00Ch       |
| EPWM30_G0     | 5001 E00Ch       |
| EPWM30_G1     | 5005 E00Ch       |
| EPWM30_G2     | 5009 E00Ch       |
| EPWM30_G3     | 500D E00Ch       |
| EPWM31_G0     | 5001 F00Ch       |
| EPWM31_G1     | 5005 F00Ch       |
| EPWM31_G2     | 5009 F00Ch       |
| EPWM31_G3     | 500D F00Ch       |



**Figure 3-257. EPWM\_EPWMSYNCOUEN Name Register**

| 15         | 14        | 13        | 12     | 11     | 10     | 9      | 8    |
|------------|-----------|-----------|--------|--------|--------|--------|------|
| RESERVED_2 |           |           |        |        |        |        |      |
| R          |           |           |        |        |        |        |      |
| 0h         |           |           |        |        |        |        |      |
| 7          | 6         | 5         | 4      | 3      | 2      | 1      | 0    |
| RESERVED_1 | DCBEVT1EN | DCAEVT1EN | CMPDEN | CMPCEN | CMPBEN | ZEROEN | SWEN |
| R          | R/W       | R/W       | R/W    | R/W    | R/W    | R/W    | R/W  |
| 0h         | 0h        | 0h        | 0h     | 0h     | 0h     | 0h     | 1h   |

**Table 3-831. EPWM\_EPWMSYNCOUEN Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                |
|------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                   |
| 7    | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                   |
| 6    | DCBEVT1EN  | R/W  | 0h    | This bit enables the DCBEVT1.sync event to set the EPWMxSYNCO signal.<br>0 Disabled<br>1 The EPWMxSYNCO signal is pulsed for one PWM clock period upon a DCBEVT1.sync event                                                |
| 5    | DCAEVT1EN  | R/W  | 0h    | This bit enables the DCAEVT1.sync event to set the EPWMxSYNCOU signal.<br>0 Disabled<br>1 The EPWMxSYNCOU signal is pulsed for one PWM clock period upon a DCAEVT1.sync event                                              |
| 4    | CMPDEN     | R/W  | 0h    | This bit enables the TBCTR = CMPD event to set the EPWMxSYNCO signal.<br>0 Disabled<br>1 The EPWMxSYNCO signal is pulsed for one PWM clock period upon a time-base counter equal to counter compare D event [TBCTR = CMPD] |
| 3    | CMPCEN     | R/W  | 0h    | This bit enables the TBCTR = CMPC event to set the EPWMxSYNCO signal.<br>0 Disabled<br>1 The EPWMxSYNCO signal is pulsed for one PWM clock period upon a time-base counter equal to counter compare C event [TBCTR = CMPC] |
| 2    | CMPBEN     | R/W  | 0h    | This bit enables the TBCTR = CMPB event to set the EPWMxSYNCO signal.<br>0 Disabled<br>1 The EPWMxSYNCO signal is pulsed for one PWM clock period upon a time-base counter equal to counter compare B event [TBCTR = CMPB] |
| 1    | ZEROEN     | R/W  | 0h    | This bit enables the TBCTR = 0x0000 event to set the EPWMxSYNCOU signal.<br>0 Disabled<br>1 The EPWMxSYNCOU signal is pulsed for one PWM clock period upon the value of TBCTR changing to 0x0000                           |
| 0    | SWEN       | R/W  | 1h    | This bit enables the TBCTL.SWFSYNC bit to set the EPWMxSYNCO signal.<br>0 Disabled<br>1 The EPWMxSYNCO signal is pulsed for one PWM clock period when the TBCTL.SWFSYNC bit is set                                         |

### 3.7.2.7 EPWM\_TBCTL3 Register

#### 1 EPWM\_TBCTL3 Register (Offset = Eh) [reset = 0h]

Time Base Control Register 3

Return to [Summary Table](#)

**Table 3-832. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 000Eh       |
| EPWM0_G1      | 5004 000Eh       |
| EPWM0_G2      | 5008 000Eh       |
| EPWM0_G3      | 500C 000Eh       |
| EPWM1_G0      | 5000 100Eh       |
| EPWM1_G1      | 5004 100Eh       |
| EPWM1_G2      | 5008 100Eh       |
| EPWM1_G3      | 500C 100Eh       |
| EPWM2_G0      | 5000 200Eh       |
| EPWM2_G1      | 5004 200Eh       |
| EPWM2_G2      | 5008 200Eh       |
| EPWM2_G3      | 500C 200Eh       |
| EPWM3_G0      | 5000 300Eh       |
| EPWM3_G1      | 5004 300Eh       |
| EPWM3_G2      | 5008 300Eh       |
| EPWM3_G3      | 500C 300Eh       |
| EPWM4_G0      | 5000 400Eh       |
| EPWM4_G1      | 5004 400Eh       |
| EPWM4_G2      | 5008 400Eh       |
| EPWM4_G3      | 500C 400Eh       |
| EPWM5_G0      | 5000 500Eh       |
| EPWM5_G1      | 5004 500Eh       |
| EPWM5_G2      | 5008 500Eh       |
| EPWM5_G3      | 500C 500Eh       |
| EPWM6_G0      | 5000 600Eh       |
| EPWM6_G1      | 5004 600Eh       |
| EPWM6_G2      | 5008 600Eh       |
| EPWM6_G3      | 500C 600Eh       |
| EPWM7_G0      | 5000 700Eh       |
| EPWM7_G1      | 5004 700Eh       |
| EPWM7_G2      | 5008 700Eh       |
| EPWM7_G3      | 500C 700Eh       |
| EPWM8_G0      | 5000 800Eh       |
| EPWM8_G1      | 5004 800Eh       |
| EPWM8_G2      | 5008 800Eh       |
| EPWM8_G3      | 500C 800Eh       |
| EPWM9_G0      | 5000 900Eh       |
| EPWM9_G1      | 5004 900Eh       |
| EPWM9_G2      | 5008 900Eh       |

**Table 3-832. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 900Eh       |
| EPWM10_G0     | 5000 A00Eh       |
| EPWM10_G1     | 5004 A00Eh       |
| EPWM10_G2     | 5008 A00Eh       |
| EPWM10_G3     | 500C A00Eh       |
| EPWM11_G0     | 5000 B00Eh       |
| EPWM11_G1     | 5004 B00Eh       |
| EPWM11_G2     | 5008 B00Eh       |
| EPWM11_G3     | 500C B00Eh       |
| EPWM12_G0     | 5000 C00Eh       |
| EPWM12_G1     | 5004 C00Eh       |
| EPWM12_G2     | 5008 C00Eh       |
| EPWM12_G3     | 500C C00Eh       |
| EPWM13_G0     | 5000 D00Eh       |
| EPWM13_G1     | 5004 D00Eh       |
| EPWM13_G2     | 5008 D00Eh       |
| EPWM13_G3     | 500C D00Eh       |
| EPWM14_G0     | 5000 E00Eh       |
| EPWM14_G1     | 5004 E00Eh       |
| EPWM14_G2     | 5008 E00Eh       |
| EPWM14_G3     | 500C E00Eh       |
| EPWM15_G0     | 5000 F00Eh       |
| EPWM15_G1     | 5004 F00Eh       |
| EPWM15_G2     | 5008 F00Eh       |
| EPWM15_G3     | 500C F00Eh       |
| EPWM16_G0     | 5001 000Eh       |
| EPWM16_G1     | 5005 000Eh       |
| EPWM16_G2     | 5009 000Eh       |
| EPWM16_G3     | 500D 000Eh       |
| EPWM17_G0     | 5001 100Eh       |
| EPWM17_G1     | 5005 100Eh       |
| EPWM17_G2     | 5009 100Eh       |
| EPWM17_G3     | 500D 100Eh       |
| EPWM18_G0     | 5001 200Eh       |
| EPWM18_G1     | 5005 200Eh       |
| EPWM18_G2     | 5009 200Eh       |
| EPWM18_G3     | 500D 200Eh       |
| EPWM19_G0     | 5001 300Eh       |
| EPWM19_G1     | 5005 300Eh       |
| EPWM19_G2     | 5009 300Eh       |
| EPWM19_G3     | 500D 300Eh       |
| EPWM20_G0     | 5001 400Eh       |
| EPWM20_G1     | 5005 400Eh       |
| EPWM20_G2     | 5009 400Eh       |
| EPWM20_G3     | 500D 400Eh       |

**Table 3-832. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 500Eh       |
| EPWM21_G1     | 5005 500Eh       |
| EPWM21_G2     | 5009 500Eh       |
| EPWM21_G3     | 500D 500Eh       |
| EPWM22_G0     | 5001 600Eh       |
| EPWM22_G1     | 5005 600Eh       |
| EPWM22_G2     | 5009 600Eh       |
| EPWM22_G3     | 500D 600Eh       |
| EPWM23_G0     | 5001 700Eh       |
| EPWM23_G1     | 5005 700Eh       |
| EPWM23_G2     | 5009 700Eh       |
| EPWM23_G3     | 500D 700Eh       |
| EPWM24_G0     | 5001 800Eh       |
| EPWM24_G1     | 5005 800Eh       |
| EPWM24_G2     | 5009 800Eh       |
| EPWM24_G3     | 500D 800Eh       |
| EPWM25_G0     | 5001 900Eh       |
| EPWM25_G1     | 5005 900Eh       |
| EPWM25_G2     | 5009 900Eh       |
| EPWM25_G3     | 500D 900Eh       |
| EPWM26_G0     | 5001 A00Eh       |
| EPWM26_G1     | 5005 A00Eh       |
| EPWM26_G2     | 5009 A00Eh       |
| EPWM26_G3     | 500D A00Eh       |
| EPWM27_G0     | 5001 B00Eh       |
| EPWM27_G1     | 5005 B00Eh       |
| EPWM27_G2     | 5009 B00Eh       |
| EPWM27_G3     | 500D B00Eh       |
| EPWM28_G0     | 5001 C00Eh       |
| EPWM28_G1     | 5005 C00Eh       |
| EPWM28_G2     | 5009 C00Eh       |
| EPWM28_G3     | 500D C00Eh       |
| EPWM29_G0     | 5001 D00Eh       |
| EPWM29_G1     | 5005 D00Eh       |
| EPWM29_G2     | 5009 D00Eh       |
| EPWM29_G3     | 500D D00Eh       |
| EPWM30_G0     | 5001 E00Eh       |
| EPWM30_G1     | 5005 E00Eh       |
| EPWM30_G2     | 5009 E00Eh       |
| EPWM30_G3     | 500D E00Eh       |
| EPWM31_G0     | 5001 F00Eh       |
| EPWM31_G1     | 5005 F00Eh       |
| EPWM31_G2     | 5009 F00Eh       |
| EPWM31_G3     | 500D F00Eh       |

**Figure 3-258. EPWM\_TBCTL3 Name Register**

|            |    |    |    |    |    |   |          |
|------------|----|----|----|----|----|---|----------|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8        |
| RESERVED_1 |    |    |    |    |    |   |          |
| R          |    |    |    |    |    |   |          |
| 0h         |    |    |    |    |    |   |          |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0        |
| RESERVED_1 |    |    |    |    |    |   | OSSFRGEN |
| R          |    |    |    |    |    |   | R/W      |
| 0h         |    |    |    |    |    |   | 0h       |

**Table 3-834. EPWM\_TBCTL3 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                   |
|------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:1 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                      |
| 0    | OSSFRGEN   | R/W  | 0h    | This bit determines which bit sets the EPWMxSYNCOU One Shot Latch.<br>0 TBCTL2[OSHTSYNC] sets the One Shot Latch<br>1 GLDCTL2[OSHTLD] sets the One Shot Latch |

### 3.7.2.8 EPWM\_CMPCTL Register

#### 1 EPWM\_CMPCTL Register (Offset = 10h) [reset = 0h]

Counter Compare Control Register.

Return to [Summary Table](#)

**Table 3-835. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0010h       |
| EPWM0_G1      | 5004 0010h       |
| EPWM0_G2      | 5008 0010h       |
| EPWM0_G3      | 500C 0010h       |
| EPWM1_G0      | 5000 1010h       |
| EPWM1_G1      | 5004 1010h       |
| EPWM1_G2      | 5008 1010h       |
| EPWM1_G3      | 500C 1010h       |
| EPWM2_G0      | 5000 2010h       |
| EPWM2_G1      | 5004 2010h       |
| EPWM2_G2      | 5008 2010h       |
| EPWM2_G3      | 500C 2010h       |
| EPWM3_G0      | 5000 3010h       |
| EPWM3_G1      | 5004 3010h       |
| EPWM3_G2      | 5008 3010h       |
| EPWM3_G3      | 500C 3010h       |
| EPWM4_G0      | 5000 4010h       |
| EPWM4_G1      | 5004 4010h       |
| EPWM4_G2      | 5008 4010h       |
| EPWM4_G3      | 500C 4010h       |
| EPWM5_G0      | 5000 5010h       |
| EPWM5_G1      | 5004 5010h       |
| EPWM5_G2      | 5008 5010h       |
| EPWM5_G3      | 500C 5010h       |
| EPWM6_G0      | 5000 6010h       |
| EPWM6_G1      | 5004 6010h       |
| EPWM6_G2      | 5008 6010h       |
| EPWM6_G3      | 500C 6010h       |
| EPWM7_G0      | 5000 7010h       |
| EPWM7_G1      | 5004 7010h       |
| EPWM7_G2      | 5008 7010h       |
| EPWM7_G3      | 500C 7010h       |
| EPWM8_G0      | 5000 8010h       |
| EPWM8_G1      | 5004 8010h       |
| EPWM8_G2      | 5008 8010h       |
| EPWM8_G3      | 500C 8010h       |
| EPWM9_G0      | 5000 9010h       |
| EPWM9_G1      | 5004 9010h       |
| EPWM9_G2      | 5008 9010h       |

**Table 3-835. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9010h       |
| EPWM10_G0     | 5000 A010h       |
| EPWM10_G1     | 5004 A010h       |
| EPWM10_G2     | 5008 A010h       |
| EPWM10_G3     | 500C A010h       |
| EPWM11_G0     | 5000 B010h       |
| EPWM11_G1     | 5004 B010h       |
| EPWM11_G2     | 5008 B010h       |
| EPWM11_G3     | 500C B010h       |
| EPWM12_G0     | 5000 C010h       |
| EPWM12_G1     | 5004 C010h       |
| EPWM12_G2     | 5008 C010h       |
| EPWM12_G3     | 500C C010h       |
| EPWM13_G0     | 5000 D010h       |
| EPWM13_G1     | 5004 D010h       |
| EPWM13_G2     | 5008 D010h       |
| EPWM13_G3     | 500C D010h       |
| EPWM14_G0     | 5000 E010h       |
| EPWM14_G1     | 5004 E010h       |
| EPWM14_G2     | 5008 E010h       |
| EPWM14_G3     | 500C E010h       |
| EPWM15_G0     | 5000 F010h       |
| EPWM15_G1     | 5004 F010h       |
| EPWM15_G2     | 5008 F010h       |
| EPWM15_G3     | 500C F010h       |
| EPWM16_G0     | 5001 0010h       |
| EPWM16_G1     | 5005 0010h       |
| EPWM16_G2     | 5009 0010h       |
| EPWM16_G3     | 500D 0010h       |
| EPWM17_G0     | 5001 1010h       |
| EPWM17_G1     | 5005 1010h       |
| EPWM17_G2     | 5009 1010h       |
| EPWM17_G3     | 500D 1010h       |
| EPWM18_G0     | 5001 2010h       |
| EPWM18_G1     | 5005 2010h       |
| EPWM18_G2     | 5009 2010h       |
| EPWM18_G3     | 500D 2010h       |
| EPWM19_G0     | 5001 3010h       |
| EPWM19_G1     | 5005 3010h       |
| EPWM19_G2     | 5009 3010h       |
| EPWM19_G3     | 500D 3010h       |
| EPWM20_G0     | 5001 4010h       |
| EPWM20_G1     | 5005 4010h       |
| EPWM20_G2     | 5009 4010h       |
| EPWM20_G3     | 500D 4010h       |

**Table 3-835. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5010h       |
| EPWM21_G1     | 5005 5010h       |
| EPWM21_G2     | 5009 5010h       |
| EPWM21_G3     | 500D 5010h       |
| EPWM22_G0     | 5001 6010h       |
| EPWM22_G1     | 5005 6010h       |
| EPWM22_G2     | 5009 6010h       |
| EPWM22_G3     | 500D 6010h       |
| EPWM23_G0     | 5001 7010h       |
| EPWM23_G1     | 5005 7010h       |
| EPWM23_G2     | 5009 7010h       |
| EPWM23_G3     | 500D 7010h       |
| EPWM24_G0     | 5001 8010h       |
| EPWM24_G1     | 5005 8010h       |
| EPWM24_G2     | 5009 8010h       |
| EPWM24_G3     | 500D 8010h       |
| EPWM25_G0     | 5001 9010h       |
| EPWM25_G1     | 5005 9010h       |
| EPWM25_G2     | 5009 9010h       |
| EPWM25_G3     | 500D 9010h       |
| EPWM26_G0     | 5001 A010h       |
| EPWM26_G1     | 5005 A010h       |
| EPWM26_G2     | 5009 A010h       |
| EPWM26_G3     | 500D A010h       |
| EPWM27_G0     | 5001 B010h       |
| EPWM27_G1     | 5005 B010h       |
| EPWM27_G2     | 5009 B010h       |
| EPWM27_G3     | 500D B010h       |
| EPWM28_G0     | 5001 C010h       |
| EPWM28_G1     | 5005 C010h       |
| EPWM28_G2     | 5009 C010h       |
| EPWM28_G3     | 500D C010h       |
| EPWM29_G0     | 5001 D010h       |
| EPWM29_G1     | 5005 D010h       |
| EPWM29_G2     | 5009 D010h       |
| EPWM29_G3     | 500D D010h       |
| EPWM30_G0     | 5001 E010h       |
| EPWM30_G1     | 5005 E010h       |
| EPWM30_G2     | 5009 E010h       |
| EPWM30_G3     | 500D E010h       |
| EPWM31_G0     | 5001 F010h       |
| EPWM31_G1     | 5005 F010h       |
| EPWM31_G2     | 5009 F010h       |
| EPWM31_G3     | 500D F010h       |



**Figure 3-259. EPWM\_CMPCTL Name Register**

| 15         | 14         | 13         | 12        | 11        | 10 | 9         | 8         |
|------------|------------|------------|-----------|-----------|----|-----------|-----------|
| LINKDUTYHR | RESERVED_3 | LOADBSYNC  |           | LOADASYNC |    | SHDWBFULL | SHDWAFULL |
| R/W        | R          | R/W        |           | R/W       |    | R         | R         |
| 0h         | 0h         | 0h         |           | 0h        |    | 0h        | 0h        |
| 7          | 6          | 5          | 4         | 3         | 2  | 1         | 0         |
| RESERVED_2 | SHDWBMODE  | RESERVED_1 | SHDWAMODE | LOADBMODE |    | LOADAMODE |           |
| R          | R/W        | R          | R/W       | R/W       |    | R/W       |           |
| 0h         | 0h         | 0h         | 0h        | 0h        |    | 0h        |           |

**Table 3-837. EPWM\_CMPCTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | LINKDUTYHR | R/W  | 0h    | CMPAHR, CMPBHR Register Linking:<br>0 PWMA and PWMB outputs generated independently and CMPAHR, CMPBHR are independent values as on Type-4<br>1 When this bit is set CMPBHR assumes the same value as CMPAHR. This is typically used in complimentary PWM output generation<br>[Section 7 details of the operation]                                                                                                        |
| 14    | RESERVED_3 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 13:12 | LOADBSYNC  | R/W  | 0h    | Shadow to Active CMPB Register Load on SYNC event<br>00:Shadow to Active Load of CMPB:CMPBHR occurs according to LOADBMODE [bits 2'b10] [same as legacy]<br>01:Shadow to Active Load of CMPB:CMPBHR occurs both according to LOADBMODE bits and when SYNC occurs<br>10:Shadow to Active Load of CMPB:CMPBHR occurs only when a SYNC is received<br>11:Reserved<br>Note: This bit is valid only if CMPCTL[SHDWBMODE] = 0.   |
| 11:10 | LOADASYNC  | R/W  | 0h    | Shadow to Active CMPA Register Load on SYNC event<br>00:Shadow to Active Load of CMPA:CMPAHR occurs according to LOADAMODE [bits 2'b10] [same as legacy]<br>01:Shadow to Active Load of CMPA:CMPAHR occurs both according to LOADAMODE bits and when SYNC occurs<br>10:Shadow to Active Load of CMPA:CMPAHR occurs only when a SYNC is received<br>11:Reserved<br>Note: This bit is valid only if CMPCTL[SHDWAMODE] = 0.   |
| 9     | SHDWBFULL  | R    | 0h    | Counter-compare B [CMPB] Shadow Register Full Status Flag<br>This bit self clears once a loadstrobe occurs.<br>0: CMPB shadow FIFO not full yet<br>1: Indicates the CMPB shadow FIFO is full<br>a CPU write will overwrite current shadow value                                                                                                                                                                            |
| 8     | SHDWAFULL  | R    | 0h    | Counter-compare A [CMPA] Shadow Register Full Status Flag<br>The flag bit is set when a 32-bit write to CMPA:CMPAHR register or a 16-bit write to CMPA register is made. A 16-bit write to CMPAHR register will not effect the flag. This bit self clears once a load-strobe occurs.<br>0: CMPA shadow FIFO not full yet<br>1: Indicates the CMPA shadow FIFO is full, a CPU write will overwrite the current shadow value |
| 7     | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 6     | SHDWBMODE  | R/W  | 0h    | Counter-compare B [CMPB] Register Operating Mode<br>0: Shadow mode. Operates as a double buffer. All writes via the CPU access the shadow register<br>1: Immediate mode. Only the active compare B register is used. All writes and reads directly access the active register for immediate compare action                                                                                                                 |
| 5     | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                   |

**Table 3-837. EPWM\_CMPCTL Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                           |
|-----|-----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | SHDWAMODE | R/W  | 0h    | Counter-compare A [CMPA] Register Operating Mode<br>0:Shadow mode. Operates as a double buffer. All writes via the CPU access the shadow register<br>1:Immediate mode. Only the active compare register is used. All writes and reads directly access the active register for immediate compare action                                                                |
| 3:2 | LOADBMODE | R/W  | 0h    | Active Counter-Compare B [CMPB] Load From Shadow Select Mode<br>This bit has no effect in immediate mode [CMPCTL[SHDWBMODE] = 1].<br>00:Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000]<br>01:Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD]<br>10:Load on either CTR = Zero or CTR = PRD<br>11:Freeze [no loads possible] |
| 1:0 | LOADAMODE | R/W  | 0h    | Active Counter-Compare A [CMPA] Load From Shadow Select Mode<br>This bit has no effect in immediate mode [CMPCTL[SHDWAMODE] = 1].<br>00:Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000]<br>01:Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD]<br>10:Load on either CTR = Zero or CTR = PRD<br>11:Freeze [no loads possible] |

### 3.7.2.9 EPWM\_CMPCTL2 Register

#### 1 EPWM\_CMPCTL2 Register (Offset = 12h) [reset = 0h]

Counter Compare Control Register 2

Return to [Summary Table](#)

**Table 3-838. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0012h       |
| EPWM0_G1      | 5004 0012h       |
| EPWM0_G2      | 5008 0012h       |
| EPWM0_G3      | 500C 0012h       |
| EPWM1_G0      | 5000 1012h       |
| EPWM1_G1      | 5004 1012h       |
| EPWM1_G2      | 5008 1012h       |
| EPWM1_G3      | 500C 1012h       |
| EPWM2_G0      | 5000 2012h       |
| EPWM2_G1      | 5004 2012h       |
| EPWM2_G2      | 5008 2012h       |
| EPWM2_G3      | 500C 2012h       |
| EPWM3_G0      | 5000 3012h       |
| EPWM3_G1      | 5004 3012h       |
| EPWM3_G2      | 5008 3012h       |
| EPWM3_G3      | 500C 3012h       |
| EPWM4_G0      | 5000 4012h       |
| EPWM4_G1      | 5004 4012h       |
| EPWM4_G2      | 5008 4012h       |
| EPWM4_G3      | 500C 4012h       |
| EPWM5_G0      | 5000 5012h       |
| EPWM5_G1      | 5004 5012h       |
| EPWM5_G2      | 5008 5012h       |
| EPWM5_G3      | 500C 5012h       |
| EPWM6_G0      | 5000 6012h       |
| EPWM6_G1      | 5004 6012h       |
| EPWM6_G2      | 5008 6012h       |
| EPWM6_G3      | 500C 6012h       |
| EPWM7_G0      | 5000 7012h       |
| EPWM7_G1      | 5004 7012h       |
| EPWM7_G2      | 5008 7012h       |
| EPWM7_G3      | 500C 7012h       |
| EPWM8_G0      | 5000 8012h       |
| EPWM8_G1      | 5004 8012h       |
| EPWM8_G2      | 5008 8012h       |
| EPWM8_G3      | 500C 8012h       |
| EPWM9_G0      | 5000 9012h       |
| EPWM9_G1      | 5004 9012h       |
| EPWM9_G2      | 5008 9012h       |

**Table 3-838. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9012h       |
| EPWM10_G0     | 5000 A012h       |
| EPWM10_G1     | 5004 A012h       |
| EPWM10_G2     | 5008 A012h       |
| EPWM10_G3     | 500C A012h       |
| EPWM11_G0     | 5000 B012h       |
| EPWM11_G1     | 5004 B012h       |
| EPWM11_G2     | 5008 B012h       |
| EPWM11_G3     | 500C B012h       |
| EPWM12_G0     | 5000 C012h       |
| EPWM12_G1     | 5004 C012h       |
| EPWM12_G2     | 5008 C012h       |
| EPWM12_G3     | 500C C012h       |
| EPWM13_G0     | 5000 D012h       |
| EPWM13_G1     | 5004 D012h       |
| EPWM13_G2     | 5008 D012h       |
| EPWM13_G3     | 500C D012h       |
| EPWM14_G0     | 5000 E012h       |
| EPWM14_G1     | 5004 E012h       |
| EPWM14_G2     | 5008 E012h       |
| EPWM14_G3     | 500C E012h       |
| EPWM15_G0     | 5000 F012h       |
| EPWM15_G1     | 5004 F012h       |
| EPWM15_G2     | 5008 F012h       |
| EPWM15_G3     | 500C F012h       |
| EPWM16_G0     | 5001 0012h       |
| EPWM16_G1     | 5005 0012h       |
| EPWM16_G2     | 5009 0012h       |
| EPWM16_G3     | 500D 0012h       |
| EPWM17_G0     | 5001 1012h       |
| EPWM17_G1     | 5005 1012h       |
| EPWM17_G2     | 5009 1012h       |
| EPWM17_G3     | 500D 1012h       |
| EPWM18_G0     | 5001 2012h       |
| EPWM18_G1     | 5005 2012h       |
| EPWM18_G2     | 5009 2012h       |
| EPWM18_G3     | 500D 2012h       |
| EPWM19_G0     | 5001 3012h       |
| EPWM19_G1     | 5005 3012h       |
| EPWM19_G2     | 5009 3012h       |
| EPWM19_G3     | 500D 3012h       |
| EPWM20_G0     | 5001 4012h       |
| EPWM20_G1     | 5005 4012h       |
| EPWM20_G2     | 5009 4012h       |
| EPWM20_G3     | 500D 4012h       |

**Table 3-838. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5012h       |
| EPWM21_G1     | 5005 5012h       |
| EPWM21_G2     | 5009 5012h       |
| EPWM21_G3     | 500D 5012h       |
| EPWM22_G0     | 5001 6012h       |
| EPWM22_G1     | 5005 6012h       |
| EPWM22_G2     | 5009 6012h       |
| EPWM22_G3     | 500D 6012h       |
| EPWM23_G0     | 5001 7012h       |
| EPWM23_G1     | 5005 7012h       |
| EPWM23_G2     | 5009 7012h       |
| EPWM23_G3     | 500D 7012h       |
| EPWM24_G0     | 5001 8012h       |
| EPWM24_G1     | 5005 8012h       |
| EPWM24_G2     | 5009 8012h       |
| EPWM24_G3     | 500D 8012h       |
| EPWM25_G0     | 5001 9012h       |
| EPWM25_G1     | 5005 9012h       |
| EPWM25_G2     | 5009 9012h       |
| EPWM25_G3     | 500D 9012h       |
| EPWM26_G0     | 5001 A012h       |
| EPWM26_G1     | 5005 A012h       |
| EPWM26_G2     | 5009 A012h       |
| EPWM26_G3     | 500D A012h       |
| EPWM27_G0     | 5001 B012h       |
| EPWM27_G1     | 5005 B012h       |
| EPWM27_G2     | 5009 B012h       |
| EPWM27_G3     | 500D B012h       |
| EPWM28_G0     | 5001 C012h       |
| EPWM28_G1     | 5005 C012h       |
| EPWM28_G2     | 5009 C012h       |
| EPWM28_G3     | 500D C012h       |
| EPWM29_G0     | 5001 D012h       |
| EPWM29_G1     | 5005 D012h       |
| EPWM29_G2     | 5009 D012h       |
| EPWM29_G3     | 500D D012h       |
| EPWM30_G0     | 5001 E012h       |
| EPWM30_G1     | 5005 E012h       |
| EPWM30_G2     | 5009 E012h       |
| EPWM30_G3     | 500D E012h       |
| EPWM31_G0     | 5001 F012h       |
| EPWM31_G1     | 5005 F012h       |
| EPWM31_G2     | 5009 F012h       |
| EPWM31_G3     | 500D F012h       |

**Figure 3-260. EPWM\_CMPCTL2 Name Register**

| 15         | 14        | 13         | 12        | 11        | 10 | 9          | 8 |
|------------|-----------|------------|-----------|-----------|----|------------|---|
| RESERVED_3 |           | LOADDSYNC  |           | LOADCSYNC |    | RESERVED_2 |   |
| R          |           | R/W        |           | R/W       |    | R          |   |
| 0h         |           | 0h         |           | 0h        |    | 0h         |   |
| 7          | 6         | 5          | 4         | 3         | 2  | 1          | 0 |
| RESERVED_2 | SHDWDMODE | RESERVED_1 | SHDWCMODE | LOADDMODE |    | LOADCMODE  |   |
| R          | R/W       | R          | R/W       | R/W       |    | R/W        |   |
| 0h         | 0h        | 0h         | 0h        | 0h        |    | 0h         |   |

**Table 3-840. EPWM\_CMPCTL2 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                            |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | RESERVED_3 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                               |
| 13:12 | LOADDSYNC  | R/W  | 0h    | Shadow to Active CMPD Register Load on SYNC event<br>00:Shadow to Active Load of CMPD occurs according to LOADDMODE<br>01:Shadow to Active Load of CMPD occurs both according to LOADDMODE bits and when SYNC occurs<br>10:Shadow to Active Load of CMPD occurs only when a SYNC is received<br>11:Reserved<br>Note: This bit is valid only if CMPCTL2[SHDWDMODE] = 0. |
| 11:10 | LOADCSYNC  | R/W  | 0h    | Shadow to Active CMPC Register Load on SYNC event<br>00:Shadow to Active Load of CMPC occurs according to LOADCMODE<br>01:Shadow to Active Load of CMPC occurs both according to LOADCMODE bits and when SYNC occurs<br>10:Shadow to Active Load of CMPC occurs only when a SYNC is received<br>11:Reserved<br>Note: This bit is valid only if CMPCTL2[SHDWCMODE] = 0. |
| 9:7   | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                               |
| 6     | SHDWDMODE  | R/W  | 0h    | Counter-Compare D Register Operating Mode<br>0:Shadow mode - operates as a double buffer. All writes via the CPU access Shadow register.<br>1:Immediate mode - only the Active compare register is used. All writes/reads via the CPU directly access the Active register for immediate Compare action.                                                                |
| 5     | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                               |
| 4     | SHDWCMODE  | R/W  | 0h    | Counter-Compare C Register Operating Mode<br>0:Shadow mode - operates as a double buffer. All writes via the CPU access Shadow register.<br>1:Immediate mode - only the Active compare register is used. All writes/reads via the CPU directly access the Active register for immediate Compare action.                                                                |
| 3:2   | LOADDMODE  | R/W  | 0h    | Active Counter-Compare D [CMPD] Load from Shadow Select Mode<br>00:Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000]<br>01:Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD]<br>10:Load on either CTR = Zero or CTR = PRD<br>11:Freeze [no loads possible]<br>Note: Has no effect in Immediate mode.                             |

**Table 3-840. EPWM\_CMPCTL2 Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                |
|-----|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0 | LOADCMODE | R/W  | 0h    | Active Counter-Compare C [CMPC] Load from Shadow Select Mode<br>00:Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000]<br>01:Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD]<br>10:Load on either CTR = Zero or CTR = PRD<br>11:Freeze [no loads possible]<br>Note: Has no effect in Immediate mode. |

### 3.7.2.10 EPWM\_DBCTL Register

#### 1 EPWM\_DBCTL Register (Offset = 18h) [reset = 0h]

Dead-Band Generator Control Register.

Return to [Summary Table](#)

**Table 3-841. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0018h       |
| EPWM0_G1      | 5004 0018h       |
| EPWM0_G2      | 5008 0018h       |
| EPWM0_G3      | 500C 0018h       |
| EPWM1_G0      | 5000 1018h       |
| EPWM1_G1      | 5004 1018h       |
| EPWM1_G2      | 5008 1018h       |
| EPWM1_G3      | 500C 1018h       |
| EPWM2_G0      | 5000 2018h       |
| EPWM2_G1      | 5004 2018h       |
| EPWM2_G2      | 5008 2018h       |
| EPWM2_G3      | 500C 2018h       |
| EPWM3_G0      | 5000 3018h       |
| EPWM3_G1      | 5004 3018h       |
| EPWM3_G2      | 5008 3018h       |
| EPWM3_G3      | 500C 3018h       |
| EPWM4_G0      | 5000 4018h       |
| EPWM4_G1      | 5004 4018h       |
| EPWM4_G2      | 5008 4018h       |
| EPWM4_G3      | 500C 4018h       |
| EPWM5_G0      | 5000 5018h       |
| EPWM5_G1      | 5004 5018h       |
| EPWM5_G2      | 5008 5018h       |
| EPWM5_G3      | 500C 5018h       |
| EPWM6_G0      | 5000 6018h       |
| EPWM6_G1      | 5004 6018h       |
| EPWM6_G2      | 5008 6018h       |
| EPWM6_G3      | 500C 6018h       |
| EPWM7_G0      | 5000 7018h       |
| EPWM7_G1      | 5004 7018h       |
| EPWM7_G2      | 5008 7018h       |
| EPWM7_G3      | 500C 7018h       |
| EPWM8_G0      | 5000 8018h       |
| EPWM8_G1      | 5004 8018h       |
| EPWM8_G2      | 5008 8018h       |
| EPWM8_G3      | 500C 8018h       |
| EPWM9_G0      | 5000 9018h       |
| EPWM9_G1      | 5004 9018h       |
| EPWM9_G2      | 5008 9018h       |



**Table 3-841. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9018h       |
| EPWM10_G0     | 5000 A018h       |
| EPWM10_G1     | 5004 A018h       |
| EPWM10_G2     | 5008 A018h       |
| EPWM10_G3     | 500C A018h       |
| EPWM11_G0     | 5000 B018h       |
| EPWM11_G1     | 5004 B018h       |
| EPWM11_G2     | 5008 B018h       |
| EPWM11_G3     | 500C B018h       |
| EPWM12_G0     | 5000 C018h       |
| EPWM12_G1     | 5004 C018h       |
| EPWM12_G2     | 5008 C018h       |
| EPWM12_G3     | 500C C018h       |
| EPWM13_G0     | 5000 D018h       |
| EPWM13_G1     | 5004 D018h       |
| EPWM13_G2     | 5008 D018h       |
| EPWM13_G3     | 500C D018h       |
| EPWM14_G0     | 5000 E018h       |
| EPWM14_G1     | 5004 E018h       |
| EPWM14_G2     | 5008 E018h       |
| EPWM14_G3     | 500C E018h       |
| EPWM15_G0     | 5000 F018h       |
| EPWM15_G1     | 5004 F018h       |
| EPWM15_G2     | 5008 F018h       |
| EPWM15_G3     | 500C F018h       |
| EPWM16_G0     | 5001 0018h       |
| EPWM16_G1     | 5005 0018h       |
| EPWM16_G2     | 5009 0018h       |
| EPWM16_G3     | 500D 0018h       |
| EPWM17_G0     | 5001 1018h       |
| EPWM17_G1     | 5005 1018h       |
| EPWM17_G2     | 5009 1018h       |
| EPWM17_G3     | 500D 1018h       |
| EPWM18_G0     | 5001 2018h       |
| EPWM18_G1     | 5005 2018h       |
| EPWM18_G2     | 5009 2018h       |
| EPWM18_G3     | 500D 2018h       |
| EPWM19_G0     | 5001 3018h       |
| EPWM19_G1     | 5005 3018h       |
| EPWM19_G2     | 5009 3018h       |
| EPWM19_G3     | 500D 3018h       |
| EPWM20_G0     | 5001 4018h       |
| EPWM20_G1     | 5005 4018h       |
| EPWM20_G2     | 5009 4018h       |
| EPWM20_G3     | 500D 4018h       |

**Table 3-841. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5018h       |
| EPWM21_G1     | 5005 5018h       |
| EPWM21_G2     | 5009 5018h       |
| EPWM21_G3     | 500D 5018h       |
| EPWM22_G0     | 5001 6018h       |
| EPWM22_G1     | 5005 6018h       |
| EPWM22_G2     | 5009 6018h       |
| EPWM22_G3     | 500D 6018h       |
| EPWM23_G0     | 5001 7018h       |
| EPWM23_G1     | 5005 7018h       |
| EPWM23_G2     | 5009 7018h       |
| EPWM23_G3     | 500D 7018h       |
| EPWM24_G0     | 5001 8018h       |
| EPWM24_G1     | 5005 8018h       |
| EPWM24_G2     | 5009 8018h       |
| EPWM24_G3     | 500D 8018h       |
| EPWM25_G0     | 5001 9018h       |
| EPWM25_G1     | 5005 9018h       |
| EPWM25_G2     | 5009 9018h       |
| EPWM25_G3     | 500D 9018h       |
| EPWM26_G0     | 5001 A018h       |
| EPWM26_G1     | 5005 A018h       |
| EPWM26_G2     | 5009 A018h       |
| EPWM26_G3     | 500D A018h       |
| EPWM27_G0     | 5001 B018h       |
| EPWM27_G1     | 5005 B018h       |
| EPWM27_G2     | 5009 B018h       |
| EPWM27_G3     | 500D B018h       |
| EPWM28_G0     | 5001 C018h       |
| EPWM28_G1     | 5005 C018h       |
| EPWM28_G2     | 5009 C018h       |
| EPWM28_G3     | 500D C018h       |
| EPWM29_G0     | 5001 D018h       |
| EPWM29_G1     | 5005 D018h       |
| EPWM29_G2     | 5009 D018h       |
| EPWM29_G3     | 500D D018h       |
| EPWM30_G0     | 5001 E018h       |
| EPWM30_G1     | 5005 E018h       |
| EPWM30_G2     | 5009 E018h       |
| EPWM30_G3     | 500D E018h       |
| EPWM31_G0     | 5001 F018h       |
| EPWM31_G1     | 5005 F018h       |
| EPWM31_G2     | 5009 F018h       |
| EPWM31_G3     | 500D F018h       |

**Figure 3-261. EPWM\_DBCTL Name Register**

| 15          | 14        | 13      | 12 | 11                | 10                | 9           | 8 |
|-------------|-----------|---------|----|-------------------|-------------------|-------------|---|
| HALFCYCLE   | DEDB_MODE | OUTSWAP |    | SHDWDBFED<br>MODE | SHDWDBRED<br>MODE | LOADFEDMODE |   |
| R/W         | R/W       | R/W     |    | R/W               | R/W               | R/W         |   |
| 0h          | 0h        | 0h      |    | 0h                | 0h                | 0h          |   |
| 7           | 6         | 5       | 4  | 3                 | 2                 | 1           | 0 |
| LOADREDMODE |           | IN_MODE |    | POLSEL            |                   | OUT_MODE    |   |
| R/W         |           | R/W     |    | R/W               |                   | R/W         |   |
| 0h          |           | 0h      |    | 0h                |                   | 0h          |   |

**Table 3-843. EPWM\_DBCTL Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|---------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | HALFCYCLE     | R/W  | 0h    | Half Cycle Clocking Enable Bit<br>0: Full cycle clocking enabled. The dead-band counters are clocked at the TBCLK rate.<br>1: Half cycle clocking enabled. The dead-band counters are clocked at TBCLK*2.                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 14    | DEDB_MODE     | R/W  | 0h    | Dead Band Dual-Edge B Mode Control [S8 switch]<br>0: Rising edge delay applied to InA/InB as selected by S4 switch [IN-MODE bits] on A signal path only. Falling edge delay applied to InA/InB as selected by S5 switch [INMODE bits] on B signal path only.<br>1: Rising edge delay and falling edge delay applied to source selected by S4 switch [INMODE bits] and output to B signal path only. Note: When this bit is set to 1, user should always either set OUT_MODE bits such that Apath = InA OR OUTSWAP bits such that OutA=Bpath otherwise, OutA will be invalid.                                                                                                      |
| 13:12 | OUTSWAP       | R/W  | 0h    | Dead Band Output Swap Control<br>Bit 13 controls the S6 switch and bit 12 controls the S7 switch.<br>00: OutA and OutB signals are as defined by OUT-MODE bits.<br>01: OutA = A-path as defined by OUT-MODE bits.<br>OutB = A-path as defined by OUT-MODE bits [rising edge delay or delay-bypassed A signal path].<br>10: OutA = B-path as defined by OUT-MODE bits [falling edge delay or delay-bypassed B signal path].<br>OutB = B-path as defined by OUT-MODE bits.<br>11: OutA = B-path as defined by OUT-MODE bits [falling edge delay or delay-bypassed B signal path].<br>OutB = A-path as defined by OUT-MODE bits [rising edge delay or delay-bypassed A signal path]. |
| 11    | SHDWDBFEDMODE | R/W  | 0h    | FED Dead-Band Load Mode<br>0: Immediate mode. Only the active DBFED register is used. All writes/reads via the CPU directly access the active register for immediate "FED dead-band action."<br>1: Shadow mode. Operates as a double buffer. All writes via the CPU access Shadow register. Default at Reset is Immediate mode [for compatibility with legacy].                                                                                                                                                                                                                                                                                                                   |
| 10    | SHDWDBREDMODE | R/W  | 0h    | RED Dead-Band Load Mode<br>0: Immediate mode. Only the active DBRED register is used. All writes/reads via the CPU directly access the active register for immediate "RED dead-band action."<br>1: Shadow mode. Operates as a double buffer. All writes via the CPU access Shadow register. Default at Reset is Immediate mode [for compatibility with legacy].                                                                                                                                                                                                                                                                                                                   |

**Table 3-843. EPWM\_DBCTL Register Field Descriptions (continued)**

| Bit | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|-------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9:8 | LOADFEDMODE | R/W  | 0h    | Active DBFED Load from Shadow Select Mode<br>00:Load on Counter = 0 [CNT_eq]<br>01:Load on Counter = Period [PRD_eq]<br>10:Load on either Counter = 0, or Counter = Period<br>11:Freeze [no loads possible]<br>Note: has no effect in Immediate mode.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 7:6 | LOADREDMODE | R/W  | 0h    | Active DBRED Load from Shadow Select Mode<br>00:Load on Counter = 0 [CNT_eq]<br>01:Load on Counter = Period [PRD_eq]<br>10:Load on either Counter = 0, or Counter = Period<br>11:Freeze [no loads possible]<br>Note: has no effect in Immediate mode.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 5:4 | IN_MODE     | R/W  | 0h    | Dead-Band Input Mode Control<br>Bit 5 controls the S5 switch and bit 4 controls the S4 switch shown. This allows you to select the input source to the falling-edge and rising-edge delay. To produce classical dead-band waveforms the default is EPWMxA In is the source for both falling and rising-edge delays.<br>00:EPWMxA In [from the action-qualifier] is the source for both falling-edge and rising-edge delay.<br>01:EPWMxB In [from the action-qualifier] is the source for rising-edge delayed signal.<br>EPWMxA In [from the action-qualifier] is the source for falling-edge delayed signal.<br>10:EPWMxA In [from the action-qualifier] is the source for rising-edge delayed signal.<br>EPWMxB In [from the action-qualifier] is the source for falling-edge delayed signal.<br>11:EPWMxB In [from the action-qualifier] is the source for both rising-edge delay and falling-edge delayed signal. |
| 3:2 | POLSEL      | R/W  | 0h    | Polarity Select Control<br>Bit 3 controls the S3 switch and bit 2 controls the S2 switch. This allows you to selectively invert one of the delayed signals before it is sent out of the dead-band submodule. The following descriptions correspond to classical upper/lower switch control as found in one leg of a digital motor control inverter. These assume that DBCTL[OUT_MODE] = 2'b11 and DBCTL[IN_MODE] = 0x0. Other enhanced modes are also possible, but not regarded as typical usage modes.<br>00:Active high [AH] mode. Neither EPWMxA nor EPWMxB is inverted [default].<br>01:Active low complementary [ALC] mode. EPWMxA is inverted.<br>10:Active high complementary [AHC]. EPWMxB is inverted.<br>11:Active low [AL] mode. Both EPWMxA and EPWMxB are inverted.                                                                                                                                    |
| 1:0 | OUT_MODE    | R/W  | 0h    | Dead-Band Output Mode Control<br>Bit 1 controls the S1 switch and bit 0 controls the S0 switch.<br>00:DBM is fully disabled or by-passed. In this mode the POLSEL and IN-MODE bits have no effect.<br>01:Apath = InA [delay is by-passed for A signal path]<br>Bpath = FED [Falling Edge Delay in B signal path]<br>10:Apath = RED [Rising Edge Delay in A signal path]<br>Bpath = InB [delay is by-passed for B signal path]<br>11:DBM is fully enabled [i.e. both RED and FED active]                                                                                                                                                                                                                                                                                                                                                                                                                              |

### 3.7.2.11 EPWM\_DBCTL2 Register

#### 1 EPWM\_DBCTL2 Register (Offset = 1Ah) [reset = 0h]

Dead-Band Generator Control Register 2

Return to [Summary Table](#)

**Table 3-844. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 001Ah       |
| EPWM0_G1      | 5004 001Ah       |
| EPWM0_G2      | 5008 001Ah       |
| EPWM0_G3      | 500C 001Ah       |
| EPWM1_G0      | 5000 101Ah       |
| EPWM1_G1      | 5004 101Ah       |
| EPWM1_G2      | 5008 101Ah       |
| EPWM1_G3      | 500C 101Ah       |
| EPWM2_G0      | 5000 201Ah       |
| EPWM2_G1      | 5004 201Ah       |
| EPWM2_G2      | 5008 201Ah       |
| EPWM2_G3      | 500C 201Ah       |
| EPWM3_G0      | 5000 301Ah       |
| EPWM3_G1      | 5004 301Ah       |
| EPWM3_G2      | 5008 301Ah       |
| EPWM3_G3      | 500C 301Ah       |
| EPWM4_G0      | 5000 401Ah       |
| EPWM4_G1      | 5004 401Ah       |
| EPWM4_G2      | 5008 401Ah       |
| EPWM4_G3      | 500C 401Ah       |
| EPWM5_G0      | 5000 501Ah       |
| EPWM5_G1      | 5004 501Ah       |
| EPWM5_G2      | 5008 501Ah       |
| EPWM5_G3      | 500C 501Ah       |
| EPWM6_G0      | 5000 601Ah       |
| EPWM6_G1      | 5004 601Ah       |
| EPWM6_G2      | 5008 601Ah       |
| EPWM6_G3      | 500C 601Ah       |
| EPWM7_G0      | 5000 701Ah       |
| EPWM7_G1      | 5004 701Ah       |
| EPWM7_G2      | 5008 701Ah       |
| EPWM7_G3      | 500C 701Ah       |
| EPWM8_G0      | 5000 801Ah       |
| EPWM8_G1      | 5004 801Ah       |
| EPWM8_G2      | 5008 801Ah       |
| EPWM8_G3      | 500C 801Ah       |
| EPWM9_G0      | 5000 901Ah       |
| EPWM9_G1      | 5004 901Ah       |
| EPWM9_G2      | 5008 901Ah       |

**Table 3-844. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 901Ah       |
| EPWM10_G0     | 5000 A01Ah       |
| EPWM10_G1     | 5004 A01Ah       |
| EPWM10_G2     | 5008 A01Ah       |
| EPWM10_G3     | 500C A01Ah       |
| EPWM11_G0     | 5000 B01Ah       |
| EPWM11_G1     | 5004 B01Ah       |
| EPWM11_G2     | 5008 B01Ah       |
| EPWM11_G3     | 500C B01Ah       |
| EPWM12_G0     | 5000 C01Ah       |
| EPWM12_G1     | 5004 C01Ah       |
| EPWM12_G2     | 5008 C01Ah       |
| EPWM12_G3     | 500C C01Ah       |
| EPWM13_G0     | 5000 D01Ah       |
| EPWM13_G1     | 5004 D01Ah       |
| EPWM13_G2     | 5008 D01Ah       |
| EPWM13_G3     | 500C D01Ah       |
| EPWM14_G0     | 5000 E01Ah       |
| EPWM14_G1     | 5004 E01Ah       |
| EPWM14_G2     | 5008 E01Ah       |
| EPWM14_G3     | 500C E01Ah       |
| EPWM15_G0     | 5000 F01Ah       |
| EPWM15_G1     | 5004 F01Ah       |
| EPWM15_G2     | 5008 F01Ah       |
| EPWM15_G3     | 500C F01Ah       |
| EPWM16_G0     | 5001 001Ah       |
| EPWM16_G1     | 5005 001Ah       |
| EPWM16_G2     | 5009 001Ah       |
| EPWM16_G3     | 500D 001Ah       |
| EPWM17_G0     | 5001 101Ah       |
| EPWM17_G1     | 5005 101Ah       |
| EPWM17_G2     | 5009 101Ah       |
| EPWM17_G3     | 500D 101Ah       |
| EPWM18_G0     | 5001 201Ah       |
| EPWM18_G1     | 5005 201Ah       |
| EPWM18_G2     | 5009 201Ah       |
| EPWM18_G3     | 500D 201Ah       |
| EPWM19_G0     | 5001 301Ah       |
| EPWM19_G1     | 5005 301Ah       |
| EPWM19_G2     | 5009 301Ah       |
| EPWM19_G3     | 500D 301Ah       |
| EPWM20_G0     | 5001 401Ah       |
| EPWM20_G1     | 5005 401Ah       |
| EPWM20_G2     | 5009 401Ah       |
| EPWM20_G3     | 500D 401Ah       |

**Table 3-844. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 501Ah       |
| EPWM21_G1     | 5005 501Ah       |
| EPWM21_G2     | 5009 501Ah       |
| EPWM21_G3     | 500D 501Ah       |
| EPWM22_G0     | 5001 601Ah       |
| EPWM22_G1     | 5005 601Ah       |
| EPWM22_G2     | 5009 601Ah       |
| EPWM22_G3     | 500D 601Ah       |
| EPWM23_G0     | 5001 701Ah       |
| EPWM23_G1     | 5005 701Ah       |
| EPWM23_G2     | 5009 701Ah       |
| EPWM23_G3     | 500D 701Ah       |
| EPWM24_G0     | 5001 801Ah       |
| EPWM24_G1     | 5005 801Ah       |
| EPWM24_G2     | 5009 801Ah       |
| EPWM24_G3     | 500D 801Ah       |
| EPWM25_G0     | 5001 901Ah       |
| EPWM25_G1     | 5005 901Ah       |
| EPWM25_G2     | 5009 901Ah       |
| EPWM25_G3     | 500D 901Ah       |
| EPWM26_G0     | 5001 A01Ah       |
| EPWM26_G1     | 5005 A01Ah       |
| EPWM26_G2     | 5009 A01Ah       |
| EPWM26_G3     | 500D A01Ah       |
| EPWM27_G0     | 5001 B01Ah       |
| EPWM27_G1     | 5005 B01Ah       |
| EPWM27_G2     | 5009 B01Ah       |
| EPWM27_G3     | 500D B01Ah       |
| EPWM28_G0     | 5001 C01Ah       |
| EPWM28_G1     | 5005 C01Ah       |
| EPWM28_G2     | 5009 C01Ah       |
| EPWM28_G3     | 500D C01Ah       |
| EPWM29_G0     | 5001 D01Ah       |
| EPWM29_G1     | 5005 D01Ah       |
| EPWM29_G2     | 5009 D01Ah       |
| EPWM29_G3     | 500D D01Ah       |
| EPWM30_G0     | 5001 E01Ah       |
| EPWM30_G1     | 5005 E01Ah       |
| EPWM30_G2     | 5009 E01Ah       |
| EPWM30_G3     | 500D E01Ah       |
| EPWM31_G0     | 5001 F01Ah       |
| EPWM31_G1     | 5005 F01Ah       |
| EPWM31_G2     | 5009 F01Ah       |
| EPWM31_G3     | 500D F01Ah       |

**Figure 3-262. EPWM\_DBCTL2 Name Register**

|            |    |    |    |    |               |               |   |
|------------|----|----|----|----|---------------|---------------|---|
| 15         | 14 | 13 | 12 | 11 | 10            | 9             | 8 |
| RESERVED_1 |    |    |    |    |               |               |   |
| R          |    |    |    |    |               |               |   |
| 0h         |    |    |    |    |               |               |   |
| 7          | 6  | 5  | 4  | 3  | 2             | 1             | 0 |
| RESERVED_1 |    |    |    |    | SHDWDBCTLMODE | LOADDBCTLMODE |   |
| R          |    |    |    |    | R/W           | R/W           |   |
| 0h         |    |    |    |    | 0h            | 0h            |   |

**Table 3-846. EPWM\_DBCTL2 Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                                                                                                                                                                                                                                                                |
|------|---------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:3 | RESERVED_1    | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                   |
| 2    | SHDWDBCTLMODE | R/W  | 0h    | DBCTL Load Mode<br>0:Immediate mode - only the Active DBCTL register is used. All writes/reads via the CPU directly access the Active register.<br>1:Shadow mode - All writes and reads to bits [5:0] of the DBCTL register are shadowed. All other bits still access the active register. |
| 1:0  | LOADDBCTLMODE | R/W  | 0h    | Active DBCTL Load from Shadow Select Mode<br>00:Load on Counter = 0 [CNT_eq]<br>01:Load on Counter = Period [PRD_eq]<br>10:Load on either Counter = 0, or Counter = Period<br>11:Freeze [no loads possible]<br>Note: has no effect in Immediate mode                                       |



### 3.7.2.12 EPWM\_AQCTL Register

#### 1 EPWM\_AQCTL Register (Offset = 20h) [reset = 0h]

Action Qualifier Control Register.

Return to [Summary Table](#)

**Table 3-847. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0020h       |
| EPWM0_G1      | 5004 0020h       |
| EPWM0_G2      | 5008 0020h       |
| EPWM0_G3      | 500C 0020h       |
| EPWM1_G0      | 5000 1020h       |
| EPWM1_G1      | 5004 1020h       |
| EPWM1_G2      | 5008 1020h       |
| EPWM1_G3      | 500C 1020h       |
| EPWM2_G0      | 5000 2020h       |
| EPWM2_G1      | 5004 2020h       |
| EPWM2_G2      | 5008 2020h       |
| EPWM2_G3      | 500C 2020h       |
| EPWM3_G0      | 5000 3020h       |
| EPWM3_G1      | 5004 3020h       |
| EPWM3_G2      | 5008 3020h       |
| EPWM3_G3      | 500C 3020h       |
| EPWM4_G0      | 5000 4020h       |
| EPWM4_G1      | 5004 4020h       |
| EPWM4_G2      | 5008 4020h       |
| EPWM4_G3      | 500C 4020h       |
| EPWM5_G0      | 5000 5020h       |
| EPWM5_G1      | 5004 5020h       |
| EPWM5_G2      | 5008 5020h       |
| EPWM5_G3      | 500C 5020h       |
| EPWM6_G0      | 5000 6020h       |
| EPWM6_G1      | 5004 6020h       |
| EPWM6_G2      | 5008 6020h       |
| EPWM6_G3      | 500C 6020h       |
| EPWM7_G0      | 5000 7020h       |
| EPWM7_G1      | 5004 7020h       |
| EPWM7_G2      | 5008 7020h       |
| EPWM7_G3      | 500C 7020h       |
| EPWM8_G0      | 5000 8020h       |
| EPWM8_G1      | 5004 8020h       |
| EPWM8_G2      | 5008 8020h       |
| EPWM8_G3      | 500C 8020h       |
| EPWM9_G0      | 5000 9020h       |
| EPWM9_G1      | 5004 9020h       |
| EPWM9_G2      | 5008 9020h       |

**Table 3-847. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9020h       |
| EPWM10_G0     | 5000 A020h       |
| EPWM10_G1     | 5004 A020h       |
| EPWM10_G2     | 5008 A020h       |
| EPWM10_G3     | 500C A020h       |
| EPWM11_G0     | 5000 B020h       |
| EPWM11_G1     | 5004 B020h       |
| EPWM11_G2     | 5008 B020h       |
| EPWM11_G3     | 500C B020h       |
| EPWM12_G0     | 5000 C020h       |
| EPWM12_G1     | 5004 C020h       |
| EPWM12_G2     | 5008 C020h       |
| EPWM12_G3     | 500C C020h       |
| EPWM13_G0     | 5000 D020h       |
| EPWM13_G1     | 5004 D020h       |
| EPWM13_G2     | 5008 D020h       |
| EPWM13_G3     | 500C D020h       |
| EPWM14_G0     | 5000 E020h       |
| EPWM14_G1     | 5004 E020h       |
| EPWM14_G2     | 5008 E020h       |
| EPWM14_G3     | 500C E020h       |
| EPWM15_G0     | 5000 F020h       |
| EPWM15_G1     | 5004 F020h       |
| EPWM15_G2     | 5008 F020h       |
| EPWM15_G3     | 500C F020h       |
| EPWM16_G0     | 5001 0020h       |
| EPWM16_G1     | 5005 0020h       |
| EPWM16_G2     | 5009 0020h       |
| EPWM16_G3     | 500D 0020h       |
| EPWM17_G0     | 5001 1020h       |
| EPWM17_G1     | 5005 1020h       |
| EPWM17_G2     | 5009 1020h       |
| EPWM17_G3     | 500D 1020h       |
| EPWM18_G0     | 5001 2020h       |
| EPWM18_G1     | 5005 2020h       |
| EPWM18_G2     | 5009 2020h       |
| EPWM18_G3     | 500D 2020h       |
| EPWM19_G0     | 5001 3020h       |
| EPWM19_G1     | 5005 3020h       |
| EPWM19_G2     | 5009 3020h       |
| EPWM19_G3     | 500D 3020h       |
| EPWM20_G0     | 5001 4020h       |
| EPWM20_G1     | 5005 4020h       |
| EPWM20_G2     | 5009 4020h       |
| EPWM20_G3     | 500D 4020h       |

**Table 3-847. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5020h       |
| EPWM21_G1     | 5005 5020h       |
| EPWM21_G2     | 5009 5020h       |
| EPWM21_G3     | 500D 5020h       |
| EPWM22_G0     | 5001 6020h       |
| EPWM22_G1     | 5005 6020h       |
| EPWM22_G2     | 5009 6020h       |
| EPWM22_G3     | 500D 6020h       |
| EPWM23_G0     | 5001 7020h       |
| EPWM23_G1     | 5005 7020h       |
| EPWM23_G2     | 5009 7020h       |
| EPWM23_G3     | 500D 7020h       |
| EPWM24_G0     | 5001 8020h       |
| EPWM24_G1     | 5005 8020h       |
| EPWM24_G2     | 5009 8020h       |
| EPWM24_G3     | 500D 8020h       |
| EPWM25_G0     | 5001 9020h       |
| EPWM25_G1     | 5005 9020h       |
| EPWM25_G2     | 5009 9020h       |
| EPWM25_G3     | 500D 9020h       |
| EPWM26_G0     | 5001 A020h       |
| EPWM26_G1     | 5005 A020h       |
| EPWM26_G2     | 5009 A020h       |
| EPWM26_G3     | 500D A020h       |
| EPWM27_G0     | 5001 B020h       |
| EPWM27_G1     | 5005 B020h       |
| EPWM27_G2     | 5009 B020h       |
| EPWM27_G3     | 500D B020h       |
| EPWM28_G0     | 5001 C020h       |
| EPWM28_G1     | 5005 C020h       |
| EPWM28_G2     | 5009 C020h       |
| EPWM28_G3     | 500D C020h       |
| EPWM29_G0     | 5001 D020h       |
| EPWM29_G1     | 5005 D020h       |
| EPWM29_G2     | 5009 D020h       |
| EPWM29_G3     | 500D D020h       |
| EPWM30_G0     | 5001 E020h       |
| EPWM30_G1     | 5005 E020h       |
| EPWM30_G2     | 5009 E020h       |
| EPWM30_G3     | 500D E020h       |
| EPWM31_G0     | 5001 F020h       |
| EPWM31_G1     | 5005 F020h       |
| EPWM31_G2     | 5009 F020h       |
| EPWM31_G3     | 500D F020h       |

**Figure 3-263. EPWM\_AQCTL Name Register**

| 15         | 14          | 13         | 12          | 11        | 10 | 9         | 8 |
|------------|-------------|------------|-------------|-----------|----|-----------|---|
| RESERVED_3 |             |            |             | LDAQBSYNC |    | LDAQASYNC |   |
| R          |             |            |             | R/W       |    | R/W       |   |
| 0h         |             |            |             | 0h        |    | 0h        |   |
| 7          | 6           | 5          | 4           | 3         | 2  | 1         | 0 |
| RESERVED_2 | SHDWAQBMODE | RESERVED_1 | SHDWAQAMODE | LDAQBMODE |    | LDAQAMODE |   |
| R          | R/W         | R          | R/W         | R/W       |    | R/W       |   |
| 0h         | 0h          | 0h         | 0h          | 0h        |    | 0h        |   |

**Table 3-849. EPWM\_AQCTL Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                      |
|-------|-------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | RESERVED_3  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                         |
| 11:10 | LDAQBSYNC   | R/W  | 0h    | Shadow to Active AQCTLB Register Load on SYNC event<br>00:Shadow to Active Load of AQCTLB occurs according to LDAQBMODE<br>01:Shadow to Active Load of AQCTLB occurs both according to LDAQBMODE bits and when SYNC occurs.<br>10:Shadow to Active Load of AQCTLB occurs only when a SYNC is received.<br>11:Reserved<br>Note: This bit is valid only if AQCTL[SHDWAQBMODE] = 1. |
| 9:8   | LDAQASYNC   | R/W  | 0h    | Shadow to Active AQCTLA Register Load on SYNC event<br>00:Shadow to Active Load of AQCTLA occurs according to LDAQAMODE<br>01:Shadow to Active Load of AQCTLA occurs both according to LDAQAMODE bits and when SYNC occurs.<br>10:Shadow to Active Load of AQCTLA occurs only when a SYNC is received.<br>11:Reserved<br>Note: This bit is valid only if AQCTL[SHDWAQAMODE] = 1. |
| 7     | RESERVED_2  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                         |
| 6     | SHDWAQBMODE | R/W  | 0h    | Action Qualifier B Register operating mode<br>1:Shadow mode - operates as a double buffer. All writes via the CPU access Shadow register.<br>0:Immediate mode - only the Active action qualifier register is used. All writes/reads via the CPU directly access the Active register.                                                                                             |
| 5     | RESERVED_1  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                         |
| 4     | SHDWAQAMODE | R/W  | 0h    | Action Qualifier A Register operating mode<br>1:Shadow mode - operates as a double buffer. All writes via the CPU access Shadow register.<br>0:Immediate mode - only the Active action qualifier register is used. All writes/reads via the CPU directly access the Active register.                                                                                             |
| 3:2   | LDAQBMODE   | R/W  | 0h    | Active Action Qualifier B Load from Shadow Select Mode<br>00:Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000]<br>01:Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD]<br>10:Load on either CTR = Zero or CTR = PRD<br>11:Freeze [no loads possible]<br>Note: has no effect in Immediate mode.                                             |

**Table 3-849. EPWM\_AQCTL Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                          |
|-----|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0 | LDAQAMODE | R/W  | 0h    | Active Action Qualifier A Load from Shadow Select Mode<br>00:Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000]<br>01:Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD]<br>10:Load on either CTR = Zero or CTR = PRD<br>11:Freeze [no loads possible]<br>Note: has no effect in Immediate mode. |

### 3.7.2.13 EPWM\_AQTSRCSEL Register

#### 1 EPWM\_AQTSRCSEL Register (Offset = 22h) [reset = 0h]

Action Qualifier Trigger Event Source Select Register.

Return to [Summary Table](#)

**Table 3-850. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0022h       |
| EPWM0_G1      | 5004 0022h       |
| EPWM0_G2      | 5008 0022h       |
| EPWM0_G3      | 500C 0022h       |
| EPWM1_G0      | 5000 1022h       |
| EPWM1_G1      | 5004 1022h       |
| EPWM1_G2      | 5008 1022h       |
| EPWM1_G3      | 500C 1022h       |
| EPWM2_G0      | 5000 2022h       |
| EPWM2_G1      | 5004 2022h       |
| EPWM2_G2      | 5008 2022h       |
| EPWM2_G3      | 500C 2022h       |
| EPWM3_G0      | 5000 3022h       |
| EPWM3_G1      | 5004 3022h       |
| EPWM3_G2      | 5008 3022h       |
| EPWM3_G3      | 500C 3022h       |
| EPWM4_G0      | 5000 4022h       |
| EPWM4_G1      | 5004 4022h       |
| EPWM4_G2      | 5008 4022h       |
| EPWM4_G3      | 500C 4022h       |
| EPWM5_G0      | 5000 5022h       |
| EPWM5_G1      | 5004 5022h       |
| EPWM5_G2      | 5008 5022h       |
| EPWM5_G3      | 500C 5022h       |
| EPWM6_G0      | 5000 6022h       |
| EPWM6_G1      | 5004 6022h       |
| EPWM6_G2      | 5008 6022h       |
| EPWM6_G3      | 500C 6022h       |
| EPWM7_G0      | 5000 7022h       |
| EPWM7_G1      | 5004 7022h       |
| EPWM7_G2      | 5008 7022h       |
| EPWM7_G3      | 500C 7022h       |
| EPWM8_G0      | 5000 8022h       |
| EPWM8_G1      | 5004 8022h       |
| EPWM8_G2      | 5008 8022h       |
| EPWM8_G3      | 500C 8022h       |
| EPWM9_G0      | 5000 9022h       |
| EPWM9_G1      | 5004 9022h       |
| EPWM9_G2      | 5008 9022h       |

**Table 3-850. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9022h       |
| EPWM10_G0     | 5000 A022h       |
| EPWM10_G1     | 5004 A022h       |
| EPWM10_G2     | 5008 A022h       |
| EPWM10_G3     | 500C A022h       |
| EPWM11_G0     | 5000 B022h       |
| EPWM11_G1     | 5004 B022h       |
| EPWM11_G2     | 5008 B022h       |
| EPWM11_G3     | 500C B022h       |
| EPWM12_G0     | 5000 C022h       |
| EPWM12_G1     | 5004 C022h       |
| EPWM12_G2     | 5008 C022h       |
| EPWM12_G3     | 500C C022h       |
| EPWM13_G0     | 5000 D022h       |
| EPWM13_G1     | 5004 D022h       |
| EPWM13_G2     | 5008 D022h       |
| EPWM13_G3     | 500C D022h       |
| EPWM14_G0     | 5000 E022h       |
| EPWM14_G1     | 5004 E022h       |
| EPWM14_G2     | 5008 E022h       |
| EPWM14_G3     | 500C E022h       |
| EPWM15_G0     | 5000 F022h       |
| EPWM15_G1     | 5004 F022h       |
| EPWM15_G2     | 5008 F022h       |
| EPWM15_G3     | 500C F022h       |
| EPWM16_G0     | 5001 0022h       |
| EPWM16_G1     | 5005 0022h       |
| EPWM16_G2     | 5009 0022h       |
| EPWM16_G3     | 500D 0022h       |
| EPWM17_G0     | 5001 1022h       |
| EPWM17_G1     | 5005 1022h       |
| EPWM17_G2     | 5009 1022h       |
| EPWM17_G3     | 500D 1022h       |
| EPWM18_G0     | 5001 2022h       |
| EPWM18_G1     | 5005 2022h       |
| EPWM18_G2     | 5009 2022h       |
| EPWM18_G3     | 500D 2022h       |
| EPWM19_G0     | 5001 3022h       |
| EPWM19_G1     | 5005 3022h       |
| EPWM19_G2     | 5009 3022h       |
| EPWM19_G3     | 500D 3022h       |
| EPWM20_G0     | 5001 4022h       |
| EPWM20_G1     | 5005 4022h       |
| EPWM20_G2     | 5009 4022h       |
| EPWM20_G3     | 500D 4022h       |

**Table 3-850. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5022h       |
| EPWM21_G1     | 5005 5022h       |
| EPWM21_G2     | 5009 5022h       |
| EPWM21_G3     | 500D 5022h       |
| EPWM22_G0     | 5001 6022h       |
| EPWM22_G1     | 5005 6022h       |
| EPWM22_G2     | 5009 6022h       |
| EPWM22_G3     | 500D 6022h       |
| EPWM23_G0     | 5001 7022h       |
| EPWM23_G1     | 5005 7022h       |
| EPWM23_G2     | 5009 7022h       |
| EPWM23_G3     | 500D 7022h       |
| EPWM24_G0     | 5001 8022h       |
| EPWM24_G1     | 5005 8022h       |
| EPWM24_G2     | 5009 8022h       |
| EPWM24_G3     | 500D 8022h       |
| EPWM25_G0     | 5001 9022h       |
| EPWM25_G1     | 5005 9022h       |
| EPWM25_G2     | 5009 9022h       |
| EPWM25_G3     | 500D 9022h       |
| EPWM26_G0     | 5001 A022h       |
| EPWM26_G1     | 5005 A022h       |
| EPWM26_G2     | 5009 A022h       |
| EPWM26_G3     | 500D A022h       |
| EPWM27_G0     | 5001 B022h       |
| EPWM27_G1     | 5005 B022h       |
| EPWM27_G2     | 5009 B022h       |
| EPWM27_G3     | 500D B022h       |
| EPWM28_G0     | 5001 C022h       |
| EPWM28_G1     | 5005 C022h       |
| EPWM28_G2     | 5009 C022h       |
| EPWM28_G3     | 500D C022h       |
| EPWM29_G0     | 5001 D022h       |
| EPWM29_G1     | 5005 D022h       |
| EPWM29_G2     | 5009 D022h       |
| EPWM29_G3     | 500D D022h       |
| EPWM30_G0     | 5001 E022h       |
| EPWM30_G1     | 5005 E022h       |
| EPWM30_G2     | 5009 E022h       |
| EPWM30_G3     | 500D E022h       |
| EPWM31_G0     | 5001 F022h       |
| EPWM31_G1     | 5005 F022h       |
| EPWM31_G2     | 5009 F022h       |
| EPWM31_G3     | 500D F022h       |



**Figure 3-264. EPWM\_AQTSRCSEL Name Register**

|            |    |    |    |       |    |   |   |
|------------|----|----|----|-------|----|---|---|
| 15         | 14 | 13 | 12 | 11    | 10 | 9 | 8 |
| RESERVED_1 |    |    |    |       |    |   |   |
| R          |    |    |    |       |    |   |   |
| 0h         |    |    |    |       |    |   |   |
| 7          | 6  | 5  | 4  | 3     | 2  | 1 | 0 |
| T2SEL      |    |    |    | T1SEL |    |   |   |
| R/W        |    |    |    | R/W   |    |   |   |
| 0h         |    |    |    | 0h    |    |   |   |

**Table 3-852. EPWM\_AQTSRCSEL Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                              |
|------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                 |
| 7:4  | T2SEL      | R/W  | 0h    | T2 Event Source Select Bits<br>0000 DCAEVT1<br>0001 DCAEVT2<br>0010 DCBEVT1<br>0011 DCBEVT2<br>0100 TZ1<br>0101 TZ2<br>0110 TZ3<br>0111 EPWMxSYNCl<br>1000 DCEVTFILT<br>Others: Reserved |
| 3:0  | T1SEL      | R/W  | 0h    | T1 Event Source Select Bits<br>0000 DCAEVT1<br>0001 DCAEVT2<br>0010 DCBEVT1<br>0011 DCBEVT2<br>0100 TZ1<br>0101 TZ2<br>0110 TZ3<br>0111 EPWMxSYNCl<br>1000 DCEVTFILT<br>Others: Reserved |

### 3.7.2.14 EPWM\_PCCTL Register

#### 1 EPWM\_PCCTL Register (Offset = 28h) [reset = 0h]

PWM Chopper Control Register.

Return to [Summary Table](#)

**Table 3-853. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0028h       |
| EPWM0_G1      | 5004 0028h       |
| EPWM0_G2      | 5008 0028h       |
| EPWM0_G3      | 500C 0028h       |
| EPWM1_G0      | 5000 1028h       |
| EPWM1_G1      | 5004 1028h       |
| EPWM1_G2      | 5008 1028h       |
| EPWM1_G3      | 500C 1028h       |
| EPWM2_G0      | 5000 2028h       |
| EPWM2_G1      | 5004 2028h       |
| EPWM2_G2      | 5008 2028h       |
| EPWM2_G3      | 500C 2028h       |
| EPWM3_G0      | 5000 3028h       |
| EPWM3_G1      | 5004 3028h       |
| EPWM3_G2      | 5008 3028h       |
| EPWM3_G3      | 500C 3028h       |
| EPWM4_G0      | 5000 4028h       |
| EPWM4_G1      | 5004 4028h       |
| EPWM4_G2      | 5008 4028h       |
| EPWM4_G3      | 500C 4028h       |
| EPWM5_G0      | 5000 5028h       |
| EPWM5_G1      | 5004 5028h       |
| EPWM5_G2      | 5008 5028h       |
| EPWM5_G3      | 500C 5028h       |
| EPWM6_G0      | 5000 6028h       |
| EPWM6_G1      | 5004 6028h       |
| EPWM6_G2      | 5008 6028h       |
| EPWM6_G3      | 500C 6028h       |
| EPWM7_G0      | 5000 7028h       |
| EPWM7_G1      | 5004 7028h       |
| EPWM7_G2      | 5008 7028h       |
| EPWM7_G3      | 500C 7028h       |
| EPWM8_G0      | 5000 8028h       |
| EPWM8_G1      | 5004 8028h       |
| EPWM8_G2      | 5008 8028h       |
| EPWM8_G3      | 500C 8028h       |
| EPWM9_G0      | 5000 9028h       |
| EPWM9_G1      | 5004 9028h       |
| EPWM9_G2      | 5008 9028h       |

**Table 3-853. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9028h       |
| EPWM10_G0     | 5000 A028h       |
| EPWM10_G1     | 5004 A028h       |
| EPWM10_G2     | 5008 A028h       |
| EPWM10_G3     | 500C A028h       |
| EPWM11_G0     | 5000 B028h       |
| EPWM11_G1     | 5004 B028h       |
| EPWM11_G2     | 5008 B028h       |
| EPWM11_G3     | 500C B028h       |
| EPWM12_G0     | 5000 C028h       |
| EPWM12_G1     | 5004 C028h       |
| EPWM12_G2     | 5008 C028h       |
| EPWM12_G3     | 500C C028h       |
| EPWM13_G0     | 5000 D028h       |
| EPWM13_G1     | 5004 D028h       |
| EPWM13_G2     | 5008 D028h       |
| EPWM13_G3     | 500C D028h       |
| EPWM14_G0     | 5000 E028h       |
| EPWM14_G1     | 5004 E028h       |
| EPWM14_G2     | 5008 E028h       |
| EPWM14_G3     | 500C E028h       |
| EPWM15_G0     | 5000 F028h       |
| EPWM15_G1     | 5004 F028h       |
| EPWM15_G2     | 5008 F028h       |
| EPWM15_G3     | 500C F028h       |
| EPWM16_G0     | 5001 0028h       |
| EPWM16_G1     | 5005 0028h       |
| EPWM16_G2     | 5009 0028h       |
| EPWM16_G3     | 500D 0028h       |
| EPWM17_G0     | 5001 1028h       |
| EPWM17_G1     | 5005 1028h       |
| EPWM17_G2     | 5009 1028h       |
| EPWM17_G3     | 500D 1028h       |
| EPWM18_G0     | 5001 2028h       |
| EPWM18_G1     | 5005 2028h       |
| EPWM18_G2     | 5009 2028h       |
| EPWM18_G3     | 500D 2028h       |
| EPWM19_G0     | 5001 3028h       |
| EPWM19_G1     | 5005 3028h       |
| EPWM19_G2     | 5009 3028h       |
| EPWM19_G3     | 500D 3028h       |
| EPWM20_G0     | 5001 4028h       |
| EPWM20_G1     | 5005 4028h       |
| EPWM20_G2     | 5009 4028h       |
| EPWM20_G3     | 500D 4028h       |

**Table 3-853. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5028h       |
| EPWM21_G1     | 5005 5028h       |
| EPWM21_G2     | 5009 5028h       |
| EPWM21_G3     | 500D 5028h       |
| EPWM22_G0     | 5001 6028h       |
| EPWM22_G1     | 5005 6028h       |
| EPWM22_G2     | 5009 6028h       |
| EPWM22_G3     | 500D 6028h       |
| EPWM23_G0     | 5001 7028h       |
| EPWM23_G1     | 5005 7028h       |
| EPWM23_G2     | 5009 7028h       |
| EPWM23_G3     | 500D 7028h       |
| EPWM24_G0     | 5001 8028h       |
| EPWM24_G1     | 5005 8028h       |
| EPWM24_G2     | 5009 8028h       |
| EPWM24_G3     | 500D 8028h       |
| EPWM25_G0     | 5001 9028h       |
| EPWM25_G1     | 5005 9028h       |
| EPWM25_G2     | 5009 9028h       |
| EPWM25_G3     | 500D 9028h       |
| EPWM26_G0     | 5001 A028h       |
| EPWM26_G1     | 5005 A028h       |
| EPWM26_G2     | 5009 A028h       |
| EPWM26_G3     | 500D A028h       |
| EPWM27_G0     | 5001 B028h       |
| EPWM27_G1     | 5005 B028h       |
| EPWM27_G2     | 5009 B028h       |
| EPWM27_G3     | 500D B028h       |
| EPWM28_G0     | 5001 C028h       |
| EPWM28_G1     | 5005 C028h       |
| EPWM28_G2     | 5009 C028h       |
| EPWM28_G3     | 500D C028h       |
| EPWM29_G0     | 5001 D028h       |
| EPWM29_G1     | 5005 D028h       |
| EPWM29_G2     | 5009 D028h       |
| EPWM29_G3     | 500D D028h       |
| EPWM30_G0     | 5001 E028h       |
| EPWM30_G1     | 5005 E028h       |
| EPWM30_G2     | 5009 E028h       |
| EPWM30_G3     | 500D E028h       |
| EPWM31_G0     | 5001 F028h       |
| EPWM31_G1     | 5005 F028h       |
| EPWM31_G2     | 5009 F028h       |
| EPWM31_G3     | 500D F028h       |

**Figure 3-265. EPWM\_PCCTL Name Register**

| 15         | 14 | 13 | 12      | 11 | 10 | 9       | 8 |
|------------|----|----|---------|----|----|---------|---|
| RESERVED_1 |    |    |         |    |    | CHPDUTY |   |
| R          |    |    |         |    |    | R/W     |   |
| 0h         |    |    |         |    |    | 0h      |   |
| 7          | 6  | 5  | 4       | 3  | 2  | 1       | 0 |
| CHPFREQ    |    |    | OSHTWTH |    |    | CHPEN   |   |
| R/W        |    |    | R/W     |    |    | R/W     |   |
| 0h         |    |    | 0h      |    |    | 0h      |   |

**Table 3-855. EPWM\_PCCTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 10:8  | CHPDUTY    | R/W  | 0h    | Chopping Clock Duty Cycle<br>000:Duty = 1/8 [12.5%]<br>001:Duty = 2/8 [25.0%]<br>010:Duty = 3/8 [37.5%]<br>011:Duty = 4/8 [50.0%]<br>100:Duty = 5/8 [62.5%]<br>101:Duty = 6/8 [75.0%]<br>110:Duty = 7/8 [87.5%]<br>111:Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 7:5   | CHPFREQ    | R/W  | 0h    | Chopping Clock Frequency<br>000:Divide by 1 [no prescale, = 12.5 MHz at 100 MHz TBCLK]<br>001:Divide by 2 [6.25 MHz at 100 MHz TBCLK]<br>010:Divide by 3 [4.16 MHz at 100 MHz TBCLK]<br>011:Divide by 4 [3.12 MHz at 100 MHz TBCLK]<br>100:Divide by 5 [2.50 MHz at 100 MHz TBCLK]<br>101:Divide by 6 [2.08 MHz at 100 MHz TBCLK]<br>110:Divide by 7 [1.78 MHz at 100 MHz TBCLK]<br>111:Divide by 8 [1.56 MHz at 100 MHz TBCLK]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 4:1   | OSHTWTH    | R/W  | 0h    | One-Shot Pulse Width<br>0000 1 x EPWMCLK / 8 wide [ = 80 ns at 100 MHz EPWMCLK]<br>0001 2 x EPWMCLK / 8 wide [ = 160 ns at 100 MHz EPWMCLK]<br>0010 3 x EPWMCLK / 8 wide [ = 240 ns at 100 MHz EPWMCLK]<br>0011 4 x EPWMCLK / 8 wide [ = 320 ns at 100 MHz EPWMCLK]<br>0100 5 x EPWMCLK / 8 wide [ = 400 ns at 100 MHz EPWMCLK]<br>0101 6 x EPWMCLK / 8 wide [ = 480 ns at 100 MHz EPWMCLK]<br>0110 7 x EPWMCLK / 8 wide [ = 560 ns at 100 MHz EPWMCLK]<br>0111 8 x EPWMCLK / 8 wide [ = 640 ns at 100 MHz EPWMCLK]<br>1000 9 x EPWMCLK / 8 wide [ = 720 ns at 100 MHz EPWMCLK]<br>1001 10 x EPWMCLK / 8 wide [ = 800 ns at 100 MHz EPWMCLK]<br>1010 11 x EPWMCLK / 8 wide [ = 880 ns at 100 MHz EPWMCLK]<br>1011 12 x EPWMCLK / 8 wide [ = 960 ns at 100 MHz EPWMCLK]<br>1100 13 x EPWMCLK / 8 wide [ =<br>1040ns at 100 MHz EPWMCLK]<br>1101 14 x EPWMCLK / 8 wide [ =<br>1120ns at 100 MHz EPWMCLK]<br>1110 15 x EPWMCLK / 8 wide [ =<br>1200ns at 100 MHz EPWMCLK]<br>1111 16 x EPWMCLK / 8 wide [ =<br>1280ns at 100 MHz EPWMCLK] |
| 0     | CHPEN      | R/W  | 0h    | PWM-Chopping Enable<br>0:Disable [bypass] PWM chopping function<br>1:Enable chopping function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

### 3.7.2.15 EPWM\_VCAPCTL Register

#### 1 EPWM\_VCAPCTL Register (Offset = 30h) [reset = 0h]

Valley Capture Control Register.

Return to [Summary Table](#)

**Table 3-856. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0030h       |
| EPWM0_G1      | 5004 0030h       |
| EPWM0_G2      | 5008 0030h       |
| EPWM0_G3      | 500C 0030h       |
| EPWM1_G0      | 5000 1030h       |
| EPWM1_G1      | 5004 1030h       |
| EPWM1_G2      | 5008 1030h       |
| EPWM1_G3      | 500C 1030h       |
| EPWM2_G0      | 5000 2030h       |
| EPWM2_G1      | 5004 2030h       |
| EPWM2_G2      | 5008 2030h       |
| EPWM2_G3      | 500C 2030h       |
| EPWM3_G0      | 5000 3030h       |
| EPWM3_G1      | 5004 3030h       |
| EPWM3_G2      | 5008 3030h       |
| EPWM3_G3      | 500C 3030h       |
| EPWM4_G0      | 5000 4030h       |
| EPWM4_G1      | 5004 4030h       |
| EPWM4_G2      | 5008 4030h       |
| EPWM4_G3      | 500C 4030h       |
| EPWM5_G0      | 5000 5030h       |
| EPWM5_G1      | 5004 5030h       |
| EPWM5_G2      | 5008 5030h       |
| EPWM5_G3      | 500C 5030h       |
| EPWM6_G0      | 5000 6030h       |
| EPWM6_G1      | 5004 6030h       |
| EPWM6_G2      | 5008 6030h       |
| EPWM6_G3      | 500C 6030h       |
| EPWM7_G0      | 5000 7030h       |
| EPWM7_G1      | 5004 7030h       |
| EPWM7_G2      | 5008 7030h       |
| EPWM7_G3      | 500C 7030h       |
| EPWM8_G0      | 5000 8030h       |
| EPWM8_G1      | 5004 8030h       |
| EPWM8_G2      | 5008 8030h       |
| EPWM8_G3      | 500C 8030h       |
| EPWM9_G0      | 5000 9030h       |
| EPWM9_G1      | 5004 9030h       |
| EPWM9_G2      | 5008 9030h       |

**Table 3-856. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9030h       |
| EPWM10_G0     | 5000 A030h       |
| EPWM10_G1     | 5004 A030h       |
| EPWM10_G2     | 5008 A030h       |
| EPWM10_G3     | 500C A030h       |
| EPWM11_G0     | 5000 B030h       |
| EPWM11_G1     | 5004 B030h       |
| EPWM11_G2     | 5008 B030h       |
| EPWM11_G3     | 500C B030h       |
| EPWM12_G0     | 5000 C030h       |
| EPWM12_G1     | 5004 C030h       |
| EPWM12_G2     | 5008 C030h       |
| EPWM12_G3     | 500C C030h       |
| EPWM13_G0     | 5000 D030h       |
| EPWM13_G1     | 5004 D030h       |
| EPWM13_G2     | 5008 D030h       |
| EPWM13_G3     | 500C D030h       |
| EPWM14_G0     | 5000 E030h       |
| EPWM14_G1     | 5004 E030h       |
| EPWM14_G2     | 5008 E030h       |
| EPWM14_G3     | 500C E030h       |
| EPWM15_G0     | 5000 F030h       |
| EPWM15_G1     | 5004 F030h       |
| EPWM15_G2     | 5008 F030h       |
| EPWM15_G3     | 500C F030h       |
| EPWM16_G0     | 5001 0030h       |
| EPWM16_G1     | 5005 0030h       |
| EPWM16_G2     | 5009 0030h       |
| EPWM16_G3     | 500D 0030h       |
| EPWM17_G0     | 5001 1030h       |
| EPWM17_G1     | 5005 1030h       |
| EPWM17_G2     | 5009 1030h       |
| EPWM17_G3     | 500D 1030h       |
| EPWM18_G0     | 5001 2030h       |
| EPWM18_G1     | 5005 2030h       |
| EPWM18_G2     | 5009 2030h       |
| EPWM18_G3     | 500D 2030h       |
| EPWM19_G0     | 5001 3030h       |
| EPWM19_G1     | 5005 3030h       |
| EPWM19_G2     | 5009 3030h       |
| EPWM19_G3     | 500D 3030h       |
| EPWM20_G0     | 5001 4030h       |
| EPWM20_G1     | 5005 4030h       |
| EPWM20_G2     | 5009 4030h       |
| EPWM20_G3     | 500D 4030h       |

**Table 3-856. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5030h       |
| EPWM21_G1     | 5005 5030h       |
| EPWM21_G2     | 5009 5030h       |
| EPWM21_G3     | 500D 5030h       |
| EPWM22_G0     | 5001 6030h       |
| EPWM22_G1     | 5005 6030h       |
| EPWM22_G2     | 5009 6030h       |
| EPWM22_G3     | 500D 6030h       |
| EPWM23_G0     | 5001 7030h       |
| EPWM23_G1     | 5005 7030h       |
| EPWM23_G2     | 5009 7030h       |
| EPWM23_G3     | 500D 7030h       |
| EPWM24_G0     | 5001 8030h       |
| EPWM24_G1     | 5005 8030h       |
| EPWM24_G2     | 5009 8030h       |
| EPWM24_G3     | 500D 8030h       |
| EPWM25_G0     | 5001 9030h       |
| EPWM25_G1     | 5005 9030h       |
| EPWM25_G2     | 5009 9030h       |
| EPWM25_G3     | 500D 9030h       |
| EPWM26_G0     | 5001 A030h       |
| EPWM26_G1     | 5005 A030h       |
| EPWM26_G2     | 5009 A030h       |
| EPWM26_G3     | 500D A030h       |
| EPWM27_G0     | 5001 B030h       |
| EPWM27_G1     | 5005 B030h       |
| EPWM27_G2     | 5009 B030h       |
| EPWM27_G3     | 500D B030h       |
| EPWM28_G0     | 5001 C030h       |
| EPWM28_G1     | 5005 C030h       |
| EPWM28_G2     | 5009 C030h       |
| EPWM28_G3     | 500D C030h       |
| EPWM29_G0     | 5001 D030h       |
| EPWM29_G1     | 5005 D030h       |
| EPWM29_G2     | 5009 D030h       |
| EPWM29_G3     | 500D D030h       |
| EPWM30_G0     | 5001 E030h       |
| EPWM30_G1     | 5005 E030h       |
| EPWM30_G2     | 5009 E030h       |
| EPWM30_G3     | 500D E030h       |
| EPWM31_G0     | 5001 F030h       |
| EPWM31_G1     | 5005 F030h       |
| EPWM31_G2     | 5009 F030h       |
| EPWM31_G3     | 500D F030h       |



**Figure 3-266. EPWM\_VCAPCTL Name Register**

| 15         | 14         | 13 | 12      | 11 | 10 | 9                  | 8         |
|------------|------------|----|---------|----|----|--------------------|-----------|
| RESERVED_2 |            |    |         |    |    | EDGEFILTDLY<br>SEL | VDELAYDIV |
| R          |            |    |         |    |    | R/W                | R/W       |
| 0h         |            |    |         |    |    | 0h                 | 0h        |
| 7          | 6          | 5  | 4       | 3  | 2  | 1                  | 0         |
| VDELAYDIV  | RESERVED_1 |    | TRIGSEL |    |    | VCAPSTART          | VCAPE     |
| R/W        | R          |    | R/W     |    |    | R/W1TS             | R/W       |
| 0h         | 0h         |    | 0h      |    |    | 0h                 | 0h        |

**Table 3-858. EPWM\_VCAPCTL Register Field Descriptions**

| Bit   | Field          | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|----------------|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | RESERVED_2     | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 10    | EDGEFILTDLYSEL | R/W    | 0h    | Valley Switching Mode Delay Selection<br>0:No delay applied to the edge filter output<br>1:HWDELAYVAL delay applied to the edge filter output                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 9:7   | VDELAYDIV      | R/W    | 0h    | Valley Delay Mode Divide Enable<br>000:HWVDELVAL = SWVDELVAL<br>001:HWVDELVAL = VCNTVAL+SWVDELVAL<br>010:HWVDELVAL = VCNTVAL>>1+SWVDELVAL<br>011:HWVDELVAL = VCNTVAL>>2+SWVDELVAL<br>100:HWVDELVAL = VCNTVAL>>4+SWVDELVAL<br>Note: Delay value between the consecutive edge captures can optionally be divided by using these bits.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 6:5   | RESERVED_1     | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 4:2   | TRIGSEL        | R/W    | 0h    | Status of Numbered of Captured Events<br>000:Capture sequence is triggered by software via writes to VCAPCTL[VCAPSTART].<br>001:Capture sequence is triggered by CNT_zero event.<br>010:Capture sequence is triggered by PRD_eq event.<br>011:Capture sequence is triggered by CNT_zero or PRD_eq event.<br>100:Capture sequence is triggered by DCAEVT1 event.<br>101:Capture sequence is triggered by DCAEVT2 event.<br>110:Capture sequence is triggered by DCBEVT1 event.<br>111:Capture sequence is triggered by DCBEVT2 event.<br>Note: Valley capture sequence triggered by the selected event in this register field. Once the chosen event occurs the capture sequence is armed. Event captures occur based of the event chosen in DCFCTL[SRCSEL] register.<br>Note: Same event may not be chosen in both DCFCTL[SRCSEL] and VCAPCTL[TRIGSEL] registers.<br>Note: Once the chosen event in VCAPCTL[TRIGSEL] occurs, irrespective of the current capture status, capture sequence is retrigged. |
| 1     | VCAPSTART      | R/W1TS | 0h    | Valley Capture Start<br>0:Writing a 0 has no effect<br>1:Trigger the capture sequence once if VCAPCTL[TRIGSEL]=0x0<br>Note: This bit is used to start valley capture sequence through software. VCAPCTL[TRIGSEL] has to be chosen for software trigger for this bit to have any effect. Writing of 1 will result in one capture sequence trigger.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 0     | VCAPE          | R/W    | 0h    | Valley Capture Enable/Disable<br>0:Disabled<br>1:Enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

### 3.7.2.16 EPWM\_VCNTCFG Register

#### 1 EPWM\_VCNTCFG Register (Offset = 32h) [reset = 0h]

Valley Counter Config Register.

Return to [Summary Table](#)

**Table 3-859. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0032h       |
| EPWM0_G1      | 5004 0032h       |
| EPWM0_G2      | 5008 0032h       |
| EPWM0_G3      | 500C 0032h       |
| EPWM1_G0      | 5000 1032h       |
| EPWM1_G1      | 5004 1032h       |
| EPWM1_G2      | 5008 1032h       |
| EPWM1_G3      | 500C 1032h       |
| EPWM2_G0      | 5000 2032h       |
| EPWM2_G1      | 5004 2032h       |
| EPWM2_G2      | 5008 2032h       |
| EPWM2_G3      | 500C 2032h       |
| EPWM3_G0      | 5000 3032h       |
| EPWM3_G1      | 5004 3032h       |
| EPWM3_G2      | 5008 3032h       |
| EPWM3_G3      | 500C 3032h       |
| EPWM4_G0      | 5000 4032h       |
| EPWM4_G1      | 5004 4032h       |
| EPWM4_G2      | 5008 4032h       |
| EPWM4_G3      | 500C 4032h       |
| EPWM5_G0      | 5000 5032h       |
| EPWM5_G1      | 5004 5032h       |
| EPWM5_G2      | 5008 5032h       |
| EPWM5_G3      | 500C 5032h       |
| EPWM6_G0      | 5000 6032h       |
| EPWM6_G1      | 5004 6032h       |
| EPWM6_G2      | 5008 6032h       |
| EPWM6_G3      | 500C 6032h       |
| EPWM7_G0      | 5000 7032h       |
| EPWM7_G1      | 5004 7032h       |
| EPWM7_G2      | 5008 7032h       |
| EPWM7_G3      | 500C 7032h       |
| EPWM8_G0      | 5000 8032h       |
| EPWM8_G1      | 5004 8032h       |
| EPWM8_G2      | 5008 8032h       |
| EPWM8_G3      | 500C 8032h       |
| EPWM9_G0      | 5000 9032h       |
| EPWM9_G1      | 5004 9032h       |
| EPWM9_G2      | 5008 9032h       |

**Table 3-859. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9032h       |
| EPWM10_G0     | 5000 A032h       |
| EPWM10_G1     | 5004 A032h       |
| EPWM10_G2     | 5008 A032h       |
| EPWM10_G3     | 500C A032h       |
| EPWM11_G0     | 5000 B032h       |
| EPWM11_G1     | 5004 B032h       |
| EPWM11_G2     | 5008 B032h       |
| EPWM11_G3     | 500C B032h       |
| EPWM12_G0     | 5000 C032h       |
| EPWM12_G1     | 5004 C032h       |
| EPWM12_G2     | 5008 C032h       |
| EPWM12_G3     | 500C C032h       |
| EPWM13_G0     | 5000 D032h       |
| EPWM13_G1     | 5004 D032h       |
| EPWM13_G2     | 5008 D032h       |
| EPWM13_G3     | 500C D032h       |
| EPWM14_G0     | 5000 E032h       |
| EPWM14_G1     | 5004 E032h       |
| EPWM14_G2     | 5008 E032h       |
| EPWM14_G3     | 500C E032h       |
| EPWM15_G0     | 5000 F032h       |
| EPWM15_G1     | 5004 F032h       |
| EPWM15_G2     | 5008 F032h       |
| EPWM15_G3     | 500C F032h       |
| EPWM16_G0     | 5001 0032h       |
| EPWM16_G1     | 5005 0032h       |
| EPWM16_G2     | 5009 0032h       |
| EPWM16_G3     | 500D 0032h       |
| EPWM17_G0     | 5001 1032h       |
| EPWM17_G1     | 5005 1032h       |
| EPWM17_G2     | 5009 1032h       |
| EPWM17_G3     | 500D 1032h       |
| EPWM18_G0     | 5001 2032h       |
| EPWM18_G1     | 5005 2032h       |
| EPWM18_G2     | 5009 2032h       |
| EPWM18_G3     | 500D 2032h       |
| EPWM19_G0     | 5001 3032h       |
| EPWM19_G1     | 5005 3032h       |
| EPWM19_G2     | 5009 3032h       |
| EPWM19_G3     | 500D 3032h       |
| EPWM20_G0     | 5001 4032h       |
| EPWM20_G1     | 5005 4032h       |
| EPWM20_G2     | 5009 4032h       |
| EPWM20_G3     | 500D 4032h       |

**Table 3-859. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5032h       |
| EPWM21_G1     | 5005 5032h       |
| EPWM21_G2     | 5009 5032h       |
| EPWM21_G3     | 500D 5032h       |
| EPWM22_G0     | 5001 6032h       |
| EPWM22_G1     | 5005 6032h       |
| EPWM22_G2     | 5009 6032h       |
| EPWM22_G3     | 500D 6032h       |
| EPWM23_G0     | 5001 7032h       |
| EPWM23_G1     | 5005 7032h       |
| EPWM23_G2     | 5009 7032h       |
| EPWM23_G3     | 500D 7032h       |
| EPWM24_G0     | 5001 8032h       |
| EPWM24_G1     | 5005 8032h       |
| EPWM24_G2     | 5009 8032h       |
| EPWM24_G3     | 500D 8032h       |
| EPWM25_G0     | 5001 9032h       |
| EPWM25_G1     | 5005 9032h       |
| EPWM25_G2     | 5009 9032h       |
| EPWM25_G3     | 500D 9032h       |
| EPWM26_G0     | 5001 A032h       |
| EPWM26_G1     | 5005 A032h       |
| EPWM26_G2     | 5009 A032h       |
| EPWM26_G3     | 500D A032h       |
| EPWM27_G0     | 5001 B032h       |
| EPWM27_G1     | 5005 B032h       |
| EPWM27_G2     | 5009 B032h       |
| EPWM27_G3     | 500D B032h       |
| EPWM28_G0     | 5001 C032h       |
| EPWM28_G1     | 5005 C032h       |
| EPWM28_G2     | 5009 C032h       |
| EPWM28_G3     | 500D C032h       |
| EPWM29_G0     | 5001 D032h       |
| EPWM29_G1     | 5005 D032h       |
| EPWM29_G2     | 5009 D032h       |
| EPWM29_G3     | 500D D032h       |
| EPWM30_G0     | 5001 E032h       |
| EPWM30_G1     | 5005 E032h       |
| EPWM30_G2     | 5009 E032h       |
| EPWM30_G3     | 500D E032h       |
| EPWM31_G0     | 5001 F032h       |
| EPWM31_G1     | 5005 F032h       |
| EPWM31_G2     | 5009 F032h       |
| EPWM31_G3     | 500D F032h       |

**Figure 3-267. EPWM\_VCNTCFG Name Register**

| 15           | 14         | 13 | 12 | 11 | 10        | 9 | 8 |
|--------------|------------|----|----|----|-----------|---|---|
| STOPEDGESTS  | RESERVED_2 |    |    |    | STOPEDGE  |   |   |
| R            | R          |    |    |    | R/W       |   |   |
| 0h           | 0h         |    |    |    | 0h        |   |   |
| 7            | 6          | 5  | 4  | 3  | 2         | 1 | 0 |
| STARTEDGESTS | RESERVED_1 |    |    |    | STARTEDGE |   |   |
| R            | R          |    |    |    | R/W       |   |   |
| 0h           | 0h         |    |    |    | 0h        |   |   |

**Table 3-861. EPWM\_VCNTCFG Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|--------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | STOPEDGESTS  | R    | 0h    | Stop Edge Status Bit<br>0:Stop edge has not occurred<br>1:Stop edge occurred<br>Note: This bit is set only after the trigger sequence is armed [upon occurrence of trigger pulse selected through VCAPCTL[TRIGSEL]] and STOPEDGE occurs.<br>Note:This bit is reset by the occurrence of the trigger pulse selected through VCAPCTL[TRIGSEL]                                                  |
| 14:12 | RESERVED_2   | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                     |
| 11:8  | STOPEDGE     | R/W  | 0h    | Counter Stop Edge Selection<br>Once the counter operation is armed, upon occurrence of trigger pulse selected through VCAPCTL[TRIGSEL] pulse - valley counter would stop counting upon the occurrence of chosen number of events thorough this bit field. Stop counting on occurrence of:<br>0000 Do not stop<br>0001<br>1st edge<br>0010 2nd edge<br>0011 3rd edge<br>...<br>1111 15th edge |
| 7     | STARTEDGESTS | R    | 0h    | Start Edge Status Bit<br>0:Start edge has not occurred<br>1:Start edge occurred<br>Note: This bit is set only after the trigger sequence is armed [upon occurrence of trigger pulse selected through VCAPCTL[TRIGSEL]] and STARTEDGE occurs.<br>Note:This bit is reset by the occurrence of the trigger pulse selected through VCAPCTL[TRIGSEL]                                              |
| 6:4   | RESERVED_1   | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                     |
| 3:0   | STARTEDGE    | R/W  | 0h    | Counter Start Edge Selection<br>Once the counter operation is armed, upon occurrence of trigger pulse selected through VCAPCTL[TRIGSEL] pulse - valley counter would start counting upon the occurrence of chosen number of events thorough this bit field. Start counting on occurrence of<br>0000 Do not start<br>0001 1st edge<br>0010 2nd edge<br>0011 3rd edge<br>...<br>1111 15th edge |

### 3.7.2.17 EPWM\_HRCNFG Register

#### 1 EPWM\_HRCNFG Register (Offset = 40h) [reset = 0h]

HRPWM Configuration Register

This register is only accessible on EPWM modules with HRPWM capabilities.

Return to [Summary Table](#)

**Table 3-862. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0040h       |
| EPWM0_G1      | 5004 0040h       |
| EPWM0_G2      | 5008 0040h       |
| EPWM0_G3      | 500C 0040h       |
| EPWM1_G0      | 5000 1040h       |
| EPWM1_G1      | 5004 1040h       |
| EPWM1_G2      | 5008 1040h       |
| EPWM1_G3      | 500C 1040h       |
| EPWM2_G0      | 5000 2040h       |
| EPWM2_G1      | 5004 2040h       |
| EPWM2_G2      | 5008 2040h       |
| EPWM2_G3      | 500C 2040h       |
| EPWM3_G0      | 5000 3040h       |
| EPWM3_G1      | 5004 3040h       |
| EPWM3_G2      | 5008 3040h       |
| EPWM3_G3      | 500C 3040h       |
| EPWM4_G0      | 5000 4040h       |
| EPWM4_G1      | 5004 4040h       |
| EPWM4_G2      | 5008 4040h       |
| EPWM4_G3      | 500C 4040h       |
| EPWM5_G0      | 5000 5040h       |
| EPWM5_G1      | 5004 5040h       |
| EPWM5_G2      | 5008 5040h       |
| EPWM5_G3      | 500C 5040h       |
| EPWM6_G0      | 5000 6040h       |
| EPWM6_G1      | 5004 6040h       |
| EPWM6_G2      | 5008 6040h       |
| EPWM6_G3      | 500C 6040h       |
| EPWM7_G0      | 5000 7040h       |
| EPWM7_G1      | 5004 7040h       |
| EPWM7_G2      | 5008 7040h       |
| EPWM7_G3      | 500C 7040h       |
| EPWM8_G0      | 5000 8040h       |
| EPWM8_G1      | 5004 8040h       |
| EPWM8_G2      | 5008 8040h       |
| EPWM8_G3      | 500C 8040h       |
| EPWM9_G0      | 5000 9040h       |
| EPWM9_G1      | 5004 9040h       |

**Table 3-862. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G2      | 5008 9040h       |
| EPWM9_G3      | 500C 9040h       |
| EPWM10_G0     | 5000 A040h       |
| EPWM10_G1     | 5004 A040h       |
| EPWM10_G2     | 5008 A040h       |
| EPWM10_G3     | 500C A040h       |
| EPWM11_G0     | 5000 B040h       |
| EPWM11_G1     | 5004 B040h       |
| EPWM11_G2     | 5008 B040h       |
| EPWM11_G3     | 500C B040h       |
| EPWM12_G0     | 5000 C040h       |
| EPWM12_G1     | 5004 C040h       |
| EPWM12_G2     | 5008 C040h       |
| EPWM12_G3     | 500C C040h       |
| EPWM13_G0     | 5000 D040h       |
| EPWM13_G1     | 5004 D040h       |
| EPWM13_G2     | 5008 D040h       |
| EPWM13_G3     | 500C D040h       |
| EPWM14_G0     | 5000 E040h       |
| EPWM14_G1     | 5004 E040h       |
| EPWM14_G2     | 5008 E040h       |
| EPWM14_G3     | 500C E040h       |
| EPWM15_G0     | 5000 F040h       |
| EPWM15_G1     | 5004 F040h       |
| EPWM15_G2     | 5008 F040h       |
| EPWM15_G3     | 500C F040h       |
| EPWM16_G0     | 5001 0040h       |
| EPWM16_G1     | 5005 0040h       |
| EPWM16_G2     | 5009 0040h       |
| EPWM16_G3     | 500D 0040h       |
| EPWM17_G0     | 5001 1040h       |
| EPWM17_G1     | 5005 1040h       |
| EPWM17_G2     | 5009 1040h       |
| EPWM17_G3     | 500D 1040h       |
| EPWM18_G0     | 5001 2040h       |
| EPWM18_G1     | 5005 2040h       |
| EPWM18_G2     | 5009 2040h       |
| EPWM18_G3     | 500D 2040h       |
| EPWM19_G0     | 5001 3040h       |
| EPWM19_G1     | 5005 3040h       |
| EPWM19_G2     | 5009 3040h       |
| EPWM19_G3     | 500D 3040h       |
| EPWM20_G0     | 5001 4040h       |
| EPWM20_G1     | 5005 4040h       |
| EPWM20_G2     | 5009 4040h       |

**Table 3-862. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM20_G3     | 500D 4040h       |
| EPWM21_G0     | 5001 5040h       |
| EPWM21_G1     | 5005 5040h       |
| EPWM21_G2     | 5009 5040h       |
| EPWM21_G3     | 500D 5040h       |
| EPWM22_G0     | 5001 6040h       |
| EPWM22_G1     | 5005 6040h       |
| EPWM22_G2     | 5009 6040h       |
| EPWM22_G3     | 500D 6040h       |
| EPWM23_G0     | 5001 7040h       |
| EPWM23_G1     | 5005 7040h       |
| EPWM23_G2     | 5009 7040h       |
| EPWM23_G3     | 500D 7040h       |
| EPWM24_G0     | 5001 8040h       |
| EPWM24_G1     | 5005 8040h       |
| EPWM24_G2     | 5009 8040h       |
| EPWM24_G3     | 500D 8040h       |
| EPWM25_G0     | 5001 9040h       |
| EPWM25_G1     | 5005 9040h       |
| EPWM25_G2     | 5009 9040h       |
| EPWM25_G3     | 500D 9040h       |
| EPWM26_G0     | 5001 A040h       |
| EPWM26_G1     | 5005 A040h       |
| EPWM26_G2     | 5009 A040h       |
| EPWM26_G3     | 500D A040h       |
| EPWM27_G0     | 5001 B040h       |
| EPWM27_G1     | 5005 B040h       |
| EPWM27_G2     | 5009 B040h       |
| EPWM27_G3     | 500D B040h       |
| EPWM28_G0     | 5001 C040h       |
| EPWM28_G1     | 5005 C040h       |
| EPWM28_G2     | 5009 C040h       |
| EPWM28_G3     | 500D C040h       |
| EPWM29_G0     | 5001 D040h       |
| EPWM29_G1     | 5005 D040h       |
| EPWM29_G2     | 5009 D040h       |
| EPWM29_G3     | 500D D040h       |
| EPWM30_G0     | 5001 E040h       |
| EPWM30_G1     | 5005 E040h       |
| EPWM30_G2     | 5009 E040h       |
| EPWM30_G3     | 500D E040h       |
| EPWM31_G0     | 5001 F040h       |
| EPWM31_G1     | 5005 F040h       |
| EPWM31_G2     | 5009 F040h       |



**Table 3-862. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM31_G3     | 500D F040h       |

**Figure 3-268. EPWM\_HRCNFG Name Register**

|         |          |            |         |    |          |          |   |
|---------|----------|------------|---------|----|----------|----------|---|
| 15      | 14       | 13         | 12      | 11 | 10       | 9        | 8 |
| LINESEL |          | RESERVED_1 | HRLOADB |    | CTLMODEB | EDGMODEB |   |
| R/W     |          | R          | R/W     |    | R/W      | R/W      |   |
| 0h      |          | 0h         | 0h      |    | 0h       | 0h       |   |
| 7       | 6        | 5          | 4       | 3  | 2        | 1        | 0 |
| SWAPAB  | AUTOCONV | SELOUTB    | HRLOAD  |    | CTLMODE  | EDGMODE  |   |
| R/W     | R/W      | R/W        | R/W     |    | R/W      | R/W      |   |
| 0h      | 0h       | 0h         | 0h      |    | 0h       | 0h       |   |

**Table 3-864. EPWM\_HRCNFG Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                               |
|-------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | LINESEL    | R/W  | 0h    | Delay Line Selection Bits: Selects which of the 4 delay lines for a particular EPWM/EPWM module to send to CALIN for calibration.                                                                                                                                                                                                                         |
| 13    | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                  |
| 12:11 | HRLOADB    | R/W  | 0h    | Shadow Mode Bit<br>Selects the time event that loads the CMPBHR shadow value into the active register.<br>00:Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000]<br>01:Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD]<br>10:Load on either CTR = Zero or CTR = PRD<br>11:Load on CMPB_EQ [Translator Event CMPB-3] |
| 10    | CTLMODEB   | R/W  | 0h    | Control Mode Bits<br>Selects the register [CMP/TBPRD or TBPHS] that controls the MEP:<br>0: CMPBHR[8] or TBPRDHR[8] Register controls the edge position [i.e., this is duty or period control mode]. [Default on Reset]<br>1: TBPHSHR[8] Register controls the edge position [i.e., this is phase control mode].                                          |
| 9:8   | EDGMODEB   | R/W  | 0h    | Edge Mode Bits<br>Selects the edge of the PWM that is controlled by the micro-edge position [MEP] logic:<br>00: HRPWM capability is disabled [default on reset]<br>01: MEP control of rising edge [CMPBHR]<br>10: MEP control of falling edge [CMPBHR]<br>11: MEP control of both edges [TBPHSHR or TBPRDHR]                                              |
| 7     | SWAPAB     | R/W  | 0h    | Swap EPWM A & B Output Signals<br>This bit enables the swapping of the A & B signal outputs. The selection is as follows:<br>0: EPWMxA and EPWMxB outputs are unchanged.<br>1: EPWMxA signal appears on EPWMxB output and EPWMxB signal appears on EPWMxA output.                                                                                         |

**Table 3-864. EPWM\_HRCNFG Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6   | AUTOCONV | R/W  | 0h    | Auto Convert Delay Line Value<br>Selects whether the fractional duty cycle/period/phase in the CMPAHR/TBPRDHR/TBPHSHR register is automatically scaled by the MEP scale factor in the HRMSTEP register or manually scaled by calculations in application software. The SFO library function automatically updates the HRMSTEP register with the appropriate MEP scale factor.<br>0:Automatic HRMSTEP scaling is disabled.<br>1:Automatic HRMSTEP scaling is enabled.<br>If application software is manually scaling the fractional duty cycle, or phase [i.e. software sets CMPAHR = [fraction[PWMduty * PWMperiod] * MEP Scale Factor]<<8 + 0x080 for duty cycle], then this mode must be disabled. |
| 5   | SELOUTB  | R/W  | 0h    | EPWMxB Output Select Bit<br>This bit selects which signal is output on the EPWMxB channel output.<br>The inversion will take the high resolution mode into account and the inverted signal will contain any high resolution modification. The inversion takes place as the last step in modifying the EPWMxB signal.<br>0:EPWMxB output is normal.<br>1:EPWMxB output is inverted version of EPWMxA signal.                                                                                                                                                                                                                                                                                          |
| 4:3 | HRLOAD   | R/W  | 0h    | Shadow Mode Bit<br>Selects the time event that loads the CMPAHR shadow value into the active register.<br>00:Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000]<br>01:Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD]<br>10:Load on either CTR = Zero or CTR = PRD<br>11:Load on CMPA_EQ [Translator Event CMPA-3]                                                                                                                                                                                                                                                                                                                                            |
| 2   | CTLMODE  | R/W  | 0h    | Control Mode Bits<br>Selects the register [CMP/TBPRD or TBPHS] that controls the MEP:<br>0:CMPAHR[8] or TBPRDHR[8] Register controls the edge position [i.e., this is duty or period control mode]. [Default on Reset]<br>1:TBPHSHR[8] Register controls the edge position [i.e., this is phase control mode].                                                                                                                                                                                                                                                                                                                                                                                       |
| 1:0 | EDGMODE  | R/W  | 0h    | Edge Mode Bits<br>Selects the edge of the PWM that is controlled by the micro-edge position [MEP] logic:<br>00:HRPWM capability is disabled [default on reset]<br>01:MEP control of rising edge [CMPAHR]<br>10:MEP control of falling edge [CMPAHR]<br>11:MEP control of both edges [TBPHSHR or TBPRDHR]                                                                                                                                                                                                                                                                                                                                                                                             |

### 3.7.2.18 EPWM\_HRCNFG2 Register

#### 1 EPWM\_HRCNFG2 Register (Offset = 4Eh) [reset = 0h]

HRPWM Configuration 2 Register

This register is only accessible on EPWM modules with HRPWM capabilities. Only 16 bit accesses are allowed for this register. Debugger access in 32 bit mode may display incorrect values.

Return to [Summary Table](#)

**Table 3-865. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 004Eh       |
| EPWM0_G1      | 5004 004Eh       |
| EPWM0_G2      | 5008 004Eh       |
| EPWM0_G3      | 500C 004Eh       |
| EPWM1_G0      | 5000 104Eh       |
| EPWM1_G1      | 5004 104Eh       |
| EPWM1_G2      | 5008 104Eh       |
| EPWM1_G3      | 500C 104Eh       |
| EPWM2_G0      | 5000 204Eh       |
| EPWM2_G1      | 5004 204Eh       |
| EPWM2_G2      | 5008 204Eh       |
| EPWM2_G3      | 500C 204Eh       |
| EPWM3_G0      | 5000 304Eh       |
| EPWM3_G1      | 5004 304Eh       |
| EPWM3_G2      | 5008 304Eh       |
| EPWM3_G3      | 500C 304Eh       |
| EPWM4_G0      | 5000 404Eh       |
| EPWM4_G1      | 5004 404Eh       |
| EPWM4_G2      | 5008 404Eh       |
| EPWM4_G3      | 500C 404Eh       |
| EPWM5_G0      | 5000 504Eh       |
| EPWM5_G1      | 5004 504Eh       |
| EPWM5_G2      | 5008 504Eh       |
| EPWM5_G3      | 500C 504Eh       |
| EPWM6_G0      | 5000 604Eh       |
| EPWM6_G1      | 5004 604Eh       |
| EPWM6_G2      | 5008 604Eh       |
| EPWM6_G3      | 500C 604Eh       |
| EPWM7_G0      | 5000 704Eh       |
| EPWM7_G1      | 5004 704Eh       |
| EPWM7_G2      | 5008 704Eh       |
| EPWM7_G3      | 500C 704Eh       |
| EPWM8_G0      | 5000 804Eh       |
| EPWM8_G1      | 5004 804Eh       |
| EPWM8_G2      | 5008 804Eh       |
| EPWM8_G3      | 500C 804Eh       |
| EPWM9_G0      | 5000 904Eh       |

**Table 3-865. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G1      | 5004 904Eh       |
| EPWM9_G2      | 5008 904Eh       |
| EPWM9_G3      | 500C 904Eh       |
| EPWM10_G0     | 5000 A04Eh       |
| EPWM10_G1     | 5004 A04Eh       |
| EPWM10_G2     | 5008 A04Eh       |
| EPWM10_G3     | 500C A04Eh       |
| EPWM11_G0     | 5000 B04Eh       |
| EPWM11_G1     | 5004 B04Eh       |
| EPWM11_G2     | 5008 B04Eh       |
| EPWM11_G3     | 500C B04Eh       |
| EPWM12_G0     | 5000 C04Eh       |
| EPWM12_G1     | 5004 C04Eh       |
| EPWM12_G2     | 5008 C04Eh       |
| EPWM12_G3     | 500C C04Eh       |
| EPWM13_G0     | 5000 D04Eh       |
| EPWM13_G1     | 5004 D04Eh       |
| EPWM13_G2     | 5008 D04Eh       |
| EPWM13_G3     | 500C D04Eh       |
| EPWM14_G0     | 5000 E04Eh       |
| EPWM14_G1     | 5004 E04Eh       |
| EPWM14_G2     | 5008 E04Eh       |
| EPWM14_G3     | 500C E04Eh       |
| EPWM15_G0     | 5000 F04Eh       |
| EPWM15_G1     | 5004 F04Eh       |
| EPWM15_G2     | 5008 F04Eh       |
| EPWM15_G3     | 500C F04Eh       |
| EPWM16_G0     | 5001 004Eh       |
| EPWM16_G1     | 5005 004Eh       |
| EPWM16_G2     | 5009 004Eh       |
| EPWM16_G3     | 500D 004Eh       |
| EPWM17_G0     | 5001 104Eh       |
| EPWM17_G1     | 5005 104Eh       |
| EPWM17_G2     | 5009 104Eh       |
| EPWM17_G3     | 500D 104Eh       |
| EPWM18_G0     | 5001 204Eh       |
| EPWM18_G1     | 5005 204Eh       |
| EPWM18_G2     | 5009 204Eh       |
| EPWM18_G3     | 500D 204Eh       |
| EPWM19_G0     | 5001 304Eh       |
| EPWM19_G1     | 5005 304Eh       |
| EPWM19_G2     | 5009 304Eh       |
| EPWM19_G3     | 500D 304Eh       |
| EPWM20_G0     | 5001 404Eh       |
| EPWM20_G1     | 5005 404Eh       |

**Table 3-865. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM20_G2     | 5009 404Eh       |
| EPWM20_G3     | 500D 404Eh       |
| EPWM21_G0     | 5001 504Eh       |
| EPWM21_G1     | 5005 504Eh       |
| EPWM21_G2     | 5009 504Eh       |
| EPWM21_G3     | 500D 504Eh       |
| EPWM22_G0     | 5001 604Eh       |
| EPWM22_G1     | 5005 604Eh       |
| EPWM22_G2     | 5009 604Eh       |
| EPWM22_G3     | 500D 604Eh       |
| EPWM23_G0     | 5001 704Eh       |
| EPWM23_G1     | 5005 704Eh       |
| EPWM23_G2     | 5009 704Eh       |
| EPWM23_G3     | 500D 704Eh       |
| EPWM24_G0     | 5001 804Eh       |
| EPWM24_G1     | 5005 804Eh       |
| EPWM24_G2     | 5009 804Eh       |
| EPWM24_G3     | 500D 804Eh       |
| EPWM25_G0     | 5001 904Eh       |
| EPWM25_G1     | 5005 904Eh       |
| EPWM25_G2     | 5009 904Eh       |
| EPWM25_G3     | 500D 904Eh       |
| EPWM26_G0     | 5001 A04Eh       |
| EPWM26_G1     | 5005 A04Eh       |
| EPWM26_G2     | 5009 A04Eh       |
| EPWM26_G3     | 500D A04Eh       |
| EPWM27_G0     | 5001 B04Eh       |
| EPWM27_G1     | 5005 B04Eh       |
| EPWM27_G2     | 5009 B04Eh       |
| EPWM27_G3     | 500D B04Eh       |
| EPWM28_G0     | 5001 C04Eh       |
| EPWM28_G1     | 5005 C04Eh       |
| EPWM28_G2     | 5009 C04Eh       |
| EPWM28_G3     | 500D C04Eh       |
| EPWM29_G0     | 5001 D04Eh       |
| EPWM29_G1     | 5005 D04Eh       |
| EPWM29_G2     | 5009 D04Eh       |
| EPWM29_G3     | 500D D04Eh       |
| EPWM30_G0     | 5001 E04Eh       |
| EPWM30_G1     | 5005 E04Eh       |
| EPWM30_G2     | 5009 E04Eh       |
| EPWM30_G3     | 500D E04Eh       |
| EPWM31_G0     | 5001 F04Eh       |
| EPWM31_G1     | 5005 F04Eh       |
| EPWM31_G2     | 5009 F04Eh       |

**Table 3-865. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM31_G3     | 500D F04Eh       |

**Figure 3-269. EPWM\_HRCNFG2 Name Register**

| 15         | 14        | 13           | 12 | 11           | 10 | 9         | 8 |
|------------|-----------|--------------|----|--------------|----|-----------|---|
| NOBYPASS   | DELOADFRC | RESERVED_1   |    |              |    |           |   |
| R/W        | R/W1TS    | R            |    |              |    |           |   |
| 0h         | 0h        | 0h           |    |              |    |           |   |
| 7          | 6         | 5            | 4  | 3            | 2  | 1         | 0 |
| RESERVED_1 |           | CTLMODEDBFED |    | CTLMODEDBRED |    | EDGMODEDB |   |
| R          |           | R/W          |    | R/W          |    | R/W       |   |
| 0h         |           | 0h           |    | 0h           |    | 0h        |   |

**Table 3-867. EPWM\_HRCNFG2 Register Field Descriptions**

| Bit  | Field        | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                           |
|------|--------------|--------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | NOBYPASS     | R/W    | 0h    | No Bypass Delay Line Update Bit: For internal test purposes, this bit disables the 1 SYSCLK cycle bypass before delay line is updated.                                                                                                                                                                                                                                |
| 14   | DELOADFRC    | R/W1TS | 0h    | Delay Line Load Software Force: For internal test purposes, software force generates a pulse which forces a delay line update [similar to PRD_eq/CNT_zero strobe].                                                                                                                                                                                                    |
| 13:6 | RESERVED_1   | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                              |
| 5:4  | CTLMODEDBFED | R/W    | 0h    | Shadow Mode Bit - selection should match DBCTL[LOADFEDMODE]<br>Selects the time event that loads the DBFEDHR shadow value into the active register.<br>00 Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000]<br>01 Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD]<br>10 Load on either CTR = Zero or CTR = PRD<br>11 Reserved |
| 3:2  | CTLMODEDBRED | R/W    | 0h    | Shadow Mode Bit - selection should match DBCTL[LOADREDMODE]<br>Selects the time event that loads the DBREDHR shadow value into the active register.<br>00 Load on CTR = Zero: Time-base counter equal to zero [TBCTR = 0x0000]<br>01 Load on CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD]<br>10 Load on either CTR = Zero or CTR = PRD<br>11 Reserved |
| 1:0  | EDGMODEDB    | R/W    | 0h    | Edge Mode Bits<br>Selects the edge of the PWM that is controlled by the micro-edge position [MEP] logic:<br>00 HRPWM capability is disabled [default on reset]<br>01 MEP control of rising edge [DBREDHR]<br>10 MEP control of falling edge [DBFEDHR]<br>11 MEP control of both edges [rising edge of DBREDHR or falling edge of DBFEDHR]                             |

### 3.7.2.19 EPWM\_HRPCTL Register

#### 1 EPWM\_HRPCTL Register (Offset = 5Ah) [reset = 0h]

High Resolution Period Control Register

This register is only accessible on EPWM modules with HRPWM capabilities.

Return to [Summary Table](#)

**Table 3-868. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 005Ah       |
| EPWM0_G1      | 5004 005Ah       |
| EPWM0_G2      | 5008 005Ah       |
| EPWM0_G3      | 500C 005Ah       |
| EPWM1_G0      | 5000 105Ah       |
| EPWM1_G1      | 5004 105Ah       |
| EPWM1_G2      | 5008 105Ah       |
| EPWM1_G3      | 500C 105Ah       |
| EPWM2_G0      | 5000 205Ah       |
| EPWM2_G1      | 5004 205Ah       |
| EPWM2_G2      | 5008 205Ah       |
| EPWM2_G3      | 500C 205Ah       |
| EPWM3_G0      | 5000 305Ah       |
| EPWM3_G1      | 5004 305Ah       |
| EPWM3_G2      | 5008 305Ah       |
| EPWM3_G3      | 500C 305Ah       |
| EPWM4_G0      | 5000 405Ah       |
| EPWM4_G1      | 5004 405Ah       |
| EPWM4_G2      | 5008 405Ah       |
| EPWM4_G3      | 500C 405Ah       |
| EPWM5_G0      | 5000 505Ah       |
| EPWM5_G1      | 5004 505Ah       |
| EPWM5_G2      | 5008 505Ah       |
| EPWM5_G3      | 500C 505Ah       |
| EPWM6_G0      | 5000 605Ah       |
| EPWM6_G1      | 5004 605Ah       |
| EPWM6_G2      | 5008 605Ah       |
| EPWM6_G3      | 500C 605Ah       |
| EPWM7_G0      | 5000 705Ah       |
| EPWM7_G1      | 5004 705Ah       |
| EPWM7_G2      | 5008 705Ah       |
| EPWM7_G3      | 500C 705Ah       |
| EPWM8_G0      | 5000 805Ah       |
| EPWM8_G1      | 5004 805Ah       |
| EPWM8_G2      | 5008 805Ah       |
| EPWM8_G3      | 500C 805Ah       |
| EPWM9_G0      | 5000 905Ah       |
| EPWM9_G1      | 5004 905Ah       |

**Table 3-868. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G2      | 5008 905Ah       |
| EPWM9_G3      | 500C 905Ah       |
| EPWM10_G0     | 5000 A05Ah       |
| EPWM10_G1     | 5004 A05Ah       |
| EPWM10_G2     | 5008 A05Ah       |
| EPWM10_G3     | 500C A05Ah       |
| EPWM11_G0     | 5000 B05Ah       |
| EPWM11_G1     | 5004 B05Ah       |
| EPWM11_G2     | 5008 B05Ah       |
| EPWM11_G3     | 500C B05Ah       |
| EPWM12_G0     | 5000 C05Ah       |
| EPWM12_G1     | 5004 C05Ah       |
| EPWM12_G2     | 5008 C05Ah       |
| EPWM12_G3     | 500C C05Ah       |
| EPWM13_G0     | 5000 D05Ah       |
| EPWM13_G1     | 5004 D05Ah       |
| EPWM13_G2     | 5008 D05Ah       |
| EPWM13_G3     | 500C D05Ah       |
| EPWM14_G0     | 5000 E05Ah       |
| EPWM14_G1     | 5004 E05Ah       |
| EPWM14_G2     | 5008 E05Ah       |
| EPWM14_G3     | 500C E05Ah       |
| EPWM15_G0     | 5000 F05Ah       |
| EPWM15_G1     | 5004 F05Ah       |
| EPWM15_G2     | 5008 F05Ah       |
| EPWM15_G3     | 500C F05Ah       |
| EPWM16_G0     | 5001 005Ah       |
| EPWM16_G1     | 5005 005Ah       |
| EPWM16_G2     | 5009 005Ah       |
| EPWM16_G3     | 500D 005Ah       |
| EPWM17_G0     | 5001 105Ah       |
| EPWM17_G1     | 5005 105Ah       |
| EPWM17_G2     | 5009 105Ah       |
| EPWM17_G3     | 500D 105Ah       |
| EPWM18_G0     | 5001 205Ah       |
| EPWM18_G1     | 5005 205Ah       |
| EPWM18_G2     | 5009 205Ah       |
| EPWM18_G3     | 500D 205Ah       |
| EPWM19_G0     | 5001 305Ah       |
| EPWM19_G1     | 5005 305Ah       |
| EPWM19_G2     | 5009 305Ah       |
| EPWM19_G3     | 500D 305Ah       |
| EPWM20_G0     | 5001 405Ah       |
| EPWM20_G1     | 5005 405Ah       |
| EPWM20_G2     | 5009 405Ah       |



**Table 3-868. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM20_G3     | 500D 405Ah       |
| EPWM21_G0     | 5001 505Ah       |
| EPWM21_G1     | 5005 505Ah       |
| EPWM21_G2     | 5009 505Ah       |
| EPWM21_G3     | 500D 505Ah       |
| EPWM22_G0     | 5001 605Ah       |
| EPWM22_G1     | 5005 605Ah       |
| EPWM22_G2     | 5009 605Ah       |
| EPWM22_G3     | 500D 605Ah       |
| EPWM23_G0     | 5001 705Ah       |
| EPWM23_G1     | 5005 705Ah       |
| EPWM23_G2     | 5009 705Ah       |
| EPWM23_G3     | 500D 705Ah       |
| EPWM24_G0     | 5001 805Ah       |
| EPWM24_G1     | 5005 805Ah       |
| EPWM24_G2     | 5009 805Ah       |
| EPWM24_G3     | 500D 805Ah       |
| EPWM25_G0     | 5001 905Ah       |
| EPWM25_G1     | 5005 905Ah       |
| EPWM25_G2     | 5009 905Ah       |
| EPWM25_G3     | 500D 905Ah       |
| EPWM26_G0     | 5001 A05Ah       |
| EPWM26_G1     | 5005 A05Ah       |
| EPWM26_G2     | 5009 A05Ah       |
| EPWM26_G3     | 500D A05Ah       |
| EPWM27_G0     | 5001 B05Ah       |
| EPWM27_G1     | 5005 B05Ah       |
| EPWM27_G2     | 5009 B05Ah       |
| EPWM27_G3     | 500D B05Ah       |
| EPWM28_G0     | 5001 C05Ah       |
| EPWM28_G1     | 5005 C05Ah       |
| EPWM28_G2     | 5009 C05Ah       |
| EPWM28_G3     | 500D C05Ah       |
| EPWM29_G0     | 5001 D05Ah       |
| EPWM29_G1     | 5005 D05Ah       |
| EPWM29_G2     | 5009 D05Ah       |
| EPWM29_G3     | 500D D05Ah       |
| EPWM30_G0     | 5001 E05Ah       |
| EPWM30_G1     | 5005 E05Ah       |
| EPWM30_G2     | 5009 E05Ah       |
| EPWM30_G3     | 500D E05Ah       |
| EPWM31_G0     | 5001 F05Ah       |
| EPWM31_G1     | 5005 F05Ah       |
| EPWM31_G2     | 5009 F05Ah       |

**Table 3-868. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM31_G3     | 500D F05Ah       |

**Figure 3-270. EPWM\_HRPCTL Name Register**

| 15         | 14          | 13 | 12 | 11       | 10           | 9          | 8    |
|------------|-------------|----|----|----------|--------------|------------|------|
| RESERVED_1 |             |    |    |          |              |            |      |
| R          |             |    |    |          |              |            |      |
| 0h         |             |    |    |          |              |            |      |
| 7          | 6           | 5  | 4  | 3        | 2            | 1          | 0    |
| RESERVED_1 | PWMSYNCSELX |    |    | HRPSYNCE | TBPHSHRLOADE | PWMSYNCSEL | HRPE |
| R          | R/W         |    |    | R/W      | R/W          | R/W        | R/W  |
| 0h         | 0h          |    |    | 0h       | 0h           | 0h         | 0h   |

**Table 3-870. EPWM\_HRPCTL Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|------|--------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:7 | RESERVED_1   | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 6:4  | PWMSYNCSELX  | R/W  | 0h    | Extended selection bits for EPWMSYNCPER<br>000:EPWMSYNCPER is defined by PWMSYNCSEL - > default condition [compatible with previous EPWM versions]<br>001:Reserved<br>010:Reserved<br>011:Reserved<br>100:CTR = CMPC, Count direction Up<br>101:CTR = CMPC, Count direction Down<br>110:CTR = CMPD, Count direction Up<br>111:CTR = CMPD, Count direction Down                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 3    | HRPSYNCE     | R/W  | 0h    | SYNC Enable Bit [TRSYNCE]/High Resolution Period SYNC Enable Bit [HRPSYNCE]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 2    | TBPHSHRLOADE | R/W  | 0h    | TBPHSHR Load Enable<br>This bit allows you to synchronize EPWM modules with a high-resolution phase on a SYNCIN, TBCTL[SWFSYNC] or digital compare event. This allows for multiple EPWM modules operating at the same frequency to be phase aligned with high-resolution.<br>0:Disables synchronization of high-resolution phase on a SYNCIN, TBCTL[SWFSYNC] or digital compare event:<br>1:Synchronize the high-resolution phase on a SYNCIN, TBCTL[SWFSYNC] or digital comparator synchronization event. The phase is synchronized using the contents of the high-resolution phase TBPHSHR register. The TBCTL[PHSEN] bit which enables the loading of the TBCTR register with TBPHS register value on a SYNCIN or TBCTL[SWFSYNC] event works independently. However, users need to enable this bit also if they want to control phase in conjunction with the high-resolution period feature. This bit and the TBCTL[PHSEN] bit must be set to 1 when high-resolution period is enabled for up-down count mode even if TBPHSHR = 0x0000. This bit does not need to be set when only high-resolution duty is enabled. |
| 1    | PWMSYNCSEL   | R/W  | 0h    | PWMSYNC Source Select Bit: This bit selects the source for the EPWMSYNCPER signal that goes to the CMPSS and GPDAC:<br>0 CTR = PRD: Time-base counter equal to period [TBCTR = TBPRD]<br>1 CTR = zero: Time-base counter equal to zero [TBCTR = 0x00]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

**Table 3-870. EPWM\_HRPCTL Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                       |
|-----|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | HRPE  | R/W  | 0h    | High Resolution Period Enable Bit<br>0:High resolution period feature disabled. In this mode the EPWM behaves as a Type 0 EPWM.<br>1:High resolution period enabled. In this mode the HRPWM module can control high-resolution of both the duty and frequency. When high-resolution period is enabled, TBCTL[CTRMODE] = 2'b01 [down-count mode] is not supported. |

### 3.7.2.20 EPWM\_TRREM Register

#### 1 EPWM\_TRREM Register (Offset = 5Ch) [reset = 0h]

HRPWM High Resolution Remainder Register

This register is only accessible on EPWM modules with HRPWM capabilities.

Return to [Summary Table](#)

**Table 3-871. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 005Ch       |
| EPWM0_G1      | 5004 005Ch       |
| EPWM0_G2      | 5008 005Ch       |
| EPWM0_G3      | 500C 005Ch       |
| EPWM1_G0      | 5000 105Ch       |
| EPWM1_G1      | 5004 105Ch       |
| EPWM1_G2      | 5008 105Ch       |
| EPWM1_G3      | 500C 105Ch       |
| EPWM2_G0      | 5000 205Ch       |
| EPWM2_G1      | 5004 205Ch       |
| EPWM2_G2      | 5008 205Ch       |
| EPWM2_G3      | 500C 205Ch       |
| EPWM3_G0      | 5000 305Ch       |
| EPWM3_G1      | 5004 305Ch       |
| EPWM3_G2      | 5008 305Ch       |
| EPWM3_G3      | 500C 305Ch       |
| EPWM4_G0      | 5000 405Ch       |
| EPWM4_G1      | 5004 405Ch       |
| EPWM4_G2      | 5008 405Ch       |
| EPWM4_G3      | 500C 405Ch       |
| EPWM5_G0      | 5000 505Ch       |
| EPWM5_G1      | 5004 505Ch       |
| EPWM5_G2      | 5008 505Ch       |
| EPWM5_G3      | 500C 505Ch       |
| EPWM6_G0      | 5000 605Ch       |
| EPWM6_G1      | 5004 605Ch       |
| EPWM6_G2      | 5008 605Ch       |
| EPWM6_G3      | 500C 605Ch       |
| EPWM7_G0      | 5000 705Ch       |
| EPWM7_G1      | 5004 705Ch       |
| EPWM7_G2      | 5008 705Ch       |
| EPWM7_G3      | 500C 705Ch       |
| EPWM8_G0      | 5000 805Ch       |
| EPWM8_G1      | 5004 805Ch       |
| EPWM8_G2      | 5008 805Ch       |
| EPWM8_G3      | 500C 805Ch       |
| EPWM9_G0      | 5000 905Ch       |
| EPWM9_G1      | 5004 905Ch       |

**Table 3-871. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G2      | 5008 905Ch       |
| EPWM9_G3      | 500C 905Ch       |
| EPWM10_G0     | 5000 A05Ch       |
| EPWM10_G1     | 5004 A05Ch       |
| EPWM10_G2     | 5008 A05Ch       |
| EPWM10_G3     | 500C A05Ch       |
| EPWM11_G0     | 5000 B05Ch       |
| EPWM11_G1     | 5004 B05Ch       |
| EPWM11_G2     | 5008 B05Ch       |
| EPWM11_G3     | 500C B05Ch       |
| EPWM12_G0     | 5000 C05Ch       |
| EPWM12_G1     | 5004 C05Ch       |
| EPWM12_G2     | 5008 C05Ch       |
| EPWM12_G3     | 500C C05Ch       |
| EPWM13_G0     | 5000 D05Ch       |
| EPWM13_G1     | 5004 D05Ch       |
| EPWM13_G2     | 5008 D05Ch       |
| EPWM13_G3     | 500C D05Ch       |
| EPWM14_G0     | 5000 E05Ch       |
| EPWM14_G1     | 5004 E05Ch       |
| EPWM14_G2     | 5008 E05Ch       |
| EPWM14_G3     | 500C E05Ch       |
| EPWM15_G0     | 5000 F05Ch       |
| EPWM15_G1     | 5004 F05Ch       |
| EPWM15_G2     | 5008 F05Ch       |
| EPWM15_G3     | 500C F05Ch       |
| EPWM16_G0     | 5001 005Ch       |
| EPWM16_G1     | 5005 005Ch       |
| EPWM16_G2     | 5009 005Ch       |
| EPWM16_G3     | 500D 005Ch       |
| EPWM17_G0     | 5001 105Ch       |
| EPWM17_G1     | 5005 105Ch       |
| EPWM17_G2     | 5009 105Ch       |
| EPWM17_G3     | 500D 105Ch       |
| EPWM18_G0     | 5001 205Ch       |
| EPWM18_G1     | 5005 205Ch       |
| EPWM18_G2     | 5009 205Ch       |
| EPWM18_G3     | 500D 205Ch       |
| EPWM19_G0     | 5001 305Ch       |
| EPWM19_G1     | 5005 305Ch       |
| EPWM19_G2     | 5009 305Ch       |
| EPWM19_G3     | 500D 305Ch       |
| EPWM20_G0     | 5001 405Ch       |
| EPWM20_G1     | 5005 405Ch       |
| EPWM20_G2     | 5009 405Ch       |

**Table 3-871. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM20_G3     | 500D 405Ch       |
| EPWM21_G0     | 5001 505Ch       |
| EPWM21_G1     | 5005 505Ch       |
| EPWM21_G2     | 5009 505Ch       |
| EPWM21_G3     | 500D 505Ch       |
| EPWM22_G0     | 5001 605Ch       |
| EPWM22_G1     | 5005 605Ch       |
| EPWM22_G2     | 5009 605Ch       |
| EPWM22_G3     | 500D 605Ch       |
| EPWM23_G0     | 5001 705Ch       |
| EPWM23_G1     | 5005 705Ch       |
| EPWM23_G2     | 5009 705Ch       |
| EPWM23_G3     | 500D 705Ch       |
| EPWM24_G0     | 5001 805Ch       |
| EPWM24_G1     | 5005 805Ch       |
| EPWM24_G2     | 5009 805Ch       |
| EPWM24_G3     | 500D 805Ch       |
| EPWM25_G0     | 5001 905Ch       |
| EPWM25_G1     | 5005 905Ch       |
| EPWM25_G2     | 5009 905Ch       |
| EPWM25_G3     | 500D 905Ch       |
| EPWM26_G0     | 5001 A05Ch       |
| EPWM26_G1     | 5005 A05Ch       |
| EPWM26_G2     | 5009 A05Ch       |
| EPWM26_G3     | 500D A05Ch       |
| EPWM27_G0     | 5001 B05Ch       |
| EPWM27_G1     | 5005 B05Ch       |
| EPWM27_G2     | 5009 B05Ch       |
| EPWM27_G3     | 500D B05Ch       |
| EPWM28_G0     | 5001 C05Ch       |
| EPWM28_G1     | 5005 C05Ch       |
| EPWM28_G2     | 5009 C05Ch       |
| EPWM28_G3     | 500D C05Ch       |
| EPWM29_G0     | 5001 D05Ch       |
| EPWM29_G1     | 5005 D05Ch       |
| EPWM29_G2     | 5009 D05Ch       |
| EPWM29_G3     | 500D D05Ch       |
| EPWM30_G0     | 5001 E05Ch       |
| EPWM30_G1     | 5005 E05Ch       |
| EPWM30_G2     | 5009 E05Ch       |
| EPWM30_G3     | 500D E05Ch       |
| EPWM31_G0     | 5001 F05Ch       |
| EPWM31_G1     | 5005 F05Ch       |
| EPWM31_G2     | 5009 F05Ch       |

**Table 3-871. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM31_G3     | 500D F05Ch       |

**Figure 3-271. EPWM\_TRREM Name Register**

|            |    |    |    |    |    |       |   |
|------------|----|----|----|----|----|-------|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9     | 8 |
| RESERVED_1 |    |    |    |    |    | TRREM |   |
| R          |    |    |    |    |    | R/W   |   |
| 0h         |    |    |    |    |    | 0h    |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1     | 0 |
| TRREM      |    |    |    |    |    |       |   |
| R/W        |    |    |    |    |    |       |   |
| 0h         |    |    |    |    |    |       |   |

**Table 3-873. EPWM\_TRREM Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 10:0  | TRREM      | R/W  | 0h    | <p>HRPWM Remainder Bits: This 11-bit value keeps track of the remainder portion of the HRPWM algorithm calculations. This value keeps track of the remainder portion of the HRPWM hardware calculations.</p> <p>Notes:</p> <ol style="list-style-type: none"> <li>The lower 8-bits of the TRREM register can be automatically initialized with the TBPHSHR value on a SYNCIN or TBCTL[SWFSYNC] event or DC event [if enabled]. The user can also write a value with the CPU.</li> <li>Priority of TRREM register updates:<br/>Sync [software or hardware] TBPHSHR copied to TRREM : Highest Priority<br/>HRPWM Hardware [updates TRREM register]: Next priority<br/>CPU Write To TRREM Register: Lowest Priority</li> <li>Bit 10 of TRREM register is not used in asymmetrical mode. This bit can be forced to zero.<br/>TRREM will be initialized to 0x0 and 0x100 in Up and Up-down modes respectively.</li> </ol> <p>Asymmetrical Mode:<br/>TRREM[7:0] = TBPHSHR[15:8]<br/>TRREM[10,9,8] = 3'b000</p> <p>Symmetrical Mode:<br/>TRREM[7:0] = TBPHSHR[15:8]<br/>TRREM[10,9,8] = 3'b001</p> |

### 3.7.2.21 EPWM\_GLDCTL Register

#### 1 EPWM\_GLDCTL Register (Offset = 68h) [reset = 0h]

Global PWM Load Control Register.

Return to [Summary Table](#)

**Table 3-874. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0068h       |
| EPWM0_G1      | 5004 0068h       |
| EPWM0_G2      | 5008 0068h       |
| EPWM0_G3      | 500C 0068h       |
| EPWM1_G0      | 5000 1068h       |
| EPWM1_G1      | 5004 1068h       |
| EPWM1_G2      | 5008 1068h       |
| EPWM1_G3      | 500C 1068h       |
| EPWM2_G0      | 5000 2068h       |
| EPWM2_G1      | 5004 2068h       |
| EPWM2_G2      | 5008 2068h       |
| EPWM2_G3      | 500C 2068h       |
| EPWM3_G0      | 5000 3068h       |
| EPWM3_G1      | 5004 3068h       |
| EPWM3_G2      | 5008 3068h       |
| EPWM3_G3      | 500C 3068h       |
| EPWM4_G0      | 5000 4068h       |
| EPWM4_G1      | 5004 4068h       |
| EPWM4_G2      | 5008 4068h       |
| EPWM4_G3      | 500C 4068h       |
| EPWM5_G0      | 5000 5068h       |
| EPWM5_G1      | 5004 5068h       |
| EPWM5_G2      | 5008 5068h       |
| EPWM5_G3      | 500C 5068h       |
| EPWM6_G0      | 5000 6068h       |
| EPWM6_G1      | 5004 6068h       |
| EPWM6_G2      | 5008 6068h       |
| EPWM6_G3      | 500C 6068h       |
| EPWM7_G0      | 5000 7068h       |
| EPWM7_G1      | 5004 7068h       |
| EPWM7_G2      | 5008 7068h       |
| EPWM7_G3      | 500C 7068h       |
| EPWM8_G0      | 5000 8068h       |
| EPWM8_G1      | 5004 8068h       |
| EPWM8_G2      | 5008 8068h       |
| EPWM8_G3      | 500C 8068h       |
| EPWM9_G0      | 5000 9068h       |
| EPWM9_G1      | 5004 9068h       |
| EPWM9_G2      | 5008 9068h       |



**Table 3-874. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9068h       |
| EPWM10_G0     | 5000 A068h       |
| EPWM10_G1     | 5004 A068h       |
| EPWM10_G2     | 5008 A068h       |
| EPWM10_G3     | 500C A068h       |
| EPWM11_G0     | 5000 B068h       |
| EPWM11_G1     | 5004 B068h       |
| EPWM11_G2     | 5008 B068h       |
| EPWM11_G3     | 500C B068h       |
| EPWM12_G0     | 5000 C068h       |
| EPWM12_G1     | 5004 C068h       |
| EPWM12_G2     | 5008 C068h       |
| EPWM12_G3     | 500C C068h       |
| EPWM13_G0     | 5000 D068h       |
| EPWM13_G1     | 5004 D068h       |
| EPWM13_G2     | 5008 D068h       |
| EPWM13_G3     | 500C D068h       |
| EPWM14_G0     | 5000 E068h       |
| EPWM14_G1     | 5004 E068h       |
| EPWM14_G2     | 5008 E068h       |
| EPWM14_G3     | 500C E068h       |
| EPWM15_G0     | 5000 F068h       |
| EPWM15_G1     | 5004 F068h       |
| EPWM15_G2     | 5008 F068h       |
| EPWM15_G3     | 500C F068h       |
| EPWM16_G0     | 5001 0068h       |
| EPWM16_G1     | 5005 0068h       |
| EPWM16_G2     | 5009 0068h       |
| EPWM16_G3     | 500D 0068h       |
| EPWM17_G0     | 5001 1068h       |
| EPWM17_G1     | 5005 1068h       |
| EPWM17_G2     | 5009 1068h       |
| EPWM17_G3     | 500D 1068h       |
| EPWM18_G0     | 5001 2068h       |
| EPWM18_G1     | 5005 2068h       |
| EPWM18_G2     | 5009 2068h       |
| EPWM18_G3     | 500D 2068h       |
| EPWM19_G0     | 5001 3068h       |
| EPWM19_G1     | 5005 3068h       |
| EPWM19_G2     | 5009 3068h       |
| EPWM19_G3     | 500D 3068h       |
| EPWM20_G0     | 5001 4068h       |
| EPWM20_G1     | 5005 4068h       |
| EPWM20_G2     | 5009 4068h       |
| EPWM20_G3     | 500D 4068h       |

**Table 3-874. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5068h       |
| EPWM21_G1     | 5005 5068h       |
| EPWM21_G2     | 5009 5068h       |
| EPWM21_G3     | 500D 5068h       |
| EPWM22_G0     | 5001 6068h       |
| EPWM22_G1     | 5005 6068h       |
| EPWM22_G2     | 5009 6068h       |
| EPWM22_G3     | 500D 6068h       |
| EPWM23_G0     | 5001 7068h       |
| EPWM23_G1     | 5005 7068h       |
| EPWM23_G2     | 5009 7068h       |
| EPWM23_G3     | 500D 7068h       |
| EPWM24_G0     | 5001 8068h       |
| EPWM24_G1     | 5005 8068h       |
| EPWM24_G2     | 5009 8068h       |
| EPWM24_G3     | 500D 8068h       |
| EPWM25_G0     | 5001 9068h       |
| EPWM25_G1     | 5005 9068h       |
| EPWM25_G2     | 5009 9068h       |
| EPWM25_G3     | 500D 9068h       |
| EPWM26_G0     | 5001 A068h       |
| EPWM26_G1     | 5005 A068h       |
| EPWM26_G2     | 5009 A068h       |
| EPWM26_G3     | 500D A068h       |
| EPWM27_G0     | 5001 B068h       |
| EPWM27_G1     | 5005 B068h       |
| EPWM27_G2     | 5009 B068h       |
| EPWM27_G3     | 500D B068h       |
| EPWM28_G0     | 5001 C068h       |
| EPWM28_G1     | 5005 C068h       |
| EPWM28_G2     | 5009 C068h       |
| EPWM28_G3     | 500D C068h       |
| EPWM29_G0     | 5001 D068h       |
| EPWM29_G1     | 5005 D068h       |
| EPWM29_G2     | 5009 D068h       |
| EPWM29_G3     | 500D D068h       |
| EPWM30_G0     | 5001 E068h       |
| EPWM30_G1     | 5005 E068h       |
| EPWM30_G2     | 5009 E068h       |
| EPWM30_G3     | 500D E068h       |
| EPWM31_G0     | 5001 F068h       |
| EPWM31_G1     | 5005 F068h       |
| EPWM31_G2     | 5009 F068h       |
| EPWM31_G3     | 500D F068h       |

**Figure 3-272. EPWM\_GLDCTL Name Register**

| 15         | 14         | 13       | 12      | 11 | 10 | 9      | 8 |
|------------|------------|----------|---------|----|----|--------|---|
| RESERVED_2 |            |          | GLDCNT  |    |    | GLDPRD |   |
| R          |            |          | R       |    |    | R/W    |   |
| 0h         |            |          | 0h      |    |    | 0h     |   |
| 7          | 6          | 5        | 4       | 3  | 2  | 1      | 0 |
| GLDPRD     | RESERVED_1 | OSHTMODE | GLDMODE |    |    | GLD    |   |
| R/W        | R          | R/W      | R/W     |    |    | R/W    |   |
| 0h         | 0h         | 0h       | 0h      |    |    | 0h     |   |

**Table 3-876. EPWM\_GLDCTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 12:10 | GLDCNT     | R    | 0h    | Global Load Strobe Counter Register<br>These bits indicate how many selected events have occurred:<br>000:No events<br>001:1 event<br>010:2 events<br>011:3 events<br>100:4 events<br>101:5 events<br>110:6 events<br>111:7 events                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 9:7   | GLDPRD     | R/W  | 0h    | Global Load Strobe Period Select Register<br>These bits select how many selected events need to occur before a load strobe is generated<br>000:Disable counter<br>001:Generate strobe on GLDCNT = 001 [1st event]<br>010:Generate strobe on GLDCNT = 010 [2nd event]<br>011:Generate strobe on GLDCNT = 011 [3rd event]<br>100:Generate strobe on GLDCNT = 011 [4th event]<br>101:Generate strobe on GLDCNT = 001 [5th event]<br>110:Generate strobe on GLDCNT = 010 [6th event]<br>111:Generate strobe on GLDCNT = 011 [7th event]                                                                                                                                                                                                                                          |
| 6     | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 5     | OSHTMODE   | R/W  | 0h    | One Shot Load Mode Control Bit<br>0:One shot load mode is disabled and shadow to active loading happens continuously on all the chosen load strobes.<br>1:One shot mode is active. All load strobes are blocked until GLDCTL2[OSHTLD] is written with 1.<br>Note: One Shot mode can only be used with global shadow to active load mode enabled [GLDCTL[GLD]=1]                                                                                                                                                                                                                                                                                                                                                                                                              |
| 4:1   | GLDMODE    | R/W  | 0h    | Global Load Pulse selection for Shadow to Active Mode Reloads<br>0000 Load on Counter = 0 [CNT_ZRO]<br>0001 Load on Counter = Period [PRD_EQ]<br>0010 Load on either Counter = 0, or Counter = Period<br>0011 Load on SYNCEVT - this is logical OR of DCAEVT1.sync, DCBEVT1.sync, EPWMxSYNCL and TBCTL[SWFSYNC]<br>0100 Load on SYNCEVT or CNT_ZRO<br>0101 Load on SYNCEVT or PRD_EQ<br>0110 Load on SYNCEVT or CNT_ZRO or PRD_EQ<br>1000 Load on Counter = CMPCU [CMPC_EQ counter incrementing]<br>1001 Load on Counter = CMPCD [CMPC_EQ counter decrementing]<br>1010 Load on Counter = CMPDU [CMPD_EQ counter incrementing]<br>1011 Load on Counter = CMPDD [CMPD_EQ counter decrementing]<br>1100 Reserved<br>...<br>1110 Reserved<br>1111 Load on GLDCTL2[GFRCLD] write |

**Table 3-876. EPWM\_GLDCTL Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | GLD   | R/W  | 0h    | Global Shadow to Active Load Event Control<br>0:Shadow to active reload for all shadowed registers happens as per the individual reload control bits specified [Compatible with previous EPWM versions].<br>1:When set, all the shadow to active reload events are defined by GLDMODE bits in GLDCTL register. All the shadow registers use same reload pulse from shadow to active reloading. Individual LOADMODE bits are ignored. |

### 3.7.2.22 EPWM\_GLDCFG Register

#### 1 EPWM\_GLDCFG Register (Offset = 6Ah) [reset = 0h]

Global PWM Load Config Register .

Return to [Summary Table](#)

**Table 3-877. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 006Ah       |
| EPWM0_G1      | 5004 006Ah       |
| EPWM0_G2      | 5008 006Ah       |
| EPWM0_G3      | 500C 006Ah       |
| EPWM1_G0      | 5000 106Ah       |
| EPWM1_G1      | 5004 106Ah       |
| EPWM1_G2      | 5008 106Ah       |
| EPWM1_G3      | 500C 106Ah       |
| EPWM2_G0      | 5000 206Ah       |
| EPWM2_G1      | 5004 206Ah       |
| EPWM2_G2      | 5008 206Ah       |
| EPWM2_G3      | 500C 206Ah       |
| EPWM3_G0      | 5000 306Ah       |
| EPWM3_G1      | 5004 306Ah       |
| EPWM3_G2      | 5008 306Ah       |
| EPWM3_G3      | 500C 306Ah       |
| EPWM4_G0      | 5000 406Ah       |
| EPWM4_G1      | 5004 406Ah       |
| EPWM4_G2      | 5008 406Ah       |
| EPWM4_G3      | 500C 406Ah       |
| EPWM5_G0      | 5000 506Ah       |
| EPWM5_G1      | 5004 506Ah       |
| EPWM5_G2      | 5008 506Ah       |
| EPWM5_G3      | 500C 506Ah       |
| EPWM6_G0      | 5000 606Ah       |
| EPWM6_G1      | 5004 606Ah       |
| EPWM6_G2      | 5008 606Ah       |
| EPWM6_G3      | 500C 606Ah       |
| EPWM7_G0      | 5000 706Ah       |
| EPWM7_G1      | 5004 706Ah       |
| EPWM7_G2      | 5008 706Ah       |
| EPWM7_G3      | 500C 706Ah       |
| EPWM8_G0      | 5000 806Ah       |
| EPWM8_G1      | 5004 806Ah       |
| EPWM8_G2      | 5008 806Ah       |
| EPWM8_G3      | 500C 806Ah       |
| EPWM9_G0      | 5000 906Ah       |
| EPWM9_G1      | 5004 906Ah       |
| EPWM9_G2      | 5008 906Ah       |

**Table 3-877. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 906Ah       |
| EPWM10_G0     | 5000 A06Ah       |
| EPWM10_G1     | 5004 A06Ah       |
| EPWM10_G2     | 5008 A06Ah       |
| EPWM10_G3     | 500C A06Ah       |
| EPWM11_G0     | 5000 B06Ah       |
| EPWM11_G1     | 5004 B06Ah       |
| EPWM11_G2     | 5008 B06Ah       |
| EPWM11_G3     | 500C B06Ah       |
| EPWM12_G0     | 5000 C06Ah       |
| EPWM12_G1     | 5004 C06Ah       |
| EPWM12_G2     | 5008 C06Ah       |
| EPWM12_G3     | 500C C06Ah       |
| EPWM13_G0     | 5000 D06Ah       |
| EPWM13_G1     | 5004 D06Ah       |
| EPWM13_G2     | 5008 D06Ah       |
| EPWM13_G3     | 500C D06Ah       |
| EPWM14_G0     | 5000 E06Ah       |
| EPWM14_G1     | 5004 E06Ah       |
| EPWM14_G2     | 5008 E06Ah       |
| EPWM14_G3     | 500C E06Ah       |
| EPWM15_G0     | 5000 F06Ah       |
| EPWM15_G1     | 5004 F06Ah       |
| EPWM15_G2     | 5008 F06Ah       |
| EPWM15_G3     | 500C F06Ah       |
| EPWM16_G0     | 5001 006Ah       |
| EPWM16_G1     | 5005 006Ah       |
| EPWM16_G2     | 5009 006Ah       |
| EPWM16_G3     | 500D 006Ah       |
| EPWM17_G0     | 5001 106Ah       |
| EPWM17_G1     | 5005 106Ah       |
| EPWM17_G2     | 5009 106Ah       |
| EPWM17_G3     | 500D 106Ah       |
| EPWM18_G0     | 5001 206Ah       |
| EPWM18_G1     | 5005 206Ah       |
| EPWM18_G2     | 5009 206Ah       |
| EPWM18_G3     | 500D 206Ah       |
| EPWM19_G0     | 5001 306Ah       |
| EPWM19_G1     | 5005 306Ah       |
| EPWM19_G2     | 5009 306Ah       |
| EPWM19_G3     | 500D 306Ah       |
| EPWM20_G0     | 5001 406Ah       |
| EPWM20_G1     | 5005 406Ah       |
| EPWM20_G2     | 5009 406Ah       |
| EPWM20_G3     | 500D 406Ah       |

**Table 3-877. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 506Ah       |
| EPWM21_G1     | 5005 506Ah       |
| EPWM21_G2     | 5009 506Ah       |
| EPWM21_G3     | 500D 506Ah       |
| EPWM22_G0     | 5001 606Ah       |
| EPWM22_G1     | 5005 606Ah       |
| EPWM22_G2     | 5009 606Ah       |
| EPWM22_G3     | 500D 606Ah       |
| EPWM23_G0     | 5001 706Ah       |
| EPWM23_G1     | 5005 706Ah       |
| EPWM23_G2     | 5009 706Ah       |
| EPWM23_G3     | 500D 706Ah       |
| EPWM24_G0     | 5001 806Ah       |
| EPWM24_G1     | 5005 806Ah       |
| EPWM24_G2     | 5009 806Ah       |
| EPWM24_G3     | 500D 806Ah       |
| EPWM25_G0     | 5001 906Ah       |
| EPWM25_G1     | 5005 906Ah       |
| EPWM25_G2     | 5009 906Ah       |
| EPWM25_G3     | 500D 906Ah       |
| EPWM26_G0     | 5001 A06Ah       |
| EPWM26_G1     | 5005 A06Ah       |
| EPWM26_G2     | 5009 A06Ah       |
| EPWM26_G3     | 500D A06Ah       |
| EPWM27_G0     | 5001 B06Ah       |
| EPWM27_G1     | 5005 B06Ah       |
| EPWM27_G2     | 5009 B06Ah       |
| EPWM27_G3     | 500D B06Ah       |
| EPWM28_G0     | 5001 C06Ah       |
| EPWM28_G1     | 5005 C06Ah       |
| EPWM28_G2     | 5009 C06Ah       |
| EPWM28_G3     | 500D C06Ah       |
| EPWM29_G0     | 5001 D06Ah       |
| EPWM29_G1     | 5005 D06Ah       |
| EPWM29_G2     | 5009 D06Ah       |
| EPWM29_G3     | 500D D06Ah       |
| EPWM30_G0     | 5001 E06Ah       |
| EPWM30_G1     | 5005 E06Ah       |
| EPWM30_G2     | 5009 E06Ah       |
| EPWM30_G3     | 500D E06Ah       |
| EPWM31_G0     | 5001 F06Ah       |
| EPWM31_G1     | 5005 F06Ah       |
| EPWM31_G2     | 5009 F06Ah       |
| EPWM31_G3     | 500D F06Ah       |

**Figure 3-273. EPWM\_GLDCFG Name Register**

| 15         | 14                | 13                | 12   | 11   | 10              | 9                  | 8                  |
|------------|-------------------|-------------------|------|------|-----------------|--------------------|--------------------|
| RESERVED_1 |                   |                   |      |      | AQCSFRC         | AQCTLB_AQC<br>TLB2 | AQCTLA_AQC<br>TLA2 |
| R          |                   |                   |      |      | R/W             | R/W                | R/W                |
| 0h         |                   |                   |      |      | 0h              | 0h                 | 0h                 |
| 7          | 6                 | 5                 | 4    | 3    | 2               | 1                  | 0                  |
| DBCTL      | DBFED_DBFE<br>DHR | DBRED_DBRE<br>DHR | CMPD | CMPC | CMPB_CMPBH<br>R | CMPA_CMPAH<br>R    | TBPRD_TBPR<br>DHR  |
| R/W        | R/W               | R/W               | R/W  | R/W  | R/W             | R/W                | R/W                |
| 0h         | 0h                | 0h                | 0h   | 0h   | 0h              | 0h                 | 0h                 |

**Table 3-879. EPWM\_GLDCFG Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                               |
|-------|----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | RESERVED_1     | R    | 0h    | Reserved                                                                                                                                                                                                                                                  |
| 10    | AQCSFRC        | R/W  | 0h    | Global load event configuration for AQCSFRC<br>0:Registers use local reload configuration even if GLDCTL[GLD]=1<br>[reload is compatible with previous EPWMs]<br>1:Registers use global load configuration if this bit is set and<br>GLDCTL[GLD]=1        |
| 9     | AQCTLB_AQCTLB2 | R/W  | 0h    | Global load event configuration for AQCTLB_AQCTLB2<br>0:Registers use local reload configuration even if GLDCTL[GLD]=1<br>[reload is compatible with previous EPWMs]<br>1:Registers use global load configuration if this bit is set and<br>GLDCTL[GLD]=1 |
| 8     | AQCTLA_AQCTLA2 | R/W  | 0h    | Global load event configuration for AQCTLA_AQCTLA2<br>0:Registers use local reload configuration even if GLDCTL[GLD]=1<br>[reload is compatible with previous EPWMs]<br>1:Registers use global load configuration if this bit is set and<br>GLDCTL[GLD]=1 |
| 7     | DBCTL          | R/W  | 0h    | Global load event configuration for DBCTL<br>0:Registers use local reload configuration even if GLDCTL[GLD]=1<br>[reload is compatible with previous EPWMs]<br>1:Registers use global load configuration if this bit is set and<br>GLDCTL[GLD]=1          |
| 6     | DBFED_DBFEDHR  | R/W  | 0h    | Global load event configuration for DBFED_DBFEDHR<br>0:Registers use local reload configuration even if GLDCTL[GLD]=1<br>[reload is compatible with previous EPWMs]<br>1:Registers use global load configuration if this bit is set and<br>GLDCTL[GLD]=1  |
| 5     | DBRED_DBREDHR  | R/W  | 0h    | Global load event configuration for DBRED_DBREDHR<br>0:Registers use local reload configuration even if GLDCTL[GLD]=1<br>[reload is compatible with previous EPWMs]<br>1:Registers use global load configuration if this bit is set and<br>GLDCTL[GLD]=1  |
| 4     | CMPD           | R/W  | 0h    | Global load event configuration for CMPD<br>0:Registers use local reload configuration even if GLDCTL[GLD]=1<br>[reload is compatible with previous EPWMs]<br>1:Registers use global load configuration if this bit is set and<br>GLDCTL[GLD]=1           |
| 3     | CMPC           | R/W  | 0h    | Global load event configuration for CMPC<br>0:Registers use local reload configuration even if GLDCTL[GLD]=1<br>[reload is compatible with previous EPWMs]<br>1:Registers use global load configuration if this bit is set and<br>GLDCTL[GLD]=1           |



**Table 3-879. EPWM\_GLDCFG Register Field Descriptions (continued)**

| Bit | Field         | Type | Reset | Description                                                                                                                                                                                                                                        |
|-----|---------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | CMPB_CMPBHR   | R/W  | 0h    | Global load event configuration for CMPB_CMPBHR<br>0:Registers use local reload configuration even if GLDCTL[GLD]=1 [reload is compatible with previous EPWMs]<br>1:Registers use global load configuration if this bit is set and GLDCTL[GLD]=1   |
| 1   | CMPA_CMPAHR   | R/W  | 0h    | Global load event configuration for CMPA_CMPAHR<br>0:Registers use local reload configuration even if GLDCTL[GLD]=1 [reload is compatible with previous EPWMs]<br>1:Registers use global load configuration if this bit is set and GLDCTL[GLD]=1   |
| 0   | TBPRD_TBPRDHR | R/W  | 0h    | Global load event configuration for TBPRD_TBPRDHR<br>0:Registers use local reload configuration even if GLDCTL[GLD]=1 [reload is compatible with previous EPWMs]<br>1:Registers use global load configuration if this bit is set and GLDCTL[GLD]=1 |

### 3.7.2.23 EPWM\_EPWMXLINK Register

#### 1 EPWM\_EPWMXLINK Register (Offset = 70h) [reset = 0h]

##### EPWMx Link Register

This register controls which EPWMs are linked to other EPWM modules. The default reset value will vary for each module. The reset value will link each EPWM module to itself to prevent unintentional linking of modules.

Return to [Summary Table](#)

**Table 3-880. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0070h       |
| EPWM0_G1      | 5004 0070h       |
| EPWM0_G2      | 5008 0070h       |
| EPWM0_G3      | 500C 0070h       |
| EPWM1_G0      | 5000 1070h       |
| EPWM1_G1      | 5004 1070h       |
| EPWM1_G2      | 5008 1070h       |
| EPWM1_G3      | 500C 1070h       |
| EPWM2_G0      | 5000 2070h       |
| EPWM2_G1      | 5004 2070h       |
| EPWM2_G2      | 5008 2070h       |
| EPWM2_G3      | 500C 2070h       |
| EPWM3_G0      | 5000 3070h       |
| EPWM3_G1      | 5004 3070h       |
| EPWM3_G2      | 5008 3070h       |
| EPWM3_G3      | 500C 3070h       |
| EPWM4_G0      | 5000 4070h       |
| EPWM4_G1      | 5004 4070h       |
| EPWM4_G2      | 5008 4070h       |
| EPWM4_G3      | 500C 4070h       |
| EPWM5_G0      | 5000 5070h       |
| EPWM5_G1      | 5004 5070h       |
| EPWM5_G2      | 5008 5070h       |
| EPWM5_G3      | 500C 5070h       |
| EPWM6_G0      | 5000 6070h       |
| EPWM6_G1      | 5004 6070h       |
| EPWM6_G2      | 5008 6070h       |
| EPWM6_G3      | 500C 6070h       |
| EPWM7_G0      | 5000 7070h       |
| EPWM7_G1      | 5004 7070h       |
| EPWM7_G2      | 5008 7070h       |
| EPWM7_G3      | 500C 7070h       |
| EPWM8_G0      | 5000 8070h       |
| EPWM8_G1      | 5004 8070h       |
| EPWM8_G2      | 5008 8070h       |
| EPWM8_G3      | 500C 8070h       |
| EPWM9_G0      | 5000 9070h       |

**Table 3-880. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G1      | 5004 9070h       |
| EPWM9_G2      | 5008 9070h       |
| EPWM9_G3      | 500C 9070h       |
| EPWM10_G0     | 5000 A070h       |
| EPWM10_G1     | 5004 A070h       |
| EPWM10_G2     | 5008 A070h       |
| EPWM10_G3     | 500C A070h       |
| EPWM11_G0     | 5000 B070h       |
| EPWM11_G1     | 5004 B070h       |
| EPWM11_G2     | 5008 B070h       |
| EPWM11_G3     | 500C B070h       |
| EPWM12_G0     | 5000 C070h       |
| EPWM12_G1     | 5004 C070h       |
| EPWM12_G2     | 5008 C070h       |
| EPWM12_G3     | 500C C070h       |
| EPWM13_G0     | 5000 D070h       |
| EPWM13_G1     | 5004 D070h       |
| EPWM13_G2     | 5008 D070h       |
| EPWM13_G3     | 500C D070h       |
| EPWM14_G0     | 5000 E070h       |
| EPWM14_G1     | 5004 E070h       |
| EPWM14_G2     | 5008 E070h       |
| EPWM14_G3     | 500C E070h       |
| EPWM15_G0     | 5000 F070h       |
| EPWM15_G1     | 5004 F070h       |
| EPWM15_G2     | 5008 F070h       |
| EPWM15_G3     | 500C F070h       |
| EPWM16_G0     | 5001 0070h       |
| EPWM16_G1     | 5005 0070h       |
| EPWM16_G2     | 5009 0070h       |
| EPWM16_G3     | 500D 0070h       |
| EPWM17_G0     | 5001 1070h       |
| EPWM17_G1     | 5005 1070h       |
| EPWM17_G2     | 5009 1070h       |
| EPWM17_G3     | 500D 1070h       |
| EPWM18_G0     | 5001 2070h       |
| EPWM18_G1     | 5005 2070h       |
| EPWM18_G2     | 5009 2070h       |
| EPWM18_G3     | 500D 2070h       |
| EPWM19_G0     | 5001 3070h       |
| EPWM19_G1     | 5005 3070h       |
| EPWM19_G2     | 5009 3070h       |
| EPWM19_G3     | 500D 3070h       |
| EPWM20_G0     | 5001 4070h       |
| EPWM20_G1     | 5005 4070h       |

**Table 3-880. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM20_G2     | 5009 4070h       |
| EPWM20_G3     | 500D 4070h       |
| EPWM21_G0     | 5001 5070h       |
| EPWM21_G1     | 5005 5070h       |
| EPWM21_G2     | 5009 5070h       |
| EPWM21_G3     | 500D 5070h       |
| EPWM22_G0     | 5001 6070h       |
| EPWM22_G1     | 5005 6070h       |
| EPWM22_G2     | 5009 6070h       |
| EPWM22_G3     | 500D 6070h       |
| EPWM23_G0     | 5001 7070h       |
| EPWM23_G1     | 5005 7070h       |
| EPWM23_G2     | 5009 7070h       |
| EPWM23_G3     | 500D 7070h       |
| EPWM24_G0     | 5001 8070h       |
| EPWM24_G1     | 5005 8070h       |
| EPWM24_G2     | 5009 8070h       |
| EPWM24_G3     | 500D 8070h       |
| EPWM25_G0     | 5001 9070h       |
| EPWM25_G1     | 5005 9070h       |
| EPWM25_G2     | 5009 9070h       |
| EPWM25_G3     | 500D 9070h       |
| EPWM26_G0     | 5001 A070h       |
| EPWM26_G1     | 5005 A070h       |
| EPWM26_G2     | 5009 A070h       |
| EPWM26_G3     | 500D A070h       |
| EPWM27_G0     | 5001 B070h       |
| EPWM27_G1     | 5005 B070h       |
| EPWM27_G2     | 5009 B070h       |
| EPWM27_G3     | 500D B070h       |
| EPWM28_G0     | 5001 C070h       |
| EPWM28_G1     | 5005 C070h       |
| EPWM28_G2     | 5009 C070h       |
| EPWM28_G3     | 500D C070h       |
| EPWM29_G0     | 5001 D070h       |
| EPWM29_G1     | 5005 D070h       |
| EPWM29_G2     | 5009 D070h       |
| EPWM29_G3     | 500D D070h       |
| EPWM30_G0     | 5001 E070h       |
| EPWM30_G1     | 5005 E070h       |
| EPWM30_G2     | 5009 E070h       |
| EPWM30_G3     | 500D E070h       |
| EPWM31_G0     | 5001 F070h       |
| EPWM31_G1     | 5005 F070h       |
| EPWM31_G2     | 5009 F070h       |

**Table 3-880. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM31_G3     | 500D F070h       |

**Figure 3-274. EPWM\_EPWMXLINK Name Register**

|            |             |    |           |    |    |          |    |
|------------|-------------|----|-----------|----|----|----------|----|
| 31         | 30          | 29 | 28        | 27 | 26 | 25       | 24 |
| RESERVED_2 | GLDCTL2LINK |    |           |    |    | CMPDLINK |    |
| R          | R/W         |    |           |    |    | R/W      |    |
| 0h         | 0h          |    |           |    |    | 0h       |    |
| 23         | 22          | 21 | 20        | 19 | 18 | 17       | 16 |
| CMPDLINK   |             |    | CMPCLINK  |    |    |          |    |
| R/W        |             |    | R/W       |    |    |          |    |
| 0h         |             |    | 0h        |    |    |          |    |
| 15         | 14          | 13 | 12        | 11 | 10 | 9        | 8  |
| RESERVED_1 | CMPBLINK    |    |           |    |    | CMPALINK |    |
| R          | R/W         |    |           |    |    | R/W      |    |
| 0h         | 0h          |    |           |    |    | 0h       |    |
| 7          | 6           | 5  | 4         | 3  | 2  | 1        | 0  |
| CMPALINK   |             |    | TBPRDLINK |    |    |          |    |
| R/W        |             |    | R/W       |    |    |          |    |
| 0h         |             |    | 0h        |    |    |          |    |

**Table 3-882. EPWM\_EPWMXLINK Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|-------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | RESERVED_2  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 30:26 | GLDCTL2LINK | R/W  | 0h    | GLDCTL2 Link Bits<br>Writes to the GLDCTL2 registers in the EPWM module selected by the following bit selections results in a simultaneous write to the current EPWM module's GLDCTL2 registers.<br>5'b00000: EPWM0<br>5'b00001: EPWM1<br>5'b00010: EPWM2<br>5'b00011: EPWM3<br>5'b00100: EPWM4<br>5'b00101: EPWM5<br>5'b00110: EPWM6<br>5'b00111: EPWM7<br>5'b01000: EPWM8<br>5'b01001: EPWM9<br>5'b01010: EPWM10<br>5'b01011: EPWM11<br>5'b01100: EPWM12<br>...<br>5'b11111: EPWM31 |

**Table 3-882. EPWM\_EPWMXLINK Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 25:21 | CMPDLINK   | R/W  | 0h    | <p>CMPD Link Bits</p> <p>Writes to the CMPD registers in the EPWM module selected by the following bit selections results in a simultaneous write to the current EPWM module's CMPD registers.</p> <p>5'b00000: EPWM0<br/> 5'b00001: EPWM1<br/> 5'b00010: EPWM2<br/> 5'b00011: EPWM3<br/> 5'b00100: EPWM4<br/> 5'b00101: EPWM5<br/> 5'b00110: EPWM6<br/> 5'b00111: EPWM7<br/> 5'b01000: EPWM8<br/> 5'b01001: EPWM9<br/> 5'b01010: EPWM10<br/> 5'b01011: EPWM11<br/> 5'b01100: EPWM12<br/> ...<br/> 5'b11111: EPWM31</p>                      |
| 20:16 | CMPCLINK   | R/W  | 0h    | <p>CMPC Link Bits</p> <p>Writes to the CMPC registers in the EPWM module selected by the following bit selections results in a simultaneous write to the current EPWM module's CMPC registers.</p> <p>5'b00000: EPWM0<br/> 5'b00001: EPWM1<br/> 5'b00010: EPWM2<br/> 5'b00011: EPWM3<br/> 5'b00100: EPWM4<br/> 5'b00101: EPWM5<br/> 5'b00110: EPWM6<br/> 5'b00111: EPWM7<br/> 5'b01000: EPWM8<br/> 5'b01001: EPWM9<br/> 5'b01010: EPWM10<br/> 5'b01011: EPWM11<br/> 5'b01100: EPWM12<br/> ...<br/> 5'b11111: EPWM31</p>                      |
| 15    | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 14:10 | CMPBLINK   | R/W  | 0h    | <p>CMPB_CMPBHR Link Bits</p> <p>Writes to the CMPB_CMPBHR registers in the EPWM module selected by the following bit selections results in a simultaneous write to the current EPWM module's CMPB_CMPBHR registers.</p> <p>5'b00000: EPWM0<br/> 5'b00001: EPWM1<br/> 5'b00010: EPWM2<br/> 5'b00011: EPWM3<br/> 5'b00100: EPWM4<br/> 5'b00101: EPWM5<br/> 5'b00110: EPWM6<br/> 5'b00111: EPWM7<br/> 5'b01000: EPWM8<br/> 5'b01001: EPWM9<br/> 5'b01010: EPWM10<br/> 5'b01011: EPWM11<br/> 5'b01100: EPWM12<br/> ...<br/> 5'b11111: EPWM31</p> |

**Table 3-882. EPWM\_EPWMXLINK Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-----|-----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9:5 | CMPALINK  | R/W  | 0h    | CMPA_CMPAHR Link Bits<br>Writes to the CMPA_CMPAHR registers in the EPWM module selected by the following bit selections results in a simultaneous write to the current EPWM module's CMPA_CMPAHR registers.<br>5'b00000: EPWM0<br>5'b00001: EPWM1<br>5'b00010: EPWM2<br>5'b00011: EPWM3<br>5'b00100: EPWM4<br>5'b00101: EPWM5<br>5'b00110: EPWM6<br>5'b00111: EPWM7<br>5'b01000: EPWM8<br>5'b01001: EPWM9<br>5'b01010: EPWM10<br>5'b01011: EPWM11<br>5'b01100: EPWM12<br>...<br>5'b11111: EPWM31       |
| 4:0 | TBPRDLINK | R/W  | 0h    | TBPRD_TBPRDHR Link Bits<br>Writes to the TBPRD_TBPRDHR registers in the EPWM module selected by the following bit selections results in a simultaneous write to the current EPWM module's TBPRD_TBPRDHR registers.<br>5'b00000: EPWM0<br>5'b00001: EPWM1<br>5'b00010: EPWM2<br>5'b00011: EPWM3<br>5'b00100: EPWM4<br>5'b00101: EPWM5<br>5'b00110: EPWM6<br>5'b00111: EPWM7<br>5'b01000: EPWM8<br>5'b01001: EPWM9<br>5'b01010: EPWM10<br>5'b01011: EPWM11<br>5'b01100: EPWM12<br>...<br>5'b11111: EPWM31 |

### 3.7.2.24 EPWM\_EPWMXLINK2 Register

#### 1 EPWM\_EPWMXLINK2 Register (Offset = 74h) [reset = 0h]

EPWMx Link 2 Register

This register controls which EPWMs are linked to other EPWM modules. The default reset value will vary for each module. The reset value will link each EPWM module to itself to prevent unintentional linking of modules.

Return to [Summary Table](#)

**Table 3-883. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0074h       |
| EPWM0_G1      | 5004 0074h       |
| EPWM0_G2      | 5008 0074h       |
| EPWM0_G3      | 500C 0074h       |
| EPWM1_G0      | 5000 1074h       |
| EPWM1_G1      | 5004 1074h       |
| EPWM1_G2      | 5008 1074h       |
| EPWM1_G3      | 500C 1074h       |
| EPWM2_G0      | 5000 2074h       |
| EPWM2_G1      | 5004 2074h       |
| EPWM2_G2      | 5008 2074h       |
| EPWM2_G3      | 500C 2074h       |
| EPWM3_G0      | 5000 3074h       |
| EPWM3_G1      | 5004 3074h       |
| EPWM3_G2      | 5008 3074h       |
| EPWM3_G3      | 500C 3074h       |
| EPWM4_G0      | 5000 4074h       |
| EPWM4_G1      | 5004 4074h       |
| EPWM4_G2      | 5008 4074h       |
| EPWM4_G3      | 500C 4074h       |
| EPWM5_G0      | 5000 5074h       |
| EPWM5_G1      | 5004 5074h       |
| EPWM5_G2      | 5008 5074h       |
| EPWM5_G3      | 500C 5074h       |
| EPWM6_G0      | 5000 6074h       |
| EPWM6_G1      | 5004 6074h       |
| EPWM6_G2      | 5008 6074h       |
| EPWM6_G3      | 500C 6074h       |
| EPWM7_G0      | 5000 7074h       |
| EPWM7_G1      | 5004 7074h       |
| EPWM7_G2      | 5008 7074h       |
| EPWM7_G3      | 500C 7074h       |
| EPWM8_G0      | 5000 8074h       |
| EPWM8_G1      | 5004 8074h       |
| EPWM8_G2      | 5008 8074h       |
| EPWM8_G3      | 500C 8074h       |
| EPWM9_G0      | 5000 9074h       |



**Table 3-883. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G1      | 5004 9074h       |
| EPWM9_G2      | 5008 9074h       |
| EPWM9_G3      | 500C 9074h       |
| EPWM10_G0     | 5000 A074h       |
| EPWM10_G1     | 5004 A074h       |
| EPWM10_G2     | 5008 A074h       |
| EPWM10_G3     | 500C A074h       |
| EPWM11_G0     | 5000 B074h       |
| EPWM11_G1     | 5004 B074h       |
| EPWM11_G2     | 5008 B074h       |
| EPWM11_G3     | 500C B074h       |
| EPWM12_G0     | 5000 C074h       |
| EPWM12_G1     | 5004 C074h       |
| EPWM12_G2     | 5008 C074h       |
| EPWM12_G3     | 500C C074h       |
| EPWM13_G0     | 5000 D074h       |
| EPWM13_G1     | 5004 D074h       |
| EPWM13_G2     | 5008 D074h       |
| EPWM13_G3     | 500C D074h       |
| EPWM14_G0     | 5000 E074h       |
| EPWM14_G1     | 5004 E074h       |
| EPWM14_G2     | 5008 E074h       |
| EPWM14_G3     | 500C E074h       |
| EPWM15_G0     | 5000 F074h       |
| EPWM15_G1     | 5004 F074h       |
| EPWM15_G2     | 5008 F074h       |
| EPWM15_G3     | 500C F074h       |
| EPWM16_G0     | 5001 0074h       |
| EPWM16_G1     | 5005 0074h       |
| EPWM16_G2     | 5009 0074h       |
| EPWM16_G3     | 500D 0074h       |
| EPWM17_G0     | 5001 1074h       |
| EPWM17_G1     | 5005 1074h       |
| EPWM17_G2     | 5009 1074h       |
| EPWM17_G3     | 500D 1074h       |
| EPWM18_G0     | 5001 2074h       |
| EPWM18_G1     | 5005 2074h       |
| EPWM18_G2     | 5009 2074h       |
| EPWM18_G3     | 500D 2074h       |
| EPWM19_G0     | 5001 3074h       |
| EPWM19_G1     | 5005 3074h       |
| EPWM19_G2     | 5009 3074h       |
| EPWM19_G3     | 500D 3074h       |
| EPWM20_G0     | 5001 4074h       |
| EPWM20_G1     | 5005 4074h       |

**Table 3-883. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM20_G2     | 5009 4074h       |
| EPWM20_G3     | 500D 4074h       |
| EPWM21_G0     | 5001 5074h       |
| EPWM21_G1     | 5005 5074h       |
| EPWM21_G2     | 5009 5074h       |
| EPWM21_G3     | 500D 5074h       |
| EPWM22_G0     | 5001 6074h       |
| EPWM22_G1     | 5005 6074h       |
| EPWM22_G2     | 5009 6074h       |
| EPWM22_G3     | 500D 6074h       |
| EPWM23_G0     | 5001 7074h       |
| EPWM23_G1     | 5005 7074h       |
| EPWM23_G2     | 5009 7074h       |
| EPWM23_G3     | 500D 7074h       |
| EPWM24_G0     | 5001 8074h       |
| EPWM24_G1     | 5005 8074h       |
| EPWM24_G2     | 5009 8074h       |
| EPWM24_G3     | 500D 8074h       |
| EPWM25_G0     | 5001 9074h       |
| EPWM25_G1     | 5005 9074h       |
| EPWM25_G2     | 5009 9074h       |
| EPWM25_G3     | 500D 9074h       |
| EPWM26_G0     | 5001 A074h       |
| EPWM26_G1     | 5005 A074h       |
| EPWM26_G2     | 5009 A074h       |
| EPWM26_G3     | 500D A074h       |
| EPWM27_G0     | 5001 B074h       |
| EPWM27_G1     | 5005 B074h       |
| EPWM27_G2     | 5009 B074h       |
| EPWM27_G3     | 500D B074h       |
| EPWM28_G0     | 5001 C074h       |
| EPWM28_G1     | 5005 C074h       |
| EPWM28_G2     | 5009 C074h       |
| EPWM28_G3     | 500D C074h       |
| EPWM29_G0     | 5001 D074h       |
| EPWM29_G1     | 5005 D074h       |
| EPWM29_G2     | 5009 D074h       |
| EPWM29_G3     | 500D D074h       |
| EPWM30_G0     | 5001 E074h       |
| EPWM30_G1     | 5005 E074h       |
| EPWM30_G2     | 5009 E074h       |
| EPWM30_G3     | 500D E074h       |
| EPWM31_G0     | 5001 F074h       |
| EPWM31_G1     | 5005 F074h       |
| EPWM31_G2     | 5009 F074h       |

**Table 3-883. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM31_G3     | 500D F074h       |

**Figure 3-275. EPWM\_EPWMXLINK2 Name Register**

|            |    |    |           |    |    |           |    |
|------------|----|----|-----------|----|----|-----------|----|
| 31         | 30 | 29 | 28        | 27 | 26 | 25        | 24 |
| RESERVED_1 |    |    |           |    |    |           |    |
| R          |    |    |           |    |    |           |    |
| 0h         |    |    |           |    |    |           |    |
| 23         | 22 | 21 | 20        | 19 | 18 | 17        | 16 |
| RESERVED_1 |    |    |           |    |    |           |    |
| R          |    |    |           |    |    |           |    |
| 0h         |    |    |           |    |    |           |    |
| 15         | 14 | 13 | 12        | 11 | 10 | 9         | 8  |
| RESERVED_1 |    |    |           |    |    | DBFEDLINK |    |
| R          |    |    |           |    |    | R/W       |    |
| 0h         |    |    |           |    |    | 0h        |    |
| 7          | 6  | 5  | 4         | 3  | 2  | 1         | 0  |
| DBFEDLINK  |    |    | DBREDLINK |    |    |           |    |
| R/W        |    |    | R/W       |    |    |           |    |
| 0h         |    |    | 0h        |    |    |           |    |

**Table 3-885. EPWM\_EPWMXLINK2 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 9:5   | DBFEDLINK  | R/W  | 0h    | DBFED_DBFEDHR Link Bits<br>Writes to the DBFED:DBFEDHR registers in the EPWM module selected by the following bit selections results in a simultaneous write to the current EPWM module's DBFED_DBFEDHR registers.<br>5'b00000: EPWM0<br>5'b00001: EPWM1<br>5'b00010: EPWM2<br>5'b00011: EPWM3<br>5'b00100: EPWM4<br>5'b00101: EPWM5<br>5'b00110: EPWM6<br>5'b00111: EPWM7<br>5'b01000: EPWM8<br>5'b01001: EPWM9<br>5'b01010: EPWM10<br>5'b01011: EPWM11<br>5'b01100: EPWM12<br>...<br>5'b11111: EPWM31 |

**Table 3-885. EPWM\_EPWMXLINK2 Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | DBREDLINK | R/W  | 0h    | <p>DBRED_DBREDHR Link Bits</p> <p>Writes to the DBRED:DBREDHR registers in the EPWM module selected by the following bit selections results in a simultaneous write to the current EPWM module's DBRED_DBREDHR registers.</p> <p>5'b00000: EPWM0</p> <p>5'b00001: EPWM1</p> <p>5'b00010: EPWM2</p> <p>5'b00011: EPWM3</p> <p>5'b00100: EPWM4</p> <p>5'b00101: EPWM5</p> <p>5'b00110: EPWM6</p> <p>5'b00111: EPWM7</p> <p>5'b01000: EPWM8</p> <p>5'b01001: EPWM9</p> <p>5'b01010: EPWM10</p> <p>5'b01011: EPWM11</p> <p>5'b01100: EPWM12</p> <p>...</p> <p>5'b11111: EPWM31</p> |

### 3.7.2.25 EPWM\_ETEST Register

#### 1 EPWM\_ETEST Register (Offset = 7Ah) [reset = 1h]

EPWM Test Register.

Return to [Summary Table](#)

**Table 3-886. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 007Ah       |
| EPWM0_G1      | 5004 007Ah       |
| EPWM0_G2      | 5008 007Ah       |
| EPWM0_G3      | 500C 007Ah       |
| EPWM1_G0      | 5000 107Ah       |
| EPWM1_G1      | 5004 107Ah       |
| EPWM1_G2      | 5008 107Ah       |
| EPWM1_G3      | 500C 107Ah       |
| EPWM2_G0      | 5000 207Ah       |
| EPWM2_G1      | 5004 207Ah       |
| EPWM2_G2      | 5008 207Ah       |
| EPWM2_G3      | 500C 207Ah       |
| EPWM3_G0      | 5000 307Ah       |
| EPWM3_G1      | 5004 307Ah       |
| EPWM3_G2      | 5008 307Ah       |
| EPWM3_G3      | 500C 307Ah       |
| EPWM4_G0      | 5000 407Ah       |
| EPWM4_G1      | 5004 407Ah       |
| EPWM4_G2      | 5008 407Ah       |
| EPWM4_G3      | 500C 407Ah       |
| EPWM5_G0      | 5000 507Ah       |
| EPWM5_G1      | 5004 507Ah       |
| EPWM5_G2      | 5008 507Ah       |
| EPWM5_G3      | 500C 507Ah       |
| EPWM6_G0      | 5000 607Ah       |
| EPWM6_G1      | 5004 607Ah       |
| EPWM6_G2      | 5008 607Ah       |
| EPWM6_G3      | 500C 607Ah       |
| EPWM7_G0      | 5000 707Ah       |
| EPWM7_G1      | 5004 707Ah       |
| EPWM7_G2      | 5008 707Ah       |
| EPWM7_G3      | 500C 707Ah       |
| EPWM8_G0      | 5000 807Ah       |
| EPWM8_G1      | 5004 807Ah       |
| EPWM8_G2      | 5008 807Ah       |
| EPWM8_G3      | 500C 807Ah       |
| EPWM9_G0      | 5000 907Ah       |
| EPWM9_G1      | 5004 907Ah       |
| EPWM9_G2      | 5008 907Ah       |

**Table 3-886. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 907Ah       |
| EPWM10_G0     | 5000 A07Ah       |
| EPWM10_G1     | 5004 A07Ah       |
| EPWM10_G2     | 5008 A07Ah       |
| EPWM10_G3     | 500C A07Ah       |
| EPWM11_G0     | 5000 B07Ah       |
| EPWM11_G1     | 5004 B07Ah       |
| EPWM11_G2     | 5008 B07Ah       |
| EPWM11_G3     | 500C B07Ah       |
| EPWM12_G0     | 5000 C07Ah       |
| EPWM12_G1     | 5004 C07Ah       |
| EPWM12_G2     | 5008 C07Ah       |
| EPWM12_G3     | 500C C07Ah       |
| EPWM13_G0     | 5000 D07Ah       |
| EPWM13_G1     | 5004 D07Ah       |
| EPWM13_G2     | 5008 D07Ah       |
| EPWM13_G3     | 500C D07Ah       |
| EPWM14_G0     | 5000 E07Ah       |
| EPWM14_G1     | 5004 E07Ah       |
| EPWM14_G2     | 5008 E07Ah       |
| EPWM14_G3     | 500C E07Ah       |
| EPWM15_G0     | 5000 F07Ah       |
| EPWM15_G1     | 5004 F07Ah       |
| EPWM15_G2     | 5008 F07Ah       |
| EPWM15_G3     | 500C F07Ah       |
| EPWM16_G0     | 5001 007Ah       |
| EPWM16_G1     | 5005 007Ah       |
| EPWM16_G2     | 5009 007Ah       |
| EPWM16_G3     | 500D 007Ah       |
| EPWM17_G0     | 5001 107Ah       |
| EPWM17_G1     | 5005 107Ah       |
| EPWM17_G2     | 5009 107Ah       |
| EPWM17_G3     | 500D 107Ah       |
| EPWM18_G0     | 5001 207Ah       |
| EPWM18_G1     | 5005 207Ah       |
| EPWM18_G2     | 5009 207Ah       |
| EPWM18_G3     | 500D 207Ah       |
| EPWM19_G0     | 5001 307Ah       |
| EPWM19_G1     | 5005 307Ah       |
| EPWM19_G2     | 5009 307Ah       |
| EPWM19_G3     | 500D 307Ah       |
| EPWM20_G0     | 5001 407Ah       |
| EPWM20_G1     | 5005 407Ah       |
| EPWM20_G2     | 5009 407Ah       |
| EPWM20_G3     | 500D 407Ah       |

**Table 3-886. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 507Ah       |
| EPWM21_G1     | 5005 507Ah       |
| EPWM21_G2     | 5009 507Ah       |
| EPWM21_G3     | 500D 507Ah       |
| EPWM22_G0     | 5001 607Ah       |
| EPWM22_G1     | 5005 607Ah       |
| EPWM22_G2     | 5009 607Ah       |
| EPWM22_G3     | 500D 607Ah       |
| EPWM23_G0     | 5001 707Ah       |
| EPWM23_G1     | 5005 707Ah       |
| EPWM23_G2     | 5009 707Ah       |
| EPWM23_G3     | 500D 707Ah       |
| EPWM24_G0     | 5001 807Ah       |
| EPWM24_G1     | 5005 807Ah       |
| EPWM24_G2     | 5009 807Ah       |
| EPWM24_G3     | 500D 807Ah       |
| EPWM25_G0     | 5001 907Ah       |
| EPWM25_G1     | 5005 907Ah       |
| EPWM25_G2     | 5009 907Ah       |
| EPWM25_G3     | 500D 907Ah       |
| EPWM26_G0     | 5001 A07Ah       |
| EPWM26_G1     | 5005 A07Ah       |
| EPWM26_G2     | 5009 A07Ah       |
| EPWM26_G3     | 500D A07Ah       |
| EPWM27_G0     | 5001 B07Ah       |
| EPWM27_G1     | 5005 B07Ah       |
| EPWM27_G2     | 5009 B07Ah       |
| EPWM27_G3     | 500D B07Ah       |
| EPWM28_G0     | 5001 C07Ah       |
| EPWM28_G1     | 5005 C07Ah       |
| EPWM28_G2     | 5009 C07Ah       |
| EPWM28_G3     | 500D C07Ah       |
| EPWM29_G0     | 5001 D07Ah       |
| EPWM29_G1     | 5005 D07Ah       |
| EPWM29_G2     | 5009 D07Ah       |
| EPWM29_G3     | 500D D07Ah       |
| EPWM30_G0     | 5001 E07Ah       |
| EPWM30_G1     | 5005 E07Ah       |
| EPWM30_G2     | 5009 E07Ah       |
| EPWM30_G3     | 500D E07Ah       |
| EPWM31_G0     | 5001 F07Ah       |
| EPWM31_G1     | 5005 F07Ah       |
| EPWM31_G2     | 5009 F07Ah       |
| EPWM31_G3     | 500D F07Ah       |

**Figure 3-276. EPWM\_ETEST Name Register**

|            |    |    |    |    |    |   |                 |
|------------|----|----|----|----|----|---|-----------------|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8               |
| RESERVED_1 |    |    |    |    |    |   |                 |
| R          |    |    |    |    |    |   |                 |
| 0h         |    |    |    |    |    |   |                 |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0               |
| RESERVED_1 |    |    |    |    |    |   | CMPFIX_OVERRIDE |
| R          |    |    |    |    |    |   | R/W             |
| 0h         |    |    |    |    |    |   | 1h              |

**Table 3-888. EPWM\_ETEST Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                      |
|------|-----------------|------|-------|--------------------------------------------------|
| 15:1 | RESERVED_1      | R    | 0h    | Reserved                                         |
| 0    | CMPFIX_OVERRIDE | R/W  | 1h    | 0: Bug fix overridden<br>1: Bug fix takes effect |



### 3.7.2.26 EPWM\_EPWMREV Register

#### 1 EPWM\_EPWMREV Register (Offset = 7Ch) [reset = 500h]

EPWM Revision Register.

Return to [Summary Table](#)

**Table 3-889. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 007Ch       |
| EPWM0_G1      | 5004 007Ch       |
| EPWM0_G2      | 5008 007Ch       |
| EPWM0_G3      | 500C 007Ch       |
| EPWM1_G0      | 5000 107Ch       |
| EPWM1_G1      | 5004 107Ch       |
| EPWM1_G2      | 5008 107Ch       |
| EPWM1_G3      | 500C 107Ch       |
| EPWM2_G0      | 5000 207Ch       |
| EPWM2_G1      | 5004 207Ch       |
| EPWM2_G2      | 5008 207Ch       |
| EPWM2_G3      | 500C 207Ch       |
| EPWM3_G0      | 5000 307Ch       |
| EPWM3_G1      | 5004 307Ch       |
| EPWM3_G2      | 5008 307Ch       |
| EPWM3_G3      | 500C 307Ch       |
| EPWM4_G0      | 5000 407Ch       |
| EPWM4_G1      | 5004 407Ch       |
| EPWM4_G2      | 5008 407Ch       |
| EPWM4_G3      | 500C 407Ch       |
| EPWM5_G0      | 5000 507Ch       |
| EPWM5_G1      | 5004 507Ch       |
| EPWM5_G2      | 5008 507Ch       |
| EPWM5_G3      | 500C 507Ch       |
| EPWM6_G0      | 5000 607Ch       |
| EPWM6_G1      | 5004 607Ch       |
| EPWM6_G2      | 5008 607Ch       |
| EPWM6_G3      | 500C 607Ch       |
| EPWM7_G0      | 5000 707Ch       |
| EPWM7_G1      | 5004 707Ch       |
| EPWM7_G2      | 5008 707Ch       |
| EPWM7_G3      | 500C 707Ch       |
| EPWM8_G0      | 5000 807Ch       |
| EPWM8_G1      | 5004 807Ch       |
| EPWM8_G2      | 5008 807Ch       |
| EPWM8_G3      | 500C 807Ch       |
| EPWM9_G0      | 5000 907Ch       |
| EPWM9_G1      | 5004 907Ch       |
| EPWM9_G2      | 5008 907Ch       |

**Table 3-889. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 907Ch       |
| EPWM10_G0     | 5000 A07Ch       |
| EPWM10_G1     | 5004 A07Ch       |
| EPWM10_G2     | 5008 A07Ch       |
| EPWM10_G3     | 500C A07Ch       |
| EPWM11_G0     | 5000 B07Ch       |
| EPWM11_G1     | 5004 B07Ch       |
| EPWM11_G2     | 5008 B07Ch       |
| EPWM11_G3     | 500C B07Ch       |
| EPWM12_G0     | 5000 C07Ch       |
| EPWM12_G1     | 5004 C07Ch       |
| EPWM12_G2     | 5008 C07Ch       |
| EPWM12_G3     | 500C C07Ch       |
| EPWM13_G0     | 5000 D07Ch       |
| EPWM13_G1     | 5004 D07Ch       |
| EPWM13_G2     | 5008 D07Ch       |
| EPWM13_G3     | 500C D07Ch       |
| EPWM14_G0     | 5000 E07Ch       |
| EPWM14_G1     | 5004 E07Ch       |
| EPWM14_G2     | 5008 E07Ch       |
| EPWM14_G3     | 500C E07Ch       |
| EPWM15_G0     | 5000 F07Ch       |
| EPWM15_G1     | 5004 F07Ch       |
| EPWM15_G2     | 5008 F07Ch       |
| EPWM15_G3     | 500C F07Ch       |
| EPWM16_G0     | 5001 007Ch       |
| EPWM16_G1     | 5005 007Ch       |
| EPWM16_G2     | 5009 007Ch       |
| EPWM16_G3     | 500D 007Ch       |
| EPWM17_G0     | 5001 107Ch       |
| EPWM17_G1     | 5005 107Ch       |
| EPWM17_G2     | 5009 107Ch       |
| EPWM17_G3     | 500D 107Ch       |
| EPWM18_G0     | 5001 207Ch       |
| EPWM18_G1     | 5005 207Ch       |
| EPWM18_G2     | 5009 207Ch       |
| EPWM18_G3     | 500D 207Ch       |
| EPWM19_G0     | 5001 307Ch       |
| EPWM19_G1     | 5005 307Ch       |
| EPWM19_G2     | 5009 307Ch       |
| EPWM19_G3     | 500D 307Ch       |
| EPWM20_G0     | 5001 407Ch       |
| EPWM20_G1     | 5005 407Ch       |
| EPWM20_G2     | 5009 407Ch       |
| EPWM20_G3     | 500D 407Ch       |

**Table 3-889. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 507Ch       |
| EPWM21_G1     | 5005 507Ch       |
| EPWM21_G2     | 5009 507Ch       |
| EPWM21_G3     | 500D 507Ch       |
| EPWM22_G0     | 5001 607Ch       |
| EPWM22_G1     | 5005 607Ch       |
| EPWM22_G2     | 5009 607Ch       |
| EPWM22_G3     | 500D 607Ch       |
| EPWM23_G0     | 5001 707Ch       |
| EPWM23_G1     | 5005 707Ch       |
| EPWM23_G2     | 5009 707Ch       |
| EPWM23_G3     | 500D 707Ch       |
| EPWM24_G0     | 5001 807Ch       |
| EPWM24_G1     | 5005 807Ch       |
| EPWM24_G2     | 5009 807Ch       |
| EPWM24_G3     | 500D 807Ch       |
| EPWM25_G0     | 5001 907Ch       |
| EPWM25_G1     | 5005 907Ch       |
| EPWM25_G2     | 5009 907Ch       |
| EPWM25_G3     | 500D 907Ch       |
| EPWM26_G0     | 5001 A07Ch       |
| EPWM26_G1     | 5005 A07Ch       |
| EPWM26_G2     | 5009 A07Ch       |
| EPWM26_G3     | 500D A07Ch       |
| EPWM27_G0     | 5001 B07Ch       |
| EPWM27_G1     | 5005 B07Ch       |
| EPWM27_G2     | 5009 B07Ch       |
| EPWM27_G3     | 500D B07Ch       |
| EPWM28_G0     | 5001 C07Ch       |
| EPWM28_G1     | 5005 C07Ch       |
| EPWM28_G2     | 5009 C07Ch       |
| EPWM28_G3     | 500D C07Ch       |
| EPWM29_G0     | 5001 D07Ch       |
| EPWM29_G1     | 5005 D07Ch       |
| EPWM29_G2     | 5009 D07Ch       |
| EPWM29_G3     | 500D D07Ch       |
| EPWM30_G0     | 5001 E07Ch       |
| EPWM30_G1     | 5005 E07Ch       |
| EPWM30_G2     | 5009 E07Ch       |
| EPWM30_G3     | 500D E07Ch       |
| EPWM31_G0     | 5001 F07Ch       |
| EPWM31_G1     | 5005 F07Ch       |
| EPWM31_G2     | 5009 F07Ch       |
| EPWM31_G3     | 500D F07Ch       |

**Figure 3-277. EPWM\_EPWMREV Name Register**

|      |    |    |    |    |    |   |   |
|------|----|----|----|----|----|---|---|
| 15   | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TYPE |    |    |    |    |    |   |   |
| R    |    |    |    |    |    |   |   |
| 5h   |    |    |    |    |    |   |   |
| 7    | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| REV  |    |    |    |    |    |   |   |
| R    |    |    |    |    |    |   |   |
| 0h   |    |    |    |    |    |   |   |

**Table 3-891. EPWM\_EPWMREV Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                              |
|------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | TYPE  | R    | 5h    | EPWM Type Bits: These bits specify the EPWM type. These bits are changed if the functionality of the EPWM is changed or any feature is added or removed: |
| 7:0  | REV   | R    | 0h    | EPWM Silicon Revision Bits: These bits specify the EPWM revision. These bits are changed if any bug fixes are performed:                                 |

### 3.7.2.27 EPWM\_HRPWMREV Register

#### 1 EPWM\_HRPWMREV Register (Offset = 7Eh) [reset = 300h]

High Resolution Revision Register.

Return to [Summary Table](#)

**Table 3-892. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 007Eh       |
| EPWM0_G1      | 5004 007Eh       |
| EPWM0_G2      | 5008 007Eh       |
| EPWM0_G3      | 500C 007Eh       |
| EPWM1_G0      | 5000 107Eh       |
| EPWM1_G1      | 5004 107Eh       |
| EPWM1_G2      | 5008 107Eh       |
| EPWM1_G3      | 500C 107Eh       |
| EPWM2_G0      | 5000 207Eh       |
| EPWM2_G1      | 5004 207Eh       |
| EPWM2_G2      | 5008 207Eh       |
| EPWM2_G3      | 500C 207Eh       |
| EPWM3_G0      | 5000 307Eh       |
| EPWM3_G1      | 5004 307Eh       |
| EPWM3_G2      | 5008 307Eh       |
| EPWM3_G3      | 500C 307Eh       |
| EPWM4_G0      | 5000 407Eh       |
| EPWM4_G1      | 5004 407Eh       |
| EPWM4_G2      | 5008 407Eh       |
| EPWM4_G3      | 500C 407Eh       |
| EPWM5_G0      | 5000 507Eh       |
| EPWM5_G1      | 5004 507Eh       |
| EPWM5_G2      | 5008 507Eh       |
| EPWM5_G3      | 500C 507Eh       |
| EPWM6_G0      | 5000 607Eh       |
| EPWM6_G1      | 5004 607Eh       |
| EPWM6_G2      | 5008 607Eh       |
| EPWM6_G3      | 500C 607Eh       |
| EPWM7_G0      | 5000 707Eh       |
| EPWM7_G1      | 5004 707Eh       |
| EPWM7_G2      | 5008 707Eh       |
| EPWM7_G3      | 500C 707Eh       |
| EPWM8_G0      | 5000 807Eh       |
| EPWM8_G1      | 5004 807Eh       |
| EPWM8_G2      | 5008 807Eh       |
| EPWM8_G3      | 500C 807Eh       |
| EPWM9_G0      | 5000 907Eh       |
| EPWM9_G1      | 5004 907Eh       |
| EPWM9_G2      | 5008 907Eh       |

**Table 3-892. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 907Eh       |
| EPWM10_G0     | 5000 A07Eh       |
| EPWM10_G1     | 5004 A07Eh       |
| EPWM10_G2     | 5008 A07Eh       |
| EPWM10_G3     | 500C A07Eh       |
| EPWM11_G0     | 5000 B07Eh       |
| EPWM11_G1     | 5004 B07Eh       |
| EPWM11_G2     | 5008 B07Eh       |
| EPWM11_G3     | 500C B07Eh       |
| EPWM12_G0     | 5000 C07Eh       |
| EPWM12_G1     | 5004 C07Eh       |
| EPWM12_G2     | 5008 C07Eh       |
| EPWM12_G3     | 500C C07Eh       |
| EPWM13_G0     | 5000 D07Eh       |
| EPWM13_G1     | 5004 D07Eh       |
| EPWM13_G2     | 5008 D07Eh       |
| EPWM13_G3     | 500C D07Eh       |
| EPWM14_G0     | 5000 E07Eh       |
| EPWM14_G1     | 5004 E07Eh       |
| EPWM14_G2     | 5008 E07Eh       |
| EPWM14_G3     | 500C E07Eh       |
| EPWM15_G0     | 5000 F07Eh       |
| EPWM15_G1     | 5004 F07Eh       |
| EPWM15_G2     | 5008 F07Eh       |
| EPWM15_G3     | 500C F07Eh       |
| EPWM16_G0     | 5001 007Eh       |
| EPWM16_G1     | 5005 007Eh       |
| EPWM16_G2     | 5009 007Eh       |
| EPWM16_G3     | 500D 007Eh       |
| EPWM17_G0     | 5001 107Eh       |
| EPWM17_G1     | 5005 107Eh       |
| EPWM17_G2     | 5009 107Eh       |
| EPWM17_G3     | 500D 107Eh       |
| EPWM18_G0     | 5001 207Eh       |
| EPWM18_G1     | 5005 207Eh       |
| EPWM18_G2     | 5009 207Eh       |
| EPWM18_G3     | 500D 207Eh       |
| EPWM19_G0     | 5001 307Eh       |
| EPWM19_G1     | 5005 307Eh       |
| EPWM19_G2     | 5009 307Eh       |
| EPWM19_G3     | 500D 307Eh       |
| EPWM20_G0     | 5001 407Eh       |
| EPWM20_G1     | 5005 407Eh       |
| EPWM20_G2     | 5009 407Eh       |
| EPWM20_G3     | 500D 407Eh       |

**Table 3-892. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 507Eh       |
| EPWM21_G1     | 5005 507Eh       |
| EPWM21_G2     | 5009 507Eh       |
| EPWM21_G3     | 500D 507Eh       |
| EPWM22_G0     | 5001 607Eh       |
| EPWM22_G1     | 5005 607Eh       |
| EPWM22_G2     | 5009 607Eh       |
| EPWM22_G3     | 500D 607Eh       |
| EPWM23_G0     | 5001 707Eh       |
| EPWM23_G1     | 5005 707Eh       |
| EPWM23_G2     | 5009 707Eh       |
| EPWM23_G3     | 500D 707Eh       |
| EPWM24_G0     | 5001 807Eh       |
| EPWM24_G1     | 5005 807Eh       |
| EPWM24_G2     | 5009 807Eh       |
| EPWM24_G3     | 500D 807Eh       |
| EPWM25_G0     | 5001 907Eh       |
| EPWM25_G1     | 5005 907Eh       |
| EPWM25_G2     | 5009 907Eh       |
| EPWM25_G3     | 500D 907Eh       |
| EPWM26_G0     | 5001 A07Eh       |
| EPWM26_G1     | 5005 A07Eh       |
| EPWM26_G2     | 5009 A07Eh       |
| EPWM26_G3     | 500D A07Eh       |
| EPWM27_G0     | 5001 B07Eh       |
| EPWM27_G1     | 5005 B07Eh       |
| EPWM27_G2     | 5009 B07Eh       |
| EPWM27_G3     | 500D B07Eh       |
| EPWM28_G0     | 5001 C07Eh       |
| EPWM28_G1     | 5005 C07Eh       |
| EPWM28_G2     | 5009 C07Eh       |
| EPWM28_G3     | 500D C07Eh       |
| EPWM29_G0     | 5001 D07Eh       |
| EPWM29_G1     | 5005 D07Eh       |
| EPWM29_G2     | 5009 D07Eh       |
| EPWM29_G3     | 500D D07Eh       |
| EPWM30_G0     | 5001 E07Eh       |
| EPWM30_G1     | 5005 E07Eh       |
| EPWM30_G2     | 5009 E07Eh       |
| EPWM30_G3     | 500D E07Eh       |
| EPWM31_G0     | 5001 F07Eh       |
| EPWM31_G1     | 5005 F07Eh       |
| EPWM31_G2     | 5009 F07Eh       |
| EPWM31_G3     | 500D F07Eh       |

**Figure 3-278. EPWM\_HRPWMREV Name Register**

|      |    |    |    |    |    |   |   |
|------|----|----|----|----|----|---|---|
| 15   | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TYPE |    |    |    |    |    |   |   |
| R    |    |    |    |    |    |   |   |
| 3h   |    |    |    |    |    |   |   |
| 7    | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| REV  |    |    |    |    |    |   |   |
| R    |    |    |    |    |    |   |   |
| 0h   |    |    |    |    |    |   |   |

**Table 3-894. EPWM\_HRPWMREV Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                 |
|------|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | TYPE  | R    | 3h    | HRPWM Type Bits: These bits specify the HRPWM type. These bits are changed if the functionality of the HRPWM is changed or any feature is added or removed: |
| 7:0  | REV   | R    | 0h    | HRPWM Silicon Revision Bits: These bits specify the HRPWM revision. These bits are changed if any bug fixes are performed:                                  |



### 3.7.2.28 EPWM\_AQCTLA Register

#### 1 EPWM\_AQCTLA Register (Offset = 80h) [reset = 0h]

Action Qualifier Control Register For Output A .

Return to [Summary Table](#)

**Table 3-895. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0080h       |
| EPWM0_G1      | 5004 0080h       |
| EPWM0_G2      | 5008 0080h       |
| EPWM0_G3      | 500C 0080h       |
| EPWM1_G0      | 5000 1080h       |
| EPWM1_G1      | 5004 1080h       |
| EPWM1_G2      | 5008 1080h       |
| EPWM1_G3      | 500C 1080h       |
| EPWM2_G0      | 5000 2080h       |
| EPWM2_G1      | 5004 2080h       |
| EPWM2_G2      | 5008 2080h       |
| EPWM2_G3      | 500C 2080h       |
| EPWM3_G0      | 5000 3080h       |
| EPWM3_G1      | 5004 3080h       |
| EPWM3_G2      | 5008 3080h       |
| EPWM3_G3      | 500C 3080h       |
| EPWM4_G0      | 5000 4080h       |
| EPWM4_G1      | 5004 4080h       |
| EPWM4_G2      | 5008 4080h       |
| EPWM4_G3      | 500C 4080h       |
| EPWM5_G0      | 5000 5080h       |
| EPWM5_G1      | 5004 5080h       |
| EPWM5_G2      | 5008 5080h       |
| EPWM5_G3      | 500C 5080h       |
| EPWM6_G0      | 5000 6080h       |
| EPWM6_G1      | 5004 6080h       |
| EPWM6_G2      | 5008 6080h       |
| EPWM6_G3      | 500C 6080h       |
| EPWM7_G0      | 5000 7080h       |
| EPWM7_G1      | 5004 7080h       |
| EPWM7_G2      | 5008 7080h       |
| EPWM7_G3      | 500C 7080h       |
| EPWM8_G0      | 5000 8080h       |
| EPWM8_G1      | 5004 8080h       |
| EPWM8_G2      | 5008 8080h       |
| EPWM8_G3      | 500C 8080h       |
| EPWM9_G0      | 5000 9080h       |
| EPWM9_G1      | 5004 9080h       |
| EPWM9_G2      | 5008 9080h       |

**Table 3-895. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9080h       |
| EPWM10_G0     | 5000 A080h       |
| EPWM10_G1     | 5004 A080h       |
| EPWM10_G2     | 5008 A080h       |
| EPWM10_G3     | 500C A080h       |
| EPWM11_G0     | 5000 B080h       |
| EPWM11_G1     | 5004 B080h       |
| EPWM11_G2     | 5008 B080h       |
| EPWM11_G3     | 500C B080h       |
| EPWM12_G0     | 5000 C080h       |
| EPWM12_G1     | 5004 C080h       |
| EPWM12_G2     | 5008 C080h       |
| EPWM12_G3     | 500C C080h       |
| EPWM13_G0     | 5000 D080h       |
| EPWM13_G1     | 5004 D080h       |
| EPWM13_G2     | 5008 D080h       |
| EPWM13_G3     | 500C D080h       |
| EPWM14_G0     | 5000 E080h       |
| EPWM14_G1     | 5004 E080h       |
| EPWM14_G2     | 5008 E080h       |
| EPWM14_G3     | 500C E080h       |
| EPWM15_G0     | 5000 F080h       |
| EPWM15_G1     | 5004 F080h       |
| EPWM15_G2     | 5008 F080h       |
| EPWM15_G3     | 500C F080h       |
| EPWM16_G0     | 5001 0080h       |
| EPWM16_G1     | 5005 0080h       |
| EPWM16_G2     | 5009 0080h       |
| EPWM16_G3     | 500D 0080h       |
| EPWM17_G0     | 5001 1080h       |
| EPWM17_G1     | 5005 1080h       |
| EPWM17_G2     | 5009 1080h       |
| EPWM17_G3     | 500D 1080h       |
| EPWM18_G0     | 5001 2080h       |
| EPWM18_G1     | 5005 2080h       |
| EPWM18_G2     | 5009 2080h       |
| EPWM18_G3     | 500D 2080h       |
| EPWM19_G0     | 5001 3080h       |
| EPWM19_G1     | 5005 3080h       |
| EPWM19_G2     | 5009 3080h       |
| EPWM19_G3     | 500D 3080h       |
| EPWM20_G0     | 5001 4080h       |
| EPWM20_G1     | 5005 4080h       |
| EPWM20_G2     | 5009 4080h       |
| EPWM20_G3     | 500D 4080h       |

**Table 3-895. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5080h       |
| EPWM21_G1     | 5005 5080h       |
| EPWM21_G2     | 5009 5080h       |
| EPWM21_G3     | 500D 5080h       |
| EPWM22_G0     | 5001 6080h       |
| EPWM22_G1     | 5005 6080h       |
| EPWM22_G2     | 5009 6080h       |
| EPWM22_G3     | 500D 6080h       |
| EPWM23_G0     | 5001 7080h       |
| EPWM23_G1     | 5005 7080h       |
| EPWM23_G2     | 5009 7080h       |
| EPWM23_G3     | 500D 7080h       |
| EPWM24_G0     | 5001 8080h       |
| EPWM24_G1     | 5005 8080h       |
| EPWM24_G2     | 5009 8080h       |
| EPWM24_G3     | 500D 8080h       |
| EPWM25_G0     | 5001 9080h       |
| EPWM25_G1     | 5005 9080h       |
| EPWM25_G2     | 5009 9080h       |
| EPWM25_G3     | 500D 9080h       |
| EPWM26_G0     | 5001 A080h       |
| EPWM26_G1     | 5005 A080h       |
| EPWM26_G2     | 5009 A080h       |
| EPWM26_G3     | 500D A080h       |
| EPWM27_G0     | 5001 B080h       |
| EPWM27_G1     | 5005 B080h       |
| EPWM27_G2     | 5009 B080h       |
| EPWM27_G3     | 500D B080h       |
| EPWM28_G0     | 5001 C080h       |
| EPWM28_G1     | 5005 C080h       |
| EPWM28_G2     | 5009 C080h       |
| EPWM28_G3     | 500D C080h       |
| EPWM29_G0     | 5001 D080h       |
| EPWM29_G1     | 5005 D080h       |
| EPWM29_G2     | 5009 D080h       |
| EPWM29_G3     | 500D D080h       |
| EPWM30_G0     | 5001 E080h       |
| EPWM30_G1     | 5005 E080h       |
| EPWM30_G2     | 5009 E080h       |
| EPWM30_G3     | 500D E080h       |
| EPWM31_G0     | 5001 F080h       |
| EPWM31_G1     | 5005 F080h       |
| EPWM31_G2     | 5009 F080h       |
| EPWM31_G3     | 500D F080h       |

**Figure 3-279. EPWM\_AQCTLA Name Register**

| 15         | 14 | 13  | 12 | 11  | 10 | 9   | 8 |
|------------|----|-----|----|-----|----|-----|---|
| RESERVED_1 |    |     |    | CBD |    | CBU |   |
| R          |    |     |    | R/W |    | R/W |   |
| 0h         |    |     |    | 0h  |    | 0h  |   |
| 7          | 6  | 5   | 4  | 3   | 2  | 1   | 0 |
| CAD        |    | CAU |    | PRD |    | ZRO |   |
| R/W        |    | R/W |    | R/W |    | R/W |   |
| 0h         |    | 0h  |    | 0h  |    | 0h  |   |

**Table 3-897. EPWM\_AQCTLA Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                         |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                            |
| 11:10 | CBD        | R/W  | 0h    | Action When TBCTR = CMPB on Down Count<br>Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.<br>00:Do nothing [action disabled]<br>01:Clear: force EPWMxA output low.<br>10:Set: force EPWMxA output high.<br>11:Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low. |
| 9:8   | CBU        | R/W  | 0h    | Action When TBCTR = CMPB on Up Count<br>Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.<br>00:Do nothing [action disabled]<br>01:Clear: force EPWMxA output low.<br>10:Set: force EPWMxA output high.<br>11:Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.   |
| 7:6   | CAD        | R/W  | 0h    | Action When TBCTR = CMPA on Down Count<br>Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.<br>00:Do nothing [action disabled]<br>01:Clear: force EPWMxA output low.<br>10:Set: force EPWMxA output high.<br>11:Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low. |
| 5:4   | CAU        | R/W  | 0h    | Action When TBCTR = CMPA on Up Count<br>Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.<br>00:Do nothing [action disabled]<br>01:Clear: force EPWMxA output low.<br>10:Set: force EPWMxA output high.<br>11:Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.   |
| 3:2   | PRD        | R/W  | 0h    | Action When TBCTR = TBPRD<br>Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.<br>00:Do nothing [action disabled]<br>01:Clear: force EPWMxA output low.<br>10:Set: force EPWMxA output high.<br>11:Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.              |

**Table 3-897. EPWM\_AQCTLA Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                   |
|-----|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0 | ZRO   | R/W  | 0h    | <p>Action When TBCTR = 0</p> <p>Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.</p> <p>00:Do nothing [action disabled]</p> <p>01:Clear: force EPWMxA output low.</p> <p>10:Set: force EPWMxA output high.</p> <p>11:Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.</p> |

### 3.7.2.29 EPWM\_AQCTLA2 Register

#### 1 EPWM\_AQCTLA2 Register (Offset = 82h) [reset = 0h]

Additional Action Qualifier Control Register For Output A .

Return to [Summary Table](#)

**Table 3-898. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0082h       |
| EPWM0_G1      | 5004 0082h       |
| EPWM0_G2      | 5008 0082h       |
| EPWM0_G3      | 500C 0082h       |
| EPWM1_G0      | 5000 1082h       |
| EPWM1_G1      | 5004 1082h       |
| EPWM1_G2      | 5008 1082h       |
| EPWM1_G3      | 500C 1082h       |
| EPWM2_G0      | 5000 2082h       |
| EPWM2_G1      | 5004 2082h       |
| EPWM2_G2      | 5008 2082h       |
| EPWM2_G3      | 500C 2082h       |
| EPWM3_G0      | 5000 3082h       |
| EPWM3_G1      | 5004 3082h       |
| EPWM3_G2      | 5008 3082h       |
| EPWM3_G3      | 500C 3082h       |
| EPWM4_G0      | 5000 4082h       |
| EPWM4_G1      | 5004 4082h       |
| EPWM4_G2      | 5008 4082h       |
| EPWM4_G3      | 500C 4082h       |
| EPWM5_G0      | 5000 5082h       |
| EPWM5_G1      | 5004 5082h       |
| EPWM5_G2      | 5008 5082h       |
| EPWM5_G3      | 500C 5082h       |
| EPWM6_G0      | 5000 6082h       |
| EPWM6_G1      | 5004 6082h       |
| EPWM6_G2      | 5008 6082h       |
| EPWM6_G3      | 500C 6082h       |
| EPWM7_G0      | 5000 7082h       |
| EPWM7_G1      | 5004 7082h       |
| EPWM7_G2      | 5008 7082h       |
| EPWM7_G3      | 500C 7082h       |
| EPWM8_G0      | 5000 8082h       |
| EPWM8_G1      | 5004 8082h       |
| EPWM8_G2      | 5008 8082h       |
| EPWM8_G3      | 500C 8082h       |
| EPWM9_G0      | 5000 9082h       |
| EPWM9_G1      | 5004 9082h       |
| EPWM9_G2      | 5008 9082h       |

**Table 3-898. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9082h       |
| EPWM10_G0     | 5000 A082h       |
| EPWM10_G1     | 5004 A082h       |
| EPWM10_G2     | 5008 A082h       |
| EPWM10_G3     | 500C A082h       |
| EPWM11_G0     | 5000 B082h       |
| EPWM11_G1     | 5004 B082h       |
| EPWM11_G2     | 5008 B082h       |
| EPWM11_G3     | 500C B082h       |
| EPWM12_G0     | 5000 C082h       |
| EPWM12_G1     | 5004 C082h       |
| EPWM12_G2     | 5008 C082h       |
| EPWM12_G3     | 500C C082h       |
| EPWM13_G0     | 5000 D082h       |
| EPWM13_G1     | 5004 D082h       |
| EPWM13_G2     | 5008 D082h       |
| EPWM13_G3     | 500C D082h       |
| EPWM14_G0     | 5000 E082h       |
| EPWM14_G1     | 5004 E082h       |
| EPWM14_G2     | 5008 E082h       |
| EPWM14_G3     | 500C E082h       |
| EPWM15_G0     | 5000 F082h       |
| EPWM15_G1     | 5004 F082h       |
| EPWM15_G2     | 5008 F082h       |
| EPWM15_G3     | 500C F082h       |
| EPWM16_G0     | 5001 0082h       |
| EPWM16_G1     | 5005 0082h       |
| EPWM16_G2     | 5009 0082h       |
| EPWM16_G3     | 500D 0082h       |
| EPWM17_G0     | 5001 1082h       |
| EPWM17_G1     | 5005 1082h       |
| EPWM17_G2     | 5009 1082h       |
| EPWM17_G3     | 500D 1082h       |
| EPWM18_G0     | 5001 2082h       |
| EPWM18_G1     | 5005 2082h       |
| EPWM18_G2     | 5009 2082h       |
| EPWM18_G3     | 500D 2082h       |
| EPWM19_G0     | 5001 3082h       |
| EPWM19_G1     | 5005 3082h       |
| EPWM19_G2     | 5009 3082h       |
| EPWM19_G3     | 500D 3082h       |
| EPWM20_G0     | 5001 4082h       |
| EPWM20_G1     | 5005 4082h       |
| EPWM20_G2     | 5009 4082h       |
| EPWM20_G3     | 500D 4082h       |

**Table 3-898. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5082h       |
| EPWM21_G1     | 5005 5082h       |
| EPWM21_G2     | 5009 5082h       |
| EPWM21_G3     | 500D 5082h       |
| EPWM22_G0     | 5001 6082h       |
| EPWM22_G1     | 5005 6082h       |
| EPWM22_G2     | 5009 6082h       |
| EPWM22_G3     | 500D 6082h       |
| EPWM23_G0     | 5001 7082h       |
| EPWM23_G1     | 5005 7082h       |
| EPWM23_G2     | 5009 7082h       |
| EPWM23_G3     | 500D 7082h       |
| EPWM24_G0     | 5001 8082h       |
| EPWM24_G1     | 5005 8082h       |
| EPWM24_G2     | 5009 8082h       |
| EPWM24_G3     | 500D 8082h       |
| EPWM25_G0     | 5001 9082h       |
| EPWM25_G1     | 5005 9082h       |
| EPWM25_G2     | 5009 9082h       |
| EPWM25_G3     | 500D 9082h       |
| EPWM26_G0     | 5001 A082h       |
| EPWM26_G1     | 5005 A082h       |
| EPWM26_G2     | 5009 A082h       |
| EPWM26_G3     | 500D A082h       |
| EPWM27_G0     | 5001 B082h       |
| EPWM27_G1     | 5005 B082h       |
| EPWM27_G2     | 5009 B082h       |
| EPWM27_G3     | 500D B082h       |
| EPWM28_G0     | 5001 C082h       |
| EPWM28_G1     | 5005 C082h       |
| EPWM28_G2     | 5009 C082h       |
| EPWM28_G3     | 500D C082h       |
| EPWM29_G0     | 5001 D082h       |
| EPWM29_G1     | 5005 D082h       |
| EPWM29_G2     | 5009 D082h       |
| EPWM29_G3     | 500D D082h       |
| EPWM30_G0     | 5001 E082h       |
| EPWM30_G1     | 5005 E082h       |
| EPWM30_G2     | 5009 E082h       |
| EPWM30_G3     | 500D E082h       |
| EPWM31_G0     | 5001 F082h       |
| EPWM31_G1     | 5005 F082h       |
| EPWM31_G2     | 5009 F082h       |
| EPWM31_G3     | 500D F082h       |



**Figure 3-280. EPWM\_AQCTLA2 Name Register**

|            |     |    |     |    |     |   |   |
|------------|-----|----|-----|----|-----|---|---|
| 15         | 14  | 13 | 12  | 11 | 10  | 9 | 8 |
| RESERVED_1 |     |    |     |    |     |   |   |
| R          |     |    |     |    |     |   |   |
| 0h         |     |    |     |    |     |   |   |
| 7          | 6   | 5  | 4   | 3  | 2   | 1 | 0 |
| T2D        | T2U |    | T1D |    | T1U |   |   |
| R/W        | R/W |    | R/W |    | R/W |   |   |
| 0h         | 0h  |    | 0h  |    | 0h  |   |   |

**Table 3-900. EPWM\_AQCTLA2 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                               |
|------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                  |
| 7:6  | T2D        | R/W  | 0h    | Action when event occurs on T2 in DOWN-Count<br>Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.<br>00:Do nothing [action disabled]<br>01:Clear: force EPWMxA output low.<br>10:Set: force EPWMxA output high.<br>11:Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low. |
| 5:4  | T2U        | R/W  | 0h    | Action when event occurs on T2 in UP-Count<br>Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.<br>00:Do nothing [action disabled]<br>01:Clear: force EPWMxA output low.<br>10:Set: force EPWMxA output high.<br>11:Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.   |
| 3:2  | T1D        | R/W  | 0h    | Action when event occurs on T1 in DOWN-Count<br>Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.<br>00:Do nothing [action disabled]<br>01:Clear: force EPWMxA output low.<br>10:Set: force EPWMxA output high.<br>11:Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low. |
| 1:0  | T1U        | R/W  | 0h    | Action when event occurs on T1 in UP-Count<br>Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.<br>00:Do nothing [action disabled]<br>01:Clear: force EPWMxA output low.<br>10:Set: force EPWMxA output high.<br>11:Toggle EPWMxA output: low output signal will be forced high, and a high signal will be forced low.   |

### 3.7.2.30 EPWM\_AQCTLB Register

#### 1 EPWM\_AQCTLB Register (Offset = 84h) [reset = 0h]

Action Qualifier Control Register For Output B .

Return to [Summary Table](#)

**Table 3-901. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0084h       |
| EPWM0_G1      | 5004 0084h       |
| EPWM0_G2      | 5008 0084h       |
| EPWM0_G3      | 500C 0084h       |
| EPWM1_G0      | 5000 1084h       |
| EPWM1_G1      | 5004 1084h       |
| EPWM1_G2      | 5008 1084h       |
| EPWM1_G3      | 500C 1084h       |
| EPWM2_G0      | 5000 2084h       |
| EPWM2_G1      | 5004 2084h       |
| EPWM2_G2      | 5008 2084h       |
| EPWM2_G3      | 500C 2084h       |
| EPWM3_G0      | 5000 3084h       |
| EPWM3_G1      | 5004 3084h       |
| EPWM3_G2      | 5008 3084h       |
| EPWM3_G3      | 500C 3084h       |
| EPWM4_G0      | 5000 4084h       |
| EPWM4_G1      | 5004 4084h       |
| EPWM4_G2      | 5008 4084h       |
| EPWM4_G3      | 500C 4084h       |
| EPWM5_G0      | 5000 5084h       |
| EPWM5_G1      | 5004 5084h       |
| EPWM5_G2      | 5008 5084h       |
| EPWM5_G3      | 500C 5084h       |
| EPWM6_G0      | 5000 6084h       |
| EPWM6_G1      | 5004 6084h       |
| EPWM6_G2      | 5008 6084h       |
| EPWM6_G3      | 500C 6084h       |
| EPWM7_G0      | 5000 7084h       |
| EPWM7_G1      | 5004 7084h       |
| EPWM7_G2      | 5008 7084h       |
| EPWM7_G3      | 500C 7084h       |
| EPWM8_G0      | 5000 8084h       |
| EPWM8_G1      | 5004 8084h       |
| EPWM8_G2      | 5008 8084h       |
| EPWM8_G3      | 500C 8084h       |
| EPWM9_G0      | 5000 9084h       |
| EPWM9_G1      | 5004 9084h       |
| EPWM9_G2      | 5008 9084h       |

**Table 3-901. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9084h       |
| EPWM10_G0     | 5000 A084h       |
| EPWM10_G1     | 5004 A084h       |
| EPWM10_G2     | 5008 A084h       |
| EPWM10_G3     | 500C A084h       |
| EPWM11_G0     | 5000 B084h       |
| EPWM11_G1     | 5004 B084h       |
| EPWM11_G2     | 5008 B084h       |
| EPWM11_G3     | 500C B084h       |
| EPWM12_G0     | 5000 C084h       |
| EPWM12_G1     | 5004 C084h       |
| EPWM12_G2     | 5008 C084h       |
| EPWM12_G3     | 500C C084h       |
| EPWM13_G0     | 5000 D084h       |
| EPWM13_G1     | 5004 D084h       |
| EPWM13_G2     | 5008 D084h       |
| EPWM13_G3     | 500C D084h       |
| EPWM14_G0     | 5000 E084h       |
| EPWM14_G1     | 5004 E084h       |
| EPWM14_G2     | 5008 E084h       |
| EPWM14_G3     | 500C E084h       |
| EPWM15_G0     | 5000 F084h       |
| EPWM15_G1     | 5004 F084h       |
| EPWM15_G2     | 5008 F084h       |
| EPWM15_G3     | 500C F084h       |
| EPWM16_G0     | 5001 0084h       |
| EPWM16_G1     | 5005 0084h       |
| EPWM16_G2     | 5009 0084h       |
| EPWM16_G3     | 500D 0084h       |
| EPWM17_G0     | 5001 1084h       |
| EPWM17_G1     | 5005 1084h       |
| EPWM17_G2     | 5009 1084h       |
| EPWM17_G3     | 500D 1084h       |
| EPWM18_G0     | 5001 2084h       |
| EPWM18_G1     | 5005 2084h       |
| EPWM18_G2     | 5009 2084h       |
| EPWM18_G3     | 500D 2084h       |
| EPWM19_G0     | 5001 3084h       |
| EPWM19_G1     | 5005 3084h       |
| EPWM19_G2     | 5009 3084h       |
| EPWM19_G3     | 500D 3084h       |
| EPWM20_G0     | 5001 4084h       |
| EPWM20_G1     | 5005 4084h       |
| EPWM20_G2     | 5009 4084h       |
| EPWM20_G3     | 500D 4084h       |

**Table 3-901. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5084h       |
| EPWM21_G1     | 5005 5084h       |
| EPWM21_G2     | 5009 5084h       |
| EPWM21_G3     | 500D 5084h       |
| EPWM22_G0     | 5001 6084h       |
| EPWM22_G1     | 5005 6084h       |
| EPWM22_G2     | 5009 6084h       |
| EPWM22_G3     | 500D 6084h       |
| EPWM23_G0     | 5001 7084h       |
| EPWM23_G1     | 5005 7084h       |
| EPWM23_G2     | 5009 7084h       |
| EPWM23_G3     | 500D 7084h       |
| EPWM24_G0     | 5001 8084h       |
| EPWM24_G1     | 5005 8084h       |
| EPWM24_G2     | 5009 8084h       |
| EPWM24_G3     | 500D 8084h       |
| EPWM25_G0     | 5001 9084h       |
| EPWM25_G1     | 5005 9084h       |
| EPWM25_G2     | 5009 9084h       |
| EPWM25_G3     | 500D 9084h       |
| EPWM26_G0     | 5001 A084h       |
| EPWM26_G1     | 5005 A084h       |
| EPWM26_G2     | 5009 A084h       |
| EPWM26_G3     | 500D A084h       |
| EPWM27_G0     | 5001 B084h       |
| EPWM27_G1     | 5005 B084h       |
| EPWM27_G2     | 5009 B084h       |
| EPWM27_G3     | 500D B084h       |
| EPWM28_G0     | 5001 C084h       |
| EPWM28_G1     | 5005 C084h       |
| EPWM28_G2     | 5009 C084h       |
| EPWM28_G3     | 500D C084h       |
| EPWM29_G0     | 5001 D084h       |
| EPWM29_G1     | 5005 D084h       |
| EPWM29_G2     | 5009 D084h       |
| EPWM29_G3     | 500D D084h       |
| EPWM30_G0     | 5001 E084h       |
| EPWM30_G1     | 5005 E084h       |
| EPWM30_G2     | 5009 E084h       |
| EPWM30_G3     | 500D E084h       |
| EPWM31_G0     | 5001 F084h       |
| EPWM31_G1     | 5005 F084h       |
| EPWM31_G2     | 5009 F084h       |
| EPWM31_G3     | 500D F084h       |

**Figure 3-281. EPWM\_AQCTLB Name Register**

| 15         | 14 | 13  | 12 | 11  | 10 | 9   | 8 |
|------------|----|-----|----|-----|----|-----|---|
| RESERVED_1 |    |     |    | CBD |    | CBU |   |
| R          |    |     |    | R/W |    | R/W |   |
| 0h         |    |     |    | 0h  |    | 0h  |   |
| 7          | 6  | 5   | 4  | 3   | 2  | 1   | 0 |
| CAD        |    | CAU |    | PRD |    | ZRO |   |
| R/W        |    | R/W |    | R/W |    | R/W |   |
| 0h         |    | 0h  |    | 0h  |    | 0h  |   |

**Table 3-903. EPWM\_AQCTLB Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                         |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                            |
| 11:10 | CBD        | R/W  | 0h    | Action When TBCTR = CMPB on Down Count<br>Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.<br>00:Do nothing [action disabled]<br>01:Clear: force EPWMxB output low.<br>10:Set: force EPWMxB output high.<br>11:Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low. |
| 9:8   | CBU        | R/W  | 0h    | Action When TBCTR = CMPB on Up Count<br>Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.<br>00:Do nothing [action disabled]<br>01:Clear: force EPWMxB output low.<br>10:Set: force EPWMxB output high.<br>11:Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.   |
| 7:6   | CAD        | R/W  | 0h    | Action When TBCTR = CMPA on Down Count<br>Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.<br>00:Do nothing [action disabled]<br>01:Clear: force EPWMxB output low.<br>10:Set: force EPWMxB output high.<br>11:Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low. |
| 5:4   | CAU        | R/W  | 0h    | Action When TBCTR = CMPA on Up Count<br>Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.<br>00:Do nothing [action disabled]<br>01:Clear: force EPWMxB output low.<br>10:Set: force EPWMxB output high.<br>11:Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.   |
| 3:2   | PRD        | R/W  | 0h    | Action When TBCTR = TBPRD<br>Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.<br>00:Do nothing [action disabled]<br>01:Clear: force EPWMxB output low.<br>10:Set: force EPWMxB output high.<br>11:Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.              |

**Table 3-903. EPWM\_AQCTLB Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                   |
|-----|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0 | ZRO   | R/W  | 0h    | <p>Action When TBCTR = 0</p> <p>Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.</p> <p>00:Do nothing [action disabled]</p> <p>01:Clear: force EPWMxB output low.</p> <p>10:Set: force EPWMxB output high.</p> <p>11:Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.</p> |

### 3.7.2.31 EPWM\_AQCTLB2 Register

#### 1 EPWM\_AQCTLB2 Register (Offset = 86h) [reset = 0h]

Additional Action Qualifier Control Register For Output B .

Return to [Summary Table](#)

**Table 3-904. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0086h       |
| EPWM0_G1      | 5004 0086h       |
| EPWM0_G2      | 5008 0086h       |
| EPWM0_G3      | 500C 0086h       |
| EPWM1_G0      | 5000 1086h       |
| EPWM1_G1      | 5004 1086h       |
| EPWM1_G2      | 5008 1086h       |
| EPWM1_G3      | 500C 1086h       |
| EPWM2_G0      | 5000 2086h       |
| EPWM2_G1      | 5004 2086h       |
| EPWM2_G2      | 5008 2086h       |
| EPWM2_G3      | 500C 2086h       |
| EPWM3_G0      | 5000 3086h       |
| EPWM3_G1      | 5004 3086h       |
| EPWM3_G2      | 5008 3086h       |
| EPWM3_G3      | 500C 3086h       |
| EPWM4_G0      | 5000 4086h       |
| EPWM4_G1      | 5004 4086h       |
| EPWM4_G2      | 5008 4086h       |
| EPWM4_G3      | 500C 4086h       |
| EPWM5_G0      | 5000 5086h       |
| EPWM5_G1      | 5004 5086h       |
| EPWM5_G2      | 5008 5086h       |
| EPWM5_G3      | 500C 5086h       |
| EPWM6_G0      | 5000 6086h       |
| EPWM6_G1      | 5004 6086h       |
| EPWM6_G2      | 5008 6086h       |
| EPWM6_G3      | 500C 6086h       |
| EPWM7_G0      | 5000 7086h       |
| EPWM7_G1      | 5004 7086h       |
| EPWM7_G2      | 5008 7086h       |
| EPWM7_G3      | 500C 7086h       |
| EPWM8_G0      | 5000 8086h       |
| EPWM8_G1      | 5004 8086h       |
| EPWM8_G2      | 5008 8086h       |
| EPWM8_G3      | 500C 8086h       |
| EPWM9_G0      | 5000 9086h       |
| EPWM9_G1      | 5004 9086h       |
| EPWM9_G2      | 5008 9086h       |

**Table 3-904. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9086h       |
| EPWM10_G0     | 5000 A086h       |
| EPWM10_G1     | 5004 A086h       |
| EPWM10_G2     | 5008 A086h       |
| EPWM10_G3     | 500C A086h       |
| EPWM11_G0     | 5000 B086h       |
| EPWM11_G1     | 5004 B086h       |
| EPWM11_G2     | 5008 B086h       |
| EPWM11_G3     | 500C B086h       |
| EPWM12_G0     | 5000 C086h       |
| EPWM12_G1     | 5004 C086h       |
| EPWM12_G2     | 5008 C086h       |
| EPWM12_G3     | 500C C086h       |
| EPWM13_G0     | 5000 D086h       |
| EPWM13_G1     | 5004 D086h       |
| EPWM13_G2     | 5008 D086h       |
| EPWM13_G3     | 500C D086h       |
| EPWM14_G0     | 5000 E086h       |
| EPWM14_G1     | 5004 E086h       |
| EPWM14_G2     | 5008 E086h       |
| EPWM14_G3     | 500C E086h       |
| EPWM15_G0     | 5000 F086h       |
| EPWM15_G1     | 5004 F086h       |
| EPWM15_G2     | 5008 F086h       |
| EPWM15_G3     | 500C F086h       |
| EPWM16_G0     | 5001 0086h       |
| EPWM16_G1     | 5005 0086h       |
| EPWM16_G2     | 5009 0086h       |
| EPWM16_G3     | 500D 0086h       |
| EPWM17_G0     | 5001 1086h       |
| EPWM17_G1     | 5005 1086h       |
| EPWM17_G2     | 5009 1086h       |
| EPWM17_G3     | 500D 1086h       |
| EPWM18_G0     | 5001 2086h       |
| EPWM18_G1     | 5005 2086h       |
| EPWM18_G2     | 5009 2086h       |
| EPWM18_G3     | 500D 2086h       |
| EPWM19_G0     | 5001 3086h       |
| EPWM19_G1     | 5005 3086h       |
| EPWM19_G2     | 5009 3086h       |
| EPWM19_G3     | 500D 3086h       |
| EPWM20_G0     | 5001 4086h       |
| EPWM20_G1     | 5005 4086h       |
| EPWM20_G2     | 5009 4086h       |
| EPWM20_G3     | 500D 4086h       |



**Table 3-904. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5086h       |
| EPWM21_G1     | 5005 5086h       |
| EPWM21_G2     | 5009 5086h       |
| EPWM21_G3     | 500D 5086h       |
| EPWM22_G0     | 5001 6086h       |
| EPWM22_G1     | 5005 6086h       |
| EPWM22_G2     | 5009 6086h       |
| EPWM22_G3     | 500D 6086h       |
| EPWM23_G0     | 5001 7086h       |
| EPWM23_G1     | 5005 7086h       |
| EPWM23_G2     | 5009 7086h       |
| EPWM23_G3     | 500D 7086h       |
| EPWM24_G0     | 5001 8086h       |
| EPWM24_G1     | 5005 8086h       |
| EPWM24_G2     | 5009 8086h       |
| EPWM24_G3     | 500D 8086h       |
| EPWM25_G0     | 5001 9086h       |
| EPWM25_G1     | 5005 9086h       |
| EPWM25_G2     | 5009 9086h       |
| EPWM25_G3     | 500D 9086h       |
| EPWM26_G0     | 5001 A086h       |
| EPWM26_G1     | 5005 A086h       |
| EPWM26_G2     | 5009 A086h       |
| EPWM26_G3     | 500D A086h       |
| EPWM27_G0     | 5001 B086h       |
| EPWM27_G1     | 5005 B086h       |
| EPWM27_G2     | 5009 B086h       |
| EPWM27_G3     | 500D B086h       |
| EPWM28_G0     | 5001 C086h       |
| EPWM28_G1     | 5005 C086h       |
| EPWM28_G2     | 5009 C086h       |
| EPWM28_G3     | 500D C086h       |
| EPWM29_G0     | 5001 D086h       |
| EPWM29_G1     | 5005 D086h       |
| EPWM29_G2     | 5009 D086h       |
| EPWM29_G3     | 500D D086h       |
| EPWM30_G0     | 5001 E086h       |
| EPWM30_G1     | 5005 E086h       |
| EPWM30_G2     | 5009 E086h       |
| EPWM30_G3     | 500D E086h       |
| EPWM31_G0     | 5001 F086h       |
| EPWM31_G1     | 5005 F086h       |
| EPWM31_G2     | 5009 F086h       |
| EPWM31_G3     | 500D F086h       |

**Figure 3-282. EPWM\_AQCTLB2 Name Register**

|            |     |    |     |    |     |   |   |
|------------|-----|----|-----|----|-----|---|---|
| 15         | 14  | 13 | 12  | 11 | 10  | 9 | 8 |
| RESERVED_1 |     |    |     |    |     |   |   |
| R          |     |    |     |    |     |   |   |
| 0h         |     |    |     |    |     |   |   |
| 7          | 6   | 5  | 4   | 3  | 2   | 1 | 0 |
| T2D        | T2U |    | T1D |    | T1U |   |   |
| R/W        | R/W |    | R/W |    | R/W |   |   |
| 0h         | 0h  |    | 0h  |    | 0h  |   |   |

**Table 3-906. EPWM\_AQCTLB2 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                               |
|------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                  |
| 7:6  | T2D        | R/W  | 0h    | Action when event occurs on T2 in DOWN-Count<br>Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.<br>00:Do nothing [action disabled]<br>01:Clear: force EPWMxB output low.<br>10:Set: force EPWMxB output high.<br>11:Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low. |
| 5:4  | T2U        | R/W  | 0h    | Action when event occurs on T2 in UP-Count<br>Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.<br>00:Do nothing [action disabled]<br>01:Clear: force EPWMxB output low.<br>10:Set: force EPWMxB output high.<br>11:Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.   |
| 3:2  | T1D        | R/W  | 0h    | Action when event occurs on T1 in DOWN-Count<br>Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.<br>00:Do nothing [action disabled]<br>01:Clear: force EPWMxB output low.<br>10:Set: force EPWMxB output high.<br>11:Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low. |
| 1:0  | T1U        | R/W  | 0h    | Action when event occurs on T1 in UP-Count<br>Note: By definition, in count up-down mode when the counter equals 0 the direction is defined as 1 or counting up.<br>00:Do nothing [action disabled]<br>01:Clear: force EPWMxB output low.<br>10:Set: force EPWMxB output high.<br>11:Toggle EPWMxB output: low output signal will be forced high, and a high signal will be forced low.   |

### 3.7.2.32 EPWM\_AQSFRC Register

#### 1 EPWM\_AQSFRC Register (Offset = 8Eh) [reset = 0h]

Action Qualifier Software Force Register.

Return to [Summary Table](#)

**Table 3-907. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 008Eh       |
| EPWM0_G1      | 5004 008Eh       |
| EPWM0_G2      | 5008 008Eh       |
| EPWM0_G3      | 500C 008Eh       |
| EPWM1_G0      | 5000 108Eh       |
| EPWM1_G1      | 5004 108Eh       |
| EPWM1_G2      | 5008 108Eh       |
| EPWM1_G3      | 500C 108Eh       |
| EPWM2_G0      | 5000 208Eh       |
| EPWM2_G1      | 5004 208Eh       |
| EPWM2_G2      | 5008 208Eh       |
| EPWM2_G3      | 500C 208Eh       |
| EPWM3_G0      | 5000 308Eh       |
| EPWM3_G1      | 5004 308Eh       |
| EPWM3_G2      | 5008 308Eh       |
| EPWM3_G3      | 500C 308Eh       |
| EPWM4_G0      | 5000 408Eh       |
| EPWM4_G1      | 5004 408Eh       |
| EPWM4_G2      | 5008 408Eh       |
| EPWM4_G3      | 500C 408Eh       |
| EPWM5_G0      | 5000 508Eh       |
| EPWM5_G1      | 5004 508Eh       |
| EPWM5_G2      | 5008 508Eh       |
| EPWM5_G3      | 500C 508Eh       |
| EPWM6_G0      | 5000 608Eh       |
| EPWM6_G1      | 5004 608Eh       |
| EPWM6_G2      | 5008 608Eh       |
| EPWM6_G3      | 500C 608Eh       |
| EPWM7_G0      | 5000 708Eh       |
| EPWM7_G1      | 5004 708Eh       |
| EPWM7_G2      | 5008 708Eh       |
| EPWM7_G3      | 500C 708Eh       |
| EPWM8_G0      | 5000 808Eh       |
| EPWM8_G1      | 5004 808Eh       |
| EPWM8_G2      | 5008 808Eh       |
| EPWM8_G3      | 500C 808Eh       |
| EPWM9_G0      | 5000 908Eh       |
| EPWM9_G1      | 5004 908Eh       |
| EPWM9_G2      | 5008 908Eh       |

**Table 3-907. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 908Eh       |
| EPWM10_G0     | 5000 A08Eh       |
| EPWM10_G1     | 5004 A08Eh       |
| EPWM10_G2     | 5008 A08Eh       |
| EPWM10_G3     | 500C A08Eh       |
| EPWM11_G0     | 5000 B08Eh       |
| EPWM11_G1     | 5004 B08Eh       |
| EPWM11_G2     | 5008 B08Eh       |
| EPWM11_G3     | 500C B08Eh       |
| EPWM12_G0     | 5000 C08Eh       |
| EPWM12_G1     | 5004 C08Eh       |
| EPWM12_G2     | 5008 C08Eh       |
| EPWM12_G3     | 500C C08Eh       |
| EPWM13_G0     | 5000 D08Eh       |
| EPWM13_G1     | 5004 D08Eh       |
| EPWM13_G2     | 5008 D08Eh       |
| EPWM13_G3     | 500C D08Eh       |
| EPWM14_G0     | 5000 E08Eh       |
| EPWM14_G1     | 5004 E08Eh       |
| EPWM14_G2     | 5008 E08Eh       |
| EPWM14_G3     | 500C E08Eh       |
| EPWM15_G0     | 5000 F08Eh       |
| EPWM15_G1     | 5004 F08Eh       |
| EPWM15_G2     | 5008 F08Eh       |
| EPWM15_G3     | 500C F08Eh       |
| EPWM16_G0     | 5001 008Eh       |
| EPWM16_G1     | 5005 008Eh       |
| EPWM16_G2     | 5009 008Eh       |
| EPWM16_G3     | 500D 008Eh       |
| EPWM17_G0     | 5001 108Eh       |
| EPWM17_G1     | 5005 108Eh       |
| EPWM17_G2     | 5009 108Eh       |
| EPWM17_G3     | 500D 108Eh       |
| EPWM18_G0     | 5001 208Eh       |
| EPWM18_G1     | 5005 208Eh       |
| EPWM18_G2     | 5009 208Eh       |
| EPWM18_G3     | 500D 208Eh       |
| EPWM19_G0     | 5001 308Eh       |
| EPWM19_G1     | 5005 308Eh       |
| EPWM19_G2     | 5009 308Eh       |
| EPWM19_G3     | 500D 308Eh       |
| EPWM20_G0     | 5001 408Eh       |
| EPWM20_G1     | 5005 408Eh       |
| EPWM20_G2     | 5009 408Eh       |
| EPWM20_G3     | 500D 408Eh       |

**Table 3-907. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 508Eh       |
| EPWM21_G1     | 5005 508Eh       |
| EPWM21_G2     | 5009 508Eh       |
| EPWM21_G3     | 500D 508Eh       |
| EPWM22_G0     | 5001 608Eh       |
| EPWM22_G1     | 5005 608Eh       |
| EPWM22_G2     | 5009 608Eh       |
| EPWM22_G3     | 500D 608Eh       |
| EPWM23_G0     | 5001 708Eh       |
| EPWM23_G1     | 5005 708Eh       |
| EPWM23_G2     | 5009 708Eh       |
| EPWM23_G3     | 500D 708Eh       |
| EPWM24_G0     | 5001 808Eh       |
| EPWM24_G1     | 5005 808Eh       |
| EPWM24_G2     | 5009 808Eh       |
| EPWM24_G3     | 500D 808Eh       |
| EPWM25_G0     | 5001 908Eh       |
| EPWM25_G1     | 5005 908Eh       |
| EPWM25_G2     | 5009 908Eh       |
| EPWM25_G3     | 500D 908Eh       |
| EPWM26_G0     | 5001 A08Eh       |
| EPWM26_G1     | 5005 A08Eh       |
| EPWM26_G2     | 5009 A08Eh       |
| EPWM26_G3     | 500D A08Eh       |
| EPWM27_G0     | 5001 B08Eh       |
| EPWM27_G1     | 5005 B08Eh       |
| EPWM27_G2     | 5009 B08Eh       |
| EPWM27_G3     | 500D B08Eh       |
| EPWM28_G0     | 5001 C08Eh       |
| EPWM28_G1     | 5005 C08Eh       |
| EPWM28_G2     | 5009 C08Eh       |
| EPWM28_G3     | 500D C08Eh       |
| EPWM29_G0     | 5001 D08Eh       |
| EPWM29_G1     | 5005 D08Eh       |
| EPWM29_G2     | 5009 D08Eh       |
| EPWM29_G3     | 500D D08Eh       |
| EPWM30_G0     | 5001 E08Eh       |
| EPWM30_G1     | 5005 E08Eh       |
| EPWM30_G2     | 5009 E08Eh       |
| EPWM30_G3     | 500D E08Eh       |
| EPWM31_G0     | 5001 F08Eh       |
| EPWM31_G1     | 5005 F08Eh       |
| EPWM31_G2     | 5009 F08Eh       |
| EPWM31_G3     | 500D F08Eh       |

**Figure 3-283. EPWM\_AQSFR Name Register**

|            |        |        |    |        |        |   |   |
|------------|--------|--------|----|--------|--------|---|---|
| 15         | 14     | 13     | 12 | 11     | 10     | 9 | 8 |
| RESERVED_1 |        |        |    |        |        |   |   |
| R          |        |        |    |        |        |   |   |
| 0h         |        |        |    |        |        |   |   |
| 7          | 6      | 5      | 4  | 3      | 2      | 1 | 0 |
| RLDCSF     | OTSFB  | ACTSFB |    | OTSFA  | ACTSFA |   |   |
| R/W        | R/W1TS | R/W    |    | R/W1TS | R/W    |   |   |
| 0h         | 0h     | 0h     |    | 0h     | 0h     |   |   |

**Table 3-909. EPWM\_AQSFR Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                    |
|------|------------|--------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                       |
| 7:6  | RLDCSF     | R/W    | 0h    | AQCSFRC Active Register Reload From Shadow Options<br>00:Load on event counter equals zero<br>01:Load on event counter equals period<br>10:Load on event counter equals zero or counter equals period<br>11:Load immediately [the active register is directly accessed by the CPU and is not loaded from the shadow register].                                 |
| 5    | OTSFB      | R/W1TS | 0h    | One-Time Software Forced Event on Output B<br>0:Writing a 0 [zero] has no effect. Always reads back a 0. This bit is auto cleared once a write to this register is complete [i.e., a forced event is initiated.]. This is a one-shot forced event. It can be overridden by another subsequent event on output B.<br>1:Initiates a single software forced event |
| 4:3  | ACTSFB     | R/W    | 0h    | Action When One-Time Software Force B is Invoked<br>00:Does nothing [action disabled]<br>01:Clear [low]<br>10:Set [high]<br>11:Toggle [Low -> High, High -> Low]<br>Note: This action is not qualified by counter direction [CNT_dir]                                                                                                                          |
| 2    | OTSFA      | R/W1TS | 0h    | One-Time Software Forced Event on Output A<br>0:Writing a 0 [zero] has no effect. Always reads back a 0. This bit is auto cleared once a write to this register is complete [ i.e., a forced event is initiated]. This is a one-shot forced event. It can be overridden by another subsequent event on output A.<br>1:Initiates a single software forced event |
| 1:0  | ACTSFA     | R/W    | 0h    | Action When One-Time Software Force A Is Invoked<br>00:Does nothing [action disabled]<br>01:Clear [low]<br>10:Set [high]<br>11:Toggle [Low -> High, High -> Low]<br>Note: This action is not qualified by counter direction [CNT_dir]                                                                                                                          |

### 3.7.2.33 EPWM\_AQCSFRC Register

#### 1 EPWM\_AQCSFRC Register (Offset = 92h) [reset = 0h]

Action Qualifier Continuous S/W Force Register .

Return to [Summary Table](#)

**Table 3-910. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0092h       |
| EPWM0_G1      | 5004 0092h       |
| EPWM0_G2      | 5008 0092h       |
| EPWM0_G3      | 500C 0092h       |
| EPWM1_G0      | 5000 1092h       |
| EPWM1_G1      | 5004 1092h       |
| EPWM1_G2      | 5008 1092h       |
| EPWM1_G3      | 500C 1092h       |
| EPWM2_G0      | 5000 2092h       |
| EPWM2_G1      | 5004 2092h       |
| EPWM2_G2      | 5008 2092h       |
| EPWM2_G3      | 500C 2092h       |
| EPWM3_G0      | 5000 3092h       |
| EPWM3_G1      | 5004 3092h       |
| EPWM3_G2      | 5008 3092h       |
| EPWM3_G3      | 500C 3092h       |
| EPWM4_G0      | 5000 4092h       |
| EPWM4_G1      | 5004 4092h       |
| EPWM4_G2      | 5008 4092h       |
| EPWM4_G3      | 500C 4092h       |
| EPWM5_G0      | 5000 5092h       |
| EPWM5_G1      | 5004 5092h       |
| EPWM5_G2      | 5008 5092h       |
| EPWM5_G3      | 500C 5092h       |
| EPWM6_G0      | 5000 6092h       |
| EPWM6_G1      | 5004 6092h       |
| EPWM6_G2      | 5008 6092h       |
| EPWM6_G3      | 500C 6092h       |
| EPWM7_G0      | 5000 7092h       |
| EPWM7_G1      | 5004 7092h       |
| EPWM7_G2      | 5008 7092h       |
| EPWM7_G3      | 500C 7092h       |
| EPWM8_G0      | 5000 8092h       |
| EPWM8_G1      | 5004 8092h       |
| EPWM8_G2      | 5008 8092h       |
| EPWM8_G3      | 500C 8092h       |
| EPWM9_G0      | 5000 9092h       |
| EPWM9_G1      | 5004 9092h       |
| EPWM9_G2      | 5008 9092h       |

**Table 3-910. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9092h       |
| EPWM10_G0     | 5000 A092h       |
| EPWM10_G1     | 5004 A092h       |
| EPWM10_G2     | 5008 A092h       |
| EPWM10_G3     | 500C A092h       |
| EPWM11_G0     | 5000 B092h       |
| EPWM11_G1     | 5004 B092h       |
| EPWM11_G2     | 5008 B092h       |
| EPWM11_G3     | 500C B092h       |
| EPWM12_G0     | 5000 C092h       |
| EPWM12_G1     | 5004 C092h       |
| EPWM12_G2     | 5008 C092h       |
| EPWM12_G3     | 500C C092h       |
| EPWM13_G0     | 5000 D092h       |
| EPWM13_G1     | 5004 D092h       |
| EPWM13_G2     | 5008 D092h       |
| EPWM13_G3     | 500C D092h       |
| EPWM14_G0     | 5000 E092h       |
| EPWM14_G1     | 5004 E092h       |
| EPWM14_G2     | 5008 E092h       |
| EPWM14_G3     | 500C E092h       |
| EPWM15_G0     | 5000 F092h       |
| EPWM15_G1     | 5004 F092h       |
| EPWM15_G2     | 5008 F092h       |
| EPWM15_G3     | 500C F092h       |
| EPWM16_G0     | 5001 0092h       |
| EPWM16_G1     | 5005 0092h       |
| EPWM16_G2     | 5009 0092h       |
| EPWM16_G3     | 500D 0092h       |
| EPWM17_G0     | 5001 1092h       |
| EPWM17_G1     | 5005 1092h       |
| EPWM17_G2     | 5009 1092h       |
| EPWM17_G3     | 500D 1092h       |
| EPWM18_G0     | 5001 2092h       |
| EPWM18_G1     | 5005 2092h       |
| EPWM18_G2     | 5009 2092h       |
| EPWM18_G3     | 500D 2092h       |
| EPWM19_G0     | 5001 3092h       |
| EPWM19_G1     | 5005 3092h       |
| EPWM19_G2     | 5009 3092h       |
| EPWM19_G3     | 500D 3092h       |
| EPWM20_G0     | 5001 4092h       |
| EPWM20_G1     | 5005 4092h       |
| EPWM20_G2     | 5009 4092h       |
| EPWM20_G3     | 500D 4092h       |



**Table 3-910. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5092h       |
| EPWM21_G1     | 5005 5092h       |
| EPWM21_G2     | 5009 5092h       |
| EPWM21_G3     | 500D 5092h       |
| EPWM22_G0     | 5001 6092h       |
| EPWM22_G1     | 5005 6092h       |
| EPWM22_G2     | 5009 6092h       |
| EPWM22_G3     | 500D 6092h       |
| EPWM23_G0     | 5001 7092h       |
| EPWM23_G1     | 5005 7092h       |
| EPWM23_G2     | 5009 7092h       |
| EPWM23_G3     | 500D 7092h       |
| EPWM24_G0     | 5001 8092h       |
| EPWM24_G1     | 5005 8092h       |
| EPWM24_G2     | 5009 8092h       |
| EPWM24_G3     | 500D 8092h       |
| EPWM25_G0     | 5001 9092h       |
| EPWM25_G1     | 5005 9092h       |
| EPWM25_G2     | 5009 9092h       |
| EPWM25_G3     | 500D 9092h       |
| EPWM26_G0     | 5001 A092h       |
| EPWM26_G1     | 5005 A092h       |
| EPWM26_G2     | 5009 A092h       |
| EPWM26_G3     | 500D A092h       |
| EPWM27_G0     | 5001 B092h       |
| EPWM27_G1     | 5005 B092h       |
| EPWM27_G2     | 5009 B092h       |
| EPWM27_G3     | 500D B092h       |
| EPWM28_G0     | 5001 C092h       |
| EPWM28_G1     | 5005 C092h       |
| EPWM28_G2     | 5009 C092h       |
| EPWM28_G3     | 500D C092h       |
| EPWM29_G0     | 5001 D092h       |
| EPWM29_G1     | 5005 D092h       |
| EPWM29_G2     | 5009 D092h       |
| EPWM29_G3     | 500D D092h       |
| EPWM30_G0     | 5001 E092h       |
| EPWM30_G1     | 5005 E092h       |
| EPWM30_G2     | 5009 E092h       |
| EPWM30_G3     | 500D E092h       |
| EPWM31_G0     | 5001 F092h       |
| EPWM31_G1     | 5005 F092h       |
| EPWM31_G2     | 5009 F092h       |
| EPWM31_G3     | 500D F092h       |

**Figure 3-284. EPWM\_AQCSFRC Name Register**

|            |    |    |    |      |    |      |   |
|------------|----|----|----|------|----|------|---|
| 15         | 14 | 13 | 12 | 11   | 10 | 9    | 8 |
| RESERVED_1 |    |    |    |      |    |      |   |
| R          |    |    |    |      |    |      |   |
| 0h         |    |    |    |      |    |      |   |
| 7          | 6  | 5  | 4  | 3    | 2  | 1    | 0 |
| RESERVED_1 |    |    |    | CSFB |    | CSFA |   |
| R          |    |    |    | R/W  |    | R/W  |   |
| 0h         |    |    |    | 0h   |    | 0h   |   |

**Table 3-912. EPWM\_AQCSFRC Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:4 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 3:2  | CSFB       | R/W  | 0h    | Continuous Software Force on Output B<br>In immediate mode, a continuous force takes effect on the next TBCLK edge. In shadow mode, a continuous force takes effect on the next TBCLK edge after a shadow load into the active register. To configure shadow mode, use AQSFRC[RLDCSF].<br>00:Software forcing is disabled and has no effect<br>01:Forces a continuous low on output B<br>10:Forces a continuous high on output B<br>11:Software forcing is disabled and has no effect |
| 1:0  | CSFA       | R/W  | 0h    | Continuous Software Force on Output A<br>In immediate mode, a continuous force takes effect on the next TBCLK edge. In shadow mode, a continuous force takes effect on the next TBCLK edge after a shadow load into the active register.<br>00:Software forcing is disabled and has no effect<br>01:Forces a continuous low on output A<br>10:Forces a continuous high on output A<br>11:Software forcing is disabled and has no effect                                               |

### 3.7.2.34 EPWM\_DBREDHR Register

#### 1 EPWM\_DBREDHR Register (Offset = A0h) [reset = 0h]

Dead-Band Generator Rising Edge Delay High Resolution Mirror Register .

Return to [Summary Table](#)

**Table 3-913. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 00A0h       |
| EPWM0_G1      | 5004 00A0h       |
| EPWM0_G2      | 5008 00A0h       |
| EPWM0_G3      | 500C 00A0h       |
| EPWM1_G0      | 5000 10A0h       |
| EPWM1_G1      | 5004 10A0h       |
| EPWM1_G2      | 5008 10A0h       |
| EPWM1_G3      | 500C 10A0h       |
| EPWM2_G0      | 5000 20A0h       |
| EPWM2_G1      | 5004 20A0h       |
| EPWM2_G2      | 5008 20A0h       |
| EPWM2_G3      | 500C 20A0h       |
| EPWM3_G0      | 5000 30A0h       |
| EPWM3_G1      | 5004 30A0h       |
| EPWM3_G2      | 5008 30A0h       |
| EPWM3_G3      | 500C 30A0h       |
| EPWM4_G0      | 5000 40A0h       |
| EPWM4_G1      | 5004 40A0h       |
| EPWM4_G2      | 5008 40A0h       |
| EPWM4_G3      | 500C 40A0h       |
| EPWM5_G0      | 5000 50A0h       |
| EPWM5_G1      | 5004 50A0h       |
| EPWM5_G2      | 5008 50A0h       |
| EPWM5_G3      | 500C 50A0h       |
| EPWM6_G0      | 5000 60A0h       |
| EPWM6_G1      | 5004 60A0h       |
| EPWM6_G2      | 5008 60A0h       |
| EPWM6_G3      | 500C 60A0h       |
| EPWM7_G0      | 5000 70A0h       |
| EPWM7_G1      | 5004 70A0h       |
| EPWM7_G2      | 5008 70A0h       |
| EPWM7_G3      | 500C 70A0h       |
| EPWM8_G0      | 5000 80A0h       |
| EPWM8_G1      | 5004 80A0h       |
| EPWM8_G2      | 5008 80A0h       |
| EPWM8_G3      | 500C 80A0h       |
| EPWM9_G0      | 5000 90A0h       |
| EPWM9_G1      | 5004 90A0h       |
| EPWM9_G2      | 5008 90A0h       |

**Table 3-913. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 90A0h       |
| EPWM10_G0     | 5000 A0A0h       |
| EPWM10_G1     | 5004 A0A0h       |
| EPWM10_G2     | 5008 A0A0h       |
| EPWM10_G3     | 500C A0A0h       |
| EPWM11_G0     | 5000 B0A0h       |
| EPWM11_G1     | 5004 B0A0h       |
| EPWM11_G2     | 5008 B0A0h       |
| EPWM11_G3     | 500C B0A0h       |
| EPWM12_G0     | 5000 C0A0h       |
| EPWM12_G1     | 5004 C0A0h       |
| EPWM12_G2     | 5008 C0A0h       |
| EPWM12_G3     | 500C C0A0h       |
| EPWM13_G0     | 5000 D0A0h       |
| EPWM13_G1     | 5004 D0A0h       |
| EPWM13_G2     | 5008 D0A0h       |
| EPWM13_G3     | 500C D0A0h       |
| EPWM14_G0     | 5000 E0A0h       |
| EPWM14_G1     | 5004 E0A0h       |
| EPWM14_G2     | 5008 E0A0h       |
| EPWM14_G3     | 500C E0A0h       |
| EPWM15_G0     | 5000 F0A0h       |
| EPWM15_G1     | 5004 F0A0h       |
| EPWM15_G2     | 5008 F0A0h       |
| EPWM15_G3     | 500C F0A0h       |
| EPWM16_G0     | 5001 00A0h       |
| EPWM16_G1     | 5005 00A0h       |
| EPWM16_G2     | 5009 00A0h       |
| EPWM16_G3     | 500D 00A0h       |
| EPWM17_G0     | 5001 10A0h       |
| EPWM17_G1     | 5005 10A0h       |
| EPWM17_G2     | 5009 10A0h       |
| EPWM17_G3     | 500D 10A0h       |
| EPWM18_G0     | 5001 20A0h       |
| EPWM18_G1     | 5005 20A0h       |
| EPWM18_G2     | 5009 20A0h       |
| EPWM18_G3     | 500D 20A0h       |
| EPWM19_G0     | 5001 30A0h       |
| EPWM19_G1     | 5005 30A0h       |
| EPWM19_G2     | 5009 30A0h       |
| EPWM19_G3     | 500D 30A0h       |
| EPWM20_G0     | 5001 40A0h       |
| EPWM20_G1     | 5005 40A0h       |
| EPWM20_G2     | 5009 40A0h       |
| EPWM20_G3     | 500D 40A0h       |

**Table 3-913. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 50A0h       |
| EPWM21_G1     | 5005 50A0h       |
| EPWM21_G2     | 5009 50A0h       |
| EPWM21_G3     | 500D 50A0h       |
| EPWM22_G0     | 5001 60A0h       |
| EPWM22_G1     | 5005 60A0h       |
| EPWM22_G2     | 5009 60A0h       |
| EPWM22_G3     | 500D 60A0h       |
| EPWM23_G0     | 5001 70A0h       |
| EPWM23_G1     | 5005 70A0h       |
| EPWM23_G2     | 5009 70A0h       |
| EPWM23_G3     | 500D 70A0h       |
| EPWM24_G0     | 5001 80A0h       |
| EPWM24_G1     | 5005 80A0h       |
| EPWM24_G2     | 5009 80A0h       |
| EPWM24_G3     | 500D 80A0h       |
| EPWM25_G0     | 5001 90A0h       |
| EPWM25_G1     | 5005 90A0h       |
| EPWM25_G2     | 5009 90A0h       |
| EPWM25_G3     | 500D 90A0h       |
| EPWM26_G0     | 5001 A0A0h       |
| EPWM26_G1     | 5005 A0A0h       |
| EPWM26_G2     | 5009 A0A0h       |
| EPWM26_G3     | 500D A0A0h       |
| EPWM27_G0     | 5001 B0A0h       |
| EPWM27_G1     | 5005 B0A0h       |
| EPWM27_G2     | 5009 B0A0h       |
| EPWM27_G3     | 500D B0A0h       |
| EPWM28_G0     | 5001 C0A0h       |
| EPWM28_G1     | 5005 C0A0h       |
| EPWM28_G2     | 5009 C0A0h       |
| EPWM28_G3     | 500D C0A0h       |
| EPWM29_G0     | 5001 D0A0h       |
| EPWM29_G1     | 5005 D0A0h       |
| EPWM29_G2     | 5009 D0A0h       |
| EPWM29_G3     | 500D D0A0h       |
| EPWM30_G0     | 5001 E0A0h       |
| EPWM30_G1     | 5005 E0A0h       |
| EPWM30_G2     | 5009 E0A0h       |
| EPWM30_G3     | 500D E0A0h       |
| EPWM31_G0     | 5001 F0A0h       |
| EPWM31_G1     | 5005 F0A0h       |
| EPWM31_G2     | 5009 F0A0h       |
| EPWM31_G3     | 500D F0A0h       |

**Figure 3-285. EPWM\_DBREDHR Name Register**

|               |    |    |    |    |    |   |            |
|---------------|----|----|----|----|----|---|------------|
| 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8          |
| DBREDHR       |    |    |    |    |    |   | RESERVED_2 |
| R/W           |    |    |    |    |    |   | R          |
| 0h            |    |    |    |    |    |   | 0h         |
| 7             | 6  | 5  | 4  | 3  | 2  | 1 | 0          |
| DBREDHR_DELAY |    |    |    |    |    |   | RESERVED_1 |
| R             |    |    |    |    |    |   | R          |
| 0h            |    |    |    |    |    |   | 0h         |

**Table 3-915. EPWM\_DBREDHR Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                                                          |
|------|---------------|------|-------|--------------------------------------------------------------------------------------|
| 15:9 | DBREDHR       | R/W  | 0h    | Dead Band Rising Edge Delay High Resolution Bits                                     |
| 8    | RESERVED_2    | R    | 0h    | Reserved                                                                             |
| 7:1  | DBREDHR_DELAY | R    | 0h    | These 7-bits contain the results of OTTO calculation [if auto-conversion is enabled] |
| 0    | RESERVED_1    | R    | 0h    | Reserved                                                                             |

### 3.7.2.35 EPWM\_DBRED Register

#### 1 EPWM\_DBRED Register (Offset = A2h) [reset = 0h]

Dead-Band Generator Rising Edge Delay High Resolution Mirror Register .

Return to [Summary Table](#)

**Table 3-916. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 00A2h       |
| EPWM0_G1      | 5004 00A2h       |
| EPWM0_G2      | 5008 00A2h       |
| EPWM0_G3      | 500C 00A2h       |
| EPWM1_G0      | 5000 10A2h       |
| EPWM1_G1      | 5004 10A2h       |
| EPWM1_G2      | 5008 10A2h       |
| EPWM1_G3      | 500C 10A2h       |
| EPWM2_G0      | 5000 20A2h       |
| EPWM2_G1      | 5004 20A2h       |
| EPWM2_G2      | 5008 20A2h       |
| EPWM2_G3      | 500C 20A2h       |
| EPWM3_G0      | 5000 30A2h       |
| EPWM3_G1      | 5004 30A2h       |
| EPWM3_G2      | 5008 30A2h       |
| EPWM3_G3      | 500C 30A2h       |
| EPWM4_G0      | 5000 40A2h       |
| EPWM4_G1      | 5004 40A2h       |
| EPWM4_G2      | 5008 40A2h       |
| EPWM4_G3      | 500C 40A2h       |
| EPWM5_G0      | 5000 50A2h       |
| EPWM5_G1      | 5004 50A2h       |
| EPWM5_G2      | 5008 50A2h       |
| EPWM5_G3      | 500C 50A2h       |
| EPWM6_G0      | 5000 60A2h       |
| EPWM6_G1      | 5004 60A2h       |
| EPWM6_G2      | 5008 60A2h       |
| EPWM6_G3      | 500C 60A2h       |
| EPWM7_G0      | 5000 70A2h       |
| EPWM7_G1      | 5004 70A2h       |
| EPWM7_G2      | 5008 70A2h       |
| EPWM7_G3      | 500C 70A2h       |
| EPWM8_G0      | 5000 80A2h       |
| EPWM8_G1      | 5004 80A2h       |
| EPWM8_G2      | 5008 80A2h       |
| EPWM8_G3      | 500C 80A2h       |
| EPWM9_G0      | 5000 90A2h       |
| EPWM9_G1      | 5004 90A2h       |
| EPWM9_G2      | 5008 90A2h       |

**Table 3-916. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 90A2h       |
| EPWM10_G0     | 5000 A0A2h       |
| EPWM10_G1     | 5004 A0A2h       |
| EPWM10_G2     | 5008 A0A2h       |
| EPWM10_G3     | 500C A0A2h       |
| EPWM11_G0     | 5000 B0A2h       |
| EPWM11_G1     | 5004 B0A2h       |
| EPWM11_G2     | 5008 B0A2h       |
| EPWM11_G3     | 500C B0A2h       |
| EPWM12_G0     | 5000 C0A2h       |
| EPWM12_G1     | 5004 C0A2h       |
| EPWM12_G2     | 5008 C0A2h       |
| EPWM12_G3     | 500C C0A2h       |
| EPWM13_G0     | 5000 D0A2h       |
| EPWM13_G1     | 5004 D0A2h       |
| EPWM13_G2     | 5008 D0A2h       |
| EPWM13_G3     | 500C D0A2h       |
| EPWM14_G0     | 5000 E0A2h       |
| EPWM14_G1     | 5004 E0A2h       |
| EPWM14_G2     | 5008 E0A2h       |
| EPWM14_G3     | 500C E0A2h       |
| EPWM15_G0     | 5000 F0A2h       |
| EPWM15_G1     | 5004 F0A2h       |
| EPWM15_G2     | 5008 F0A2h       |
| EPWM15_G3     | 500C F0A2h       |
| EPWM16_G0     | 5001 00A2h       |
| EPWM16_G1     | 5005 00A2h       |
| EPWM16_G2     | 5009 00A2h       |
| EPWM16_G3     | 500D 00A2h       |
| EPWM17_G0     | 5001 10A2h       |
| EPWM17_G1     | 5005 10A2h       |
| EPWM17_G2     | 5009 10A2h       |
| EPWM17_G3     | 500D 10A2h       |
| EPWM18_G0     | 5001 20A2h       |
| EPWM18_G1     | 5005 20A2h       |
| EPWM18_G2     | 5009 20A2h       |
| EPWM18_G3     | 500D 20A2h       |
| EPWM19_G0     | 5001 30A2h       |
| EPWM19_G1     | 5005 30A2h       |
| EPWM19_G2     | 5009 30A2h       |
| EPWM19_G3     | 500D 30A2h       |
| EPWM20_G0     | 5001 40A2h       |
| EPWM20_G1     | 5005 40A2h       |
| EPWM20_G2     | 5009 40A2h       |
| EPWM20_G3     | 500D 40A2h       |



**Table 3-916. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 50A2h       |
| EPWM21_G1     | 5005 50A2h       |
| EPWM21_G2     | 5009 50A2h       |
| EPWM21_G3     | 500D 50A2h       |
| EPWM22_G0     | 5001 60A2h       |
| EPWM22_G1     | 5005 60A2h       |
| EPWM22_G2     | 5009 60A2h       |
| EPWM22_G3     | 500D 60A2h       |
| EPWM23_G0     | 5001 70A2h       |
| EPWM23_G1     | 5005 70A2h       |
| EPWM23_G2     | 5009 70A2h       |
| EPWM23_G3     | 500D 70A2h       |
| EPWM24_G0     | 5001 80A2h       |
| EPWM24_G1     | 5005 80A2h       |
| EPWM24_G2     | 5009 80A2h       |
| EPWM24_G3     | 500D 80A2h       |
| EPWM25_G0     | 5001 90A2h       |
| EPWM25_G1     | 5005 90A2h       |
| EPWM25_G2     | 5009 90A2h       |
| EPWM25_G3     | 500D 90A2h       |
| EPWM26_G0     | 5001 A0A2h       |
| EPWM26_G1     | 5005 A0A2h       |
| EPWM26_G2     | 5009 A0A2h       |
| EPWM26_G3     | 500D A0A2h       |
| EPWM27_G0     | 5001 B0A2h       |
| EPWM27_G1     | 5005 B0A2h       |
| EPWM27_G2     | 5009 B0A2h       |
| EPWM27_G3     | 500D B0A2h       |
| EPWM28_G0     | 5001 C0A2h       |
| EPWM28_G1     | 5005 C0A2h       |
| EPWM28_G2     | 5009 C0A2h       |
| EPWM28_G3     | 500D C0A2h       |
| EPWM29_G0     | 5001 D0A2h       |
| EPWM29_G1     | 5005 D0A2h       |
| EPWM29_G2     | 5009 D0A2h       |
| EPWM29_G3     | 500D D0A2h       |
| EPWM30_G0     | 5001 E0A2h       |
| EPWM30_G1     | 5005 E0A2h       |
| EPWM30_G2     | 5009 E0A2h       |
| EPWM30_G3     | 500D E0A2h       |
| EPWM31_G0     | 5001 F0A2h       |
| EPWM31_G1     | 5005 F0A2h       |
| EPWM31_G2     | 5009 F0A2h       |
| EPWM31_G3     | 500D F0A2h       |

**Figure 3-286. EPWM\_DBRED Name Register**

|            |    |       |    |    |    |   |   |
|------------|----|-------|----|----|----|---|---|
| 15         | 14 | 13    | 12 | 11 | 10 | 9 | 8 |
| RESERVED_1 |    | DBRED |    |    |    |   |   |
| R          |    | R/W   |    |    |    |   |   |
| 0h         |    | 0h    |    |    |    |   |   |
| 7          | 6  | 5     | 4  | 3  | 2  | 1 | 0 |
| DBRED      |    |       |    |    |    |   |   |
| R/W        |    |       |    |    |    |   |   |
| 0h         |    |       |    |    |    |   |   |

**Table 3-918. EPWM\_DBRED Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description             |
|-------|------------|------|-------|-------------------------|
| 15:14 | RESERVED_1 | R    | 0h    | Reserved                |
| 13:0  | DBRED      | R/W  | 0h    | Rising edge delay value |

### 3.7.2.36 EPWM\_DBFEDHR Register

#### 1 EPWM\_DBFEDHR Register (Offset = A4h) [reset = 0h]

Dead-Band Generator Falling Edge Delay High Resolution Register .

Return to [Summary Table](#)

**Table 3-919. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 00A4h       |
| EPWM0_G1      | 5004 00A4h       |
| EPWM0_G2      | 5008 00A4h       |
| EPWM0_G3      | 500C 00A4h       |
| EPWM1_G0      | 5000 10A4h       |
| EPWM1_G1      | 5004 10A4h       |
| EPWM1_G2      | 5008 10A4h       |
| EPWM1_G3      | 500C 10A4h       |
| EPWM2_G0      | 5000 20A4h       |
| EPWM2_G1      | 5004 20A4h       |
| EPWM2_G2      | 5008 20A4h       |
| EPWM2_G3      | 500C 20A4h       |
| EPWM3_G0      | 5000 30A4h       |
| EPWM3_G1      | 5004 30A4h       |
| EPWM3_G2      | 5008 30A4h       |
| EPWM3_G3      | 500C 30A4h       |
| EPWM4_G0      | 5000 40A4h       |
| EPWM4_G1      | 5004 40A4h       |
| EPWM4_G2      | 5008 40A4h       |
| EPWM4_G3      | 500C 40A4h       |
| EPWM5_G0      | 5000 50A4h       |
| EPWM5_G1      | 5004 50A4h       |
| EPWM5_G2      | 5008 50A4h       |
| EPWM5_G3      | 500C 50A4h       |
| EPWM6_G0      | 5000 60A4h       |
| EPWM6_G1      | 5004 60A4h       |
| EPWM6_G2      | 5008 60A4h       |
| EPWM6_G3      | 500C 60A4h       |
| EPWM7_G0      | 5000 70A4h       |
| EPWM7_G1      | 5004 70A4h       |
| EPWM7_G2      | 5008 70A4h       |
| EPWM7_G3      | 500C 70A4h       |
| EPWM8_G0      | 5000 80A4h       |
| EPWM8_G1      | 5004 80A4h       |
| EPWM8_G2      | 5008 80A4h       |
| EPWM8_G3      | 500C 80A4h       |
| EPWM9_G0      | 5000 90A4h       |
| EPWM9_G1      | 5004 90A4h       |
| EPWM9_G2      | 5008 90A4h       |

**Table 3-919. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 90A4h       |
| EPWM10_G0     | 5000 A0A4h       |
| EPWM10_G1     | 5004 A0A4h       |
| EPWM10_G2     | 5008 A0A4h       |
| EPWM10_G3     | 500C A0A4h       |
| EPWM11_G0     | 5000 B0A4h       |
| EPWM11_G1     | 5004 B0A4h       |
| EPWM11_G2     | 5008 B0A4h       |
| EPWM11_G3     | 500C B0A4h       |
| EPWM12_G0     | 5000 C0A4h       |
| EPWM12_G1     | 5004 C0A4h       |
| EPWM12_G2     | 5008 C0A4h       |
| EPWM12_G3     | 500C C0A4h       |
| EPWM13_G0     | 5000 D0A4h       |
| EPWM13_G1     | 5004 D0A4h       |
| EPWM13_G2     | 5008 D0A4h       |
| EPWM13_G3     | 500C D0A4h       |
| EPWM14_G0     | 5000 E0A4h       |
| EPWM14_G1     | 5004 E0A4h       |
| EPWM14_G2     | 5008 E0A4h       |
| EPWM14_G3     | 500C E0A4h       |
| EPWM15_G0     | 5000 F0A4h       |
| EPWM15_G1     | 5004 F0A4h       |
| EPWM15_G2     | 5008 F0A4h       |
| EPWM15_G3     | 500C F0A4h       |
| EPWM16_G0     | 5001 00A4h       |
| EPWM16_G1     | 5005 00A4h       |
| EPWM16_G2     | 5009 00A4h       |
| EPWM16_G3     | 500D 00A4h       |
| EPWM17_G0     | 5001 10A4h       |
| EPWM17_G1     | 5005 10A4h       |
| EPWM17_G2     | 5009 10A4h       |
| EPWM17_G3     | 500D 10A4h       |
| EPWM18_G0     | 5001 20A4h       |
| EPWM18_G1     | 5005 20A4h       |
| EPWM18_G2     | 5009 20A4h       |
| EPWM18_G3     | 500D 20A4h       |
| EPWM19_G0     | 5001 30A4h       |
| EPWM19_G1     | 5005 30A4h       |
| EPWM19_G2     | 5009 30A4h       |
| EPWM19_G3     | 500D 30A4h       |
| EPWM20_G0     | 5001 40A4h       |
| EPWM20_G1     | 5005 40A4h       |
| EPWM20_G2     | 5009 40A4h       |
| EPWM20_G3     | 500D 40A4h       |

**Table 3-919. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 50A4h       |
| EPWM21_G1     | 5005 50A4h       |
| EPWM21_G2     | 5009 50A4h       |
| EPWM21_G3     | 500D 50A4h       |
| EPWM22_G0     | 5001 60A4h       |
| EPWM22_G1     | 5005 60A4h       |
| EPWM22_G2     | 5009 60A4h       |
| EPWM22_G3     | 500D 60A4h       |
| EPWM23_G0     | 5001 70A4h       |
| EPWM23_G1     | 5005 70A4h       |
| EPWM23_G2     | 5009 70A4h       |
| EPWM23_G3     | 500D 70A4h       |
| EPWM24_G0     | 5001 80A4h       |
| EPWM24_G1     | 5005 80A4h       |
| EPWM24_G2     | 5009 80A4h       |
| EPWM24_G3     | 500D 80A4h       |
| EPWM25_G0     | 5001 90A4h       |
| EPWM25_G1     | 5005 90A4h       |
| EPWM25_G2     | 5009 90A4h       |
| EPWM25_G3     | 500D 90A4h       |
| EPWM26_G0     | 5001 A0A4h       |
| EPWM26_G1     | 5005 A0A4h       |
| EPWM26_G2     | 5009 A0A4h       |
| EPWM26_G3     | 500D A0A4h       |
| EPWM27_G0     | 5001 B0A4h       |
| EPWM27_G1     | 5005 B0A4h       |
| EPWM27_G2     | 5009 B0A4h       |
| EPWM27_G3     | 500D B0A4h       |
| EPWM28_G0     | 5001 C0A4h       |
| EPWM28_G1     | 5005 C0A4h       |
| EPWM28_G2     | 5009 C0A4h       |
| EPWM28_G3     | 500D C0A4h       |
| EPWM29_G0     | 5001 D0A4h       |
| EPWM29_G1     | 5005 D0A4h       |
| EPWM29_G2     | 5009 D0A4h       |
| EPWM29_G3     | 500D D0A4h       |
| EPWM30_G0     | 5001 E0A4h       |
| EPWM30_G1     | 5005 E0A4h       |
| EPWM30_G2     | 5009 E0A4h       |
| EPWM30_G3     | 500D E0A4h       |
| EPWM31_G0     | 5001 F0A4h       |
| EPWM31_G1     | 5005 F0A4h       |
| EPWM31_G2     | 5009 F0A4h       |
| EPWM31_G3     | 500D F0A4h       |

**Figure 3-287. EPWM\_DBFEDHR Name Register**

|               |    |    |    |    |    |   |            |
|---------------|----|----|----|----|----|---|------------|
| 15            | 14 | 13 | 12 | 11 | 10 | 9 | 8          |
| DBFEDHR       |    |    |    |    |    |   | RESERVED_2 |
| R/W           |    |    |    |    |    |   | R          |
| 0h            |    |    |    |    |    |   | 0h         |
| 7             | 6  | 5  | 4  | 3  | 2  | 1 | 0          |
| DBFEDHR_DELAY |    |    |    |    |    |   | RESERVED_1 |
| R             |    |    |    |    |    |   | R          |
| 0h            |    |    |    |    |    |   | 0h         |

**Table 3-921. EPWM\_DBFEDHR Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                                                          |
|------|---------------|------|-------|--------------------------------------------------------------------------------------|
| 15:9 | DBFEDHR       | R/W  | 0h    | Dead Band Falling Edge Delay High Resolution Bits                                    |
| 8    | RESERVED_2    | R    | 0h    | Reserved                                                                             |
| 7:1  | DBFEDHR_DELAY | R    | 0h    | These 7-bits contain the results of OTTO calculation [if auto-conversion is enabled] |
| 0    | RESERVED_1    | R    | 0h    | Reserved                                                                             |

### 3.7.2.37 EPWM\_DBFED Register

#### 1 EPWM\_DBFED Register (Offset = A6h) [reset = 0h]

Dead-Band Generator Falling Edge Delay Count Register.

Return to [Summary Table](#)

**Table 3-922. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 00A6h       |
| EPWM0_G1      | 5004 00A6h       |
| EPWM0_G2      | 5008 00A6h       |
| EPWM0_G3      | 500C 00A6h       |
| EPWM1_G0      | 5000 10A6h       |
| EPWM1_G1      | 5004 10A6h       |
| EPWM1_G2      | 5008 10A6h       |
| EPWM1_G3      | 500C 10A6h       |
| EPWM2_G0      | 5000 20A6h       |
| EPWM2_G1      | 5004 20A6h       |
| EPWM2_G2      | 5008 20A6h       |
| EPWM2_G3      | 500C 20A6h       |
| EPWM3_G0      | 5000 30A6h       |
| EPWM3_G1      | 5004 30A6h       |
| EPWM3_G2      | 5008 30A6h       |
| EPWM3_G3      | 500C 30A6h       |
| EPWM4_G0      | 5000 40A6h       |
| EPWM4_G1      | 5004 40A6h       |
| EPWM4_G2      | 5008 40A6h       |
| EPWM4_G3      | 500C 40A6h       |
| EPWM5_G0      | 5000 50A6h       |
| EPWM5_G1      | 5004 50A6h       |
| EPWM5_G2      | 5008 50A6h       |
| EPWM5_G3      | 500C 50A6h       |
| EPWM6_G0      | 5000 60A6h       |
| EPWM6_G1      | 5004 60A6h       |
| EPWM6_G2      | 5008 60A6h       |
| EPWM6_G3      | 500C 60A6h       |
| EPWM7_G0      | 5000 70A6h       |
| EPWM7_G1      | 5004 70A6h       |
| EPWM7_G2      | 5008 70A6h       |
| EPWM7_G3      | 500C 70A6h       |
| EPWM8_G0      | 5000 80A6h       |
| EPWM8_G1      | 5004 80A6h       |
| EPWM8_G2      | 5008 80A6h       |
| EPWM8_G3      | 500C 80A6h       |
| EPWM9_G0      | 5000 90A6h       |
| EPWM9_G1      | 5004 90A6h       |
| EPWM9_G2      | 5008 90A6h       |

**Table 3-922. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 90A6h       |
| EPWM10_G0     | 5000 A0A6h       |
| EPWM10_G1     | 5004 A0A6h       |
| EPWM10_G2     | 5008 A0A6h       |
| EPWM10_G3     | 500C A0A6h       |
| EPWM11_G0     | 5000 B0A6h       |
| EPWM11_G1     | 5004 B0A6h       |
| EPWM11_G2     | 5008 B0A6h       |
| EPWM11_G3     | 500C B0A6h       |
| EPWM12_G0     | 5000 C0A6h       |
| EPWM12_G1     | 5004 C0A6h       |
| EPWM12_G2     | 5008 C0A6h       |
| EPWM12_G3     | 500C C0A6h       |
| EPWM13_G0     | 5000 D0A6h       |
| EPWM13_G1     | 5004 D0A6h       |
| EPWM13_G2     | 5008 D0A6h       |
| EPWM13_G3     | 500C D0A6h       |
| EPWM14_G0     | 5000 E0A6h       |
| EPWM14_G1     | 5004 E0A6h       |
| EPWM14_G2     | 5008 E0A6h       |
| EPWM14_G3     | 500C E0A6h       |
| EPWM15_G0     | 5000 F0A6h       |
| EPWM15_G1     | 5004 F0A6h       |
| EPWM15_G2     | 5008 F0A6h       |
| EPWM15_G3     | 500C F0A6h       |
| EPWM16_G0     | 5001 00A6h       |
| EPWM16_G1     | 5005 00A6h       |
| EPWM16_G2     | 5009 00A6h       |
| EPWM16_G3     | 500D 00A6h       |
| EPWM17_G0     | 5001 10A6h       |
| EPWM17_G1     | 5005 10A6h       |
| EPWM17_G2     | 5009 10A6h       |
| EPWM17_G3     | 500D 10A6h       |
| EPWM18_G0     | 5001 20A6h       |
| EPWM18_G1     | 5005 20A6h       |
| EPWM18_G2     | 5009 20A6h       |
| EPWM18_G3     | 500D 20A6h       |
| EPWM19_G0     | 5001 30A6h       |
| EPWM19_G1     | 5005 30A6h       |
| EPWM19_G2     | 5009 30A6h       |
| EPWM19_G3     | 500D 30A6h       |
| EPWM20_G0     | 5001 40A6h       |
| EPWM20_G1     | 5005 40A6h       |
| EPWM20_G2     | 5009 40A6h       |
| EPWM20_G3     | 500D 40A6h       |



**Table 3-922. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 50A6h       |
| EPWM21_G1     | 5005 50A6h       |
| EPWM21_G2     | 5009 50A6h       |
| EPWM21_G3     | 500D 50A6h       |
| EPWM22_G0     | 5001 60A6h       |
| EPWM22_G1     | 5005 60A6h       |
| EPWM22_G2     | 5009 60A6h       |
| EPWM22_G3     | 500D 60A6h       |
| EPWM23_G0     | 5001 70A6h       |
| EPWM23_G1     | 5005 70A6h       |
| EPWM23_G2     | 5009 70A6h       |
| EPWM23_G3     | 500D 70A6h       |
| EPWM24_G0     | 5001 80A6h       |
| EPWM24_G1     | 5005 80A6h       |
| EPWM24_G2     | 5009 80A6h       |
| EPWM24_G3     | 500D 80A6h       |
| EPWM25_G0     | 5001 90A6h       |
| EPWM25_G1     | 5005 90A6h       |
| EPWM25_G2     | 5009 90A6h       |
| EPWM25_G3     | 500D 90A6h       |
| EPWM26_G0     | 5001 A0A6h       |
| EPWM26_G1     | 5005 A0A6h       |
| EPWM26_G2     | 5009 A0A6h       |
| EPWM26_G3     | 500D A0A6h       |
| EPWM27_G0     | 5001 B0A6h       |
| EPWM27_G1     | 5005 B0A6h       |
| EPWM27_G2     | 5009 B0A6h       |
| EPWM27_G3     | 500D B0A6h       |
| EPWM28_G0     | 5001 C0A6h       |
| EPWM28_G1     | 5005 C0A6h       |
| EPWM28_G2     | 5009 C0A6h       |
| EPWM28_G3     | 500D C0A6h       |
| EPWM29_G0     | 5001 D0A6h       |
| EPWM29_G1     | 5005 D0A6h       |
| EPWM29_G2     | 5009 D0A6h       |
| EPWM29_G3     | 500D D0A6h       |
| EPWM30_G0     | 5001 E0A6h       |
| EPWM30_G1     | 5005 E0A6h       |
| EPWM30_G2     | 5009 E0A6h       |
| EPWM30_G3     | 500D E0A6h       |
| EPWM31_G0     | 5001 F0A6h       |
| EPWM31_G1     | 5005 F0A6h       |
| EPWM31_G2     | 5009 F0A6h       |
| EPWM31_G3     | 500D F0A6h       |

**Figure 3-288. EPWM\_DBFED Name Register**

|            |    |       |    |    |    |   |   |
|------------|----|-------|----|----|----|---|---|
| 15         | 14 | 13    | 12 | 11 | 10 | 9 | 8 |
| RESERVED_1 |    | DBFED |    |    |    |   |   |
| R          |    | R/W   |    |    |    |   |   |
| 0h         |    | 0h    |    |    |    |   |   |
| 7          | 6  | 5     | 4  | 3  | 2  | 1 | 0 |
| DBFED      |    |       |    |    |    |   |   |
| R/W        |    |       |    |    |    |   |   |
| 0h         |    |       |    |    |    |   |   |

**Table 3-924. EPWM\_DBFED Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                |
|-------|------------|------|-------|--------------------------------------------|
| 15:14 | RESERVED_1 | R    | 0h    | Reserved                                   |
| 13:0  | DBFED      | R/W  | 0h    | Falling Edge Delay Count<br>14-bit counter |

### 3.7.2.38 EPWM\_TBPHS Register

#### 1 EPWM\_TBPHS Register (Offset = C0h) [reset = 0h]

Time Base Phase High.

Return to [Summary Table](#)

**Table 3-925. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 00C0h       |
| EPWM0_G1      | 5004 00C0h       |
| EPWM0_G2      | 5008 00C0h       |
| EPWM0_G3      | 500C 00C0h       |
| EPWM1_G0      | 5000 10C0h       |
| EPWM1_G1      | 5004 10C0h       |
| EPWM1_G2      | 5008 10C0h       |
| EPWM1_G3      | 500C 10C0h       |
| EPWM2_G0      | 5000 20C0h       |
| EPWM2_G1      | 5004 20C0h       |
| EPWM2_G2      | 5008 20C0h       |
| EPWM2_G3      | 500C 20C0h       |
| EPWM3_G0      | 5000 30C0h       |
| EPWM3_G1      | 5004 30C0h       |
| EPWM3_G2      | 5008 30C0h       |
| EPWM3_G3      | 500C 30C0h       |
| EPWM4_G0      | 5000 40C0h       |
| EPWM4_G1      | 5004 40C0h       |
| EPWM4_G2      | 5008 40C0h       |
| EPWM4_G3      | 500C 40C0h       |
| EPWM5_G0      | 5000 50C0h       |
| EPWM5_G1      | 5004 50C0h       |
| EPWM5_G2      | 5008 50C0h       |
| EPWM5_G3      | 500C 50C0h       |
| EPWM6_G0      | 5000 60C0h       |
| EPWM6_G1      | 5004 60C0h       |
| EPWM6_G2      | 5008 60C0h       |
| EPWM6_G3      | 500C 60C0h       |
| EPWM7_G0      | 5000 70C0h       |
| EPWM7_G1      | 5004 70C0h       |
| EPWM7_G2      | 5008 70C0h       |
| EPWM7_G3      | 500C 70C0h       |
| EPWM8_G0      | 5000 80C0h       |
| EPWM8_G1      | 5004 80C0h       |
| EPWM8_G2      | 5008 80C0h       |
| EPWM8_G3      | 500C 80C0h       |
| EPWM9_G0      | 5000 90C0h       |
| EPWM9_G1      | 5004 90C0h       |
| EPWM9_G2      | 5008 90C0h       |

**Table 3-925. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 90C0h       |
| EPWM10_G0     | 5000 A0C0h       |
| EPWM10_G1     | 5004 A0C0h       |
| EPWM10_G2     | 5008 A0C0h       |
| EPWM10_G3     | 500C A0C0h       |
| EPWM11_G0     | 5000 B0C0h       |
| EPWM11_G1     | 5004 B0C0h       |
| EPWM11_G2     | 5008 B0C0h       |
| EPWM11_G3     | 500C B0C0h       |
| EPWM12_G0     | 5000 C0C0h       |
| EPWM12_G1     | 5004 C0C0h       |
| EPWM12_G2     | 5008 C0C0h       |
| EPWM12_G3     | 500C C0C0h       |
| EPWM13_G0     | 5000 D0C0h       |
| EPWM13_G1     | 5004 D0C0h       |
| EPWM13_G2     | 5008 D0C0h       |
| EPWM13_G3     | 500C D0C0h       |
| EPWM14_G0     | 5000 E0C0h       |
| EPWM14_G1     | 5004 E0C0h       |
| EPWM14_G2     | 5008 E0C0h       |
| EPWM14_G3     | 500C E0C0h       |
| EPWM15_G0     | 5000 F0C0h       |
| EPWM15_G1     | 5004 F0C0h       |
| EPWM15_G2     | 5008 F0C0h       |
| EPWM15_G3     | 500C F0C0h       |
| EPWM16_G0     | 5001 00C0h       |
| EPWM16_G1     | 5005 00C0h       |
| EPWM16_G2     | 5009 00C0h       |
| EPWM16_G3     | 500D 00C0h       |
| EPWM17_G0     | 5001 10C0h       |
| EPWM17_G1     | 5005 10C0h       |
| EPWM17_G2     | 5009 10C0h       |
| EPWM17_G3     | 500D 10C0h       |
| EPWM18_G0     | 5001 20C0h       |
| EPWM18_G1     | 5005 20C0h       |
| EPWM18_G2     | 5009 20C0h       |
| EPWM18_G3     | 500D 20C0h       |
| EPWM19_G0     | 5001 30C0h       |
| EPWM19_G1     | 5005 30C0h       |
| EPWM19_G2     | 5009 30C0h       |
| EPWM19_G3     | 500D 30C0h       |
| EPWM20_G0     | 5001 40C0h       |
| EPWM20_G1     | 5005 40C0h       |
| EPWM20_G2     | 5009 40C0h       |
| EPWM20_G3     | 500D 40C0h       |

**Table 3-925. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 50C0h       |
| EPWM21_G1     | 5005 50C0h       |
| EPWM21_G2     | 5009 50C0h       |
| EPWM21_G3     | 500D 50C0h       |
| EPWM22_G0     | 5001 60C0h       |
| EPWM22_G1     | 5005 60C0h       |
| EPWM22_G2     | 5009 60C0h       |
| EPWM22_G3     | 500D 60C0h       |
| EPWM23_G0     | 5001 70C0h       |
| EPWM23_G1     | 5005 70C0h       |
| EPWM23_G2     | 5009 70C0h       |
| EPWM23_G3     | 500D 70C0h       |
| EPWM24_G0     | 5001 80C0h       |
| EPWM24_G1     | 5005 80C0h       |
| EPWM24_G2     | 5009 80C0h       |
| EPWM24_G3     | 500D 80C0h       |
| EPWM25_G0     | 5001 90C0h       |
| EPWM25_G1     | 5005 90C0h       |
| EPWM25_G2     | 5009 90C0h       |
| EPWM25_G3     | 500D 90C0h       |
| EPWM26_G0     | 5001 A0C0h       |
| EPWM26_G1     | 5005 A0C0h       |
| EPWM26_G2     | 5009 A0C0h       |
| EPWM26_G3     | 500D A0C0h       |
| EPWM27_G0     | 5001 B0C0h       |
| EPWM27_G1     | 5005 B0C0h       |
| EPWM27_G2     | 5009 B0C0h       |
| EPWM27_G3     | 500D B0C0h       |
| EPWM28_G0     | 5001 C0C0h       |
| EPWM28_G1     | 5005 C0C0h       |
| EPWM28_G2     | 5009 C0C0h       |
| EPWM28_G3     | 500D C0C0h       |
| EPWM29_G0     | 5001 D0C0h       |
| EPWM29_G1     | 5005 D0C0h       |
| EPWM29_G2     | 5009 D0C0h       |
| EPWM29_G3     | 500D D0C0h       |
| EPWM30_G0     | 5001 E0C0h       |
| EPWM30_G1     | 5005 E0C0h       |
| EPWM30_G2     | 5009 E0C0h       |
| EPWM30_G3     | 500D E0C0h       |
| EPWM31_G0     | 5001 F0C0h       |
| EPWM31_G1     | 5005 F0C0h       |
| EPWM31_G2     | 5009 F0C0h       |
| EPWM31_G3     | 500D F0C0h       |

**Figure 3-289. EPWM\_TBPHS Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TBPHS   |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TBPHS   |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TBPHSHR |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TBPHSHR |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 3-927. EPWM\_TBPHS Register Field Descriptions**

| Bit   | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|---------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | TBPHS   | R/W  | 0h    | Phase Offset Register<br>These bits set time-base counter phase of the selected EPWM relative to the time-base that is supplying the synchronization input signal.<br>- If TBCTL[PHSEN] = 0, then the synchronization event is ignored and the time-base counter is not loaded with the phase.<br>- If TBCTL[PHSEN] = 1, then the time-base counter [TBCTR] will be loaded with the phase [TBPHS] when a synchronization event occurs. The synchronization event can be initiated by the input synchronization signal [EPWMxSYNCl] or by a software forced synchronization. |
| 15:0  | TBPHSHR | R/W  | 0h    | Phase Offset [High Resolution] Register.<br>TBPHSHR must not be used. Instead TRREM [HRPWM remainder register] must be used to mimic the functionality of TBPHSHR. The lower 8 bits in this register are ignored - writes are ignored and reads return zero                                                                                                                                                                                                                                                                                                                 |

### 3.7.2.39 EPWM\_TBPRDHR Register

#### 1 EPWM\_TBPRDHR Register (Offset = C4h) [reset = 0h]

Time Base Period High Resolution Register .

Return to [Summary Table](#)

**Table 3-928. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 00C4h       |
| EPWM0_G1      | 5004 00C4h       |
| EPWM0_G2      | 5008 00C4h       |
| EPWM0_G3      | 500C 00C4h       |
| EPWM1_G0      | 5000 10C4h       |
| EPWM1_G1      | 5004 10C4h       |
| EPWM1_G2      | 5008 10C4h       |
| EPWM1_G3      | 500C 10C4h       |
| EPWM2_G0      | 5000 20C4h       |
| EPWM2_G1      | 5004 20C4h       |
| EPWM2_G2      | 5008 20C4h       |
| EPWM2_G3      | 500C 20C4h       |
| EPWM3_G0      | 5000 30C4h       |
| EPWM3_G1      | 5004 30C4h       |
| EPWM3_G2      | 5008 30C4h       |
| EPWM3_G3      | 500C 30C4h       |
| EPWM4_G0      | 5000 40C4h       |
| EPWM4_G1      | 5004 40C4h       |
| EPWM4_G2      | 5008 40C4h       |
| EPWM4_G3      | 500C 40C4h       |
| EPWM5_G0      | 5000 50C4h       |
| EPWM5_G1      | 5004 50C4h       |
| EPWM5_G2      | 5008 50C4h       |
| EPWM5_G3      | 500C 50C4h       |
| EPWM6_G0      | 5000 60C4h       |
| EPWM6_G1      | 5004 60C4h       |
| EPWM6_G2      | 5008 60C4h       |
| EPWM6_G3      | 500C 60C4h       |
| EPWM7_G0      | 5000 70C4h       |
| EPWM7_G1      | 5004 70C4h       |
| EPWM7_G2      | 5008 70C4h       |
| EPWM7_G3      | 500C 70C4h       |
| EPWM8_G0      | 5000 80C4h       |
| EPWM8_G1      | 5004 80C4h       |
| EPWM8_G2      | 5008 80C4h       |
| EPWM8_G3      | 500C 80C4h       |
| EPWM9_G0      | 5000 90C4h       |
| EPWM9_G1      | 5004 90C4h       |
| EPWM9_G2      | 5008 90C4h       |

**Table 3-928. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 90C4h       |
| EPWM10_G0     | 5000 A0C4h       |
| EPWM10_G1     | 5004 A0C4h       |
| EPWM10_G2     | 5008 A0C4h       |
| EPWM10_G3     | 500C A0C4h       |
| EPWM11_G0     | 5000 B0C4h       |
| EPWM11_G1     | 5004 B0C4h       |
| EPWM11_G2     | 5008 B0C4h       |
| EPWM11_G3     | 500C B0C4h       |
| EPWM12_G0     | 5000 C0C4h       |
| EPWM12_G1     | 5004 C0C4h       |
| EPWM12_G2     | 5008 C0C4h       |
| EPWM12_G3     | 500C C0C4h       |
| EPWM13_G0     | 5000 D0C4h       |
| EPWM13_G1     | 5004 D0C4h       |
| EPWM13_G2     | 5008 D0C4h       |
| EPWM13_G3     | 500C D0C4h       |
| EPWM14_G0     | 5000 E0C4h       |
| EPWM14_G1     | 5004 E0C4h       |
| EPWM14_G2     | 5008 E0C4h       |
| EPWM14_G3     | 500C E0C4h       |
| EPWM15_G0     | 5000 F0C4h       |
| EPWM15_G1     | 5004 F0C4h       |
| EPWM15_G2     | 5008 F0C4h       |
| EPWM15_G3     | 500C F0C4h       |
| EPWM16_G0     | 5001 00C4h       |
| EPWM16_G1     | 5005 00C4h       |
| EPWM16_G2     | 5009 00C4h       |
| EPWM16_G3     | 500D 00C4h       |
| EPWM17_G0     | 5001 10C4h       |
| EPWM17_G1     | 5005 10C4h       |
| EPWM17_G2     | 5009 10C4h       |
| EPWM17_G3     | 500D 10C4h       |
| EPWM18_G0     | 5001 20C4h       |
| EPWM18_G1     | 5005 20C4h       |
| EPWM18_G2     | 5009 20C4h       |
| EPWM18_G3     | 500D 20C4h       |
| EPWM19_G0     | 5001 30C4h       |
| EPWM19_G1     | 5005 30C4h       |
| EPWM19_G2     | 5009 30C4h       |
| EPWM19_G3     | 500D 30C4h       |
| EPWM20_G0     | 5001 40C4h       |
| EPWM20_G1     | 5005 40C4h       |
| EPWM20_G2     | 5009 40C4h       |
| EPWM20_G3     | 500D 40C4h       |



**Table 3-928. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 50C4h       |
| EPWM21_G1     | 5005 50C4h       |
| EPWM21_G2     | 5009 50C4h       |
| EPWM21_G3     | 500D 50C4h       |
| EPWM22_G0     | 5001 60C4h       |
| EPWM22_G1     | 5005 60C4h       |
| EPWM22_G2     | 5009 60C4h       |
| EPWM22_G3     | 500D 60C4h       |
| EPWM23_G0     | 5001 70C4h       |
| EPWM23_G1     | 5005 70C4h       |
| EPWM23_G2     | 5009 70C4h       |
| EPWM23_G3     | 500D 70C4h       |
| EPWM24_G0     | 5001 80C4h       |
| EPWM24_G1     | 5005 80C4h       |
| EPWM24_G2     | 5009 80C4h       |
| EPWM24_G3     | 500D 80C4h       |
| EPWM25_G0     | 5001 90C4h       |
| EPWM25_G1     | 5005 90C4h       |
| EPWM25_G2     | 5009 90C4h       |
| EPWM25_G3     | 500D 90C4h       |
| EPWM26_G0     | 5001 A0C4h       |
| EPWM26_G1     | 5005 A0C4h       |
| EPWM26_G2     | 5009 A0C4h       |
| EPWM26_G3     | 500D A0C4h       |
| EPWM27_G0     | 5001 B0C4h       |
| EPWM27_G1     | 5005 B0C4h       |
| EPWM27_G2     | 5009 B0C4h       |
| EPWM27_G3     | 500D B0C4h       |
| EPWM28_G0     | 5001 C0C4h       |
| EPWM28_G1     | 5005 C0C4h       |
| EPWM28_G2     | 5009 C0C4h       |
| EPWM28_G3     | 500D C0C4h       |
| EPWM29_G0     | 5001 D0C4h       |
| EPWM29_G1     | 5005 D0C4h       |
| EPWM29_G2     | 5009 D0C4h       |
| EPWM29_G3     | 500D D0C4h       |
| EPWM30_G0     | 5001 E0C4h       |
| EPWM30_G1     | 5005 E0C4h       |
| EPWM30_G2     | 5009 E0C4h       |
| EPWM30_G3     | 500D E0C4h       |
| EPWM31_G0     | 5001 F0C4h       |
| EPWM31_G1     | 5005 F0C4h       |
| EPWM31_G2     | 5009 F0C4h       |
| EPWM31_G3     | 500D F0C4h       |

**Figure 3-290. EPWM\_TBPRDHR Name Register**

|         |    |    |    |    |    |   |   |
|---------|----|----|----|----|----|---|---|
| 15      | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TBPRDHR |    |    |    |    |    |   |   |
| R/W     |    |    |    |    |    |   |   |
| 0h      |    |    |    |    |    |   |   |
| 7       | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| TBPRDHR |    |    |    |    |    |   |   |
| R/W     |    |    |    |    |    |   |   |
| 0h      |    |    |    |    |    |   |   |

**Table 3-930. EPWM\_TBPRDHR Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|------|---------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | TBPRDHR | R/W  | 0h    | <p>Period High Resolution Bits</p> <p>The upper 8-bits contain the high-resolution portion of the period value. The TBPRDHR register is not affected by the TBCTL[PRDLD] bit. Reads from this register always reflect the shadow register. Likewise writes are also to the shadow register. The TBPRDHR register is only used when the high resolution period feature is enabled. This register is only available with EPWM modules which support high-resolution period control.</p> <p>The lower 8 bits in this register are ignored - writes are ignored and reads return zero</p> |

### 3.7.2.40 EPWM\_TBPRD Register

#### 1 EPWM\_TBPRD Register (Offset = C6h) [reset = 0h]

Time Base Period Register .

Return to [Summary Table](#)

**Table 3-931. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 00C6h       |
| EPWM0_G1      | 5004 00C6h       |
| EPWM0_G2      | 5008 00C6h       |
| EPWM0_G3      | 500C 00C6h       |
| EPWM1_G0      | 5000 10C6h       |
| EPWM1_G1      | 5004 10C6h       |
| EPWM1_G2      | 5008 10C6h       |
| EPWM1_G3      | 500C 10C6h       |
| EPWM2_G0      | 5000 20C6h       |
| EPWM2_G1      | 5004 20C6h       |
| EPWM2_G2      | 5008 20C6h       |
| EPWM2_G3      | 500C 20C6h       |
| EPWM3_G0      | 5000 30C6h       |
| EPWM3_G1      | 5004 30C6h       |
| EPWM3_G2      | 5008 30C6h       |
| EPWM3_G3      | 500C 30C6h       |
| EPWM4_G0      | 5000 40C6h       |
| EPWM4_G1      | 5004 40C6h       |
| EPWM4_G2      | 5008 40C6h       |
| EPWM4_G3      | 500C 40C6h       |
| EPWM5_G0      | 5000 50C6h       |
| EPWM5_G1      | 5004 50C6h       |
| EPWM5_G2      | 5008 50C6h       |
| EPWM5_G3      | 500C 50C6h       |
| EPWM6_G0      | 5000 60C6h       |
| EPWM6_G1      | 5004 60C6h       |
| EPWM6_G2      | 5008 60C6h       |
| EPWM6_G3      | 500C 60C6h       |
| EPWM7_G0      | 5000 70C6h       |
| EPWM7_G1      | 5004 70C6h       |
| EPWM7_G2      | 5008 70C6h       |
| EPWM7_G3      | 500C 70C6h       |
| EPWM8_G0      | 5000 80C6h       |
| EPWM8_G1      | 5004 80C6h       |
| EPWM8_G2      | 5008 80C6h       |
| EPWM8_G3      | 500C 80C6h       |
| EPWM9_G0      | 5000 90C6h       |
| EPWM9_G1      | 5004 90C6h       |
| EPWM9_G2      | 5008 90C6h       |

**Table 3-931. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 90C6h       |
| EPWM10_G0     | 5000 A0C6h       |
| EPWM10_G1     | 5004 A0C6h       |
| EPWM10_G2     | 5008 A0C6h       |
| EPWM10_G3     | 500C A0C6h       |
| EPWM11_G0     | 5000 B0C6h       |
| EPWM11_G1     | 5004 B0C6h       |
| EPWM11_G2     | 5008 B0C6h       |
| EPWM11_G3     | 500C B0C6h       |
| EPWM12_G0     | 5000 C0C6h       |
| EPWM12_G1     | 5004 C0C6h       |
| EPWM12_G2     | 5008 C0C6h       |
| EPWM12_G3     | 500C C0C6h       |
| EPWM13_G0     | 5000 D0C6h       |
| EPWM13_G1     | 5004 D0C6h       |
| EPWM13_G2     | 5008 D0C6h       |
| EPWM13_G3     | 500C D0C6h       |
| EPWM14_G0     | 5000 E0C6h       |
| EPWM14_G1     | 5004 E0C6h       |
| EPWM14_G2     | 5008 E0C6h       |
| EPWM14_G3     | 500C E0C6h       |
| EPWM15_G0     | 5000 F0C6h       |
| EPWM15_G1     | 5004 F0C6h       |
| EPWM15_G2     | 5008 F0C6h       |
| EPWM15_G3     | 500C F0C6h       |
| EPWM16_G0     | 5001 00C6h       |
| EPWM16_G1     | 5005 00C6h       |
| EPWM16_G2     | 5009 00C6h       |
| EPWM16_G3     | 500D 00C6h       |
| EPWM17_G0     | 5001 10C6h       |
| EPWM17_G1     | 5005 10C6h       |
| EPWM17_G2     | 5009 10C6h       |
| EPWM17_G3     | 500D 10C6h       |
| EPWM18_G0     | 5001 20C6h       |
| EPWM18_G1     | 5005 20C6h       |
| EPWM18_G2     | 5009 20C6h       |
| EPWM18_G3     | 500D 20C6h       |
| EPWM19_G0     | 5001 30C6h       |
| EPWM19_G1     | 5005 30C6h       |
| EPWM19_G2     | 5009 30C6h       |
| EPWM19_G3     | 500D 30C6h       |
| EPWM20_G0     | 5001 40C6h       |
| EPWM20_G1     | 5005 40C6h       |
| EPWM20_G2     | 5009 40C6h       |
| EPWM20_G3     | 500D 40C6h       |

**Table 3-931. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 50C6h       |
| EPWM21_G1     | 5005 50C6h       |
| EPWM21_G2     | 5009 50C6h       |
| EPWM21_G3     | 500D 50C6h       |
| EPWM22_G0     | 5001 60C6h       |
| EPWM22_G1     | 5005 60C6h       |
| EPWM22_G2     | 5009 60C6h       |
| EPWM22_G3     | 500D 60C6h       |
| EPWM23_G0     | 5001 70C6h       |
| EPWM23_G1     | 5005 70C6h       |
| EPWM23_G2     | 5009 70C6h       |
| EPWM23_G3     | 500D 70C6h       |
| EPWM24_G0     | 5001 80C6h       |
| EPWM24_G1     | 5005 80C6h       |
| EPWM24_G2     | 5009 80C6h       |
| EPWM24_G3     | 500D 80C6h       |
| EPWM25_G0     | 5001 90C6h       |
| EPWM25_G1     | 5005 90C6h       |
| EPWM25_G2     | 5009 90C6h       |
| EPWM25_G3     | 500D 90C6h       |
| EPWM26_G0     | 5001 A0C6h       |
| EPWM26_G1     | 5005 A0C6h       |
| EPWM26_G2     | 5009 A0C6h       |
| EPWM26_G3     | 500D A0C6h       |
| EPWM27_G0     | 5001 B0C6h       |
| EPWM27_G1     | 5005 B0C6h       |
| EPWM27_G2     | 5009 B0C6h       |
| EPWM27_G3     | 500D B0C6h       |
| EPWM28_G0     | 5001 C0C6h       |
| EPWM28_G1     | 5005 C0C6h       |
| EPWM28_G2     | 5009 C0C6h       |
| EPWM28_G3     | 500D C0C6h       |
| EPWM29_G0     | 5001 D0C6h       |
| EPWM29_G1     | 5005 D0C6h       |
| EPWM29_G2     | 5009 D0C6h       |
| EPWM29_G3     | 500D D0C6h       |
| EPWM30_G0     | 5001 E0C6h       |
| EPWM30_G1     | 5005 E0C6h       |
| EPWM30_G2     | 5009 E0C6h       |
| EPWM30_G3     | 500D E0C6h       |
| EPWM31_G0     | 5001 F0C6h       |
| EPWM31_G1     | 5005 F0C6h       |
| EPWM31_G2     | 5009 F0C6h       |
| EPWM31_G3     | 500D F0C6h       |

**Figure 3-291. EPWM\_TBPRD Name Register**

|       |    |    |    |    |    |   |   |
|-------|----|----|----|----|----|---|---|
| 15    | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TBPRD |    |    |    |    |    |   |   |
| R/W   |    |    |    |    |    |   |   |
| 0h    |    |    |    |    |    |   |   |
| 7     | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| TBPRD |    |    |    |    |    |   |   |
| R/W   |    |    |    |    |    |   |   |
| 0h    |    |    |    |    |    |   |   |

**Table 3-933. EPWM\_TBPRD Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | TBPRD | R/W  | 0h    | <p>Time Base Period Register</p> <p>These bits determine the period of the time-base counter. This sets the PWM frequency. Shadowing of this register is enabled and disabled by the TBCTL[PRDLD] bit. By default this register is shadowed.</p> <ul style="list-style-type: none"> <li>- If TBCTL[PRDLD] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the active register will be loaded from the shadow register when the time-base counter equals zero.</li> <li>- If TBCTL[PRDLD] = 1, then the shadow is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware.</li> <li>- The active and shadow registers share the same memory map address.</li> </ul> |

### 3.7.2.41 EPWM\_TBPRDHRB Register

#### 1 EPWM\_TBPRDHRB Register (Offset = C8h) [reset = 0h]

Calculation Result for EPWMxB.

Return to [Summary Table](#)

**Table 3-934. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 00C8h       |
| EPWM0_G1      | 5004 00C8h       |
| EPWM0_G2      | 5008 00C8h       |
| EPWM0_G3      | 500C 00C8h       |
| EPWM1_G0      | 5000 10C8h       |
| EPWM1_G1      | 5004 10C8h       |
| EPWM1_G2      | 5008 10C8h       |
| EPWM1_G3      | 500C 10C8h       |
| EPWM2_G0      | 5000 20C8h       |
| EPWM2_G1      | 5004 20C8h       |
| EPWM2_G2      | 5008 20C8h       |
| EPWM2_G3      | 500C 20C8h       |
| EPWM3_G0      | 5000 30C8h       |
| EPWM3_G1      | 5004 30C8h       |
| EPWM3_G2      | 5008 30C8h       |
| EPWM3_G3      | 500C 30C8h       |
| EPWM4_G0      | 5000 40C8h       |
| EPWM4_G1      | 5004 40C8h       |
| EPWM4_G2      | 5008 40C8h       |
| EPWM4_G3      | 500C 40C8h       |
| EPWM5_G0      | 5000 50C8h       |
| EPWM5_G1      | 5004 50C8h       |
| EPWM5_G2      | 5008 50C8h       |
| EPWM5_G3      | 500C 50C8h       |
| EPWM6_G0      | 5000 60C8h       |
| EPWM6_G1      | 5004 60C8h       |
| EPWM6_G2      | 5008 60C8h       |
| EPWM6_G3      | 500C 60C8h       |
| EPWM7_G0      | 5000 70C8h       |
| EPWM7_G1      | 5004 70C8h       |
| EPWM7_G2      | 5008 70C8h       |
| EPWM7_G3      | 500C 70C8h       |
| EPWM8_G0      | 5000 80C8h       |
| EPWM8_G1      | 5004 80C8h       |
| EPWM8_G2      | 5008 80C8h       |
| EPWM8_G3      | 500C 80C8h       |
| EPWM9_G0      | 5000 90C8h       |
| EPWM9_G1      | 5004 90C8h       |
| EPWM9_G2      | 5008 90C8h       |

**Table 3-934. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 90C8h       |
| EPWM10_G0     | 5000 A0C8h       |
| EPWM10_G1     | 5004 A0C8h       |
| EPWM10_G2     | 5008 A0C8h       |
| EPWM10_G3     | 500C A0C8h       |
| EPWM11_G0     | 5000 B0C8h       |
| EPWM11_G1     | 5004 B0C8h       |
| EPWM11_G2     | 5008 B0C8h       |
| EPWM11_G3     | 500C B0C8h       |
| EPWM12_G0     | 5000 C0C8h       |
| EPWM12_G1     | 5004 C0C8h       |
| EPWM12_G2     | 5008 C0C8h       |
| EPWM12_G3     | 500C C0C8h       |
| EPWM13_G0     | 5000 D0C8h       |
| EPWM13_G1     | 5004 D0C8h       |
| EPWM13_G2     | 5008 D0C8h       |
| EPWM13_G3     | 500C D0C8h       |
| EPWM14_G0     | 5000 E0C8h       |
| EPWM14_G1     | 5004 E0C8h       |
| EPWM14_G2     | 5008 E0C8h       |
| EPWM14_G3     | 500C E0C8h       |
| EPWM15_G0     | 5000 F0C8h       |
| EPWM15_G1     | 5004 F0C8h       |
| EPWM15_G2     | 5008 F0C8h       |
| EPWM15_G3     | 500C F0C8h       |
| EPWM16_G0     | 5001 00C8h       |
| EPWM16_G1     | 5005 00C8h       |
| EPWM16_G2     | 5009 00C8h       |
| EPWM16_G3     | 500D 00C8h       |
| EPWM17_G0     | 5001 10C8h       |
| EPWM17_G1     | 5005 10C8h       |
| EPWM17_G2     | 5009 10C8h       |
| EPWM17_G3     | 500D 10C8h       |
| EPWM18_G0     | 5001 20C8h       |
| EPWM18_G1     | 5005 20C8h       |
| EPWM18_G2     | 5009 20C8h       |
| EPWM18_G3     | 500D 20C8h       |
| EPWM19_G0     | 5001 30C8h       |
| EPWM19_G1     | 5005 30C8h       |
| EPWM19_G2     | 5009 30C8h       |
| EPWM19_G3     | 500D 30C8h       |
| EPWM20_G0     | 5001 40C8h       |
| EPWM20_G1     | 5005 40C8h       |
| EPWM20_G2     | 5009 40C8h       |
| EPWM20_G3     | 500D 40C8h       |



**Table 3-934. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 50C8h       |
| EPWM21_G1     | 5005 50C8h       |
| EPWM21_G2     | 5009 50C8h       |
| EPWM21_G3     | 500D 50C8h       |
| EPWM22_G0     | 5001 60C8h       |
| EPWM22_G1     | 5005 60C8h       |
| EPWM22_G2     | 5009 60C8h       |
| EPWM22_G3     | 500D 60C8h       |
| EPWM23_G0     | 5001 70C8h       |
| EPWM23_G1     | 5005 70C8h       |
| EPWM23_G2     | 5009 70C8h       |
| EPWM23_G3     | 500D 70C8h       |
| EPWM24_G0     | 5001 80C8h       |
| EPWM24_G1     | 5005 80C8h       |
| EPWM24_G2     | 5009 80C8h       |
| EPWM24_G3     | 500D 80C8h       |
| EPWM25_G0     | 5001 90C8h       |
| EPWM25_G1     | 5005 90C8h       |
| EPWM25_G2     | 5009 90C8h       |
| EPWM25_G3     | 500D 90C8h       |
| EPWM26_G0     | 5001 A0C8h       |
| EPWM26_G1     | 5005 A0C8h       |
| EPWM26_G2     | 5009 A0C8h       |
| EPWM26_G3     | 500D A0C8h       |
| EPWM27_G0     | 5001 B0C8h       |
| EPWM27_G1     | 5005 B0C8h       |
| EPWM27_G2     | 5009 B0C8h       |
| EPWM27_G3     | 500D B0C8h       |
| EPWM28_G0     | 5001 C0C8h       |
| EPWM28_G1     | 5005 C0C8h       |
| EPWM28_G2     | 5009 C0C8h       |
| EPWM28_G3     | 500D C0C8h       |
| EPWM29_G0     | 5001 D0C8h       |
| EPWM29_G1     | 5005 D0C8h       |
| EPWM29_G2     | 5009 D0C8h       |
| EPWM29_G3     | 500D D0C8h       |
| EPWM30_G0     | 5001 E0C8h       |
| EPWM30_G1     | 5005 E0C8h       |
| EPWM30_G2     | 5009 E0C8h       |
| EPWM30_G3     | 500D E0C8h       |
| EPWM31_G0     | 5001 F0C8h       |
| EPWM31_G1     | 5005 F0C8h       |
| EPWM31_G2     | 5009 F0C8h       |
| EPWM31_G3     | 500D F0C8h       |

**Figure 3-292. EPWM\_TBPRDHRB Name Register**

|                |    |    |    |    |    |   |   |
|----------------|----|----|----|----|----|---|---|
| 15             | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| TBPRDHRB       |    |    |    |    |    |   |   |
| R/W            |    |    |    |    |    |   |   |
| 0h             |    |    |    |    |    |   |   |
| 7              | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| TBPRDHRB_DELAY |    |    |    |    |    |   |   |
| R/W            |    |    |    |    |    |   |   |
| 0h             |    |    |    |    |    |   |   |

**Table 3-936. EPWM\_TBPRDHRB Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                              |
|------|----------------|------|-------|--------------------------------------------------------------------------|
| 15:8 | TBPRDHRB       | R/W  | 0h    | TBPRD High Resolution Calculation [2] Results for EPWMxB HRPWM Equations |
| 7:0  | TBPRDHRB_DELAY | R/W  | 0h    | TBPRDHRB Delay                                                           |

### 3.7.2.42 EPWM\_CMPA Register

#### 1 EPWM\_CMPA Register (Offset = D4h) [reset = 0h]

Counter Compare A Register .

Return to [Summary Table](#)

**Table 3-937. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 00D4h       |
| EPWM0_G1      | 5004 00D4h       |
| EPWM0_G2      | 5008 00D4h       |
| EPWM0_G3      | 500C 00D4h       |
| EPWM1_G0      | 5000 10D4h       |
| EPWM1_G1      | 5004 10D4h       |
| EPWM1_G2      | 5008 10D4h       |
| EPWM1_G3      | 500C 10D4h       |
| EPWM2_G0      | 5000 20D4h       |
| EPWM2_G1      | 5004 20D4h       |
| EPWM2_G2      | 5008 20D4h       |
| EPWM2_G3      | 500C 20D4h       |
| EPWM3_G0      | 5000 30D4h       |
| EPWM3_G1      | 5004 30D4h       |
| EPWM3_G2      | 5008 30D4h       |
| EPWM3_G3      | 500C 30D4h       |
| EPWM4_G0      | 5000 40D4h       |
| EPWM4_G1      | 5004 40D4h       |
| EPWM4_G2      | 5008 40D4h       |
| EPWM4_G3      | 500C 40D4h       |
| EPWM5_G0      | 5000 50D4h       |
| EPWM5_G1      | 5004 50D4h       |
| EPWM5_G2      | 5008 50D4h       |
| EPWM5_G3      | 500C 50D4h       |
| EPWM6_G0      | 5000 60D4h       |
| EPWM6_G1      | 5004 60D4h       |
| EPWM6_G2      | 5008 60D4h       |
| EPWM6_G3      | 500C 60D4h       |
| EPWM7_G0      | 5000 70D4h       |
| EPWM7_G1      | 5004 70D4h       |
| EPWM7_G2      | 5008 70D4h       |
| EPWM7_G3      | 500C 70D4h       |
| EPWM8_G0      | 5000 80D4h       |
| EPWM8_G1      | 5004 80D4h       |
| EPWM8_G2      | 5008 80D4h       |
| EPWM8_G3      | 500C 80D4h       |
| EPWM9_G0      | 5000 90D4h       |
| EPWM9_G1      | 5004 90D4h       |
| EPWM9_G2      | 5008 90D4h       |

**Table 3-937. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 90D4h       |
| EPWM10_G0     | 5000 A0D4h       |
| EPWM10_G1     | 5004 A0D4h       |
| EPWM10_G2     | 5008 A0D4h       |
| EPWM10_G3     | 500C A0D4h       |
| EPWM11_G0     | 5000 B0D4h       |
| EPWM11_G1     | 5004 B0D4h       |
| EPWM11_G2     | 5008 B0D4h       |
| EPWM11_G3     | 500C B0D4h       |
| EPWM12_G0     | 5000 C0D4h       |
| EPWM12_G1     | 5004 C0D4h       |
| EPWM12_G2     | 5008 C0D4h       |
| EPWM12_G3     | 500C C0D4h       |
| EPWM13_G0     | 5000 D0D4h       |
| EPWM13_G1     | 5004 D0D4h       |
| EPWM13_G2     | 5008 D0D4h       |
| EPWM13_G3     | 500C D0D4h       |
| EPWM14_G0     | 5000 E0D4h       |
| EPWM14_G1     | 5004 E0D4h       |
| EPWM14_G2     | 5008 E0D4h       |
| EPWM14_G3     | 500C E0D4h       |
| EPWM15_G0     | 5000 F0D4h       |
| EPWM15_G1     | 5004 F0D4h       |
| EPWM15_G2     | 5008 F0D4h       |
| EPWM15_G3     | 500C F0D4h       |
| EPWM16_G0     | 5001 00D4h       |
| EPWM16_G1     | 5005 00D4h       |
| EPWM16_G2     | 5009 00D4h       |
| EPWM16_G3     | 500D 00D4h       |
| EPWM17_G0     | 5001 10D4h       |
| EPWM17_G1     | 5005 10D4h       |
| EPWM17_G2     | 5009 10D4h       |
| EPWM17_G3     | 500D 10D4h       |
| EPWM18_G0     | 5001 20D4h       |
| EPWM18_G1     | 5005 20D4h       |
| EPWM18_G2     | 5009 20D4h       |
| EPWM18_G3     | 500D 20D4h       |
| EPWM19_G0     | 5001 30D4h       |
| EPWM19_G1     | 5005 30D4h       |
| EPWM19_G2     | 5009 30D4h       |
| EPWM19_G3     | 500D 30D4h       |
| EPWM20_G0     | 5001 40D4h       |
| EPWM20_G1     | 5005 40D4h       |
| EPWM20_G2     | 5009 40D4h       |
| EPWM20_G3     | 500D 40D4h       |

**Table 3-937. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 50D4h       |
| EPWM21_G1     | 5005 50D4h       |
| EPWM21_G2     | 5009 50D4h       |
| EPWM21_G3     | 500D 50D4h       |
| EPWM22_G0     | 5001 60D4h       |
| EPWM22_G1     | 5005 60D4h       |
| EPWM22_G2     | 5009 60D4h       |
| EPWM22_G3     | 500D 60D4h       |
| EPWM23_G0     | 5001 70D4h       |
| EPWM23_G1     | 5005 70D4h       |
| EPWM23_G2     | 5009 70D4h       |
| EPWM23_G3     | 500D 70D4h       |
| EPWM24_G0     | 5001 80D4h       |
| EPWM24_G1     | 5005 80D4h       |
| EPWM24_G2     | 5009 80D4h       |
| EPWM24_G3     | 500D 80D4h       |
| EPWM25_G0     | 5001 90D4h       |
| EPWM25_G1     | 5005 90D4h       |
| EPWM25_G2     | 5009 90D4h       |
| EPWM25_G3     | 500D 90D4h       |
| EPWM26_G0     | 5001 A0D4h       |
| EPWM26_G1     | 5005 A0D4h       |
| EPWM26_G2     | 5009 A0D4h       |
| EPWM26_G3     | 500D A0D4h       |
| EPWM27_G0     | 5001 B0D4h       |
| EPWM27_G1     | 5005 B0D4h       |
| EPWM27_G2     | 5009 B0D4h       |
| EPWM27_G3     | 500D B0D4h       |
| EPWM28_G0     | 5001 C0D4h       |
| EPWM28_G1     | 5005 C0D4h       |
| EPWM28_G2     | 5009 C0D4h       |
| EPWM28_G3     | 500D C0D4h       |
| EPWM29_G0     | 5001 D0D4h       |
| EPWM29_G1     | 5005 D0D4h       |
| EPWM29_G2     | 5009 D0D4h       |
| EPWM29_G3     | 500D D0D4h       |
| EPWM30_G0     | 5001 E0D4h       |
| EPWM30_G1     | 5005 E0D4h       |
| EPWM30_G2     | 5009 E0D4h       |
| EPWM30_G3     | 500D E0D4h       |
| EPWM31_G0     | 5001 F0D4h       |
| EPWM31_G1     | 5005 F0D4h       |
| EPWM31_G2     | 5009 F0D4h       |
| EPWM31_G3     | 500D F0D4h       |

**Figure 3-293. EPWM\_CMPA Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMPA   |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMPA   |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMPAHR |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMPAHR |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 3-939. EPWM\_CMPA Register Field Descriptions**

| Bit   | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|--------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | CMPA   | R/W  | 0h    | <p>Compare A Register</p> <p>The value in the active CMPA register is continuously compared to the time-base counter [TBCTR]. When the values are equal, the counter-compare module generates a "time-base counter equal to counter compare A" event. This event is sent to the action-qualifier where it is qualified and converted it into one or more actions. These actions can be applied to either the EPWMxA or the EPWMxB output depending on the configuration of the AQCTLA and AQCTLB registers. The actions that can be defined in the AQCTLA and AQCTLB registers include:</p> <ul style="list-style-type: none"> <li>- Do nothing</li> <li>- the event is ignored.</li> <li>- Clear: Pull the EPWMxA and/or EPWMxB signal low</li> <li>- Set: Pull the EPWMxA and/or EPWMxB signal high</li> <li>- Toggle the EPWMxA and/or EPWMxB signal</li> </ul> <p>Shadowing of this register is enabled and disabled by the CMPCTL[SHDWAMODE] bit. By default this register is shadowed.</p> <ul style="list-style-type: none"> <li>- If CMPCTL[SHDWAMODE] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the CMPCTL[LOADAMODE] bit field determines which event will load the active register from the shadow register.</li> <li>- Before a write, the CMPCTL[SHDWAFULL] bit can be read to determine if the shadow register is currently full.</li> <li>- If CMPCTL[SHDWAMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware.</li> <li>- In either mode, the active and shadow registers share the same memory map address.</li> </ul> |
| 15:0  | CMPAHR | R/W  | 0h    | <p>Compare A HRPWM Extension Register</p> <p>The UPPER 8-bits contain the high-resolution portion [most significant 8-bits] of the counter-compare A value. CMPA:CMPAHR can be accessed in a single 32-bit read/write. Shadowing is enabled and disabled by the CMPCTL[SHDWAMODE] bit as described for the CMPA register.</p> <p>The lower 8 bits in this register are ignored</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

### 3.7.2.43 EPWM\_CMPB Register

#### 1 EPWM\_CMPB Register (Offset = D8h) [reset = 0h]

Compare B Register .

Return to [Summary Table](#)

**Table 3-940. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 00D8h       |
| EPWM0_G1      | 5004 00D8h       |
| EPWM0_G2      | 5008 00D8h       |
| EPWM0_G3      | 500C 00D8h       |
| EPWM1_G0      | 5000 10D8h       |
| EPWM1_G1      | 5004 10D8h       |
| EPWM1_G2      | 5008 10D8h       |
| EPWM1_G3      | 500C 10D8h       |
| EPWM2_G0      | 5000 20D8h       |
| EPWM2_G1      | 5004 20D8h       |
| EPWM2_G2      | 5008 20D8h       |
| EPWM2_G3      | 500C 20D8h       |
| EPWM3_G0      | 5000 30D8h       |
| EPWM3_G1      | 5004 30D8h       |
| EPWM3_G2      | 5008 30D8h       |
| EPWM3_G3      | 500C 30D8h       |
| EPWM4_G0      | 5000 40D8h       |
| EPWM4_G1      | 5004 40D8h       |
| EPWM4_G2      | 5008 40D8h       |
| EPWM4_G3      | 500C 40D8h       |
| EPWM5_G0      | 5000 50D8h       |
| EPWM5_G1      | 5004 50D8h       |
| EPWM5_G2      | 5008 50D8h       |
| EPWM5_G3      | 500C 50D8h       |
| EPWM6_G0      | 5000 60D8h       |
| EPWM6_G1      | 5004 60D8h       |
| EPWM6_G2      | 5008 60D8h       |
| EPWM6_G3      | 500C 60D8h       |
| EPWM7_G0      | 5000 70D8h       |
| EPWM7_G1      | 5004 70D8h       |
| EPWM7_G2      | 5008 70D8h       |
| EPWM7_G3      | 500C 70D8h       |
| EPWM8_G0      | 5000 80D8h       |
| EPWM8_G1      | 5004 80D8h       |
| EPWM8_G2      | 5008 80D8h       |
| EPWM8_G3      | 500C 80D8h       |
| EPWM9_G0      | 5000 90D8h       |
| EPWM9_G1      | 5004 90D8h       |
| EPWM9_G2      | 5008 90D8h       |

**Table 3-940. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 90D8h       |
| EPWM10_G0     | 5000 A0D8h       |
| EPWM10_G1     | 5004 A0D8h       |
| EPWM10_G2     | 5008 A0D8h       |
| EPWM10_G3     | 500C A0D8h       |
| EPWM11_G0     | 5000 B0D8h       |
| EPWM11_G1     | 5004 B0D8h       |
| EPWM11_G2     | 5008 B0D8h       |
| EPWM11_G3     | 500C B0D8h       |
| EPWM12_G0     | 5000 C0D8h       |
| EPWM12_G1     | 5004 C0D8h       |
| EPWM12_G2     | 5008 C0D8h       |
| EPWM12_G3     | 500C C0D8h       |
| EPWM13_G0     | 5000 D0D8h       |
| EPWM13_G1     | 5004 D0D8h       |
| EPWM13_G2     | 5008 D0D8h       |
| EPWM13_G3     | 500C D0D8h       |
| EPWM14_G0     | 5000 E0D8h       |
| EPWM14_G1     | 5004 E0D8h       |
| EPWM14_G2     | 5008 E0D8h       |
| EPWM14_G3     | 500C E0D8h       |
| EPWM15_G0     | 5000 F0D8h       |
| EPWM15_G1     | 5004 F0D8h       |
| EPWM15_G2     | 5008 F0D8h       |
| EPWM15_G3     | 500C F0D8h       |
| EPWM16_G0     | 5001 00D8h       |
| EPWM16_G1     | 5005 00D8h       |
| EPWM16_G2     | 5009 00D8h       |
| EPWM16_G3     | 500D 00D8h       |
| EPWM17_G0     | 5001 10D8h       |
| EPWM17_G1     | 5005 10D8h       |
| EPWM17_G2     | 5009 10D8h       |
| EPWM17_G3     | 500D 10D8h       |
| EPWM18_G0     | 5001 20D8h       |
| EPWM18_G1     | 5005 20D8h       |
| EPWM18_G2     | 5009 20D8h       |
| EPWM18_G3     | 500D 20D8h       |
| EPWM19_G0     | 5001 30D8h       |
| EPWM19_G1     | 5005 30D8h       |
| EPWM19_G2     | 5009 30D8h       |
| EPWM19_G3     | 500D 30D8h       |
| EPWM20_G0     | 5001 40D8h       |
| EPWM20_G1     | 5005 40D8h       |
| EPWM20_G2     | 5009 40D8h       |
| EPWM20_G3     | 500D 40D8h       |



**Table 3-940. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 50D8h       |
| EPWM21_G1     | 5005 50D8h       |
| EPWM21_G2     | 5009 50D8h       |
| EPWM21_G3     | 500D 50D8h       |
| EPWM22_G0     | 5001 60D8h       |
| EPWM22_G1     | 5005 60D8h       |
| EPWM22_G2     | 5009 60D8h       |
| EPWM22_G3     | 500D 60D8h       |
| EPWM23_G0     | 5001 70D8h       |
| EPWM23_G1     | 5005 70D8h       |
| EPWM23_G2     | 5009 70D8h       |
| EPWM23_G3     | 500D 70D8h       |
| EPWM24_G0     | 5001 80D8h       |
| EPWM24_G1     | 5005 80D8h       |
| EPWM24_G2     | 5009 80D8h       |
| EPWM24_G3     | 500D 80D8h       |
| EPWM25_G0     | 5001 90D8h       |
| EPWM25_G1     | 5005 90D8h       |
| EPWM25_G2     | 5009 90D8h       |
| EPWM25_G3     | 500D 90D8h       |
| EPWM26_G0     | 5001 A0D8h       |
| EPWM26_G1     | 5005 A0D8h       |
| EPWM26_G2     | 5009 A0D8h       |
| EPWM26_G3     | 500D A0D8h       |
| EPWM27_G0     | 5001 B0D8h       |
| EPWM27_G1     | 5005 B0D8h       |
| EPWM27_G2     | 5009 B0D8h       |
| EPWM27_G3     | 500D B0D8h       |
| EPWM28_G0     | 5001 C0D8h       |
| EPWM28_G1     | 5005 C0D8h       |
| EPWM28_G2     | 5009 C0D8h       |
| EPWM28_G3     | 500D C0D8h       |
| EPWM29_G0     | 5001 D0D8h       |
| EPWM29_G1     | 5005 D0D8h       |
| EPWM29_G2     | 5009 D0D8h       |
| EPWM29_G3     | 500D D0D8h       |
| EPWM30_G0     | 5001 E0D8h       |
| EPWM30_G1     | 5005 E0D8h       |
| EPWM30_G2     | 5009 E0D8h       |
| EPWM30_G3     | 500D E0D8h       |
| EPWM31_G0     | 5001 F0D8h       |
| EPWM31_G1     | 5005 F0D8h       |
| EPWM31_G2     | 5009 F0D8h       |
| EPWM31_G3     | 500D F0D8h       |

**Figure 3-294. EPWM\_CMPB Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMPB   |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMPB   |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMPBHR |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMPBHR |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 3-942. EPWM\_CMPB Register Field Descriptions**

| Bit   | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|--------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | CMPB   | R/W  | 0h    | <p>Compare B Register</p> <p>The value in the active CMPB register is continuously compared to the time-base counter [TBCTR]. When the values are equal, the counter-compare module generates a "time-base counter equal to counter compare B" event. This event is sent to the action-qualifier where it is qualified and converted it into one or more actions. These actions can be applied to either the EPWMxA or the EPWMxB output depending on the configuration of the AQCTLA and AQCTLB registers. The actions that can be defined in the AQCTLA and AQCTLB registers include:</p> <ul style="list-style-type: none"> <li>- Do nothing</li> <li>- the event is ignored.</li> <li>- Clear: Pull the EPWMxA and/or EPWMxB signal low</li> <li>- Set: Pull the EPWMxA and/or EPWMxB signal high</li> <li>- Toggle the EPWMxA and/or EPWMxB signal</li> </ul> <p>Shadowing of this register is enabled and disabled by the CMPCTL[SHDWBMODE] bit. By default this register is shadowed.</p> <ul style="list-style-type: none"> <li>- If CMPCTL[SHDWBMODE] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the CMPCTL[LOADBMODE] bit field determines which event will load the active register from the shadow register.</li> <li>- Before a write, the CMPCTL[SHDWBFULL] bit can be read to determine if the shadow register is currently full.</li> <li>- If CMPCTL[SHDWBMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register, that is the register actively controlling the hardware.</li> <li>- In either mode, the active and shadow registers share the same memory map address.</li> </ul> |
| 15:0  | CMPBHR | R/W  | 0h    | <p>Compare B High Resolution Bits</p> <p>The lower 8 bits in this register are ignored</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

### 3.7.2.44 EPWM\_CMPC Register

#### 1 EPWM\_CMPC Register (Offset = DEh) [reset = 0h]

Counter Compare C Register

LINK feature access should always be 16-bit.

Return to [Summary Table](#)

**Table 3-943. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 00DEh       |
| EPWM0_G1      | 5004 00DEh       |
| EPWM0_G2      | 5008 00DEh       |
| EPWM0_G3      | 500C 00DEh       |
| EPWM1_G0      | 5000 10DEh       |
| EPWM1_G1      | 5004 10DEh       |
| EPWM1_G2      | 5008 10DEh       |
| EPWM1_G3      | 500C 10DEh       |
| EPWM2_G0      | 5000 20DEh       |
| EPWM2_G1      | 5004 20DEh       |
| EPWM2_G2      | 5008 20DEh       |
| EPWM2_G3      | 500C 20DEh       |
| EPWM3_G0      | 5000 30DEh       |
| EPWM3_G1      | 5004 30DEh       |
| EPWM3_G2      | 5008 30DEh       |
| EPWM3_G3      | 500C 30DEh       |
| EPWM4_G0      | 5000 40DEh       |
| EPWM4_G1      | 5004 40DEh       |
| EPWM4_G2      | 5008 40DEh       |
| EPWM4_G3      | 500C 40DEh       |
| EPWM5_G0      | 5000 50DEh       |
| EPWM5_G1      | 5004 50DEh       |
| EPWM5_G2      | 5008 50DEh       |
| EPWM5_G3      | 500C 50DEh       |
| EPWM6_G0      | 5000 60DEh       |
| EPWM6_G1      | 5004 60DEh       |
| EPWM6_G2      | 5008 60DEh       |
| EPWM6_G3      | 500C 60DEh       |
| EPWM7_G0      | 5000 70DEh       |
| EPWM7_G1      | 5004 70DEh       |
| EPWM7_G2      | 5008 70DEh       |
| EPWM7_G3      | 500C 70DEh       |
| EPWM8_G0      | 5000 80DEh       |
| EPWM8_G1      | 5004 80DEh       |
| EPWM8_G2      | 5008 80DEh       |
| EPWM8_G3      | 500C 80DEh       |
| EPWM9_G0      | 5000 90DEh       |
| EPWM9_G1      | 5004 90DEh       |

**Table 3-943. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G2      | 5008 90DEh       |
| EPWM9_G3      | 500C 90DEh       |
| EPWM10_G0     | 5000 A0DEh       |
| EPWM10_G1     | 5004 A0DEh       |
| EPWM10_G2     | 5008 A0DEh       |
| EPWM10_G3     | 500C A0DEh       |
| EPWM11_G0     | 5000 B0DEh       |
| EPWM11_G1     | 5004 B0DEh       |
| EPWM11_G2     | 5008 B0DEh       |
| EPWM11_G3     | 500C B0DEh       |
| EPWM12_G0     | 5000 C0DEh       |
| EPWM12_G1     | 5004 C0DEh       |
| EPWM12_G2     | 5008 C0DEh       |
| EPWM12_G3     | 500C C0DEh       |
| EPWM13_G0     | 5000 D0DEh       |
| EPWM13_G1     | 5004 D0DEh       |
| EPWM13_G2     | 5008 D0DEh       |
| EPWM13_G3     | 500C D0DEh       |
| EPWM14_G0     | 5000 E0DEh       |
| EPWM14_G1     | 5004 E0DEh       |
| EPWM14_G2     | 5008 E0DEh       |
| EPWM14_G3     | 500C E0DEh       |
| EPWM15_G0     | 5000 F0DEh       |
| EPWM15_G1     | 5004 F0DEh       |
| EPWM15_G2     | 5008 F0DEh       |
| EPWM15_G3     | 500C F0DEh       |
| EPWM16_G0     | 5001 00DEh       |
| EPWM16_G1     | 5005 00DEh       |
| EPWM16_G2     | 5009 00DEh       |
| EPWM16_G3     | 500D 00DEh       |
| EPWM17_G0     | 5001 10DEh       |
| EPWM17_G1     | 5005 10DEh       |
| EPWM17_G2     | 5009 10DEh       |
| EPWM17_G3     | 500D 10DEh       |
| EPWM18_G0     | 5001 20DEh       |
| EPWM18_G1     | 5005 20DEh       |
| EPWM18_G2     | 5009 20DEh       |
| EPWM18_G3     | 500D 20DEh       |
| EPWM19_G0     | 5001 30DEh       |
| EPWM19_G1     | 5005 30DEh       |
| EPWM19_G2     | 5009 30DEh       |
| EPWM19_G3     | 500D 30DEh       |
| EPWM20_G0     | 5001 40DEh       |
| EPWM20_G1     | 5005 40DEh       |
| EPWM20_G2     | 5009 40DEh       |

**Table 3-943. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM20_G3     | 500D 40DEh       |
| EPWM21_G0     | 5001 50DEh       |
| EPWM21_G1     | 5005 50DEh       |
| EPWM21_G2     | 5009 50DEh       |
| EPWM21_G3     | 500D 50DEh       |
| EPWM22_G0     | 5001 60DEh       |
| EPWM22_G1     | 5005 60DEh       |
| EPWM22_G2     | 5009 60DEh       |
| EPWM22_G3     | 500D 60DEh       |
| EPWM23_G0     | 5001 70DEh       |
| EPWM23_G1     | 5005 70DEh       |
| EPWM23_G2     | 5009 70DEh       |
| EPWM23_G3     | 500D 70DEh       |
| EPWM24_G0     | 5001 80DEh       |
| EPWM24_G1     | 5005 80DEh       |
| EPWM24_G2     | 5009 80DEh       |
| EPWM24_G3     | 500D 80DEh       |
| EPWM25_G0     | 5001 90DEh       |
| EPWM25_G1     | 5005 90DEh       |
| EPWM25_G2     | 5009 90DEh       |
| EPWM25_G3     | 500D 90DEh       |
| EPWM26_G0     | 5001 A0DEh       |
| EPWM26_G1     | 5005 A0DEh       |
| EPWM26_G2     | 5009 A0DEh       |
| EPWM26_G3     | 500D A0DEh       |
| EPWM27_G0     | 5001 B0DEh       |
| EPWM27_G1     | 5005 B0DEh       |
| EPWM27_G2     | 5009 B0DEh       |
| EPWM27_G3     | 500D B0DEh       |
| EPWM28_G0     | 5001 C0DEh       |
| EPWM28_G1     | 5005 C0DEh       |
| EPWM28_G2     | 5009 C0DEh       |
| EPWM28_G3     | 500D C0DEh       |
| EPWM29_G0     | 5001 D0DEh       |
| EPWM29_G1     | 5005 D0DEh       |
| EPWM29_G2     | 5009 D0DEh       |
| EPWM29_G3     | 500D D0DEh       |
| EPWM30_G0     | 5001 E0DEh       |
| EPWM30_G1     | 5005 E0DEh       |
| EPWM30_G2     | 5009 E0DEh       |
| EPWM30_G3     | 500D E0DEh       |
| EPWM31_G0     | 5001 F0DEh       |
| EPWM31_G1     | 5005 F0DEh       |
| EPWM31_G2     | 5009 F0DEh       |

**Table 3-943. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM31_G3     | 500D F0DEh       |

**Figure 3-295. EPWM\_CMPC Name Register**

|      |    |    |    |    |    |   |   |
|------|----|----|----|----|----|---|---|
| 15   | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMPC |    |    |    |    |    |   |   |
| R/W  |    |    |    |    |    |   |   |
| 0h   |    |    |    |    |    |   |   |
| 7    | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| CMPC |    |    |    |    |    |   |   |
| R/W  |    |    |    |    |    |   |   |
| 0h   |    |    |    |    |    |   |   |

**Table 3-945. EPWM\_CMPC Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | CMPC  | R/W  | 0h    | <p>Compare C Register</p> <p>The value in the active CMPC register is continuously compared to the time-base counter [TBCTR]. When the values are equal, the counter-compare module generates a "time-base counter equal to counter compare C" event.</p> <p>Shadowing of this register is enabled and disabled by the CMPCTL2[SHDWCMODE] bit. By default this register is shadowed.</p> <ul style="list-style-type: none"> <li>- If CMPCTL2[SHDWCMODE] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the CMPCTL2[LOADCMODE] bit field determines which event will load the active register from the shadow register:</li> <li>- If CMPCTL2[SHDWCMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register that is, the register actively controlling the hardware.</li> <li>- In either mode, the active and shadow registers share the same memory map address.</li> </ul> |

### 3.7.2.45 EPWM\_CMPD Register

#### 1 EPWM\_CMPD Register (Offset = E2h) [reset = 0h]

Counter Compare D Register

LINK feature access should always be 16-bit.

Return to [Summary Table](#)

**Table 3-946. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 00E2h       |
| EPWM0_G1      | 5004 00E2h       |
| EPWM0_G2      | 5008 00E2h       |
| EPWM0_G3      | 500C 00E2h       |
| EPWM1_G0      | 5000 10E2h       |
| EPWM1_G1      | 5004 10E2h       |
| EPWM1_G2      | 5008 10E2h       |
| EPWM1_G3      | 500C 10E2h       |
| EPWM2_G0      | 5000 20E2h       |
| EPWM2_G1      | 5004 20E2h       |
| EPWM2_G2      | 5008 20E2h       |
| EPWM2_G3      | 500C 20E2h       |
| EPWM3_G0      | 5000 30E2h       |
| EPWM3_G1      | 5004 30E2h       |
| EPWM3_G2      | 5008 30E2h       |
| EPWM3_G3      | 500C 30E2h       |
| EPWM4_G0      | 5000 40E2h       |
| EPWM4_G1      | 5004 40E2h       |
| EPWM4_G2      | 5008 40E2h       |
| EPWM4_G3      | 500C 40E2h       |
| EPWM5_G0      | 5000 50E2h       |
| EPWM5_G1      | 5004 50E2h       |
| EPWM5_G2      | 5008 50E2h       |
| EPWM5_G3      | 500C 50E2h       |
| EPWM6_G0      | 5000 60E2h       |
| EPWM6_G1      | 5004 60E2h       |
| EPWM6_G2      | 5008 60E2h       |
| EPWM6_G3      | 500C 60E2h       |
| EPWM7_G0      | 5000 70E2h       |
| EPWM7_G1      | 5004 70E2h       |
| EPWM7_G2      | 5008 70E2h       |
| EPWM7_G3      | 500C 70E2h       |
| EPWM8_G0      | 5000 80E2h       |
| EPWM8_G1      | 5004 80E2h       |
| EPWM8_G2      | 5008 80E2h       |
| EPWM8_G3      | 500C 80E2h       |
| EPWM9_G0      | 5000 90E2h       |
| EPWM9_G1      | 5004 90E2h       |

**Table 3-946. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G2      | 5008 90E2h       |
| EPWM9_G3      | 500C 90E2h       |
| EPWM10_G0     | 5000 A0E2h       |
| EPWM10_G1     | 5004 A0E2h       |
| EPWM10_G2     | 5008 A0E2h       |
| EPWM10_G3     | 500C A0E2h       |
| EPWM11_G0     | 5000 B0E2h       |
| EPWM11_G1     | 5004 B0E2h       |
| EPWM11_G2     | 5008 B0E2h       |
| EPWM11_G3     | 500C B0E2h       |
| EPWM12_G0     | 5000 C0E2h       |
| EPWM12_G1     | 5004 C0E2h       |
| EPWM12_G2     | 5008 C0E2h       |
| EPWM12_G3     | 500C C0E2h       |
| EPWM13_G0     | 5000 D0E2h       |
| EPWM13_G1     | 5004 D0E2h       |
| EPWM13_G2     | 5008 D0E2h       |
| EPWM13_G3     | 500C D0E2h       |
| EPWM14_G0     | 5000 E0E2h       |
| EPWM14_G1     | 5004 E0E2h       |
| EPWM14_G2     | 5008 E0E2h       |
| EPWM14_G3     | 500C E0E2h       |
| EPWM15_G0     | 5000 F0E2h       |
| EPWM15_G1     | 5004 F0E2h       |
| EPWM15_G2     | 5008 F0E2h       |
| EPWM15_G3     | 500C F0E2h       |
| EPWM16_G0     | 5001 00E2h       |
| EPWM16_G1     | 5005 00E2h       |
| EPWM16_G2     | 5009 00E2h       |
| EPWM16_G3     | 500D 00E2h       |
| EPWM17_G0     | 5001 10E2h       |
| EPWM17_G1     | 5005 10E2h       |
| EPWM17_G2     | 5009 10E2h       |
| EPWM17_G3     | 500D 10E2h       |
| EPWM18_G0     | 5001 20E2h       |
| EPWM18_G1     | 5005 20E2h       |
| EPWM18_G2     | 5009 20E2h       |
| EPWM18_G3     | 500D 20E2h       |
| EPWM19_G0     | 5001 30E2h       |
| EPWM19_G1     | 5005 30E2h       |
| EPWM19_G2     | 5009 30E2h       |
| EPWM19_G3     | 500D 30E2h       |
| EPWM20_G0     | 5001 40E2h       |
| EPWM20_G1     | 5005 40E2h       |
| EPWM20_G2     | 5009 40E2h       |



**Table 3-946. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM20_G3     | 500D 40E2h       |
| EPWM21_G0     | 5001 50E2h       |
| EPWM21_G1     | 5005 50E2h       |
| EPWM21_G2     | 5009 50E2h       |
| EPWM21_G3     | 500D 50E2h       |
| EPWM22_G0     | 5001 60E2h       |
| EPWM22_G1     | 5005 60E2h       |
| EPWM22_G2     | 5009 60E2h       |
| EPWM22_G3     | 500D 60E2h       |
| EPWM23_G0     | 5001 70E2h       |
| EPWM23_G1     | 5005 70E2h       |
| EPWM23_G2     | 5009 70E2h       |
| EPWM23_G3     | 500D 70E2h       |
| EPWM24_G0     | 5001 80E2h       |
| EPWM24_G1     | 5005 80E2h       |
| EPWM24_G2     | 5009 80E2h       |
| EPWM24_G3     | 500D 80E2h       |
| EPWM25_G0     | 5001 90E2h       |
| EPWM25_G1     | 5005 90E2h       |
| EPWM25_G2     | 5009 90E2h       |
| EPWM25_G3     | 500D 90E2h       |
| EPWM26_G0     | 5001 A0E2h       |
| EPWM26_G1     | 5005 A0E2h       |
| EPWM26_G2     | 5009 A0E2h       |
| EPWM26_G3     | 500D A0E2h       |
| EPWM27_G0     | 5001 B0E2h       |
| EPWM27_G1     | 5005 B0E2h       |
| EPWM27_G2     | 5009 B0E2h       |
| EPWM27_G3     | 500D B0E2h       |
| EPWM28_G0     | 5001 C0E2h       |
| EPWM28_G1     | 5005 C0E2h       |
| EPWM28_G2     | 5009 C0E2h       |
| EPWM28_G3     | 500D C0E2h       |
| EPWM29_G0     | 5001 D0E2h       |
| EPWM29_G1     | 5005 D0E2h       |
| EPWM29_G2     | 5009 D0E2h       |
| EPWM29_G3     | 500D D0E2h       |
| EPWM30_G0     | 5001 E0E2h       |
| EPWM30_G1     | 5005 E0E2h       |
| EPWM30_G2     | 5009 E0E2h       |
| EPWM30_G3     | 500D E0E2h       |
| EPWM31_G0     | 5001 F0E2h       |
| EPWM31_G1     | 5005 F0E2h       |
| EPWM31_G2     | 5009 F0E2h       |

**Table 3-946. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM31_G3     | 500D F0E2h       |

**Figure 3-296. EPWM\_CMPD Name Register**

|      |    |    |    |    |    |   |   |
|------|----|----|----|----|----|---|---|
| 15   | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMPD |    |    |    |    |    |   |   |
| R/W  |    |    |    |    |    |   |   |
| 0h   |    |    |    |    |    |   |   |
| 7    | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| CMPD |    |    |    |    |    |   |   |
| R/W  |    |    |    |    |    |   |   |
| 0h   |    |    |    |    |    |   |   |

**Table 3-948. EPWM\_CMPD Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | CMPD  | R/W  | 0h    | <p>Compare D Register</p> <p>The value in the active CMPD register is continuously compared to the time-base counter [TBCTR]. When the values are equal, the counter-compare module generates a "time-base counter equal to counter compare D" event.</p> <p>Shadowing of this register is enabled and disabled by the CMPCTL2[SHDWDMODE] bit. By default this register is shadowed.</p> <ul style="list-style-type: none"> <li>- If CMPCTL2[SHDWDMODE] = 0, then the shadow is enabled and any write or read will automatically go to the shadow register. In this case, the CMPCTL2[LOADDMODE] bit field determines which event will load the active register from the shadow register:</li> <li>- If CMPCTL2[SHDWDMODE] = 1, then the shadow register is disabled and any write or read will go directly to the active register that is, the register actively controlling the hardware.</li> <li>- In either mode, the active and shadow registers share the same memory map address.</li> </ul> |

### 3.7.2.46 EPWM\_GLDCTL2 Register

#### 1 EPWM\_GLDCTL2 Register (Offset = E8h) [reset = 0h]

Global PWM Load Control Register 2

Return to [Summary Table](#)

**Table 3-949. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 00E8h       |
| EPWM0_G1      | 5004 00E8h       |
| EPWM0_G2      | 5008 00E8h       |
| EPWM0_G3      | 500C 00E8h       |
| EPWM1_G0      | 5000 10E8h       |
| EPWM1_G1      | 5004 10E8h       |
| EPWM1_G2      | 5008 10E8h       |
| EPWM1_G3      | 500C 10E8h       |
| EPWM2_G0      | 5000 20E8h       |
| EPWM2_G1      | 5004 20E8h       |
| EPWM2_G2      | 5008 20E8h       |
| EPWM2_G3      | 500C 20E8h       |
| EPWM3_G0      | 5000 30E8h       |
| EPWM3_G1      | 5004 30E8h       |
| EPWM3_G2      | 5008 30E8h       |
| EPWM3_G3      | 500C 30E8h       |
| EPWM4_G0      | 5000 40E8h       |
| EPWM4_G1      | 5004 40E8h       |
| EPWM4_G2      | 5008 40E8h       |
| EPWM4_G3      | 500C 40E8h       |
| EPWM5_G0      | 5000 50E8h       |
| EPWM5_G1      | 5004 50E8h       |
| EPWM5_G2      | 5008 50E8h       |
| EPWM5_G3      | 500C 50E8h       |
| EPWM6_G0      | 5000 60E8h       |
| EPWM6_G1      | 5004 60E8h       |
| EPWM6_G2      | 5008 60E8h       |
| EPWM6_G3      | 500C 60E8h       |
| EPWM7_G0      | 5000 70E8h       |
| EPWM7_G1      | 5004 70E8h       |
| EPWM7_G2      | 5008 70E8h       |
| EPWM7_G3      | 500C 70E8h       |
| EPWM8_G0      | 5000 80E8h       |
| EPWM8_G1      | 5004 80E8h       |
| EPWM8_G2      | 5008 80E8h       |
| EPWM8_G3      | 500C 80E8h       |
| EPWM9_G0      | 5000 90E8h       |
| EPWM9_G1      | 5004 90E8h       |
| EPWM9_G2      | 5008 90E8h       |

**Table 3-949. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 90E8h       |
| EPWM10_G0     | 5000 A0E8h       |
| EPWM10_G1     | 5004 A0E8h       |
| EPWM10_G2     | 5008 A0E8h       |
| EPWM10_G3     | 500C A0E8h       |
| EPWM11_G0     | 5000 B0E8h       |
| EPWM11_G1     | 5004 B0E8h       |
| EPWM11_G2     | 5008 B0E8h       |
| EPWM11_G3     | 500C B0E8h       |
| EPWM12_G0     | 5000 C0E8h       |
| EPWM12_G1     | 5004 C0E8h       |
| EPWM12_G2     | 5008 C0E8h       |
| EPWM12_G3     | 500C C0E8h       |
| EPWM13_G0     | 5000 D0E8h       |
| EPWM13_G1     | 5004 D0E8h       |
| EPWM13_G2     | 5008 D0E8h       |
| EPWM13_G3     | 500C D0E8h       |
| EPWM14_G0     | 5000 E0E8h       |
| EPWM14_G1     | 5004 E0E8h       |
| EPWM14_G2     | 5008 E0E8h       |
| EPWM14_G3     | 500C E0E8h       |
| EPWM15_G0     | 5000 F0E8h       |
| EPWM15_G1     | 5004 F0E8h       |
| EPWM15_G2     | 5008 F0E8h       |
| EPWM15_G3     | 500C F0E8h       |
| EPWM16_G0     | 5001 00E8h       |
| EPWM16_G1     | 5005 00E8h       |
| EPWM16_G2     | 5009 00E8h       |
| EPWM16_G3     | 500D 00E8h       |
| EPWM17_G0     | 5001 10E8h       |
| EPWM17_G1     | 5005 10E8h       |
| EPWM17_G2     | 5009 10E8h       |
| EPWM17_G3     | 500D 10E8h       |
| EPWM18_G0     | 5001 20E8h       |
| EPWM18_G1     | 5005 20E8h       |
| EPWM18_G2     | 5009 20E8h       |
| EPWM18_G3     | 500D 20E8h       |
| EPWM19_G0     | 5001 30E8h       |
| EPWM19_G1     | 5005 30E8h       |
| EPWM19_G2     | 5009 30E8h       |
| EPWM19_G3     | 500D 30E8h       |
| EPWM20_G0     | 5001 40E8h       |
| EPWM20_G1     | 5005 40E8h       |
| EPWM20_G2     | 5009 40E8h       |
| EPWM20_G3     | 500D 40E8h       |

**Table 3-949. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 50E8h       |
| EPWM21_G1     | 5005 50E8h       |
| EPWM21_G2     | 5009 50E8h       |
| EPWM21_G3     | 500D 50E8h       |
| EPWM22_G0     | 5001 60E8h       |
| EPWM22_G1     | 5005 60E8h       |
| EPWM22_G2     | 5009 60E8h       |
| EPWM22_G3     | 500D 60E8h       |
| EPWM23_G0     | 5001 70E8h       |
| EPWM23_G1     | 5005 70E8h       |
| EPWM23_G2     | 5009 70E8h       |
| EPWM23_G3     | 500D 70E8h       |
| EPWM24_G0     | 5001 80E8h       |
| EPWM24_G1     | 5005 80E8h       |
| EPWM24_G2     | 5009 80E8h       |
| EPWM24_G3     | 500D 80E8h       |
| EPWM25_G0     | 5001 90E8h       |
| EPWM25_G1     | 5005 90E8h       |
| EPWM25_G2     | 5009 90E8h       |
| EPWM25_G3     | 500D 90E8h       |
| EPWM26_G0     | 5001 A0E8h       |
| EPWM26_G1     | 5005 A0E8h       |
| EPWM26_G2     | 5009 A0E8h       |
| EPWM26_G3     | 500D A0E8h       |
| EPWM27_G0     | 5001 B0E8h       |
| EPWM27_G1     | 5005 B0E8h       |
| EPWM27_G2     | 5009 B0E8h       |
| EPWM27_G3     | 500D B0E8h       |
| EPWM28_G0     | 5001 C0E8h       |
| EPWM28_G1     | 5005 C0E8h       |
| EPWM28_G2     | 5009 C0E8h       |
| EPWM28_G3     | 500D C0E8h       |
| EPWM29_G0     | 5001 D0E8h       |
| EPWM29_G1     | 5005 D0E8h       |
| EPWM29_G2     | 5009 D0E8h       |
| EPWM29_G3     | 500D D0E8h       |
| EPWM30_G0     | 5001 E0E8h       |
| EPWM30_G1     | 5005 E0E8h       |
| EPWM30_G2     | 5009 E0E8h       |
| EPWM30_G3     | 500D E0E8h       |
| EPWM31_G0     | 5001 F0E8h       |
| EPWM31_G1     | 5005 F0E8h       |
| EPWM31_G2     | 5009 F0E8h       |
| EPWM31_G3     | 500D F0E8h       |

**Figure 3-297. EPWM\_GLDCTL2 Name Register**

|            |    |    |    |    |    |        |        |
|------------|----|----|----|----|----|--------|--------|
| 15         | 14 | 13 | 12 | 11 | 10 | 9      | 8      |
| RESERVED_1 |    |    |    |    |    |        |        |
| R          |    |    |    |    |    |        |        |
| 0h         |    |    |    |    |    |        |        |
| 7          | 6  | 5  | 4  | 3  | 2  | 1      | 0      |
| RESERVED_1 |    |    |    |    |    | GFRCLD | OSHTLD |
| R          |    |    |    |    |    | R/W1TS | R/W1TS |
| 0h         |    |    |    |    |    | 0h     | 0h     |

**Table 3-951. EPWM\_GLDCTL2 Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                          |
|------|------------|--------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:2 | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                             |
| 1    | GFRCLD     | R/W1TS | 0h    | Force Load Event in One Shot Mode<br>0:Writing of 0 will be ignored. Always reads back a 0.<br>1:Force one load event at the input of the event pre-scale counter as shown in the diagram below. This bit is intended to be used for testing and/or software force loading of the events in global load mode.                                                        |
| 0    | OSHTLD     | R/W1TS | 0h    | Enable Reload Event in One Shot Mode<br>0:Writing of 0 will be ignored. Always reads back a 0.<br>1:Turns the one shot latch condition ON. Upon occurrence of a chosen load strobe, one shadow to active reload occurs and the latch will be cleared. Hence Writing 1 to this bit would allow one load strobe event to pass through and block further strobe events. |

### 3.7.2.47 EPWM\_SWVDELVAL Register

#### 1 EPWM\_SWVDELVAL Register (Offset = EEh) [reset = 0h]

Software Valley Mode Delay Register.

Return to [Summary Table](#)

**Table 3-952. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 00EEh       |
| EPWM0_G1      | 5004 00EEh       |
| EPWM0_G2      | 5008 00EEh       |
| EPWM0_G3      | 500C 00EEh       |
| EPWM1_G0      | 5000 10EEh       |
| EPWM1_G1      | 5004 10EEh       |
| EPWM1_G2      | 5008 10EEh       |
| EPWM1_G3      | 500C 10EEh       |
| EPWM2_G0      | 5000 20EEh       |
| EPWM2_G1      | 5004 20EEh       |
| EPWM2_G2      | 5008 20EEh       |
| EPWM2_G3      | 500C 20EEh       |
| EPWM3_G0      | 5000 30EEh       |
| EPWM3_G1      | 5004 30EEh       |
| EPWM3_G2      | 5008 30EEh       |
| EPWM3_G3      | 500C 30EEh       |
| EPWM4_G0      | 5000 40EEh       |
| EPWM4_G1      | 5004 40EEh       |
| EPWM4_G2      | 5008 40EEh       |
| EPWM4_G3      | 500C 40EEh       |
| EPWM5_G0      | 5000 50EEh       |
| EPWM5_G1      | 5004 50EEh       |
| EPWM5_G2      | 5008 50EEh       |
| EPWM5_G3      | 500C 50EEh       |
| EPWM6_G0      | 5000 60EEh       |
| EPWM6_G1      | 5004 60EEh       |
| EPWM6_G2      | 5008 60EEh       |
| EPWM6_G3      | 500C 60EEh       |
| EPWM7_G0      | 5000 70EEh       |
| EPWM7_G1      | 5004 70EEh       |
| EPWM7_G2      | 5008 70EEh       |
| EPWM7_G3      | 500C 70EEh       |
| EPWM8_G0      | 5000 80EEh       |
| EPWM8_G1      | 5004 80EEh       |
| EPWM8_G2      | 5008 80EEh       |
| EPWM8_G3      | 500C 80EEh       |
| EPWM9_G0      | 5000 90EEh       |
| EPWM9_G1      | 5004 90EEh       |
| EPWM9_G2      | 5008 90EEh       |

**Table 3-952. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 90EEh       |
| EPWM10_G0     | 5000 A0EEh       |
| EPWM10_G1     | 5004 A0EEh       |
| EPWM10_G2     | 5008 A0EEh       |
| EPWM10_G3     | 500C A0EEh       |
| EPWM11_G0     | 5000 B0EEh       |
| EPWM11_G1     | 5004 B0EEh       |
| EPWM11_G2     | 5008 B0EEh       |
| EPWM11_G3     | 500C B0EEh       |
| EPWM12_G0     | 5000 C0EEh       |
| EPWM12_G1     | 5004 C0EEh       |
| EPWM12_G2     | 5008 C0EEh       |
| EPWM12_G3     | 500C C0EEh       |
| EPWM13_G0     | 5000 D0EEh       |
| EPWM13_G1     | 5004 D0EEh       |
| EPWM13_G2     | 5008 D0EEh       |
| EPWM13_G3     | 500C D0EEh       |
| EPWM14_G0     | 5000 E0EEh       |
| EPWM14_G1     | 5004 E0EEh       |
| EPWM14_G2     | 5008 E0EEh       |
| EPWM14_G3     | 500C E0EEh       |
| EPWM15_G0     | 5000 F0EEh       |
| EPWM15_G1     | 5004 F0EEh       |
| EPWM15_G2     | 5008 F0EEh       |
| EPWM15_G3     | 500C F0EEh       |
| EPWM16_G0     | 5001 00EEh       |
| EPWM16_G1     | 5005 00EEh       |
| EPWM16_G2     | 5009 00EEh       |
| EPWM16_G3     | 500D 00EEh       |
| EPWM17_G0     | 5001 10EEh       |
| EPWM17_G1     | 5005 10EEh       |
| EPWM17_G2     | 5009 10EEh       |
| EPWM17_G3     | 500D 10EEh       |
| EPWM18_G0     | 5001 20EEh       |
| EPWM18_G1     | 5005 20EEh       |
| EPWM18_G2     | 5009 20EEh       |
| EPWM18_G3     | 500D 20EEh       |
| EPWM19_G0     | 5001 30EEh       |
| EPWM19_G1     | 5005 30EEh       |
| EPWM19_G2     | 5009 30EEh       |
| EPWM19_G3     | 500D 30EEh       |
| EPWM20_G0     | 5001 40EEh       |
| EPWM20_G1     | 5005 40EEh       |
| EPWM20_G2     | 5009 40EEh       |
| EPWM20_G3     | 500D 40EEh       |



**Table 3-952. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 50EEh       |
| EPWM21_G1     | 5005 50EEh       |
| EPWM21_G2     | 5009 50EEh       |
| EPWM21_G3     | 500D 50EEh       |
| EPWM22_G0     | 5001 60EEh       |
| EPWM22_G1     | 5005 60EEh       |
| EPWM22_G2     | 5009 60EEh       |
| EPWM22_G3     | 500D 60EEh       |
| EPWM23_G0     | 5001 70EEh       |
| EPWM23_G1     | 5005 70EEh       |
| EPWM23_G2     | 5009 70EEh       |
| EPWM23_G3     | 500D 70EEh       |
| EPWM24_G0     | 5001 80EEh       |
| EPWM24_G1     | 5005 80EEh       |
| EPWM24_G2     | 5009 80EEh       |
| EPWM24_G3     | 500D 80EEh       |
| EPWM25_G0     | 5001 90EEh       |
| EPWM25_G1     | 5005 90EEh       |
| EPWM25_G2     | 5009 90EEh       |
| EPWM25_G3     | 500D 90EEh       |
| EPWM26_G0     | 5001 A0EEh       |
| EPWM26_G1     | 5005 A0EEh       |
| EPWM26_G2     | 5009 A0EEh       |
| EPWM26_G3     | 500D A0EEh       |
| EPWM27_G0     | 5001 B0EEh       |
| EPWM27_G1     | 5005 B0EEh       |
| EPWM27_G2     | 5009 B0EEh       |
| EPWM27_G3     | 500D B0EEh       |
| EPWM28_G0     | 5001 C0EEh       |
| EPWM28_G1     | 5005 C0EEh       |
| EPWM28_G2     | 5009 C0EEh       |
| EPWM28_G3     | 500D C0EEh       |
| EPWM29_G0     | 5001 D0EEh       |
| EPWM29_G1     | 5005 D0EEh       |
| EPWM29_G2     | 5009 D0EEh       |
| EPWM29_G3     | 500D D0EEh       |
| EPWM30_G0     | 5001 E0EEh       |
| EPWM30_G1     | 5005 E0EEh       |
| EPWM30_G2     | 5009 E0EEh       |
| EPWM30_G3     | 500D E0EEh       |
| EPWM31_G0     | 5001 F0EEh       |
| EPWM31_G1     | 5005 F0EEh       |
| EPWM31_G2     | 5009 F0EEh       |
| EPWM31_G3     | 500D F0EEh       |

**Figure 3-298. EPWM\_SWVDELVAL Name Register**

|           |    |    |    |    |    |   |   |
|-----------|----|----|----|----|----|---|---|
| 15        | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| SWVDELVAL |    |    |    |    |    |   |   |
| R/W       |    |    |    |    |    |   |   |
| 0h        |    |    |    |    |    |   |   |
| 7         | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| SWVDELVAL |    |    |    |    |    |   |   |
| R/W       |    |    |    |    |    |   |   |
| 0h        |    |    |    |    |    |   |   |

**Table 3-954. EPWM\_SWVDELVAL Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                          |
|------|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | SWVDELVAL | R/W  | 0h    | Software Valley Delay Value Register<br>This register can be optionally used define offset value for the hardware calculated delay HWDELAYVAL as defined in VCAPCTL[VDELAYDIV] bits. |

### 3.7.2.48 EPWM\_TZSEL Register

#### 1 EPWM\_TZSEL Register (Offset = 100h) [reset = 0h]

Trip Zone Select Register .

Return to [Summary Table](#)

**Table 3-955. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0100h       |
| EPWM0_G1      | 5004 0100h       |
| EPWM0_G2      | 5008 0100h       |
| EPWM0_G3      | 500C 0100h       |
| EPWM1_G0      | 5000 1100h       |
| EPWM1_G1      | 5004 1100h       |
| EPWM1_G2      | 5008 1100h       |
| EPWM1_G3      | 500C 1100h       |
| EPWM2_G0      | 5000 2100h       |
| EPWM2_G1      | 5004 2100h       |
| EPWM2_G2      | 5008 2100h       |
| EPWM2_G3      | 500C 2100h       |
| EPWM3_G0      | 5000 3100h       |
| EPWM3_G1      | 5004 3100h       |
| EPWM3_G2      | 5008 3100h       |
| EPWM3_G3      | 500C 3100h       |
| EPWM4_G0      | 5000 4100h       |
| EPWM4_G1      | 5004 4100h       |
| EPWM4_G2      | 5008 4100h       |
| EPWM4_G3      | 500C 4100h       |
| EPWM5_G0      | 5000 5100h       |
| EPWM5_G1      | 5004 5100h       |
| EPWM5_G2      | 5008 5100h       |
| EPWM5_G3      | 500C 5100h       |
| EPWM6_G0      | 5000 6100h       |
| EPWM6_G1      | 5004 6100h       |
| EPWM6_G2      | 5008 6100h       |
| EPWM6_G3      | 500C 6100h       |
| EPWM7_G0      | 5000 7100h       |
| EPWM7_G1      | 5004 7100h       |
| EPWM7_G2      | 5008 7100h       |
| EPWM7_G3      | 500C 7100h       |
| EPWM8_G0      | 5000 8100h       |
| EPWM8_G1      | 5004 8100h       |
| EPWM8_G2      | 5008 8100h       |
| EPWM8_G3      | 500C 8100h       |
| EPWM9_G0      | 5000 9100h       |
| EPWM9_G1      | 5004 9100h       |
| EPWM9_G2      | 5008 9100h       |

**Table 3-955. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9100h       |
| EPWM10_G0     | 5000 A100h       |
| EPWM10_G1     | 5004 A100h       |
| EPWM10_G2     | 5008 A100h       |
| EPWM10_G3     | 500C A100h       |
| EPWM11_G0     | 5000 B100h       |
| EPWM11_G1     | 5004 B100h       |
| EPWM11_G2     | 5008 B100h       |
| EPWM11_G3     | 500C B100h       |
| EPWM12_G0     | 5000 C100h       |
| EPWM12_G1     | 5004 C100h       |
| EPWM12_G2     | 5008 C100h       |
| EPWM12_G3     | 500C C100h       |
| EPWM13_G0     | 5000 D100h       |
| EPWM13_G1     | 5004 D100h       |
| EPWM13_G2     | 5008 D100h       |
| EPWM13_G3     | 500C D100h       |
| EPWM14_G0     | 5000 E100h       |
| EPWM14_G1     | 5004 E100h       |
| EPWM14_G2     | 5008 E100h       |
| EPWM14_G3     | 500C E100h       |
| EPWM15_G0     | 5000 F100h       |
| EPWM15_G1     | 5004 F100h       |
| EPWM15_G2     | 5008 F100h       |
| EPWM15_G3     | 500C F100h       |
| EPWM16_G0     | 5001 0100h       |
| EPWM16_G1     | 5005 0100h       |
| EPWM16_G2     | 5009 0100h       |
| EPWM16_G3     | 500D 0100h       |
| EPWM17_G0     | 5001 1100h       |
| EPWM17_G1     | 5005 1100h       |
| EPWM17_G2     | 5009 1100h       |
| EPWM17_G3     | 500D 1100h       |
| EPWM18_G0     | 5001 2100h       |
| EPWM18_G1     | 5005 2100h       |
| EPWM18_G2     | 5009 2100h       |
| EPWM18_G3     | 500D 2100h       |
| EPWM19_G0     | 5001 3100h       |
| EPWM19_G1     | 5005 3100h       |
| EPWM19_G2     | 5009 3100h       |
| EPWM19_G3     | 500D 3100h       |
| EPWM20_G0     | 5001 4100h       |
| EPWM20_G1     | 5005 4100h       |
| EPWM20_G2     | 5009 4100h       |
| EPWM20_G3     | 500D 4100h       |

**Table 3-955. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5100h       |
| EPWM21_G1     | 5005 5100h       |
| EPWM21_G2     | 5009 5100h       |
| EPWM21_G3     | 500D 5100h       |
| EPWM22_G0     | 5001 6100h       |
| EPWM22_G1     | 5005 6100h       |
| EPWM22_G2     | 5009 6100h       |
| EPWM22_G3     | 500D 6100h       |
| EPWM23_G0     | 5001 7100h       |
| EPWM23_G1     | 5005 7100h       |
| EPWM23_G2     | 5009 7100h       |
| EPWM23_G3     | 500D 7100h       |
| EPWM24_G0     | 5001 8100h       |
| EPWM24_G1     | 5005 8100h       |
| EPWM24_G2     | 5009 8100h       |
| EPWM24_G3     | 500D 8100h       |
| EPWM25_G0     | 5001 9100h       |
| EPWM25_G1     | 5005 9100h       |
| EPWM25_G2     | 5009 9100h       |
| EPWM25_G3     | 500D 9100h       |
| EPWM26_G0     | 5001 A100h       |
| EPWM26_G1     | 5005 A100h       |
| EPWM26_G2     | 5009 A100h       |
| EPWM26_G3     | 500D A100h       |
| EPWM27_G0     | 5001 B100h       |
| EPWM27_G1     | 5005 B100h       |
| EPWM27_G2     | 5009 B100h       |
| EPWM27_G3     | 500D B100h       |
| EPWM28_G0     | 5001 C100h       |
| EPWM28_G1     | 5005 C100h       |
| EPWM28_G2     | 5009 C100h       |
| EPWM28_G3     | 500D C100h       |
| EPWM29_G0     | 5001 D100h       |
| EPWM29_G1     | 5005 D100h       |
| EPWM29_G2     | 5009 D100h       |
| EPWM29_G3     | 500D D100h       |
| EPWM30_G0     | 5001 E100h       |
| EPWM30_G1     | 5005 E100h       |
| EPWM30_G2     | 5009 E100h       |
| EPWM30_G3     | 500D E100h       |
| EPWM31_G0     | 5001 F100h       |
| EPWM31_G1     | 5005 F100h       |
| EPWM31_G2     | 5009 F100h       |
| EPWM31_G3     | 500D F100h       |

**Figure 3-299. EPWM\_TZSEL Name Register**

| 15      | 14      | 13    | 12    | 11    | 10    | 9     | 8     |
|---------|---------|-------|-------|-------|-------|-------|-------|
| DCBEVT1 | DCAEVT1 | OSHT6 | OSHT5 | OSHT4 | OSHT3 | OSHT2 | OSHT1 |
| R/W     | R/W     | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   |
| 0h      | 0h      | 0h    | 0h    | 0h    | 0h    | 0h    | 0h    |
| 7       | 6       | 5     | 4     | 3     | 2     | 1     | 0     |
| DCBEVT2 | DCAEVT2 | CBC6  | CBC5  | CBC4  | CBC3  | CBC2  | CBC1  |
| R/W     | R/W     | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   |
| 0h      | 0h      | 0h    | 0h    | 0h    | 0h    | 0h    | 0h    |

**Table 3-957. EPWM\_TZSEL Register Field Descriptions**

| Bit | Field   | Type | Reset | Description                                                                                                                                                                  |
|-----|---------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | DCBEVT1 | R/W  | 0h    | Digital Compare Output B Event 1 Select<br>0:Disable DCBEVT1 as one-shot-trip source for this EPWM module.<br>1:Enable DCBEVT1 as one-shot-trip source for this EPWM module. |
| 14  | DCAEVT1 | R/W  | 0h    | Digital Compare Output A Event 1 Select<br>0:Disable DCAEVT1 as one-shot-trip source for this EPWM module.<br>1:Enable DCAEVT1 as one-shot-trip source for this EPWM module. |
| 13  | OSHT6   | R/W  | 0h    | Trip-Zone 6 [TZ6] Select<br>0:Disable TZ6 as a one-shot trip source for this EPWM module<br>1:Enable TZ6 as a one-shot trip source for this EPWM module                      |
| 12  | OSHT5   | R/W  | 0h    | Trip-Zone 5 [TZ5] Select<br>0:Disable TZ5 as a one-shot trip source for this EPWM module<br>1:Enable TZ5 as a one-shot trip source for this EPWM module                      |
| 11  | OSHT4   | R/W  | 0h    | Trip-Zone 4 [TZ4] Select<br>0:Disable TZ4 as a one-shot trip source for this EPWM module<br>1:Enable TZ4 as a one-shot trip source for this EPWM module                      |
| 10  | OSHT3   | R/W  | 0h    | Trip-Zone 3 [TZ3] Select<br>0:Disable TZ3 as a one-shot trip source for this EPWM module<br>1:Enable TZ3 as a one-shot trip source for this EPWM module                      |
| 9   | OSHT2   | R/W  | 0h    | Trip-Zone 2 [TZ2] Select<br>0:Disable TZ2 as a one-shot trip source for this EPWM module<br>1:Enable TZ2 as a one-shot trip source for this EPWM module                      |
| 8   | OSHT1   | R/W  | 0h    | Trip-Zone 1 [TZ1] Select<br>0:Disable TZ1 as a one-shot trip source for this EPWM module<br>1:Enable TZ1 as a one-shot trip source for this EPWM module                      |
| 7   | DCBEVT2 | R/W  | 0h    | Digital Compare Output B Event 2 Select<br>0:Disable DCBEVT2 as a CBC trip source for this EPWM module<br>1:Enable DCBEVT2 as a CBC trip source for this EPWM module         |
| 6   | DCAEVT2 | R/W  | 0h    | Digital Compare Output A Event 2 Select<br>0:Disable DCAEVT2 as a CBC trip source for this EPWM module<br>1:Enable DCAEVT2 as a CBC trip source for this EPWM module         |
| 5   | CBC6    | R/W  | 0h    | Trip-Zone 6 [TZ6] Select<br>0:Disable TZ6 as a CBC trip source for this EPWM module<br>1:Enable TZ6 as a CBC trip source for this EPWM module                                |
| 4   | CBC5    | R/W  | 0h    | Trip-Zone 5 [TZ5] Select<br>0:Disable TZ5 as a CBC trip source for this EPWM module<br>1:Enable TZ5 as a CBC trip source for this EPWM module                                |
| 3   | CBC4    | R/W  | 0h    | Trip-Zone 4 [TZ4] Select<br>0:Disable TZ4 as a CBC trip source for this EPWM module<br>1:Enable TZ4 as a CBC trip source for this EPWM module                                |
| 2   | CBC3    | R/W  | 0h    | Trip-Zone 3 [TZ3] Select<br>0:Disable TZ3 as a CBC trip source for this EPWM module<br>1:Enable TZ3 as a CBC trip source for this EPWM module                                |
| 1   | CBC2    | R/W  | 0h    | Trip-Zone 2 [TZ2] Select<br>0:Disable TZ2 as a CBC trip source for this EPWM module<br>1:Enable TZ2 as a CBC trip source for this EPWM module                                |

**Table 3-957. EPWM\_TZSEL Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                   |
|-----|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | CBC1  | R/W  | 0h    | Trip-Zone 1 [TZ1] Select<br>0:Disable TZ1 as a CBC trip source for this EPWM module<br>1:Enable TZ1 as a CBC trip source for this EPWM module |

### 3.7.2.49 EPWM\_TZSEL2 Register

#### 1 EPWM\_TZSEL2 Register (Offset = 102h) [reset = 0h]

Trip Zone Select Register 2

Return to [Summary Table](#)

**Table 3-958. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0102h       |
| EPWM0_G1      | 5004 0102h       |
| EPWM0_G2      | 5008 0102h       |
| EPWM0_G3      | 500C 0102h       |
| EPWM1_G0      | 5000 1102h       |
| EPWM1_G1      | 5004 1102h       |
| EPWM1_G2      | 5008 1102h       |
| EPWM1_G3      | 500C 1102h       |
| EPWM2_G0      | 5000 2102h       |
| EPWM2_G1      | 5004 2102h       |
| EPWM2_G2      | 5008 2102h       |
| EPWM2_G3      | 500C 2102h       |
| EPWM3_G0      | 5000 3102h       |
| EPWM3_G1      | 5004 3102h       |
| EPWM3_G2      | 5008 3102h       |
| EPWM3_G3      | 500C 3102h       |
| EPWM4_G0      | 5000 4102h       |
| EPWM4_G1      | 5004 4102h       |
| EPWM4_G2      | 5008 4102h       |
| EPWM4_G3      | 500C 4102h       |
| EPWM5_G0      | 5000 5102h       |
| EPWM5_G1      | 5004 5102h       |
| EPWM5_G2      | 5008 5102h       |
| EPWM5_G3      | 500C 5102h       |
| EPWM6_G0      | 5000 6102h       |
| EPWM6_G1      | 5004 6102h       |
| EPWM6_G2      | 5008 6102h       |
| EPWM6_G3      | 500C 6102h       |
| EPWM7_G0      | 5000 7102h       |
| EPWM7_G1      | 5004 7102h       |
| EPWM7_G2      | 5008 7102h       |
| EPWM7_G3      | 500C 7102h       |
| EPWM8_G0      | 5000 8102h       |
| EPWM8_G1      | 5004 8102h       |
| EPWM8_G2      | 5008 8102h       |
| EPWM8_G3      | 500C 8102h       |
| EPWM9_G0      | 5000 9102h       |
| EPWM9_G1      | 5004 9102h       |
| EPWM9_G2      | 5008 9102h       |



**Table 3-958. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9102h       |
| EPWM10_G0     | 5000 A102h       |
| EPWM10_G1     | 5004 A102h       |
| EPWM10_G2     | 5008 A102h       |
| EPWM10_G3     | 500C A102h       |
| EPWM11_G0     | 5000 B102h       |
| EPWM11_G1     | 5004 B102h       |
| EPWM11_G2     | 5008 B102h       |
| EPWM11_G3     | 500C B102h       |
| EPWM12_G0     | 5000 C102h       |
| EPWM12_G1     | 5004 C102h       |
| EPWM12_G2     | 5008 C102h       |
| EPWM12_G3     | 500C C102h       |
| EPWM13_G0     | 5000 D102h       |
| EPWM13_G1     | 5004 D102h       |
| EPWM13_G2     | 5008 D102h       |
| EPWM13_G3     | 500C D102h       |
| EPWM14_G0     | 5000 E102h       |
| EPWM14_G1     | 5004 E102h       |
| EPWM14_G2     | 5008 E102h       |
| EPWM14_G3     | 500C E102h       |
| EPWM15_G0     | 5000 F102h       |
| EPWM15_G1     | 5004 F102h       |
| EPWM15_G2     | 5008 F102h       |
| EPWM15_G3     | 500C F102h       |
| EPWM16_G0     | 5001 0102h       |
| EPWM16_G1     | 5005 0102h       |
| EPWM16_G2     | 5009 0102h       |
| EPWM16_G3     | 500D 0102h       |
| EPWM17_G0     | 5001 1102h       |
| EPWM17_G1     | 5005 1102h       |
| EPWM17_G2     | 5009 1102h       |
| EPWM17_G3     | 500D 1102h       |
| EPWM18_G0     | 5001 2102h       |
| EPWM18_G1     | 5005 2102h       |
| EPWM18_G2     | 5009 2102h       |
| EPWM18_G3     | 500D 2102h       |
| EPWM19_G0     | 5001 3102h       |
| EPWM19_G1     | 5005 3102h       |
| EPWM19_G2     | 5009 3102h       |
| EPWM19_G3     | 500D 3102h       |
| EPWM20_G0     | 5001 4102h       |
| EPWM20_G1     | 5005 4102h       |
| EPWM20_G2     | 5009 4102h       |
| EPWM20_G3     | 500D 4102h       |

**Table 3-958. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5102h       |
| EPWM21_G1     | 5005 5102h       |
| EPWM21_G2     | 5009 5102h       |
| EPWM21_G3     | 500D 5102h       |
| EPWM22_G0     | 5001 6102h       |
| EPWM22_G1     | 5005 6102h       |
| EPWM22_G2     | 5009 6102h       |
| EPWM22_G3     | 500D 6102h       |
| EPWM23_G0     | 5001 7102h       |
| EPWM23_G1     | 5005 7102h       |
| EPWM23_G2     | 5009 7102h       |
| EPWM23_G3     | 500D 7102h       |
| EPWM24_G0     | 5001 8102h       |
| EPWM24_G1     | 5005 8102h       |
| EPWM24_G2     | 5009 8102h       |
| EPWM24_G3     | 500D 8102h       |
| EPWM25_G0     | 5001 9102h       |
| EPWM25_G1     | 5005 9102h       |
| EPWM25_G2     | 5009 9102h       |
| EPWM25_G3     | 500D 9102h       |
| EPWM26_G0     | 5001 A102h       |
| EPWM26_G1     | 5005 A102h       |
| EPWM26_G2     | 5009 A102h       |
| EPWM26_G3     | 500D A102h       |
| EPWM27_G0     | 5001 B102h       |
| EPWM27_G1     | 5005 B102h       |
| EPWM27_G2     | 5009 B102h       |
| EPWM27_G3     | 500D B102h       |
| EPWM28_G0     | 5001 C102h       |
| EPWM28_G1     | 5005 C102h       |
| EPWM28_G2     | 5009 C102h       |
| EPWM28_G3     | 500D C102h       |
| EPWM29_G0     | 5001 D102h       |
| EPWM29_G1     | 5005 D102h       |
| EPWM29_G2     | 5009 D102h       |
| EPWM29_G3     | 500D D102h       |
| EPWM30_G0     | 5001 E102h       |
| EPWM30_G1     | 5005 E102h       |
| EPWM30_G2     | 5009 E102h       |
| EPWM30_G3     | 500D E102h       |
| EPWM31_G0     | 5001 F102h       |
| EPWM31_G1     | 5005 F102h       |
| EPWM31_G2     | 5009 F102h       |
| EPWM31_G3     | 500D F102h       |

**Figure 3-300. EPWM\_TZSEL2 Name Register**

|            |    |    |    |    |    |   |           |
|------------|----|----|----|----|----|---|-----------|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8         |
| RESERVED_2 |    |    |    |    |    |   | CAPEVTOST |
| R          |    |    |    |    |    |   | R/W       |
| 0h         |    |    |    |    |    |   | 0h        |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0         |
| RESERVED_1 |    |    |    |    |    |   | CAPEVTCBC |
| R          |    |    |    |    |    |   | R/W       |
| 0h         |    |    |    |    |    |   | 0h        |

**Table 3-960. EPWM\_TZSEL2 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                            |
|------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:9 | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                               |
| 8    | CAPEVTOST  | R/W  | 0h    | CAPEVT OST Select<br>0:Disable CAPEVT as a one-shot trip source for this EPWM module<br>1:Enable CAPEVT as a one-shot trip source for this EPWM module |
| 7:1  | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                               |
| 0    | CAPEVTCBC  | R/W  | 0h    | CAPEVT CBC mode Select<br>0:Disable CAPEVT as a CBC trip source for this EPWM module<br>1:Enable CAPEVT as a CBC trip source for this EPWM module      |

### 3.7.2.50 EPWM\_TZDCSEL Register

#### 1 EPWM\_TZDCSEL Register (Offset = 104h) [reset = 0h]

Trip Zone Digital Comparator Select Register.

Return to [Summary Table](#)

**Table 3-961. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0104h       |
| EPWM0_G1      | 5004 0104h       |
| EPWM0_G2      | 5008 0104h       |
| EPWM0_G3      | 500C 0104h       |
| EPWM1_G0      | 5000 1104h       |
| EPWM1_G1      | 5004 1104h       |
| EPWM1_G2      | 5008 1104h       |
| EPWM1_G3      | 500C 1104h       |
| EPWM2_G0      | 5000 2104h       |
| EPWM2_G1      | 5004 2104h       |
| EPWM2_G2      | 5008 2104h       |
| EPWM2_G3      | 500C 2104h       |
| EPWM3_G0      | 5000 3104h       |
| EPWM3_G1      | 5004 3104h       |
| EPWM3_G2      | 5008 3104h       |
| EPWM3_G3      | 500C 3104h       |
| EPWM4_G0      | 5000 4104h       |
| EPWM4_G1      | 5004 4104h       |
| EPWM4_G2      | 5008 4104h       |
| EPWM4_G3      | 500C 4104h       |
| EPWM5_G0      | 5000 5104h       |
| EPWM5_G1      | 5004 5104h       |
| EPWM5_G2      | 5008 5104h       |
| EPWM5_G3      | 500C 5104h       |
| EPWM6_G0      | 5000 6104h       |
| EPWM6_G1      | 5004 6104h       |
| EPWM6_G2      | 5008 6104h       |
| EPWM6_G3      | 500C 6104h       |
| EPWM7_G0      | 5000 7104h       |
| EPWM7_G1      | 5004 7104h       |
| EPWM7_G2      | 5008 7104h       |
| EPWM7_G3      | 500C 7104h       |
| EPWM8_G0      | 5000 8104h       |
| EPWM8_G1      | 5004 8104h       |
| EPWM8_G2      | 5008 8104h       |
| EPWM8_G3      | 500C 8104h       |
| EPWM9_G0      | 5000 9104h       |
| EPWM9_G1      | 5004 9104h       |
| EPWM9_G2      | 5008 9104h       |

**Table 3-961. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9104h       |
| EPWM10_G0     | 5000 A104h       |
| EPWM10_G1     | 5004 A104h       |
| EPWM10_G2     | 5008 A104h       |
| EPWM10_G3     | 500C A104h       |
| EPWM11_G0     | 5000 B104h       |
| EPWM11_G1     | 5004 B104h       |
| EPWM11_G2     | 5008 B104h       |
| EPWM11_G3     | 500C B104h       |
| EPWM12_G0     | 5000 C104h       |
| EPWM12_G1     | 5004 C104h       |
| EPWM12_G2     | 5008 C104h       |
| EPWM12_G3     | 500C C104h       |
| EPWM13_G0     | 5000 D104h       |
| EPWM13_G1     | 5004 D104h       |
| EPWM13_G2     | 5008 D104h       |
| EPWM13_G3     | 500C D104h       |
| EPWM14_G0     | 5000 E104h       |
| EPWM14_G1     | 5004 E104h       |
| EPWM14_G2     | 5008 E104h       |
| EPWM14_G3     | 500C E104h       |
| EPWM15_G0     | 5000 F104h       |
| EPWM15_G1     | 5004 F104h       |
| EPWM15_G2     | 5008 F104h       |
| EPWM15_G3     | 500C F104h       |
| EPWM16_G0     | 5001 0104h       |
| EPWM16_G1     | 5005 0104h       |
| EPWM16_G2     | 5009 0104h       |
| EPWM16_G3     | 500D 0104h       |
| EPWM17_G0     | 5001 1104h       |
| EPWM17_G1     | 5005 1104h       |
| EPWM17_G2     | 5009 1104h       |
| EPWM17_G3     | 500D 1104h       |
| EPWM18_G0     | 5001 2104h       |
| EPWM18_G1     | 5005 2104h       |
| EPWM18_G2     | 5009 2104h       |
| EPWM18_G3     | 500D 2104h       |
| EPWM19_G0     | 5001 3104h       |
| EPWM19_G1     | 5005 3104h       |
| EPWM19_G2     | 5009 3104h       |
| EPWM19_G3     | 500D 3104h       |
| EPWM20_G0     | 5001 4104h       |
| EPWM20_G1     | 5005 4104h       |
| EPWM20_G2     | 5009 4104h       |
| EPWM20_G3     | 500D 4104h       |

**Table 3-961. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5104h       |
| EPWM21_G1     | 5005 5104h       |
| EPWM21_G2     | 5009 5104h       |
| EPWM21_G3     | 500D 5104h       |
| EPWM22_G0     | 5001 6104h       |
| EPWM22_G1     | 5005 6104h       |
| EPWM22_G2     | 5009 6104h       |
| EPWM22_G3     | 500D 6104h       |
| EPWM23_G0     | 5001 7104h       |
| EPWM23_G1     | 5005 7104h       |
| EPWM23_G2     | 5009 7104h       |
| EPWM23_G3     | 500D 7104h       |
| EPWM24_G0     | 5001 8104h       |
| EPWM24_G1     | 5005 8104h       |
| EPWM24_G2     | 5009 8104h       |
| EPWM24_G3     | 500D 8104h       |
| EPWM25_G0     | 5001 9104h       |
| EPWM25_G1     | 5005 9104h       |
| EPWM25_G2     | 5009 9104h       |
| EPWM25_G3     | 500D 9104h       |
| EPWM26_G0     | 5001 A104h       |
| EPWM26_G1     | 5005 A104h       |
| EPWM26_G2     | 5009 A104h       |
| EPWM26_G3     | 500D A104h       |
| EPWM27_G0     | 5001 B104h       |
| EPWM27_G1     | 5005 B104h       |
| EPWM27_G2     | 5009 B104h       |
| EPWM27_G3     | 500D B104h       |
| EPWM28_G0     | 5001 C104h       |
| EPWM28_G1     | 5005 C104h       |
| EPWM28_G2     | 5009 C104h       |
| EPWM28_G3     | 500D C104h       |
| EPWM29_G0     | 5001 D104h       |
| EPWM29_G1     | 5005 D104h       |
| EPWM29_G2     | 5009 D104h       |
| EPWM29_G3     | 500D D104h       |
| EPWM30_G0     | 5001 E104h       |
| EPWM30_G1     | 5005 E104h       |
| EPWM30_G2     | 5009 E104h       |
| EPWM30_G3     | 500D E104h       |
| EPWM31_G0     | 5001 F104h       |
| EPWM31_G1     | 5005 F104h       |
| EPWM31_G2     | 5009 F104h       |
| EPWM31_G3     | 500D F104h       |

**Figure 3-301. EPWM\_TZDCSEL Name Register**

| 15         | 14 | 13      | 12 | 11      | 10      | 9 | 8       |
|------------|----|---------|----|---------|---------|---|---------|
| RESERVED_1 |    |         |    | DCBEVT2 |         |   | DCBEVT1 |
| R          |    |         |    | R/W     |         |   | R/W     |
| 0h         |    |         |    | 0h      |         |   | 0h      |
| 7          | 6  | 5       | 4  | 3       | 2       | 1 | 0       |
| DCBEVT1    |    | DCAEVT2 |    |         | DCAEVT1 |   |         |
| R/W        |    | R/W     |    |         | R/W     |   |         |
| 0h         |    | 0h      |    |         | 0h      |   |         |

**Table 3-963. EPWM\_TZDCSEL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                           |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                              |
| 11:9  | DCBEVT2    | R/W  | 0h    | Digital Compare Output B Event 2 Selection<br>000:Event disabled<br>001:DCBH = low, DCBL = don't care<br>010:DCBH = high, DCBL = don't care<br>011:DCBL = low, DCBH = don't care<br>100:DCBL = high, DCBH = don't care<br>101:DCBL = high, DCBH = low<br>110:Reserved<br>111:Reserved |
| 8:6   | DCBEVT1    | R/W  | 0h    | Digital Compare Output B Event 1 Selection<br>000:Event disabled<br>001:DCBH = low, DCBL = don't care<br>010:DCBH = high, DCBL = don't care<br>011:DCBL = low, DCBH = don't care<br>100:DCBL = high, DCBH = don't care<br>101:DCBL = high, DCBH = low<br>110:Reserved<br>111:Reserved |
| 5:3   | DCAEVT2    | R/W  | 0h    | Digital Compare Output A Event 2 Selection<br>000:Event disabled<br>001:DCAH = low, DCAL = don't care<br>010:DCAH = high, DCAL = don't care<br>011:DCAL = low, DCAH = don't care<br>100:DCAL = high, DCAH = don't care<br>101:DCAL = high, DCAH = low<br>110:Reserved<br>111:Reserved |
| 2:0   | DCAEVT1    | R/W  | 0h    | Digital Compare Output A Event 1 Selection<br>000:Event disabled<br>001:DCAH = low, DCAL = don't care<br>010:DCAH = high, DCAL = don't care<br>011:DCAL = low, DCAH = don't care<br>100:DCAL = high, DCAH = don't care<br>101:DCAL = high, DCAH = low<br>110:Reserved<br>111:Reserved |

### 3.7.2.51 EPWM\_TZCTL Register

#### 1 EPWM\_TZCTL Register (Offset = 108h) [reset = 0h]

Trip Zone Control Register.

Return to [Summary Table](#)

**Table 3-964. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0108h       |
| EPWM0_G1      | 5004 0108h       |
| EPWM0_G2      | 5008 0108h       |
| EPWM0_G3      | 500C 0108h       |
| EPWM1_G0      | 5000 1108h       |
| EPWM1_G1      | 5004 1108h       |
| EPWM1_G2      | 5008 1108h       |
| EPWM1_G3      | 500C 1108h       |
| EPWM2_G0      | 5000 2108h       |
| EPWM2_G1      | 5004 2108h       |
| EPWM2_G2      | 5008 2108h       |
| EPWM2_G3      | 500C 2108h       |
| EPWM3_G0      | 5000 3108h       |
| EPWM3_G1      | 5004 3108h       |
| EPWM3_G2      | 5008 3108h       |
| EPWM3_G3      | 500C 3108h       |
| EPWM4_G0      | 5000 4108h       |
| EPWM4_G1      | 5004 4108h       |
| EPWM4_G2      | 5008 4108h       |
| EPWM4_G3      | 500C 4108h       |
| EPWM5_G0      | 5000 5108h       |
| EPWM5_G1      | 5004 5108h       |
| EPWM5_G2      | 5008 5108h       |
| EPWM5_G3      | 500C 5108h       |
| EPWM6_G0      | 5000 6108h       |
| EPWM6_G1      | 5004 6108h       |
| EPWM6_G2      | 5008 6108h       |
| EPWM6_G3      | 500C 6108h       |
| EPWM7_G0      | 5000 7108h       |
| EPWM7_G1      | 5004 7108h       |
| EPWM7_G2      | 5008 7108h       |
| EPWM7_G3      | 500C 7108h       |
| EPWM8_G0      | 5000 8108h       |
| EPWM8_G1      | 5004 8108h       |
| EPWM8_G2      | 5008 8108h       |
| EPWM8_G3      | 500C 8108h       |
| EPWM9_G0      | 5000 9108h       |
| EPWM9_G1      | 5004 9108h       |
| EPWM9_G2      | 5008 9108h       |



**Table 3-964. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9108h       |
| EPWM10_G0     | 5000 A108h       |
| EPWM10_G1     | 5004 A108h       |
| EPWM10_G2     | 5008 A108h       |
| EPWM10_G3     | 500C A108h       |
| EPWM11_G0     | 5000 B108h       |
| EPWM11_G1     | 5004 B108h       |
| EPWM11_G2     | 5008 B108h       |
| EPWM11_G3     | 500C B108h       |
| EPWM12_G0     | 5000 C108h       |
| EPWM12_G1     | 5004 C108h       |
| EPWM12_G2     | 5008 C108h       |
| EPWM12_G3     | 500C C108h       |
| EPWM13_G0     | 5000 D108h       |
| EPWM13_G1     | 5004 D108h       |
| EPWM13_G2     | 5008 D108h       |
| EPWM13_G3     | 500C D108h       |
| EPWM14_G0     | 5000 E108h       |
| EPWM14_G1     | 5004 E108h       |
| EPWM14_G2     | 5008 E108h       |
| EPWM14_G3     | 500C E108h       |
| EPWM15_G0     | 5000 F108h       |
| EPWM15_G1     | 5004 F108h       |
| EPWM15_G2     | 5008 F108h       |
| EPWM15_G3     | 500C F108h       |
| EPWM16_G0     | 5001 0108h       |
| EPWM16_G1     | 5005 0108h       |
| EPWM16_G2     | 5009 0108h       |
| EPWM16_G3     | 500D 0108h       |
| EPWM17_G0     | 5001 1108h       |
| EPWM17_G1     | 5005 1108h       |
| EPWM17_G2     | 5009 1108h       |
| EPWM17_G3     | 500D 1108h       |
| EPWM18_G0     | 5001 2108h       |
| EPWM18_G1     | 5005 2108h       |
| EPWM18_G2     | 5009 2108h       |
| EPWM18_G3     | 500D 2108h       |
| EPWM19_G0     | 5001 3108h       |
| EPWM19_G1     | 5005 3108h       |
| EPWM19_G2     | 5009 3108h       |
| EPWM19_G3     | 500D 3108h       |
| EPWM20_G0     | 5001 4108h       |
| EPWM20_G1     | 5005 4108h       |
| EPWM20_G2     | 5009 4108h       |
| EPWM20_G3     | 500D 4108h       |

**Table 3-964. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5108h       |
| EPWM21_G1     | 5005 5108h       |
| EPWM21_G2     | 5009 5108h       |
| EPWM21_G3     | 500D 5108h       |
| EPWM22_G0     | 5001 6108h       |
| EPWM22_G1     | 5005 6108h       |
| EPWM22_G2     | 5009 6108h       |
| EPWM22_G3     | 500D 6108h       |
| EPWM23_G0     | 5001 7108h       |
| EPWM23_G1     | 5005 7108h       |
| EPWM23_G2     | 5009 7108h       |
| EPWM23_G3     | 500D 7108h       |
| EPWM24_G0     | 5001 8108h       |
| EPWM24_G1     | 5005 8108h       |
| EPWM24_G2     | 5009 8108h       |
| EPWM24_G3     | 500D 8108h       |
| EPWM25_G0     | 5001 9108h       |
| EPWM25_G1     | 5005 9108h       |
| EPWM25_G2     | 5009 9108h       |
| EPWM25_G3     | 500D 9108h       |
| EPWM26_G0     | 5001 A108h       |
| EPWM26_G1     | 5005 A108h       |
| EPWM26_G2     | 5009 A108h       |
| EPWM26_G3     | 500D A108h       |
| EPWM27_G0     | 5001 B108h       |
| EPWM27_G1     | 5005 B108h       |
| EPWM27_G2     | 5009 B108h       |
| EPWM27_G3     | 500D B108h       |
| EPWM28_G0     | 5001 C108h       |
| EPWM28_G1     | 5005 C108h       |
| EPWM28_G2     | 5009 C108h       |
| EPWM28_G3     | 500D C108h       |
| EPWM29_G0     | 5001 D108h       |
| EPWM29_G1     | 5005 D108h       |
| EPWM29_G2     | 5009 D108h       |
| EPWM29_G3     | 500D D108h       |
| EPWM30_G0     | 5001 E108h       |
| EPWM30_G1     | 5005 E108h       |
| EPWM30_G2     | 5009 E108h       |
| EPWM30_G3     | 500D E108h       |
| EPWM31_G0     | 5001 F108h       |
| EPWM31_G1     | 5005 F108h       |
| EPWM31_G2     | 5009 F108h       |
| EPWM31_G3     | 500D F108h       |

**Figure 3-302. EPWM\_TZCTL Name Register**

| 15         | 14 | 13      | 12 | 11      | 10 | 9       | 8 |
|------------|----|---------|----|---------|----|---------|---|
| RESERVED_1 |    |         |    | DCBEVT2 |    | DCBEVT1 |   |
| R          |    |         |    | R/W     |    | R/W     |   |
| 0h         |    |         |    | 0h      |    | 0h      |   |
| 7          | 6  | 5       | 4  | 3       | 2  | 1       | 0 |
| DCAEVT2    |    | DCAEVT1 |    | TZB     |    | TZA     |   |
| R/W        |    | R/W     |    | R/W     |    | R/W     |   |
| 0h         |    | 0h      |    | 0h      |    | 0h      |   |

**Table 3-966. EPWM\_TZCTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                            |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                               |
| 11:10 | DCBEVT2    | R/W  | 0h    | Digital Compare Output B Event 2 Action On EPWMxB<br>00:High-impedance [EPWMxB = High-impedance state]<br>01:Force EPWMxB to a high state.<br>10:Force EPWMxB to a low state.<br>11:Do Nothing, trip action is disabled                                                                                                                                                                |
| 9:8   | DCBEVT1    | R/W  | 0h    | Digital Compare Output B Event 1 Action On EPWMxB<br>00:High-impedance [EPWMxB = High-impedance state]<br>01:Force EPWMxB to a high state.<br>10:Force EPWMxB to a low state.<br>11:Do Nothing, trip action is disabled                                                                                                                                                                |
| 7:6   | DCAEVT2    | R/W  | 0h    | Digital Compare Output A Event 2 Action On EPWMxA<br>00:High-impedance [EPWMxA = High-impedance state]<br>01:Force EPWMxA to a high state.<br>10:Force EPWMxA to a low state.<br>11:Do Nothing, trip action is disabled                                                                                                                                                                |
| 5:4   | DCAEVT1    | R/W  | 0h    | Digital Compare Output A Event 1 Action On EPWMxA<br>00:High-impedance [EPWMxA = High-impedance state]<br>01:Force EPWMxA to a high state.<br>10:Force EPWMxA to a low state.<br>11:Do Nothing, trip action is disabled                                                                                                                                                                |
| 3:2   | TZB        | R/W  | 0h    | TZ1 to TZ6, DCAEVT1/2, DCBEVT1/2 Trip Action On EPWMxB<br>When a trip event occurs the following action is taken on output EPWMxB. Which trip-zone pins can cause an event is defined in the TZSEL register.<br>00:High-impedance [EPWMxB = High-impedance state]<br>01:Force EPWMxB to a high state<br>10:Force EPWMxB to a low state<br>11:Do nothing, no action is taken on EPWMxB. |
| 1:0   | TZA        | R/W  | 0h    | TZ1 to TZ6, DCAEVT1/2, DCBEVT1/2 Trip Action On EPWMxA<br>When a trip event occurs the following action is taken on output EPWMxA. Which trip-zone pins can cause an event is defined in the TZSEL register.<br>00:High-impedance [EPWMxA = High-impedance state]<br>01:Force EPWMxA to a high state<br>10:Force EPWMxA to a low state<br>11:Do nothing, no action is taken on EPWMxA. |

### 3.7.2.52 EPWM\_TZCTL2 Register

#### 1 EPWM\_TZCTL2 Register (Offset = 10Ah) [reset = 0h]

Additional Trip Zone Control Register.

Return to [Summary Table](#)

**Table 3-967. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 010Ah       |
| EPWM0_G1      | 5004 010Ah       |
| EPWM0_G2      | 5008 010Ah       |
| EPWM0_G3      | 500C 010Ah       |
| EPWM1_G0      | 5000 110Ah       |
| EPWM1_G1      | 5004 110Ah       |
| EPWM1_G2      | 5008 110Ah       |
| EPWM1_G3      | 500C 110Ah       |
| EPWM2_G0      | 5000 210Ah       |
| EPWM2_G1      | 5004 210Ah       |
| EPWM2_G2      | 5008 210Ah       |
| EPWM2_G3      | 500C 210Ah       |
| EPWM3_G0      | 5000 310Ah       |
| EPWM3_G1      | 5004 310Ah       |
| EPWM3_G2      | 5008 310Ah       |
| EPWM3_G3      | 500C 310Ah       |
| EPWM4_G0      | 5000 410Ah       |
| EPWM4_G1      | 5004 410Ah       |
| EPWM4_G2      | 5008 410Ah       |
| EPWM4_G3      | 500C 410Ah       |
| EPWM5_G0      | 5000 510Ah       |
| EPWM5_G1      | 5004 510Ah       |
| EPWM5_G2      | 5008 510Ah       |
| EPWM5_G3      | 500C 510Ah       |
| EPWM6_G0      | 5000 610Ah       |
| EPWM6_G1      | 5004 610Ah       |
| EPWM6_G2      | 5008 610Ah       |
| EPWM6_G3      | 500C 610Ah       |
| EPWM7_G0      | 5000 710Ah       |
| EPWM7_G1      | 5004 710Ah       |
| EPWM7_G2      | 5008 710Ah       |
| EPWM7_G3      | 500C 710Ah       |
| EPWM8_G0      | 5000 810Ah       |
| EPWM8_G1      | 5004 810Ah       |
| EPWM8_G2      | 5008 810Ah       |
| EPWM8_G3      | 500C 810Ah       |
| EPWM9_G0      | 5000 910Ah       |
| EPWM9_G1      | 5004 910Ah       |
| EPWM9_G2      | 5008 910Ah       |

**Table 3-967. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 910Ah       |
| EPWM10_G0     | 5000 A10Ah       |
| EPWM10_G1     | 5004 A10Ah       |
| EPWM10_G2     | 5008 A10Ah       |
| EPWM10_G3     | 500C A10Ah       |
| EPWM11_G0     | 5000 B10Ah       |
| EPWM11_G1     | 5004 B10Ah       |
| EPWM11_G2     | 5008 B10Ah       |
| EPWM11_G3     | 500C B10Ah       |
| EPWM12_G0     | 5000 C10Ah       |
| EPWM12_G1     | 5004 C10Ah       |
| EPWM12_G2     | 5008 C10Ah       |
| EPWM12_G3     | 500C C10Ah       |
| EPWM13_G0     | 5000 D10Ah       |
| EPWM13_G1     | 5004 D10Ah       |
| EPWM13_G2     | 5008 D10Ah       |
| EPWM13_G3     | 500C D10Ah       |
| EPWM14_G0     | 5000 E10Ah       |
| EPWM14_G1     | 5004 E10Ah       |
| EPWM14_G2     | 5008 E10Ah       |
| EPWM14_G3     | 500C E10Ah       |
| EPWM15_G0     | 5000 F10Ah       |
| EPWM15_G1     | 5004 F10Ah       |
| EPWM15_G2     | 5008 F10Ah       |
| EPWM15_G3     | 500C F10Ah       |
| EPWM16_G0     | 5001 010Ah       |
| EPWM16_G1     | 5005 010Ah       |
| EPWM16_G2     | 5009 010Ah       |
| EPWM16_G3     | 500D 010Ah       |
| EPWM17_G0     | 5001 110Ah       |
| EPWM17_G1     | 5005 110Ah       |
| EPWM17_G2     | 5009 110Ah       |
| EPWM17_G3     | 500D 110Ah       |
| EPWM18_G0     | 5001 210Ah       |
| EPWM18_G1     | 5005 210Ah       |
| EPWM18_G2     | 5009 210Ah       |
| EPWM18_G3     | 500D 210Ah       |
| EPWM19_G0     | 5001 310Ah       |
| EPWM19_G1     | 5005 310Ah       |
| EPWM19_G2     | 5009 310Ah       |
| EPWM19_G3     | 500D 310Ah       |
| EPWM20_G0     | 5001 410Ah       |
| EPWM20_G1     | 5005 410Ah       |
| EPWM20_G2     | 5009 410Ah       |
| EPWM20_G3     | 500D 410Ah       |

**Table 3-967. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 510Ah       |
| EPWM21_G1     | 5005 510Ah       |
| EPWM21_G2     | 5009 510Ah       |
| EPWM21_G3     | 500D 510Ah       |
| EPWM22_G0     | 5001 610Ah       |
| EPWM22_G1     | 5005 610Ah       |
| EPWM22_G2     | 5009 610Ah       |
| EPWM22_G3     | 500D 610Ah       |
| EPWM23_G0     | 5001 710Ah       |
| EPWM23_G1     | 5005 710Ah       |
| EPWM23_G2     | 5009 710Ah       |
| EPWM23_G3     | 500D 710Ah       |
| EPWM24_G0     | 5001 810Ah       |
| EPWM24_G1     | 5005 810Ah       |
| EPWM24_G2     | 5009 810Ah       |
| EPWM24_G3     | 500D 810Ah       |
| EPWM25_G0     | 5001 910Ah       |
| EPWM25_G1     | 5005 910Ah       |
| EPWM25_G2     | 5009 910Ah       |
| EPWM25_G3     | 500D 910Ah       |
| EPWM26_G0     | 5001 A10Ah       |
| EPWM26_G1     | 5005 A10Ah       |
| EPWM26_G2     | 5009 A10Ah       |
| EPWM26_G3     | 500D A10Ah       |
| EPWM27_G0     | 5001 B10Ah       |
| EPWM27_G1     | 5005 B10Ah       |
| EPWM27_G2     | 5009 B10Ah       |
| EPWM27_G3     | 500D B10Ah       |
| EPWM28_G0     | 5001 C10Ah       |
| EPWM28_G1     | 5005 C10Ah       |
| EPWM28_G2     | 5009 C10Ah       |
| EPWM28_G3     | 500D C10Ah       |
| EPWM29_G0     | 5001 D10Ah       |
| EPWM29_G1     | 5005 D10Ah       |
| EPWM29_G2     | 5009 D10Ah       |
| EPWM29_G3     | 500D D10Ah       |
| EPWM30_G0     | 5001 E10Ah       |
| EPWM30_G1     | 5005 E10Ah       |
| EPWM30_G2     | 5009 E10Ah       |
| EPWM30_G3     | 500D E10Ah       |
| EPWM31_G0     | 5001 F10Ah       |
| EPWM31_G1     | 5005 F10Ah       |
| EPWM31_G2     | 5009 F10Ah       |
| EPWM31_G3     | 500D F10Ah       |

**Figure 3-303. EPWM\_TZCTL2 Name Register**

| 15   | 14         | 13   | 12 | 11 | 10   | 9 | 8    |
|------|------------|------|----|----|------|---|------|
| ETZE | RESERVED_1 |      |    |    | TZBD |   | TZBU |
| R/W  | R          |      |    |    | R/W  |   | R/W  |
| 0h   | 0h         |      |    |    | 0h   |   | 0h   |
| 7    | 6          | 5    | 4  | 3  | 2    | 1 | 0    |
| TZBU |            | TZAD |    |    | TZAU |   |      |
| R/W  |            | R/W  |    |    | R/W  |   |      |
| 0h   |            | 0h   |    |    | 0h   |   |      |

**Table 3-969. EPWM\_TZCTL2 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                          |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | ETZE       | R/W  | 0h    | TZCTL2 Enable<br>0:Use trip action from TZCTL [legacy EPWM compatibility]<br>1:Use trip action defined in TZCTL2, TZCTLDCA and TZCTLDCB.<br>Settings in TZCTL are ignored                                                                                                                                                            |
| 14:12 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                             |
| 11:9  | TZBD       | R/W  | 0h    | TZ1 to TZ6 Trip Action On EPWMxB while Count direction is DOWN<br>000:HiZ [EPWMxB = HiZ state]<br>001:Forced Hi [EPWMxB = High state]<br>010:Forced Lo [EPWMxB = Lo state]<br>011:Toggle [Low -> High, High -> Low]<br>100:Reserved<br>101:Reserved<br>110:Reserved<br>111:Do Nothing, trip action is disabled                       |
| 8:6   | TZBU       | R/W  | 0h    | TZ1 to TZ6, DCAEVT1/2, DCBEVT1/2 Trip Action On EPWMxB while Count direction is UP<br>000:HiZ [EPWMxB = HiZ state]<br>001:Forced Hi [EPWMxB = High state]<br>010:Forced Lo [EPWMxB = Lo state]<br>011:Toggle [Low -> High, High -> Low]<br>100:Reserved<br>101:Reserved<br>110:Reserved<br>111:Do Nothing, trip action is disabled   |
| 5:3   | TZAD       | R/W  | 0h    | TZ1 to TZ6, DCAEVT1/2, DCBEVT1/2 Trip Action On EPWMxA while Count direction is DOWN<br>000:HiZ [EPWMxA = HiZ state]<br>001:Forced Hi [EPWMxA = High state]<br>010:Forced Lo [EPWMxA = Lo state]<br>011:Toggle [Low -> High, High -> Low]<br>100:Reserved<br>101:Reserved<br>110:Reserved<br>111:Do Nothing, trip action is disabled |
| 2:0   | TZAU       | R/W  | 0h    | TZ1 to TZ6, DCAEVT1/2, DCBEVT1/2 Trip Action On EPWMxA while Count direction is UP<br>000:HiZ [EPWMxA = HiZ state]<br>001:Forced Hi [EPWMxA = High state]<br>010:Forced Lo [EPWMxA = Lo state]<br>011:Toggle [Low -> High, High -> Low]<br>100:Reserved<br>101:Reserved<br>110:Reserved<br>111:Do Nothing, trip action is disabled   |

### 3.7.2.53 EPWM\_TZCTLDCA Register

#### 1 EPWM\_TZCTLDCA Register (Offset = 10Ch) [reset = 0h]

Trip Zone Control Register Digital Compare A .

Return to [Summary Table](#)

**Table 3-970. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 010Ch       |
| EPWM0_G1      | 5004 010Ch       |
| EPWM0_G2      | 5008 010Ch       |
| EPWM0_G3      | 500C 010Ch       |
| EPWM1_G0      | 5000 110Ch       |
| EPWM1_G1      | 5004 110Ch       |
| EPWM1_G2      | 5008 110Ch       |
| EPWM1_G3      | 500C 110Ch       |
| EPWM2_G0      | 5000 210Ch       |
| EPWM2_G1      | 5004 210Ch       |
| EPWM2_G2      | 5008 210Ch       |
| EPWM2_G3      | 500C 210Ch       |
| EPWM3_G0      | 5000 310Ch       |
| EPWM3_G1      | 5004 310Ch       |
| EPWM3_G2      | 5008 310Ch       |
| EPWM3_G3      | 500C 310Ch       |
| EPWM4_G0      | 5000 410Ch       |
| EPWM4_G1      | 5004 410Ch       |
| EPWM4_G2      | 5008 410Ch       |
| EPWM4_G3      | 500C 410Ch       |
| EPWM5_G0      | 5000 510Ch       |
| EPWM5_G1      | 5004 510Ch       |
| EPWM5_G2      | 5008 510Ch       |
| EPWM5_G3      | 500C 510Ch       |
| EPWM6_G0      | 5000 610Ch       |
| EPWM6_G1      | 5004 610Ch       |
| EPWM6_G2      | 5008 610Ch       |
| EPWM6_G3      | 500C 610Ch       |
| EPWM7_G0      | 5000 710Ch       |
| EPWM7_G1      | 5004 710Ch       |
| EPWM7_G2      | 5008 710Ch       |
| EPWM7_G3      | 500C 710Ch       |
| EPWM8_G0      | 5000 810Ch       |
| EPWM8_G1      | 5004 810Ch       |
| EPWM8_G2      | 5008 810Ch       |
| EPWM8_G3      | 500C 810Ch       |
| EPWM9_G0      | 5000 910Ch       |
| EPWM9_G1      | 5004 910Ch       |
| EPWM9_G2      | 5008 910Ch       |



**Table 3-970. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 910Ch       |
| EPWM10_G0     | 5000 A10Ch       |
| EPWM10_G1     | 5004 A10Ch       |
| EPWM10_G2     | 5008 A10Ch       |
| EPWM10_G3     | 500C A10Ch       |
| EPWM11_G0     | 5000 B10Ch       |
| EPWM11_G1     | 5004 B10Ch       |
| EPWM11_G2     | 5008 B10Ch       |
| EPWM11_G3     | 500C B10Ch       |
| EPWM12_G0     | 5000 C10Ch       |
| EPWM12_G1     | 5004 C10Ch       |
| EPWM12_G2     | 5008 C10Ch       |
| EPWM12_G3     | 500C C10Ch       |
| EPWM13_G0     | 5000 D10Ch       |
| EPWM13_G1     | 5004 D10Ch       |
| EPWM13_G2     | 5008 D10Ch       |
| EPWM13_G3     | 500C D10Ch       |
| EPWM14_G0     | 5000 E10Ch       |
| EPWM14_G1     | 5004 E10Ch       |
| EPWM14_G2     | 5008 E10Ch       |
| EPWM14_G3     | 500C E10Ch       |
| EPWM15_G0     | 5000 F10Ch       |
| EPWM15_G1     | 5004 F10Ch       |
| EPWM15_G2     | 5008 F10Ch       |
| EPWM15_G3     | 500C F10Ch       |
| EPWM16_G0     | 5001 010Ch       |
| EPWM16_G1     | 5005 010Ch       |
| EPWM16_G2     | 5009 010Ch       |
| EPWM16_G3     | 500D 010Ch       |
| EPWM17_G0     | 5001 110Ch       |
| EPWM17_G1     | 5005 110Ch       |
| EPWM17_G2     | 5009 110Ch       |
| EPWM17_G3     | 500D 110Ch       |
| EPWM18_G0     | 5001 210Ch       |
| EPWM18_G1     | 5005 210Ch       |
| EPWM18_G2     | 5009 210Ch       |
| EPWM18_G3     | 500D 210Ch       |
| EPWM19_G0     | 5001 310Ch       |
| EPWM19_G1     | 5005 310Ch       |
| EPWM19_G2     | 5009 310Ch       |
| EPWM19_G3     | 500D 310Ch       |
| EPWM20_G0     | 5001 410Ch       |
| EPWM20_G1     | 5005 410Ch       |
| EPWM20_G2     | 5009 410Ch       |
| EPWM20_G3     | 500D 410Ch       |

**Table 3-970. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 510Ch       |
| EPWM21_G1     | 5005 510Ch       |
| EPWM21_G2     | 5009 510Ch       |
| EPWM21_G3     | 500D 510Ch       |
| EPWM22_G0     | 5001 610Ch       |
| EPWM22_G1     | 5005 610Ch       |
| EPWM22_G2     | 5009 610Ch       |
| EPWM22_G3     | 500D 610Ch       |
| EPWM23_G0     | 5001 710Ch       |
| EPWM23_G1     | 5005 710Ch       |
| EPWM23_G2     | 5009 710Ch       |
| EPWM23_G3     | 500D 710Ch       |
| EPWM24_G0     | 5001 810Ch       |
| EPWM24_G1     | 5005 810Ch       |
| EPWM24_G2     | 5009 810Ch       |
| EPWM24_G3     | 500D 810Ch       |
| EPWM25_G0     | 5001 910Ch       |
| EPWM25_G1     | 5005 910Ch       |
| EPWM25_G2     | 5009 910Ch       |
| EPWM25_G3     | 500D 910Ch       |
| EPWM26_G0     | 5001 A10Ch       |
| EPWM26_G1     | 5005 A10Ch       |
| EPWM26_G2     | 5009 A10Ch       |
| EPWM26_G3     | 500D A10Ch       |
| EPWM27_G0     | 5001 B10Ch       |
| EPWM27_G1     | 5005 B10Ch       |
| EPWM27_G2     | 5009 B10Ch       |
| EPWM27_G3     | 500D B10Ch       |
| EPWM28_G0     | 5001 C10Ch       |
| EPWM28_G1     | 5005 C10Ch       |
| EPWM28_G2     | 5009 C10Ch       |
| EPWM28_G3     | 500D C10Ch       |
| EPWM29_G0     | 5001 D10Ch       |
| EPWM29_G1     | 5005 D10Ch       |
| EPWM29_G2     | 5009 D10Ch       |
| EPWM29_G3     | 500D D10Ch       |
| EPWM30_G0     | 5001 E10Ch       |
| EPWM30_G1     | 5005 E10Ch       |
| EPWM30_G2     | 5009 E10Ch       |
| EPWM30_G3     | 500D E10Ch       |
| EPWM31_G0     | 5001 F10Ch       |
| EPWM31_G1     | 5005 F10Ch       |
| EPWM31_G2     | 5009 F10Ch       |
| EPWM31_G3     | 500D F10Ch       |

**Figure 3-304. EPWM\_TZCTLDCA Name Register**

| 15         | 14 | 13       | 12 | 11       | 10       | 9 | 8        |
|------------|----|----------|----|----------|----------|---|----------|
| RESERVED_1 |    |          |    | DCAEVT2D |          |   | DCAEVT2U |
| R          |    |          |    | R/W      |          |   | R/W      |
| 0h         |    |          |    | 0h       |          |   | 0h       |
| 7          | 6  | 5        | 4  | 3        | 2        | 1 | 0        |
| DCAEVT2U   |    | DCAEVT1D |    |          | DCAEVT1U |   |          |
| R/W        |    | R/W      |    |          | R/W      |   |          |
| 0h         |    | 0h       |    |          | 0h       |   |          |

**Table 3-972. EPWM\_TZCTLDCA Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                     |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                        |
| 11:9  | DCAEVT2D   | R/W  | 0h    | Digital Compare Output A Event 2 Action On EPWMxA while Count direction is DOWN<br>000:HiZ [EPWMxA = HiZ state]<br>001:Forced Hi [EPWMxA = High state]<br>010:Forced Lo [EPWMxA = Lo state]<br>011:Toggle [Low -> High, High -> Low]<br>100:Reserved<br>101:Reserved<br>110:Reserved<br>111:Do Nothing, trip action is disabled |
| 8:6   | DCAEVT2U   | R/W  | 0h    | Digital Compare Output A Event 2 Action On EPWMxA while Count direction is UP<br>000:HiZ [EPWMxA = HiZ state]<br>001:Forced Hi [EPWMxA = High state]<br>010:Forced Lo [EPWMxA = Lo state]<br>011:Toggle [Low -> High, High -> Low]<br>100:Reserved<br>101:Reserved<br>110:Reserved<br>111:Do Nothing, trip action is disabled   |
| 5:3   | DCAEVT1D   | R/W  | 0h    | Digital Compare Output A Event 1 Action On EPWMxA while Count direction is DOWN<br>000:HiZ [EPWMxA = HiZ state]<br>001:Forced Hi [EPWMxA = High state]<br>010:Forced Lo [EPWMxA = Lo state]<br>011:Toggle [Low -> High, High -> Low]<br>100:Reserved<br>101:Reserved<br>110:Reserved<br>111:Do Nothing, trip action is disabled |
| 2:0   | DCAEVT1U   | R/W  | 0h    | Digital Compare Output A Event 1 Action On EPWMxA while Count direction is UP<br>000:HiZ [EPWMxA = HiZ state]<br>001:Forced Hi [EPWMxA = High state]<br>010:Forced Lo [EPWMxA = Lo state]<br>011:Toggle [Low -> High, High -> Low]<br>100:Reserved<br>101:Reserved<br>110:Reserved<br>111:Do Nothing, trip action is disabled   |

### 3.7.2.54 EPWM\_TZCTLDCB Register

#### 1 EPWM\_TZCTLDCB Register (Offset = 10Eh) [reset = 0h]

Trip Zone Control Register Digital Compare B .

Return to [Summary Table](#)

**Table 3-973. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 010Eh       |
| EPWM0_G1      | 5004 010Eh       |
| EPWM0_G2      | 5008 010Eh       |
| EPWM0_G3      | 500C 010Eh       |
| EPWM1_G0      | 5000 110Eh       |
| EPWM1_G1      | 5004 110Eh       |
| EPWM1_G2      | 5008 110Eh       |
| EPWM1_G3      | 500C 110Eh       |
| EPWM2_G0      | 5000 210Eh       |
| EPWM2_G1      | 5004 210Eh       |
| EPWM2_G2      | 5008 210Eh       |
| EPWM2_G3      | 500C 210Eh       |
| EPWM3_G0      | 5000 310Eh       |
| EPWM3_G1      | 5004 310Eh       |
| EPWM3_G2      | 5008 310Eh       |
| EPWM3_G3      | 500C 310Eh       |
| EPWM4_G0      | 5000 410Eh       |
| EPWM4_G1      | 5004 410Eh       |
| EPWM4_G2      | 5008 410Eh       |
| EPWM4_G3      | 500C 410Eh       |
| EPWM5_G0      | 5000 510Eh       |
| EPWM5_G1      | 5004 510Eh       |
| EPWM5_G2      | 5008 510Eh       |
| EPWM5_G3      | 500C 510Eh       |
| EPWM6_G0      | 5000 610Eh       |
| EPWM6_G1      | 5004 610Eh       |
| EPWM6_G2      | 5008 610Eh       |
| EPWM6_G3      | 500C 610Eh       |
| EPWM7_G0      | 5000 710Eh       |
| EPWM7_G1      | 5004 710Eh       |
| EPWM7_G2      | 5008 710Eh       |
| EPWM7_G3      | 500C 710Eh       |
| EPWM8_G0      | 5000 810Eh       |
| EPWM8_G1      | 5004 810Eh       |
| EPWM8_G2      | 5008 810Eh       |
| EPWM8_G3      | 500C 810Eh       |
| EPWM9_G0      | 5000 910Eh       |
| EPWM9_G1      | 5004 910Eh       |
| EPWM9_G2      | 5008 910Eh       |

**Table 3-973. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 910Eh       |
| EPWM10_G0     | 5000 A10Eh       |
| EPWM10_G1     | 5004 A10Eh       |
| EPWM10_G2     | 5008 A10Eh       |
| EPWM10_G3     | 500C A10Eh       |
| EPWM11_G0     | 5000 B10Eh       |
| EPWM11_G1     | 5004 B10Eh       |
| EPWM11_G2     | 5008 B10Eh       |
| EPWM11_G3     | 500C B10Eh       |
| EPWM12_G0     | 5000 C10Eh       |
| EPWM12_G1     | 5004 C10Eh       |
| EPWM12_G2     | 5008 C10Eh       |
| EPWM12_G3     | 500C C10Eh       |
| EPWM13_G0     | 5000 D10Eh       |
| EPWM13_G1     | 5004 D10Eh       |
| EPWM13_G2     | 5008 D10Eh       |
| EPWM13_G3     | 500C D10Eh       |
| EPWM14_G0     | 5000 E10Eh       |
| EPWM14_G1     | 5004 E10Eh       |
| EPWM14_G2     | 5008 E10Eh       |
| EPWM14_G3     | 500C E10Eh       |
| EPWM15_G0     | 5000 F10Eh       |
| EPWM15_G1     | 5004 F10Eh       |
| EPWM15_G2     | 5008 F10Eh       |
| EPWM15_G3     | 500C F10Eh       |
| EPWM16_G0     | 5001 010Eh       |
| EPWM16_G1     | 5005 010Eh       |
| EPWM16_G2     | 5009 010Eh       |
| EPWM16_G3     | 500D 010Eh       |
| EPWM17_G0     | 5001 110Eh       |
| EPWM17_G1     | 5005 110Eh       |
| EPWM17_G2     | 5009 110Eh       |
| EPWM17_G3     | 500D 110Eh       |
| EPWM18_G0     | 5001 210Eh       |
| EPWM18_G1     | 5005 210Eh       |
| EPWM18_G2     | 5009 210Eh       |
| EPWM18_G3     | 500D 210Eh       |
| EPWM19_G0     | 5001 310Eh       |
| EPWM19_G1     | 5005 310Eh       |
| EPWM19_G2     | 5009 310Eh       |
| EPWM19_G3     | 500D 310Eh       |
| EPWM20_G0     | 5001 410Eh       |
| EPWM20_G1     | 5005 410Eh       |
| EPWM20_G2     | 5009 410Eh       |
| EPWM20_G3     | 500D 410Eh       |

**Table 3-973. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 510Eh       |
| EPWM21_G1     | 5005 510Eh       |
| EPWM21_G2     | 5009 510Eh       |
| EPWM21_G3     | 500D 510Eh       |
| EPWM22_G0     | 5001 610Eh       |
| EPWM22_G1     | 5005 610Eh       |
| EPWM22_G2     | 5009 610Eh       |
| EPWM22_G3     | 500D 610Eh       |
| EPWM23_G0     | 5001 710Eh       |
| EPWM23_G1     | 5005 710Eh       |
| EPWM23_G2     | 5009 710Eh       |
| EPWM23_G3     | 500D 710Eh       |
| EPWM24_G0     | 5001 810Eh       |
| EPWM24_G1     | 5005 810Eh       |
| EPWM24_G2     | 5009 810Eh       |
| EPWM24_G3     | 500D 810Eh       |
| EPWM25_G0     | 5001 910Eh       |
| EPWM25_G1     | 5005 910Eh       |
| EPWM25_G2     | 5009 910Eh       |
| EPWM25_G3     | 500D 910Eh       |
| EPWM26_G0     | 5001 A10Eh       |
| EPWM26_G1     | 5005 A10Eh       |
| EPWM26_G2     | 5009 A10Eh       |
| EPWM26_G3     | 500D A10Eh       |
| EPWM27_G0     | 5001 B10Eh       |
| EPWM27_G1     | 5005 B10Eh       |
| EPWM27_G2     | 5009 B10Eh       |
| EPWM27_G3     | 500D B10Eh       |
| EPWM28_G0     | 5001 C10Eh       |
| EPWM28_G1     | 5005 C10Eh       |
| EPWM28_G2     | 5009 C10Eh       |
| EPWM28_G3     | 500D C10Eh       |
| EPWM29_G0     | 5001 D10Eh       |
| EPWM29_G1     | 5005 D10Eh       |
| EPWM29_G2     | 5009 D10Eh       |
| EPWM29_G3     | 500D D10Eh       |
| EPWM30_G0     | 5001 E10Eh       |
| EPWM30_G1     | 5005 E10Eh       |
| EPWM30_G2     | 5009 E10Eh       |
| EPWM30_G3     | 500D E10Eh       |
| EPWM31_G0     | 5001 F10Eh       |
| EPWM31_G1     | 5005 F10Eh       |
| EPWM31_G2     | 5009 F10Eh       |
| EPWM31_G3     | 500D F10Eh       |

**Figure 3-305. EPWM\_TZCTLDCB Name Register**

| 15         | 14 | 13       | 12 | 11       | 10       | 9 | 8        |
|------------|----|----------|----|----------|----------|---|----------|
| RESERVED_1 |    |          |    | DCBEVT2D |          |   | DCBEVT2U |
| R          |    |          |    | R/W      |          |   | R/W      |
| 0h         |    |          |    | 0h       |          |   | 0h       |
| 7          | 6  | 5        | 4  | 3        | 2        | 1 | 0        |
| DCBEVT2U   |    | DCBEVT1D |    |          | DCBEVT1U |   |          |
| R/W        |    | R/W      |    |          | R/W      |   |          |
| 0h         |    | 0h       |    |          | 0h       |   |          |

**Table 3-975. EPWM\_TZCTLDCB Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                     |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                        |
| 11:9  | DCBEVT2D   | R/W  | 0h    | Digital Compare Output B Event 2 Action On EPWMxB while Count direction is DOWN<br>000:HiZ [EPWMxB = HiZ state]<br>001:Forced Hi [EPWMxB = High state]<br>010:Forced Lo [EPWMxB = Lo state]<br>011:Toggle [Low -> High, High -> Low]<br>100:Reserved<br>101:Reserved<br>110:Reserved<br>111:Do Nothing, trip action is disabled |
| 8:6   | DCBEVT2U   | R/W  | 0h    | Digital Compare Output B Event 2 Action On EPWMxB while Count direction is UP<br>000:HiZ [EPWMxB = HiZ state]<br>001:Forced Hi [EPWMxB = High state]<br>010:Forced Lo [EPWMxB = Lo state]<br>011:Toggle [Low -> High, High -> Low]<br>100:Reserved<br>101:Reserved<br>110:Reserved<br>111:Do Nothing, trip action is disabled   |
| 5:3   | DCBEVT1D   | R/W  | 0h    | Digital Compare Output B Event 1 Action On EPWMxB while Count direction is DOWN<br>000:HiZ [EPWMxB = HiZ state]<br>001:Forced Hi [EPWMxB = High state]<br>010:Forced Lo [EPWMxB = Lo state]<br>011:Toggle [Low -> High, High -> Low]<br>100:Reserved<br>101:Reserved<br>110:Reserved<br>111:Do Nothing, trip action is disabled |
| 2:0   | DCBEVT1U   | R/W  | 0h    | Digital Compare Output B Event 1 Action On EPWMxB while Count direction is UP<br>000:HiZ [EPWMxB = HiZ state]<br>001:Forced Hi [EPWMxB = High state]<br>010:Forced Lo [EPWMxB = Lo state]<br>011:Toggle [Low -> High, High -> Low]<br>100:Reserved<br>101:Reserved<br>110:Reserved<br>111:Do Nothing, trip action is disabled   |

### 3.7.2.55 EPWM\_TZEINT Register

#### 1 EPWM\_TZEINT Register (Offset = 11Ah) [reset = 0h]

Trip Zone Enable Interrupt Register.

Return to [Summary Table](#)

**Table 3-976. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 011Ah       |
| EPWM0_G1      | 5004 011Ah       |
| EPWM0_G2      | 5008 011Ah       |
| EPWM0_G3      | 500C 011Ah       |
| EPWM1_G0      | 5000 111Ah       |
| EPWM1_G1      | 5004 111Ah       |
| EPWM1_G2      | 5008 111Ah       |
| EPWM1_G3      | 500C 111Ah       |
| EPWM2_G0      | 5000 211Ah       |
| EPWM2_G1      | 5004 211Ah       |
| EPWM2_G2      | 5008 211Ah       |
| EPWM2_G3      | 500C 211Ah       |
| EPWM3_G0      | 5000 311Ah       |
| EPWM3_G1      | 5004 311Ah       |
| EPWM3_G2      | 5008 311Ah       |
| EPWM3_G3      | 500C 311Ah       |
| EPWM4_G0      | 5000 411Ah       |
| EPWM4_G1      | 5004 411Ah       |
| EPWM4_G2      | 5008 411Ah       |
| EPWM4_G3      | 500C 411Ah       |
| EPWM5_G0      | 5000 511Ah       |
| EPWM5_G1      | 5004 511Ah       |
| EPWM5_G2      | 5008 511Ah       |
| EPWM5_G3      | 500C 511Ah       |
| EPWM6_G0      | 5000 611Ah       |
| EPWM6_G1      | 5004 611Ah       |
| EPWM6_G2      | 5008 611Ah       |
| EPWM6_G3      | 500C 611Ah       |
| EPWM7_G0      | 5000 711Ah       |
| EPWM7_G1      | 5004 711Ah       |
| EPWM7_G2      | 5008 711Ah       |
| EPWM7_G3      | 500C 711Ah       |
| EPWM8_G0      | 5000 811Ah       |
| EPWM8_G1      | 5004 811Ah       |
| EPWM8_G2      | 5008 811Ah       |
| EPWM8_G3      | 500C 811Ah       |
| EPWM9_G0      | 5000 911Ah       |
| EPWM9_G1      | 5004 911Ah       |
| EPWM9_G2      | 5008 911Ah       |



**Table 3-976. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 911Ah       |
| EPWM10_G0     | 5000 A11Ah       |
| EPWM10_G1     | 5004 A11Ah       |
| EPWM10_G2     | 5008 A11Ah       |
| EPWM10_G3     | 500C A11Ah       |
| EPWM11_G0     | 5000 B11Ah       |
| EPWM11_G1     | 5004 B11Ah       |
| EPWM11_G2     | 5008 B11Ah       |
| EPWM11_G3     | 500C B11Ah       |
| EPWM12_G0     | 5000 C11Ah       |
| EPWM12_G1     | 5004 C11Ah       |
| EPWM12_G2     | 5008 C11Ah       |
| EPWM12_G3     | 500C C11Ah       |
| EPWM13_G0     | 5000 D11Ah       |
| EPWM13_G1     | 5004 D11Ah       |
| EPWM13_G2     | 5008 D11Ah       |
| EPWM13_G3     | 500C D11Ah       |
| EPWM14_G0     | 5000 E11Ah       |
| EPWM14_G1     | 5004 E11Ah       |
| EPWM14_G2     | 5008 E11Ah       |
| EPWM14_G3     | 500C E11Ah       |
| EPWM15_G0     | 5000 F11Ah       |
| EPWM15_G1     | 5004 F11Ah       |
| EPWM15_G2     | 5008 F11Ah       |
| EPWM15_G3     | 500C F11Ah       |
| EPWM16_G0     | 5001 011Ah       |
| EPWM16_G1     | 5005 011Ah       |
| EPWM16_G2     | 5009 011Ah       |
| EPWM16_G3     | 500D 011Ah       |
| EPWM17_G0     | 5001 111Ah       |
| EPWM17_G1     | 5005 111Ah       |
| EPWM17_G2     | 5009 111Ah       |
| EPWM17_G3     | 500D 111Ah       |
| EPWM18_G0     | 5001 211Ah       |
| EPWM18_G1     | 5005 211Ah       |
| EPWM18_G2     | 5009 211Ah       |
| EPWM18_G3     | 500D 211Ah       |
| EPWM19_G0     | 5001 311Ah       |
| EPWM19_G1     | 5005 311Ah       |
| EPWM19_G2     | 5009 311Ah       |
| EPWM19_G3     | 500D 311Ah       |
| EPWM20_G0     | 5001 411Ah       |
| EPWM20_G1     | 5005 411Ah       |
| EPWM20_G2     | 5009 411Ah       |
| EPWM20_G3     | 500D 411Ah       |

**Table 3-976. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 511Ah       |
| EPWM21_G1     | 5005 511Ah       |
| EPWM21_G2     | 5009 511Ah       |
| EPWM21_G3     | 500D 511Ah       |
| EPWM22_G0     | 5001 611Ah       |
| EPWM22_G1     | 5005 611Ah       |
| EPWM22_G2     | 5009 611Ah       |
| EPWM22_G3     | 500D 611Ah       |
| EPWM23_G0     | 5001 711Ah       |
| EPWM23_G1     | 5005 711Ah       |
| EPWM23_G2     | 5009 711Ah       |
| EPWM23_G3     | 500D 711Ah       |
| EPWM24_G0     | 5001 811Ah       |
| EPWM24_G1     | 5005 811Ah       |
| EPWM24_G2     | 5009 811Ah       |
| EPWM24_G3     | 500D 811Ah       |
| EPWM25_G0     | 5001 911Ah       |
| EPWM25_G1     | 5005 911Ah       |
| EPWM25_G2     | 5009 911Ah       |
| EPWM25_G3     | 500D 911Ah       |
| EPWM26_G0     | 5001 A11Ah       |
| EPWM26_G1     | 5005 A11Ah       |
| EPWM26_G2     | 5009 A11Ah       |
| EPWM26_G3     | 500D A11Ah       |
| EPWM27_G0     | 5001 B11Ah       |
| EPWM27_G1     | 5005 B11Ah       |
| EPWM27_G2     | 5009 B11Ah       |
| EPWM27_G3     | 500D B11Ah       |
| EPWM28_G0     | 5001 C11Ah       |
| EPWM28_G1     | 5005 C11Ah       |
| EPWM28_G2     | 5009 C11Ah       |
| EPWM28_G3     | 500D C11Ah       |
| EPWM29_G0     | 5001 D11Ah       |
| EPWM29_G1     | 5005 D11Ah       |
| EPWM29_G2     | 5009 D11Ah       |
| EPWM29_G3     | 500D D11Ah       |
| EPWM30_G0     | 5001 E11Ah       |
| EPWM30_G1     | 5005 E11Ah       |
| EPWM30_G2     | 5009 E11Ah       |
| EPWM30_G3     | 500D E11Ah       |
| EPWM31_G0     | 5001 F11Ah       |
| EPWM31_G1     | 5005 F11Ah       |
| EPWM31_G2     | 5009 F11Ah       |
| EPWM31_G3     | 500D F11Ah       |

**Figure 3-306. EPWM\_TZEINT Name Register**

| 15         | 14      | 13      | 12      | 11      | 10  | 9   | 8          |
|------------|---------|---------|---------|---------|-----|-----|------------|
| RESERVED_2 |         |         |         |         |     |     |            |
| R          |         |         |         |         |     |     |            |
| 0h         |         |         |         |         |     |     |            |
| 7          | 6       | 5       | 4       | 3       | 2   | 1   | 0          |
| CAPEVT     | DCBEVT2 | DCBEVT1 | DCAEVT2 | DCAEVT1 | OST | CBC | RESERVED_1 |
| R/W        | R/W     | R/W     | R/W     | R/W     | R/W | R/W | R          |
| 0h         | 0h      | 0h      | 0h      | 0h      | 0h  | 0h  | 0h         |

**Table 3-978. EPWM\_TZEINT Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                          |
|------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                             |
| 7    | CAPEVT     | R/W  | 0h    | Capture Event Interrupt Enable<br>0:Disabled<br>1:Enabled                                                                                                                                            |
| 6    | DCBEVT2    | R/W  | 0h    | Digital Compare Output B Event 2 Interrupt Enable<br>0:Disabled<br>1:Enabled                                                                                                                         |
| 5    | DCBEVT1    | R/W  | 0h    | Digital Compare Output B Event 1 Interrupt Enable<br>0:Disabled<br>1:Enabled                                                                                                                         |
| 4    | DCAEVT2    | R/W  | 0h    | Digital Compare Output A Event 2 Interrupt Enable<br>0:Disabled<br>1:Enabled                                                                                                                         |
| 3    | DCAEVT1    | R/W  | 0h    | Digital Compare Output A Event 1 Interrupt Enable<br>0:Disabled<br>1:Enabled                                                                                                                         |
| 2    | OST        | R/W  | 0h    | Trip-Zone One-Shot Interrupt Enable<br>0:Disable one-shot interrupt generation<br>1:Enable Interrupt generation<br>a one-shot trip event will cause a EPWMx_TZINT VIM interrupt.                     |
| 1    | CBC        | R/W  | 0h    | Trip-Zone Cycle-by-Cycle Interrupt Enable<br>0:Disable cycle-by-cycle interrupt generation.<br>1:Enable interrupt generation<br>A cycle-by-cycle trip event will cause an EPWMx_TZINT VIM interrupt. |
| 0    | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                             |

### 3.7.2.56 EPWM\_TZFLG Register

#### 1 EPWM\_TZFLG Register (Offset = 126h) [reset = 0h]

Trip Zone Flag Register.

Return to [Summary Table](#)

**Table 3-979. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0126h       |
| EPWM0_G1      | 5004 0126h       |
| EPWM0_G2      | 5008 0126h       |
| EPWM0_G3      | 500C 0126h       |
| EPWM1_G0      | 5000 1126h       |
| EPWM1_G1      | 5004 1126h       |
| EPWM1_G2      | 5008 1126h       |
| EPWM1_G3      | 500C 1126h       |
| EPWM2_G0      | 5000 2126h       |
| EPWM2_G1      | 5004 2126h       |
| EPWM2_G2      | 5008 2126h       |
| EPWM2_G3      | 500C 2126h       |
| EPWM3_G0      | 5000 3126h       |
| EPWM3_G1      | 5004 3126h       |
| EPWM3_G2      | 5008 3126h       |
| EPWM3_G3      | 500C 3126h       |
| EPWM4_G0      | 5000 4126h       |
| EPWM4_G1      | 5004 4126h       |
| EPWM4_G2      | 5008 4126h       |
| EPWM4_G3      | 500C 4126h       |
| EPWM5_G0      | 5000 5126h       |
| EPWM5_G1      | 5004 5126h       |
| EPWM5_G2      | 5008 5126h       |
| EPWM5_G3      | 500C 5126h       |
| EPWM6_G0      | 5000 6126h       |
| EPWM6_G1      | 5004 6126h       |
| EPWM6_G2      | 5008 6126h       |
| EPWM6_G3      | 500C 6126h       |
| EPWM7_G0      | 5000 7126h       |
| EPWM7_G1      | 5004 7126h       |
| EPWM7_G2      | 5008 7126h       |
| EPWM7_G3      | 500C 7126h       |
| EPWM8_G0      | 5000 8126h       |
| EPWM8_G1      | 5004 8126h       |
| EPWM8_G2      | 5008 8126h       |
| EPWM8_G3      | 500C 8126h       |
| EPWM9_G0      | 5000 9126h       |
| EPWM9_G1      | 5004 9126h       |
| EPWM9_G2      | 5008 9126h       |

**Table 3-979. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9126h       |
| EPWM10_G0     | 5000 A126h       |
| EPWM10_G1     | 5004 A126h       |
| EPWM10_G2     | 5008 A126h       |
| EPWM10_G3     | 500C A126h       |
| EPWM11_G0     | 5000 B126h       |
| EPWM11_G1     | 5004 B126h       |
| EPWM11_G2     | 5008 B126h       |
| EPWM11_G3     | 500C B126h       |
| EPWM12_G0     | 5000 C126h       |
| EPWM12_G1     | 5004 C126h       |
| EPWM12_G2     | 5008 C126h       |
| EPWM12_G3     | 500C C126h       |
| EPWM13_G0     | 5000 D126h       |
| EPWM13_G1     | 5004 D126h       |
| EPWM13_G2     | 5008 D126h       |
| EPWM13_G3     | 500C D126h       |
| EPWM14_G0     | 5000 E126h       |
| EPWM14_G1     | 5004 E126h       |
| EPWM14_G2     | 5008 E126h       |
| EPWM14_G3     | 500C E126h       |
| EPWM15_G0     | 5000 F126h       |
| EPWM15_G1     | 5004 F126h       |
| EPWM15_G2     | 5008 F126h       |
| EPWM15_G3     | 500C F126h       |
| EPWM16_G0     | 5001 0126h       |
| EPWM16_G1     | 5005 0126h       |
| EPWM16_G2     | 5009 0126h       |
| EPWM16_G3     | 500D 0126h       |
| EPWM17_G0     | 5001 1126h       |
| EPWM17_G1     | 5005 1126h       |
| EPWM17_G2     | 5009 1126h       |
| EPWM17_G3     | 500D 1126h       |
| EPWM18_G0     | 5001 2126h       |
| EPWM18_G1     | 5005 2126h       |
| EPWM18_G2     | 5009 2126h       |
| EPWM18_G3     | 500D 2126h       |
| EPWM19_G0     | 5001 3126h       |
| EPWM19_G1     | 5005 3126h       |
| EPWM19_G2     | 5009 3126h       |
| EPWM19_G3     | 500D 3126h       |
| EPWM20_G0     | 5001 4126h       |
| EPWM20_G1     | 5005 4126h       |
| EPWM20_G2     | 5009 4126h       |
| EPWM20_G3     | 500D 4126h       |

**Table 3-979. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5126h       |
| EPWM21_G1     | 5005 5126h       |
| EPWM21_G2     | 5009 5126h       |
| EPWM21_G3     | 500D 5126h       |
| EPWM22_G0     | 5001 6126h       |
| EPWM22_G1     | 5005 6126h       |
| EPWM22_G2     | 5009 6126h       |
| EPWM22_G3     | 500D 6126h       |
| EPWM23_G0     | 5001 7126h       |
| EPWM23_G1     | 5005 7126h       |
| EPWM23_G2     | 5009 7126h       |
| EPWM23_G3     | 500D 7126h       |
| EPWM24_G0     | 5001 8126h       |
| EPWM24_G1     | 5005 8126h       |
| EPWM24_G2     | 5009 8126h       |
| EPWM24_G3     | 500D 8126h       |
| EPWM25_G0     | 5001 9126h       |
| EPWM25_G1     | 5005 9126h       |
| EPWM25_G2     | 5009 9126h       |
| EPWM25_G3     | 500D 9126h       |
| EPWM26_G0     | 5001 A126h       |
| EPWM26_G1     | 5005 A126h       |
| EPWM26_G2     | 5009 A126h       |
| EPWM26_G3     | 500D A126h       |
| EPWM27_G0     | 5001 B126h       |
| EPWM27_G1     | 5005 B126h       |
| EPWM27_G2     | 5009 B126h       |
| EPWM27_G3     | 500D B126h       |
| EPWM28_G0     | 5001 C126h       |
| EPWM28_G1     | 5005 C126h       |
| EPWM28_G2     | 5009 C126h       |
| EPWM28_G3     | 500D C126h       |
| EPWM29_G0     | 5001 D126h       |
| EPWM29_G1     | 5005 D126h       |
| EPWM29_G2     | 5009 D126h       |
| EPWM29_G3     | 500D D126h       |
| EPWM30_G0     | 5001 E126h       |
| EPWM30_G1     | 5005 E126h       |
| EPWM30_G2     | 5009 E126h       |
| EPWM30_G3     | 500D E126h       |
| EPWM31_G0     | 5001 F126h       |
| EPWM31_G1     | 5005 F126h       |
| EPWM31_G2     | 5009 F126h       |
| EPWM31_G3     | 500D F126h       |

**Figure 3-307. EPWM\_TZFLG Name Register**

| 15         | 14      | 13      | 12      | 11      | 10  | 9   | 8   |
|------------|---------|---------|---------|---------|-----|-----|-----|
| RESERVED_1 |         |         |         |         |     |     |     |
| R          |         |         |         |         |     |     |     |
| 0h         |         |         |         |         |     |     |     |
| 7          | 6       | 5       | 4       | 3       | 2   | 1   | 0   |
| CAPEVT     | DCBEVT2 | DCBEVT1 | DCAEVT2 | DCAEVT1 | OST | CBC | INT |
| R          | R       | R       | R       | R       | R   | R   | R   |
| 0h         | 0h      | 0h      | 0h      | 0h      | 0h  | 0h  | 0h  |

**Table 3-981. EPWM\_TZFLG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 7    | CAPEVT     | R    | 0h    | Latched Status Flag for Capture Event<br>0:Indicates no trip event has occurred on CAPEVT<br>1:Indicates a trip event has occurred for the event defined for CAPEVT                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 6    | DCBEVT2    | R    | 0h    | Latched Status Flag for Digital Compare Output B Event 2<br>0:Indicates no trip event has occurred on DCBEVT2<br>1:Indicates a trip event has occurred for the event defined for DCBEVT2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 5    | DCBEVT1    | R    | 0h    | Latched Status Flag for Digital Compare Output B Event 1<br>0:Indicates no trip event has occurred on DCBEVT1<br>1:Indicates a trip event has occurred for the event defined for DCBEVT1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 4    | DCAEVT2    | R    | 0h    | Latched Status Flag for Digital Compare Output A Event 2<br>0:Indicates no trip event has occurred on DCAEVT2<br>1:Indicates a trip event has occurred for the event defined for DCAEVT2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 3    | DCAEVT1    | R    | 0h    | Latched Status Flag for Digital Compare Output A Event 1<br>0:Indicates no trip event has occurred on DCAEVT1<br>1:Indicates a trip event has occurred for the event defined for DCAEVT1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 2    | OST        | R    | 0h    | Latched Status Flag for A One-Shot Trip Event<br>0:No one-shot trip event has occurred.<br>1:Indicates a trip event has occurred on a pin selected as a one-shot trip source.<br>This bit is cleared by Writing the appropriate value to the TZCLR register.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 1    | CBC        | R    | 0h    | Latched Status Flag for Cycle-By-Cycle Trip Event<br>0:No cycle-by-cycle trip event has occurred.<br>1:Indicates a trip event has occurred on a signal selected as a cycle-by-cycle trip source. The TZFLG[CBC] bit will remain set until it is manually cleared by the user. If the cycle-by-cycle trip event is still present when the CBC bit is cleared, then CBC will be immediately set again. The specified condition on the signal is automatically cleared when the EPWM time-base counter reaches zero [TBCTR = 0x00] if the trip condition is no longer present. The condition on the signal is only cleared when the TBCTR = 0x00 no matter where in the cycle the CBC flag is cleared.<br>This bit is cleared by Writing the appropriate value to the TZCLR register. |

**Table 3-981. EPWM\_TZFLG Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-----|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | INT   | R    | 0h    | <p>Latched Trip Interrupt Status Flag</p> <p>0:Indicates no interrupt has been generated.</p> <p>1:Indicates an EPWMx_TZINT VIM interrupt was generated because of a trip condition.</p> <p>No further EPWMx_TZINT VIM interrupts will be generated until this flag is cleared. If the interrupt flag is cleared when either CBC or OST is set, then another interrupt pulse will be generated. Clearing all flag bits will prevent further interrupts. This bit is cleared by Writing the appropriate value to the TZCLR register.</p> |



### 3.7.2.57 EPWM\_TZCBCFLG Register

#### 1 EPWM\_TZCBCFLG Register (Offset = 128h) [reset = 0h]

Trip Zone CBC Flag Register.

Return to [Summary Table](#)

**Table 3-982. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0128h       |
| EPWM0_G1      | 5004 0128h       |
| EPWM0_G2      | 5008 0128h       |
| EPWM0_G3      | 500C 0128h       |
| EPWM1_G0      | 5000 1128h       |
| EPWM1_G1      | 5004 1128h       |
| EPWM1_G2      | 5008 1128h       |
| EPWM1_G3      | 500C 1128h       |
| EPWM2_G0      | 5000 2128h       |
| EPWM2_G1      | 5004 2128h       |
| EPWM2_G2      | 5008 2128h       |
| EPWM2_G3      | 500C 2128h       |
| EPWM3_G0      | 5000 3128h       |
| EPWM3_G1      | 5004 3128h       |
| EPWM3_G2      | 5008 3128h       |
| EPWM3_G3      | 500C 3128h       |
| EPWM4_G0      | 5000 4128h       |
| EPWM4_G1      | 5004 4128h       |
| EPWM4_G2      | 5008 4128h       |
| EPWM4_G3      | 500C 4128h       |
| EPWM5_G0      | 5000 5128h       |
| EPWM5_G1      | 5004 5128h       |
| EPWM5_G2      | 5008 5128h       |
| EPWM5_G3      | 500C 5128h       |
| EPWM6_G0      | 5000 6128h       |
| EPWM6_G1      | 5004 6128h       |
| EPWM6_G2      | 5008 6128h       |
| EPWM6_G3      | 500C 6128h       |
| EPWM7_G0      | 5000 7128h       |
| EPWM7_G1      | 5004 7128h       |
| EPWM7_G2      | 5008 7128h       |
| EPWM7_G3      | 500C 7128h       |
| EPWM8_G0      | 5000 8128h       |
| EPWM8_G1      | 5004 8128h       |
| EPWM8_G2      | 5008 8128h       |
| EPWM8_G3      | 500C 8128h       |
| EPWM9_G0      | 5000 9128h       |
| EPWM9_G1      | 5004 9128h       |
| EPWM9_G2      | 5008 9128h       |

**Table 3-982. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9128h       |
| EPWM10_G0     | 5000 A128h       |
| EPWM10_G1     | 5004 A128h       |
| EPWM10_G2     | 5008 A128h       |
| EPWM10_G3     | 500C A128h       |
| EPWM11_G0     | 5000 B128h       |
| EPWM11_G1     | 5004 B128h       |
| EPWM11_G2     | 5008 B128h       |
| EPWM11_G3     | 500C B128h       |
| EPWM12_G0     | 5000 C128h       |
| EPWM12_G1     | 5004 C128h       |
| EPWM12_G2     | 5008 C128h       |
| EPWM12_G3     | 500C C128h       |
| EPWM13_G0     | 5000 D128h       |
| EPWM13_G1     | 5004 D128h       |
| EPWM13_G2     | 5008 D128h       |
| EPWM13_G3     | 500C D128h       |
| EPWM14_G0     | 5000 E128h       |
| EPWM14_G1     | 5004 E128h       |
| EPWM14_G2     | 5008 E128h       |
| EPWM14_G3     | 500C E128h       |
| EPWM15_G0     | 5000 F128h       |
| EPWM15_G1     | 5004 F128h       |
| EPWM15_G2     | 5008 F128h       |
| EPWM15_G3     | 500C F128h       |
| EPWM16_G0     | 5001 0128h       |
| EPWM16_G1     | 5005 0128h       |
| EPWM16_G2     | 5009 0128h       |
| EPWM16_G3     | 500D 0128h       |
| EPWM17_G0     | 5001 1128h       |
| EPWM17_G1     | 5005 1128h       |
| EPWM17_G2     | 5009 1128h       |
| EPWM17_G3     | 500D 1128h       |
| EPWM18_G0     | 5001 2128h       |
| EPWM18_G1     | 5005 2128h       |
| EPWM18_G2     | 5009 2128h       |
| EPWM18_G3     | 500D 2128h       |
| EPWM19_G0     | 5001 3128h       |
| EPWM19_G1     | 5005 3128h       |
| EPWM19_G2     | 5009 3128h       |
| EPWM19_G3     | 500D 3128h       |
| EPWM20_G0     | 5001 4128h       |
| EPWM20_G1     | 5005 4128h       |
| EPWM20_G2     | 5009 4128h       |
| EPWM20_G3     | 500D 4128h       |

**Table 3-982. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5128h       |
| EPWM21_G1     | 5005 5128h       |
| EPWM21_G2     | 5009 5128h       |
| EPWM21_G3     | 500D 5128h       |
| EPWM22_G0     | 5001 6128h       |
| EPWM22_G1     | 5005 6128h       |
| EPWM22_G2     | 5009 6128h       |
| EPWM22_G3     | 500D 6128h       |
| EPWM23_G0     | 5001 7128h       |
| EPWM23_G1     | 5005 7128h       |
| EPWM23_G2     | 5009 7128h       |
| EPWM23_G3     | 500D 7128h       |
| EPWM24_G0     | 5001 8128h       |
| EPWM24_G1     | 5005 8128h       |
| EPWM24_G2     | 5009 8128h       |
| EPWM24_G3     | 500D 8128h       |
| EPWM25_G0     | 5001 9128h       |
| EPWM25_G1     | 5005 9128h       |
| EPWM25_G2     | 5009 9128h       |
| EPWM25_G3     | 500D 9128h       |
| EPWM26_G0     | 5001 A128h       |
| EPWM26_G1     | 5005 A128h       |
| EPWM26_G2     | 5009 A128h       |
| EPWM26_G3     | 500D A128h       |
| EPWM27_G0     | 5001 B128h       |
| EPWM27_G1     | 5005 B128h       |
| EPWM27_G2     | 5009 B128h       |
| EPWM27_G3     | 500D B128h       |
| EPWM28_G0     | 5001 C128h       |
| EPWM28_G1     | 5005 C128h       |
| EPWM28_G2     | 5009 C128h       |
| EPWM28_G3     | 500D C128h       |
| EPWM29_G0     | 5001 D128h       |
| EPWM29_G1     | 5005 D128h       |
| EPWM29_G2     | 5009 D128h       |
| EPWM29_G3     | 500D D128h       |
| EPWM30_G0     | 5001 E128h       |
| EPWM30_G1     | 5005 E128h       |
| EPWM30_G2     | 5009 E128h       |
| EPWM30_G3     | 500D E128h       |
| EPWM31_G0     | 5001 F128h       |
| EPWM31_G1     | 5005 F128h       |
| EPWM31_G2     | 5009 F128h       |
| EPWM31_G3     | 500D F128h       |

**Figure 3-308. EPWM\_TZCBCFLG Name Register**

| 15         | 14      | 13   | 12   | 11   | 10   | 9    | 8      |
|------------|---------|------|------|------|------|------|--------|
| RESERVED_1 |         |      |      |      |      |      | CAPEVT |
| R          |         |      |      |      |      |      | R      |
| 0h         |         |      |      |      |      |      | 0h     |
| 7          | 6       | 5    | 4    | 3    | 2    | 1    | 0      |
| DCBEVT2    | DCAEVT2 | CBC6 | CBC5 | CBC4 | CBC3 | CBC2 | CBC1   |
| R          | R       | R    | R    | R    | R    | R    | R      |
| 0h         | 0h      | 0h   | 0h   | 0h   | 0h   | 0h   | 0h     |

**Table 3-984. EPWM\_TZCBCFLG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                        |
|------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:9 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                           |
| 8    | CAPEVT     | R    | 0h    | Latched Status Flag for Capture Event<br>0:Indicates no trip event has occurred on CAPEVT<br>1:Indicates a trip event has occurred for the event defined for CAPEVT                                                |
| 7    | DCBEVT2    | R    | 0h    | Latched Status Flag for Digital Compare B Output Event 2 Trip Latch<br>0:Reading a 0 indicates that no trip has occurred on DCBEVT2.<br>1:Reading a 1 indicates a trip has occurred on the DCBEVT2 selected event. |
| 6    | DCAEVT2    | R    | 0h    | Latched Status Flag for Digital Compare A Output Event 2 Trip Latch<br>0:Reading a 0 indicates that no trip has occurred on DCAEVT2.<br>1:Reading a 1 indicates a trip has occurred on the DCAEVT2 selected event. |
| 5    | CBC6       | R    | 0h    | Latched Status Flag for CBC6 Trip Latch<br>0:Reading a 0 indicates that no trip has occurred on CBC6.<br>1:Reading a 1 indicates a trip has occurred on the CBC6 selected event.                                   |
| 4    | CBC5       | R    | 0h    | Latched Status Flag for CBC5 Trip Latch<br>0:Reading a 0 indicates that no trip has occurred on CBC5.<br>1:Reading a 1 indicates a trip has occurred on the CBC5 selected event.                                   |
| 3    | CBC4       | R    | 0h    | Latched Status Flag for CBC4 Trip Latch<br>0:Reading a 0 indicates that no trip has occurred on CBC4.<br>1:Reading a 1 indicates a trip has occurred on the CBC4 selected event.                                   |
| 2    | CBC3       | R    | 0h    | Latched Status Flag for CBC3 Trip Latch<br>0:Reading a 0 indicates that no trip has occurred on CBC3.<br>1:Reading a 1 indicates a trip has occurred on the CBC3 selected event.                                   |
| 1    | CBC2       | R    | 0h    | Latched Status Flag for CBC2 Trip Latch<br>0:Reading a 0 indicates that no trip has occurred on CBC2.<br>1:Reading a 1 indicates a trip has occurred on the CBC2 selected event.                                   |
| 0    | CBC1       | R    | 0h    | Latched Status Flag for CBC1 Trip Latch<br>0:Reading a 0 indicates that no trip has occurred on CBC1.<br>1:Reading a 1 indicates a trip has occurred on the CBC1 selected event.                                   |

### 3.7.2.58 EPWM\_TZOSTFLG Register

#### 1 EPWM\_TZOSTFLG Register (Offset = 12Ah) [reset = 0h]

Trip Zone OST Flag Register.

Return to [Summary Table](#)

**Table 3-985. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 012Ah       |
| EPWM0_G1      | 5004 012Ah       |
| EPWM0_G2      | 5008 012Ah       |
| EPWM0_G3      | 500C 012Ah       |
| EPWM1_G0      | 5000 112Ah       |
| EPWM1_G1      | 5004 112Ah       |
| EPWM1_G2      | 5008 112Ah       |
| EPWM1_G3      | 500C 112Ah       |
| EPWM2_G0      | 5000 212Ah       |
| EPWM2_G1      | 5004 212Ah       |
| EPWM2_G2      | 5008 212Ah       |
| EPWM2_G3      | 500C 212Ah       |
| EPWM3_G0      | 5000 312Ah       |
| EPWM3_G1      | 5004 312Ah       |
| EPWM3_G2      | 5008 312Ah       |
| EPWM3_G3      | 500C 312Ah       |
| EPWM4_G0      | 5000 412Ah       |
| EPWM4_G1      | 5004 412Ah       |
| EPWM4_G2      | 5008 412Ah       |
| EPWM4_G3      | 500C 412Ah       |
| EPWM5_G0      | 5000 512Ah       |
| EPWM5_G1      | 5004 512Ah       |
| EPWM5_G2      | 5008 512Ah       |
| EPWM5_G3      | 500C 512Ah       |
| EPWM6_G0      | 5000 612Ah       |
| EPWM6_G1      | 5004 612Ah       |
| EPWM6_G2      | 5008 612Ah       |
| EPWM6_G3      | 500C 612Ah       |
| EPWM7_G0      | 5000 712Ah       |
| EPWM7_G1      | 5004 712Ah       |
| EPWM7_G2      | 5008 712Ah       |
| EPWM7_G3      | 500C 712Ah       |
| EPWM8_G0      | 5000 812Ah       |
| EPWM8_G1      | 5004 812Ah       |
| EPWM8_G2      | 5008 812Ah       |
| EPWM8_G3      | 500C 812Ah       |
| EPWM9_G0      | 5000 912Ah       |
| EPWM9_G1      | 5004 912Ah       |
| EPWM9_G2      | 5008 912Ah       |

**Table 3-985. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 912Ah       |
| EPWM10_G0     | 5000 A12Ah       |
| EPWM10_G1     | 5004 A12Ah       |
| EPWM10_G2     | 5008 A12Ah       |
| EPWM10_G3     | 500C A12Ah       |
| EPWM11_G0     | 5000 B12Ah       |
| EPWM11_G1     | 5004 B12Ah       |
| EPWM11_G2     | 5008 B12Ah       |
| EPWM11_G3     | 500C B12Ah       |
| EPWM12_G0     | 5000 C12Ah       |
| EPWM12_G1     | 5004 C12Ah       |
| EPWM12_G2     | 5008 C12Ah       |
| EPWM12_G3     | 500C C12Ah       |
| EPWM13_G0     | 5000 D12Ah       |
| EPWM13_G1     | 5004 D12Ah       |
| EPWM13_G2     | 5008 D12Ah       |
| EPWM13_G3     | 500C D12Ah       |
| EPWM14_G0     | 5000 E12Ah       |
| EPWM14_G1     | 5004 E12Ah       |
| EPWM14_G2     | 5008 E12Ah       |
| EPWM14_G3     | 500C E12Ah       |
| EPWM15_G0     | 5000 F12Ah       |
| EPWM15_G1     | 5004 F12Ah       |
| EPWM15_G2     | 5008 F12Ah       |
| EPWM15_G3     | 500C F12Ah       |
| EPWM16_G0     | 5001 012Ah       |
| EPWM16_G1     | 5005 012Ah       |
| EPWM16_G2     | 5009 012Ah       |
| EPWM16_G3     | 500D 012Ah       |
| EPWM17_G0     | 5001 112Ah       |
| EPWM17_G1     | 5005 112Ah       |
| EPWM17_G2     | 5009 112Ah       |
| EPWM17_G3     | 500D 112Ah       |
| EPWM18_G0     | 5001 212Ah       |
| EPWM18_G1     | 5005 212Ah       |
| EPWM18_G2     | 5009 212Ah       |
| EPWM18_G3     | 500D 212Ah       |
| EPWM19_G0     | 5001 312Ah       |
| EPWM19_G1     | 5005 312Ah       |
| EPWM19_G2     | 5009 312Ah       |
| EPWM19_G3     | 500D 312Ah       |
| EPWM20_G0     | 5001 412Ah       |
| EPWM20_G1     | 5005 412Ah       |
| EPWM20_G2     | 5009 412Ah       |
| EPWM20_G3     | 500D 412Ah       |

**Table 3-985. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 512Ah       |
| EPWM21_G1     | 5005 512Ah       |
| EPWM21_G2     | 5009 512Ah       |
| EPWM21_G3     | 500D 512Ah       |
| EPWM22_G0     | 5001 612Ah       |
| EPWM22_G1     | 5005 612Ah       |
| EPWM22_G2     | 5009 612Ah       |
| EPWM22_G3     | 500D 612Ah       |
| EPWM23_G0     | 5001 712Ah       |
| EPWM23_G1     | 5005 712Ah       |
| EPWM23_G2     | 5009 712Ah       |
| EPWM23_G3     | 500D 712Ah       |
| EPWM24_G0     | 5001 812Ah       |
| EPWM24_G1     | 5005 812Ah       |
| EPWM24_G2     | 5009 812Ah       |
| EPWM24_G3     | 500D 812Ah       |
| EPWM25_G0     | 5001 912Ah       |
| EPWM25_G1     | 5005 912Ah       |
| EPWM25_G2     | 5009 912Ah       |
| EPWM25_G3     | 500D 912Ah       |
| EPWM26_G0     | 5001 A12Ah       |
| EPWM26_G1     | 5005 A12Ah       |
| EPWM26_G2     | 5009 A12Ah       |
| EPWM26_G3     | 500D A12Ah       |
| EPWM27_G0     | 5001 B12Ah       |
| EPWM27_G1     | 5005 B12Ah       |
| EPWM27_G2     | 5009 B12Ah       |
| EPWM27_G3     | 500D B12Ah       |
| EPWM28_G0     | 5001 C12Ah       |
| EPWM28_G1     | 5005 C12Ah       |
| EPWM28_G2     | 5009 C12Ah       |
| EPWM28_G3     | 500D C12Ah       |
| EPWM29_G0     | 5001 D12Ah       |
| EPWM29_G1     | 5005 D12Ah       |
| EPWM29_G2     | 5009 D12Ah       |
| EPWM29_G3     | 500D D12Ah       |
| EPWM30_G0     | 5001 E12Ah       |
| EPWM30_G1     | 5005 E12Ah       |
| EPWM30_G2     | 5009 E12Ah       |
| EPWM30_G3     | 500D E12Ah       |
| EPWM31_G0     | 5001 F12Ah       |
| EPWM31_G1     | 5005 F12Ah       |
| EPWM31_G2     | 5009 F12Ah       |
| EPWM31_G3     | 500D F12Ah       |

**Figure 3-309. EPWM\_TZOSTFLG Name Register**

| 15         | 14      | 13   | 12   | 11   | 10   | 9    | 8      |
|------------|---------|------|------|------|------|------|--------|
| RESERVED_1 |         |      |      |      |      |      | CAPEVT |
| R          |         |      |      |      |      |      | R      |
| 0h         |         |      |      |      |      |      | 0h     |
| 7          | 6       | 5    | 4    | 3    | 2    | 1    | 0      |
| DCBEVT1    | DCAEVT1 | OST6 | OST5 | OST4 | OST3 | OST2 | OST1   |
| R          | R       | R    | R    | R    | R    | R    | R      |
| 0h         | 0h      | 0h   | 0h   | 0h   | 0h   | 0h   | 0h     |

**Table 3-987. EPWM\_TZOSTFLG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                        |
|------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:9 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                           |
| 8    | CAPEVT     | R    | 0h    | Latched Status Flag for Capture Event<br>0:Indicates no trip event has occurred on CAPEVT<br>1:Indicates a trip event has occurred for the event defined for CAPEVT                                                |
| 7    | DCBEVT1    | R    | 0h    | Latched Status Flag for Digital Compare B Output Event 1 Trip Latch<br>0:Reading a 0 indicates that no trip has occurred on DCBEVT1.<br>1:Reading a 1 indicates a trip has occurred on the DCBEVT1 selected event. |
| 6    | DCAEVT1    | R    | 0h    | Latched Status Flag for Digital Compare A Output Event 1 Trip Latch<br>0:Reading a 0 indicates that no trip has occurred on DCAEVT1.<br>1:Reading a 1 indicates a trip has occurred on the DCAEVT1 selected event. |
| 5    | OST6       | R    | 0h    | Latched Status Flag for OST6 Trip Latch<br>0:Reading a 0 indicates that no trip has occurred on OST6.<br>1:Reading a 1 indicates a trip has occurred on the OST6 selected event.                                   |
| 4    | OST5       | R    | 0h    | Latched Status Flag for OST5 Trip Latch<br>0:Reading a 0 indicates that no trip has occurred on OST5.<br>1:Reading a 1 indicates a trip has occurred on the OST5 selected event.                                   |
| 3    | OST4       | R    | 0h    | Latched Status Flag for OST4 Trip Latch<br>0:Reading a 0 indicates that no trip has occurred on OST4.<br>1:Reading a 1 indicates a trip has occurred on the OST4 selected event.                                   |
| 2    | OST3       | R    | 0h    | Latched Status Flag for OST3 Trip Latch<br>0:Reading a 0 indicates that no trip has occurred on OST3.<br>1:Reading a 1 indicates a trip has occurred on the OST3 selected event.                                   |
| 1    | OST2       | R    | 0h    | Latched Status Flag for OST2 Trip Latch<br>0:Reading a 0 indicates that no trip has occurred on OST2.<br>1:Reading a 1 indicates a trip has occurred on the OST2 selected event.                                   |
| 0    | OST1       | R    | 0h    | Latched Status Flag for OST1 Trip Latch<br>0:Reading a 0 indicates that no trip has occurred on OST1.<br>1:Reading a 1 indicates a trip has occurred on the OST1 selected event.                                   |



### 3.7.2.59 EPWM\_TZCLR Register

#### 1 EPWM\_TZCLR Register (Offset = 12Eh) [reset = 0h]

Trip Zone Clear Register.

Return to [Summary Table](#)

**Table 3-988. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 012Eh       |
| EPWM0_G1      | 5004 012Eh       |
| EPWM0_G2      | 5008 012Eh       |
| EPWM0_G3      | 500C 012Eh       |
| EPWM1_G0      | 5000 112Eh       |
| EPWM1_G1      | 5004 112Eh       |
| EPWM1_G2      | 5008 112Eh       |
| EPWM1_G3      | 500C 112Eh       |
| EPWM2_G0      | 5000 212Eh       |
| EPWM2_G1      | 5004 212Eh       |
| EPWM2_G2      | 5008 212Eh       |
| EPWM2_G3      | 500C 212Eh       |
| EPWM3_G0      | 5000 312Eh       |
| EPWM3_G1      | 5004 312Eh       |
| EPWM3_G2      | 5008 312Eh       |
| EPWM3_G3      | 500C 312Eh       |
| EPWM4_G0      | 5000 412Eh       |
| EPWM4_G1      | 5004 412Eh       |
| EPWM4_G2      | 5008 412Eh       |
| EPWM4_G3      | 500C 412Eh       |
| EPWM5_G0      | 5000 512Eh       |
| EPWM5_G1      | 5004 512Eh       |
| EPWM5_G2      | 5008 512Eh       |
| EPWM5_G3      | 500C 512Eh       |
| EPWM6_G0      | 5000 612Eh       |
| EPWM6_G1      | 5004 612Eh       |
| EPWM6_G2      | 5008 612Eh       |
| EPWM6_G3      | 500C 612Eh       |
| EPWM7_G0      | 5000 712Eh       |
| EPWM7_G1      | 5004 712Eh       |
| EPWM7_G2      | 5008 712Eh       |
| EPWM7_G3      | 500C 712Eh       |
| EPWM8_G0      | 5000 812Eh       |
| EPWM8_G1      | 5004 812Eh       |
| EPWM8_G2      | 5008 812Eh       |
| EPWM8_G3      | 500C 812Eh       |
| EPWM9_G0      | 5000 912Eh       |
| EPWM9_G1      | 5004 912Eh       |
| EPWM9_G2      | 5008 912Eh       |

**Table 3-988. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 912Eh       |
| EPWM10_G0     | 5000 A12Eh       |
| EPWM10_G1     | 5004 A12Eh       |
| EPWM10_G2     | 5008 A12Eh       |
| EPWM10_G3     | 500C A12Eh       |
| EPWM11_G0     | 5000 B12Eh       |
| EPWM11_G1     | 5004 B12Eh       |
| EPWM11_G2     | 5008 B12Eh       |
| EPWM11_G3     | 500C B12Eh       |
| EPWM12_G0     | 5000 C12Eh       |
| EPWM12_G1     | 5004 C12Eh       |
| EPWM12_G2     | 5008 C12Eh       |
| EPWM12_G3     | 500C C12Eh       |
| EPWM13_G0     | 5000 D12Eh       |
| EPWM13_G1     | 5004 D12Eh       |
| EPWM13_G2     | 5008 D12Eh       |
| EPWM13_G3     | 500C D12Eh       |
| EPWM14_G0     | 5000 E12Eh       |
| EPWM14_G1     | 5004 E12Eh       |
| EPWM14_G2     | 5008 E12Eh       |
| EPWM14_G3     | 500C E12Eh       |
| EPWM15_G0     | 5000 F12Eh       |
| EPWM15_G1     | 5004 F12Eh       |
| EPWM15_G2     | 5008 F12Eh       |
| EPWM15_G3     | 500C F12Eh       |
| EPWM16_G0     | 5001 012Eh       |
| EPWM16_G1     | 5005 012Eh       |
| EPWM16_G2     | 5009 012Eh       |
| EPWM16_G3     | 500D 012Eh       |
| EPWM17_G0     | 5001 112Eh       |
| EPWM17_G1     | 5005 112Eh       |
| EPWM17_G2     | 5009 112Eh       |
| EPWM17_G3     | 500D 112Eh       |
| EPWM18_G0     | 5001 212Eh       |
| EPWM18_G1     | 5005 212Eh       |
| EPWM18_G2     | 5009 212Eh       |
| EPWM18_G3     | 500D 212Eh       |
| EPWM19_G0     | 5001 312Eh       |
| EPWM19_G1     | 5005 312Eh       |
| EPWM19_G2     | 5009 312Eh       |
| EPWM19_G3     | 500D 312Eh       |
| EPWM20_G0     | 5001 412Eh       |
| EPWM20_G1     | 5005 412Eh       |
| EPWM20_G2     | 5009 412Eh       |
| EPWM20_G3     | 500D 412Eh       |

**Table 3-988. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 512Eh       |
| EPWM21_G1     | 5005 512Eh       |
| EPWM21_G2     | 5009 512Eh       |
| EPWM21_G3     | 500D 512Eh       |
| EPWM22_G0     | 5001 612Eh       |
| EPWM22_G1     | 5005 612Eh       |
| EPWM22_G2     | 5009 612Eh       |
| EPWM22_G3     | 500D 612Eh       |
| EPWM23_G0     | 5001 712Eh       |
| EPWM23_G1     | 5005 712Eh       |
| EPWM23_G2     | 5009 712Eh       |
| EPWM23_G3     | 500D 712Eh       |
| EPWM24_G0     | 5001 812Eh       |
| EPWM24_G1     | 5005 812Eh       |
| EPWM24_G2     | 5009 812Eh       |
| EPWM24_G3     | 500D 812Eh       |
| EPWM25_G0     | 5001 912Eh       |
| EPWM25_G1     | 5005 912Eh       |
| EPWM25_G2     | 5009 912Eh       |
| EPWM25_G3     | 500D 912Eh       |
| EPWM26_G0     | 5001 A12Eh       |
| EPWM26_G1     | 5005 A12Eh       |
| EPWM26_G2     | 5009 A12Eh       |
| EPWM26_G3     | 500D A12Eh       |
| EPWM27_G0     | 5001 B12Eh       |
| EPWM27_G1     | 5005 B12Eh       |
| EPWM27_G2     | 5009 B12Eh       |
| EPWM27_G3     | 500D B12Eh       |
| EPWM28_G0     | 5001 C12Eh       |
| EPWM28_G1     | 5005 C12Eh       |
| EPWM28_G2     | 5009 C12Eh       |
| EPWM28_G3     | 500D C12Eh       |
| EPWM29_G0     | 5001 D12Eh       |
| EPWM29_G1     | 5005 D12Eh       |
| EPWM29_G2     | 5009 D12Eh       |
| EPWM29_G3     | 500D D12Eh       |
| EPWM30_G0     | 5001 E12Eh       |
| EPWM30_G1     | 5005 E12Eh       |
| EPWM30_G2     | 5009 E12Eh       |
| EPWM30_G3     | 500D E12Eh       |
| EPWM31_G0     | 5001 F12Eh       |
| EPWM31_G1     | 5005 F12Eh       |
| EPWM31_G2     | 5009 F12Eh       |
| EPWM31_G3     | 500D F12Eh       |

**Figure 3-310. EPWM\_TZCLR Name Register**

| 15       | 14      | 13         | 12      | 11      | 10     | 9      | 8      |
|----------|---------|------------|---------|---------|--------|--------|--------|
| CBCPULSE |         | RESERVED_1 |         |         |        |        |        |
| R/W      |         | R          |         |         |        |        |        |
| 0h       |         | 0h         |         |         |        |        |        |
| 7        | 6       | 5          | 4       | 3       | 2      | 1      | 0      |
| CAPEVT   | DCBEVT2 | DCBEVT1    | DCAEVT2 | DCAEVT1 | OST    | CBC    | INT    |
| R/W1TS   | R/W1TS  | R/W1TS     | R/W1TS  | R/W1TS  | R/W1TS | R/W1TS | R/W1TS |
| 0h       | 0h      | 0h         | 0h      | 0h      | 0h     | 0h     | 0h     |

**Table 3-990. EPWM\_TZCLR Register Field Descriptions**

| Bit   | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|------------|--------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | CBCPULSE   | R/W    | 0h    | Clear Pulse for Cycle-By-Cycle [CBC] Trip Latch<br>This bit field determines which pulse clears the CBC trip latch.<br>00:CTR = zero pulse clears CBC trip latch. [Same as legacy designs.]<br>01:CTR = PRD pulse clears CBC trip latch.<br>10:CTR = zero or CTR = PRD pulse clears CBC trip latch.<br>11:CBC trip latch is not cleared                                                                                    |
| 13:8  | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 7     | CAPEVT     | R/W1TS | 0h    | Clear Flag for Capture Event<br>0:Writing 0 has no effect. This bit always reads back 0.<br>1:Writing 1 clears the CAPEVT event trip condition.                                                                                                                                                                                                                                                                            |
| 6     | DCBEVT2    | R/W1TS | 0h    | Clear Flag for Digital Compare Output B Event 2<br>0:Writing 0 has no effect. This bit always reads back 0.<br>1:Writing 1 clears the DCBEVT2 event trip condition.                                                                                                                                                                                                                                                        |
| 5     | DCBEVT1    | R/W1TS | 0h    | Clear Flag for Digital Compare Output B Event 1<br>0:Writing 0 has no effect. This bit always reads back 0.<br>1:Writing 1 clears the DCBEVT1 event trip condition.                                                                                                                                                                                                                                                        |
| 4     | DCAEVT2    | R/W1TS | 0h    | Clear Flag for Digital Compare Output A Event 2<br>0:Writing 0 has no effect. This bit always reads back 0.<br>1:Writing 1 clears the DCAEVT2 event trip condition.                                                                                                                                                                                                                                                        |
| 3     | DCAEVT1    | R/W1TS | 0h    | Clear Flag for Digital Compare Output A Event 1<br>0:Writing 0 has no effect. This bit always reads back 0.<br>1:Writing 1 clears the DCAEVT1 event trip condition.                                                                                                                                                                                                                                                        |
| 2     | OST        | R/W1TS | 0h    | Clear Flag for One-Shot Trip [OST] Latch<br>0:Has no effect. Always reads back a 0.<br>1:Clears this Trip [set] condition.                                                                                                                                                                                                                                                                                                 |
| 1     | CBC        | R/W1TS | 0h    | Clear Flag for Cycle-By-Cycle [CBC] Trip Latch<br>0:Has no effect. Always reads back a 0.<br>1:Clears this Trip [set] condition.                                                                                                                                                                                                                                                                                           |
| 0     | INT        | R/W1TS | 0h    | Global Interrupt Clear Flag<br>0:Has no effect. Always reads back a 0.<br>1:Clears the trip-interrupt flag for this EPWM module [TZFLG[INT]].<br>NOTE: No further EPWMx_TZINT VIM interrupts will be generated until the flag is cleared. If the TZFLG[INT] bit is cleared and any of the other flag bits are set, then another interrupt pulse will be generated. Clearing all flag bits will prevent further interrupts. |

### 3.7.2.60 EPWM\_TZCBCCLR Register

#### 1 EPWM\_TZCBCCLR Register (Offset = 130h) [reset = 0h]

Trip Zone CBC Clear Register.

Return to [Summary Table](#)

**Table 3-991. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0130h       |
| EPWM0_G1      | 5004 0130h       |
| EPWM0_G2      | 5008 0130h       |
| EPWM0_G3      | 500C 0130h       |
| EPWM1_G0      | 5000 1130h       |
| EPWM1_G1      | 5004 1130h       |
| EPWM1_G2      | 5008 1130h       |
| EPWM1_G3      | 500C 1130h       |
| EPWM2_G0      | 5000 2130h       |
| EPWM2_G1      | 5004 2130h       |
| EPWM2_G2      | 5008 2130h       |
| EPWM2_G3      | 500C 2130h       |
| EPWM3_G0      | 5000 3130h       |
| EPWM3_G1      | 5004 3130h       |
| EPWM3_G2      | 5008 3130h       |
| EPWM3_G3      | 500C 3130h       |
| EPWM4_G0      | 5000 4130h       |
| EPWM4_G1      | 5004 4130h       |
| EPWM4_G2      | 5008 4130h       |
| EPWM4_G3      | 500C 4130h       |
| EPWM5_G0      | 5000 5130h       |
| EPWM5_G1      | 5004 5130h       |
| EPWM5_G2      | 5008 5130h       |
| EPWM5_G3      | 500C 5130h       |
| EPWM6_G0      | 5000 6130h       |
| EPWM6_G1      | 5004 6130h       |
| EPWM6_G2      | 5008 6130h       |
| EPWM6_G3      | 500C 6130h       |
| EPWM7_G0      | 5000 7130h       |
| EPWM7_G1      | 5004 7130h       |
| EPWM7_G2      | 5008 7130h       |
| EPWM7_G3      | 500C 7130h       |
| EPWM8_G0      | 5000 8130h       |
| EPWM8_G1      | 5004 8130h       |
| EPWM8_G2      | 5008 8130h       |
| EPWM8_G3      | 500C 8130h       |
| EPWM9_G0      | 5000 9130h       |
| EPWM9_G1      | 5004 9130h       |
| EPWM9_G2      | 5008 9130h       |

**Table 3-991. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9130h       |
| EPWM10_G0     | 5000 A130h       |
| EPWM10_G1     | 5004 A130h       |
| EPWM10_G2     | 5008 A130h       |
| EPWM10_G3     | 500C A130h       |
| EPWM11_G0     | 5000 B130h       |
| EPWM11_G1     | 5004 B130h       |
| EPWM11_G2     | 5008 B130h       |
| EPWM11_G3     | 500C B130h       |
| EPWM12_G0     | 5000 C130h       |
| EPWM12_G1     | 5004 C130h       |
| EPWM12_G2     | 5008 C130h       |
| EPWM12_G3     | 500C C130h       |
| EPWM13_G0     | 5000 D130h       |
| EPWM13_G1     | 5004 D130h       |
| EPWM13_G2     | 5008 D130h       |
| EPWM13_G3     | 500C D130h       |
| EPWM14_G0     | 5000 E130h       |
| EPWM14_G1     | 5004 E130h       |
| EPWM14_G2     | 5008 E130h       |
| EPWM14_G3     | 500C E130h       |
| EPWM15_G0     | 5000 F130h       |
| EPWM15_G1     | 5004 F130h       |
| EPWM15_G2     | 5008 F130h       |
| EPWM15_G3     | 500C F130h       |
| EPWM16_G0     | 5001 0130h       |
| EPWM16_G1     | 5005 0130h       |
| EPWM16_G2     | 5009 0130h       |
| EPWM16_G3     | 500D 0130h       |
| EPWM17_G0     | 5001 1130h       |
| EPWM17_G1     | 5005 1130h       |
| EPWM17_G2     | 5009 1130h       |
| EPWM17_G3     | 500D 1130h       |
| EPWM18_G0     | 5001 2130h       |
| EPWM18_G1     | 5005 2130h       |
| EPWM18_G2     | 5009 2130h       |
| EPWM18_G3     | 500D 2130h       |
| EPWM19_G0     | 5001 3130h       |
| EPWM19_G1     | 5005 3130h       |
| EPWM19_G2     | 5009 3130h       |
| EPWM19_G3     | 500D 3130h       |
| EPWM20_G0     | 5001 4130h       |
| EPWM20_G1     | 5005 4130h       |
| EPWM20_G2     | 5009 4130h       |
| EPWM20_G3     | 500D 4130h       |

**Table 3-991. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5130h       |
| EPWM21_G1     | 5005 5130h       |
| EPWM21_G2     | 5009 5130h       |
| EPWM21_G3     | 500D 5130h       |
| EPWM22_G0     | 5001 6130h       |
| EPWM22_G1     | 5005 6130h       |
| EPWM22_G2     | 5009 6130h       |
| EPWM22_G3     | 500D 6130h       |
| EPWM23_G0     | 5001 7130h       |
| EPWM23_G1     | 5005 7130h       |
| EPWM23_G2     | 5009 7130h       |
| EPWM23_G3     | 500D 7130h       |
| EPWM24_G0     | 5001 8130h       |
| EPWM24_G1     | 5005 8130h       |
| EPWM24_G2     | 5009 8130h       |
| EPWM24_G3     | 500D 8130h       |
| EPWM25_G0     | 5001 9130h       |
| EPWM25_G1     | 5005 9130h       |
| EPWM25_G2     | 5009 9130h       |
| EPWM25_G3     | 500D 9130h       |
| EPWM26_G0     | 5001 A130h       |
| EPWM26_G1     | 5005 A130h       |
| EPWM26_G2     | 5009 A130h       |
| EPWM26_G3     | 500D A130h       |
| EPWM27_G0     | 5001 B130h       |
| EPWM27_G1     | 5005 B130h       |
| EPWM27_G2     | 5009 B130h       |
| EPWM27_G3     | 500D B130h       |
| EPWM28_G0     | 5001 C130h       |
| EPWM28_G1     | 5005 C130h       |
| EPWM28_G2     | 5009 C130h       |
| EPWM28_G3     | 500D C130h       |
| EPWM29_G0     | 5001 D130h       |
| EPWM29_G1     | 5005 D130h       |
| EPWM29_G2     | 5009 D130h       |
| EPWM29_G3     | 500D D130h       |
| EPWM30_G0     | 5001 E130h       |
| EPWM30_G1     | 5005 E130h       |
| EPWM30_G2     | 5009 E130h       |
| EPWM30_G3     | 500D E130h       |
| EPWM31_G0     | 5001 F130h       |
| EPWM31_G1     | 5005 F130h       |
| EPWM31_G2     | 5009 F130h       |
| EPWM31_G3     | 500D F130h       |

**Figure 3-311. EPWM\_TZCBCCLR Name Register**

| 15         | 14      | 13     | 12     | 11     | 10     | 9      | 8      |
|------------|---------|--------|--------|--------|--------|--------|--------|
| RESERVED_1 |         |        |        |        |        |        | CAPEVT |
| R          |         |        |        |        |        |        | R/W1TS |
| 0h         |         |        |        |        |        |        | 0h     |
| 7          | 6       | 5      | 4      | 3      | 2      | 1      | 0      |
| DCBEVT2    | DCAEVT2 | CBC6   | CBC5   | CBC4   | CBC3   | CBC2   | CBC1   |
| R/W1TS     | R/W1TS  | R/W1TS | R/W1TS | R/W1TS | R/W1TS | R/W1TS | R/W1TS |
| 0h         | 0h      | 0h     | 0h     | 0h     | 0h     | 0h     | 0h     |

**Table 3-993. EPWM\_TZCBCCLR Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                             |
|------|------------|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:9 | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                |
| 8    | CAPEVT     | R/W1TS | 0h    | Clear Flag for CAPEVT selected for CBC<br>0:Writing a 0 has no effect.<br>1:Writing a 1 will clear the TZCBCFLG[CAPEVT] bit.                            |
| 7    | DCBEVT2    | R/W1TS | 0h    | Clear Flag for Digital Compare Output B Event 2 selected for CBC<br>0:Writing a 0 has no effect.<br>1:Writing a 1 will clear the TZCBCFLG[DCBEVT2] bit. |
| 6    | DCAEVT2    | R/W1TS | 0h    | Clear Flag for Digital Compare Output A Event 2 selected for CBC<br>0:Writing a 0 has no effect.<br>1:Writing a 1 will clear the TZCBCFLG[DCAEVT2] bit. |
| 5    | CBC6       | R/W1TS | 0h    | Clear Flag for Cycle-By-Cycle [CBC6] Trip Latch<br>0:Writing a 0 has no effect.<br>1:Writing a 1 will clear the TZCBCFLG[CBC6] bit.                     |
| 4    | CBC5       | R/W1TS | 0h    | Clear Flag for Cycle-By-Cycle [CBC5] Trip Latch<br>0:Writing a 0 has no effect.<br>1:Writing a 1 will clear the TZCBCFLG[CBC5] bit.                     |
| 3    | CBC4       | R/W1TS | 0h    | Clear Flag for Cycle-By-Cycle [CBC4] Trip Latch<br>0:Writing a 0 has no effect.<br>1:Writing a 1 will clear the TZCBCFLG[CBC4] bit.                     |
| 2    | CBC3       | R/W1TS | 0h    | Clear Flag for Cycle-By-Cycle [CBC3] Trip Latch<br>0:Writing a 0 has no effect.<br>1:Writing a 1 will clear the TZCBCFLG[CBC3] bit.                     |
| 1    | CBC2       | R/W1TS | 0h    | Clear Flag for Cycle-By-Cycle [CBC2] Trip Latch<br>0:Writing a 0 has no effect.<br>1:Writing a 1 will clear the TZCBCFLG[CBC2] bit.                     |
| 0    | CBC1       | R/W1TS | 0h    | Clear Flag for Cycle-By-Cycle [CBC1] Trip Latch<br>0:Writing a 0 has no effect.<br>1:Writing a 1 will clear the TZCBCFLG[CBC1] bit.                     |



### 3.7.2.61 EPWM\_TZOSTCLR Register

#### 1 EPWM\_TZOSTCLR Register (Offset = 132h) [reset = 0h]

Trip Zone OST Clear Register.

Return to [Summary Table](#)

**Table 3-994. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0132h       |
| EPWM0_G1      | 5004 0132h       |
| EPWM0_G2      | 5008 0132h       |
| EPWM0_G3      | 500C 0132h       |
| EPWM1_G0      | 5000 1132h       |
| EPWM1_G1      | 5004 1132h       |
| EPWM1_G2      | 5008 1132h       |
| EPWM1_G3      | 500C 1132h       |
| EPWM2_G0      | 5000 2132h       |
| EPWM2_G1      | 5004 2132h       |
| EPWM2_G2      | 5008 2132h       |
| EPWM2_G3      | 500C 2132h       |
| EPWM3_G0      | 5000 3132h       |
| EPWM3_G1      | 5004 3132h       |
| EPWM3_G2      | 5008 3132h       |
| EPWM3_G3      | 500C 3132h       |
| EPWM4_G0      | 5000 4132h       |
| EPWM4_G1      | 5004 4132h       |
| EPWM4_G2      | 5008 4132h       |
| EPWM4_G3      | 500C 4132h       |
| EPWM5_G0      | 5000 5132h       |
| EPWM5_G1      | 5004 5132h       |
| EPWM5_G2      | 5008 5132h       |
| EPWM5_G3      | 500C 5132h       |
| EPWM6_G0      | 5000 6132h       |
| EPWM6_G1      | 5004 6132h       |
| EPWM6_G2      | 5008 6132h       |
| EPWM6_G3      | 500C 6132h       |
| EPWM7_G0      | 5000 7132h       |
| EPWM7_G1      | 5004 7132h       |
| EPWM7_G2      | 5008 7132h       |
| EPWM7_G3      | 500C 7132h       |
| EPWM8_G0      | 5000 8132h       |
| EPWM8_G1      | 5004 8132h       |
| EPWM8_G2      | 5008 8132h       |
| EPWM8_G3      | 500C 8132h       |
| EPWM9_G0      | 5000 9132h       |
| EPWM9_G1      | 5004 9132h       |
| EPWM9_G2      | 5008 9132h       |

**Table 3-994. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9132h       |
| EPWM10_G0     | 5000 A132h       |
| EPWM10_G1     | 5004 A132h       |
| EPWM10_G2     | 5008 A132h       |
| EPWM10_G3     | 500C A132h       |
| EPWM11_G0     | 5000 B132h       |
| EPWM11_G1     | 5004 B132h       |
| EPWM11_G2     | 5008 B132h       |
| EPWM11_G3     | 500C B132h       |
| EPWM12_G0     | 5000 C132h       |
| EPWM12_G1     | 5004 C132h       |
| EPWM12_G2     | 5008 C132h       |
| EPWM12_G3     | 500C C132h       |
| EPWM13_G0     | 5000 D132h       |
| EPWM13_G1     | 5004 D132h       |
| EPWM13_G2     | 5008 D132h       |
| EPWM13_G3     | 500C D132h       |
| EPWM14_G0     | 5000 E132h       |
| EPWM14_G1     | 5004 E132h       |
| EPWM14_G2     | 5008 E132h       |
| EPWM14_G3     | 500C E132h       |
| EPWM15_G0     | 5000 F132h       |
| EPWM15_G1     | 5004 F132h       |
| EPWM15_G2     | 5008 F132h       |
| EPWM15_G3     | 500C F132h       |
| EPWM16_G0     | 5001 0132h       |
| EPWM16_G1     | 5005 0132h       |
| EPWM16_G2     | 5009 0132h       |
| EPWM16_G3     | 500D 0132h       |
| EPWM17_G0     | 5001 1132h       |
| EPWM17_G1     | 5005 1132h       |
| EPWM17_G2     | 5009 1132h       |
| EPWM17_G3     | 500D 1132h       |
| EPWM18_G0     | 5001 2132h       |
| EPWM18_G1     | 5005 2132h       |
| EPWM18_G2     | 5009 2132h       |
| EPWM18_G3     | 500D 2132h       |
| EPWM19_G0     | 5001 3132h       |
| EPWM19_G1     | 5005 3132h       |
| EPWM19_G2     | 5009 3132h       |
| EPWM19_G3     | 500D 3132h       |
| EPWM20_G0     | 5001 4132h       |
| EPWM20_G1     | 5005 4132h       |
| EPWM20_G2     | 5009 4132h       |
| EPWM20_G3     | 500D 4132h       |

**Table 3-994. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5132h       |
| EPWM21_G1     | 5005 5132h       |
| EPWM21_G2     | 5009 5132h       |
| EPWM21_G3     | 500D 5132h       |
| EPWM22_G0     | 5001 6132h       |
| EPWM22_G1     | 5005 6132h       |
| EPWM22_G2     | 5009 6132h       |
| EPWM22_G3     | 500D 6132h       |
| EPWM23_G0     | 5001 7132h       |
| EPWM23_G1     | 5005 7132h       |
| EPWM23_G2     | 5009 7132h       |
| EPWM23_G3     | 500D 7132h       |
| EPWM24_G0     | 5001 8132h       |
| EPWM24_G1     | 5005 8132h       |
| EPWM24_G2     | 5009 8132h       |
| EPWM24_G3     | 500D 8132h       |
| EPWM25_G0     | 5001 9132h       |
| EPWM25_G1     | 5005 9132h       |
| EPWM25_G2     | 5009 9132h       |
| EPWM25_G3     | 500D 9132h       |
| EPWM26_G0     | 5001 A132h       |
| EPWM26_G1     | 5005 A132h       |
| EPWM26_G2     | 5009 A132h       |
| EPWM26_G3     | 500D A132h       |
| EPWM27_G0     | 5001 B132h       |
| EPWM27_G1     | 5005 B132h       |
| EPWM27_G2     | 5009 B132h       |
| EPWM27_G3     | 500D B132h       |
| EPWM28_G0     | 5001 C132h       |
| EPWM28_G1     | 5005 C132h       |
| EPWM28_G2     | 5009 C132h       |
| EPWM28_G3     | 500D C132h       |
| EPWM29_G0     | 5001 D132h       |
| EPWM29_G1     | 5005 D132h       |
| EPWM29_G2     | 5009 D132h       |
| EPWM29_G3     | 500D D132h       |
| EPWM30_G0     | 5001 E132h       |
| EPWM30_G1     | 5005 E132h       |
| EPWM30_G2     | 5009 E132h       |
| EPWM30_G3     | 500D E132h       |
| EPWM31_G0     | 5001 F132h       |
| EPWM31_G1     | 5005 F132h       |
| EPWM31_G2     | 5009 F132h       |
| EPWM31_G3     | 500D F132h       |

**Figure 3-312. EPWM\_TZOSTCLR Name Register**

| 15         | 14      | 13     | 12     | 11     | 10     | 9      | 8      |
|------------|---------|--------|--------|--------|--------|--------|--------|
| RESERVED_1 |         |        |        |        |        |        | CAPEVT |
| R          |         |        |        |        |        |        | R/W1TS |
| 0h         |         |        |        |        |        |        | 0h     |
| 7          | 6       | 5      | 4      | 3      | 2      | 1      | 0      |
| DCBEVT1    | DCAEVT1 | OST6   | OST5   | OST4   | OST3   | OST2   | OST1   |
| R/W1TS     | R/W1TS  | R/W1TS | R/W1TS | R/W1TS | R/W1TS | R/W1TS | R/W1TS |
| 0h         | 0h      | 0h     | 0h     | 0h     | 0h     | 0h     | 0h     |

**Table 3-996. EPWM\_TZOSTCLR Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                             |
|------|------------|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:9 | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                |
| 8    | CAPEVT     | R/W1TS | 0h    | Clear Flag for CAPEVT selected for OST<br>0:Writing a 0 has no effect.<br>1:Writing a 1 will clear the TZOSTFLG[CAPEVT] bit.                            |
| 7    | DCBEVT1    | R/W1TS | 0h    | Clear Flag for Digital Compare Output B Event 1 selected for OST<br>0:Writing a 0 has no effect.<br>1:Writing a 1 will clear the TZOSTFLG[DCBEVT1] bit. |
| 6    | DCAEVT1    | R/W1TS | 0h    | Clear Flag for Digital Compare Output A Event 1 selected for OST<br>0:Writing a 0 has no effect.<br>1:Writing a 1 will clear the TZOSTFLG[DCAEVT1] bit. |
| 5    | OST6       | R/W1TS | 0h    | Clear Flag for Oneshot [OST6] Trip Latch<br>0:Writing a 0 has no effect.<br>1:Writing a 1 will clear the TZOSTFLG[OST6] bit.                            |
| 4    | OST5       | R/W1TS | 0h    | Clear Flag for Oneshot [OST5] Trip Latch<br>0:Writing a 0 has no effect.<br>1:Writing a 1 will clear the TZOSTFLG[OST5] bit.                            |
| 3    | OST4       | R/W1TS | 0h    | Clear Flag for Oneshot [OST4] Trip Latch<br>0:Writing a 0 has no effect.<br>1:Writing a 1 will clear the TZOSTFLG[OST4] bit.                            |
| 2    | OST3       | R/W1TS | 0h    | Clear Flag for Oneshot [OST3] Trip Latch<br>0:Writing a 0 has no effect.<br>1:Writing a 1 will clear the TZOSTFLG[OST3] bit.                            |
| 1    | OST2       | R/W1TS | 0h    | Clear Flag for Oneshot [OST2] Trip Latch<br>0:Writing a 0 has no effect.<br>1:Writing a 1 will clear the TZOSTFLG[OST2] bit.                            |
| 0    | OST1       | R/W1TS | 0h    | Clear Flag for Oneshot [OST1] Trip Latch<br>0:Writing a 0 has no effect.<br>1:Writing a 1 will clear the TZOSTFLG[OST1] bit.                            |

### 3.7.2.62 EPWM\_TZFRC Register

#### 1 EPWM\_TZFRC Register (Offset = 136h) [reset = 0h]

Trip Zone Force Register.

Return to [Summary Table](#)

**Table 3-997. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0136h       |
| EPWM0_G1      | 5004 0136h       |
| EPWM0_G2      | 5008 0136h       |
| EPWM0_G3      | 500C 0136h       |
| EPWM1_G0      | 5000 1136h       |
| EPWM1_G1      | 5004 1136h       |
| EPWM1_G2      | 5008 1136h       |
| EPWM1_G3      | 500C 1136h       |
| EPWM2_G0      | 5000 2136h       |
| EPWM2_G1      | 5004 2136h       |
| EPWM2_G2      | 5008 2136h       |
| EPWM2_G3      | 500C 2136h       |
| EPWM3_G0      | 5000 3136h       |
| EPWM3_G1      | 5004 3136h       |
| EPWM3_G2      | 5008 3136h       |
| EPWM3_G3      | 500C 3136h       |
| EPWM4_G0      | 5000 4136h       |
| EPWM4_G1      | 5004 4136h       |
| EPWM4_G2      | 5008 4136h       |
| EPWM4_G3      | 500C 4136h       |
| EPWM5_G0      | 5000 5136h       |
| EPWM5_G1      | 5004 5136h       |
| EPWM5_G2      | 5008 5136h       |
| EPWM5_G3      | 500C 5136h       |
| EPWM6_G0      | 5000 6136h       |
| EPWM6_G1      | 5004 6136h       |
| EPWM6_G2      | 5008 6136h       |
| EPWM6_G3      | 500C 6136h       |
| EPWM7_G0      | 5000 7136h       |
| EPWM7_G1      | 5004 7136h       |
| EPWM7_G2      | 5008 7136h       |
| EPWM7_G3      | 500C 7136h       |
| EPWM8_G0      | 5000 8136h       |
| EPWM8_G1      | 5004 8136h       |
| EPWM8_G2      | 5008 8136h       |
| EPWM8_G3      | 500C 8136h       |
| EPWM9_G0      | 5000 9136h       |
| EPWM9_G1      | 5004 9136h       |
| EPWM9_G2      | 5008 9136h       |

**Table 3-997. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9136h       |
| EPWM10_G0     | 5000 A136h       |
| EPWM10_G1     | 5004 A136h       |
| EPWM10_G2     | 5008 A136h       |
| EPWM10_G3     | 500C A136h       |
| EPWM11_G0     | 5000 B136h       |
| EPWM11_G1     | 5004 B136h       |
| EPWM11_G2     | 5008 B136h       |
| EPWM11_G3     | 500C B136h       |
| EPWM12_G0     | 5000 C136h       |
| EPWM12_G1     | 5004 C136h       |
| EPWM12_G2     | 5008 C136h       |
| EPWM12_G3     | 500C C136h       |
| EPWM13_G0     | 5000 D136h       |
| EPWM13_G1     | 5004 D136h       |
| EPWM13_G2     | 5008 D136h       |
| EPWM13_G3     | 500C D136h       |
| EPWM14_G0     | 5000 E136h       |
| EPWM14_G1     | 5004 E136h       |
| EPWM14_G2     | 5008 E136h       |
| EPWM14_G3     | 500C E136h       |
| EPWM15_G0     | 5000 F136h       |
| EPWM15_G1     | 5004 F136h       |
| EPWM15_G2     | 5008 F136h       |
| EPWM15_G3     | 500C F136h       |
| EPWM16_G0     | 5001 0136h       |
| EPWM16_G1     | 5005 0136h       |
| EPWM16_G2     | 5009 0136h       |
| EPWM16_G3     | 500D 0136h       |
| EPWM17_G0     | 5001 1136h       |
| EPWM17_G1     | 5005 1136h       |
| EPWM17_G2     | 5009 1136h       |
| EPWM17_G3     | 500D 1136h       |
| EPWM18_G0     | 5001 2136h       |
| EPWM18_G1     | 5005 2136h       |
| EPWM18_G2     | 5009 2136h       |
| EPWM18_G3     | 500D 2136h       |
| EPWM19_G0     | 5001 3136h       |
| EPWM19_G1     | 5005 3136h       |
| EPWM19_G2     | 5009 3136h       |
| EPWM19_G3     | 500D 3136h       |
| EPWM20_G0     | 5001 4136h       |
| EPWM20_G1     | 5005 4136h       |
| EPWM20_G2     | 5009 4136h       |
| EPWM20_G3     | 500D 4136h       |

**Table 3-997. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5136h       |
| EPWM21_G1     | 5005 5136h       |
| EPWM21_G2     | 5009 5136h       |
| EPWM21_G3     | 500D 5136h       |
| EPWM22_G0     | 5001 6136h       |
| EPWM22_G1     | 5005 6136h       |
| EPWM22_G2     | 5009 6136h       |
| EPWM22_G3     | 500D 6136h       |
| EPWM23_G0     | 5001 7136h       |
| EPWM23_G1     | 5005 7136h       |
| EPWM23_G2     | 5009 7136h       |
| EPWM23_G3     | 500D 7136h       |
| EPWM24_G0     | 5001 8136h       |
| EPWM24_G1     | 5005 8136h       |
| EPWM24_G2     | 5009 8136h       |
| EPWM24_G3     | 500D 8136h       |
| EPWM25_G0     | 5001 9136h       |
| EPWM25_G1     | 5005 9136h       |
| EPWM25_G2     | 5009 9136h       |
| EPWM25_G3     | 500D 9136h       |
| EPWM26_G0     | 5001 A136h       |
| EPWM26_G1     | 5005 A136h       |
| EPWM26_G2     | 5009 A136h       |
| EPWM26_G3     | 500D A136h       |
| EPWM27_G0     | 5001 B136h       |
| EPWM27_G1     | 5005 B136h       |
| EPWM27_G2     | 5009 B136h       |
| EPWM27_G3     | 500D B136h       |
| EPWM28_G0     | 5001 C136h       |
| EPWM28_G1     | 5005 C136h       |
| EPWM28_G2     | 5009 C136h       |
| EPWM28_G3     | 500D C136h       |
| EPWM29_G0     | 5001 D136h       |
| EPWM29_G1     | 5005 D136h       |
| EPWM29_G2     | 5009 D136h       |
| EPWM29_G3     | 500D D136h       |
| EPWM30_G0     | 5001 E136h       |
| EPWM30_G1     | 5005 E136h       |
| EPWM30_G2     | 5009 E136h       |
| EPWM30_G3     | 500D E136h       |
| EPWM31_G0     | 5001 F136h       |
| EPWM31_G1     | 5005 F136h       |
| EPWM31_G2     | 5009 F136h       |
| EPWM31_G3     | 500D F136h       |

**Figure 3-313. EPWM\_TZFRC Name Register**

| 15         | 14      | 13      | 12      | 11      | 10     | 9      | 8          |
|------------|---------|---------|---------|---------|--------|--------|------------|
| RESERVED_2 |         |         |         |         |        |        |            |
| R          |         |         |         |         |        |        |            |
| 0h         |         |         |         |         |        |        |            |
| 7          | 6       | 5       | 4       | 3       | 2      | 1      | 0          |
| CAPEVT     | DCBEVT2 | DCBEVT1 | DCAEVT2 | DCAEVT1 | OST    | CBC    | RESERVED_1 |
| R/W1TS     | R/W1TS  | R/W1TS  | R/W1TS  | R/W1TS  | R/W1TS | R/W1TS | R          |
| 0h         | 0h      | 0h      | 0h      | 0h      | 0h     | 0h     | 0h         |

**Table 3-999. EPWM\_TZFRC Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                                                         |
|------|------------|--------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED_2 | R      | 0h    | Reserved                                                                                                                                                                                            |
| 7    | CAPEVT     | R/W1TS | 0h    | Force Flag for Capture Event Output<br>0:Writing 0 has no effect. This bit always reads back 0.<br>1:Writing 1 forces the CAPEVT event trip condition and sets the TZFLG[CAPEVT] bit.               |
| 6    | DCBEVT2    | R/W1TS | 0h    | Force Flag for Digital Compare Output B Event 2<br>0:Writing 0 has no effect. This bit always reads back 0.<br>1:Writing 1 forces the DCBEVT2 event trip condition and sets the TZFLG[DCBEVT2] bit. |
| 5    | DCBEVT1    | R/W1TS | 0h    | Force Flag for Digital Compare Output B Event 1<br>0:Writing 0 has no effect. This bit always reads back 0.<br>1:Writing 1 forces the DCBEVT1 event trip condition and sets the TZFLG[DCBEVT1] bit. |
| 4    | DCAEVT2    | R/W1TS | 0h    | Force Flag for Digital Compare Output A Event 2<br>0:Writing 0 has no effect. This bit always reads back 0.<br>1:Writing 1 forces the DCAEVT2 event trip condition and sets the TZFLG[DCAEVT2] bit. |
| 3    | DCAEVT1    | R/W1TS | 0h    | Force Flag for Digital Compare Output A Event 1<br>0:Writing 0 has no effect. This bit always reads back 0.<br>1:Writing 1 forces the DCAEVT1 event trip condition and sets the TZFLG[DCAEVT1] bit. |
| 2    | OST        | R/W1TS | 0h    | Force a One-Shot Trip Event via Software<br>0:Writing of 0 is ignored. Always reads back a 0.<br>1:Forces a one-shot trip event and sets the TZFLG[OST] bit.                                        |
| 1    | CBC        | R/W1TS | 0h    | Force a Cycle-by-Cycle Trip Event via Software<br>0:Writing of 0 is ignored. Always reads back a 0.<br>1:Forces a cycle-by-cycle trip event and sets the TZFLG[CBC] bit.                            |
| 0    | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                            |



### 3.7.2.63 EPWM\_TZTRIPOUTSEL Register

#### 1 EPWM\_TZTRIPOUTSEL Register (Offset = 13Ah) [reset = 0h]

Trip Zone Force Register.

Return to [Summary Table](#)

**Table 3-1000. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 013Ah       |
| EPWM0_G1      | 5004 013Ah       |
| EPWM0_G2      | 5008 013Ah       |
| EPWM0_G3      | 500C 013Ah       |
| EPWM1_G0      | 5000 113Ah       |
| EPWM1_G1      | 5004 113Ah       |
| EPWM1_G2      | 5008 113Ah       |
| EPWM1_G3      | 500C 113Ah       |
| EPWM2_G0      | 5000 213Ah       |
| EPWM2_G1      | 5004 213Ah       |
| EPWM2_G2      | 5008 213Ah       |
| EPWM2_G3      | 500C 213Ah       |
| EPWM3_G0      | 5000 313Ah       |
| EPWM3_G1      | 5004 313Ah       |
| EPWM3_G2      | 5008 313Ah       |
| EPWM3_G3      | 500C 313Ah       |
| EPWM4_G0      | 5000 413Ah       |
| EPWM4_G1      | 5004 413Ah       |
| EPWM4_G2      | 5008 413Ah       |
| EPWM4_G3      | 500C 413Ah       |
| EPWM5_G0      | 5000 513Ah       |
| EPWM5_G1      | 5004 513Ah       |
| EPWM5_G2      | 5008 513Ah       |
| EPWM5_G3      | 500C 513Ah       |
| EPWM6_G0      | 5000 613Ah       |
| EPWM6_G1      | 5004 613Ah       |
| EPWM6_G2      | 5008 613Ah       |
| EPWM6_G3      | 500C 613Ah       |
| EPWM7_G0      | 5000 713Ah       |
| EPWM7_G1      | 5004 713Ah       |
| EPWM7_G2      | 5008 713Ah       |
| EPWM7_G3      | 500C 713Ah       |
| EPWM8_G0      | 5000 813Ah       |
| EPWM8_G1      | 5004 813Ah       |
| EPWM8_G2      | 5008 813Ah       |
| EPWM8_G3      | 500C 813Ah       |
| EPWM9_G0      | 5000 913Ah       |
| EPWM9_G1      | 5004 913Ah       |
| EPWM9_G2      | 5008 913Ah       |

**Table 3-1000. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 913Ah       |
| EPWM10_G0     | 5000 A13Ah       |
| EPWM10_G1     | 5004 A13Ah       |
| EPWM10_G2     | 5008 A13Ah       |
| EPWM10_G3     | 500C A13Ah       |
| EPWM11_G0     | 5000 B13Ah       |
| EPWM11_G1     | 5004 B13Ah       |
| EPWM11_G2     | 5008 B13Ah       |
| EPWM11_G3     | 500C B13Ah       |
| EPWM12_G0     | 5000 C13Ah       |
| EPWM12_G1     | 5004 C13Ah       |
| EPWM12_G2     | 5008 C13Ah       |
| EPWM12_G3     | 500C C13Ah       |
| EPWM13_G0     | 5000 D13Ah       |
| EPWM13_G1     | 5004 D13Ah       |
| EPWM13_G2     | 5008 D13Ah       |
| EPWM13_G3     | 500C D13Ah       |
| EPWM14_G0     | 5000 E13Ah       |
| EPWM14_G1     | 5004 E13Ah       |
| EPWM14_G2     | 5008 E13Ah       |
| EPWM14_G3     | 500C E13Ah       |
| EPWM15_G0     | 5000 F13Ah       |
| EPWM15_G1     | 5004 F13Ah       |
| EPWM15_G2     | 5008 F13Ah       |
| EPWM15_G3     | 500C F13Ah       |
| EPWM16_G0     | 5001 013Ah       |
| EPWM16_G1     | 5005 013Ah       |
| EPWM16_G2     | 5009 013Ah       |
| EPWM16_G3     | 500D 013Ah       |
| EPWM17_G0     | 5001 113Ah       |
| EPWM17_G1     | 5005 113Ah       |
| EPWM17_G2     | 5009 113Ah       |
| EPWM17_G3     | 500D 113Ah       |
| EPWM18_G0     | 5001 213Ah       |
| EPWM18_G1     | 5005 213Ah       |
| EPWM18_G2     | 5009 213Ah       |
| EPWM18_G3     | 500D 213Ah       |
| EPWM19_G0     | 5001 313Ah       |
| EPWM19_G1     | 5005 313Ah       |
| EPWM19_G2     | 5009 313Ah       |
| EPWM19_G3     | 500D 313Ah       |
| EPWM20_G0     | 5001 413Ah       |
| EPWM20_G1     | 5005 413Ah       |
| EPWM20_G2     | 5009 413Ah       |
| EPWM20_G3     | 500D 413Ah       |

**Table 3-1000. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 513Ah       |
| EPWM21_G1     | 5005 513Ah       |
| EPWM21_G2     | 5009 513Ah       |
| EPWM21_G3     | 500D 513Ah       |
| EPWM22_G0     | 5001 613Ah       |
| EPWM22_G1     | 5005 613Ah       |
| EPWM22_G2     | 5009 613Ah       |
| EPWM22_G3     | 500D 613Ah       |
| EPWM23_G0     | 5001 713Ah       |
| EPWM23_G1     | 5005 713Ah       |
| EPWM23_G2     | 5009 713Ah       |
| EPWM23_G3     | 500D 713Ah       |
| EPWM24_G0     | 5001 813Ah       |
| EPWM24_G1     | 5005 813Ah       |
| EPWM24_G2     | 5009 813Ah       |
| EPWM24_G3     | 500D 813Ah       |
| EPWM25_G0     | 5001 913Ah       |
| EPWM25_G1     | 5005 913Ah       |
| EPWM25_G2     | 5009 913Ah       |
| EPWM25_G3     | 500D 913Ah       |
| EPWM26_G0     | 5001 A13Ah       |
| EPWM26_G1     | 5005 A13Ah       |
| EPWM26_G2     | 5009 A13Ah       |
| EPWM26_G3     | 500D A13Ah       |
| EPWM27_G0     | 5001 B13Ah       |
| EPWM27_G1     | 5005 B13Ah       |
| EPWM27_G2     | 5009 B13Ah       |
| EPWM27_G3     | 500D B13Ah       |
| EPWM28_G0     | 5001 C13Ah       |
| EPWM28_G1     | 5005 C13Ah       |
| EPWM28_G2     | 5009 C13Ah       |
| EPWM28_G3     | 500D C13Ah       |
| EPWM29_G0     | 5001 D13Ah       |
| EPWM29_G1     | 5005 D13Ah       |
| EPWM29_G2     | 5009 D13Ah       |
| EPWM29_G3     | 500D D13Ah       |
| EPWM30_G0     | 5001 E13Ah       |
| EPWM30_G1     | 5005 E13Ah       |
| EPWM30_G2     | 5009 E13Ah       |
| EPWM30_G3     | 500D E13Ah       |
| EPWM31_G0     | 5001 F13Ah       |
| EPWM31_G1     | 5005 F13Ah       |
| EPWM31_G2     | 5009 F13Ah       |
| EPWM31_G3     | 500D F13Ah       |

**Figure 3-314. EPWM\_TZTRIPOUTSEL Name Register**

| 15         | 14  | 13  | 12     | 11      | 10      | 9       | 8       |
|------------|-----|-----|--------|---------|---------|---------|---------|
| RESERVED_1 |     |     | CAPEVT | DCBEVT2 | DCBEVT1 | DCAEVT2 | DCAEVT1 |
| R          |     |     | R/W    | R/W     | R/W     | R/W     | R/W     |
| 0h         |     |     | 0h     | 0h      | 0h      | 0h      | 0h      |
| 7          | 6   | 5   | 4      | 3       | 2       | 1       | 0       |
| TZ6        | TZ5 | TZ4 | TZ3    | TZ2     | TZ1     | CBC     | OST     |
| R/W        | R/W | R/W | R/W    | R/W     | R/W     | R/W     | R/W     |
| 0h         | 0h  | 0h  | 0h     | 0h      | 0h      | 0h      | 0h      |

**Table 3-1002. EPWM\_TZTRIPOUTSEL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                 |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                    |
| 12    | CAPEVT     | R/W  | 0h    | CAPEVT Select<br>0:Disable TZ6 as a TRIPOUT source for this EPWM module<br>1:Enable TZ6 as a TRIPOUT source for this EPWM module            |
| 11    | DCBEVT2    | R/W  | 0h    | DCBEVT2 Select<br>0:Disable TZ6 as a TRIPOUT source for this EPWM module<br>1:Enable TZ6 as a TRIPOUT source for this EPWM module           |
| 10    | DCBEVT1    | R/W  | 0h    | DCBEVT1 Select<br>0:Disable TZ6 as a TRIPOUT source for this EPWM module<br>1:Enable TZ6 as a TRIPOUT source for this EPWM module           |
| 9     | DCAEVT2    | R/W  | 0h    | DCAEVT2 Select<br>0:Disable TZ6 as a TRIPOUT source for this EPWM module<br>1:Enable TZ6 as a TRIPOUT source for this EPWM module           |
| 8     | DCAEVT1    | R/W  | 0h    | DCAEVT1 Select<br>0:Disable TZ6 as a TRIPOUT source for this EPWM module<br>1:Enable TZ6 as a TRIPOUT source for this EPWM module           |
| 7     | TZ6        | R/W  | 0h    | Trip-Zone 6 [TZ6] Select<br>0:Disable TZ6 as a TRIPOUT source for this EPWM module<br>1:Enable TZ6 as a TRIPOUT source for this EPWM module |
| 6     | TZ5        | R/W  | 0h    | Trip-Zone 5 [TZ5] Select<br>0:Disable TZ5 as a TRIPOUT source for this EPWM module<br>1:Enable TZ5 as a TRIPOUT source for this EPWM module |
| 5     | TZ4        | R/W  | 0h    | Trip-Zone 4 [TZ4] Select<br>0:Disable TZ4 as a TRIPOUT source for this EPWM module<br>1:Enable TZ4 as a TRIPOUT source for this EPWM module |
| 4     | TZ3        | R/W  | 0h    | Trip-Zone 3 [TZ3] Select<br>0:Disable TZ3 as a TRIPOUT source for this EPWM module<br>1:Enable TZ3 as a TRIPOUT source for this EPWM module |
| 3     | TZ2        | R/W  | 0h    | Trip-Zone 2 [TZ2] Select<br>0:Disable TZ2 as a TRIPOUT source for this EPWM module<br>1:Enable TZ2 as a TRIPOUT source for this EPWM module |
| 2     | TZ1        | R/W  | 0h    | Trip-Zone 1 [TZ1] Select<br>0:Disable TZ1 as a TRIPOUT source for this EPWM module<br>1:Enable TZ1 as a TRIPOUT source for this EPWM module |
| 1     | CBC        | R/W  | 0h    | CBC Select<br>0:Disable TZ1 as a TRIPOUT source for this EPWM module<br>1:Enable TZ1 as a TRIPOUT source for this EPWM module               |
| 0     | OST        | R/W  | 0h    | OST Select<br>0:Disable TZ1 as a TRIPOUT source for this EPWM module<br>1:Enable TZ1 as a TRIPOUT source for this EPWM module               |

### 3.7.2.64 EPWM\_ETSEL Register

#### 1 EPWM\_ETSEL Register (Offset = 148h) [reset = 0h]

Event Trigger Selection Register.

Return to [Summary Table](#)

**Table 3-1003. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0148h       |
| EPWM0_G1      | 5004 0148h       |
| EPWM0_G2      | 5008 0148h       |
| EPWM0_G3      | 500C 0148h       |
| EPWM1_G0      | 5000 1148h       |
| EPWM1_G1      | 5004 1148h       |
| EPWM1_G2      | 5008 1148h       |
| EPWM1_G3      | 500C 1148h       |
| EPWM2_G0      | 5000 2148h       |
| EPWM2_G1      | 5004 2148h       |
| EPWM2_G2      | 5008 2148h       |
| EPWM2_G3      | 500C 2148h       |
| EPWM3_G0      | 5000 3148h       |
| EPWM3_G1      | 5004 3148h       |
| EPWM3_G2      | 5008 3148h       |
| EPWM3_G3      | 500C 3148h       |
| EPWM4_G0      | 5000 4148h       |
| EPWM4_G1      | 5004 4148h       |
| EPWM4_G2      | 5008 4148h       |
| EPWM4_G3      | 500C 4148h       |
| EPWM5_G0      | 5000 5148h       |
| EPWM5_G1      | 5004 5148h       |
| EPWM5_G2      | 5008 5148h       |
| EPWM5_G3      | 500C 5148h       |
| EPWM6_G0      | 5000 6148h       |
| EPWM6_G1      | 5004 6148h       |
| EPWM6_G2      | 5008 6148h       |
| EPWM6_G3      | 500C 6148h       |
| EPWM7_G0      | 5000 7148h       |
| EPWM7_G1      | 5004 7148h       |
| EPWM7_G2      | 5008 7148h       |
| EPWM7_G3      | 500C 7148h       |
| EPWM8_G0      | 5000 8148h       |
| EPWM8_G1      | 5004 8148h       |
| EPWM8_G2      | 5008 8148h       |
| EPWM8_G3      | 500C 8148h       |
| EPWM9_G0      | 5000 9148h       |
| EPWM9_G1      | 5004 9148h       |
| EPWM9_G2      | 5008 9148h       |

**Table 3-1003. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9148h       |
| EPWM10_G0     | 5000 A148h       |
| EPWM10_G1     | 5004 A148h       |
| EPWM10_G2     | 5008 A148h       |
| EPWM10_G3     | 500C A148h       |
| EPWM11_G0     | 5000 B148h       |
| EPWM11_G1     | 5004 B148h       |
| EPWM11_G2     | 5008 B148h       |
| EPWM11_G3     | 500C B148h       |
| EPWM12_G0     | 5000 C148h       |
| EPWM12_G1     | 5004 C148h       |
| EPWM12_G2     | 5008 C148h       |
| EPWM12_G3     | 500C C148h       |
| EPWM13_G0     | 5000 D148h       |
| EPWM13_G1     | 5004 D148h       |
| EPWM13_G2     | 5008 D148h       |
| EPWM13_G3     | 500C D148h       |
| EPWM14_G0     | 5000 E148h       |
| EPWM14_G1     | 5004 E148h       |
| EPWM14_G2     | 5008 E148h       |
| EPWM14_G3     | 500C E148h       |
| EPWM15_G0     | 5000 F148h       |
| EPWM15_G1     | 5004 F148h       |
| EPWM15_G2     | 5008 F148h       |
| EPWM15_G3     | 500C F148h       |
| EPWM16_G0     | 5001 0148h       |
| EPWM16_G1     | 5005 0148h       |
| EPWM16_G2     | 5009 0148h       |
| EPWM16_G3     | 500D 0148h       |
| EPWM17_G0     | 5001 1148h       |
| EPWM17_G1     | 5005 1148h       |
| EPWM17_G2     | 5009 1148h       |
| EPWM17_G3     | 500D 1148h       |
| EPWM18_G0     | 5001 2148h       |
| EPWM18_G1     | 5005 2148h       |
| EPWM18_G2     | 5009 2148h       |
| EPWM18_G3     | 500D 2148h       |
| EPWM19_G0     | 5001 3148h       |
| EPWM19_G1     | 5005 3148h       |
| EPWM19_G2     | 5009 3148h       |
| EPWM19_G3     | 500D 3148h       |
| EPWM20_G0     | 5001 4148h       |
| EPWM20_G1     | 5005 4148h       |
| EPWM20_G2     | 5009 4148h       |
| EPWM20_G3     | 500D 4148h       |

**Table 3-1003. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5148h       |
| EPWM21_G1     | 5005 5148h       |
| EPWM21_G2     | 5009 5148h       |
| EPWM21_G3     | 500D 5148h       |
| EPWM22_G0     | 5001 6148h       |
| EPWM22_G1     | 5005 6148h       |
| EPWM22_G2     | 5009 6148h       |
| EPWM22_G3     | 500D 6148h       |
| EPWM23_G0     | 5001 7148h       |
| EPWM23_G1     | 5005 7148h       |
| EPWM23_G2     | 5009 7148h       |
| EPWM23_G3     | 500D 7148h       |
| EPWM24_G0     | 5001 8148h       |
| EPWM24_G1     | 5005 8148h       |
| EPWM24_G2     | 5009 8148h       |
| EPWM24_G3     | 500D 8148h       |
| EPWM25_G0     | 5001 9148h       |
| EPWM25_G1     | 5005 9148h       |
| EPWM25_G2     | 5009 9148h       |
| EPWM25_G3     | 500D 9148h       |
| EPWM26_G0     | 5001 A148h       |
| EPWM26_G1     | 5005 A148h       |
| EPWM26_G2     | 5009 A148h       |
| EPWM26_G3     | 500D A148h       |
| EPWM27_G0     | 5001 B148h       |
| EPWM27_G1     | 5005 B148h       |
| EPWM27_G2     | 5009 B148h       |
| EPWM27_G3     | 500D B148h       |
| EPWM28_G0     | 5001 C148h       |
| EPWM28_G1     | 5005 C148h       |
| EPWM28_G2     | 5009 C148h       |
| EPWM28_G3     | 500D C148h       |
| EPWM29_G0     | 5001 D148h       |
| EPWM29_G1     | 5005 D148h       |
| EPWM29_G2     | 5009 D148h       |
| EPWM29_G3     | 500D D148h       |
| EPWM30_G0     | 5001 E148h       |
| EPWM30_G1     | 5005 E148h       |
| EPWM30_G2     | 5009 E148h       |
| EPWM30_G3     | 500D E148h       |
| EPWM31_G0     | 5001 F148h       |
| EPWM31_G1     | 5005 F148h       |
| EPWM31_G2     | 5009 F148h       |
| EPWM31_G3     | 500D F148h       |

**Figure 3-315. EPWM\_ETSEL Name Register**

| 15         | 14        | 13         | 12         | 11     | 10      | 9 | 8 |
|------------|-----------|------------|------------|--------|---------|---|---|
| SOCBEN     | SOCBSEL   |            |            | SOCAEN | SOCASEL |   |   |
| R/W        | R/W       |            |            | R/W    | R/W     |   |   |
| 0h         | 0h        |            |            | 0h     | 0h      |   |   |
| 7          | 6         | 5          | 4          | 3      | 2       | 1 | 0 |
| RESERVED_1 | INTSELCMP | SOCBSELCMP | SOCASELCMP | INTEN  | INTSEL  |   |   |
| R          | R/W       | R/W        | R/W        | R/W    | R/W     |   |   |
| 0h         | 0h        | 0h         | 0h         | 0h     | 0h      |   |   |

**Table 3-1005. EPWM\_ETSEL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | SOCBEN     | R/W  | 0h    | Enable the ADC Start of Conversion B [EPWMxSOCB] Pulse<br>0:Disable EPWMxSOCB.<br>1:Enable EPWMxSOCB pulse.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 14:12 | SOCBSEL    | R/W  | 0h    | EPWMxSOCB Selection Options<br>These bits determine when a EPWMxSOCB pulse will be generated.<br>000:Enable DCBEVT1.soc event<br>001:Enable event time-base counter equal to zero. [TBCTR = 0x00]<br>010:Enable event time-base counter equal to period [TBCTR = TBPRD]<br>011:Enable event time-base counter based on mixed events [ETSOCBMIX]. ETSOCBMIX is configured in the ETSOCBMIXEN register.<br>100:Enable event time-base counter equal to CMPA when the timer is incrementing or CMPC when the timer is incrementing<br>101:Enable event time-base counter equal to CMPA when the timer is decrementing or CMPC when the timer is decrementing<br>110:Enable event: time-base counter equal to CMPB when the timer is incrementing or CMPD when the timer is incrementing<br>111:Enable event: time-base counter equal to CMPB when the timer is decrementing or CMPD when the timer is decrementing [*] Event selected is determined by SOCBSELCMP bit. |
| 11    | SOCAEN     | R/W  | 0h    | Enable the ADC Start of Conversion A [EPWMxSOCA] Pulse<br>0:Disable EPWMxSOCA.<br>1:Enable EPWMxSOCA pulse.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 10:8  | SOCASEL    | R/W  | 0h    | EPWMxSOCA Selection Options<br>These bits determine when a EPWMxSOCA pulse will be generated.<br>000:Enable DCAEVT1.soc event<br>001:Enable event time-base counter equal to zero. [TBCTR = 0x00]<br>010:Enable event time-base counter equal to period [TBCTR = TBPRD]<br>011:Enable event time-base counter based on mixed events [ETSOCAMIX]. ETSOCAMIX is configured in the ETSOCAMIXEN register.<br>100:Enable event time-base counter equal to CMPA when the timer is incrementing or CMPC when the timer is incrementing<br>101:Enable event time-base counter equal to CMPA when the timer is decrementing or CMPC when the timer is decrementing<br>110:Enable event: time-base counter equal to CMPB when the timer is incrementing or CMPD when the timer is incrementing<br>111:Enable event: time-base counter equal to CMPB when the timer is decrementing or CMPD when the timer is decrementing [*] Event selected is determined by SOCASELCMP bit. |
| 7     | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |



**Table 3-1005. EPWM\_ETSEL Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-----|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6   | INTSELCMP  | R/W  | 0h    | <p>EPWMxINT Compare Register Selection Options</p> <p>0:Enable event time-base counter equal to CMPA when the timer is incrementing / Enable event time-base counter equal to CMPA when the timer is decrementing / Enable event: time-base counter equal to CMPB when the timer is incrementing / Enable event: time-base counter equal to CMPB when the timer is decrementing to INTSEL selection mux.</p> <p>1:Enable event time-base counter equal to CMPC when the timer is incrementing / Enable event time-base counter equal to CMPC when the timer is decrementing / Enable event: time-base counter equal to CMPD when the timer is incrementing / Enable event: time-base counter equal to CMPD when the timer is decrementing to INTSEL selection mux.</p>                                                                                                                                                                |
| 5   | SOCBSELCMP | R/W  | 0h    | <p>EPWMxSOCB Compare Register Selection Options</p> <p>0:Enable event time-base counter equal to CMPA when the timer is incrementing / Enable event time-base counter equal to CMPA when the timer is decrementing / Enable event: time-base counter equal to CMPB when the timer is incrementing / Enable event: time-base counter equal to CMPB when the timer is decrementing to SOCBSEL selection mux.</p> <p>1:Enable event time-base counter equal to CMPC when the timer is incrementing / Enable event time-base counter equal to CMPC when the timer is decrementing / Enable event: time-base counter equal to CMPD when the timer is incrementing / Enable event: time-base counter equal to CMPD when the timer is decrementing to SOCBSEL selection mux.</p>                                                                                                                                                             |
| 4   | SOCASELCMP | R/W  | 0h    | <p>EPWMxSOCA Compare Register Selection Options</p> <p>0:Enable event time-base counter equal to CMPA when the timer is incrementing / Enable event time-base counter equal to CMPA when the timer is decrementing / Enable event: time-base counter equal to CMPB when the timer is incrementing / Enable event: time-base counter equal to CMPB when the timer is decrementing to SOCASEL selection mux.</p> <p>1:Enable event time-base counter equal to CMPC when the timer is incrementing / Enable event time-base counter equal to CMPC when the timer is decrementing / Enable event: time-base counter equal to CMPD when the timer is incrementing / Enable event: time-base counter equal to CMPD when the timer is decrementing to SOCASEL selection mux.</p>                                                                                                                                                             |
| 3   | INTEN      | R/W  | 0h    | <p>Enable EPWM Interrupt [EPWMx_INT] Generation</p> <p>0:Disable EPWMx_INT generation</p> <p>1:Enable EPWMx_INT generation</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 2:0 | INTSEL     | R/W  | 0h    | <p>EPWM Interrupt [EPWMx_INT] Selection Options</p> <p>000:Reserved</p> <p>001:Enable event time-base counter equal to zero. [TBCTR = 0x00]</p> <p>010:Enable event time-base counter equal to period [TBCTR = TBPRD]</p> <p>011:Enable event time-base counter based on mixed events [ETINTMIX]. ETINTMIX is configured in the ETINTMIXEN register.</p> <p>100:Enable event time-base counter equal to CMPA when the timer is incrementing or CMPC when the timer is incrementing</p> <p>101:Enable event time-base counter equal to CMPA when the timer is decrementing or CMPC when the timer is decrementing</p> <p>110:Enable event: time-base counter equal to CMPB when the timer is incrementing or CMPD when the timer is incrementing</p> <p>111:Enable event: time-base counter equal to CMPB when the timer is decrementing or CMPD when the timer is decrementing [*] Event selected is determined by INTSELCMP bit.</p> |

### 3.7.2.65 EPWM\_ETPS Register

#### 1 EPWM\_ETPS Register (Offset = 14Ch) [reset = 0h]

Event Trigger Pre-Scale Register.

Return to [Summary Table](#)

**Table 3-1006. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 014Ch       |
| EPWM0_G1      | 5004 014Ch       |
| EPWM0_G2      | 5008 014Ch       |
| EPWM0_G3      | 500C 014Ch       |
| EPWM1_G0      | 5000 114Ch       |
| EPWM1_G1      | 5004 114Ch       |
| EPWM1_G2      | 5008 114Ch       |
| EPWM1_G3      | 500C 114Ch       |
| EPWM2_G0      | 5000 214Ch       |
| EPWM2_G1      | 5004 214Ch       |
| EPWM2_G2      | 5008 214Ch       |
| EPWM2_G3      | 500C 214Ch       |
| EPWM3_G0      | 5000 314Ch       |
| EPWM3_G1      | 5004 314Ch       |
| EPWM3_G2      | 5008 314Ch       |
| EPWM3_G3      | 500C 314Ch       |
| EPWM4_G0      | 5000 414Ch       |
| EPWM4_G1      | 5004 414Ch       |
| EPWM4_G2      | 5008 414Ch       |
| EPWM4_G3      | 500C 414Ch       |
| EPWM5_G0      | 5000 514Ch       |
| EPWM5_G1      | 5004 514Ch       |
| EPWM5_G2      | 5008 514Ch       |
| EPWM5_G3      | 500C 514Ch       |
| EPWM6_G0      | 5000 614Ch       |
| EPWM6_G1      | 5004 614Ch       |
| EPWM6_G2      | 5008 614Ch       |
| EPWM6_G3      | 500C 614Ch       |
| EPWM7_G0      | 5000 714Ch       |
| EPWM7_G1      | 5004 714Ch       |
| EPWM7_G2      | 5008 714Ch       |
| EPWM7_G3      | 500C 714Ch       |
| EPWM8_G0      | 5000 814Ch       |
| EPWM8_G1      | 5004 814Ch       |
| EPWM8_G2      | 5008 814Ch       |
| EPWM8_G3      | 500C 814Ch       |
| EPWM9_G0      | 5000 914Ch       |
| EPWM9_G1      | 5004 914Ch       |
| EPWM9_G2      | 5008 914Ch       |

**Table 3-1006. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 914Ch       |
| EPWM10_G0     | 5000 A14Ch       |
| EPWM10_G1     | 5004 A14Ch       |
| EPWM10_G2     | 5008 A14Ch       |
| EPWM10_G3     | 500C A14Ch       |
| EPWM11_G0     | 5000 B14Ch       |
| EPWM11_G1     | 5004 B14Ch       |
| EPWM11_G2     | 5008 B14Ch       |
| EPWM11_G3     | 500C B14Ch       |
| EPWM12_G0     | 5000 C14Ch       |
| EPWM12_G1     | 5004 C14Ch       |
| EPWM12_G2     | 5008 C14Ch       |
| EPWM12_G3     | 500C C14Ch       |
| EPWM13_G0     | 5000 D14Ch       |
| EPWM13_G1     | 5004 D14Ch       |
| EPWM13_G2     | 5008 D14Ch       |
| EPWM13_G3     | 500C D14Ch       |
| EPWM14_G0     | 5000 E14Ch       |
| EPWM14_G1     | 5004 E14Ch       |
| EPWM14_G2     | 5008 E14Ch       |
| EPWM14_G3     | 500C E14Ch       |
| EPWM15_G0     | 5000 F14Ch       |
| EPWM15_G1     | 5004 F14Ch       |
| EPWM15_G2     | 5008 F14Ch       |
| EPWM15_G3     | 500C F14Ch       |
| EPWM16_G0     | 5001 014Ch       |
| EPWM16_G1     | 5005 014Ch       |
| EPWM16_G2     | 5009 014Ch       |
| EPWM16_G3     | 500D 014Ch       |
| EPWM17_G0     | 5001 114Ch       |
| EPWM17_G1     | 5005 114Ch       |
| EPWM17_G2     | 5009 114Ch       |
| EPWM17_G3     | 500D 114Ch       |
| EPWM18_G0     | 5001 214Ch       |
| EPWM18_G1     | 5005 214Ch       |
| EPWM18_G2     | 5009 214Ch       |
| EPWM18_G3     | 500D 214Ch       |
| EPWM19_G0     | 5001 314Ch       |
| EPWM19_G1     | 5005 314Ch       |
| EPWM19_G2     | 5009 314Ch       |
| EPWM19_G3     | 500D 314Ch       |
| EPWM20_G0     | 5001 414Ch       |
| EPWM20_G1     | 5005 414Ch       |
| EPWM20_G2     | 5009 414Ch       |
| EPWM20_G3     | 500D 414Ch       |

**Table 3-1006. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 514Ch       |
| EPWM21_G1     | 5005 514Ch       |
| EPWM21_G2     | 5009 514Ch       |
| EPWM21_G3     | 500D 514Ch       |
| EPWM22_G0     | 5001 614Ch       |
| EPWM22_G1     | 5005 614Ch       |
| EPWM22_G2     | 5009 614Ch       |
| EPWM22_G3     | 500D 614Ch       |
| EPWM23_G0     | 5001 714Ch       |
| EPWM23_G1     | 5005 714Ch       |
| EPWM23_G2     | 5009 714Ch       |
| EPWM23_G3     | 500D 714Ch       |
| EPWM24_G0     | 5001 814Ch       |
| EPWM24_G1     | 5005 814Ch       |
| EPWM24_G2     | 5009 814Ch       |
| EPWM24_G3     | 500D 814Ch       |
| EPWM25_G0     | 5001 914Ch       |
| EPWM25_G1     | 5005 914Ch       |
| EPWM25_G2     | 5009 914Ch       |
| EPWM25_G3     | 500D 914Ch       |
| EPWM26_G0     | 5001 A14Ch       |
| EPWM26_G1     | 5005 A14Ch       |
| EPWM26_G2     | 5009 A14Ch       |
| EPWM26_G3     | 500D A14Ch       |
| EPWM27_G0     | 5001 B14Ch       |
| EPWM27_G1     | 5005 B14Ch       |
| EPWM27_G2     | 5009 B14Ch       |
| EPWM27_G3     | 500D B14Ch       |
| EPWM28_G0     | 5001 C14Ch       |
| EPWM28_G1     | 5005 C14Ch       |
| EPWM28_G2     | 5009 C14Ch       |
| EPWM28_G3     | 500D C14Ch       |
| EPWM29_G0     | 5001 D14Ch       |
| EPWM29_G1     | 5005 D14Ch       |
| EPWM29_G2     | 5009 D14Ch       |
| EPWM29_G3     | 500D D14Ch       |
| EPWM30_G0     | 5001 E14Ch       |
| EPWM30_G1     | 5005 E14Ch       |
| EPWM30_G2     | 5009 E14Ch       |
| EPWM30_G3     | 500D E14Ch       |
| EPWM31_G0     | 5001 F14Ch       |
| EPWM31_G1     | 5005 F14Ch       |
| EPWM31_G2     | 5009 F14Ch       |
| EPWM31_G3     | 500D F14Ch       |

**Figure 3-316. EPWM\_ETPS Name Register**

| 15         | 14 | 13       | 12      | 11      | 10 | 9       | 8 |
|------------|----|----------|---------|---------|----|---------|---|
| SOCBCNT    |    | SOCBPRD  |         | SOCACNT |    | SOCAPRD |   |
| R          |    | R/W      |         | R       |    | R/W     |   |
| 0h         |    | 0h       |         | 0h      |    | 0h      |   |
| 7          | 6  | 5        | 4       | 3       | 2  | 1       | 0 |
| RESERVED_1 |    | SOCPSSEL | INTPSEL | INTCNT  |    | INTPRD  |   |
| R          |    | R/W      | R/W     | R       |    | R/W     |   |
| 0h         |    | 0h       | 0h      | 0h      |    | 0h      |   |

**Table 3-1008. EPWM\_ETPS Register Field Descriptions**

| Bit   | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|---------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | SOCBCNT | R    | 0h    | EPWM ADC Start-of-Conversion B Event [EPWMxSOCB] Counter Register<br>These bits indicate how many selected ETSEL[SOCBSEL] events have occurred:<br>00:No events have occurred.<br>01:1 event has occurred.<br>10:2 events have occurred.<br>11:3 events have occurred.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 13:12 | SOCBPRD | R/W  | 0h    | EPWM ADC Start-of-Conversion B Event [EPWMxSOCB] Period Select<br>These bits determine how many selected ETSEL[SOCBSEL] events need to occur before an EPWMxSOCB pulse is generated. To be generated, the pulse must be enabled [ETSEL[SOCBEN] = 1]. The SOCB pulse will be generated even if the status flag is set from a previous start of conversion [ETFLG[SOCB] = 1]. Once the SOCB pulse is generated, the ETPS[SOCBCNT] bits will automatically be cleared.<br>00:Disable the SOCB event counter. No EPWMxSOCB pulse will be generated<br>01:Generate the EPWMxSOCB pulse on the first event:<br>ETPS[SOCBCNT] = 2'b01<br>10:Generate the EPWMxSOCB pulse on the second event:<br>ETPS[SOCBCNT] = 2'b10<br>11:Generate the EPWMxSOCB pulse on the third event:<br>ETPS[SOCBCNT] = 2'b11 |
| 11:10 | SOCACNT | R    | 0h    | EPWM ADC Start-of-Conversion A Event [EPWMxSOCA] Counter Register<br>These bits indicate how many selected ETSEL[SOCASEL] events have occurred:<br>00:No events have occurred.<br>01:1 event has occurred.<br>10:2 events have occurred.<br>11:3 events have occurred.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 9:8   | SOCAPRD | R/W  | 0h    | EPWM ADC Start-of-Conversion A Event [EPWMxSOCA] Period Select<br>These bits determine how many selected ETSEL[SOCASEL] events need to occur before an EPWMxSOCA pulse is generated. To be generated, the pulse must be enabled [ETSEL[SOCAEN] = 1]. The SOCA pulse will be generated even if the status flag is set from a previous start of conversion [ETFLG[SOCA] = 1]. Once the SOCA pulse is generated, the ETPS[SOCACNT] bits will automatically be cleared.<br>00:Disable the SOCA event counter. No EPWMxSOCA pulse will be generated<br>01:Generate the EPWMxSOCA pulse on the first event:<br>ETPS[SOCACNT] = 2'b01<br>10:Generate the EPWMxSOCA pulse on the second event:<br>ETPS[SOCACNT] = 2'b10<br>11:Generate the EPWMxSOCA pulse on the third event:<br>ETPS[SOCACNT] = 2'b11 |

**Table 3-1008. EPWM\_ETPS Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 5   | SOCPSSEL   | R/W  | 0h    | EPWMxSOC A/B Pre-Scale Selection Bits<br>0:Selects ETPS [SOCACNT/SOCBCNT] and [SOCAPRD/ SOCBPRD] registers to determine frequency of events [interrupt once every 0-3 events].<br>1:Selects ETSOCPS [SOCACNT2/SOCBCNT2] and [SOCAPRD2/ SOCBPRD2] registers to determine frequency of events [interrupt once every 0-15 events].                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 4   | INTPSSEL   | R/W  | 0h    | EPWMxINTn Pre-Scale Selection Bits<br>0:Selects ETPS [INTCNT, and INTPRD] registers to determine frequency of events [interrupt once every 0-3 events].<br>1:Selects ETINTPS [ INTCNT2, and INTPRD2 ] registers to determine frequency of events [interrupt once every 0-15 events].                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 3:2 | INTCNT     | R    | 0h    | EPWM Interrupt Event [EPWMx_INT] Counter Register<br>These bits indicate how many selected ETSEL[INTSEL] events have occurred. These bits are automatically cleared when an interrupt pulse is generated. If interrupts are disabled, ETSEL[INT] = 0 or the interrupt flag is set, ETFLG[INT] = 1, the counter will stop counting events when it reaches the period value ETPS[INTCNT] = ETPS[INTPRD].<br>00:No events have occurred.<br>01:1 event has occurred.<br>10:2 events have occurred.<br>11:3 events have occurred.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 1:0 | INTPRD     | R/W  | 0h    | EPWM Interrupt [EPWMx_INT] Period Select<br>These bits determine how many selected ETSEL[INTSEL] events need to occur before an interrupt is generated. To be generated, the interrupt must be enabled [ETSEL[INT] = 1]. If the interrupt status flag is set from a previous interrupt [ETFLG[INT] = 1] then no interrupt will be generated until the flag is cleared via the ETCLR[INT] bit. This allows for one interrupt to be pending while another is still being serviced. Once the interrupt is generated, the ETPS[INTCNT] bits will automatically be cleared.<br>Writing a INTPRD value that is the same as the current counter value will trigger an interrupt if it is enabled and the status flag is clear.<br>Writing a INTPRD value that is less than the current counter value will result in an undefined state. If a counter event occurs at the same instant as a new zero or non-zero INTPRD value is written, the counter is incremented.<br>00:Disable the interrupt event counter. No interrupt will be generated and ETFRC[INT] is ignored.<br>01:Generate an interrupt on the first event INTCNT = 01 [first event]<br>10:Generate interrupt on ETPS[INTCNT] = 2'b10 [second event]<br>11:Generate interrupt on ETPS[INTCNT] = 2'b11 [third event] |

### 3.7.2.66 EPWM\_ETFLG Register

#### 1 EPWM\_ETFLG Register (Offset = 150h) [reset = 0h]

Event Trigger Flag Register.

Return to [Summary Table](#)

**Table 3-1009. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0150h       |
| EPWM0_G1      | 5004 0150h       |
| EPWM0_G2      | 5008 0150h       |
| EPWM0_G3      | 500C 0150h       |
| EPWM1_G0      | 5000 1150h       |
| EPWM1_G1      | 5004 1150h       |
| EPWM1_G2      | 5008 1150h       |
| EPWM1_G3      | 500C 1150h       |
| EPWM2_G0      | 5000 2150h       |
| EPWM2_G1      | 5004 2150h       |
| EPWM2_G2      | 5008 2150h       |
| EPWM2_G3      | 500C 2150h       |
| EPWM3_G0      | 5000 3150h       |
| EPWM3_G1      | 5004 3150h       |
| EPWM3_G2      | 5008 3150h       |
| EPWM3_G3      | 500C 3150h       |
| EPWM4_G0      | 5000 4150h       |
| EPWM4_G1      | 5004 4150h       |
| EPWM4_G2      | 5008 4150h       |
| EPWM4_G3      | 500C 4150h       |
| EPWM5_G0      | 5000 5150h       |
| EPWM5_G1      | 5004 5150h       |
| EPWM5_G2      | 5008 5150h       |
| EPWM5_G3      | 500C 5150h       |
| EPWM6_G0      | 5000 6150h       |
| EPWM6_G1      | 5004 6150h       |
| EPWM6_G2      | 5008 6150h       |
| EPWM6_G3      | 500C 6150h       |
| EPWM7_G0      | 5000 7150h       |
| EPWM7_G1      | 5004 7150h       |
| EPWM7_G2      | 5008 7150h       |
| EPWM7_G3      | 500C 7150h       |
| EPWM8_G0      | 5000 8150h       |
| EPWM8_G1      | 5004 8150h       |
| EPWM8_G2      | 5008 8150h       |
| EPWM8_G3      | 500C 8150h       |
| EPWM9_G0      | 5000 9150h       |
| EPWM9_G1      | 5004 9150h       |
| EPWM9_G2      | 5008 9150h       |

**Table 3-1009. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9150h       |
| EPWM10_G0     | 5000 A150h       |
| EPWM10_G1     | 5004 A150h       |
| EPWM10_G2     | 5008 A150h       |
| EPWM10_G3     | 500C A150h       |
| EPWM11_G0     | 5000 B150h       |
| EPWM11_G1     | 5004 B150h       |
| EPWM11_G2     | 5008 B150h       |
| EPWM11_G3     | 500C B150h       |
| EPWM12_G0     | 5000 C150h       |
| EPWM12_G1     | 5004 C150h       |
| EPWM12_G2     | 5008 C150h       |
| EPWM12_G3     | 500C C150h       |
| EPWM13_G0     | 5000 D150h       |
| EPWM13_G1     | 5004 D150h       |
| EPWM13_G2     | 5008 D150h       |
| EPWM13_G3     | 500C D150h       |
| EPWM14_G0     | 5000 E150h       |
| EPWM14_G1     | 5004 E150h       |
| EPWM14_G2     | 5008 E150h       |
| EPWM14_G3     | 500C E150h       |
| EPWM15_G0     | 5000 F150h       |
| EPWM15_G1     | 5004 F150h       |
| EPWM15_G2     | 5008 F150h       |
| EPWM15_G3     | 500C F150h       |
| EPWM16_G0     | 5001 0150h       |
| EPWM16_G1     | 5005 0150h       |
| EPWM16_G2     | 5009 0150h       |
| EPWM16_G3     | 500D 0150h       |
| EPWM17_G0     | 5001 1150h       |
| EPWM17_G1     | 5005 1150h       |
| EPWM17_G2     | 5009 1150h       |
| EPWM17_G3     | 500D 1150h       |
| EPWM18_G0     | 5001 2150h       |
| EPWM18_G1     | 5005 2150h       |
| EPWM18_G2     | 5009 2150h       |
| EPWM18_G3     | 500D 2150h       |
| EPWM19_G0     | 5001 3150h       |
| EPWM19_G1     | 5005 3150h       |
| EPWM19_G2     | 5009 3150h       |
| EPWM19_G3     | 500D 3150h       |
| EPWM20_G0     | 5001 4150h       |
| EPWM20_G1     | 5005 4150h       |
| EPWM20_G2     | 5009 4150h       |
| EPWM20_G3     | 500D 4150h       |



**Table 3-1009. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5150h       |
| EPWM21_G1     | 5005 5150h       |
| EPWM21_G2     | 5009 5150h       |
| EPWM21_G3     | 500D 5150h       |
| EPWM22_G0     | 5001 6150h       |
| EPWM22_G1     | 5005 6150h       |
| EPWM22_G2     | 5009 6150h       |
| EPWM22_G3     | 500D 6150h       |
| EPWM23_G0     | 5001 7150h       |
| EPWM23_G1     | 5005 7150h       |
| EPWM23_G2     | 5009 7150h       |
| EPWM23_G3     | 500D 7150h       |
| EPWM24_G0     | 5001 8150h       |
| EPWM24_G1     | 5005 8150h       |
| EPWM24_G2     | 5009 8150h       |
| EPWM24_G3     | 500D 8150h       |
| EPWM25_G0     | 5001 9150h       |
| EPWM25_G1     | 5005 9150h       |
| EPWM25_G2     | 5009 9150h       |
| EPWM25_G3     | 500D 9150h       |
| EPWM26_G0     | 5001 A150h       |
| EPWM26_G1     | 5005 A150h       |
| EPWM26_G2     | 5009 A150h       |
| EPWM26_G3     | 500D A150h       |
| EPWM27_G0     | 5001 B150h       |
| EPWM27_G1     | 5005 B150h       |
| EPWM27_G2     | 5009 B150h       |
| EPWM27_G3     | 500D B150h       |
| EPWM28_G0     | 5001 C150h       |
| EPWM28_G1     | 5005 C150h       |
| EPWM28_G2     | 5009 C150h       |
| EPWM28_G3     | 500D C150h       |
| EPWM29_G0     | 5001 D150h       |
| EPWM29_G1     | 5005 D150h       |
| EPWM29_G2     | 5009 D150h       |
| EPWM29_G3     | 500D D150h       |
| EPWM30_G0     | 5001 E150h       |
| EPWM30_G1     | 5005 E150h       |
| EPWM30_G2     | 5009 E150h       |
| EPWM30_G3     | 500D E150h       |
| EPWM31_G0     | 5001 F150h       |
| EPWM31_G1     | 5005 F150h       |
| EPWM31_G2     | 5009 F150h       |
| EPWM31_G3     | 500D F150h       |

**Figure 3-317. EPWM\_ETFLG Name Register**

|            |    |    |    |      |      |            |     |
|------------|----|----|----|------|------|------------|-----|
| 15         | 14 | 13 | 12 | 11   | 10   | 9          | 8   |
| RESERVED_2 |    |    |    |      |      |            |     |
| R          |    |    |    |      |      |            |     |
| 0h         |    |    |    |      |      |            |     |
| 7          | 6  | 5  | 4  | 3    | 2    | 1          | 0   |
| RESERVED_2 |    |    |    | SOCB | SOCA | RESERVED_1 | INT |
| R          |    |    |    | R    | R    | R          | R   |
| 0h         |    |    |    | 0h   | 0h   | 0h         | 0h  |

**Table 3-1011. EPWM\_ETFLG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:4 | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                           |
| 3    | SOCB       | R    | 0h    | Latched EPWM ADC Start-of-Conversion A [EPWMxSOCB] Status Flag<br>Unlike the ETFLG[INT] flag, the EPWMxSOCB output will continue to pulse even if the flag bit is set.<br>0:Indicates no event occurred<br>1:Indicates that a start of conversion pulse was generated on EPWMxSOCB. The EPWMxSOCB output will continue to be generated even if the flag bit is set.                                |
| 2    | SOCA       | R    | 0h    | Latched EPWM ADC Start-of-Conversion A [EPWMxSOCA] Status Flag<br>Unlike the ETFLG[INT] flag, the EPWMxSOCA output will continue to pulse even if the flag bit is set.<br>0:Indicates no event occurred<br>1:Indicates that a start of conversion pulse was generated on EPWMxSOCA. The EPWMxSOCA output will continue to be generated even if the flag bit is set.                                |
| 1    | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                           |
| 0    | INT        | R    | 0h    | Latched EPWM Interrupt [EPWMx_INT] Status Flag<br>0:Indicates no event occurred<br>1:Indicates that an EPWMx interrupt [EPWMx_INT] was generated. No further interrupts will be generated until the flag bit is cleared. Up to one interrupt can be pending while the ETFLG[INT] bit is still set. If an interrupt is pending, it will not be generated until after the ETFLG[INT] bit is cleared. |

### 3.7.2.67 EPWM\_ETCLR Register

#### 1 EPWM\_ETCLR Register (Offset = 154h) [reset = 0h]

Event Trigger Clear Register.

Return to [Summary Table](#)

**Table 3-1012. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0154h       |
| EPWM0_G1      | 5004 0154h       |
| EPWM0_G2      | 5008 0154h       |
| EPWM0_G3      | 500C 0154h       |
| EPWM1_G0      | 5000 1154h       |
| EPWM1_G1      | 5004 1154h       |
| EPWM1_G2      | 5008 1154h       |
| EPWM1_G3      | 500C 1154h       |
| EPWM2_G0      | 5000 2154h       |
| EPWM2_G1      | 5004 2154h       |
| EPWM2_G2      | 5008 2154h       |
| EPWM2_G3      | 500C 2154h       |
| EPWM3_G0      | 5000 3154h       |
| EPWM3_G1      | 5004 3154h       |
| EPWM3_G2      | 5008 3154h       |
| EPWM3_G3      | 500C 3154h       |
| EPWM4_G0      | 5000 4154h       |
| EPWM4_G1      | 5004 4154h       |
| EPWM4_G2      | 5008 4154h       |
| EPWM4_G3      | 500C 4154h       |
| EPWM5_G0      | 5000 5154h       |
| EPWM5_G1      | 5004 5154h       |
| EPWM5_G2      | 5008 5154h       |
| EPWM5_G3      | 500C 5154h       |
| EPWM6_G0      | 5000 6154h       |
| EPWM6_G1      | 5004 6154h       |
| EPWM6_G2      | 5008 6154h       |
| EPWM6_G3      | 500C 6154h       |
| EPWM7_G0      | 5000 7154h       |
| EPWM7_G1      | 5004 7154h       |
| EPWM7_G2      | 5008 7154h       |
| EPWM7_G3      | 500C 7154h       |
| EPWM8_G0      | 5000 8154h       |
| EPWM8_G1      | 5004 8154h       |
| EPWM8_G2      | 5008 8154h       |
| EPWM8_G3      | 500C 8154h       |
| EPWM9_G0      | 5000 9154h       |
| EPWM9_G1      | 5004 9154h       |
| EPWM9_G2      | 5008 9154h       |

**Table 3-1012. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9154h       |
| EPWM10_G0     | 5000 A154h       |
| EPWM10_G1     | 5004 A154h       |
| EPWM10_G2     | 5008 A154h       |
| EPWM10_G3     | 500C A154h       |
| EPWM11_G0     | 5000 B154h       |
| EPWM11_G1     | 5004 B154h       |
| EPWM11_G2     | 5008 B154h       |
| EPWM11_G3     | 500C B154h       |
| EPWM12_G0     | 5000 C154h       |
| EPWM12_G1     | 5004 C154h       |
| EPWM12_G2     | 5008 C154h       |
| EPWM12_G3     | 500C C154h       |
| EPWM13_G0     | 5000 D154h       |
| EPWM13_G1     | 5004 D154h       |
| EPWM13_G2     | 5008 D154h       |
| EPWM13_G3     | 500C D154h       |
| EPWM14_G0     | 5000 E154h       |
| EPWM14_G1     | 5004 E154h       |
| EPWM14_G2     | 5008 E154h       |
| EPWM14_G3     | 500C E154h       |
| EPWM15_G0     | 5000 F154h       |
| EPWM15_G1     | 5004 F154h       |
| EPWM15_G2     | 5008 F154h       |
| EPWM15_G3     | 500C F154h       |
| EPWM16_G0     | 5001 0154h       |
| EPWM16_G1     | 5005 0154h       |
| EPWM16_G2     | 5009 0154h       |
| EPWM16_G3     | 500D 0154h       |
| EPWM17_G0     | 5001 1154h       |
| EPWM17_G1     | 5005 1154h       |
| EPWM17_G2     | 5009 1154h       |
| EPWM17_G3     | 500D 1154h       |
| EPWM18_G0     | 5001 2154h       |
| EPWM18_G1     | 5005 2154h       |
| EPWM18_G2     | 5009 2154h       |
| EPWM18_G3     | 500D 2154h       |
| EPWM19_G0     | 5001 3154h       |
| EPWM19_G1     | 5005 3154h       |
| EPWM19_G2     | 5009 3154h       |
| EPWM19_G3     | 500D 3154h       |
| EPWM20_G0     | 5001 4154h       |
| EPWM20_G1     | 5005 4154h       |
| EPWM20_G2     | 5009 4154h       |
| EPWM20_G3     | 500D 4154h       |

**Table 3-1012. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5154h       |
| EPWM21_G1     | 5005 5154h       |
| EPWM21_G2     | 5009 5154h       |
| EPWM21_G3     | 500D 5154h       |
| EPWM22_G0     | 5001 6154h       |
| EPWM22_G1     | 5005 6154h       |
| EPWM22_G2     | 5009 6154h       |
| EPWM22_G3     | 500D 6154h       |
| EPWM23_G0     | 5001 7154h       |
| EPWM23_G1     | 5005 7154h       |
| EPWM23_G2     | 5009 7154h       |
| EPWM23_G3     | 500D 7154h       |
| EPWM24_G0     | 5001 8154h       |
| EPWM24_G1     | 5005 8154h       |
| EPWM24_G2     | 5009 8154h       |
| EPWM24_G3     | 500D 8154h       |
| EPWM25_G0     | 5001 9154h       |
| EPWM25_G1     | 5005 9154h       |
| EPWM25_G2     | 5009 9154h       |
| EPWM25_G3     | 500D 9154h       |
| EPWM26_G0     | 5001 A154h       |
| EPWM26_G1     | 5005 A154h       |
| EPWM26_G2     | 5009 A154h       |
| EPWM26_G3     | 500D A154h       |
| EPWM27_G0     | 5001 B154h       |
| EPWM27_G1     | 5005 B154h       |
| EPWM27_G2     | 5009 B154h       |
| EPWM27_G3     | 500D B154h       |
| EPWM28_G0     | 5001 C154h       |
| EPWM28_G1     | 5005 C154h       |
| EPWM28_G2     | 5009 C154h       |
| EPWM28_G3     | 500D C154h       |
| EPWM29_G0     | 5001 D154h       |
| EPWM29_G1     | 5005 D154h       |
| EPWM29_G2     | 5009 D154h       |
| EPWM29_G3     | 500D D154h       |
| EPWM30_G0     | 5001 E154h       |
| EPWM30_G1     | 5005 E154h       |
| EPWM30_G2     | 5009 E154h       |
| EPWM30_G3     | 500D E154h       |
| EPWM31_G0     | 5001 F154h       |
| EPWM31_G1     | 5005 F154h       |
| EPWM31_G2     | 5009 F154h       |
| EPWM31_G3     | 500D F154h       |

**Figure 3-318. EPWM\_ETCLR Name Register**

|            |    |    |    |        |        |            |        |
|------------|----|----|----|--------|--------|------------|--------|
| 15         | 14 | 13 | 12 | 11     | 10     | 9          | 8      |
| RESERVED_2 |    |    |    |        |        |            |        |
| R          |    |    |    |        |        |            |        |
| 0h         |    |    |    |        |        |            |        |
| 7          | 6  | 5  | 4  | 3      | 2      | 1          | 0      |
| RESERVED_2 |    |    |    | SOCB   | SOCA   | RESERVED_1 | INT    |
| R          |    |    |    | R/W1TS | R/W1TS | R          | R/W1TS |
| 0h         |    |    |    | 0h     | 0h     | 0h         | 0h     |

**Table 3-1014. EPWM\_ETCLR Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                                              |
|------|------------|--------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:4 | RESERVED_2 | R      | 0h    | Reserved                                                                                                                                                                                 |
| 3    | SOCB       | R/W1TS | 0h    | EPWM ADC Start-of-Conversion A [EPWMxSOCB] Flag Clear Bit<br>0:Writing a 0 has no effect. Always reads back a 0<br>1:Clears the ETFLG[SOCB] flag bit                                     |
| 2    | SOCA       | R/W1TS | 0h    | EPWM ADC Start-of-Conversion A [EPWMxSOCA] Flag Clear Bit<br>0:Writing a 0 has no effect. Always reads back a 0<br>1:Clears the ETFLG[SOCA] flag bit                                     |
| 1    | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                 |
| 0    | INT        | R/W1TS | 0h    | EPWM Interrupt [EPWMx_INT] Flag Clear Bit<br>0:Writing a 0 has no effect. Always reads back a 0<br>1:Clears the ETFLG[INT] flag bit and enable further interrupts pulses to be generated |

### 3.7.2.68 EPWM ETFRC Register

#### 1 EPWM ETFRC Register (Offset = 158h) [reset = 0h]

Event Trigger Force Register.

Return to [Summary Table](#)

**Table 3-1015. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0158h       |
| EPWM0_G1      | 5004 0158h       |
| EPWM0_G2      | 5008 0158h       |
| EPWM0_G3      | 500C 0158h       |
| EPWM1_G0      | 5000 1158h       |
| EPWM1_G1      | 5004 1158h       |
| EPWM1_G2      | 5008 1158h       |
| EPWM1_G3      | 500C 1158h       |
| EPWM2_G0      | 5000 2158h       |
| EPWM2_G1      | 5004 2158h       |
| EPWM2_G2      | 5008 2158h       |
| EPWM2_G3      | 500C 2158h       |
| EPWM3_G0      | 5000 3158h       |
| EPWM3_G1      | 5004 3158h       |
| EPWM3_G2      | 5008 3158h       |
| EPWM3_G3      | 500C 3158h       |
| EPWM4_G0      | 5000 4158h       |
| EPWM4_G1      | 5004 4158h       |
| EPWM4_G2      | 5008 4158h       |
| EPWM4_G3      | 500C 4158h       |
| EPWM5_G0      | 5000 5158h       |
| EPWM5_G1      | 5004 5158h       |
| EPWM5_G2      | 5008 5158h       |
| EPWM5_G3      | 500C 5158h       |
| EPWM6_G0      | 5000 6158h       |
| EPWM6_G1      | 5004 6158h       |
| EPWM6_G2      | 5008 6158h       |
| EPWM6_G3      | 500C 6158h       |
| EPWM7_G0      | 5000 7158h       |
| EPWM7_G1      | 5004 7158h       |
| EPWM7_G2      | 5008 7158h       |
| EPWM7_G3      | 500C 7158h       |
| EPWM8_G0      | 5000 8158h       |
| EPWM8_G1      | 5004 8158h       |
| EPWM8_G2      | 5008 8158h       |
| EPWM8_G3      | 500C 8158h       |
| EPWM9_G0      | 5000 9158h       |
| EPWM9_G1      | 5004 9158h       |
| EPWM9_G2      | 5008 9158h       |

**Table 3-1015. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9158h       |
| EPWM10_G0     | 5000 A158h       |
| EPWM10_G1     | 5004 A158h       |
| EPWM10_G2     | 5008 A158h       |
| EPWM10_G3     | 500C A158h       |
| EPWM11_G0     | 5000 B158h       |
| EPWM11_G1     | 5004 B158h       |
| EPWM11_G2     | 5008 B158h       |
| EPWM11_G3     | 500C B158h       |
| EPWM12_G0     | 5000 C158h       |
| EPWM12_G1     | 5004 C158h       |
| EPWM12_G2     | 5008 C158h       |
| EPWM12_G3     | 500C C158h       |
| EPWM13_G0     | 5000 D158h       |
| EPWM13_G1     | 5004 D158h       |
| EPWM13_G2     | 5008 D158h       |
| EPWM13_G3     | 500C D158h       |
| EPWM14_G0     | 5000 E158h       |
| EPWM14_G1     | 5004 E158h       |
| EPWM14_G2     | 5008 E158h       |
| EPWM14_G3     | 500C E158h       |
| EPWM15_G0     | 5000 F158h       |
| EPWM15_G1     | 5004 F158h       |
| EPWM15_G2     | 5008 F158h       |
| EPWM15_G3     | 500C F158h       |
| EPWM16_G0     | 5001 0158h       |
| EPWM16_G1     | 5005 0158h       |
| EPWM16_G2     | 5009 0158h       |
| EPWM16_G3     | 500D 0158h       |
| EPWM17_G0     | 5001 1158h       |
| EPWM17_G1     | 5005 1158h       |
| EPWM17_G2     | 5009 1158h       |
| EPWM17_G3     | 500D 1158h       |
| EPWM18_G0     | 5001 2158h       |
| EPWM18_G1     | 5005 2158h       |
| EPWM18_G2     | 5009 2158h       |
| EPWM18_G3     | 500D 2158h       |
| EPWM19_G0     | 5001 3158h       |
| EPWM19_G1     | 5005 3158h       |
| EPWM19_G2     | 5009 3158h       |
| EPWM19_G3     | 500D 3158h       |
| EPWM20_G0     | 5001 4158h       |
| EPWM20_G1     | 5005 4158h       |
| EPWM20_G2     | 5009 4158h       |
| EPWM20_G3     | 500D 4158h       |



**Table 3-1015. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5158h       |
| EPWM21_G1     | 5005 5158h       |
| EPWM21_G2     | 5009 5158h       |
| EPWM21_G3     | 500D 5158h       |
| EPWM22_G0     | 5001 6158h       |
| EPWM22_G1     | 5005 6158h       |
| EPWM22_G2     | 5009 6158h       |
| EPWM22_G3     | 500D 6158h       |
| EPWM23_G0     | 5001 7158h       |
| EPWM23_G1     | 5005 7158h       |
| EPWM23_G2     | 5009 7158h       |
| EPWM23_G3     | 500D 7158h       |
| EPWM24_G0     | 5001 8158h       |
| EPWM24_G1     | 5005 8158h       |
| EPWM24_G2     | 5009 8158h       |
| EPWM24_G3     | 500D 8158h       |
| EPWM25_G0     | 5001 9158h       |
| EPWM25_G1     | 5005 9158h       |
| EPWM25_G2     | 5009 9158h       |
| EPWM25_G3     | 500D 9158h       |
| EPWM26_G0     | 5001 A158h       |
| EPWM26_G1     | 5005 A158h       |
| EPWM26_G2     | 5009 A158h       |
| EPWM26_G3     | 500D A158h       |
| EPWM27_G0     | 5001 B158h       |
| EPWM27_G1     | 5005 B158h       |
| EPWM27_G2     | 5009 B158h       |
| EPWM27_G3     | 500D B158h       |
| EPWM28_G0     | 5001 C158h       |
| EPWM28_G1     | 5005 C158h       |
| EPWM28_G2     | 5009 C158h       |
| EPWM28_G3     | 500D C158h       |
| EPWM29_G0     | 5001 D158h       |
| EPWM29_G1     | 5005 D158h       |
| EPWM29_G2     | 5009 D158h       |
| EPWM29_G3     | 500D D158h       |
| EPWM30_G0     | 5001 E158h       |
| EPWM30_G1     | 5005 E158h       |
| EPWM30_G2     | 5009 E158h       |
| EPWM30_G3     | 500D E158h       |
| EPWM31_G0     | 5001 F158h       |
| EPWM31_G1     | 5005 F158h       |
| EPWM31_G2     | 5009 F158h       |
| EPWM31_G3     | 500D F158h       |

**Figure 3-319. EPWM\_ETFRC Name Register**

|            |    |    |    |        |        |            |        |
|------------|----|----|----|--------|--------|------------|--------|
| 15         | 14 | 13 | 12 | 11     | 10     | 9          | 8      |
| RESERVED_2 |    |    |    |        |        |            |        |
| R          |    |    |    |        |        |            |        |
| 0h         |    |    |    |        |        |            |        |
| 7          | 6  | 5  | 4  | 3      | 2      | 1          | 0      |
| RESERVED_2 |    |    |    | SOCB   | SOCA   | RESERVED_1 | INT    |
| R          |    |    |    | R/W1TS | R/W1TS | R          | R/W1TS |
| 0h         |    |    |    | 0h     | 0h     | 0h         | 0h     |

**Table 3-1017. EPWM\_ETFRC Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                 |
|------|------------|--------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:4 | RESERVED_2 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                    |
| 3    | SOCB       | R/W1TS | 0h    | SOCB Force Bit<br>The SOCB pulse will only be generated if the event is enabled in the ETSEL register. The ETFLG[SOCB] flag bit will be set regardless.<br>0:Writing 0 to this bit will be ignored. Always reads back a 0.<br>1:Generates a pulse on EPWMxSOCB and set the SOCBFLG bit. This bit is used for test purposes. |
| 2    | SOCA       | R/W1TS | 0h    | SOCA Force Bit<br>The SOCA pulse will only be generated if the event is enabled in the ETSEL register. The ETFLG[SOCA] flag bit will be set regardless.<br>0:Writing 0 to this bit will be ignored. Always reads back a 0.<br>1:Generates a pulse on EPWMxSOCA and set the SOCAFLG bit. This bit is used for test purposes. |
| 1    | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                    |
| 0    | INT        | R/W1TS | 0h    | INT Force Bit<br>The interrupt will only be generated if the event is enabled in the ETSEL register. The INT flag bit will be set regardless.<br>0:Writing 0 to this bit will be ignored. Always reads back a 0.<br>1:Generates an interrupt on EPWMxINT and set the INT flag bit. This bit is used for test purposes.      |

### 3.7.2.69 EPWM\_ETINTPS Register

#### 1 EPWM\_ETINTPS Register (Offset = 15Ch) [reset = 0h]

Event-Trigger Interrupt Pre-Scale Register.

Return to [Summary Table](#)

**Table 3-1018. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 015Ch       |
| EPWM0_G1      | 5004 015Ch       |
| EPWM0_G2      | 5008 015Ch       |
| EPWM0_G3      | 500C 015Ch       |
| EPWM1_G0      | 5000 115Ch       |
| EPWM1_G1      | 5004 115Ch       |
| EPWM1_G2      | 5008 115Ch       |
| EPWM1_G3      | 500C 115Ch       |
| EPWM2_G0      | 5000 215Ch       |
| EPWM2_G1      | 5004 215Ch       |
| EPWM2_G2      | 5008 215Ch       |
| EPWM2_G3      | 500C 215Ch       |
| EPWM3_G0      | 5000 315Ch       |
| EPWM3_G1      | 5004 315Ch       |
| EPWM3_G2      | 5008 315Ch       |
| EPWM3_G3      | 500C 315Ch       |
| EPWM4_G0      | 5000 415Ch       |
| EPWM4_G1      | 5004 415Ch       |
| EPWM4_G2      | 5008 415Ch       |
| EPWM4_G3      | 500C 415Ch       |
| EPWM5_G0      | 5000 515Ch       |
| EPWM5_G1      | 5004 515Ch       |
| EPWM5_G2      | 5008 515Ch       |
| EPWM5_G3      | 500C 515Ch       |
| EPWM6_G0      | 5000 615Ch       |
| EPWM6_G1      | 5004 615Ch       |
| EPWM6_G2      | 5008 615Ch       |
| EPWM6_G3      | 500C 615Ch       |
| EPWM7_G0      | 5000 715Ch       |
| EPWM7_G1      | 5004 715Ch       |
| EPWM7_G2      | 5008 715Ch       |
| EPWM7_G3      | 500C 715Ch       |
| EPWM8_G0      | 5000 815Ch       |
| EPWM8_G1      | 5004 815Ch       |
| EPWM8_G2      | 5008 815Ch       |
| EPWM8_G3      | 500C 815Ch       |
| EPWM9_G0      | 5000 915Ch       |
| EPWM9_G1      | 5004 915Ch       |
| EPWM9_G2      | 5008 915Ch       |

**Table 3-1018. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 915Ch       |
| EPWM10_G0     | 5000 A15Ch       |
| EPWM10_G1     | 5004 A15Ch       |
| EPWM10_G2     | 5008 A15Ch       |
| EPWM10_G3     | 500C A15Ch       |
| EPWM11_G0     | 5000 B15Ch       |
| EPWM11_G1     | 5004 B15Ch       |
| EPWM11_G2     | 5008 B15Ch       |
| EPWM11_G3     | 500C B15Ch       |
| EPWM12_G0     | 5000 C15Ch       |
| EPWM12_G1     | 5004 C15Ch       |
| EPWM12_G2     | 5008 C15Ch       |
| EPWM12_G3     | 500C C15Ch       |
| EPWM13_G0     | 5000 D15Ch       |
| EPWM13_G1     | 5004 D15Ch       |
| EPWM13_G2     | 5008 D15Ch       |
| EPWM13_G3     | 500C D15Ch       |
| EPWM14_G0     | 5000 E15Ch       |
| EPWM14_G1     | 5004 E15Ch       |
| EPWM14_G2     | 5008 E15Ch       |
| EPWM14_G3     | 500C E15Ch       |
| EPWM15_G0     | 5000 F15Ch       |
| EPWM15_G1     | 5004 F15Ch       |
| EPWM15_G2     | 5008 F15Ch       |
| EPWM15_G3     | 500C F15Ch       |
| EPWM16_G0     | 5001 015Ch       |
| EPWM16_G1     | 5005 015Ch       |
| EPWM16_G2     | 5009 015Ch       |
| EPWM16_G3     | 500D 015Ch       |
| EPWM17_G0     | 5001 115Ch       |
| EPWM17_G1     | 5005 115Ch       |
| EPWM17_G2     | 5009 115Ch       |
| EPWM17_G3     | 500D 115Ch       |
| EPWM18_G0     | 5001 215Ch       |
| EPWM18_G1     | 5005 215Ch       |
| EPWM18_G2     | 5009 215Ch       |
| EPWM18_G3     | 500D 215Ch       |
| EPWM19_G0     | 5001 315Ch       |
| EPWM19_G1     | 5005 315Ch       |
| EPWM19_G2     | 5009 315Ch       |
| EPWM19_G3     | 500D 315Ch       |
| EPWM20_G0     | 5001 415Ch       |
| EPWM20_G1     | 5005 415Ch       |
| EPWM20_G2     | 5009 415Ch       |
| EPWM20_G3     | 500D 415Ch       |

**Table 3-1018. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 515Ch       |
| EPWM21_G1     | 5005 515Ch       |
| EPWM21_G2     | 5009 515Ch       |
| EPWM21_G3     | 500D 515Ch       |
| EPWM22_G0     | 5001 615Ch       |
| EPWM22_G1     | 5005 615Ch       |
| EPWM22_G2     | 5009 615Ch       |
| EPWM22_G3     | 500D 615Ch       |
| EPWM23_G0     | 5001 715Ch       |
| EPWM23_G1     | 5005 715Ch       |
| EPWM23_G2     | 5009 715Ch       |
| EPWM23_G3     | 500D 715Ch       |
| EPWM24_G0     | 5001 815Ch       |
| EPWM24_G1     | 5005 815Ch       |
| EPWM24_G2     | 5009 815Ch       |
| EPWM24_G3     | 500D 815Ch       |
| EPWM25_G0     | 5001 915Ch       |
| EPWM25_G1     | 5005 915Ch       |
| EPWM25_G2     | 5009 915Ch       |
| EPWM25_G3     | 500D 915Ch       |
| EPWM26_G0     | 5001 A15Ch       |
| EPWM26_G1     | 5005 A15Ch       |
| EPWM26_G2     | 5009 A15Ch       |
| EPWM26_G3     | 500D A15Ch       |
| EPWM27_G0     | 5001 B15Ch       |
| EPWM27_G1     | 5005 B15Ch       |
| EPWM27_G2     | 5009 B15Ch       |
| EPWM27_G3     | 500D B15Ch       |
| EPWM28_G0     | 5001 C15Ch       |
| EPWM28_G1     | 5005 C15Ch       |
| EPWM28_G2     | 5009 C15Ch       |
| EPWM28_G3     | 500D C15Ch       |
| EPWM29_G0     | 5001 D15Ch       |
| EPWM29_G1     | 5005 D15Ch       |
| EPWM29_G2     | 5009 D15Ch       |
| EPWM29_G3     | 500D D15Ch       |
| EPWM30_G0     | 5001 E15Ch       |
| EPWM30_G1     | 5005 E15Ch       |
| EPWM30_G2     | 5009 E15Ch       |
| EPWM30_G3     | 500D E15Ch       |
| EPWM31_G0     | 5001 F15Ch       |
| EPWM31_G1     | 5005 F15Ch       |
| EPWM31_G2     | 5009 F15Ch       |
| EPWM31_G3     | 500D F15Ch       |

**Figure 3-320. EPWM\_ETINTPS Name Register**

|            |    |    |    |         |    |   |   |
|------------|----|----|----|---------|----|---|---|
| 15         | 14 | 13 | 12 | 11      | 10 | 9 | 8 |
| RESERVED_1 |    |    |    |         |    |   |   |
| R          |    |    |    |         |    |   |   |
| 0h         |    |    |    |         |    |   |   |
| 7          | 6  | 5  | 4  | 3       | 2  | 1 | 0 |
| INTCNT2    |    |    |    | INTPRD2 |    |   |   |
| R          |    |    |    | R/W     |    |   |   |
| 0h         |    |    |    | 0h      |    |   |   |

**Table 3-1020. EPWM\_ETINTPS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 7:4  | INTCNT2    | R    | 0h    | EPWMxINT Counter 2<br>When ETPS[INTPSSEL]=1, these bits indicate how many selected events have occurred:<br>0000 No events<br>0001 1 event<br>0010 2 events<br>0011 3 events<br>0100 4 events<br>...<br>1111 15 events                                                                                                                                                                                                                                                   |
| 3:0  | INTPRD2    | R/W  | 0h    | EPWMxINT Period 2 Select<br>When ETPS[INTPSSEL] = 1, these bits select how many selected events need to occur before an interrupt is generated:<br>0000 Disable counter<br>0001 Generate interrupt on INTCNT = 1 [first event]<br>0010 Generate interrupt on INTCNT = 2 [second event]<br>0011 Generate interrupt on INTCNT = 3 [third event]<br>0100 Generate interrupt on INTCNT = 4 [fourth event]<br>...<br>1111 Generate interrupt on INTCNT = 15 [fifteenth event] |

### 3.7.2.70 EPWM\_ETSOCPS Register

#### 1 EPWM\_ETSOCPS Register (Offset = 160h) [reset = 0h]

Event-Trigger SOC Pre-Scale Register.

Return to [Summary Table](#)

**Table 3-1021. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0160h       |
| EPWM0_G1      | 5004 0160h       |
| EPWM0_G2      | 5008 0160h       |
| EPWM0_G3      | 500C 0160h       |
| EPWM1_G0      | 5000 1160h       |
| EPWM1_G1      | 5004 1160h       |
| EPWM1_G2      | 5008 1160h       |
| EPWM1_G3      | 500C 1160h       |
| EPWM2_G0      | 5000 2160h       |
| EPWM2_G1      | 5004 2160h       |
| EPWM2_G2      | 5008 2160h       |
| EPWM2_G3      | 500C 2160h       |
| EPWM3_G0      | 5000 3160h       |
| EPWM3_G1      | 5004 3160h       |
| EPWM3_G2      | 5008 3160h       |
| EPWM3_G3      | 500C 3160h       |
| EPWM4_G0      | 5000 4160h       |
| EPWM4_G1      | 5004 4160h       |
| EPWM4_G2      | 5008 4160h       |
| EPWM4_G3      | 500C 4160h       |
| EPWM5_G0      | 5000 5160h       |
| EPWM5_G1      | 5004 5160h       |
| EPWM5_G2      | 5008 5160h       |
| EPWM5_G3      | 500C 5160h       |
| EPWM6_G0      | 5000 6160h       |
| EPWM6_G1      | 5004 6160h       |
| EPWM6_G2      | 5008 6160h       |
| EPWM6_G3      | 500C 6160h       |
| EPWM7_G0      | 5000 7160h       |
| EPWM7_G1      | 5004 7160h       |
| EPWM7_G2      | 5008 7160h       |
| EPWM7_G3      | 500C 7160h       |
| EPWM8_G0      | 5000 8160h       |
| EPWM8_G1      | 5004 8160h       |
| EPWM8_G2      | 5008 8160h       |
| EPWM8_G3      | 500C 8160h       |
| EPWM9_G0      | 5000 9160h       |
| EPWM9_G1      | 5004 9160h       |
| EPWM9_G2      | 5008 9160h       |

**Table 3-1021. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9160h       |
| EPWM10_G0     | 5000 A160h       |
| EPWM10_G1     | 5004 A160h       |
| EPWM10_G2     | 5008 A160h       |
| EPWM10_G3     | 500C A160h       |
| EPWM11_G0     | 5000 B160h       |
| EPWM11_G1     | 5004 B160h       |
| EPWM11_G2     | 5008 B160h       |
| EPWM11_G3     | 500C B160h       |
| EPWM12_G0     | 5000 C160h       |
| EPWM12_G1     | 5004 C160h       |
| EPWM12_G2     | 5008 C160h       |
| EPWM12_G3     | 500C C160h       |
| EPWM13_G0     | 5000 D160h       |
| EPWM13_G1     | 5004 D160h       |
| EPWM13_G2     | 5008 D160h       |
| EPWM13_G3     | 500C D160h       |
| EPWM14_G0     | 5000 E160h       |
| EPWM14_G1     | 5004 E160h       |
| EPWM14_G2     | 5008 E160h       |
| EPWM14_G3     | 500C E160h       |
| EPWM15_G0     | 5000 F160h       |
| EPWM15_G1     | 5004 F160h       |
| EPWM15_G2     | 5008 F160h       |
| EPWM15_G3     | 500C F160h       |
| EPWM16_G0     | 5001 0160h       |
| EPWM16_G1     | 5005 0160h       |
| EPWM16_G2     | 5009 0160h       |
| EPWM16_G3     | 500D 0160h       |
| EPWM17_G0     | 5001 1160h       |
| EPWM17_G1     | 5005 1160h       |
| EPWM17_G2     | 5009 1160h       |
| EPWM17_G3     | 500D 1160h       |
| EPWM18_G0     | 5001 2160h       |
| EPWM18_G1     | 5005 2160h       |
| EPWM18_G2     | 5009 2160h       |
| EPWM18_G3     | 500D 2160h       |
| EPWM19_G0     | 5001 3160h       |
| EPWM19_G1     | 5005 3160h       |
| EPWM19_G2     | 5009 3160h       |
| EPWM19_G3     | 500D 3160h       |
| EPWM20_G0     | 5001 4160h       |
| EPWM20_G1     | 5005 4160h       |
| EPWM20_G2     | 5009 4160h       |
| EPWM20_G3     | 500D 4160h       |



**Table 3-1021. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5160h       |
| EPWM21_G1     | 5005 5160h       |
| EPWM21_G2     | 5009 5160h       |
| EPWM21_G3     | 500D 5160h       |
| EPWM22_G0     | 5001 6160h       |
| EPWM22_G1     | 5005 6160h       |
| EPWM22_G2     | 5009 6160h       |
| EPWM22_G3     | 500D 6160h       |
| EPWM23_G0     | 5001 7160h       |
| EPWM23_G1     | 5005 7160h       |
| EPWM23_G2     | 5009 7160h       |
| EPWM23_G3     | 500D 7160h       |
| EPWM24_G0     | 5001 8160h       |
| EPWM24_G1     | 5005 8160h       |
| EPWM24_G2     | 5009 8160h       |
| EPWM24_G3     | 500D 8160h       |
| EPWM25_G0     | 5001 9160h       |
| EPWM25_G1     | 5005 9160h       |
| EPWM25_G2     | 5009 9160h       |
| EPWM25_G3     | 500D 9160h       |
| EPWM26_G0     | 5001 A160h       |
| EPWM26_G1     | 5005 A160h       |
| EPWM26_G2     | 5009 A160h       |
| EPWM26_G3     | 500D A160h       |
| EPWM27_G0     | 5001 B160h       |
| EPWM27_G1     | 5005 B160h       |
| EPWM27_G2     | 5009 B160h       |
| EPWM27_G3     | 500D B160h       |
| EPWM28_G0     | 5001 C160h       |
| EPWM28_G1     | 5005 C160h       |
| EPWM28_G2     | 5009 C160h       |
| EPWM28_G3     | 500D C160h       |
| EPWM29_G0     | 5001 D160h       |
| EPWM29_G1     | 5005 D160h       |
| EPWM29_G2     | 5009 D160h       |
| EPWM29_G3     | 500D D160h       |
| EPWM30_G0     | 5001 E160h       |
| EPWM30_G1     | 5005 E160h       |
| EPWM30_G2     | 5009 E160h       |
| EPWM30_G3     | 500D E160h       |
| EPWM31_G0     | 5001 F160h       |
| EPWM31_G1     | 5005 F160h       |
| EPWM31_G2     | 5009 F160h       |
| EPWM31_G3     | 500D F160h       |

**Figure 3-321. EPWM\_ETSOCPS Name Register**

| 15       | 14 | 13 | 12 | 11       | 10 | 9 | 8 |
|----------|----|----|----|----------|----|---|---|
| SOCBCNT2 |    |    |    | SOCBPRD2 |    |   |   |
| R        |    |    |    | R/W      |    |   |   |
| 0h       |    |    |    | 0h       |    |   |   |
| 7        | 6  | 5  | 4  | 3        | 2  | 1 | 0 |
| SOCACNT2 |    |    |    | SOCAPRD2 |    |   |   |
| R        |    |    |    | R/W      |    |   |   |
| 0h       |    |    |    | 0h       |    |   |   |

**Table 3-1023. EPWM\_ETSOCPS Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | SOCBCNT2 | R    | 0h    | EPWMxSOCB Counter 2<br>When ETPS[SOCPSSEL] = 1, these bits indicate how many selected events have occurred:<br>0000 No events<br>0001 1 event<br>0010 2 events<br>0011 3 events<br>0100 4 events<br>...<br>1111 15 events                                                                                                                                                                                                                                                           |
| 11:8  | SOCBPRD2 | R/W  | 0h    | EPWMxSOCB Period 2 Select<br>When ETPS[SOCPSSEL] = 1, these bits select how many selected event need to occur before an SOCB pulse is generated:<br>0000 Disable counter<br>0001 Generate interrupt on SOCBCNT2 = 1 [first event]<br>0010 Generate interrupt on SOCBCNT2 = 2 [second event]<br>0011 Generate interrupt on SOCBCNT2 = 3 [third event]<br>0100 Generate interrupt on SOCBCNT2 = 4 [fourth event]<br>...<br>1111 Generate interrupt on SOCBCNT2 = 15 [fifteenth event] |
| 7:4   | SOCACNT2 | R    | 0h    | EPWMxSOCA Counter 2<br>When ETPS[SOCPSSEL] = 1, these bits indicate how many selected events have occurred:<br>0000 No events<br>0001 1 event<br>0010 2 events<br>0011 3 events<br>0100 4 events<br>...<br>1111 15 events                                                                                                                                                                                                                                                           |
| 3:0   | SOCAPRD2 | R/W  | 0h    | EPWMxSOCA Period 2 Select<br>When ETPS[SOCPSSEL] = 1, these bits select how many selected event need to occur before an SOCA pulse is generated:<br>0000 Disable counter<br>0001 Generate interrupt on SOCACNT2 = 1 [first event]<br>0010 Generate interrupt on SOCACNT2 = 2 [second event]<br>0011 Generate interrupt on SOCACNT2 = 3 [third event]<br>0100 Generate interrupt on SOCACNT2 = 4 [fourth event]<br>...<br>1111 Generate interrupt on SOCACNT2 = 15 [fifteenth event] |

### 3.7.2.71 EPWM\_ETCNTINITCTL Register

#### 1 EPWM\_ETCNTINITCTL Register (Offset = 164h) [reset = 0h]

Event-Trigger Counter Initialization Control Register.

Return to [Summary Table](#)

**Table 3-1024. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0164h       |
| EPWM0_G1      | 5004 0164h       |
| EPWM0_G2      | 5008 0164h       |
| EPWM0_G3      | 500C 0164h       |
| EPWM1_G0      | 5000 1164h       |
| EPWM1_G1      | 5004 1164h       |
| EPWM1_G2      | 5008 1164h       |
| EPWM1_G3      | 500C 1164h       |
| EPWM2_G0      | 5000 2164h       |
| EPWM2_G1      | 5004 2164h       |
| EPWM2_G2      | 5008 2164h       |
| EPWM2_G3      | 500C 2164h       |
| EPWM3_G0      | 5000 3164h       |
| EPWM3_G1      | 5004 3164h       |
| EPWM3_G2      | 5008 3164h       |
| EPWM3_G3      | 500C 3164h       |
| EPWM4_G0      | 5000 4164h       |
| EPWM4_G1      | 5004 4164h       |
| EPWM4_G2      | 5008 4164h       |
| EPWM4_G3      | 500C 4164h       |
| EPWM5_G0      | 5000 5164h       |
| EPWM5_G1      | 5004 5164h       |
| EPWM5_G2      | 5008 5164h       |
| EPWM5_G3      | 500C 5164h       |
| EPWM6_G0      | 5000 6164h       |
| EPWM6_G1      | 5004 6164h       |
| EPWM6_G2      | 5008 6164h       |
| EPWM6_G3      | 500C 6164h       |
| EPWM7_G0      | 5000 7164h       |
| EPWM7_G1      | 5004 7164h       |
| EPWM7_G2      | 5008 7164h       |
| EPWM7_G3      | 500C 7164h       |
| EPWM8_G0      | 5000 8164h       |
| EPWM8_G1      | 5004 8164h       |
| EPWM8_G2      | 5008 8164h       |
| EPWM8_G3      | 500C 8164h       |
| EPWM9_G0      | 5000 9164h       |
| EPWM9_G1      | 5004 9164h       |
| EPWM9_G2      | 5008 9164h       |

**Table 3-1024. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9164h       |
| EPWM10_G0     | 5000 A164h       |
| EPWM10_G1     | 5004 A164h       |
| EPWM10_G2     | 5008 A164h       |
| EPWM10_G3     | 500C A164h       |
| EPWM11_G0     | 5000 B164h       |
| EPWM11_G1     | 5004 B164h       |
| EPWM11_G2     | 5008 B164h       |
| EPWM11_G3     | 500C B164h       |
| EPWM12_G0     | 5000 C164h       |
| EPWM12_G1     | 5004 C164h       |
| EPWM12_G2     | 5008 C164h       |
| EPWM12_G3     | 500C C164h       |
| EPWM13_G0     | 5000 D164h       |
| EPWM13_G1     | 5004 D164h       |
| EPWM13_G2     | 5008 D164h       |
| EPWM13_G3     | 500C D164h       |
| EPWM14_G0     | 5000 E164h       |
| EPWM14_G1     | 5004 E164h       |
| EPWM14_G2     | 5008 E164h       |
| EPWM14_G3     | 500C E164h       |
| EPWM15_G0     | 5000 F164h       |
| EPWM15_G1     | 5004 F164h       |
| EPWM15_G2     | 5008 F164h       |
| EPWM15_G3     | 500C F164h       |
| EPWM16_G0     | 5001 0164h       |
| EPWM16_G1     | 5005 0164h       |
| EPWM16_G2     | 5009 0164h       |
| EPWM16_G3     | 500D 0164h       |
| EPWM17_G0     | 5001 1164h       |
| EPWM17_G1     | 5005 1164h       |
| EPWM17_G2     | 5009 1164h       |
| EPWM17_G3     | 500D 1164h       |
| EPWM18_G0     | 5001 2164h       |
| EPWM18_G1     | 5005 2164h       |
| EPWM18_G2     | 5009 2164h       |
| EPWM18_G3     | 500D 2164h       |
| EPWM19_G0     | 5001 3164h       |
| EPWM19_G1     | 5005 3164h       |
| EPWM19_G2     | 5009 3164h       |
| EPWM19_G3     | 500D 3164h       |
| EPWM20_G0     | 5001 4164h       |
| EPWM20_G1     | 5005 4164h       |
| EPWM20_G2     | 5009 4164h       |
| EPWM20_G3     | 500D 4164h       |

**Table 3-1024. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5164h       |
| EPWM21_G1     | 5005 5164h       |
| EPWM21_G2     | 5009 5164h       |
| EPWM21_G3     | 500D 5164h       |
| EPWM22_G0     | 5001 6164h       |
| EPWM22_G1     | 5005 6164h       |
| EPWM22_G2     | 5009 6164h       |
| EPWM22_G3     | 500D 6164h       |
| EPWM23_G0     | 5001 7164h       |
| EPWM23_G1     | 5005 7164h       |
| EPWM23_G2     | 5009 7164h       |
| EPWM23_G3     | 500D 7164h       |
| EPWM24_G0     | 5001 8164h       |
| EPWM24_G1     | 5005 8164h       |
| EPWM24_G2     | 5009 8164h       |
| EPWM24_G3     | 500D 8164h       |
| EPWM25_G0     | 5001 9164h       |
| EPWM25_G1     | 5005 9164h       |
| EPWM25_G2     | 5009 9164h       |
| EPWM25_G3     | 500D 9164h       |
| EPWM26_G0     | 5001 A164h       |
| EPWM26_G1     | 5005 A164h       |
| EPWM26_G2     | 5009 A164h       |
| EPWM26_G3     | 500D A164h       |
| EPWM27_G0     | 5001 B164h       |
| EPWM27_G1     | 5005 B164h       |
| EPWM27_G2     | 5009 B164h       |
| EPWM27_G3     | 500D B164h       |
| EPWM28_G0     | 5001 C164h       |
| EPWM28_G1     | 5005 C164h       |
| EPWM28_G2     | 5009 C164h       |
| EPWM28_G3     | 500D C164h       |
| EPWM29_G0     | 5001 D164h       |
| EPWM29_G1     | 5005 D164h       |
| EPWM29_G2     | 5009 D164h       |
| EPWM29_G3     | 500D D164h       |
| EPWM30_G0     | 5001 E164h       |
| EPWM30_G1     | 5005 E164h       |
| EPWM30_G2     | 5009 E164h       |
| EPWM30_G3     | 500D E164h       |
| EPWM31_G0     | 5001 F164h       |
| EPWM31_G1     | 5005 F164h       |
| EPWM31_G2     | 5009 F164h       |
| EPWM31_G3     | 500D F164h       |

**Figure 3-322. EPWM\_ETCNTINITCTL Name Register**

| 15         | 14         | 13        | 12          | 11          | 10         | 9          | 8 |
|------------|------------|-----------|-------------|-------------|------------|------------|---|
| SOCBINITEN | SOCAINITEN | INTINITEN | SOCBINITFRC | SOCAINITFRC | INTINITFRC | RESERVED_1 |   |
| R/W        | R/W        | R/W       | R/W1TS      | R/W1TS      | R/W1TS     | R          |   |
| 0h         | 0h         | 0h        | 0h          | 0h          | 0h         | 0h         |   |
| 7          | 6          | 5         | 4           | 3           | 2          | 1          | 0 |
| RESERVED_1 |            |           |             |             |            |            |   |
| R          |            |           |             |             |            |            |   |
| 0h         |            |           |             |             |            |            |   |

**Table 3-1026. EPWM\_ETCNTINITCTL Register Field Descriptions**

| Bit | Field       | Type   | Reset | Description                                                                                                                                                                           |
|-----|-------------|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | SOCBINITEN  | R/W    | 0h    | EPWMxSOCB Counter 2 Initialization Enable<br>0:Has no effect.<br>1:Enable initialization of EPWMxSOCB counter with contents of ETCNTINIT[SOCBINIT] on a SYNC event or software force. |
| 14  | SOCAINITEN  | R/W    | 0h    | EPWMxSOCA Counter 2 Initialization Enable<br>0:Has no effect.<br>1:Enable initialization of EPWMxSOCA counter with contents of ETCNTINIT[SOCAINIT] on a SYNC event or software force. |
| 13  | INTINITEN   | R/W    | 0h    | EPWMxINT Counter 2 Initialization Enable<br>0:Has no effect.<br>1:Enable initialization of EPWMxINT counter 2 with contents of ETCNTINIT[INTINIT] on a SYNC event or software force.  |
| 12  | SOCBINITFRC | R/W1TS | 0h    | EPWMxSOCB Counter 2 Initialization Force<br>0:Has no effect.<br>1:This bit forces the ET EPWMxSOCB counter to be initialized with the contents of ETCNTINIT[SOCBINIT].                |
| 11  | SOCAINITFRC | R/W1TS | 0h    | EPWMxSOCA Counter 2 Initialization Force<br>0:Has no effect.<br>1:This bit forces the ET EPWMxSOCA counter to be initialized with the contents of ETCNTINIT[SOCAINIT].                |
| 10  | INTINITFRC  | R/W1TS | 0h    | EPWMxINT Counter 2 Initialization Force<br>0:Has no effect.<br>1:This bit forces the ET EPWMxINT counter to be initialized with the contents of ETCNTINIT[INTINIT].                   |
| 9:0 | RESERVED_1  | R      | 0h    | Reserved                                                                                                                                                                              |

### 3.7.2.72 EPWM\_ETCNTINIT Register

#### 1 EPWM\_ETCNTINIT Register (Offset = 168h) [reset = 0h]

Event-Trigger Counter Initialization Register.

Return to [Summary Table](#)

**Table 3-1027. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0168h       |
| EPWM0_G1      | 5004 0168h       |
| EPWM0_G2      | 5008 0168h       |
| EPWM0_G3      | 500C 0168h       |
| EPWM1_G0      | 5000 1168h       |
| EPWM1_G1      | 5004 1168h       |
| EPWM1_G2      | 5008 1168h       |
| EPWM1_G3      | 500C 1168h       |
| EPWM2_G0      | 5000 2168h       |
| EPWM2_G1      | 5004 2168h       |
| EPWM2_G2      | 5008 2168h       |
| EPWM2_G3      | 500C 2168h       |
| EPWM3_G0      | 5000 3168h       |
| EPWM3_G1      | 5004 3168h       |
| EPWM3_G2      | 5008 3168h       |
| EPWM3_G3      | 500C 3168h       |
| EPWM4_G0      | 5000 4168h       |
| EPWM4_G1      | 5004 4168h       |
| EPWM4_G2      | 5008 4168h       |
| EPWM4_G3      | 500C 4168h       |
| EPWM5_G0      | 5000 5168h       |
| EPWM5_G1      | 5004 5168h       |
| EPWM5_G2      | 5008 5168h       |
| EPWM5_G3      | 500C 5168h       |
| EPWM6_G0      | 5000 6168h       |
| EPWM6_G1      | 5004 6168h       |
| EPWM6_G2      | 5008 6168h       |
| EPWM6_G3      | 500C 6168h       |
| EPWM7_G0      | 5000 7168h       |
| EPWM7_G1      | 5004 7168h       |
| EPWM7_G2      | 5008 7168h       |
| EPWM7_G3      | 500C 7168h       |
| EPWM8_G0      | 5000 8168h       |
| EPWM8_G1      | 5004 8168h       |
| EPWM8_G2      | 5008 8168h       |
| EPWM8_G3      | 500C 8168h       |
| EPWM9_G0      | 5000 9168h       |
| EPWM9_G1      | 5004 9168h       |
| EPWM9_G2      | 5008 9168h       |

**Table 3-1027. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9168h       |
| EPWM10_G0     | 5000 A168h       |
| EPWM10_G1     | 5004 A168h       |
| EPWM10_G2     | 5008 A168h       |
| EPWM10_G3     | 500C A168h       |
| EPWM11_G0     | 5000 B168h       |
| EPWM11_G1     | 5004 B168h       |
| EPWM11_G2     | 5008 B168h       |
| EPWM11_G3     | 500C B168h       |
| EPWM12_G0     | 5000 C168h       |
| EPWM12_G1     | 5004 C168h       |
| EPWM12_G2     | 5008 C168h       |
| EPWM12_G3     | 500C C168h       |
| EPWM13_G0     | 5000 D168h       |
| EPWM13_G1     | 5004 D168h       |
| EPWM13_G2     | 5008 D168h       |
| EPWM13_G3     | 500C D168h       |
| EPWM14_G0     | 5000 E168h       |
| EPWM14_G1     | 5004 E168h       |
| EPWM14_G2     | 5008 E168h       |
| EPWM14_G3     | 500C E168h       |
| EPWM15_G0     | 5000 F168h       |
| EPWM15_G1     | 5004 F168h       |
| EPWM15_G2     | 5008 F168h       |
| EPWM15_G3     | 500C F168h       |
| EPWM16_G0     | 5001 0168h       |
| EPWM16_G1     | 5005 0168h       |
| EPWM16_G2     | 5009 0168h       |
| EPWM16_G3     | 500D 0168h       |
| EPWM17_G0     | 5001 1168h       |
| EPWM17_G1     | 5005 1168h       |
| EPWM17_G2     | 5009 1168h       |
| EPWM17_G3     | 500D 1168h       |
| EPWM18_G0     | 5001 2168h       |
| EPWM18_G1     | 5005 2168h       |
| EPWM18_G2     | 5009 2168h       |
| EPWM18_G3     | 500D 2168h       |
| EPWM19_G0     | 5001 3168h       |
| EPWM19_G1     | 5005 3168h       |
| EPWM19_G2     | 5009 3168h       |
| EPWM19_G3     | 500D 3168h       |
| EPWM20_G0     | 5001 4168h       |
| EPWM20_G1     | 5005 4168h       |
| EPWM20_G2     | 5009 4168h       |
| EPWM20_G3     | 500D 4168h       |



**Table 3-1027. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5168h       |
| EPWM21_G1     | 5005 5168h       |
| EPWM21_G2     | 5009 5168h       |
| EPWM21_G3     | 500D 5168h       |
| EPWM22_G0     | 5001 6168h       |
| EPWM22_G1     | 5005 6168h       |
| EPWM22_G2     | 5009 6168h       |
| EPWM22_G3     | 500D 6168h       |
| EPWM23_G0     | 5001 7168h       |
| EPWM23_G1     | 5005 7168h       |
| EPWM23_G2     | 5009 7168h       |
| EPWM23_G3     | 500D 7168h       |
| EPWM24_G0     | 5001 8168h       |
| EPWM24_G1     | 5005 8168h       |
| EPWM24_G2     | 5009 8168h       |
| EPWM24_G3     | 500D 8168h       |
| EPWM25_G0     | 5001 9168h       |
| EPWM25_G1     | 5005 9168h       |
| EPWM25_G2     | 5009 9168h       |
| EPWM25_G3     | 500D 9168h       |
| EPWM26_G0     | 5001 A168h       |
| EPWM26_G1     | 5005 A168h       |
| EPWM26_G2     | 5009 A168h       |
| EPWM26_G3     | 500D A168h       |
| EPWM27_G0     | 5001 B168h       |
| EPWM27_G1     | 5005 B168h       |
| EPWM27_G2     | 5009 B168h       |
| EPWM27_G3     | 500D B168h       |
| EPWM28_G0     | 5001 C168h       |
| EPWM28_G1     | 5005 C168h       |
| EPWM28_G2     | 5009 C168h       |
| EPWM28_G3     | 500D C168h       |
| EPWM29_G0     | 5001 D168h       |
| EPWM29_G1     | 5005 D168h       |
| EPWM29_G2     | 5009 D168h       |
| EPWM29_G3     | 500D D168h       |
| EPWM30_G0     | 5001 E168h       |
| EPWM30_G1     | 5005 E168h       |
| EPWM30_G2     | 5009 E168h       |
| EPWM30_G3     | 500D E168h       |
| EPWM31_G0     | 5001 F168h       |
| EPWM31_G1     | 5005 F168h       |
| EPWM31_G2     | 5009 F168h       |
| EPWM31_G3     | 500D F168h       |

**Figure 3-323. EPWM\_ETCNTINIT Name Register**

| 15         | 14 | 13 | 12 | 11       | 10 | 9 | 8 |
|------------|----|----|----|----------|----|---|---|
| RESERVED_1 |    |    |    | SOCBINIT |    |   |   |
| R          |    |    |    | R/W      |    |   |   |
| 0h         |    |    |    | 0h       |    |   |   |
| 7          | 6  | 5  | 4  | 3        | 2  | 1 | 0 |
| SOCAINIT   |    |    |    | INTINIT  |    |   |   |
| R/W        |    |    |    | R/W      |    |   |   |
| 0h         |    |    |    | 0h       |    |   |   |

**Table 3-1029. EPWM\_ETCNTINIT Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                      |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                         |
| 11:8  | SOCBINIT   | R/W  | 0h    | EPWMxSOCB Counter 2 Initialization Bits<br>The ET EPWMxSOCB counter is initialized with the contents of this register on an EPWM SYNC event or a software force. |
| 7:4   | SOCAINIT   | R/W  | 0h    | EPWMxSOCA Counter 2 Initialization Bits<br>The ET EPWMxSOCA counter is initialized with the contents of this register on an EPWM SYNC event or a software force. |
| 3:0   | INTINIT    | R/W  | 0h    | EPWMxINT Counter 2 Initialization Bits<br>The ET EPWMxINT counter is initialized with the contents of this register on an EPWM SYNC event or a software force.   |

### 3.7.2.73 EPWM\_ETINTMIXEN Register

#### 1 EPWM\_ETINTMIXEN Register (Offset = 16Ch) [reset = 3h]

Event-Trigger Mixed INT Selection.

Return to [Summary Table](#)

**Table 3-1030. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 016Ch       |
| EPWM0_G1      | 5004 016Ch       |
| EPWM0_G2      | 5008 016Ch       |
| EPWM0_G3      | 500C 016Ch       |
| EPWM1_G0      | 5000 116Ch       |
| EPWM1_G1      | 5004 116Ch       |
| EPWM1_G2      | 5008 116Ch       |
| EPWM1_G3      | 500C 116Ch       |
| EPWM2_G0      | 5000 216Ch       |
| EPWM2_G1      | 5004 216Ch       |
| EPWM2_G2      | 5008 216Ch       |
| EPWM2_G3      | 500C 216Ch       |
| EPWM3_G0      | 5000 316Ch       |
| EPWM3_G1      | 5004 316Ch       |
| EPWM3_G2      | 5008 316Ch       |
| EPWM3_G3      | 500C 316Ch       |
| EPWM4_G0      | 5000 416Ch       |
| EPWM4_G1      | 5004 416Ch       |
| EPWM4_G2      | 5008 416Ch       |
| EPWM4_G3      | 500C 416Ch       |
| EPWM5_G0      | 5000 516Ch       |
| EPWM5_G1      | 5004 516Ch       |
| EPWM5_G2      | 5008 516Ch       |
| EPWM5_G3      | 500C 516Ch       |
| EPWM6_G0      | 5000 616Ch       |
| EPWM6_G1      | 5004 616Ch       |
| EPWM6_G2      | 5008 616Ch       |
| EPWM6_G3      | 500C 616Ch       |
| EPWM7_G0      | 5000 716Ch       |
| EPWM7_G1      | 5004 716Ch       |
| EPWM7_G2      | 5008 716Ch       |
| EPWM7_G3      | 500C 716Ch       |
| EPWM8_G0      | 5000 816Ch       |
| EPWM8_G1      | 5004 816Ch       |
| EPWM8_G2      | 5008 816Ch       |
| EPWM8_G3      | 500C 816Ch       |
| EPWM9_G0      | 5000 916Ch       |
| EPWM9_G1      | 5004 916Ch       |
| EPWM9_G2      | 5008 916Ch       |

**Table 3-1030. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 916Ch       |
| EPWM10_G0     | 5000 A16Ch       |
| EPWM10_G1     | 5004 A16Ch       |
| EPWM10_G2     | 5008 A16Ch       |
| EPWM10_G3     | 500C A16Ch       |
| EPWM11_G0     | 5000 B16Ch       |
| EPWM11_G1     | 5004 B16Ch       |
| EPWM11_G2     | 5008 B16Ch       |
| EPWM11_G3     | 500C B16Ch       |
| EPWM12_G0     | 5000 C16Ch       |
| EPWM12_G1     | 5004 C16Ch       |
| EPWM12_G2     | 5008 C16Ch       |
| EPWM12_G3     | 500C C16Ch       |
| EPWM13_G0     | 5000 D16Ch       |
| EPWM13_G1     | 5004 D16Ch       |
| EPWM13_G2     | 5008 D16Ch       |
| EPWM13_G3     | 500C D16Ch       |
| EPWM14_G0     | 5000 E16Ch       |
| EPWM14_G1     | 5004 E16Ch       |
| EPWM14_G2     | 5008 E16Ch       |
| EPWM14_G3     | 500C E16Ch       |
| EPWM15_G0     | 5000 F16Ch       |
| EPWM15_G1     | 5004 F16Ch       |
| EPWM15_G2     | 5008 F16Ch       |
| EPWM15_G3     | 500C F16Ch       |
| EPWM16_G0     | 5001 016Ch       |
| EPWM16_G1     | 5005 016Ch       |
| EPWM16_G2     | 5009 016Ch       |
| EPWM16_G3     | 500D 016Ch       |
| EPWM17_G0     | 5001 116Ch       |
| EPWM17_G1     | 5005 116Ch       |
| EPWM17_G2     | 5009 116Ch       |
| EPWM17_G3     | 500D 116Ch       |
| EPWM18_G0     | 5001 216Ch       |
| EPWM18_G1     | 5005 216Ch       |
| EPWM18_G2     | 5009 216Ch       |
| EPWM18_G3     | 500D 216Ch       |
| EPWM19_G0     | 5001 316Ch       |
| EPWM19_G1     | 5005 316Ch       |
| EPWM19_G2     | 5009 316Ch       |
| EPWM19_G3     | 500D 316Ch       |
| EPWM20_G0     | 5001 416Ch       |
| EPWM20_G1     | 5005 416Ch       |
| EPWM20_G2     | 5009 416Ch       |
| EPWM20_G3     | 500D 416Ch       |

**Table 3-1030. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 516Ch       |
| EPWM21_G1     | 5005 516Ch       |
| EPWM21_G2     | 5009 516Ch       |
| EPWM21_G3     | 500D 516Ch       |
| EPWM22_G0     | 5001 616Ch       |
| EPWM22_G1     | 5005 616Ch       |
| EPWM22_G2     | 5009 616Ch       |
| EPWM22_G3     | 500D 616Ch       |
| EPWM23_G0     | 5001 716Ch       |
| EPWM23_G1     | 5005 716Ch       |
| EPWM23_G2     | 5009 716Ch       |
| EPWM23_G3     | 500D 716Ch       |
| EPWM24_G0     | 5001 816Ch       |
| EPWM24_G1     | 5005 816Ch       |
| EPWM24_G2     | 5009 816Ch       |
| EPWM24_G3     | 500D 816Ch       |
| EPWM25_G0     | 5001 916Ch       |
| EPWM25_G1     | 5005 916Ch       |
| EPWM25_G2     | 5009 916Ch       |
| EPWM25_G3     | 500D 916Ch       |
| EPWM26_G0     | 5001 A16Ch       |
| EPWM26_G1     | 5005 A16Ch       |
| EPWM26_G2     | 5009 A16Ch       |
| EPWM26_G3     | 500D A16Ch       |
| EPWM27_G0     | 5001 B16Ch       |
| EPWM27_G1     | 5005 B16Ch       |
| EPWM27_G2     | 5009 B16Ch       |
| EPWM27_G3     | 500D B16Ch       |
| EPWM28_G0     | 5001 C16Ch       |
| EPWM28_G1     | 5005 C16Ch       |
| EPWM28_G2     | 5009 C16Ch       |
| EPWM28_G3     | 500D C16Ch       |
| EPWM29_G0     | 5001 D16Ch       |
| EPWM29_G1     | 5005 D16Ch       |
| EPWM29_G2     | 5009 D16Ch       |
| EPWM29_G3     | 500D D16Ch       |
| EPWM30_G0     | 5001 E16Ch       |
| EPWM30_G1     | 5005 E16Ch       |
| EPWM30_G2     | 5009 E16Ch       |
| EPWM30_G3     | 500D E16Ch       |
| EPWM31_G0     | 5001 F16Ch       |
| EPWM31_G1     | 5005 F16Ch       |
| EPWM31_G2     | 5009 F16Ch       |
| EPWM31_G3     | 500D F16Ch       |

**Figure 3-324. EPWM\_ETINTMIXEN Name Register**

| 15         | 14  | 13  | 12  | 11  | 10      | 9   | 8   |
|------------|-----|-----|-----|-----|---------|-----|-----|
| RESERVED_1 |     |     |     |     | DCAEVT1 | CDD | CDU |
| R          |     |     |     |     | R/W     | R/W | R/W |
| 0h         |     |     |     |     | 0h      | 0h  | 0h  |
| 7          | 6   | 5   | 4   | 3   | 2       | 1   | 0   |
| CCD        | CCU | CBD | CBU | CAD | CAU     | PRD | ZRO |
| R/W        | R/W | R/W | R/W | R/W | R/W     | R/W | R/W |
| 0h         | 0h  | 0h  | 0h  | 0h  | 0h      | 1h  | 1h  |

**Table 3-1032. EPWM\_ETINTMIXEN Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                            |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                               |
| 10    | DCAEVT1    | R/W  | 0h    | Enable DCAEVT1.inter to the mixed ET interrupt trigger signal [ETINTMIX].<br>0:DCAEVT1.soc event is not enabled<br>1:Enable DCAEVT1.soc event                                                                                          |
| 9     | CDD        | R/W  | 0h    | Enable event time-base counter equal to CMPD when the timer is decrementing to the mixed ET interrupt trigger signal [ETINTMIX].<br>0:CMPC down-count match enable event is not enabled<br>1:Enable CMPD down-count match enable event |
| 8     | CDU        | R/W  | 0h    | Enable event time-base counter equal to CMPD when the timer is incrementing to the mixed ET interrupt trigger signal [ETINTMIX].<br>0:CMPC up-count match enable event is not enabled<br>1:Enable CMPD up-count match enable event     |
| 7     | CCD        | R/W  | 0h    | Enable event time-base counter equal to CMPC when the timer is decrementing to the mixed ET interrupt trigger signal [ETINTMIX].<br>0:CMPC down-count match enable event is not enabled<br>1:Enable CMPC down-count match enable event |
| 6     | CCU        | R/W  | 0h    | Enable event time-base counter equal to CMPC when the timer is incrementing to the mixed ET interrupt trigger signal [ETINTMIX].<br>0:CMPC up-count match enable event is not enabled<br>1:Enable CMPC up-count match enable event     |
| 5     | CBD        | R/W  | 0h    | Enable event time-base counter equal to CMPB when the timer is decrementing to the mixed ET interrupt trigger signal [ETINTMIX].<br>0:CMPC down-count match enable event is not enabled<br>1:Enable CMPB down-count match enable event |
| 4     | CBU        | R/W  | 0h    | Enable event time-base counter equal to CMPB when the timer is incrementing to the mixed ET interrupt trigger signal [ETINTMIX].<br>0:CMPC up-count match enable event is not enabled<br>1:Enable CMPB up-count match enable event     |
| 3     | CAD        | R/W  | 0h    | Enable event time-base counter equal to CMPA when the timer is decrementing to the mixed ET interrupt trigger signal [ETINTMIX].<br>0:CMPC down-count match enable event is not enabled<br>1:Enable CMPA down-count match enable event |
| 2     | CAU        | R/W  | 0h    | Enable event time-base counter equal to CMPA when the timer is incrementing to the mixed ET interrupt trigger signal [ETINTMIX].<br>0:CMPC up-count match enable event is not enabled<br>1:Enable CMPA up-count match enable event     |
| 1     | PRD        | R/W  | 1h    | Enable event time-base counter equal to period [TBCTR = TBPRD] to the mixed ET interrupt trigger signal [ETINTMIX].<br>0:Period match event is not enabled<br>1:Enable period match event                                              |
| 0     | ZRO        | R/W  | 1h    | Enable event time-base counter equal to zero [TBCTR = 0x00] to the mixed ET interrupt trigger signal [ETINTMIX].<br>0:Zero match event is not enabled<br>1:Enable zero match event                                                     |

### 3.7.2.74 EPWM\_ETSOCAMIXEN Register

#### 1 EPWM\_ETSOCAMIXEN Register (Offset = 170h) [reset = 3h]

Event-Trigger Mixed SOCA Selection.

Return to [Summary Table](#)

**Table 3-1033. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0170h       |
| EPWM0_G1      | 5004 0170h       |
| EPWM0_G2      | 5008 0170h       |
| EPWM0_G3      | 500C 0170h       |
| EPWM1_G0      | 5000 1170h       |
| EPWM1_G1      | 5004 1170h       |
| EPWM1_G2      | 5008 1170h       |
| EPWM1_G3      | 500C 1170h       |
| EPWM2_G0      | 5000 2170h       |
| EPWM2_G1      | 5004 2170h       |
| EPWM2_G2      | 5008 2170h       |
| EPWM2_G3      | 500C 2170h       |
| EPWM3_G0      | 5000 3170h       |
| EPWM3_G1      | 5004 3170h       |
| EPWM3_G2      | 5008 3170h       |
| EPWM3_G3      | 500C 3170h       |
| EPWM4_G0      | 5000 4170h       |
| EPWM4_G1      | 5004 4170h       |
| EPWM4_G2      | 5008 4170h       |
| EPWM4_G3      | 500C 4170h       |
| EPWM5_G0      | 5000 5170h       |
| EPWM5_G1      | 5004 5170h       |
| EPWM5_G2      | 5008 5170h       |
| EPWM5_G3      | 500C 5170h       |
| EPWM6_G0      | 5000 6170h       |
| EPWM6_G1      | 5004 6170h       |
| EPWM6_G2      | 5008 6170h       |
| EPWM6_G3      | 500C 6170h       |
| EPWM7_G0      | 5000 7170h       |
| EPWM7_G1      | 5004 7170h       |
| EPWM7_G2      | 5008 7170h       |
| EPWM7_G3      | 500C 7170h       |
| EPWM8_G0      | 5000 8170h       |
| EPWM8_G1      | 5004 8170h       |
| EPWM8_G2      | 5008 8170h       |
| EPWM8_G3      | 500C 8170h       |
| EPWM9_G0      | 5000 9170h       |
| EPWM9_G1      | 5004 9170h       |
| EPWM9_G2      | 5008 9170h       |

**Table 3-1033. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9170h       |
| EPWM10_G0     | 5000 A170h       |
| EPWM10_G1     | 5004 A170h       |
| EPWM10_G2     | 5008 A170h       |
| EPWM10_G3     | 500C A170h       |
| EPWM11_G0     | 5000 B170h       |
| EPWM11_G1     | 5004 B170h       |
| EPWM11_G2     | 5008 B170h       |
| EPWM11_G3     | 500C B170h       |
| EPWM12_G0     | 5000 C170h       |
| EPWM12_G1     | 5004 C170h       |
| EPWM12_G2     | 5008 C170h       |
| EPWM12_G3     | 500C C170h       |
| EPWM13_G0     | 5000 D170h       |
| EPWM13_G1     | 5004 D170h       |
| EPWM13_G2     | 5008 D170h       |
| EPWM13_G3     | 500C D170h       |
| EPWM14_G0     | 5000 E170h       |
| EPWM14_G1     | 5004 E170h       |
| EPWM14_G2     | 5008 E170h       |
| EPWM14_G3     | 500C E170h       |
| EPWM15_G0     | 5000 F170h       |
| EPWM15_G1     | 5004 F170h       |
| EPWM15_G2     | 5008 F170h       |
| EPWM15_G3     | 500C F170h       |
| EPWM16_G0     | 5001 0170h       |
| EPWM16_G1     | 5005 0170h       |
| EPWM16_G2     | 5009 0170h       |
| EPWM16_G3     | 500D 0170h       |
| EPWM17_G0     | 5001 1170h       |
| EPWM17_G1     | 5005 1170h       |
| EPWM17_G2     | 5009 1170h       |
| EPWM17_G3     | 500D 1170h       |
| EPWM18_G0     | 5001 2170h       |
| EPWM18_G1     | 5005 2170h       |
| EPWM18_G2     | 5009 2170h       |
| EPWM18_G3     | 500D 2170h       |
| EPWM19_G0     | 5001 3170h       |
| EPWM19_G1     | 5005 3170h       |
| EPWM19_G2     | 5009 3170h       |
| EPWM19_G3     | 500D 3170h       |
| EPWM20_G0     | 5001 4170h       |
| EPWM20_G1     | 5005 4170h       |
| EPWM20_G2     | 5009 4170h       |
| EPWM20_G3     | 500D 4170h       |



**Table 3-1033. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5170h       |
| EPWM21_G1     | 5005 5170h       |
| EPWM21_G2     | 5009 5170h       |
| EPWM21_G3     | 500D 5170h       |
| EPWM22_G0     | 5001 6170h       |
| EPWM22_G1     | 5005 6170h       |
| EPWM22_G2     | 5009 6170h       |
| EPWM22_G3     | 500D 6170h       |
| EPWM23_G0     | 5001 7170h       |
| EPWM23_G1     | 5005 7170h       |
| EPWM23_G2     | 5009 7170h       |
| EPWM23_G3     | 500D 7170h       |
| EPWM24_G0     | 5001 8170h       |
| EPWM24_G1     | 5005 8170h       |
| EPWM24_G2     | 5009 8170h       |
| EPWM24_G3     | 500D 8170h       |
| EPWM25_G0     | 5001 9170h       |
| EPWM25_G1     | 5005 9170h       |
| EPWM25_G2     | 5009 9170h       |
| EPWM25_G3     | 500D 9170h       |
| EPWM26_G0     | 5001 A170h       |
| EPWM26_G1     | 5005 A170h       |
| EPWM26_G2     | 5009 A170h       |
| EPWM26_G3     | 500D A170h       |
| EPWM27_G0     | 5001 B170h       |
| EPWM27_G1     | 5005 B170h       |
| EPWM27_G2     | 5009 B170h       |
| EPWM27_G3     | 500D B170h       |
| EPWM28_G0     | 5001 C170h       |
| EPWM28_G1     | 5005 C170h       |
| EPWM28_G2     | 5009 C170h       |
| EPWM28_G3     | 500D C170h       |
| EPWM29_G0     | 5001 D170h       |
| EPWM29_G1     | 5005 D170h       |
| EPWM29_G2     | 5009 D170h       |
| EPWM29_G3     | 500D D170h       |
| EPWM30_G0     | 5001 E170h       |
| EPWM30_G1     | 5005 E170h       |
| EPWM30_G2     | 5009 E170h       |
| EPWM30_G3     | 500D E170h       |
| EPWM31_G0     | 5001 F170h       |
| EPWM31_G1     | 5005 F170h       |
| EPWM31_G2     | 5009 F170h       |
| EPWM31_G3     | 500D F170h       |

**Figure 3-325. EPWM\_ETSOCAMIXEN Name Register**

| 15         | 14  | 13  | 12  | 11  | 10      | 9   | 8   |
|------------|-----|-----|-----|-----|---------|-----|-----|
| RESERVED_1 |     |     |     |     | DCAEVT1 | CDD | CDU |
| R          |     |     |     |     | R/W     | R/W | R/W |
| 0h         |     |     |     |     | 0h      | 0h  | 0h  |
| 7          | 6   | 5   | 4   | 3   | 2       | 1   | 0   |
| CCD        | CCU | CBD | CBU | CAD | CAU     | PRD | ZRO |
| R/W        | R/W | R/W | R/W | R/W | R/W     | R/W | R/W |
| 0h         | 0h  | 0h  | 0h  | 0h  | 0h      | 1h  | 1h  |

**Table 3-1035. EPWM\_ETSOCAMIXEN Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                        |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                           |
| 10    | DCAEVT1    | R/W  | 0h    | Enable DCAEVT1.inter to the mixed ET SOCA trigger signal [ETSOCAMIX].<br>0:DCAEVT1.soc event is not enabled<br>1:Enable DCAEVT1.soc event                                                                                          |
| 9     | CDD        | R/W  | 0h    | Enable event time-base counter equal to CMPD when the timer is decrementing to the mixed ET SOCA trigger signal [ETSOCAMIX].<br>0:CMPC down-count match enable event is not enabled<br>1:Enable CMPD down-count match enable event |
| 8     | CDU        | R/W  | 0h    | Enable event time-base counter equal to CMPD when the timer is incrementing to the mixed ET SOCA trigger signal [ETSOCAMIX].<br>0:CMPC up-count match enable event is not enabled<br>1:Enable CMPD up-count match enable event     |
| 7     | CCD        | R/W  | 0h    | Enable event time-base counter equal to CMPC when the timer is decrementing to the mixed ET SOCA trigger signal [ETSOCAMIX].<br>0:CMPC down-count match enable event is not enabled<br>1:Enable CMPC down-count match enable event |
| 6     | CCU        | R/W  | 0h    | Enable event time-base counter equal to CMPC when the timer is incrementing to the mixed ET SOCA trigger signal [ETSOCAMIX].<br>0:CMPC up-count match enable event is not enabled<br>1:Enable CMPC up-count match enable event     |
| 5     | CBD        | R/W  | 0h    | Enable event time-base counter equal to CMPB when the timer is decrementing to the mixed ET SOCA trigger signal [ETSOCAMIX].<br>0:CMPC down-count match enable event is not enabled<br>1:Enable CMPB down-count match enable event |
| 4     | CBU        | R/W  | 0h    | Enable event time-base counter equal to CMPB when the timer is incrementing to the mixed ET SOCA trigger signal [ETSOCAMIX].<br>0:CMPC up-count match enable event is not enabled<br>1:Enable CMPB up-count match enable event     |
| 3     | CAD        | R/W  | 0h    | Enable event time-base counter equal to CMPA when the timer is decrementing to the mixed ET SOCA trigger signal [ETSOCAMIX].<br>0:CMPC down-count match enable event is not enabled<br>1:Enable CMPA down-count match enable event |
| 2     | CAU        | R/W  | 0h    | Enable event time-base counter equal to CMPA when the timer is incrementing to the mixed ET SOCA trigger signal [ETSOCAMIX].<br>0:CMPC up-count match enable event is not enabled<br>1:Enable CMPA up-count match enable event     |
| 1     | PRD        | R/W  | 1h    | Enable event time-base counter equal to period [TBCTR = TBPRD] to the mixed ET SOCA trigger signal [ETSOCAMIX].<br>0:Period match event is not enabled<br>1:Enable period match event                                              |
| 0     | ZRO        | R/W  | 1h    | Enable event time-base counter equal to zero [TBCTR = 0x00] to the mixed ET SOCA trigger signal [ETSOCAMIX].<br>0:Zero match event is not enabled<br>1:Enable zero match event                                                     |

### 3.7.2.75 EPWM\_ETSOCBMIXEN Register

#### 1 EPWM\_ETSOCBMIXEN Register (Offset = 174h) [reset = 3h]

Event-Trigger Mixed SOCB Selection.

Return to [Summary Table](#)

**Table 3-1036. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0174h       |
| EPWM0_G1      | 5004 0174h       |
| EPWM0_G2      | 5008 0174h       |
| EPWM0_G3      | 500C 0174h       |
| EPWM1_G0      | 5000 1174h       |
| EPWM1_G1      | 5004 1174h       |
| EPWM1_G2      | 5008 1174h       |
| EPWM1_G3      | 500C 1174h       |
| EPWM2_G0      | 5000 2174h       |
| EPWM2_G1      | 5004 2174h       |
| EPWM2_G2      | 5008 2174h       |
| EPWM2_G3      | 500C 2174h       |
| EPWM3_G0      | 5000 3174h       |
| EPWM3_G1      | 5004 3174h       |
| EPWM3_G2      | 5008 3174h       |
| EPWM3_G3      | 500C 3174h       |
| EPWM4_G0      | 5000 4174h       |
| EPWM4_G1      | 5004 4174h       |
| EPWM4_G2      | 5008 4174h       |
| EPWM4_G3      | 500C 4174h       |
| EPWM5_G0      | 5000 5174h       |
| EPWM5_G1      | 5004 5174h       |
| EPWM5_G2      | 5008 5174h       |
| EPWM5_G3      | 500C 5174h       |
| EPWM6_G0      | 5000 6174h       |
| EPWM6_G1      | 5004 6174h       |
| EPWM6_G2      | 5008 6174h       |
| EPWM6_G3      | 500C 6174h       |
| EPWM7_G0      | 5000 7174h       |
| EPWM7_G1      | 5004 7174h       |
| EPWM7_G2      | 5008 7174h       |
| EPWM7_G3      | 500C 7174h       |
| EPWM8_G0      | 5000 8174h       |
| EPWM8_G1      | 5004 8174h       |
| EPWM8_G2      | 5008 8174h       |
| EPWM8_G3      | 500C 8174h       |
| EPWM9_G0      | 5000 9174h       |
| EPWM9_G1      | 5004 9174h       |
| EPWM9_G2      | 5008 9174h       |

**Table 3-1036. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9174h       |
| EPWM10_G0     | 5000 A174h       |
| EPWM10_G1     | 5004 A174h       |
| EPWM10_G2     | 5008 A174h       |
| EPWM10_G3     | 500C A174h       |
| EPWM11_G0     | 5000 B174h       |
| EPWM11_G1     | 5004 B174h       |
| EPWM11_G2     | 5008 B174h       |
| EPWM11_G3     | 500C B174h       |
| EPWM12_G0     | 5000 C174h       |
| EPWM12_G1     | 5004 C174h       |
| EPWM12_G2     | 5008 C174h       |
| EPWM12_G3     | 500C C174h       |
| EPWM13_G0     | 5000 D174h       |
| EPWM13_G1     | 5004 D174h       |
| EPWM13_G2     | 5008 D174h       |
| EPWM13_G3     | 500C D174h       |
| EPWM14_G0     | 5000 E174h       |
| EPWM14_G1     | 5004 E174h       |
| EPWM14_G2     | 5008 E174h       |
| EPWM14_G3     | 500C E174h       |
| EPWM15_G0     | 5000 F174h       |
| EPWM15_G1     | 5004 F174h       |
| EPWM15_G2     | 5008 F174h       |
| EPWM15_G3     | 500C F174h       |
| EPWM16_G0     | 5001 0174h       |
| EPWM16_G1     | 5005 0174h       |
| EPWM16_G2     | 5009 0174h       |
| EPWM16_G3     | 500D 0174h       |
| EPWM17_G0     | 5001 1174h       |
| EPWM17_G1     | 5005 1174h       |
| EPWM17_G2     | 5009 1174h       |
| EPWM17_G3     | 500D 1174h       |
| EPWM18_G0     | 5001 2174h       |
| EPWM18_G1     | 5005 2174h       |
| EPWM18_G2     | 5009 2174h       |
| EPWM18_G3     | 500D 2174h       |
| EPWM19_G0     | 5001 3174h       |
| EPWM19_G1     | 5005 3174h       |
| EPWM19_G2     | 5009 3174h       |
| EPWM19_G3     | 500D 3174h       |
| EPWM20_G0     | 5001 4174h       |
| EPWM20_G1     | 5005 4174h       |
| EPWM20_G2     | 5009 4174h       |
| EPWM20_G3     | 500D 4174h       |

**Table 3-1036. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5174h       |
| EPWM21_G1     | 5005 5174h       |
| EPWM21_G2     | 5009 5174h       |
| EPWM21_G3     | 500D 5174h       |
| EPWM22_G0     | 5001 6174h       |
| EPWM22_G1     | 5005 6174h       |
| EPWM22_G2     | 5009 6174h       |
| EPWM22_G3     | 500D 6174h       |
| EPWM23_G0     | 5001 7174h       |
| EPWM23_G1     | 5005 7174h       |
| EPWM23_G2     | 5009 7174h       |
| EPWM23_G3     | 500D 7174h       |
| EPWM24_G0     | 5001 8174h       |
| EPWM24_G1     | 5005 8174h       |
| EPWM24_G2     | 5009 8174h       |
| EPWM24_G3     | 500D 8174h       |
| EPWM25_G0     | 5001 9174h       |
| EPWM25_G1     | 5005 9174h       |
| EPWM25_G2     | 5009 9174h       |
| EPWM25_G3     | 500D 9174h       |
| EPWM26_G0     | 5001 A174h       |
| EPWM26_G1     | 5005 A174h       |
| EPWM26_G2     | 5009 A174h       |
| EPWM26_G3     | 500D A174h       |
| EPWM27_G0     | 5001 B174h       |
| EPWM27_G1     | 5005 B174h       |
| EPWM27_G2     | 5009 B174h       |
| EPWM27_G3     | 500D B174h       |
| EPWM28_G0     | 5001 C174h       |
| EPWM28_G1     | 5005 C174h       |
| EPWM28_G2     | 5009 C174h       |
| EPWM28_G3     | 500D C174h       |
| EPWM29_G0     | 5001 D174h       |
| EPWM29_G1     | 5005 D174h       |
| EPWM29_G2     | 5009 D174h       |
| EPWM29_G3     | 500D D174h       |
| EPWM30_G0     | 5001 E174h       |
| EPWM30_G1     | 5005 E174h       |
| EPWM30_G2     | 5009 E174h       |
| EPWM30_G3     | 500D E174h       |
| EPWM31_G0     | 5001 F174h       |
| EPWM31_G1     | 5005 F174h       |
| EPWM31_G2     | 5009 F174h       |
| EPWM31_G3     | 500D F174h       |

**Figure 3-326. EPWM\_ETSOCBMIXEN Name Register**

| 15         | 14  | 13  | 12  | 11  | 10      | 9   | 8   |
|------------|-----|-----|-----|-----|---------|-----|-----|
| RESERVED_1 |     |     |     |     | DCBEVT1 | CDD | CDU |
| R          |     |     |     |     | R/W     | R/W | R/W |
| 0h         |     |     |     |     | 0h      | 0h  | 0h  |
| 7          | 6   | 5   | 4   | 3   | 2       | 1   | 0   |
| CCD        | CCU | CBD | CBU | CAD | CAU     | PRD | ZRO |
| R/W        | R/W | R/W | R/W | R/W | R/W     | R/W | R/W |
| 0h         | 0h  | 0h  | 0h  | 0h  | 0h      | 1h  | 1h  |

**Table 3-1038. EPWM\_ETSOCBMIXEN Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                        |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                           |
| 10    | DCBEVT1    | R/W  | 0h    | Enable DCBEVT1.inter to the mixed ET SOCB trigger signal [ETSOCBMIX].<br>0:DCBEVT1.soc event is not enabled<br>1:Enable DCBEVT1.soc event                                                                                          |
| 9     | CDD        | R/W  | 0h    | Enable event time-base counter equal to CMPD when the timer is decrementing to the mixed ET SOCB trigger signal [ETSOCBMIX].<br>0:CMPC down-count match enable event is not enabled<br>1:Enable CMPD down-count match enable event |
| 8     | CDU        | R/W  | 0h    | Enable event time-base counter equal to CMPD when the timer is incrementing to the mixed ET SOCB trigger signal [ETSOCBMIX].<br>0:CMPC up-count match enable event is not enabled<br>1:Enable CMPD up-count match enable event     |
| 7     | CCD        | R/W  | 0h    | Enable event time-base counter equal to CMPC when the timer is decrementing to the mixed ET SOCB trigger signal [ETSOCBMIX].<br>0:CMPC down-count match enable event is not enabled<br>1:Enable CMPC down-count match enable event |
| 6     | CCU        | R/W  | 0h    | Enable event time-base counter equal to CMPC when the timer is incrementing to the mixed ET SOCB trigger signal [ETSOCBMIX].<br>0:CMPC up-count match enable event is not enabled<br>1:Enable CMPC up-count match enable event     |
| 5     | CBD        | R/W  | 0h    | Enable event time-base counter equal to CMPB when the timer is decrementing to the mixed ET SOCB trigger signal [ETSOCBMIX].<br>0:CMPC down-count match enable event is not enabled<br>1:Enable CMPB down-count match enable event |
| 4     | CBU        | R/W  | 0h    | Enable event time-base counter equal to CMPB when the timer is incrementing to the mixed ET SOCB trigger signal [ETSOCBMIX].<br>0:CMPC up-count match enable event is not enabled<br>1:Enable CMPB up-count match enable event     |
| 3     | CAD        | R/W  | 0h    | Enable event time-base counter equal to CMPA when the timer is decrementing to the mixed ET SOCB trigger signal [ETSOCBMIX].<br>0:CMPC down-count match enable event is not enabled<br>1:Enable CMPA down-count match enable event |
| 2     | CAU        | R/W  | 0h    | Enable event time-base counter equal to CMPA when the timer is incrementing to the mixed ET SOCB trigger signal [ETSOCBMIX].<br>0:CMPC up-count match enable event is not enabled<br>1:Enable CMPA up-count match enable event     |
| 1     | PRD        | R/W  | 1h    | Enable event time-base counter equal to period [TBCTR = TBPRD] to the mixed ET SOCB trigger signal [ETSOCBMIX].<br>0:Period match event is not enabled<br>1:Enable period match event                                              |
| 0     | ZRO        | R/W  | 1h    | Enable event time-base counter equal to zero [TBCTR = 0x00] to the mixed ET SOCB trigger signal [ETSOCBMIX].<br>0:Zero match event is not enabled<br>1:Enable zero match event                                                     |

### 3.7.2.76 EPWM\_DCTRISEL Register

#### 1 EPWM\_DCTRISEL Register (Offset = 180h) [reset = 0h]

Digital Compare Trip Select Register.

Return to [Summary Table](#)

**Table 3-1039. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0180h       |
| EPWM0_G1      | 5004 0180h       |
| EPWM0_G2      | 5008 0180h       |
| EPWM0_G3      | 500C 0180h       |
| EPWM1_G0      | 5000 1180h       |
| EPWM1_G1      | 5004 1180h       |
| EPWM1_G2      | 5008 1180h       |
| EPWM1_G3      | 500C 1180h       |
| EPWM2_G0      | 5000 2180h       |
| EPWM2_G1      | 5004 2180h       |
| EPWM2_G2      | 5008 2180h       |
| EPWM2_G3      | 500C 2180h       |
| EPWM3_G0      | 5000 3180h       |
| EPWM3_G1      | 5004 3180h       |
| EPWM3_G2      | 5008 3180h       |
| EPWM3_G3      | 500C 3180h       |
| EPWM4_G0      | 5000 4180h       |
| EPWM4_G1      | 5004 4180h       |
| EPWM4_G2      | 5008 4180h       |
| EPWM4_G3      | 500C 4180h       |
| EPWM5_G0      | 5000 5180h       |
| EPWM5_G1      | 5004 5180h       |
| EPWM5_G2      | 5008 5180h       |
| EPWM5_G3      | 500C 5180h       |
| EPWM6_G0      | 5000 6180h       |
| EPWM6_G1      | 5004 6180h       |
| EPWM6_G2      | 5008 6180h       |
| EPWM6_G3      | 500C 6180h       |
| EPWM7_G0      | 5000 7180h       |
| EPWM7_G1      | 5004 7180h       |
| EPWM7_G2      | 5008 7180h       |
| EPWM7_G3      | 500C 7180h       |
| EPWM8_G0      | 5000 8180h       |
| EPWM8_G1      | 5004 8180h       |
| EPWM8_G2      | 5008 8180h       |
| EPWM8_G3      | 500C 8180h       |
| EPWM9_G0      | 5000 9180h       |
| EPWM9_G1      | 5004 9180h       |
| EPWM9_G2      | 5008 9180h       |

**Table 3-1039. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9180h       |
| EPWM10_G0     | 5000 A180h       |
| EPWM10_G1     | 5004 A180h       |
| EPWM10_G2     | 5008 A180h       |
| EPWM10_G3     | 500C A180h       |
| EPWM11_G0     | 5000 B180h       |
| EPWM11_G1     | 5004 B180h       |
| EPWM11_G2     | 5008 B180h       |
| EPWM11_G3     | 500C B180h       |
| EPWM12_G0     | 5000 C180h       |
| EPWM12_G1     | 5004 C180h       |
| EPWM12_G2     | 5008 C180h       |
| EPWM12_G3     | 500C C180h       |
| EPWM13_G0     | 5000 D180h       |
| EPWM13_G1     | 5004 D180h       |
| EPWM13_G2     | 5008 D180h       |
| EPWM13_G3     | 500C D180h       |
| EPWM14_G0     | 5000 E180h       |
| EPWM14_G1     | 5004 E180h       |
| EPWM14_G2     | 5008 E180h       |
| EPWM14_G3     | 500C E180h       |
| EPWM15_G0     | 5000 F180h       |
| EPWM15_G1     | 5004 F180h       |
| EPWM15_G2     | 5008 F180h       |
| EPWM15_G3     | 500C F180h       |
| EPWM16_G0     | 5001 0180h       |
| EPWM16_G1     | 5005 0180h       |
| EPWM16_G2     | 5009 0180h       |
| EPWM16_G3     | 500D 0180h       |
| EPWM17_G0     | 5001 1180h       |
| EPWM17_G1     | 5005 1180h       |
| EPWM17_G2     | 5009 1180h       |
| EPWM17_G3     | 500D 1180h       |
| EPWM18_G0     | 5001 2180h       |
| EPWM18_G1     | 5005 2180h       |
| EPWM18_G2     | 5009 2180h       |
| EPWM18_G3     | 500D 2180h       |
| EPWM19_G0     | 5001 3180h       |
| EPWM19_G1     | 5005 3180h       |
| EPWM19_G2     | 5009 3180h       |
| EPWM19_G3     | 500D 3180h       |
| EPWM20_G0     | 5001 4180h       |
| EPWM20_G1     | 5005 4180h       |
| EPWM20_G2     | 5009 4180h       |
| EPWM20_G3     | 500D 4180h       |



**Table 3-1039. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5180h       |
| EPWM21_G1     | 5005 5180h       |
| EPWM21_G2     | 5009 5180h       |
| EPWM21_G3     | 500D 5180h       |
| EPWM22_G0     | 5001 6180h       |
| EPWM22_G1     | 5005 6180h       |
| EPWM22_G2     | 5009 6180h       |
| EPWM22_G3     | 500D 6180h       |
| EPWM23_G0     | 5001 7180h       |
| EPWM23_G1     | 5005 7180h       |
| EPWM23_G2     | 5009 7180h       |
| EPWM23_G3     | 500D 7180h       |
| EPWM24_G0     | 5001 8180h       |
| EPWM24_G1     | 5005 8180h       |
| EPWM24_G2     | 5009 8180h       |
| EPWM24_G3     | 500D 8180h       |
| EPWM25_G0     | 5001 9180h       |
| EPWM25_G1     | 5005 9180h       |
| EPWM25_G2     | 5009 9180h       |
| EPWM25_G3     | 500D 9180h       |
| EPWM26_G0     | 5001 A180h       |
| EPWM26_G1     | 5005 A180h       |
| EPWM26_G2     | 5009 A180h       |
| EPWM26_G3     | 500D A180h       |
| EPWM27_G0     | 5001 B180h       |
| EPWM27_G1     | 5005 B180h       |
| EPWM27_G2     | 5009 B180h       |
| EPWM27_G3     | 500D B180h       |
| EPWM28_G0     | 5001 C180h       |
| EPWM28_G1     | 5005 C180h       |
| EPWM28_G2     | 5009 C180h       |
| EPWM28_G3     | 500D C180h       |
| EPWM29_G0     | 5001 D180h       |
| EPWM29_G1     | 5005 D180h       |
| EPWM29_G2     | 5009 D180h       |
| EPWM29_G3     | 500D D180h       |
| EPWM30_G0     | 5001 E180h       |
| EPWM30_G1     | 5005 E180h       |
| EPWM30_G2     | 5009 E180h       |
| EPWM30_G3     | 500D E180h       |
| EPWM31_G0     | 5001 F180h       |
| EPWM31_G1     | 5005 F180h       |
| EPWM31_G2     | 5009 F180h       |
| EPWM31_G3     | 500D F180h       |

**Figure 3-327. EPWM\_DCTRIPSEL Name Register**

|             |    |    |    |             |    |   |   |
|-------------|----|----|----|-------------|----|---|---|
| 15          | 14 | 13 | 12 | 11          | 10 | 9 | 8 |
| DCBLCOMPSEL |    |    |    | DCBHCOMPSEL |    |   |   |
| R/W         |    |    |    | R/W         |    |   |   |
| 0h          |    |    |    | 0h          |    |   |   |
| 7           | 6  | 5  | 4  | 3           | 2  | 1 | 0 |
| DCALCOMPSEL |    |    |    | DCAHCOMPSEL |    |   |   |
| R/W         |    |    |    | R/W         |    |   |   |
| 0h          |    |    |    | 0h          |    |   |   |

**Table 3-1041. EPWM\_DCTRIPSEL Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                         |
|-------|-------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | DCBLCOMPSEL | R/W  | 0h    | Digital Compare B Low Input Select Bits<br>0000 TRIPIN1<br>0001 TRIPIN2<br>0010 TRIPIN3<br>0011 TRIPIN4<br>...<br>1011 TRIPIN12<br>1100 Reserved<br>1101 TRIPIN14<br>1110 TRIPIN15<br>1111 Trip combination input [all trip inputs selected by DCBLTRIPSEL register ORed together]  |
| 11:8  | DCBHCOMPSEL | R/W  | 0h    | Digital Compare B High Input Select Bits<br>0000 TRIPIN1<br>0001 TRIPIN2<br>0010 TRIPIN3<br>0011 TRIPIN4<br>...<br>1011 TRIPIN12<br>1100 Reserved<br>1101 TRIPIN14<br>1110 TRIPIN15<br>1111 Trip combination input [all trip inputs selected by DCBHTRIPSEL register ORed together] |
| 7:4   | DCALCOMPSEL | R/W  | 0h    | Digital Compare A Low Input Select Bits<br>0000 TRIPIN1<br>0001 TRIPIN2<br>0010 TRIPIN3<br>0011 TRIPIN4<br>...<br>1011 TRIPIN12<br>1100 Reserved<br>1101 TRIPIN14<br>1110 TRIPIN15<br>1111 Trip combination input [all trip inputs selected by DCALTRIPSEL register ORed together]  |
| 3:0   | DCAHCOMPSEL | R/W  | 0h    | Digital Compare A High Input Select Bits<br>0000 TRIPIN1<br>0001 TRIPIN2<br>0010 TRIPIN3<br>0011 TRIPIN4<br>...<br>1011 TRIPIN12<br>1100 Reserved<br>1101 TRIPIN14<br>1110 TRIPIN15<br>1111 Trip combination input [all trip inputs selected by DCAHTRIPSEL register ORed together] |

### 3.7.2.77 EPWM\_DCACTL Register

#### 1 EPWM\_DCACTL Register (Offset = 186h) [reset = 0h]

Digital Compare A Control Register.

Return to [Summary Table](#)

**Table 3-1042. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0186h       |
| EPWM0_G1      | 5004 0186h       |
| EPWM0_G2      | 5008 0186h       |
| EPWM0_G3      | 500C 0186h       |
| EPWM1_G0      | 5000 1186h       |
| EPWM1_G1      | 5004 1186h       |
| EPWM1_G2      | 5008 1186h       |
| EPWM1_G3      | 500C 1186h       |
| EPWM2_G0      | 5000 2186h       |
| EPWM2_G1      | 5004 2186h       |
| EPWM2_G2      | 5008 2186h       |
| EPWM2_G3      | 500C 2186h       |
| EPWM3_G0      | 5000 3186h       |
| EPWM3_G1      | 5004 3186h       |
| EPWM3_G2      | 5008 3186h       |
| EPWM3_G3      | 500C 3186h       |
| EPWM4_G0      | 5000 4186h       |
| EPWM4_G1      | 5004 4186h       |
| EPWM4_G2      | 5008 4186h       |
| EPWM4_G3      | 500C 4186h       |
| EPWM5_G0      | 5000 5186h       |
| EPWM5_G1      | 5004 5186h       |
| EPWM5_G2      | 5008 5186h       |
| EPWM5_G3      | 500C 5186h       |
| EPWM6_G0      | 5000 6186h       |
| EPWM6_G1      | 5004 6186h       |
| EPWM6_G2      | 5008 6186h       |
| EPWM6_G3      | 500C 6186h       |
| EPWM7_G0      | 5000 7186h       |
| EPWM7_G1      | 5004 7186h       |
| EPWM7_G2      | 5008 7186h       |
| EPWM7_G3      | 500C 7186h       |
| EPWM8_G0      | 5000 8186h       |
| EPWM8_G1      | 5004 8186h       |
| EPWM8_G2      | 5008 8186h       |
| EPWM8_G3      | 500C 8186h       |
| EPWM9_G0      | 5000 9186h       |
| EPWM9_G1      | 5004 9186h       |
| EPWM9_G2      | 5008 9186h       |

**Table 3-1042. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9186h       |
| EPWM10_G0     | 5000 A186h       |
| EPWM10_G1     | 5004 A186h       |
| EPWM10_G2     | 5008 A186h       |
| EPWM10_G3     | 500C A186h       |
| EPWM11_G0     | 5000 B186h       |
| EPWM11_G1     | 5004 B186h       |
| EPWM11_G2     | 5008 B186h       |
| EPWM11_G3     | 500C B186h       |
| EPWM12_G0     | 5000 C186h       |
| EPWM12_G1     | 5004 C186h       |
| EPWM12_G2     | 5008 C186h       |
| EPWM12_G3     | 500C C186h       |
| EPWM13_G0     | 5000 D186h       |
| EPWM13_G1     | 5004 D186h       |
| EPWM13_G2     | 5008 D186h       |
| EPWM13_G3     | 500C D186h       |
| EPWM14_G0     | 5000 E186h       |
| EPWM14_G1     | 5004 E186h       |
| EPWM14_G2     | 5008 E186h       |
| EPWM14_G3     | 500C E186h       |
| EPWM15_G0     | 5000 F186h       |
| EPWM15_G1     | 5004 F186h       |
| EPWM15_G2     | 5008 F186h       |
| EPWM15_G3     | 500C F186h       |
| EPWM16_G0     | 5001 0186h       |
| EPWM16_G1     | 5005 0186h       |
| EPWM16_G2     | 5009 0186h       |
| EPWM16_G3     | 500D 0186h       |
| EPWM17_G0     | 5001 1186h       |
| EPWM17_G1     | 5005 1186h       |
| EPWM17_G2     | 5009 1186h       |
| EPWM17_G3     | 500D 1186h       |
| EPWM18_G0     | 5001 2186h       |
| EPWM18_G1     | 5005 2186h       |
| EPWM18_G2     | 5009 2186h       |
| EPWM18_G3     | 500D 2186h       |
| EPWM19_G0     | 5001 3186h       |
| EPWM19_G1     | 5005 3186h       |
| EPWM19_G2     | 5009 3186h       |
| EPWM19_G3     | 500D 3186h       |
| EPWM20_G0     | 5001 4186h       |
| EPWM20_G1     | 5005 4186h       |
| EPWM20_G2     | 5009 4186h       |
| EPWM20_G3     | 500D 4186h       |

**Table 3-1042. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5186h       |
| EPWM21_G1     | 5005 5186h       |
| EPWM21_G2     | 5009 5186h       |
| EPWM21_G3     | 500D 5186h       |
| EPWM22_G0     | 5001 6186h       |
| EPWM22_G1     | 5005 6186h       |
| EPWM22_G2     | 5009 6186h       |
| EPWM22_G3     | 500D 6186h       |
| EPWM23_G0     | 5001 7186h       |
| EPWM23_G1     | 5005 7186h       |
| EPWM23_G2     | 5009 7186h       |
| EPWM23_G3     | 500D 7186h       |
| EPWM24_G0     | 5001 8186h       |
| EPWM24_G1     | 5005 8186h       |
| EPWM24_G2     | 5009 8186h       |
| EPWM24_G3     | 500D 8186h       |
| EPWM25_G0     | 5001 9186h       |
| EPWM25_G1     | 5005 9186h       |
| EPWM25_G2     | 5009 9186h       |
| EPWM25_G3     | 500D 9186h       |
| EPWM26_G0     | 5001 A186h       |
| EPWM26_G1     | 5005 A186h       |
| EPWM26_G2     | 5009 A186h       |
| EPWM26_G3     | 500D A186h       |
| EPWM27_G0     | 5001 B186h       |
| EPWM27_G1     | 5005 B186h       |
| EPWM27_G2     | 5009 B186h       |
| EPWM27_G3     | 500D B186h       |
| EPWM28_G0     | 5001 C186h       |
| EPWM28_G1     | 5005 C186h       |
| EPWM28_G2     | 5009 C186h       |
| EPWM28_G3     | 500D C186h       |
| EPWM29_G0     | 5001 D186h       |
| EPWM29_G1     | 5005 D186h       |
| EPWM29_G2     | 5009 D186h       |
| EPWM29_G3     | 500D D186h       |
| EPWM30_G0     | 5001 E186h       |
| EPWM30_G1     | 5005 E186h       |
| EPWM30_G2     | 5009 E186h       |
| EPWM30_G3     | 500D E186h       |
| EPWM31_G0     | 5001 F186h       |
| EPWM31_G1     | 5005 F186h       |
| EPWM31_G2     | 5009 F186h       |
| EPWM31_G3     | 500D F186h       |

**Figure 3-328. EPWM\_DCACTL Name Register**

| 15      | 14            | 13         | 12         | 11                 | 10                 | 9          | 8 |
|---------|---------------|------------|------------|--------------------|--------------------|------------|---|
| EVT2LAT | EVT2LATCLRSEL | EVT2LATSEL | RESERVED_1 | EVT2FRCSYN<br>CSEL | EVT2SRCSEL         |            |   |
| R       | R/W           | R/W        | R          | R/W                | R/W                |            |   |
| 0h      | 0h            | 0h         | 0h         | 0h                 | 0h                 |            |   |
| 7       | 6             | 5          | 4          | 3                  | 2                  | 1          | 0 |
| EVT1LAT | EVT1LATCLRSEL | EVT1LATSEL | EVT1SYNCE  | EVT1SOCE           | EVT1FRCSYN<br>CSEL | EVT1SRCSEL |   |
| R       | R/W           | R/W        | R/W        | R/W                | R/W                | R/W        |   |
| 0h      | 0h            | 0h         | 0h         | 0h                 | 0h                 | 0h         |   |

**Table 3-1044. EPWM\_DCACTL Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                         |
|-------|-----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | EVT2LAT         | R    | 0h    | Indicates the status of DCAEVT2LAT signal.<br>0 The DCAEVT2LAT latch is cleared.<br>1 The DCAEVT2LAT latch is set.                                                                                  |
| 14:13 | EVT2LATCLRSEL   | R/W  | 0h    | DCAEVT2 Latched clear source select:<br>00 CNT_ZERO event clears DCAEVT2 latch.<br>01 PRD_EQ event clears DCAEVT2 latch.<br>10 CNT_ZERO event or PRD_EQ event clears DCAEVT2 latch.<br>11 Reserved. |
| 12    | EVT2LATSEL      | R/W  | 0h    | DCAEVT2 Latched signal select:<br>0 Does not select the DCAEVT2 latched signal as source of DCAEVT2.force.<br>1 Selects the DCAEVT2 latched signal as source of DCAEVT2.force.                      |
| 11:10 | RESERVED_1      | R    | 0h    | Reserved                                                                                                                                                                                            |
| 9     | EVT2FRCSYNCSSEL | R/W  | 0h    | DCAEVT2 Force Synchronization Signal Select<br>0:Source is synchronized with EPWMCLK<br>1:Source is passed through asynchronously                                                                   |
| 8     | EVT2SRCSEL      | R/W  | 0h    | DCAEVT2 Source Signal Select<br>0:Source Is DCAEVT2 Signal<br>1:Source Is DCEVTFILT Signal                                                                                                          |
| 7     | EVT1LAT         | R    | 0h    | Indicates the status of DCAEVT1LAT signal.<br>0 The DCAEVT1LAT latch is cleared.<br>1 The DCAEVT1LAT latch is set.                                                                                  |
| 6:5   | EVT1LATCLRSEL   | R/W  | 0h    | DCAEVT1 Latched clear source select:<br>00 CNT_ZERO event clears DCAEVT1 latch.<br>01 PRD_EQ event clears DCAEVT1 latch.<br>10 CNT_ZERO event or PRD_EQ event clears DCAEVT1 latch.<br>11 Reserved. |
| 4     | EVT1LATSEL      | R/W  | 0h    | DCAEVT1 Latched signal select:<br>0 Does not select the DCAEVT1 latched signal as source of DCAEVT1.force.<br>1 Selects the DCAEVT1 latched signal as source of DCAEVT1.force.                      |
| 3     | EVT1SYNCE       | R/W  | 0h    | DCAEVT1 SYNC, Enable/Disable<br>0:SYNC Generation Disabled<br>1:SYNC Generation Enabled                                                                                                             |
| 2     | EVT1SOCE        | R/W  | 0h    | DCAEVT1 SOC, Enable/Disable<br>0:SOC Generation Disabled<br>1:SOC Generation Enabled                                                                                                                |
| 1     | EVT1FRCSYNCSSEL | R/W  | 0h    | DCAEVT1 Force Synchronization Signal Select<br>0:Source is synchronized with EPWMCLK<br>1:Source is passed through asynchronously                                                                   |
| 0     | EVT1SRCSEL      | R/W  | 0h    | DCAEVT1 Source Signal Select<br>0:Source Is DCAEVT1 Signal<br>1:Source Is DCEVTFILT Signal                                                                                                          |

### 3.7.2.78 EPWM\_DCBCTL Register

#### 1 EPWM\_DCBCTL Register (Offset = 188h) [reset = 0h]

Digital Compare B Control Register.

Return to [Summary Table](#)

**Table 3-1045. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0188h       |
| EPWM0_G1      | 5004 0188h       |
| EPWM0_G2      | 5008 0188h       |
| EPWM0_G3      | 500C 0188h       |
| EPWM1_G0      | 5000 1188h       |
| EPWM1_G1      | 5004 1188h       |
| EPWM1_G2      | 5008 1188h       |
| EPWM1_G3      | 500C 1188h       |
| EPWM2_G0      | 5000 2188h       |
| EPWM2_G1      | 5004 2188h       |
| EPWM2_G2      | 5008 2188h       |
| EPWM2_G3      | 500C 2188h       |
| EPWM3_G0      | 5000 3188h       |
| EPWM3_G1      | 5004 3188h       |
| EPWM3_G2      | 5008 3188h       |
| EPWM3_G3      | 500C 3188h       |
| EPWM4_G0      | 5000 4188h       |
| EPWM4_G1      | 5004 4188h       |
| EPWM4_G2      | 5008 4188h       |
| EPWM4_G3      | 500C 4188h       |
| EPWM5_G0      | 5000 5188h       |
| EPWM5_G1      | 5004 5188h       |
| EPWM5_G2      | 5008 5188h       |
| EPWM5_G3      | 500C 5188h       |
| EPWM6_G0      | 5000 6188h       |
| EPWM6_G1      | 5004 6188h       |
| EPWM6_G2      | 5008 6188h       |
| EPWM6_G3      | 500C 6188h       |
| EPWM7_G0      | 5000 7188h       |
| EPWM7_G1      | 5004 7188h       |
| EPWM7_G2      | 5008 7188h       |
| EPWM7_G3      | 500C 7188h       |
| EPWM8_G0      | 5000 8188h       |
| EPWM8_G1      | 5004 8188h       |
| EPWM8_G2      | 5008 8188h       |
| EPWM8_G3      | 500C 8188h       |
| EPWM9_G0      | 5000 9188h       |
| EPWM9_G1      | 5004 9188h       |
| EPWM9_G2      | 5008 9188h       |

**Table 3-1045. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9188h       |
| EPWM10_G0     | 5000 A188h       |
| EPWM10_G1     | 5004 A188h       |
| EPWM10_G2     | 5008 A188h       |
| EPWM10_G3     | 500C A188h       |
| EPWM11_G0     | 5000 B188h       |
| EPWM11_G1     | 5004 B188h       |
| EPWM11_G2     | 5008 B188h       |
| EPWM11_G3     | 500C B188h       |
| EPWM12_G0     | 5000 C188h       |
| EPWM12_G1     | 5004 C188h       |
| EPWM12_G2     | 5008 C188h       |
| EPWM12_G3     | 500C C188h       |
| EPWM13_G0     | 5000 D188h       |
| EPWM13_G1     | 5004 D188h       |
| EPWM13_G2     | 5008 D188h       |
| EPWM13_G3     | 500C D188h       |
| EPWM14_G0     | 5000 E188h       |
| EPWM14_G1     | 5004 E188h       |
| EPWM14_G2     | 5008 E188h       |
| EPWM14_G3     | 500C E188h       |
| EPWM15_G0     | 5000 F188h       |
| EPWM15_G1     | 5004 F188h       |
| EPWM15_G2     | 5008 F188h       |
| EPWM15_G3     | 500C F188h       |
| EPWM16_G0     | 5001 0188h       |
| EPWM16_G1     | 5005 0188h       |
| EPWM16_G2     | 5009 0188h       |
| EPWM16_G3     | 500D 0188h       |
| EPWM17_G0     | 5001 1188h       |
| EPWM17_G1     | 5005 1188h       |
| EPWM17_G2     | 5009 1188h       |
| EPWM17_G3     | 500D 1188h       |
| EPWM18_G0     | 5001 2188h       |
| EPWM18_G1     | 5005 2188h       |
| EPWM18_G2     | 5009 2188h       |
| EPWM18_G3     | 500D 2188h       |
| EPWM19_G0     | 5001 3188h       |
| EPWM19_G1     | 5005 3188h       |
| EPWM19_G2     | 5009 3188h       |
| EPWM19_G3     | 500D 3188h       |
| EPWM20_G0     | 5001 4188h       |
| EPWM20_G1     | 5005 4188h       |
| EPWM20_G2     | 5009 4188h       |
| EPWM20_G3     | 500D 4188h       |



**Table 3-1045. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5188h       |
| EPWM21_G1     | 5005 5188h       |
| EPWM21_G2     | 5009 5188h       |
| EPWM21_G3     | 500D 5188h       |
| EPWM22_G0     | 5001 6188h       |
| EPWM22_G1     | 5005 6188h       |
| EPWM22_G2     | 5009 6188h       |
| EPWM22_G3     | 500D 6188h       |
| EPWM23_G0     | 5001 7188h       |
| EPWM23_G1     | 5005 7188h       |
| EPWM23_G2     | 5009 7188h       |
| EPWM23_G3     | 500D 7188h       |
| EPWM24_G0     | 5001 8188h       |
| EPWM24_G1     | 5005 8188h       |
| EPWM24_G2     | 5009 8188h       |
| EPWM24_G3     | 500D 8188h       |
| EPWM25_G0     | 5001 9188h       |
| EPWM25_G1     | 5005 9188h       |
| EPWM25_G2     | 5009 9188h       |
| EPWM25_G3     | 500D 9188h       |
| EPWM26_G0     | 5001 A188h       |
| EPWM26_G1     | 5005 A188h       |
| EPWM26_G2     | 5009 A188h       |
| EPWM26_G3     | 500D A188h       |
| EPWM27_G0     | 5001 B188h       |
| EPWM27_G1     | 5005 B188h       |
| EPWM27_G2     | 5009 B188h       |
| EPWM27_G3     | 500D B188h       |
| EPWM28_G0     | 5001 C188h       |
| EPWM28_G1     | 5005 C188h       |
| EPWM28_G2     | 5009 C188h       |
| EPWM28_G3     | 500D C188h       |
| EPWM29_G0     | 5001 D188h       |
| EPWM29_G1     | 5005 D188h       |
| EPWM29_G2     | 5009 D188h       |
| EPWM29_G3     | 500D D188h       |
| EPWM30_G0     | 5001 E188h       |
| EPWM30_G1     | 5005 E188h       |
| EPWM30_G2     | 5009 E188h       |
| EPWM30_G3     | 500D E188h       |
| EPWM31_G0     | 5001 F188h       |
| EPWM31_G1     | 5005 F188h       |
| EPWM31_G2     | 5009 F188h       |
| EPWM31_G3     | 500D F188h       |

**Figure 3-329. EPWM\_DCBCTL Name Register**

| 15      | 14            | 13         | 12         | 11              | 10              | 9          | 8 |
|---------|---------------|------------|------------|-----------------|-----------------|------------|---|
| EVT2LAT | EVT2LATCLRSEL | EVT2LATSEL | RESERVED_1 | EVT2FRCSYN CSEL | EVT2SRCSEL      |            |   |
| R       | R/W           | R/W        | R          | R/W             | R/W             |            |   |
| 0h      | 0h            | 0h         | 0h         | 0h              | 0h              |            |   |
| 7       | 6             | 5          | 4          | 3               | 2               | 1          | 0 |
| EVT1LAT | EVT1LATCLRSEL | EVT1LATSEL | EVT1SYNCE  | EVT1SOCE        | EVT1FRCSYN CSEL | EVT1SRCSEL |   |
| R       | R/W           | R/W        | R/W        | R/W             | R/W             | R/W        |   |
| 0h      | 0h            | 0h         | 0h         | 0h              | 0h              | 0h         |   |

**Table 3-1047. EPWM\_DCBCTL Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                         |
|-------|-----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | EVT2LAT         | R    | 0h    | Indicates the status of DCBEVT2LAT signal.<br>0 The DCBEVT2LAT latch is cleared.<br>1 The DCBEVT2LAT latch is set.                                                                                  |
| 14:13 | EVT2LATCLRSEL   | R/W  | 0h    | DCBEVT2 Latched clear source select:<br>00 CNT_ZERO event clears DCBEVT2 latch.<br>01 PRD_EQ event clears DCBEVT2 latch.<br>10 CNT_ZERO event or PRD_EQ event clears DCBEVT2 latch.<br>11 Reserved. |
| 12    | EVT2LATSEL      | R/W  | 0h    | DCBEVT2 Latched signal select:<br>0 Does not select the DCBEVT2 latched signal as source of DCBEVT2.force.<br>1 Selects the DCBEVT2 latched signal as source of DCBEVT2.force.                      |
| 11:10 | RESERVED_1      | R    | 0h    | Reserved                                                                                                                                                                                            |
| 9     | EVT2FRCSYNCSSEL | R/W  | 0h    | DCBEVT2 Force Synchronization Signal Select<br>0:Source is synchronized with EPWMCLK<br>1:Source is passed through asynchronously                                                                   |
| 8     | EVT2SRCSEL      | R/W  | 0h    | DCBEVT2 Source Signal Select<br>0:Source Is DCBEVT2 Signal<br>1:Source Is DCEVTFILT Signal                                                                                                          |
| 7     | EVT1LAT         | R    | 0h    | Indicates the status of DCBEVT1LAT signal.<br>0 The DCBEVT1LAT latch is cleared.<br>1 The DCBEVT1LAT latch is set.                                                                                  |
| 6:5   | EVT1LATCLRSEL   | R/W  | 0h    | DCBEVT1 Latched clear source select:<br>00 CNT_ZERO event clears DCBEVT1 latch.<br>01 PRD_EQ event clears DCBEVT1 latch.<br>10 CNT_ZERO event or PRD_EQ event clears DCBEVT1 latch.<br>11 Reserved. |
| 4     | EVT1LATSEL      | R/W  | 0h    | DCBEVT1 Latched signal select:<br>0 Does not select the DCBEVT1 latched signal as source of DCBEVT1.force.<br>1 Selects the DCBEVT1 latched signal as source of DCBEVT1.force.                      |
| 3     | EVT1SYNCE       | R/W  | 0h    | DCBEVT1 SYNC, Enable/Disable<br>0:SYNC Generation Disabled<br>1:SYNC Generation Enabled                                                                                                             |
| 2     | EVT1SOCE        | R/W  | 0h    | DCBEVT1 SOC, Enable/Disable<br>0:SOC Generation Disabled<br>1:SOC Generation Enabled                                                                                                                |
| 1     | EVT1FRCSYNCSSEL | R/W  | 0h    | DCBEVT1 Force Synchronization Signal Select<br>0:Source is synchronized with EPWMCLK<br>1:Source is passed through asynchronously                                                                   |
| 0     | EVT1SRCSEL      | R/W  | 0h    | DCBEVT1 Source Signal Select<br>0:Source Is DCBEVT1 Signal<br>1:Source Is DCEVTFILT Signal                                                                                                          |

### 3.7.2.79 EPWM\_DCFCTL Register

#### 1 EPWM\_DCFCTL Register (Offset = 18Eh) [reset = 0h]

Digital Compare Filter Control Register.

Return to [Summary Table](#)

**Table 3-1048. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 018Eh       |
| EPWM0_G1      | 5004 018Eh       |
| EPWM0_G2      | 5008 018Eh       |
| EPWM0_G3      | 500C 018Eh       |
| EPWM1_G0      | 5000 118Eh       |
| EPWM1_G1      | 5004 118Eh       |
| EPWM1_G2      | 5008 118Eh       |
| EPWM1_G3      | 500C 118Eh       |
| EPWM2_G0      | 5000 218Eh       |
| EPWM2_G1      | 5004 218Eh       |
| EPWM2_G2      | 5008 218Eh       |
| EPWM2_G3      | 500C 218Eh       |
| EPWM3_G0      | 5000 318Eh       |
| EPWM3_G1      | 5004 318Eh       |
| EPWM3_G2      | 5008 318Eh       |
| EPWM3_G3      | 500C 318Eh       |
| EPWM4_G0      | 5000 418Eh       |
| EPWM4_G1      | 5004 418Eh       |
| EPWM4_G2      | 5008 418Eh       |
| EPWM4_G3      | 500C 418Eh       |
| EPWM5_G0      | 5000 518Eh       |
| EPWM5_G1      | 5004 518Eh       |
| EPWM5_G2      | 5008 518Eh       |
| EPWM5_G3      | 500C 518Eh       |
| EPWM6_G0      | 5000 618Eh       |
| EPWM6_G1      | 5004 618Eh       |
| EPWM6_G2      | 5008 618Eh       |
| EPWM6_G3      | 500C 618Eh       |
| EPWM7_G0      | 5000 718Eh       |
| EPWM7_G1      | 5004 718Eh       |
| EPWM7_G2      | 5008 718Eh       |
| EPWM7_G3      | 500C 718Eh       |
| EPWM8_G0      | 5000 818Eh       |
| EPWM8_G1      | 5004 818Eh       |
| EPWM8_G2      | 5008 818Eh       |
| EPWM8_G3      | 500C 818Eh       |
| EPWM9_G0      | 5000 918Eh       |
| EPWM9_G1      | 5004 918Eh       |
| EPWM9_G2      | 5008 918Eh       |

**Table 3-1048. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 918Eh       |
| EPWM10_G0     | 5000 A18Eh       |
| EPWM10_G1     | 5004 A18Eh       |
| EPWM10_G2     | 5008 A18Eh       |
| EPWM10_G3     | 500C A18Eh       |
| EPWM11_G0     | 5000 B18Eh       |
| EPWM11_G1     | 5004 B18Eh       |
| EPWM11_G2     | 5008 B18Eh       |
| EPWM11_G3     | 500C B18Eh       |
| EPWM12_G0     | 5000 C18Eh       |
| EPWM12_G1     | 5004 C18Eh       |
| EPWM12_G2     | 5008 C18Eh       |
| EPWM12_G3     | 500C C18Eh       |
| EPWM13_G0     | 5000 D18Eh       |
| EPWM13_G1     | 5004 D18Eh       |
| EPWM13_G2     | 5008 D18Eh       |
| EPWM13_G3     | 500C D18Eh       |
| EPWM14_G0     | 5000 E18Eh       |
| EPWM14_G1     | 5004 E18Eh       |
| EPWM14_G2     | 5008 E18Eh       |
| EPWM14_G3     | 500C E18Eh       |
| EPWM15_G0     | 5000 F18Eh       |
| EPWM15_G1     | 5004 F18Eh       |
| EPWM15_G2     | 5008 F18Eh       |
| EPWM15_G3     | 500C F18Eh       |
| EPWM16_G0     | 5001 018Eh       |
| EPWM16_G1     | 5005 018Eh       |
| EPWM16_G2     | 5009 018Eh       |
| EPWM16_G3     | 500D 018Eh       |
| EPWM17_G0     | 5001 118Eh       |
| EPWM17_G1     | 5005 118Eh       |
| EPWM17_G2     | 5009 118Eh       |
| EPWM17_G3     | 500D 118Eh       |
| EPWM18_G0     | 5001 218Eh       |
| EPWM18_G1     | 5005 218Eh       |
| EPWM18_G2     | 5009 218Eh       |
| EPWM18_G3     | 500D 218Eh       |
| EPWM19_G0     | 5001 318Eh       |
| EPWM19_G1     | 5005 318Eh       |
| EPWM19_G2     | 5009 318Eh       |
| EPWM19_G3     | 500D 318Eh       |
| EPWM20_G0     | 5001 418Eh       |
| EPWM20_G1     | 5005 418Eh       |
| EPWM20_G2     | 5009 418Eh       |
| EPWM20_G3     | 500D 418Eh       |

**Table 3-1048. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 518Eh       |
| EPWM21_G1     | 5005 518Eh       |
| EPWM21_G2     | 5009 518Eh       |
| EPWM21_G3     | 500D 518Eh       |
| EPWM22_G0     | 5001 618Eh       |
| EPWM22_G1     | 5005 618Eh       |
| EPWM22_G2     | 5009 618Eh       |
| EPWM22_G3     | 500D 618Eh       |
| EPWM23_G0     | 5001 718Eh       |
| EPWM23_G1     | 5005 718Eh       |
| EPWM23_G2     | 5009 718Eh       |
| EPWM23_G3     | 500D 718Eh       |
| EPWM24_G0     | 5001 818Eh       |
| EPWM24_G1     | 5005 818Eh       |
| EPWM24_G2     | 5009 818Eh       |
| EPWM24_G3     | 500D 818Eh       |
| EPWM25_G0     | 5001 918Eh       |
| EPWM25_G1     | 5005 918Eh       |
| EPWM25_G2     | 5009 918Eh       |
| EPWM25_G3     | 500D 918Eh       |
| EPWM26_G0     | 5001 A18Eh       |
| EPWM26_G1     | 5005 A18Eh       |
| EPWM26_G2     | 5009 A18Eh       |
| EPWM26_G3     | 500D A18Eh       |
| EPWM27_G0     | 5001 B18Eh       |
| EPWM27_G1     | 5005 B18Eh       |
| EPWM27_G2     | 5009 B18Eh       |
| EPWM27_G3     | 500D B18Eh       |
| EPWM28_G0     | 5001 C18Eh       |
| EPWM28_G1     | 5005 C18Eh       |
| EPWM28_G2     | 5009 C18Eh       |
| EPWM28_G3     | 500D C18Eh       |
| EPWM29_G0     | 5001 D18Eh       |
| EPWM29_G1     | 5005 D18Eh       |
| EPWM29_G2     | 5009 D18Eh       |
| EPWM29_G3     | 500D D18Eh       |
| EPWM30_G0     | 5001 E18Eh       |
| EPWM30_G1     | 5005 E18Eh       |
| EPWM30_G2     | 5009 E18Eh       |
| EPWM30_G3     | 500D E18Eh       |
| EPWM31_G0     | 5001 F18Eh       |
| EPWM31_G1     | 5005 F18Eh       |
| EPWM31_G2     | 5009 F18Eh       |
| EPWM31_G3     | 500D F18Eh       |

**Figure 3-330. EPWM\_DCFCTL Name Register**

| 15         | 14          | 13       | 12        | 11       | 10     | 9        | 8 |
|------------|-------------|----------|-----------|----------|--------|----------|---|
| EDGESTATUS |             |          | EDGECOUNT |          |        | EDGEMODE |   |
| R          |             |          | R/W       |          |        | R/W      |   |
| 0h         |             |          | 0h        |          |        | 0h       |   |
| 7          | 6           | 5        | 4         | 3        | 2      | 1        | 0 |
| RESERVED_1 | EDGEFILTSEL | PULSESEL |           | BLANKINV | BLANKE | SRCSEL   |   |
| R          | R/W         | R/W      |           | R/W      | R/W    | R/W      |   |
| 0h         | 0h          | 0h       |           | 0h       | 0h     | 0h       |   |

**Table 3-1050. EPWM\_DCFCTL Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                        |
|-------|-------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | EDGESTATUS  | R    | 0h    | Edge Status:<br>These bits reflect the total number of edges currently captured. When the value matches the EDGECOUNT, the status bits are set to zero. and a TBCLK wide pulse is generated which can then be output on the DCEVTFILT signal. The edge counter can be reset by Writing 000 to the EDGECOUNT value: |
| 12:10 | EDGECOUNT   | R/W  | 0h    | Edge Count: These bits select how many edges to count before generating a TBCLK wide pulse on the DCEVTFILT signal:<br>000:no edges, reset current EDGESTATUS bits to 3'b000<br>001:1 edge<br>010:2 edges<br>011:3 edges<br>100:4 edges<br>101:5 edges<br>110:6 edges<br>111:7 edges                               |
| 9:8   | EDGEMODE    | R/W  | 0h    | Edge Mode Select:<br>00:Low To High Edge<br>01:High To Low Edge<br>10:Both Edges<br>11:Reserved                                                                                                                                                                                                                    |
| 7     | RESERVED_1  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                           |
| 6     | EDGEFILTSEL | R/W  | 0h    | Edge Filter Select:<br>0:Edge Filter Not Selected<br>1:Edge Filter Selected                                                                                                                                                                                                                                        |
| 5:4   | PULSESEL    | R/W  | 0h    | Pulse Select For Blanking & Capture Alignment<br>00:Time-base counter equal to period [TBCTR = TBPRD]<br>01:Time-base counter equal to zero [TBCTR = 0x00]<br>10:Time-base counter equal to zero [TBCTR = 0x00] or period [TBCTR = TBPRD]<br>11:Blank Pulse Mix                                                    |
| 3     | BLANKINV    | R/W  | 0h    | Blanking Window Inversion<br>0:Blanking window not inverted<br>1:Blanking window inverted                                                                                                                                                                                                                          |
| 2     | BLANKE      | R/W  | 0h    | Blanking Window Enable/Disable<br>0:Blanking window is disabled<br>1:Blanking window is enabled                                                                                                                                                                                                                    |
| 1:0   | SRCSEL      | R/W  | 0h    | Filter Block Signal Source Select<br>00:Source Is DCAEVT1 Signal<br>01:Source Is DCAEVT2 Signal<br>10:Source Is DCBEVT1 Signal<br>11:Source Is DCBEVT2 Signal                                                                                                                                                      |

### 3.7.2.80 EPWM\_DCCAPCTL Register

#### 1 EPWM\_DCCAPCTL Register (Offset = 190h) [reset = 0h]

Digital Compare Capture Control Register.

Return to [Summary Table](#)

**Table 3-1051. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0190h       |
| EPWM0_G1      | 5004 0190h       |
| EPWM0_G2      | 5008 0190h       |
| EPWM0_G3      | 500C 0190h       |
| EPWM1_G0      | 5000 1190h       |
| EPWM1_G1      | 5004 1190h       |
| EPWM1_G2      | 5008 1190h       |
| EPWM1_G3      | 500C 1190h       |
| EPWM2_G0      | 5000 2190h       |
| EPWM2_G1      | 5004 2190h       |
| EPWM2_G2      | 5008 2190h       |
| EPWM2_G3      | 500C 2190h       |
| EPWM3_G0      | 5000 3190h       |
| EPWM3_G1      | 5004 3190h       |
| EPWM3_G2      | 5008 3190h       |
| EPWM3_G3      | 500C 3190h       |
| EPWM4_G0      | 5000 4190h       |
| EPWM4_G1      | 5004 4190h       |
| EPWM4_G2      | 5008 4190h       |
| EPWM4_G3      | 500C 4190h       |
| EPWM5_G0      | 5000 5190h       |
| EPWM5_G1      | 5004 5190h       |
| EPWM5_G2      | 5008 5190h       |
| EPWM5_G3      | 500C 5190h       |
| EPWM6_G0      | 5000 6190h       |
| EPWM6_G1      | 5004 6190h       |
| EPWM6_G2      | 5008 6190h       |
| EPWM6_G3      | 500C 6190h       |
| EPWM7_G0      | 5000 7190h       |
| EPWM7_G1      | 5004 7190h       |
| EPWM7_G2      | 5008 7190h       |
| EPWM7_G3      | 500C 7190h       |
| EPWM8_G0      | 5000 8190h       |
| EPWM8_G1      | 5004 8190h       |
| EPWM8_G2      | 5008 8190h       |
| EPWM8_G3      | 500C 8190h       |
| EPWM9_G0      | 5000 9190h       |
| EPWM9_G1      | 5004 9190h       |
| EPWM9_G2      | 5008 9190h       |

**Table 3-1051. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9190h       |
| EPWM10_G0     | 5000 A190h       |
| EPWM10_G1     | 5004 A190h       |
| EPWM10_G2     | 5008 A190h       |
| EPWM10_G3     | 500C A190h       |
| EPWM11_G0     | 5000 B190h       |
| EPWM11_G1     | 5004 B190h       |
| EPWM11_G2     | 5008 B190h       |
| EPWM11_G3     | 500C B190h       |
| EPWM12_G0     | 5000 C190h       |
| EPWM12_G1     | 5004 C190h       |
| EPWM12_G2     | 5008 C190h       |
| EPWM12_G3     | 500C C190h       |
| EPWM13_G0     | 5000 D190h       |
| EPWM13_G1     | 5004 D190h       |
| EPWM13_G2     | 5008 D190h       |
| EPWM13_G3     | 500C D190h       |
| EPWM14_G0     | 5000 E190h       |
| EPWM14_G1     | 5004 E190h       |
| EPWM14_G2     | 5008 E190h       |
| EPWM14_G3     | 500C E190h       |
| EPWM15_G0     | 5000 F190h       |
| EPWM15_G1     | 5004 F190h       |
| EPWM15_G2     | 5008 F190h       |
| EPWM15_G3     | 500C F190h       |
| EPWM16_G0     | 5001 0190h       |
| EPWM16_G1     | 5005 0190h       |
| EPWM16_G2     | 5009 0190h       |
| EPWM16_G3     | 500D 0190h       |
| EPWM17_G0     | 5001 1190h       |
| EPWM17_G1     | 5005 1190h       |
| EPWM17_G2     | 5009 1190h       |
| EPWM17_G3     | 500D 1190h       |
| EPWM18_G0     | 5001 2190h       |
| EPWM18_G1     | 5005 2190h       |
| EPWM18_G2     | 5009 2190h       |
| EPWM18_G3     | 500D 2190h       |
| EPWM19_G0     | 5001 3190h       |
| EPWM19_G1     | 5005 3190h       |
| EPWM19_G2     | 5009 3190h       |
| EPWM19_G3     | 500D 3190h       |
| EPWM20_G0     | 5001 4190h       |
| EPWM20_G1     | 5005 4190h       |
| EPWM20_G2     | 5009 4190h       |
| EPWM20_G3     | 500D 4190h       |



**Table 3-1051. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5190h       |
| EPWM21_G1     | 5005 5190h       |
| EPWM21_G2     | 5009 5190h       |
| EPWM21_G3     | 500D 5190h       |
| EPWM22_G0     | 5001 6190h       |
| EPWM22_G1     | 5005 6190h       |
| EPWM22_G2     | 5009 6190h       |
| EPWM22_G3     | 500D 6190h       |
| EPWM23_G0     | 5001 7190h       |
| EPWM23_G1     | 5005 7190h       |
| EPWM23_G2     | 5009 7190h       |
| EPWM23_G3     | 500D 7190h       |
| EPWM24_G0     | 5001 8190h       |
| EPWM24_G1     | 5005 8190h       |
| EPWM24_G2     | 5009 8190h       |
| EPWM24_G3     | 500D 8190h       |
| EPWM25_G0     | 5001 9190h       |
| EPWM25_G1     | 5005 9190h       |
| EPWM25_G2     | 5009 9190h       |
| EPWM25_G3     | 500D 9190h       |
| EPWM26_G0     | 5001 A190h       |
| EPWM26_G1     | 5005 A190h       |
| EPWM26_G2     | 5009 A190h       |
| EPWM26_G3     | 500D A190h       |
| EPWM27_G0     | 5001 B190h       |
| EPWM27_G1     | 5005 B190h       |
| EPWM27_G2     | 5009 B190h       |
| EPWM27_G3     | 500D B190h       |
| EPWM28_G0     | 5001 C190h       |
| EPWM28_G1     | 5005 C190h       |
| EPWM28_G2     | 5009 C190h       |
| EPWM28_G3     | 500D C190h       |
| EPWM29_G0     | 5001 D190h       |
| EPWM29_G1     | 5005 D190h       |
| EPWM29_G2     | 5009 D190h       |
| EPWM29_G3     | 500D D190h       |
| EPWM30_G0     | 5001 E190h       |
| EPWM30_G1     | 5005 E190h       |
| EPWM30_G2     | 5009 E190h       |
| EPWM30_G3     | 500D E190h       |
| EPWM31_G0     | 5001 F190h       |
| EPWM31_G1     | 5005 F190h       |
| EPWM31_G2     | 5009 F190h       |
| EPWM31_G3     | 500D F190h       |

**Figure 3-331. EPWM\_DCCAPCTL Name Register**

| 15         | 14     | 13     | 12         | 11 | 10 | 9        | 8    |
|------------|--------|--------|------------|----|----|----------|------|
| CAPMODE    | CAPCLR | CAPSTS | RESERVED_1 |    |    |          |      |
| R/W        | R/W1TS | R      | R          |    |    |          |      |
| 0h         | 0h     | 0h     | 0h         |    |    |          |      |
| 7          | 6      | 5      | 4          | 3  | 2  | 1        | 0    |
| RESERVED_1 |        |        |            |    |    | SHDWMODE | CAPE |
| R          |        |        |            |    |    | R/W      | R/W  |
| 0h         |        |        |            |    |    | 0h       | 0h   |

**Table 3-1053. EPWM\_DCCAPCTL Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------|--------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | CAPMODE    | R/W    | 0h    | Counter Capture Mode<br>0:When a DCEVTFILT occurs and the counter capture is enabled, then the current TBCNT value is captured in the active register. When the respective trip event occurs, further trip [capture] events are ignored until the next PRD_eq or CNT_zero event [as selected by the PULSESEL bit in the DCFCTL register] re-triggers the capture mechanism.<br>If active mode is enabled, via SHDWMODE bit in DCC0PCTL register, CPU reads of this register will return the active register value.<br>If shadow mode is enabled, via SHDWMODE bit in DCC0PCTL register, the active register is copied to the shadow register on the PRD_eq or CNT_zero event [whichever is selected by PULSESEL bit in DCFCTL register]. CPU reads of this register will return the shadow register value.<br>1:When a DCEVTFILT occurs and the counter capture is enabled, then the current TBCNT value is captured in the active register. When the respective trip event occurs - it will set the CAPSTS flag and further trip [capture] events are ignored until this bit is cleared. CAPSTS can be cleared by writing to CAPCLR bit in DCC0PCTL register and it re-triggers the capture mechanism.<br>If active mode is enabled, via SHDWMODE bit in DCC0PCTL register, CPU reads of this register will return the active register value.<br>If shadow mode is enabled, via SHDWMODE bit in DCC0PCTL register, the active register is copied to the shadow register on the PRD_eq or CNT_zero event [whichever is selected by PULSESEL bit in DCFCTL register]. CPU reads of this register will return the shadow register value. |
| 14   | CAPCLR     | R/W1TS | 0h    | DC Capture Latched Status Clear Flag<br>0:Writing a 0 has no effect.<br>1:Writing a 1 will clear this CAPSTS [set] condition.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 13   | CAPSTS     | R      | 0h    | Latched Status Flag for Capture Event<br>0:No DC capture event occurred.<br>1:A DC capture event has occurred.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 12:2 | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 1    | SHDWMODE   | R/W    | 0h    | TBCTR Counter Capture Shadow Select Mode<br>0:Enable shadow mode. The DCC0P active register is copied to shadow register on a TBCTR = TBPRD or TBCTR = zero event as defined by the DCFCTL[PULSESEL] bit. CPU reads of the DCC0P register will return the shadow register contents.<br>1:Active Mode. In this mode the shadow register is disabled. CPU reads from the DCC0P register will always return the active register contents.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 0    | CAPE       | R/W    | 0h    | TBCTR Counter Capture Enable/Disable<br>0:Disable the time-base counter capture.<br>1:Enable the time-base counter capture.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

### 3.7.2.81 EPWM\_DCOFFSET Register

#### 1 EPWM\_DCOFFSET Register (Offset = 192h) [reset = 0h]

Digital Compare Filter Offset Register .

Return to [Summary Table](#)

**Table 3-1054. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0192h       |
| EPWM0_G1      | 5004 0192h       |
| EPWM0_G2      | 5008 0192h       |
| EPWM0_G3      | 500C 0192h       |
| EPWM1_G0      | 5000 1192h       |
| EPWM1_G1      | 5004 1192h       |
| EPWM1_G2      | 5008 1192h       |
| EPWM1_G3      | 500C 1192h       |
| EPWM2_G0      | 5000 2192h       |
| EPWM2_G1      | 5004 2192h       |
| EPWM2_G2      | 5008 2192h       |
| EPWM2_G3      | 500C 2192h       |
| EPWM3_G0      | 5000 3192h       |
| EPWM3_G1      | 5004 3192h       |
| EPWM3_G2      | 5008 3192h       |
| EPWM3_G3      | 500C 3192h       |
| EPWM4_G0      | 5000 4192h       |
| EPWM4_G1      | 5004 4192h       |
| EPWM4_G2      | 5008 4192h       |
| EPWM4_G3      | 500C 4192h       |
| EPWM5_G0      | 5000 5192h       |
| EPWM5_G1      | 5004 5192h       |
| EPWM5_G2      | 5008 5192h       |
| EPWM5_G3      | 500C 5192h       |
| EPWM6_G0      | 5000 6192h       |
| EPWM6_G1      | 5004 6192h       |
| EPWM6_G2      | 5008 6192h       |
| EPWM6_G3      | 500C 6192h       |
| EPWM7_G0      | 5000 7192h       |
| EPWM7_G1      | 5004 7192h       |
| EPWM7_G2      | 5008 7192h       |
| EPWM7_G3      | 500C 7192h       |
| EPWM8_G0      | 5000 8192h       |
| EPWM8_G1      | 5004 8192h       |
| EPWM8_G2      | 5008 8192h       |
| EPWM8_G3      | 500C 8192h       |
| EPWM9_G0      | 5000 9192h       |
| EPWM9_G1      | 5004 9192h       |
| EPWM9_G2      | 5008 9192h       |

**Table 3-1054. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9192h       |
| EPWM10_G0     | 5000 A192h       |
| EPWM10_G1     | 5004 A192h       |
| EPWM10_G2     | 5008 A192h       |
| EPWM10_G3     | 500C A192h       |
| EPWM11_G0     | 5000 B192h       |
| EPWM11_G1     | 5004 B192h       |
| EPWM11_G2     | 5008 B192h       |
| EPWM11_G3     | 500C B192h       |
| EPWM12_G0     | 5000 C192h       |
| EPWM12_G1     | 5004 C192h       |
| EPWM12_G2     | 5008 C192h       |
| EPWM12_G3     | 500C C192h       |
| EPWM13_G0     | 5000 D192h       |
| EPWM13_G1     | 5004 D192h       |
| EPWM13_G2     | 5008 D192h       |
| EPWM13_G3     | 500C D192h       |
| EPWM14_G0     | 5000 E192h       |
| EPWM14_G1     | 5004 E192h       |
| EPWM14_G2     | 5008 E192h       |
| EPWM14_G3     | 500C E192h       |
| EPWM15_G0     | 5000 F192h       |
| EPWM15_G1     | 5004 F192h       |
| EPWM15_G2     | 5008 F192h       |
| EPWM15_G3     | 500C F192h       |
| EPWM16_G0     | 5001 0192h       |
| EPWM16_G1     | 5005 0192h       |
| EPWM16_G2     | 5009 0192h       |
| EPWM16_G3     | 500D 0192h       |
| EPWM17_G0     | 5001 1192h       |
| EPWM17_G1     | 5005 1192h       |
| EPWM17_G2     | 5009 1192h       |
| EPWM17_G3     | 500D 1192h       |
| EPWM18_G0     | 5001 2192h       |
| EPWM18_G1     | 5005 2192h       |
| EPWM18_G2     | 5009 2192h       |
| EPWM18_G3     | 500D 2192h       |
| EPWM19_G0     | 5001 3192h       |
| EPWM19_G1     | 5005 3192h       |
| EPWM19_G2     | 5009 3192h       |
| EPWM19_G3     | 500D 3192h       |
| EPWM20_G0     | 5001 4192h       |
| EPWM20_G1     | 5005 4192h       |
| EPWM20_G2     | 5009 4192h       |
| EPWM20_G3     | 500D 4192h       |

**Table 3-1054. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5192h       |
| EPWM21_G1     | 5005 5192h       |
| EPWM21_G2     | 5009 5192h       |
| EPWM21_G3     | 500D 5192h       |
| EPWM22_G0     | 5001 6192h       |
| EPWM22_G1     | 5005 6192h       |
| EPWM22_G2     | 5009 6192h       |
| EPWM22_G3     | 500D 6192h       |
| EPWM23_G0     | 5001 7192h       |
| EPWM23_G1     | 5005 7192h       |
| EPWM23_G2     | 5009 7192h       |
| EPWM23_G3     | 500D 7192h       |
| EPWM24_G0     | 5001 8192h       |
| EPWM24_G1     | 5005 8192h       |
| EPWM24_G2     | 5009 8192h       |
| EPWM24_G3     | 500D 8192h       |
| EPWM25_G0     | 5001 9192h       |
| EPWM25_G1     | 5005 9192h       |
| EPWM25_G2     | 5009 9192h       |
| EPWM25_G3     | 500D 9192h       |
| EPWM26_G0     | 5001 A192h       |
| EPWM26_G1     | 5005 A192h       |
| EPWM26_G2     | 5009 A192h       |
| EPWM26_G3     | 500D A192h       |
| EPWM27_G0     | 5001 B192h       |
| EPWM27_G1     | 5005 B192h       |
| EPWM27_G2     | 5009 B192h       |
| EPWM27_G3     | 500D B192h       |
| EPWM28_G0     | 5001 C192h       |
| EPWM28_G1     | 5005 C192h       |
| EPWM28_G2     | 5009 C192h       |
| EPWM28_G3     | 500D C192h       |
| EPWM29_G0     | 5001 D192h       |
| EPWM29_G1     | 5005 D192h       |
| EPWM29_G2     | 5009 D192h       |
| EPWM29_G3     | 500D D192h       |
| EPWM30_G0     | 5001 E192h       |
| EPWM30_G1     | 5005 E192h       |
| EPWM30_G2     | 5009 E192h       |
| EPWM30_G3     | 500D E192h       |
| EPWM31_G0     | 5001 F192h       |
| EPWM31_G1     | 5005 F192h       |
| EPWM31_G2     | 5009 F192h       |
| EPWM31_G3     | 500D F192h       |

**Figure 3-332. EPWM\_DCFOFFSET Name Register**

|           |    |    |    |    |    |   |   |
|-----------|----|----|----|----|----|---|---|
| 15        | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DCFOFFSET |    |    |    |    |    |   |   |
| R/W       |    |    |    |    |    |   |   |
| 0h        |    |    |    |    |    |   |   |
| 7         | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| DCFOFFSET |    |    |    |    |    |   |   |
| R/W       |    |    |    |    |    |   |   |
| 0h        |    |    |    |    |    |   |   |

**Table 3-1056. EPWM\_DCFOFFSET Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------|-----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | DCFOFFSET | R/W  | 0h    | <p>Blanking Window Offset</p> <p>These 16-bits specify the number of TBCLK cycles from the blanking window reference to the point when the blanking window is applied. The blanking window reference is either period or zero as defined by the DCFCTL[PULSESEL] bit. This offset register is shadowed and the active register is loaded at the reference point defined by DCFCTL[PULSESEL]. The offset counter is also initialized and begins to count down when the active register is loaded. When the counter expires, the blanking window is applied. If the blanking window is currently active, then the blanking window counter is restarted.</p> |

### 3.7.2.82 EPWM\_DCOFFSETCNT Register

#### 1 EPWM\_DCOFFSETCNT Register (Offset = 194h) [reset = 0h]

Digital Compare Filter Offset Counter Register.

Return to [Summary Table](#)

**Table 3-1057. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0194h       |
| EPWM0_G1      | 5004 0194h       |
| EPWM0_G2      | 5008 0194h       |
| EPWM0_G3      | 500C 0194h       |
| EPWM1_G0      | 5000 1194h       |
| EPWM1_G1      | 5004 1194h       |
| EPWM1_G2      | 5008 1194h       |
| EPWM1_G3      | 500C 1194h       |
| EPWM2_G0      | 5000 2194h       |
| EPWM2_G1      | 5004 2194h       |
| EPWM2_G2      | 5008 2194h       |
| EPWM2_G3      | 500C 2194h       |
| EPWM3_G0      | 5000 3194h       |
| EPWM3_G1      | 5004 3194h       |
| EPWM3_G2      | 5008 3194h       |
| EPWM3_G3      | 500C 3194h       |
| EPWM4_G0      | 5000 4194h       |
| EPWM4_G1      | 5004 4194h       |
| EPWM4_G2      | 5008 4194h       |
| EPWM4_G3      | 500C 4194h       |
| EPWM5_G0      | 5000 5194h       |
| EPWM5_G1      | 5004 5194h       |
| EPWM5_G2      | 5008 5194h       |
| EPWM5_G3      | 500C 5194h       |
| EPWM6_G0      | 5000 6194h       |
| EPWM6_G1      | 5004 6194h       |
| EPWM6_G2      | 5008 6194h       |
| EPWM6_G3      | 500C 6194h       |
| EPWM7_G0      | 5000 7194h       |
| EPWM7_G1      | 5004 7194h       |
| EPWM7_G2      | 5008 7194h       |
| EPWM7_G3      | 500C 7194h       |
| EPWM8_G0      | 5000 8194h       |
| EPWM8_G1      | 5004 8194h       |
| EPWM8_G2      | 5008 8194h       |
| EPWM8_G3      | 500C 8194h       |
| EPWM9_G0      | 5000 9194h       |
| EPWM9_G1      | 5004 9194h       |
| EPWM9_G2      | 5008 9194h       |

**Table 3-1057. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9194h       |
| EPWM10_G0     | 5000 A194h       |
| EPWM10_G1     | 5004 A194h       |
| EPWM10_G2     | 5008 A194h       |
| EPWM10_G3     | 500C A194h       |
| EPWM11_G0     | 5000 B194h       |
| EPWM11_G1     | 5004 B194h       |
| EPWM11_G2     | 5008 B194h       |
| EPWM11_G3     | 500C B194h       |
| EPWM12_G0     | 5000 C194h       |
| EPWM12_G1     | 5004 C194h       |
| EPWM12_G2     | 5008 C194h       |
| EPWM12_G3     | 500C C194h       |
| EPWM13_G0     | 5000 D194h       |
| EPWM13_G1     | 5004 D194h       |
| EPWM13_G2     | 5008 D194h       |
| EPWM13_G3     | 500C D194h       |
| EPWM14_G0     | 5000 E194h       |
| EPWM14_G1     | 5004 E194h       |
| EPWM14_G2     | 5008 E194h       |
| EPWM14_G3     | 500C E194h       |
| EPWM15_G0     | 5000 F194h       |
| EPWM15_G1     | 5004 F194h       |
| EPWM15_G2     | 5008 F194h       |
| EPWM15_G3     | 500C F194h       |
| EPWM16_G0     | 5001 0194h       |
| EPWM16_G1     | 5005 0194h       |
| EPWM16_G2     | 5009 0194h       |
| EPWM16_G3     | 500D 0194h       |
| EPWM17_G0     | 5001 1194h       |
| EPWM17_G1     | 5005 1194h       |
| EPWM17_G2     | 5009 1194h       |
| EPWM17_G3     | 500D 1194h       |
| EPWM18_G0     | 5001 2194h       |
| EPWM18_G1     | 5005 2194h       |
| EPWM18_G2     | 5009 2194h       |
| EPWM18_G3     | 500D 2194h       |
| EPWM19_G0     | 5001 3194h       |
| EPWM19_G1     | 5005 3194h       |
| EPWM19_G2     | 5009 3194h       |
| EPWM19_G3     | 500D 3194h       |
| EPWM20_G0     | 5001 4194h       |
| EPWM20_G1     | 5005 4194h       |
| EPWM20_G2     | 5009 4194h       |
| EPWM20_G3     | 500D 4194h       |



**Table 3-1057. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5194h       |
| EPWM21_G1     | 5005 5194h       |
| EPWM21_G2     | 5009 5194h       |
| EPWM21_G3     | 500D 5194h       |
| EPWM22_G0     | 5001 6194h       |
| EPWM22_G1     | 5005 6194h       |
| EPWM22_G2     | 5009 6194h       |
| EPWM22_G3     | 500D 6194h       |
| EPWM23_G0     | 5001 7194h       |
| EPWM23_G1     | 5005 7194h       |
| EPWM23_G2     | 5009 7194h       |
| EPWM23_G3     | 500D 7194h       |
| EPWM24_G0     | 5001 8194h       |
| EPWM24_G1     | 5005 8194h       |
| EPWM24_G2     | 5009 8194h       |
| EPWM24_G3     | 500D 8194h       |
| EPWM25_G0     | 5001 9194h       |
| EPWM25_G1     | 5005 9194h       |
| EPWM25_G2     | 5009 9194h       |
| EPWM25_G3     | 500D 9194h       |
| EPWM26_G0     | 5001 A194h       |
| EPWM26_G1     | 5005 A194h       |
| EPWM26_G2     | 5009 A194h       |
| EPWM26_G3     | 500D A194h       |
| EPWM27_G0     | 5001 B194h       |
| EPWM27_G1     | 5005 B194h       |
| EPWM27_G2     | 5009 B194h       |
| EPWM27_G3     | 500D B194h       |
| EPWM28_G0     | 5001 C194h       |
| EPWM28_G1     | 5005 C194h       |
| EPWM28_G2     | 5009 C194h       |
| EPWM28_G3     | 500D C194h       |
| EPWM29_G0     | 5001 D194h       |
| EPWM29_G1     | 5005 D194h       |
| EPWM29_G2     | 5009 D194h       |
| EPWM29_G3     | 500D D194h       |
| EPWM30_G0     | 5001 E194h       |
| EPWM30_G1     | 5005 E194h       |
| EPWM30_G2     | 5009 E194h       |
| EPWM30_G3     | 500D E194h       |
| EPWM31_G0     | 5001 F194h       |
| EPWM31_G1     | 5005 F194h       |
| EPWM31_G2     | 5009 F194h       |
| EPWM31_G3     | 500D F194h       |

**Figure 3-333. EPWM\_DCFOFFSETCNT Name Register**

|              |    |    |    |    |    |   |   |
|--------------|----|----|----|----|----|---|---|
| 15           | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DCFOFFSETCNT |    |    |    |    |    |   |   |
| R            |    |    |    |    |    |   |   |
| 0h           |    |    |    |    |    |   |   |
| 7            | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| DCFOFFSETCNT |    |    |    |    |    |   |   |
| R            |    |    |    |    |    |   |   |
| 0h           |    |    |    |    |    |   |   |

**Table 3-1059. EPWM\_DCFOFFSETCNT Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                |
|------|--------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | DCFOFFSETCNT | R    | 0h    | Blanking Offset Counter<br>These 16-bits are read only and indicate the current value of the offset counter. The counter counts down to zero and then stops until it is re-loaded on the next period or zero event as defined by the DCFCTL[PULSESEL] bit. The offset counter is not affected by the free/soft emulation bits. That is, it will always continue to count down if the device is halted by a emulation stop. |

### 3.7.2.83 EPWM\_DCFWINDOW Register

#### 1 EPWM\_DCFWINDOW Register (Offset = 196h) [reset = 0h]

Digital Compare Filter Window Register.

Return to [Summary Table](#)

**Table 3-1060. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0196h       |
| EPWM0_G1      | 5004 0196h       |
| EPWM0_G2      | 5008 0196h       |
| EPWM0_G3      | 500C 0196h       |
| EPWM1_G0      | 5000 1196h       |
| EPWM1_G1      | 5004 1196h       |
| EPWM1_G2      | 5008 1196h       |
| EPWM1_G3      | 500C 1196h       |
| EPWM2_G0      | 5000 2196h       |
| EPWM2_G1      | 5004 2196h       |
| EPWM2_G2      | 5008 2196h       |
| EPWM2_G3      | 500C 2196h       |
| EPWM3_G0      | 5000 3196h       |
| EPWM3_G1      | 5004 3196h       |
| EPWM3_G2      | 5008 3196h       |
| EPWM3_G3      | 500C 3196h       |
| EPWM4_G0      | 5000 4196h       |
| EPWM4_G1      | 5004 4196h       |
| EPWM4_G2      | 5008 4196h       |
| EPWM4_G3      | 500C 4196h       |
| EPWM5_G0      | 5000 5196h       |
| EPWM5_G1      | 5004 5196h       |
| EPWM5_G2      | 5008 5196h       |
| EPWM5_G3      | 500C 5196h       |
| EPWM6_G0      | 5000 6196h       |
| EPWM6_G1      | 5004 6196h       |
| EPWM6_G2      | 5008 6196h       |
| EPWM6_G3      | 500C 6196h       |
| EPWM7_G0      | 5000 7196h       |
| EPWM7_G1      | 5004 7196h       |
| EPWM7_G2      | 5008 7196h       |
| EPWM7_G3      | 500C 7196h       |
| EPWM8_G0      | 5000 8196h       |
| EPWM8_G1      | 5004 8196h       |
| EPWM8_G2      | 5008 8196h       |
| EPWM8_G3      | 500C 8196h       |
| EPWM9_G0      | 5000 9196h       |
| EPWM9_G1      | 5004 9196h       |
| EPWM9_G2      | 5008 9196h       |

**Table 3-1060. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9196h       |
| EPWM10_G0     | 5000 A196h       |
| EPWM10_G1     | 5004 A196h       |
| EPWM10_G2     | 5008 A196h       |
| EPWM10_G3     | 500C A196h       |
| EPWM11_G0     | 5000 B196h       |
| EPWM11_G1     | 5004 B196h       |
| EPWM11_G2     | 5008 B196h       |
| EPWM11_G3     | 500C B196h       |
| EPWM12_G0     | 5000 C196h       |
| EPWM12_G1     | 5004 C196h       |
| EPWM12_G2     | 5008 C196h       |
| EPWM12_G3     | 500C C196h       |
| EPWM13_G0     | 5000 D196h       |
| EPWM13_G1     | 5004 D196h       |
| EPWM13_G2     | 5008 D196h       |
| EPWM13_G3     | 500C D196h       |
| EPWM14_G0     | 5000 E196h       |
| EPWM14_G1     | 5004 E196h       |
| EPWM14_G2     | 5008 E196h       |
| EPWM14_G3     | 500C E196h       |
| EPWM15_G0     | 5000 F196h       |
| EPWM15_G1     | 5004 F196h       |
| EPWM15_G2     | 5008 F196h       |
| EPWM15_G3     | 500C F196h       |
| EPWM16_G0     | 5001 0196h       |
| EPWM16_G1     | 5005 0196h       |
| EPWM16_G2     | 5009 0196h       |
| EPWM16_G3     | 500D 0196h       |
| EPWM17_G0     | 5001 1196h       |
| EPWM17_G1     | 5005 1196h       |
| EPWM17_G2     | 5009 1196h       |
| EPWM17_G3     | 500D 1196h       |
| EPWM18_G0     | 5001 2196h       |
| EPWM18_G1     | 5005 2196h       |
| EPWM18_G2     | 5009 2196h       |
| EPWM18_G3     | 500D 2196h       |
| EPWM19_G0     | 5001 3196h       |
| EPWM19_G1     | 5005 3196h       |
| EPWM19_G2     | 5009 3196h       |
| EPWM19_G3     | 500D 3196h       |
| EPWM20_G0     | 5001 4196h       |
| EPWM20_G1     | 5005 4196h       |
| EPWM20_G2     | 5009 4196h       |
| EPWM20_G3     | 500D 4196h       |

**Table 3-1060. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5196h       |
| EPWM21_G1     | 5005 5196h       |
| EPWM21_G2     | 5009 5196h       |
| EPWM21_G3     | 500D 5196h       |
| EPWM22_G0     | 5001 6196h       |
| EPWM22_G1     | 5005 6196h       |
| EPWM22_G2     | 5009 6196h       |
| EPWM22_G3     | 500D 6196h       |
| EPWM23_G0     | 5001 7196h       |
| EPWM23_G1     | 5005 7196h       |
| EPWM23_G2     | 5009 7196h       |
| EPWM23_G3     | 500D 7196h       |
| EPWM24_G0     | 5001 8196h       |
| EPWM24_G1     | 5005 8196h       |
| EPWM24_G2     | 5009 8196h       |
| EPWM24_G3     | 500D 8196h       |
| EPWM25_G0     | 5001 9196h       |
| EPWM25_G1     | 5005 9196h       |
| EPWM25_G2     | 5009 9196h       |
| EPWM25_G3     | 500D 9196h       |
| EPWM26_G0     | 5001 A196h       |
| EPWM26_G1     | 5005 A196h       |
| EPWM26_G2     | 5009 A196h       |
| EPWM26_G3     | 500D A196h       |
| EPWM27_G0     | 5001 B196h       |
| EPWM27_G1     | 5005 B196h       |
| EPWM27_G2     | 5009 B196h       |
| EPWM27_G3     | 500D B196h       |
| EPWM28_G0     | 5001 C196h       |
| EPWM28_G1     | 5005 C196h       |
| EPWM28_G2     | 5009 C196h       |
| EPWM28_G3     | 500D C196h       |
| EPWM29_G0     | 5001 D196h       |
| EPWM29_G1     | 5005 D196h       |
| EPWM29_G2     | 5009 D196h       |
| EPWM29_G3     | 500D D196h       |
| EPWM30_G0     | 5001 E196h       |
| EPWM30_G1     | 5005 E196h       |
| EPWM30_G2     | 5009 E196h       |
| EPWM30_G3     | 500D E196h       |
| EPWM31_G0     | 5001 F196h       |
| EPWM31_G1     | 5005 F196h       |
| EPWM31_G2     | 5009 F196h       |
| EPWM31_G3     | 500D F196h       |

**Figure 3-334. EPWM\_DCFWINDOW Name Register**

|           |    |    |    |    |    |   |   |
|-----------|----|----|----|----|----|---|---|
| 15        | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DCFWINDOW |    |    |    |    |    |   |   |
| R/W       |    |    |    |    |    |   |   |
| 0h        |    |    |    |    |    |   |   |
| 7         | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| DCFWINDOW |    |    |    |    |    |   |   |
| R/W       |    |    |    |    |    |   |   |
| 0h        |    |    |    |    |    |   |   |

**Table 3-1062. EPWM\_DCFWINDOW Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|------|-----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | DCFWINDOW | R/W  | 0h    | Blanking Window Width<br>00h No blanking window is generated.<br>01-FFFFh: Specifies the width of the blanking window in TBCLK cycles. The blanking window begins when the offset counter expires. When this occurs, the window counter is loaded and begins to count down. If the blanking window is currently active and the offset counter expires, the blanking window counter is not restarted and the blanking window is cut short prematurely. Care should be taken to avoid this situation. The blanking window can cross a PWM period boundary. |

### 3.7.2.84 EPWM\_DCFWINDOWCNT Register

#### 1 EPWM\_DCFWINDOWCNT Register (Offset = 198h) [reset = 0h]

Digital Compare Filter Window Counter Register.

Return to [Summary Table](#)

**Table 3-1063. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0198h       |
| EPWM0_G1      | 5004 0198h       |
| EPWM0_G2      | 5008 0198h       |
| EPWM0_G3      | 500C 0198h       |
| EPWM1_G0      | 5000 1198h       |
| EPWM1_G1      | 5004 1198h       |
| EPWM1_G2      | 5008 1198h       |
| EPWM1_G3      | 500C 1198h       |
| EPWM2_G0      | 5000 2198h       |
| EPWM2_G1      | 5004 2198h       |
| EPWM2_G2      | 5008 2198h       |
| EPWM2_G3      | 500C 2198h       |
| EPWM3_G0      | 5000 3198h       |
| EPWM3_G1      | 5004 3198h       |
| EPWM3_G2      | 5008 3198h       |
| EPWM3_G3      | 500C 3198h       |
| EPWM4_G0      | 5000 4198h       |
| EPWM4_G1      | 5004 4198h       |
| EPWM4_G2      | 5008 4198h       |
| EPWM4_G3      | 500C 4198h       |
| EPWM5_G0      | 5000 5198h       |
| EPWM5_G1      | 5004 5198h       |
| EPWM5_G2      | 5008 5198h       |
| EPWM5_G3      | 500C 5198h       |
| EPWM6_G0      | 5000 6198h       |
| EPWM6_G1      | 5004 6198h       |
| EPWM6_G2      | 5008 6198h       |
| EPWM6_G3      | 500C 6198h       |
| EPWM7_G0      | 5000 7198h       |
| EPWM7_G1      | 5004 7198h       |
| EPWM7_G2      | 5008 7198h       |
| EPWM7_G3      | 500C 7198h       |
| EPWM8_G0      | 5000 8198h       |
| EPWM8_G1      | 5004 8198h       |
| EPWM8_G2      | 5008 8198h       |
| EPWM8_G3      | 500C 8198h       |
| EPWM9_G0      | 5000 9198h       |
| EPWM9_G1      | 5004 9198h       |
| EPWM9_G2      | 5008 9198h       |

**Table 3-1063. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9198h       |
| EPWM10_G0     | 5000 A198h       |
| EPWM10_G1     | 5004 A198h       |
| EPWM10_G2     | 5008 A198h       |
| EPWM10_G3     | 500C A198h       |
| EPWM11_G0     | 5000 B198h       |
| EPWM11_G1     | 5004 B198h       |
| EPWM11_G2     | 5008 B198h       |
| EPWM11_G3     | 500C B198h       |
| EPWM12_G0     | 5000 C198h       |
| EPWM12_G1     | 5004 C198h       |
| EPWM12_G2     | 5008 C198h       |
| EPWM12_G3     | 500C C198h       |
| EPWM13_G0     | 5000 D198h       |
| EPWM13_G1     | 5004 D198h       |
| EPWM13_G2     | 5008 D198h       |
| EPWM13_G3     | 500C D198h       |
| EPWM14_G0     | 5000 E198h       |
| EPWM14_G1     | 5004 E198h       |
| EPWM14_G2     | 5008 E198h       |
| EPWM14_G3     | 500C E198h       |
| EPWM15_G0     | 5000 F198h       |
| EPWM15_G1     | 5004 F198h       |
| EPWM15_G2     | 5008 F198h       |
| EPWM15_G3     | 500C F198h       |
| EPWM16_G0     | 5001 0198h       |
| EPWM16_G1     | 5005 0198h       |
| EPWM16_G2     | 5009 0198h       |
| EPWM16_G3     | 500D 0198h       |
| EPWM17_G0     | 5001 1198h       |
| EPWM17_G1     | 5005 1198h       |
| EPWM17_G2     | 5009 1198h       |
| EPWM17_G3     | 500D 1198h       |
| EPWM18_G0     | 5001 2198h       |
| EPWM18_G1     | 5005 2198h       |
| EPWM18_G2     | 5009 2198h       |
| EPWM18_G3     | 500D 2198h       |
| EPWM19_G0     | 5001 3198h       |
| EPWM19_G1     | 5005 3198h       |
| EPWM19_G2     | 5009 3198h       |
| EPWM19_G3     | 500D 3198h       |
| EPWM20_G0     | 5001 4198h       |
| EPWM20_G1     | 5005 4198h       |
| EPWM20_G2     | 5009 4198h       |
| EPWM20_G3     | 500D 4198h       |



**Table 3-1063. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5198h       |
| EPWM21_G1     | 5005 5198h       |
| EPWM21_G2     | 5009 5198h       |
| EPWM21_G3     | 500D 5198h       |
| EPWM22_G0     | 5001 6198h       |
| EPWM22_G1     | 5005 6198h       |
| EPWM22_G2     | 5009 6198h       |
| EPWM22_G3     | 500D 6198h       |
| EPWM23_G0     | 5001 7198h       |
| EPWM23_G1     | 5005 7198h       |
| EPWM23_G2     | 5009 7198h       |
| EPWM23_G3     | 500D 7198h       |
| EPWM24_G0     | 5001 8198h       |
| EPWM24_G1     | 5005 8198h       |
| EPWM24_G2     | 5009 8198h       |
| EPWM24_G3     | 500D 8198h       |
| EPWM25_G0     | 5001 9198h       |
| EPWM25_G1     | 5005 9198h       |
| EPWM25_G2     | 5009 9198h       |
| EPWM25_G3     | 500D 9198h       |
| EPWM26_G0     | 5001 A198h       |
| EPWM26_G1     | 5005 A198h       |
| EPWM26_G2     | 5009 A198h       |
| EPWM26_G3     | 500D A198h       |
| EPWM27_G0     | 5001 B198h       |
| EPWM27_G1     | 5005 B198h       |
| EPWM27_G2     | 5009 B198h       |
| EPWM27_G3     | 500D B198h       |
| EPWM28_G0     | 5001 C198h       |
| EPWM28_G1     | 5005 C198h       |
| EPWM28_G2     | 5009 C198h       |
| EPWM28_G3     | 500D C198h       |
| EPWM29_G0     | 5001 D198h       |
| EPWM29_G1     | 5005 D198h       |
| EPWM29_G2     | 5009 D198h       |
| EPWM29_G3     | 500D D198h       |
| EPWM30_G0     | 5001 E198h       |
| EPWM30_G1     | 5005 E198h       |
| EPWM30_G2     | 5009 E198h       |
| EPWM30_G3     | 500D E198h       |
| EPWM31_G0     | 5001 F198h       |
| EPWM31_G1     | 5005 F198h       |
| EPWM31_G2     | 5009 F198h       |
| EPWM31_G3     | 500D F198h       |

**Figure 3-335. EPWM\_DCFWINDOWCNT Name Register**

|              |    |    |    |    |    |   |   |
|--------------|----|----|----|----|----|---|---|
| 15           | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DCFWINDOWCNT |    |    |    |    |    |   |   |
| R            |    |    |    |    |    |   |   |
| 0h           |    |    |    |    |    |   |   |
| 7            | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| DCFWINDOWCNT |    |    |    |    |    |   |   |
| R            |    |    |    |    |    |   |   |
| 0h           |    |    |    |    |    |   |   |

**Table 3-1065. EPWM\_DCFWINDOWCNT Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                                                                                                                                                   |
|------|--------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | DCFWINDOWCNT | R    | 0h    | Blanking Window Counter<br>These 16 bits are read only and indicate the current value of the window counter. The counter counts down to zero and then stops until it is re-loaded when the offset counter reaches zero again. |

### 3.7.2.85 EPWM\_BLANKPULSEMIXSEL Register

#### 1 EPWM\_BLANKPULSEMIXSEL Register (Offset = 19Ah) [reset = 0h]

Blanking window trigger pulse select register.

Return to [Summary Table](#)

**Table 3-1066. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 019Ah       |
| EPWM0_G1      | 5004 019Ah       |
| EPWM0_G2      | 5008 019Ah       |
| EPWM0_G3      | 500C 019Ah       |
| EPWM1_G0      | 5000 119Ah       |
| EPWM1_G1      | 5004 119Ah       |
| EPWM1_G2      | 5008 119Ah       |
| EPWM1_G3      | 500C 119Ah       |
| EPWM2_G0      | 5000 219Ah       |
| EPWM2_G1      | 5004 219Ah       |
| EPWM2_G2      | 5008 219Ah       |
| EPWM2_G3      | 500C 219Ah       |
| EPWM3_G0      | 5000 319Ah       |
| EPWM3_G1      | 5004 319Ah       |
| EPWM3_G2      | 5008 319Ah       |
| EPWM3_G3      | 500C 319Ah       |
| EPWM4_G0      | 5000 419Ah       |
| EPWM4_G1      | 5004 419Ah       |
| EPWM4_G2      | 5008 419Ah       |
| EPWM4_G3      | 500C 419Ah       |
| EPWM5_G0      | 5000 519Ah       |
| EPWM5_G1      | 5004 519Ah       |
| EPWM5_G2      | 5008 519Ah       |
| EPWM5_G3      | 500C 519Ah       |
| EPWM6_G0      | 5000 619Ah       |
| EPWM6_G1      | 5004 619Ah       |
| EPWM6_G2      | 5008 619Ah       |
| EPWM6_G3      | 500C 619Ah       |
| EPWM7_G0      | 5000 719Ah       |
| EPWM7_G1      | 5004 719Ah       |
| EPWM7_G2      | 5008 719Ah       |
| EPWM7_G3      | 500C 719Ah       |
| EPWM8_G0      | 5000 819Ah       |
| EPWM8_G1      | 5004 819Ah       |
| EPWM8_G2      | 5008 819Ah       |
| EPWM8_G3      | 500C 819Ah       |
| EPWM9_G0      | 5000 919Ah       |
| EPWM9_G1      | 5004 919Ah       |
| EPWM9_G2      | 5008 919Ah       |

**Table 3-1066. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 919Ah       |
| EPWM10_G0     | 5000 A19Ah       |
| EPWM10_G1     | 5004 A19Ah       |
| EPWM10_G2     | 5008 A19Ah       |
| EPWM10_G3     | 500C A19Ah       |
| EPWM11_G0     | 5000 B19Ah       |
| EPWM11_G1     | 5004 B19Ah       |
| EPWM11_G2     | 5008 B19Ah       |
| EPWM11_G3     | 500C B19Ah       |
| EPWM12_G0     | 5000 C19Ah       |
| EPWM12_G1     | 5004 C19Ah       |
| EPWM12_G2     | 5008 C19Ah       |
| EPWM12_G3     | 500C C19Ah       |
| EPWM13_G0     | 5000 D19Ah       |
| EPWM13_G1     | 5004 D19Ah       |
| EPWM13_G2     | 5008 D19Ah       |
| EPWM13_G3     | 500C D19Ah       |
| EPWM14_G0     | 5000 E19Ah       |
| EPWM14_G1     | 5004 E19Ah       |
| EPWM14_G2     | 5008 E19Ah       |
| EPWM14_G3     | 500C E19Ah       |
| EPWM15_G0     | 5000 F19Ah       |
| EPWM15_G1     | 5004 F19Ah       |
| EPWM15_G2     | 5008 F19Ah       |
| EPWM15_G3     | 500C F19Ah       |
| EPWM16_G0     | 5001 019Ah       |
| EPWM16_G1     | 5005 019Ah       |
| EPWM16_G2     | 5009 019Ah       |
| EPWM16_G3     | 500D 019Ah       |
| EPWM17_G0     | 5001 119Ah       |
| EPWM17_G1     | 5005 119Ah       |
| EPWM17_G2     | 5009 119Ah       |
| EPWM17_G3     | 500D 119Ah       |
| EPWM18_G0     | 5001 219Ah       |
| EPWM18_G1     | 5005 219Ah       |
| EPWM18_G2     | 5009 219Ah       |
| EPWM18_G3     | 500D 219Ah       |
| EPWM19_G0     | 5001 319Ah       |
| EPWM19_G1     | 5005 319Ah       |
| EPWM19_G2     | 5009 319Ah       |
| EPWM19_G3     | 500D 319Ah       |
| EPWM20_G0     | 5001 419Ah       |
| EPWM20_G1     | 5005 419Ah       |
| EPWM20_G2     | 5009 419Ah       |
| EPWM20_G3     | 500D 419Ah       |

**Table 3-1066. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 519Ah       |
| EPWM21_G1     | 5005 519Ah       |
| EPWM21_G2     | 5009 519Ah       |
| EPWM21_G3     | 500D 519Ah       |
| EPWM22_G0     | 5001 619Ah       |
| EPWM22_G1     | 5005 619Ah       |
| EPWM22_G2     | 5009 619Ah       |
| EPWM22_G3     | 500D 619Ah       |
| EPWM23_G0     | 5001 719Ah       |
| EPWM23_G1     | 5005 719Ah       |
| EPWM23_G2     | 5009 719Ah       |
| EPWM23_G3     | 500D 719Ah       |
| EPWM24_G0     | 5001 819Ah       |
| EPWM24_G1     | 5005 819Ah       |
| EPWM24_G2     | 5009 819Ah       |
| EPWM24_G3     | 500D 819Ah       |
| EPWM25_G0     | 5001 919Ah       |
| EPWM25_G1     | 5005 919Ah       |
| EPWM25_G2     | 5009 919Ah       |
| EPWM25_G3     | 500D 919Ah       |
| EPWM26_G0     | 5001 A19Ah       |
| EPWM26_G1     | 5005 A19Ah       |
| EPWM26_G2     | 5009 A19Ah       |
| EPWM26_G3     | 500D A19Ah       |
| EPWM27_G0     | 5001 B19Ah       |
| EPWM27_G1     | 5005 B19Ah       |
| EPWM27_G2     | 5009 B19Ah       |
| EPWM27_G3     | 500D B19Ah       |
| EPWM28_G0     | 5001 C19Ah       |
| EPWM28_G1     | 5005 C19Ah       |
| EPWM28_G2     | 5009 C19Ah       |
| EPWM28_G3     | 500D C19Ah       |
| EPWM29_G0     | 5001 D19Ah       |
| EPWM29_G1     | 5005 D19Ah       |
| EPWM29_G2     | 5009 D19Ah       |
| EPWM29_G3     | 500D D19Ah       |
| EPWM30_G0     | 5001 E19Ah       |
| EPWM30_G1     | 5005 E19Ah       |
| EPWM30_G2     | 5009 E19Ah       |
| EPWM30_G3     | 500D E19Ah       |
| EPWM31_G0     | 5001 F19Ah       |
| EPWM31_G1     | 5005 F19Ah       |
| EPWM31_G2     | 5009 F19Ah       |
| EPWM31_G3     | 500D F19Ah       |

**Figure 3-336. EPWM\_BLANKPULSEMIXSEL Name Register**

| 15         | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|------------|-----|-----|-----|-----|-----|-----|-----|
| RESERVED_1 |     |     |     |     |     | CDD | CDU |
| R          |     |     |     |     |     | R/W | R/W |
| 0h         |     |     |     |     |     | 0h  | 0h  |
| 7          | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| CCD        | CCU | CBD | CBU | CAD | CAU | PRD | ZRO |
| R/W        | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| 0h         | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 3-1068. EPWM\_BLANKPULSEMIXSEL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                               |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                  |
| 9     | CDD        | R/W  | 0h    | Enable event time-base counter equal to CMPD when the timer is decrementing to the blanking window trigger [BLANKPULSEMIX].<br>0: CMPD down-count match enable event is not enabled<br>1: Enable CMPD down-count match enable event       |
| 8     | CDU        | R/W  | 0h    | Enable event time-base counter equal to CMPD when the timer is incrementing to the blanking window trigger [BLANKPULSEMIX].<br>0: CMPD up-count match enable event is not enabled<br>1: Enable CMPD up-count match enable event           |
| 7     | CCD        | R/W  | 0h    | Enable event time-base counter equal to CMPC when the timer is decrementing to the blanking window trigger [BLANKPULSEMIX].<br>0: CMPC down-count match enable event is not enabled<br>1: Enable CMPC down-count match enable event       |
| 6     | CCU        | R/W  | 0h    | Enable event time-base counter equal to CMPC when the timer is incrementing to the blanking window trigger [BLANKPULSEMIX].<br>0: CMPC up-count match enable event is not enabled<br>1: Enable CMPC up-count match enable event           |
| 5     | CBD        | R/W  | 0h    | Enable event time-base counter equal to CMPB when the timer is decrementing to the blanking window trigger [BLANKPULSEMIX].<br>0: CMPB down-count match enable event is not enabled<br>1: Enable CMPB down-count match enable event       |
| 4     | CBU        | R/W  | 0h    | Enable event time-base counter equal to CMPB when the timer is incrementing to the mixed ET interrupt trigger signal [BLANKPULSEMIX].<br>0: CMPB up-count match enable event is not enabled<br>1: Enable CMPB up-count match enable event |
| 3     | CAD        | R/W  | 0h    | Enable event time-base counter equal to CMPA when the timer is decrementing to the blanking window trigger [BLANKPULSEMIX].<br>0: CMPA down-count match enable event is not enabled<br>1: Enable CMPA down-count match enable event       |
| 2     | CAU        | R/W  | 0h    | Enable event time-base counter equal to CMPA when the timer is incrementing to the blanking window trigger [BLANKPULSEMIX].<br>0: CMPA up-count match enable event is not enabled<br>1: Enable CMPA up-count match enable event           |
| 1     | PRD        | R/W  | 0h    | Enable event time-base counter equal to period [TBCTR = TBPRD] to the blanking window trigger [BLANKPULSEMIX].<br>0: Period match event is not enabled<br>1: Enable period match event                                                    |
| 0     | ZRO        | R/W  | 0h    | Enable event time-base counter equal to zero [TBCTR = 0x00] to the blanking window trigger [BLANKPULSEMIX].<br>0: Zero match event is not enabled<br>1: Enable zero match event                                                           |

### 3.7.2.86 EPWM\_DCCAPMIXSEL Register

#### 1 EPWM\_DCCAPMIXSEL Register (Offset = 19Ch) [reset = 0h]

Capture Event pulse select register.

Return to [Summary Table](#)

**Table 3-1069. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 019Ch       |
| EPWM0_G1      | 5004 019Ch       |
| EPWM0_G2      | 5008 019Ch       |
| EPWM0_G3      | 500C 019Ch       |
| EPWM1_G0      | 5000 119Ch       |
| EPWM1_G1      | 5004 119Ch       |
| EPWM1_G2      | 5008 119Ch       |
| EPWM1_G3      | 500C 119Ch       |
| EPWM2_G0      | 5000 219Ch       |
| EPWM2_G1      | 5004 219Ch       |
| EPWM2_G2      | 5008 219Ch       |
| EPWM2_G3      | 500C 219Ch       |
| EPWM3_G0      | 5000 319Ch       |
| EPWM3_G1      | 5004 319Ch       |
| EPWM3_G2      | 5008 319Ch       |
| EPWM3_G3      | 500C 319Ch       |
| EPWM4_G0      | 5000 419Ch       |
| EPWM4_G1      | 5004 419Ch       |
| EPWM4_G2      | 5008 419Ch       |
| EPWM4_G3      | 500C 419Ch       |
| EPWM5_G0      | 5000 519Ch       |
| EPWM5_G1      | 5004 519Ch       |
| EPWM5_G2      | 5008 519Ch       |
| EPWM5_G3      | 500C 519Ch       |
| EPWM6_G0      | 5000 619Ch       |
| EPWM6_G1      | 5004 619Ch       |
| EPWM6_G2      | 5008 619Ch       |
| EPWM6_G3      | 500C 619Ch       |
| EPWM7_G0      | 5000 719Ch       |
| EPWM7_G1      | 5004 719Ch       |
| EPWM7_G2      | 5008 719Ch       |
| EPWM7_G3      | 500C 719Ch       |
| EPWM8_G0      | 5000 819Ch       |
| EPWM8_G1      | 5004 819Ch       |
| EPWM8_G2      | 5008 819Ch       |
| EPWM8_G3      | 500C 819Ch       |
| EPWM9_G0      | 5000 919Ch       |
| EPWM9_G1      | 5004 919Ch       |
| EPWM9_G2      | 5008 919Ch       |

**Table 3-1069. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 919Ch       |
| EPWM10_G0     | 5000 A19Ch       |
| EPWM10_G1     | 5004 A19Ch       |
| EPWM10_G2     | 5008 A19Ch       |
| EPWM10_G3     | 500C A19Ch       |
| EPWM11_G0     | 5000 B19Ch       |
| EPWM11_G1     | 5004 B19Ch       |
| EPWM11_G2     | 5008 B19Ch       |
| EPWM11_G3     | 500C B19Ch       |
| EPWM12_G0     | 5000 C19Ch       |
| EPWM12_G1     | 5004 C19Ch       |
| EPWM12_G2     | 5008 C19Ch       |
| EPWM12_G3     | 500C C19Ch       |
| EPWM13_G0     | 5000 D19Ch       |
| EPWM13_G1     | 5004 D19Ch       |
| EPWM13_G2     | 5008 D19Ch       |
| EPWM13_G3     | 500C D19Ch       |
| EPWM14_G0     | 5000 E19Ch       |
| EPWM14_G1     | 5004 E19Ch       |
| EPWM14_G2     | 5008 E19Ch       |
| EPWM14_G3     | 500C E19Ch       |
| EPWM15_G0     | 5000 F19Ch       |
| EPWM15_G1     | 5004 F19Ch       |
| EPWM15_G2     | 5008 F19Ch       |
| EPWM15_G3     | 500C F19Ch       |
| EPWM16_G0     | 5001 019Ch       |
| EPWM16_G1     | 5005 019Ch       |
| EPWM16_G2     | 5009 019Ch       |
| EPWM16_G3     | 500D 019Ch       |
| EPWM17_G0     | 5001 119Ch       |
| EPWM17_G1     | 5005 119Ch       |
| EPWM17_G2     | 5009 119Ch       |
| EPWM17_G3     | 500D 119Ch       |
| EPWM18_G0     | 5001 219Ch       |
| EPWM18_G1     | 5005 219Ch       |
| EPWM18_G2     | 5009 219Ch       |
| EPWM18_G3     | 500D 219Ch       |
| EPWM19_G0     | 5001 319Ch       |
| EPWM19_G1     | 5005 319Ch       |
| EPWM19_G2     | 5009 319Ch       |
| EPWM19_G3     | 500D 319Ch       |
| EPWM20_G0     | 5001 419Ch       |
| EPWM20_G1     | 5005 419Ch       |
| EPWM20_G2     | 5009 419Ch       |
| EPWM20_G3     | 500D 419Ch       |



**Table 3-1069. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 519Ch       |
| EPWM21_G1     | 5005 519Ch       |
| EPWM21_G2     | 5009 519Ch       |
| EPWM21_G3     | 500D 519Ch       |
| EPWM22_G0     | 5001 619Ch       |
| EPWM22_G1     | 5005 619Ch       |
| EPWM22_G2     | 5009 619Ch       |
| EPWM22_G3     | 500D 619Ch       |
| EPWM23_G0     | 5001 719Ch       |
| EPWM23_G1     | 5005 719Ch       |
| EPWM23_G2     | 5009 719Ch       |
| EPWM23_G3     | 500D 719Ch       |
| EPWM24_G0     | 5001 819Ch       |
| EPWM24_G1     | 5005 819Ch       |
| EPWM24_G2     | 5009 819Ch       |
| EPWM24_G3     | 500D 819Ch       |
| EPWM25_G0     | 5001 919Ch       |
| EPWM25_G1     | 5005 919Ch       |
| EPWM25_G2     | 5009 919Ch       |
| EPWM25_G3     | 500D 919Ch       |
| EPWM26_G0     | 5001 A19Ch       |
| EPWM26_G1     | 5005 A19Ch       |
| EPWM26_G2     | 5009 A19Ch       |
| EPWM26_G3     | 500D A19Ch       |
| EPWM27_G0     | 5001 B19Ch       |
| EPWM27_G1     | 5005 B19Ch       |
| EPWM27_G2     | 5009 B19Ch       |
| EPWM27_G3     | 500D B19Ch       |
| EPWM28_G0     | 5001 C19Ch       |
| EPWM28_G1     | 5005 C19Ch       |
| EPWM28_G2     | 5009 C19Ch       |
| EPWM28_G3     | 500D C19Ch       |
| EPWM29_G0     | 5001 D19Ch       |
| EPWM29_G1     | 5005 D19Ch       |
| EPWM29_G2     | 5009 D19Ch       |
| EPWM29_G3     | 500D D19Ch       |
| EPWM30_G0     | 5001 E19Ch       |
| EPWM30_G1     | 5005 E19Ch       |
| EPWM30_G2     | 5009 E19Ch       |
| EPWM30_G3     | 500D E19Ch       |
| EPWM31_G0     | 5001 F19Ch       |
| EPWM31_G1     | 5005 F19Ch       |
| EPWM31_G2     | 5009 F19Ch       |
| EPWM31_G3     | 500D F19Ch       |

**Figure 3-337. EPWM\_DCCAPMIXSEL Name Register**

| 15         | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
|------------|-----|-----|-----|-----|-----|-----|-----|
| RESERVED_1 |     |     |     |     |     | CDD | CDU |
| R          |     |     |     |     |     | R/W | R/W |
| 0h         |     |     |     |     |     | 0h  | 0h  |
| 7          | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| CCD        | CCU | CBD | CBU | CAD | CAU | PRD | ZRO |
| R/W        | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| 0h         | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 3-1071. EPWM\_DCCAPMIXSEL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                          |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                             |
| 9     | CDD        | R/W  | 0h    | Enable event time-base counter equal to CMPD when the timer is decrementing to the blanking window trigger [DCC0PMIX].<br>0: CMPD down-count match enable event is not enabled<br>1: Enable CMPD down-count match enable event       |
| 8     | CDU        | R/W  | 0h    | Enable event time-base counter equal to CMPD when the timer is incrementing to the blanking window trigger [DCC0PMIX].<br>0: CMPD up-count match enable event is not enabled<br>1: Enable CMPD up-count match enable event           |
| 7     | CCD        | R/W  | 0h    | Enable event time-base counter equal to CMPC when the timer is decrementing to the blanking window trigger [DCC0PMIX].<br>0: CMPC down-count match enable event is not enabled<br>1: Enable CMPC down-count match enable event       |
| 6     | CCU        | R/W  | 0h    | Enable event time-base counter equal to CMPC when the timer is incrementing to the blanking window trigger [DCC0PMIX].<br>0: CMPC up-count match enable event is not enabled<br>1: Enable CMPC up-count match enable event           |
| 5     | CBD        | R/W  | 0h    | Enable event time-base counter equal to CMPB when the timer is decrementing to the blanking window trigger [DCC0PMIX].<br>0: CMPB down-count match enable event is not enabled<br>1: Enable CMPB down-count match enable event       |
| 4     | CBU        | R/W  | 0h    | Enable event time-base counter equal to CMPB when the timer is incrementing to the mixed ET interrupt trigger signal [DCC0PMIX].<br>0: CMPB up-count match enable event is not enabled<br>1: Enable CMPB up-count match enable event |
| 3     | CAD        | R/W  | 0h    | Enable event time-base counter equal to CMPA when the timer is decrementing to the blanking window trigger [DCC0PMIX].<br>0: CMPA down-count match enable event is not enabled<br>1: Enable CMPA down-count match enable event       |
| 2     | CAU        | R/W  | 0h    | Enable event time-base counter equal to CMPA when the timer is incrementing to the blanking window trigger [DCC0PMIX].<br>0: CMPA up-count match enable event is not enabled<br>1: Enable CMPA up-count match enable event           |
| 1     | PRD        | R/W  | 0h    | Enable event time-base counter equal to period [TBCTR = TBPRD] to the blanking window trigger [DCC0PMIX].<br>0: Period match event is not enabled<br>1: Enable period match event                                                    |
| 0     | ZRO        | R/W  | 0h    | Enable event time-base counter equal to zero [TBCTR = 0x00] to the blanking window trigger [DCC0PMIX].<br>0: Zero match event is not enabled<br>1: Enable zero match event                                                           |

### 3.7.2.87 EPWM\_DCCAP Register

#### 1 EPWM\_DCCAP Register (Offset = 19Eh) [reset = 0h]

Digital Compare Counter Capture Register .

Return to [Summary Table](#)

**Table 3-1072. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 019Eh       |
| EPWM0_G1      | 5004 019Eh       |
| EPWM0_G2      | 5008 019Eh       |
| EPWM0_G3      | 500C 019Eh       |
| EPWM1_G0      | 5000 119Eh       |
| EPWM1_G1      | 5004 119Eh       |
| EPWM1_G2      | 5008 119Eh       |
| EPWM1_G3      | 500C 119Eh       |
| EPWM2_G0      | 5000 219Eh       |
| EPWM2_G1      | 5004 219Eh       |
| EPWM2_G2      | 5008 219Eh       |
| EPWM2_G3      | 500C 219Eh       |
| EPWM3_G0      | 5000 319Eh       |
| EPWM3_G1      | 5004 319Eh       |
| EPWM3_G2      | 5008 319Eh       |
| EPWM3_G3      | 500C 319Eh       |
| EPWM4_G0      | 5000 419Eh       |
| EPWM4_G1      | 5004 419Eh       |
| EPWM4_G2      | 5008 419Eh       |
| EPWM4_G3      | 500C 419Eh       |
| EPWM5_G0      | 5000 519Eh       |
| EPWM5_G1      | 5004 519Eh       |
| EPWM5_G2      | 5008 519Eh       |
| EPWM5_G3      | 500C 519Eh       |
| EPWM6_G0      | 5000 619Eh       |
| EPWM6_G1      | 5004 619Eh       |
| EPWM6_G2      | 5008 619Eh       |
| EPWM6_G3      | 500C 619Eh       |
| EPWM7_G0      | 5000 719Eh       |
| EPWM7_G1      | 5004 719Eh       |
| EPWM7_G2      | 5008 719Eh       |
| EPWM7_G3      | 500C 719Eh       |
| EPWM8_G0      | 5000 819Eh       |
| EPWM8_G1      | 5004 819Eh       |
| EPWM8_G2      | 5008 819Eh       |
| EPWM8_G3      | 500C 819Eh       |
| EPWM9_G0      | 5000 919Eh       |
| EPWM9_G1      | 5004 919Eh       |
| EPWM9_G2      | 5008 919Eh       |

**Table 3-1072. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 919Eh       |
| EPWM10_G0     | 5000 A19Eh       |
| EPWM10_G1     | 5004 A19Eh       |
| EPWM10_G2     | 5008 A19Eh       |
| EPWM10_G3     | 500C A19Eh       |
| EPWM11_G0     | 5000 B19Eh       |
| EPWM11_G1     | 5004 B19Eh       |
| EPWM11_G2     | 5008 B19Eh       |
| EPWM11_G3     | 500C B19Eh       |
| EPWM12_G0     | 5000 C19Eh       |
| EPWM12_G1     | 5004 C19Eh       |
| EPWM12_G2     | 5008 C19Eh       |
| EPWM12_G3     | 500C C19Eh       |
| EPWM13_G0     | 5000 D19Eh       |
| EPWM13_G1     | 5004 D19Eh       |
| EPWM13_G2     | 5008 D19Eh       |
| EPWM13_G3     | 500C D19Eh       |
| EPWM14_G0     | 5000 E19Eh       |
| EPWM14_G1     | 5004 E19Eh       |
| EPWM14_G2     | 5008 E19Eh       |
| EPWM14_G3     | 500C E19Eh       |
| EPWM15_G0     | 5000 F19Eh       |
| EPWM15_G1     | 5004 F19Eh       |
| EPWM15_G2     | 5008 F19Eh       |
| EPWM15_G3     | 500C F19Eh       |
| EPWM16_G0     | 5001 019Eh       |
| EPWM16_G1     | 5005 019Eh       |
| EPWM16_G2     | 5009 019Eh       |
| EPWM16_G3     | 500D 019Eh       |
| EPWM17_G0     | 5001 119Eh       |
| EPWM17_G1     | 5005 119Eh       |
| EPWM17_G2     | 5009 119Eh       |
| EPWM17_G3     | 500D 119Eh       |
| EPWM18_G0     | 5001 219Eh       |
| EPWM18_G1     | 5005 219Eh       |
| EPWM18_G2     | 5009 219Eh       |
| EPWM18_G3     | 500D 219Eh       |
| EPWM19_G0     | 5001 319Eh       |
| EPWM19_G1     | 5005 319Eh       |
| EPWM19_G2     | 5009 319Eh       |
| EPWM19_G3     | 500D 319Eh       |
| EPWM20_G0     | 5001 419Eh       |
| EPWM20_G1     | 5005 419Eh       |
| EPWM20_G2     | 5009 419Eh       |
| EPWM20_G3     | 500D 419Eh       |

**Table 3-1072. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 519Eh       |
| EPWM21_G1     | 5005 519Eh       |
| EPWM21_G2     | 5009 519Eh       |
| EPWM21_G3     | 500D 519Eh       |
| EPWM22_G0     | 5001 619Eh       |
| EPWM22_G1     | 5005 619Eh       |
| EPWM22_G2     | 5009 619Eh       |
| EPWM22_G3     | 500D 619Eh       |
| EPWM23_G0     | 5001 719Eh       |
| EPWM23_G1     | 5005 719Eh       |
| EPWM23_G2     | 5009 719Eh       |
| EPWM23_G3     | 500D 719Eh       |
| EPWM24_G0     | 5001 819Eh       |
| EPWM24_G1     | 5005 819Eh       |
| EPWM24_G2     | 5009 819Eh       |
| EPWM24_G3     | 500D 819Eh       |
| EPWM25_G0     | 5001 919Eh       |
| EPWM25_G1     | 5005 919Eh       |
| EPWM25_G2     | 5009 919Eh       |
| EPWM25_G3     | 500D 919Eh       |
| EPWM26_G0     | 5001 A19Eh       |
| EPWM26_G1     | 5005 A19Eh       |
| EPWM26_G2     | 5009 A19Eh       |
| EPWM26_G3     | 500D A19Eh       |
| EPWM27_G0     | 5001 B19Eh       |
| EPWM27_G1     | 5005 B19Eh       |
| EPWM27_G2     | 5009 B19Eh       |
| EPWM27_G3     | 500D B19Eh       |
| EPWM28_G0     | 5001 C19Eh       |
| EPWM28_G1     | 5005 C19Eh       |
| EPWM28_G2     | 5009 C19Eh       |
| EPWM28_G3     | 500D C19Eh       |
| EPWM29_G0     | 5001 D19Eh       |
| EPWM29_G1     | 5005 D19Eh       |
| EPWM29_G2     | 5009 D19Eh       |
| EPWM29_G3     | 500D D19Eh       |
| EPWM30_G0     | 5001 E19Eh       |
| EPWM30_G1     | 5005 E19Eh       |
| EPWM30_G2     | 5009 E19Eh       |
| EPWM30_G3     | 500D E19Eh       |
| EPWM31_G0     | 5001 F19Eh       |
| EPWM31_G1     | 5005 F19Eh       |
| EPWM31_G2     | 5009 F19Eh       |
| EPWM31_G3     | 500D F19Eh       |

**Figure 3-338. EPWM\_DCCAP Name Register**

|       |    |    |    |    |    |   |   |
|-------|----|----|----|----|----|---|---|
| 15    | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DCCAP |    |    |    |    |    |   |   |
| R     |    |    |    |    |    |   |   |
| 0h    |    |    |    |    |    |   |   |
| 7     | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| DCCAP |    |    |    |    |    |   |   |
| R     |    |    |    |    |    |   |   |
| 0h    |    |    |    |    |    |   |   |

**Table 3-1074. EPWM\_DCCAP Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | DCCAP | R    | 0h    | <p>Digital Compare Time-Base Counter Capture</p> <p>To enable time-base counter capture, set the DCC0PCLT[CAPE] bit to 1. If enabled, reflects the value of the time-base counter [TBCTR] on the low to high edge transition of a filtered [DCEVTFLT] event. Further capture events are ignored until the next period or zero as selected by the DCFCTL[PULSESEL] bit. Shadowing of DCC0P is enabled and disabled by the DCC0PCTL[SHDWMODE] bit. By default this register is shadowed.</p> <ul style="list-style-type: none"> <li>- If DCC0PCTL[SHDWMODE] = 0, then the shadow is enabled. In this mode, the active register is copied to the shadow register on the TBCTR = TBPRD or TBCTR = zero as defined by the DCFCTL[PULSESEL] bit. CPU reads of this register will return the shadow register value.</li> <li>- If DCC0PCTL[SHDWMODE] = 1, then the shadow register is disabled. In this mode, CPU reads will return the active register value. The active and shadow registers share the same memory map address.</li> </ul> |

### 3.7.2.88 EPWM\_DCAHTRIPSEL Register

#### 1 EPWM\_DCAHTRIPSEL Register (Offset = 1A4h) [reset = 0h]

Digital Compare AH Trip Select .

Return to [Summary Table](#)

**Table 3-1075. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 01A4h       |
| EPWM0_G1      | 5004 01A4h       |
| EPWM0_G2      | 5008 01A4h       |
| EPWM0_G3      | 500C 01A4h       |
| EPWM1_G0      | 5000 11A4h       |
| EPWM1_G1      | 5004 11A4h       |
| EPWM1_G2      | 5008 11A4h       |
| EPWM1_G3      | 500C 11A4h       |
| EPWM2_G0      | 5000 21A4h       |
| EPWM2_G1      | 5004 21A4h       |
| EPWM2_G2      | 5008 21A4h       |
| EPWM2_G3      | 500C 21A4h       |
| EPWM3_G0      | 5000 31A4h       |
| EPWM3_G1      | 5004 31A4h       |
| EPWM3_G2      | 5008 31A4h       |
| EPWM3_G3      | 500C 31A4h       |
| EPWM4_G0      | 5000 41A4h       |
| EPWM4_G1      | 5004 41A4h       |
| EPWM4_G2      | 5008 41A4h       |
| EPWM4_G3      | 500C 41A4h       |
| EPWM5_G0      | 5000 51A4h       |
| EPWM5_G1      | 5004 51A4h       |
| EPWM5_G2      | 5008 51A4h       |
| EPWM5_G3      | 500C 51A4h       |
| EPWM6_G0      | 5000 61A4h       |
| EPWM6_G1      | 5004 61A4h       |
| EPWM6_G2      | 5008 61A4h       |
| EPWM6_G3      | 500C 61A4h       |
| EPWM7_G0      | 5000 71A4h       |
| EPWM7_G1      | 5004 71A4h       |
| EPWM7_G2      | 5008 71A4h       |
| EPWM7_G3      | 500C 71A4h       |
| EPWM8_G0      | 5000 81A4h       |
| EPWM8_G1      | 5004 81A4h       |
| EPWM8_G2      | 5008 81A4h       |
| EPWM8_G3      | 500C 81A4h       |
| EPWM9_G0      | 5000 91A4h       |
| EPWM9_G1      | 5004 91A4h       |
| EPWM9_G2      | 5008 91A4h       |

**Table 3-1075. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 91A4h       |
| EPWM10_G0     | 5000 A1A4h       |
| EPWM10_G1     | 5004 A1A4h       |
| EPWM10_G2     | 5008 A1A4h       |
| EPWM10_G3     | 500C A1A4h       |
| EPWM11_G0     | 5000 B1A4h       |
| EPWM11_G1     | 5004 B1A4h       |
| EPWM11_G2     | 5008 B1A4h       |
| EPWM11_G3     | 500C B1A4h       |
| EPWM12_G0     | 5000 C1A4h       |
| EPWM12_G1     | 5004 C1A4h       |
| EPWM12_G2     | 5008 C1A4h       |
| EPWM12_G3     | 500C C1A4h       |
| EPWM13_G0     | 5000 D1A4h       |
| EPWM13_G1     | 5004 D1A4h       |
| EPWM13_G2     | 5008 D1A4h       |
| EPWM13_G3     | 500C D1A4h       |
| EPWM14_G0     | 5000 E1A4h       |
| EPWM14_G1     | 5004 E1A4h       |
| EPWM14_G2     | 5008 E1A4h       |
| EPWM14_G3     | 500C E1A4h       |
| EPWM15_G0     | 5000 F1A4h       |
| EPWM15_G1     | 5004 F1A4h       |
| EPWM15_G2     | 5008 F1A4h       |
| EPWM15_G3     | 500C F1A4h       |
| EPWM16_G0     | 5001 01A4h       |
| EPWM16_G1     | 5005 01A4h       |
| EPWM16_G2     | 5009 01A4h       |
| EPWM16_G3     | 500D 01A4h       |
| EPWM17_G0     | 5001 11A4h       |
| EPWM17_G1     | 5005 11A4h       |
| EPWM17_G2     | 5009 11A4h       |
| EPWM17_G3     | 500D 11A4h       |
| EPWM18_G0     | 5001 21A4h       |
| EPWM18_G1     | 5005 21A4h       |
| EPWM18_G2     | 5009 21A4h       |
| EPWM18_G3     | 500D 21A4h       |
| EPWM19_G0     | 5001 31A4h       |
| EPWM19_G1     | 5005 31A4h       |
| EPWM19_G2     | 5009 31A4h       |
| EPWM19_G3     | 500D 31A4h       |
| EPWM20_G0     | 5001 41A4h       |
| EPWM20_G1     | 5005 41A4h       |
| EPWM20_G2     | 5009 41A4h       |
| EPWM20_G3     | 500D 41A4h       |



**Table 3-1075. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 51A4h       |
| EPWM21_G1     | 5005 51A4h       |
| EPWM21_G2     | 5009 51A4h       |
| EPWM21_G3     | 500D 51A4h       |
| EPWM22_G0     | 5001 61A4h       |
| EPWM22_G1     | 5005 61A4h       |
| EPWM22_G2     | 5009 61A4h       |
| EPWM22_G3     | 500D 61A4h       |
| EPWM23_G0     | 5001 71A4h       |
| EPWM23_G1     | 5005 71A4h       |
| EPWM23_G2     | 5009 71A4h       |
| EPWM23_G3     | 500D 71A4h       |
| EPWM24_G0     | 5001 81A4h       |
| EPWM24_G1     | 5005 81A4h       |
| EPWM24_G2     | 5009 81A4h       |
| EPWM24_G3     | 500D 81A4h       |
| EPWM25_G0     | 5001 91A4h       |
| EPWM25_G1     | 5005 91A4h       |
| EPWM25_G2     | 5009 91A4h       |
| EPWM25_G3     | 500D 91A4h       |
| EPWM26_G0     | 5001 A1A4h       |
| EPWM26_G1     | 5005 A1A4h       |
| EPWM26_G2     | 5009 A1A4h       |
| EPWM26_G3     | 500D A1A4h       |
| EPWM27_G0     | 5001 B1A4h       |
| EPWM27_G1     | 5005 B1A4h       |
| EPWM27_G2     | 5009 B1A4h       |
| EPWM27_G3     | 500D B1A4h       |
| EPWM28_G0     | 5001 C1A4h       |
| EPWM28_G1     | 5005 C1A4h       |
| EPWM28_G2     | 5009 C1A4h       |
| EPWM28_G3     | 500D C1A4h       |
| EPWM29_G0     | 5001 D1A4h       |
| EPWM29_G1     | 5005 D1A4h       |
| EPWM29_G2     | 5009 D1A4h       |
| EPWM29_G3     | 500D D1A4h       |
| EPWM30_G0     | 5001 E1A4h       |
| EPWM30_G1     | 5005 E1A4h       |
| EPWM30_G2     | 5009 E1A4h       |
| EPWM30_G3     | 500D E1A4h       |
| EPWM31_G0     | 5001 F1A4h       |
| EPWM31_G1     | 5005 F1A4h       |
| EPWM31_G2     | 5009 F1A4h       |
| EPWM31_G3     | 500D F1A4h       |

**Figure 3-339. EPWM\_DCAHTRIPSEL Name Register**

| 15         | 14          | 13          | 12          | 11          | 10          | 9           | 8          |
|------------|-------------|-------------|-------------|-------------|-------------|-------------|------------|
| RESERVED_1 | TRIPINPUT15 | TRIPINPUT14 | TRIPINPUT13 | TRIPINPUT12 | TRIPINPUT11 | TRIPINPUT10 | TRIPINPUT9 |
| R          | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W        |
| 0h         | 0h          | 0h          | 0h          | 0h          | 0h          | 0h          | 0h         |
| 7          | 6           | 5           | 4           | 3           | 2           | 1           | 0          |
| TRIPINPUT8 | TRIPINPUT7  | TRIPINPUT6  | TRIPINPUT5  | TRIPINPUT4  | TRIPINPUT3  | TRIPINPUT2  | TRIPINPUT1 |
| R/W        | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W        |
| 0h         | 0h          | 0h          | 0h          | 0h          | 0h          | 0h          | 0h         |

**Table 3-1077. EPWM\_DCAHTRIPSEL Register Field Descriptions**

| Bit | Field       | Type | Reset | Description                                                                                                                                     |
|-----|-------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | RESERVED_1  | R    | 0h    | Reserved                                                                                                                                        |
| 14  | TRIPINPUT15 | R/W  | 0h    | TRIP Input 15<br>0: Trip Input 15 not selected as combinational ORed input<br>1: Trip Input 15 selected as combinational ORed input to DCAH mux |
| 13  | TRIPINPUT14 | R/W  | 0h    | TRIP Input 14<br>0: Trip Input 14 not selected as combinational ORed input<br>1: Trip Input 14 selected as combinational ORed input to DCAH mux |
| 12  | TRIPINPUT13 | R/W  | 0h    | TRIP Input 13<br>0: Trip Input 13 not selected as combinational ORed input<br>1: Trip Input 13 selected as combinational ORed input to DCAH mux |
| 11  | TRIPINPUT12 | R/W  | 0h    | TRIP Input 12<br>0: Trip Input 12 not selected as combinational ORed input<br>1: Trip Input 12 selected as combinational ORed input to DCAH mux |
| 10  | TRIPINPUT11 | R/W  | 0h    | TRIP Input 11<br>0: Trip Input 11 not selected as combinational ORed input<br>1: Trip Input 11 selected as combinational ORed input to DCAH mux |
| 9   | TRIPINPUT10 | R/W  | 0h    | TRIP Input 10<br>0: Trip Input 10 not selected as combinational ORed input<br>1: Trip Input 10 selected as combinational ORed input to DCAH mux |
| 8   | TRIPINPUT9  | R/W  | 0h    | TRIP Input 9<br>0: Trip Input 9 not selected as combinational ORed input<br>1: Trip Input 9 selected as combinational ORed input to DCAH mux    |
| 7   | TRIPINPUT8  | R/W  | 0h    | TRIP Input 8<br>0: Trip Input 8 not selected as combinational ORed input<br>1: Trip Input 8 selected as combinational ORed input to DCAH mux    |
| 6   | TRIPINPUT7  | R/W  | 0h    | TRIP Input 7<br>0: Trip Input 7 not selected as combinational ORed input<br>1: Trip Input 7 selected as combinational ORed input to DCAH mux    |
| 5   | TRIPINPUT6  | R/W  | 0h    | TRIP Input 6<br>0: Trip Input 6 not selected as combinational ORed input<br>1: Trip Input 6 selected as combinational ORed input to DCAH mux    |
| 4   | TRIPINPUT5  | R/W  | 0h    | TRIP Input 5<br>0: Trip Input 5 not selected as combinational ORed input<br>1: Trip Input 5 selected as combinational ORed input to DCAH mux    |
| 3   | TRIPINPUT4  | R/W  | 0h    | TRIP Input 4<br>0: Trip Input 4 not selected as combinational ORed input<br>1: Trip Input 4 selected as combinational ORed input to DCAH mux    |
| 2   | TRIPINPUT3  | R/W  | 0h    | TRIP Input 3<br>0: Trip Input 3 not selected as combinational ORed input<br>1: Trip Input 3 selected as combinational ORed input to DCAH mux    |
| 1   | TRIPINPUT2  | R/W  | 0h    | TRIP Input 2<br>0: Trip Input 2 not selected as combinational ORed input<br>1: Trip Input 2 selected as combinational ORed input to DCAH mux    |

**Table 3-1077. EPWM\_DCAHTRIPSEL Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                  |
|-----|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | TRIPINPUT1 | R/W  | 0h    | TRIP Input 1<br>0: Trip Input 1 not selected as combinational ORed input<br>1: Trip Input 1 selected as combinational ORed input to DCAH mux |

### 3.7.2.89 EPWM\_DCALTRIPSEL Register

#### 1 EPWM\_DCALTRIPSEL Register (Offset = 1A6h) [reset = 0h]

Digital Compare AL Trip Select .

Return to [Summary Table](#)

**Table 3-1078. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 01A6h       |
| EPWM0_G1      | 5004 01A6h       |
| EPWM0_G2      | 5008 01A6h       |
| EPWM0_G3      | 500C 01A6h       |
| EPWM1_G0      | 5000 11A6h       |
| EPWM1_G1      | 5004 11A6h       |
| EPWM1_G2      | 5008 11A6h       |
| EPWM1_G3      | 500C 11A6h       |
| EPWM2_G0      | 5000 21A6h       |
| EPWM2_G1      | 5004 21A6h       |
| EPWM2_G2      | 5008 21A6h       |
| EPWM2_G3      | 500C 21A6h       |
| EPWM3_G0      | 5000 31A6h       |
| EPWM3_G1      | 5004 31A6h       |
| EPWM3_G2      | 5008 31A6h       |
| EPWM3_G3      | 500C 31A6h       |
| EPWM4_G0      | 5000 41A6h       |
| EPWM4_G1      | 5004 41A6h       |
| EPWM4_G2      | 5008 41A6h       |
| EPWM4_G3      | 500C 41A6h       |
| EPWM5_G0      | 5000 51A6h       |
| EPWM5_G1      | 5004 51A6h       |
| EPWM5_G2      | 5008 51A6h       |
| EPWM5_G3      | 500C 51A6h       |
| EPWM6_G0      | 5000 61A6h       |
| EPWM6_G1      | 5004 61A6h       |
| EPWM6_G2      | 5008 61A6h       |
| EPWM6_G3      | 500C 61A6h       |
| EPWM7_G0      | 5000 71A6h       |
| EPWM7_G1      | 5004 71A6h       |
| EPWM7_G2      | 5008 71A6h       |
| EPWM7_G3      | 500C 71A6h       |
| EPWM8_G0      | 5000 81A6h       |
| EPWM8_G1      | 5004 81A6h       |
| EPWM8_G2      | 5008 81A6h       |
| EPWM8_G3      | 500C 81A6h       |
| EPWM9_G0      | 5000 91A6h       |
| EPWM9_G1      | 5004 91A6h       |
| EPWM9_G2      | 5008 91A6h       |

**Table 3-1078. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 91A6h       |
| EPWM10_G0     | 5000 A1A6h       |
| EPWM10_G1     | 5004 A1A6h       |
| EPWM10_G2     | 5008 A1A6h       |
| EPWM10_G3     | 500C A1A6h       |
| EPWM11_G0     | 5000 B1A6h       |
| EPWM11_G1     | 5004 B1A6h       |
| EPWM11_G2     | 5008 B1A6h       |
| EPWM11_G3     | 500C B1A6h       |
| EPWM12_G0     | 5000 C1A6h       |
| EPWM12_G1     | 5004 C1A6h       |
| EPWM12_G2     | 5008 C1A6h       |
| EPWM12_G3     | 500C C1A6h       |
| EPWM13_G0     | 5000 D1A6h       |
| EPWM13_G1     | 5004 D1A6h       |
| EPWM13_G2     | 5008 D1A6h       |
| EPWM13_G3     | 500C D1A6h       |
| EPWM14_G0     | 5000 E1A6h       |
| EPWM14_G1     | 5004 E1A6h       |
| EPWM14_G2     | 5008 E1A6h       |
| EPWM14_G3     | 500C E1A6h       |
| EPWM15_G0     | 5000 F1A6h       |
| EPWM15_G1     | 5004 F1A6h       |
| EPWM15_G2     | 5008 F1A6h       |
| EPWM15_G3     | 500C F1A6h       |
| EPWM16_G0     | 5001 01A6h       |
| EPWM16_G1     | 5005 01A6h       |
| EPWM16_G2     | 5009 01A6h       |
| EPWM16_G3     | 500D 01A6h       |
| EPWM17_G0     | 5001 11A6h       |
| EPWM17_G1     | 5005 11A6h       |
| EPWM17_G2     | 5009 11A6h       |
| EPWM17_G3     | 500D 11A6h       |
| EPWM18_G0     | 5001 21A6h       |
| EPWM18_G1     | 5005 21A6h       |
| EPWM18_G2     | 5009 21A6h       |
| EPWM18_G3     | 500D 21A6h       |
| EPWM19_G0     | 5001 31A6h       |
| EPWM19_G1     | 5005 31A6h       |
| EPWM19_G2     | 5009 31A6h       |
| EPWM19_G3     | 500D 31A6h       |
| EPWM20_G0     | 5001 41A6h       |
| EPWM20_G1     | 5005 41A6h       |
| EPWM20_G2     | 5009 41A6h       |
| EPWM20_G3     | 500D 41A6h       |

**Table 3-1078. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 51A6h       |
| EPWM21_G1     | 5005 51A6h       |
| EPWM21_G2     | 5009 51A6h       |
| EPWM21_G3     | 500D 51A6h       |
| EPWM22_G0     | 5001 61A6h       |
| EPWM22_G1     | 5005 61A6h       |
| EPWM22_G2     | 5009 61A6h       |
| EPWM22_G3     | 500D 61A6h       |
| EPWM23_G0     | 5001 71A6h       |
| EPWM23_G1     | 5005 71A6h       |
| EPWM23_G2     | 5009 71A6h       |
| EPWM23_G3     | 500D 71A6h       |
| EPWM24_G0     | 5001 81A6h       |
| EPWM24_G1     | 5005 81A6h       |
| EPWM24_G2     | 5009 81A6h       |
| EPWM24_G3     | 500D 81A6h       |
| EPWM25_G0     | 5001 91A6h       |
| EPWM25_G1     | 5005 91A6h       |
| EPWM25_G2     | 5009 91A6h       |
| EPWM25_G3     | 500D 91A6h       |
| EPWM26_G0     | 5001 A1A6h       |
| EPWM26_G1     | 5005 A1A6h       |
| EPWM26_G2     | 5009 A1A6h       |
| EPWM26_G3     | 500D A1A6h       |
| EPWM27_G0     | 5001 B1A6h       |
| EPWM27_G1     | 5005 B1A6h       |
| EPWM27_G2     | 5009 B1A6h       |
| EPWM27_G3     | 500D B1A6h       |
| EPWM28_G0     | 5001 C1A6h       |
| EPWM28_G1     | 5005 C1A6h       |
| EPWM28_G2     | 5009 C1A6h       |
| EPWM28_G3     | 500D C1A6h       |
| EPWM29_G0     | 5001 D1A6h       |
| EPWM29_G1     | 5005 D1A6h       |
| EPWM29_G2     | 5009 D1A6h       |
| EPWM29_G3     | 500D D1A6h       |
| EPWM30_G0     | 5001 E1A6h       |
| EPWM30_G1     | 5005 E1A6h       |
| EPWM30_G2     | 5009 E1A6h       |
| EPWM30_G3     | 500D E1A6h       |
| EPWM31_G0     | 5001 F1A6h       |
| EPWM31_G1     | 5005 F1A6h       |
| EPWM31_G2     | 5009 F1A6h       |
| EPWM31_G3     | 500D F1A6h       |

**Figure 3-340. EPWM\_DCALTRIPSEL Name Register**

| 15         | 14          | 13          | 12          | 11          | 10          | 9           | 8          |
|------------|-------------|-------------|-------------|-------------|-------------|-------------|------------|
| RESERVED_1 | TRIPINPUT15 | TRIPINPUT14 | TRIPINPUT13 | TRIPINPUT12 | TRIPINPUT11 | TRIPINPUT10 | TRIPINPUT9 |
| R          | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W        |
| 0h         | 0h          | 0h          | 0h          | 0h          | 0h          | 0h          | 0h         |
| 7          | 6           | 5           | 4           | 3           | 2           | 1           | 0          |
| TRIPINPUT8 | TRIPINPUT7  | TRIPINPUT6  | TRIPINPUT5  | TRIPINPUT4  | TRIPINPUT3  | TRIPINPUT2  | TRIPINPUT1 |
| R/W        | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W        |
| 0h         | 0h          | 0h          | 0h          | 0h          | 0h          | 0h          | 0h         |

**Table 3-1080. EPWM\_DCALTRIPSEL Register Field Descriptions**

| Bit | Field       | Type | Reset | Description                                                                                                                                     |
|-----|-------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | RESERVED_1  | R    | 0h    | Reserved                                                                                                                                        |
| 14  | TRIPINPUT15 | R/W  | 0h    | TRIP Input 15<br>0: Trip Input 15 not selected as combinational ORed input<br>1: Trip Input 15 selected as combinational ORed input to DCAL mux |
| 13  | TRIPINPUT14 | R/W  | 0h    | TRIP Input 14<br>0: Trip Input 14 not selected as combinational ORed input<br>1: Trip Input 14 selected as combinational ORed input to DCAL mux |
| 12  | TRIPINPUT13 | R/W  | 0h    | TRIP Input 13<br>0: Trip Input 13 not selected as combinational ORed input<br>1: Trip Input 13 selected as combinational ORed input to DCAL mux |
| 11  | TRIPINPUT12 | R/W  | 0h    | TRIP Input 12<br>0: Trip Input 12 not selected as combinational ORed input<br>1: Trip Input 12 selected as combinational ORed input to DCAL mux |
| 10  | TRIPINPUT11 | R/W  | 0h    | TRIP Input 11<br>0: Trip Input 11 not selected as combinational ORed input<br>1: Trip Input 11 selected as combinational ORed input to DCAL mux |
| 9   | TRIPINPUT10 | R/W  | 0h    | TRIP Input 10<br>0: Trip Input 10 not selected as combinational ORed input<br>1: Trip Input 10 selected as combinational ORed input to DCAL mux |
| 8   | TRIPINPUT9  | R/W  | 0h    | TRIP Input 9<br>0: Trip Input 9 not selected as combinational ORed input<br>1: Trip Input 9 selected as combinational ORed input to DCAL mux    |
| 7   | TRIPINPUT8  | R/W  | 0h    | TRIP Input 8<br>0: Trip Input 8 not selected as combinational ORed input<br>1: Trip Input 8 selected as combinational ORed input to DCAL mux    |
| 6   | TRIPINPUT7  | R/W  | 0h    | TRIP Input 7<br>0: Trip Input 7 not selected as combinational ORed input<br>1: Trip Input 7 selected as combinational ORed input to DCAL mux    |
| 5   | TRIPINPUT6  | R/W  | 0h    | TRIP Input 6<br>0: Trip Input 6 not selected as combinational ORed input<br>1: Trip Input 6 selected as combinational ORed input to DCAL mux    |
| 4   | TRIPINPUT5  | R/W  | 0h    | TRIP Input 5<br>0: Trip Input 5 not selected as combinational ORed input<br>1: Trip Input 5 selected as combinational ORed input to DCAL mux    |
| 3   | TRIPINPUT4  | R/W  | 0h    | TRIP Input 4<br>0: Trip Input 4 not selected as combinational ORed input<br>1: Trip Input 4 selected as combinational ORed input to DCAL mux    |
| 2   | TRIPINPUT3  | R/W  | 0h    | TRIP Input 3<br>0: Trip Input 3 not selected as combinational ORed input<br>1: Trip Input 3 selected as combinational ORed input to DCAL mux    |
| 1   | TRIPINPUT2  | R/W  | 0h    | TRIP Input 2<br>0: Trip Input 2 not selected as combinational ORed input<br>1: Trip Input 2 selected as combinational ORed input to DCAL mux    |

**Table 3-1080. EPWM\_DCALTRIPSEL Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                  |
|-----|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | TRIPINPUT1 | R/W  | 0h    | TRIP Input 1<br>0: Trip Input 1 not selected as combinational ORed input<br>1: Trip Input 1 selected as combinational ORed input to DCAL mux |



### 3.7.2.90 EPWM\_DCBHTRIPSEL Register

#### 1 EPWM\_DCBHTRIPSEL Register (Offset = 1A8h) [reset = 0h]

Digital Compare BH Trip Select .

Return to [Summary Table](#)

**Table 3-1081. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 01A8h       |
| EPWM0_G1      | 5004 01A8h       |
| EPWM0_G2      | 5008 01A8h       |
| EPWM0_G3      | 500C 01A8h       |
| EPWM1_G0      | 5000 11A8h       |
| EPWM1_G1      | 5004 11A8h       |
| EPWM1_G2      | 5008 11A8h       |
| EPWM1_G3      | 500C 11A8h       |
| EPWM2_G0      | 5000 21A8h       |
| EPWM2_G1      | 5004 21A8h       |
| EPWM2_G2      | 5008 21A8h       |
| EPWM2_G3      | 500C 21A8h       |
| EPWM3_G0      | 5000 31A8h       |
| EPWM3_G1      | 5004 31A8h       |
| EPWM3_G2      | 5008 31A8h       |
| EPWM3_G3      | 500C 31A8h       |
| EPWM4_G0      | 5000 41A8h       |
| EPWM4_G1      | 5004 41A8h       |
| EPWM4_G2      | 5008 41A8h       |
| EPWM4_G3      | 500C 41A8h       |
| EPWM5_G0      | 5000 51A8h       |
| EPWM5_G1      | 5004 51A8h       |
| EPWM5_G2      | 5008 51A8h       |
| EPWM5_G3      | 500C 51A8h       |
| EPWM6_G0      | 5000 61A8h       |
| EPWM6_G1      | 5004 61A8h       |
| EPWM6_G2      | 5008 61A8h       |
| EPWM6_G3      | 500C 61A8h       |
| EPWM7_G0      | 5000 71A8h       |
| EPWM7_G1      | 5004 71A8h       |
| EPWM7_G2      | 5008 71A8h       |
| EPWM7_G3      | 500C 71A8h       |
| EPWM8_G0      | 5000 81A8h       |
| EPWM8_G1      | 5004 81A8h       |
| EPWM8_G2      | 5008 81A8h       |
| EPWM8_G3      | 500C 81A8h       |
| EPWM9_G0      | 5000 91A8h       |
| EPWM9_G1      | 5004 91A8h       |
| EPWM9_G2      | 5008 91A8h       |

**Table 3-1081. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 91A8h       |
| EPWM10_G0     | 5000 A1A8h       |
| EPWM10_G1     | 5004 A1A8h       |
| EPWM10_G2     | 5008 A1A8h       |
| EPWM10_G3     | 500C A1A8h       |
| EPWM11_G0     | 5000 B1A8h       |
| EPWM11_G1     | 5004 B1A8h       |
| EPWM11_G2     | 5008 B1A8h       |
| EPWM11_G3     | 500C B1A8h       |
| EPWM12_G0     | 5000 C1A8h       |
| EPWM12_G1     | 5004 C1A8h       |
| EPWM12_G2     | 5008 C1A8h       |
| EPWM12_G3     | 500C C1A8h       |
| EPWM13_G0     | 5000 D1A8h       |
| EPWM13_G1     | 5004 D1A8h       |
| EPWM13_G2     | 5008 D1A8h       |
| EPWM13_G3     | 500C D1A8h       |
| EPWM14_G0     | 5000 E1A8h       |
| EPWM14_G1     | 5004 E1A8h       |
| EPWM14_G2     | 5008 E1A8h       |
| EPWM14_G3     | 500C E1A8h       |
| EPWM15_G0     | 5000 F1A8h       |
| EPWM15_G1     | 5004 F1A8h       |
| EPWM15_G2     | 5008 F1A8h       |
| EPWM15_G3     | 500C F1A8h       |
| EPWM16_G0     | 5001 01A8h       |
| EPWM16_G1     | 5005 01A8h       |
| EPWM16_G2     | 5009 01A8h       |
| EPWM16_G3     | 500D 01A8h       |
| EPWM17_G0     | 5001 11A8h       |
| EPWM17_G1     | 5005 11A8h       |
| EPWM17_G2     | 5009 11A8h       |
| EPWM17_G3     | 500D 11A8h       |
| EPWM18_G0     | 5001 21A8h       |
| EPWM18_G1     | 5005 21A8h       |
| EPWM18_G2     | 5009 21A8h       |
| EPWM18_G3     | 500D 21A8h       |
| EPWM19_G0     | 5001 31A8h       |
| EPWM19_G1     | 5005 31A8h       |
| EPWM19_G2     | 5009 31A8h       |
| EPWM19_G3     | 500D 31A8h       |
| EPWM20_G0     | 5001 41A8h       |
| EPWM20_G1     | 5005 41A8h       |
| EPWM20_G2     | 5009 41A8h       |
| EPWM20_G3     | 500D 41A8h       |

**Table 3-1081. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 51A8h       |
| EPWM21_G1     | 5005 51A8h       |
| EPWM21_G2     | 5009 51A8h       |
| EPWM21_G3     | 500D 51A8h       |
| EPWM22_G0     | 5001 61A8h       |
| EPWM22_G1     | 5005 61A8h       |
| EPWM22_G2     | 5009 61A8h       |
| EPWM22_G3     | 500D 61A8h       |
| EPWM23_G0     | 5001 71A8h       |
| EPWM23_G1     | 5005 71A8h       |
| EPWM23_G2     | 5009 71A8h       |
| EPWM23_G3     | 500D 71A8h       |
| EPWM24_G0     | 5001 81A8h       |
| EPWM24_G1     | 5005 81A8h       |
| EPWM24_G2     | 5009 81A8h       |
| EPWM24_G3     | 500D 81A8h       |
| EPWM25_G0     | 5001 91A8h       |
| EPWM25_G1     | 5005 91A8h       |
| EPWM25_G2     | 5009 91A8h       |
| EPWM25_G3     | 500D 91A8h       |
| EPWM26_G0     | 5001 A1A8h       |
| EPWM26_G1     | 5005 A1A8h       |
| EPWM26_G2     | 5009 A1A8h       |
| EPWM26_G3     | 500D A1A8h       |
| EPWM27_G0     | 5001 B1A8h       |
| EPWM27_G1     | 5005 B1A8h       |
| EPWM27_G2     | 5009 B1A8h       |
| EPWM27_G3     | 500D B1A8h       |
| EPWM28_G0     | 5001 C1A8h       |
| EPWM28_G1     | 5005 C1A8h       |
| EPWM28_G2     | 5009 C1A8h       |
| EPWM28_G3     | 500D C1A8h       |
| EPWM29_G0     | 5001 D1A8h       |
| EPWM29_G1     | 5005 D1A8h       |
| EPWM29_G2     | 5009 D1A8h       |
| EPWM29_G3     | 500D D1A8h       |
| EPWM30_G0     | 5001 E1A8h       |
| EPWM30_G1     | 5005 E1A8h       |
| EPWM30_G2     | 5009 E1A8h       |
| EPWM30_G3     | 500D E1A8h       |
| EPWM31_G0     | 5001 F1A8h       |
| EPWM31_G1     | 5005 F1A8h       |
| EPWM31_G2     | 5009 F1A8h       |
| EPWM31_G3     | 500D F1A8h       |

**Figure 3-341. EPWM\_DCBHTRIPSEL Name Register**

| 15         | 14          | 13          | 12          | 11          | 10          | 9           | 8          |
|------------|-------------|-------------|-------------|-------------|-------------|-------------|------------|
| RESERVED_1 | TRIPINPUT15 | TRIPINPUT14 | TRIPINPUT13 | TRIPINPUT12 | TRIPINPUT11 | TRIPINPUT10 | TRIPINPUT9 |
| R          | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W        |
| 0h         | 0h          | 0h          | 0h          | 0h          | 0h          | 0h          | 0h         |
| 7          | 6           | 5           | 4           | 3           | 2           | 1           | 0          |
| TRIPINPUT8 | TRIPINPUT7  | TRIPINPUT6  | TRIPINPUT5  | TRIPINPUT4  | TRIPINPUT3  | TRIPINPUT2  | TRIPINPUT1 |
| R/W        | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W        |
| 0h         | 0h          | 0h          | 0h          | 0h          | 0h          | 0h          | 0h         |

**Table 3-1083. EPWM\_DCBHTRIPSEL Register Field Descriptions**

| Bit | Field       | Type | Reset | Description                                                                                                                                     |
|-----|-------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | RESERVED_1  | R    | 0h    | Reserved                                                                                                                                        |
| 14  | TRIPINPUT15 | R/W  | 0h    | TRIP Input 15<br>0: Trip Input 15 not selected as combinational ORed input<br>1: Trip Input 15 selected as combinational ORed input to DCBH mux |
| 13  | TRIPINPUT14 | R/W  | 0h    | TRIP Input 14<br>0: Trip Input 14 not selected as combinational ORed input<br>1: Trip Input 14 selected as combinational ORed input to DCBH mux |
| 12  | TRIPINPUT13 | R/W  | 0h    | TRIP Input 13<br>0: Trip Input 13 not selected as combinational ORed input<br>1: Trip Input 13 selected as combinational ORed input to DCBH mux |
| 11  | TRIPINPUT12 | R/W  | 0h    | TRIP Input 12<br>0: Trip Input 12 not selected as combinational ORed input<br>1: Trip Input 12 selected as combinational ORed input to DCBH mux |
| 10  | TRIPINPUT11 | R/W  | 0h    | TRIP Input 11<br>0: Trip Input 11 not selected as combinational ORed input<br>1: Trip Input 11 selected as combinational ORed input to DCBH mux |
| 9   | TRIPINPUT10 | R/W  | 0h    | TRIP Input 10<br>0: Trip Input 10 not selected as combinational ORed input<br>1: Trip Input 10 selected as combinational ORed input to DCBH mux |
| 8   | TRIPINPUT9  | R/W  | 0h    | TRIP Input 9<br>0: Trip Input 9 not selected as combinational ORed input<br>1: Trip Input 9 selected as combinational ORed input to DCBH mux    |
| 7   | TRIPINPUT8  | R/W  | 0h    | TRIP Input 8<br>0: Trip Input 8 not selected as combinational ORed input<br>1: Trip Input 8 selected as combinational ORed input to DCBH mux    |
| 6   | TRIPINPUT7  | R/W  | 0h    | TRIP Input 7<br>0: Trip Input 7 not selected as combinational ORed input<br>1: Trip Input 7 selected as combinational ORed input to DCBH mux    |
| 5   | TRIPINPUT6  | R/W  | 0h    | TRIP Input 6<br>0: Trip Input 6 not selected as combinational ORed input<br>1: Trip Input 6 selected as combinational ORed input to DCBH mux    |
| 4   | TRIPINPUT5  | R/W  | 0h    | TRIP Input 5<br>0: Trip Input 5 not selected as combinational ORed input<br>1: Trip Input 5 selected as combinational ORed input to DCBH mux    |
| 3   | TRIPINPUT4  | R/W  | 0h    | TRIP Input 4<br>0: Trip Input 4 not selected as combinational ORed input<br>1: Trip Input 4 selected as combinational ORed input to DCBH mux    |
| 2   | TRIPINPUT3  | R/W  | 0h    | TRIP Input 3<br>0: Trip Input 3 not selected as combinational ORed input<br>1: Trip Input 3 selected as combinational ORed input to DCBH mux    |
| 1   | TRIPINPUT2  | R/W  | 0h    | TRIP Input 2<br>0: Trip Input 2 not selected as combinational ORed input<br>1: Trip Input 2 selected as combinational ORed input to DCBH mux    |

**Table 3-1083. EPWM\_DCBHTRIPSEL Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                  |
|-----|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | TRIPINPUT1 | R/W  | 0h    | TRIP Input 1<br>0: Trip Input 1 not selected as combinational ORed input<br>1: Trip Input 1 selected as combinational ORed input to DCBH mux |

### 3.7.2.91 EPWM\_DCBLTRIPSEL Register

#### 1 EPWM\_DCBLTRIPSEL Register (Offset = 1AAh) [reset = 0h]

Digital Compare BL Trip Select .

Return to [Summary Table](#)

**Table 3-1084. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 01AAh       |
| EPWM0_G1      | 5004 01AAh       |
| EPWM0_G2      | 5008 01AAh       |
| EPWM0_G3      | 500C 01AAh       |
| EPWM1_G0      | 5000 11AAh       |
| EPWM1_G1      | 5004 11AAh       |
| EPWM1_G2      | 5008 11AAh       |
| EPWM1_G3      | 500C 11AAh       |
| EPWM2_G0      | 5000 21AAh       |
| EPWM2_G1      | 5004 21AAh       |
| EPWM2_G2      | 5008 21AAh       |
| EPWM2_G3      | 500C 21AAh       |
| EPWM3_G0      | 5000 31AAh       |
| EPWM3_G1      | 5004 31AAh       |
| EPWM3_G2      | 5008 31AAh       |
| EPWM3_G3      | 500C 31AAh       |
| EPWM4_G0      | 5000 41AAh       |
| EPWM4_G1      | 5004 41AAh       |
| EPWM4_G2      | 5008 41AAh       |
| EPWM4_G3      | 500C 41AAh       |
| EPWM5_G0      | 5000 51AAh       |
| EPWM5_G1      | 5004 51AAh       |
| EPWM5_G2      | 5008 51AAh       |
| EPWM5_G3      | 500C 51AAh       |
| EPWM6_G0      | 5000 61AAh       |
| EPWM6_G1      | 5004 61AAh       |
| EPWM6_G2      | 5008 61AAh       |
| EPWM6_G3      | 500C 61AAh       |
| EPWM7_G0      | 5000 71AAh       |
| EPWM7_G1      | 5004 71AAh       |
| EPWM7_G2      | 5008 71AAh       |
| EPWM7_G3      | 500C 71AAh       |
| EPWM8_G0      | 5000 81AAh       |
| EPWM8_G1      | 5004 81AAh       |
| EPWM8_G2      | 5008 81AAh       |
| EPWM8_G3      | 500C 81AAh       |
| EPWM9_G0      | 5000 91AAh       |
| EPWM9_G1      | 5004 91AAh       |
| EPWM9_G2      | 5008 91AAh       |

**Table 3-1084. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 91AAh       |
| EPWM10_G0     | 5000 A1AAh       |
| EPWM10_G1     | 5004 A1AAh       |
| EPWM10_G2     | 5008 A1AAh       |
| EPWM10_G3     | 500C A1AAh       |
| EPWM11_G0     | 5000 B1AAh       |
| EPWM11_G1     | 5004 B1AAh       |
| EPWM11_G2     | 5008 B1AAh       |
| EPWM11_G3     | 500C B1AAh       |
| EPWM12_G0     | 5000 C1AAh       |
| EPWM12_G1     | 5004 C1AAh       |
| EPWM12_G2     | 5008 C1AAh       |
| EPWM12_G3     | 500C C1AAh       |
| EPWM13_G0     | 5000 D1AAh       |
| EPWM13_G1     | 5004 D1AAh       |
| EPWM13_G2     | 5008 D1AAh       |
| EPWM13_G3     | 500C D1AAh       |
| EPWM14_G0     | 5000 E1AAh       |
| EPWM14_G1     | 5004 E1AAh       |
| EPWM14_G2     | 5008 E1AAh       |
| EPWM14_G3     | 500C E1AAh       |
| EPWM15_G0     | 5000 F1AAh       |
| EPWM15_G1     | 5004 F1AAh       |
| EPWM15_G2     | 5008 F1AAh       |
| EPWM15_G3     | 500C F1AAh       |
| EPWM16_G0     | 5001 01AAh       |
| EPWM16_G1     | 5005 01AAh       |
| EPWM16_G2     | 5009 01AAh       |
| EPWM16_G3     | 500D 01AAh       |
| EPWM17_G0     | 5001 11AAh       |
| EPWM17_G1     | 5005 11AAh       |
| EPWM17_G2     | 5009 11AAh       |
| EPWM17_G3     | 500D 11AAh       |
| EPWM18_G0     | 5001 21AAh       |
| EPWM18_G1     | 5005 21AAh       |
| EPWM18_G2     | 5009 21AAh       |
| EPWM18_G3     | 500D 21AAh       |
| EPWM19_G0     | 5001 31AAh       |
| EPWM19_G1     | 5005 31AAh       |
| EPWM19_G2     | 5009 31AAh       |
| EPWM19_G3     | 500D 31AAh       |
| EPWM20_G0     | 5001 41AAh       |
| EPWM20_G1     | 5005 41AAh       |
| EPWM20_G2     | 5009 41AAh       |
| EPWM20_G3     | 500D 41AAh       |

**Table 3-1084. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 51AAh       |
| EPWM21_G1     | 5005 51AAh       |
| EPWM21_G2     | 5009 51AAh       |
| EPWM21_G3     | 500D 51AAh       |
| EPWM22_G0     | 5001 61AAh       |
| EPWM22_G1     | 5005 61AAh       |
| EPWM22_G2     | 5009 61AAh       |
| EPWM22_G3     | 500D 61AAh       |
| EPWM23_G0     | 5001 71AAh       |
| EPWM23_G1     | 5005 71AAh       |
| EPWM23_G2     | 5009 71AAh       |
| EPWM23_G3     | 500D 71AAh       |
| EPWM24_G0     | 5001 81AAh       |
| EPWM24_G1     | 5005 81AAh       |
| EPWM24_G2     | 5009 81AAh       |
| EPWM24_G3     | 500D 81AAh       |
| EPWM25_G0     | 5001 91AAh       |
| EPWM25_G1     | 5005 91AAh       |
| EPWM25_G2     | 5009 91AAh       |
| EPWM25_G3     | 500D 91AAh       |
| EPWM26_G0     | 5001 A1AAh       |
| EPWM26_G1     | 5005 A1AAh       |
| EPWM26_G2     | 5009 A1AAh       |
| EPWM26_G3     | 500D A1AAh       |
| EPWM27_G0     | 5001 B1AAh       |
| EPWM27_G1     | 5005 B1AAh       |
| EPWM27_G2     | 5009 B1AAh       |
| EPWM27_G3     | 500D B1AAh       |
| EPWM28_G0     | 5001 C1AAh       |
| EPWM28_G1     | 5005 C1AAh       |
| EPWM28_G2     | 5009 C1AAh       |
| EPWM28_G3     | 500D C1AAh       |
| EPWM29_G0     | 5001 D1AAh       |
| EPWM29_G1     | 5005 D1AAh       |
| EPWM29_G2     | 5009 D1AAh       |
| EPWM29_G3     | 500D D1AAh       |
| EPWM30_G0     | 5001 E1AAh       |
| EPWM30_G1     | 5005 E1AAh       |
| EPWM30_G2     | 5009 E1AAh       |
| EPWM30_G3     | 500D E1AAh       |
| EPWM31_G0     | 5001 F1AAh       |
| EPWM31_G1     | 5005 F1AAh       |
| EPWM31_G2     | 5009 F1AAh       |
| EPWM31_G3     | 500D F1AAh       |



**Figure 3-342. EPWM\_DCBLTRIPSEL Name Register**

| 15         | 14          | 13          | 12          | 11          | 10          | 9           | 8          |
|------------|-------------|-------------|-------------|-------------|-------------|-------------|------------|
| RESERVED_1 | TRIPINPUT15 | TRIPINPUT14 | TRIPINPUT13 | TRIPINPUT12 | TRIPINPUT11 | TRIPINPUT10 | TRIPINPUT9 |
| R          | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W        |
| 0h         | 0h          | 0h          | 0h          | 0h          | 0h          | 0h          | 0h         |
| 7          | 6           | 5           | 4           | 3           | 2           | 1           | 0          |
| TRIPINPUT8 | TRIPINPUT7  | TRIPINPUT6  | TRIPINPUT5  | TRIPINPUT4  | TRIPINPUT3  | TRIPINPUT2  | TRIPINPUT1 |
| R/W        | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W        |
| 0h         | 0h          | 0h          | 0h          | 0h          | 0h          | 0h          | 0h         |

**Table 3-1086. EPWM\_DCBLTRIPSEL Register Field Descriptions**

| Bit | Field       | Type | Reset | Description                                                                                                                                     |
|-----|-------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | RESERVED_1  | R    | 0h    | Reserved                                                                                                                                        |
| 14  | TRIPINPUT15 | R/W  | 0h    | TRIP Input 15<br>0: Trip Input 15 not selected as combinational ORed input<br>1: Trip Input 15 selected as combinational ORed input to DCAL mux |
| 13  | TRIPINPUT14 | R/W  | 0h    | TRIP Input 14<br>0: Trip Input 14 not selected as combinational ORed input<br>1: Trip Input 14 selected as combinational ORed input to DCAL mux |
| 12  | TRIPINPUT13 | R/W  | 0h    | TRIP Input 13<br>0: Trip Input 13 not selected as combinational ORed input<br>1: Trip Input 13 selected as combinational ORed input to DCAL mux |
| 11  | TRIPINPUT12 | R/W  | 0h    | TRIP Input 12<br>0: Trip Input 12 not selected as combinational ORed input<br>1: Trip Input 12 selected as combinational ORed input to DCAL mux |
| 10  | TRIPINPUT11 | R/W  | 0h    | TRIP Input 11<br>0: Trip Input 11 not selected as combinational ORed input<br>1: Trip Input 11 selected as combinational ORed input to DCAL mux |
| 9   | TRIPINPUT10 | R/W  | 0h    | TRIP Input 10<br>0: Trip Input 10 not selected as combinational ORed input<br>1: Trip Input 10 selected as combinational ORed input to DCAL mux |
| 8   | TRIPINPUT9  | R/W  | 0h    | TRIP Input 9<br>0: Trip Input 9 not selected as combinational ORed input<br>1: Trip Input 9 selected as combinational ORed input to DCAL mux    |
| 7   | TRIPINPUT8  | R/W  | 0h    | TRIP Input 8<br>0: Trip Input 8 not selected as combinational ORed input<br>1: Trip Input 8 selected as combinational ORed input to DCAL mux    |
| 6   | TRIPINPUT7  | R/W  | 0h    | TRIP Input 7<br>0: Trip Input 7 not selected as combinational ORed input<br>1: Trip Input 7 selected as combinational ORed input to DCAL mux    |
| 5   | TRIPINPUT6  | R/W  | 0h    | TRIP Input 6<br>0: Trip Input 6 not selected as combinational ORed input<br>1: Trip Input 6 selected as combinational ORed input to DCAL mux    |
| 4   | TRIPINPUT5  | R/W  | 0h    | TRIP Input 5<br>0: Trip Input 5 not selected as combinational ORed input<br>1: Trip Input 5 selected as combinational ORed input to DCAL mux    |
| 3   | TRIPINPUT4  | R/W  | 0h    | TRIP Input 4<br>0: Trip Input 4 not selected as combinational ORed input<br>1: Trip Input 4 selected as combinational ORed input to DCAL mux    |
| 2   | TRIPINPUT3  | R/W  | 0h    | TRIP Input 3<br>0: Trip Input 3 not selected as combinational ORed input<br>1: Trip Input 3 selected as combinational ORed input to DCAL mux    |
| 1   | TRIPINPUT2  | R/W  | 0h    | TRIP Input 2<br>0: Trip Input 2 not selected as combinational ORed input<br>1: Trip Input 2 selected as combinational ORed input to DCAL mux    |

**Table 3-1086. EPWM\_DCBLTRIPSEL Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                  |
|-----|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | TRIPINPUT1 | R/W  | 0h    | TRIP Input 1<br>0: Trip Input 1 not selected as combinational ORed input<br>1: Trip Input 1 selected as combinational ORed input to DCAL mux |

### 3.7.2.92 EPWM\_CAPCTL Register

#### 1 EPWM\_CAPCTL Register (Offset = 1ACh) [reset = 0h]

Event Capture Control Register.

Return to [Summary Table](#)

**Table 3-1087. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 01ACh       |
| EPWM0_G1      | 5004 01ACh       |
| EPWM0_G2      | 5008 01ACh       |
| EPWM0_G3      | 500C 01ACh       |
| EPWM1_G0      | 5000 11ACh       |
| EPWM1_G1      | 5004 11ACh       |
| EPWM1_G2      | 5008 11ACh       |
| EPWM1_G3      | 500C 11ACh       |
| EPWM2_G0      | 5000 21ACh       |
| EPWM2_G1      | 5004 21ACh       |
| EPWM2_G2      | 5008 21ACh       |
| EPWM2_G3      | 500C 21ACh       |
| EPWM3_G0      | 5000 31ACh       |
| EPWM3_G1      | 5004 31ACh       |
| EPWM3_G2      | 5008 31ACh       |
| EPWM3_G3      | 500C 31ACh       |
| EPWM4_G0      | 5000 41ACh       |
| EPWM4_G1      | 5004 41ACh       |
| EPWM4_G2      | 5008 41ACh       |
| EPWM4_G3      | 500C 41ACh       |
| EPWM5_G0      | 5000 51ACh       |
| EPWM5_G1      | 5004 51ACh       |
| EPWM5_G2      | 5008 51ACh       |
| EPWM5_G3      | 500C 51ACh       |
| EPWM6_G0      | 5000 61ACh       |
| EPWM6_G1      | 5004 61ACh       |
| EPWM6_G2      | 5008 61ACh       |
| EPWM6_G3      | 500C 61ACh       |
| EPWM7_G0      | 5000 71ACh       |
| EPWM7_G1      | 5004 71ACh       |
| EPWM7_G2      | 5008 71ACh       |
| EPWM7_G3      | 500C 71ACh       |
| EPWM8_G0      | 5000 81ACh       |
| EPWM8_G1      | 5004 81ACh       |
| EPWM8_G2      | 5008 81ACh       |
| EPWM8_G3      | 500C 81ACh       |
| EPWM9_G0      | 5000 91ACh       |
| EPWM9_G1      | 5004 91ACh       |
| EPWM9_G2      | 5008 91ACh       |

**Table 3-1087. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 91ACh       |
| EPWM10_G0     | 5000 A1ACh       |
| EPWM10_G1     | 5004 A1ACh       |
| EPWM10_G2     | 5008 A1ACh       |
| EPWM10_G3     | 500C A1ACh       |
| EPWM11_G0     | 5000 B1ACh       |
| EPWM11_G1     | 5004 B1ACh       |
| EPWM11_G2     | 5008 B1ACh       |
| EPWM11_G3     | 500C B1ACh       |
| EPWM12_G0     | 5000 C1ACh       |
| EPWM12_G1     | 5004 C1ACh       |
| EPWM12_G2     | 5008 C1ACh       |
| EPWM12_G3     | 500C C1ACh       |
| EPWM13_G0     | 5000 D1ACh       |
| EPWM13_G1     | 5004 D1ACh       |
| EPWM13_G2     | 5008 D1ACh       |
| EPWM13_G3     | 500C D1ACh       |
| EPWM14_G0     | 5000 E1ACh       |
| EPWM14_G1     | 5004 E1ACh       |
| EPWM14_G2     | 5008 E1ACh       |
| EPWM14_G3     | 500C E1ACh       |
| EPWM15_G0     | 5000 F1ACh       |
| EPWM15_G1     | 5004 F1ACh       |
| EPWM15_G2     | 5008 F1ACh       |
| EPWM15_G3     | 500C F1ACh       |
| EPWM16_G0     | 5001 01ACh       |
| EPWM16_G1     | 5005 01ACh       |
| EPWM16_G2     | 5009 01ACh       |
| EPWM16_G3     | 500D 01ACh       |
| EPWM17_G0     | 5001 11ACh       |
| EPWM17_G1     | 5005 11ACh       |
| EPWM17_G2     | 5009 11ACh       |
| EPWM17_G3     | 500D 11ACh       |
| EPWM18_G0     | 5001 21ACh       |
| EPWM18_G1     | 5005 21ACh       |
| EPWM18_G2     | 5009 21ACh       |
| EPWM18_G3     | 500D 21ACh       |
| EPWM19_G0     | 5001 31ACh       |
| EPWM19_G1     | 5005 31ACh       |
| EPWM19_G2     | 5009 31ACh       |
| EPWM19_G3     | 500D 31ACh       |
| EPWM20_G0     | 5001 41ACh       |
| EPWM20_G1     | 5005 41ACh       |
| EPWM20_G2     | 5009 41ACh       |
| EPWM20_G3     | 500D 41ACh       |

**Table 3-1087. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 51ACh       |
| EPWM21_G1     | 5005 51ACh       |
| EPWM21_G2     | 5009 51ACh       |
| EPWM21_G3     | 500D 51ACh       |
| EPWM22_G0     | 5001 61ACh       |
| EPWM22_G1     | 5005 61ACh       |
| EPWM22_G2     | 5009 61ACh       |
| EPWM22_G3     | 500D 61ACh       |
| EPWM23_G0     | 5001 71ACh       |
| EPWM23_G1     | 5005 71ACh       |
| EPWM23_G2     | 5009 71ACh       |
| EPWM23_G3     | 500D 71ACh       |
| EPWM24_G0     | 5001 81ACh       |
| EPWM24_G1     | 5005 81ACh       |
| EPWM24_G2     | 5009 81ACh       |
| EPWM24_G3     | 500D 81ACh       |
| EPWM25_G0     | 5001 91ACh       |
| EPWM25_G1     | 5005 91ACh       |
| EPWM25_G2     | 5009 91ACh       |
| EPWM25_G3     | 500D 91ACh       |
| EPWM26_G0     | 5001 A1ACh       |
| EPWM26_G1     | 5005 A1ACh       |
| EPWM26_G2     | 5009 A1ACh       |
| EPWM26_G3     | 500D A1ACh       |
| EPWM27_G0     | 5001 B1ACh       |
| EPWM27_G1     | 5005 B1ACh       |
| EPWM27_G2     | 5009 B1ACh       |
| EPWM27_G3     | 500D B1ACh       |
| EPWM28_G0     | 5001 C1ACh       |
| EPWM28_G1     | 5005 C1ACh       |
| EPWM28_G2     | 5009 C1ACh       |
| EPWM28_G3     | 500D C1ACh       |
| EPWM29_G0     | 5001 D1ACh       |
| EPWM29_G1     | 5005 D1ACh       |
| EPWM29_G2     | 5009 D1ACh       |
| EPWM29_G3     | 500D D1ACh       |
| EPWM30_G0     | 5001 E1ACh       |
| EPWM30_G1     | 5005 E1ACh       |
| EPWM30_G2     | 5009 E1ACh       |
| EPWM30_G3     | 500D E1ACh       |
| EPWM31_G0     | 5001 F1ACh       |
| EPWM31_G1     | 5005 F1ACh       |
| EPWM31_G2     | 5009 F1ACh       |
| EPWM31_G3     | 500D F1ACh       |

**Figure 3-343. EPWM\_CAPCTL Name Register**

| 15         | 14 | 13 | 12       | 11       | 10         | 9 | 8       |
|------------|----|----|----------|----------|------------|---|---------|
| RESERVED_2 |    |    |          |          |            |   | FRCLOAD |
| R          |    |    |          |          |            |   | R/W1TS  |
| 0h         |    |    |          |          |            |   | 0h      |
| 7          | 6  | 5  | 4        | 3        | 2          | 1 | 0       |
| RESERVED_1 |    |    | PULSECTL | CAPINPOL | CAPGATEPOL |   | SRCSEL  |
| R          |    |    | R/W      | R/W      | R/W        |   | R/W     |
| 0h         |    |    | 0h       | 0h       | 0h         |   | 0h      |

**Table 3-1089. EPWM\_CAPCTL Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                                                                       |
|------|------------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:9 | RESERVED_2 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                          |
| 8    | FRCLOAD    | R/W1TS | 0h    | 0:Writing of 0 is ignored. Always reads back a 0.<br>1:Forces a LOAD to occur on the DCC0P - an equivalent LOAD.active pulse                                                                                                                                                                                      |
| 7:5  | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                          |
| 4    | PULSECTL   | R/W    | 0h    | Capture Input Polarity Select Mux:<br>0:Pulse selection determined by PULSESEL bits [common pulse selection for Blanking and Capture logic]<br>1:Pulse selection determined by CAPMIXSEL register [independent pulse selection for Blanking and Capture logic]                                                    |
| 3    | CAPINPOL   | R/W    | 0h    | Capture Input Polarity Select Mux:<br>0:CAPIN.sync not inverted<br>1:CAPIN.sync Inverted<br>Default state assumption for these inputs can be active high.<br>If the user is providing active low signal then invert option can be configured                                                                      |
| 2:1  | CAPGATEPOL | R/W    | 0h    | Capture Gate Input Polarity Select Mux:<br>00:Set to 1 - Gate is always ON<br>01:Set to 0 - Gate is always OFF<br>10:CAPGATE.sync<br>11:CAPGATE.sync Inverted<br>Default state assumption for these inputs can be active high.<br>If the user is providing active low signal then invert option can be configured |
| 0    | SRCSEL     | R/W    | 0h    | Capture Logic Input Select Mux:<br>0:DCEVTFILT [Sync] - same as Type-4<br>1:CAPIN.sync                                                                                                                                                                                                                            |

### 3.7.2.93 EPWM\_CAPGATETRIPSEL Register

#### 1 EPWM\_CAPGATETRIPSEL Register (Offset = 1AEh) [reset = 0h]

Event Capture Gate Trip input select.

Return to [Summary Table](#)

**Table 3-1090. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 01AEh       |
| EPWM0_G1      | 5004 01AEh       |
| EPWM0_G2      | 5008 01AEh       |
| EPWM0_G3      | 500C 01AEh       |
| EPWM1_G0      | 5000 11AEh       |
| EPWM1_G1      | 5004 11AEh       |
| EPWM1_G2      | 5008 11AEh       |
| EPWM1_G3      | 500C 11AEh       |
| EPWM2_G0      | 5000 21AEh       |
| EPWM2_G1      | 5004 21AEh       |
| EPWM2_G2      | 5008 21AEh       |
| EPWM2_G3      | 500C 21AEh       |
| EPWM3_G0      | 5000 31AEh       |
| EPWM3_G1      | 5004 31AEh       |
| EPWM3_G2      | 5008 31AEh       |
| EPWM3_G3      | 500C 31AEh       |
| EPWM4_G0      | 5000 41AEh       |
| EPWM4_G1      | 5004 41AEh       |
| EPWM4_G2      | 5008 41AEh       |
| EPWM4_G3      | 500C 41AEh       |
| EPWM5_G0      | 5000 51AEh       |
| EPWM5_G1      | 5004 51AEh       |
| EPWM5_G2      | 5008 51AEh       |
| EPWM5_G3      | 500C 51AEh       |
| EPWM6_G0      | 5000 61AEh       |
| EPWM6_G1      | 5004 61AEh       |
| EPWM6_G2      | 5008 61AEh       |
| EPWM6_G3      | 500C 61AEh       |
| EPWM7_G0      | 5000 71AEh       |
| EPWM7_G1      | 5004 71AEh       |
| EPWM7_G2      | 5008 71AEh       |
| EPWM7_G3      | 500C 71AEh       |
| EPWM8_G0      | 5000 81AEh       |
| EPWM8_G1      | 5004 81AEh       |
| EPWM8_G2      | 5008 81AEh       |
| EPWM8_G3      | 500C 81AEh       |
| EPWM9_G0      | 5000 91AEh       |
| EPWM9_G1      | 5004 91AEh       |
| EPWM9_G2      | 5008 91AEh       |

**Table 3-1090. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 91AEh       |
| EPWM10_G0     | 5000 A1AEh       |
| EPWM10_G1     | 5004 A1AEh       |
| EPWM10_G2     | 5008 A1AEh       |
| EPWM10_G3     | 500C A1AEh       |
| EPWM11_G0     | 5000 B1AEh       |
| EPWM11_G1     | 5004 B1AEh       |
| EPWM11_G2     | 5008 B1AEh       |
| EPWM11_G3     | 500C B1AEh       |
| EPWM12_G0     | 5000 C1AEh       |
| EPWM12_G1     | 5004 C1AEh       |
| EPWM12_G2     | 5008 C1AEh       |
| EPWM12_G3     | 500C C1AEh       |
| EPWM13_G0     | 5000 D1AEh       |
| EPWM13_G1     | 5004 D1AEh       |
| EPWM13_G2     | 5008 D1AEh       |
| EPWM13_G3     | 500C D1AEh       |
| EPWM14_G0     | 5000 E1AEh       |
| EPWM14_G1     | 5004 E1AEh       |
| EPWM14_G2     | 5008 E1AEh       |
| EPWM14_G3     | 500C E1AEh       |
| EPWM15_G0     | 5000 F1AEh       |
| EPWM15_G1     | 5004 F1AEh       |
| EPWM15_G2     | 5008 F1AEh       |
| EPWM15_G3     | 500C F1AEh       |
| EPWM16_G0     | 5001 01AEh       |
| EPWM16_G1     | 5005 01AEh       |
| EPWM16_G2     | 5009 01AEh       |
| EPWM16_G3     | 500D 01AEh       |
| EPWM17_G0     | 5001 11AEh       |
| EPWM17_G1     | 5005 11AEh       |
| EPWM17_G2     | 5009 11AEh       |
| EPWM17_G3     | 500D 11AEh       |
| EPWM18_G0     | 5001 21AEh       |
| EPWM18_G1     | 5005 21AEh       |
| EPWM18_G2     | 5009 21AEh       |
| EPWM18_G3     | 500D 21AEh       |
| EPWM19_G0     | 5001 31AEh       |
| EPWM19_G1     | 5005 31AEh       |
| EPWM19_G2     | 5009 31AEh       |
| EPWM19_G3     | 500D 31AEh       |
| EPWM20_G0     | 5001 41AEh       |
| EPWM20_G1     | 5005 41AEh       |
| EPWM20_G2     | 5009 41AEh       |
| EPWM20_G3     | 500D 41AEh       |



**Table 3-1090. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 51AEh       |
| EPWM21_G1     | 5005 51AEh       |
| EPWM21_G2     | 5009 51AEh       |
| EPWM21_G3     | 500D 51AEh       |
| EPWM22_G0     | 5001 61AEh       |
| EPWM22_G1     | 5005 61AEh       |
| EPWM22_G2     | 5009 61AEh       |
| EPWM22_G3     | 500D 61AEh       |
| EPWM23_G0     | 5001 71AEh       |
| EPWM23_G1     | 5005 71AEh       |
| EPWM23_G2     | 5009 71AEh       |
| EPWM23_G3     | 500D 71AEh       |
| EPWM24_G0     | 5001 81AEh       |
| EPWM24_G1     | 5005 81AEh       |
| EPWM24_G2     | 5009 81AEh       |
| EPWM24_G3     | 500D 81AEh       |
| EPWM25_G0     | 5001 91AEh       |
| EPWM25_G1     | 5005 91AEh       |
| EPWM25_G2     | 5009 91AEh       |
| EPWM25_G3     | 500D 91AEh       |
| EPWM26_G0     | 5001 A1AEh       |
| EPWM26_G1     | 5005 A1AEh       |
| EPWM26_G2     | 5009 A1AEh       |
| EPWM26_G3     | 500D A1AEh       |
| EPWM27_G0     | 5001 B1AEh       |
| EPWM27_G1     | 5005 B1AEh       |
| EPWM27_G2     | 5009 B1AEh       |
| EPWM27_G3     | 500D B1AEh       |
| EPWM28_G0     | 5001 C1AEh       |
| EPWM28_G1     | 5005 C1AEh       |
| EPWM28_G2     | 5009 C1AEh       |
| EPWM28_G3     | 500D C1AEh       |
| EPWM29_G0     | 5001 D1AEh       |
| EPWM29_G1     | 5005 D1AEh       |
| EPWM29_G2     | 5009 D1AEh       |
| EPWM29_G3     | 500D D1AEh       |
| EPWM30_G0     | 5001 E1AEh       |
| EPWM30_G1     | 5005 E1AEh       |
| EPWM30_G2     | 5009 E1AEh       |
| EPWM30_G3     | 500D E1AEh       |
| EPWM31_G0     | 5001 F1AEh       |
| EPWM31_G1     | 5005 F1AEh       |
| EPWM31_G2     | 5009 F1AEh       |
| EPWM31_G3     | 500D F1AEh       |

**Figure 3-344. EPWM\_CAPGATETRIPSEL Name Register**

| 15         | 14          | 13          | 12          | 11          | 10          | 9           | 8          |
|------------|-------------|-------------|-------------|-------------|-------------|-------------|------------|
| RESERVED_1 | TRIPINPUT15 | TRIPINPUT14 | TRIPINPUT13 | TRIPINPUT12 | TRIPINPUT11 | TRIPINPUT10 | TRIPINPUT9 |
| R          | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W        |
| 0h         | 0h          | 0h          | 0h          | 0h          | 0h          | 0h          | 0h         |
| 7          | 6           | 5           | 4           | 3           | 2           | 1           | 0          |
| TRIPINPUT8 | TRIPINPUT7  | TRIPINPUT6  | TRIPINPUT5  | TRIPINPUT4  | TRIPINPUT3  | TRIPINPUT2  | TRIPINPUT1 |
| R/W        | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W        |
| 0h         | 0h          | 0h          | 0h          | 0h          | 0h          | 0h          | 0h         |

**Table 3-1092. EPWM\_CAPGATETRIPSEL Register Field Descriptions**

| Bit | Field       | Type | Reset | Description                                                                                                                                        |
|-----|-------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | RESERVED_1  | R    | 0h    | Reserved                                                                                                                                           |
| 14  | TRIPINPUT15 | R/W  | 0h    | TRIP Input 15<br>0: Trip Input 15 not selected as combinational ORed input<br>1: Trip Input 15 selected as combinational ORed input to CAPGATE mux |
| 13  | TRIPINPUT14 | R/W  | 0h    | TRIP Input 14<br>0: Trip Input 14 not selected as combinational ORed input<br>1: Trip Input 14 selected as combinational ORed input to CAPGATE mux |
| 12  | TRIPINPUT13 | R/W  | 0h    | TRIP Input 13<br>0: Trip Input 13 not selected as combinational ORed input<br>1: Trip Input 13 selected as combinational ORed input to CAPGATE mux |
| 11  | TRIPINPUT12 | R/W  | 0h    | TRIP Input 12<br>0: Trip Input 12 not selected as combinational ORed input<br>1: Trip Input 12 selected as combinational ORed input to CAPGATE mux |
| 10  | TRIPINPUT11 | R/W  | 0h    | TRIP Input 11<br>0: Trip Input 11 not selected as combinational ORed input<br>1: Trip Input 11 selected as combinational ORed input to CAPGATE mux |
| 9   | TRIPINPUT10 | R/W  | 0h    | TRIP Input 10<br>0: Trip Input 10 not selected as combinational ORed input<br>1: Trip Input 10 selected as combinational ORed input to CAPGATE mux |
| 8   | TRIPINPUT9  | R/W  | 0h    | TRIP Input 9<br>0: Trip Input 9 not selected as combinational ORed input<br>1: Trip Input 9 selected as combinational ORed input to CAPGATE mux    |
| 7   | TRIPINPUT8  | R/W  | 0h    | TRIP Input 8<br>0: Trip Input 8 not selected as combinational ORed input<br>1: Trip Input 8 selected as combinational ORed input to CAPGATE mux    |
| 6   | TRIPINPUT7  | R/W  | 0h    | TRIP Input 7<br>0: Trip Input 7 not selected as combinational ORed input<br>1: Trip Input 7 selected as combinational ORed input to CAPGATE mux    |
| 5   | TRIPINPUT6  | R/W  | 0h    | TRIP Input 6<br>0: Trip Input 6 not selected as combinational ORed input<br>1: Trip Input 6 selected as combinational ORed input to CAPGATE mux    |
| 4   | TRIPINPUT5  | R/W  | 0h    | TRIP Input 5<br>0: Trip Input 5 not selected as combinational ORed input<br>1: Trip Input 5 selected as combinational ORed input to CAPGATE mux    |

**Table 3-1092. EPWM\_CAPGATETRIPSEL Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                     |
|-----|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 3   | TRIPINPUT4 | R/W  | 0h    | TRIP Input 4<br>0: Trip Input 4 not selected as combinational ORed input<br>1: Trip Input 4 selected as combinational ORed input to CAPGATE mux |
| 2   | TRIPINPUT3 | R/W  | 0h    | TRIP Input 3<br>0: Trip Input 3 not selected as combinational ORed input<br>1: Trip Input 3 selected as combinational ORed input to CAPGATE mux |
| 1   | TRIPINPUT2 | R/W  | 0h    | TRIP Input 2<br>0: Trip Input 2 not selected as combinational ORed input<br>1: Trip Input 2 selected as combinational ORed input to CAPGATE mux |
| 0   | TRIPINPUT1 | R/W  | 0h    | TRIP Input 1<br>0: Trip Input 1 not selected as combinational ORed input<br>1: Trip Input 1 selected as combinational ORed input to CAPGATE mux |

### 3.7.2.94 EPWM\_CAPINTRIPSEL Register

#### 1 EPWM\_CAPINTRIPSEL Register (Offset = 1B0h) [reset = 0h]

Event Capture Trip input select.

Return to [Summary Table](#)

**Table 3-1093. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 01B0h       |
| EPWM0_G1      | 5004 01B0h       |
| EPWM0_G2      | 5008 01B0h       |
| EPWM0_G3      | 500C 01B0h       |
| EPWM1_G0      | 5000 11B0h       |
| EPWM1_G1      | 5004 11B0h       |
| EPWM1_G2      | 5008 11B0h       |
| EPWM1_G3      | 500C 11B0h       |
| EPWM2_G0      | 5000 21B0h       |
| EPWM2_G1      | 5004 21B0h       |
| EPWM2_G2      | 5008 21B0h       |
| EPWM2_G3      | 500C 21B0h       |
| EPWM3_G0      | 5000 31B0h       |
| EPWM3_G1      | 5004 31B0h       |
| EPWM3_G2      | 5008 31B0h       |
| EPWM3_G3      | 500C 31B0h       |
| EPWM4_G0      | 5000 41B0h       |
| EPWM4_G1      | 5004 41B0h       |
| EPWM4_G2      | 5008 41B0h       |
| EPWM4_G3      | 500C 41B0h       |
| EPWM5_G0      | 5000 51B0h       |
| EPWM5_G1      | 5004 51B0h       |
| EPWM5_G2      | 5008 51B0h       |
| EPWM5_G3      | 500C 51B0h       |
| EPWM6_G0      | 5000 61B0h       |
| EPWM6_G1      | 5004 61B0h       |
| EPWM6_G2      | 5008 61B0h       |
| EPWM6_G3      | 500C 61B0h       |
| EPWM7_G0      | 5000 71B0h       |
| EPWM7_G1      | 5004 71B0h       |
| EPWM7_G2      | 5008 71B0h       |
| EPWM7_G3      | 500C 71B0h       |
| EPWM8_G0      | 5000 81B0h       |
| EPWM8_G1      | 5004 81B0h       |
| EPWM8_G2      | 5008 81B0h       |
| EPWM8_G3      | 500C 81B0h       |
| EPWM9_G0      | 5000 91B0h       |
| EPWM9_G1      | 5004 91B0h       |
| EPWM9_G2      | 5008 91B0h       |

**Table 3-1093. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 91B0h       |
| EPWM10_G0     | 5000 A1B0h       |
| EPWM10_G1     | 5004 A1B0h       |
| EPWM10_G2     | 5008 A1B0h       |
| EPWM10_G3     | 500C A1B0h       |
| EPWM11_G0     | 5000 B1B0h       |
| EPWM11_G1     | 5004 B1B0h       |
| EPWM11_G2     | 5008 B1B0h       |
| EPWM11_G3     | 500C B1B0h       |
| EPWM12_G0     | 5000 C1B0h       |
| EPWM12_G1     | 5004 C1B0h       |
| EPWM12_G2     | 5008 C1B0h       |
| EPWM12_G3     | 500C C1B0h       |
| EPWM13_G0     | 5000 D1B0h       |
| EPWM13_G1     | 5004 D1B0h       |
| EPWM13_G2     | 5008 D1B0h       |
| EPWM13_G3     | 500C D1B0h       |
| EPWM14_G0     | 5000 E1B0h       |
| EPWM14_G1     | 5004 E1B0h       |
| EPWM14_G2     | 5008 E1B0h       |
| EPWM14_G3     | 500C E1B0h       |
| EPWM15_G0     | 5000 F1B0h       |
| EPWM15_G1     | 5004 F1B0h       |
| EPWM15_G2     | 5008 F1B0h       |
| EPWM15_G3     | 500C F1B0h       |
| EPWM16_G0     | 5001 01B0h       |
| EPWM16_G1     | 5005 01B0h       |
| EPWM16_G2     | 5009 01B0h       |
| EPWM16_G3     | 500D 01B0h       |
| EPWM17_G0     | 5001 11B0h       |
| EPWM17_G1     | 5005 11B0h       |
| EPWM17_G2     | 5009 11B0h       |
| EPWM17_G3     | 500D 11B0h       |
| EPWM18_G0     | 5001 21B0h       |
| EPWM18_G1     | 5005 21B0h       |
| EPWM18_G2     | 5009 21B0h       |
| EPWM18_G3     | 500D 21B0h       |
| EPWM19_G0     | 5001 31B0h       |
| EPWM19_G1     | 5005 31B0h       |
| EPWM19_G2     | 5009 31B0h       |
| EPWM19_G3     | 500D 31B0h       |
| EPWM20_G0     | 5001 41B0h       |
| EPWM20_G1     | 5005 41B0h       |
| EPWM20_G2     | 5009 41B0h       |
| EPWM20_G3     | 500D 41B0h       |

**Table 3-1093. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 51B0h       |
| EPWM21_G1     | 5005 51B0h       |
| EPWM21_G2     | 5009 51B0h       |
| EPWM21_G3     | 500D 51B0h       |
| EPWM22_G0     | 5001 61B0h       |
| EPWM22_G1     | 5005 61B0h       |
| EPWM22_G2     | 5009 61B0h       |
| EPWM22_G3     | 500D 61B0h       |
| EPWM23_G0     | 5001 71B0h       |
| EPWM23_G1     | 5005 71B0h       |
| EPWM23_G2     | 5009 71B0h       |
| EPWM23_G3     | 500D 71B0h       |
| EPWM24_G0     | 5001 81B0h       |
| EPWM24_G1     | 5005 81B0h       |
| EPWM24_G2     | 5009 81B0h       |
| EPWM24_G3     | 500D 81B0h       |
| EPWM25_G0     | 5001 91B0h       |
| EPWM25_G1     | 5005 91B0h       |
| EPWM25_G2     | 5009 91B0h       |
| EPWM25_G3     | 500D 91B0h       |
| EPWM26_G0     | 5001 A1B0h       |
| EPWM26_G1     | 5005 A1B0h       |
| EPWM26_G2     | 5009 A1B0h       |
| EPWM26_G3     | 500D A1B0h       |
| EPWM27_G0     | 5001 B1B0h       |
| EPWM27_G1     | 5005 B1B0h       |
| EPWM27_G2     | 5009 B1B0h       |
| EPWM27_G3     | 500D B1B0h       |
| EPWM28_G0     | 5001 C1B0h       |
| EPWM28_G1     | 5005 C1B0h       |
| EPWM28_G2     | 5009 C1B0h       |
| EPWM28_G3     | 500D C1B0h       |
| EPWM29_G0     | 5001 D1B0h       |
| EPWM29_G1     | 5005 D1B0h       |
| EPWM29_G2     | 5009 D1B0h       |
| EPWM29_G3     | 500D D1B0h       |
| EPWM30_G0     | 5001 E1B0h       |
| EPWM30_G1     | 5005 E1B0h       |
| EPWM30_G2     | 5009 E1B0h       |
| EPWM30_G3     | 500D E1B0h       |
| EPWM31_G0     | 5001 F1B0h       |
| EPWM31_G1     | 5005 F1B0h       |
| EPWM31_G2     | 5009 F1B0h       |
| EPWM31_G3     | 500D F1B0h       |

**Figure 3-345. EPWM\_CAPINTRIPSEL Name Register**

| 15         | 14          | 13          | 12          | 11          | 10          | 9           | 8          |
|------------|-------------|-------------|-------------|-------------|-------------|-------------|------------|
| RESERVED_1 | TRIPINPUT15 | TRIPINPUT14 | TRIPINPUT13 | TRIPINPUT12 | TRIPINPUT11 | TRIPINPUT10 | TRIPINPUT9 |
| R          | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W        |
| 0h         | 0h          | 0h          | 0h          | 0h          | 0h          | 0h          | 0h         |
| 7          | 6           | 5           | 4           | 3           | 2           | 1           | 0          |
| TRIPINPUT8 | TRIPINPUT7  | TRIPINPUT6  | TRIPINPUT5  | TRIPINPUT4  | TRIPINPUT3  | TRIPINPUT2  | TRIPINPUT1 |
| R/W        | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W        |
| 0h         | 0h          | 0h          | 0h          | 0h          | 0h          | 0h          | 0h         |

**Table 3-1095. EPWM\_CAPINTRIPSEL Register Field Descriptions**

| Bit | Field       | Type | Reset | Description                                                                                                                                      |
|-----|-------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | RESERVED_1  | R    | 0h    | Reserved                                                                                                                                         |
| 14  | TRIPINPUT15 | R/W  | 0h    | TRIP Input 15<br>0: Trip Input 15 not selected as combinational ORed input<br>1: Trip Input 15 selected as combinational ORed input to CAPIN mux |
| 13  | TRIPINPUT14 | R/W  | 0h    | TRIP Input 14<br>0: Trip Input 14 not selected as combinational ORed input<br>1: Trip Input 14 selected as combinational ORed input to CAPIN mux |
| 12  | TRIPINPUT13 | R/W  | 0h    | TRIP Input 13<br>0: Trip Input 13 not selected as combinational ORed input<br>1: Trip Input 13 selected as combinational ORed input to CAPIN mux |
| 11  | TRIPINPUT12 | R/W  | 0h    | TRIP Input 12<br>0: Trip Input 12 not selected as combinational ORed input<br>1: Trip Input 12 selected as combinational ORed input to CAPIN mux |
| 10  | TRIPINPUT11 | R/W  | 0h    | TRIP Input 11<br>0: Trip Input 11 not selected as combinational ORed input<br>1: Trip Input 11 selected as combinational ORed input to CAPIN mux |
| 9   | TRIPINPUT10 | R/W  | 0h    | TRIP Input 10<br>0: Trip Input 10 not selected as combinational ORed input<br>1: Trip Input 10 selected as combinational ORed input to CAPIN mux |
| 8   | TRIPINPUT9  | R/W  | 0h    | TRIP Input 9<br>0: Trip Input 9 not selected as combinational ORed input<br>1: Trip Input 9 selected as combinational ORed input to CAPIN mux    |
| 7   | TRIPINPUT8  | R/W  | 0h    | TRIP Input 8<br>0: Trip Input 8 not selected as combinational ORed input<br>1: Trip Input 8 selected as combinational ORed input to CAPIN mux    |
| 6   | TRIPINPUT7  | R/W  | 0h    | TRIP Input 7<br>0: Trip Input 7 not selected as combinational ORed input<br>1: Trip Input 7 selected as combinational ORed input to CAPIN mux    |
| 5   | TRIPINPUT6  | R/W  | 0h    | TRIP Input 6<br>0: Trip Input 6 not selected as combinational ORed input<br>1: Trip Input 6 selected as combinational ORed input to CAPIN mux    |
| 4   | TRIPINPUT5  | R/W  | 0h    | TRIP Input 5<br>0: Trip Input 5 not selected as combinational ORed input<br>1: Trip Input 5 selected as combinational ORed input to CAPIN mux    |
| 3   | TRIPINPUT4  | R/W  | 0h    | TRIP Input 4<br>0: Trip Input 4 not selected as combinational ORed input<br>1: Trip Input 4 selected as combinational ORed input to CAPIN mux    |
| 2   | TRIPINPUT3  | R/W  | 0h    | TRIP Input 3<br>0: Trip Input 3 not selected as combinational ORed input<br>1: Trip Input 3 selected as combinational ORed input to CAPIN mux    |
| 1   | TRIPINPUT2  | R/W  | 0h    | TRIP Input 2<br>0: Trip Input 2 not selected as combinational ORed input<br>1: Trip Input 2 selected as combinational ORed input to CAPIN mux    |

**Table 3-1095. EPWM\_CAPINTRIPSEL Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                   |
|-----|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | TRIPINPUT1 | R/W  | 0h    | TRIP Input 1<br>0: Trip Input 1 not selected as combinational ORed input<br>1: Trip Input 1 selected as combinational ORed input to CAPIN mux |



### 3.7.2.95 EPWM\_CAPTRIPSEL Register

#### 1 EPWM\_CAPTRIPSEL Register (Offset = 1B2h) [reset = 0h]

Event Capture Signal Select.

Return to [Summary Table](#)

**Table 3-1096. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 01B2h       |
| EPWM0_G1      | 5004 01B2h       |
| EPWM0_G2      | 5008 01B2h       |
| EPWM0_G3      | 500C 01B2h       |
| EPWM1_G0      | 5000 11B2h       |
| EPWM1_G1      | 5004 11B2h       |
| EPWM1_G2      | 5008 11B2h       |
| EPWM1_G3      | 500C 11B2h       |
| EPWM2_G0      | 5000 21B2h       |
| EPWM2_G1      | 5004 21B2h       |
| EPWM2_G2      | 5008 21B2h       |
| EPWM2_G3      | 500C 21B2h       |
| EPWM3_G0      | 5000 31B2h       |
| EPWM3_G1      | 5004 31B2h       |
| EPWM3_G2      | 5008 31B2h       |
| EPWM3_G3      | 500C 31B2h       |
| EPWM4_G0      | 5000 41B2h       |
| EPWM4_G1      | 5004 41B2h       |
| EPWM4_G2      | 5008 41B2h       |
| EPWM4_G3      | 500C 41B2h       |
| EPWM5_G0      | 5000 51B2h       |
| EPWM5_G1      | 5004 51B2h       |
| EPWM5_G2      | 5008 51B2h       |
| EPWM5_G3      | 500C 51B2h       |
| EPWM6_G0      | 5000 61B2h       |
| EPWM6_G1      | 5004 61B2h       |
| EPWM6_G2      | 5008 61B2h       |
| EPWM6_G3      | 500C 61B2h       |
| EPWM7_G0      | 5000 71B2h       |
| EPWM7_G1      | 5004 71B2h       |
| EPWM7_G2      | 5008 71B2h       |
| EPWM7_G3      | 500C 71B2h       |
| EPWM8_G0      | 5000 81B2h       |
| EPWM8_G1      | 5004 81B2h       |
| EPWM8_G2      | 5008 81B2h       |
| EPWM8_G3      | 500C 81B2h       |
| EPWM9_G0      | 5000 91B2h       |
| EPWM9_G1      | 5004 91B2h       |
| EPWM9_G2      | 5008 91B2h       |

**Table 3-1096. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 91B2h       |
| EPWM10_G0     | 5000 A1B2h       |
| EPWM10_G1     | 5004 A1B2h       |
| EPWM10_G2     | 5008 A1B2h       |
| EPWM10_G3     | 500C A1B2h       |
| EPWM11_G0     | 5000 B1B2h       |
| EPWM11_G1     | 5004 B1B2h       |
| EPWM11_G2     | 5008 B1B2h       |
| EPWM11_G3     | 500C B1B2h       |
| EPWM12_G0     | 5000 C1B2h       |
| EPWM12_G1     | 5004 C1B2h       |
| EPWM12_G2     | 5008 C1B2h       |
| EPWM12_G3     | 500C C1B2h       |
| EPWM13_G0     | 5000 D1B2h       |
| EPWM13_G1     | 5004 D1B2h       |
| EPWM13_G2     | 5008 D1B2h       |
| EPWM13_G3     | 500C D1B2h       |
| EPWM14_G0     | 5000 E1B2h       |
| EPWM14_G1     | 5004 E1B2h       |
| EPWM14_G2     | 5008 E1B2h       |
| EPWM14_G3     | 500C E1B2h       |
| EPWM15_G0     | 5000 F1B2h       |
| EPWM15_G1     | 5004 F1B2h       |
| EPWM15_G2     | 5008 F1B2h       |
| EPWM15_G3     | 500C F1B2h       |
| EPWM16_G0     | 5001 01B2h       |
| EPWM16_G1     | 5005 01B2h       |
| EPWM16_G2     | 5009 01B2h       |
| EPWM16_G3     | 500D 01B2h       |
| EPWM17_G0     | 5001 11B2h       |
| EPWM17_G1     | 5005 11B2h       |
| EPWM17_G2     | 5009 11B2h       |
| EPWM17_G3     | 500D 11B2h       |
| EPWM18_G0     | 5001 21B2h       |
| EPWM18_G1     | 5005 21B2h       |
| EPWM18_G2     | 5009 21B2h       |
| EPWM18_G3     | 500D 21B2h       |
| EPWM19_G0     | 5001 31B2h       |
| EPWM19_G1     | 5005 31B2h       |
| EPWM19_G2     | 5009 31B2h       |
| EPWM19_G3     | 500D 31B2h       |
| EPWM20_G0     | 5001 41B2h       |
| EPWM20_G1     | 5005 41B2h       |
| EPWM20_G2     | 5009 41B2h       |
| EPWM20_G3     | 500D 41B2h       |

**Table 3-1096. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 51B2h       |
| EPWM21_G1     | 5005 51B2h       |
| EPWM21_G2     | 5009 51B2h       |
| EPWM21_G3     | 500D 51B2h       |
| EPWM22_G0     | 5001 61B2h       |
| EPWM22_G1     | 5005 61B2h       |
| EPWM22_G2     | 5009 61B2h       |
| EPWM22_G3     | 500D 61B2h       |
| EPWM23_G0     | 5001 71B2h       |
| EPWM23_G1     | 5005 71B2h       |
| EPWM23_G2     | 5009 71B2h       |
| EPWM23_G3     | 500D 71B2h       |
| EPWM24_G0     | 5001 81B2h       |
| EPWM24_G1     | 5005 81B2h       |
| EPWM24_G2     | 5009 81B2h       |
| EPWM24_G3     | 500D 81B2h       |
| EPWM25_G0     | 5001 91B2h       |
| EPWM25_G1     | 5005 91B2h       |
| EPWM25_G2     | 5009 91B2h       |
| EPWM25_G3     | 500D 91B2h       |
| EPWM26_G0     | 5001 A1B2h       |
| EPWM26_G1     | 5005 A1B2h       |
| EPWM26_G2     | 5009 A1B2h       |
| EPWM26_G3     | 500D A1B2h       |
| EPWM27_G0     | 5001 B1B2h       |
| EPWM27_G1     | 5005 B1B2h       |
| EPWM27_G2     | 5009 B1B2h       |
| EPWM27_G3     | 500D B1B2h       |
| EPWM28_G0     | 5001 C1B2h       |
| EPWM28_G1     | 5005 C1B2h       |
| EPWM28_G2     | 5009 C1B2h       |
| EPWM28_G3     | 500D C1B2h       |
| EPWM29_G0     | 5001 D1B2h       |
| EPWM29_G1     | 5005 D1B2h       |
| EPWM29_G2     | 5009 D1B2h       |
| EPWM29_G3     | 500D D1B2h       |
| EPWM30_G0     | 5001 E1B2h       |
| EPWM30_G1     | 5005 E1B2h       |
| EPWM30_G2     | 5009 E1B2h       |
| EPWM30_G3     | 500D E1B2h       |
| EPWM31_G0     | 5001 F1B2h       |
| EPWM31_G1     | 5005 F1B2h       |
| EPWM31_G2     | 5009 F1B2h       |
| EPWM31_G3     | 500D F1B2h       |

**Figure 3-346. EPWM\_CAPTRIPSEL Name Register**

|                |    |    |    |              |    |   |   |
|----------------|----|----|----|--------------|----|---|---|
| 15             | 14 | 13 | 12 | 11           | 10 | 9 | 8 |
| RESERVED_1     |    |    |    |              |    |   |   |
| R              |    |    |    |              |    |   |   |
| 0h             |    |    |    |              |    |   |   |
| 7              | 6  | 5  | 4  | 3            | 2  | 1 | 0 |
| CAPGATECOMPSEL |    |    |    | CAPINCOMPSEL |    |   |   |
| R/W            |    |    |    | R/W          |    |   |   |
| 0h             |    |    |    | 0h           |    |   |   |

**Table 3-1098. EPWM\_CAPTRIPSEL Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                           |
|------|----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED_1     | R    | 0h    | Reserved                                                                                                                                                                                                                                                                              |
| 7:4  | CAPGATECOMPSEL | R/W  | 0h    | Digital Compare A Low Input Select Bits<br>0000 TRIPIN1<br>0001 TRIPIN2<br>0010 TRIPIN3<br>0011 TRIPIN4<br>...<br>1011 TRIPIN12<br>1100 Reserved<br>1101 TRIPIN14<br>1110 TRIPIN15<br>1111 Trip combination input [all trip inputs selected by CAPGATETRIPSEL register ORed together] |
| 3:0  | CAPINCOMPSEL   | R/W  | 0h    | Digital Compare A High Input Select Bits<br>0000 TRIPIN1<br>0001 TRIPIN2<br>0010 TRIPIN3<br>0011 TRIPIN4<br>...<br>1011 TRIPIN12<br>1100 Reserved<br>1101 TRIPIN14<br>1110 TRIPIN15<br>1111 Trip combination input [all trip inputs selected by CAPINTRIPSEL register ORed together]  |

### 3.7.2.96 EPWM\_EPWMLOCK Register

#### 1 EPWM\_EPWMLOCK Register (Offset = 1F4h) [reset = 0h]

EPWM Lock Register.

Return to [Summary Table](#)

**Table 3-1099. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 01F4h       |
| EPWM0_G1      | 5004 01F4h       |
| EPWM0_G2      | 5008 01F4h       |
| EPWM0_G3      | 500C 01F4h       |
| EPWM1_G0      | 5000 11F4h       |
| EPWM1_G1      | 5004 11F4h       |
| EPWM1_G2      | 5008 11F4h       |
| EPWM1_G3      | 500C 11F4h       |
| EPWM2_G0      | 5000 21F4h       |
| EPWM2_G1      | 5004 21F4h       |
| EPWM2_G2      | 5008 21F4h       |
| EPWM2_G3      | 500C 21F4h       |
| EPWM3_G0      | 5000 31F4h       |
| EPWM3_G1      | 5004 31F4h       |
| EPWM3_G2      | 5008 31F4h       |
| EPWM3_G3      | 500C 31F4h       |
| EPWM4_G0      | 5000 41F4h       |
| EPWM4_G1      | 5004 41F4h       |
| EPWM4_G2      | 5008 41F4h       |
| EPWM4_G3      | 500C 41F4h       |
| EPWM5_G0      | 5000 51F4h       |
| EPWM5_G1      | 5004 51F4h       |
| EPWM5_G2      | 5008 51F4h       |
| EPWM5_G3      | 500C 51F4h       |
| EPWM6_G0      | 5000 61F4h       |
| EPWM6_G1      | 5004 61F4h       |
| EPWM6_G2      | 5008 61F4h       |
| EPWM6_G3      | 500C 61F4h       |
| EPWM7_G0      | 5000 71F4h       |
| EPWM7_G1      | 5004 71F4h       |
| EPWM7_G2      | 5008 71F4h       |
| EPWM7_G3      | 500C 71F4h       |
| EPWM8_G0      | 5000 81F4h       |
| EPWM8_G1      | 5004 81F4h       |
| EPWM8_G2      | 5008 81F4h       |
| EPWM8_G3      | 500C 81F4h       |
| EPWM9_G0      | 5000 91F4h       |
| EPWM9_G1      | 5004 91F4h       |
| EPWM9_G2      | 5008 91F4h       |

**Table 3-1099. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 91F4h       |
| EPWM10_G0     | 5000 A1F4h       |
| EPWM10_G1     | 5004 A1F4h       |
| EPWM10_G2     | 5008 A1F4h       |
| EPWM10_G3     | 500C A1F4h       |
| EPWM11_G0     | 5000 B1F4h       |
| EPWM11_G1     | 5004 B1F4h       |
| EPWM11_G2     | 5008 B1F4h       |
| EPWM11_G3     | 500C B1F4h       |
| EPWM12_G0     | 5000 C1F4h       |
| EPWM12_G1     | 5004 C1F4h       |
| EPWM12_G2     | 5008 C1F4h       |
| EPWM12_G3     | 500C C1F4h       |
| EPWM13_G0     | 5000 D1F4h       |
| EPWM13_G1     | 5004 D1F4h       |
| EPWM13_G2     | 5008 D1F4h       |
| EPWM13_G3     | 500C D1F4h       |
| EPWM14_G0     | 5000 E1F4h       |
| EPWM14_G1     | 5004 E1F4h       |
| EPWM14_G2     | 5008 E1F4h       |
| EPWM14_G3     | 500C E1F4h       |
| EPWM15_G0     | 5000 F1F4h       |
| EPWM15_G1     | 5004 F1F4h       |
| EPWM15_G2     | 5008 F1F4h       |
| EPWM15_G3     | 500C F1F4h       |
| EPWM16_G0     | 5001 01F4h       |
| EPWM16_G1     | 5005 01F4h       |
| EPWM16_G2     | 5009 01F4h       |
| EPWM16_G3     | 500D 01F4h       |
| EPWM17_G0     | 5001 11F4h       |
| EPWM17_G1     | 5005 11F4h       |
| EPWM17_G2     | 5009 11F4h       |
| EPWM17_G3     | 500D 11F4h       |
| EPWM18_G0     | 5001 21F4h       |
| EPWM18_G1     | 5005 21F4h       |
| EPWM18_G2     | 5009 21F4h       |
| EPWM18_G3     | 500D 21F4h       |
| EPWM19_G0     | 5001 31F4h       |
| EPWM19_G1     | 5005 31F4h       |
| EPWM19_G2     | 5009 31F4h       |
| EPWM19_G3     | 500D 31F4h       |
| EPWM20_G0     | 5001 41F4h       |
| EPWM20_G1     | 5005 41F4h       |
| EPWM20_G2     | 5009 41F4h       |
| EPWM20_G3     | 500D 41F4h       |

**Table 3-1099. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 51F4h       |
| EPWM21_G1     | 5005 51F4h       |
| EPWM21_G2     | 5009 51F4h       |
| EPWM21_G3     | 500D 51F4h       |
| EPWM22_G0     | 5001 61F4h       |
| EPWM22_G1     | 5005 61F4h       |
| EPWM22_G2     | 5009 61F4h       |
| EPWM22_G3     | 500D 61F4h       |
| EPWM23_G0     | 5001 71F4h       |
| EPWM23_G1     | 5005 71F4h       |
| EPWM23_G2     | 5009 71F4h       |
| EPWM23_G3     | 500D 71F4h       |
| EPWM24_G0     | 5001 81F4h       |
| EPWM24_G1     | 5005 81F4h       |
| EPWM24_G2     | 5009 81F4h       |
| EPWM24_G3     | 500D 81F4h       |
| EPWM25_G0     | 5001 91F4h       |
| EPWM25_G1     | 5005 91F4h       |
| EPWM25_G2     | 5009 91F4h       |
| EPWM25_G3     | 500D 91F4h       |
| EPWM26_G0     | 5001 A1F4h       |
| EPWM26_G1     | 5005 A1F4h       |
| EPWM26_G2     | 5009 A1F4h       |
| EPWM26_G3     | 500D A1F4h       |
| EPWM27_G0     | 5001 B1F4h       |
| EPWM27_G1     | 5005 B1F4h       |
| EPWM27_G2     | 5009 B1F4h       |
| EPWM27_G3     | 500D B1F4h       |
| EPWM28_G0     | 5001 C1F4h       |
| EPWM28_G1     | 5005 C1F4h       |
| EPWM28_G2     | 5009 C1F4h       |
| EPWM28_G3     | 500D C1F4h       |
| EPWM29_G0     | 5001 D1F4h       |
| EPWM29_G1     | 5005 D1F4h       |
| EPWM29_G2     | 5009 D1F4h       |
| EPWM29_G3     | 500D D1F4h       |
| EPWM30_G0     | 5001 E1F4h       |
| EPWM30_G1     | 5005 E1F4h       |
| EPWM30_G2     | 5009 E1F4h       |
| EPWM30_G3     | 500D E1F4h       |
| EPWM31_G0     | 5001 F1F4h       |
| EPWM31_G1     | 5005 F1F4h       |
| EPWM31_G2     | 5009 F1F4h       |
| EPWM31_G3     | 500D F1F4h       |

**Figure 3-347. EPWM\_EPWMLOCK Name Register**

|            |    |    |           |           |           |           |           |
|------------|----|----|-----------|-----------|-----------|-----------|-----------|
| 31         | 30 | 29 | 28        | 27        | 26        | 25        | 24        |
| KEY        |    |    |           |           |           |           |           |
| R/W        |    |    |           |           |           |           |           |
| 0h         |    |    |           |           |           |           |           |
| 23         | 22 | 21 | 20        | 19        | 18        | 17        | 16        |
| KEY        |    |    |           |           |           |           |           |
| R/W        |    |    |           |           |           |           |           |
| 0h         |    |    |           |           |           |           |           |
| 15         | 14 | 13 | 12        | 11        | 10        | 9         | 8         |
| RESERVED_1 |    |    |           |           |           |           |           |
| R          |    |    |           |           |           |           |           |
| 0h         |    |    |           |           |           |           |           |
| 7          | 6  | 5  | 4         | 3         | 2         | 1         | 0         |
| RESERVED_1 |    |    | DCLOCK    | TZCLRLOCK | TZCFGLOCK | GLLOCK    | HRLOCK    |
| R          |    |    | R/R/WONCE | R/R/WONCE | R/R/WONCE | R/R/WONCE | R/R/WONCE |
| 0h         |    |    | 0h        | 0h        | 0h        | 0h        | 0h        |

**Table 3-1101. EPWM\_EPWMLOCK Register Field Descriptions**

| Bit   | Field      | Type          | Reset | Description                                                                                                                                                                                                                                                 |
|-------|------------|---------------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | KEY        | R/W           | 0h    | Write to this register succeeds only if this field is written with a value of 0xa5a5<br>Note:<br>[1] Due to this KEY, only 32-bit writes will succeed [provided the KEY matches]. 16-bit writes to the upper or lower half of this register will be ignored |
| 15:5  | RESERVED_1 | R             | 0h    | Reserved                                                                                                                                                                                                                                                    |
| 4     | DCLOCK     | R/R/<br>WONCE | 0h    | 0:Digital Compare registers from 0xC0 to 0xD9 offsets are protected by EALLOW.<br>1:Digital Compare registers from 0xC0 and 0xD9 offsets are locked and not writable.                                                                                       |
| 3     | TZCLRLOCK  | R/R/<br>WONCE | 0h    | 0:Digital Compare registers from 0x97 to 0x9B offsets are protected by EALLOW.<br>1:Digital Compare registers from 0x97 and 0x9B offsets are locked and not writable.                                                                                       |
| 2     | TZCFGLOCK  | R/R/<br>WONCE | 0h    | 0:TripZone registers from 0x80 to 0x8D and TZTRIPOUTSEL at 0x9D offsets are protected by EALLOW.<br>1:TripZone registers from 0x80 and 0x8D and TZTRIPOUTSEL at 0x9D offsets are locked and not writable.                                                   |
| 1     | GLLOCK     | R/R/<br>WONCE | 0h    | 0:TripZone registers from 0x34 to 0x35 offsets are protected by EALLOW.<br>1:TripZone registers from 0x34 to 0x35 offsets are locked and not writable                                                                                                       |
| 0     | HRLOCK     | R/R/<br>WONCE | 0h    | 0: HRPWM registers from 0x20 to 0x2D offsets are protected by EALLOW<br>1:HRPWM registers from 0x20 and 0x2D offsets are locked and not writable.                                                                                                           |



### 3.7.2.97 EPWM\_HWVDELVAL Register

#### 1 EPWM\_HWVDELVAL Register (Offset = 1FAh) [reset = 0h]

Hardware Valley Mode Delay Register.

Return to [Summary Table](#)

**Table 3-1102. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 01FAh       |
| EPWM0_G1      | 5004 01FAh       |
| EPWM0_G2      | 5008 01FAh       |
| EPWM0_G3      | 500C 01FAh       |
| EPWM1_G0      | 5000 11FAh       |
| EPWM1_G1      | 5004 11FAh       |
| EPWM1_G2      | 5008 11FAh       |
| EPWM1_G3      | 500C 11FAh       |
| EPWM2_G0      | 5000 21FAh       |
| EPWM2_G1      | 5004 21FAh       |
| EPWM2_G2      | 5008 21FAh       |
| EPWM2_G3      | 500C 21FAh       |
| EPWM3_G0      | 5000 31FAh       |
| EPWM3_G1      | 5004 31FAh       |
| EPWM3_G2      | 5008 31FAh       |
| EPWM3_G3      | 500C 31FAh       |
| EPWM4_G0      | 5000 41FAh       |
| EPWM4_G1      | 5004 41FAh       |
| EPWM4_G2      | 5008 41FAh       |
| EPWM4_G3      | 500C 41FAh       |
| EPWM5_G0      | 5000 51FAh       |
| EPWM5_G1      | 5004 51FAh       |
| EPWM5_G2      | 5008 51FAh       |
| EPWM5_G3      | 500C 51FAh       |
| EPWM6_G0      | 5000 61FAh       |
| EPWM6_G1      | 5004 61FAh       |
| EPWM6_G2      | 5008 61FAh       |
| EPWM6_G3      | 500C 61FAh       |
| EPWM7_G0      | 5000 71FAh       |
| EPWM7_G1      | 5004 71FAh       |
| EPWM7_G2      | 5008 71FAh       |
| EPWM7_G3      | 500C 71FAh       |
| EPWM8_G0      | 5000 81FAh       |
| EPWM8_G1      | 5004 81FAh       |
| EPWM8_G2      | 5008 81FAh       |
| EPWM8_G3      | 500C 81FAh       |
| EPWM9_G0      | 5000 91FAh       |
| EPWM9_G1      | 5004 91FAh       |
| EPWM9_G2      | 5008 91FAh       |

**Table 3-1102. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 91FAh       |
| EPWM10_G0     | 5000 A1FAh       |
| EPWM10_G1     | 5004 A1FAh       |
| EPWM10_G2     | 5008 A1FAh       |
| EPWM10_G3     | 500C A1FAh       |
| EPWM11_G0     | 5000 B1FAh       |
| EPWM11_G1     | 5004 B1FAh       |
| EPWM11_G2     | 5008 B1FAh       |
| EPWM11_G3     | 500C B1FAh       |
| EPWM12_G0     | 5000 C1FAh       |
| EPWM12_G1     | 5004 C1FAh       |
| EPWM12_G2     | 5008 C1FAh       |
| EPWM12_G3     | 500C C1FAh       |
| EPWM13_G0     | 5000 D1FAh       |
| EPWM13_G1     | 5004 D1FAh       |
| EPWM13_G2     | 5008 D1FAh       |
| EPWM13_G3     | 500C D1FAh       |
| EPWM14_G0     | 5000 E1FAh       |
| EPWM14_G1     | 5004 E1FAh       |
| EPWM14_G2     | 5008 E1FAh       |
| EPWM14_G3     | 500C E1FAh       |
| EPWM15_G0     | 5000 F1FAh       |
| EPWM15_G1     | 5004 F1FAh       |
| EPWM15_G2     | 5008 F1FAh       |
| EPWM15_G3     | 500C F1FAh       |
| EPWM16_G0     | 5001 01FAh       |
| EPWM16_G1     | 5005 01FAh       |
| EPWM16_G2     | 5009 01FAh       |
| EPWM16_G3     | 500D 01FAh       |
| EPWM17_G0     | 5001 11FAh       |
| EPWM17_G1     | 5005 11FAh       |
| EPWM17_G2     | 5009 11FAh       |
| EPWM17_G3     | 500D 11FAh       |
| EPWM18_G0     | 5001 21FAh       |
| EPWM18_G1     | 5005 21FAh       |
| EPWM18_G2     | 5009 21FAh       |
| EPWM18_G3     | 500D 21FAh       |
| EPWM19_G0     | 5001 31FAh       |
| EPWM19_G1     | 5005 31FAh       |
| EPWM19_G2     | 5009 31FAh       |
| EPWM19_G3     | 500D 31FAh       |
| EPWM20_G0     | 5001 41FAh       |
| EPWM20_G1     | 5005 41FAh       |
| EPWM20_G2     | 5009 41FAh       |
| EPWM20_G3     | 500D 41FAh       |

**Table 3-1102. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 51FAh       |
| EPWM21_G1     | 5005 51FAh       |
| EPWM21_G2     | 5009 51FAh       |
| EPWM21_G3     | 500D 51FAh       |
| EPWM22_G0     | 5001 61FAh       |
| EPWM22_G1     | 5005 61FAh       |
| EPWM22_G2     | 5009 61FAh       |
| EPWM22_G3     | 500D 61FAh       |
| EPWM23_G0     | 5001 71FAh       |
| EPWM23_G1     | 5005 71FAh       |
| EPWM23_G2     | 5009 71FAh       |
| EPWM23_G3     | 500D 71FAh       |
| EPWM24_G0     | 5001 81FAh       |
| EPWM24_G1     | 5005 81FAh       |
| EPWM24_G2     | 5009 81FAh       |
| EPWM24_G3     | 500D 81FAh       |
| EPWM25_G0     | 5001 91FAh       |
| EPWM25_G1     | 5005 91FAh       |
| EPWM25_G2     | 5009 91FAh       |
| EPWM25_G3     | 500D 91FAh       |
| EPWM26_G0     | 5001 A1FAh       |
| EPWM26_G1     | 5005 A1FAh       |
| EPWM26_G2     | 5009 A1FAh       |
| EPWM26_G3     | 500D A1FAh       |
| EPWM27_G0     | 5001 B1FAh       |
| EPWM27_G1     | 5005 B1FAh       |
| EPWM27_G2     | 5009 B1FAh       |
| EPWM27_G3     | 500D B1FAh       |
| EPWM28_G0     | 5001 C1FAh       |
| EPWM28_G1     | 5005 C1FAh       |
| EPWM28_G2     | 5009 C1FAh       |
| EPWM28_G3     | 500D C1FAh       |
| EPWM29_G0     | 5001 D1FAh       |
| EPWM29_G1     | 5005 D1FAh       |
| EPWM29_G2     | 5009 D1FAh       |
| EPWM29_G3     | 500D D1FAh       |
| EPWM30_G0     | 5001 E1FAh       |
| EPWM30_G1     | 5005 E1FAh       |
| EPWM30_G2     | 5009 E1FAh       |
| EPWM30_G3     | 500D E1FAh       |
| EPWM31_G0     | 5001 F1FAh       |
| EPWM31_G1     | 5005 F1FAh       |
| EPWM31_G2     | 5009 F1FAh       |
| EPWM31_G3     | 500D F1FAh       |

**Figure 3-348. EPWM\_HWVDELVAL Name Register**

|           |    |    |    |    |    |   |   |
|-----------|----|----|----|----|----|---|---|
| 15        | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| HWVDELVAL |    |    |    |    |    |   |   |
| R         |    |    |    |    |    |   |   |
| 0h        |    |    |    |    |    |   |   |
| 7         | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| HWVDELVAL |    |    |    |    |    |   |   |
| R         |    |    |    |    |    |   |   |
| 0h        |    |    |    |    |    |   |   |

**Table 3-1104. EPWM\_HWVDELVAL Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|------|-----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | HWVDELVAL | R    | 0h    | <p>Hardware Valley Delay Value Register</p> <p>This read only register reflects the hardware delay value calculated by the equations defined in VCAPCTL[VDELAYDIV]. This reflects the latest value from the hardware calculations and can change every time valley capture sequence is triggered and VCAP1 and VCAP2 values are updated.</p> |

### 3.7.2.98 EPWM\_VCNTVAL Register

#### 1 EPWM\_VCNTVAL Register (Offset = 1FCh) [reset = 0h]

Hardware Valley Counter Register.

Return to [Summary Table](#)

**Table 3-1105. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 01FCh       |
| EPWM0_G1      | 5004 01FCh       |
| EPWM0_G2      | 5008 01FCh       |
| EPWM0_G3      | 500C 01FCh       |
| EPWM1_G0      | 5000 11FCh       |
| EPWM1_G1      | 5004 11FCh       |
| EPWM1_G2      | 5008 11FCh       |
| EPWM1_G3      | 500C 11FCh       |
| EPWM2_G0      | 5000 21FCh       |
| EPWM2_G1      | 5004 21FCh       |
| EPWM2_G2      | 5008 21FCh       |
| EPWM2_G3      | 500C 21FCh       |
| EPWM3_G0      | 5000 31FCh       |
| EPWM3_G1      | 5004 31FCh       |
| EPWM3_G2      | 5008 31FCh       |
| EPWM3_G3      | 500C 31FCh       |
| EPWM4_G0      | 5000 41FCh       |
| EPWM4_G1      | 5004 41FCh       |
| EPWM4_G2      | 5008 41FCh       |
| EPWM4_G3      | 500C 41FCh       |
| EPWM5_G0      | 5000 51FCh       |
| EPWM5_G1      | 5004 51FCh       |
| EPWM5_G2      | 5008 51FCh       |
| EPWM5_G3      | 500C 51FCh       |
| EPWM6_G0      | 5000 61FCh       |
| EPWM6_G1      | 5004 61FCh       |
| EPWM6_G2      | 5008 61FCh       |
| EPWM6_G3      | 500C 61FCh       |
| EPWM7_G0      | 5000 71FCh       |
| EPWM7_G1      | 5004 71FCh       |
| EPWM7_G2      | 5008 71FCh       |
| EPWM7_G3      | 500C 71FCh       |
| EPWM8_G0      | 5000 81FCh       |
| EPWM8_G1      | 5004 81FCh       |
| EPWM8_G2      | 5008 81FCh       |
| EPWM8_G3      | 500C 81FCh       |
| EPWM9_G0      | 5000 91FCh       |
| EPWM9_G1      | 5004 91FCh       |
| EPWM9_G2      | 5008 91FCh       |

**Table 3-1105. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 91FCh       |
| EPWM10_G0     | 5000 A1FCh       |
| EPWM10_G1     | 5004 A1FCh       |
| EPWM10_G2     | 5008 A1FCh       |
| EPWM10_G3     | 500C A1FCh       |
| EPWM11_G0     | 5000 B1FCh       |
| EPWM11_G1     | 5004 B1FCh       |
| EPWM11_G2     | 5008 B1FCh       |
| EPWM11_G3     | 500C B1FCh       |
| EPWM12_G0     | 5000 C1FCh       |
| EPWM12_G1     | 5004 C1FCh       |
| EPWM12_G2     | 5008 C1FCh       |
| EPWM12_G3     | 500C C1FCh       |
| EPWM13_G0     | 5000 D1FCh       |
| EPWM13_G1     | 5004 D1FCh       |
| EPWM13_G2     | 5008 D1FCh       |
| EPWM13_G3     | 500C D1FCh       |
| EPWM14_G0     | 5000 E1FCh       |
| EPWM14_G1     | 5004 E1FCh       |
| EPWM14_G2     | 5008 E1FCh       |
| EPWM14_G3     | 500C E1FCh       |
| EPWM15_G0     | 5000 F1FCh       |
| EPWM15_G1     | 5004 F1FCh       |
| EPWM15_G2     | 5008 F1FCh       |
| EPWM15_G3     | 500C F1FCh       |
| EPWM16_G0     | 5001 01FCh       |
| EPWM16_G1     | 5005 01FCh       |
| EPWM16_G2     | 5009 01FCh       |
| EPWM16_G3     | 500D 01FCh       |
| EPWM17_G0     | 5001 11FCh       |
| EPWM17_G1     | 5005 11FCh       |
| EPWM17_G2     | 5009 11FCh       |
| EPWM17_G3     | 500D 11FCh       |
| EPWM18_G0     | 5001 21FCh       |
| EPWM18_G1     | 5005 21FCh       |
| EPWM18_G2     | 5009 21FCh       |
| EPWM18_G3     | 500D 21FCh       |
| EPWM19_G0     | 5001 31FCh       |
| EPWM19_G1     | 5005 31FCh       |
| EPWM19_G2     | 5009 31FCh       |
| EPWM19_G3     | 500D 31FCh       |
| EPWM20_G0     | 5001 41FCh       |
| EPWM20_G1     | 5005 41FCh       |
| EPWM20_G2     | 5009 41FCh       |
| EPWM20_G3     | 500D 41FCh       |

**Table 3-1105. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 51FCh       |
| EPWM21_G1     | 5005 51FCh       |
| EPWM21_G2     | 5009 51FCh       |
| EPWM21_G3     | 500D 51FCh       |
| EPWM22_G0     | 5001 61FCh       |
| EPWM22_G1     | 5005 61FCh       |
| EPWM22_G2     | 5009 61FCh       |
| EPWM22_G3     | 500D 61FCh       |
| EPWM23_G0     | 5001 71FCh       |
| EPWM23_G1     | 5005 71FCh       |
| EPWM23_G2     | 5009 71FCh       |
| EPWM23_G3     | 500D 71FCh       |
| EPWM24_G0     | 5001 81FCh       |
| EPWM24_G1     | 5005 81FCh       |
| EPWM24_G2     | 5009 81FCh       |
| EPWM24_G3     | 500D 81FCh       |
| EPWM25_G0     | 5001 91FCh       |
| EPWM25_G1     | 5005 91FCh       |
| EPWM25_G2     | 5009 91FCh       |
| EPWM25_G3     | 500D 91FCh       |
| EPWM26_G0     | 5001 A1FCh       |
| EPWM26_G1     | 5005 A1FCh       |
| EPWM26_G2     | 5009 A1FCh       |
| EPWM26_G3     | 500D A1FCh       |
| EPWM27_G0     | 5001 B1FCh       |
| EPWM27_G1     | 5005 B1FCh       |
| EPWM27_G2     | 5009 B1FCh       |
| EPWM27_G3     | 500D B1FCh       |
| EPWM28_G0     | 5001 C1FCh       |
| EPWM28_G1     | 5005 C1FCh       |
| EPWM28_G2     | 5009 C1FCh       |
| EPWM28_G3     | 500D C1FCh       |
| EPWM29_G0     | 5001 D1FCh       |
| EPWM29_G1     | 5005 D1FCh       |
| EPWM29_G2     | 5009 D1FCh       |
| EPWM29_G3     | 500D D1FCh       |
| EPWM30_G0     | 5001 E1FCh       |
| EPWM30_G1     | 5005 E1FCh       |
| EPWM30_G2     | 5009 E1FCh       |
| EPWM30_G3     | 500D E1FCh       |
| EPWM31_G0     | 5001 F1FCh       |
| EPWM31_G1     | 5005 F1FCh       |
| EPWM31_G2     | 5009 F1FCh       |
| EPWM31_G3     | 500D F1FCh       |

**Figure 3-349. EPWM\_VCNTVAL Name Register**

|         |    |    |    |    |    |   |   |
|---------|----|----|----|----|----|---|---|
| 15      | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| VCNTVAL |    |    |    |    |    |   |   |
| R       |    |    |    |    |    |   |   |
| 0h      |    |    |    |    |    |   |   |
| 7       | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| VCNTVAL |    |    |    |    |    |   |   |
| R       |    |    |    |    |    |   |   |
| 0h      |    |    |    |    |    |   |   |

**Table 3-1107. EPWM\_VCNTVAL Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                   |
|------|---------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | VCNTVAL | R    | 0h    | Valley Time Base Counter Register<br>This register reflects the captured VCNT value upon occurrence of STOPEDGE selected in VCNTCFG register. |



### 3.7.2.99 EPWM\_XCMPCTL1 Register

#### 1 EPWM\_XCMPCTL1 Register (Offset = 400h) [reset = 0h]

XCMP Mode Control Register.

Return to [Summary Table](#)

**Table 3-1108. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0400h       |
| EPWM0_G1      | 5004 0400h       |
| EPWM0_G2      | 5008 0400h       |
| EPWM0_G3      | 500C 0400h       |
| EPWM1_G0      | 5000 1400h       |
| EPWM1_G1      | 5004 1400h       |
| EPWM1_G2      | 5008 1400h       |
| EPWM1_G3      | 500C 1400h       |
| EPWM2_G0      | 5000 2400h       |
| EPWM2_G1      | 5004 2400h       |
| EPWM2_G2      | 5008 2400h       |
| EPWM2_G3      | 500C 2400h       |
| EPWM3_G0      | 5000 3400h       |
| EPWM3_G1      | 5004 3400h       |
| EPWM3_G2      | 5008 3400h       |
| EPWM3_G3      | 500C 3400h       |
| EPWM4_G0      | 5000 4400h       |
| EPWM4_G1      | 5004 4400h       |
| EPWM4_G2      | 5008 4400h       |
| EPWM4_G3      | 500C 4400h       |
| EPWM5_G0      | 5000 5400h       |
| EPWM5_G1      | 5004 5400h       |
| EPWM5_G2      | 5008 5400h       |
| EPWM5_G3      | 500C 5400h       |
| EPWM6_G0      | 5000 6400h       |
| EPWM6_G1      | 5004 6400h       |
| EPWM6_G2      | 5008 6400h       |
| EPWM6_G3      | 500C 6400h       |
| EPWM7_G0      | 5000 7400h       |
| EPWM7_G1      | 5004 7400h       |
| EPWM7_G2      | 5008 7400h       |
| EPWM7_G3      | 500C 7400h       |
| EPWM8_G0      | 5000 8400h       |
| EPWM8_G1      | 5004 8400h       |
| EPWM8_G2      | 5008 8400h       |
| EPWM8_G3      | 500C 8400h       |
| EPWM9_G0      | 5000 9400h       |
| EPWM9_G1      | 5004 9400h       |
| EPWM9_G2      | 5008 9400h       |

**Table 3-1108. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9400h       |
| EPWM10_G0     | 5000 A400h       |
| EPWM10_G1     | 5004 A400h       |
| EPWM10_G2     | 5008 A400h       |
| EPWM10_G3     | 500C A400h       |
| EPWM11_G0     | 5000 B400h       |
| EPWM11_G1     | 5004 B400h       |
| EPWM11_G2     | 5008 B400h       |
| EPWM11_G3     | 500C B400h       |
| EPWM12_G0     | 5000 C400h       |
| EPWM12_G1     | 5004 C400h       |
| EPWM12_G2     | 5008 C400h       |
| EPWM12_G3     | 500C C400h       |
| EPWM13_G0     | 5000 D400h       |
| EPWM13_G1     | 5004 D400h       |
| EPWM13_G2     | 5008 D400h       |
| EPWM13_G3     | 500C D400h       |
| EPWM14_G0     | 5000 E400h       |
| EPWM14_G1     | 5004 E400h       |
| EPWM14_G2     | 5008 E400h       |
| EPWM14_G3     | 500C E400h       |
| EPWM15_G0     | 5000 F400h       |
| EPWM15_G1     | 5004 F400h       |
| EPWM15_G2     | 5008 F400h       |
| EPWM15_G3     | 500C F400h       |
| EPWM16_G0     | 5001 0400h       |
| EPWM16_G1     | 5005 0400h       |
| EPWM16_G2     | 5009 0400h       |
| EPWM16_G3     | 500D 0400h       |
| EPWM17_G0     | 5001 1400h       |
| EPWM17_G1     | 5005 1400h       |
| EPWM17_G2     | 5009 1400h       |
| EPWM17_G3     | 500D 1400h       |
| EPWM18_G0     | 5001 2400h       |
| EPWM18_G1     | 5005 2400h       |
| EPWM18_G2     | 5009 2400h       |
| EPWM18_G3     | 500D 2400h       |
| EPWM19_G0     | 5001 3400h       |
| EPWM19_G1     | 5005 3400h       |
| EPWM19_G2     | 5009 3400h       |
| EPWM19_G3     | 500D 3400h       |
| EPWM20_G0     | 5001 4400h       |
| EPWM20_G1     | 5005 4400h       |
| EPWM20_G2     | 5009 4400h       |
| EPWM20_G3     | 500D 4400h       |

**Table 3-1108. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5400h       |
| EPWM21_G1     | 5005 5400h       |
| EPWM21_G2     | 5009 5400h       |
| EPWM21_G3     | 500D 5400h       |
| EPWM22_G0     | 5001 6400h       |
| EPWM22_G1     | 5005 6400h       |
| EPWM22_G2     | 5009 6400h       |
| EPWM22_G3     | 500D 6400h       |
| EPWM23_G0     | 5001 7400h       |
| EPWM23_G1     | 5005 7400h       |
| EPWM23_G2     | 5009 7400h       |
| EPWM23_G3     | 500D 7400h       |
| EPWM24_G0     | 5001 8400h       |
| EPWM24_G1     | 5005 8400h       |
| EPWM24_G2     | 5009 8400h       |
| EPWM24_G3     | 500D 8400h       |
| EPWM25_G0     | 5001 9400h       |
| EPWM25_G1     | 5005 9400h       |
| EPWM25_G2     | 5009 9400h       |
| EPWM25_G3     | 500D 9400h       |
| EPWM26_G0     | 5001 A400h       |
| EPWM26_G1     | 5005 A400h       |
| EPWM26_G2     | 5009 A400h       |
| EPWM26_G3     | 500D A400h       |
| EPWM27_G0     | 5001 B400h       |
| EPWM27_G1     | 5005 B400h       |
| EPWM27_G2     | 5009 B400h       |
| EPWM27_G3     | 500D B400h       |
| EPWM28_G0     | 5001 C400h       |
| EPWM28_G1     | 5005 C400h       |
| EPWM28_G2     | 5009 C400h       |
| EPWM28_G3     | 500D C400h       |
| EPWM29_G0     | 5001 D400h       |
| EPWM29_G1     | 5005 D400h       |
| EPWM29_G2     | 5009 D400h       |
| EPWM29_G3     | 500D D400h       |
| EPWM30_G0     | 5001 E400h       |
| EPWM30_G1     | 5005 E400h       |
| EPWM30_G2     | 5009 E400h       |
| EPWM30_G3     | 500D E400h       |
| EPWM31_G0     | 5001 F400h       |
| EPWM31_G1     | 5005 F400h       |
| EPWM31_G2     | 5009 F400h       |
| EPWM31_G3     | 500D F400h       |

**Figure 3-350. EPWM\_XCMPCTL1 Name Register**

|             |    |    |    |             |    |            |        |
|-------------|----|----|----|-------------|----|------------|--------|
| 31          | 30 | 29 | 28 | 27          | 26 | 25         | 24     |
| RESERVED_2  |    |    |    |             |    |            |        |
| R           |    |    |    |             |    |            |        |
| 0h          |    |    |    |             |    |            |        |
| 23          | 22 | 21 | 20 | 19          | 18 | 17         | 16     |
| RESERVED_2  |    |    |    |             |    |            |        |
| R           |    |    |    |             |    |            |        |
| 0h          |    |    |    |             |    |            |        |
| 15          | 14 | 13 | 12 | 11          | 10 | 9          | 8      |
| RESERVED_2  |    |    |    | XCMPB_ALLOC |    |            |        |
| R           |    |    |    | R/W         |    |            |        |
| 0h          |    |    |    | 0h          |    |            |        |
| 7           | 6  | 5  | 4  | 3           | 2  | 1          | 0      |
| XCMPA_ALLOC |    |    |    | RESERVED_1  |    | XCMPSPPLIT | XCMPEN |
| R/W         |    |    |    | R           |    | R/W        | R/W    |
| 0h          |    |    |    | 0h          |    | 0h         | 0h     |

**Table 3-1110. EPWM\_XCMPCTL1 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|-------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED_2  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 11:8  | XCMPB_ALLOC | R/W  | 0h    | XCMPn register allocation for CMPB:<br>- 0 --> Reserved<br>- 1 --> Reserved<br>- 2 --> Reserved<br>- 3 --> Reserved<br>- 4 --> Reserved<br>- 5 --> XCMP5<br>- 6 --> XCMP5, XCMP6<br>- 7 --> XCMP5, XCMP6, XCMP7<br>- 8 --> XCMP5, XCMP6, XCMP7, XCMP8<br>This register settings will take effect only when XCMPEN==1<br>And XCMPSPPLIT ==1                                                                                                                                                                                                                                               |
| 7:4   | XCMPA_ALLOC | R/W  | 0h    | XCMPn register allocation for CMPA:<br>- 0 --> No XCMP<br>- 1 --> XCMP1<br>- 2 --> XCMP1, XCMP2<br>- 3 --> XCMP1, XCMP2, XCMP3<br>- 4 --> XCMP1, XCMP2, XCMP3, XCMP4<br>- 5 --> XCMP1, XCMP2, XCMP3, XCMP4, XCMP5<br>- 6 --> XCMP1, XCMP2, XCMP3, XCMP4, XCMP5, XCMP6<br>- 7 --> XCMP1, XCMP2, XCMP3, XCMP4, XCMP5, XCMP6, XCMP7<br>- 8 --> XCMP1, XCMP2, XCMP3, XCMP4, XCMP5, XCMP6, XCMP7, XCMP8<br>This register settings will take effect only when XCMPEN==1<br>If XCMPSPPLIT ==1, this field cannot be greater than 4. If XCMPSPPLIT ==1 only lower 3 bits are used in this field. |
| 3:2   | RESERVED_1  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 1     | XCMPSPPLIT  | R/W  | 0h    | XCMP Register Allocation Options:<br>0 : XCMP1-8 --> CMPA<br>1 : XCMP1-4 -->CMPA, XCMP5-8 CMPB<br>This register settings will take effect only when XCMPEN==1                                                                                                                                                                                                                                                                                                                                                                                                                            |

**Table 3-1110. EPWM\_XCMPCTL1 Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                                                      |
|-----|--------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | XCMPEN | R/W  | 0h    | XCMP Compare Register Operation Enable:<br>0 XCMP register operation Disabled<br>[operation compatible to Type-4]<br>1 XCMP register operation Enabled<br>[New CMPx registers are effective - section 1.3 details the operation] |

### 3.7.2.100 EPWM\_XLOADCTL Register

#### 1 EPWM\_XLOADCTL Register (Offset = 410h) [reset = 0h]

XCMP Mode Load Control Register.

Return to [Summary Table](#)

**Table 3-1111. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0410h       |
| EPWM0_G1      | 5004 0410h       |
| EPWM0_G2      | 5008 0410h       |
| EPWM0_G3      | 500C 0410h       |
| EPWM1_G0      | 5000 1410h       |
| EPWM1_G1      | 5004 1410h       |
| EPWM1_G2      | 5008 1410h       |
| EPWM1_G3      | 500C 1410h       |
| EPWM2_G0      | 5000 2410h       |
| EPWM2_G1      | 5004 2410h       |
| EPWM2_G2      | 5008 2410h       |
| EPWM2_G3      | 500C 2410h       |
| EPWM3_G0      | 5000 3410h       |
| EPWM3_G1      | 5004 3410h       |
| EPWM3_G2      | 5008 3410h       |
| EPWM3_G3      | 500C 3410h       |
| EPWM4_G0      | 5000 4410h       |
| EPWM4_G1      | 5004 4410h       |
| EPWM4_G2      | 5008 4410h       |
| EPWM4_G3      | 500C 4410h       |
| EPWM5_G0      | 5000 5410h       |
| EPWM5_G1      | 5004 5410h       |
| EPWM5_G2      | 5008 5410h       |
| EPWM5_G3      | 500C 5410h       |
| EPWM6_G0      | 5000 6410h       |
| EPWM6_G1      | 5004 6410h       |
| EPWM6_G2      | 5008 6410h       |
| EPWM6_G3      | 500C 6410h       |
| EPWM7_G0      | 5000 7410h       |
| EPWM7_G1      | 5004 7410h       |
| EPWM7_G2      | 5008 7410h       |
| EPWM7_G3      | 500C 7410h       |
| EPWM8_G0      | 5000 8410h       |
| EPWM8_G1      | 5004 8410h       |
| EPWM8_G2      | 5008 8410h       |
| EPWM8_G3      | 500C 8410h       |
| EPWM9_G0      | 5000 9410h       |
| EPWM9_G1      | 5004 9410h       |
| EPWM9_G2      | 5008 9410h       |

**Table 3-1111. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9410h       |
| EPWM10_G0     | 5000 A410h       |
| EPWM10_G1     | 5004 A410h       |
| EPWM10_G2     | 5008 A410h       |
| EPWM10_G3     | 500C A410h       |
| EPWM11_G0     | 5000 B410h       |
| EPWM11_G1     | 5004 B410h       |
| EPWM11_G2     | 5008 B410h       |
| EPWM11_G3     | 500C B410h       |
| EPWM12_G0     | 5000 C410h       |
| EPWM12_G1     | 5004 C410h       |
| EPWM12_G2     | 5008 C410h       |
| EPWM12_G3     | 500C C410h       |
| EPWM13_G0     | 5000 D410h       |
| EPWM13_G1     | 5004 D410h       |
| EPWM13_G2     | 5008 D410h       |
| EPWM13_G3     | 500C D410h       |
| EPWM14_G0     | 5000 E410h       |
| EPWM14_G1     | 5004 E410h       |
| EPWM14_G2     | 5008 E410h       |
| EPWM14_G3     | 500C E410h       |
| EPWM15_G0     | 5000 F410h       |
| EPWM15_G1     | 5004 F410h       |
| EPWM15_G2     | 5008 F410h       |
| EPWM15_G3     | 500C F410h       |
| EPWM16_G0     | 5001 0410h       |
| EPWM16_G1     | 5005 0410h       |
| EPWM16_G2     | 5009 0410h       |
| EPWM16_G3     | 500D 0410h       |
| EPWM17_G0     | 5001 1410h       |
| EPWM17_G1     | 5005 1410h       |
| EPWM17_G2     | 5009 1410h       |
| EPWM17_G3     | 500D 1410h       |
| EPWM18_G0     | 5001 2410h       |
| EPWM18_G1     | 5005 2410h       |
| EPWM18_G2     | 5009 2410h       |
| EPWM18_G3     | 500D 2410h       |
| EPWM19_G0     | 5001 3410h       |
| EPWM19_G1     | 5005 3410h       |
| EPWM19_G2     | 5009 3410h       |
| EPWM19_G3     | 500D 3410h       |
| EPWM20_G0     | 5001 4410h       |
| EPWM20_G1     | 5005 4410h       |
| EPWM20_G2     | 5009 4410h       |
| EPWM20_G3     | 500D 4410h       |

**Table 3-1111. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5410h       |
| EPWM21_G1     | 5005 5410h       |
| EPWM21_G2     | 5009 5410h       |
| EPWM21_G3     | 500D 5410h       |
| EPWM22_G0     | 5001 6410h       |
| EPWM22_G1     | 5005 6410h       |
| EPWM22_G2     | 5009 6410h       |
| EPWM22_G3     | 500D 6410h       |
| EPWM23_G0     | 5001 7410h       |
| EPWM23_G1     | 5005 7410h       |
| EPWM23_G2     | 5009 7410h       |
| EPWM23_G3     | 500D 7410h       |
| EPWM24_G0     | 5001 8410h       |
| EPWM24_G1     | 5005 8410h       |
| EPWM24_G2     | 5009 8410h       |
| EPWM24_G3     | 500D 8410h       |
| EPWM25_G0     | 5001 9410h       |
| EPWM25_G1     | 5005 9410h       |
| EPWM25_G2     | 5009 9410h       |
| EPWM25_G3     | 500D 9410h       |
| EPWM26_G0     | 5001 A410h       |
| EPWM26_G1     | 5005 A410h       |
| EPWM26_G2     | 5009 A410h       |
| EPWM26_G3     | 500D A410h       |
| EPWM27_G0     | 5001 B410h       |
| EPWM27_G1     | 5005 B410h       |
| EPWM27_G2     | 5009 B410h       |
| EPWM27_G3     | 500D B410h       |
| EPWM28_G0     | 5001 C410h       |
| EPWM28_G1     | 5005 C410h       |
| EPWM28_G2     | 5009 C410h       |
| EPWM28_G3     | 500D C410h       |
| EPWM29_G0     | 5001 D410h       |
| EPWM29_G1     | 5005 D410h       |
| EPWM29_G2     | 5009 D410h       |
| EPWM29_G3     | 500D D410h       |
| EPWM30_G0     | 5001 E410h       |
| EPWM30_G1     | 5005 E410h       |
| EPWM30_G2     | 5009 E410h       |
| EPWM30_G3     | 500D E410h       |
| EPWM31_G0     | 5001 F410h       |
| EPWM31_G1     | 5005 F410h       |
| EPWM31_G2     | 5009 F410h       |
| EPWM31_G3     | 500D F410h       |



**Figure 3-351. EPWM\_XLOADCTL Name Register**

| 31         | 30         | 29 | 28 | 27                      | 26                  | 25         | 24 |
|------------|------------|----|----|-------------------------|---------------------|------------|----|
| RESERVED_8 | RPTBUF3CNT |    |    | RESERVED_7              | RPTBUF3PRD          |            |    |
| R          | R          |    |    | R                       | R/W                 |            |    |
| 0h         | 0h         |    |    | 0h                      | 0h                  |            |    |
| 23         | 22         | 21 | 20 | 19                      | 18                  | 17         | 16 |
| RESERVED_6 | RPTBUF2CNT |    |    | RESERVED_5              | RPTBUF2PRD          |            |    |
| R          | R          |    |    | R                       | R/W                 |            |    |
| 0h         | 0h         |    |    | 0h                      | 0h                  |            |    |
| 15         | 14         | 13 | 12 | 11                      | 10                  | 9          | 8  |
| RESERVED_4 |            |    |    | SHDWBUFPTR_LOADMULTIPLE | SHDWBUFPTR_LOADONCE |            |    |
| R          |            |    |    | R                       | R/W                 |            |    |
| 0h         |            |    |    | 0h                      | 0h                  |            |    |
| 7          | 6          | 5  | 4  | 3                       | 2                   | 1          | 0  |
| RESERVED_3 | SHDWLEVEL  |    |    | RESERVED_2              | LOADMODE            | RESERVED_1 |    |
| R          | R/W        |    |    | R                       | R/W                 | R          |    |
| 0h         | 0h         |    |    | 0h                      | 0h                  | 0h         |    |

**Table 3-1113. EPWM\_XLOADCTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | RESERVED_8 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 30:28 | RPTBUF3CNT | R    | 0h    | Repeat Count Status Shadow Buffer<br>3: These bits indicate how many times shadow buffer 3 has been be applied before moving to the next buffer, i.e., shadow buffer 2.<br>3'b000 Shadow buffer reset value with STARTLD and copied to Active register<br>3'b001 Shadow buffer applied twice on 2 successive load strobes<br>3'b010 Shadow buffer applied thrice on 3 successive load strobes<br>.<br>.<br>3'b111 Shadow buffer applied 8 times on 8 successive load strobes<br>These bits reset to zero every time STARTLD is initiated.                                                                                                                                    |
| 27    | RESERVED_7 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 26:24 | RPTBUF3PRD | R/W  | 0h    | Repeat Count Shadow Buffer<br>3 : These bits indicate how many times shadow buffer 3 will be applied before moving to the next buffer, i.e., shadow buffer 2.<br>3'b000 Apply shadow buffer once and move to the next shadow buffer on the following load pulse<br>3'b001 Apply shadow buffer twice on 2 successive load strobes and move to the next shadow buffer on the following load pulse<br>3'b010 Apply shadow buffer thrice on 3 successive load strobes and move to the next shadow buffer on the following load pulse<br>.<br>.<br>3'b111 Apply shadow buffer 8 times on 8 successive load strobes and move to the next shadow buffer on the following load pulse |
| 23    | RESERVED_6 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

**Table 3-1113. EPWM\_XLOADCTL Register Field Descriptions (continued)**

| Bit   | Field                   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|-------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 22:20 | RPTBUF2CNT              | R    | 0h    | Repeat Count Status Shadow Buffer<br>2: These bits indicate how many times shadow buffer 2 has been be applied before moving to the next buffer I,e, shadow buffer 1.<br>3'b000 Shadow buffer reset value with STARTLD and copied to Active register<br>3'b001 Shadow buffer applied twice on 2 successive load strobes<br>3'b010 Shadow buffer applied thrice on 3 successive load strobes<br>.<br>.<br>3'b111 Shadow buffer applied 8 times on 8 successive load strobes<br>These bits reset to zero every time STARTLD is initiated.                                                                                                                                       |
| 19    | RESERVED_5              | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 18:16 | RPTBUF2PRD              | R/W  | 0h    | Repeat Count Shadow Buffer<br>2 : These bits indicate how many times shadow buffer 2 will be applied before moving to the next buffer I,e, shadow buffer 1.<br>3'b000 Apply shadow buffer once and move to the next shadow buffer on the following load pulse<br>3'b001 Apply shadow buffer twice on 2 successive load strobes and move to the next shadow buffer on the following load pulse<br>3'b010 Apply shadow buffer thrice on 3 successive load strobes and move to the next shadow buffer on the following load pulse<br>.<br>.<br>2'b12'b11 Apply shadow buffer 8 times on 8 successive load strobes and move to the next shadow buffer on the following load pulse |
| 15:12 | RESERVED_4              | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 11:10 | SHDWBUFPTR_LOADMULTIPLE | R    | 0h    | Register Load event count: These bits indicate the current shadow buffer in use.<br>2'b00 Reset value<br>0,1 1 Shadow buffer 1 in use<br>2'b10 2 Shadow buffer 2 in use<br>2'b11 3 Shadow buffer 3 in use                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 9:8   | SHDWBUFPTR_LOADONCE     | R/W  | 0h    | Register Load event count: These bits indicate the current shadow buffer in use.<br>2'b00 Reset value<br>0,1 1 Shadow buffer 1 in use<br>2'b10 2 Shadow buffer 2 in use<br>2'b11 3 Shadow buffer 3 in use                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 7:6   | RESERVED_3              | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 5:4   | SHDWLEVEL               | R/W  | 0h    | Shadow Register Level Allocation Options: These bits are effective only when XCMPE is enabled.<br>2'b00 : XXXX Shadow level is set at zero. XXXX Active register is available<br>2'b01 : XXXX Shadow level is set at 1. XXXX_SHDW1 and Active registers are available<br>2'b10 : XXXX Shadow level is set at 1. XXXX_SHDW1, XXXX_SHDW2 and Active registers are available<br>2'b11 : XXXX Shadow level is set at 1. XXXX_SHDW1, XXXX_SHDW2, XXXX_SHDW3 and Active registers are available                                                                                                                                                                                     |
| 3     | RESERVED_2              | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

**Table 3-1113. EPWM\_XLOADCTL Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-----|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | LOADMODE   | R/W  | 0h    | Load mode selection for Shadow registers: These bits are effective only when XCMPE is enabled.<br>0 : [LOADONCE] Load occurs at every load strobe [CNT_Zero or FRCLD] from SHDWn Active registers. And STARTLD is cleared after 1 load strobe. SHDWBUFPtr is not automatically decremented in this case. User would set the SHDWBUFPtr for subsequent loads.<br>1 : [LOADMULTIPLE] Load occurs at every load strobe [CNT_Zero or FRCLD] from SHDWnActive registers. And STARTLD is cleared after SHDWLEVEL number of load strobes. SHDWBUFPtr decrements by 1 on a load strobe, until the SHDWBUFPtr reaches 1. |
| 1:0 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

### 3.7.2.101 EPWM\_XLOAD Register

#### 1 EPWM\_XLOAD Register (Offset = 418h) [reset = 0h]

XCMP Mode Load Enable Register.

Return to [Summary Table](#)

**Table 3-1114. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0418h       |
| EPWM0_G1      | 5004 0418h       |
| EPWM0_G2      | 5008 0418h       |
| EPWM0_G3      | 500C 0418h       |
| EPWM1_G0      | 5000 1418h       |
| EPWM1_G1      | 5004 1418h       |
| EPWM1_G2      | 5008 1418h       |
| EPWM1_G3      | 500C 1418h       |
| EPWM2_G0      | 5000 2418h       |
| EPWM2_G1      | 5004 2418h       |
| EPWM2_G2      | 5008 2418h       |
| EPWM2_G3      | 500C 2418h       |
| EPWM3_G0      | 5000 3418h       |
| EPWM3_G1      | 5004 3418h       |
| EPWM3_G2      | 5008 3418h       |
| EPWM3_G3      | 500C 3418h       |
| EPWM4_G0      | 5000 4418h       |
| EPWM4_G1      | 5004 4418h       |
| EPWM4_G2      | 5008 4418h       |
| EPWM4_G3      | 500C 4418h       |
| EPWM5_G0      | 5000 5418h       |
| EPWM5_G1      | 5004 5418h       |
| EPWM5_G2      | 5008 5418h       |
| EPWM5_G3      | 500C 5418h       |
| EPWM6_G0      | 5000 6418h       |
| EPWM6_G1      | 5004 6418h       |
| EPWM6_G2      | 5008 6418h       |
| EPWM6_G3      | 500C 6418h       |
| EPWM7_G0      | 5000 7418h       |
| EPWM7_G1      | 5004 7418h       |
| EPWM7_G2      | 5008 7418h       |
| EPWM7_G3      | 500C 7418h       |
| EPWM8_G0      | 5000 8418h       |
| EPWM8_G1      | 5004 8418h       |
| EPWM8_G2      | 5008 8418h       |
| EPWM8_G3      | 500C 8418h       |
| EPWM9_G0      | 5000 9418h       |
| EPWM9_G1      | 5004 9418h       |
| EPWM9_G2      | 5008 9418h       |

**Table 3-1114. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9418h       |
| EPWM10_G0     | 5000 A418h       |
| EPWM10_G1     | 5004 A418h       |
| EPWM10_G2     | 5008 A418h       |
| EPWM10_G3     | 500C A418h       |
| EPWM11_G0     | 5000 B418h       |
| EPWM11_G1     | 5004 B418h       |
| EPWM11_G2     | 5008 B418h       |
| EPWM11_G3     | 500C B418h       |
| EPWM12_G0     | 5000 C418h       |
| EPWM12_G1     | 5004 C418h       |
| EPWM12_G2     | 5008 C418h       |
| EPWM12_G3     | 500C C418h       |
| EPWM13_G0     | 5000 D418h       |
| EPWM13_G1     | 5004 D418h       |
| EPWM13_G2     | 5008 D418h       |
| EPWM13_G3     | 500C D418h       |
| EPWM14_G0     | 5000 E418h       |
| EPWM14_G1     | 5004 E418h       |
| EPWM14_G2     | 5008 E418h       |
| EPWM14_G3     | 500C E418h       |
| EPWM15_G0     | 5000 F418h       |
| EPWM15_G1     | 5004 F418h       |
| EPWM15_G2     | 5008 F418h       |
| EPWM15_G3     | 500C F418h       |
| EPWM16_G0     | 5001 0418h       |
| EPWM16_G1     | 5005 0418h       |
| EPWM16_G2     | 5009 0418h       |
| EPWM16_G3     | 500D 0418h       |
| EPWM17_G0     | 5001 1418h       |
| EPWM17_G1     | 5005 1418h       |
| EPWM17_G2     | 5009 1418h       |
| EPWM17_G3     | 500D 1418h       |
| EPWM18_G0     | 5001 2418h       |
| EPWM18_G1     | 5005 2418h       |
| EPWM18_G2     | 5009 2418h       |
| EPWM18_G3     | 500D 2418h       |
| EPWM19_G0     | 5001 3418h       |
| EPWM19_G1     | 5005 3418h       |
| EPWM19_G2     | 5009 3418h       |
| EPWM19_G3     | 500D 3418h       |
| EPWM20_G0     | 5001 4418h       |
| EPWM20_G1     | 5005 4418h       |
| EPWM20_G2     | 5009 4418h       |
| EPWM20_G3     | 500D 4418h       |

**Table 3-1114. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5418h       |
| EPWM21_G1     | 5005 5418h       |
| EPWM21_G2     | 5009 5418h       |
| EPWM21_G3     | 500D 5418h       |
| EPWM22_G0     | 5001 6418h       |
| EPWM22_G1     | 5005 6418h       |
| EPWM22_G2     | 5009 6418h       |
| EPWM22_G3     | 500D 6418h       |
| EPWM23_G0     | 5001 7418h       |
| EPWM23_G1     | 5005 7418h       |
| EPWM23_G2     | 5009 7418h       |
| EPWM23_G3     | 500D 7418h       |
| EPWM24_G0     | 5001 8418h       |
| EPWM24_G1     | 5005 8418h       |
| EPWM24_G2     | 5009 8418h       |
| EPWM24_G3     | 500D 8418h       |
| EPWM25_G0     | 5001 9418h       |
| EPWM25_G1     | 5005 9418h       |
| EPWM25_G2     | 5009 9418h       |
| EPWM25_G3     | 500D 9418h       |
| EPWM26_G0     | 5001 A418h       |
| EPWM26_G1     | 5005 A418h       |
| EPWM26_G2     | 5009 A418h       |
| EPWM26_G3     | 500D A418h       |
| EPWM27_G0     | 5001 B418h       |
| EPWM27_G1     | 5005 B418h       |
| EPWM27_G2     | 5009 B418h       |
| EPWM27_G3     | 500D B418h       |
| EPWM28_G0     | 5001 C418h       |
| EPWM28_G1     | 5005 C418h       |
| EPWM28_G2     | 5009 C418h       |
| EPWM28_G3     | 500D C418h       |
| EPWM29_G0     | 5001 D418h       |
| EPWM29_G1     | 5005 D418h       |
| EPWM29_G2     | 5009 D418h       |
| EPWM29_G3     | 500D D418h       |
| EPWM30_G0     | 5001 E418h       |
| EPWM30_G1     | 5005 E418h       |
| EPWM30_G2     | 5009 E418h       |
| EPWM30_G3     | 500D E418h       |
| EPWM31_G0     | 5001 F418h       |
| EPWM31_G1     | 5005 F418h       |
| EPWM31_G2     | 5009 F418h       |
| EPWM31_G3     | 500D F418h       |

**Figure 3-352. EPWM\_XLOAD Name Register**

|            |    |    |    |    |    |        |         |
|------------|----|----|----|----|----|--------|---------|
| 31         | 30 | 29 | 28 | 27 | 26 | 25     | 24      |
| RESERVED_1 |    |    |    |    |    |        |         |
| R          |    |    |    |    |    |        |         |
| 0h         |    |    |    |    |    |        |         |
| 23         | 22 | 21 | 20 | 19 | 18 | 17     | 16      |
| RESERVED_1 |    |    |    |    |    |        |         |
| R          |    |    |    |    |    |        |         |
| 0h         |    |    |    |    |    |        |         |
| 15         | 14 | 13 | 12 | 11 | 10 | 9      | 8       |
| RESERVED_1 |    |    |    |    |    |        |         |
| R          |    |    |    |    |    |        |         |
| 0h         |    |    |    |    |    |        |         |
| 7          | 6  | 5  | 4  | 3  | 2  | 1      | 0       |
| RESERVED_1 |    |    |    |    |    | FRCLD  | STARTLD |
| R          |    |    |    |    |    | R/W1TS | R/W1TS  |
| 0h         |    |    |    |    |    | 0h     | 0h      |

**Table 3-1116. EPWM\_XLOAD Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                               |
|------|------------|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                  |
| 1    | FRCLD      | R/W1TS | 0h    | Force reload event in one shot mode :<br>Writing a 1 to this bit turn force one load event at the input of the event pre-scale counter as shown in the diagram below. This bit is intended to be used for testing and/or software force loading of the events in global load mode.<br>Writing of 0 will be ignored.<br>Always reads back a 0.                             |
| 0    | STARTLD    | R/W1TS | 0h    | Enable reload event :<br>Writing a 1 to this bit turn the one shot latch condition ON. Upon occurrence of a chosen load strobe, one shadow to active reload occurs and the latch will be cleared. Hence Writing "1" to this bit would allow load strobe event to pass through and block further strobe events.<br>Writing of 0 will be ignored.<br>Always reads back a 0. |

### 3.7.2.102 EPWM\_EPWMXLINKXLOAD Register

#### 1 EPWM\_EPWMXLINKXLOAD Register (Offset = 41Ch) [reset = 0h]

Link register across PWM modules.

Return to [Summary Table](#)

**Table 3-1117. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 041Ch       |
| EPWM0_G1      | 5004 041Ch       |
| EPWM0_G2      | 5008 041Ch       |
| EPWM0_G3      | 500C 041Ch       |
| EPWM1_G0      | 5000 141Ch       |
| EPWM1_G1      | 5004 141Ch       |
| EPWM1_G2      | 5008 141Ch       |
| EPWM1_G3      | 500C 141Ch       |
| EPWM2_G0      | 5000 241Ch       |
| EPWM2_G1      | 5004 241Ch       |
| EPWM2_G2      | 5008 241Ch       |
| EPWM2_G3      | 500C 241Ch       |
| EPWM3_G0      | 5000 341Ch       |
| EPWM3_G1      | 5004 341Ch       |
| EPWM3_G2      | 5008 341Ch       |
| EPWM3_G3      | 500C 341Ch       |
| EPWM4_G0      | 5000 441Ch       |
| EPWM4_G1      | 5004 441Ch       |
| EPWM4_G2      | 5008 441Ch       |
| EPWM4_G3      | 500C 441Ch       |
| EPWM5_G0      | 5000 541Ch       |
| EPWM5_G1      | 5004 541Ch       |
| EPWM5_G2      | 5008 541Ch       |
| EPWM5_G3      | 500C 541Ch       |
| EPWM6_G0      | 5000 641Ch       |
| EPWM6_G1      | 5004 641Ch       |
| EPWM6_G2      | 5008 641Ch       |
| EPWM6_G3      | 500C 641Ch       |
| EPWM7_G0      | 5000 741Ch       |
| EPWM7_G1      | 5004 741Ch       |
| EPWM7_G2      | 5008 741Ch       |
| EPWM7_G3      | 500C 741Ch       |
| EPWM8_G0      | 5000 841Ch       |
| EPWM8_G1      | 5004 841Ch       |
| EPWM8_G2      | 5008 841Ch       |
| EPWM8_G3      | 500C 841Ch       |
| EPWM9_G0      | 5000 941Ch       |
| EPWM9_G1      | 5004 941Ch       |
| EPWM9_G2      | 5008 941Ch       |



**Table 3-1117. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 941Ch       |
| EPWM10_G0     | 5000 A41Ch       |
| EPWM10_G1     | 5004 A41Ch       |
| EPWM10_G2     | 5008 A41Ch       |
| EPWM10_G3     | 500C A41Ch       |
| EPWM11_G0     | 5000 B41Ch       |
| EPWM11_G1     | 5004 B41Ch       |
| EPWM11_G2     | 5008 B41Ch       |
| EPWM11_G3     | 500C B41Ch       |
| EPWM12_G0     | 5000 C41Ch       |
| EPWM12_G1     | 5004 C41Ch       |
| EPWM12_G2     | 5008 C41Ch       |
| EPWM12_G3     | 500C C41Ch       |
| EPWM13_G0     | 5000 D41Ch       |
| EPWM13_G1     | 5004 D41Ch       |
| EPWM13_G2     | 5008 D41Ch       |
| EPWM13_G3     | 500C D41Ch       |
| EPWM14_G0     | 5000 E41Ch       |
| EPWM14_G1     | 5004 E41Ch       |
| EPWM14_G2     | 5008 E41Ch       |
| EPWM14_G3     | 500C E41Ch       |
| EPWM15_G0     | 5000 F41Ch       |
| EPWM15_G1     | 5004 F41Ch       |
| EPWM15_G2     | 5008 F41Ch       |
| EPWM15_G3     | 500C F41Ch       |
| EPWM16_G0     | 5001 041Ch       |
| EPWM16_G1     | 5005 041Ch       |
| EPWM16_G2     | 5009 041Ch       |
| EPWM16_G3     | 500D 041Ch       |
| EPWM17_G0     | 5001 141Ch       |
| EPWM17_G1     | 5005 141Ch       |
| EPWM17_G2     | 5009 141Ch       |
| EPWM17_G3     | 500D 141Ch       |
| EPWM18_G0     | 5001 241Ch       |
| EPWM18_G1     | 5005 241Ch       |
| EPWM18_G2     | 5009 241Ch       |
| EPWM18_G3     | 500D 241Ch       |
| EPWM19_G0     | 5001 341Ch       |
| EPWM19_G1     | 5005 341Ch       |
| EPWM19_G2     | 5009 341Ch       |
| EPWM19_G3     | 500D 341Ch       |
| EPWM20_G0     | 5001 441Ch       |
| EPWM20_G1     | 5005 441Ch       |
| EPWM20_G2     | 5009 441Ch       |
| EPWM20_G3     | 500D 441Ch       |

**Table 3-1117. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 541Ch       |
| EPWM21_G1     | 5005 541Ch       |
| EPWM21_G2     | 5009 541Ch       |
| EPWM21_G3     | 500D 541Ch       |
| EPWM22_G0     | 5001 641Ch       |
| EPWM22_G1     | 5005 641Ch       |
| EPWM22_G2     | 5009 641Ch       |
| EPWM22_G3     | 500D 641Ch       |
| EPWM23_G0     | 5001 741Ch       |
| EPWM23_G1     | 5005 741Ch       |
| EPWM23_G2     | 5009 741Ch       |
| EPWM23_G3     | 500D 741Ch       |
| EPWM24_G0     | 5001 841Ch       |
| EPWM24_G1     | 5005 841Ch       |
| EPWM24_G2     | 5009 841Ch       |
| EPWM24_G3     | 500D 841Ch       |
| EPWM25_G0     | 5001 941Ch       |
| EPWM25_G1     | 5005 941Ch       |
| EPWM25_G2     | 5009 941Ch       |
| EPWM25_G3     | 500D 941Ch       |
| EPWM26_G0     | 5001 A41Ch       |
| EPWM26_G1     | 5005 A41Ch       |
| EPWM26_G2     | 5009 A41Ch       |
| EPWM26_G3     | 500D A41Ch       |
| EPWM27_G0     | 5001 B41Ch       |
| EPWM27_G1     | 5005 B41Ch       |
| EPWM27_G2     | 5009 B41Ch       |
| EPWM27_G3     | 500D B41Ch       |
| EPWM28_G0     | 5001 C41Ch       |
| EPWM28_G1     | 5005 C41Ch       |
| EPWM28_G2     | 5009 C41Ch       |
| EPWM28_G3     | 500D C41Ch       |
| EPWM29_G0     | 5001 D41Ch       |
| EPWM29_G1     | 5005 D41Ch       |
| EPWM29_G2     | 5009 D41Ch       |
| EPWM29_G3     | 500D D41Ch       |
| EPWM30_G0     | 5001 E41Ch       |
| EPWM30_G1     | 5005 E41Ch       |
| EPWM30_G2     | 5009 E41Ch       |
| EPWM30_G3     | 500D E41Ch       |
| EPWM31_G0     | 5001 F41Ch       |
| EPWM31_G1     | 5005 F41Ch       |
| EPWM31_G2     | 5009 F41Ch       |
| EPWM31_G3     | 500D F41Ch       |

**Figure 3-353. EPWM\_EPWMXLINKXLOAD Name Register**

|            |    |    |    |           |    |    |    |
|------------|----|----|----|-----------|----|----|----|
| 31         | 30 | 29 | 28 | 27        | 26 | 25 | 24 |
| RESERVED_1 |    |    |    |           |    |    |    |
| R          |    |    |    |           |    |    |    |
| 0h         |    |    |    |           |    |    |    |
| 23         | 22 | 21 | 20 | 19        | 18 | 17 | 16 |
| RESERVED_1 |    |    |    |           |    |    |    |
| R          |    |    |    |           |    |    |    |
| 0h         |    |    |    |           |    |    |    |
| 15         | 14 | 13 | 12 | 11        | 10 | 9  | 8  |
| RESERVED_1 |    |    |    |           |    |    |    |
| R          |    |    |    |           |    |    |    |
| 0h         |    |    |    |           |    |    |    |
| 7          | 6  | 5  | 4  | 3         | 2  | 1  | 0  |
| RESERVED_1 |    |    |    | XLOADLINK |    |    |    |
| R          |    |    |    | R/W       |    |    |    |
| 0h         |    |    |    | 0h        |    |    |    |

**Table 3-1119. EPWM\_EPWMXLINKXLOAD Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:5 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 4:0  | XLOADLINK  | R/W  | 0h    | <p>XLOAD Link Bits:</p> <p>Writes to the XLOAD registers in the EPWM module selected by the following bit selections results in a simultaneous write to the current EPWM module's XLOAD registers</p> <p>5'b00000: EPWM0</p> <p>5'b00001: EPWM1</p> <p>5'b00010: EPWM2</p> <p>5'b00011: EPWM3</p> <p>5'b00100: EPWM4</p> <p>5'b00101: EPWM5</p> <p>5'b00110: EPWM6</p> <p>5'b00111: EPWM7</p> <p>5'b01000: EPWM8</p> <p>5'b01001: EPWM9</p> <p>5'b01010: EPWM10</p> <p>5'b01011: EPWM11</p> <p>5'b01100: EPWM12</p> <p>...</p> <p>5'b11111: EPWM31</p> |

### 3.7.2.103 EPWM\_XREGSHDW1STS Register

#### 1 EPWM\_XREGSHDW1STS Register (Offset = 420h) [reset = 0h]

Shadow Buffer 1 Update Status Register.

Return to [Summary Table](#)

**Table 3-1120. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0420h       |
| EPWM0_G1      | 5004 0420h       |
| EPWM0_G2      | 5008 0420h       |
| EPWM0_G3      | 500C 0420h       |
| EPWM1_G0      | 5000 1420h       |
| EPWM1_G1      | 5004 1420h       |
| EPWM1_G2      | 5008 1420h       |
| EPWM1_G3      | 500C 1420h       |
| EPWM2_G0      | 5000 2420h       |
| EPWM2_G1      | 5004 2420h       |
| EPWM2_G2      | 5008 2420h       |
| EPWM2_G3      | 500C 2420h       |
| EPWM3_G0      | 5000 3420h       |
| EPWM3_G1      | 5004 3420h       |
| EPWM3_G2      | 5008 3420h       |
| EPWM3_G3      | 500C 3420h       |
| EPWM4_G0      | 5000 4420h       |
| EPWM4_G1      | 5004 4420h       |
| EPWM4_G2      | 5008 4420h       |
| EPWM4_G3      | 500C 4420h       |
| EPWM5_G0      | 5000 5420h       |
| EPWM5_G1      | 5004 5420h       |
| EPWM5_G2      | 5008 5420h       |
| EPWM5_G3      | 500C 5420h       |
| EPWM6_G0      | 5000 6420h       |
| EPWM6_G1      | 5004 6420h       |
| EPWM6_G2      | 5008 6420h       |
| EPWM6_G3      | 500C 6420h       |
| EPWM7_G0      | 5000 7420h       |
| EPWM7_G1      | 5004 7420h       |
| EPWM7_G2      | 5008 7420h       |
| EPWM7_G3      | 500C 7420h       |
| EPWM8_G0      | 5000 8420h       |
| EPWM8_G1      | 5004 8420h       |
| EPWM8_G2      | 5008 8420h       |
| EPWM8_G3      | 500C 8420h       |
| EPWM9_G0      | 5000 9420h       |
| EPWM9_G1      | 5004 9420h       |
| EPWM9_G2      | 5008 9420h       |

**Table 3-1120. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9420h       |
| EPWM10_G0     | 5000 A420h       |
| EPWM10_G1     | 5004 A420h       |
| EPWM10_G2     | 5008 A420h       |
| EPWM10_G3     | 500C A420h       |
| EPWM11_G0     | 5000 B420h       |
| EPWM11_G1     | 5004 B420h       |
| EPWM11_G2     | 5008 B420h       |
| EPWM11_G3     | 500C B420h       |
| EPWM12_G0     | 5000 C420h       |
| EPWM12_G1     | 5004 C420h       |
| EPWM12_G2     | 5008 C420h       |
| EPWM12_G3     | 500C C420h       |
| EPWM13_G0     | 5000 D420h       |
| EPWM13_G1     | 5004 D420h       |
| EPWM13_G2     | 5008 D420h       |
| EPWM13_G3     | 500C D420h       |
| EPWM14_G0     | 5000 E420h       |
| EPWM14_G1     | 5004 E420h       |
| EPWM14_G2     | 5008 E420h       |
| EPWM14_G3     | 500C E420h       |
| EPWM15_G0     | 5000 F420h       |
| EPWM15_G1     | 5004 F420h       |
| EPWM15_G2     | 5008 F420h       |
| EPWM15_G3     | 500C F420h       |
| EPWM16_G0     | 5001 0420h       |
| EPWM16_G1     | 5005 0420h       |
| EPWM16_G2     | 5009 0420h       |
| EPWM16_G3     | 500D 0420h       |
| EPWM17_G0     | 5001 1420h       |
| EPWM17_G1     | 5005 1420h       |
| EPWM17_G2     | 5009 1420h       |
| EPWM17_G3     | 500D 1420h       |
| EPWM18_G0     | 5001 2420h       |
| EPWM18_G1     | 5005 2420h       |
| EPWM18_G2     | 5009 2420h       |
| EPWM18_G3     | 500D 2420h       |
| EPWM19_G0     | 5001 3420h       |
| EPWM19_G1     | 5005 3420h       |
| EPWM19_G2     | 5009 3420h       |
| EPWM19_G3     | 500D 3420h       |
| EPWM20_G0     | 5001 4420h       |
| EPWM20_G1     | 5005 4420h       |
| EPWM20_G2     | 5009 4420h       |
| EPWM20_G3     | 500D 4420h       |

**Table 3-1120. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5420h       |
| EPWM21_G1     | 5005 5420h       |
| EPWM21_G2     | 5009 5420h       |
| EPWM21_G3     | 500D 5420h       |
| EPWM22_G0     | 5001 6420h       |
| EPWM22_G1     | 5005 6420h       |
| EPWM22_G2     | 5009 6420h       |
| EPWM22_G3     | 500D 6420h       |
| EPWM23_G0     | 5001 7420h       |
| EPWM23_G1     | 5005 7420h       |
| EPWM23_G2     | 5009 7420h       |
| EPWM23_G3     | 500D 7420h       |
| EPWM24_G0     | 5001 8420h       |
| EPWM24_G1     | 5005 8420h       |
| EPWM24_G2     | 5009 8420h       |
| EPWM24_G3     | 500D 8420h       |
| EPWM25_G0     | 5001 9420h       |
| EPWM25_G1     | 5005 9420h       |
| EPWM25_G2     | 5009 9420h       |
| EPWM25_G3     | 500D 9420h       |
| EPWM26_G0     | 5001 A420h       |
| EPWM26_G1     | 5005 A420h       |
| EPWM26_G2     | 5009 A420h       |
| EPWM26_G3     | 500D A420h       |
| EPWM27_G0     | 5001 B420h       |
| EPWM27_G1     | 5005 B420h       |
| EPWM27_G2     | 5009 B420h       |
| EPWM27_G3     | 500D B420h       |
| EPWM28_G0     | 5001 C420h       |
| EPWM28_G1     | 5005 C420h       |
| EPWM28_G2     | 5009 C420h       |
| EPWM28_G3     | 500D C420h       |
| EPWM29_G0     | 5001 D420h       |
| EPWM29_G1     | 5005 D420h       |
| EPWM29_G2     | 5009 D420h       |
| EPWM29_G3     | 500D D420h       |
| EPWM30_G0     | 5001 E420h       |
| EPWM30_G1     | 5005 E420h       |
| EPWM30_G2     | 5009 E420h       |
| EPWM30_G3     | 500D E420h       |
| EPWM31_G0     | 5001 F420h       |
| EPWM31_G1     | 5005 F420h       |
| EPWM31_G2     | 5009 F420h       |
| EPWM31_G3     | 500D F420h       |

**Figure 3-354. EPWM\_XREGSHDW1STS Name Register**

|                 |                 |                 |                   |                   |                 |                 |                  |
|-----------------|-----------------|-----------------|-------------------|-------------------|-----------------|-----------------|------------------|
| 31              | 30              | 29              | 28                | 27                | 26              | 25              | 24               |
| RESERVED_1      |                 |                 |                   |                   |                 |                 |                  |
| R               |                 |                 |                   |                   |                 |                 |                  |
| 0h              |                 |                 |                   |                   |                 |                 |                  |
| 23              | 22              | 21              | 20                | 19                | 18              | 17              | 16               |
| RESERVED_1      |                 |                 |                   |                   |                 |                 |                  |
| R               |                 |                 |                   |                   |                 |                 |                  |
| 0h              |                 |                 |                   |                   |                 |                 |                  |
| 15              | 14              | 13              | 12                | 11                | 10              | 9               | 8                |
| RESERVED_1      | XMIN_SHDW1FULL  | XMAX_SHDW1FULL  | XAQCTLB_SHDW1FULL | XAQCTLA_SHDW1FULL | CMPD_SHDW1FULL  | CMPC_SHDW1FULL  | XTBPRD_SHDW1FULL |
| R               | R               | R               | R                 | R                 | R               | R               | R                |
| 0h              | 0h              | 0h              | 0h                | 0h                | 0h              | 0h              | 0h               |
| 7               | 6               | 5               | 4                 | 3                 | 2               | 1               | 0                |
| XCMP8_SHDW1FULL | XCMP7_SHDW1FULL | XCMP6_SHDW1FULL | XCMP5_SHDW1FULL   | XCMP4_SHDW1FULL   | XCMP3_SHDW1FULL | XCMP2_SHDW1FULL | XCMP1_SHDW1FULL  |
| R               | R               | R               | R                 | R                 | R               | R               | R                |
| 0h              | 0h              | 0h              | 0h                | 0h                | 0h              | 0h              | 0h               |

**Table 3-1122. EPWM\_XREGSHDW1STS Register Field Descriptions**

| Bit   | Field             | Type | Reset | Description                                                                                                                    |
|-------|-------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------|
| 31:15 | RESERVED_1        | R    | 0h    | Reserved                                                                                                                       |
| 14    | XMIN_SHDW1FULL    | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 13    | XMAX_SHDW1FULL    | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 12    | XAQCTLB_SHDW1FULL | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 11    | XAQCTLA_SHDW1FULL | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 10    | CMPD_SHDW1FULL    | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 9     | CMPC_SHDW1FULL    | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 8     | XTBPRD_SHDW1FULL  | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 7     | XCMP8_SHDW1FULL   | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 6     | XCMP7_SHDW1FULL   | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 5     | XCMP6_SHDW1FULL   | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |

**Table 3-1122. EPWM\_XREGSHDW1STS Register Field Descriptions (continued)**

| Bit | Field           | Type | Reset | Description                                                                                                                    |
|-----|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------|
| 4   | XCMP5_SHDW1FULL | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 3   | XCMP4_SHDW1FULL | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 2   | XCMP3_SHDW1FULL | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 1   | XCMP2_SHDW1FULL | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 0   | XCMP1_SHDW1FULL | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |



### 3.7.2.104 EPWM\_XREGSHDW2STS Register

#### 1 EPWM\_XREGSHDW2STS Register (Offset = 428h) [reset = 0h]

Shadow Buffer 2 Update Status Register.

Return to [Summary Table](#)

**Table 3-1123. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0428h       |
| EPWM0_G1      | 5004 0428h       |
| EPWM0_G2      | 5008 0428h       |
| EPWM0_G3      | 500C 0428h       |
| EPWM1_G0      | 5000 1428h       |
| EPWM1_G1      | 5004 1428h       |
| EPWM1_G2      | 5008 1428h       |
| EPWM1_G3      | 500C 1428h       |
| EPWM2_G0      | 5000 2428h       |
| EPWM2_G1      | 5004 2428h       |
| EPWM2_G2      | 5008 2428h       |
| EPWM2_G3      | 500C 2428h       |
| EPWM3_G0      | 5000 3428h       |
| EPWM3_G1      | 5004 3428h       |
| EPWM3_G2      | 5008 3428h       |
| EPWM3_G3      | 500C 3428h       |
| EPWM4_G0      | 5000 4428h       |
| EPWM4_G1      | 5004 4428h       |
| EPWM4_G2      | 5008 4428h       |
| EPWM4_G3      | 500C 4428h       |
| EPWM5_G0      | 5000 5428h       |
| EPWM5_G1      | 5004 5428h       |
| EPWM5_G2      | 5008 5428h       |
| EPWM5_G3      | 500C 5428h       |
| EPWM6_G0      | 5000 6428h       |
| EPWM6_G1      | 5004 6428h       |
| EPWM6_G2      | 5008 6428h       |
| EPWM6_G3      | 500C 6428h       |
| EPWM7_G0      | 5000 7428h       |
| EPWM7_G1      | 5004 7428h       |
| EPWM7_G2      | 5008 7428h       |
| EPWM7_G3      | 500C 7428h       |
| EPWM8_G0      | 5000 8428h       |
| EPWM8_G1      | 5004 8428h       |
| EPWM8_G2      | 5008 8428h       |
| EPWM8_G3      | 500C 8428h       |
| EPWM9_G0      | 5000 9428h       |
| EPWM9_G1      | 5004 9428h       |
| EPWM9_G2      | 5008 9428h       |

**Table 3-1123. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9428h       |
| EPWM10_G0     | 5000 A428h       |
| EPWM10_G1     | 5004 A428h       |
| EPWM10_G2     | 5008 A428h       |
| EPWM10_G3     | 500C A428h       |
| EPWM11_G0     | 5000 B428h       |
| EPWM11_G1     | 5004 B428h       |
| EPWM11_G2     | 5008 B428h       |
| EPWM11_G3     | 500C B428h       |
| EPWM12_G0     | 5000 C428h       |
| EPWM12_G1     | 5004 C428h       |
| EPWM12_G2     | 5008 C428h       |
| EPWM12_G3     | 500C C428h       |
| EPWM13_G0     | 5000 D428h       |
| EPWM13_G1     | 5004 D428h       |
| EPWM13_G2     | 5008 D428h       |
| EPWM13_G3     | 500C D428h       |
| EPWM14_G0     | 5000 E428h       |
| EPWM14_G1     | 5004 E428h       |
| EPWM14_G2     | 5008 E428h       |
| EPWM14_G3     | 500C E428h       |
| EPWM15_G0     | 5000 F428h       |
| EPWM15_G1     | 5004 F428h       |
| EPWM15_G2     | 5008 F428h       |
| EPWM15_G3     | 500C F428h       |
| EPWM16_G0     | 5001 0428h       |
| EPWM16_G1     | 5005 0428h       |
| EPWM16_G2     | 5009 0428h       |
| EPWM16_G3     | 500D 0428h       |
| EPWM17_G0     | 5001 1428h       |
| EPWM17_G1     | 5005 1428h       |
| EPWM17_G2     | 5009 1428h       |
| EPWM17_G3     | 500D 1428h       |
| EPWM18_G0     | 5001 2428h       |
| EPWM18_G1     | 5005 2428h       |
| EPWM18_G2     | 5009 2428h       |
| EPWM18_G3     | 500D 2428h       |
| EPWM19_G0     | 5001 3428h       |
| EPWM19_G1     | 5005 3428h       |
| EPWM19_G2     | 5009 3428h       |
| EPWM19_G3     | 500D 3428h       |
| EPWM20_G0     | 5001 4428h       |
| EPWM20_G1     | 5005 4428h       |
| EPWM20_G2     | 5009 4428h       |
| EPWM20_G3     | 500D 4428h       |

**Table 3-1123. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5428h       |
| EPWM21_G1     | 5005 5428h       |
| EPWM21_G2     | 5009 5428h       |
| EPWM21_G3     | 500D 5428h       |
| EPWM22_G0     | 5001 6428h       |
| EPWM22_G1     | 5005 6428h       |
| EPWM22_G2     | 5009 6428h       |
| EPWM22_G3     | 500D 6428h       |
| EPWM23_G0     | 5001 7428h       |
| EPWM23_G1     | 5005 7428h       |
| EPWM23_G2     | 5009 7428h       |
| EPWM23_G3     | 500D 7428h       |
| EPWM24_G0     | 5001 8428h       |
| EPWM24_G1     | 5005 8428h       |
| EPWM24_G2     | 5009 8428h       |
| EPWM24_G3     | 500D 8428h       |
| EPWM25_G0     | 5001 9428h       |
| EPWM25_G1     | 5005 9428h       |
| EPWM25_G2     | 5009 9428h       |
| EPWM25_G3     | 500D 9428h       |
| EPWM26_G0     | 5001 A428h       |
| EPWM26_G1     | 5005 A428h       |
| EPWM26_G2     | 5009 A428h       |
| EPWM26_G3     | 500D A428h       |
| EPWM27_G0     | 5001 B428h       |
| EPWM27_G1     | 5005 B428h       |
| EPWM27_G2     | 5009 B428h       |
| EPWM27_G3     | 500D B428h       |
| EPWM28_G0     | 5001 C428h       |
| EPWM28_G1     | 5005 C428h       |
| EPWM28_G2     | 5009 C428h       |
| EPWM28_G3     | 500D C428h       |
| EPWM29_G0     | 5001 D428h       |
| EPWM29_G1     | 5005 D428h       |
| EPWM29_G2     | 5009 D428h       |
| EPWM29_G3     | 500D D428h       |
| EPWM30_G0     | 5001 E428h       |
| EPWM30_G1     | 5005 E428h       |
| EPWM30_G2     | 5009 E428h       |
| EPWM30_G3     | 500D E428h       |
| EPWM31_G0     | 5001 F428h       |
| EPWM31_G1     | 5005 F428h       |
| EPWM31_G2     | 5009 F428h       |
| EPWM31_G3     | 500D F428h       |

**Figure 3-355. EPWM\_XREGSHDW2STS Name Register**

|                 |                 |                 |                   |                   |                 |                 |                  |
|-----------------|-----------------|-----------------|-------------------|-------------------|-----------------|-----------------|------------------|
| 31              | 30              | 29              | 28                | 27                | 26              | 25              | 24               |
| RESERVED_1      |                 |                 |                   |                   |                 |                 |                  |
| R               |                 |                 |                   |                   |                 |                 |                  |
| 0h              |                 |                 |                   |                   |                 |                 |                  |
| 23              | 22              | 21              | 20                | 19                | 18              | 17              | 16               |
| RESERVED_1      |                 |                 |                   |                   |                 |                 |                  |
| R               |                 |                 |                   |                   |                 |                 |                  |
| 0h              |                 |                 |                   |                   |                 |                 |                  |
| 15              | 14              | 13              | 12                | 11                | 10              | 9               | 8                |
| RESERVED_1      | XMIN_SHDW2FULL  | XMAX_SHDW2FULL  | XAQCTLB_SHDW2FULL | XAQCTLA_SHDW2FULL | CMPD_SHDW2FULL  | CMPC_SHDW2FULL  | XTBPRD_SHDW2FULL |
| R               | R               | R               | R                 | R                 | R               | R               | R                |
| 0h              | 0h              | 0h              | 0h                | 0h                | 0h              | 0h              | 0h               |
| 7               | 6               | 5               | 4                 | 3                 | 2               | 1               | 0                |
| XCMP8_SHDW2FULL | XCMP7_SHDW2FULL | XCMP6_SHDW2FULL | XCMP5_SHDW2FULL   | XCMP4_SHDW2FULL   | XCMP3_SHDW2FULL | XCMP2_SHDW2FULL | XCMP1_SHDW2FULL  |
| R               | R               | R               | R                 | R                 | R               | R               | R                |
| 0h              | 0h              | 0h              | 0h                | 0h                | 0h              | 0h              | 0h               |

**Table 3-1125. EPWM\_XREGSHDW2STS Register Field Descriptions**

| Bit   | Field             | Type | Reset | Description                                                                                                                    |
|-------|-------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------|
| 31:15 | RESERVED_1        | R    | 0h    | Reserved                                                                                                                       |
| 14    | XMIN_SHDW2FULL    | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 13    | XMAX_SHDW2FULL    | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 12    | XAQCTLB_SHDW2FULL | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 11    | XAQCTLA_SHDW2FULL | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 10    | CMPD_SHDW2FULL    | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 9     | CMPC_SHDW2FULL    | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 8     | XTBPRD_SHDW2FULL  | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 7     | XCMP8_SHDW2FULL   | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 6     | XCMP7_SHDW2FULL   | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 5     | XCMP6_SHDW2FULL   | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |

**Table 3-1125. EPWM\_XREGSHDW2STS Register Field Descriptions (continued)**

| Bit | Field           | Type | Reset | Description                                                                                                                    |
|-----|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------|
| 4   | XCMP5_SHDW2FULL | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 3   | XCMP4_SHDW2FULL | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 2   | XCMP3_SHDW2FULL | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 1   | XCMP2_SHDW2FULL | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 0   | XCMP1_SHDW2FULL | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |

### 3.7.2.105 EPWM\_XREGSHDW3STS Register

#### 1 EPWM\_XREGSHDW3STS Register (Offset = 430h) [reset = 0h]

Shadow Buffer 3 Update Status Register.

Return to [Summary Table](#)

**Table 3-1126. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0430h       |
| EPWM0_G1      | 5004 0430h       |
| EPWM0_G2      | 5008 0430h       |
| EPWM0_G3      | 500C 0430h       |
| EPWM1_G0      | 5000 1430h       |
| EPWM1_G1      | 5004 1430h       |
| EPWM1_G2      | 5008 1430h       |
| EPWM1_G3      | 500C 1430h       |
| EPWM2_G0      | 5000 2430h       |
| EPWM2_G1      | 5004 2430h       |
| EPWM2_G2      | 5008 2430h       |
| EPWM2_G3      | 500C 2430h       |
| EPWM3_G0      | 5000 3430h       |
| EPWM3_G1      | 5004 3430h       |
| EPWM3_G2      | 5008 3430h       |
| EPWM3_G3      | 500C 3430h       |
| EPWM4_G0      | 5000 4430h       |
| EPWM4_G1      | 5004 4430h       |
| EPWM4_G2      | 5008 4430h       |
| EPWM4_G3      | 500C 4430h       |
| EPWM5_G0      | 5000 5430h       |
| EPWM5_G1      | 5004 5430h       |
| EPWM5_G2      | 5008 5430h       |
| EPWM5_G3      | 500C 5430h       |
| EPWM6_G0      | 5000 6430h       |
| EPWM6_G1      | 5004 6430h       |
| EPWM6_G2      | 5008 6430h       |
| EPWM6_G3      | 500C 6430h       |
| EPWM7_G0      | 5000 7430h       |
| EPWM7_G1      | 5004 7430h       |
| EPWM7_G2      | 5008 7430h       |
| EPWM7_G3      | 500C 7430h       |
| EPWM8_G0      | 5000 8430h       |
| EPWM8_G1      | 5004 8430h       |
| EPWM8_G2      | 5008 8430h       |
| EPWM8_G3      | 500C 8430h       |
| EPWM9_G0      | 5000 9430h       |
| EPWM9_G1      | 5004 9430h       |
| EPWM9_G2      | 5008 9430h       |

**Table 3-1126. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9430h       |
| EPWM10_G0     | 5000 A430h       |
| EPWM10_G1     | 5004 A430h       |
| EPWM10_G2     | 5008 A430h       |
| EPWM10_G3     | 500C A430h       |
| EPWM11_G0     | 5000 B430h       |
| EPWM11_G1     | 5004 B430h       |
| EPWM11_G2     | 5008 B430h       |
| EPWM11_G3     | 500C B430h       |
| EPWM12_G0     | 5000 C430h       |
| EPWM12_G1     | 5004 C430h       |
| EPWM12_G2     | 5008 C430h       |
| EPWM12_G3     | 500C C430h       |
| EPWM13_G0     | 5000 D430h       |
| EPWM13_G1     | 5004 D430h       |
| EPWM13_G2     | 5008 D430h       |
| EPWM13_G3     | 500C D430h       |
| EPWM14_G0     | 5000 E430h       |
| EPWM14_G1     | 5004 E430h       |
| EPWM14_G2     | 5008 E430h       |
| EPWM14_G3     | 500C E430h       |
| EPWM15_G0     | 5000 F430h       |
| EPWM15_G1     | 5004 F430h       |
| EPWM15_G2     | 5008 F430h       |
| EPWM15_G3     | 500C F430h       |
| EPWM16_G0     | 5001 0430h       |
| EPWM16_G1     | 5005 0430h       |
| EPWM16_G2     | 5009 0430h       |
| EPWM16_G3     | 500D 0430h       |
| EPWM17_G0     | 5001 1430h       |
| EPWM17_G1     | 5005 1430h       |
| EPWM17_G2     | 5009 1430h       |
| EPWM17_G3     | 500D 1430h       |
| EPWM18_G0     | 5001 2430h       |
| EPWM18_G1     | 5005 2430h       |
| EPWM18_G2     | 5009 2430h       |
| EPWM18_G3     | 500D 2430h       |
| EPWM19_G0     | 5001 3430h       |
| EPWM19_G1     | 5005 3430h       |
| EPWM19_G2     | 5009 3430h       |
| EPWM19_G3     | 500D 3430h       |
| EPWM20_G0     | 5001 4430h       |
| EPWM20_G1     | 5005 4430h       |
| EPWM20_G2     | 5009 4430h       |
| EPWM20_G3     | 500D 4430h       |

**Table 3-1126. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5430h       |
| EPWM21_G1     | 5005 5430h       |
| EPWM21_G2     | 5009 5430h       |
| EPWM21_G3     | 500D 5430h       |
| EPWM22_G0     | 5001 6430h       |
| EPWM22_G1     | 5005 6430h       |
| EPWM22_G2     | 5009 6430h       |
| EPWM22_G3     | 500D 6430h       |
| EPWM23_G0     | 5001 7430h       |
| EPWM23_G1     | 5005 7430h       |
| EPWM23_G2     | 5009 7430h       |
| EPWM23_G3     | 500D 7430h       |
| EPWM24_G0     | 5001 8430h       |
| EPWM24_G1     | 5005 8430h       |
| EPWM24_G2     | 5009 8430h       |
| EPWM24_G3     | 500D 8430h       |
| EPWM25_G0     | 5001 9430h       |
| EPWM25_G1     | 5005 9430h       |
| EPWM25_G2     | 5009 9430h       |
| EPWM25_G3     | 500D 9430h       |
| EPWM26_G0     | 5001 A430h       |
| EPWM26_G1     | 5005 A430h       |
| EPWM26_G2     | 5009 A430h       |
| EPWM26_G3     | 500D A430h       |
| EPWM27_G0     | 5001 B430h       |
| EPWM27_G1     | 5005 B430h       |
| EPWM27_G2     | 5009 B430h       |
| EPWM27_G3     | 500D B430h       |
| EPWM28_G0     | 5001 C430h       |
| EPWM28_G1     | 5005 C430h       |
| EPWM28_G2     | 5009 C430h       |
| EPWM28_G3     | 500D C430h       |
| EPWM29_G0     | 5001 D430h       |
| EPWM29_G1     | 5005 D430h       |
| EPWM29_G2     | 5009 D430h       |
| EPWM29_G3     | 500D D430h       |
| EPWM30_G0     | 5001 E430h       |
| EPWM30_G1     | 5005 E430h       |
| EPWM30_G2     | 5009 E430h       |
| EPWM30_G3     | 500D E430h       |
| EPWM31_G0     | 5001 F430h       |
| EPWM31_G1     | 5005 F430h       |
| EPWM31_G2     | 5009 F430h       |
| EPWM31_G3     | 500D F430h       |



**Figure 3-356. EPWM\_XREGSHDW3STS Name Register**

|                     |                     |                     |                       |                       |                     |                     |                      |
|---------------------|---------------------|---------------------|-----------------------|-----------------------|---------------------|---------------------|----------------------|
| 31                  | 30                  | 29                  | 28                    | 27                    | 26                  | 25                  | 24                   |
| RESERVED_1          |                     |                     |                       |                       |                     |                     |                      |
| R                   |                     |                     |                       |                       |                     |                     |                      |
| 0h                  |                     |                     |                       |                       |                     |                     |                      |
| 23                  | 22                  | 21                  | 20                    | 19                    | 18                  | 17                  | 16                   |
| RESERVED_1          |                     |                     |                       |                       |                     |                     |                      |
| R                   |                     |                     |                       |                       |                     |                     |                      |
| 0h                  |                     |                     |                       |                       |                     |                     |                      |
| 15                  | 14                  | 13                  | 12                    | 11                    | 10                  | 9                   | 8                    |
| RESERVED_1          | XMIN_SHDW3<br>FULL  | XMAX_SHDW3<br>FULL  | XAQCTLB_SH<br>DW3FULL | XAQCTLA_SH<br>DW3FULL | CMPD_SHDW3<br>FULL  | CMPC_SHDW3<br>FULL  | XTBPRD_SHD<br>W3FULL |
| R                   | R                   | R                   | R                     | R                     | R                   | R                   | R                    |
| 0h                  | 0h                  | 0h                  | 0h                    | 0h                    | 0h                  | 0h                  | 0h                   |
| 7                   | 6                   | 5                   | 4                     | 3                     | 2                   | 1                   | 0                    |
| XCMP8_SHDW<br>3FULL | XCMP7_SHDW<br>3FULL | XCMP6_SHDW<br>3FULL | XCMP5_SHDW<br>3FULL   | XCMP4_SHDW<br>3FULL   | XCMP3_SHDW<br>3FULL | XCMP2_SHDW<br>3FULL | XCMP1_SHDW<br>3FULL  |
| R                   | R                   | R                   | R                     | R                     | R                   | R                   | R                    |
| 0h                  | 0h                  | 0h                  | 0h                    | 0h                    | 0h                  | 0h                  | 0h                   |

**Table 3-1128. EPWM\_XREGSHDW3STS Register Field Descriptions**

| Bit   | Field             | Type | Reset | Description                                                                                                                    |
|-------|-------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------|
| 31:15 | RESERVED_1        | R    | 0h    | Reserved                                                                                                                       |
| 14    | XMIN_SHDW3FULL    | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 13    | XMAX_SHDW3FULL    | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 12    | XAQCTLB_SHDW3FULL | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 11    | XAQCTLA_SHDW3FULL | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 10    | CMPD_SHDW3FULL    | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 9     | CMPC_SHDW3FULL    | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 8     | XTBPRD_SHDW3FULL  | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 7     | XCMP8_SHDW3FULL   | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 6     | XCMP7_SHDW3FULL   | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 5     | XCMP6_SHDW3FULL   | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |

**Table 3-1128. EPWM\_XREGSHDW3STS Register Field Descriptions (continued)**

| Bit | Field           | Type | Reset | Description                                                                                                                    |
|-----|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------|
| 4   | XCMP5_SHDW3FULL | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 3   | XCMP4_SHDW3FULL | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 2   | XCMP3_SHDW3FULL | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 1   | XCMP2_SHDW3FULL | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |
| 0   | XCMP1_SHDW3FULL | R    | 0h    | 0 Shadow Register is not full yet<br>1 Indicates the Shadow Register is full, a CPU write will over-write current Shadow value |

### 3.7.2.106 EPWM\_XCMP1\_ACTIVE Register

#### 1 EPWM\_XCMP1\_ACTIVE Register (Offset = 600h) [reset = 0h]

Additional Compare 1 Active Register.

Return to [Summary Table](#)

**Table 3-1129. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0600h       |
| EPWM0_G1      | 5004 0600h       |
| EPWM0_G2      | 5008 0600h       |
| EPWM0_G3      | 500C 0600h       |
| EPWM1_G0      | 5000 1600h       |
| EPWM1_G1      | 5004 1600h       |
| EPWM1_G2      | 5008 1600h       |
| EPWM1_G3      | 500C 1600h       |
| EPWM2_G0      | 5000 2600h       |
| EPWM2_G1      | 5004 2600h       |
| EPWM2_G2      | 5008 2600h       |
| EPWM2_G3      | 500C 2600h       |
| EPWM3_G0      | 5000 3600h       |
| EPWM3_G1      | 5004 3600h       |
| EPWM3_G2      | 5008 3600h       |
| EPWM3_G3      | 500C 3600h       |
| EPWM4_G0      | 5000 4600h       |
| EPWM4_G1      | 5004 4600h       |
| EPWM4_G2      | 5008 4600h       |
| EPWM4_G3      | 500C 4600h       |
| EPWM5_G0      | 5000 5600h       |
| EPWM5_G1      | 5004 5600h       |
| EPWM5_G2      | 5008 5600h       |
| EPWM5_G3      | 500C 5600h       |
| EPWM6_G0      | 5000 6600h       |
| EPWM6_G1      | 5004 6600h       |
| EPWM6_G2      | 5008 6600h       |
| EPWM6_G3      | 500C 6600h       |
| EPWM7_G0      | 5000 7600h       |
| EPWM7_G1      | 5004 7600h       |
| EPWM7_G2      | 5008 7600h       |
| EPWM7_G3      | 500C 7600h       |
| EPWM8_G0      | 5000 8600h       |
| EPWM8_G1      | 5004 8600h       |
| EPWM8_G2      | 5008 8600h       |
| EPWM8_G3      | 500C 8600h       |
| EPWM9_G0      | 5000 9600h       |
| EPWM9_G1      | 5004 9600h       |
| EPWM9_G2      | 5008 9600h       |

**Table 3-1129. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9600h       |
| EPWM10_G0     | 5000 A600h       |
| EPWM10_G1     | 5004 A600h       |
| EPWM10_G2     | 5008 A600h       |
| EPWM10_G3     | 500C A600h       |
| EPWM11_G0     | 5000 B600h       |
| EPWM11_G1     | 5004 B600h       |
| EPWM11_G2     | 5008 B600h       |
| EPWM11_G3     | 500C B600h       |
| EPWM12_G0     | 5000 C600h       |
| EPWM12_G1     | 5004 C600h       |
| EPWM12_G2     | 5008 C600h       |
| EPWM12_G3     | 500C C600h       |
| EPWM13_G0     | 5000 D600h       |
| EPWM13_G1     | 5004 D600h       |
| EPWM13_G2     | 5008 D600h       |
| EPWM13_G3     | 500C D600h       |
| EPWM14_G0     | 5000 E600h       |
| EPWM14_G1     | 5004 E600h       |
| EPWM14_G2     | 5008 E600h       |
| EPWM14_G3     | 500C E600h       |
| EPWM15_G0     | 5000 F600h       |
| EPWM15_G1     | 5004 F600h       |
| EPWM15_G2     | 5008 F600h       |
| EPWM15_G3     | 500C F600h       |
| EPWM16_G0     | 5001 0600h       |
| EPWM16_G1     | 5005 0600h       |
| EPWM16_G2     | 5009 0600h       |
| EPWM16_G3     | 500D 0600h       |
| EPWM17_G0     | 5001 1600h       |
| EPWM17_G1     | 5005 1600h       |
| EPWM17_G2     | 5009 1600h       |
| EPWM17_G3     | 500D 1600h       |
| EPWM18_G0     | 5001 2600h       |
| EPWM18_G1     | 5005 2600h       |
| EPWM18_G2     | 5009 2600h       |
| EPWM18_G3     | 500D 2600h       |
| EPWM19_G0     | 5001 3600h       |
| EPWM19_G1     | 5005 3600h       |
| EPWM19_G2     | 5009 3600h       |
| EPWM19_G3     | 500D 3600h       |
| EPWM20_G0     | 5001 4600h       |
| EPWM20_G1     | 5005 4600h       |
| EPWM20_G2     | 5009 4600h       |
| EPWM20_G3     | 500D 4600h       |

**Table 3-1129. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5600h       |
| EPWM21_G1     | 5005 5600h       |
| EPWM21_G2     | 5009 5600h       |
| EPWM21_G3     | 500D 5600h       |
| EPWM22_G0     | 5001 6600h       |
| EPWM22_G1     | 5005 6600h       |
| EPWM22_G2     | 5009 6600h       |
| EPWM22_G3     | 500D 6600h       |
| EPWM23_G0     | 5001 7600h       |
| EPWM23_G1     | 5005 7600h       |
| EPWM23_G2     | 5009 7600h       |
| EPWM23_G3     | 500D 7600h       |
| EPWM24_G0     | 5001 8600h       |
| EPWM24_G1     | 5005 8600h       |
| EPWM24_G2     | 5009 8600h       |
| EPWM24_G3     | 500D 8600h       |
| EPWM25_G0     | 5001 9600h       |
| EPWM25_G1     | 5005 9600h       |
| EPWM25_G2     | 5009 9600h       |
| EPWM25_G3     | 500D 9600h       |
| EPWM26_G0     | 5001 A600h       |
| EPWM26_G1     | 5005 A600h       |
| EPWM26_G2     | 5009 A600h       |
| EPWM26_G3     | 500D A600h       |
| EPWM27_G0     | 5001 B600h       |
| EPWM27_G1     | 5005 B600h       |
| EPWM27_G2     | 5009 B600h       |
| EPWM27_G3     | 500D B600h       |
| EPWM28_G0     | 5001 C600h       |
| EPWM28_G1     | 5005 C600h       |
| EPWM28_G2     | 5009 C600h       |
| EPWM28_G3     | 500D C600h       |
| EPWM29_G0     | 5001 D600h       |
| EPWM29_G1     | 5005 D600h       |
| EPWM29_G2     | 5009 D600h       |
| EPWM29_G3     | 500D D600h       |
| EPWM30_G0     | 5001 E600h       |
| EPWM30_G1     | 5005 E600h       |
| EPWM30_G2     | 5009 E600h       |
| EPWM30_G3     | 500D E600h       |
| EPWM31_G0     | 5001 F600h       |
| EPWM31_G1     | 5005 F600h       |
| EPWM31_G2     | 5009 F600h       |
| EPWM31_G3     | 500D F600h       |

**Figure 3-357. EPWM\_XCMP1\_ACTIVE Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP1_ACTIVE   |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP1_ACTIVE   |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP1HR_ACTIVE |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP1HR_ACTIVE |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 3-1131. EPWM\_XCMP1\_ACTIVE Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                              |
|-------|----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP1_ACTIVE   | R/W  | 0h    | XCMP1_ACTIVE Register<br>The value in the XCMP1_ACTIVE register is loaded into CMPA/B [shadow/active] registers when shadow to active load occurs.       |
| 15:0  | XCMP1HR_ACTIVE | R/W  | 0h    | XCMP1HR_ACTIVE Register<br>The value in the XCMP1HR_ACTIVE register is loaded into CMPA/BHR [shadow/active] registers when shadow to active load occurs. |

### 3.7.2.107 EPWM\_XCMP2\_ACTIVE Register

#### 1 EPWM\_XCMP2\_ACTIVE Register (Offset = 604h) [reset = 0h]

Additional Compare 2 Active Register.

Return to [Summary Table](#)

**Table 3-1132. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0604h       |
| EPWM0_G1      | 5004 0604h       |
| EPWM0_G2      | 5008 0604h       |
| EPWM0_G3      | 500C 0604h       |
| EPWM1_G0      | 5000 1604h       |
| EPWM1_G1      | 5004 1604h       |
| EPWM1_G2      | 5008 1604h       |
| EPWM1_G3      | 500C 1604h       |
| EPWM2_G0      | 5000 2604h       |
| EPWM2_G1      | 5004 2604h       |
| EPWM2_G2      | 5008 2604h       |
| EPWM2_G3      | 500C 2604h       |
| EPWM3_G0      | 5000 3604h       |
| EPWM3_G1      | 5004 3604h       |
| EPWM3_G2      | 5008 3604h       |
| EPWM3_G3      | 500C 3604h       |
| EPWM4_G0      | 5000 4604h       |
| EPWM4_G1      | 5004 4604h       |
| EPWM4_G2      | 5008 4604h       |
| EPWM4_G3      | 500C 4604h       |
| EPWM5_G0      | 5000 5604h       |
| EPWM5_G1      | 5004 5604h       |
| EPWM5_G2      | 5008 5604h       |
| EPWM5_G3      | 500C 5604h       |
| EPWM6_G0      | 5000 6604h       |
| EPWM6_G1      | 5004 6604h       |
| EPWM6_G2      | 5008 6604h       |
| EPWM6_G3      | 500C 6604h       |
| EPWM7_G0      | 5000 7604h       |
| EPWM7_G1      | 5004 7604h       |
| EPWM7_G2      | 5008 7604h       |
| EPWM7_G3      | 500C 7604h       |
| EPWM8_G0      | 5000 8604h       |
| EPWM8_G1      | 5004 8604h       |
| EPWM8_G2      | 5008 8604h       |
| EPWM8_G3      | 500C 8604h       |
| EPWM9_G0      | 5000 9604h       |
| EPWM9_G1      | 5004 9604h       |
| EPWM9_G2      | 5008 9604h       |

**Table 3-1132. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9604h       |
| EPWM10_G0     | 5000 A604h       |
| EPWM10_G1     | 5004 A604h       |
| EPWM10_G2     | 5008 A604h       |
| EPWM10_G3     | 500C A604h       |
| EPWM11_G0     | 5000 B604h       |
| EPWM11_G1     | 5004 B604h       |
| EPWM11_G2     | 5008 B604h       |
| EPWM11_G3     | 500C B604h       |
| EPWM12_G0     | 5000 C604h       |
| EPWM12_G1     | 5004 C604h       |
| EPWM12_G2     | 5008 C604h       |
| EPWM12_G3     | 500C C604h       |
| EPWM13_G0     | 5000 D604h       |
| EPWM13_G1     | 5004 D604h       |
| EPWM13_G2     | 5008 D604h       |
| EPWM13_G3     | 500C D604h       |
| EPWM14_G0     | 5000 E604h       |
| EPWM14_G1     | 5004 E604h       |
| EPWM14_G2     | 5008 E604h       |
| EPWM14_G3     | 500C E604h       |
| EPWM15_G0     | 5000 F604h       |
| EPWM15_G1     | 5004 F604h       |
| EPWM15_G2     | 5008 F604h       |
| EPWM15_G3     | 500C F604h       |
| EPWM16_G0     | 5001 0604h       |
| EPWM16_G1     | 5005 0604h       |
| EPWM16_G2     | 5009 0604h       |
| EPWM16_G3     | 500D 0604h       |
| EPWM17_G0     | 5001 1604h       |
| EPWM17_G1     | 5005 1604h       |
| EPWM17_G2     | 5009 1604h       |
| EPWM17_G3     | 500D 1604h       |
| EPWM18_G0     | 5001 2604h       |
| EPWM18_G1     | 5005 2604h       |
| EPWM18_G2     | 5009 2604h       |
| EPWM18_G3     | 500D 2604h       |
| EPWM19_G0     | 5001 3604h       |
| EPWM19_G1     | 5005 3604h       |
| EPWM19_G2     | 5009 3604h       |
| EPWM19_G3     | 500D 3604h       |
| EPWM20_G0     | 5001 4604h       |
| EPWM20_G1     | 5005 4604h       |
| EPWM20_G2     | 5009 4604h       |
| EPWM20_G3     | 500D 4604h       |



**Table 3-1132. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5604h       |
| EPWM21_G1     | 5005 5604h       |
| EPWM21_G2     | 5009 5604h       |
| EPWM21_G3     | 500D 5604h       |
| EPWM22_G0     | 5001 6604h       |
| EPWM22_G1     | 5005 6604h       |
| EPWM22_G2     | 5009 6604h       |
| EPWM22_G3     | 500D 6604h       |
| EPWM23_G0     | 5001 7604h       |
| EPWM23_G1     | 5005 7604h       |
| EPWM23_G2     | 5009 7604h       |
| EPWM23_G3     | 500D 7604h       |
| EPWM24_G0     | 5001 8604h       |
| EPWM24_G1     | 5005 8604h       |
| EPWM24_G2     | 5009 8604h       |
| EPWM24_G3     | 500D 8604h       |
| EPWM25_G0     | 5001 9604h       |
| EPWM25_G1     | 5005 9604h       |
| EPWM25_G2     | 5009 9604h       |
| EPWM25_G3     | 500D 9604h       |
| EPWM26_G0     | 5001 A604h       |
| EPWM26_G1     | 5005 A604h       |
| EPWM26_G2     | 5009 A604h       |
| EPWM26_G3     | 500D A604h       |
| EPWM27_G0     | 5001 B604h       |
| EPWM27_G1     | 5005 B604h       |
| EPWM27_G2     | 5009 B604h       |
| EPWM27_G3     | 500D B604h       |
| EPWM28_G0     | 5001 C604h       |
| EPWM28_G1     | 5005 C604h       |
| EPWM28_G2     | 5009 C604h       |
| EPWM28_G3     | 500D C604h       |
| EPWM29_G0     | 5001 D604h       |
| EPWM29_G1     | 5005 D604h       |
| EPWM29_G2     | 5009 D604h       |
| EPWM29_G3     | 500D D604h       |
| EPWM30_G0     | 5001 E604h       |
| EPWM30_G1     | 5005 E604h       |
| EPWM30_G2     | 5009 E604h       |
| EPWM30_G3     | 500D E604h       |
| EPWM31_G0     | 5001 F604h       |
| EPWM31_G1     | 5005 F604h       |
| EPWM31_G2     | 5009 F604h       |
| EPWM31_G3     | 500D F604h       |

**Figure 3-358. EPWM\_XCMP2\_ACTIVE Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP2_ACTIVE   |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP2_ACTIVE   |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP2HR_ACTIVE |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP2HR_ACTIVE |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 3-1134. EPWM\_XCMP2\_ACTIVE Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                              |
|-------|----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP2_ACTIVE   | R/W  | 0h    | XCMP2_ACTIVE Register<br>The value in the XCMP2_ACTIVE register is loaded into CMPA/B [shadow/active] registers when shadow to active load occurs.       |
| 15:0  | XCMP2HR_ACTIVE | R/W  | 0h    | XCMP2HR_ACTIVE Register<br>The value in the XCMP2HR_ACTIVE register is loaded into CMPA/BHR [shadow/active] registers when shadow to active load occurs. |

### 3.7.2.108 EPWM\_XCMP3\_ACTIVE Register

#### 1 EPWM\_XCMP3\_ACTIVE Register (Offset = 608h) [reset = 0h]

Additional Compare 3 Active Register.

Return to [Summary Table](#)

**Table 3-1135. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0608h       |
| EPWM0_G1      | 5004 0608h       |
| EPWM0_G2      | 5008 0608h       |
| EPWM0_G3      | 500C 0608h       |
| EPWM1_G0      | 5000 1608h       |
| EPWM1_G1      | 5004 1608h       |
| EPWM1_G2      | 5008 1608h       |
| EPWM1_G3      | 500C 1608h       |
| EPWM2_G0      | 5000 2608h       |
| EPWM2_G1      | 5004 2608h       |
| EPWM2_G2      | 5008 2608h       |
| EPWM2_G3      | 500C 2608h       |
| EPWM3_G0      | 5000 3608h       |
| EPWM3_G1      | 5004 3608h       |
| EPWM3_G2      | 5008 3608h       |
| EPWM3_G3      | 500C 3608h       |
| EPWM4_G0      | 5000 4608h       |
| EPWM4_G1      | 5004 4608h       |
| EPWM4_G2      | 5008 4608h       |
| EPWM4_G3      | 500C 4608h       |
| EPWM5_G0      | 5000 5608h       |
| EPWM5_G1      | 5004 5608h       |
| EPWM5_G2      | 5008 5608h       |
| EPWM5_G3      | 500C 5608h       |
| EPWM6_G0      | 5000 6608h       |
| EPWM6_G1      | 5004 6608h       |
| EPWM6_G2      | 5008 6608h       |
| EPWM6_G3      | 500C 6608h       |
| EPWM7_G0      | 5000 7608h       |
| EPWM7_G1      | 5004 7608h       |
| EPWM7_G2      | 5008 7608h       |
| EPWM7_G3      | 500C 7608h       |
| EPWM8_G0      | 5000 8608h       |
| EPWM8_G1      | 5004 8608h       |
| EPWM8_G2      | 5008 8608h       |
| EPWM8_G3      | 500C 8608h       |
| EPWM9_G0      | 5000 9608h       |
| EPWM9_G1      | 5004 9608h       |
| EPWM9_G2      | 5008 9608h       |

**Table 3-1135. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9608h       |
| EPWM10_G0     | 5000 A608h       |
| EPWM10_G1     | 5004 A608h       |
| EPWM10_G2     | 5008 A608h       |
| EPWM10_G3     | 500C A608h       |
| EPWM11_G0     | 5000 B608h       |
| EPWM11_G1     | 5004 B608h       |
| EPWM11_G2     | 5008 B608h       |
| EPWM11_G3     | 500C B608h       |
| EPWM12_G0     | 5000 C608h       |
| EPWM12_G1     | 5004 C608h       |
| EPWM12_G2     | 5008 C608h       |
| EPWM12_G3     | 500C C608h       |
| EPWM13_G0     | 5000 D608h       |
| EPWM13_G1     | 5004 D608h       |
| EPWM13_G2     | 5008 D608h       |
| EPWM13_G3     | 500C D608h       |
| EPWM14_G0     | 5000 E608h       |
| EPWM14_G1     | 5004 E608h       |
| EPWM14_G2     | 5008 E608h       |
| EPWM14_G3     | 500C E608h       |
| EPWM15_G0     | 5000 F608h       |
| EPWM15_G1     | 5004 F608h       |
| EPWM15_G2     | 5008 F608h       |
| EPWM15_G3     | 500C F608h       |
| EPWM16_G0     | 5001 0608h       |
| EPWM16_G1     | 5005 0608h       |
| EPWM16_G2     | 5009 0608h       |
| EPWM16_G3     | 500D 0608h       |
| EPWM17_G0     | 5001 1608h       |
| EPWM17_G1     | 5005 1608h       |
| EPWM17_G2     | 5009 1608h       |
| EPWM17_G3     | 500D 1608h       |
| EPWM18_G0     | 5001 2608h       |
| EPWM18_G1     | 5005 2608h       |
| EPWM18_G2     | 5009 2608h       |
| EPWM18_G3     | 500D 2608h       |
| EPWM19_G0     | 5001 3608h       |
| EPWM19_G1     | 5005 3608h       |
| EPWM19_G2     | 5009 3608h       |
| EPWM19_G3     | 500D 3608h       |
| EPWM20_G0     | 5001 4608h       |
| EPWM20_G1     | 5005 4608h       |
| EPWM20_G2     | 5009 4608h       |
| EPWM20_G3     | 500D 4608h       |

**Table 3-1135. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5608h       |
| EPWM21_G1     | 5005 5608h       |
| EPWM21_G2     | 5009 5608h       |
| EPWM21_G3     | 500D 5608h       |
| EPWM22_G0     | 5001 6608h       |
| EPWM22_G1     | 5005 6608h       |
| EPWM22_G2     | 5009 6608h       |
| EPWM22_G3     | 500D 6608h       |
| EPWM23_G0     | 5001 7608h       |
| EPWM23_G1     | 5005 7608h       |
| EPWM23_G2     | 5009 7608h       |
| EPWM23_G3     | 500D 7608h       |
| EPWM24_G0     | 5001 8608h       |
| EPWM24_G1     | 5005 8608h       |
| EPWM24_G2     | 5009 8608h       |
| EPWM24_G3     | 500D 8608h       |
| EPWM25_G0     | 5001 9608h       |
| EPWM25_G1     | 5005 9608h       |
| EPWM25_G2     | 5009 9608h       |
| EPWM25_G3     | 500D 9608h       |
| EPWM26_G0     | 5001 A608h       |
| EPWM26_G1     | 5005 A608h       |
| EPWM26_G2     | 5009 A608h       |
| EPWM26_G3     | 500D A608h       |
| EPWM27_G0     | 5001 B608h       |
| EPWM27_G1     | 5005 B608h       |
| EPWM27_G2     | 5009 B608h       |
| EPWM27_G3     | 500D B608h       |
| EPWM28_G0     | 5001 C608h       |
| EPWM28_G1     | 5005 C608h       |
| EPWM28_G2     | 5009 C608h       |
| EPWM28_G3     | 500D C608h       |
| EPWM29_G0     | 5001 D608h       |
| EPWM29_G1     | 5005 D608h       |
| EPWM29_G2     | 5009 D608h       |
| EPWM29_G3     | 500D D608h       |
| EPWM30_G0     | 5001 E608h       |
| EPWM30_G1     | 5005 E608h       |
| EPWM30_G2     | 5009 E608h       |
| EPWM30_G3     | 500D E608h       |
| EPWM31_G0     | 5001 F608h       |
| EPWM31_G1     | 5005 F608h       |
| EPWM31_G2     | 5009 F608h       |
| EPWM31_G3     | 500D F608h       |

**Figure 3-359. EPWM\_XCMP3\_ACTIVE Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP3_ACTIVE   |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP3_ACTIVE   |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP3HR_ACTIVE |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP3HR_ACTIVE |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 3-1137. EPWM\_XCMP3\_ACTIVE Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                              |
|-------|----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP3_ACTIVE   | R/W  | 0h    | XCMP3_ACTIVE Register<br>The value in the XCMP3_ACTIVE register is loaded into CMPA/B [shadow/active] registers when shadow to active load occurs.       |
| 15:0  | XCMP3HR_ACTIVE | R/W  | 0h    | XCMP3HR_ACTIVE Register<br>The value in the XCMP3HR_ACTIVE register is loaded into CMPA/BHR [shadow/active] registers when shadow to active load occurs. |

### 3.7.2.109 EPWM\_XCMP4\_ACTIVE Register

#### 1 EPWM\_XCMP4\_ACTIVE Register (Offset = 60Ch) [reset = 0h]

Additional Compare 4 Active Register.

Return to [Summary Table](#)

**Table 3-1138. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 060Ch       |
| EPWM0_G1      | 5004 060Ch       |
| EPWM0_G2      | 5008 060Ch       |
| EPWM0_G3      | 500C 060Ch       |
| EPWM1_G0      | 5000 160Ch       |
| EPWM1_G1      | 5004 160Ch       |
| EPWM1_G2      | 5008 160Ch       |
| EPWM1_G3      | 500C 160Ch       |
| EPWM2_G0      | 5000 260Ch       |
| EPWM2_G1      | 5004 260Ch       |
| EPWM2_G2      | 5008 260Ch       |
| EPWM2_G3      | 500C 260Ch       |
| EPWM3_G0      | 5000 360Ch       |
| EPWM3_G1      | 5004 360Ch       |
| EPWM3_G2      | 5008 360Ch       |
| EPWM3_G3      | 500C 360Ch       |
| EPWM4_G0      | 5000 460Ch       |
| EPWM4_G1      | 5004 460Ch       |
| EPWM4_G2      | 5008 460Ch       |
| EPWM4_G3      | 500C 460Ch       |
| EPWM5_G0      | 5000 560Ch       |
| EPWM5_G1      | 5004 560Ch       |
| EPWM5_G2      | 5008 560Ch       |
| EPWM5_G3      | 500C 560Ch       |
| EPWM6_G0      | 5000 660Ch       |
| EPWM6_G1      | 5004 660Ch       |
| EPWM6_G2      | 5008 660Ch       |
| EPWM6_G3      | 500C 660Ch       |
| EPWM7_G0      | 5000 760Ch       |
| EPWM7_G1      | 5004 760Ch       |
| EPWM7_G2      | 5008 760Ch       |
| EPWM7_G3      | 500C 760Ch       |
| EPWM8_G0      | 5000 860Ch       |
| EPWM8_G1      | 5004 860Ch       |
| EPWM8_G2      | 5008 860Ch       |
| EPWM8_G3      | 500C 860Ch       |
| EPWM9_G0      | 5000 960Ch       |
| EPWM9_G1      | 5004 960Ch       |
| EPWM9_G2      | 5008 960Ch       |

**Table 3-1138. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 960Ch       |
| EPWM10_G0     | 5000 A60Ch       |
| EPWM10_G1     | 5004 A60Ch       |
| EPWM10_G2     | 5008 A60Ch       |
| EPWM10_G3     | 500C A60Ch       |
| EPWM11_G0     | 5000 B60Ch       |
| EPWM11_G1     | 5004 B60Ch       |
| EPWM11_G2     | 5008 B60Ch       |
| EPWM11_G3     | 500C B60Ch       |
| EPWM12_G0     | 5000 C60Ch       |
| EPWM12_G1     | 5004 C60Ch       |
| EPWM12_G2     | 5008 C60Ch       |
| EPWM12_G3     | 500C C60Ch       |
| EPWM13_G0     | 5000 D60Ch       |
| EPWM13_G1     | 5004 D60Ch       |
| EPWM13_G2     | 5008 D60Ch       |
| EPWM13_G3     | 500C D60Ch       |
| EPWM14_G0     | 5000 E60Ch       |
| EPWM14_G1     | 5004 E60Ch       |
| EPWM14_G2     | 5008 E60Ch       |
| EPWM14_G3     | 500C E60Ch       |
| EPWM15_G0     | 5000 F60Ch       |
| EPWM15_G1     | 5004 F60Ch       |
| EPWM15_G2     | 5008 F60Ch       |
| EPWM15_G3     | 500C F60Ch       |
| EPWM16_G0     | 5001 060Ch       |
| EPWM16_G1     | 5005 060Ch       |
| EPWM16_G2     | 5009 060Ch       |
| EPWM16_G3     | 500D 060Ch       |
| EPWM17_G0     | 5001 160Ch       |
| EPWM17_G1     | 5005 160Ch       |
| EPWM17_G2     | 5009 160Ch       |
| EPWM17_G3     | 500D 160Ch       |
| EPWM18_G0     | 5001 260Ch       |
| EPWM18_G1     | 5005 260Ch       |
| EPWM18_G2     | 5009 260Ch       |
| EPWM18_G3     | 500D 260Ch       |
| EPWM19_G0     | 5001 360Ch       |
| EPWM19_G1     | 5005 360Ch       |
| EPWM19_G2     | 5009 360Ch       |
| EPWM19_G3     | 500D 360Ch       |
| EPWM20_G0     | 5001 460Ch       |
| EPWM20_G1     | 5005 460Ch       |
| EPWM20_G2     | 5009 460Ch       |
| EPWM20_G3     | 500D 460Ch       |



**Table 3-1138. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 560Ch       |
| EPWM21_G1     | 5005 560Ch       |
| EPWM21_G2     | 5009 560Ch       |
| EPWM21_G3     | 500D 560Ch       |
| EPWM22_G0     | 5001 660Ch       |
| EPWM22_G1     | 5005 660Ch       |
| EPWM22_G2     | 5009 660Ch       |
| EPWM22_G3     | 500D 660Ch       |
| EPWM23_G0     | 5001 760Ch       |
| EPWM23_G1     | 5005 760Ch       |
| EPWM23_G2     | 5009 760Ch       |
| EPWM23_G3     | 500D 760Ch       |
| EPWM24_G0     | 5001 860Ch       |
| EPWM24_G1     | 5005 860Ch       |
| EPWM24_G2     | 5009 860Ch       |
| EPWM24_G3     | 500D 860Ch       |
| EPWM25_G0     | 5001 960Ch       |
| EPWM25_G1     | 5005 960Ch       |
| EPWM25_G2     | 5009 960Ch       |
| EPWM25_G3     | 500D 960Ch       |
| EPWM26_G0     | 5001 A60Ch       |
| EPWM26_G1     | 5005 A60Ch       |
| EPWM26_G2     | 5009 A60Ch       |
| EPWM26_G3     | 500D A60Ch       |
| EPWM27_G0     | 5001 B60Ch       |
| EPWM27_G1     | 5005 B60Ch       |
| EPWM27_G2     | 5009 B60Ch       |
| EPWM27_G3     | 500D B60Ch       |
| EPWM28_G0     | 5001 C60Ch       |
| EPWM28_G1     | 5005 C60Ch       |
| EPWM28_G2     | 5009 C60Ch       |
| EPWM28_G3     | 500D C60Ch       |
| EPWM29_G0     | 5001 D60Ch       |
| EPWM29_G1     | 5005 D60Ch       |
| EPWM29_G2     | 5009 D60Ch       |
| EPWM29_G3     | 500D D60Ch       |
| EPWM30_G0     | 5001 E60Ch       |
| EPWM30_G1     | 5005 E60Ch       |
| EPWM30_G2     | 5009 E60Ch       |
| EPWM30_G3     | 500D E60Ch       |
| EPWM31_G0     | 5001 F60Ch       |
| EPWM31_G1     | 5005 F60Ch       |
| EPWM31_G2     | 5009 F60Ch       |
| EPWM31_G3     | 500D F60Ch       |

**Figure 3-360. EPWM\_XCMP4\_ACTIVE Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP4_ACTIVE   |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP4_ACTIVE   |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP4HR_ACTIVE |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP4HR_ACTIVE |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 3-1140. EPWM\_XCMP4\_ACTIVE Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                              |
|-------|----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP4_ACTIVE   | R/W  | 0h    | XCMP4_ACTIVE Register<br>The value in the XCMP4_ACTIVE register is loaded into CMPA/B [shadow/active] registers when shadow to active load occurs.       |
| 15:0  | XCMP4HR_ACTIVE | R/W  | 0h    | XCMP4HR_ACTIVE Register<br>The value in the XCMP4HR_ACTIVE register is loaded into CMPA/BHR [shadow/active] registers when shadow to active load occurs. |

### 3.7.2.110 EPWM\_XCMP5\_ACTIVE Register

#### 1 EPWM\_XCMP5\_ACTIVE Register (Offset = 610h) [reset = 0h]

Additional Compare 5 Active Register.

Return to [Summary Table](#)

**Table 3-1141. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0610h       |
| EPWM0_G1      | 5004 0610h       |
| EPWM0_G2      | 5008 0610h       |
| EPWM0_G3      | 500C 0610h       |
| EPWM1_G0      | 5000 1610h       |
| EPWM1_G1      | 5004 1610h       |
| EPWM1_G2      | 5008 1610h       |
| EPWM1_G3      | 500C 1610h       |
| EPWM2_G0      | 5000 2610h       |
| EPWM2_G1      | 5004 2610h       |
| EPWM2_G2      | 5008 2610h       |
| EPWM2_G3      | 500C 2610h       |
| EPWM3_G0      | 5000 3610h       |
| EPWM3_G1      | 5004 3610h       |
| EPWM3_G2      | 5008 3610h       |
| EPWM3_G3      | 500C 3610h       |
| EPWM4_G0      | 5000 4610h       |
| EPWM4_G1      | 5004 4610h       |
| EPWM4_G2      | 5008 4610h       |
| EPWM4_G3      | 500C 4610h       |
| EPWM5_G0      | 5000 5610h       |
| EPWM5_G1      | 5004 5610h       |
| EPWM5_G2      | 5008 5610h       |
| EPWM5_G3      | 500C 5610h       |
| EPWM6_G0      | 5000 6610h       |
| EPWM6_G1      | 5004 6610h       |
| EPWM6_G2      | 5008 6610h       |
| EPWM6_G3      | 500C 6610h       |
| EPWM7_G0      | 5000 7610h       |
| EPWM7_G1      | 5004 7610h       |
| EPWM7_G2      | 5008 7610h       |
| EPWM7_G3      | 500C 7610h       |
| EPWM8_G0      | 5000 8610h       |
| EPWM8_G1      | 5004 8610h       |
| EPWM8_G2      | 5008 8610h       |
| EPWM8_G3      | 500C 8610h       |
| EPWM9_G0      | 5000 9610h       |
| EPWM9_G1      | 5004 9610h       |
| EPWM9_G2      | 5008 9610h       |

**Table 3-1141. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9610h       |
| EPWM10_G0     | 5000 A610h       |
| EPWM10_G1     | 5004 A610h       |
| EPWM10_G2     | 5008 A610h       |
| EPWM10_G3     | 500C A610h       |
| EPWM11_G0     | 5000 B610h       |
| EPWM11_G1     | 5004 B610h       |
| EPWM11_G2     | 5008 B610h       |
| EPWM11_G3     | 500C B610h       |
| EPWM12_G0     | 5000 C610h       |
| EPWM12_G1     | 5004 C610h       |
| EPWM12_G2     | 5008 C610h       |
| EPWM12_G3     | 500C C610h       |
| EPWM13_G0     | 5000 D610h       |
| EPWM13_G1     | 5004 D610h       |
| EPWM13_G2     | 5008 D610h       |
| EPWM13_G3     | 500C D610h       |
| EPWM14_G0     | 5000 E610h       |
| EPWM14_G1     | 5004 E610h       |
| EPWM14_G2     | 5008 E610h       |
| EPWM14_G3     | 500C E610h       |
| EPWM15_G0     | 5000 F610h       |
| EPWM15_G1     | 5004 F610h       |
| EPWM15_G2     | 5008 F610h       |
| EPWM15_G3     | 500C F610h       |
| EPWM16_G0     | 5001 0610h       |
| EPWM16_G1     | 5005 0610h       |
| EPWM16_G2     | 5009 0610h       |
| EPWM16_G3     | 500D 0610h       |
| EPWM17_G0     | 5001 1610h       |
| EPWM17_G1     | 5005 1610h       |
| EPWM17_G2     | 5009 1610h       |
| EPWM17_G3     | 500D 1610h       |
| EPWM18_G0     | 5001 2610h       |
| EPWM18_G1     | 5005 2610h       |
| EPWM18_G2     | 5009 2610h       |
| EPWM18_G3     | 500D 2610h       |
| EPWM19_G0     | 5001 3610h       |
| EPWM19_G1     | 5005 3610h       |
| EPWM19_G2     | 5009 3610h       |
| EPWM19_G3     | 500D 3610h       |
| EPWM20_G0     | 5001 4610h       |
| EPWM20_G1     | 5005 4610h       |
| EPWM20_G2     | 5009 4610h       |
| EPWM20_G3     | 500D 4610h       |

**Table 3-1141. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5610h       |
| EPWM21_G1     | 5005 5610h       |
| EPWM21_G2     | 5009 5610h       |
| EPWM21_G3     | 500D 5610h       |
| EPWM22_G0     | 5001 6610h       |
| EPWM22_G1     | 5005 6610h       |
| EPWM22_G2     | 5009 6610h       |
| EPWM22_G3     | 500D 6610h       |
| EPWM23_G0     | 5001 7610h       |
| EPWM23_G1     | 5005 7610h       |
| EPWM23_G2     | 5009 7610h       |
| EPWM23_G3     | 500D 7610h       |
| EPWM24_G0     | 5001 8610h       |
| EPWM24_G1     | 5005 8610h       |
| EPWM24_G2     | 5009 8610h       |
| EPWM24_G3     | 500D 8610h       |
| EPWM25_G0     | 5001 9610h       |
| EPWM25_G1     | 5005 9610h       |
| EPWM25_G2     | 5009 9610h       |
| EPWM25_G3     | 500D 9610h       |
| EPWM26_G0     | 5001 A610h       |
| EPWM26_G1     | 5005 A610h       |
| EPWM26_G2     | 5009 A610h       |
| EPWM26_G3     | 500D A610h       |
| EPWM27_G0     | 5001 B610h       |
| EPWM27_G1     | 5005 B610h       |
| EPWM27_G2     | 5009 B610h       |
| EPWM27_G3     | 500D B610h       |
| EPWM28_G0     | 5001 C610h       |
| EPWM28_G1     | 5005 C610h       |
| EPWM28_G2     | 5009 C610h       |
| EPWM28_G3     | 500D C610h       |
| EPWM29_G0     | 5001 D610h       |
| EPWM29_G1     | 5005 D610h       |
| EPWM29_G2     | 5009 D610h       |
| EPWM29_G3     | 500D D610h       |
| EPWM30_G0     | 5001 E610h       |
| EPWM30_G1     | 5005 E610h       |
| EPWM30_G2     | 5009 E610h       |
| EPWM30_G3     | 500D E610h       |
| EPWM31_G0     | 5001 F610h       |
| EPWM31_G1     | 5005 F610h       |
| EPWM31_G2     | 5009 F610h       |
| EPWM31_G3     | 500D F610h       |

**Figure 3-361. EPWM\_XCMP5\_ACTIVE Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP5_ACTIVE   |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP5_ACTIVE   |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP5HR_ACTIVE |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP5HR_ACTIVE |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 3-1143. EPWM\_XCMP5\_ACTIVE Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                              |
|-------|----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP5_ACTIVE   | R/W  | 0h    | XCMP5_ACTIVE Register<br>The value in the XCMP5_ACTIVE register is loaded into CMPA/B [shadow/active] registers when shadow to active load occurs.       |
| 15:0  | XCMP5HR_ACTIVE | R/W  | 0h    | XCMP5HR_ACTIVE Register<br>The value in the XCMP5HR_ACTIVE register is loaded into CMPA/BHR [shadow/active] registers when shadow to active load occurs. |

### 3.7.2.111 EPWM\_XCMP6\_ACTIVE Register

#### 1 EPWM\_XCMP6\_ACTIVE Register (Offset = 614h) [reset = 0h]

Additional Compare 6 Active Register.

Return to [Summary Table](#)

**Table 3-1144. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0614h       |
| EPWM0_G1      | 5004 0614h       |
| EPWM0_G2      | 5008 0614h       |
| EPWM0_G3      | 500C 0614h       |
| EPWM1_G0      | 5000 1614h       |
| EPWM1_G1      | 5004 1614h       |
| EPWM1_G2      | 5008 1614h       |
| EPWM1_G3      | 500C 1614h       |
| EPWM2_G0      | 5000 2614h       |
| EPWM2_G1      | 5004 2614h       |
| EPWM2_G2      | 5008 2614h       |
| EPWM2_G3      | 500C 2614h       |
| EPWM3_G0      | 5000 3614h       |
| EPWM3_G1      | 5004 3614h       |
| EPWM3_G2      | 5008 3614h       |
| EPWM3_G3      | 500C 3614h       |
| EPWM4_G0      | 5000 4614h       |
| EPWM4_G1      | 5004 4614h       |
| EPWM4_G2      | 5008 4614h       |
| EPWM4_G3      | 500C 4614h       |
| EPWM5_G0      | 5000 5614h       |
| EPWM5_G1      | 5004 5614h       |
| EPWM5_G2      | 5008 5614h       |
| EPWM5_G3      | 500C 5614h       |
| EPWM6_G0      | 5000 6614h       |
| EPWM6_G1      | 5004 6614h       |
| EPWM6_G2      | 5008 6614h       |
| EPWM6_G3      | 500C 6614h       |
| EPWM7_G0      | 5000 7614h       |
| EPWM7_G1      | 5004 7614h       |
| EPWM7_G2      | 5008 7614h       |
| EPWM7_G3      | 500C 7614h       |
| EPWM8_G0      | 5000 8614h       |
| EPWM8_G1      | 5004 8614h       |
| EPWM8_G2      | 5008 8614h       |
| EPWM8_G3      | 500C 8614h       |
| EPWM9_G0      | 5000 9614h       |
| EPWM9_G1      | 5004 9614h       |
| EPWM9_G2      | 5008 9614h       |

**Table 3-1144. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9614h       |
| EPWM10_G0     | 5000 A614h       |
| EPWM10_G1     | 5004 A614h       |
| EPWM10_G2     | 5008 A614h       |
| EPWM10_G3     | 500C A614h       |
| EPWM11_G0     | 5000 B614h       |
| EPWM11_G1     | 5004 B614h       |
| EPWM11_G2     | 5008 B614h       |
| EPWM11_G3     | 500C B614h       |
| EPWM12_G0     | 5000 C614h       |
| EPWM12_G1     | 5004 C614h       |
| EPWM12_G2     | 5008 C614h       |
| EPWM12_G3     | 500C C614h       |
| EPWM13_G0     | 5000 D614h       |
| EPWM13_G1     | 5004 D614h       |
| EPWM13_G2     | 5008 D614h       |
| EPWM13_G3     | 500C D614h       |
| EPWM14_G0     | 5000 E614h       |
| EPWM14_G1     | 5004 E614h       |
| EPWM14_G2     | 5008 E614h       |
| EPWM14_G3     | 500C E614h       |
| EPWM15_G0     | 5000 F614h       |
| EPWM15_G1     | 5004 F614h       |
| EPWM15_G2     | 5008 F614h       |
| EPWM15_G3     | 500C F614h       |
| EPWM16_G0     | 5001 0614h       |
| EPWM16_G1     | 5005 0614h       |
| EPWM16_G2     | 5009 0614h       |
| EPWM16_G3     | 500D 0614h       |
| EPWM17_G0     | 5001 1614h       |
| EPWM17_G1     | 5005 1614h       |
| EPWM17_G2     | 5009 1614h       |
| EPWM17_G3     | 500D 1614h       |
| EPWM18_G0     | 5001 2614h       |
| EPWM18_G1     | 5005 2614h       |
| EPWM18_G2     | 5009 2614h       |
| EPWM18_G3     | 500D 2614h       |
| EPWM19_G0     | 5001 3614h       |
| EPWM19_G1     | 5005 3614h       |
| EPWM19_G2     | 5009 3614h       |
| EPWM19_G3     | 500D 3614h       |
| EPWM20_G0     | 5001 4614h       |
| EPWM20_G1     | 5005 4614h       |
| EPWM20_G2     | 5009 4614h       |
| EPWM20_G3     | 500D 4614h       |



**Table 3-1144. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5614h       |
| EPWM21_G1     | 5005 5614h       |
| EPWM21_G2     | 5009 5614h       |
| EPWM21_G3     | 500D 5614h       |
| EPWM22_G0     | 5001 6614h       |
| EPWM22_G1     | 5005 6614h       |
| EPWM22_G2     | 5009 6614h       |
| EPWM22_G3     | 500D 6614h       |
| EPWM23_G0     | 5001 7614h       |
| EPWM23_G1     | 5005 7614h       |
| EPWM23_G2     | 5009 7614h       |
| EPWM23_G3     | 500D 7614h       |
| EPWM24_G0     | 5001 8614h       |
| EPWM24_G1     | 5005 8614h       |
| EPWM24_G2     | 5009 8614h       |
| EPWM24_G3     | 500D 8614h       |
| EPWM25_G0     | 5001 9614h       |
| EPWM25_G1     | 5005 9614h       |
| EPWM25_G2     | 5009 9614h       |
| EPWM25_G3     | 500D 9614h       |
| EPWM26_G0     | 5001 A614h       |
| EPWM26_G1     | 5005 A614h       |
| EPWM26_G2     | 5009 A614h       |
| EPWM26_G3     | 500D A614h       |
| EPWM27_G0     | 5001 B614h       |
| EPWM27_G1     | 5005 B614h       |
| EPWM27_G2     | 5009 B614h       |
| EPWM27_G3     | 500D B614h       |
| EPWM28_G0     | 5001 C614h       |
| EPWM28_G1     | 5005 C614h       |
| EPWM28_G2     | 5009 C614h       |
| EPWM28_G3     | 500D C614h       |
| EPWM29_G0     | 5001 D614h       |
| EPWM29_G1     | 5005 D614h       |
| EPWM29_G2     | 5009 D614h       |
| EPWM29_G3     | 500D D614h       |
| EPWM30_G0     | 5001 E614h       |
| EPWM30_G1     | 5005 E614h       |
| EPWM30_G2     | 5009 E614h       |
| EPWM30_G3     | 500D E614h       |
| EPWM31_G0     | 5001 F614h       |
| EPWM31_G1     | 5005 F614h       |
| EPWM31_G2     | 5009 F614h       |
| EPWM31_G3     | 500D F614h       |

**Figure 3-362. EPWM\_XCMP6\_ACTIVE Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP6_ACTIVE   |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP6_ACTIVE   |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP6HR_ACTIVE |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP6HR_ACTIVE |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 3-1146. EPWM\_XCMP6\_ACTIVE Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                              |
|-------|----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP6_ACTIVE   | R/W  | 0h    | XCMP6_ACTIVE Register<br>The value in the XCMP6_ACTIVE register is loaded into CMPA/B [shadow/active] registers when shadow to active load occurs.       |
| 15:0  | XCMP6HR_ACTIVE | R/W  | 0h    | XCMP6HR_ACTIVE Register<br>The value in the XCMP6HR_ACTIVE register is loaded into CMPA/BHR [shadow/active] registers when shadow to active load occurs. |

### 3.7.2.112 EPWM\_XCMP7\_ACTIVE Register

#### 1 EPWM\_XCMP7\_ACTIVE Register (Offset = 618h) [reset = 0h]

Additional Compare 7 Active Register.

Return to [Summary Table](#)

**Table 3-1147. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0618h       |
| EPWM0_G1      | 5004 0618h       |
| EPWM0_G2      | 5008 0618h       |
| EPWM0_G3      | 500C 0618h       |
| EPWM1_G0      | 5000 1618h       |
| EPWM1_G1      | 5004 1618h       |
| EPWM1_G2      | 5008 1618h       |
| EPWM1_G3      | 500C 1618h       |
| EPWM2_G0      | 5000 2618h       |
| EPWM2_G1      | 5004 2618h       |
| EPWM2_G2      | 5008 2618h       |
| EPWM2_G3      | 500C 2618h       |
| EPWM3_G0      | 5000 3618h       |
| EPWM3_G1      | 5004 3618h       |
| EPWM3_G2      | 5008 3618h       |
| EPWM3_G3      | 500C 3618h       |
| EPWM4_G0      | 5000 4618h       |
| EPWM4_G1      | 5004 4618h       |
| EPWM4_G2      | 5008 4618h       |
| EPWM4_G3      | 500C 4618h       |
| EPWM5_G0      | 5000 5618h       |
| EPWM5_G1      | 5004 5618h       |
| EPWM5_G2      | 5008 5618h       |
| EPWM5_G3      | 500C 5618h       |
| EPWM6_G0      | 5000 6618h       |
| EPWM6_G1      | 5004 6618h       |
| EPWM6_G2      | 5008 6618h       |
| EPWM6_G3      | 500C 6618h       |
| EPWM7_G0      | 5000 7618h       |
| EPWM7_G1      | 5004 7618h       |
| EPWM7_G2      | 5008 7618h       |
| EPWM7_G3      | 500C 7618h       |
| EPWM8_G0      | 5000 8618h       |
| EPWM8_G1      | 5004 8618h       |
| EPWM8_G2      | 5008 8618h       |
| EPWM8_G3      | 500C 8618h       |
| EPWM9_G0      | 5000 9618h       |
| EPWM9_G1      | 5004 9618h       |
| EPWM9_G2      | 5008 9618h       |

**Table 3-1147. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9618h       |
| EPWM10_G0     | 5000 A618h       |
| EPWM10_G1     | 5004 A618h       |
| EPWM10_G2     | 5008 A618h       |
| EPWM10_G3     | 500C A618h       |
| EPWM11_G0     | 5000 B618h       |
| EPWM11_G1     | 5004 B618h       |
| EPWM11_G2     | 5008 B618h       |
| EPWM11_G3     | 500C B618h       |
| EPWM12_G0     | 5000 C618h       |
| EPWM12_G1     | 5004 C618h       |
| EPWM12_G2     | 5008 C618h       |
| EPWM12_G3     | 500C C618h       |
| EPWM13_G0     | 5000 D618h       |
| EPWM13_G1     | 5004 D618h       |
| EPWM13_G2     | 5008 D618h       |
| EPWM13_G3     | 500C D618h       |
| EPWM14_G0     | 5000 E618h       |
| EPWM14_G1     | 5004 E618h       |
| EPWM14_G2     | 5008 E618h       |
| EPWM14_G3     | 500C E618h       |
| EPWM15_G0     | 5000 F618h       |
| EPWM15_G1     | 5004 F618h       |
| EPWM15_G2     | 5008 F618h       |
| EPWM15_G3     | 500C F618h       |
| EPWM16_G0     | 5001 0618h       |
| EPWM16_G1     | 5005 0618h       |
| EPWM16_G2     | 5009 0618h       |
| EPWM16_G3     | 500D 0618h       |
| EPWM17_G0     | 5001 1618h       |
| EPWM17_G1     | 5005 1618h       |
| EPWM17_G2     | 5009 1618h       |
| EPWM17_G3     | 500D 1618h       |
| EPWM18_G0     | 5001 2618h       |
| EPWM18_G1     | 5005 2618h       |
| EPWM18_G2     | 5009 2618h       |
| EPWM18_G3     | 500D 2618h       |
| EPWM19_G0     | 5001 3618h       |
| EPWM19_G1     | 5005 3618h       |
| EPWM19_G2     | 5009 3618h       |
| EPWM19_G3     | 500D 3618h       |
| EPWM20_G0     | 5001 4618h       |
| EPWM20_G1     | 5005 4618h       |
| EPWM20_G2     | 5009 4618h       |
| EPWM20_G3     | 500D 4618h       |

**Table 3-1147. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5618h       |
| EPWM21_G1     | 5005 5618h       |
| EPWM21_G2     | 5009 5618h       |
| EPWM21_G3     | 500D 5618h       |
| EPWM22_G0     | 5001 6618h       |
| EPWM22_G1     | 5005 6618h       |
| EPWM22_G2     | 5009 6618h       |
| EPWM22_G3     | 500D 6618h       |
| EPWM23_G0     | 5001 7618h       |
| EPWM23_G1     | 5005 7618h       |
| EPWM23_G2     | 5009 7618h       |
| EPWM23_G3     | 500D 7618h       |
| EPWM24_G0     | 5001 8618h       |
| EPWM24_G1     | 5005 8618h       |
| EPWM24_G2     | 5009 8618h       |
| EPWM24_G3     | 500D 8618h       |
| EPWM25_G0     | 5001 9618h       |
| EPWM25_G1     | 5005 9618h       |
| EPWM25_G2     | 5009 9618h       |
| EPWM25_G3     | 500D 9618h       |
| EPWM26_G0     | 5001 A618h       |
| EPWM26_G1     | 5005 A618h       |
| EPWM26_G2     | 5009 A618h       |
| EPWM26_G3     | 500D A618h       |
| EPWM27_G0     | 5001 B618h       |
| EPWM27_G1     | 5005 B618h       |
| EPWM27_G2     | 5009 B618h       |
| EPWM27_G3     | 500D B618h       |
| EPWM28_G0     | 5001 C618h       |
| EPWM28_G1     | 5005 C618h       |
| EPWM28_G2     | 5009 C618h       |
| EPWM28_G3     | 500D C618h       |
| EPWM29_G0     | 5001 D618h       |
| EPWM29_G1     | 5005 D618h       |
| EPWM29_G2     | 5009 D618h       |
| EPWM29_G3     | 500D D618h       |
| EPWM30_G0     | 5001 E618h       |
| EPWM30_G1     | 5005 E618h       |
| EPWM30_G2     | 5009 E618h       |
| EPWM30_G3     | 500D E618h       |
| EPWM31_G0     | 5001 F618h       |
| EPWM31_G1     | 5005 F618h       |
| EPWM31_G2     | 5009 F618h       |
| EPWM31_G3     | 500D F618h       |

**Figure 3-363. EPWM\_XCMP7\_ACTIVE Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP7_ACTIVE   |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP7_ACTIVE   |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP7HR_ACTIVE |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP7HR_ACTIVE |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 3-1149. EPWM\_XCMP7\_ACTIVE Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                              |
|-------|----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP7_ACTIVE   | R/W  | 0h    | XCMP7_ACTIVE Register<br>The value in the XCMP7_ACTIVE register is loaded into CMPA/B [shadow/active] registers when shadow to active load occurs.       |
| 15:0  | XCMP7HR_ACTIVE | R/W  | 0h    | XCMP7HR_ACTIVE Register<br>The value in the XCMP7HR_ACTIVE register is loaded into CMPA/BHR [shadow/active] registers when shadow to active load occurs. |

### 3.7.2.113 EPWM\_XCMP8\_ACTIVE Register

#### 1 EPWM\_XCMP8\_ACTIVE Register (Offset = 61Ch) [reset = 0h]

Additional Compare 8 Active Register.

Return to [Summary Table](#)

**Table 3-1150. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 061Ch       |
| EPWM0_G1      | 5004 061Ch       |
| EPWM0_G2      | 5008 061Ch       |
| EPWM0_G3      | 500C 061Ch       |
| EPWM1_G0      | 5000 161Ch       |
| EPWM1_G1      | 5004 161Ch       |
| EPWM1_G2      | 5008 161Ch       |
| EPWM1_G3      | 500C 161Ch       |
| EPWM2_G0      | 5000 261Ch       |
| EPWM2_G1      | 5004 261Ch       |
| EPWM2_G2      | 5008 261Ch       |
| EPWM2_G3      | 500C 261Ch       |
| EPWM3_G0      | 5000 361Ch       |
| EPWM3_G1      | 5004 361Ch       |
| EPWM3_G2      | 5008 361Ch       |
| EPWM3_G3      | 500C 361Ch       |
| EPWM4_G0      | 5000 461Ch       |
| EPWM4_G1      | 5004 461Ch       |
| EPWM4_G2      | 5008 461Ch       |
| EPWM4_G3      | 500C 461Ch       |
| EPWM5_G0      | 5000 561Ch       |
| EPWM5_G1      | 5004 561Ch       |
| EPWM5_G2      | 5008 561Ch       |
| EPWM5_G3      | 500C 561Ch       |
| EPWM6_G0      | 5000 661Ch       |
| EPWM6_G1      | 5004 661Ch       |
| EPWM6_G2      | 5008 661Ch       |
| EPWM6_G3      | 500C 661Ch       |
| EPWM7_G0      | 5000 761Ch       |
| EPWM7_G1      | 5004 761Ch       |
| EPWM7_G2      | 5008 761Ch       |
| EPWM7_G3      | 500C 761Ch       |
| EPWM8_G0      | 5000 861Ch       |
| EPWM8_G1      | 5004 861Ch       |
| EPWM8_G2      | 5008 861Ch       |
| EPWM8_G3      | 500C 861Ch       |
| EPWM9_G0      | 5000 961Ch       |
| EPWM9_G1      | 5004 961Ch       |
| EPWM9_G2      | 5008 961Ch       |

**Table 3-1150. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 961Ch       |
| EPWM10_G0     | 5000 A61Ch       |
| EPWM10_G1     | 5004 A61Ch       |
| EPWM10_G2     | 5008 A61Ch       |
| EPWM10_G3     | 500C A61Ch       |
| EPWM11_G0     | 5000 B61Ch       |
| EPWM11_G1     | 5004 B61Ch       |
| EPWM11_G2     | 5008 B61Ch       |
| EPWM11_G3     | 500C B61Ch       |
| EPWM12_G0     | 5000 C61Ch       |
| EPWM12_G1     | 5004 C61Ch       |
| EPWM12_G2     | 5008 C61Ch       |
| EPWM12_G3     | 500C C61Ch       |
| EPWM13_G0     | 5000 D61Ch       |
| EPWM13_G1     | 5004 D61Ch       |
| EPWM13_G2     | 5008 D61Ch       |
| EPWM13_G3     | 500C D61Ch       |
| EPWM14_G0     | 5000 E61Ch       |
| EPWM14_G1     | 5004 E61Ch       |
| EPWM14_G2     | 5008 E61Ch       |
| EPWM14_G3     | 500C E61Ch       |
| EPWM15_G0     | 5000 F61Ch       |
| EPWM15_G1     | 5004 F61Ch       |
| EPWM15_G2     | 5008 F61Ch       |
| EPWM15_G3     | 500C F61Ch       |
| EPWM16_G0     | 5001 061Ch       |
| EPWM16_G1     | 5005 061Ch       |
| EPWM16_G2     | 5009 061Ch       |
| EPWM16_G3     | 500D 061Ch       |
| EPWM17_G0     | 5001 161Ch       |
| EPWM17_G1     | 5005 161Ch       |
| EPWM17_G2     | 5009 161Ch       |
| EPWM17_G3     | 500D 161Ch       |
| EPWM18_G0     | 5001 261Ch       |
| EPWM18_G1     | 5005 261Ch       |
| EPWM18_G2     | 5009 261Ch       |
| EPWM18_G3     | 500D 261Ch       |
| EPWM19_G0     | 5001 361Ch       |
| EPWM19_G1     | 5005 361Ch       |
| EPWM19_G2     | 5009 361Ch       |
| EPWM19_G3     | 500D 361Ch       |
| EPWM20_G0     | 5001 461Ch       |
| EPWM20_G1     | 5005 461Ch       |
| EPWM20_G2     | 5009 461Ch       |
| EPWM20_G3     | 500D 461Ch       |



**Table 3-1150. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 561Ch       |
| EPWM21_G1     | 5005 561Ch       |
| EPWM21_G2     | 5009 561Ch       |
| EPWM21_G3     | 500D 561Ch       |
| EPWM22_G0     | 5001 661Ch       |
| EPWM22_G1     | 5005 661Ch       |
| EPWM22_G2     | 5009 661Ch       |
| EPWM22_G3     | 500D 661Ch       |
| EPWM23_G0     | 5001 761Ch       |
| EPWM23_G1     | 5005 761Ch       |
| EPWM23_G2     | 5009 761Ch       |
| EPWM23_G3     | 500D 761Ch       |
| EPWM24_G0     | 5001 861Ch       |
| EPWM24_G1     | 5005 861Ch       |
| EPWM24_G2     | 5009 861Ch       |
| EPWM24_G3     | 500D 861Ch       |
| EPWM25_G0     | 5001 961Ch       |
| EPWM25_G1     | 5005 961Ch       |
| EPWM25_G2     | 5009 961Ch       |
| EPWM25_G3     | 500D 961Ch       |
| EPWM26_G0     | 5001 A61Ch       |
| EPWM26_G1     | 5005 A61Ch       |
| EPWM26_G2     | 5009 A61Ch       |
| EPWM26_G3     | 500D A61Ch       |
| EPWM27_G0     | 5001 B61Ch       |
| EPWM27_G1     | 5005 B61Ch       |
| EPWM27_G2     | 5009 B61Ch       |
| EPWM27_G3     | 500D B61Ch       |
| EPWM28_G0     | 5001 C61Ch       |
| EPWM28_G1     | 5005 C61Ch       |
| EPWM28_G2     | 5009 C61Ch       |
| EPWM28_G3     | 500D C61Ch       |
| EPWM29_G0     | 5001 D61Ch       |
| EPWM29_G1     | 5005 D61Ch       |
| EPWM29_G2     | 5009 D61Ch       |
| EPWM29_G3     | 500D D61Ch       |
| EPWM30_G0     | 5001 E61Ch       |
| EPWM30_G1     | 5005 E61Ch       |
| EPWM30_G2     | 5009 E61Ch       |
| EPWM30_G3     | 500D E61Ch       |
| EPWM31_G0     | 5001 F61Ch       |
| EPWM31_G1     | 5005 F61Ch       |
| EPWM31_G2     | 5009 F61Ch       |
| EPWM31_G3     | 500D F61Ch       |

**Figure 3-364. EPWM\_XCMP8\_ACTIVE Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP8_ACTIVE   |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP8_ACTIVE   |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP8HR_ACTIVE |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP8HR_ACTIVE |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 3-1152. EPWM\_XCMP8\_ACTIVE Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                              |
|-------|----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP8_ACTIVE   | R/W  | 0h    | XCMP8_ACTIVE Register<br>The value in the XCMP8_ACTIVE register is loaded into CMPA/B [shadow/active] registers when shadow to active load occurs.       |
| 15:0  | XCMP8HR_ACTIVE | R/W  | 0h    | XCMP8HR_ACTIVE Register<br>The value in the XCMP8HR_ACTIVE register is loaded into CMPA/BHR [shadow/active] registers when shadow to active load occurs. |

### 3.7.2.114 EPWM\_XTBPRD\_ACTIVE Register

#### 1 EPWM\_XTBPRD\_ACTIVE Register (Offset = 620h) [reset = 0h]

Additional Time Base Period Active Register.

Return to [Summary Table](#)

**Table 3-1153. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0620h       |
| EPWM0_G1      | 5004 0620h       |
| EPWM0_G2      | 5008 0620h       |
| EPWM0_G3      | 500C 0620h       |
| EPWM1_G0      | 5000 1620h       |
| EPWM1_G1      | 5004 1620h       |
| EPWM1_G2      | 5008 1620h       |
| EPWM1_G3      | 500C 1620h       |
| EPWM2_G0      | 5000 2620h       |
| EPWM2_G1      | 5004 2620h       |
| EPWM2_G2      | 5008 2620h       |
| EPWM2_G3      | 500C 2620h       |
| EPWM3_G0      | 5000 3620h       |
| EPWM3_G1      | 5004 3620h       |
| EPWM3_G2      | 5008 3620h       |
| EPWM3_G3      | 500C 3620h       |
| EPWM4_G0      | 5000 4620h       |
| EPWM4_G1      | 5004 4620h       |
| EPWM4_G2      | 5008 4620h       |
| EPWM4_G3      | 500C 4620h       |
| EPWM5_G0      | 5000 5620h       |
| EPWM5_G1      | 5004 5620h       |
| EPWM5_G2      | 5008 5620h       |
| EPWM5_G3      | 500C 5620h       |
| EPWM6_G0      | 5000 6620h       |
| EPWM6_G1      | 5004 6620h       |
| EPWM6_G2      | 5008 6620h       |
| EPWM6_G3      | 500C 6620h       |
| EPWM7_G0      | 5000 7620h       |
| EPWM7_G1      | 5004 7620h       |
| EPWM7_G2      | 5008 7620h       |
| EPWM7_G3      | 500C 7620h       |
| EPWM8_G0      | 5000 8620h       |
| EPWM8_G1      | 5004 8620h       |
| EPWM8_G2      | 5008 8620h       |
| EPWM8_G3      | 500C 8620h       |
| EPWM9_G0      | 5000 9620h       |
| EPWM9_G1      | 5004 9620h       |
| EPWM9_G2      | 5008 9620h       |

**Table 3-1153. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9620h       |
| EPWM10_G0     | 5000 A620h       |
| EPWM10_G1     | 5004 A620h       |
| EPWM10_G2     | 5008 A620h       |
| EPWM10_G3     | 500C A620h       |
| EPWM11_G0     | 5000 B620h       |
| EPWM11_G1     | 5004 B620h       |
| EPWM11_G2     | 5008 B620h       |
| EPWM11_G3     | 500C B620h       |
| EPWM12_G0     | 5000 C620h       |
| EPWM12_G1     | 5004 C620h       |
| EPWM12_G2     | 5008 C620h       |
| EPWM12_G3     | 500C C620h       |
| EPWM13_G0     | 5000 D620h       |
| EPWM13_G1     | 5004 D620h       |
| EPWM13_G2     | 5008 D620h       |
| EPWM13_G3     | 500C D620h       |
| EPWM14_G0     | 5000 E620h       |
| EPWM14_G1     | 5004 E620h       |
| EPWM14_G2     | 5008 E620h       |
| EPWM14_G3     | 500C E620h       |
| EPWM15_G0     | 5000 F620h       |
| EPWM15_G1     | 5004 F620h       |
| EPWM15_G2     | 5008 F620h       |
| EPWM15_G3     | 500C F620h       |
| EPWM16_G0     | 5001 0620h       |
| EPWM16_G1     | 5005 0620h       |
| EPWM16_G2     | 5009 0620h       |
| EPWM16_G3     | 500D 0620h       |
| EPWM17_G0     | 5001 1620h       |
| EPWM17_G1     | 5005 1620h       |
| EPWM17_G2     | 5009 1620h       |
| EPWM17_G3     | 500D 1620h       |
| EPWM18_G0     | 5001 2620h       |
| EPWM18_G1     | 5005 2620h       |
| EPWM18_G2     | 5009 2620h       |
| EPWM18_G3     | 500D 2620h       |
| EPWM19_G0     | 5001 3620h       |
| EPWM19_G1     | 5005 3620h       |
| EPWM19_G2     | 5009 3620h       |
| EPWM19_G3     | 500D 3620h       |
| EPWM20_G0     | 5001 4620h       |
| EPWM20_G1     | 5005 4620h       |
| EPWM20_G2     | 5009 4620h       |
| EPWM20_G3     | 500D 4620h       |

**Table 3-1153. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5620h       |
| EPWM21_G1     | 5005 5620h       |
| EPWM21_G2     | 5009 5620h       |
| EPWM21_G3     | 500D 5620h       |
| EPWM22_G0     | 5001 6620h       |
| EPWM22_G1     | 5005 6620h       |
| EPWM22_G2     | 5009 6620h       |
| EPWM22_G3     | 500D 6620h       |
| EPWM23_G0     | 5001 7620h       |
| EPWM23_G1     | 5005 7620h       |
| EPWM23_G2     | 5009 7620h       |
| EPWM23_G3     | 500D 7620h       |
| EPWM24_G0     | 5001 8620h       |
| EPWM24_G1     | 5005 8620h       |
| EPWM24_G2     | 5009 8620h       |
| EPWM24_G3     | 500D 8620h       |
| EPWM25_G0     | 5001 9620h       |
| EPWM25_G1     | 5005 9620h       |
| EPWM25_G2     | 5009 9620h       |
| EPWM25_G3     | 500D 9620h       |
| EPWM26_G0     | 5001 A620h       |
| EPWM26_G1     | 5005 A620h       |
| EPWM26_G2     | 5009 A620h       |
| EPWM26_G3     | 500D A620h       |
| EPWM27_G0     | 5001 B620h       |
| EPWM27_G1     | 5005 B620h       |
| EPWM27_G2     | 5009 B620h       |
| EPWM27_G3     | 500D B620h       |
| EPWM28_G0     | 5001 C620h       |
| EPWM28_G1     | 5005 C620h       |
| EPWM28_G2     | 5009 C620h       |
| EPWM28_G3     | 500D C620h       |
| EPWM29_G0     | 5001 D620h       |
| EPWM29_G1     | 5005 D620h       |
| EPWM29_G2     | 5009 D620h       |
| EPWM29_G3     | 500D D620h       |
| EPWM30_G0     | 5001 E620h       |
| EPWM30_G1     | 5005 E620h       |
| EPWM30_G2     | 5009 E620h       |
| EPWM30_G3     | 500D E620h       |
| EPWM31_G0     | 5001 F620h       |
| EPWM31_G1     | 5005 F620h       |
| EPWM31_G2     | 5009 F620h       |
| EPWM31_G3     | 500D F620h       |

**Figure 3-365. EPWM\_XTBPRD\_ACTIVE Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XTBPRD_ACTIVE   |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XTBPRD_ACTIVE   |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XTBPRDHR_ACTIVE |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XTBPRDHR_ACTIVE |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-1155. EPWM\_XTBPRD\_ACTIVE Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                   |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XTBPRD_ACTIVE   | R/W  | 0h    | The value in the XTBPRD_ACTIVE register is loaded into TBPRD [shadow/active] registers when shadow to active load occurs.     |
| 15:0  | XTBPRDHR_ACTIVE | R/W  | 0h    | The value in the XTBPRDHR_ACTIVE register is loaded into TBPRDHR [shadow/active] registers when shadow to active load occurs. |

### 3.7.2.115 EPWM\_XAQCTLA\_ACTIVE Register

#### 1 EPWM\_XAQCTLA\_ACTIVE Register (Offset = 630h) [reset = 0h]

AQCTLA Active Register.

Return to [Summary Table](#)

**Table 3-1156. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0630h       |
| EPWM0_G1      | 5004 0630h       |
| EPWM0_G2      | 5008 0630h       |
| EPWM0_G3      | 500C 0630h       |
| EPWM1_G0      | 5000 1630h       |
| EPWM1_G1      | 5004 1630h       |
| EPWM1_G2      | 5008 1630h       |
| EPWM1_G3      | 500C 1630h       |
| EPWM2_G0      | 5000 2630h       |
| EPWM2_G1      | 5004 2630h       |
| EPWM2_G2      | 5008 2630h       |
| EPWM2_G3      | 500C 2630h       |
| EPWM3_G0      | 5000 3630h       |
| EPWM3_G1      | 5004 3630h       |
| EPWM3_G2      | 5008 3630h       |
| EPWM3_G3      | 500C 3630h       |
| EPWM4_G0      | 5000 4630h       |
| EPWM4_G1      | 5004 4630h       |
| EPWM4_G2      | 5008 4630h       |
| EPWM4_G3      | 500C 4630h       |
| EPWM5_G0      | 5000 5630h       |
| EPWM5_G1      | 5004 5630h       |
| EPWM5_G2      | 5008 5630h       |
| EPWM5_G3      | 500C 5630h       |
| EPWM6_G0      | 5000 6630h       |
| EPWM6_G1      | 5004 6630h       |
| EPWM6_G2      | 5008 6630h       |
| EPWM6_G3      | 500C 6630h       |
| EPWM7_G0      | 5000 7630h       |
| EPWM7_G1      | 5004 7630h       |
| EPWM7_G2      | 5008 7630h       |
| EPWM7_G3      | 500C 7630h       |
| EPWM8_G0      | 5000 8630h       |
| EPWM8_G1      | 5004 8630h       |
| EPWM8_G2      | 5008 8630h       |
| EPWM8_G3      | 500C 8630h       |
| EPWM9_G0      | 5000 9630h       |
| EPWM9_G1      | 5004 9630h       |
| EPWM9_G2      | 5008 9630h       |

**Table 3-1156. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9630h       |
| EPWM10_G0     | 5000 A630h       |
| EPWM10_G1     | 5004 A630h       |
| EPWM10_G2     | 5008 A630h       |
| EPWM10_G3     | 500C A630h       |
| EPWM11_G0     | 5000 B630h       |
| EPWM11_G1     | 5004 B630h       |
| EPWM11_G2     | 5008 B630h       |
| EPWM11_G3     | 500C B630h       |
| EPWM12_G0     | 5000 C630h       |
| EPWM12_G1     | 5004 C630h       |
| EPWM12_G2     | 5008 C630h       |
| EPWM12_G3     | 500C C630h       |
| EPWM13_G0     | 5000 D630h       |
| EPWM13_G1     | 5004 D630h       |
| EPWM13_G2     | 5008 D630h       |
| EPWM13_G3     | 500C D630h       |
| EPWM14_G0     | 5000 E630h       |
| EPWM14_G1     | 5004 E630h       |
| EPWM14_G2     | 5008 E630h       |
| EPWM14_G3     | 500C E630h       |
| EPWM15_G0     | 5000 F630h       |
| EPWM15_G1     | 5004 F630h       |
| EPWM15_G2     | 5008 F630h       |
| EPWM15_G3     | 500C F630h       |
| EPWM16_G0     | 5001 0630h       |
| EPWM16_G1     | 5005 0630h       |
| EPWM16_G2     | 5009 0630h       |
| EPWM16_G3     | 500D 0630h       |
| EPWM17_G0     | 5001 1630h       |
| EPWM17_G1     | 5005 1630h       |
| EPWM17_G2     | 5009 1630h       |
| EPWM17_G3     | 500D 1630h       |
| EPWM18_G0     | 5001 2630h       |
| EPWM18_G1     | 5005 2630h       |
| EPWM18_G2     | 5009 2630h       |
| EPWM18_G3     | 500D 2630h       |
| EPWM19_G0     | 5001 3630h       |
| EPWM19_G1     | 5005 3630h       |
| EPWM19_G2     | 5009 3630h       |
| EPWM19_G3     | 500D 3630h       |
| EPWM20_G0     | 5001 4630h       |
| EPWM20_G1     | 5005 4630h       |
| EPWM20_G2     | 5009 4630h       |
| EPWM20_G3     | 500D 4630h       |



**Table 3-1156. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5630h       |
| EPWM21_G1     | 5005 5630h       |
| EPWM21_G2     | 5009 5630h       |
| EPWM21_G3     | 500D 5630h       |
| EPWM22_G0     | 5001 6630h       |
| EPWM22_G1     | 5005 6630h       |
| EPWM22_G2     | 5009 6630h       |
| EPWM22_G3     | 500D 6630h       |
| EPWM23_G0     | 5001 7630h       |
| EPWM23_G1     | 5005 7630h       |
| EPWM23_G2     | 5009 7630h       |
| EPWM23_G3     | 500D 7630h       |
| EPWM24_G0     | 5001 8630h       |
| EPWM24_G1     | 5005 8630h       |
| EPWM24_G2     | 5009 8630h       |
| EPWM24_G3     | 500D 8630h       |
| EPWM25_G0     | 5001 9630h       |
| EPWM25_G1     | 5005 9630h       |
| EPWM25_G2     | 5009 9630h       |
| EPWM25_G3     | 500D 9630h       |
| EPWM26_G0     | 5001 A630h       |
| EPWM26_G1     | 5005 A630h       |
| EPWM26_G2     | 5009 A630h       |
| EPWM26_G3     | 500D A630h       |
| EPWM27_G0     | 5001 B630h       |
| EPWM27_G1     | 5005 B630h       |
| EPWM27_G2     | 5009 B630h       |
| EPWM27_G3     | 500D B630h       |
| EPWM28_G0     | 5001 C630h       |
| EPWM28_G1     | 5005 C630h       |
| EPWM28_G2     | 5009 C630h       |
| EPWM28_G3     | 500D C630h       |
| EPWM29_G0     | 5001 D630h       |
| EPWM29_G1     | 5005 D630h       |
| EPWM29_G2     | 5009 D630h       |
| EPWM29_G3     | 500D D630h       |
| EPWM30_G0     | 5001 E630h       |
| EPWM30_G1     | 5005 E630h       |
| EPWM30_G2     | 5009 E630h       |
| EPWM30_G3     | 500D E630h       |
| EPWM31_G0     | 5001 F630h       |
| EPWM31_G1     | 5005 F630h       |
| EPWM31_G2     | 5009 F630h       |
| EPWM31_G3     | 500D F630h       |

**Figure 3-366. EPWM\_XAQCTLA\_ACTIVE Name Register**

| 15    | 14 | 13    | 12 | 11    | 10 | 9     | 8 |
|-------|----|-------|----|-------|----|-------|---|
| XCMP8 |    | XCMP7 |    | XCMP6 |    | XCMP5 |   |
| R/W   |    | R/W   |    | R/W   |    | R/W   |   |
| 0h    |    | 0h    |    | 0h    |    | 0h    |   |
| 7     | 6  | 5     | 4  | 3     | 2  | 1     | 0 |
| XCMP4 |    | XCMP3 |    | XCMP2 |    | XCMP1 |   |
| R/W   |    | R/W   |    | R/W   |    | R/W   |   |
| 0h    |    | 0h    |    | 0h    |    | 0h    |   |

**Table 3-1158. EPWM\_XAQCTLA\_ACTIVE Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                          |
|-------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | XCMP8 | R/W  | 0h    | Action when Counter = CMP8<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 13:12 | XCMP7 | R/W  | 0h    | Action when Counter = CMP7<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 11:10 | XCMP6 | R/W  | 0h    | Action when Counter = CMP6<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 9:8   | XCMP5 | R/W  | 0h    | Action when Counter = CMP5<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 7:6   | XCMP4 | R/W  | 0h    | Action when Counter = CMP4<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 5:4   | XCMP3 | R/W  | 0h    | Action when Counter = CMP3<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 3:2   | XCMP2 | R/W  | 0h    | Action when Counter = CMP2<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 1:0   | XCMP1 | R/W  | 0h    | Action when Counter = CMP1<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |

### 3.7.2.116 EPWM\_XAQCTLB\_ACTIVE Register

#### 1 EPWM\_XAQCTLB\_ACTIVE Register (Offset = 632h) [reset = 0h]

AQCTLB Active Register.

Return to [Summary Table](#)

**Table 3-1159. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0632h       |
| EPWM0_G1      | 5004 0632h       |
| EPWM0_G2      | 5008 0632h       |
| EPWM0_G3      | 500C 0632h       |
| EPWM1_G0      | 5000 1632h       |
| EPWM1_G1      | 5004 1632h       |
| EPWM1_G2      | 5008 1632h       |
| EPWM1_G3      | 500C 1632h       |
| EPWM2_G0      | 5000 2632h       |
| EPWM2_G1      | 5004 2632h       |
| EPWM2_G2      | 5008 2632h       |
| EPWM2_G3      | 500C 2632h       |
| EPWM3_G0      | 5000 3632h       |
| EPWM3_G1      | 5004 3632h       |
| EPWM3_G2      | 5008 3632h       |
| EPWM3_G3      | 500C 3632h       |
| EPWM4_G0      | 5000 4632h       |
| EPWM4_G1      | 5004 4632h       |
| EPWM4_G2      | 5008 4632h       |
| EPWM4_G3      | 500C 4632h       |
| EPWM5_G0      | 5000 5632h       |
| EPWM5_G1      | 5004 5632h       |
| EPWM5_G2      | 5008 5632h       |
| EPWM5_G3      | 500C 5632h       |
| EPWM6_G0      | 5000 6632h       |
| EPWM6_G1      | 5004 6632h       |
| EPWM6_G2      | 5008 6632h       |
| EPWM6_G3      | 500C 6632h       |
| EPWM7_G0      | 5000 7632h       |
| EPWM7_G1      | 5004 7632h       |
| EPWM7_G2      | 5008 7632h       |
| EPWM7_G3      | 500C 7632h       |
| EPWM8_G0      | 5000 8632h       |
| EPWM8_G1      | 5004 8632h       |
| EPWM8_G2      | 5008 8632h       |
| EPWM8_G3      | 500C 8632h       |
| EPWM9_G0      | 5000 9632h       |
| EPWM9_G1      | 5004 9632h       |
| EPWM9_G2      | 5008 9632h       |

**Table 3-1159. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9632h       |
| EPWM10_G0     | 5000 A632h       |
| EPWM10_G1     | 5004 A632h       |
| EPWM10_G2     | 5008 A632h       |
| EPWM10_G3     | 500C A632h       |
| EPWM11_G0     | 5000 B632h       |
| EPWM11_G1     | 5004 B632h       |
| EPWM11_G2     | 5008 B632h       |
| EPWM11_G3     | 500C B632h       |
| EPWM12_G0     | 5000 C632h       |
| EPWM12_G1     | 5004 C632h       |
| EPWM12_G2     | 5008 C632h       |
| EPWM12_G3     | 500C C632h       |
| EPWM13_G0     | 5000 D632h       |
| EPWM13_G1     | 5004 D632h       |
| EPWM13_G2     | 5008 D632h       |
| EPWM13_G3     | 500C D632h       |
| EPWM14_G0     | 5000 E632h       |
| EPWM14_G1     | 5004 E632h       |
| EPWM14_G2     | 5008 E632h       |
| EPWM14_G3     | 500C E632h       |
| EPWM15_G0     | 5000 F632h       |
| EPWM15_G1     | 5004 F632h       |
| EPWM15_G2     | 5008 F632h       |
| EPWM15_G3     | 500C F632h       |
| EPWM16_G0     | 5001 0632h       |
| EPWM16_G1     | 5005 0632h       |
| EPWM16_G2     | 5009 0632h       |
| EPWM16_G3     | 500D 0632h       |
| EPWM17_G0     | 5001 1632h       |
| EPWM17_G1     | 5005 1632h       |
| EPWM17_G2     | 5009 1632h       |
| EPWM17_G3     | 500D 1632h       |
| EPWM18_G0     | 5001 2632h       |
| EPWM18_G1     | 5005 2632h       |
| EPWM18_G2     | 5009 2632h       |
| EPWM18_G3     | 500D 2632h       |
| EPWM19_G0     | 5001 3632h       |
| EPWM19_G1     | 5005 3632h       |
| EPWM19_G2     | 5009 3632h       |
| EPWM19_G3     | 500D 3632h       |
| EPWM20_G0     | 5001 4632h       |
| EPWM20_G1     | 5005 4632h       |
| EPWM20_G2     | 5009 4632h       |
| EPWM20_G3     | 500D 4632h       |

**Table 3-1159. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5632h       |
| EPWM21_G1     | 5005 5632h       |
| EPWM21_G2     | 5009 5632h       |
| EPWM21_G3     | 500D 5632h       |
| EPWM22_G0     | 5001 6632h       |
| EPWM22_G1     | 5005 6632h       |
| EPWM22_G2     | 5009 6632h       |
| EPWM22_G3     | 500D 6632h       |
| EPWM23_G0     | 5001 7632h       |
| EPWM23_G1     | 5005 7632h       |
| EPWM23_G2     | 5009 7632h       |
| EPWM23_G3     | 500D 7632h       |
| EPWM24_G0     | 5001 8632h       |
| EPWM24_G1     | 5005 8632h       |
| EPWM24_G2     | 5009 8632h       |
| EPWM24_G3     | 500D 8632h       |
| EPWM25_G0     | 5001 9632h       |
| EPWM25_G1     | 5005 9632h       |
| EPWM25_G2     | 5009 9632h       |
| EPWM25_G3     | 500D 9632h       |
| EPWM26_G0     | 5001 A632h       |
| EPWM26_G1     | 5005 A632h       |
| EPWM26_G2     | 5009 A632h       |
| EPWM26_G3     | 500D A632h       |
| EPWM27_G0     | 5001 B632h       |
| EPWM27_G1     | 5005 B632h       |
| EPWM27_G2     | 5009 B632h       |
| EPWM27_G3     | 500D B632h       |
| EPWM28_G0     | 5001 C632h       |
| EPWM28_G1     | 5005 C632h       |
| EPWM28_G2     | 5009 C632h       |
| EPWM28_G3     | 500D C632h       |
| EPWM29_G0     | 5001 D632h       |
| EPWM29_G1     | 5005 D632h       |
| EPWM29_G2     | 5009 D632h       |
| EPWM29_G3     | 500D D632h       |
| EPWM30_G0     | 5001 E632h       |
| EPWM30_G1     | 5005 E632h       |
| EPWM30_G2     | 5009 E632h       |
| EPWM30_G3     | 500D E632h       |
| EPWM31_G0     | 5001 F632h       |
| EPWM31_G1     | 5005 F632h       |
| EPWM31_G2     | 5009 F632h       |
| EPWM31_G3     | 500D F632h       |

**Figure 3-367. EPWM\_XAQCTLB\_ACTIVE Name Register**

|          |    |       |    |       |    |       |   |
|----------|----|-------|----|-------|----|-------|---|
| 15       | 14 | 13    | 12 | 11    | 10 | 9     | 8 |
| XCMP8    |    | XCMP7 |    | XCMP6 |    | XCMP5 |   |
| R/W      |    | R/W   |    | R/W   |    | R/W   |   |
| 0h       |    | 0h    |    | 0h    |    | 0h    |   |
| 7        | 6  | 5     | 4  | 3     | 2  | 1     | 0 |
| RESERVED |    |       |    |       |    |       |   |
| NONE     |    |       |    |       |    |       |   |
| 0h       |    |       |    |       |    |       |   |

**Table 3-1161. EPWM\_XAQCTLB\_ACTIVE Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                          |
|-------|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | XCMP8    | R/W  | 0h    | Action when Counter = CMP8<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 13:12 | XCMP7    | R/W  | 0h    | Action when Counter = CMP7<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 11:10 | XCMP6    | R/W  | 0h    | Action when Counter = CMP6<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 9:8   | XCMP5    | R/W  | 0h    | Action when Counter = CMP5<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 7:0   | RESERVED | NONE | 0h    | Reserved                                                                                                                                             |

### 3.7.2.117 EPWM\_XMINMAX\_ACTIVE Register

#### 1 EPWM\_XMINMAX\_ACTIVE Register (Offset = 644h) [reset = 0h]

XMINMAX Active Register.

Return to [Summary Table](#)

**Table 3-1162. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0644h       |
| EPWM0_G1      | 5004 0644h       |
| EPWM0_G2      | 5008 0644h       |
| EPWM0_G3      | 500C 0644h       |
| EPWM1_G0      | 5000 1644h       |
| EPWM1_G1      | 5004 1644h       |
| EPWM1_G2      | 5008 1644h       |
| EPWM1_G3      | 500C 1644h       |
| EPWM2_G0      | 5000 2644h       |
| EPWM2_G1      | 5004 2644h       |
| EPWM2_G2      | 5008 2644h       |
| EPWM2_G3      | 500C 2644h       |
| EPWM3_G0      | 5000 3644h       |
| EPWM3_G1      | 5004 3644h       |
| EPWM3_G2      | 5008 3644h       |
| EPWM3_G3      | 500C 3644h       |
| EPWM4_G0      | 5000 4644h       |
| EPWM4_G1      | 5004 4644h       |
| EPWM4_G2      | 5008 4644h       |
| EPWM4_G3      | 500C 4644h       |
| EPWM5_G0      | 5000 5644h       |
| EPWM5_G1      | 5004 5644h       |
| EPWM5_G2      | 5008 5644h       |
| EPWM5_G3      | 500C 5644h       |
| EPWM6_G0      | 5000 6644h       |
| EPWM6_G1      | 5004 6644h       |
| EPWM6_G2      | 5008 6644h       |
| EPWM6_G3      | 500C 6644h       |
| EPWM7_G0      | 5000 7644h       |
| EPWM7_G1      | 5004 7644h       |
| EPWM7_G2      | 5008 7644h       |
| EPWM7_G3      | 500C 7644h       |
| EPWM8_G0      | 5000 8644h       |
| EPWM8_G1      | 5004 8644h       |
| EPWM8_G2      | 5008 8644h       |
| EPWM8_G3      | 500C 8644h       |
| EPWM9_G0      | 5000 9644h       |
| EPWM9_G1      | 5004 9644h       |
| EPWM9_G2      | 5008 9644h       |

**Table 3-1162. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9644h       |
| EPWM10_G0     | 5000 A644h       |
| EPWM10_G1     | 5004 A644h       |
| EPWM10_G2     | 5008 A644h       |
| EPWM10_G3     | 500C A644h       |
| EPWM11_G0     | 5000 B644h       |
| EPWM11_G1     | 5004 B644h       |
| EPWM11_G2     | 5008 B644h       |
| EPWM11_G3     | 500C B644h       |
| EPWM12_G0     | 5000 C644h       |
| EPWM12_G1     | 5004 C644h       |
| EPWM12_G2     | 5008 C644h       |
| EPWM12_G3     | 500C C644h       |
| EPWM13_G0     | 5000 D644h       |
| EPWM13_G1     | 5004 D644h       |
| EPWM13_G2     | 5008 D644h       |
| EPWM13_G3     | 500C D644h       |
| EPWM14_G0     | 5000 E644h       |
| EPWM14_G1     | 5004 E644h       |
| EPWM14_G2     | 5008 E644h       |
| EPWM14_G3     | 500C E644h       |
| EPWM15_G0     | 5000 F644h       |
| EPWM15_G1     | 5004 F644h       |
| EPWM15_G2     | 5008 F644h       |
| EPWM15_G3     | 500C F644h       |
| EPWM16_G0     | 5001 0644h       |
| EPWM16_G1     | 5005 0644h       |
| EPWM16_G2     | 5009 0644h       |
| EPWM16_G3     | 500D 0644h       |
| EPWM17_G0     | 5001 1644h       |
| EPWM17_G1     | 5005 1644h       |
| EPWM17_G2     | 5009 1644h       |
| EPWM17_G3     | 500D 1644h       |
| EPWM18_G0     | 5001 2644h       |
| EPWM18_G1     | 5005 2644h       |
| EPWM18_G2     | 5009 2644h       |
| EPWM18_G3     | 500D 2644h       |
| EPWM19_G0     | 5001 3644h       |
| EPWM19_G1     | 5005 3644h       |
| EPWM19_G2     | 5009 3644h       |
| EPWM19_G3     | 500D 3644h       |
| EPWM20_G0     | 5001 4644h       |
| EPWM20_G1     | 5005 4644h       |
| EPWM20_G2     | 5009 4644h       |
| EPWM20_G3     | 500D 4644h       |



**Table 3-1162. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5644h       |
| EPWM21_G1     | 5005 5644h       |
| EPWM21_G2     | 5009 5644h       |
| EPWM21_G3     | 500D 5644h       |
| EPWM22_G0     | 5001 6644h       |
| EPWM22_G1     | 5005 6644h       |
| EPWM22_G2     | 5009 6644h       |
| EPWM22_G3     | 500D 6644h       |
| EPWM23_G0     | 5001 7644h       |
| EPWM23_G1     | 5005 7644h       |
| EPWM23_G2     | 5009 7644h       |
| EPWM23_G3     | 500D 7644h       |
| EPWM24_G0     | 5001 8644h       |
| EPWM24_G1     | 5005 8644h       |
| EPWM24_G2     | 5009 8644h       |
| EPWM24_G3     | 500D 8644h       |
| EPWM25_G0     | 5001 9644h       |
| EPWM25_G1     | 5005 9644h       |
| EPWM25_G2     | 5009 9644h       |
| EPWM25_G3     | 500D 9644h       |
| EPWM26_G0     | 5001 A644h       |
| EPWM26_G1     | 5005 A644h       |
| EPWM26_G2     | 5009 A644h       |
| EPWM26_G3     | 500D A644h       |
| EPWM27_G0     | 5001 B644h       |
| EPWM27_G1     | 5005 B644h       |
| EPWM27_G2     | 5009 B644h       |
| EPWM27_G3     | 500D B644h       |
| EPWM28_G0     | 5001 C644h       |
| EPWM28_G1     | 5005 C644h       |
| EPWM28_G2     | 5009 C644h       |
| EPWM28_G3     | 500D C644h       |
| EPWM29_G0     | 5001 D644h       |
| EPWM29_G1     | 5005 D644h       |
| EPWM29_G2     | 5009 D644h       |
| EPWM29_G3     | 500D D644h       |
| EPWM30_G0     | 5001 E644h       |
| EPWM30_G1     | 5005 E644h       |
| EPWM30_G2     | 5009 E644h       |
| EPWM30_G3     | 500D E644h       |
| EPWM31_G0     | 5001 F644h       |
| EPWM31_G1     | 5005 F644h       |
| EPWM31_G2     | 5009 F644h       |
| EPWM31_G3     | 500D F644h       |

**Figure 3-368. EPWM\_XMINMAX\_ACTIVE Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XMIN_ACTIVE |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XMIN_ACTIVE |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XMAX_ACTIVE |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XMAX_ACTIVE |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 3-1164. EPWM\_XMINMAX\_ACTIVE Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                  |
|-------|-------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XMIN_ACTIVE | R/W  | 0h    | The value in the XMIN_ACTIVE register is used for comparison against the threshold of the capture counter at any given time. |
| 15:0  | XMAX_ACTIVE | R/W  | 0h    | The value in the XMAX_ACTIVE register is used for comparison against the threshold of the capture counter at any given time. |

### 3.7.2.118 EPWM\_XCMP1\_SHDW1 Register

#### 1 EPWM\_XCMP1\_SHDW1 Register (Offset = 680h) [reset = 0h]

Additional Compare 1 Shadow 1 Register.

Return to [Summary Table](#)

**Table 3-1165. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0680h       |
| EPWM0_G1      | 5004 0680h       |
| EPWM0_G2      | 5008 0680h       |
| EPWM0_G3      | 500C 0680h       |
| EPWM1_G0      | 5000 1680h       |
| EPWM1_G1      | 5004 1680h       |
| EPWM1_G2      | 5008 1680h       |
| EPWM1_G3      | 500C 1680h       |
| EPWM2_G0      | 5000 2680h       |
| EPWM2_G1      | 5004 2680h       |
| EPWM2_G2      | 5008 2680h       |
| EPWM2_G3      | 500C 2680h       |
| EPWM3_G0      | 5000 3680h       |
| EPWM3_G1      | 5004 3680h       |
| EPWM3_G2      | 5008 3680h       |
| EPWM3_G3      | 500C 3680h       |
| EPWM4_G0      | 5000 4680h       |
| EPWM4_G1      | 5004 4680h       |
| EPWM4_G2      | 5008 4680h       |
| EPWM4_G3      | 500C 4680h       |
| EPWM5_G0      | 5000 5680h       |
| EPWM5_G1      | 5004 5680h       |
| EPWM5_G2      | 5008 5680h       |
| EPWM5_G3      | 500C 5680h       |
| EPWM6_G0      | 5000 6680h       |
| EPWM6_G1      | 5004 6680h       |
| EPWM6_G2      | 5008 6680h       |
| EPWM6_G3      | 500C 6680h       |
| EPWM7_G0      | 5000 7680h       |
| EPWM7_G1      | 5004 7680h       |
| EPWM7_G2      | 5008 7680h       |
| EPWM7_G3      | 500C 7680h       |
| EPWM8_G0      | 5000 8680h       |
| EPWM8_G1      | 5004 8680h       |
| EPWM8_G2      | 5008 8680h       |
| EPWM8_G3      | 500C 8680h       |
| EPWM9_G0      | 5000 9680h       |
| EPWM9_G1      | 5004 9680h       |
| EPWM9_G2      | 5008 9680h       |

**Table 3-1165. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9680h       |
| EPWM10_G0     | 5000 A680h       |
| EPWM10_G1     | 5004 A680h       |
| EPWM10_G2     | 5008 A680h       |
| EPWM10_G3     | 500C A680h       |
| EPWM11_G0     | 5000 B680h       |
| EPWM11_G1     | 5004 B680h       |
| EPWM11_G2     | 5008 B680h       |
| EPWM11_G3     | 500C B680h       |
| EPWM12_G0     | 5000 C680h       |
| EPWM12_G1     | 5004 C680h       |
| EPWM12_G2     | 5008 C680h       |
| EPWM12_G3     | 500C C680h       |
| EPWM13_G0     | 5000 D680h       |
| EPWM13_G1     | 5004 D680h       |
| EPWM13_G2     | 5008 D680h       |
| EPWM13_G3     | 500C D680h       |
| EPWM14_G0     | 5000 E680h       |
| EPWM14_G1     | 5004 E680h       |
| EPWM14_G2     | 5008 E680h       |
| EPWM14_G3     | 500C E680h       |
| EPWM15_G0     | 5000 F680h       |
| EPWM15_G1     | 5004 F680h       |
| EPWM15_G2     | 5008 F680h       |
| EPWM15_G3     | 500C F680h       |
| EPWM16_G0     | 5001 0680h       |
| EPWM16_G1     | 5005 0680h       |
| EPWM16_G2     | 5009 0680h       |
| EPWM16_G3     | 500D 0680h       |
| EPWM17_G0     | 5001 1680h       |
| EPWM17_G1     | 5005 1680h       |
| EPWM17_G2     | 5009 1680h       |
| EPWM17_G3     | 500D 1680h       |
| EPWM18_G0     | 5001 2680h       |
| EPWM18_G1     | 5005 2680h       |
| EPWM18_G2     | 5009 2680h       |
| EPWM18_G3     | 500D 2680h       |
| EPWM19_G0     | 5001 3680h       |
| EPWM19_G1     | 5005 3680h       |
| EPWM19_G2     | 5009 3680h       |
| EPWM19_G3     | 500D 3680h       |
| EPWM20_G0     | 5001 4680h       |
| EPWM20_G1     | 5005 4680h       |
| EPWM20_G2     | 5009 4680h       |
| EPWM20_G3     | 500D 4680h       |

**Table 3-1165. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5680h       |
| EPWM21_G1     | 5005 5680h       |
| EPWM21_G2     | 5009 5680h       |
| EPWM21_G3     | 500D 5680h       |
| EPWM22_G0     | 5001 6680h       |
| EPWM22_G1     | 5005 6680h       |
| EPWM22_G2     | 5009 6680h       |
| EPWM22_G3     | 500D 6680h       |
| EPWM23_G0     | 5001 7680h       |
| EPWM23_G1     | 5005 7680h       |
| EPWM23_G2     | 5009 7680h       |
| EPWM23_G3     | 500D 7680h       |
| EPWM24_G0     | 5001 8680h       |
| EPWM24_G1     | 5005 8680h       |
| EPWM24_G2     | 5009 8680h       |
| EPWM24_G3     | 500D 8680h       |
| EPWM25_G0     | 5001 9680h       |
| EPWM25_G1     | 5005 9680h       |
| EPWM25_G2     | 5009 9680h       |
| EPWM25_G3     | 500D 9680h       |
| EPWM26_G0     | 5001 A680h       |
| EPWM26_G1     | 5005 A680h       |
| EPWM26_G2     | 5009 A680h       |
| EPWM26_G3     | 500D A680h       |
| EPWM27_G0     | 5001 B680h       |
| EPWM27_G1     | 5005 B680h       |
| EPWM27_G2     | 5009 B680h       |
| EPWM27_G3     | 500D B680h       |
| EPWM28_G0     | 5001 C680h       |
| EPWM28_G1     | 5005 C680h       |
| EPWM28_G2     | 5009 C680h       |
| EPWM28_G3     | 500D C680h       |
| EPWM29_G0     | 5001 D680h       |
| EPWM29_G1     | 5005 D680h       |
| EPWM29_G2     | 5009 D680h       |
| EPWM29_G3     | 500D D680h       |
| EPWM30_G0     | 5001 E680h       |
| EPWM30_G1     | 5005 E680h       |
| EPWM30_G2     | 5009 E680h       |
| EPWM30_G3     | 500D E680h       |
| EPWM31_G0     | 5001 F680h       |
| EPWM31_G1     | 5005 F680h       |
| EPWM31_G2     | 5009 F680h       |
| EPWM31_G3     | 500D F680h       |

**Figure 3-369. EPWM\_XCMP1\_SHDW1 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP1_SHDW1   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP1_SHDW1   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP1HR_SHDW1 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP1HR_SHDW1 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 3-1167. EPWM\_XCMP1\_SHDW1 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                 |
|-------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP1_SHDW1   | R/W  | 0h    | XCMP1_SHDW1 Register<br>The value in the XCMP1_SHDW1 register is loaded into XCMP1_ACTIVE register when shadow to active load occurs.       |
| 15:0  | XCMP1HR_SHDW1 | R/W  | 0h    | XCMP1HR_SHDW1 Register<br>The value in the XCMP1HR_SHDW1 register is loaded into XCMP1HR_ACTIVE register when shadow to active load occurs. |

### 3.7.2.119 EPWM\_XCMP2\_SHDW1 Register

#### 1 EPWM\_XCMP2\_SHDW1 Register (Offset = 684h) [reset = 0h]

Additional Compare 2 Shadow 1 Register.

Return to [Summary Table](#)

**Table 3-1168. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0684h       |
| EPWM0_G1      | 5004 0684h       |
| EPWM0_G2      | 5008 0684h       |
| EPWM0_G3      | 500C 0684h       |
| EPWM1_G0      | 5000 1684h       |
| EPWM1_G1      | 5004 1684h       |
| EPWM1_G2      | 5008 1684h       |
| EPWM1_G3      | 500C 1684h       |
| EPWM2_G0      | 5000 2684h       |
| EPWM2_G1      | 5004 2684h       |
| EPWM2_G2      | 5008 2684h       |
| EPWM2_G3      | 500C 2684h       |
| EPWM3_G0      | 5000 3684h       |
| EPWM3_G1      | 5004 3684h       |
| EPWM3_G2      | 5008 3684h       |
| EPWM3_G3      | 500C 3684h       |
| EPWM4_G0      | 5000 4684h       |
| EPWM4_G1      | 5004 4684h       |
| EPWM4_G2      | 5008 4684h       |
| EPWM4_G3      | 500C 4684h       |
| EPWM5_G0      | 5000 5684h       |
| EPWM5_G1      | 5004 5684h       |
| EPWM5_G2      | 5008 5684h       |
| EPWM5_G3      | 500C 5684h       |
| EPWM6_G0      | 5000 6684h       |
| EPWM6_G1      | 5004 6684h       |
| EPWM6_G2      | 5008 6684h       |
| EPWM6_G3      | 500C 6684h       |
| EPWM7_G0      | 5000 7684h       |
| EPWM7_G1      | 5004 7684h       |
| EPWM7_G2      | 5008 7684h       |
| EPWM7_G3      | 500C 7684h       |
| EPWM8_G0      | 5000 8684h       |
| EPWM8_G1      | 5004 8684h       |
| EPWM8_G2      | 5008 8684h       |
| EPWM8_G3      | 500C 8684h       |
| EPWM9_G0      | 5000 9684h       |
| EPWM9_G1      | 5004 9684h       |
| EPWM9_G2      | 5008 9684h       |

**Table 3-1168. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9684h       |
| EPWM10_G0     | 5000 A684h       |
| EPWM10_G1     | 5004 A684h       |
| EPWM10_G2     | 5008 A684h       |
| EPWM10_G3     | 500C A684h       |
| EPWM11_G0     | 5000 B684h       |
| EPWM11_G1     | 5004 B684h       |
| EPWM11_G2     | 5008 B684h       |
| EPWM11_G3     | 500C B684h       |
| EPWM12_G0     | 5000 C684h       |
| EPWM12_G1     | 5004 C684h       |
| EPWM12_G2     | 5008 C684h       |
| EPWM12_G3     | 500C C684h       |
| EPWM13_G0     | 5000 D684h       |
| EPWM13_G1     | 5004 D684h       |
| EPWM13_G2     | 5008 D684h       |
| EPWM13_G3     | 500C D684h       |
| EPWM14_G0     | 5000 E684h       |
| EPWM14_G1     | 5004 E684h       |
| EPWM14_G2     | 5008 E684h       |
| EPWM14_G3     | 500C E684h       |
| EPWM15_G0     | 5000 F684h       |
| EPWM15_G1     | 5004 F684h       |
| EPWM15_G2     | 5008 F684h       |
| EPWM15_G3     | 500C F684h       |
| EPWM16_G0     | 5001 0684h       |
| EPWM16_G1     | 5005 0684h       |
| EPWM16_G2     | 5009 0684h       |
| EPWM16_G3     | 500D 0684h       |
| EPWM17_G0     | 5001 1684h       |
| EPWM17_G1     | 5005 1684h       |
| EPWM17_G2     | 5009 1684h       |
| EPWM17_G3     | 500D 1684h       |
| EPWM18_G0     | 5001 2684h       |
| EPWM18_G1     | 5005 2684h       |
| EPWM18_G2     | 5009 2684h       |
| EPWM18_G3     | 500D 2684h       |
| EPWM19_G0     | 5001 3684h       |
| EPWM19_G1     | 5005 3684h       |
| EPWM19_G2     | 5009 3684h       |
| EPWM19_G3     | 500D 3684h       |
| EPWM20_G0     | 5001 4684h       |
| EPWM20_G1     | 5005 4684h       |
| EPWM20_G2     | 5009 4684h       |
| EPWM20_G3     | 500D 4684h       |



**Table 3-1168. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5684h       |
| EPWM21_G1     | 5005 5684h       |
| EPWM21_G2     | 5009 5684h       |
| EPWM21_G3     | 500D 5684h       |
| EPWM22_G0     | 5001 6684h       |
| EPWM22_G1     | 5005 6684h       |
| EPWM22_G2     | 5009 6684h       |
| EPWM22_G3     | 500D 6684h       |
| EPWM23_G0     | 5001 7684h       |
| EPWM23_G1     | 5005 7684h       |
| EPWM23_G2     | 5009 7684h       |
| EPWM23_G3     | 500D 7684h       |
| EPWM24_G0     | 5001 8684h       |
| EPWM24_G1     | 5005 8684h       |
| EPWM24_G2     | 5009 8684h       |
| EPWM24_G3     | 500D 8684h       |
| EPWM25_G0     | 5001 9684h       |
| EPWM25_G1     | 5005 9684h       |
| EPWM25_G2     | 5009 9684h       |
| EPWM25_G3     | 500D 9684h       |
| EPWM26_G0     | 5001 A684h       |
| EPWM26_G1     | 5005 A684h       |
| EPWM26_G2     | 5009 A684h       |
| EPWM26_G3     | 500D A684h       |
| EPWM27_G0     | 5001 B684h       |
| EPWM27_G1     | 5005 B684h       |
| EPWM27_G2     | 5009 B684h       |
| EPWM27_G3     | 500D B684h       |
| EPWM28_G0     | 5001 C684h       |
| EPWM28_G1     | 5005 C684h       |
| EPWM28_G2     | 5009 C684h       |
| EPWM28_G3     | 500D C684h       |
| EPWM29_G0     | 5001 D684h       |
| EPWM29_G1     | 5005 D684h       |
| EPWM29_G2     | 5009 D684h       |
| EPWM29_G3     | 500D D684h       |
| EPWM30_G0     | 5001 E684h       |
| EPWM30_G1     | 5005 E684h       |
| EPWM30_G2     | 5009 E684h       |
| EPWM30_G3     | 500D E684h       |
| EPWM31_G0     | 5001 F684h       |
| EPWM31_G1     | 5005 F684h       |
| EPWM31_G2     | 5009 F684h       |
| EPWM31_G3     | 500D F684h       |

**Figure 3-370. EPWM\_XCMP2\_SHDW1 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP2_SHDW1   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP2_SHDW1   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP2HR_SHDW1 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP2HR_SHDW1 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 3-1170. EPWM\_XCMP2\_SHDW1 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                 |
|-------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP2_SHDW1   | R/W  | 0h    | XCMP2_SHDW1 Register<br>The value in the XCMP2_SHDW1 register is loaded into XCMP2_ACTIVE register when shadow to active load occurs.       |
| 15:0  | XCMP2HR_SHDW1 | R/W  | 0h    | XCMP2HR_SHDW1 Register<br>The value in the XCMP2HR_SHDW1 register is loaded into XCMP2HR_ACTIVE register when shadow to active load occurs. |

### 3.7.2.120 EPWM\_XCMP3\_SHDW1 Register

#### 1 EPWM\_XCMP3\_SHDW1 Register (Offset = 688h) [reset = 0h]

Additional Compare 3 Shadow 1 Register.

Return to [Summary Table](#)

**Table 3-1171. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0688h       |
| EPWM0_G1      | 5004 0688h       |
| EPWM0_G2      | 5008 0688h       |
| EPWM0_G3      | 500C 0688h       |
| EPWM1_G0      | 5000 1688h       |
| EPWM1_G1      | 5004 1688h       |
| EPWM1_G2      | 5008 1688h       |
| EPWM1_G3      | 500C 1688h       |
| EPWM2_G0      | 5000 2688h       |
| EPWM2_G1      | 5004 2688h       |
| EPWM2_G2      | 5008 2688h       |
| EPWM2_G3      | 500C 2688h       |
| EPWM3_G0      | 5000 3688h       |
| EPWM3_G1      | 5004 3688h       |
| EPWM3_G2      | 5008 3688h       |
| EPWM3_G3      | 500C 3688h       |
| EPWM4_G0      | 5000 4688h       |
| EPWM4_G1      | 5004 4688h       |
| EPWM4_G2      | 5008 4688h       |
| EPWM4_G3      | 500C 4688h       |
| EPWM5_G0      | 5000 5688h       |
| EPWM5_G1      | 5004 5688h       |
| EPWM5_G2      | 5008 5688h       |
| EPWM5_G3      | 500C 5688h       |
| EPWM6_G0      | 5000 6688h       |
| EPWM6_G1      | 5004 6688h       |
| EPWM6_G2      | 5008 6688h       |
| EPWM6_G3      | 500C 6688h       |
| EPWM7_G0      | 5000 7688h       |
| EPWM7_G1      | 5004 7688h       |
| EPWM7_G2      | 5008 7688h       |
| EPWM7_G3      | 500C 7688h       |
| EPWM8_G0      | 5000 8688h       |
| EPWM8_G1      | 5004 8688h       |
| EPWM8_G2      | 5008 8688h       |
| EPWM8_G3      | 500C 8688h       |
| EPWM9_G0      | 5000 9688h       |
| EPWM9_G1      | 5004 9688h       |
| EPWM9_G2      | 5008 9688h       |

**Table 3-1171. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9688h       |
| EPWM10_G0     | 5000 A688h       |
| EPWM10_G1     | 5004 A688h       |
| EPWM10_G2     | 5008 A688h       |
| EPWM10_G3     | 500C A688h       |
| EPWM11_G0     | 5000 B688h       |
| EPWM11_G1     | 5004 B688h       |
| EPWM11_G2     | 5008 B688h       |
| EPWM11_G3     | 500C B688h       |
| EPWM12_G0     | 5000 C688h       |
| EPWM12_G1     | 5004 C688h       |
| EPWM12_G2     | 5008 C688h       |
| EPWM12_G3     | 500C C688h       |
| EPWM13_G0     | 5000 D688h       |
| EPWM13_G1     | 5004 D688h       |
| EPWM13_G2     | 5008 D688h       |
| EPWM13_G3     | 500C D688h       |
| EPWM14_G0     | 5000 E688h       |
| EPWM14_G1     | 5004 E688h       |
| EPWM14_G2     | 5008 E688h       |
| EPWM14_G3     | 500C E688h       |
| EPWM15_G0     | 5000 F688h       |
| EPWM15_G1     | 5004 F688h       |
| EPWM15_G2     | 5008 F688h       |
| EPWM15_G3     | 500C F688h       |
| EPWM16_G0     | 5001 0688h       |
| EPWM16_G1     | 5005 0688h       |
| EPWM16_G2     | 5009 0688h       |
| EPWM16_G3     | 500D 0688h       |
| EPWM17_G0     | 5001 1688h       |
| EPWM17_G1     | 5005 1688h       |
| EPWM17_G2     | 5009 1688h       |
| EPWM17_G3     | 500D 1688h       |
| EPWM18_G0     | 5001 2688h       |
| EPWM18_G1     | 5005 2688h       |
| EPWM18_G2     | 5009 2688h       |
| EPWM18_G3     | 500D 2688h       |
| EPWM19_G0     | 5001 3688h       |
| EPWM19_G1     | 5005 3688h       |
| EPWM19_G2     | 5009 3688h       |
| EPWM19_G3     | 500D 3688h       |
| EPWM20_G0     | 5001 4688h       |
| EPWM20_G1     | 5005 4688h       |
| EPWM20_G2     | 5009 4688h       |
| EPWM20_G3     | 500D 4688h       |

**Table 3-1171. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5688h       |
| EPWM21_G1     | 5005 5688h       |
| EPWM21_G2     | 5009 5688h       |
| EPWM21_G3     | 500D 5688h       |
| EPWM22_G0     | 5001 6688h       |
| EPWM22_G1     | 5005 6688h       |
| EPWM22_G2     | 5009 6688h       |
| EPWM22_G3     | 500D 6688h       |
| EPWM23_G0     | 5001 7688h       |
| EPWM23_G1     | 5005 7688h       |
| EPWM23_G2     | 5009 7688h       |
| EPWM23_G3     | 500D 7688h       |
| EPWM24_G0     | 5001 8688h       |
| EPWM24_G1     | 5005 8688h       |
| EPWM24_G2     | 5009 8688h       |
| EPWM24_G3     | 500D 8688h       |
| EPWM25_G0     | 5001 9688h       |
| EPWM25_G1     | 5005 9688h       |
| EPWM25_G2     | 5009 9688h       |
| EPWM25_G3     | 500D 9688h       |
| EPWM26_G0     | 5001 A688h       |
| EPWM26_G1     | 5005 A688h       |
| EPWM26_G2     | 5009 A688h       |
| EPWM26_G3     | 500D A688h       |
| EPWM27_G0     | 5001 B688h       |
| EPWM27_G1     | 5005 B688h       |
| EPWM27_G2     | 5009 B688h       |
| EPWM27_G3     | 500D B688h       |
| EPWM28_G0     | 5001 C688h       |
| EPWM28_G1     | 5005 C688h       |
| EPWM28_G2     | 5009 C688h       |
| EPWM28_G3     | 500D C688h       |
| EPWM29_G0     | 5001 D688h       |
| EPWM29_G1     | 5005 D688h       |
| EPWM29_G2     | 5009 D688h       |
| EPWM29_G3     | 500D D688h       |
| EPWM30_G0     | 5001 E688h       |
| EPWM30_G1     | 5005 E688h       |
| EPWM30_G2     | 5009 E688h       |
| EPWM30_G3     | 500D E688h       |
| EPWM31_G0     | 5001 F688h       |
| EPWM31_G1     | 5005 F688h       |
| EPWM31_G2     | 5009 F688h       |
| EPWM31_G3     | 500D F688h       |

**Figure 3-371. EPWM\_XCMP3\_SHDW1 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP3_SHDW1   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP3_SHDW1   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP3HR_SHDW1 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP3HR_SHDW1 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 3-1173. EPWM\_XCMP3\_SHDW1 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                 |
|-------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP3_SHDW1   | R/W  | 0h    | XCMP3_SHDW1 Register<br>The value in the XCMP3_SHDW1 register is loaded into XCMP3_ACTIVE register when shadow to active load occurs.       |
| 15:0  | XCMP3HR_SHDW1 | R/W  | 0h    | XCMP3HR_SHDW1 Register<br>The value in the XCMP3HR_SHDW1 register is loaded into XCMP3HR_ACTIVE register when shadow to active load occurs. |

### 3.7.2.121 EPWM\_XCMP4\_SHDW1 Register

#### 1 EPWM\_XCMP4\_SHDW1 Register (Offset = 68Ch) [reset = 0h]

Additional Compare 4 Shadow 1 Register.

Return to [Summary Table](#)

**Table 3-1174. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 068Ch       |
| EPWM0_G1      | 5004 068Ch       |
| EPWM0_G2      | 5008 068Ch       |
| EPWM0_G3      | 500C 068Ch       |
| EPWM1_G0      | 5000 168Ch       |
| EPWM1_G1      | 5004 168Ch       |
| EPWM1_G2      | 5008 168Ch       |
| EPWM1_G3      | 500C 168Ch       |
| EPWM2_G0      | 5000 268Ch       |
| EPWM2_G1      | 5004 268Ch       |
| EPWM2_G2      | 5008 268Ch       |
| EPWM2_G3      | 500C 268Ch       |
| EPWM3_G0      | 5000 368Ch       |
| EPWM3_G1      | 5004 368Ch       |
| EPWM3_G2      | 5008 368Ch       |
| EPWM3_G3      | 500C 368Ch       |
| EPWM4_G0      | 5000 468Ch       |
| EPWM4_G1      | 5004 468Ch       |
| EPWM4_G2      | 5008 468Ch       |
| EPWM4_G3      | 500C 468Ch       |
| EPWM5_G0      | 5000 568Ch       |
| EPWM5_G1      | 5004 568Ch       |
| EPWM5_G2      | 5008 568Ch       |
| EPWM5_G3      | 500C 568Ch       |
| EPWM6_G0      | 5000 668Ch       |
| EPWM6_G1      | 5004 668Ch       |
| EPWM6_G2      | 5008 668Ch       |
| EPWM6_G3      | 500C 668Ch       |
| EPWM7_G0      | 5000 768Ch       |
| EPWM7_G1      | 5004 768Ch       |
| EPWM7_G2      | 5008 768Ch       |
| EPWM7_G3      | 500C 768Ch       |
| EPWM8_G0      | 5000 868Ch       |
| EPWM8_G1      | 5004 868Ch       |
| EPWM8_G2      | 5008 868Ch       |
| EPWM8_G3      | 500C 868Ch       |
| EPWM9_G0      | 5000 968Ch       |
| EPWM9_G1      | 5004 968Ch       |
| EPWM9_G2      | 5008 968Ch       |

**Table 3-1174. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 968Ch       |
| EPWM10_G0     | 5000 A68Ch       |
| EPWM10_G1     | 5004 A68Ch       |
| EPWM10_G2     | 5008 A68Ch       |
| EPWM10_G3     | 500C A68Ch       |
| EPWM11_G0     | 5000 B68Ch       |
| EPWM11_G1     | 5004 B68Ch       |
| EPWM11_G2     | 5008 B68Ch       |
| EPWM11_G3     | 500C B68Ch       |
| EPWM12_G0     | 5000 C68Ch       |
| EPWM12_G1     | 5004 C68Ch       |
| EPWM12_G2     | 5008 C68Ch       |
| EPWM12_G3     | 500C C68Ch       |
| EPWM13_G0     | 5000 D68Ch       |
| EPWM13_G1     | 5004 D68Ch       |
| EPWM13_G2     | 5008 D68Ch       |
| EPWM13_G3     | 500C D68Ch       |
| EPWM14_G0     | 5000 E68Ch       |
| EPWM14_G1     | 5004 E68Ch       |
| EPWM14_G2     | 5008 E68Ch       |
| EPWM14_G3     | 500C E68Ch       |
| EPWM15_G0     | 5000 F68Ch       |
| EPWM15_G1     | 5004 F68Ch       |
| EPWM15_G2     | 5008 F68Ch       |
| EPWM15_G3     | 500C F68Ch       |
| EPWM16_G0     | 5001 068Ch       |
| EPWM16_G1     | 5005 068Ch       |
| EPWM16_G2     | 5009 068Ch       |
| EPWM16_G3     | 500D 068Ch       |
| EPWM17_G0     | 5001 168Ch       |
| EPWM17_G1     | 5005 168Ch       |
| EPWM17_G2     | 5009 168Ch       |
| EPWM17_G3     | 500D 168Ch       |
| EPWM18_G0     | 5001 268Ch       |
| EPWM18_G1     | 5005 268Ch       |
| EPWM18_G2     | 5009 268Ch       |
| EPWM18_G3     | 500D 268Ch       |
| EPWM19_G0     | 5001 368Ch       |
| EPWM19_G1     | 5005 368Ch       |
| EPWM19_G2     | 5009 368Ch       |
| EPWM19_G3     | 500D 368Ch       |
| EPWM20_G0     | 5001 468Ch       |
| EPWM20_G1     | 5005 468Ch       |
| EPWM20_G2     | 5009 468Ch       |
| EPWM20_G3     | 500D 468Ch       |



**Table 3-1174. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 568Ch       |
| EPWM21_G1     | 5005 568Ch       |
| EPWM21_G2     | 5009 568Ch       |
| EPWM21_G3     | 500D 568Ch       |
| EPWM22_G0     | 5001 668Ch       |
| EPWM22_G1     | 5005 668Ch       |
| EPWM22_G2     | 5009 668Ch       |
| EPWM22_G3     | 500D 668Ch       |
| EPWM23_G0     | 5001 768Ch       |
| EPWM23_G1     | 5005 768Ch       |
| EPWM23_G2     | 5009 768Ch       |
| EPWM23_G3     | 500D 768Ch       |
| EPWM24_G0     | 5001 868Ch       |
| EPWM24_G1     | 5005 868Ch       |
| EPWM24_G2     | 5009 868Ch       |
| EPWM24_G3     | 500D 868Ch       |
| EPWM25_G0     | 5001 968Ch       |
| EPWM25_G1     | 5005 968Ch       |
| EPWM25_G2     | 5009 968Ch       |
| EPWM25_G3     | 500D 968Ch       |
| EPWM26_G0     | 5001 A68Ch       |
| EPWM26_G1     | 5005 A68Ch       |
| EPWM26_G2     | 5009 A68Ch       |
| EPWM26_G3     | 500D A68Ch       |
| EPWM27_G0     | 5001 B68Ch       |
| EPWM27_G1     | 5005 B68Ch       |
| EPWM27_G2     | 5009 B68Ch       |
| EPWM27_G3     | 500D B68Ch       |
| EPWM28_G0     | 5001 C68Ch       |
| EPWM28_G1     | 5005 C68Ch       |
| EPWM28_G2     | 5009 C68Ch       |
| EPWM28_G3     | 500D C68Ch       |
| EPWM29_G0     | 5001 D68Ch       |
| EPWM29_G1     | 5005 D68Ch       |
| EPWM29_G2     | 5009 D68Ch       |
| EPWM29_G3     | 500D D68Ch       |
| EPWM30_G0     | 5001 E68Ch       |
| EPWM30_G1     | 5005 E68Ch       |
| EPWM30_G2     | 5009 E68Ch       |
| EPWM30_G3     | 500D E68Ch       |
| EPWM31_G0     | 5001 F68Ch       |
| EPWM31_G1     | 5005 F68Ch       |
| EPWM31_G2     | 5009 F68Ch       |
| EPWM31_G3     | 500D F68Ch       |

**Figure 3-372. EPWM\_XCMP4\_SHDW1 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP4_SHDW1   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP4_SHDW1   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP4HR_SHDW1 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP4HR_SHDW1 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 3-1176. EPWM\_XCMP4\_SHDW1 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                 |
|-------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP4_SHDW1   | R/W  | 0h    | XCMP4_SHDW1 Register<br>The value in the XCMP4_SHDW1 register is loaded into XCMP4_ACTIVE register when shadow to active load occurs.       |
| 15:0  | XCMP4HR_SHDW1 | R/W  | 0h    | XCMP4HR_SHDW1 Register<br>The value in the XCMP4HR_SHDW1 register is loaded into XCMP4HR_ACTIVE register when shadow to active load occurs. |

### 3.7.2.122 EPWM\_XCMP5\_SHDW1 Register

#### 1 EPWM\_XCMP5\_SHDW1 Register (Offset = 690h) [reset = 0h]

Additional Compare 5 Shadow 1 Register.

Return to [Summary Table](#)

**Table 3-1177. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0690h       |
| EPWM0_G1      | 5004 0690h       |
| EPWM0_G2      | 5008 0690h       |
| EPWM0_G3      | 500C 0690h       |
| EPWM1_G0      | 5000 1690h       |
| EPWM1_G1      | 5004 1690h       |
| EPWM1_G2      | 5008 1690h       |
| EPWM1_G3      | 500C 1690h       |
| EPWM2_G0      | 5000 2690h       |
| EPWM2_G1      | 5004 2690h       |
| EPWM2_G2      | 5008 2690h       |
| EPWM2_G3      | 500C 2690h       |
| EPWM3_G0      | 5000 3690h       |
| EPWM3_G1      | 5004 3690h       |
| EPWM3_G2      | 5008 3690h       |
| EPWM3_G3      | 500C 3690h       |
| EPWM4_G0      | 5000 4690h       |
| EPWM4_G1      | 5004 4690h       |
| EPWM4_G2      | 5008 4690h       |
| EPWM4_G3      | 500C 4690h       |
| EPWM5_G0      | 5000 5690h       |
| EPWM5_G1      | 5004 5690h       |
| EPWM5_G2      | 5008 5690h       |
| EPWM5_G3      | 500C 5690h       |
| EPWM6_G0      | 5000 6690h       |
| EPWM6_G1      | 5004 6690h       |
| EPWM6_G2      | 5008 6690h       |
| EPWM6_G3      | 500C 6690h       |
| EPWM7_G0      | 5000 7690h       |
| EPWM7_G1      | 5004 7690h       |
| EPWM7_G2      | 5008 7690h       |
| EPWM7_G3      | 500C 7690h       |
| EPWM8_G0      | 5000 8690h       |
| EPWM8_G1      | 5004 8690h       |
| EPWM8_G2      | 5008 8690h       |
| EPWM8_G3      | 500C 8690h       |
| EPWM9_G0      | 5000 9690h       |
| EPWM9_G1      | 5004 9690h       |
| EPWM9_G2      | 5008 9690h       |

**Table 3-1177. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9690h       |
| EPWM10_G0     | 5000 A690h       |
| EPWM10_G1     | 5004 A690h       |
| EPWM10_G2     | 5008 A690h       |
| EPWM10_G3     | 500C A690h       |
| EPWM11_G0     | 5000 B690h       |
| EPWM11_G1     | 5004 B690h       |
| EPWM11_G2     | 5008 B690h       |
| EPWM11_G3     | 500C B690h       |
| EPWM12_G0     | 5000 C690h       |
| EPWM12_G1     | 5004 C690h       |
| EPWM12_G2     | 5008 C690h       |
| EPWM12_G3     | 500C C690h       |
| EPWM13_G0     | 5000 D690h       |
| EPWM13_G1     | 5004 D690h       |
| EPWM13_G2     | 5008 D690h       |
| EPWM13_G3     | 500C D690h       |
| EPWM14_G0     | 5000 E690h       |
| EPWM14_G1     | 5004 E690h       |
| EPWM14_G2     | 5008 E690h       |
| EPWM14_G3     | 500C E690h       |
| EPWM15_G0     | 5000 F690h       |
| EPWM15_G1     | 5004 F690h       |
| EPWM15_G2     | 5008 F690h       |
| EPWM15_G3     | 500C F690h       |
| EPWM16_G0     | 5001 0690h       |
| EPWM16_G1     | 5005 0690h       |
| EPWM16_G2     | 5009 0690h       |
| EPWM16_G3     | 500D 0690h       |
| EPWM17_G0     | 5001 1690h       |
| EPWM17_G1     | 5005 1690h       |
| EPWM17_G2     | 5009 1690h       |
| EPWM17_G3     | 500D 1690h       |
| EPWM18_G0     | 5001 2690h       |
| EPWM18_G1     | 5005 2690h       |
| EPWM18_G2     | 5009 2690h       |
| EPWM18_G3     | 500D 2690h       |
| EPWM19_G0     | 5001 3690h       |
| EPWM19_G1     | 5005 3690h       |
| EPWM19_G2     | 5009 3690h       |
| EPWM19_G3     | 500D 3690h       |
| EPWM20_G0     | 5001 4690h       |
| EPWM20_G1     | 5005 4690h       |
| EPWM20_G2     | 5009 4690h       |
| EPWM20_G3     | 500D 4690h       |

**Table 3-1177. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5690h       |
| EPWM21_G1     | 5005 5690h       |
| EPWM21_G2     | 5009 5690h       |
| EPWM21_G3     | 500D 5690h       |
| EPWM22_G0     | 5001 6690h       |
| EPWM22_G1     | 5005 6690h       |
| EPWM22_G2     | 5009 6690h       |
| EPWM22_G3     | 500D 6690h       |
| EPWM23_G0     | 5001 7690h       |
| EPWM23_G1     | 5005 7690h       |
| EPWM23_G2     | 5009 7690h       |
| EPWM23_G3     | 500D 7690h       |
| EPWM24_G0     | 5001 8690h       |
| EPWM24_G1     | 5005 8690h       |
| EPWM24_G2     | 5009 8690h       |
| EPWM24_G3     | 500D 8690h       |
| EPWM25_G0     | 5001 9690h       |
| EPWM25_G1     | 5005 9690h       |
| EPWM25_G2     | 5009 9690h       |
| EPWM25_G3     | 500D 9690h       |
| EPWM26_G0     | 5001 A690h       |
| EPWM26_G1     | 5005 A690h       |
| EPWM26_G2     | 5009 A690h       |
| EPWM26_G3     | 500D A690h       |
| EPWM27_G0     | 5001 B690h       |
| EPWM27_G1     | 5005 B690h       |
| EPWM27_G2     | 5009 B690h       |
| EPWM27_G3     | 500D B690h       |
| EPWM28_G0     | 5001 C690h       |
| EPWM28_G1     | 5005 C690h       |
| EPWM28_G2     | 5009 C690h       |
| EPWM28_G3     | 500D C690h       |
| EPWM29_G0     | 5001 D690h       |
| EPWM29_G1     | 5005 D690h       |
| EPWM29_G2     | 5009 D690h       |
| EPWM29_G3     | 500D D690h       |
| EPWM30_G0     | 5001 E690h       |
| EPWM30_G1     | 5005 E690h       |
| EPWM30_G2     | 5009 E690h       |
| EPWM30_G3     | 500D E690h       |
| EPWM31_G0     | 5001 F690h       |
| EPWM31_G1     | 5005 F690h       |
| EPWM31_G2     | 5009 F690h       |
| EPWM31_G3     | 500D F690h       |

**Figure 3-373. EPWM\_XCMP5\_SHDW1 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP5_SHDW1   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP5_SHDW1   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP5HR_SHDW1 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP5HR_SHDW1 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 3-1179. EPWM\_XCMP5\_SHDW1 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                 |
|-------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP5_SHDW1   | R/W  | 0h    | XCMP5_SHDW1 Register<br>The value in the XCMP5_SHDW1 register is loaded into XCMP5_ACTIVE register when shadow to active load occurs.       |
| 15:0  | XCMP5HR_SHDW1 | R/W  | 0h    | XCMP5HR_SHDW1 Register<br>The value in the XCMP5HR_SHDW1 register is loaded into XCMP5HR_ACTIVE register when shadow to active load occurs. |

### 3.7.2.123 EPWM\_XCMP6\_SHDW1 Register

#### 1 EPWM\_XCMP6\_SHDW1 Register (Offset = 694h) [reset = 0h]

Additional Compare 6 Shadow 1 Register.

Return to [Summary Table](#)

**Table 3-1180. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0694h       |
| EPWM0_G1      | 5004 0694h       |
| EPWM0_G2      | 5008 0694h       |
| EPWM0_G3      | 500C 0694h       |
| EPWM1_G0      | 5000 1694h       |
| EPWM1_G1      | 5004 1694h       |
| EPWM1_G2      | 5008 1694h       |
| EPWM1_G3      | 500C 1694h       |
| EPWM2_G0      | 5000 2694h       |
| EPWM2_G1      | 5004 2694h       |
| EPWM2_G2      | 5008 2694h       |
| EPWM2_G3      | 500C 2694h       |
| EPWM3_G0      | 5000 3694h       |
| EPWM3_G1      | 5004 3694h       |
| EPWM3_G2      | 5008 3694h       |
| EPWM3_G3      | 500C 3694h       |
| EPWM4_G0      | 5000 4694h       |
| EPWM4_G1      | 5004 4694h       |
| EPWM4_G2      | 5008 4694h       |
| EPWM4_G3      | 500C 4694h       |
| EPWM5_G0      | 5000 5694h       |
| EPWM5_G1      | 5004 5694h       |
| EPWM5_G2      | 5008 5694h       |
| EPWM5_G3      | 500C 5694h       |
| EPWM6_G0      | 5000 6694h       |
| EPWM6_G1      | 5004 6694h       |
| EPWM6_G2      | 5008 6694h       |
| EPWM6_G3      | 500C 6694h       |
| EPWM7_G0      | 5000 7694h       |
| EPWM7_G1      | 5004 7694h       |
| EPWM7_G2      | 5008 7694h       |
| EPWM7_G3      | 500C 7694h       |
| EPWM8_G0      | 5000 8694h       |
| EPWM8_G1      | 5004 8694h       |
| EPWM8_G2      | 5008 8694h       |
| EPWM8_G3      | 500C 8694h       |
| EPWM9_G0      | 5000 9694h       |
| EPWM9_G1      | 5004 9694h       |
| EPWM9_G2      | 5008 9694h       |

**Table 3-1180. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9694h       |
| EPWM10_G0     | 5000 A694h       |
| EPWM10_G1     | 5004 A694h       |
| EPWM10_G2     | 5008 A694h       |
| EPWM10_G3     | 500C A694h       |
| EPWM11_G0     | 5000 B694h       |
| EPWM11_G1     | 5004 B694h       |
| EPWM11_G2     | 5008 B694h       |
| EPWM11_G3     | 500C B694h       |
| EPWM12_G0     | 5000 C694h       |
| EPWM12_G1     | 5004 C694h       |
| EPWM12_G2     | 5008 C694h       |
| EPWM12_G3     | 500C C694h       |
| EPWM13_G0     | 5000 D694h       |
| EPWM13_G1     | 5004 D694h       |
| EPWM13_G2     | 5008 D694h       |
| EPWM13_G3     | 500C D694h       |
| EPWM14_G0     | 5000 E694h       |
| EPWM14_G1     | 5004 E694h       |
| EPWM14_G2     | 5008 E694h       |
| EPWM14_G3     | 500C E694h       |
| EPWM15_G0     | 5000 F694h       |
| EPWM15_G1     | 5004 F694h       |
| EPWM15_G2     | 5008 F694h       |
| EPWM15_G3     | 500C F694h       |
| EPWM16_G0     | 5001 0694h       |
| EPWM16_G1     | 5005 0694h       |
| EPWM16_G2     | 5009 0694h       |
| EPWM16_G3     | 500D 0694h       |
| EPWM17_G0     | 5001 1694h       |
| EPWM17_G1     | 5005 1694h       |
| EPWM17_G2     | 5009 1694h       |
| EPWM17_G3     | 500D 1694h       |
| EPWM18_G0     | 5001 2694h       |
| EPWM18_G1     | 5005 2694h       |
| EPWM18_G2     | 5009 2694h       |
| EPWM18_G3     | 500D 2694h       |
| EPWM19_G0     | 5001 3694h       |
| EPWM19_G1     | 5005 3694h       |
| EPWM19_G2     | 5009 3694h       |
| EPWM19_G3     | 500D 3694h       |
| EPWM20_G0     | 5001 4694h       |
| EPWM20_G1     | 5005 4694h       |
| EPWM20_G2     | 5009 4694h       |
| EPWM20_G3     | 500D 4694h       |



**Table 3-1180. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5694h       |
| EPWM21_G1     | 5005 5694h       |
| EPWM21_G2     | 5009 5694h       |
| EPWM21_G3     | 500D 5694h       |
| EPWM22_G0     | 5001 6694h       |
| EPWM22_G1     | 5005 6694h       |
| EPWM22_G2     | 5009 6694h       |
| EPWM22_G3     | 500D 6694h       |
| EPWM23_G0     | 5001 7694h       |
| EPWM23_G1     | 5005 7694h       |
| EPWM23_G2     | 5009 7694h       |
| EPWM23_G3     | 500D 7694h       |
| EPWM24_G0     | 5001 8694h       |
| EPWM24_G1     | 5005 8694h       |
| EPWM24_G2     | 5009 8694h       |
| EPWM24_G3     | 500D 8694h       |
| EPWM25_G0     | 5001 9694h       |
| EPWM25_G1     | 5005 9694h       |
| EPWM25_G2     | 5009 9694h       |
| EPWM25_G3     | 500D 9694h       |
| EPWM26_G0     | 5001 A694h       |
| EPWM26_G1     | 5005 A694h       |
| EPWM26_G2     | 5009 A694h       |
| EPWM26_G3     | 500D A694h       |
| EPWM27_G0     | 5001 B694h       |
| EPWM27_G1     | 5005 B694h       |
| EPWM27_G2     | 5009 B694h       |
| EPWM27_G3     | 500D B694h       |
| EPWM28_G0     | 5001 C694h       |
| EPWM28_G1     | 5005 C694h       |
| EPWM28_G2     | 5009 C694h       |
| EPWM28_G3     | 500D C694h       |
| EPWM29_G0     | 5001 D694h       |
| EPWM29_G1     | 5005 D694h       |
| EPWM29_G2     | 5009 D694h       |
| EPWM29_G3     | 500D D694h       |
| EPWM30_G0     | 5001 E694h       |
| EPWM30_G1     | 5005 E694h       |
| EPWM30_G2     | 5009 E694h       |
| EPWM30_G3     | 500D E694h       |
| EPWM31_G0     | 5001 F694h       |
| EPWM31_G1     | 5005 F694h       |
| EPWM31_G2     | 5009 F694h       |
| EPWM31_G3     | 500D F694h       |

**Figure 3-374. EPWM\_XCMP6\_SHDW1 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP6_SHDW1   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP6_SHDW1   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP6HR_SHDW1 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP6HR_SHDW1 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 3-1182. EPWM\_XCMP6\_SHDW1 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                 |
|-------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP6_SHDW1   | R/W  | 0h    | XCMP6_SHDW1 Register<br>The value in the XCMP6_SHDW1 register is loaded into XCMP6_ACTIVE register when shadow to active load occurs.       |
| 15:0  | XCMP6HR_SHDW1 | R/W  | 0h    | XCMP6HR_SHDW1 Register<br>The value in the XCMP6HR_SHDW1 register is loaded into XCMP6HR_ACTIVE register when shadow to active load occurs. |

### 3.7.2.124 EPWM\_XCMP7\_SHDW1 Register

#### 1 EPWM\_XCMP7\_SHDW1 Register (Offset = 698h) [reset = 0h]

Additional Compare 7 Shadow 1 Register.

Return to [Summary Table](#)

**Table 3-1183. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0698h       |
| EPWM0_G1      | 5004 0698h       |
| EPWM0_G2      | 5008 0698h       |
| EPWM0_G3      | 500C 0698h       |
| EPWM1_G0      | 5000 1698h       |
| EPWM1_G1      | 5004 1698h       |
| EPWM1_G2      | 5008 1698h       |
| EPWM1_G3      | 500C 1698h       |
| EPWM2_G0      | 5000 2698h       |
| EPWM2_G1      | 5004 2698h       |
| EPWM2_G2      | 5008 2698h       |
| EPWM2_G3      | 500C 2698h       |
| EPWM3_G0      | 5000 3698h       |
| EPWM3_G1      | 5004 3698h       |
| EPWM3_G2      | 5008 3698h       |
| EPWM3_G3      | 500C 3698h       |
| EPWM4_G0      | 5000 4698h       |
| EPWM4_G1      | 5004 4698h       |
| EPWM4_G2      | 5008 4698h       |
| EPWM4_G3      | 500C 4698h       |
| EPWM5_G0      | 5000 5698h       |
| EPWM5_G1      | 5004 5698h       |
| EPWM5_G2      | 5008 5698h       |
| EPWM5_G3      | 500C 5698h       |
| EPWM6_G0      | 5000 6698h       |
| EPWM6_G1      | 5004 6698h       |
| EPWM6_G2      | 5008 6698h       |
| EPWM6_G3      | 500C 6698h       |
| EPWM7_G0      | 5000 7698h       |
| EPWM7_G1      | 5004 7698h       |
| EPWM7_G2      | 5008 7698h       |
| EPWM7_G3      | 500C 7698h       |
| EPWM8_G0      | 5000 8698h       |
| EPWM8_G1      | 5004 8698h       |
| EPWM8_G2      | 5008 8698h       |
| EPWM8_G3      | 500C 8698h       |
| EPWM9_G0      | 5000 9698h       |
| EPWM9_G1      | 5004 9698h       |
| EPWM9_G2      | 5008 9698h       |

**Table 3-1183. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9698h       |
| EPWM10_G0     | 5000 A698h       |
| EPWM10_G1     | 5004 A698h       |
| EPWM10_G2     | 5008 A698h       |
| EPWM10_G3     | 500C A698h       |
| EPWM11_G0     | 5000 B698h       |
| EPWM11_G1     | 5004 B698h       |
| EPWM11_G2     | 5008 B698h       |
| EPWM11_G3     | 500C B698h       |
| EPWM12_G0     | 5000 C698h       |
| EPWM12_G1     | 5004 C698h       |
| EPWM12_G2     | 5008 C698h       |
| EPWM12_G3     | 500C C698h       |
| EPWM13_G0     | 5000 D698h       |
| EPWM13_G1     | 5004 D698h       |
| EPWM13_G2     | 5008 D698h       |
| EPWM13_G3     | 500C D698h       |
| EPWM14_G0     | 5000 E698h       |
| EPWM14_G1     | 5004 E698h       |
| EPWM14_G2     | 5008 E698h       |
| EPWM14_G3     | 500C E698h       |
| EPWM15_G0     | 5000 F698h       |
| EPWM15_G1     | 5004 F698h       |
| EPWM15_G2     | 5008 F698h       |
| EPWM15_G3     | 500C F698h       |
| EPWM16_G0     | 5001 0698h       |
| EPWM16_G1     | 5005 0698h       |
| EPWM16_G2     | 5009 0698h       |
| EPWM16_G3     | 500D 0698h       |
| EPWM17_G0     | 5001 1698h       |
| EPWM17_G1     | 5005 1698h       |
| EPWM17_G2     | 5009 1698h       |
| EPWM17_G3     | 500D 1698h       |
| EPWM18_G0     | 5001 2698h       |
| EPWM18_G1     | 5005 2698h       |
| EPWM18_G2     | 5009 2698h       |
| EPWM18_G3     | 500D 2698h       |
| EPWM19_G0     | 5001 3698h       |
| EPWM19_G1     | 5005 3698h       |
| EPWM19_G2     | 5009 3698h       |
| EPWM19_G3     | 500D 3698h       |
| EPWM20_G0     | 5001 4698h       |
| EPWM20_G1     | 5005 4698h       |
| EPWM20_G2     | 5009 4698h       |
| EPWM20_G3     | 500D 4698h       |

**Table 3-1183. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5698h       |
| EPWM21_G1     | 5005 5698h       |
| EPWM21_G2     | 5009 5698h       |
| EPWM21_G3     | 500D 5698h       |
| EPWM22_G0     | 5001 6698h       |
| EPWM22_G1     | 5005 6698h       |
| EPWM22_G2     | 5009 6698h       |
| EPWM22_G3     | 500D 6698h       |
| EPWM23_G0     | 5001 7698h       |
| EPWM23_G1     | 5005 7698h       |
| EPWM23_G2     | 5009 7698h       |
| EPWM23_G3     | 500D 7698h       |
| EPWM24_G0     | 5001 8698h       |
| EPWM24_G1     | 5005 8698h       |
| EPWM24_G2     | 5009 8698h       |
| EPWM24_G3     | 500D 8698h       |
| EPWM25_G0     | 5001 9698h       |
| EPWM25_G1     | 5005 9698h       |
| EPWM25_G2     | 5009 9698h       |
| EPWM25_G3     | 500D 9698h       |
| EPWM26_G0     | 5001 A698h       |
| EPWM26_G1     | 5005 A698h       |
| EPWM26_G2     | 5009 A698h       |
| EPWM26_G3     | 500D A698h       |
| EPWM27_G0     | 5001 B698h       |
| EPWM27_G1     | 5005 B698h       |
| EPWM27_G2     | 5009 B698h       |
| EPWM27_G3     | 500D B698h       |
| EPWM28_G0     | 5001 C698h       |
| EPWM28_G1     | 5005 C698h       |
| EPWM28_G2     | 5009 C698h       |
| EPWM28_G3     | 500D C698h       |
| EPWM29_G0     | 5001 D698h       |
| EPWM29_G1     | 5005 D698h       |
| EPWM29_G2     | 5009 D698h       |
| EPWM29_G3     | 500D D698h       |
| EPWM30_G0     | 5001 E698h       |
| EPWM30_G1     | 5005 E698h       |
| EPWM30_G2     | 5009 E698h       |
| EPWM30_G3     | 500D E698h       |
| EPWM31_G0     | 5001 F698h       |
| EPWM31_G1     | 5005 F698h       |
| EPWM31_G2     | 5009 F698h       |
| EPWM31_G3     | 500D F698h       |

**Figure 3-375. EPWM\_XCMP7\_SHDW1 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP7_SHDW1   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP7_SHDW1   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP7HR_SHDW1 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP7HR_SHDW1 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 3-1185. EPWM\_XCMP7\_SHDW1 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                 |
|-------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP7_SHDW1   | R/W  | 0h    | XCMP7_SHDW1 Register<br>The value in the XCMP7_SHDW1 register is loaded into XCMP7_ACTIVE register when shadow to active load occurs.       |
| 15:0  | XCMP7HR_SHDW1 | R/W  | 0h    | XCMP7HR_SHDW1 Register<br>The value in the XCMP7HR_SHDW1 register is loaded into XCMP7HR_ACTIVE register when shadow to active load occurs. |

### 3.7.2.125 EPWM\_XCMP8\_SHDW1 Register

#### 1 EPWM\_XCMP8\_SHDW1 Register (Offset = 69Ch) [reset = 0h]

Additional Compare 8 Shadow 1 Register.

Return to [Summary Table](#)

**Table 3-1186. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 069Ch       |
| EPWM0_G1      | 5004 069Ch       |
| EPWM0_G2      | 5008 069Ch       |
| EPWM0_G3      | 500C 069Ch       |
| EPWM1_G0      | 5000 169Ch       |
| EPWM1_G1      | 5004 169Ch       |
| EPWM1_G2      | 5008 169Ch       |
| EPWM1_G3      | 500C 169Ch       |
| EPWM2_G0      | 5000 269Ch       |
| EPWM2_G1      | 5004 269Ch       |
| EPWM2_G2      | 5008 269Ch       |
| EPWM2_G3      | 500C 269Ch       |
| EPWM3_G0      | 5000 369Ch       |
| EPWM3_G1      | 5004 369Ch       |
| EPWM3_G2      | 5008 369Ch       |
| EPWM3_G3      | 500C 369Ch       |
| EPWM4_G0      | 5000 469Ch       |
| EPWM4_G1      | 5004 469Ch       |
| EPWM4_G2      | 5008 469Ch       |
| EPWM4_G3      | 500C 469Ch       |
| EPWM5_G0      | 5000 569Ch       |
| EPWM5_G1      | 5004 569Ch       |
| EPWM5_G2      | 5008 569Ch       |
| EPWM5_G3      | 500C 569Ch       |
| EPWM6_G0      | 5000 669Ch       |
| EPWM6_G1      | 5004 669Ch       |
| EPWM6_G2      | 5008 669Ch       |
| EPWM6_G3      | 500C 669Ch       |
| EPWM7_G0      | 5000 769Ch       |
| EPWM7_G1      | 5004 769Ch       |
| EPWM7_G2      | 5008 769Ch       |
| EPWM7_G3      | 500C 769Ch       |
| EPWM8_G0      | 5000 869Ch       |
| EPWM8_G1      | 5004 869Ch       |
| EPWM8_G2      | 5008 869Ch       |
| EPWM8_G3      | 500C 869Ch       |
| EPWM9_G0      | 5000 969Ch       |
| EPWM9_G1      | 5004 969Ch       |
| EPWM9_G2      | 5008 969Ch       |

**Table 3-1186. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 969Ch       |
| EPWM10_G0     | 5000 A69Ch       |
| EPWM10_G1     | 5004 A69Ch       |
| EPWM10_G2     | 5008 A69Ch       |
| EPWM10_G3     | 500C A69Ch       |
| EPWM11_G0     | 5000 B69Ch       |
| EPWM11_G1     | 5004 B69Ch       |
| EPWM11_G2     | 5008 B69Ch       |
| EPWM11_G3     | 500C B69Ch       |
| EPWM12_G0     | 5000 C69Ch       |
| EPWM12_G1     | 5004 C69Ch       |
| EPWM12_G2     | 5008 C69Ch       |
| EPWM12_G3     | 500C C69Ch       |
| EPWM13_G0     | 5000 D69Ch       |
| EPWM13_G1     | 5004 D69Ch       |
| EPWM13_G2     | 5008 D69Ch       |
| EPWM13_G3     | 500C D69Ch       |
| EPWM14_G0     | 5000 E69Ch       |
| EPWM14_G1     | 5004 E69Ch       |
| EPWM14_G2     | 5008 E69Ch       |
| EPWM14_G3     | 500C E69Ch       |
| EPWM15_G0     | 5000 F69Ch       |
| EPWM15_G1     | 5004 F69Ch       |
| EPWM15_G2     | 5008 F69Ch       |
| EPWM15_G3     | 500C F69Ch       |
| EPWM16_G0     | 5001 069Ch       |
| EPWM16_G1     | 5005 069Ch       |
| EPWM16_G2     | 5009 069Ch       |
| EPWM16_G3     | 500D 069Ch       |
| EPWM17_G0     | 5001 169Ch       |
| EPWM17_G1     | 5005 169Ch       |
| EPWM17_G2     | 5009 169Ch       |
| EPWM17_G3     | 500D 169Ch       |
| EPWM18_G0     | 5001 269Ch       |
| EPWM18_G1     | 5005 269Ch       |
| EPWM18_G2     | 5009 269Ch       |
| EPWM18_G3     | 500D 269Ch       |
| EPWM19_G0     | 5001 369Ch       |
| EPWM19_G1     | 5005 369Ch       |
| EPWM19_G2     | 5009 369Ch       |
| EPWM19_G3     | 500D 369Ch       |
| EPWM20_G0     | 5001 469Ch       |
| EPWM20_G1     | 5005 469Ch       |
| EPWM20_G2     | 5009 469Ch       |
| EPWM20_G3     | 500D 469Ch       |



**Table 3-1186. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 569Ch       |
| EPWM21_G1     | 5005 569Ch       |
| EPWM21_G2     | 5009 569Ch       |
| EPWM21_G3     | 500D 569Ch       |
| EPWM22_G0     | 5001 669Ch       |
| EPWM22_G1     | 5005 669Ch       |
| EPWM22_G2     | 5009 669Ch       |
| EPWM22_G3     | 500D 669Ch       |
| EPWM23_G0     | 5001 769Ch       |
| EPWM23_G1     | 5005 769Ch       |
| EPWM23_G2     | 5009 769Ch       |
| EPWM23_G3     | 500D 769Ch       |
| EPWM24_G0     | 5001 869Ch       |
| EPWM24_G1     | 5005 869Ch       |
| EPWM24_G2     | 5009 869Ch       |
| EPWM24_G3     | 500D 869Ch       |
| EPWM25_G0     | 5001 969Ch       |
| EPWM25_G1     | 5005 969Ch       |
| EPWM25_G2     | 5009 969Ch       |
| EPWM25_G3     | 500D 969Ch       |
| EPWM26_G0     | 5001 A69Ch       |
| EPWM26_G1     | 5005 A69Ch       |
| EPWM26_G2     | 5009 A69Ch       |
| EPWM26_G3     | 500D A69Ch       |
| EPWM27_G0     | 5001 B69Ch       |
| EPWM27_G1     | 5005 B69Ch       |
| EPWM27_G2     | 5009 B69Ch       |
| EPWM27_G3     | 500D B69Ch       |
| EPWM28_G0     | 5001 C69Ch       |
| EPWM28_G1     | 5005 C69Ch       |
| EPWM28_G2     | 5009 C69Ch       |
| EPWM28_G3     | 500D C69Ch       |
| EPWM29_G0     | 5001 D69Ch       |
| EPWM29_G1     | 5005 D69Ch       |
| EPWM29_G2     | 5009 D69Ch       |
| EPWM29_G3     | 500D D69Ch       |
| EPWM30_G0     | 5001 E69Ch       |
| EPWM30_G1     | 5005 E69Ch       |
| EPWM30_G2     | 5009 E69Ch       |
| EPWM30_G3     | 500D E69Ch       |
| EPWM31_G0     | 5001 F69Ch       |
| EPWM31_G1     | 5005 F69Ch       |
| EPWM31_G2     | 5009 F69Ch       |
| EPWM31_G3     | 500D F69Ch       |

**Figure 3-376. EPWM\_XCMP8\_SHDW1 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP8_SHDW1   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP8_SHDW1   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP8HR_SHDW1 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP8HR_SHDW1 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 3-1188. EPWM\_XCMP8\_SHDW1 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                 |
|-------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP8_SHDW1   | R/W  | 0h    | XCMP8_SHDW1 Register<br>The value in the XCMP8_SHDW1 register is loaded into XCMP8_ACTIVE register when shadow to active load occurs.       |
| 15:0  | XCMP8HR_SHDW1 | R/W  | 0h    | XCMP8HR_SHDW1 Register<br>The value in the XCMP8HR_SHDW1 register is loaded into XCMP8HR_ACTIVE register when shadow to active load occurs. |

### 3.7.2.126 EPWM\_XTBPRD\_SHDW1 Register

#### 1 EPWM\_XTBPRD\_SHDW1 Register (Offset = 6A0h) [reset = 0h]

Additional Time Base Period Shadow 1 Register.

Return to [Summary Table](#)

**Table 3-1189. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 06A0h       |
| EPWM0_G1      | 5004 06A0h       |
| EPWM0_G2      | 5008 06A0h       |
| EPWM0_G3      | 500C 06A0h       |
| EPWM1_G0      | 5000 16A0h       |
| EPWM1_G1      | 5004 16A0h       |
| EPWM1_G2      | 5008 16A0h       |
| EPWM1_G3      | 500C 16A0h       |
| EPWM2_G0      | 5000 26A0h       |
| EPWM2_G1      | 5004 26A0h       |
| EPWM2_G2      | 5008 26A0h       |
| EPWM2_G3      | 500C 26A0h       |
| EPWM3_G0      | 5000 36A0h       |
| EPWM3_G1      | 5004 36A0h       |
| EPWM3_G2      | 5008 36A0h       |
| EPWM3_G3      | 500C 36A0h       |
| EPWM4_G0      | 5000 46A0h       |
| EPWM4_G1      | 5004 46A0h       |
| EPWM4_G2      | 5008 46A0h       |
| EPWM4_G3      | 500C 46A0h       |
| EPWM5_G0      | 5000 56A0h       |
| EPWM5_G1      | 5004 56A0h       |
| EPWM5_G2      | 5008 56A0h       |
| EPWM5_G3      | 500C 56A0h       |
| EPWM6_G0      | 5000 66A0h       |
| EPWM6_G1      | 5004 66A0h       |
| EPWM6_G2      | 5008 66A0h       |
| EPWM6_G3      | 500C 66A0h       |
| EPWM7_G0      | 5000 76A0h       |
| EPWM7_G1      | 5004 76A0h       |
| EPWM7_G2      | 5008 76A0h       |
| EPWM7_G3      | 500C 76A0h       |
| EPWM8_G0      | 5000 86A0h       |
| EPWM8_G1      | 5004 86A0h       |
| EPWM8_G2      | 5008 86A0h       |
| EPWM8_G3      | 500C 86A0h       |
| EPWM9_G0      | 5000 96A0h       |
| EPWM9_G1      | 5004 96A0h       |
| EPWM9_G2      | 5008 96A0h       |

**Table 3-1189. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 96A0h       |
| EPWM10_G0     | 5000 A6A0h       |
| EPWM10_G1     | 5004 A6A0h       |
| EPWM10_G2     | 5008 A6A0h       |
| EPWM10_G3     | 500C A6A0h       |
| EPWM11_G0     | 5000 B6A0h       |
| EPWM11_G1     | 5004 B6A0h       |
| EPWM11_G2     | 5008 B6A0h       |
| EPWM11_G3     | 500C B6A0h       |
| EPWM12_G0     | 5000 C6A0h       |
| EPWM12_G1     | 5004 C6A0h       |
| EPWM12_G2     | 5008 C6A0h       |
| EPWM12_G3     | 500C C6A0h       |
| EPWM13_G0     | 5000 D6A0h       |
| EPWM13_G1     | 5004 D6A0h       |
| EPWM13_G2     | 5008 D6A0h       |
| EPWM13_G3     | 500C D6A0h       |
| EPWM14_G0     | 5000 E6A0h       |
| EPWM14_G1     | 5004 E6A0h       |
| EPWM14_G2     | 5008 E6A0h       |
| EPWM14_G3     | 500C E6A0h       |
| EPWM15_G0     | 5000 F6A0h       |
| EPWM15_G1     | 5004 F6A0h       |
| EPWM15_G2     | 5008 F6A0h       |
| EPWM15_G3     | 500C F6A0h       |
| EPWM16_G0     | 5001 06A0h       |
| EPWM16_G1     | 5005 06A0h       |
| EPWM16_G2     | 5009 06A0h       |
| EPWM16_G3     | 500D 06A0h       |
| EPWM17_G0     | 5001 16A0h       |
| EPWM17_G1     | 5005 16A0h       |
| EPWM17_G2     | 5009 16A0h       |
| EPWM17_G3     | 500D 16A0h       |
| EPWM18_G0     | 5001 26A0h       |
| EPWM18_G1     | 5005 26A0h       |
| EPWM18_G2     | 5009 26A0h       |
| EPWM18_G3     | 500D 26A0h       |
| EPWM19_G0     | 5001 36A0h       |
| EPWM19_G1     | 5005 36A0h       |
| EPWM19_G2     | 5009 36A0h       |
| EPWM19_G3     | 500D 36A0h       |
| EPWM20_G0     | 5001 46A0h       |
| EPWM20_G1     | 5005 46A0h       |
| EPWM20_G2     | 5009 46A0h       |
| EPWM20_G3     | 500D 46A0h       |

**Table 3-1189. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 56A0h       |
| EPWM21_G1     | 5005 56A0h       |
| EPWM21_G2     | 5009 56A0h       |
| EPWM21_G3     | 500D 56A0h       |
| EPWM22_G0     | 5001 66A0h       |
| EPWM22_G1     | 5005 66A0h       |
| EPWM22_G2     | 5009 66A0h       |
| EPWM22_G3     | 500D 66A0h       |
| EPWM23_G0     | 5001 76A0h       |
| EPWM23_G1     | 5005 76A0h       |
| EPWM23_G2     | 5009 76A0h       |
| EPWM23_G3     | 500D 76A0h       |
| EPWM24_G0     | 5001 86A0h       |
| EPWM24_G1     | 5005 86A0h       |
| EPWM24_G2     | 5009 86A0h       |
| EPWM24_G3     | 500D 86A0h       |
| EPWM25_G0     | 5001 96A0h       |
| EPWM25_G1     | 5005 96A0h       |
| EPWM25_G2     | 5009 96A0h       |
| EPWM25_G3     | 500D 96A0h       |
| EPWM26_G0     | 5001 A6A0h       |
| EPWM26_G1     | 5005 A6A0h       |
| EPWM26_G2     | 5009 A6A0h       |
| EPWM26_G3     | 500D A6A0h       |
| EPWM27_G0     | 5001 B6A0h       |
| EPWM27_G1     | 5005 B6A0h       |
| EPWM27_G2     | 5009 B6A0h       |
| EPWM27_G3     | 500D B6A0h       |
| EPWM28_G0     | 5001 C6A0h       |
| EPWM28_G1     | 5005 C6A0h       |
| EPWM28_G2     | 5009 C6A0h       |
| EPWM28_G3     | 500D C6A0h       |
| EPWM29_G0     | 5001 D6A0h       |
| EPWM29_G1     | 5005 D6A0h       |
| EPWM29_G2     | 5009 D6A0h       |
| EPWM29_G3     | 500D D6A0h       |
| EPWM30_G0     | 5001 E6A0h       |
| EPWM30_G1     | 5005 E6A0h       |
| EPWM30_G2     | 5009 E6A0h       |
| EPWM30_G3     | 500D E6A0h       |
| EPWM31_G0     | 5001 F6A0h       |
| EPWM31_G1     | 5005 F6A0h       |
| EPWM31_G2     | 5009 F6A0h       |
| EPWM31_G3     | 500D F6A0h       |

**Figure 3-377. EPWM\_XTBPRD\_SHDW1 Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XTBPRD_SHDW1   |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XTBPRD_SHDW1   |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XTBPRDHR_SHDW1 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XTBPRDHR_SHDW1 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 3-1191. EPWM\_XTBPRD\_SHDW1 Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                         |
|-------|----------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:16 | XTBPRD_SHDW1   | R/W  | 0h    | The value in the XTBPRD_SHDW1 register is loaded into XTBPRD_ACTIVE register when shadow to active load occurs.     |
| 15:0  | XTBPRDHR_SHDW1 | R/W  | 0h    | The value in the XTBPRDHR_SHDW1 register is loaded into XTBPRDHR_ACTIVE register when shadow to active load occurs. |

### 3.7.2.127 EPWM\_XAQCTLA\_SHDW1 Register

#### 1 EPWM\_XAQCTLA\_SHDW1 Register (Offset = 6B0h) [reset = 0h]

XAQCTLA Shadow 1 Register.

Return to [Summary Table](#)

**Table 3-1192. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 06B0h       |
| EPWM0_G1      | 5004 06B0h       |
| EPWM0_G2      | 5008 06B0h       |
| EPWM0_G3      | 500C 06B0h       |
| EPWM1_G0      | 5000 16B0h       |
| EPWM1_G1      | 5004 16B0h       |
| EPWM1_G2      | 5008 16B0h       |
| EPWM1_G3      | 500C 16B0h       |
| EPWM2_G0      | 5000 26B0h       |
| EPWM2_G1      | 5004 26B0h       |
| EPWM2_G2      | 5008 26B0h       |
| EPWM2_G3      | 500C 26B0h       |
| EPWM3_G0      | 5000 36B0h       |
| EPWM3_G1      | 5004 36B0h       |
| EPWM3_G2      | 5008 36B0h       |
| EPWM3_G3      | 500C 36B0h       |
| EPWM4_G0      | 5000 46B0h       |
| EPWM4_G1      | 5004 46B0h       |
| EPWM4_G2      | 5008 46B0h       |
| EPWM4_G3      | 500C 46B0h       |
| EPWM5_G0      | 5000 56B0h       |
| EPWM5_G1      | 5004 56B0h       |
| EPWM5_G2      | 5008 56B0h       |
| EPWM5_G3      | 500C 56B0h       |
| EPWM6_G0      | 5000 66B0h       |
| EPWM6_G1      | 5004 66B0h       |
| EPWM6_G2      | 5008 66B0h       |
| EPWM6_G3      | 500C 66B0h       |
| EPWM7_G0      | 5000 76B0h       |
| EPWM7_G1      | 5004 76B0h       |
| EPWM7_G2      | 5008 76B0h       |
| EPWM7_G3      | 500C 76B0h       |
| EPWM8_G0      | 5000 86B0h       |
| EPWM8_G1      | 5004 86B0h       |
| EPWM8_G2      | 5008 86B0h       |
| EPWM8_G3      | 500C 86B0h       |
| EPWM9_G0      | 5000 96B0h       |
| EPWM9_G1      | 5004 96B0h       |
| EPWM9_G2      | 5008 96B0h       |

**Table 3-1192. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 96B0h       |
| EPWM10_G0     | 5000 A6B0h       |
| EPWM10_G1     | 5004 A6B0h       |
| EPWM10_G2     | 5008 A6B0h       |
| EPWM10_G3     | 500C A6B0h       |
| EPWM11_G0     | 5000 B6B0h       |
| EPWM11_G1     | 5004 B6B0h       |
| EPWM11_G2     | 5008 B6B0h       |
| EPWM11_G3     | 500C B6B0h       |
| EPWM12_G0     | 5000 C6B0h       |
| EPWM12_G1     | 5004 C6B0h       |
| EPWM12_G2     | 5008 C6B0h       |
| EPWM12_G3     | 500C C6B0h       |
| EPWM13_G0     | 5000 D6B0h       |
| EPWM13_G1     | 5004 D6B0h       |
| EPWM13_G2     | 5008 D6B0h       |
| EPWM13_G3     | 500C D6B0h       |
| EPWM14_G0     | 5000 E6B0h       |
| EPWM14_G1     | 5004 E6B0h       |
| EPWM14_G2     | 5008 E6B0h       |
| EPWM14_G3     | 500C E6B0h       |
| EPWM15_G0     | 5000 F6B0h       |
| EPWM15_G1     | 5004 F6B0h       |
| EPWM15_G2     | 5008 F6B0h       |
| EPWM15_G3     | 500C F6B0h       |
| EPWM16_G0     | 5001 06B0h       |
| EPWM16_G1     | 5005 06B0h       |
| EPWM16_G2     | 5009 06B0h       |
| EPWM16_G3     | 500D 06B0h       |
| EPWM17_G0     | 5001 16B0h       |
| EPWM17_G1     | 5005 16B0h       |
| EPWM17_G2     | 5009 16B0h       |
| EPWM17_G3     | 500D 16B0h       |
| EPWM18_G0     | 5001 26B0h       |
| EPWM18_G1     | 5005 26B0h       |
| EPWM18_G2     | 5009 26B0h       |
| EPWM18_G3     | 500D 26B0h       |
| EPWM19_G0     | 5001 36B0h       |
| EPWM19_G1     | 5005 36B0h       |
| EPWM19_G2     | 5009 36B0h       |
| EPWM19_G3     | 500D 36B0h       |
| EPWM20_G0     | 5001 46B0h       |
| EPWM20_G1     | 5005 46B0h       |
| EPWM20_G2     | 5009 46B0h       |
| EPWM20_G3     | 500D 46B0h       |



**Table 3-1192. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 56B0h       |
| EPWM21_G1     | 5005 56B0h       |
| EPWM21_G2     | 5009 56B0h       |
| EPWM21_G3     | 500D 56B0h       |
| EPWM22_G0     | 5001 66B0h       |
| EPWM22_G1     | 5005 66B0h       |
| EPWM22_G2     | 5009 66B0h       |
| EPWM22_G3     | 500D 66B0h       |
| EPWM23_G0     | 5001 76B0h       |
| EPWM23_G1     | 5005 76B0h       |
| EPWM23_G2     | 5009 76B0h       |
| EPWM23_G3     | 500D 76B0h       |
| EPWM24_G0     | 5001 86B0h       |
| EPWM24_G1     | 5005 86B0h       |
| EPWM24_G2     | 5009 86B0h       |
| EPWM24_G3     | 500D 86B0h       |
| EPWM25_G0     | 5001 96B0h       |
| EPWM25_G1     | 5005 96B0h       |
| EPWM25_G2     | 5009 96B0h       |
| EPWM25_G3     | 500D 96B0h       |
| EPWM26_G0     | 5001 A6B0h       |
| EPWM26_G1     | 5005 A6B0h       |
| EPWM26_G2     | 5009 A6B0h       |
| EPWM26_G3     | 500D A6B0h       |
| EPWM27_G0     | 5001 B6B0h       |
| EPWM27_G1     | 5005 B6B0h       |
| EPWM27_G2     | 5009 B6B0h       |
| EPWM27_G3     | 500D B6B0h       |
| EPWM28_G0     | 5001 C6B0h       |
| EPWM28_G1     | 5005 C6B0h       |
| EPWM28_G2     | 5009 C6B0h       |
| EPWM28_G3     | 500D C6B0h       |
| EPWM29_G0     | 5001 D6B0h       |
| EPWM29_G1     | 5005 D6B0h       |
| EPWM29_G2     | 5009 D6B0h       |
| EPWM29_G3     | 500D D6B0h       |
| EPWM30_G0     | 5001 E6B0h       |
| EPWM30_G1     | 5005 E6B0h       |
| EPWM30_G2     | 5009 E6B0h       |
| EPWM30_G3     | 500D E6B0h       |
| EPWM31_G0     | 5001 F6B0h       |
| EPWM31_G1     | 5005 F6B0h       |
| EPWM31_G2     | 5009 F6B0h       |
| EPWM31_G3     | 500D F6B0h       |

**Figure 3-378. EPWM\_XAQCTLA\_SHDW1 Name Register**

| 15    | 14 | 13    | 12 | 11    | 10 | 9     | 8 |
|-------|----|-------|----|-------|----|-------|---|
| XCMP8 |    | XCMP7 |    | XCMP6 |    | XCMP5 |   |
| R/W   |    | R/W   |    | R/W   |    | R/W   |   |
| 0h    |    | 0h    |    | 0h    |    | 0h    |   |
| 7     | 6  | 5     | 4  | 3     | 2  | 1     | 0 |
| XCMP4 |    | XCMP3 |    | XCMP2 |    | XCMP1 |   |
| R/W   |    | R/W   |    | R/W   |    | R/W   |   |
| 0h    |    | 0h    |    | 0h    |    | 0h    |   |

**Table 3-1194. EPWM\_XAQCTLA\_SHDW1 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                          |
|-------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | XCMP8 | R/W  | 0h    | Action when Counter = CMP8<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 13:12 | XCMP7 | R/W  | 0h    | Action when Counter = CMP7<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 11:10 | XCMP6 | R/W  | 0h    | Action when Counter = CMP6<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 9:8   | XCMP5 | R/W  | 0h    | Action when Counter = CMP5<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 7:6   | XCMP4 | R/W  | 0h    | Action when Counter = CMP4<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 5:4   | XCMP3 | R/W  | 0h    | Action when Counter = CMP3<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 3:2   | XCMP2 | R/W  | 0h    | Action when Counter = CMP2<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 1:0   | XCMP1 | R/W  | 0h    | Action when Counter = CMP1<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |

### 3.7.2.128 EPWM\_XAQCTLB\_SHDW1 Register

#### 1 EPWM\_XAQCTLB\_SHDW1 Register (Offset = 6B2h) [reset = 0h]

XAQCTLB Shadow 1 Register.

Return to [Summary Table](#)

**Table 3-1195. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 06B2h       |
| EPWM0_G1      | 5004 06B2h       |
| EPWM0_G2      | 5008 06B2h       |
| EPWM0_G3      | 500C 06B2h       |
| EPWM1_G0      | 5000 16B2h       |
| EPWM1_G1      | 5004 16B2h       |
| EPWM1_G2      | 5008 16B2h       |
| EPWM1_G3      | 500C 16B2h       |
| EPWM2_G0      | 5000 26B2h       |
| EPWM2_G1      | 5004 26B2h       |
| EPWM2_G2      | 5008 26B2h       |
| EPWM2_G3      | 500C 26B2h       |
| EPWM3_G0      | 5000 36B2h       |
| EPWM3_G1      | 5004 36B2h       |
| EPWM3_G2      | 5008 36B2h       |
| EPWM3_G3      | 500C 36B2h       |
| EPWM4_G0      | 5000 46B2h       |
| EPWM4_G1      | 5004 46B2h       |
| EPWM4_G2      | 5008 46B2h       |
| EPWM4_G3      | 500C 46B2h       |
| EPWM5_G0      | 5000 56B2h       |
| EPWM5_G1      | 5004 56B2h       |
| EPWM5_G2      | 5008 56B2h       |
| EPWM5_G3      | 500C 56B2h       |
| EPWM6_G0      | 5000 66B2h       |
| EPWM6_G1      | 5004 66B2h       |
| EPWM6_G2      | 5008 66B2h       |
| EPWM6_G3      | 500C 66B2h       |
| EPWM7_G0      | 5000 76B2h       |
| EPWM7_G1      | 5004 76B2h       |
| EPWM7_G2      | 5008 76B2h       |
| EPWM7_G3      | 500C 76B2h       |
| EPWM8_G0      | 5000 86B2h       |
| EPWM8_G1      | 5004 86B2h       |
| EPWM8_G2      | 5008 86B2h       |
| EPWM8_G3      | 500C 86B2h       |
| EPWM9_G0      | 5000 96B2h       |
| EPWM9_G1      | 5004 96B2h       |
| EPWM9_G2      | 5008 96B2h       |

**Table 3-1195. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 96B2h       |
| EPWM10_G0     | 5000 A6B2h       |
| EPWM10_G1     | 5004 A6B2h       |
| EPWM10_G2     | 5008 A6B2h       |
| EPWM10_G3     | 500C A6B2h       |
| EPWM11_G0     | 5000 B6B2h       |
| EPWM11_G1     | 5004 B6B2h       |
| EPWM11_G2     | 5008 B6B2h       |
| EPWM11_G3     | 500C B6B2h       |
| EPWM12_G0     | 5000 C6B2h       |
| EPWM12_G1     | 5004 C6B2h       |
| EPWM12_G2     | 5008 C6B2h       |
| EPWM12_G3     | 500C C6B2h       |
| EPWM13_G0     | 5000 D6B2h       |
| EPWM13_G1     | 5004 D6B2h       |
| EPWM13_G2     | 5008 D6B2h       |
| EPWM13_G3     | 500C D6B2h       |
| EPWM14_G0     | 5000 E6B2h       |
| EPWM14_G1     | 5004 E6B2h       |
| EPWM14_G2     | 5008 E6B2h       |
| EPWM14_G3     | 500C E6B2h       |
| EPWM15_G0     | 5000 F6B2h       |
| EPWM15_G1     | 5004 F6B2h       |
| EPWM15_G2     | 5008 F6B2h       |
| EPWM15_G3     | 500C F6B2h       |
| EPWM16_G0     | 5001 06B2h       |
| EPWM16_G1     | 5005 06B2h       |
| EPWM16_G2     | 5009 06B2h       |
| EPWM16_G3     | 500D 06B2h       |
| EPWM17_G0     | 5001 16B2h       |
| EPWM17_G1     | 5005 16B2h       |
| EPWM17_G2     | 5009 16B2h       |
| EPWM17_G3     | 500D 16B2h       |
| EPWM18_G0     | 5001 26B2h       |
| EPWM18_G1     | 5005 26B2h       |
| EPWM18_G2     | 5009 26B2h       |
| EPWM18_G3     | 500D 26B2h       |
| EPWM19_G0     | 5001 36B2h       |
| EPWM19_G1     | 5005 36B2h       |
| EPWM19_G2     | 5009 36B2h       |
| EPWM19_G3     | 500D 36B2h       |
| EPWM20_G0     | 5001 46B2h       |
| EPWM20_G1     | 5005 46B2h       |
| EPWM20_G2     | 5009 46B2h       |
| EPWM20_G3     | 500D 46B2h       |

**Table 3-1195. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 56B2h       |
| EPWM21_G1     | 5005 56B2h       |
| EPWM21_G2     | 5009 56B2h       |
| EPWM21_G3     | 500D 56B2h       |
| EPWM22_G0     | 5001 66B2h       |
| EPWM22_G1     | 5005 66B2h       |
| EPWM22_G2     | 5009 66B2h       |
| EPWM22_G3     | 500D 66B2h       |
| EPWM23_G0     | 5001 76B2h       |
| EPWM23_G1     | 5005 76B2h       |
| EPWM23_G2     | 5009 76B2h       |
| EPWM23_G3     | 500D 76B2h       |
| EPWM24_G0     | 5001 86B2h       |
| EPWM24_G1     | 5005 86B2h       |
| EPWM24_G2     | 5009 86B2h       |
| EPWM24_G3     | 500D 86B2h       |
| EPWM25_G0     | 5001 96B2h       |
| EPWM25_G1     | 5005 96B2h       |
| EPWM25_G2     | 5009 96B2h       |
| EPWM25_G3     | 500D 96B2h       |
| EPWM26_G0     | 5001 A6B2h       |
| EPWM26_G1     | 5005 A6B2h       |
| EPWM26_G2     | 5009 A6B2h       |
| EPWM26_G3     | 500D A6B2h       |
| EPWM27_G0     | 5001 B6B2h       |
| EPWM27_G1     | 5005 B6B2h       |
| EPWM27_G2     | 5009 B6B2h       |
| EPWM27_G3     | 500D B6B2h       |
| EPWM28_G0     | 5001 C6B2h       |
| EPWM28_G1     | 5005 C6B2h       |
| EPWM28_G2     | 5009 C6B2h       |
| EPWM28_G3     | 500D C6B2h       |
| EPWM29_G0     | 5001 D6B2h       |
| EPWM29_G1     | 5005 D6B2h       |
| EPWM29_G2     | 5009 D6B2h       |
| EPWM29_G3     | 500D D6B2h       |
| EPWM30_G0     | 5001 E6B2h       |
| EPWM30_G1     | 5005 E6B2h       |
| EPWM30_G2     | 5009 E6B2h       |
| EPWM30_G3     | 500D E6B2h       |
| EPWM31_G0     | 5001 F6B2h       |
| EPWM31_G1     | 5005 F6B2h       |
| EPWM31_G2     | 5009 F6B2h       |
| EPWM31_G3     | 500D F6B2h       |

**Figure 3-379. EPWM\_XAQCTLB\_SHDW1 Name Register**

|            |    |       |    |       |    |       |   |
|------------|----|-------|----|-------|----|-------|---|
| 15         | 14 | 13    | 12 | 11    | 10 | 9     | 8 |
| XCMP8      |    | XCMP7 |    | XCMP6 |    | XCMP5 |   |
| R/W        |    | R/W   |    | R/W   |    | R/W   |   |
| 0h         |    | 0h    |    | 0h    |    | 0h    |   |
| 7          | 6  | 5     | 4  | 3     | 2  | 1     | 0 |
| RESERVED_1 |    |       |    |       |    |       |   |
| R          |    |       |    |       |    |       |   |
| 0h         |    |       |    |       |    |       |   |

**Table 3-1197. EPWM\_XAQCTLB\_SHDW1 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                          |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | XCMP8      | R/W  | 0h    | Action when Counter = CMP8<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 13:12 | XCMP7      | R/W  | 0h    | Action when Counter = CMP7<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 11:10 | XCMP6      | R/W  | 0h    | Action when Counter = CMP6<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 9:8   | XCMP5      | R/W  | 0h    | Action when Counter = CMP5<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 7:0   | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                             |

### 3.7.2.129 EPWM\_CMPC\_SHDW1 Register

#### 1 EPWM\_CMPC\_SHDW1 Register (Offset = 6BAh) [reset = 0h]

CMPC Shadow 1 Register.

Return to [Summary Table](#)

**Table 3-1198. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 06BAh       |
| EPWM0_G1      | 5004 06BAh       |
| EPWM0_G2      | 5008 06BAh       |
| EPWM0_G3      | 500C 06BAh       |
| EPWM1_G0      | 5000 16BAh       |
| EPWM1_G1      | 5004 16BAh       |
| EPWM1_G2      | 5008 16BAh       |
| EPWM1_G3      | 500C 16BAh       |
| EPWM2_G0      | 5000 26BAh       |
| EPWM2_G1      | 5004 26BAh       |
| EPWM2_G2      | 5008 26BAh       |
| EPWM2_G3      | 500C 26BAh       |
| EPWM3_G0      | 5000 36BAh       |
| EPWM3_G1      | 5004 36BAh       |
| EPWM3_G2      | 5008 36BAh       |
| EPWM3_G3      | 500C 36BAh       |
| EPWM4_G0      | 5000 46BAh       |
| EPWM4_G1      | 5004 46BAh       |
| EPWM4_G2      | 5008 46BAh       |
| EPWM4_G3      | 500C 46BAh       |
| EPWM5_G0      | 5000 56BAh       |
| EPWM5_G1      | 5004 56BAh       |
| EPWM5_G2      | 5008 56BAh       |
| EPWM5_G3      | 500C 56BAh       |
| EPWM6_G0      | 5000 66BAh       |
| EPWM6_G1      | 5004 66BAh       |
| EPWM6_G2      | 5008 66BAh       |
| EPWM6_G3      | 500C 66BAh       |
| EPWM7_G0      | 5000 76BAh       |
| EPWM7_G1      | 5004 76BAh       |
| EPWM7_G2      | 5008 76BAh       |
| EPWM7_G3      | 500C 76BAh       |
| EPWM8_G0      | 5000 86BAh       |
| EPWM8_G1      | 5004 86BAh       |
| EPWM8_G2      | 5008 86BAh       |
| EPWM8_G3      | 500C 86BAh       |
| EPWM9_G0      | 5000 96BAh       |
| EPWM9_G1      | 5004 96BAh       |
| EPWM9_G2      | 5008 96BAh       |

**Table 3-1198. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 96BAh       |
| EPWM10_G0     | 5000 A6BAh       |
| EPWM10_G1     | 5004 A6BAh       |
| EPWM10_G2     | 5008 A6BAh       |
| EPWM10_G3     | 500C A6BAh       |
| EPWM11_G0     | 5000 B6BAh       |
| EPWM11_G1     | 5004 B6BAh       |
| EPWM11_G2     | 5008 B6BAh       |
| EPWM11_G3     | 500C B6BAh       |
| EPWM12_G0     | 5000 C6BAh       |
| EPWM12_G1     | 5004 C6BAh       |
| EPWM12_G2     | 5008 C6BAh       |
| EPWM12_G3     | 500C C6BAh       |
| EPWM13_G0     | 5000 D6BAh       |
| EPWM13_G1     | 5004 D6BAh       |
| EPWM13_G2     | 5008 D6BAh       |
| EPWM13_G3     | 500C D6BAh       |
| EPWM14_G0     | 5000 E6BAh       |
| EPWM14_G1     | 5004 E6BAh       |
| EPWM14_G2     | 5008 E6BAh       |
| EPWM14_G3     | 500C E6BAh       |
| EPWM15_G0     | 5000 F6BAh       |
| EPWM15_G1     | 5004 F6BAh       |
| EPWM15_G2     | 5008 F6BAh       |
| EPWM15_G3     | 500C F6BAh       |
| EPWM16_G0     | 5001 06BAh       |
| EPWM16_G1     | 5005 06BAh       |
| EPWM16_G2     | 5009 06BAh       |
| EPWM16_G3     | 500D 06BAh       |
| EPWM17_G0     | 5001 16BAh       |
| EPWM17_G1     | 5005 16BAh       |
| EPWM17_G2     | 5009 16BAh       |
| EPWM17_G3     | 500D 16BAh       |
| EPWM18_G0     | 5001 26BAh       |
| EPWM18_G1     | 5005 26BAh       |
| EPWM18_G2     | 5009 26BAh       |
| EPWM18_G3     | 500D 26BAh       |
| EPWM19_G0     | 5001 36BAh       |
| EPWM19_G1     | 5005 36BAh       |
| EPWM19_G2     | 5009 36BAh       |
| EPWM19_G3     | 500D 36BAh       |
| EPWM20_G0     | 5001 46BAh       |
| EPWM20_G1     | 5005 46BAh       |
| EPWM20_G2     | 5009 46BAh       |
| EPWM20_G3     | 500D 46BAh       |



**Table 3-1198. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 56BAh       |
| EPWM21_G1     | 5005 56BAh       |
| EPWM21_G2     | 5009 56BAh       |
| EPWM21_G3     | 500D 56BAh       |
| EPWM22_G0     | 5001 66BAh       |
| EPWM22_G1     | 5005 66BAh       |
| EPWM22_G2     | 5009 66BAh       |
| EPWM22_G3     | 500D 66BAh       |
| EPWM23_G0     | 5001 76BAh       |
| EPWM23_G1     | 5005 76BAh       |
| EPWM23_G2     | 5009 76BAh       |
| EPWM23_G3     | 500D 76BAh       |
| EPWM24_G0     | 5001 86BAh       |
| EPWM24_G1     | 5005 86BAh       |
| EPWM24_G2     | 5009 86BAh       |
| EPWM24_G3     | 500D 86BAh       |
| EPWM25_G0     | 5001 96BAh       |
| EPWM25_G1     | 5005 96BAh       |
| EPWM25_G2     | 5009 96BAh       |
| EPWM25_G3     | 500D 96BAh       |
| EPWM26_G0     | 5001 A6BAh       |
| EPWM26_G1     | 5005 A6BAh       |
| EPWM26_G2     | 5009 A6BAh       |
| EPWM26_G3     | 500D A6BAh       |
| EPWM27_G0     | 5001 B6BAh       |
| EPWM27_G1     | 5005 B6BAh       |
| EPWM27_G2     | 5009 B6BAh       |
| EPWM27_G3     | 500D B6BAh       |
| EPWM28_G0     | 5001 C6BAh       |
| EPWM28_G1     | 5005 C6BAh       |
| EPWM28_G2     | 5009 C6BAh       |
| EPWM28_G3     | 500D C6BAh       |
| EPWM29_G0     | 5001 D6BAh       |
| EPWM29_G1     | 5005 D6BAh       |
| EPWM29_G2     | 5009 D6BAh       |
| EPWM29_G3     | 500D D6BAh       |
| EPWM30_G0     | 5001 E6BAh       |
| EPWM30_G1     | 5005 E6BAh       |
| EPWM30_G2     | 5009 E6BAh       |
| EPWM30_G3     | 500D E6BAh       |
| EPWM31_G0     | 5001 F6BAh       |
| EPWM31_G1     | 5005 F6BAh       |
| EPWM31_G2     | 5009 F6BAh       |
| EPWM31_G3     | 500D F6BAh       |

**Figure 3-380. EPWM\_CMPC\_SHDW1 Name Register**

|            |    |    |    |    |    |   |   |
|------------|----|----|----|----|----|---|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMPC_SHDW1 |    |    |    |    |    |   |   |
| R/W        |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| CMPC_SHDW1 |    |    |    |    |    |   |   |
| R/W        |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |

**Table 3-1200. EPWM\_CMPC\_SHDW1 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                 |
|------|------------|------|-------|-------------------------------------------------------------------------------------------------------------|
| 15:0 | CMPC_SHDW1 | R/W  | 0h    | The value in the CMPC_SHDW1 register is loaded into CMPC_ACTIVE register when shadow to active load occurs. |

### 3.7.2.130 EPWM\_CMPD\_SHDW1 Register

#### 1 EPWM\_CMPD\_SHDW1 Register (Offset = 6BEh) [reset = 0h]

CMPD Shadow 1 Register.

Return to [Summary Table](#)

**Table 3-1201. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 06BEh       |
| EPWM0_G1      | 5004 06BEh       |
| EPWM0_G2      | 5008 06BEh       |
| EPWM0_G3      | 500C 06BEh       |
| EPWM1_G0      | 5000 16BEh       |
| EPWM1_G1      | 5004 16BEh       |
| EPWM1_G2      | 5008 16BEh       |
| EPWM1_G3      | 500C 16BEh       |
| EPWM2_G0      | 5000 26BEh       |
| EPWM2_G1      | 5004 26BEh       |
| EPWM2_G2      | 5008 26BEh       |
| EPWM2_G3      | 500C 26BEh       |
| EPWM3_G0      | 5000 36BEh       |
| EPWM3_G1      | 5004 36BEh       |
| EPWM3_G2      | 5008 36BEh       |
| EPWM3_G3      | 500C 36BEh       |
| EPWM4_G0      | 5000 46BEh       |
| EPWM4_G1      | 5004 46BEh       |
| EPWM4_G2      | 5008 46BEh       |
| EPWM4_G3      | 500C 46BEh       |
| EPWM5_G0      | 5000 56BEh       |
| EPWM5_G1      | 5004 56BEh       |
| EPWM5_G2      | 5008 56BEh       |
| EPWM5_G3      | 500C 56BEh       |
| EPWM6_G0      | 5000 66BEh       |
| EPWM6_G1      | 5004 66BEh       |
| EPWM6_G2      | 5008 66BEh       |
| EPWM6_G3      | 500C 66BEh       |
| EPWM7_G0      | 5000 76BEh       |
| EPWM7_G1      | 5004 76BEh       |
| EPWM7_G2      | 5008 76BEh       |
| EPWM7_G3      | 500C 76BEh       |
| EPWM8_G0      | 5000 86BEh       |
| EPWM8_G1      | 5004 86BEh       |
| EPWM8_G2      | 5008 86BEh       |
| EPWM8_G3      | 500C 86BEh       |
| EPWM9_G0      | 5000 96BEh       |
| EPWM9_G1      | 5004 96BEh       |
| EPWM9_G2      | 5008 96BEh       |

**Table 3-1201. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 96BEh       |
| EPWM10_G0     | 5000 A6BEh       |
| EPWM10_G1     | 5004 A6BEh       |
| EPWM10_G2     | 5008 A6BEh       |
| EPWM10_G3     | 500C A6BEh       |
| EPWM11_G0     | 5000 B6BEh       |
| EPWM11_G1     | 5004 B6BEh       |
| EPWM11_G2     | 5008 B6BEh       |
| EPWM11_G3     | 500C B6BEh       |
| EPWM12_G0     | 5000 C6BEh       |
| EPWM12_G1     | 5004 C6BEh       |
| EPWM12_G2     | 5008 C6BEh       |
| EPWM12_G3     | 500C C6BEh       |
| EPWM13_G0     | 5000 D6BEh       |
| EPWM13_G1     | 5004 D6BEh       |
| EPWM13_G2     | 5008 D6BEh       |
| EPWM13_G3     | 500C D6BEh       |
| EPWM14_G0     | 5000 E6BEh       |
| EPWM14_G1     | 5004 E6BEh       |
| EPWM14_G2     | 5008 E6BEh       |
| EPWM14_G3     | 500C E6BEh       |
| EPWM15_G0     | 5000 F6BEh       |
| EPWM15_G1     | 5004 F6BEh       |
| EPWM15_G2     | 5008 F6BEh       |
| EPWM15_G3     | 500C F6BEh       |
| EPWM16_G0     | 5001 06BEh       |
| EPWM16_G1     | 5005 06BEh       |
| EPWM16_G2     | 5009 06BEh       |
| EPWM16_G3     | 500D 06BEh       |
| EPWM17_G0     | 5001 16BEh       |
| EPWM17_G1     | 5005 16BEh       |
| EPWM17_G2     | 5009 16BEh       |
| EPWM17_G3     | 500D 16BEh       |
| EPWM18_G0     | 5001 26BEh       |
| EPWM18_G1     | 5005 26BEh       |
| EPWM18_G2     | 5009 26BEh       |
| EPWM18_G3     | 500D 26BEh       |
| EPWM19_G0     | 5001 36BEh       |
| EPWM19_G1     | 5005 36BEh       |
| EPWM19_G2     | 5009 36BEh       |
| EPWM19_G3     | 500D 36BEh       |
| EPWM20_G0     | 5001 46BEh       |
| EPWM20_G1     | 5005 46BEh       |
| EPWM20_G2     | 5009 46BEh       |
| EPWM20_G3     | 500D 46BEh       |

**Table 3-1201. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 56BEh       |
| EPWM21_G1     | 5005 56BEh       |
| EPWM21_G2     | 5009 56BEh       |
| EPWM21_G3     | 500D 56BEh       |
| EPWM22_G0     | 5001 66BEh       |
| EPWM22_G1     | 5005 66BEh       |
| EPWM22_G2     | 5009 66BEh       |
| EPWM22_G3     | 500D 66BEh       |
| EPWM23_G0     | 5001 76BEh       |
| EPWM23_G1     | 5005 76BEh       |
| EPWM23_G2     | 5009 76BEh       |
| EPWM23_G3     | 500D 76BEh       |
| EPWM24_G0     | 5001 86BEh       |
| EPWM24_G1     | 5005 86BEh       |
| EPWM24_G2     | 5009 86BEh       |
| EPWM24_G3     | 500D 86BEh       |
| EPWM25_G0     | 5001 96BEh       |
| EPWM25_G1     | 5005 96BEh       |
| EPWM25_G2     | 5009 96BEh       |
| EPWM25_G3     | 500D 96BEh       |
| EPWM26_G0     | 5001 A6BEh       |
| EPWM26_G1     | 5005 A6BEh       |
| EPWM26_G2     | 5009 A6BEh       |
| EPWM26_G3     | 500D A6BEh       |
| EPWM27_G0     | 5001 B6BEh       |
| EPWM27_G1     | 5005 B6BEh       |
| EPWM27_G2     | 5009 B6BEh       |
| EPWM27_G3     | 500D B6BEh       |
| EPWM28_G0     | 5001 C6BEh       |
| EPWM28_G1     | 5005 C6BEh       |
| EPWM28_G2     | 5009 C6BEh       |
| EPWM28_G3     | 500D C6BEh       |
| EPWM29_G0     | 5001 D6BEh       |
| EPWM29_G1     | 5005 D6BEh       |
| EPWM29_G2     | 5009 D6BEh       |
| EPWM29_G3     | 500D D6BEh       |
| EPWM30_G0     | 5001 E6BEh       |
| EPWM30_G1     | 5005 E6BEh       |
| EPWM30_G2     | 5009 E6BEh       |
| EPWM30_G3     | 500D E6BEh       |
| EPWM31_G0     | 5001 F6BEh       |
| EPWM31_G1     | 5005 F6BEh       |
| EPWM31_G2     | 5009 F6BEh       |
| EPWM31_G3     | 500D F6BEh       |

**Figure 3-381. EPWM\_CMPD\_SHDW1 Name Register**

|            |    |    |    |    |    |   |   |
|------------|----|----|----|----|----|---|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMPD_SHDW1 |    |    |    |    |    |   |   |
| R/W        |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| CMPD_SHDW1 |    |    |    |    |    |   |   |
| R/W        |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |

**Table 3-1203. EPWM\_CMPD\_SHDW1 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                 |
|------|------------|------|-------|-------------------------------------------------------------------------------------------------------------|
| 15:0 | CMPD_SHDW1 | R/W  | 0h    | The value in the CMPD_SHDW1 register is loaded into CMPD_ACTIVE register when shadow to active load occurs. |

### 3.7.2.131 EPWM\_XMINMAX\_SHDW1 Register

#### 1 EPWM\_XMINMAX\_SHDW1 Register (Offset = 6C4h) [reset = 0h]

XMINMAX Shadow 1 Register.

Return to [Summary Table](#)

**Table 3-1204. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 06C4h       |
| EPWM0_G1      | 5004 06C4h       |
| EPWM0_G2      | 5008 06C4h       |
| EPWM0_G3      | 500C 06C4h       |
| EPWM1_G0      | 5000 16C4h       |
| EPWM1_G1      | 5004 16C4h       |
| EPWM1_G2      | 5008 16C4h       |
| EPWM1_G3      | 500C 16C4h       |
| EPWM2_G0      | 5000 26C4h       |
| EPWM2_G1      | 5004 26C4h       |
| EPWM2_G2      | 5008 26C4h       |
| EPWM2_G3      | 500C 26C4h       |
| EPWM3_G0      | 5000 36C4h       |
| EPWM3_G1      | 5004 36C4h       |
| EPWM3_G2      | 5008 36C4h       |
| EPWM3_G3      | 500C 36C4h       |
| EPWM4_G0      | 5000 46C4h       |
| EPWM4_G1      | 5004 46C4h       |
| EPWM4_G2      | 5008 46C4h       |
| EPWM4_G3      | 500C 46C4h       |
| EPWM5_G0      | 5000 56C4h       |
| EPWM5_G1      | 5004 56C4h       |
| EPWM5_G2      | 5008 56C4h       |
| EPWM5_G3      | 500C 56C4h       |
| EPWM6_G0      | 5000 66C4h       |
| EPWM6_G1      | 5004 66C4h       |
| EPWM6_G2      | 5008 66C4h       |
| EPWM6_G3      | 500C 66C4h       |
| EPWM7_G0      | 5000 76C4h       |
| EPWM7_G1      | 5004 76C4h       |
| EPWM7_G2      | 5008 76C4h       |
| EPWM7_G3      | 500C 76C4h       |
| EPWM8_G0      | 5000 86C4h       |
| EPWM8_G1      | 5004 86C4h       |
| EPWM8_G2      | 5008 86C4h       |
| EPWM8_G3      | 500C 86C4h       |
| EPWM9_G0      | 5000 96C4h       |
| EPWM9_G1      | 5004 96C4h       |
| EPWM9_G2      | 5008 96C4h       |

**Table 3-1204. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 96C4h       |
| EPWM10_G0     | 5000 A6C4h       |
| EPWM10_G1     | 5004 A6C4h       |
| EPWM10_G2     | 5008 A6C4h       |
| EPWM10_G3     | 500C A6C4h       |
| EPWM11_G0     | 5000 B6C4h       |
| EPWM11_G1     | 5004 B6C4h       |
| EPWM11_G2     | 5008 B6C4h       |
| EPWM11_G3     | 500C B6C4h       |
| EPWM12_G0     | 5000 C6C4h       |
| EPWM12_G1     | 5004 C6C4h       |
| EPWM12_G2     | 5008 C6C4h       |
| EPWM12_G3     | 500C C6C4h       |
| EPWM13_G0     | 5000 D6C4h       |
| EPWM13_G1     | 5004 D6C4h       |
| EPWM13_G2     | 5008 D6C4h       |
| EPWM13_G3     | 500C D6C4h       |
| EPWM14_G0     | 5000 E6C4h       |
| EPWM14_G1     | 5004 E6C4h       |
| EPWM14_G2     | 5008 E6C4h       |
| EPWM14_G3     | 500C E6C4h       |
| EPWM15_G0     | 5000 F6C4h       |
| EPWM15_G1     | 5004 F6C4h       |
| EPWM15_G2     | 5008 F6C4h       |
| EPWM15_G3     | 500C F6C4h       |
| EPWM16_G0     | 5001 06C4h       |
| EPWM16_G1     | 5005 06C4h       |
| EPWM16_G2     | 5009 06C4h       |
| EPWM16_G3     | 500D 06C4h       |
| EPWM17_G0     | 5001 16C4h       |
| EPWM17_G1     | 5005 16C4h       |
| EPWM17_G2     | 5009 16C4h       |
| EPWM17_G3     | 500D 16C4h       |
| EPWM18_G0     | 5001 26C4h       |
| EPWM18_G1     | 5005 26C4h       |
| EPWM18_G2     | 5009 26C4h       |
| EPWM18_G3     | 500D 26C4h       |
| EPWM19_G0     | 5001 36C4h       |
| EPWM19_G1     | 5005 36C4h       |
| EPWM19_G2     | 5009 36C4h       |
| EPWM19_G3     | 500D 36C4h       |
| EPWM20_G0     | 5001 46C4h       |
| EPWM20_G1     | 5005 46C4h       |
| EPWM20_G2     | 5009 46C4h       |
| EPWM20_G3     | 500D 46C4h       |



**Table 3-1204. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 56C4h       |
| EPWM21_G1     | 5005 56C4h       |
| EPWM21_G2     | 5009 56C4h       |
| EPWM21_G3     | 500D 56C4h       |
| EPWM22_G0     | 5001 66C4h       |
| EPWM22_G1     | 5005 66C4h       |
| EPWM22_G2     | 5009 66C4h       |
| EPWM22_G3     | 500D 66C4h       |
| EPWM23_G0     | 5001 76C4h       |
| EPWM23_G1     | 5005 76C4h       |
| EPWM23_G2     | 5009 76C4h       |
| EPWM23_G3     | 500D 76C4h       |
| EPWM24_G0     | 5001 86C4h       |
| EPWM24_G1     | 5005 86C4h       |
| EPWM24_G2     | 5009 86C4h       |
| EPWM24_G3     | 500D 86C4h       |
| EPWM25_G0     | 5001 96C4h       |
| EPWM25_G1     | 5005 96C4h       |
| EPWM25_G2     | 5009 96C4h       |
| EPWM25_G3     | 500D 96C4h       |
| EPWM26_G0     | 5001 A6C4h       |
| EPWM26_G1     | 5005 A6C4h       |
| EPWM26_G2     | 5009 A6C4h       |
| EPWM26_G3     | 500D A6C4h       |
| EPWM27_G0     | 5001 B6C4h       |
| EPWM27_G1     | 5005 B6C4h       |
| EPWM27_G2     | 5009 B6C4h       |
| EPWM27_G3     | 500D B6C4h       |
| EPWM28_G0     | 5001 C6C4h       |
| EPWM28_G1     | 5005 C6C4h       |
| EPWM28_G2     | 5009 C6C4h       |
| EPWM28_G3     | 500D C6C4h       |
| EPWM29_G0     | 5001 D6C4h       |
| EPWM29_G1     | 5005 D6C4h       |
| EPWM29_G2     | 5009 D6C4h       |
| EPWM29_G3     | 500D D6C4h       |
| EPWM30_G0     | 5001 E6C4h       |
| EPWM30_G1     | 5005 E6C4h       |
| EPWM30_G2     | 5009 E6C4h       |
| EPWM30_G3     | 500D E6C4h       |
| EPWM31_G0     | 5001 F6C4h       |
| EPWM31_G1     | 5005 F6C4h       |
| EPWM31_G2     | 5009 F6C4h       |
| EPWM31_G3     | 500D F6C4h       |

**Figure 3-382. EPWM\_XMINMAX\_SHDW1 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XMIN_SHDW1 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XMIN_SHDW1 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XMAX_SHDW1 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XMAX_SHDW1 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 3-1206. EPWM\_XMINMAX\_SHDW1 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                 |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------|
| 31:16 | XMIN_SHDW1 | R/W  | 0h    | The value in the XMIN_SHDW1 register is loaded into XMIN_ACTIVE register when shadow to active load occurs. |
| 15:0  | XMAX_SHDW1 | R/W  | 0h    | The value in the XMAX_SHDW1 register is loaded into XMAX_ACTIVE register when shadow to active load occurs. |

### 3.7.2.132 EPWM\_XCMP1\_SHDW2 Register

#### 1 EPWM\_XCMP1\_SHDW2 Register (Offset = 700h) [reset = 0h]

Additional Compare 1 Shadow 2 Register.

Return to [Summary Table](#)

**Table 3-1207. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0700h       |
| EPWM0_G1      | 5004 0700h       |
| EPWM0_G2      | 5008 0700h       |
| EPWM0_G3      | 500C 0700h       |
| EPWM1_G0      | 5000 1700h       |
| EPWM1_G1      | 5004 1700h       |
| EPWM1_G2      | 5008 1700h       |
| EPWM1_G3      | 500C 1700h       |
| EPWM2_G0      | 5000 2700h       |
| EPWM2_G1      | 5004 2700h       |
| EPWM2_G2      | 5008 2700h       |
| EPWM2_G3      | 500C 2700h       |
| EPWM3_G0      | 5000 3700h       |
| EPWM3_G1      | 5004 3700h       |
| EPWM3_G2      | 5008 3700h       |
| EPWM3_G3      | 500C 3700h       |
| EPWM4_G0      | 5000 4700h       |
| EPWM4_G1      | 5004 4700h       |
| EPWM4_G2      | 5008 4700h       |
| EPWM4_G3      | 500C 4700h       |
| EPWM5_G0      | 5000 5700h       |
| EPWM5_G1      | 5004 5700h       |
| EPWM5_G2      | 5008 5700h       |
| EPWM5_G3      | 500C 5700h       |
| EPWM6_G0      | 5000 6700h       |
| EPWM6_G1      | 5004 6700h       |
| EPWM6_G2      | 5008 6700h       |
| EPWM6_G3      | 500C 6700h       |
| EPWM7_G0      | 5000 7700h       |
| EPWM7_G1      | 5004 7700h       |
| EPWM7_G2      | 5008 7700h       |
| EPWM7_G3      | 500C 7700h       |
| EPWM8_G0      | 5000 8700h       |
| EPWM8_G1      | 5004 8700h       |
| EPWM8_G2      | 5008 8700h       |
| EPWM8_G3      | 500C 8700h       |
| EPWM9_G0      | 5000 9700h       |
| EPWM9_G1      | 5004 9700h       |
| EPWM9_G2      | 5008 9700h       |

**Table 3-1207. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9700h       |
| EPWM10_G0     | 5000 A700h       |
| EPWM10_G1     | 5004 A700h       |
| EPWM10_G2     | 5008 A700h       |
| EPWM10_G3     | 500C A700h       |
| EPWM11_G0     | 5000 B700h       |
| EPWM11_G1     | 5004 B700h       |
| EPWM11_G2     | 5008 B700h       |
| EPWM11_G3     | 500C B700h       |
| EPWM12_G0     | 5000 C700h       |
| EPWM12_G1     | 5004 C700h       |
| EPWM12_G2     | 5008 C700h       |
| EPWM12_G3     | 500C C700h       |
| EPWM13_G0     | 5000 D700h       |
| EPWM13_G1     | 5004 D700h       |
| EPWM13_G2     | 5008 D700h       |
| EPWM13_G3     | 500C D700h       |
| EPWM14_G0     | 5000 E700h       |
| EPWM14_G1     | 5004 E700h       |
| EPWM14_G2     | 5008 E700h       |
| EPWM14_G3     | 500C E700h       |
| EPWM15_G0     | 5000 F700h       |
| EPWM15_G1     | 5004 F700h       |
| EPWM15_G2     | 5008 F700h       |
| EPWM15_G3     | 500C F700h       |
| EPWM16_G0     | 5001 0700h       |
| EPWM16_G1     | 5005 0700h       |
| EPWM16_G2     | 5009 0700h       |
| EPWM16_G3     | 500D 0700h       |
| EPWM17_G0     | 5001 1700h       |
| EPWM17_G1     | 5005 1700h       |
| EPWM17_G2     | 5009 1700h       |
| EPWM17_G3     | 500D 1700h       |
| EPWM18_G0     | 5001 2700h       |
| EPWM18_G1     | 5005 2700h       |
| EPWM18_G2     | 5009 2700h       |
| EPWM18_G3     | 500D 2700h       |
| EPWM19_G0     | 5001 3700h       |
| EPWM19_G1     | 5005 3700h       |
| EPWM19_G2     | 5009 3700h       |
| EPWM19_G3     | 500D 3700h       |
| EPWM20_G0     | 5001 4700h       |
| EPWM20_G1     | 5005 4700h       |
| EPWM20_G2     | 5009 4700h       |
| EPWM20_G3     | 500D 4700h       |

**Table 3-1207. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5700h       |
| EPWM21_G1     | 5005 5700h       |
| EPWM21_G2     | 5009 5700h       |
| EPWM21_G3     | 500D 5700h       |
| EPWM22_G0     | 5001 6700h       |
| EPWM22_G1     | 5005 6700h       |
| EPWM22_G2     | 5009 6700h       |
| EPWM22_G3     | 500D 6700h       |
| EPWM23_G0     | 5001 7700h       |
| EPWM23_G1     | 5005 7700h       |
| EPWM23_G2     | 5009 7700h       |
| EPWM23_G3     | 500D 7700h       |
| EPWM24_G0     | 5001 8700h       |
| EPWM24_G1     | 5005 8700h       |
| EPWM24_G2     | 5009 8700h       |
| EPWM24_G3     | 500D 8700h       |
| EPWM25_G0     | 5001 9700h       |
| EPWM25_G1     | 5005 9700h       |
| EPWM25_G2     | 5009 9700h       |
| EPWM25_G3     | 500D 9700h       |
| EPWM26_G0     | 5001 A700h       |
| EPWM26_G1     | 5005 A700h       |
| EPWM26_G2     | 5009 A700h       |
| EPWM26_G3     | 500D A700h       |
| EPWM27_G0     | 5001 B700h       |
| EPWM27_G1     | 5005 B700h       |
| EPWM27_G2     | 5009 B700h       |
| EPWM27_G3     | 500D B700h       |
| EPWM28_G0     | 5001 C700h       |
| EPWM28_G1     | 5005 C700h       |
| EPWM28_G2     | 5009 C700h       |
| EPWM28_G3     | 500D C700h       |
| EPWM29_G0     | 5001 D700h       |
| EPWM29_G1     | 5005 D700h       |
| EPWM29_G2     | 5009 D700h       |
| EPWM29_G3     | 500D D700h       |
| EPWM30_G0     | 5001 E700h       |
| EPWM30_G1     | 5005 E700h       |
| EPWM30_G2     | 5009 E700h       |
| EPWM30_G3     | 500D E700h       |
| EPWM31_G0     | 5001 F700h       |
| EPWM31_G1     | 5005 F700h       |
| EPWM31_G2     | 5009 F700h       |
| EPWM31_G3     | 500D F700h       |

**Figure 3-383. EPWM\_XCMP1\_SHDW2 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP1_SHDW2   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP1_SHDW2   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP1HR_SHDW2 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP1HR_SHDW2 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 3-1209. EPWM\_XCMP1\_SHDW2 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                 |
|-------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP1_SHDW2   | R/W  | 0h    | XCMP1_SHDW2 Register<br>The value in the XCMP1_SHDW2 register is loaded into XCMP1_ACTIVE register when shadow to active load occurs.       |
| 15:0  | XCMP1HR_SHDW2 | R/W  | 0h    | XCMP1HR_SHDW2 Register<br>The value in the XCMP1HR_SHDW2 register is loaded into XCMP1HR_ACTIVE register when shadow to active load occurs. |

### 3.7.2.133 EPWM\_XCMP2\_SHDW2 Register

#### 1 EPWM\_XCMP2\_SHDW2 Register (Offset = 704h) [reset = 0h]

Additional Compare 2 Shadow 2 Register.

Return to [Summary Table](#)

**Table 3-1210. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0704h       |
| EPWM0_G1      | 5004 0704h       |
| EPWM0_G2      | 5008 0704h       |
| EPWM0_G3      | 500C 0704h       |
| EPWM1_G0      | 5000 1704h       |
| EPWM1_G1      | 5004 1704h       |
| EPWM1_G2      | 5008 1704h       |
| EPWM1_G3      | 500C 1704h       |
| EPWM2_G0      | 5000 2704h       |
| EPWM2_G1      | 5004 2704h       |
| EPWM2_G2      | 5008 2704h       |
| EPWM2_G3      | 500C 2704h       |
| EPWM3_G0      | 5000 3704h       |
| EPWM3_G1      | 5004 3704h       |
| EPWM3_G2      | 5008 3704h       |
| EPWM3_G3      | 500C 3704h       |
| EPWM4_G0      | 5000 4704h       |
| EPWM4_G1      | 5004 4704h       |
| EPWM4_G2      | 5008 4704h       |
| EPWM4_G3      | 500C 4704h       |
| EPWM5_G0      | 5000 5704h       |
| EPWM5_G1      | 5004 5704h       |
| EPWM5_G2      | 5008 5704h       |
| EPWM5_G3      | 500C 5704h       |
| EPWM6_G0      | 5000 6704h       |
| EPWM6_G1      | 5004 6704h       |
| EPWM6_G2      | 5008 6704h       |
| EPWM6_G3      | 500C 6704h       |
| EPWM7_G0      | 5000 7704h       |
| EPWM7_G1      | 5004 7704h       |
| EPWM7_G2      | 5008 7704h       |
| EPWM7_G3      | 500C 7704h       |
| EPWM8_G0      | 5000 8704h       |
| EPWM8_G1      | 5004 8704h       |
| EPWM8_G2      | 5008 8704h       |
| EPWM8_G3      | 500C 8704h       |
| EPWM9_G0      | 5000 9704h       |
| EPWM9_G1      | 5004 9704h       |
| EPWM9_G2      | 5008 9704h       |

**Table 3-1210. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9704h       |
| EPWM10_G0     | 5000 A704h       |
| EPWM10_G1     | 5004 A704h       |
| EPWM10_G2     | 5008 A704h       |
| EPWM10_G3     | 500C A704h       |
| EPWM11_G0     | 5000 B704h       |
| EPWM11_G1     | 5004 B704h       |
| EPWM11_G2     | 5008 B704h       |
| EPWM11_G3     | 500C B704h       |
| EPWM12_G0     | 5000 C704h       |
| EPWM12_G1     | 5004 C704h       |
| EPWM12_G2     | 5008 C704h       |
| EPWM12_G3     | 500C C704h       |
| EPWM13_G0     | 5000 D704h       |
| EPWM13_G1     | 5004 D704h       |
| EPWM13_G2     | 5008 D704h       |
| EPWM13_G3     | 500C D704h       |
| EPWM14_G0     | 5000 E704h       |
| EPWM14_G1     | 5004 E704h       |
| EPWM14_G2     | 5008 E704h       |
| EPWM14_G3     | 500C E704h       |
| EPWM15_G0     | 5000 F704h       |
| EPWM15_G1     | 5004 F704h       |
| EPWM15_G2     | 5008 F704h       |
| EPWM15_G3     | 500C F704h       |
| EPWM16_G0     | 5001 0704h       |
| EPWM16_G1     | 5005 0704h       |
| EPWM16_G2     | 5009 0704h       |
| EPWM16_G3     | 500D 0704h       |
| EPWM17_G0     | 5001 1704h       |
| EPWM17_G1     | 5005 1704h       |
| EPWM17_G2     | 5009 1704h       |
| EPWM17_G3     | 500D 1704h       |
| EPWM18_G0     | 5001 2704h       |
| EPWM18_G1     | 5005 2704h       |
| EPWM18_G2     | 5009 2704h       |
| EPWM18_G3     | 500D 2704h       |
| EPWM19_G0     | 5001 3704h       |
| EPWM19_G1     | 5005 3704h       |
| EPWM19_G2     | 5009 3704h       |
| EPWM19_G3     | 500D 3704h       |
| EPWM20_G0     | 5001 4704h       |
| EPWM20_G1     | 5005 4704h       |
| EPWM20_G2     | 5009 4704h       |
| EPWM20_G3     | 500D 4704h       |



**Table 3-1210. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5704h       |
| EPWM21_G1     | 5005 5704h       |
| EPWM21_G2     | 5009 5704h       |
| EPWM21_G3     | 500D 5704h       |
| EPWM22_G0     | 5001 6704h       |
| EPWM22_G1     | 5005 6704h       |
| EPWM22_G2     | 5009 6704h       |
| EPWM22_G3     | 500D 6704h       |
| EPWM23_G0     | 5001 7704h       |
| EPWM23_G1     | 5005 7704h       |
| EPWM23_G2     | 5009 7704h       |
| EPWM23_G3     | 500D 7704h       |
| EPWM24_G0     | 5001 8704h       |
| EPWM24_G1     | 5005 8704h       |
| EPWM24_G2     | 5009 8704h       |
| EPWM24_G3     | 500D 8704h       |
| EPWM25_G0     | 5001 9704h       |
| EPWM25_G1     | 5005 9704h       |
| EPWM25_G2     | 5009 9704h       |
| EPWM25_G3     | 500D 9704h       |
| EPWM26_G0     | 5001 A704h       |
| EPWM26_G1     | 5005 A704h       |
| EPWM26_G2     | 5009 A704h       |
| EPWM26_G3     | 500D A704h       |
| EPWM27_G0     | 5001 B704h       |
| EPWM27_G1     | 5005 B704h       |
| EPWM27_G2     | 5009 B704h       |
| EPWM27_G3     | 500D B704h       |
| EPWM28_G0     | 5001 C704h       |
| EPWM28_G1     | 5005 C704h       |
| EPWM28_G2     | 5009 C704h       |
| EPWM28_G3     | 500D C704h       |
| EPWM29_G0     | 5001 D704h       |
| EPWM29_G1     | 5005 D704h       |
| EPWM29_G2     | 5009 D704h       |
| EPWM29_G3     | 500D D704h       |
| EPWM30_G0     | 5001 E704h       |
| EPWM30_G1     | 5005 E704h       |
| EPWM30_G2     | 5009 E704h       |
| EPWM30_G3     | 500D E704h       |
| EPWM31_G0     | 5001 F704h       |
| EPWM31_G1     | 5005 F704h       |
| EPWM31_G2     | 5009 F704h       |
| EPWM31_G3     | 500D F704h       |

**Figure 3-384. EPWM\_XCMP2\_SHDW2 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP2_SHDW2   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP2_SHDW2   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP2HR_SHDW2 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP2HR_SHDW2 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 3-1212. EPWM\_XCMP2\_SHDW2 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                 |
|-------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP2_SHDW2   | R/W  | 0h    | XCMP2_SHDW2 Register<br>The value in the XCMP2_SHDW2 register is loaded into XCMP2_ACTIVE register when shadow to active load occurs.       |
| 15:0  | XCMP2HR_SHDW2 | R/W  | 0h    | XCMP2HR_SHDW2 Register<br>The value in the XCMP2HR_SHDW2 register is loaded into XCMP2HR_ACTIVE register when shadow to active load occurs. |

### 3.7.2.134 EPWM\_XCMP3\_SHDW2 Register

#### 1 EPWM\_XCMP3\_SHDW2 Register (Offset = 708h) [reset = 0h]

Additional Compare 3 Shadow 2 Register.

Return to [Summary Table](#)

**Table 3-1213. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0708h       |
| EPWM0_G1      | 5004 0708h       |
| EPWM0_G2      | 5008 0708h       |
| EPWM0_G3      | 500C 0708h       |
| EPWM1_G0      | 5000 1708h       |
| EPWM1_G1      | 5004 1708h       |
| EPWM1_G2      | 5008 1708h       |
| EPWM1_G3      | 500C 1708h       |
| EPWM2_G0      | 5000 2708h       |
| EPWM2_G1      | 5004 2708h       |
| EPWM2_G2      | 5008 2708h       |
| EPWM2_G3      | 500C 2708h       |
| EPWM3_G0      | 5000 3708h       |
| EPWM3_G1      | 5004 3708h       |
| EPWM3_G2      | 5008 3708h       |
| EPWM3_G3      | 500C 3708h       |
| EPWM4_G0      | 5000 4708h       |
| EPWM4_G1      | 5004 4708h       |
| EPWM4_G2      | 5008 4708h       |
| EPWM4_G3      | 500C 4708h       |
| EPWM5_G0      | 5000 5708h       |
| EPWM5_G1      | 5004 5708h       |
| EPWM5_G2      | 5008 5708h       |
| EPWM5_G3      | 500C 5708h       |
| EPWM6_G0      | 5000 6708h       |
| EPWM6_G1      | 5004 6708h       |
| EPWM6_G2      | 5008 6708h       |
| EPWM6_G3      | 500C 6708h       |
| EPWM7_G0      | 5000 7708h       |
| EPWM7_G1      | 5004 7708h       |
| EPWM7_G2      | 5008 7708h       |
| EPWM7_G3      | 500C 7708h       |
| EPWM8_G0      | 5000 8708h       |
| EPWM8_G1      | 5004 8708h       |
| EPWM8_G2      | 5008 8708h       |
| EPWM8_G3      | 500C 8708h       |
| EPWM9_G0      | 5000 9708h       |
| EPWM9_G1      | 5004 9708h       |
| EPWM9_G2      | 5008 9708h       |

**Table 3-1213. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9708h       |
| EPWM10_G0     | 5000 A708h       |
| EPWM10_G1     | 5004 A708h       |
| EPWM10_G2     | 5008 A708h       |
| EPWM10_G3     | 500C A708h       |
| EPWM11_G0     | 5000 B708h       |
| EPWM11_G1     | 5004 B708h       |
| EPWM11_G2     | 5008 B708h       |
| EPWM11_G3     | 500C B708h       |
| EPWM12_G0     | 5000 C708h       |
| EPWM12_G1     | 5004 C708h       |
| EPWM12_G2     | 5008 C708h       |
| EPWM12_G3     | 500C C708h       |
| EPWM13_G0     | 5000 D708h       |
| EPWM13_G1     | 5004 D708h       |
| EPWM13_G2     | 5008 D708h       |
| EPWM13_G3     | 500C D708h       |
| EPWM14_G0     | 5000 E708h       |
| EPWM14_G1     | 5004 E708h       |
| EPWM14_G2     | 5008 E708h       |
| EPWM14_G3     | 500C E708h       |
| EPWM15_G0     | 5000 F708h       |
| EPWM15_G1     | 5004 F708h       |
| EPWM15_G2     | 5008 F708h       |
| EPWM15_G3     | 500C F708h       |
| EPWM16_G0     | 5001 0708h       |
| EPWM16_G1     | 5005 0708h       |
| EPWM16_G2     | 5009 0708h       |
| EPWM16_G3     | 500D 0708h       |
| EPWM17_G0     | 5001 1708h       |
| EPWM17_G1     | 5005 1708h       |
| EPWM17_G2     | 5009 1708h       |
| EPWM17_G3     | 500D 1708h       |
| EPWM18_G0     | 5001 2708h       |
| EPWM18_G1     | 5005 2708h       |
| EPWM18_G2     | 5009 2708h       |
| EPWM18_G3     | 500D 2708h       |
| EPWM19_G0     | 5001 3708h       |
| EPWM19_G1     | 5005 3708h       |
| EPWM19_G2     | 5009 3708h       |
| EPWM19_G3     | 500D 3708h       |
| EPWM20_G0     | 5001 4708h       |
| EPWM20_G1     | 5005 4708h       |
| EPWM20_G2     | 5009 4708h       |
| EPWM20_G3     | 500D 4708h       |

**Table 3-1213. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5708h       |
| EPWM21_G1     | 5005 5708h       |
| EPWM21_G2     | 5009 5708h       |
| EPWM21_G3     | 500D 5708h       |
| EPWM22_G0     | 5001 6708h       |
| EPWM22_G1     | 5005 6708h       |
| EPWM22_G2     | 5009 6708h       |
| EPWM22_G3     | 500D 6708h       |
| EPWM23_G0     | 5001 7708h       |
| EPWM23_G1     | 5005 7708h       |
| EPWM23_G2     | 5009 7708h       |
| EPWM23_G3     | 500D 7708h       |
| EPWM24_G0     | 5001 8708h       |
| EPWM24_G1     | 5005 8708h       |
| EPWM24_G2     | 5009 8708h       |
| EPWM24_G3     | 500D 8708h       |
| EPWM25_G0     | 5001 9708h       |
| EPWM25_G1     | 5005 9708h       |
| EPWM25_G2     | 5009 9708h       |
| EPWM25_G3     | 500D 9708h       |
| EPWM26_G0     | 5001 A708h       |
| EPWM26_G1     | 5005 A708h       |
| EPWM26_G2     | 5009 A708h       |
| EPWM26_G3     | 500D A708h       |
| EPWM27_G0     | 5001 B708h       |
| EPWM27_G1     | 5005 B708h       |
| EPWM27_G2     | 5009 B708h       |
| EPWM27_G3     | 500D B708h       |
| EPWM28_G0     | 5001 C708h       |
| EPWM28_G1     | 5005 C708h       |
| EPWM28_G2     | 5009 C708h       |
| EPWM28_G3     | 500D C708h       |
| EPWM29_G0     | 5001 D708h       |
| EPWM29_G1     | 5005 D708h       |
| EPWM29_G2     | 5009 D708h       |
| EPWM29_G3     | 500D D708h       |
| EPWM30_G0     | 5001 E708h       |
| EPWM30_G1     | 5005 E708h       |
| EPWM30_G2     | 5009 E708h       |
| EPWM30_G3     | 500D E708h       |
| EPWM31_G0     | 5001 F708h       |
| EPWM31_G1     | 5005 F708h       |
| EPWM31_G2     | 5009 F708h       |
| EPWM31_G3     | 500D F708h       |

**Figure 3-385. EPWM\_XCMP3\_SHDW2 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP3_SHDW2   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP3_SHDW2   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP3HR_SHDW2 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP3HR_SHDW2 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 3-1215. EPWM\_XCMP3\_SHDW2 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                 |
|-------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP3_SHDW2   | R/W  | 0h    | XCMP3_SHDW2 Register<br>The value in the XCMP3_SHDW2 register is loaded into XCMP3_ACTIVE register when shadow to active load occurs.       |
| 15:0  | XCMP3HR_SHDW2 | R/W  | 0h    | XCMP3HR_SHDW2 Register<br>The value in the XCMP3HR_SHDW2 register is loaded into XCMP3HR_ACTIVE register when shadow to active load occurs. |

### 3.7.2.135 EPWM\_XCMP4\_SHDW2 Register

#### 1 EPWM\_XCMP4\_SHDW2 Register (Offset = 70Ch) [reset = 0h]

Additional Compare 4 Shadow 2 Register.

Return to [Summary Table](#)

**Table 3-1216. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 070Ch       |
| EPWM0_G1      | 5004 070Ch       |
| EPWM0_G2      | 5008 070Ch       |
| EPWM0_G3      | 500C 070Ch       |
| EPWM1_G0      | 5000 170Ch       |
| EPWM1_G1      | 5004 170Ch       |
| EPWM1_G2      | 5008 170Ch       |
| EPWM1_G3      | 500C 170Ch       |
| EPWM2_G0      | 5000 270Ch       |
| EPWM2_G1      | 5004 270Ch       |
| EPWM2_G2      | 5008 270Ch       |
| EPWM2_G3      | 500C 270Ch       |
| EPWM3_G0      | 5000 370Ch       |
| EPWM3_G1      | 5004 370Ch       |
| EPWM3_G2      | 5008 370Ch       |
| EPWM3_G3      | 500C 370Ch       |
| EPWM4_G0      | 5000 470Ch       |
| EPWM4_G1      | 5004 470Ch       |
| EPWM4_G2      | 5008 470Ch       |
| EPWM4_G3      | 500C 470Ch       |
| EPWM5_G0      | 5000 570Ch       |
| EPWM5_G1      | 5004 570Ch       |
| EPWM5_G2      | 5008 570Ch       |
| EPWM5_G3      | 500C 570Ch       |
| EPWM6_G0      | 5000 670Ch       |
| EPWM6_G1      | 5004 670Ch       |
| EPWM6_G2      | 5008 670Ch       |
| EPWM6_G3      | 500C 670Ch       |
| EPWM7_G0      | 5000 770Ch       |
| EPWM7_G1      | 5004 770Ch       |
| EPWM7_G2      | 5008 770Ch       |
| EPWM7_G3      | 500C 770Ch       |
| EPWM8_G0      | 5000 870Ch       |
| EPWM8_G1      | 5004 870Ch       |
| EPWM8_G2      | 5008 870Ch       |
| EPWM8_G3      | 500C 870Ch       |
| EPWM9_G0      | 5000 970Ch       |
| EPWM9_G1      | 5004 970Ch       |
| EPWM9_G2      | 5008 970Ch       |

**Table 3-1216. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 970Ch       |
| EPWM10_G0     | 5000 A70Ch       |
| EPWM10_G1     | 5004 A70Ch       |
| EPWM10_G2     | 5008 A70Ch       |
| EPWM10_G3     | 500C A70Ch       |
| EPWM11_G0     | 5000 B70Ch       |
| EPWM11_G1     | 5004 B70Ch       |
| EPWM11_G2     | 5008 B70Ch       |
| EPWM11_G3     | 500C B70Ch       |
| EPWM12_G0     | 5000 C70Ch       |
| EPWM12_G1     | 5004 C70Ch       |
| EPWM12_G2     | 5008 C70Ch       |
| EPWM12_G3     | 500C C70Ch       |
| EPWM13_G0     | 5000 D70Ch       |
| EPWM13_G1     | 5004 D70Ch       |
| EPWM13_G2     | 5008 D70Ch       |
| EPWM13_G3     | 500C D70Ch       |
| EPWM14_G0     | 5000 E70Ch       |
| EPWM14_G1     | 5004 E70Ch       |
| EPWM14_G2     | 5008 E70Ch       |
| EPWM14_G3     | 500C E70Ch       |
| EPWM15_G0     | 5000 F70Ch       |
| EPWM15_G1     | 5004 F70Ch       |
| EPWM15_G2     | 5008 F70Ch       |
| EPWM15_G3     | 500C F70Ch       |
| EPWM16_G0     | 5001 070Ch       |
| EPWM16_G1     | 5005 070Ch       |
| EPWM16_G2     | 5009 070Ch       |
| EPWM16_G3     | 500D 070Ch       |
| EPWM17_G0     | 5001 170Ch       |
| EPWM17_G1     | 5005 170Ch       |
| EPWM17_G2     | 5009 170Ch       |
| EPWM17_G3     | 500D 170Ch       |
| EPWM18_G0     | 5001 270Ch       |
| EPWM18_G1     | 5005 270Ch       |
| EPWM18_G2     | 5009 270Ch       |
| EPWM18_G3     | 500D 270Ch       |
| EPWM19_G0     | 5001 370Ch       |
| EPWM19_G1     | 5005 370Ch       |
| EPWM19_G2     | 5009 370Ch       |
| EPWM19_G3     | 500D 370Ch       |
| EPWM20_G0     | 5001 470Ch       |
| EPWM20_G1     | 5005 470Ch       |
| EPWM20_G2     | 5009 470Ch       |
| EPWM20_G3     | 500D 470Ch       |



**Table 3-1216. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 570Ch       |
| EPWM21_G1     | 5005 570Ch       |
| EPWM21_G2     | 5009 570Ch       |
| EPWM21_G3     | 500D 570Ch       |
| EPWM22_G0     | 5001 670Ch       |
| EPWM22_G1     | 5005 670Ch       |
| EPWM22_G2     | 5009 670Ch       |
| EPWM22_G3     | 500D 670Ch       |
| EPWM23_G0     | 5001 770Ch       |
| EPWM23_G1     | 5005 770Ch       |
| EPWM23_G2     | 5009 770Ch       |
| EPWM23_G3     | 500D 770Ch       |
| EPWM24_G0     | 5001 870Ch       |
| EPWM24_G1     | 5005 870Ch       |
| EPWM24_G2     | 5009 870Ch       |
| EPWM24_G3     | 500D 870Ch       |
| EPWM25_G0     | 5001 970Ch       |
| EPWM25_G1     | 5005 970Ch       |
| EPWM25_G2     | 5009 970Ch       |
| EPWM25_G3     | 500D 970Ch       |
| EPWM26_G0     | 5001 A70Ch       |
| EPWM26_G1     | 5005 A70Ch       |
| EPWM26_G2     | 5009 A70Ch       |
| EPWM26_G3     | 500D A70Ch       |
| EPWM27_G0     | 5001 B70Ch       |
| EPWM27_G1     | 5005 B70Ch       |
| EPWM27_G2     | 5009 B70Ch       |
| EPWM27_G3     | 500D B70Ch       |
| EPWM28_G0     | 5001 C70Ch       |
| EPWM28_G1     | 5005 C70Ch       |
| EPWM28_G2     | 5009 C70Ch       |
| EPWM28_G3     | 500D C70Ch       |
| EPWM29_G0     | 5001 D70Ch       |
| EPWM29_G1     | 5005 D70Ch       |
| EPWM29_G2     | 5009 D70Ch       |
| EPWM29_G3     | 500D D70Ch       |
| EPWM30_G0     | 5001 E70Ch       |
| EPWM30_G1     | 5005 E70Ch       |
| EPWM30_G2     | 5009 E70Ch       |
| EPWM30_G3     | 500D E70Ch       |
| EPWM31_G0     | 5001 F70Ch       |
| EPWM31_G1     | 5005 F70Ch       |
| EPWM31_G2     | 5009 F70Ch       |
| EPWM31_G3     | 500D F70Ch       |

**Figure 3-386. EPWM\_XCMP4\_SHDW2 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP4_SHDW2   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP4_SHDW2   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP4HR_SHDW2 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP4HR_SHDW2 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 3-1218. EPWM\_XCMP4\_SHDW2 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                 |
|-------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP4_SHDW2   | R/W  | 0h    | XCMP4_SHDW2 Register<br>The value in the XCMP4_SHDW2 register is loaded into XCMP4_ACTIVE register when shadow to active load occurs.       |
| 15:0  | XCMP4HR_SHDW2 | R/W  | 0h    | XCMP4HR_SHDW2 Register<br>The value in the XCMP4HR_SHDW2 register is loaded into XCMP4HR_ACTIVE register when shadow to active load occurs. |

### 3.7.2.136 EPWM\_XCMP5\_SHDW2 Register

#### 1 EPWM\_XCMP5\_SHDW2 Register (Offset = 710h) [reset = 0h]

Additional Compare 5 Shadow 2 Register.

Return to [Summary Table](#)

**Table 3-1219. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0710h       |
| EPWM0_G1      | 5004 0710h       |
| EPWM0_G2      | 5008 0710h       |
| EPWM0_G3      | 500C 0710h       |
| EPWM1_G0      | 5000 1710h       |
| EPWM1_G1      | 5004 1710h       |
| EPWM1_G2      | 5008 1710h       |
| EPWM1_G3      | 500C 1710h       |
| EPWM2_G0      | 5000 2710h       |
| EPWM2_G1      | 5004 2710h       |
| EPWM2_G2      | 5008 2710h       |
| EPWM2_G3      | 500C 2710h       |
| EPWM3_G0      | 5000 3710h       |
| EPWM3_G1      | 5004 3710h       |
| EPWM3_G2      | 5008 3710h       |
| EPWM3_G3      | 500C 3710h       |
| EPWM4_G0      | 5000 4710h       |
| EPWM4_G1      | 5004 4710h       |
| EPWM4_G2      | 5008 4710h       |
| EPWM4_G3      | 500C 4710h       |
| EPWM5_G0      | 5000 5710h       |
| EPWM5_G1      | 5004 5710h       |
| EPWM5_G2      | 5008 5710h       |
| EPWM5_G3      | 500C 5710h       |
| EPWM6_G0      | 5000 6710h       |
| EPWM6_G1      | 5004 6710h       |
| EPWM6_G2      | 5008 6710h       |
| EPWM6_G3      | 500C 6710h       |
| EPWM7_G0      | 5000 7710h       |
| EPWM7_G1      | 5004 7710h       |
| EPWM7_G2      | 5008 7710h       |
| EPWM7_G3      | 500C 7710h       |
| EPWM8_G0      | 5000 8710h       |
| EPWM8_G1      | 5004 8710h       |
| EPWM8_G2      | 5008 8710h       |
| EPWM8_G3      | 500C 8710h       |
| EPWM9_G0      | 5000 9710h       |
| EPWM9_G1      | 5004 9710h       |
| EPWM9_G2      | 5008 9710h       |

**Table 3-1219. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9710h       |
| EPWM10_G0     | 5000 A710h       |
| EPWM10_G1     | 5004 A710h       |
| EPWM10_G2     | 5008 A710h       |
| EPWM10_G3     | 500C A710h       |
| EPWM11_G0     | 5000 B710h       |
| EPWM11_G1     | 5004 B710h       |
| EPWM11_G2     | 5008 B710h       |
| EPWM11_G3     | 500C B710h       |
| EPWM12_G0     | 5000 C710h       |
| EPWM12_G1     | 5004 C710h       |
| EPWM12_G2     | 5008 C710h       |
| EPWM12_G3     | 500C C710h       |
| EPWM13_G0     | 5000 D710h       |
| EPWM13_G1     | 5004 D710h       |
| EPWM13_G2     | 5008 D710h       |
| EPWM13_G3     | 500C D710h       |
| EPWM14_G0     | 5000 E710h       |
| EPWM14_G1     | 5004 E710h       |
| EPWM14_G2     | 5008 E710h       |
| EPWM14_G3     | 500C E710h       |
| EPWM15_G0     | 5000 F710h       |
| EPWM15_G1     | 5004 F710h       |
| EPWM15_G2     | 5008 F710h       |
| EPWM15_G3     | 500C F710h       |
| EPWM16_G0     | 5001 0710h       |
| EPWM16_G1     | 5005 0710h       |
| EPWM16_G2     | 5009 0710h       |
| EPWM16_G3     | 500D 0710h       |
| EPWM17_G0     | 5001 1710h       |
| EPWM17_G1     | 5005 1710h       |
| EPWM17_G2     | 5009 1710h       |
| EPWM17_G3     | 500D 1710h       |
| EPWM18_G0     | 5001 2710h       |
| EPWM18_G1     | 5005 2710h       |
| EPWM18_G2     | 5009 2710h       |
| EPWM18_G3     | 500D 2710h       |
| EPWM19_G0     | 5001 3710h       |
| EPWM19_G1     | 5005 3710h       |
| EPWM19_G2     | 5009 3710h       |
| EPWM19_G3     | 500D 3710h       |
| EPWM20_G0     | 5001 4710h       |
| EPWM20_G1     | 5005 4710h       |
| EPWM20_G2     | 5009 4710h       |
| EPWM20_G3     | 500D 4710h       |

**Table 3-1219. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5710h       |
| EPWM21_G1     | 5005 5710h       |
| EPWM21_G2     | 5009 5710h       |
| EPWM21_G3     | 500D 5710h       |
| EPWM22_G0     | 5001 6710h       |
| EPWM22_G1     | 5005 6710h       |
| EPWM22_G2     | 5009 6710h       |
| EPWM22_G3     | 500D 6710h       |
| EPWM23_G0     | 5001 7710h       |
| EPWM23_G1     | 5005 7710h       |
| EPWM23_G2     | 5009 7710h       |
| EPWM23_G3     | 500D 7710h       |
| EPWM24_G0     | 5001 8710h       |
| EPWM24_G1     | 5005 8710h       |
| EPWM24_G2     | 5009 8710h       |
| EPWM24_G3     | 500D 8710h       |
| EPWM25_G0     | 5001 9710h       |
| EPWM25_G1     | 5005 9710h       |
| EPWM25_G2     | 5009 9710h       |
| EPWM25_G3     | 500D 9710h       |
| EPWM26_G0     | 5001 A710h       |
| EPWM26_G1     | 5005 A710h       |
| EPWM26_G2     | 5009 A710h       |
| EPWM26_G3     | 500D A710h       |
| EPWM27_G0     | 5001 B710h       |
| EPWM27_G1     | 5005 B710h       |
| EPWM27_G2     | 5009 B710h       |
| EPWM27_G3     | 500D B710h       |
| EPWM28_G0     | 5001 C710h       |
| EPWM28_G1     | 5005 C710h       |
| EPWM28_G2     | 5009 C710h       |
| EPWM28_G3     | 500D C710h       |
| EPWM29_G0     | 5001 D710h       |
| EPWM29_G1     | 5005 D710h       |
| EPWM29_G2     | 5009 D710h       |
| EPWM29_G3     | 500D D710h       |
| EPWM30_G0     | 5001 E710h       |
| EPWM30_G1     | 5005 E710h       |
| EPWM30_G2     | 5009 E710h       |
| EPWM30_G3     | 500D E710h       |
| EPWM31_G0     | 5001 F710h       |
| EPWM31_G1     | 5005 F710h       |
| EPWM31_G2     | 5009 F710h       |
| EPWM31_G3     | 500D F710h       |

**Figure 3-387. EPWM\_XCMP5\_SHDW2 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP5_SHDW2   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP5_SHDW2   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP5HR_SHDW2 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP5HR_SHDW2 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 3-1221. EPWM\_XCMP5\_SHDW2 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                 |
|-------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP5_SHDW2   | R/W  | 0h    | XCMP5_SHDW2 Register<br>The value in the XCMP5_SHDW2 register is loaded into XCMP5_ACTIVE register when shadow to active load occurs.       |
| 15:0  | XCMP5HR_SHDW2 | R/W  | 0h    | XCMP5HR_SHDW2 Register<br>The value in the XCMP5HR_SHDW2 register is loaded into XCMP5HR_ACTIVE register when shadow to active load occurs. |

### 3.7.2.137 EPWM\_XCMP6\_SHDW2 Register

#### 1 EPWM\_XCMP6\_SHDW2 Register (Offset = 714h) [reset = 0h]

Additional Compare 6 Shadow 2 Register.

Return to [Summary Table](#)

**Table 3-1222. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0714h       |
| EPWM0_G1      | 5004 0714h       |
| EPWM0_G2      | 5008 0714h       |
| EPWM0_G3      | 500C 0714h       |
| EPWM1_G0      | 5000 1714h       |
| EPWM1_G1      | 5004 1714h       |
| EPWM1_G2      | 5008 1714h       |
| EPWM1_G3      | 500C 1714h       |
| EPWM2_G0      | 5000 2714h       |
| EPWM2_G1      | 5004 2714h       |
| EPWM2_G2      | 5008 2714h       |
| EPWM2_G3      | 500C 2714h       |
| EPWM3_G0      | 5000 3714h       |
| EPWM3_G1      | 5004 3714h       |
| EPWM3_G2      | 5008 3714h       |
| EPWM3_G3      | 500C 3714h       |
| EPWM4_G0      | 5000 4714h       |
| EPWM4_G1      | 5004 4714h       |
| EPWM4_G2      | 5008 4714h       |
| EPWM4_G3      | 500C 4714h       |
| EPWM5_G0      | 5000 5714h       |
| EPWM5_G1      | 5004 5714h       |
| EPWM5_G2      | 5008 5714h       |
| EPWM5_G3      | 500C 5714h       |
| EPWM6_G0      | 5000 6714h       |
| EPWM6_G1      | 5004 6714h       |
| EPWM6_G2      | 5008 6714h       |
| EPWM6_G3      | 500C 6714h       |
| EPWM7_G0      | 5000 7714h       |
| EPWM7_G1      | 5004 7714h       |
| EPWM7_G2      | 5008 7714h       |
| EPWM7_G3      | 500C 7714h       |
| EPWM8_G0      | 5000 8714h       |
| EPWM8_G1      | 5004 8714h       |
| EPWM8_G2      | 5008 8714h       |
| EPWM8_G3      | 500C 8714h       |
| EPWM9_G0      | 5000 9714h       |
| EPWM9_G1      | 5004 9714h       |
| EPWM9_G2      | 5008 9714h       |

**Table 3-1222. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9714h       |
| EPWM10_G0     | 5000 A714h       |
| EPWM10_G1     | 5004 A714h       |
| EPWM10_G2     | 5008 A714h       |
| EPWM10_G3     | 500C A714h       |
| EPWM11_G0     | 5000 B714h       |
| EPWM11_G1     | 5004 B714h       |
| EPWM11_G2     | 5008 B714h       |
| EPWM11_G3     | 500C B714h       |
| EPWM12_G0     | 5000 C714h       |
| EPWM12_G1     | 5004 C714h       |
| EPWM12_G2     | 5008 C714h       |
| EPWM12_G3     | 500C C714h       |
| EPWM13_G0     | 5000 D714h       |
| EPWM13_G1     | 5004 D714h       |
| EPWM13_G2     | 5008 D714h       |
| EPWM13_G3     | 500C D714h       |
| EPWM14_G0     | 5000 E714h       |
| EPWM14_G1     | 5004 E714h       |
| EPWM14_G2     | 5008 E714h       |
| EPWM14_G3     | 500C E714h       |
| EPWM15_G0     | 5000 F714h       |
| EPWM15_G1     | 5004 F714h       |
| EPWM15_G2     | 5008 F714h       |
| EPWM15_G3     | 500C F714h       |
| EPWM16_G0     | 5001 0714h       |
| EPWM16_G1     | 5005 0714h       |
| EPWM16_G2     | 5009 0714h       |
| EPWM16_G3     | 500D 0714h       |
| EPWM17_G0     | 5001 1714h       |
| EPWM17_G1     | 5005 1714h       |
| EPWM17_G2     | 5009 1714h       |
| EPWM17_G3     | 500D 1714h       |
| EPWM18_G0     | 5001 2714h       |
| EPWM18_G1     | 5005 2714h       |
| EPWM18_G2     | 5009 2714h       |
| EPWM18_G3     | 500D 2714h       |
| EPWM19_G0     | 5001 3714h       |
| EPWM19_G1     | 5005 3714h       |
| EPWM19_G2     | 5009 3714h       |
| EPWM19_G3     | 500D 3714h       |
| EPWM20_G0     | 5001 4714h       |
| EPWM20_G1     | 5005 4714h       |
| EPWM20_G2     | 5009 4714h       |
| EPWM20_G3     | 500D 4714h       |



**Table 3-1222. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5714h       |
| EPWM21_G1     | 5005 5714h       |
| EPWM21_G2     | 5009 5714h       |
| EPWM21_G3     | 500D 5714h       |
| EPWM22_G0     | 5001 6714h       |
| EPWM22_G1     | 5005 6714h       |
| EPWM22_G2     | 5009 6714h       |
| EPWM22_G3     | 500D 6714h       |
| EPWM23_G0     | 5001 7714h       |
| EPWM23_G1     | 5005 7714h       |
| EPWM23_G2     | 5009 7714h       |
| EPWM23_G3     | 500D 7714h       |
| EPWM24_G0     | 5001 8714h       |
| EPWM24_G1     | 5005 8714h       |
| EPWM24_G2     | 5009 8714h       |
| EPWM24_G3     | 500D 8714h       |
| EPWM25_G0     | 5001 9714h       |
| EPWM25_G1     | 5005 9714h       |
| EPWM25_G2     | 5009 9714h       |
| EPWM25_G3     | 500D 9714h       |
| EPWM26_G0     | 5001 A714h       |
| EPWM26_G1     | 5005 A714h       |
| EPWM26_G2     | 5009 A714h       |
| EPWM26_G3     | 500D A714h       |
| EPWM27_G0     | 5001 B714h       |
| EPWM27_G1     | 5005 B714h       |
| EPWM27_G2     | 5009 B714h       |
| EPWM27_G3     | 500D B714h       |
| EPWM28_G0     | 5001 C714h       |
| EPWM28_G1     | 5005 C714h       |
| EPWM28_G2     | 5009 C714h       |
| EPWM28_G3     | 500D C714h       |
| EPWM29_G0     | 5001 D714h       |
| EPWM29_G1     | 5005 D714h       |
| EPWM29_G2     | 5009 D714h       |
| EPWM29_G3     | 500D D714h       |
| EPWM30_G0     | 5001 E714h       |
| EPWM30_G1     | 5005 E714h       |
| EPWM30_G2     | 5009 E714h       |
| EPWM30_G3     | 500D E714h       |
| EPWM31_G0     | 5001 F714h       |
| EPWM31_G1     | 5005 F714h       |
| EPWM31_G2     | 5009 F714h       |
| EPWM31_G3     | 500D F714h       |

**Figure 3-388. EPWM\_XCMP6\_SHDW2 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP6_SHDW2   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP6_SHDW2   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP6HR_SHDW2 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP6HR_SHDW2 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 3-1224. EPWM\_XCMP6\_SHDW2 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                 |
|-------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP6_SHDW2   | R/W  | 0h    | XCMP6_SHDW2 Register<br>The value in the XCMP6_SHDW2 register is loaded into XCMP6_ACTIVE register when shadow to active load occurs.       |
| 15:0  | XCMP6HR_SHDW2 | R/W  | 0h    | XCMP6HR_SHDW2 Register<br>The value in the XCMP6HR_SHDW2 register is loaded into XCMP6HR_ACTIVE register when shadow to active load occurs. |

### 3.7.2.138 EPWM\_XCMP7\_SHDW2 Register

#### 1 EPWM\_XCMP7\_SHDW2 Register (Offset = 718h) [reset = 0h]

Additional Compare 7 Shadow 2 Register.

Return to [Summary Table](#)

**Table 3-1225. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0718h       |
| EPWM0_G1      | 5004 0718h       |
| EPWM0_G2      | 5008 0718h       |
| EPWM0_G3      | 500C 0718h       |
| EPWM1_G0      | 5000 1718h       |
| EPWM1_G1      | 5004 1718h       |
| EPWM1_G2      | 5008 1718h       |
| EPWM1_G3      | 500C 1718h       |
| EPWM2_G0      | 5000 2718h       |
| EPWM2_G1      | 5004 2718h       |
| EPWM2_G2      | 5008 2718h       |
| EPWM2_G3      | 500C 2718h       |
| EPWM3_G0      | 5000 3718h       |
| EPWM3_G1      | 5004 3718h       |
| EPWM3_G2      | 5008 3718h       |
| EPWM3_G3      | 500C 3718h       |
| EPWM4_G0      | 5000 4718h       |
| EPWM4_G1      | 5004 4718h       |
| EPWM4_G2      | 5008 4718h       |
| EPWM4_G3      | 500C 4718h       |
| EPWM5_G0      | 5000 5718h       |
| EPWM5_G1      | 5004 5718h       |
| EPWM5_G2      | 5008 5718h       |
| EPWM5_G3      | 500C 5718h       |
| EPWM6_G0      | 5000 6718h       |
| EPWM6_G1      | 5004 6718h       |
| EPWM6_G2      | 5008 6718h       |
| EPWM6_G3      | 500C 6718h       |
| EPWM7_G0      | 5000 7718h       |
| EPWM7_G1      | 5004 7718h       |
| EPWM7_G2      | 5008 7718h       |
| EPWM7_G3      | 500C 7718h       |
| EPWM8_G0      | 5000 8718h       |
| EPWM8_G1      | 5004 8718h       |
| EPWM8_G2      | 5008 8718h       |
| EPWM8_G3      | 500C 8718h       |
| EPWM9_G0      | 5000 9718h       |
| EPWM9_G1      | 5004 9718h       |
| EPWM9_G2      | 5008 9718h       |

**Table 3-1225. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9718h       |
| EPWM10_G0     | 5000 A718h       |
| EPWM10_G1     | 5004 A718h       |
| EPWM10_G2     | 5008 A718h       |
| EPWM10_G3     | 500C A718h       |
| EPWM11_G0     | 5000 B718h       |
| EPWM11_G1     | 5004 B718h       |
| EPWM11_G2     | 5008 B718h       |
| EPWM11_G3     | 500C B718h       |
| EPWM12_G0     | 5000 C718h       |
| EPWM12_G1     | 5004 C718h       |
| EPWM12_G2     | 5008 C718h       |
| EPWM12_G3     | 500C C718h       |
| EPWM13_G0     | 5000 D718h       |
| EPWM13_G1     | 5004 D718h       |
| EPWM13_G2     | 5008 D718h       |
| EPWM13_G3     | 500C D718h       |
| EPWM14_G0     | 5000 E718h       |
| EPWM14_G1     | 5004 E718h       |
| EPWM14_G2     | 5008 E718h       |
| EPWM14_G3     | 500C E718h       |
| EPWM15_G0     | 5000 F718h       |
| EPWM15_G1     | 5004 F718h       |
| EPWM15_G2     | 5008 F718h       |
| EPWM15_G3     | 500C F718h       |
| EPWM16_G0     | 5001 0718h       |
| EPWM16_G1     | 5005 0718h       |
| EPWM16_G2     | 5009 0718h       |
| EPWM16_G3     | 500D 0718h       |
| EPWM17_G0     | 5001 1718h       |
| EPWM17_G1     | 5005 1718h       |
| EPWM17_G2     | 5009 1718h       |
| EPWM17_G3     | 500D 1718h       |
| EPWM18_G0     | 5001 2718h       |
| EPWM18_G1     | 5005 2718h       |
| EPWM18_G2     | 5009 2718h       |
| EPWM18_G3     | 500D 2718h       |
| EPWM19_G0     | 5001 3718h       |
| EPWM19_G1     | 5005 3718h       |
| EPWM19_G2     | 5009 3718h       |
| EPWM19_G3     | 500D 3718h       |
| EPWM20_G0     | 5001 4718h       |
| EPWM20_G1     | 5005 4718h       |
| EPWM20_G2     | 5009 4718h       |
| EPWM20_G3     | 500D 4718h       |

**Table 3-1225. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5718h       |
| EPWM21_G1     | 5005 5718h       |
| EPWM21_G2     | 5009 5718h       |
| EPWM21_G3     | 500D 5718h       |
| EPWM22_G0     | 5001 6718h       |
| EPWM22_G1     | 5005 6718h       |
| EPWM22_G2     | 5009 6718h       |
| EPWM22_G3     | 500D 6718h       |
| EPWM23_G0     | 5001 7718h       |
| EPWM23_G1     | 5005 7718h       |
| EPWM23_G2     | 5009 7718h       |
| EPWM23_G3     | 500D 7718h       |
| EPWM24_G0     | 5001 8718h       |
| EPWM24_G1     | 5005 8718h       |
| EPWM24_G2     | 5009 8718h       |
| EPWM24_G3     | 500D 8718h       |
| EPWM25_G0     | 5001 9718h       |
| EPWM25_G1     | 5005 9718h       |
| EPWM25_G2     | 5009 9718h       |
| EPWM25_G3     | 500D 9718h       |
| EPWM26_G0     | 5001 A718h       |
| EPWM26_G1     | 5005 A718h       |
| EPWM26_G2     | 5009 A718h       |
| EPWM26_G3     | 500D A718h       |
| EPWM27_G0     | 5001 B718h       |
| EPWM27_G1     | 5005 B718h       |
| EPWM27_G2     | 5009 B718h       |
| EPWM27_G3     | 500D B718h       |
| EPWM28_G0     | 5001 C718h       |
| EPWM28_G1     | 5005 C718h       |
| EPWM28_G2     | 5009 C718h       |
| EPWM28_G3     | 500D C718h       |
| EPWM29_G0     | 5001 D718h       |
| EPWM29_G1     | 5005 D718h       |
| EPWM29_G2     | 5009 D718h       |
| EPWM29_G3     | 500D D718h       |
| EPWM30_G0     | 5001 E718h       |
| EPWM30_G1     | 5005 E718h       |
| EPWM30_G2     | 5009 E718h       |
| EPWM30_G3     | 500D E718h       |
| EPWM31_G0     | 5001 F718h       |
| EPWM31_G1     | 5005 F718h       |
| EPWM31_G2     | 5009 F718h       |
| EPWM31_G3     | 500D F718h       |

**Figure 3-389. EPWM\_XCMP7\_SHDW2 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP7_SHDW2   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP7_SHDW2   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP7HR_SHDW2 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP7HR_SHDW2 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 3-1227. EPWM\_XCMP7\_SHDW2 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                 |
|-------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP7_SHDW2   | R/W  | 0h    | XCMP7_SHDW2 Register<br>The value in the XCMP7_SHDW2 register is loaded into XCMP7_ACTIVE register when shadow to active load occurs.       |
| 15:0  | XCMP7HR_SHDW2 | R/W  | 0h    | XCMP7HR_SHDW2 Register<br>The value in the XCMP7HR_SHDW2 register is loaded into XCMP7HR_ACTIVE register when shadow to active load occurs. |

### 3.7.2.139 EPWM\_XCMP8\_SHDW2 Register

#### 1 EPWM\_XCMP8\_SHDW2 Register (Offset = 71Ch) [reset = 0h]

Additional Compare 8 Shadow 2 Register.

Return to [Summary Table](#)

**Table 3-1228. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 071Ch       |
| EPWM0_G1      | 5004 071Ch       |
| EPWM0_G2      | 5008 071Ch       |
| EPWM0_G3      | 500C 071Ch       |
| EPWM1_G0      | 5000 171Ch       |
| EPWM1_G1      | 5004 171Ch       |
| EPWM1_G2      | 5008 171Ch       |
| EPWM1_G3      | 500C 171Ch       |
| EPWM2_G0      | 5000 271Ch       |
| EPWM2_G1      | 5004 271Ch       |
| EPWM2_G2      | 5008 271Ch       |
| EPWM2_G3      | 500C 271Ch       |
| EPWM3_G0      | 5000 371Ch       |
| EPWM3_G1      | 5004 371Ch       |
| EPWM3_G2      | 5008 371Ch       |
| EPWM3_G3      | 500C 371Ch       |
| EPWM4_G0      | 5000 471Ch       |
| EPWM4_G1      | 5004 471Ch       |
| EPWM4_G2      | 5008 471Ch       |
| EPWM4_G3      | 500C 471Ch       |
| EPWM5_G0      | 5000 571Ch       |
| EPWM5_G1      | 5004 571Ch       |
| EPWM5_G2      | 5008 571Ch       |
| EPWM5_G3      | 500C 571Ch       |
| EPWM6_G0      | 5000 671Ch       |
| EPWM6_G1      | 5004 671Ch       |
| EPWM6_G2      | 5008 671Ch       |
| EPWM6_G3      | 500C 671Ch       |
| EPWM7_G0      | 5000 771Ch       |
| EPWM7_G1      | 5004 771Ch       |
| EPWM7_G2      | 5008 771Ch       |
| EPWM7_G3      | 500C 771Ch       |
| EPWM8_G0      | 5000 871Ch       |
| EPWM8_G1      | 5004 871Ch       |
| EPWM8_G2      | 5008 871Ch       |
| EPWM8_G3      | 500C 871Ch       |
| EPWM9_G0      | 5000 971Ch       |
| EPWM9_G1      | 5004 971Ch       |
| EPWM9_G2      | 5008 971Ch       |

**Table 3-1228. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 971Ch       |
| EPWM10_G0     | 5000 A71Ch       |
| EPWM10_G1     | 5004 A71Ch       |
| EPWM10_G2     | 5008 A71Ch       |
| EPWM10_G3     | 500C A71Ch       |
| EPWM11_G0     | 5000 B71Ch       |
| EPWM11_G1     | 5004 B71Ch       |
| EPWM11_G2     | 5008 B71Ch       |
| EPWM11_G3     | 500C B71Ch       |
| EPWM12_G0     | 5000 C71Ch       |
| EPWM12_G1     | 5004 C71Ch       |
| EPWM12_G2     | 5008 C71Ch       |
| EPWM12_G3     | 500C C71Ch       |
| EPWM13_G0     | 5000 D71Ch       |
| EPWM13_G1     | 5004 D71Ch       |
| EPWM13_G2     | 5008 D71Ch       |
| EPWM13_G3     | 500C D71Ch       |
| EPWM14_G0     | 5000 E71Ch       |
| EPWM14_G1     | 5004 E71Ch       |
| EPWM14_G2     | 5008 E71Ch       |
| EPWM14_G3     | 500C E71Ch       |
| EPWM15_G0     | 5000 F71Ch       |
| EPWM15_G1     | 5004 F71Ch       |
| EPWM15_G2     | 5008 F71Ch       |
| EPWM15_G3     | 500C F71Ch       |
| EPWM16_G0     | 5001 071Ch       |
| EPWM16_G1     | 5005 071Ch       |
| EPWM16_G2     | 5009 071Ch       |
| EPWM16_G3     | 500D 071Ch       |
| EPWM17_G0     | 5001 171Ch       |
| EPWM17_G1     | 5005 171Ch       |
| EPWM17_G2     | 5009 171Ch       |
| EPWM17_G3     | 500D 171Ch       |
| EPWM18_G0     | 5001 271Ch       |
| EPWM18_G1     | 5005 271Ch       |
| EPWM18_G2     | 5009 271Ch       |
| EPWM18_G3     | 500D 271Ch       |
| EPWM19_G0     | 5001 371Ch       |
| EPWM19_G1     | 5005 371Ch       |
| EPWM19_G2     | 5009 371Ch       |
| EPWM19_G3     | 500D 371Ch       |
| EPWM20_G0     | 5001 471Ch       |
| EPWM20_G1     | 5005 471Ch       |
| EPWM20_G2     | 5009 471Ch       |
| EPWM20_G3     | 500D 471Ch       |



**Table 3-1228. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 571Ch       |
| EPWM21_G1     | 5005 571Ch       |
| EPWM21_G2     | 5009 571Ch       |
| EPWM21_G3     | 500D 571Ch       |
| EPWM22_G0     | 5001 671Ch       |
| EPWM22_G1     | 5005 671Ch       |
| EPWM22_G2     | 5009 671Ch       |
| EPWM22_G3     | 500D 671Ch       |
| EPWM23_G0     | 5001 771Ch       |
| EPWM23_G1     | 5005 771Ch       |
| EPWM23_G2     | 5009 771Ch       |
| EPWM23_G3     | 500D 771Ch       |
| EPWM24_G0     | 5001 871Ch       |
| EPWM24_G1     | 5005 871Ch       |
| EPWM24_G2     | 5009 871Ch       |
| EPWM24_G3     | 500D 871Ch       |
| EPWM25_G0     | 5001 971Ch       |
| EPWM25_G1     | 5005 971Ch       |
| EPWM25_G2     | 5009 971Ch       |
| EPWM25_G3     | 500D 971Ch       |
| EPWM26_G0     | 5001 A71Ch       |
| EPWM26_G1     | 5005 A71Ch       |
| EPWM26_G2     | 5009 A71Ch       |
| EPWM26_G3     | 500D A71Ch       |
| EPWM27_G0     | 5001 B71Ch       |
| EPWM27_G1     | 5005 B71Ch       |
| EPWM27_G2     | 5009 B71Ch       |
| EPWM27_G3     | 500D B71Ch       |
| EPWM28_G0     | 5001 C71Ch       |
| EPWM28_G1     | 5005 C71Ch       |
| EPWM28_G2     | 5009 C71Ch       |
| EPWM28_G3     | 500D C71Ch       |
| EPWM29_G0     | 5001 D71Ch       |
| EPWM29_G1     | 5005 D71Ch       |
| EPWM29_G2     | 5009 D71Ch       |
| EPWM29_G3     | 500D D71Ch       |
| EPWM30_G0     | 5001 E71Ch       |
| EPWM30_G1     | 5005 E71Ch       |
| EPWM30_G2     | 5009 E71Ch       |
| EPWM30_G3     | 500D E71Ch       |
| EPWM31_G0     | 5001 F71Ch       |
| EPWM31_G1     | 5005 F71Ch       |
| EPWM31_G2     | 5009 F71Ch       |
| EPWM31_G3     | 500D F71Ch       |

**Figure 3-390. EPWM\_XCMP8\_SHDW2 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP8_SHDW2   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP8_SHDW2   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP8HR_SHDW2 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP8HR_SHDW2 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 3-1230. EPWM\_XCMP8\_SHDW2 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                 |
|-------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP8_SHDW2   | R/W  | 0h    | XCMP8_SHDW2 Register<br>The value in the XCMP8_SHDW2 register is loaded into XCMP8_ACTIVE register when shadow to active load occurs.       |
| 15:0  | XCMP8HR_SHDW2 | R/W  | 0h    | XCMP8HR_SHDW2 Register<br>The value in the XCMP8HR_SHDW2 register is loaded into XCMP8HR_ACTIVE register when shadow to active load occurs. |

### 3.7.2.140 EPWM\_XTBPRD\_SHDW2 Register

#### 1 EPWM\_XTBPRD\_SHDW2 Register (Offset = 720h) [reset = 0h]

Additional Time Base Period Shadow 2 Register.

Return to [Summary Table](#)

**Table 3-1231. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0720h       |
| EPWM0_G1      | 5004 0720h       |
| EPWM0_G2      | 5008 0720h       |
| EPWM0_G3      | 500C 0720h       |
| EPWM1_G0      | 5000 1720h       |
| EPWM1_G1      | 5004 1720h       |
| EPWM1_G2      | 5008 1720h       |
| EPWM1_G3      | 500C 1720h       |
| EPWM2_G0      | 5000 2720h       |
| EPWM2_G1      | 5004 2720h       |
| EPWM2_G2      | 5008 2720h       |
| EPWM2_G3      | 500C 2720h       |
| EPWM3_G0      | 5000 3720h       |
| EPWM3_G1      | 5004 3720h       |
| EPWM3_G2      | 5008 3720h       |
| EPWM3_G3      | 500C 3720h       |
| EPWM4_G0      | 5000 4720h       |
| EPWM4_G1      | 5004 4720h       |
| EPWM4_G2      | 5008 4720h       |
| EPWM4_G3      | 500C 4720h       |
| EPWM5_G0      | 5000 5720h       |
| EPWM5_G1      | 5004 5720h       |
| EPWM5_G2      | 5008 5720h       |
| EPWM5_G3      | 500C 5720h       |
| EPWM6_G0      | 5000 6720h       |
| EPWM6_G1      | 5004 6720h       |
| EPWM6_G2      | 5008 6720h       |
| EPWM6_G3      | 500C 6720h       |
| EPWM7_G0      | 5000 7720h       |
| EPWM7_G1      | 5004 7720h       |
| EPWM7_G2      | 5008 7720h       |
| EPWM7_G3      | 500C 7720h       |
| EPWM8_G0      | 5000 8720h       |
| EPWM8_G1      | 5004 8720h       |
| EPWM8_G2      | 5008 8720h       |
| EPWM8_G3      | 500C 8720h       |
| EPWM9_G0      | 5000 9720h       |
| EPWM9_G1      | 5004 9720h       |
| EPWM9_G2      | 5008 9720h       |

**Table 3-1231. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9720h       |
| EPWM10_G0     | 5000 A720h       |
| EPWM10_G1     | 5004 A720h       |
| EPWM10_G2     | 5008 A720h       |
| EPWM10_G3     | 500C A720h       |
| EPWM11_G0     | 5000 B720h       |
| EPWM11_G1     | 5004 B720h       |
| EPWM11_G2     | 5008 B720h       |
| EPWM11_G3     | 500C B720h       |
| EPWM12_G0     | 5000 C720h       |
| EPWM12_G1     | 5004 C720h       |
| EPWM12_G2     | 5008 C720h       |
| EPWM12_G3     | 500C C720h       |
| EPWM13_G0     | 5000 D720h       |
| EPWM13_G1     | 5004 D720h       |
| EPWM13_G2     | 5008 D720h       |
| EPWM13_G3     | 500C D720h       |
| EPWM14_G0     | 5000 E720h       |
| EPWM14_G1     | 5004 E720h       |
| EPWM14_G2     | 5008 E720h       |
| EPWM14_G3     | 500C E720h       |
| EPWM15_G0     | 5000 F720h       |
| EPWM15_G1     | 5004 F720h       |
| EPWM15_G2     | 5008 F720h       |
| EPWM15_G3     | 500C F720h       |
| EPWM16_G0     | 5001 0720h       |
| EPWM16_G1     | 5005 0720h       |
| EPWM16_G2     | 5009 0720h       |
| EPWM16_G3     | 500D 0720h       |
| EPWM17_G0     | 5001 1720h       |
| EPWM17_G1     | 5005 1720h       |
| EPWM17_G2     | 5009 1720h       |
| EPWM17_G3     | 500D 1720h       |
| EPWM18_G0     | 5001 2720h       |
| EPWM18_G1     | 5005 2720h       |
| EPWM18_G2     | 5009 2720h       |
| EPWM18_G3     | 500D 2720h       |
| EPWM19_G0     | 5001 3720h       |
| EPWM19_G1     | 5005 3720h       |
| EPWM19_G2     | 5009 3720h       |
| EPWM19_G3     | 500D 3720h       |
| EPWM20_G0     | 5001 4720h       |
| EPWM20_G1     | 5005 4720h       |
| EPWM20_G2     | 5009 4720h       |
| EPWM20_G3     | 500D 4720h       |

**Table 3-1231. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5720h       |
| EPWM21_G1     | 5005 5720h       |
| EPWM21_G2     | 5009 5720h       |
| EPWM21_G3     | 500D 5720h       |
| EPWM22_G0     | 5001 6720h       |
| EPWM22_G1     | 5005 6720h       |
| EPWM22_G2     | 5009 6720h       |
| EPWM22_G3     | 500D 6720h       |
| EPWM23_G0     | 5001 7720h       |
| EPWM23_G1     | 5005 7720h       |
| EPWM23_G2     | 5009 7720h       |
| EPWM23_G3     | 500D 7720h       |
| EPWM24_G0     | 5001 8720h       |
| EPWM24_G1     | 5005 8720h       |
| EPWM24_G2     | 5009 8720h       |
| EPWM24_G3     | 500D 8720h       |
| EPWM25_G0     | 5001 9720h       |
| EPWM25_G1     | 5005 9720h       |
| EPWM25_G2     | 5009 9720h       |
| EPWM25_G3     | 500D 9720h       |
| EPWM26_G0     | 5001 A720h       |
| EPWM26_G1     | 5005 A720h       |
| EPWM26_G2     | 5009 A720h       |
| EPWM26_G3     | 500D A720h       |
| EPWM27_G0     | 5001 B720h       |
| EPWM27_G1     | 5005 B720h       |
| EPWM27_G2     | 5009 B720h       |
| EPWM27_G3     | 500D B720h       |
| EPWM28_G0     | 5001 C720h       |
| EPWM28_G1     | 5005 C720h       |
| EPWM28_G2     | 5009 C720h       |
| EPWM28_G3     | 500D C720h       |
| EPWM29_G0     | 5001 D720h       |
| EPWM29_G1     | 5005 D720h       |
| EPWM29_G2     | 5009 D720h       |
| EPWM29_G3     | 500D D720h       |
| EPWM30_G0     | 5001 E720h       |
| EPWM30_G1     | 5005 E720h       |
| EPWM30_G2     | 5009 E720h       |
| EPWM30_G3     | 500D E720h       |
| EPWM31_G0     | 5001 F720h       |
| EPWM31_G1     | 5005 F720h       |
| EPWM31_G2     | 5009 F720h       |
| EPWM31_G3     | 500D F720h       |

**Figure 3-391. EPWM\_XTBPRD\_SHDW2 Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XTBPRD_SHDW2   |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XTBPRD_SHDW2   |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XTBPRDHR_SHDW2 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XTBPRDHR_SHDW2 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 3-1233. EPWM\_XTBPRD\_SHDW2 Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                         |
|-------|----------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:16 | XTBPRD_SHDW2   | R/W  | 0h    | The value in the XTBPRD_SHDW2 register is loaded into XTBPRD_ACTIVE register when shadow to active load occurs.     |
| 15:0  | XTBPRDHR_SHDW2 | R/W  | 0h    | The value in the XTBPRDHR_SHDW2 register is loaded into XTBPRDHR_ACTIVE register when shadow to active load occurs. |

### 3.7.2.141 EPWM\_XAQCTLA\_SHDW2 Register

#### 1 EPWM\_XAQCTLA\_SHDW2 Register (Offset = 730h) [reset = 0h]

XAQCTLA Shadow 2 Register.

Return to [Summary Table](#)

**Table 3-1234. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0730h       |
| EPWM0_G1      | 5004 0730h       |
| EPWM0_G2      | 5008 0730h       |
| EPWM0_G3      | 500C 0730h       |
| EPWM1_G0      | 5000 1730h       |
| EPWM1_G1      | 5004 1730h       |
| EPWM1_G2      | 5008 1730h       |
| EPWM1_G3      | 500C 1730h       |
| EPWM2_G0      | 5000 2730h       |
| EPWM2_G1      | 5004 2730h       |
| EPWM2_G2      | 5008 2730h       |
| EPWM2_G3      | 500C 2730h       |
| EPWM3_G0      | 5000 3730h       |
| EPWM3_G1      | 5004 3730h       |
| EPWM3_G2      | 5008 3730h       |
| EPWM3_G3      | 500C 3730h       |
| EPWM4_G0      | 5000 4730h       |
| EPWM4_G1      | 5004 4730h       |
| EPWM4_G2      | 5008 4730h       |
| EPWM4_G3      | 500C 4730h       |
| EPWM5_G0      | 5000 5730h       |
| EPWM5_G1      | 5004 5730h       |
| EPWM5_G2      | 5008 5730h       |
| EPWM5_G3      | 500C 5730h       |
| EPWM6_G0      | 5000 6730h       |
| EPWM6_G1      | 5004 6730h       |
| EPWM6_G2      | 5008 6730h       |
| EPWM6_G3      | 500C 6730h       |
| EPWM7_G0      | 5000 7730h       |
| EPWM7_G1      | 5004 7730h       |
| EPWM7_G2      | 5008 7730h       |
| EPWM7_G3      | 500C 7730h       |
| EPWM8_G0      | 5000 8730h       |
| EPWM8_G1      | 5004 8730h       |
| EPWM8_G2      | 5008 8730h       |
| EPWM8_G3      | 500C 8730h       |
| EPWM9_G0      | 5000 9730h       |
| EPWM9_G1      | 5004 9730h       |
| EPWM9_G2      | 5008 9730h       |

**Table 3-1234. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9730h       |
| EPWM10_G0     | 5000 A730h       |
| EPWM10_G1     | 5004 A730h       |
| EPWM10_G2     | 5008 A730h       |
| EPWM10_G3     | 500C A730h       |
| EPWM11_G0     | 5000 B730h       |
| EPWM11_G1     | 5004 B730h       |
| EPWM11_G2     | 5008 B730h       |
| EPWM11_G3     | 500C B730h       |
| EPWM12_G0     | 5000 C730h       |
| EPWM12_G1     | 5004 C730h       |
| EPWM12_G2     | 5008 C730h       |
| EPWM12_G3     | 500C C730h       |
| EPWM13_G0     | 5000 D730h       |
| EPWM13_G1     | 5004 D730h       |
| EPWM13_G2     | 5008 D730h       |
| EPWM13_G3     | 500C D730h       |
| EPWM14_G0     | 5000 E730h       |
| EPWM14_G1     | 5004 E730h       |
| EPWM14_G2     | 5008 E730h       |
| EPWM14_G3     | 500C E730h       |
| EPWM15_G0     | 5000 F730h       |
| EPWM15_G1     | 5004 F730h       |
| EPWM15_G2     | 5008 F730h       |
| EPWM15_G3     | 500C F730h       |
| EPWM16_G0     | 5001 0730h       |
| EPWM16_G1     | 5005 0730h       |
| EPWM16_G2     | 5009 0730h       |
| EPWM16_G3     | 500D 0730h       |
| EPWM17_G0     | 5001 1730h       |
| EPWM17_G1     | 5005 1730h       |
| EPWM17_G2     | 5009 1730h       |
| EPWM17_G3     | 500D 1730h       |
| EPWM18_G0     | 5001 2730h       |
| EPWM18_G1     | 5005 2730h       |
| EPWM18_G2     | 5009 2730h       |
| EPWM18_G3     | 500D 2730h       |
| EPWM19_G0     | 5001 3730h       |
| EPWM19_G1     | 5005 3730h       |
| EPWM19_G2     | 5009 3730h       |
| EPWM19_G3     | 500D 3730h       |
| EPWM20_G0     | 5001 4730h       |
| EPWM20_G1     | 5005 4730h       |
| EPWM20_G2     | 5009 4730h       |
| EPWM20_G3     | 500D 4730h       |



**Table 3-1234. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5730h       |
| EPWM21_G1     | 5005 5730h       |
| EPWM21_G2     | 5009 5730h       |
| EPWM21_G3     | 500D 5730h       |
| EPWM22_G0     | 5001 6730h       |
| EPWM22_G1     | 5005 6730h       |
| EPWM22_G2     | 5009 6730h       |
| EPWM22_G3     | 500D 6730h       |
| EPWM23_G0     | 5001 7730h       |
| EPWM23_G1     | 5005 7730h       |
| EPWM23_G2     | 5009 7730h       |
| EPWM23_G3     | 500D 7730h       |
| EPWM24_G0     | 5001 8730h       |
| EPWM24_G1     | 5005 8730h       |
| EPWM24_G2     | 5009 8730h       |
| EPWM24_G3     | 500D 8730h       |
| EPWM25_G0     | 5001 9730h       |
| EPWM25_G1     | 5005 9730h       |
| EPWM25_G2     | 5009 9730h       |
| EPWM25_G3     | 500D 9730h       |
| EPWM26_G0     | 5001 A730h       |
| EPWM26_G1     | 5005 A730h       |
| EPWM26_G2     | 5009 A730h       |
| EPWM26_G3     | 500D A730h       |
| EPWM27_G0     | 5001 B730h       |
| EPWM27_G1     | 5005 B730h       |
| EPWM27_G2     | 5009 B730h       |
| EPWM27_G3     | 500D B730h       |
| EPWM28_G0     | 5001 C730h       |
| EPWM28_G1     | 5005 C730h       |
| EPWM28_G2     | 5009 C730h       |
| EPWM28_G3     | 500D C730h       |
| EPWM29_G0     | 5001 D730h       |
| EPWM29_G1     | 5005 D730h       |
| EPWM29_G2     | 5009 D730h       |
| EPWM29_G3     | 500D D730h       |
| EPWM30_G0     | 5001 E730h       |
| EPWM30_G1     | 5005 E730h       |
| EPWM30_G2     | 5009 E730h       |
| EPWM30_G3     | 500D E730h       |
| EPWM31_G0     | 5001 F730h       |
| EPWM31_G1     | 5005 F730h       |
| EPWM31_G2     | 5009 F730h       |
| EPWM31_G3     | 500D F730h       |

**Figure 3-392. EPWM\_XAQCTLA\_SHDW2 Name Register**

| 15    | 14 | 13    | 12 | 11    | 10 | 9     | 8 |
|-------|----|-------|----|-------|----|-------|---|
| XCMP8 |    | XCMP7 |    | XCMP6 |    | XCMP5 |   |
| R/W   |    | R/W   |    | R/W   |    | R/W   |   |
| 0h    |    | 0h    |    | 0h    |    | 0h    |   |
| 7     | 6  | 5     | 4  | 3     | 2  | 1     | 0 |
| XCMP4 |    | XCMP3 |    | XCMP2 |    | XCMP1 |   |
| R/W   |    | R/W   |    | R/W   |    | R/W   |   |
| 0h    |    | 0h    |    | 0h    |    | 0h    |   |

**Table 3-1236. EPWM\_XAQCTLA\_SHDW2 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                          |
|-------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | XCMP8 | R/W  | 0h    | Action when Counter = CMP8<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 13:12 | XCMP7 | R/W  | 0h    | Action when Counter = CMP7<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 11:10 | XCMP6 | R/W  | 0h    | Action when Counter = CMP6<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 9:8   | XCMP5 | R/W  | 0h    | Action when Counter = CMP5<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 7:6   | XCMP4 | R/W  | 0h    | Action when Counter = CMP4<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 5:4   | XCMP3 | R/W  | 0h    | Action when Counter = CMP3<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 3:2   | XCMP2 | R/W  | 0h    | Action when Counter = CMP2<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 1:0   | XCMP1 | R/W  | 0h    | Action when Counter = CMP1<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |

### 3.7.2.142 EPWM\_XAQCTLB\_SHDW2 Register

#### 1 EPWM\_XAQCTLB\_SHDW2 Register (Offset = 732h) [reset = 0h]

XAQCTLB Shadow 2 Register.

Return to [Summary Table](#)

**Table 3-1237. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0732h       |
| EPWM0_G1      | 5004 0732h       |
| EPWM0_G2      | 5008 0732h       |
| EPWM0_G3      | 500C 0732h       |
| EPWM1_G0      | 5000 1732h       |
| EPWM1_G1      | 5004 1732h       |
| EPWM1_G2      | 5008 1732h       |
| EPWM1_G3      | 500C 1732h       |
| EPWM2_G0      | 5000 2732h       |
| EPWM2_G1      | 5004 2732h       |
| EPWM2_G2      | 5008 2732h       |
| EPWM2_G3      | 500C 2732h       |
| EPWM3_G0      | 5000 3732h       |
| EPWM3_G1      | 5004 3732h       |
| EPWM3_G2      | 5008 3732h       |
| EPWM3_G3      | 500C 3732h       |
| EPWM4_G0      | 5000 4732h       |
| EPWM4_G1      | 5004 4732h       |
| EPWM4_G2      | 5008 4732h       |
| EPWM4_G3      | 500C 4732h       |
| EPWM5_G0      | 5000 5732h       |
| EPWM5_G1      | 5004 5732h       |
| EPWM5_G2      | 5008 5732h       |
| EPWM5_G3      | 500C 5732h       |
| EPWM6_G0      | 5000 6732h       |
| EPWM6_G1      | 5004 6732h       |
| EPWM6_G2      | 5008 6732h       |
| EPWM6_G3      | 500C 6732h       |
| EPWM7_G0      | 5000 7732h       |
| EPWM7_G1      | 5004 7732h       |
| EPWM7_G2      | 5008 7732h       |
| EPWM7_G3      | 500C 7732h       |
| EPWM8_G0      | 5000 8732h       |
| EPWM8_G1      | 5004 8732h       |
| EPWM8_G2      | 5008 8732h       |
| EPWM8_G3      | 500C 8732h       |
| EPWM9_G0      | 5000 9732h       |
| EPWM9_G1      | 5004 9732h       |
| EPWM9_G2      | 5008 9732h       |

**Table 3-1237. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9732h       |
| EPWM10_G0     | 5000 A732h       |
| EPWM10_G1     | 5004 A732h       |
| EPWM10_G2     | 5008 A732h       |
| EPWM10_G3     | 500C A732h       |
| EPWM11_G0     | 5000 B732h       |
| EPWM11_G1     | 5004 B732h       |
| EPWM11_G2     | 5008 B732h       |
| EPWM11_G3     | 500C B732h       |
| EPWM12_G0     | 5000 C732h       |
| EPWM12_G1     | 5004 C732h       |
| EPWM12_G2     | 5008 C732h       |
| EPWM12_G3     | 500C C732h       |
| EPWM13_G0     | 5000 D732h       |
| EPWM13_G1     | 5004 D732h       |
| EPWM13_G2     | 5008 D732h       |
| EPWM13_G3     | 500C D732h       |
| EPWM14_G0     | 5000 E732h       |
| EPWM14_G1     | 5004 E732h       |
| EPWM14_G2     | 5008 E732h       |
| EPWM14_G3     | 500C E732h       |
| EPWM15_G0     | 5000 F732h       |
| EPWM15_G1     | 5004 F732h       |
| EPWM15_G2     | 5008 F732h       |
| EPWM15_G3     | 500C F732h       |
| EPWM16_G0     | 5001 0732h       |
| EPWM16_G1     | 5005 0732h       |
| EPWM16_G2     | 5009 0732h       |
| EPWM16_G3     | 500D 0732h       |
| EPWM17_G0     | 5001 1732h       |
| EPWM17_G1     | 5005 1732h       |
| EPWM17_G2     | 5009 1732h       |
| EPWM17_G3     | 500D 1732h       |
| EPWM18_G0     | 5001 2732h       |
| EPWM18_G1     | 5005 2732h       |
| EPWM18_G2     | 5009 2732h       |
| EPWM18_G3     | 500D 2732h       |
| EPWM19_G0     | 5001 3732h       |
| EPWM19_G1     | 5005 3732h       |
| EPWM19_G2     | 5009 3732h       |
| EPWM19_G3     | 500D 3732h       |
| EPWM20_G0     | 5001 4732h       |
| EPWM20_G1     | 5005 4732h       |
| EPWM20_G2     | 5009 4732h       |
| EPWM20_G3     | 500D 4732h       |

**Table 3-1237. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5732h       |
| EPWM21_G1     | 5005 5732h       |
| EPWM21_G2     | 5009 5732h       |
| EPWM21_G3     | 500D 5732h       |
| EPWM22_G0     | 5001 6732h       |
| EPWM22_G1     | 5005 6732h       |
| EPWM22_G2     | 5009 6732h       |
| EPWM22_G3     | 500D 6732h       |
| EPWM23_G0     | 5001 7732h       |
| EPWM23_G1     | 5005 7732h       |
| EPWM23_G2     | 5009 7732h       |
| EPWM23_G3     | 500D 7732h       |
| EPWM24_G0     | 5001 8732h       |
| EPWM24_G1     | 5005 8732h       |
| EPWM24_G2     | 5009 8732h       |
| EPWM24_G3     | 500D 8732h       |
| EPWM25_G0     | 5001 9732h       |
| EPWM25_G1     | 5005 9732h       |
| EPWM25_G2     | 5009 9732h       |
| EPWM25_G3     | 500D 9732h       |
| EPWM26_G0     | 5001 A732h       |
| EPWM26_G1     | 5005 A732h       |
| EPWM26_G2     | 5009 A732h       |
| EPWM26_G3     | 500D A732h       |
| EPWM27_G0     | 5001 B732h       |
| EPWM27_G1     | 5005 B732h       |
| EPWM27_G2     | 5009 B732h       |
| EPWM27_G3     | 500D B732h       |
| EPWM28_G0     | 5001 C732h       |
| EPWM28_G1     | 5005 C732h       |
| EPWM28_G2     | 5009 C732h       |
| EPWM28_G3     | 500D C732h       |
| EPWM29_G0     | 5001 D732h       |
| EPWM29_G1     | 5005 D732h       |
| EPWM29_G2     | 5009 D732h       |
| EPWM29_G3     | 500D D732h       |
| EPWM30_G0     | 5001 E732h       |
| EPWM30_G1     | 5005 E732h       |
| EPWM30_G2     | 5009 E732h       |
| EPWM30_G3     | 500D E732h       |
| EPWM31_G0     | 5001 F732h       |
| EPWM31_G1     | 5005 F732h       |
| EPWM31_G2     | 5009 F732h       |
| EPWM31_G3     | 500D F732h       |

**Figure 3-393. EPWM\_XAQCTLB\_SHDW2 Name Register**

|            |    |       |    |       |    |       |   |
|------------|----|-------|----|-------|----|-------|---|
| 15         | 14 | 13    | 12 | 11    | 10 | 9     | 8 |
| XCMP8      |    | XCMP7 |    | XCMP6 |    | XCMP5 |   |
| R/W        |    | R/W   |    | R/W   |    | R/W   |   |
| 0h         |    | 0h    |    | 0h    |    | 0h    |   |
| 7          | 6  | 5     | 4  | 3     | 2  | 1     | 0 |
| RESERVED_1 |    |       |    |       |    |       |   |
| R          |    |       |    |       |    |       |   |
| 0h         |    |       |    |       |    |       |   |

**Table 3-1239. EPWM\_XAQCTLB\_SHDW2 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                          |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | XCMP8      | R/W  | 0h    | Action when Counter = CMP8<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 13:12 | XCMP7      | R/W  | 0h    | Action when Counter = CMP7<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 11:10 | XCMP6      | R/W  | 0h    | Action when Counter = CMP6<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 9:8   | XCMP5      | R/W  | 0h    | Action when Counter = CMP5<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 7:0   | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                             |

### 3.7.2.143 EPWM\_CMPC\_SHDW2 Register

#### 1 EPWM\_CMPC\_SHDW2 Register (Offset = 73Ah) [reset = 0h]

CMPC Shadow 2 Register.

Return to [Summary Table](#)

**Table 3-1240. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 073Ah       |
| EPWM0_G1      | 5004 073Ah       |
| EPWM0_G2      | 5008 073Ah       |
| EPWM0_G3      | 500C 073Ah       |
| EPWM1_G0      | 5000 173Ah       |
| EPWM1_G1      | 5004 173Ah       |
| EPWM1_G2      | 5008 173Ah       |
| EPWM1_G3      | 500C 173Ah       |
| EPWM2_G0      | 5000 273Ah       |
| EPWM2_G1      | 5004 273Ah       |
| EPWM2_G2      | 5008 273Ah       |
| EPWM2_G3      | 500C 273Ah       |
| EPWM3_G0      | 5000 373Ah       |
| EPWM3_G1      | 5004 373Ah       |
| EPWM3_G2      | 5008 373Ah       |
| EPWM3_G3      | 500C 373Ah       |
| EPWM4_G0      | 5000 473Ah       |
| EPWM4_G1      | 5004 473Ah       |
| EPWM4_G2      | 5008 473Ah       |
| EPWM4_G3      | 500C 473Ah       |
| EPWM5_G0      | 5000 573Ah       |
| EPWM5_G1      | 5004 573Ah       |
| EPWM5_G2      | 5008 573Ah       |
| EPWM5_G3      | 500C 573Ah       |
| EPWM6_G0      | 5000 673Ah       |
| EPWM6_G1      | 5004 673Ah       |
| EPWM6_G2      | 5008 673Ah       |
| EPWM6_G3      | 500C 673Ah       |
| EPWM7_G0      | 5000 773Ah       |
| EPWM7_G1      | 5004 773Ah       |
| EPWM7_G2      | 5008 773Ah       |
| EPWM7_G3      | 500C 773Ah       |
| EPWM8_G0      | 5000 873Ah       |
| EPWM8_G1      | 5004 873Ah       |
| EPWM8_G2      | 5008 873Ah       |
| EPWM8_G3      | 500C 873Ah       |
| EPWM9_G0      | 5000 973Ah       |
| EPWM9_G1      | 5004 973Ah       |
| EPWM9_G2      | 5008 973Ah       |

**Table 3-1240. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 973Ah       |
| EPWM10_G0     | 5000 A73Ah       |
| EPWM10_G1     | 5004 A73Ah       |
| EPWM10_G2     | 5008 A73Ah       |
| EPWM10_G3     | 500C A73Ah       |
| EPWM11_G0     | 5000 B73Ah       |
| EPWM11_G1     | 5004 B73Ah       |
| EPWM11_G2     | 5008 B73Ah       |
| EPWM11_G3     | 500C B73Ah       |
| EPWM12_G0     | 5000 C73Ah       |
| EPWM12_G1     | 5004 C73Ah       |
| EPWM12_G2     | 5008 C73Ah       |
| EPWM12_G3     | 500C C73Ah       |
| EPWM13_G0     | 5000 D73Ah       |
| EPWM13_G1     | 5004 D73Ah       |
| EPWM13_G2     | 5008 D73Ah       |
| EPWM13_G3     | 500C D73Ah       |
| EPWM14_G0     | 5000 E73Ah       |
| EPWM14_G1     | 5004 E73Ah       |
| EPWM14_G2     | 5008 E73Ah       |
| EPWM14_G3     | 500C E73Ah       |
| EPWM15_G0     | 5000 F73Ah       |
| EPWM15_G1     | 5004 F73Ah       |
| EPWM15_G2     | 5008 F73Ah       |
| EPWM15_G3     | 500C F73Ah       |
| EPWM16_G0     | 5001 073Ah       |
| EPWM16_G1     | 5005 073Ah       |
| EPWM16_G2     | 5009 073Ah       |
| EPWM16_G3     | 500D 073Ah       |
| EPWM17_G0     | 5001 173Ah       |
| EPWM17_G1     | 5005 173Ah       |
| EPWM17_G2     | 5009 173Ah       |
| EPWM17_G3     | 500D 173Ah       |
| EPWM18_G0     | 5001 273Ah       |
| EPWM18_G1     | 5005 273Ah       |
| EPWM18_G2     | 5009 273Ah       |
| EPWM18_G3     | 500D 273Ah       |
| EPWM19_G0     | 5001 373Ah       |
| EPWM19_G1     | 5005 373Ah       |
| EPWM19_G2     | 5009 373Ah       |
| EPWM19_G3     | 500D 373Ah       |
| EPWM20_G0     | 5001 473Ah       |
| EPWM20_G1     | 5005 473Ah       |
| EPWM20_G2     | 5009 473Ah       |
| EPWM20_G3     | 500D 473Ah       |



**Table 3-1240. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 573Ah       |
| EPWM21_G1     | 5005 573Ah       |
| EPWM21_G2     | 5009 573Ah       |
| EPWM21_G3     | 500D 573Ah       |
| EPWM22_G0     | 5001 673Ah       |
| EPWM22_G1     | 5005 673Ah       |
| EPWM22_G2     | 5009 673Ah       |
| EPWM22_G3     | 500D 673Ah       |
| EPWM23_G0     | 5001 773Ah       |
| EPWM23_G1     | 5005 773Ah       |
| EPWM23_G2     | 5009 773Ah       |
| EPWM23_G3     | 500D 773Ah       |
| EPWM24_G0     | 5001 873Ah       |
| EPWM24_G1     | 5005 873Ah       |
| EPWM24_G2     | 5009 873Ah       |
| EPWM24_G3     | 500D 873Ah       |
| EPWM25_G0     | 5001 973Ah       |
| EPWM25_G1     | 5005 973Ah       |
| EPWM25_G2     | 5009 973Ah       |
| EPWM25_G3     | 500D 973Ah       |
| EPWM26_G0     | 5001 A73Ah       |
| EPWM26_G1     | 5005 A73Ah       |
| EPWM26_G2     | 5009 A73Ah       |
| EPWM26_G3     | 500D A73Ah       |
| EPWM27_G0     | 5001 B73Ah       |
| EPWM27_G1     | 5005 B73Ah       |
| EPWM27_G2     | 5009 B73Ah       |
| EPWM27_G3     | 500D B73Ah       |
| EPWM28_G0     | 5001 C73Ah       |
| EPWM28_G1     | 5005 C73Ah       |
| EPWM28_G2     | 5009 C73Ah       |
| EPWM28_G3     | 500D C73Ah       |
| EPWM29_G0     | 5001 D73Ah       |
| EPWM29_G1     | 5005 D73Ah       |
| EPWM29_G2     | 5009 D73Ah       |
| EPWM29_G3     | 500D D73Ah       |
| EPWM30_G0     | 5001 E73Ah       |
| EPWM30_G1     | 5005 E73Ah       |
| EPWM30_G2     | 5009 E73Ah       |
| EPWM30_G3     | 500D E73Ah       |
| EPWM31_G0     | 5001 F73Ah       |
| EPWM31_G1     | 5005 F73Ah       |
| EPWM31_G2     | 5009 F73Ah       |
| EPWM31_G3     | 500D F73Ah       |

**Figure 3-394. EPWM\_CMPC\_SHDW2 Name Register**

|            |    |    |    |    |    |   |   |
|------------|----|----|----|----|----|---|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMPC_SHDW2 |    |    |    |    |    |   |   |
| R/W        |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| CMPC_SHDW2 |    |    |    |    |    |   |   |
| R/W        |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |

**Table 3-1242. EPWM\_CMPC\_SHDW2 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                 |
|------|------------|------|-------|-------------------------------------------------------------------------------------------------------------|
| 15:0 | CMPC_SHDW2 | R/W  | 0h    | The value in the CMPC_SHDW2 register is loaded into CMPC_ACTIVE register when shadow to active load occurs. |

### 3.7.2.144 EPWM\_CMPD\_SHDW2 Register

#### 1 EPWM\_CMPD\_SHDW2 Register (Offset = 73Eh) [reset = 0h]

CMPD Shadow 2 Register.

Return to [Summary Table](#)

**Table 3-1243. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 073Eh       |
| EPWM0_G1      | 5004 073Eh       |
| EPWM0_G2      | 5008 073Eh       |
| EPWM0_G3      | 500C 073Eh       |
| EPWM1_G0      | 5000 173Eh       |
| EPWM1_G1      | 5004 173Eh       |
| EPWM1_G2      | 5008 173Eh       |
| EPWM1_G3      | 500C 173Eh       |
| EPWM2_G0      | 5000 273Eh       |
| EPWM2_G1      | 5004 273Eh       |
| EPWM2_G2      | 5008 273Eh       |
| EPWM2_G3      | 500C 273Eh       |
| EPWM3_G0      | 5000 373Eh       |
| EPWM3_G1      | 5004 373Eh       |
| EPWM3_G2      | 5008 373Eh       |
| EPWM3_G3      | 500C 373Eh       |
| EPWM4_G0      | 5000 473Eh       |
| EPWM4_G1      | 5004 473Eh       |
| EPWM4_G2      | 5008 473Eh       |
| EPWM4_G3      | 500C 473Eh       |
| EPWM5_G0      | 5000 573Eh       |
| EPWM5_G1      | 5004 573Eh       |
| EPWM5_G2      | 5008 573Eh       |
| EPWM5_G3      | 500C 573Eh       |
| EPWM6_G0      | 5000 673Eh       |
| EPWM6_G1      | 5004 673Eh       |
| EPWM6_G2      | 5008 673Eh       |
| EPWM6_G3      | 500C 673Eh       |
| EPWM7_G0      | 5000 773Eh       |
| EPWM7_G1      | 5004 773Eh       |
| EPWM7_G2      | 5008 773Eh       |
| EPWM7_G3      | 500C 773Eh       |
| EPWM8_G0      | 5000 873Eh       |
| EPWM8_G1      | 5004 873Eh       |
| EPWM8_G2      | 5008 873Eh       |
| EPWM8_G3      | 500C 873Eh       |
| EPWM9_G0      | 5000 973Eh       |
| EPWM9_G1      | 5004 973Eh       |
| EPWM9_G2      | 5008 973Eh       |

**Table 3-1243. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 973Eh       |
| EPWM10_G0     | 5000 A73Eh       |
| EPWM10_G1     | 5004 A73Eh       |
| EPWM10_G2     | 5008 A73Eh       |
| EPWM10_G3     | 500C A73Eh       |
| EPWM11_G0     | 5000 B73Eh       |
| EPWM11_G1     | 5004 B73Eh       |
| EPWM11_G2     | 5008 B73Eh       |
| EPWM11_G3     | 500C B73Eh       |
| EPWM12_G0     | 5000 C73Eh       |
| EPWM12_G1     | 5004 C73Eh       |
| EPWM12_G2     | 5008 C73Eh       |
| EPWM12_G3     | 500C C73Eh       |
| EPWM13_G0     | 5000 D73Eh       |
| EPWM13_G1     | 5004 D73Eh       |
| EPWM13_G2     | 5008 D73Eh       |
| EPWM13_G3     | 500C D73Eh       |
| EPWM14_G0     | 5000 E73Eh       |
| EPWM14_G1     | 5004 E73Eh       |
| EPWM14_G2     | 5008 E73Eh       |
| EPWM14_G3     | 500C E73Eh       |
| EPWM15_G0     | 5000 F73Eh       |
| EPWM15_G1     | 5004 F73Eh       |
| EPWM15_G2     | 5008 F73Eh       |
| EPWM15_G3     | 500C F73Eh       |
| EPWM16_G0     | 5001 073Eh       |
| EPWM16_G1     | 5005 073Eh       |
| EPWM16_G2     | 5009 073Eh       |
| EPWM16_G3     | 500D 073Eh       |
| EPWM17_G0     | 5001 173Eh       |
| EPWM17_G1     | 5005 173Eh       |
| EPWM17_G2     | 5009 173Eh       |
| EPWM17_G3     | 500D 173Eh       |
| EPWM18_G0     | 5001 273Eh       |
| EPWM18_G1     | 5005 273Eh       |
| EPWM18_G2     | 5009 273Eh       |
| EPWM18_G3     | 500D 273Eh       |
| EPWM19_G0     | 5001 373Eh       |
| EPWM19_G1     | 5005 373Eh       |
| EPWM19_G2     | 5009 373Eh       |
| EPWM19_G3     | 500D 373Eh       |
| EPWM20_G0     | 5001 473Eh       |
| EPWM20_G1     | 5005 473Eh       |
| EPWM20_G2     | 5009 473Eh       |
| EPWM20_G3     | 500D 473Eh       |

**Table 3-1243. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 573Eh       |
| EPWM21_G1     | 5005 573Eh       |
| EPWM21_G2     | 5009 573Eh       |
| EPWM21_G3     | 500D 573Eh       |
| EPWM22_G0     | 5001 673Eh       |
| EPWM22_G1     | 5005 673Eh       |
| EPWM22_G2     | 5009 673Eh       |
| EPWM22_G3     | 500D 673Eh       |
| EPWM23_G0     | 5001 773Eh       |
| EPWM23_G1     | 5005 773Eh       |
| EPWM23_G2     | 5009 773Eh       |
| EPWM23_G3     | 500D 773Eh       |
| EPWM24_G0     | 5001 873Eh       |
| EPWM24_G1     | 5005 873Eh       |
| EPWM24_G2     | 5009 873Eh       |
| EPWM24_G3     | 500D 873Eh       |
| EPWM25_G0     | 5001 973Eh       |
| EPWM25_G1     | 5005 973Eh       |
| EPWM25_G2     | 5009 973Eh       |
| EPWM25_G3     | 500D 973Eh       |
| EPWM26_G0     | 5001 A73Eh       |
| EPWM26_G1     | 5005 A73Eh       |
| EPWM26_G2     | 5009 A73Eh       |
| EPWM26_G3     | 500D A73Eh       |
| EPWM27_G0     | 5001 B73Eh       |
| EPWM27_G1     | 5005 B73Eh       |
| EPWM27_G2     | 5009 B73Eh       |
| EPWM27_G3     | 500D B73Eh       |
| EPWM28_G0     | 5001 C73Eh       |
| EPWM28_G1     | 5005 C73Eh       |
| EPWM28_G2     | 5009 C73Eh       |
| EPWM28_G3     | 500D C73Eh       |
| EPWM29_G0     | 5001 D73Eh       |
| EPWM29_G1     | 5005 D73Eh       |
| EPWM29_G2     | 5009 D73Eh       |
| EPWM29_G3     | 500D D73Eh       |
| EPWM30_G0     | 5001 E73Eh       |
| EPWM30_G1     | 5005 E73Eh       |
| EPWM30_G2     | 5009 E73Eh       |
| EPWM30_G3     | 500D E73Eh       |
| EPWM31_G0     | 5001 F73Eh       |
| EPWM31_G1     | 5005 F73Eh       |
| EPWM31_G2     | 5009 F73Eh       |
| EPWM31_G3     | 500D F73Eh       |

**Figure 3-395. EPWM\_CMPD\_SHDW2 Name Register**

|            |    |    |    |    |    |   |   |
|------------|----|----|----|----|----|---|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMPD_SHDW2 |    |    |    |    |    |   |   |
| R/W        |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| CMPD_SHDW2 |    |    |    |    |    |   |   |
| R/W        |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |

**Table 3-1245. EPWM\_CMPD\_SHDW2 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                 |
|------|------------|------|-------|-------------------------------------------------------------------------------------------------------------|
| 15:0 | CMPD_SHDW2 | R/W  | 0h    | The value in the CMPD_SHDW2 register is loaded into CMPD_ACTIVE register when shadow to active load occurs. |

### 3.7.2.145 EPWM\_XMINMAX\_SHDW2 Register

#### 1 EPWM\_XMINMAX\_SHDW2 Register (Offset = 744h) [reset = 0h]

XMINMAX Shadow 2 Register.

Return to [Summary Table](#)

**Table 3-1246. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0744h       |
| EPWM0_G1      | 5004 0744h       |
| EPWM0_G2      | 5008 0744h       |
| EPWM0_G3      | 500C 0744h       |
| EPWM1_G0      | 5000 1744h       |
| EPWM1_G1      | 5004 1744h       |
| EPWM1_G2      | 5008 1744h       |
| EPWM1_G3      | 500C 1744h       |
| EPWM2_G0      | 5000 2744h       |
| EPWM2_G1      | 5004 2744h       |
| EPWM2_G2      | 5008 2744h       |
| EPWM2_G3      | 500C 2744h       |
| EPWM3_G0      | 5000 3744h       |
| EPWM3_G1      | 5004 3744h       |
| EPWM3_G2      | 5008 3744h       |
| EPWM3_G3      | 500C 3744h       |
| EPWM4_G0      | 5000 4744h       |
| EPWM4_G1      | 5004 4744h       |
| EPWM4_G2      | 5008 4744h       |
| EPWM4_G3      | 500C 4744h       |
| EPWM5_G0      | 5000 5744h       |
| EPWM5_G1      | 5004 5744h       |
| EPWM5_G2      | 5008 5744h       |
| EPWM5_G3      | 500C 5744h       |
| EPWM6_G0      | 5000 6744h       |
| EPWM6_G1      | 5004 6744h       |
| EPWM6_G2      | 5008 6744h       |
| EPWM6_G3      | 500C 6744h       |
| EPWM7_G0      | 5000 7744h       |
| EPWM7_G1      | 5004 7744h       |
| EPWM7_G2      | 5008 7744h       |
| EPWM7_G3      | 500C 7744h       |
| EPWM8_G0      | 5000 8744h       |
| EPWM8_G1      | 5004 8744h       |
| EPWM8_G2      | 5008 8744h       |
| EPWM8_G3      | 500C 8744h       |
| EPWM9_G0      | 5000 9744h       |
| EPWM9_G1      | 5004 9744h       |
| EPWM9_G2      | 5008 9744h       |

**Table 3-1246. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9744h       |
| EPWM10_G0     | 5000 A744h       |
| EPWM10_G1     | 5004 A744h       |
| EPWM10_G2     | 5008 A744h       |
| EPWM10_G3     | 500C A744h       |
| EPWM11_G0     | 5000 B744h       |
| EPWM11_G1     | 5004 B744h       |
| EPWM11_G2     | 5008 B744h       |
| EPWM11_G3     | 500C B744h       |
| EPWM12_G0     | 5000 C744h       |
| EPWM12_G1     | 5004 C744h       |
| EPWM12_G2     | 5008 C744h       |
| EPWM12_G3     | 500C C744h       |
| EPWM13_G0     | 5000 D744h       |
| EPWM13_G1     | 5004 D744h       |
| EPWM13_G2     | 5008 D744h       |
| EPWM13_G3     | 500C D744h       |
| EPWM14_G0     | 5000 E744h       |
| EPWM14_G1     | 5004 E744h       |
| EPWM14_G2     | 5008 E744h       |
| EPWM14_G3     | 500C E744h       |
| EPWM15_G0     | 5000 F744h       |
| EPWM15_G1     | 5004 F744h       |
| EPWM15_G2     | 5008 F744h       |
| EPWM15_G3     | 500C F744h       |
| EPWM16_G0     | 5001 0744h       |
| EPWM16_G1     | 5005 0744h       |
| EPWM16_G2     | 5009 0744h       |
| EPWM16_G3     | 500D 0744h       |
| EPWM17_G0     | 5001 1744h       |
| EPWM17_G1     | 5005 1744h       |
| EPWM17_G2     | 5009 1744h       |
| EPWM17_G3     | 500D 1744h       |
| EPWM18_G0     | 5001 2744h       |
| EPWM18_G1     | 5005 2744h       |
| EPWM18_G2     | 5009 2744h       |
| EPWM18_G3     | 500D 2744h       |
| EPWM19_G0     | 5001 3744h       |
| EPWM19_G1     | 5005 3744h       |
| EPWM19_G2     | 5009 3744h       |
| EPWM19_G3     | 500D 3744h       |
| EPWM20_G0     | 5001 4744h       |
| EPWM20_G1     | 5005 4744h       |
| EPWM20_G2     | 5009 4744h       |
| EPWM20_G3     | 500D 4744h       |



**Table 3-1246. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5744h       |
| EPWM21_G1     | 5005 5744h       |
| EPWM21_G2     | 5009 5744h       |
| EPWM21_G3     | 500D 5744h       |
| EPWM22_G0     | 5001 6744h       |
| EPWM22_G1     | 5005 6744h       |
| EPWM22_G2     | 5009 6744h       |
| EPWM22_G3     | 500D 6744h       |
| EPWM23_G0     | 5001 7744h       |
| EPWM23_G1     | 5005 7744h       |
| EPWM23_G2     | 5009 7744h       |
| EPWM23_G3     | 500D 7744h       |
| EPWM24_G0     | 5001 8744h       |
| EPWM24_G1     | 5005 8744h       |
| EPWM24_G2     | 5009 8744h       |
| EPWM24_G3     | 500D 8744h       |
| EPWM25_G0     | 5001 9744h       |
| EPWM25_G1     | 5005 9744h       |
| EPWM25_G2     | 5009 9744h       |
| EPWM25_G3     | 500D 9744h       |
| EPWM26_G0     | 5001 A744h       |
| EPWM26_G1     | 5005 A744h       |
| EPWM26_G2     | 5009 A744h       |
| EPWM26_G3     | 500D A744h       |
| EPWM27_G0     | 5001 B744h       |
| EPWM27_G1     | 5005 B744h       |
| EPWM27_G2     | 5009 B744h       |
| EPWM27_G3     | 500D B744h       |
| EPWM28_G0     | 5001 C744h       |
| EPWM28_G1     | 5005 C744h       |
| EPWM28_G2     | 5009 C744h       |
| EPWM28_G3     | 500D C744h       |
| EPWM29_G0     | 5001 D744h       |
| EPWM29_G1     | 5005 D744h       |
| EPWM29_G2     | 5009 D744h       |
| EPWM29_G3     | 500D D744h       |
| EPWM30_G0     | 5001 E744h       |
| EPWM30_G1     | 5005 E744h       |
| EPWM30_G2     | 5009 E744h       |
| EPWM30_G3     | 500D E744h       |
| EPWM31_G0     | 5001 F744h       |
| EPWM31_G1     | 5005 F744h       |
| EPWM31_G2     | 5009 F744h       |
| EPWM31_G3     | 500D F744h       |

**Figure 3-396. EPWM\_XMINMAX\_SHDW2 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XMIN_SHDW2 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XMIN_SHDW2 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XMAX_SHDW2 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XMAX_SHDW2 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 3-1248. EPWM\_XMINMAX\_SHDW2 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                 |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------|
| 31:16 | XMIN_SHDW2 | R/W  | 0h    | The value in the XMIN_SHDW2 register is loaded into XMIN_ACTIVE register when shadow to active load occurs. |
| 15:0  | XMAX_SHDW2 | R/W  | 0h    | The value in the XMAX_SHDW2 register is loaded into XMAX_ACTIVE register when shadow to active load occurs. |

### 3.7.2.146 EPWM\_XCMP1\_SHDW3 Register

#### 1 EPWM\_XCMP1\_SHDW3 Register (Offset = 780h) [reset = 0h]

Additional Compare 1 Shadow 3 Register.

Return to [Summary Table](#)

**Table 3-1249. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0780h       |
| EPWM0_G1      | 5004 0780h       |
| EPWM0_G2      | 5008 0780h       |
| EPWM0_G3      | 500C 0780h       |
| EPWM1_G0      | 5000 1780h       |
| EPWM1_G1      | 5004 1780h       |
| EPWM1_G2      | 5008 1780h       |
| EPWM1_G3      | 500C 1780h       |
| EPWM2_G0      | 5000 2780h       |
| EPWM2_G1      | 5004 2780h       |
| EPWM2_G2      | 5008 2780h       |
| EPWM2_G3      | 500C 2780h       |
| EPWM3_G0      | 5000 3780h       |
| EPWM3_G1      | 5004 3780h       |
| EPWM3_G2      | 5008 3780h       |
| EPWM3_G3      | 500C 3780h       |
| EPWM4_G0      | 5000 4780h       |
| EPWM4_G1      | 5004 4780h       |
| EPWM4_G2      | 5008 4780h       |
| EPWM4_G3      | 500C 4780h       |
| EPWM5_G0      | 5000 5780h       |
| EPWM5_G1      | 5004 5780h       |
| EPWM5_G2      | 5008 5780h       |
| EPWM5_G3      | 500C 5780h       |
| EPWM6_G0      | 5000 6780h       |
| EPWM6_G1      | 5004 6780h       |
| EPWM6_G2      | 5008 6780h       |
| EPWM6_G3      | 500C 6780h       |
| EPWM7_G0      | 5000 7780h       |
| EPWM7_G1      | 5004 7780h       |
| EPWM7_G2      | 5008 7780h       |
| EPWM7_G3      | 500C 7780h       |
| EPWM8_G0      | 5000 8780h       |
| EPWM8_G1      | 5004 8780h       |
| EPWM8_G2      | 5008 8780h       |
| EPWM8_G3      | 500C 8780h       |
| EPWM9_G0      | 5000 9780h       |
| EPWM9_G1      | 5004 9780h       |
| EPWM9_G2      | 5008 9780h       |

**Table 3-1249. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9780h       |
| EPWM10_G0     | 5000 A780h       |
| EPWM10_G1     | 5004 A780h       |
| EPWM10_G2     | 5008 A780h       |
| EPWM10_G3     | 500C A780h       |
| EPWM11_G0     | 5000 B780h       |
| EPWM11_G1     | 5004 B780h       |
| EPWM11_G2     | 5008 B780h       |
| EPWM11_G3     | 500C B780h       |
| EPWM12_G0     | 5000 C780h       |
| EPWM12_G1     | 5004 C780h       |
| EPWM12_G2     | 5008 C780h       |
| EPWM12_G3     | 500C C780h       |
| EPWM13_G0     | 5000 D780h       |
| EPWM13_G1     | 5004 D780h       |
| EPWM13_G2     | 5008 D780h       |
| EPWM13_G3     | 500C D780h       |
| EPWM14_G0     | 5000 E780h       |
| EPWM14_G1     | 5004 E780h       |
| EPWM14_G2     | 5008 E780h       |
| EPWM14_G3     | 500C E780h       |
| EPWM15_G0     | 5000 F780h       |
| EPWM15_G1     | 5004 F780h       |
| EPWM15_G2     | 5008 F780h       |
| EPWM15_G3     | 500C F780h       |
| EPWM16_G0     | 5001 0780h       |
| EPWM16_G1     | 5005 0780h       |
| EPWM16_G2     | 5009 0780h       |
| EPWM16_G3     | 500D 0780h       |
| EPWM17_G0     | 5001 1780h       |
| EPWM17_G1     | 5005 1780h       |
| EPWM17_G2     | 5009 1780h       |
| EPWM17_G3     | 500D 1780h       |
| EPWM18_G0     | 5001 2780h       |
| EPWM18_G1     | 5005 2780h       |
| EPWM18_G2     | 5009 2780h       |
| EPWM18_G3     | 500D 2780h       |
| EPWM19_G0     | 5001 3780h       |
| EPWM19_G1     | 5005 3780h       |
| EPWM19_G2     | 5009 3780h       |
| EPWM19_G3     | 500D 3780h       |
| EPWM20_G0     | 5001 4780h       |
| EPWM20_G1     | 5005 4780h       |
| EPWM20_G2     | 5009 4780h       |
| EPWM20_G3     | 500D 4780h       |

**Table 3-1249. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5780h       |
| EPWM21_G1     | 5005 5780h       |
| EPWM21_G2     | 5009 5780h       |
| EPWM21_G3     | 500D 5780h       |
| EPWM22_G0     | 5001 6780h       |
| EPWM22_G1     | 5005 6780h       |
| EPWM22_G2     | 5009 6780h       |
| EPWM22_G3     | 500D 6780h       |
| EPWM23_G0     | 5001 7780h       |
| EPWM23_G1     | 5005 7780h       |
| EPWM23_G2     | 5009 7780h       |
| EPWM23_G3     | 500D 7780h       |
| EPWM24_G0     | 5001 8780h       |
| EPWM24_G1     | 5005 8780h       |
| EPWM24_G2     | 5009 8780h       |
| EPWM24_G3     | 500D 8780h       |
| EPWM25_G0     | 5001 9780h       |
| EPWM25_G1     | 5005 9780h       |
| EPWM25_G2     | 5009 9780h       |
| EPWM25_G3     | 500D 9780h       |
| EPWM26_G0     | 5001 A780h       |
| EPWM26_G1     | 5005 A780h       |
| EPWM26_G2     | 5009 A780h       |
| EPWM26_G3     | 500D A780h       |
| EPWM27_G0     | 5001 B780h       |
| EPWM27_G1     | 5005 B780h       |
| EPWM27_G2     | 5009 B780h       |
| EPWM27_G3     | 500D B780h       |
| EPWM28_G0     | 5001 C780h       |
| EPWM28_G1     | 5005 C780h       |
| EPWM28_G2     | 5009 C780h       |
| EPWM28_G3     | 500D C780h       |
| EPWM29_G0     | 5001 D780h       |
| EPWM29_G1     | 5005 D780h       |
| EPWM29_G2     | 5009 D780h       |
| EPWM29_G3     | 500D D780h       |
| EPWM30_G0     | 5001 E780h       |
| EPWM30_G1     | 5005 E780h       |
| EPWM30_G2     | 5009 E780h       |
| EPWM30_G3     | 500D E780h       |
| EPWM31_G0     | 5001 F780h       |
| EPWM31_G1     | 5005 F780h       |
| EPWM31_G2     | 5009 F780h       |
| EPWM31_G3     | 500D F780h       |

**Figure 3-397. EPWM\_XCMP1\_SHDW3 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP1_SHDW3   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP1_SHDW3   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP1HR_SHDW3 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP1HR_SHDW3 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 3-1251. EPWM\_XCMP1\_SHDW3 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                 |
|-------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP1_SHDW3   | R/W  | 0h    | XCMP1_SHDW3 Register<br>The value in the XCMP1_SHDW3 register is loaded into XCMP1_ACTIVE register when shadow to active load occurs.       |
| 15:0  | XCMP1HR_SHDW3 | R/W  | 0h    | XCMP1HR_SHDW3 Register<br>The value in the XCMP1HR_SHDW3 register is loaded into XCMP1HR_ACTIVE register when shadow to active load occurs. |

### 3.7.2.147 EPWM\_XCMP2\_SHDW3 Register

#### 1 EPWM\_XCMP2\_SHDW3 Register (Offset = 784h) [reset = 0h]

Additional Compare 2 Shadow 3 Register.

Return to [Summary Table](#)

**Table 3-1252. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0784h       |
| EPWM0_G1      | 5004 0784h       |
| EPWM0_G2      | 5008 0784h       |
| EPWM0_G3      | 500C 0784h       |
| EPWM1_G0      | 5000 1784h       |
| EPWM1_G1      | 5004 1784h       |
| EPWM1_G2      | 5008 1784h       |
| EPWM1_G3      | 500C 1784h       |
| EPWM2_G0      | 5000 2784h       |
| EPWM2_G1      | 5004 2784h       |
| EPWM2_G2      | 5008 2784h       |
| EPWM2_G3      | 500C 2784h       |
| EPWM3_G0      | 5000 3784h       |
| EPWM3_G1      | 5004 3784h       |
| EPWM3_G2      | 5008 3784h       |
| EPWM3_G3      | 500C 3784h       |
| EPWM4_G0      | 5000 4784h       |
| EPWM4_G1      | 5004 4784h       |
| EPWM4_G2      | 5008 4784h       |
| EPWM4_G3      | 500C 4784h       |
| EPWM5_G0      | 5000 5784h       |
| EPWM5_G1      | 5004 5784h       |
| EPWM5_G2      | 5008 5784h       |
| EPWM5_G3      | 500C 5784h       |
| EPWM6_G0      | 5000 6784h       |
| EPWM6_G1      | 5004 6784h       |
| EPWM6_G2      | 5008 6784h       |
| EPWM6_G3      | 500C 6784h       |
| EPWM7_G0      | 5000 7784h       |
| EPWM7_G1      | 5004 7784h       |
| EPWM7_G2      | 5008 7784h       |
| EPWM7_G3      | 500C 7784h       |
| EPWM8_G0      | 5000 8784h       |
| EPWM8_G1      | 5004 8784h       |
| EPWM8_G2      | 5008 8784h       |
| EPWM8_G3      | 500C 8784h       |
| EPWM9_G0      | 5000 9784h       |
| EPWM9_G1      | 5004 9784h       |
| EPWM9_G2      | 5008 9784h       |

**Table 3-1252. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9784h       |
| EPWM10_G0     | 5000 A784h       |
| EPWM10_G1     | 5004 A784h       |
| EPWM10_G2     | 5008 A784h       |
| EPWM10_G3     | 500C A784h       |
| EPWM11_G0     | 5000 B784h       |
| EPWM11_G1     | 5004 B784h       |
| EPWM11_G2     | 5008 B784h       |
| EPWM11_G3     | 500C B784h       |
| EPWM12_G0     | 5000 C784h       |
| EPWM12_G1     | 5004 C784h       |
| EPWM12_G2     | 5008 C784h       |
| EPWM12_G3     | 500C C784h       |
| EPWM13_G0     | 5000 D784h       |
| EPWM13_G1     | 5004 D784h       |
| EPWM13_G2     | 5008 D784h       |
| EPWM13_G3     | 500C D784h       |
| EPWM14_G0     | 5000 E784h       |
| EPWM14_G1     | 5004 E784h       |
| EPWM14_G2     | 5008 E784h       |
| EPWM14_G3     | 500C E784h       |
| EPWM15_G0     | 5000 F784h       |
| EPWM15_G1     | 5004 F784h       |
| EPWM15_G2     | 5008 F784h       |
| EPWM15_G3     | 500C F784h       |
| EPWM16_G0     | 5001 0784h       |
| EPWM16_G1     | 5005 0784h       |
| EPWM16_G2     | 5009 0784h       |
| EPWM16_G3     | 500D 0784h       |
| EPWM17_G0     | 5001 1784h       |
| EPWM17_G1     | 5005 1784h       |
| EPWM17_G2     | 5009 1784h       |
| EPWM17_G3     | 500D 1784h       |
| EPWM18_G0     | 5001 2784h       |
| EPWM18_G1     | 5005 2784h       |
| EPWM18_G2     | 5009 2784h       |
| EPWM18_G3     | 500D 2784h       |
| EPWM19_G0     | 5001 3784h       |
| EPWM19_G1     | 5005 3784h       |
| EPWM19_G2     | 5009 3784h       |
| EPWM19_G3     | 500D 3784h       |
| EPWM20_G0     | 5001 4784h       |
| EPWM20_G1     | 5005 4784h       |
| EPWM20_G2     | 5009 4784h       |
| EPWM20_G3     | 500D 4784h       |



**Table 3-1252. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5784h       |
| EPWM21_G1     | 5005 5784h       |
| EPWM21_G2     | 5009 5784h       |
| EPWM21_G3     | 500D 5784h       |
| EPWM22_G0     | 5001 6784h       |
| EPWM22_G1     | 5005 6784h       |
| EPWM22_G2     | 5009 6784h       |
| EPWM22_G3     | 500D 6784h       |
| EPWM23_G0     | 5001 7784h       |
| EPWM23_G1     | 5005 7784h       |
| EPWM23_G2     | 5009 7784h       |
| EPWM23_G3     | 500D 7784h       |
| EPWM24_G0     | 5001 8784h       |
| EPWM24_G1     | 5005 8784h       |
| EPWM24_G2     | 5009 8784h       |
| EPWM24_G3     | 500D 8784h       |
| EPWM25_G0     | 5001 9784h       |
| EPWM25_G1     | 5005 9784h       |
| EPWM25_G2     | 5009 9784h       |
| EPWM25_G3     | 500D 9784h       |
| EPWM26_G0     | 5001 A784h       |
| EPWM26_G1     | 5005 A784h       |
| EPWM26_G2     | 5009 A784h       |
| EPWM26_G3     | 500D A784h       |
| EPWM27_G0     | 5001 B784h       |
| EPWM27_G1     | 5005 B784h       |
| EPWM27_G2     | 5009 B784h       |
| EPWM27_G3     | 500D B784h       |
| EPWM28_G0     | 5001 C784h       |
| EPWM28_G1     | 5005 C784h       |
| EPWM28_G2     | 5009 C784h       |
| EPWM28_G3     | 500D C784h       |
| EPWM29_G0     | 5001 D784h       |
| EPWM29_G1     | 5005 D784h       |
| EPWM29_G2     | 5009 D784h       |
| EPWM29_G3     | 500D D784h       |
| EPWM30_G0     | 5001 E784h       |
| EPWM30_G1     | 5005 E784h       |
| EPWM30_G2     | 5009 E784h       |
| EPWM30_G3     | 500D E784h       |
| EPWM31_G0     | 5001 F784h       |
| EPWM31_G1     | 5005 F784h       |
| EPWM31_G2     | 5009 F784h       |
| EPWM31_G3     | 500D F784h       |

**Figure 3-398. EPWM\_XCMP2\_SHDW3 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP2_SHDW3   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP2_SHDW3   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP2HR_SHDW3 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP2HR_SHDW3 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 3-1254. EPWM\_XCMP2\_SHDW3 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                 |
|-------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP2_SHDW3   | R/W  | 0h    | XCMP2_SHDW3 Register<br>The value in the XCMP2_SHDW3 register is loaded into XCMP2_ACTIVE register when shadow to active load occurs.       |
| 15:0  | XCMP2HR_SHDW3 | R/W  | 0h    | XCMP2HR_SHDW3 Register<br>The value in the XCMP2HR_SHDW3 register is loaded into XCMP2HR_ACTIVE register when shadow to active load occurs. |

### 3.7.2.148 EPWM\_XCMP3\_SHDW3 Register

#### 1 EPWM\_XCMP3\_SHDW3 Register (Offset = 788h) [reset = 0h]

Additional Compare 3 Shadow 3 Register.

Return to [Summary Table](#)

**Table 3-1255. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0788h       |
| EPWM0_G1      | 5004 0788h       |
| EPWM0_G2      | 5008 0788h       |
| EPWM0_G3      | 500C 0788h       |
| EPWM1_G0      | 5000 1788h       |
| EPWM1_G1      | 5004 1788h       |
| EPWM1_G2      | 5008 1788h       |
| EPWM1_G3      | 500C 1788h       |
| EPWM2_G0      | 5000 2788h       |
| EPWM2_G1      | 5004 2788h       |
| EPWM2_G2      | 5008 2788h       |
| EPWM2_G3      | 500C 2788h       |
| EPWM3_G0      | 5000 3788h       |
| EPWM3_G1      | 5004 3788h       |
| EPWM3_G2      | 5008 3788h       |
| EPWM3_G3      | 500C 3788h       |
| EPWM4_G0      | 5000 4788h       |
| EPWM4_G1      | 5004 4788h       |
| EPWM4_G2      | 5008 4788h       |
| EPWM4_G3      | 500C 4788h       |
| EPWM5_G0      | 5000 5788h       |
| EPWM5_G1      | 5004 5788h       |
| EPWM5_G2      | 5008 5788h       |
| EPWM5_G3      | 500C 5788h       |
| EPWM6_G0      | 5000 6788h       |
| EPWM6_G1      | 5004 6788h       |
| EPWM6_G2      | 5008 6788h       |
| EPWM6_G3      | 500C 6788h       |
| EPWM7_G0      | 5000 7788h       |
| EPWM7_G1      | 5004 7788h       |
| EPWM7_G2      | 5008 7788h       |
| EPWM7_G3      | 500C 7788h       |
| EPWM8_G0      | 5000 8788h       |
| EPWM8_G1      | 5004 8788h       |
| EPWM8_G2      | 5008 8788h       |
| EPWM8_G3      | 500C 8788h       |
| EPWM9_G0      | 5000 9788h       |
| EPWM9_G1      | 5004 9788h       |
| EPWM9_G2      | 5008 9788h       |

**Table 3-1255. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9788h       |
| EPWM10_G0     | 5000 A788h       |
| EPWM10_G1     | 5004 A788h       |
| EPWM10_G2     | 5008 A788h       |
| EPWM10_G3     | 500C A788h       |
| EPWM11_G0     | 5000 B788h       |
| EPWM11_G1     | 5004 B788h       |
| EPWM11_G2     | 5008 B788h       |
| EPWM11_G3     | 500C B788h       |
| EPWM12_G0     | 5000 C788h       |
| EPWM12_G1     | 5004 C788h       |
| EPWM12_G2     | 5008 C788h       |
| EPWM12_G3     | 500C C788h       |
| EPWM13_G0     | 5000 D788h       |
| EPWM13_G1     | 5004 D788h       |
| EPWM13_G2     | 5008 D788h       |
| EPWM13_G3     | 500C D788h       |
| EPWM14_G0     | 5000 E788h       |
| EPWM14_G1     | 5004 E788h       |
| EPWM14_G2     | 5008 E788h       |
| EPWM14_G3     | 500C E788h       |
| EPWM15_G0     | 5000 F788h       |
| EPWM15_G1     | 5004 F788h       |
| EPWM15_G2     | 5008 F788h       |
| EPWM15_G3     | 500C F788h       |
| EPWM16_G0     | 5001 0788h       |
| EPWM16_G1     | 5005 0788h       |
| EPWM16_G2     | 5009 0788h       |
| EPWM16_G3     | 500D 0788h       |
| EPWM17_G0     | 5001 1788h       |
| EPWM17_G1     | 5005 1788h       |
| EPWM17_G2     | 5009 1788h       |
| EPWM17_G3     | 500D 1788h       |
| EPWM18_G0     | 5001 2788h       |
| EPWM18_G1     | 5005 2788h       |
| EPWM18_G2     | 5009 2788h       |
| EPWM18_G3     | 500D 2788h       |
| EPWM19_G0     | 5001 3788h       |
| EPWM19_G1     | 5005 3788h       |
| EPWM19_G2     | 5009 3788h       |
| EPWM19_G3     | 500D 3788h       |
| EPWM20_G0     | 5001 4788h       |
| EPWM20_G1     | 5005 4788h       |
| EPWM20_G2     | 5009 4788h       |
| EPWM20_G3     | 500D 4788h       |

**Table 3-1255. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5788h       |
| EPWM21_G1     | 5005 5788h       |
| EPWM21_G2     | 5009 5788h       |
| EPWM21_G3     | 500D 5788h       |
| EPWM22_G0     | 5001 6788h       |
| EPWM22_G1     | 5005 6788h       |
| EPWM22_G2     | 5009 6788h       |
| EPWM22_G3     | 500D 6788h       |
| EPWM23_G0     | 5001 7788h       |
| EPWM23_G1     | 5005 7788h       |
| EPWM23_G2     | 5009 7788h       |
| EPWM23_G3     | 500D 7788h       |
| EPWM24_G0     | 5001 8788h       |
| EPWM24_G1     | 5005 8788h       |
| EPWM24_G2     | 5009 8788h       |
| EPWM24_G3     | 500D 8788h       |
| EPWM25_G0     | 5001 9788h       |
| EPWM25_G1     | 5005 9788h       |
| EPWM25_G2     | 5009 9788h       |
| EPWM25_G3     | 500D 9788h       |
| EPWM26_G0     | 5001 A788h       |
| EPWM26_G1     | 5005 A788h       |
| EPWM26_G2     | 5009 A788h       |
| EPWM26_G3     | 500D A788h       |
| EPWM27_G0     | 5001 B788h       |
| EPWM27_G1     | 5005 B788h       |
| EPWM27_G2     | 5009 B788h       |
| EPWM27_G3     | 500D B788h       |
| EPWM28_G0     | 5001 C788h       |
| EPWM28_G1     | 5005 C788h       |
| EPWM28_G2     | 5009 C788h       |
| EPWM28_G3     | 500D C788h       |
| EPWM29_G0     | 5001 D788h       |
| EPWM29_G1     | 5005 D788h       |
| EPWM29_G2     | 5009 D788h       |
| EPWM29_G3     | 500D D788h       |
| EPWM30_G0     | 5001 E788h       |
| EPWM30_G1     | 5005 E788h       |
| EPWM30_G2     | 5009 E788h       |
| EPWM30_G3     | 500D E788h       |
| EPWM31_G0     | 5001 F788h       |
| EPWM31_G1     | 5005 F788h       |
| EPWM31_G2     | 5009 F788h       |
| EPWM31_G3     | 500D F788h       |

**Figure 3-399. EPWM\_XCMP3\_SHDW3 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP3_SHDW3   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP3_SHDW3   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP3HR_SHDW3 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP3HR_SHDW3 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 3-1257. EPWM\_XCMP3\_SHDW3 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                 |
|-------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP3_SHDW3   | R/W  | 0h    | XCMP3_SHDW3 Register<br>The value in the XCMP3_SHDW3 register is loaded into XCMP3_ACTIVE register when shadow to active load occurs.       |
| 15:0  | XCMP3HR_SHDW3 | R/W  | 0h    | XCMP3HR_SHDW3 Register<br>The value in the XCMP3HR_SHDW3 register is loaded into XCMP3HR_ACTIVE register when shadow to active load occurs. |

### 3.7.2.149 EPWM\_XCMP4\_SHDW3 Register

#### 1 EPWM\_XCMP4\_SHDW3 Register (Offset = 78Ch) [reset = 0h]

Additional Compare 4 Shadow 3 Register.

Return to [Summary Table](#)

**Table 3-1258. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 078Ch       |
| EPWM0_G1      | 5004 078Ch       |
| EPWM0_G2      | 5008 078Ch       |
| EPWM0_G3      | 500C 078Ch       |
| EPWM1_G0      | 5000 178Ch       |
| EPWM1_G1      | 5004 178Ch       |
| EPWM1_G2      | 5008 178Ch       |
| EPWM1_G3      | 500C 178Ch       |
| EPWM2_G0      | 5000 278Ch       |
| EPWM2_G1      | 5004 278Ch       |
| EPWM2_G2      | 5008 278Ch       |
| EPWM2_G3      | 500C 278Ch       |
| EPWM3_G0      | 5000 378Ch       |
| EPWM3_G1      | 5004 378Ch       |
| EPWM3_G2      | 5008 378Ch       |
| EPWM3_G3      | 500C 378Ch       |
| EPWM4_G0      | 5000 478Ch       |
| EPWM4_G1      | 5004 478Ch       |
| EPWM4_G2      | 5008 478Ch       |
| EPWM4_G3      | 500C 478Ch       |
| EPWM5_G0      | 5000 578Ch       |
| EPWM5_G1      | 5004 578Ch       |
| EPWM5_G2      | 5008 578Ch       |
| EPWM5_G3      | 500C 578Ch       |
| EPWM6_G0      | 5000 678Ch       |
| EPWM6_G1      | 5004 678Ch       |
| EPWM6_G2      | 5008 678Ch       |
| EPWM6_G3      | 500C 678Ch       |
| EPWM7_G0      | 5000 778Ch       |
| EPWM7_G1      | 5004 778Ch       |
| EPWM7_G2      | 5008 778Ch       |
| EPWM7_G3      | 500C 778Ch       |
| EPWM8_G0      | 5000 878Ch       |
| EPWM8_G1      | 5004 878Ch       |
| EPWM8_G2      | 5008 878Ch       |
| EPWM8_G3      | 500C 878Ch       |
| EPWM9_G0      | 5000 978Ch       |
| EPWM9_G1      | 5004 978Ch       |
| EPWM9_G2      | 5008 978Ch       |

**Table 3-1258. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 978Ch       |
| EPWM10_G0     | 5000 A78Ch       |
| EPWM10_G1     | 5004 A78Ch       |
| EPWM10_G2     | 5008 A78Ch       |
| EPWM10_G3     | 500C A78Ch       |
| EPWM11_G0     | 5000 B78Ch       |
| EPWM11_G1     | 5004 B78Ch       |
| EPWM11_G2     | 5008 B78Ch       |
| EPWM11_G3     | 500C B78Ch       |
| EPWM12_G0     | 5000 C78Ch       |
| EPWM12_G1     | 5004 C78Ch       |
| EPWM12_G2     | 5008 C78Ch       |
| EPWM12_G3     | 500C C78Ch       |
| EPWM13_G0     | 5000 D78Ch       |
| EPWM13_G1     | 5004 D78Ch       |
| EPWM13_G2     | 5008 D78Ch       |
| EPWM13_G3     | 500C D78Ch       |
| EPWM14_G0     | 5000 E78Ch       |
| EPWM14_G1     | 5004 E78Ch       |
| EPWM14_G2     | 5008 E78Ch       |
| EPWM14_G3     | 500C E78Ch       |
| EPWM15_G0     | 5000 F78Ch       |
| EPWM15_G1     | 5004 F78Ch       |
| EPWM15_G2     | 5008 F78Ch       |
| EPWM15_G3     | 500C F78Ch       |
| EPWM16_G0     | 5001 078Ch       |
| EPWM16_G1     | 5005 078Ch       |
| EPWM16_G2     | 5009 078Ch       |
| EPWM16_G3     | 500D 078Ch       |
| EPWM17_G0     | 5001 178Ch       |
| EPWM17_G1     | 5005 178Ch       |
| EPWM17_G2     | 5009 178Ch       |
| EPWM17_G3     | 500D 178Ch       |
| EPWM18_G0     | 5001 278Ch       |
| EPWM18_G1     | 5005 278Ch       |
| EPWM18_G2     | 5009 278Ch       |
| EPWM18_G3     | 500D 278Ch       |
| EPWM19_G0     | 5001 378Ch       |
| EPWM19_G1     | 5005 378Ch       |
| EPWM19_G2     | 5009 378Ch       |
| EPWM19_G3     | 500D 378Ch       |
| EPWM20_G0     | 5001 478Ch       |
| EPWM20_G1     | 5005 478Ch       |
| EPWM20_G2     | 5009 478Ch       |
| EPWM20_G3     | 500D 478Ch       |



**Table 3-1258. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 578Ch       |
| EPWM21_G1     | 5005 578Ch       |
| EPWM21_G2     | 5009 578Ch       |
| EPWM21_G3     | 500D 578Ch       |
| EPWM22_G0     | 5001 678Ch       |
| EPWM22_G1     | 5005 678Ch       |
| EPWM22_G2     | 5009 678Ch       |
| EPWM22_G3     | 500D 678Ch       |
| EPWM23_G0     | 5001 778Ch       |
| EPWM23_G1     | 5005 778Ch       |
| EPWM23_G2     | 5009 778Ch       |
| EPWM23_G3     | 500D 778Ch       |
| EPWM24_G0     | 5001 878Ch       |
| EPWM24_G1     | 5005 878Ch       |
| EPWM24_G2     | 5009 878Ch       |
| EPWM24_G3     | 500D 878Ch       |
| EPWM25_G0     | 5001 978Ch       |
| EPWM25_G1     | 5005 978Ch       |
| EPWM25_G2     | 5009 978Ch       |
| EPWM25_G3     | 500D 978Ch       |
| EPWM26_G0     | 5001 A78Ch       |
| EPWM26_G1     | 5005 A78Ch       |
| EPWM26_G2     | 5009 A78Ch       |
| EPWM26_G3     | 500D A78Ch       |
| EPWM27_G0     | 5001 B78Ch       |
| EPWM27_G1     | 5005 B78Ch       |
| EPWM27_G2     | 5009 B78Ch       |
| EPWM27_G3     | 500D B78Ch       |
| EPWM28_G0     | 5001 C78Ch       |
| EPWM28_G1     | 5005 C78Ch       |
| EPWM28_G2     | 5009 C78Ch       |
| EPWM28_G3     | 500D C78Ch       |
| EPWM29_G0     | 5001 D78Ch       |
| EPWM29_G1     | 5005 D78Ch       |
| EPWM29_G2     | 5009 D78Ch       |
| EPWM29_G3     | 500D D78Ch       |
| EPWM30_G0     | 5001 E78Ch       |
| EPWM30_G1     | 5005 E78Ch       |
| EPWM30_G2     | 5009 E78Ch       |
| EPWM30_G3     | 500D E78Ch       |
| EPWM31_G0     | 5001 F78Ch       |
| EPWM31_G1     | 5005 F78Ch       |
| EPWM31_G2     | 5009 F78Ch       |
| EPWM31_G3     | 500D F78Ch       |

**Figure 3-400. EPWM\_XCMP4\_SHDW3 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP4_SHDW3   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP4_SHDW3   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP4HR_SHDW3 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP4HR_SHDW3 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 3-1260. EPWM\_XCMP4\_SHDW3 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                 |
|-------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP4_SHDW3   | R/W  | 0h    | XCMP4_SHDW3 Register<br>The value in the XCMP4_SHDW3 register is loaded into XCMP4_ACTIVE register when shadow to active load occurs.       |
| 15:0  | XCMP4HR_SHDW3 | R/W  | 0h    | XCMP4HR_SHDW3 Register<br>The value in the XCMP4HR_SHDW3 register is loaded into XCMP4HR_ACTIVE register when shadow to active load occurs. |

### 3.7.2.150 EPWM\_XCMP5\_SHDW3 Register

#### 1 EPWM\_XCMP5\_SHDW3 Register (Offset = 790h) [reset = 0h]

Additional Compare 5 Shadow 3 Register.

Return to [Summary Table](#)

**Table 3-1261. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0790h       |
| EPWM0_G1      | 5004 0790h       |
| EPWM0_G2      | 5008 0790h       |
| EPWM0_G3      | 500C 0790h       |
| EPWM1_G0      | 5000 1790h       |
| EPWM1_G1      | 5004 1790h       |
| EPWM1_G2      | 5008 1790h       |
| EPWM1_G3      | 500C 1790h       |
| EPWM2_G0      | 5000 2790h       |
| EPWM2_G1      | 5004 2790h       |
| EPWM2_G2      | 5008 2790h       |
| EPWM2_G3      | 500C 2790h       |
| EPWM3_G0      | 5000 3790h       |
| EPWM3_G1      | 5004 3790h       |
| EPWM3_G2      | 5008 3790h       |
| EPWM3_G3      | 500C 3790h       |
| EPWM4_G0      | 5000 4790h       |
| EPWM4_G1      | 5004 4790h       |
| EPWM4_G2      | 5008 4790h       |
| EPWM4_G3      | 500C 4790h       |
| EPWM5_G0      | 5000 5790h       |
| EPWM5_G1      | 5004 5790h       |
| EPWM5_G2      | 5008 5790h       |
| EPWM5_G3      | 500C 5790h       |
| EPWM6_G0      | 5000 6790h       |
| EPWM6_G1      | 5004 6790h       |
| EPWM6_G2      | 5008 6790h       |
| EPWM6_G3      | 500C 6790h       |
| EPWM7_G0      | 5000 7790h       |
| EPWM7_G1      | 5004 7790h       |
| EPWM7_G2      | 5008 7790h       |
| EPWM7_G3      | 500C 7790h       |
| EPWM8_G0      | 5000 8790h       |
| EPWM8_G1      | 5004 8790h       |
| EPWM8_G2      | 5008 8790h       |
| EPWM8_G3      | 500C 8790h       |
| EPWM9_G0      | 5000 9790h       |
| EPWM9_G1      | 5004 9790h       |
| EPWM9_G2      | 5008 9790h       |

**Table 3-1261. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9790h       |
| EPWM10_G0     | 5000 A790h       |
| EPWM10_G1     | 5004 A790h       |
| EPWM10_G2     | 5008 A790h       |
| EPWM10_G3     | 500C A790h       |
| EPWM11_G0     | 5000 B790h       |
| EPWM11_G1     | 5004 B790h       |
| EPWM11_G2     | 5008 B790h       |
| EPWM11_G3     | 500C B790h       |
| EPWM12_G0     | 5000 C790h       |
| EPWM12_G1     | 5004 C790h       |
| EPWM12_G2     | 5008 C790h       |
| EPWM12_G3     | 500C C790h       |
| EPWM13_G0     | 5000 D790h       |
| EPWM13_G1     | 5004 D790h       |
| EPWM13_G2     | 5008 D790h       |
| EPWM13_G3     | 500C D790h       |
| EPWM14_G0     | 5000 E790h       |
| EPWM14_G1     | 5004 E790h       |
| EPWM14_G2     | 5008 E790h       |
| EPWM14_G3     | 500C E790h       |
| EPWM15_G0     | 5000 F790h       |
| EPWM15_G1     | 5004 F790h       |
| EPWM15_G2     | 5008 F790h       |
| EPWM15_G3     | 500C F790h       |
| EPWM16_G0     | 5001 0790h       |
| EPWM16_G1     | 5005 0790h       |
| EPWM16_G2     | 5009 0790h       |
| EPWM16_G3     | 500D 0790h       |
| EPWM17_G0     | 5001 1790h       |
| EPWM17_G1     | 5005 1790h       |
| EPWM17_G2     | 5009 1790h       |
| EPWM17_G3     | 500D 1790h       |
| EPWM18_G0     | 5001 2790h       |
| EPWM18_G1     | 5005 2790h       |
| EPWM18_G2     | 5009 2790h       |
| EPWM18_G3     | 500D 2790h       |
| EPWM19_G0     | 5001 3790h       |
| EPWM19_G1     | 5005 3790h       |
| EPWM19_G2     | 5009 3790h       |
| EPWM19_G3     | 500D 3790h       |
| EPWM20_G0     | 5001 4790h       |
| EPWM20_G1     | 5005 4790h       |
| EPWM20_G2     | 5009 4790h       |
| EPWM20_G3     | 500D 4790h       |

**Table 3-1261. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5790h       |
| EPWM21_G1     | 5005 5790h       |
| EPWM21_G2     | 5009 5790h       |
| EPWM21_G3     | 500D 5790h       |
| EPWM22_G0     | 5001 6790h       |
| EPWM22_G1     | 5005 6790h       |
| EPWM22_G2     | 5009 6790h       |
| EPWM22_G3     | 500D 6790h       |
| EPWM23_G0     | 5001 7790h       |
| EPWM23_G1     | 5005 7790h       |
| EPWM23_G2     | 5009 7790h       |
| EPWM23_G3     | 500D 7790h       |
| EPWM24_G0     | 5001 8790h       |
| EPWM24_G1     | 5005 8790h       |
| EPWM24_G2     | 5009 8790h       |
| EPWM24_G3     | 500D 8790h       |
| EPWM25_G0     | 5001 9790h       |
| EPWM25_G1     | 5005 9790h       |
| EPWM25_G2     | 5009 9790h       |
| EPWM25_G3     | 500D 9790h       |
| EPWM26_G0     | 5001 A790h       |
| EPWM26_G1     | 5005 A790h       |
| EPWM26_G2     | 5009 A790h       |
| EPWM26_G3     | 500D A790h       |
| EPWM27_G0     | 5001 B790h       |
| EPWM27_G1     | 5005 B790h       |
| EPWM27_G2     | 5009 B790h       |
| EPWM27_G3     | 500D B790h       |
| EPWM28_G0     | 5001 C790h       |
| EPWM28_G1     | 5005 C790h       |
| EPWM28_G2     | 5009 C790h       |
| EPWM28_G3     | 500D C790h       |
| EPWM29_G0     | 5001 D790h       |
| EPWM29_G1     | 5005 D790h       |
| EPWM29_G2     | 5009 D790h       |
| EPWM29_G3     | 500D D790h       |
| EPWM30_G0     | 5001 E790h       |
| EPWM30_G1     | 5005 E790h       |
| EPWM30_G2     | 5009 E790h       |
| EPWM30_G3     | 500D E790h       |
| EPWM31_G0     | 5001 F790h       |
| EPWM31_G1     | 5005 F790h       |
| EPWM31_G2     | 5009 F790h       |
| EPWM31_G3     | 500D F790h       |

**Figure 3-401. EPWM\_XCMP5\_SHDW3 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP5_SHDW3   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP5_SHDW3   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP5HR_SHDW3 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP5HR_SHDW3 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 3-1263. EPWM\_XCMP5\_SHDW3 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                 |
|-------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP5_SHDW3   | R/W  | 0h    | XCMP5_SHDW3 Register<br>The value in the XCMP5_SHDW3 register is loaded into XCMP5_ACTIVE register when shadow to active load occurs.       |
| 15:0  | XCMP5HR_SHDW3 | R/W  | 0h    | XCMP5HR_SHDW3 Register<br>The value in the XCMP5HR_SHDW3 register is loaded into XCMP5HR_ACTIVE register when shadow to active load occurs. |

### 3.7.2.151 EPWM\_XCMP6\_SHDW3 Register

#### 1 EPWM\_XCMP6\_SHDW3 Register (Offset = 794h) [reset = 0h]

Additional Compare 6 Shadow 3 Register.

Return to [Summary Table](#)

**Table 3-1264. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0794h       |
| EPWM0_G1      | 5004 0794h       |
| EPWM0_G2      | 5008 0794h       |
| EPWM0_G3      | 500C 0794h       |
| EPWM1_G0      | 5000 1794h       |
| EPWM1_G1      | 5004 1794h       |
| EPWM1_G2      | 5008 1794h       |
| EPWM1_G3      | 500C 1794h       |
| EPWM2_G0      | 5000 2794h       |
| EPWM2_G1      | 5004 2794h       |
| EPWM2_G2      | 5008 2794h       |
| EPWM2_G3      | 500C 2794h       |
| EPWM3_G0      | 5000 3794h       |
| EPWM3_G1      | 5004 3794h       |
| EPWM3_G2      | 5008 3794h       |
| EPWM3_G3      | 500C 3794h       |
| EPWM4_G0      | 5000 4794h       |
| EPWM4_G1      | 5004 4794h       |
| EPWM4_G2      | 5008 4794h       |
| EPWM4_G3      | 500C 4794h       |
| EPWM5_G0      | 5000 5794h       |
| EPWM5_G1      | 5004 5794h       |
| EPWM5_G2      | 5008 5794h       |
| EPWM5_G3      | 500C 5794h       |
| EPWM6_G0      | 5000 6794h       |
| EPWM6_G1      | 5004 6794h       |
| EPWM6_G2      | 5008 6794h       |
| EPWM6_G3      | 500C 6794h       |
| EPWM7_G0      | 5000 7794h       |
| EPWM7_G1      | 5004 7794h       |
| EPWM7_G2      | 5008 7794h       |
| EPWM7_G3      | 500C 7794h       |
| EPWM8_G0      | 5000 8794h       |
| EPWM8_G1      | 5004 8794h       |
| EPWM8_G2      | 5008 8794h       |
| EPWM8_G3      | 500C 8794h       |
| EPWM9_G0      | 5000 9794h       |
| EPWM9_G1      | 5004 9794h       |
| EPWM9_G2      | 5008 9794h       |

**Table 3-1264. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9794h       |
| EPWM10_G0     | 5000 A794h       |
| EPWM10_G1     | 5004 A794h       |
| EPWM10_G2     | 5008 A794h       |
| EPWM10_G3     | 500C A794h       |
| EPWM11_G0     | 5000 B794h       |
| EPWM11_G1     | 5004 B794h       |
| EPWM11_G2     | 5008 B794h       |
| EPWM11_G3     | 500C B794h       |
| EPWM12_G0     | 5000 C794h       |
| EPWM12_G1     | 5004 C794h       |
| EPWM12_G2     | 5008 C794h       |
| EPWM12_G3     | 500C C794h       |
| EPWM13_G0     | 5000 D794h       |
| EPWM13_G1     | 5004 D794h       |
| EPWM13_G2     | 5008 D794h       |
| EPWM13_G3     | 500C D794h       |
| EPWM14_G0     | 5000 E794h       |
| EPWM14_G1     | 5004 E794h       |
| EPWM14_G2     | 5008 E794h       |
| EPWM14_G3     | 500C E794h       |
| EPWM15_G0     | 5000 F794h       |
| EPWM15_G1     | 5004 F794h       |
| EPWM15_G2     | 5008 F794h       |
| EPWM15_G3     | 500C F794h       |
| EPWM16_G0     | 5001 0794h       |
| EPWM16_G1     | 5005 0794h       |
| EPWM16_G2     | 5009 0794h       |
| EPWM16_G3     | 500D 0794h       |
| EPWM17_G0     | 5001 1794h       |
| EPWM17_G1     | 5005 1794h       |
| EPWM17_G2     | 5009 1794h       |
| EPWM17_G3     | 500D 1794h       |
| EPWM18_G0     | 5001 2794h       |
| EPWM18_G1     | 5005 2794h       |
| EPWM18_G2     | 5009 2794h       |
| EPWM18_G3     | 500D 2794h       |
| EPWM19_G0     | 5001 3794h       |
| EPWM19_G1     | 5005 3794h       |
| EPWM19_G2     | 5009 3794h       |
| EPWM19_G3     | 500D 3794h       |
| EPWM20_G0     | 5001 4794h       |
| EPWM20_G1     | 5005 4794h       |
| EPWM20_G2     | 5009 4794h       |
| EPWM20_G3     | 500D 4794h       |



**Table 3-1264. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5794h       |
| EPWM21_G1     | 5005 5794h       |
| EPWM21_G2     | 5009 5794h       |
| EPWM21_G3     | 500D 5794h       |
| EPWM22_G0     | 5001 6794h       |
| EPWM22_G1     | 5005 6794h       |
| EPWM22_G2     | 5009 6794h       |
| EPWM22_G3     | 500D 6794h       |
| EPWM23_G0     | 5001 7794h       |
| EPWM23_G1     | 5005 7794h       |
| EPWM23_G2     | 5009 7794h       |
| EPWM23_G3     | 500D 7794h       |
| EPWM24_G0     | 5001 8794h       |
| EPWM24_G1     | 5005 8794h       |
| EPWM24_G2     | 5009 8794h       |
| EPWM24_G3     | 500D 8794h       |
| EPWM25_G0     | 5001 9794h       |
| EPWM25_G1     | 5005 9794h       |
| EPWM25_G2     | 5009 9794h       |
| EPWM25_G3     | 500D 9794h       |
| EPWM26_G0     | 5001 A794h       |
| EPWM26_G1     | 5005 A794h       |
| EPWM26_G2     | 5009 A794h       |
| EPWM26_G3     | 500D A794h       |
| EPWM27_G0     | 5001 B794h       |
| EPWM27_G1     | 5005 B794h       |
| EPWM27_G2     | 5009 B794h       |
| EPWM27_G3     | 500D B794h       |
| EPWM28_G0     | 5001 C794h       |
| EPWM28_G1     | 5005 C794h       |
| EPWM28_G2     | 5009 C794h       |
| EPWM28_G3     | 500D C794h       |
| EPWM29_G0     | 5001 D794h       |
| EPWM29_G1     | 5005 D794h       |
| EPWM29_G2     | 5009 D794h       |
| EPWM29_G3     | 500D D794h       |
| EPWM30_G0     | 5001 E794h       |
| EPWM30_G1     | 5005 E794h       |
| EPWM30_G2     | 5009 E794h       |
| EPWM30_G3     | 500D E794h       |
| EPWM31_G0     | 5001 F794h       |
| EPWM31_G1     | 5005 F794h       |
| EPWM31_G2     | 5009 F794h       |
| EPWM31_G3     | 500D F794h       |

**Figure 3-402. EPWM\_XCMP6\_SHDW3 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP6_SHDW3   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP6_SHDW3   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP6HR_SHDW3 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP6HR_SHDW3 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 3-1266. EPWM\_XCMP6\_SHDW3 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                 |
|-------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP6_SHDW3   | R/W  | 0h    | XCMP6_SHDW3 Register<br>The value in the XCMP6_SHDW3 register is loaded into XCMP6_ACTIVE register when shadow to active load occurs.       |
| 15:0  | XCMP6HR_SHDW3 | R/W  | 0h    | XCMP6HR_SHDW3 Register<br>The value in the XCMP6HR_SHDW3 register is loaded into XCMP6HR_ACTIVE register when shadow to active load occurs. |

### 3.7.2.152 EPWM\_XCMP7\_SHDW3 Register

#### 1 EPWM\_XCMP7\_SHDW3 Register (Offset = 798h) [reset = 0h]

Additional Compare 7 Shadow 3 Register.

Return to [Summary Table](#)

**Table 3-1267. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0798h       |
| EPWM0_G1      | 5004 0798h       |
| EPWM0_G2      | 5008 0798h       |
| EPWM0_G3      | 500C 0798h       |
| EPWM1_G0      | 5000 1798h       |
| EPWM1_G1      | 5004 1798h       |
| EPWM1_G2      | 5008 1798h       |
| EPWM1_G3      | 500C 1798h       |
| EPWM2_G0      | 5000 2798h       |
| EPWM2_G1      | 5004 2798h       |
| EPWM2_G2      | 5008 2798h       |
| EPWM2_G3      | 500C 2798h       |
| EPWM3_G0      | 5000 3798h       |
| EPWM3_G1      | 5004 3798h       |
| EPWM3_G2      | 5008 3798h       |
| EPWM3_G3      | 500C 3798h       |
| EPWM4_G0      | 5000 4798h       |
| EPWM4_G1      | 5004 4798h       |
| EPWM4_G2      | 5008 4798h       |
| EPWM4_G3      | 500C 4798h       |
| EPWM5_G0      | 5000 5798h       |
| EPWM5_G1      | 5004 5798h       |
| EPWM5_G2      | 5008 5798h       |
| EPWM5_G3      | 500C 5798h       |
| EPWM6_G0      | 5000 6798h       |
| EPWM6_G1      | 5004 6798h       |
| EPWM6_G2      | 5008 6798h       |
| EPWM6_G3      | 500C 6798h       |
| EPWM7_G0      | 5000 7798h       |
| EPWM7_G1      | 5004 7798h       |
| EPWM7_G2      | 5008 7798h       |
| EPWM7_G3      | 500C 7798h       |
| EPWM8_G0      | 5000 8798h       |
| EPWM8_G1      | 5004 8798h       |
| EPWM8_G2      | 5008 8798h       |
| EPWM8_G3      | 500C 8798h       |
| EPWM9_G0      | 5000 9798h       |
| EPWM9_G1      | 5004 9798h       |
| EPWM9_G2      | 5008 9798h       |

**Table 3-1267. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9798h       |
| EPWM10_G0     | 5000 A798h       |
| EPWM10_G1     | 5004 A798h       |
| EPWM10_G2     | 5008 A798h       |
| EPWM10_G3     | 500C A798h       |
| EPWM11_G0     | 5000 B798h       |
| EPWM11_G1     | 5004 B798h       |
| EPWM11_G2     | 5008 B798h       |
| EPWM11_G3     | 500C B798h       |
| EPWM12_G0     | 5000 C798h       |
| EPWM12_G1     | 5004 C798h       |
| EPWM12_G2     | 5008 C798h       |
| EPWM12_G3     | 500C C798h       |
| EPWM13_G0     | 5000 D798h       |
| EPWM13_G1     | 5004 D798h       |
| EPWM13_G2     | 5008 D798h       |
| EPWM13_G3     | 500C D798h       |
| EPWM14_G0     | 5000 E798h       |
| EPWM14_G1     | 5004 E798h       |
| EPWM14_G2     | 5008 E798h       |
| EPWM14_G3     | 500C E798h       |
| EPWM15_G0     | 5000 F798h       |
| EPWM15_G1     | 5004 F798h       |
| EPWM15_G2     | 5008 F798h       |
| EPWM15_G3     | 500C F798h       |
| EPWM16_G0     | 5001 0798h       |
| EPWM16_G1     | 5005 0798h       |
| EPWM16_G2     | 5009 0798h       |
| EPWM16_G3     | 500D 0798h       |
| EPWM17_G0     | 5001 1798h       |
| EPWM17_G1     | 5005 1798h       |
| EPWM17_G2     | 5009 1798h       |
| EPWM17_G3     | 500D 1798h       |
| EPWM18_G0     | 5001 2798h       |
| EPWM18_G1     | 5005 2798h       |
| EPWM18_G2     | 5009 2798h       |
| EPWM18_G3     | 500D 2798h       |
| EPWM19_G0     | 5001 3798h       |
| EPWM19_G1     | 5005 3798h       |
| EPWM19_G2     | 5009 3798h       |
| EPWM19_G3     | 500D 3798h       |
| EPWM20_G0     | 5001 4798h       |
| EPWM20_G1     | 5005 4798h       |
| EPWM20_G2     | 5009 4798h       |
| EPWM20_G3     | 500D 4798h       |

**Table 3-1267. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5798h       |
| EPWM21_G1     | 5005 5798h       |
| EPWM21_G2     | 5009 5798h       |
| EPWM21_G3     | 500D 5798h       |
| EPWM22_G0     | 5001 6798h       |
| EPWM22_G1     | 5005 6798h       |
| EPWM22_G2     | 5009 6798h       |
| EPWM22_G3     | 500D 6798h       |
| EPWM23_G0     | 5001 7798h       |
| EPWM23_G1     | 5005 7798h       |
| EPWM23_G2     | 5009 7798h       |
| EPWM23_G3     | 500D 7798h       |
| EPWM24_G0     | 5001 8798h       |
| EPWM24_G1     | 5005 8798h       |
| EPWM24_G2     | 5009 8798h       |
| EPWM24_G3     | 500D 8798h       |
| EPWM25_G0     | 5001 9798h       |
| EPWM25_G1     | 5005 9798h       |
| EPWM25_G2     | 5009 9798h       |
| EPWM25_G3     | 500D 9798h       |
| EPWM26_G0     | 5001 A798h       |
| EPWM26_G1     | 5005 A798h       |
| EPWM26_G2     | 5009 A798h       |
| EPWM26_G3     | 500D A798h       |
| EPWM27_G0     | 5001 B798h       |
| EPWM27_G1     | 5005 B798h       |
| EPWM27_G2     | 5009 B798h       |
| EPWM27_G3     | 500D B798h       |
| EPWM28_G0     | 5001 C798h       |
| EPWM28_G1     | 5005 C798h       |
| EPWM28_G2     | 5009 C798h       |
| EPWM28_G3     | 500D C798h       |
| EPWM29_G0     | 5001 D798h       |
| EPWM29_G1     | 5005 D798h       |
| EPWM29_G2     | 5009 D798h       |
| EPWM29_G3     | 500D D798h       |
| EPWM30_G0     | 5001 E798h       |
| EPWM30_G1     | 5005 E798h       |
| EPWM30_G2     | 5009 E798h       |
| EPWM30_G3     | 500D E798h       |
| EPWM31_G0     | 5001 F798h       |
| EPWM31_G1     | 5005 F798h       |
| EPWM31_G2     | 5009 F798h       |
| EPWM31_G3     | 500D F798h       |

**Figure 3-403. EPWM\_XCMP7\_SHDW3 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP7_SHDW3   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP7_SHDW3   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP7HR_SHDW3 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP7HR_SHDW3 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 3-1269. EPWM\_XCMP7\_SHDW3 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                 |
|-------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP7_SHDW3   | R/W  | 0h    | XCMP7_SHDW3 Register<br>The value in the XCMP7_SHDW3 register is loaded into XCMP7_ACTIVE register when shadow to active load occurs.       |
| 15:0  | XCMP7HR_SHDW3 | R/W  | 0h    | XCMP7HR_SHDW3 Register<br>The value in the XCMP7HR_SHDW3 register is loaded into XCMP7HR_ACTIVE register when shadow to active load occurs. |

### 3.7.2.153 EPWM\_XCMP8\_SHDW3 Register

#### 1 EPWM\_XCMP8\_SHDW3 Register (Offset = 79Ch) [reset = 0h]

Additional Compare 8 Shadow 3 Register.

Return to [Summary Table](#)

**Table 3-1270. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 079Ch       |
| EPWM0_G1      | 5004 079Ch       |
| EPWM0_G2      | 5008 079Ch       |
| EPWM0_G3      | 500C 079Ch       |
| EPWM1_G0      | 5000 179Ch       |
| EPWM1_G1      | 5004 179Ch       |
| EPWM1_G2      | 5008 179Ch       |
| EPWM1_G3      | 500C 179Ch       |
| EPWM2_G0      | 5000 279Ch       |
| EPWM2_G1      | 5004 279Ch       |
| EPWM2_G2      | 5008 279Ch       |
| EPWM2_G3      | 500C 279Ch       |
| EPWM3_G0      | 5000 379Ch       |
| EPWM3_G1      | 5004 379Ch       |
| EPWM3_G2      | 5008 379Ch       |
| EPWM3_G3      | 500C 379Ch       |
| EPWM4_G0      | 5000 479Ch       |
| EPWM4_G1      | 5004 479Ch       |
| EPWM4_G2      | 5008 479Ch       |
| EPWM4_G3      | 500C 479Ch       |
| EPWM5_G0      | 5000 579Ch       |
| EPWM5_G1      | 5004 579Ch       |
| EPWM5_G2      | 5008 579Ch       |
| EPWM5_G3      | 500C 579Ch       |
| EPWM6_G0      | 5000 679Ch       |
| EPWM6_G1      | 5004 679Ch       |
| EPWM6_G2      | 5008 679Ch       |
| EPWM6_G3      | 500C 679Ch       |
| EPWM7_G0      | 5000 779Ch       |
| EPWM7_G1      | 5004 779Ch       |
| EPWM7_G2      | 5008 779Ch       |
| EPWM7_G3      | 500C 779Ch       |
| EPWM8_G0      | 5000 879Ch       |
| EPWM8_G1      | 5004 879Ch       |
| EPWM8_G2      | 5008 879Ch       |
| EPWM8_G3      | 500C 879Ch       |
| EPWM9_G0      | 5000 979Ch       |
| EPWM9_G1      | 5004 979Ch       |
| EPWM9_G2      | 5008 979Ch       |

**Table 3-1270. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 979Ch       |
| EPWM10_G0     | 5000 A79Ch       |
| EPWM10_G1     | 5004 A79Ch       |
| EPWM10_G2     | 5008 A79Ch       |
| EPWM10_G3     | 500C A79Ch       |
| EPWM11_G0     | 5000 B79Ch       |
| EPWM11_G1     | 5004 B79Ch       |
| EPWM11_G2     | 5008 B79Ch       |
| EPWM11_G3     | 500C B79Ch       |
| EPWM12_G0     | 5000 C79Ch       |
| EPWM12_G1     | 5004 C79Ch       |
| EPWM12_G2     | 5008 C79Ch       |
| EPWM12_G3     | 500C C79Ch       |
| EPWM13_G0     | 5000 D79Ch       |
| EPWM13_G1     | 5004 D79Ch       |
| EPWM13_G2     | 5008 D79Ch       |
| EPWM13_G3     | 500C D79Ch       |
| EPWM14_G0     | 5000 E79Ch       |
| EPWM14_G1     | 5004 E79Ch       |
| EPWM14_G2     | 5008 E79Ch       |
| EPWM14_G3     | 500C E79Ch       |
| EPWM15_G0     | 5000 F79Ch       |
| EPWM15_G1     | 5004 F79Ch       |
| EPWM15_G2     | 5008 F79Ch       |
| EPWM15_G3     | 500C F79Ch       |
| EPWM16_G0     | 5001 079Ch       |
| EPWM16_G1     | 5005 079Ch       |
| EPWM16_G2     | 5009 079Ch       |
| EPWM16_G3     | 500D 079Ch       |
| EPWM17_G0     | 5001 179Ch       |
| EPWM17_G1     | 5005 179Ch       |
| EPWM17_G2     | 5009 179Ch       |
| EPWM17_G3     | 500D 179Ch       |
| EPWM18_G0     | 5001 279Ch       |
| EPWM18_G1     | 5005 279Ch       |
| EPWM18_G2     | 5009 279Ch       |
| EPWM18_G3     | 500D 279Ch       |
| EPWM19_G0     | 5001 379Ch       |
| EPWM19_G1     | 5005 379Ch       |
| EPWM19_G2     | 5009 379Ch       |
| EPWM19_G3     | 500D 379Ch       |
| EPWM20_G0     | 5001 479Ch       |
| EPWM20_G1     | 5005 479Ch       |
| EPWM20_G2     | 5009 479Ch       |
| EPWM20_G3     | 500D 479Ch       |



**Table 3-1270. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 579Ch       |
| EPWM21_G1     | 5005 579Ch       |
| EPWM21_G2     | 5009 579Ch       |
| EPWM21_G3     | 500D 579Ch       |
| EPWM22_G0     | 5001 679Ch       |
| EPWM22_G1     | 5005 679Ch       |
| EPWM22_G2     | 5009 679Ch       |
| EPWM22_G3     | 500D 679Ch       |
| EPWM23_G0     | 5001 779Ch       |
| EPWM23_G1     | 5005 779Ch       |
| EPWM23_G2     | 5009 779Ch       |
| EPWM23_G3     | 500D 779Ch       |
| EPWM24_G0     | 5001 879Ch       |
| EPWM24_G1     | 5005 879Ch       |
| EPWM24_G2     | 5009 879Ch       |
| EPWM24_G3     | 500D 879Ch       |
| EPWM25_G0     | 5001 979Ch       |
| EPWM25_G1     | 5005 979Ch       |
| EPWM25_G2     | 5009 979Ch       |
| EPWM25_G3     | 500D 979Ch       |
| EPWM26_G0     | 5001 A79Ch       |
| EPWM26_G1     | 5005 A79Ch       |
| EPWM26_G2     | 5009 A79Ch       |
| EPWM26_G3     | 500D A79Ch       |
| EPWM27_G0     | 5001 B79Ch       |
| EPWM27_G1     | 5005 B79Ch       |
| EPWM27_G2     | 5009 B79Ch       |
| EPWM27_G3     | 500D B79Ch       |
| EPWM28_G0     | 5001 C79Ch       |
| EPWM28_G1     | 5005 C79Ch       |
| EPWM28_G2     | 5009 C79Ch       |
| EPWM28_G3     | 500D C79Ch       |
| EPWM29_G0     | 5001 D79Ch       |
| EPWM29_G1     | 5005 D79Ch       |
| EPWM29_G2     | 5009 D79Ch       |
| EPWM29_G3     | 500D D79Ch       |
| EPWM30_G0     | 5001 E79Ch       |
| EPWM30_G1     | 5005 E79Ch       |
| EPWM30_G2     | 5009 E79Ch       |
| EPWM30_G3     | 500D E79Ch       |
| EPWM31_G0     | 5001 F79Ch       |
| EPWM31_G1     | 5005 F79Ch       |
| EPWM31_G2     | 5009 F79Ch       |
| EPWM31_G3     | 500D F79Ch       |

**Figure 3-404. EPWM\_XCMP8\_SHDW3 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XCMP8_SHDW3   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XCMP8_SHDW3   |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XCMP8HR_SHDW3 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XCMP8HR_SHDW3 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 3-1272. EPWM\_XCMP8\_SHDW3 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                 |
|-------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | XCMP8_SHDW3   | R/W  | 0h    | XCMP8_SHDW3 Register<br>The value in the XCMP8_SHDW3 register is loaded into XCMP8_ACTIVE register when shadow to active load occurs.       |
| 15:0  | XCMP8HR_SHDW3 | R/W  | 0h    | XCMP8HR_SHDW3 Register<br>The value in the XCMP8HR_SHDW3 register is loaded into XCMP8HR_ACTIVE register when shadow to active load occurs. |

### 3.7.2.154 EPWM\_XTBPRD\_SHDW3 Register

#### 1 EPWM\_XTBPRD\_SHDW3 Register (Offset = 7A0h) [reset = 0h]

Additional Time Base Period Shadow 3 Register.

Return to [Summary Table](#)

**Table 3-1273. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 07A0h       |
| EPWM0_G1      | 5004 07A0h       |
| EPWM0_G2      | 5008 07A0h       |
| EPWM0_G3      | 500C 07A0h       |
| EPWM1_G0      | 5000 17A0h       |
| EPWM1_G1      | 5004 17A0h       |
| EPWM1_G2      | 5008 17A0h       |
| EPWM1_G3      | 500C 17A0h       |
| EPWM2_G0      | 5000 27A0h       |
| EPWM2_G1      | 5004 27A0h       |
| EPWM2_G2      | 5008 27A0h       |
| EPWM2_G3      | 500C 27A0h       |
| EPWM3_G0      | 5000 37A0h       |
| EPWM3_G1      | 5004 37A0h       |
| EPWM3_G2      | 5008 37A0h       |
| EPWM3_G3      | 500C 37A0h       |
| EPWM4_G0      | 5000 47A0h       |
| EPWM4_G1      | 5004 47A0h       |
| EPWM4_G2      | 5008 47A0h       |
| EPWM4_G3      | 500C 47A0h       |
| EPWM5_G0      | 5000 57A0h       |
| EPWM5_G1      | 5004 57A0h       |
| EPWM5_G2      | 5008 57A0h       |
| EPWM5_G3      | 500C 57A0h       |
| EPWM6_G0      | 5000 67A0h       |
| EPWM6_G1      | 5004 67A0h       |
| EPWM6_G2      | 5008 67A0h       |
| EPWM6_G3      | 500C 67A0h       |
| EPWM7_G0      | 5000 77A0h       |
| EPWM7_G1      | 5004 77A0h       |
| EPWM7_G2      | 5008 77A0h       |
| EPWM7_G3      | 500C 77A0h       |
| EPWM8_G0      | 5000 87A0h       |
| EPWM8_G1      | 5004 87A0h       |
| EPWM8_G2      | 5008 87A0h       |
| EPWM8_G3      | 500C 87A0h       |
| EPWM9_G0      | 5000 97A0h       |
| EPWM9_G1      | 5004 97A0h       |
| EPWM9_G2      | 5008 97A0h       |

**Table 3-1273. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 97A0h       |
| EPWM10_G0     | 5000 A7A0h       |
| EPWM10_G1     | 5004 A7A0h       |
| EPWM10_G2     | 5008 A7A0h       |
| EPWM10_G3     | 500C A7A0h       |
| EPWM11_G0     | 5000 B7A0h       |
| EPWM11_G1     | 5004 B7A0h       |
| EPWM11_G2     | 5008 B7A0h       |
| EPWM11_G3     | 500C B7A0h       |
| EPWM12_G0     | 5000 C7A0h       |
| EPWM12_G1     | 5004 C7A0h       |
| EPWM12_G2     | 5008 C7A0h       |
| EPWM12_G3     | 500C C7A0h       |
| EPWM13_G0     | 5000 D7A0h       |
| EPWM13_G1     | 5004 D7A0h       |
| EPWM13_G2     | 5008 D7A0h       |
| EPWM13_G3     | 500C D7A0h       |
| EPWM14_G0     | 5000 E7A0h       |
| EPWM14_G1     | 5004 E7A0h       |
| EPWM14_G2     | 5008 E7A0h       |
| EPWM14_G3     | 500C E7A0h       |
| EPWM15_G0     | 5000 F7A0h       |
| EPWM15_G1     | 5004 F7A0h       |
| EPWM15_G2     | 5008 F7A0h       |
| EPWM15_G3     | 500C F7A0h       |
| EPWM16_G0     | 5001 07A0h       |
| EPWM16_G1     | 5005 07A0h       |
| EPWM16_G2     | 5009 07A0h       |
| EPWM16_G3     | 500D 07A0h       |
| EPWM17_G0     | 5001 17A0h       |
| EPWM17_G1     | 5005 17A0h       |
| EPWM17_G2     | 5009 17A0h       |
| EPWM17_G3     | 500D 17A0h       |
| EPWM18_G0     | 5001 27A0h       |
| EPWM18_G1     | 5005 27A0h       |
| EPWM18_G2     | 5009 27A0h       |
| EPWM18_G3     | 500D 27A0h       |
| EPWM19_G0     | 5001 37A0h       |
| EPWM19_G1     | 5005 37A0h       |
| EPWM19_G2     | 5009 37A0h       |
| EPWM19_G3     | 500D 37A0h       |
| EPWM20_G0     | 5001 47A0h       |
| EPWM20_G1     | 5005 47A0h       |
| EPWM20_G2     | 5009 47A0h       |
| EPWM20_G3     | 500D 47A0h       |

**Table 3-1273. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 57A0h       |
| EPWM21_G1     | 5005 57A0h       |
| EPWM21_G2     | 5009 57A0h       |
| EPWM21_G3     | 500D 57A0h       |
| EPWM22_G0     | 5001 67A0h       |
| EPWM22_G1     | 5005 67A0h       |
| EPWM22_G2     | 5009 67A0h       |
| EPWM22_G3     | 500D 67A0h       |
| EPWM23_G0     | 5001 77A0h       |
| EPWM23_G1     | 5005 77A0h       |
| EPWM23_G2     | 5009 77A0h       |
| EPWM23_G3     | 500D 77A0h       |
| EPWM24_G0     | 5001 87A0h       |
| EPWM24_G1     | 5005 87A0h       |
| EPWM24_G2     | 5009 87A0h       |
| EPWM24_G3     | 500D 87A0h       |
| EPWM25_G0     | 5001 97A0h       |
| EPWM25_G1     | 5005 97A0h       |
| EPWM25_G2     | 5009 97A0h       |
| EPWM25_G3     | 500D 97A0h       |
| EPWM26_G0     | 5001 A7A0h       |
| EPWM26_G1     | 5005 A7A0h       |
| EPWM26_G2     | 5009 A7A0h       |
| EPWM26_G3     | 500D A7A0h       |
| EPWM27_G0     | 5001 B7A0h       |
| EPWM27_G1     | 5005 B7A0h       |
| EPWM27_G2     | 5009 B7A0h       |
| EPWM27_G3     | 500D B7A0h       |
| EPWM28_G0     | 5001 C7A0h       |
| EPWM28_G1     | 5005 C7A0h       |
| EPWM28_G2     | 5009 C7A0h       |
| EPWM28_G3     | 500D C7A0h       |
| EPWM29_G0     | 5001 D7A0h       |
| EPWM29_G1     | 5005 D7A0h       |
| EPWM29_G2     | 5009 D7A0h       |
| EPWM29_G3     | 500D D7A0h       |
| EPWM30_G0     | 5001 E7A0h       |
| EPWM30_G1     | 5005 E7A0h       |
| EPWM30_G2     | 5009 E7A0h       |
| EPWM30_G3     | 500D E7A0h       |
| EPWM31_G0     | 5001 F7A0h       |
| EPWM31_G1     | 5005 F7A0h       |
| EPWM31_G2     | 5009 F7A0h       |
| EPWM31_G3     | 500D F7A0h       |

**Figure 3-405. EPWM\_XTBPRD\_SHDW3 Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XTBPRD_SHDW3   |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XTBPRD_SHDW3   |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XTBPRDHR_SHDW3 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XTBPRDHR_SHDW3 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 3-1275. EPWM\_XTBPRD\_SHDW3 Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                         |
|-------|----------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:16 | XTBPRD_SHDW3   | R/W  | 0h    | The value in the XTBPRD_SHDW3 register is loaded into XTBPRD_ACTIVE register when shadow to active load occurs.     |
| 15:0  | XTBPRDHR_SHDW3 | R/W  | 0h    | The value in the XTBPRDHR_SHDW3 register is loaded into XTBPRDHR_ACTIVE register when shadow to active load occurs. |

### 3.7.2.155 EPWM\_XAQCTLA\_SHDW3 Register

#### 1 EPWM\_XAQCTLA\_SHDW3 Register (Offset = 7B0h) [reset = 0h]

XAQCTLA Shadow 3 Register.

Return to [Summary Table](#)

**Table 3-1276. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 07B0h       |
| EPWM0_G1      | 5004 07B0h       |
| EPWM0_G2      | 5008 07B0h       |
| EPWM0_G3      | 500C 07B0h       |
| EPWM1_G0      | 5000 17B0h       |
| EPWM1_G1      | 5004 17B0h       |
| EPWM1_G2      | 5008 17B0h       |
| EPWM1_G3      | 500C 17B0h       |
| EPWM2_G0      | 5000 27B0h       |
| EPWM2_G1      | 5004 27B0h       |
| EPWM2_G2      | 5008 27B0h       |
| EPWM2_G3      | 500C 27B0h       |
| EPWM3_G0      | 5000 37B0h       |
| EPWM3_G1      | 5004 37B0h       |
| EPWM3_G2      | 5008 37B0h       |
| EPWM3_G3      | 500C 37B0h       |
| EPWM4_G0      | 5000 47B0h       |
| EPWM4_G1      | 5004 47B0h       |
| EPWM4_G2      | 5008 47B0h       |
| EPWM4_G3      | 500C 47B0h       |
| EPWM5_G0      | 5000 57B0h       |
| EPWM5_G1      | 5004 57B0h       |
| EPWM5_G2      | 5008 57B0h       |
| EPWM5_G3      | 500C 57B0h       |
| EPWM6_G0      | 5000 67B0h       |
| EPWM6_G1      | 5004 67B0h       |
| EPWM6_G2      | 5008 67B0h       |
| EPWM6_G3      | 500C 67B0h       |
| EPWM7_G0      | 5000 77B0h       |
| EPWM7_G1      | 5004 77B0h       |
| EPWM7_G2      | 5008 77B0h       |
| EPWM7_G3      | 500C 77B0h       |
| EPWM8_G0      | 5000 87B0h       |
| EPWM8_G1      | 5004 87B0h       |
| EPWM8_G2      | 5008 87B0h       |
| EPWM8_G3      | 500C 87B0h       |
| EPWM9_G0      | 5000 97B0h       |
| EPWM9_G1      | 5004 97B0h       |
| EPWM9_G2      | 5008 97B0h       |

**Table 3-1276. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 97B0h       |
| EPWM10_G0     | 5000 A7B0h       |
| EPWM10_G1     | 5004 A7B0h       |
| EPWM10_G2     | 5008 A7B0h       |
| EPWM10_G3     | 500C A7B0h       |
| EPWM11_G0     | 5000 B7B0h       |
| EPWM11_G1     | 5004 B7B0h       |
| EPWM11_G2     | 5008 B7B0h       |
| EPWM11_G3     | 500C B7B0h       |
| EPWM12_G0     | 5000 C7B0h       |
| EPWM12_G1     | 5004 C7B0h       |
| EPWM12_G2     | 5008 C7B0h       |
| EPWM12_G3     | 500C C7B0h       |
| EPWM13_G0     | 5000 D7B0h       |
| EPWM13_G1     | 5004 D7B0h       |
| EPWM13_G2     | 5008 D7B0h       |
| EPWM13_G3     | 500C D7B0h       |
| EPWM14_G0     | 5000 E7B0h       |
| EPWM14_G1     | 5004 E7B0h       |
| EPWM14_G2     | 5008 E7B0h       |
| EPWM14_G3     | 500C E7B0h       |
| EPWM15_G0     | 5000 F7B0h       |
| EPWM15_G1     | 5004 F7B0h       |
| EPWM15_G2     | 5008 F7B0h       |
| EPWM15_G3     | 500C F7B0h       |
| EPWM16_G0     | 5001 07B0h       |
| EPWM16_G1     | 5005 07B0h       |
| EPWM16_G2     | 5009 07B0h       |
| EPWM16_G3     | 500D 07B0h       |
| EPWM17_G0     | 5001 17B0h       |
| EPWM17_G1     | 5005 17B0h       |
| EPWM17_G2     | 5009 17B0h       |
| EPWM17_G3     | 500D 17B0h       |
| EPWM18_G0     | 5001 27B0h       |
| EPWM18_G1     | 5005 27B0h       |
| EPWM18_G2     | 5009 27B0h       |
| EPWM18_G3     | 500D 27B0h       |
| EPWM19_G0     | 5001 37B0h       |
| EPWM19_G1     | 5005 37B0h       |
| EPWM19_G2     | 5009 37B0h       |
| EPWM19_G3     | 500D 37B0h       |
| EPWM20_G0     | 5001 47B0h       |
| EPWM20_G1     | 5005 47B0h       |
| EPWM20_G2     | 5009 47B0h       |
| EPWM20_G3     | 500D 47B0h       |



**Table 3-1276. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 57B0h       |
| EPWM21_G1     | 5005 57B0h       |
| EPWM21_G2     | 5009 57B0h       |
| EPWM21_G3     | 500D 57B0h       |
| EPWM22_G0     | 5001 67B0h       |
| EPWM22_G1     | 5005 67B0h       |
| EPWM22_G2     | 5009 67B0h       |
| EPWM22_G3     | 500D 67B0h       |
| EPWM23_G0     | 5001 77B0h       |
| EPWM23_G1     | 5005 77B0h       |
| EPWM23_G2     | 5009 77B0h       |
| EPWM23_G3     | 500D 77B0h       |
| EPWM24_G0     | 5001 87B0h       |
| EPWM24_G1     | 5005 87B0h       |
| EPWM24_G2     | 5009 87B0h       |
| EPWM24_G3     | 500D 87B0h       |
| EPWM25_G0     | 5001 97B0h       |
| EPWM25_G1     | 5005 97B0h       |
| EPWM25_G2     | 5009 97B0h       |
| EPWM25_G3     | 500D 97B0h       |
| EPWM26_G0     | 5001 A7B0h       |
| EPWM26_G1     | 5005 A7B0h       |
| EPWM26_G2     | 5009 A7B0h       |
| EPWM26_G3     | 500D A7B0h       |
| EPWM27_G0     | 5001 B7B0h       |
| EPWM27_G1     | 5005 B7B0h       |
| EPWM27_G2     | 5009 B7B0h       |
| EPWM27_G3     | 500D B7B0h       |
| EPWM28_G0     | 5001 C7B0h       |
| EPWM28_G1     | 5005 C7B0h       |
| EPWM28_G2     | 5009 C7B0h       |
| EPWM28_G3     | 500D C7B0h       |
| EPWM29_G0     | 5001 D7B0h       |
| EPWM29_G1     | 5005 D7B0h       |
| EPWM29_G2     | 5009 D7B0h       |
| EPWM29_G3     | 500D D7B0h       |
| EPWM30_G0     | 5001 E7B0h       |
| EPWM30_G1     | 5005 E7B0h       |
| EPWM30_G2     | 5009 E7B0h       |
| EPWM30_G3     | 500D E7B0h       |
| EPWM31_G0     | 5001 F7B0h       |
| EPWM31_G1     | 5005 F7B0h       |
| EPWM31_G2     | 5009 F7B0h       |
| EPWM31_G3     | 500D F7B0h       |

**Figure 3-406. EPWM\_XAQCTLA\_SHDW3 Name Register**

| 15    | 14 | 13    | 12 | 11    | 10 | 9     | 8 |
|-------|----|-------|----|-------|----|-------|---|
| XCMP8 |    | XCMP7 |    | XCMP6 |    | XCMP5 |   |
| R/W   |    | R/W   |    | R/W   |    | R/W   |   |
| 0h    |    | 0h    |    | 0h    |    | 0h    |   |
| 7     | 6  | 5     | 4  | 3     | 2  | 1     | 0 |
| XCMP4 |    | XCMP3 |    | XCMP2 |    | XCMP1 |   |
| R/W   |    | R/W   |    | R/W   |    | R/W   |   |
| 0h    |    | 0h    |    | 0h    |    | 0h    |   |

**Table 3-1278. EPWM\_XAQCTLA\_SHDW3 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                          |
|-------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | XCMP8 | R/W  | 0h    | Action when Counter = CMP8<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 13:12 | XCMP7 | R/W  | 0h    | Action when Counter = CMP7<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 11:10 | XCMP6 | R/W  | 0h    | Action when Counter = CMP6<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 9:8   | XCMP5 | R/W  | 0h    | Action when Counter = CMP5<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 7:6   | XCMP4 | R/W  | 0h    | Action when Counter = CMP4<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 5:4   | XCMP3 | R/W  | 0h    | Action when Counter = CMP3<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 3:2   | XCMP2 | R/W  | 0h    | Action when Counter = CMP2<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 1:0   | XCMP1 | R/W  | 0h    | Action when Counter = CMP1<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |

### 3.7.2.156 EPWM\_XAQCTLB\_SHDW3 Register

#### 1 EPWM\_XAQCTLB\_SHDW3 Register (Offset = 7B2h) [reset = 0h]

XAQCTLB Shadow 3 Register.

Return to [Summary Table](#)

**Table 3-1279. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 07B2h       |
| EPWM0_G1      | 5004 07B2h       |
| EPWM0_G2      | 5008 07B2h       |
| EPWM0_G3      | 500C 07B2h       |
| EPWM1_G0      | 5000 17B2h       |
| EPWM1_G1      | 5004 17B2h       |
| EPWM1_G2      | 5008 17B2h       |
| EPWM1_G3      | 500C 17B2h       |
| EPWM2_G0      | 5000 27B2h       |
| EPWM2_G1      | 5004 27B2h       |
| EPWM2_G2      | 5008 27B2h       |
| EPWM2_G3      | 500C 27B2h       |
| EPWM3_G0      | 5000 37B2h       |
| EPWM3_G1      | 5004 37B2h       |
| EPWM3_G2      | 5008 37B2h       |
| EPWM3_G3      | 500C 37B2h       |
| EPWM4_G0      | 5000 47B2h       |
| EPWM4_G1      | 5004 47B2h       |
| EPWM4_G2      | 5008 47B2h       |
| EPWM4_G3      | 500C 47B2h       |
| EPWM5_G0      | 5000 57B2h       |
| EPWM5_G1      | 5004 57B2h       |
| EPWM5_G2      | 5008 57B2h       |
| EPWM5_G3      | 500C 57B2h       |
| EPWM6_G0      | 5000 67B2h       |
| EPWM6_G1      | 5004 67B2h       |
| EPWM6_G2      | 5008 67B2h       |
| EPWM6_G3      | 500C 67B2h       |
| EPWM7_G0      | 5000 77B2h       |
| EPWM7_G1      | 5004 77B2h       |
| EPWM7_G2      | 5008 77B2h       |
| EPWM7_G3      | 500C 77B2h       |
| EPWM8_G0      | 5000 87B2h       |
| EPWM8_G1      | 5004 87B2h       |
| EPWM8_G2      | 5008 87B2h       |
| EPWM8_G3      | 500C 87B2h       |
| EPWM9_G0      | 5000 97B2h       |
| EPWM9_G1      | 5004 97B2h       |
| EPWM9_G2      | 5008 97B2h       |

**Table 3-1279. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 97B2h       |
| EPWM10_G0     | 5000 A7B2h       |
| EPWM10_G1     | 5004 A7B2h       |
| EPWM10_G2     | 5008 A7B2h       |
| EPWM10_G3     | 500C A7B2h       |
| EPWM11_G0     | 5000 B7B2h       |
| EPWM11_G1     | 5004 B7B2h       |
| EPWM11_G2     | 5008 B7B2h       |
| EPWM11_G3     | 500C B7B2h       |
| EPWM12_G0     | 5000 C7B2h       |
| EPWM12_G1     | 5004 C7B2h       |
| EPWM12_G2     | 5008 C7B2h       |
| EPWM12_G3     | 500C C7B2h       |
| EPWM13_G0     | 5000 D7B2h       |
| EPWM13_G1     | 5004 D7B2h       |
| EPWM13_G2     | 5008 D7B2h       |
| EPWM13_G3     | 500C D7B2h       |
| EPWM14_G0     | 5000 E7B2h       |
| EPWM14_G1     | 5004 E7B2h       |
| EPWM14_G2     | 5008 E7B2h       |
| EPWM14_G3     | 500C E7B2h       |
| EPWM15_G0     | 5000 F7B2h       |
| EPWM15_G1     | 5004 F7B2h       |
| EPWM15_G2     | 5008 F7B2h       |
| EPWM15_G3     | 500C F7B2h       |
| EPWM16_G0     | 5001 07B2h       |
| EPWM16_G1     | 5005 07B2h       |
| EPWM16_G2     | 5009 07B2h       |
| EPWM16_G3     | 500D 07B2h       |
| EPWM17_G0     | 5001 17B2h       |
| EPWM17_G1     | 5005 17B2h       |
| EPWM17_G2     | 5009 17B2h       |
| EPWM17_G3     | 500D 17B2h       |
| EPWM18_G0     | 5001 27B2h       |
| EPWM18_G1     | 5005 27B2h       |
| EPWM18_G2     | 5009 27B2h       |
| EPWM18_G3     | 500D 27B2h       |
| EPWM19_G0     | 5001 37B2h       |
| EPWM19_G1     | 5005 37B2h       |
| EPWM19_G2     | 5009 37B2h       |
| EPWM19_G3     | 500D 37B2h       |
| EPWM20_G0     | 5001 47B2h       |
| EPWM20_G1     | 5005 47B2h       |
| EPWM20_G2     | 5009 47B2h       |
| EPWM20_G3     | 500D 47B2h       |

**Table 3-1279. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 57B2h       |
| EPWM21_G1     | 5005 57B2h       |
| EPWM21_G2     | 5009 57B2h       |
| EPWM21_G3     | 500D 57B2h       |
| EPWM22_G0     | 5001 67B2h       |
| EPWM22_G1     | 5005 67B2h       |
| EPWM22_G2     | 5009 67B2h       |
| EPWM22_G3     | 500D 67B2h       |
| EPWM23_G0     | 5001 77B2h       |
| EPWM23_G1     | 5005 77B2h       |
| EPWM23_G2     | 5009 77B2h       |
| EPWM23_G3     | 500D 77B2h       |
| EPWM24_G0     | 5001 87B2h       |
| EPWM24_G1     | 5005 87B2h       |
| EPWM24_G2     | 5009 87B2h       |
| EPWM24_G3     | 500D 87B2h       |
| EPWM25_G0     | 5001 97B2h       |
| EPWM25_G1     | 5005 97B2h       |
| EPWM25_G2     | 5009 97B2h       |
| EPWM25_G3     | 500D 97B2h       |
| EPWM26_G0     | 5001 A7B2h       |
| EPWM26_G1     | 5005 A7B2h       |
| EPWM26_G2     | 5009 A7B2h       |
| EPWM26_G3     | 500D A7B2h       |
| EPWM27_G0     | 5001 B7B2h       |
| EPWM27_G1     | 5005 B7B2h       |
| EPWM27_G2     | 5009 B7B2h       |
| EPWM27_G3     | 500D B7B2h       |
| EPWM28_G0     | 5001 C7B2h       |
| EPWM28_G1     | 5005 C7B2h       |
| EPWM28_G2     | 5009 C7B2h       |
| EPWM28_G3     | 500D C7B2h       |
| EPWM29_G0     | 5001 D7B2h       |
| EPWM29_G1     | 5005 D7B2h       |
| EPWM29_G2     | 5009 D7B2h       |
| EPWM29_G3     | 500D D7B2h       |
| EPWM30_G0     | 5001 E7B2h       |
| EPWM30_G1     | 5005 E7B2h       |
| EPWM30_G2     | 5009 E7B2h       |
| EPWM30_G3     | 500D E7B2h       |
| EPWM31_G0     | 5001 F7B2h       |
| EPWM31_G1     | 5005 F7B2h       |
| EPWM31_G2     | 5009 F7B2h       |
| EPWM31_G3     | 500D F7B2h       |

**Figure 3-407. EPWM\_XAQCTLB\_SHDW3 Name Register**

|            |    |       |    |       |    |       |   |
|------------|----|-------|----|-------|----|-------|---|
| 15         | 14 | 13    | 12 | 11    | 10 | 9     | 8 |
| XCMP8      |    | XCMP7 |    | XCMP6 |    | XCMP5 |   |
| R/W        |    | R/W   |    | R/W   |    | R/W   |   |
| 0h         |    | 0h    |    | 0h    |    | 0h    |   |
| 7          | 6  | 5     | 4  | 3     | 2  | 1     | 0 |
| RESERVED_1 |    |       |    |       |    |       |   |
| R          |    |       |    |       |    |       |   |
| 0h         |    |       |    |       |    |       |   |

**Table 3-1281. EPWM\_XAQCTLB\_SHDW3 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                          |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | XCMP8      | R/W  | 0h    | Action when Counter = CMP8<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 13:12 | XCMP7      | R/W  | 0h    | Action when Counter = CMP7<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 11:10 | XCMP6      | R/W  | 0h    | Action when Counter = CMP6<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 9:8   | XCMP5      | R/W  | 0h    | Action when Counter = CMP5<br>2'b00 Do nothing [action disabled]<br>2'b01 Clear [low]<br>2'b10 Set [high]<br>2'b11 Toggle [Low -> High, High -> Low] |
| 7:0   | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                             |

### 3.7.2.157 EPWM\_CMPC\_SHDW3 Register

#### 1 EPWM\_CMPC\_SHDW3 Register (Offset = 7BAh) [reset = 0h]

CMPC Shadow 3 Register.

Return to [Summary Table](#)

**Table 3-1282. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 07BAh       |
| EPWM0_G1      | 5004 07BAh       |
| EPWM0_G2      | 5008 07BAh       |
| EPWM0_G3      | 500C 07BAh       |
| EPWM1_G0      | 5000 17BAh       |
| EPWM1_G1      | 5004 17BAh       |
| EPWM1_G2      | 5008 17BAh       |
| EPWM1_G3      | 500C 17BAh       |
| EPWM2_G0      | 5000 27BAh       |
| EPWM2_G1      | 5004 27BAh       |
| EPWM2_G2      | 5008 27BAh       |
| EPWM2_G3      | 500C 27BAh       |
| EPWM3_G0      | 5000 37BAh       |
| EPWM3_G1      | 5004 37BAh       |
| EPWM3_G2      | 5008 37BAh       |
| EPWM3_G3      | 500C 37BAh       |
| EPWM4_G0      | 5000 47BAh       |
| EPWM4_G1      | 5004 47BAh       |
| EPWM4_G2      | 5008 47BAh       |
| EPWM4_G3      | 500C 47BAh       |
| EPWM5_G0      | 5000 57BAh       |
| EPWM5_G1      | 5004 57BAh       |
| EPWM5_G2      | 5008 57BAh       |
| EPWM5_G3      | 500C 57BAh       |
| EPWM6_G0      | 5000 67BAh       |
| EPWM6_G1      | 5004 67BAh       |
| EPWM6_G2      | 5008 67BAh       |
| EPWM6_G3      | 500C 67BAh       |
| EPWM7_G0      | 5000 77BAh       |
| EPWM7_G1      | 5004 77BAh       |
| EPWM7_G2      | 5008 77BAh       |
| EPWM7_G3      | 500C 77BAh       |
| EPWM8_G0      | 5000 87BAh       |
| EPWM8_G1      | 5004 87BAh       |
| EPWM8_G2      | 5008 87BAh       |
| EPWM8_G3      | 500C 87BAh       |
| EPWM9_G0      | 5000 97BAh       |
| EPWM9_G1      | 5004 97BAh       |
| EPWM9_G2      | 5008 97BAh       |

**Table 3-1282. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 97BAh       |
| EPWM10_G0     | 5000 A7BAh       |
| EPWM10_G1     | 5004 A7BAh       |
| EPWM10_G2     | 5008 A7BAh       |
| EPWM10_G3     | 500C A7BAh       |
| EPWM11_G0     | 5000 B7BAh       |
| EPWM11_G1     | 5004 B7BAh       |
| EPWM11_G2     | 5008 B7BAh       |
| EPWM11_G3     | 500C B7BAh       |
| EPWM12_G0     | 5000 C7BAh       |
| EPWM12_G1     | 5004 C7BAh       |
| EPWM12_G2     | 5008 C7BAh       |
| EPWM12_G3     | 500C C7BAh       |
| EPWM13_G0     | 5000 D7BAh       |
| EPWM13_G1     | 5004 D7BAh       |
| EPWM13_G2     | 5008 D7BAh       |
| EPWM13_G3     | 500C D7BAh       |
| EPWM14_G0     | 5000 E7BAh       |
| EPWM14_G1     | 5004 E7BAh       |
| EPWM14_G2     | 5008 E7BAh       |
| EPWM14_G3     | 500C E7BAh       |
| EPWM15_G0     | 5000 F7BAh       |
| EPWM15_G1     | 5004 F7BAh       |
| EPWM15_G2     | 5008 F7BAh       |
| EPWM15_G3     | 500C F7BAh       |
| EPWM16_G0     | 5001 07BAh       |
| EPWM16_G1     | 5005 07BAh       |
| EPWM16_G2     | 5009 07BAh       |
| EPWM16_G3     | 500D 07BAh       |
| EPWM17_G0     | 5001 17BAh       |
| EPWM17_G1     | 5005 17BAh       |
| EPWM17_G2     | 5009 17BAh       |
| EPWM17_G3     | 500D 17BAh       |
| EPWM18_G0     | 5001 27BAh       |
| EPWM18_G1     | 5005 27BAh       |
| EPWM18_G2     | 5009 27BAh       |
| EPWM18_G3     | 500D 27BAh       |
| EPWM19_G0     | 5001 37BAh       |
| EPWM19_G1     | 5005 37BAh       |
| EPWM19_G2     | 5009 37BAh       |
| EPWM19_G3     | 500D 37BAh       |
| EPWM20_G0     | 5001 47BAh       |
| EPWM20_G1     | 5005 47BAh       |
| EPWM20_G2     | 5009 47BAh       |
| EPWM20_G3     | 500D 47BAh       |



**Table 3-1282. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 57BAh       |
| EPWM21_G1     | 5005 57BAh       |
| EPWM21_G2     | 5009 57BAh       |
| EPWM21_G3     | 500D 57BAh       |
| EPWM22_G0     | 5001 67BAh       |
| EPWM22_G1     | 5005 67BAh       |
| EPWM22_G2     | 5009 67BAh       |
| EPWM22_G3     | 500D 67BAh       |
| EPWM23_G0     | 5001 77BAh       |
| EPWM23_G1     | 5005 77BAh       |
| EPWM23_G2     | 5009 77BAh       |
| EPWM23_G3     | 500D 77BAh       |
| EPWM24_G0     | 5001 87BAh       |
| EPWM24_G1     | 5005 87BAh       |
| EPWM24_G2     | 5009 87BAh       |
| EPWM24_G3     | 500D 87BAh       |
| EPWM25_G0     | 5001 97BAh       |
| EPWM25_G1     | 5005 97BAh       |
| EPWM25_G2     | 5009 97BAh       |
| EPWM25_G3     | 500D 97BAh       |
| EPWM26_G0     | 5001 A7BAh       |
| EPWM26_G1     | 5005 A7BAh       |
| EPWM26_G2     | 5009 A7BAh       |
| EPWM26_G3     | 500D A7BAh       |
| EPWM27_G0     | 5001 B7BAh       |
| EPWM27_G1     | 5005 B7BAh       |
| EPWM27_G2     | 5009 B7BAh       |
| EPWM27_G3     | 500D B7BAh       |
| EPWM28_G0     | 5001 C7BAh       |
| EPWM28_G1     | 5005 C7BAh       |
| EPWM28_G2     | 5009 C7BAh       |
| EPWM28_G3     | 500D C7BAh       |
| EPWM29_G0     | 5001 D7BAh       |
| EPWM29_G1     | 5005 D7BAh       |
| EPWM29_G2     | 5009 D7BAh       |
| EPWM29_G3     | 500D D7BAh       |
| EPWM30_G0     | 5001 E7BAh       |
| EPWM30_G1     | 5005 E7BAh       |
| EPWM30_G2     | 5009 E7BAh       |
| EPWM30_G3     | 500D E7BAh       |
| EPWM31_G0     | 5001 F7BAh       |
| EPWM31_G1     | 5005 F7BAh       |
| EPWM31_G2     | 5009 F7BAh       |
| EPWM31_G3     | 500D F7BAh       |

**Figure 3-408. EPWM\_CMPC\_SHDW3 Name Register**

|            |    |    |    |    |    |   |   |
|------------|----|----|----|----|----|---|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMPC_SHDW3 |    |    |    |    |    |   |   |
| R/W        |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| CMPC_SHDW3 |    |    |    |    |    |   |   |
| R/W        |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |

**Table 3-1284. EPWM\_CMPC\_SHDW3 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                 |
|------|------------|------|-------|-------------------------------------------------------------------------------------------------------------|
| 15:0 | CMPC_SHDW3 | R/W  | 0h    | The value in the CMPC_SHDW3 register is loaded into CMPC_ACTIVE register when shadow to active load occurs. |

### 3.7.2.158 EPWM\_CMPD\_SHDW3 Register

#### 1 EPWM\_CMPD\_SHDW3 Register (Offset = 7BEh) [reset = 0h]

CMPD Shadow 3 Register.

Return to [Summary Table](#)

**Table 3-1285. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 07BEh       |
| EPWM0_G1      | 5004 07BEh       |
| EPWM0_G2      | 5008 07BEh       |
| EPWM0_G3      | 500C 07BEh       |
| EPWM1_G0      | 5000 17BEh       |
| EPWM1_G1      | 5004 17BEh       |
| EPWM1_G2      | 5008 17BEh       |
| EPWM1_G3      | 500C 17BEh       |
| EPWM2_G0      | 5000 27BEh       |
| EPWM2_G1      | 5004 27BEh       |
| EPWM2_G2      | 5008 27BEh       |
| EPWM2_G3      | 500C 27BEh       |
| EPWM3_G0      | 5000 37BEh       |
| EPWM3_G1      | 5004 37BEh       |
| EPWM3_G2      | 5008 37BEh       |
| EPWM3_G3      | 500C 37BEh       |
| EPWM4_G0      | 5000 47BEh       |
| EPWM4_G1      | 5004 47BEh       |
| EPWM4_G2      | 5008 47BEh       |
| EPWM4_G3      | 500C 47BEh       |
| EPWM5_G0      | 5000 57BEh       |
| EPWM5_G1      | 5004 57BEh       |
| EPWM5_G2      | 5008 57BEh       |
| EPWM5_G3      | 500C 57BEh       |
| EPWM6_G0      | 5000 67BEh       |
| EPWM6_G1      | 5004 67BEh       |
| EPWM6_G2      | 5008 67BEh       |
| EPWM6_G3      | 500C 67BEh       |
| EPWM7_G0      | 5000 77BEh       |
| EPWM7_G1      | 5004 77BEh       |
| EPWM7_G2      | 5008 77BEh       |
| EPWM7_G3      | 500C 77BEh       |
| EPWM8_G0      | 5000 87BEh       |
| EPWM8_G1      | 5004 87BEh       |
| EPWM8_G2      | 5008 87BEh       |
| EPWM8_G3      | 500C 87BEh       |
| EPWM9_G0      | 5000 97BEh       |
| EPWM9_G1      | 5004 97BEh       |
| EPWM9_G2      | 5008 97BEh       |

**Table 3-1285. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 97BEh       |
| EPWM10_G0     | 5000 A7BEh       |
| EPWM10_G1     | 5004 A7BEh       |
| EPWM10_G2     | 5008 A7BEh       |
| EPWM10_G3     | 500C A7BEh       |
| EPWM11_G0     | 5000 B7BEh       |
| EPWM11_G1     | 5004 B7BEh       |
| EPWM11_G2     | 5008 B7BEh       |
| EPWM11_G3     | 500C B7BEh       |
| EPWM12_G0     | 5000 C7BEh       |
| EPWM12_G1     | 5004 C7BEh       |
| EPWM12_G2     | 5008 C7BEh       |
| EPWM12_G3     | 500C C7BEh       |
| EPWM13_G0     | 5000 D7BEh       |
| EPWM13_G1     | 5004 D7BEh       |
| EPWM13_G2     | 5008 D7BEh       |
| EPWM13_G3     | 500C D7BEh       |
| EPWM14_G0     | 5000 E7BEh       |
| EPWM14_G1     | 5004 E7BEh       |
| EPWM14_G2     | 5008 E7BEh       |
| EPWM14_G3     | 500C E7BEh       |
| EPWM15_G0     | 5000 F7BEh       |
| EPWM15_G1     | 5004 F7BEh       |
| EPWM15_G2     | 5008 F7BEh       |
| EPWM15_G3     | 500C F7BEh       |
| EPWM16_G0     | 5001 07BEh       |
| EPWM16_G1     | 5005 07BEh       |
| EPWM16_G2     | 5009 07BEh       |
| EPWM16_G3     | 500D 07BEh       |
| EPWM17_G0     | 5001 17BEh       |
| EPWM17_G1     | 5005 17BEh       |
| EPWM17_G2     | 5009 17BEh       |
| EPWM17_G3     | 500D 17BEh       |
| EPWM18_G0     | 5001 27BEh       |
| EPWM18_G1     | 5005 27BEh       |
| EPWM18_G2     | 5009 27BEh       |
| EPWM18_G3     | 500D 27BEh       |
| EPWM19_G0     | 5001 37BEh       |
| EPWM19_G1     | 5005 37BEh       |
| EPWM19_G2     | 5009 37BEh       |
| EPWM19_G3     | 500D 37BEh       |
| EPWM20_G0     | 5001 47BEh       |
| EPWM20_G1     | 5005 47BEh       |
| EPWM20_G2     | 5009 47BEh       |
| EPWM20_G3     | 500D 47BEh       |

**Table 3-1285. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 57BEh       |
| EPWM21_G1     | 5005 57BEh       |
| EPWM21_G2     | 5009 57BEh       |
| EPWM21_G3     | 500D 57BEh       |
| EPWM22_G0     | 5001 67BEh       |
| EPWM22_G1     | 5005 67BEh       |
| EPWM22_G2     | 5009 67BEh       |
| EPWM22_G3     | 500D 67BEh       |
| EPWM23_G0     | 5001 77BEh       |
| EPWM23_G1     | 5005 77BEh       |
| EPWM23_G2     | 5009 77BEh       |
| EPWM23_G3     | 500D 77BEh       |
| EPWM24_G0     | 5001 87BEh       |
| EPWM24_G1     | 5005 87BEh       |
| EPWM24_G2     | 5009 87BEh       |
| EPWM24_G3     | 500D 87BEh       |
| EPWM25_G0     | 5001 97BEh       |
| EPWM25_G1     | 5005 97BEh       |
| EPWM25_G2     | 5009 97BEh       |
| EPWM25_G3     | 500D 97BEh       |
| EPWM26_G0     | 5001 A7BEh       |
| EPWM26_G1     | 5005 A7BEh       |
| EPWM26_G2     | 5009 A7BEh       |
| EPWM26_G3     | 500D A7BEh       |
| EPWM27_G0     | 5001 B7BEh       |
| EPWM27_G1     | 5005 B7BEh       |
| EPWM27_G2     | 5009 B7BEh       |
| EPWM27_G3     | 500D B7BEh       |
| EPWM28_G0     | 5001 C7BEh       |
| EPWM28_G1     | 5005 C7BEh       |
| EPWM28_G2     | 5009 C7BEh       |
| EPWM28_G3     | 500D C7BEh       |
| EPWM29_G0     | 5001 D7BEh       |
| EPWM29_G1     | 5005 D7BEh       |
| EPWM29_G2     | 5009 D7BEh       |
| EPWM29_G3     | 500D D7BEh       |
| EPWM30_G0     | 5001 E7BEh       |
| EPWM30_G1     | 5005 E7BEh       |
| EPWM30_G2     | 5009 E7BEh       |
| EPWM30_G3     | 500D E7BEh       |
| EPWM31_G0     | 5001 F7BEh       |
| EPWM31_G1     | 5005 F7BEh       |
| EPWM31_G2     | 5009 F7BEh       |
| EPWM31_G3     | 500D F7BEh       |

**Figure 3-409. EPWM\_CMPD\_SHDW3 Name Register**

|            |    |    |    |    |    |   |   |
|------------|----|----|----|----|----|---|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CMPD_SHDW3 |    |    |    |    |    |   |   |
| R/W        |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| CMPD_SHDW3 |    |    |    |    |    |   |   |
| R/W        |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |

**Table 3-1287. EPWM\_CMPD\_SHDW3 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                 |
|------|------------|------|-------|-------------------------------------------------------------------------------------------------------------|
| 15:0 | CMPD_SHDW3 | R/W  | 0h    | The value in the CMPD_SHDW3 register is loaded into CMPD_ACTIVE register when shadow to active load occurs. |

### 3.7.2.159 EPWM\_XMINMAX\_SHDW3 Register

#### 1 EPWM\_XMINMAX\_SHDW3 Register (Offset = 7C4h) [reset = 0h]

XMINMAX Shadow 3 Register.

Return to [Summary Table](#)

**Table 3-1288. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 07C4h       |
| EPWM0_G1      | 5004 07C4h       |
| EPWM0_G2      | 5008 07C4h       |
| EPWM0_G3      | 500C 07C4h       |
| EPWM1_G0      | 5000 17C4h       |
| EPWM1_G1      | 5004 17C4h       |
| EPWM1_G2      | 5008 17C4h       |
| EPWM1_G3      | 500C 17C4h       |
| EPWM2_G0      | 5000 27C4h       |
| EPWM2_G1      | 5004 27C4h       |
| EPWM2_G2      | 5008 27C4h       |
| EPWM2_G3      | 500C 27C4h       |
| EPWM3_G0      | 5000 37C4h       |
| EPWM3_G1      | 5004 37C4h       |
| EPWM3_G2      | 5008 37C4h       |
| EPWM3_G3      | 500C 37C4h       |
| EPWM4_G0      | 5000 47C4h       |
| EPWM4_G1      | 5004 47C4h       |
| EPWM4_G2      | 5008 47C4h       |
| EPWM4_G3      | 500C 47C4h       |
| EPWM5_G0      | 5000 57C4h       |
| EPWM5_G1      | 5004 57C4h       |
| EPWM5_G2      | 5008 57C4h       |
| EPWM5_G3      | 500C 57C4h       |
| EPWM6_G0      | 5000 67C4h       |
| EPWM6_G1      | 5004 67C4h       |
| EPWM6_G2      | 5008 67C4h       |
| EPWM6_G3      | 500C 67C4h       |
| EPWM7_G0      | 5000 77C4h       |
| EPWM7_G1      | 5004 77C4h       |
| EPWM7_G2      | 5008 77C4h       |
| EPWM7_G3      | 500C 77C4h       |
| EPWM8_G0      | 5000 87C4h       |
| EPWM8_G1      | 5004 87C4h       |
| EPWM8_G2      | 5008 87C4h       |
| EPWM8_G3      | 500C 87C4h       |
| EPWM9_G0      | 5000 97C4h       |
| EPWM9_G1      | 5004 97C4h       |
| EPWM9_G2      | 5008 97C4h       |

**Table 3-1288. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 97C4h       |
| EPWM10_G0     | 5000 A7C4h       |
| EPWM10_G1     | 5004 A7C4h       |
| EPWM10_G2     | 5008 A7C4h       |
| EPWM10_G3     | 500C A7C4h       |
| EPWM11_G0     | 5000 B7C4h       |
| EPWM11_G1     | 5004 B7C4h       |
| EPWM11_G2     | 5008 B7C4h       |
| EPWM11_G3     | 500C B7C4h       |
| EPWM12_G0     | 5000 C7C4h       |
| EPWM12_G1     | 5004 C7C4h       |
| EPWM12_G2     | 5008 C7C4h       |
| EPWM12_G3     | 500C C7C4h       |
| EPWM13_G0     | 5000 D7C4h       |
| EPWM13_G1     | 5004 D7C4h       |
| EPWM13_G2     | 5008 D7C4h       |
| EPWM13_G3     | 500C D7C4h       |
| EPWM14_G0     | 5000 E7C4h       |
| EPWM14_G1     | 5004 E7C4h       |
| EPWM14_G2     | 5008 E7C4h       |
| EPWM14_G3     | 500C E7C4h       |
| EPWM15_G0     | 5000 F7C4h       |
| EPWM15_G1     | 5004 F7C4h       |
| EPWM15_G2     | 5008 F7C4h       |
| EPWM15_G3     | 500C F7C4h       |
| EPWM16_G0     | 5001 07C4h       |
| EPWM16_G1     | 5005 07C4h       |
| EPWM16_G2     | 5009 07C4h       |
| EPWM16_G3     | 500D 07C4h       |
| EPWM17_G0     | 5001 17C4h       |
| EPWM17_G1     | 5005 17C4h       |
| EPWM17_G2     | 5009 17C4h       |
| EPWM17_G3     | 500D 17C4h       |
| EPWM18_G0     | 5001 27C4h       |
| EPWM18_G1     | 5005 27C4h       |
| EPWM18_G2     | 5009 27C4h       |
| EPWM18_G3     | 500D 27C4h       |
| EPWM19_G0     | 5001 37C4h       |
| EPWM19_G1     | 5005 37C4h       |
| EPWM19_G2     | 5009 37C4h       |
| EPWM19_G3     | 500D 37C4h       |
| EPWM20_G0     | 5001 47C4h       |
| EPWM20_G1     | 5005 47C4h       |
| EPWM20_G2     | 5009 47C4h       |
| EPWM20_G3     | 500D 47C4h       |



**Table 3-1288. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 57C4h       |
| EPWM21_G1     | 5005 57C4h       |
| EPWM21_G2     | 5009 57C4h       |
| EPWM21_G3     | 500D 57C4h       |
| EPWM22_G0     | 5001 67C4h       |
| EPWM22_G1     | 5005 67C4h       |
| EPWM22_G2     | 5009 67C4h       |
| EPWM22_G3     | 500D 67C4h       |
| EPWM23_G0     | 5001 77C4h       |
| EPWM23_G1     | 5005 77C4h       |
| EPWM23_G2     | 5009 77C4h       |
| EPWM23_G3     | 500D 77C4h       |
| EPWM24_G0     | 5001 87C4h       |
| EPWM24_G1     | 5005 87C4h       |
| EPWM24_G2     | 5009 87C4h       |
| EPWM24_G3     | 500D 87C4h       |
| EPWM25_G0     | 5001 97C4h       |
| EPWM25_G1     | 5005 97C4h       |
| EPWM25_G2     | 5009 97C4h       |
| EPWM25_G3     | 500D 97C4h       |
| EPWM26_G0     | 5001 A7C4h       |
| EPWM26_G1     | 5005 A7C4h       |
| EPWM26_G2     | 5009 A7C4h       |
| EPWM26_G3     | 500D A7C4h       |
| EPWM27_G0     | 5001 B7C4h       |
| EPWM27_G1     | 5005 B7C4h       |
| EPWM27_G2     | 5009 B7C4h       |
| EPWM27_G3     | 500D B7C4h       |
| EPWM28_G0     | 5001 C7C4h       |
| EPWM28_G1     | 5005 C7C4h       |
| EPWM28_G2     | 5009 C7C4h       |
| EPWM28_G3     | 500D C7C4h       |
| EPWM29_G0     | 5001 D7C4h       |
| EPWM29_G1     | 5005 D7C4h       |
| EPWM29_G2     | 5009 D7C4h       |
| EPWM29_G3     | 500D D7C4h       |
| EPWM30_G0     | 5001 E7C4h       |
| EPWM30_G1     | 5005 E7C4h       |
| EPWM30_G2     | 5009 E7C4h       |
| EPWM30_G3     | 500D E7C4h       |
| EPWM31_G0     | 5001 F7C4h       |
| EPWM31_G1     | 5005 F7C4h       |
| EPWM31_G2     | 5009 F7C4h       |
| EPWM31_G3     | 500D F7C4h       |

**Figure 3-410. EPWM\_XMINMAX\_SHDW3 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| XMIN_SHDW3 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| XMIN_SHDW3 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| XMAX_SHDW3 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XMAX_SHDW3 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 3-1290. EPWM\_XMINMAX\_SHDW3 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                 |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------|
| 31:16 | XMIN_SHDW3 | R/W  | 0h    | The value in the XMIN_SHDW3 register is loaded into XMIN_ACTIVE register when shadow to active load occurs. |
| 15:0  | XMAX_SHDW3 | R/W  | 0h    | The value in the XMAX_SHDW3 register is loaded into XMAX_ACTIVE register when shadow to active load occurs. |

### 3.7.2.160 EPWM\_DECTL Register

#### 1 EPWM\_DECTL Register (Offset = 800h) [reset = 0h]

DE control register.

Return to [Summary Table](#)

**Table 3-1291. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0800h       |
| EPWM0_G1      | 5004 0800h       |
| EPWM0_G2      | 5008 0800h       |
| EPWM0_G3      | 500C 0800h       |
| EPWM1_G0      | 5000 1800h       |
| EPWM1_G1      | 5004 1800h       |
| EPWM1_G2      | 5008 1800h       |
| EPWM1_G3      | 500C 1800h       |
| EPWM2_G0      | 5000 2800h       |
| EPWM2_G1      | 5004 2800h       |
| EPWM2_G2      | 5008 2800h       |
| EPWM2_G3      | 500C 2800h       |
| EPWM3_G0      | 5000 3800h       |
| EPWM3_G1      | 5004 3800h       |
| EPWM3_G2      | 5008 3800h       |
| EPWM3_G3      | 500C 3800h       |
| EPWM4_G0      | 5000 4800h       |
| EPWM4_G1      | 5004 4800h       |
| EPWM4_G2      | 5008 4800h       |
| EPWM4_G3      | 500C 4800h       |
| EPWM5_G0      | 5000 5800h       |
| EPWM5_G1      | 5004 5800h       |
| EPWM5_G2      | 5008 5800h       |
| EPWM5_G3      | 500C 5800h       |
| EPWM6_G0      | 5000 6800h       |
| EPWM6_G1      | 5004 6800h       |
| EPWM6_G2      | 5008 6800h       |
| EPWM6_G3      | 500C 6800h       |
| EPWM7_G0      | 5000 7800h       |
| EPWM7_G1      | 5004 7800h       |
| EPWM7_G2      | 5008 7800h       |
| EPWM7_G3      | 500C 7800h       |
| EPWM8_G0      | 5000 8800h       |
| EPWM8_G1      | 5004 8800h       |
| EPWM8_G2      | 5008 8800h       |
| EPWM8_G3      | 500C 8800h       |
| EPWM9_G0      | 5000 9800h       |
| EPWM9_G1      | 5004 9800h       |
| EPWM9_G2      | 5008 9800h       |

**Table 3-1291. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9800h       |
| EPWM10_G0     | 5000 A800h       |
| EPWM10_G1     | 5004 A800h       |
| EPWM10_G2     | 5008 A800h       |
| EPWM10_G3     | 500C A800h       |
| EPWM11_G0     | 5000 B800h       |
| EPWM11_G1     | 5004 B800h       |
| EPWM11_G2     | 5008 B800h       |
| EPWM11_G3     | 500C B800h       |
| EPWM12_G0     | 5000 C800h       |
| EPWM12_G1     | 5004 C800h       |
| EPWM12_G2     | 5008 C800h       |
| EPWM12_G3     | 500C C800h       |
| EPWM13_G0     | 5000 D800h       |
| EPWM13_G1     | 5004 D800h       |
| EPWM13_G2     | 5008 D800h       |
| EPWM13_G3     | 500C D800h       |
| EPWM14_G0     | 5000 E800h       |
| EPWM14_G1     | 5004 E800h       |
| EPWM14_G2     | 5008 E800h       |
| EPWM14_G3     | 500C E800h       |
| EPWM15_G0     | 5000 F800h       |
| EPWM15_G1     | 5004 F800h       |
| EPWM15_G2     | 5008 F800h       |
| EPWM15_G3     | 500C F800h       |
| EPWM16_G0     | 5001 0800h       |
| EPWM16_G1     | 5005 0800h       |
| EPWM16_G2     | 5009 0800h       |
| EPWM16_G3     | 500D 0800h       |
| EPWM17_G0     | 5001 1800h       |
| EPWM17_G1     | 5005 1800h       |
| EPWM17_G2     | 5009 1800h       |
| EPWM17_G3     | 500D 1800h       |
| EPWM18_G0     | 5001 2800h       |
| EPWM18_G1     | 5005 2800h       |
| EPWM18_G2     | 5009 2800h       |
| EPWM18_G3     | 500D 2800h       |
| EPWM19_G0     | 5001 3800h       |
| EPWM19_G1     | 5005 3800h       |
| EPWM19_G2     | 5009 3800h       |
| EPWM19_G3     | 500D 3800h       |
| EPWM20_G0     | 5001 4800h       |
| EPWM20_G1     | 5005 4800h       |
| EPWM20_G2     | 5009 4800h       |
| EPWM20_G3     | 500D 4800h       |

**Table 3-1291. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5800h       |
| EPWM21_G1     | 5005 5800h       |
| EPWM21_G2     | 5009 5800h       |
| EPWM21_G3     | 500D 5800h       |
| EPWM22_G0     | 5001 6800h       |
| EPWM22_G1     | 5005 6800h       |
| EPWM22_G2     | 5009 6800h       |
| EPWM22_G3     | 500D 6800h       |
| EPWM23_G0     | 5001 7800h       |
| EPWM23_G1     | 5005 7800h       |
| EPWM23_G2     | 5009 7800h       |
| EPWM23_G3     | 500D 7800h       |
| EPWM24_G0     | 5001 8800h       |
| EPWM24_G1     | 5005 8800h       |
| EPWM24_G2     | 5009 8800h       |
| EPWM24_G3     | 500D 8800h       |
| EPWM25_G0     | 5001 9800h       |
| EPWM25_G1     | 5005 9800h       |
| EPWM25_G2     | 5009 9800h       |
| EPWM25_G3     | 500D 9800h       |
| EPWM26_G0     | 5001 A800h       |
| EPWM26_G1     | 5005 A800h       |
| EPWM26_G2     | 5009 A800h       |
| EPWM26_G3     | 500D A800h       |
| EPWM27_G0     | 5001 B800h       |
| EPWM27_G1     | 5005 B800h       |
| EPWM27_G2     | 5009 B800h       |
| EPWM27_G3     | 500D B800h       |
| EPWM28_G0     | 5001 C800h       |
| EPWM28_G1     | 5005 C800h       |
| EPWM28_G2     | 5009 C800h       |
| EPWM28_G3     | 500D C800h       |
| EPWM29_G0     | 5001 D800h       |
| EPWM29_G1     | 5005 D800h       |
| EPWM29_G2     | 5009 D800h       |
| EPWM29_G3     | 500D D800h       |
| EPWM30_G0     | 5001 E800h       |
| EPWM30_G1     | 5005 E800h       |
| EPWM30_G2     | 5009 E800h       |
| EPWM30_G3     | 500D E800h       |
| EPWM31_G0     | 5001 F800h       |
| EPWM31_G1     | 5005 F800h       |
| EPWM31_G2     | 5009 F800h       |
| EPWM31_G3     | 500D F800h       |

**Figure 3-411. EPWM\_DECTL Name Register**

|            |    |    |    |    |    |      |        |
|------------|----|----|----|----|----|------|--------|
| 31         | 30 | 29 | 28 | 27 | 26 | 25   | 24     |
| RESERVED_2 |    |    |    |    |    |      |        |
| R          |    |    |    |    |    |      |        |
| 0h         |    |    |    |    |    |      |        |
| 23         | 22 | 21 | 20 | 19 | 18 | 17   | 16     |
| RESERVED_2 |    |    |    |    |    |      |        |
| R          |    |    |    |    |    |      |        |
| 0h         |    |    |    |    |    |      |        |
| 15         | 14 | 13 | 12 | 11 | 10 | 9    | 8      |
| REENTRYDLY |    |    |    |    |    |      |        |
| R/W        |    |    |    |    |    |      |        |
| 0h         |    |    |    |    |    |      |        |
| 7          | 6  | 5  | 4  | 3  | 2  | 1    | 0      |
| RESERVED_1 |    |    |    |    |    | MODE | ENABLE |
| R          |    |    |    |    |    | R/W  | R/W    |
| 0h         |    |    |    |    |    | 0h   | 0h     |

**Table 3-1293. EPWM\_DECTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                    |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                       |
| 15:8  | REENTRYDLY | R/W  | 0h    | Determines the blocking window after DEACTIVE flag is cleared in which setting of DEACTIVE flag is prevented from being set.<br>0 : No blocking<br>1 : Blocked until 1 PWMSYNCOUT event<br>2 : Blocked until 2 PWMSYNCOUT events<br>.<br>.<br>255 : Blocked until 127 PWMSYNCOUT events                                                                        |
| 7:2   | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                       |
| 1     | MODE       | R/W  | 0h    | 0 : DEACTIVE flag works in cycle by cycle mode. On every PWMSYNCOUT, set condition of DEACTIVE flag is evaluated. If the set condition is not present the flag is cleared.<br>1 : DEACTIVE flag works in one shot mode [hardware set] and software clear.                                                                                                      |
| 0     | ENABLE     | R/W  | 0h    | DE function enable<br>0 : Diode Emulation mode functionality is disabled. DEACTIVE flag is not set on a TRIPH_OR_TRIPL event.<br>1 : Diode Emulation mode functionality is enabled. DEACTIVE flag is set on a TRIPH_OR_TRIPL event.<br>Note: ENABLE bit is cleared on a PWMTRIP event. Software has to re-enable this bit after PWMTRIP condition is serviced. |

### 3.7.2.161 EPWM\_DECOMPSEL Register

#### 1 EPWM\_DECOMPSEL Register (Offset = 804h) [reset = 0h]

Used to configure the comparator whose trip sources will be used.

Return to [Summary Table](#)

**Table 3-1294. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0804h       |
| EPWM0_G1      | 5004 0804h       |
| EPWM0_G2      | 5008 0804h       |
| EPWM0_G3      | 500C 0804h       |
| EPWM1_G0      | 5000 1804h       |
| EPWM1_G1      | 5004 1804h       |
| EPWM1_G2      | 5008 1804h       |
| EPWM1_G3      | 500C 1804h       |
| EPWM2_G0      | 5000 2804h       |
| EPWM2_G1      | 5004 2804h       |
| EPWM2_G2      | 5008 2804h       |
| EPWM2_G3      | 500C 2804h       |
| EPWM3_G0      | 5000 3804h       |
| EPWM3_G1      | 5004 3804h       |
| EPWM3_G2      | 5008 3804h       |
| EPWM3_G3      | 500C 3804h       |
| EPWM4_G0      | 5000 4804h       |
| EPWM4_G1      | 5004 4804h       |
| EPWM4_G2      | 5008 4804h       |
| EPWM4_G3      | 500C 4804h       |
| EPWM5_G0      | 5000 5804h       |
| EPWM5_G1      | 5004 5804h       |
| EPWM5_G2      | 5008 5804h       |
| EPWM5_G3      | 500C 5804h       |
| EPWM6_G0      | 5000 6804h       |
| EPWM6_G1      | 5004 6804h       |
| EPWM6_G2      | 5008 6804h       |
| EPWM6_G3      | 500C 6804h       |
| EPWM7_G0      | 5000 7804h       |
| EPWM7_G1      | 5004 7804h       |
| EPWM7_G2      | 5008 7804h       |
| EPWM7_G3      | 500C 7804h       |
| EPWM8_G0      | 5000 8804h       |
| EPWM8_G1      | 5004 8804h       |
| EPWM8_G2      | 5008 8804h       |
| EPWM8_G3      | 500C 8804h       |
| EPWM9_G0      | 5000 9804h       |
| EPWM9_G1      | 5004 9804h       |
| EPWM9_G2      | 5008 9804h       |

**Table 3-1294. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9804h       |
| EPWM10_G0     | 5000 A804h       |
| EPWM10_G1     | 5004 A804h       |
| EPWM10_G2     | 5008 A804h       |
| EPWM10_G3     | 500C A804h       |
| EPWM11_G0     | 5000 B804h       |
| EPWM11_G1     | 5004 B804h       |
| EPWM11_G2     | 5008 B804h       |
| EPWM11_G3     | 500C B804h       |
| EPWM12_G0     | 5000 C804h       |
| EPWM12_G1     | 5004 C804h       |
| EPWM12_G2     | 5008 C804h       |
| EPWM12_G3     | 500C C804h       |
| EPWM13_G0     | 5000 D804h       |
| EPWM13_G1     | 5004 D804h       |
| EPWM13_G2     | 5008 D804h       |
| EPWM13_G3     | 500C D804h       |
| EPWM14_G0     | 5000 E804h       |
| EPWM14_G1     | 5004 E804h       |
| EPWM14_G2     | 5008 E804h       |
| EPWM14_G3     | 500C E804h       |
| EPWM15_G0     | 5000 F804h       |
| EPWM15_G1     | 5004 F804h       |
| EPWM15_G2     | 5008 F804h       |
| EPWM15_G3     | 500C F804h       |
| EPWM16_G0     | 5001 0804h       |
| EPWM16_G1     | 5005 0804h       |
| EPWM16_G2     | 5009 0804h       |
| EPWM16_G3     | 500D 0804h       |
| EPWM17_G0     | 5001 1804h       |
| EPWM17_G1     | 5005 1804h       |
| EPWM17_G2     | 5009 1804h       |
| EPWM17_G3     | 500D 1804h       |
| EPWM18_G0     | 5001 2804h       |
| EPWM18_G1     | 5005 2804h       |
| EPWM18_G2     | 5009 2804h       |
| EPWM18_G3     | 500D 2804h       |
| EPWM19_G0     | 5001 3804h       |
| EPWM19_G1     | 5005 3804h       |
| EPWM19_G2     | 5009 3804h       |
| EPWM19_G3     | 500D 3804h       |
| EPWM20_G0     | 5001 4804h       |
| EPWM20_G1     | 5005 4804h       |
| EPWM20_G2     | 5009 4804h       |
| EPWM20_G3     | 500D 4804h       |



**Table 3-1294. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5804h       |
| EPWM21_G1     | 5005 5804h       |
| EPWM21_G2     | 5009 5804h       |
| EPWM21_G3     | 500D 5804h       |
| EPWM22_G0     | 5001 6804h       |
| EPWM22_G1     | 5005 6804h       |
| EPWM22_G2     | 5009 6804h       |
| EPWM22_G3     | 500D 6804h       |
| EPWM23_G0     | 5001 7804h       |
| EPWM23_G1     | 5005 7804h       |
| EPWM23_G2     | 5009 7804h       |
| EPWM23_G3     | 500D 7804h       |
| EPWM24_G0     | 5001 8804h       |
| EPWM24_G1     | 5005 8804h       |
| EPWM24_G2     | 5009 8804h       |
| EPWM24_G3     | 500D 8804h       |
| EPWM25_G0     | 5001 9804h       |
| EPWM25_G1     | 5005 9804h       |
| EPWM25_G2     | 5009 9804h       |
| EPWM25_G3     | 500D 9804h       |
| EPWM26_G0     | 5001 A804h       |
| EPWM26_G1     | 5005 A804h       |
| EPWM26_G2     | 5009 A804h       |
| EPWM26_G3     | 500D A804h       |
| EPWM27_G0     | 5001 B804h       |
| EPWM27_G1     | 5005 B804h       |
| EPWM27_G2     | 5009 B804h       |
| EPWM27_G3     | 500D B804h       |
| EPWM28_G0     | 5001 C804h       |
| EPWM28_G1     | 5005 C804h       |
| EPWM28_G2     | 5009 C804h       |
| EPWM28_G3     | 500D C804h       |
| EPWM29_G0     | 5001 D804h       |
| EPWM29_G1     | 5005 D804h       |
| EPWM29_G2     | 5009 D804h       |
| EPWM29_G3     | 500D D804h       |
| EPWM30_G0     | 5001 E804h       |
| EPWM30_G1     | 5005 E804h       |
| EPWM30_G2     | 5009 E804h       |
| EPWM30_G3     | 500D E804h       |
| EPWM31_G0     | 5001 F804h       |
| EPWM31_G1     | 5005 F804h       |
| EPWM31_G2     | 5009 F804h       |
| EPWM31_G3     | 500D F804h       |

**Figure 3-412. EPWM\_DECOMPSEL Name Register**

|            |    |       |    |    |    |    |    |
|------------|----|-------|----|----|----|----|----|
| 31         | 30 | 29    | 28 | 27 | 26 | 25 | 24 |
| RESERVED_2 |    |       |    |    |    |    |    |
| R          |    |       |    |    |    |    |    |
| 0h         |    |       |    |    |    |    |    |
| 23         | 22 | 21    | 20 | 19 | 18 | 17 | 16 |
| RESERVED_2 |    | TRIPH |    |    |    |    |    |
| R          |    | R/W   |    |    |    |    |    |
| 0h         |    | 0h    |    |    |    |    |    |
| 15         | 14 | 13    | 12 | 11 | 10 | 9  | 8  |
| RESERVED_1 |    |       |    |    |    |    |    |
| R          |    |       |    |    |    |    |    |
| 0h         |    |       |    |    |    |    |    |
| 7          | 6  | 5     | 4  | 3  | 2  | 1  | 0  |
| RESERVED_1 |    | TRIPL |    |    |    |    |    |
| R          |    | R/W   |    |    |    |    |    |
| 0h         |    | 0h    |    |    |    |    |    |

**Table 3-1296. EPWM\_DECOMPSEL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:22 | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 21:16 | TRIPH      | R/W  | 0h    | 000000 : Reserved<br>000001 : Input-XBAR[0] is the source of TRIPH<br>000010 : Input-XBAR[1] is the source of TRIPH<br>.<br>.<br>100000 : Input-XBAR[31] is the source of TRIPH<br>100001 : CMPSSA0 is the source of TRIPH<br>100010 : CMPSSA1 is the source of TRIPH<br>.<br>.<br>101010 : CMPSSA9 is the source of TRIPH<br>101011 : Reserved<br>.<br>.<br>110000 : Reserved<br>110001 : CMPSSB0 is the source of TRIPH<br>110010 : CMPSSB1 is the source of TRIPH<br>.<br>.<br>111010 : CMPSSB9 is the source of TRIPH<br>111011 : Reserved<br>.<br>.<br>111111 : Reserved<br>Note: All the reserved encodings result in TRIPH being 0. |
| 15:6  | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

**Table 3-1296. EPWM\_DECOMPSEL Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5:0 | TRIPL | R/W  | 0h    | 000000 : Reserved<br>000001 : Input-XBAR[0] is the source of TRIPL<br>000010 : Input-XBAR[1] is the source of TRIPL<br>.<br>.<br>100000 : Input-XBAR[31] is the source of TRIPL<br>100001 : CMPSSA0 is the source of TRIPL<br>100010 : CMPSSA1 is the source of TRIPL<br>.<br>.<br>101010 : CMPSSA9 is the source of TRIPL<br>101011 : Reserved<br>.<br>.<br>110000 : Reserved<br>110001 : CMPSSB0 is the source of TRIPL<br>110010 : CMPSSB1 is the source of TRIPL<br>.<br>.<br>111010 : CMPSSB9 is the source of TRIPL<br>111011 : Reserved<br>.<br>.<br>111111 : Reserved<br>Note: All the reserved encodings result in TRIPL being 0. |

### 3.7.2.162 EPWM\_DEACTCTL Register

#### 1 EPWM\_DEACTCTL Register (Offset = 808h) [reset = 0h]

Used to configure the PWM controls when in DE mode.

Return to [Summary Table](#)

**Table 3-1297. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0808h       |
| EPWM0_G1      | 5004 0808h       |
| EPWM0_G2      | 5008 0808h       |
| EPWM0_G3      | 500C 0808h       |
| EPWM1_G0      | 5000 1808h       |
| EPWM1_G1      | 5004 1808h       |
| EPWM1_G2      | 5008 1808h       |
| EPWM1_G3      | 500C 1808h       |
| EPWM2_G0      | 5000 2808h       |
| EPWM2_G1      | 5004 2808h       |
| EPWM2_G2      | 5008 2808h       |
| EPWM2_G3      | 500C 2808h       |
| EPWM3_G0      | 5000 3808h       |
| EPWM3_G1      | 5004 3808h       |
| EPWM3_G2      | 5008 3808h       |
| EPWM3_G3      | 500C 3808h       |
| EPWM4_G0      | 5000 4808h       |
| EPWM4_G1      | 5004 4808h       |
| EPWM4_G2      | 5008 4808h       |
| EPWM4_G3      | 500C 4808h       |
| EPWM5_G0      | 5000 5808h       |
| EPWM5_G1      | 5004 5808h       |
| EPWM5_G2      | 5008 5808h       |
| EPWM5_G3      | 500C 5808h       |
| EPWM6_G0      | 5000 6808h       |
| EPWM6_G1      | 5004 6808h       |
| EPWM6_G2      | 5008 6808h       |
| EPWM6_G3      | 500C 6808h       |
| EPWM7_G0      | 5000 7808h       |
| EPWM7_G1      | 5004 7808h       |
| EPWM7_G2      | 5008 7808h       |
| EPWM7_G3      | 500C 7808h       |
| EPWM8_G0      | 5000 8808h       |
| EPWM8_G1      | 5004 8808h       |
| EPWM8_G2      | 5008 8808h       |
| EPWM8_G3      | 500C 8808h       |
| EPWM9_G0      | 5000 9808h       |
| EPWM9_G1      | 5004 9808h       |
| EPWM9_G2      | 5008 9808h       |

**Table 3-1297. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9808h       |
| EPWM10_G0     | 5000 A808h       |
| EPWM10_G1     | 5004 A808h       |
| EPWM10_G2     | 5008 A808h       |
| EPWM10_G3     | 500C A808h       |
| EPWM11_G0     | 5000 B808h       |
| EPWM11_G1     | 5004 B808h       |
| EPWM11_G2     | 5008 B808h       |
| EPWM11_G3     | 500C B808h       |
| EPWM12_G0     | 5000 C808h       |
| EPWM12_G1     | 5004 C808h       |
| EPWM12_G2     | 5008 C808h       |
| EPWM12_G3     | 500C C808h       |
| EPWM13_G0     | 5000 D808h       |
| EPWM13_G1     | 5004 D808h       |
| EPWM13_G2     | 5008 D808h       |
| EPWM13_G3     | 500C D808h       |
| EPWM14_G0     | 5000 E808h       |
| EPWM14_G1     | 5004 E808h       |
| EPWM14_G2     | 5008 E808h       |
| EPWM14_G3     | 500C E808h       |
| EPWM15_G0     | 5000 F808h       |
| EPWM15_G1     | 5004 F808h       |
| EPWM15_G2     | 5008 F808h       |
| EPWM15_G3     | 500C F808h       |
| EPWM16_G0     | 5001 0808h       |
| EPWM16_G1     | 5005 0808h       |
| EPWM16_G2     | 5009 0808h       |
| EPWM16_G3     | 500D 0808h       |
| EPWM17_G0     | 5001 1808h       |
| EPWM17_G1     | 5005 1808h       |
| EPWM17_G2     | 5009 1808h       |
| EPWM17_G3     | 500D 1808h       |
| EPWM18_G0     | 5001 2808h       |
| EPWM18_G1     | 5005 2808h       |
| EPWM18_G2     | 5009 2808h       |
| EPWM18_G3     | 500D 2808h       |
| EPWM19_G0     | 5001 3808h       |
| EPWM19_G1     | 5005 3808h       |
| EPWM19_G2     | 5009 3808h       |
| EPWM19_G3     | 500D 3808h       |
| EPWM20_G0     | 5001 4808h       |
| EPWM20_G1     | 5005 4808h       |
| EPWM20_G2     | 5009 4808h       |
| EPWM20_G3     | 500D 4808h       |

**Table 3-1297. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5808h       |
| EPWM21_G1     | 5005 5808h       |
| EPWM21_G2     | 5009 5808h       |
| EPWM21_G3     | 500D 5808h       |
| EPWM22_G0     | 5001 6808h       |
| EPWM22_G1     | 5005 6808h       |
| EPWM22_G2     | 5009 6808h       |
| EPWM22_G3     | 500D 6808h       |
| EPWM23_G0     | 5001 7808h       |
| EPWM23_G1     | 5005 7808h       |
| EPWM23_G2     | 5009 7808h       |
| EPWM23_G3     | 500D 7808h       |
| EPWM24_G0     | 5001 8808h       |
| EPWM24_G1     | 5005 8808h       |
| EPWM24_G2     | 5009 8808h       |
| EPWM24_G3     | 500D 8808h       |
| EPWM25_G0     | 5001 9808h       |
| EPWM25_G1     | 5005 9808h       |
| EPWM25_G2     | 5009 9808h       |
| EPWM25_G3     | 500D 9808h       |
| EPWM26_G0     | 5001 A808h       |
| EPWM26_G1     | 5005 A808h       |
| EPWM26_G2     | 5009 A808h       |
| EPWM26_G3     | 500D A808h       |
| EPWM27_G0     | 5001 B808h       |
| EPWM27_G1     | 5005 B808h       |
| EPWM27_G2     | 5009 B808h       |
| EPWM27_G3     | 500D B808h       |
| EPWM28_G0     | 5001 C808h       |
| EPWM28_G1     | 5005 C808h       |
| EPWM28_G2     | 5009 C808h       |
| EPWM28_G3     | 500D C808h       |
| EPWM29_G0     | 5001 D808h       |
| EPWM29_G1     | 5005 D808h       |
| EPWM29_G2     | 5009 D808h       |
| EPWM29_G3     | 500D D808h       |
| EPWM30_G0     | 5001 E808h       |
| EPWM30_G1     | 5005 E808h       |
| EPWM30_G2     | 5009 E808h       |
| EPWM30_G3     | 500D E808h       |
| EPWM31_G0     | 5001 F808h       |
| EPWM31_G1     | 5005 F808h       |
| EPWM31_G2     | 5009 F808h       |
| EPWM31_G3     | 500D F808h       |

**Figure 3-413. EPWM\_DEACTCTL Name Register**

|            |          |      |    |            |          |            |    |
|------------|----------|------|----|------------|----------|------------|----|
| 31         | 30       | 29   | 28 | 27         | 26       | 25         | 24 |
| RESERVED_3 |          |      |    |            |          |            |    |
| R          |          |      |    |            |          |            |    |
| 0h         |          |      |    |            |          |            |    |
| 23         | 22       | 21   | 20 | 19         | 18       | 17         | 16 |
| RESERVED_3 |          |      |    |            |          | TRIPENABLE |    |
| R          |          |      |    |            |          | R/W        |    |
| 0h         |          |      |    |            |          | 0h         |    |
| 15         | 14       | 13   | 12 | 11         | 10       | 9          | 8  |
| RESERVED_2 |          |      |    |            |          |            |    |
| R          |          |      |    |            |          |            |    |
| 0h         |          |      |    |            |          |            |    |
| 7          | 6        | 5    | 4  | 3          | 2        | 1          | 0  |
| RESERVED_2 | TRIPSELB | PWMB |    | RESERVED_1 | TRIPSELA | PWMA       |    |
| R          | R/W      | R/W  |    | R          | R/W      | R/W        |    |
| 0h         | 0h       | 0h   |    | 0h         | 0h       | 0h         |    |

**Table 3-1299. EPWM\_DEACTCTL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                           |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | RESERVED_3 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                              |
| 16    | TRIPENABLE | R/W  | 0h    | 0 : PWMTRIP does not bypass the diode emulation logic.<br>1 : PWMTRIP bypasses the diode emulation PWM generation logic [not complete bypass of module]                                                                                                                                               |
| 15:7  | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                              |
| 6     | TRIPSELB   | R/W  | 0h    | 0 : TRIPH<br>1 : TRIPL                                                                                                                                                                                                                                                                                |
| 5:4   | PWMB       | R/W  | 0h    | 00 : synchronized version of TRIPH or TRIPL signal as selected by the TRIPSELB<br>01 : synchronized and inverted version of TRIPH or TRIPL signal as selected by the TRIPSELB<br>10 : A constant 0 drives PWMB when DEACTIVE flag is set.<br>11 : A constant 1 drives PWMB when DEACTIVE flag is set. |
| 3     | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                              |
| 2     | TRIPSELA   | R/W  | 0h    | 0 : TRIPH<br>1 : TRIPL                                                                                                                                                                                                                                                                                |
| 1:0   | PWMA       | R/W  | 0h    | 00 : synchronized version of TRIPH or TRIPL signal as selected by the TRIPSELA<br>01 : synchronized and inverted version of TRIPH or TRIPL signal as selected by the TRIPSELA<br>10 : A constant 0 drives PWMA when DEACTIVE flag is set.<br>11 : A constant 1 drives PWMA when DEACTIVE flag is set. |

### 3.7.2.163 EPWM\_DESTS Register

#### 1 EPWM\_DESTS Register (Offset = 80Ch) [reset = 0h]

DE Status register.

Return to [Summary Table](#)

**Table 3-1300. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 080Ch       |
| EPWM0_G1      | 5004 080Ch       |
| EPWM0_G2      | 5008 080Ch       |
| EPWM0_G3      | 500C 080Ch       |
| EPWM1_G0      | 5000 180Ch       |
| EPWM1_G1      | 5004 180Ch       |
| EPWM1_G2      | 5008 180Ch       |
| EPWM1_G3      | 500C 180Ch       |
| EPWM2_G0      | 5000 280Ch       |
| EPWM2_G1      | 5004 280Ch       |
| EPWM2_G2      | 5008 280Ch       |
| EPWM2_G3      | 500C 280Ch       |
| EPWM3_G0      | 5000 380Ch       |
| EPWM3_G1      | 5004 380Ch       |
| EPWM3_G2      | 5008 380Ch       |
| EPWM3_G3      | 500C 380Ch       |
| EPWM4_G0      | 5000 480Ch       |
| EPWM4_G1      | 5004 480Ch       |
| EPWM4_G2      | 5008 480Ch       |
| EPWM4_G3      | 500C 480Ch       |
| EPWM5_G0      | 5000 580Ch       |
| EPWM5_G1      | 5004 580Ch       |
| EPWM5_G2      | 5008 580Ch       |
| EPWM5_G3      | 500C 580Ch       |
| EPWM6_G0      | 5000 680Ch       |
| EPWM6_G1      | 5004 680Ch       |
| EPWM6_G2      | 5008 680Ch       |
| EPWM6_G3      | 500C 680Ch       |
| EPWM7_G0      | 5000 780Ch       |
| EPWM7_G1      | 5004 780Ch       |
| EPWM7_G2      | 5008 780Ch       |
| EPWM7_G3      | 500C 780Ch       |
| EPWM8_G0      | 5000 880Ch       |
| EPWM8_G1      | 5004 880Ch       |
| EPWM8_G2      | 5008 880Ch       |
| EPWM8_G3      | 500C 880Ch       |
| EPWM9_G0      | 5000 980Ch       |
| EPWM9_G1      | 5004 980Ch       |
| EPWM9_G2      | 5008 980Ch       |



**Table 3-1300. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 980Ch       |
| EPWM10_G0     | 5000 A80Ch       |
| EPWM10_G1     | 5004 A80Ch       |
| EPWM10_G2     | 5008 A80Ch       |
| EPWM10_G3     | 500C A80Ch       |
| EPWM11_G0     | 5000 B80Ch       |
| EPWM11_G1     | 5004 B80Ch       |
| EPWM11_G2     | 5008 B80Ch       |
| EPWM11_G3     | 500C B80Ch       |
| EPWM12_G0     | 5000 C80Ch       |
| EPWM12_G1     | 5004 C80Ch       |
| EPWM12_G2     | 5008 C80Ch       |
| EPWM12_G3     | 500C C80Ch       |
| EPWM13_G0     | 5000 D80Ch       |
| EPWM13_G1     | 5004 D80Ch       |
| EPWM13_G2     | 5008 D80Ch       |
| EPWM13_G3     | 500C D80Ch       |
| EPWM14_G0     | 5000 E80Ch       |
| EPWM14_G1     | 5004 E80Ch       |
| EPWM14_G2     | 5008 E80Ch       |
| EPWM14_G3     | 500C E80Ch       |
| EPWM15_G0     | 5000 F80Ch       |
| EPWM15_G1     | 5004 F80Ch       |
| EPWM15_G2     | 5008 F80Ch       |
| EPWM15_G3     | 500C F80Ch       |
| EPWM16_G0     | 5001 080Ch       |
| EPWM16_G1     | 5005 080Ch       |
| EPWM16_G2     | 5009 080Ch       |
| EPWM16_G3     | 500D 080Ch       |
| EPWM17_G0     | 5001 180Ch       |
| EPWM17_G1     | 5005 180Ch       |
| EPWM17_G2     | 5009 180Ch       |
| EPWM17_G3     | 500D 180Ch       |
| EPWM18_G0     | 5001 280Ch       |
| EPWM18_G1     | 5005 280Ch       |
| EPWM18_G2     | 5009 280Ch       |
| EPWM18_G3     | 500D 280Ch       |
| EPWM19_G0     | 5001 380Ch       |
| EPWM19_G1     | 5005 380Ch       |
| EPWM19_G2     | 5009 380Ch       |
| EPWM19_G3     | 500D 380Ch       |
| EPWM20_G0     | 5001 480Ch       |
| EPWM20_G1     | 5005 480Ch       |
| EPWM20_G2     | 5009 480Ch       |
| EPWM20_G3     | 500D 480Ch       |

**Table 3-1300. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 580Ch       |
| EPWM21_G1     | 5005 580Ch       |
| EPWM21_G2     | 5009 580Ch       |
| EPWM21_G3     | 500D 580Ch       |
| EPWM22_G0     | 5001 680Ch       |
| EPWM22_G1     | 5005 680Ch       |
| EPWM22_G2     | 5009 680Ch       |
| EPWM22_G3     | 500D 680Ch       |
| EPWM23_G0     | 5001 780Ch       |
| EPWM23_G1     | 5005 780Ch       |
| EPWM23_G2     | 5009 780Ch       |
| EPWM23_G3     | 500D 780Ch       |
| EPWM24_G0     | 5001 880Ch       |
| EPWM24_G1     | 5005 880Ch       |
| EPWM24_G2     | 5009 880Ch       |
| EPWM24_G3     | 500D 880Ch       |
| EPWM25_G0     | 5001 980Ch       |
| EPWM25_G1     | 5005 980Ch       |
| EPWM25_G2     | 5009 980Ch       |
| EPWM25_G3     | 500D 980Ch       |
| EPWM26_G0     | 5001 A80Ch       |
| EPWM26_G1     | 5005 A80Ch       |
| EPWM26_G2     | 5009 A80Ch       |
| EPWM26_G3     | 500D A80Ch       |
| EPWM27_G0     | 5001 B80Ch       |
| EPWM27_G1     | 5005 B80Ch       |
| EPWM27_G2     | 5009 B80Ch       |
| EPWM27_G3     | 500D B80Ch       |
| EPWM28_G0     | 5001 C80Ch       |
| EPWM28_G1     | 5005 C80Ch       |
| EPWM28_G2     | 5009 C80Ch       |
| EPWM28_G3     | 500D C80Ch       |
| EPWM29_G0     | 5001 D80Ch       |
| EPWM29_G1     | 5005 D80Ch       |
| EPWM29_G2     | 5009 D80Ch       |
| EPWM29_G3     | 500D D80Ch       |
| EPWM30_G0     | 5001 E80Ch       |
| EPWM30_G1     | 5005 E80Ch       |
| EPWM30_G2     | 5009 E80Ch       |
| EPWM30_G3     | 500D E80Ch       |
| EPWM31_G0     | 5001 F80Ch       |
| EPWM31_G1     | 5005 F80Ch       |
| EPWM31_G2     | 5009 F80Ch       |
| EPWM31_G3     | 500D F80Ch       |

**Figure 3-414. EPWM\_DESTS Name Register**

|            |    |    |    |    |    |    |          |
|------------|----|----|----|----|----|----|----------|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24       |
| RESERVED_1 |    |    |    |    |    |    |          |
| R          |    |    |    |    |    |    |          |
| 0h         |    |    |    |    |    |    |          |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16       |
| RESERVED_1 |    |    |    |    |    |    |          |
| R          |    |    |    |    |    |    |          |
| 0h         |    |    |    |    |    |    |          |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8        |
| RESERVED_1 |    |    |    |    |    |    |          |
| R          |    |    |    |    |    |    |          |
| 0h         |    |    |    |    |    |    |          |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0        |
| RESERVED_1 |    |    |    |    |    |    | DEACTIVE |
| R          |    |    |    |    |    |    | R        |
| 0h         |    |    |    |    |    |    | 0h       |

**Table 3-1302. EPWM\_DESTS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                  |
|------|------------|------|-------|------------------------------------------------------------------------------|
| 31:1 | RESERVED_1 | R    | 0h    | Reserved                                                                     |
| 0    | DEACTIVE   | R    | 0h    | 0 : Diode emulation mode is not active<br>1 : Diode emulation mode is active |

### 3.7.2.164 EPWM\_DEFRC Register

#### 1 EPWM\_DEFRC Register (Offset = 810h) [reset = 0h]

DE Status force register.

Return to [Summary Table](#)

**Table 3-1303. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0810h       |
| EPWM0_G1      | 5004 0810h       |
| EPWM0_G2      | 5008 0810h       |
| EPWM0_G3      | 500C 0810h       |
| EPWM1_G0      | 5000 1810h       |
| EPWM1_G1      | 5004 1810h       |
| EPWM1_G2      | 5008 1810h       |
| EPWM1_G3      | 500C 1810h       |
| EPWM2_G0      | 5000 2810h       |
| EPWM2_G1      | 5004 2810h       |
| EPWM2_G2      | 5008 2810h       |
| EPWM2_G3      | 500C 2810h       |
| EPWM3_G0      | 5000 3810h       |
| EPWM3_G1      | 5004 3810h       |
| EPWM3_G2      | 5008 3810h       |
| EPWM3_G3      | 500C 3810h       |
| EPWM4_G0      | 5000 4810h       |
| EPWM4_G1      | 5004 4810h       |
| EPWM4_G2      | 5008 4810h       |
| EPWM4_G3      | 500C 4810h       |
| EPWM5_G0      | 5000 5810h       |
| EPWM5_G1      | 5004 5810h       |
| EPWM5_G2      | 5008 5810h       |
| EPWM5_G3      | 500C 5810h       |
| EPWM6_G0      | 5000 6810h       |
| EPWM6_G1      | 5004 6810h       |
| EPWM6_G2      | 5008 6810h       |
| EPWM6_G3      | 500C 6810h       |
| EPWM7_G0      | 5000 7810h       |
| EPWM7_G1      | 5004 7810h       |
| EPWM7_G2      | 5008 7810h       |
| EPWM7_G3      | 500C 7810h       |
| EPWM8_G0      | 5000 8810h       |
| EPWM8_G1      | 5004 8810h       |
| EPWM8_G2      | 5008 8810h       |
| EPWM8_G3      | 500C 8810h       |
| EPWM9_G0      | 5000 9810h       |
| EPWM9_G1      | 5004 9810h       |
| EPWM9_G2      | 5008 9810h       |

**Table 3-1303. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9810h       |
| EPWM10_G0     | 5000 A810h       |
| EPWM10_G1     | 5004 A810h       |
| EPWM10_G2     | 5008 A810h       |
| EPWM10_G3     | 500C A810h       |
| EPWM11_G0     | 5000 B810h       |
| EPWM11_G1     | 5004 B810h       |
| EPWM11_G2     | 5008 B810h       |
| EPWM11_G3     | 500C B810h       |
| EPWM12_G0     | 5000 C810h       |
| EPWM12_G1     | 5004 C810h       |
| EPWM12_G2     | 5008 C810h       |
| EPWM12_G3     | 500C C810h       |
| EPWM13_G0     | 5000 D810h       |
| EPWM13_G1     | 5004 D810h       |
| EPWM13_G2     | 5008 D810h       |
| EPWM13_G3     | 500C D810h       |
| EPWM14_G0     | 5000 E810h       |
| EPWM14_G1     | 5004 E810h       |
| EPWM14_G2     | 5008 E810h       |
| EPWM14_G3     | 500C E810h       |
| EPWM15_G0     | 5000 F810h       |
| EPWM15_G1     | 5004 F810h       |
| EPWM15_G2     | 5008 F810h       |
| EPWM15_G3     | 500C F810h       |
| EPWM16_G0     | 5001 0810h       |
| EPWM16_G1     | 5005 0810h       |
| EPWM16_G2     | 5009 0810h       |
| EPWM16_G3     | 500D 0810h       |
| EPWM17_G0     | 5001 1810h       |
| EPWM17_G1     | 5005 1810h       |
| EPWM17_G2     | 5009 1810h       |
| EPWM17_G3     | 500D 1810h       |
| EPWM18_G0     | 5001 2810h       |
| EPWM18_G1     | 5005 2810h       |
| EPWM18_G2     | 5009 2810h       |
| EPWM18_G3     | 500D 2810h       |
| EPWM19_G0     | 5001 3810h       |
| EPWM19_G1     | 5005 3810h       |
| EPWM19_G2     | 5009 3810h       |
| EPWM19_G3     | 500D 3810h       |
| EPWM20_G0     | 5001 4810h       |
| EPWM20_G1     | 5005 4810h       |
| EPWM20_G2     | 5009 4810h       |
| EPWM20_G3     | 500D 4810h       |

**Table 3-1303. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5810h       |
| EPWM21_G1     | 5005 5810h       |
| EPWM21_G2     | 5009 5810h       |
| EPWM21_G3     | 500D 5810h       |
| EPWM22_G0     | 5001 6810h       |
| EPWM22_G1     | 5005 6810h       |
| EPWM22_G2     | 5009 6810h       |
| EPWM22_G3     | 500D 6810h       |
| EPWM23_G0     | 5001 7810h       |
| EPWM23_G1     | 5005 7810h       |
| EPWM23_G2     | 5009 7810h       |
| EPWM23_G3     | 500D 7810h       |
| EPWM24_G0     | 5001 8810h       |
| EPWM24_G1     | 5005 8810h       |
| EPWM24_G2     | 5009 8810h       |
| EPWM24_G3     | 500D 8810h       |
| EPWM25_G0     | 5001 9810h       |
| EPWM25_G1     | 5005 9810h       |
| EPWM25_G2     | 5009 9810h       |
| EPWM25_G3     | 500D 9810h       |
| EPWM26_G0     | 5001 A810h       |
| EPWM26_G1     | 5005 A810h       |
| EPWM26_G2     | 5009 A810h       |
| EPWM26_G3     | 500D A810h       |
| EPWM27_G0     | 5001 B810h       |
| EPWM27_G1     | 5005 B810h       |
| EPWM27_G2     | 5009 B810h       |
| EPWM27_G3     | 500D B810h       |
| EPWM28_G0     | 5001 C810h       |
| EPWM28_G1     | 5005 C810h       |
| EPWM28_G2     | 5009 C810h       |
| EPWM28_G3     | 500D C810h       |
| EPWM29_G0     | 5001 D810h       |
| EPWM29_G1     | 5005 D810h       |
| EPWM29_G2     | 5009 D810h       |
| EPWM29_G3     | 500D D810h       |
| EPWM30_G0     | 5001 E810h       |
| EPWM30_G1     | 5005 E810h       |
| EPWM30_G2     | 5009 E810h       |
| EPWM30_G3     | 500D E810h       |
| EPWM31_G0     | 5001 F810h       |
| EPWM31_G1     | 5005 F810h       |
| EPWM31_G2     | 5009 F810h       |
| EPWM31_G3     | 500D F810h       |

**Figure 3-415. EPWM\_DEFRC Name Register**

|            |    |    |    |    |    |    |          |
|------------|----|----|----|----|----|----|----------|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24       |
| RESERVED_1 |    |    |    |    |    |    |          |
| R          |    |    |    |    |    |    |          |
| 0h         |    |    |    |    |    |    |          |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16       |
| RESERVED_1 |    |    |    |    |    |    |          |
| R          |    |    |    |    |    |    |          |
| 0h         |    |    |    |    |    |    |          |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8        |
| RESERVED_1 |    |    |    |    |    |    |          |
| R          |    |    |    |    |    |    |          |
| 0h         |    |    |    |    |    |    |          |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0        |
| RESERVED_1 |    |    |    |    |    |    | DEACTIVE |
| R          |    |    |    |    |    |    | R/W1TS   |
| 0h         |    |    |    |    |    |    | 0h       |

**Table 3-1305. EPWM\_DEFRC Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                      |
|------|------------|--------|-------|--------------------------------------------------|
| 31:1 | RESERVED_1 | R      | 0h    | Reserved                                         |
| 0    | DEACTIVE   | R/W1TS | 0h    | 0 : No effect.<br>1 : Forces DEACTIVE flag to 1. |

### 3.7.2.165 EPWM\_DECLR Register

#### 1 EPWM\_DECLR Register (Offset = 814h) [reset = 0h]

DE Status clear register.

Return to [Summary Table](#)

**Table 3-1306. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0814h       |
| EPWM0_G1      | 5004 0814h       |
| EPWM0_G2      | 5008 0814h       |
| EPWM0_G3      | 500C 0814h       |
| EPWM1_G0      | 5000 1814h       |
| EPWM1_G1      | 5004 1814h       |
| EPWM1_G2      | 5008 1814h       |
| EPWM1_G3      | 500C 1814h       |
| EPWM2_G0      | 5000 2814h       |
| EPWM2_G1      | 5004 2814h       |
| EPWM2_G2      | 5008 2814h       |
| EPWM2_G3      | 500C 2814h       |
| EPWM3_G0      | 5000 3814h       |
| EPWM3_G1      | 5004 3814h       |
| EPWM3_G2      | 5008 3814h       |
| EPWM3_G3      | 500C 3814h       |
| EPWM4_G0      | 5000 4814h       |
| EPWM4_G1      | 5004 4814h       |
| EPWM4_G2      | 5008 4814h       |
| EPWM4_G3      | 500C 4814h       |
| EPWM5_G0      | 5000 5814h       |
| EPWM5_G1      | 5004 5814h       |
| EPWM5_G2      | 5008 5814h       |
| EPWM5_G3      | 500C 5814h       |
| EPWM6_G0      | 5000 6814h       |
| EPWM6_G1      | 5004 6814h       |
| EPWM6_G2      | 5008 6814h       |
| EPWM6_G3      | 500C 6814h       |
| EPWM7_G0      | 5000 7814h       |
| EPWM7_G1      | 5004 7814h       |
| EPWM7_G2      | 5008 7814h       |
| EPWM7_G3      | 500C 7814h       |
| EPWM8_G0      | 5000 8814h       |
| EPWM8_G1      | 5004 8814h       |
| EPWM8_G2      | 5008 8814h       |
| EPWM8_G3      | 500C 8814h       |
| EPWM9_G0      | 5000 9814h       |
| EPWM9_G1      | 5004 9814h       |
| EPWM9_G2      | 5008 9814h       |



**Table 3-1306. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9814h       |
| EPWM10_G0     | 5000 A814h       |
| EPWM10_G1     | 5004 A814h       |
| EPWM10_G2     | 5008 A814h       |
| EPWM10_G3     | 500C A814h       |
| EPWM11_G0     | 5000 B814h       |
| EPWM11_G1     | 5004 B814h       |
| EPWM11_G2     | 5008 B814h       |
| EPWM11_G3     | 500C B814h       |
| EPWM12_G0     | 5000 C814h       |
| EPWM12_G1     | 5004 C814h       |
| EPWM12_G2     | 5008 C814h       |
| EPWM12_G3     | 500C C814h       |
| EPWM13_G0     | 5000 D814h       |
| EPWM13_G1     | 5004 D814h       |
| EPWM13_G2     | 5008 D814h       |
| EPWM13_G3     | 500C D814h       |
| EPWM14_G0     | 5000 E814h       |
| EPWM14_G1     | 5004 E814h       |
| EPWM14_G2     | 5008 E814h       |
| EPWM14_G3     | 500C E814h       |
| EPWM15_G0     | 5000 F814h       |
| EPWM15_G1     | 5004 F814h       |
| EPWM15_G2     | 5008 F814h       |
| EPWM15_G3     | 500C F814h       |
| EPWM16_G0     | 5001 0814h       |
| EPWM16_G1     | 5005 0814h       |
| EPWM16_G2     | 5009 0814h       |
| EPWM16_G3     | 500D 0814h       |
| EPWM17_G0     | 5001 1814h       |
| EPWM17_G1     | 5005 1814h       |
| EPWM17_G2     | 5009 1814h       |
| EPWM17_G3     | 500D 1814h       |
| EPWM18_G0     | 5001 2814h       |
| EPWM18_G1     | 5005 2814h       |
| EPWM18_G2     | 5009 2814h       |
| EPWM18_G3     | 500D 2814h       |
| EPWM19_G0     | 5001 3814h       |
| EPWM19_G1     | 5005 3814h       |
| EPWM19_G2     | 5009 3814h       |
| EPWM19_G3     | 500D 3814h       |
| EPWM20_G0     | 5001 4814h       |
| EPWM20_G1     | 5005 4814h       |
| EPWM20_G2     | 5009 4814h       |
| EPWM20_G3     | 500D 4814h       |

**Table 3-1306. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5814h       |
| EPWM21_G1     | 5005 5814h       |
| EPWM21_G2     | 5009 5814h       |
| EPWM21_G3     | 500D 5814h       |
| EPWM22_G0     | 5001 6814h       |
| EPWM22_G1     | 5005 6814h       |
| EPWM22_G2     | 5009 6814h       |
| EPWM22_G3     | 500D 6814h       |
| EPWM23_G0     | 5001 7814h       |
| EPWM23_G1     | 5005 7814h       |
| EPWM23_G2     | 5009 7814h       |
| EPWM23_G3     | 500D 7814h       |
| EPWM24_G0     | 5001 8814h       |
| EPWM24_G1     | 5005 8814h       |
| EPWM24_G2     | 5009 8814h       |
| EPWM24_G3     | 500D 8814h       |
| EPWM25_G0     | 5001 9814h       |
| EPWM25_G1     | 5005 9814h       |
| EPWM25_G2     | 5009 9814h       |
| EPWM25_G3     | 500D 9814h       |
| EPWM26_G0     | 5001 A814h       |
| EPWM26_G1     | 5005 A814h       |
| EPWM26_G2     | 5009 A814h       |
| EPWM26_G3     | 500D A814h       |
| EPWM27_G0     | 5001 B814h       |
| EPWM27_G1     | 5005 B814h       |
| EPWM27_G2     | 5009 B814h       |
| EPWM27_G3     | 500D B814h       |
| EPWM28_G0     | 5001 C814h       |
| EPWM28_G1     | 5005 C814h       |
| EPWM28_G2     | 5009 C814h       |
| EPWM28_G3     | 500D C814h       |
| EPWM29_G0     | 5001 D814h       |
| EPWM29_G1     | 5005 D814h       |
| EPWM29_G2     | 5009 D814h       |
| EPWM29_G3     | 500D D814h       |
| EPWM30_G0     | 5001 E814h       |
| EPWM30_G1     | 5005 E814h       |
| EPWM30_G2     | 5009 E814h       |
| EPWM30_G3     | 500D E814h       |
| EPWM31_G0     | 5001 F814h       |
| EPWM31_G1     | 5005 F814h       |
| EPWM31_G2     | 5009 F814h       |
| EPWM31_G3     | 500D F814h       |

**Figure 3-416. EPWM\_DECLR Name Register**

|            |    |    |    |    |    |    |          |
|------------|----|----|----|----|----|----|----------|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24       |
| RESERVED_1 |    |    |    |    |    |    |          |
| R          |    |    |    |    |    |    |          |
| 0h         |    |    |    |    |    |    |          |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16       |
| RESERVED_1 |    |    |    |    |    |    |          |
| R          |    |    |    |    |    |    |          |
| 0h         |    |    |    |    |    |    |          |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8        |
| RESERVED_1 |    |    |    |    |    |    |          |
| R          |    |    |    |    |    |    |          |
| 0h         |    |    |    |    |    |    |          |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0        |
| RESERVED_1 |    |    |    |    |    |    | DEACTIVE |
| R          |    |    |    |    |    |    | R/W1TS   |
| 0h         |    |    |    |    |    |    | 0h       |

**Table 3-1308. EPWM\_DECLR Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                 |
|------|------------|--------|-------|---------------------------------------------|
| 31:1 | RESERVED_1 | R      | 0h    | Reserved                                    |
| 0    | DEACTIVE   | R/W1TS | 0h    | 0 : No effect.<br>1 : Clears DEACTIVE flag. |

### 3.7.2.166 EPWM\_DEMONCNT Register

#### 1 EPWM\_DEMONCNT Register (Offset = 820h) [reset = 0h]

DE trip monitor counter.

Return to [Summary Table](#)

**Table 3-1309. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0820h       |
| EPWM0_G1      | 5004 0820h       |
| EPWM0_G2      | 5008 0820h       |
| EPWM0_G3      | 500C 0820h       |
| EPWM1_G0      | 5000 1820h       |
| EPWM1_G1      | 5004 1820h       |
| EPWM1_G2      | 5008 1820h       |
| EPWM1_G3      | 500C 1820h       |
| EPWM2_G0      | 5000 2820h       |
| EPWM2_G1      | 5004 2820h       |
| EPWM2_G2      | 5008 2820h       |
| EPWM2_G3      | 500C 2820h       |
| EPWM3_G0      | 5000 3820h       |
| EPWM3_G1      | 5004 3820h       |
| EPWM3_G2      | 5008 3820h       |
| EPWM3_G3      | 500C 3820h       |
| EPWM4_G0      | 5000 4820h       |
| EPWM4_G1      | 5004 4820h       |
| EPWM4_G2      | 5008 4820h       |
| EPWM4_G3      | 500C 4820h       |
| EPWM5_G0      | 5000 5820h       |
| EPWM5_G1      | 5004 5820h       |
| EPWM5_G2      | 5008 5820h       |
| EPWM5_G3      | 500C 5820h       |
| EPWM6_G0      | 5000 6820h       |
| EPWM6_G1      | 5004 6820h       |
| EPWM6_G2      | 5008 6820h       |
| EPWM6_G3      | 500C 6820h       |
| EPWM7_G0      | 5000 7820h       |
| EPWM7_G1      | 5004 7820h       |
| EPWM7_G2      | 5008 7820h       |
| EPWM7_G3      | 500C 7820h       |
| EPWM8_G0      | 5000 8820h       |
| EPWM8_G1      | 5004 8820h       |
| EPWM8_G2      | 5008 8820h       |
| EPWM8_G3      | 500C 8820h       |
| EPWM9_G0      | 5000 9820h       |
| EPWM9_G1      | 5004 9820h       |
| EPWM9_G2      | 5008 9820h       |

**Table 3-1309. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9820h       |
| EPWM10_G0     | 5000 A820h       |
| EPWM10_G1     | 5004 A820h       |
| EPWM10_G2     | 5008 A820h       |
| EPWM10_G3     | 500C A820h       |
| EPWM11_G0     | 5000 B820h       |
| EPWM11_G1     | 5004 B820h       |
| EPWM11_G2     | 5008 B820h       |
| EPWM11_G3     | 500C B820h       |
| EPWM12_G0     | 5000 C820h       |
| EPWM12_G1     | 5004 C820h       |
| EPWM12_G2     | 5008 C820h       |
| EPWM12_G3     | 500C C820h       |
| EPWM13_G0     | 5000 D820h       |
| EPWM13_G1     | 5004 D820h       |
| EPWM13_G2     | 5008 D820h       |
| EPWM13_G3     | 500C D820h       |
| EPWM14_G0     | 5000 E820h       |
| EPWM14_G1     | 5004 E820h       |
| EPWM14_G2     | 5008 E820h       |
| EPWM14_G3     | 500C E820h       |
| EPWM15_G0     | 5000 F820h       |
| EPWM15_G1     | 5004 F820h       |
| EPWM15_G2     | 5008 F820h       |
| EPWM15_G3     | 500C F820h       |
| EPWM16_G0     | 5001 0820h       |
| EPWM16_G1     | 5005 0820h       |
| EPWM16_G2     | 5009 0820h       |
| EPWM16_G3     | 500D 0820h       |
| EPWM17_G0     | 5001 1820h       |
| EPWM17_G1     | 5005 1820h       |
| EPWM17_G2     | 5009 1820h       |
| EPWM17_G3     | 500D 1820h       |
| EPWM18_G0     | 5001 2820h       |
| EPWM18_G1     | 5005 2820h       |
| EPWM18_G2     | 5009 2820h       |
| EPWM18_G3     | 500D 2820h       |
| EPWM19_G0     | 5001 3820h       |
| EPWM19_G1     | 5005 3820h       |
| EPWM19_G2     | 5009 3820h       |
| EPWM19_G3     | 500D 3820h       |
| EPWM20_G0     | 5001 4820h       |
| EPWM20_G1     | 5005 4820h       |
| EPWM20_G2     | 5009 4820h       |
| EPWM20_G3     | 500D 4820h       |

**Table 3-1309. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5820h       |
| EPWM21_G1     | 5005 5820h       |
| EPWM21_G2     | 5009 5820h       |
| EPWM21_G3     | 500D 5820h       |
| EPWM22_G0     | 5001 6820h       |
| EPWM22_G1     | 5005 6820h       |
| EPWM22_G2     | 5009 6820h       |
| EPWM22_G3     | 500D 6820h       |
| EPWM23_G0     | 5001 7820h       |
| EPWM23_G1     | 5005 7820h       |
| EPWM23_G2     | 5009 7820h       |
| EPWM23_G3     | 500D 7820h       |
| EPWM24_G0     | 5001 8820h       |
| EPWM24_G1     | 5005 8820h       |
| EPWM24_G2     | 5009 8820h       |
| EPWM24_G3     | 500D 8820h       |
| EPWM25_G0     | 5001 9820h       |
| EPWM25_G1     | 5005 9820h       |
| EPWM25_G2     | 5009 9820h       |
| EPWM25_G3     | 500D 9820h       |
| EPWM26_G0     | 5001 A820h       |
| EPWM26_G1     | 5005 A820h       |
| EPWM26_G2     | 5009 A820h       |
| EPWM26_G3     | 500D A820h       |
| EPWM27_G0     | 5001 B820h       |
| EPWM27_G1     | 5005 B820h       |
| EPWM27_G2     | 5009 B820h       |
| EPWM27_G3     | 500D B820h       |
| EPWM28_G0     | 5001 C820h       |
| EPWM28_G1     | 5005 C820h       |
| EPWM28_G2     | 5009 C820h       |
| EPWM28_G3     | 500D C820h       |
| EPWM29_G0     | 5001 D820h       |
| EPWM29_G1     | 5005 D820h       |
| EPWM29_G2     | 5009 D820h       |
| EPWM29_G3     | 500D D820h       |
| EPWM30_G0     | 5001 E820h       |
| EPWM30_G1     | 5005 E820h       |
| EPWM30_G2     | 5009 E820h       |
| EPWM30_G3     | 500D E820h       |
| EPWM31_G0     | 5001 F820h       |
| EPWM31_G1     | 5005 F820h       |
| EPWM31_G2     | 5009 F820h       |
| EPWM31_G3     | 500D F820h       |

**Figure 3-417. EPWM\_DEMONCNT Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_1 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_1 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CNT        |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CNT        |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 3-1311. EPWM\_DEMONCNT Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | CNT        | R    | 0h    | An 16-bit counter which monitors the frequency of diode mode trip events.<br>When TripHorTripL is active: Increment CNT [increment INCSTEP on every EPWMxSYNC]<br>When TripHorTripL is in-active: Decrement CNT [decrement DECSTEP on every EPWMxSYNC]<br>If[ CNT > THRESHOLD] then generate DETRIP and clear the counter.<br>If[ [CNT - DECSTEP] < 0] then CNT = 0<br>If[ [CNT + INCSTEP] >= 0xFFFF] then CNT = 0xFFFF<br>Note : CNT is cleared when DECTL.ENABLE is 0<br>Note: DEMONTHRES == 0x0 should not generate trip as the DEMONTHRES and DEMONCNT registers have reset value of 0x0 |

### 3.7.2.167 EPWM\_DEMONCTL Register

#### 1 EPWM\_DEMONCTL Register (Offset = 824h) [reset = 0h]

DE monitor mode control.

Return to [Summary Table](#)

**Table 3-1312. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0824h       |
| EPWM0_G1      | 5004 0824h       |
| EPWM0_G2      | 5008 0824h       |
| EPWM0_G3      | 500C 0824h       |
| EPWM1_G0      | 5000 1824h       |
| EPWM1_G1      | 5004 1824h       |
| EPWM1_G2      | 5008 1824h       |
| EPWM1_G3      | 500C 1824h       |
| EPWM2_G0      | 5000 2824h       |
| EPWM2_G1      | 5004 2824h       |
| EPWM2_G2      | 5008 2824h       |
| EPWM2_G3      | 500C 2824h       |
| EPWM3_G0      | 5000 3824h       |
| EPWM3_G1      | 5004 3824h       |
| EPWM3_G2      | 5008 3824h       |
| EPWM3_G3      | 500C 3824h       |
| EPWM4_G0      | 5000 4824h       |
| EPWM4_G1      | 5004 4824h       |
| EPWM4_G2      | 5008 4824h       |
| EPWM4_G3      | 500C 4824h       |
| EPWM5_G0      | 5000 5824h       |
| EPWM5_G1      | 5004 5824h       |
| EPWM5_G2      | 5008 5824h       |
| EPWM5_G3      | 500C 5824h       |
| EPWM6_G0      | 5000 6824h       |
| EPWM6_G1      | 5004 6824h       |
| EPWM6_G2      | 5008 6824h       |
| EPWM6_G3      | 500C 6824h       |
| EPWM7_G0      | 5000 7824h       |
| EPWM7_G1      | 5004 7824h       |
| EPWM7_G2      | 5008 7824h       |
| EPWM7_G3      | 500C 7824h       |
| EPWM8_G0      | 5000 8824h       |
| EPWM8_G1      | 5004 8824h       |
| EPWM8_G2      | 5008 8824h       |
| EPWM8_G3      | 500C 8824h       |
| EPWM9_G0      | 5000 9824h       |
| EPWM9_G1      | 5004 9824h       |
| EPWM9_G2      | 5008 9824h       |



**Table 3-1312. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9824h       |
| EPWM10_G0     | 5000 A824h       |
| EPWM10_G1     | 5004 A824h       |
| EPWM10_G2     | 5008 A824h       |
| EPWM10_G3     | 500C A824h       |
| EPWM11_G0     | 5000 B824h       |
| EPWM11_G1     | 5004 B824h       |
| EPWM11_G2     | 5008 B824h       |
| EPWM11_G3     | 500C B824h       |
| EPWM12_G0     | 5000 C824h       |
| EPWM12_G1     | 5004 C824h       |
| EPWM12_G2     | 5008 C824h       |
| EPWM12_G3     | 500C C824h       |
| EPWM13_G0     | 5000 D824h       |
| EPWM13_G1     | 5004 D824h       |
| EPWM13_G2     | 5008 D824h       |
| EPWM13_G3     | 500C D824h       |
| EPWM14_G0     | 5000 E824h       |
| EPWM14_G1     | 5004 E824h       |
| EPWM14_G2     | 5008 E824h       |
| EPWM14_G3     | 500C E824h       |
| EPWM15_G0     | 5000 F824h       |
| EPWM15_G1     | 5004 F824h       |
| EPWM15_G2     | 5008 F824h       |
| EPWM15_G3     | 500C F824h       |
| EPWM16_G0     | 5001 0824h       |
| EPWM16_G1     | 5005 0824h       |
| EPWM16_G2     | 5009 0824h       |
| EPWM16_G3     | 500D 0824h       |
| EPWM17_G0     | 5001 1824h       |
| EPWM17_G1     | 5005 1824h       |
| EPWM17_G2     | 5009 1824h       |
| EPWM17_G3     | 500D 1824h       |
| EPWM18_G0     | 5001 2824h       |
| EPWM18_G1     | 5005 2824h       |
| EPWM18_G2     | 5009 2824h       |
| EPWM18_G3     | 500D 2824h       |
| EPWM19_G0     | 5001 3824h       |
| EPWM19_G1     | 5005 3824h       |
| EPWM19_G2     | 5009 3824h       |
| EPWM19_G3     | 500D 3824h       |
| EPWM20_G0     | 5001 4824h       |
| EPWM20_G1     | 5005 4824h       |
| EPWM20_G2     | 5009 4824h       |
| EPWM20_G3     | 500D 4824h       |

**Table 3-1312. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5824h       |
| EPWM21_G1     | 5005 5824h       |
| EPWM21_G2     | 5009 5824h       |
| EPWM21_G3     | 500D 5824h       |
| EPWM22_G0     | 5001 6824h       |
| EPWM22_G1     | 5005 6824h       |
| EPWM22_G2     | 5009 6824h       |
| EPWM22_G3     | 500D 6824h       |
| EPWM23_G0     | 5001 7824h       |
| EPWM23_G1     | 5005 7824h       |
| EPWM23_G2     | 5009 7824h       |
| EPWM23_G3     | 500D 7824h       |
| EPWM24_G0     | 5001 8824h       |
| EPWM24_G1     | 5005 8824h       |
| EPWM24_G2     | 5009 8824h       |
| EPWM24_G3     | 500D 8824h       |
| EPWM25_G0     | 5001 9824h       |
| EPWM25_G1     | 5005 9824h       |
| EPWM25_G2     | 5009 9824h       |
| EPWM25_G3     | 500D 9824h       |
| EPWM26_G0     | 5001 A824h       |
| EPWM26_G1     | 5005 A824h       |
| EPWM26_G2     | 5009 A824h       |
| EPWM26_G3     | 500D A824h       |
| EPWM27_G0     | 5001 B824h       |
| EPWM27_G1     | 5005 B824h       |
| EPWM27_G2     | 5009 B824h       |
| EPWM27_G3     | 500D B824h       |
| EPWM28_G0     | 5001 C824h       |
| EPWM28_G1     | 5005 C824h       |
| EPWM28_G2     | 5009 C824h       |
| EPWM28_G3     | 500D C824h       |
| EPWM29_G0     | 5001 D824h       |
| EPWM29_G1     | 5005 D824h       |
| EPWM29_G2     | 5009 D824h       |
| EPWM29_G3     | 500D D824h       |
| EPWM30_G0     | 5001 E824h       |
| EPWM30_G1     | 5005 E824h       |
| EPWM30_G2     | 5009 E824h       |
| EPWM30_G3     | 500D E824h       |
| EPWM31_G0     | 5001 F824h       |
| EPWM31_G1     | 5005 F824h       |
| EPWM31_G2     | 5009 F824h       |
| EPWM31_G3     | 500D F824h       |

**Figure 3-418. EPWM\_DEMONCTL Name Register**

|            |    |    |    |    |    |    |        |
|------------|----|----|----|----|----|----|--------|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24     |
| RESERVED_1 |    |    |    |    |    |    |        |
| R          |    |    |    |    |    |    |        |
| 0h         |    |    |    |    |    |    |        |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16     |
| RESERVED_1 |    |    |    |    |    |    |        |
| R          |    |    |    |    |    |    |        |
| 0h         |    |    |    |    |    |    |        |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8      |
| RESERVED_1 |    |    |    |    |    |    |        |
| R          |    |    |    |    |    |    |        |
| 0h         |    |    |    |    |    |    |        |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0      |
| RESERVED_1 |    |    |    |    |    |    | ENABLE |
| R          |    |    |    |    |    |    | R/W    |
| 0h         |    |    |    |    |    |    | 0h     |

**Table 3-1314. EPWM\_DEMONCTL Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                         |
|------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                            |
| 0    | ENABLE     | R/W  | 0h    | Enable bit for DE Mode Monitor counter function.<br>0:DE Mode Monitor counter function is disabled<br>1:DE Mode Monitor counter function is enabled |

### 3.7.2.168 EPWM\_DEMONSTEP Register

#### 1 EPWM\_DEMONSTEP Register (Offset = 828h) [reset = 0h]

DE monitor counter step.

Return to [Summary Table](#)

**Table 3-1315. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0828h       |
| EPWM0_G1      | 5004 0828h       |
| EPWM0_G2      | 5008 0828h       |
| EPWM0_G3      | 500C 0828h       |
| EPWM1_G0      | 5000 1828h       |
| EPWM1_G1      | 5004 1828h       |
| EPWM1_G2      | 5008 1828h       |
| EPWM1_G3      | 500C 1828h       |
| EPWM2_G0      | 5000 2828h       |
| EPWM2_G1      | 5004 2828h       |
| EPWM2_G2      | 5008 2828h       |
| EPWM2_G3      | 500C 2828h       |
| EPWM3_G0      | 5000 3828h       |
| EPWM3_G1      | 5004 3828h       |
| EPWM3_G2      | 5008 3828h       |
| EPWM3_G3      | 500C 3828h       |
| EPWM4_G0      | 5000 4828h       |
| EPWM4_G1      | 5004 4828h       |
| EPWM4_G2      | 5008 4828h       |
| EPWM4_G3      | 500C 4828h       |
| EPWM5_G0      | 5000 5828h       |
| EPWM5_G1      | 5004 5828h       |
| EPWM5_G2      | 5008 5828h       |
| EPWM5_G3      | 500C 5828h       |
| EPWM6_G0      | 5000 6828h       |
| EPWM6_G1      | 5004 6828h       |
| EPWM6_G2      | 5008 6828h       |
| EPWM6_G3      | 500C 6828h       |
| EPWM7_G0      | 5000 7828h       |
| EPWM7_G1      | 5004 7828h       |
| EPWM7_G2      | 5008 7828h       |
| EPWM7_G3      | 500C 7828h       |
| EPWM8_G0      | 5000 8828h       |
| EPWM8_G1      | 5004 8828h       |
| EPWM8_G2      | 5008 8828h       |
| EPWM8_G3      | 500C 8828h       |
| EPWM9_G0      | 5000 9828h       |
| EPWM9_G1      | 5004 9828h       |
| EPWM9_G2      | 5008 9828h       |

**Table 3-1315. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9828h       |
| EPWM10_G0     | 5000 A828h       |
| EPWM10_G1     | 5004 A828h       |
| EPWM10_G2     | 5008 A828h       |
| EPWM10_G3     | 500C A828h       |
| EPWM11_G0     | 5000 B828h       |
| EPWM11_G1     | 5004 B828h       |
| EPWM11_G2     | 5008 B828h       |
| EPWM11_G3     | 500C B828h       |
| EPWM12_G0     | 5000 C828h       |
| EPWM12_G1     | 5004 C828h       |
| EPWM12_G2     | 5008 C828h       |
| EPWM12_G3     | 500C C828h       |
| EPWM13_G0     | 5000 D828h       |
| EPWM13_G1     | 5004 D828h       |
| EPWM13_G2     | 5008 D828h       |
| EPWM13_G3     | 500C D828h       |
| EPWM14_G0     | 5000 E828h       |
| EPWM14_G1     | 5004 E828h       |
| EPWM14_G2     | 5008 E828h       |
| EPWM14_G3     | 500C E828h       |
| EPWM15_G0     | 5000 F828h       |
| EPWM15_G1     | 5004 F828h       |
| EPWM15_G2     | 5008 F828h       |
| EPWM15_G3     | 500C F828h       |
| EPWM16_G0     | 5001 0828h       |
| EPWM16_G1     | 5005 0828h       |
| EPWM16_G2     | 5009 0828h       |
| EPWM16_G3     | 500D 0828h       |
| EPWM17_G0     | 5001 1828h       |
| EPWM17_G1     | 5005 1828h       |
| EPWM17_G2     | 5009 1828h       |
| EPWM17_G3     | 500D 1828h       |
| EPWM18_G0     | 5001 2828h       |
| EPWM18_G1     | 5005 2828h       |
| EPWM18_G2     | 5009 2828h       |
| EPWM18_G3     | 500D 2828h       |
| EPWM19_G0     | 5001 3828h       |
| EPWM19_G1     | 5005 3828h       |
| EPWM19_G2     | 5009 3828h       |
| EPWM19_G3     | 500D 3828h       |
| EPWM20_G0     | 5001 4828h       |
| EPWM20_G1     | 5005 4828h       |
| EPWM20_G2     | 5009 4828h       |
| EPWM20_G3     | 500D 4828h       |

**Table 3-1315. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5828h       |
| EPWM21_G1     | 5005 5828h       |
| EPWM21_G2     | 5009 5828h       |
| EPWM21_G3     | 500D 5828h       |
| EPWM22_G0     | 5001 6828h       |
| EPWM22_G1     | 5005 6828h       |
| EPWM22_G2     | 5009 6828h       |
| EPWM22_G3     | 500D 6828h       |
| EPWM23_G0     | 5001 7828h       |
| EPWM23_G1     | 5005 7828h       |
| EPWM23_G2     | 5009 7828h       |
| EPWM23_G3     | 500D 7828h       |
| EPWM24_G0     | 5001 8828h       |
| EPWM24_G1     | 5005 8828h       |
| EPWM24_G2     | 5009 8828h       |
| EPWM24_G3     | 500D 8828h       |
| EPWM25_G0     | 5001 9828h       |
| EPWM25_G1     | 5005 9828h       |
| EPWM25_G2     | 5009 9828h       |
| EPWM25_G3     | 500D 9828h       |
| EPWM26_G0     | 5001 A828h       |
| EPWM26_G1     | 5005 A828h       |
| EPWM26_G2     | 5009 A828h       |
| EPWM26_G3     | 500D A828h       |
| EPWM27_G0     | 5001 B828h       |
| EPWM27_G1     | 5005 B828h       |
| EPWM27_G2     | 5009 B828h       |
| EPWM27_G3     | 500D B828h       |
| EPWM28_G0     | 5001 C828h       |
| EPWM28_G1     | 5005 C828h       |
| EPWM28_G2     | 5009 C828h       |
| EPWM28_G3     | 500D C828h       |
| EPWM29_G0     | 5001 D828h       |
| EPWM29_G1     | 5005 D828h       |
| EPWM29_G2     | 5009 D828h       |
| EPWM29_G3     | 500D D828h       |
| EPWM30_G0     | 5001 E828h       |
| EPWM30_G1     | 5005 E828h       |
| EPWM30_G2     | 5009 E828h       |
| EPWM30_G3     | 500D E828h       |
| EPWM31_G0     | 5001 F828h       |
| EPWM31_G1     | 5005 F828h       |
| EPWM31_G2     | 5009 F828h       |
| EPWM31_G3     | 500D F828h       |

**Figure 3-419. EPWM\_DEMONSTEP Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_2 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DECSTEP    |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_1 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INCSTEP    |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 3-1317. EPWM\_DEMONSTEP Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                         |
|-------|------------|------|-------|-----------------------------------------------------|
| 31:24 | RESERVED_2 | R    | 0h    | Reserved                                            |
| 23:16 | DECSTEP    | R/W  | 0h    | Defines the decrement step of DEMONCNT.CNT counter. |
| 15:8  | RESERVED_1 | R    | 0h    | Reserved                                            |
| 7:0   | INCSTEP    | R/W  | 0h    | Defines the increment step of DEMONCNT.CNT counter. |

### 3.7.2.169 EPWM\_DEMONTHRES Register

#### 1 EPWM\_DEMONTHRES Register (Offset = 82Ch) [reset = 0h]

DE monitor counter threshold.

Return to [Summary Table](#)

**Table 3-1318. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 082Ch       |
| EPWM0_G1      | 5004 082Ch       |
| EPWM0_G2      | 5008 082Ch       |
| EPWM0_G3      | 500C 082Ch       |
| EPWM1_G0      | 5000 182Ch       |
| EPWM1_G1      | 5004 182Ch       |
| EPWM1_G2      | 5008 182Ch       |
| EPWM1_G3      | 500C 182Ch       |
| EPWM2_G0      | 5000 282Ch       |
| EPWM2_G1      | 5004 282Ch       |
| EPWM2_G2      | 5008 282Ch       |
| EPWM2_G3      | 500C 282Ch       |
| EPWM3_G0      | 5000 382Ch       |
| EPWM3_G1      | 5004 382Ch       |
| EPWM3_G2      | 5008 382Ch       |
| EPWM3_G3      | 500C 382Ch       |
| EPWM4_G0      | 5000 482Ch       |
| EPWM4_G1      | 5004 482Ch       |
| EPWM4_G2      | 5008 482Ch       |
| EPWM4_G3      | 500C 482Ch       |
| EPWM5_G0      | 5000 582Ch       |
| EPWM5_G1      | 5004 582Ch       |
| EPWM5_G2      | 5008 582Ch       |
| EPWM5_G3      | 500C 582Ch       |
| EPWM6_G0      | 5000 682Ch       |
| EPWM6_G1      | 5004 682Ch       |
| EPWM6_G2      | 5008 682Ch       |
| EPWM6_G3      | 500C 682Ch       |
| EPWM7_G0      | 5000 782Ch       |
| EPWM7_G1      | 5004 782Ch       |
| EPWM7_G2      | 5008 782Ch       |
| EPWM7_G3      | 500C 782Ch       |
| EPWM8_G0      | 5000 882Ch       |
| EPWM8_G1      | 5004 882Ch       |
| EPWM8_G2      | 5008 882Ch       |
| EPWM8_G3      | 500C 882Ch       |
| EPWM9_G0      | 5000 982Ch       |
| EPWM9_G1      | 5004 982Ch       |
| EPWM9_G2      | 5008 982Ch       |



**Table 3-1318. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 982Ch       |
| EPWM10_G0     | 5000 A82Ch       |
| EPWM10_G1     | 5004 A82Ch       |
| EPWM10_G2     | 5008 A82Ch       |
| EPWM10_G3     | 500C A82Ch       |
| EPWM11_G0     | 5000 B82Ch       |
| EPWM11_G1     | 5004 B82Ch       |
| EPWM11_G2     | 5008 B82Ch       |
| EPWM11_G3     | 500C B82Ch       |
| EPWM12_G0     | 5000 C82Ch       |
| EPWM12_G1     | 5004 C82Ch       |
| EPWM12_G2     | 5008 C82Ch       |
| EPWM12_G3     | 500C C82Ch       |
| EPWM13_G0     | 5000 D82Ch       |
| EPWM13_G1     | 5004 D82Ch       |
| EPWM13_G2     | 5008 D82Ch       |
| EPWM13_G3     | 500C D82Ch       |
| EPWM14_G0     | 5000 E82Ch       |
| EPWM14_G1     | 5004 E82Ch       |
| EPWM14_G2     | 5008 E82Ch       |
| EPWM14_G3     | 500C E82Ch       |
| EPWM15_G0     | 5000 F82Ch       |
| EPWM15_G1     | 5004 F82Ch       |
| EPWM15_G2     | 5008 F82Ch       |
| EPWM15_G3     | 500C F82Ch       |
| EPWM16_G0     | 5001 082Ch       |
| EPWM16_G1     | 5005 082Ch       |
| EPWM16_G2     | 5009 082Ch       |
| EPWM16_G3     | 500D 082Ch       |
| EPWM17_G0     | 5001 182Ch       |
| EPWM17_G1     | 5005 182Ch       |
| EPWM17_G2     | 5009 182Ch       |
| EPWM17_G3     | 500D 182Ch       |
| EPWM18_G0     | 5001 282Ch       |
| EPWM18_G1     | 5005 282Ch       |
| EPWM18_G2     | 5009 282Ch       |
| EPWM18_G3     | 500D 282Ch       |
| EPWM19_G0     | 5001 382Ch       |
| EPWM19_G1     | 5005 382Ch       |
| EPWM19_G2     | 5009 382Ch       |
| EPWM19_G3     | 500D 382Ch       |
| EPWM20_G0     | 5001 482Ch       |
| EPWM20_G1     | 5005 482Ch       |
| EPWM20_G2     | 5009 482Ch       |
| EPWM20_G3     | 500D 482Ch       |

**Table 3-1318. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 582Ch       |
| EPWM21_G1     | 5005 582Ch       |
| EPWM21_G2     | 5009 582Ch       |
| EPWM21_G3     | 500D 582Ch       |
| EPWM22_G0     | 5001 682Ch       |
| EPWM22_G1     | 5005 682Ch       |
| EPWM22_G2     | 5009 682Ch       |
| EPWM22_G3     | 500D 682Ch       |
| EPWM23_G0     | 5001 782Ch       |
| EPWM23_G1     | 5005 782Ch       |
| EPWM23_G2     | 5009 782Ch       |
| EPWM23_G3     | 500D 782Ch       |
| EPWM24_G0     | 5001 882Ch       |
| EPWM24_G1     | 5005 882Ch       |
| EPWM24_G2     | 5009 882Ch       |
| EPWM24_G3     | 500D 882Ch       |
| EPWM25_G0     | 5001 982Ch       |
| EPWM25_G1     | 5005 982Ch       |
| EPWM25_G2     | 5009 982Ch       |
| EPWM25_G3     | 500D 982Ch       |
| EPWM26_G0     | 5001 A82Ch       |
| EPWM26_G1     | 5005 A82Ch       |
| EPWM26_G2     | 5009 A82Ch       |
| EPWM26_G3     | 500D A82Ch       |
| EPWM27_G0     | 5001 B82Ch       |
| EPWM27_G1     | 5005 B82Ch       |
| EPWM27_G2     | 5009 B82Ch       |
| EPWM27_G3     | 500D B82Ch       |
| EPWM28_G0     | 5001 C82Ch       |
| EPWM28_G1     | 5005 C82Ch       |
| EPWM28_G2     | 5009 C82Ch       |
| EPWM28_G3     | 500D C82Ch       |
| EPWM29_G0     | 5001 D82Ch       |
| EPWM29_G1     | 5005 D82Ch       |
| EPWM29_G2     | 5009 D82Ch       |
| EPWM29_G3     | 500D D82Ch       |
| EPWM30_G0     | 5001 E82Ch       |
| EPWM30_G1     | 5005 E82Ch       |
| EPWM30_G2     | 5009 E82Ch       |
| EPWM30_G3     | 500D E82Ch       |
| EPWM31_G0     | 5001 F82Ch       |
| EPWM31_G1     | 5005 F82Ch       |
| EPWM31_G2     | 5009 F82Ch       |
| EPWM31_G3     | 500D F82Ch       |

**Figure 3-420. EPWM\_DEMONTHRES Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_1 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_1 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| THRESHOLD  |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| THRESHOLD  |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 3-1320. EPWM\_DEMONTHRES Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                  |
|-------|------------|------|-------|----------------------------------------------|
| 31:16 | RESERVED_1 | R    | 0h    | Reserved                                     |
| 15:0  | THRESHOLD  | R/W  | 0h    | Defines the threshold of DE monitor counter. |

### 3.7.2.170 EPWM\_MINDBCFCFG Register

#### 1 EPWM\_MINDBCFCFG Register (Offset = C00h) [reset = 0h]

Minimum dead band configuration register.

Return to [Summary Table](#)

**Table 3-1321. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0C00h       |
| EPWM0_G1      | 5004 0C00h       |
| EPWM0_G2      | 5008 0C00h       |
| EPWM0_G3      | 500C 0C00h       |
| EPWM1_G0      | 5000 1C00h       |
| EPWM1_G1      | 5004 1C00h       |
| EPWM1_G2      | 5008 1C00h       |
| EPWM1_G3      | 500C 1C00h       |
| EPWM2_G0      | 5000 2C00h       |
| EPWM2_G1      | 5004 2C00h       |
| EPWM2_G2      | 5008 2C00h       |
| EPWM2_G3      | 500C 2C00h       |
| EPWM3_G0      | 5000 3C00h       |
| EPWM3_G1      | 5004 3C00h       |
| EPWM3_G2      | 5008 3C00h       |
| EPWM3_G3      | 500C 3C00h       |
| EPWM4_G0      | 5000 4C00h       |
| EPWM4_G1      | 5004 4C00h       |
| EPWM4_G2      | 5008 4C00h       |
| EPWM4_G3      | 500C 4C00h       |
| EPWM5_G0      | 5000 5C00h       |
| EPWM5_G1      | 5004 5C00h       |
| EPWM5_G2      | 5008 5C00h       |
| EPWM5_G3      | 500C 5C00h       |
| EPWM6_G0      | 5000 6C00h       |
| EPWM6_G1      | 5004 6C00h       |
| EPWM6_G2      | 5008 6C00h       |
| EPWM6_G3      | 500C 6C00h       |
| EPWM7_G0      | 5000 7C00h       |
| EPWM7_G1      | 5004 7C00h       |
| EPWM7_G2      | 5008 7C00h       |
| EPWM7_G3      | 500C 7C00h       |
| EPWM8_G0      | 5000 8C00h       |
| EPWM8_G1      | 5004 8C00h       |
| EPWM8_G2      | 5008 8C00h       |
| EPWM8_G3      | 500C 8C00h       |
| EPWM9_G0      | 5000 9C00h       |
| EPWM9_G1      | 5004 9C00h       |
| EPWM9_G2      | 5008 9C00h       |

**Table 3-1321. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9C00h       |
| EPWM10_G0     | 5000 AC00h       |
| EPWM10_G1     | 5004 AC00h       |
| EPWM10_G2     | 5008 AC00h       |
| EPWM10_G3     | 500C AC00h       |
| EPWM11_G0     | 5000 BC00h       |
| EPWM11_G1     | 5004 BC00h       |
| EPWM11_G2     | 5008 BC00h       |
| EPWM11_G3     | 500C BC00h       |
| EPWM12_G0     | 5000 CC00h       |
| EPWM12_G1     | 5004 CC00h       |
| EPWM12_G2     | 5008 CC00h       |
| EPWM12_G3     | 500C CC00h       |
| EPWM13_G0     | 5000 DC00h       |
| EPWM13_G1     | 5004 DC00h       |
| EPWM13_G2     | 5008 DC00h       |
| EPWM13_G3     | 500C DC00h       |
| EPWM14_G0     | 5000 EC00h       |
| EPWM14_G1     | 5004 EC00h       |
| EPWM14_G2     | 5008 EC00h       |
| EPWM14_G3     | 500C EC00h       |
| EPWM15_G0     | 5000 FC00h       |
| EPWM15_G1     | 5004 FC00h       |
| EPWM15_G2     | 5008 FC00h       |
| EPWM15_G3     | 500C FC00h       |
| EPWM16_G0     | 5001 0C00h       |
| EPWM16_G1     | 5005 0C00h       |
| EPWM16_G2     | 5009 0C00h       |
| EPWM16_G3     | 500D 0C00h       |
| EPWM17_G0     | 5001 1C00h       |
| EPWM17_G1     | 5005 1C00h       |
| EPWM17_G2     | 5009 1C00h       |
| EPWM17_G3     | 500D 1C00h       |
| EPWM18_G0     | 5001 2C00h       |
| EPWM18_G1     | 5005 2C00h       |
| EPWM18_G2     | 5009 2C00h       |
| EPWM18_G3     | 500D 2C00h       |
| EPWM19_G0     | 5001 3C00h       |
| EPWM19_G1     | 5005 3C00h       |
| EPWM19_G2     | 5009 3C00h       |
| EPWM19_G3     | 500D 3C00h       |
| EPWM20_G0     | 5001 4C00h       |
| EPWM20_G1     | 5005 4C00h       |
| EPWM20_G2     | 5009 4C00h       |
| EPWM20_G3     | 500D 4C00h       |

**Table 3-1321. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5C00h       |
| EPWM21_G1     | 5005 5C00h       |
| EPWM21_G2     | 5009 5C00h       |
| EPWM21_G3     | 500D 5C00h       |
| EPWM22_G0     | 5001 6C00h       |
| EPWM22_G1     | 5005 6C00h       |
| EPWM22_G2     | 5009 6C00h       |
| EPWM22_G3     | 500D 6C00h       |
| EPWM23_G0     | 5001 7C00h       |
| EPWM23_G1     | 5005 7C00h       |
| EPWM23_G2     | 5009 7C00h       |
| EPWM23_G3     | 500D 7C00h       |
| EPWM24_G0     | 5001 8C00h       |
| EPWM24_G1     | 5005 8C00h       |
| EPWM24_G2     | 5009 8C00h       |
| EPWM24_G3     | 500D 8C00h       |
| EPWM25_G0     | 5001 9C00h       |
| EPWM25_G1     | 5005 9C00h       |
| EPWM25_G2     | 5009 9C00h       |
| EPWM25_G3     | 500D 9C00h       |
| EPWM26_G0     | 5001 AC00h       |
| EPWM26_G1     | 5005 AC00h       |
| EPWM26_G2     | 5009 AC00h       |
| EPWM26_G3     | 500D AC00h       |
| EPWM27_G0     | 5001 BC00h       |
| EPWM27_G1     | 5005 BC00h       |
| EPWM27_G2     | 5009 BC00h       |
| EPWM27_G3     | 500D BC00h       |
| EPWM28_G0     | 5001 CC00h       |
| EPWM28_G1     | 5005 CC00h       |
| EPWM28_G2     | 5009 CC00h       |
| EPWM28_G3     | 500D CC00h       |
| EPWM29_G0     | 5001 DC00h       |
| EPWM29_G1     | 5005 DC00h       |
| EPWM29_G2     | 5009 DC00h       |
| EPWM29_G3     | 500D DC00h       |
| EPWM30_G0     | 5001 EC00h       |
| EPWM30_G1     | 5005 EC00h       |
| EPWM30_G2     | 5009 EC00h       |
| EPWM30_G3     | 500D EC00h       |
| EPWM31_G0     | 5001 FC00h       |
| EPWM31_G1     | 5005 FC00h       |
| EPWM31_G2     | 5009 FC00h       |
| EPWM31_G3     | 500D FC00h       |

**Figure 3-421. EPWM\_MINDBCFG Name Register**

|            |    |    |    |           |         |            |         |
|------------|----|----|----|-----------|---------|------------|---------|
| 31         | 30 | 29 | 28 | 27        | 26      | 25         | 24      |
| RESERVED_4 |    |    |    |           |         |            | POLSELB |
| R          |    |    |    |           |         |            | R/W     |
| 0h         |    |    |    |           |         |            | 0h      |
| 23         | 22 | 21 | 20 | 19        | 18      | 17         | 16      |
| SELB       |    |    |    | SELBLOCKB | INVERTB | RESERVED_3 | ENABLEB |
| R/W        |    |    |    | R/W       | R/W     | R          | R/W     |
| 0h         |    |    |    | 0h        | 0h      | 0h         | 0h      |
| 15         | 14 | 13 | 12 | 11        | 10      | 9          | 8       |
| RESERVED_2 |    |    |    |           |         |            | POLSELA |
| R          |    |    |    |           |         |            | R/W     |
| 0h         |    |    |    |           |         |            | 0h      |
| 7          | 6  | 5  | 4  | 3         | 2       | 1          | 0       |
| SELA       |    |    |    | SELBLOCKA | INVERTA | RESERVED_1 | ENABLEA |
| R/W        |    |    |    | R/W       | R/W     | R          | R/W     |
| 0h         |    |    |    | 0h        | 0h      | 0h         | 0h      |

**Table 3-1323. EPWM\_MINDBCFG Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                     |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:25 | RESERVED_4 | R    | 0h    | Reserved                                                                                                                                                                                        |
| 24    | POLSELB    | R/W  | 0h    | Select signal for the AND OR logic of BLOCKB [output of SELBLOCKB mux] and PWMB signals<br>0 : Select BLOCKB is inverted and ANDed with PWMB.<br>1 : Select BLOCKB is Ored with PWMB.           |
| 23:20 | SELB       | R/W  | 0h    | PWMB min dead band reference<br>0x0 : DEPWMB<br>0x1 : Output 1 from PWMXBAR<br>0x2 : Output 2 from PWMXBAR<br>.<br>.<br>0xf : Output 15 from PWMXBAR                                            |
| 19    | SELBLOCKB  | R/W  | 0h    | 0 : Select BLOCKB as the blocking signal on PWMB.<br>1 : Select BLOCKA as the blocking signal on PWMB.                                                                                          |
| 18    | INVERTB    | R/W  | 0h    | 0 : No inversion on the selected reference signal which is used in the min deadband logic on PWMB.<br>1 : Invert the selected reference signal which is used in the min deadband logic on PWMB. |
| 17    | RESERVED_3 | R    | 0h    | Reserved                                                                                                                                                                                        |
| 16    | ENABLEB    | R/W  | 0h    | 0 : Minimum dead band logic is disabled<br>1 : Minimum dead band logic is enabled                                                                                                               |
| 15:9  | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                        |
| 8     | POLSELA    | R/W  | 0h    | Select signal for the AND OR logic of BLOCKA [output of SELBLOCKA mux] and PWMA signals<br>0 : Select BLOCKA is inverted and ANDed with PWMA.<br>1 : Select BLOCKA is Ored with PWMA.           |
| 7:4   | SELA       | R/W  | 0h    | PWMA min dead band reference<br>0x0 : DEPWMA<br>0x1 : Output 1 from PWMXBAR<br>0x2 : Output 2 from PWMXBAR<br>.<br>.<br>0xf : Output 15 from PWMXBAR                                            |
| 3     | SELBLOCKA  | R/W  | 0h    | 0 : Select BLOCKA as the blocking signal on PWMA.<br>1 : Select BLOCKB as the blocking signal on PWMB.                                                                                          |

**Table 3-1323. EPWM\_MINDBCFCFG Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                     |
|-----|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | INVERTA    | R/W  | 0h    | 0 : No inversion on the selected reference signal which is used in the min deadband logic on PWMA.<br>1 : Invert the selected reference signal which is used in the min deadband logic on PWMA. |
| 1   | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                        |
| 0   | ENABLEA    | R/W  | 0h    | 0 : Minimum dead band logic is disabled<br>1 : Minimum dead band logic is enabled                                                                                                               |



### 3.7.2.171 EPWM\_MINDBDLY Register

#### 1 EPWM\_MINDBDLY Register (Offset = C04h) [reset = 0h]

Minimum dead band delay register.

Return to [Summary Table](#)

**Table 3-1324. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0C04h       |
| EPWM0_G1      | 5004 0C04h       |
| EPWM0_G2      | 5008 0C04h       |
| EPWM0_G3      | 500C 0C04h       |
| EPWM1_G0      | 5000 1C04h       |
| EPWM1_G1      | 5004 1C04h       |
| EPWM1_G2      | 5008 1C04h       |
| EPWM1_G3      | 500C 1C04h       |
| EPWM2_G0      | 5000 2C04h       |
| EPWM2_G1      | 5004 2C04h       |
| EPWM2_G2      | 5008 2C04h       |
| EPWM2_G3      | 500C 2C04h       |
| EPWM3_G0      | 5000 3C04h       |
| EPWM3_G1      | 5004 3C04h       |
| EPWM3_G2      | 5008 3C04h       |
| EPWM3_G3      | 500C 3C04h       |
| EPWM4_G0      | 5000 4C04h       |
| EPWM4_G1      | 5004 4C04h       |
| EPWM4_G2      | 5008 4C04h       |
| EPWM4_G3      | 500C 4C04h       |
| EPWM5_G0      | 5000 5C04h       |
| EPWM5_G1      | 5004 5C04h       |
| EPWM5_G2      | 5008 5C04h       |
| EPWM5_G3      | 500C 5C04h       |
| EPWM6_G0      | 5000 6C04h       |
| EPWM6_G1      | 5004 6C04h       |
| EPWM6_G2      | 5008 6C04h       |
| EPWM6_G3      | 500C 6C04h       |
| EPWM7_G0      | 5000 7C04h       |
| EPWM7_G1      | 5004 7C04h       |
| EPWM7_G2      | 5008 7C04h       |
| EPWM7_G3      | 500C 7C04h       |
| EPWM8_G0      | 5000 8C04h       |
| EPWM8_G1      | 5004 8C04h       |
| EPWM8_G2      | 5008 8C04h       |
| EPWM8_G3      | 500C 8C04h       |
| EPWM9_G0      | 5000 9C04h       |
| EPWM9_G1      | 5004 9C04h       |
| EPWM9_G2      | 5008 9C04h       |

**Table 3-1324. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9C04h       |
| EPWM10_G0     | 5000 AC04h       |
| EPWM10_G1     | 5004 AC04h       |
| EPWM10_G2     | 5008 AC04h       |
| EPWM10_G3     | 500C AC04h       |
| EPWM11_G0     | 5000 BC04h       |
| EPWM11_G1     | 5004 BC04h       |
| EPWM11_G2     | 5008 BC04h       |
| EPWM11_G3     | 500C BC04h       |
| EPWM12_G0     | 5000 CC04h       |
| EPWM12_G1     | 5004 CC04h       |
| EPWM12_G2     | 5008 CC04h       |
| EPWM12_G3     | 500C CC04h       |
| EPWM13_G0     | 5000 DC04h       |
| EPWM13_G1     | 5004 DC04h       |
| EPWM13_G2     | 5008 DC04h       |
| EPWM13_G3     | 500C DC04h       |
| EPWM14_G0     | 5000 EC04h       |
| EPWM14_G1     | 5004 EC04h       |
| EPWM14_G2     | 5008 EC04h       |
| EPWM14_G3     | 500C EC04h       |
| EPWM15_G0     | 5000 FC04h       |
| EPWM15_G1     | 5004 FC04h       |
| EPWM15_G2     | 5008 FC04h       |
| EPWM15_G3     | 500C FC04h       |
| EPWM16_G0     | 5001 0C04h       |
| EPWM16_G1     | 5005 0C04h       |
| EPWM16_G2     | 5009 0C04h       |
| EPWM16_G3     | 500D 0C04h       |
| EPWM17_G0     | 5001 1C04h       |
| EPWM17_G1     | 5005 1C04h       |
| EPWM17_G2     | 5009 1C04h       |
| EPWM17_G3     | 500D 1C04h       |
| EPWM18_G0     | 5001 2C04h       |
| EPWM18_G1     | 5005 2C04h       |
| EPWM18_G2     | 5009 2C04h       |
| EPWM18_G3     | 500D 2C04h       |
| EPWM19_G0     | 5001 3C04h       |
| EPWM19_G1     | 5005 3C04h       |
| EPWM19_G2     | 5009 3C04h       |
| EPWM19_G3     | 500D 3C04h       |
| EPWM20_G0     | 5001 4C04h       |
| EPWM20_G1     | 5005 4C04h       |
| EPWM20_G2     | 5009 4C04h       |
| EPWM20_G3     | 500D 4C04h       |

**Table 3-1324. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5C04h       |
| EPWM21_G1     | 5005 5C04h       |
| EPWM21_G2     | 5009 5C04h       |
| EPWM21_G3     | 500D 5C04h       |
| EPWM22_G0     | 5001 6C04h       |
| EPWM22_G1     | 5005 6C04h       |
| EPWM22_G2     | 5009 6C04h       |
| EPWM22_G3     | 500D 6C04h       |
| EPWM23_G0     | 5001 7C04h       |
| EPWM23_G1     | 5005 7C04h       |
| EPWM23_G2     | 5009 7C04h       |
| EPWM23_G3     | 500D 7C04h       |
| EPWM24_G0     | 5001 8C04h       |
| EPWM24_G1     | 5005 8C04h       |
| EPWM24_G2     | 5009 8C04h       |
| EPWM24_G3     | 500D 8C04h       |
| EPWM25_G0     | 5001 9C04h       |
| EPWM25_G1     | 5005 9C04h       |
| EPWM25_G2     | 5009 9C04h       |
| EPWM25_G3     | 500D 9C04h       |
| EPWM26_G0     | 5001 AC04h       |
| EPWM26_G1     | 5005 AC04h       |
| EPWM26_G2     | 5009 AC04h       |
| EPWM26_G3     | 500D AC04h       |
| EPWM27_G0     | 5001 BC04h       |
| EPWM27_G1     | 5005 BC04h       |
| EPWM27_G2     | 5009 BC04h       |
| EPWM27_G3     | 500D BC04h       |
| EPWM28_G0     | 5001 CC04h       |
| EPWM28_G1     | 5005 CC04h       |
| EPWM28_G2     | 5009 CC04h       |
| EPWM28_G3     | 500D CC04h       |
| EPWM29_G0     | 5001 DC04h       |
| EPWM29_G1     | 5005 DC04h       |
| EPWM29_G2     | 5009 DC04h       |
| EPWM29_G3     | 500D DC04h       |
| EPWM30_G0     | 5001 EC04h       |
| EPWM30_G1     | 5005 EC04h       |
| EPWM30_G2     | 5009 EC04h       |
| EPWM30_G3     | 500D EC04h       |
| EPWM31_G0     | 5001 FC04h       |
| EPWM31_G1     | 5005 FC04h       |
| EPWM31_G2     | 5009 FC04h       |
| EPWM31_G3     | 500D FC04h       |

**Figure 3-422. EPWM\_MINDBDLY Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DELAYB |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DELAYB |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DELAYA |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DELAYA |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 3-1326. EPWM\_MINDBDLY Register Field Descriptions**

| Bit   | Field  | Type | Reset | Description                                                                                                                                                                                                                   |
|-------|--------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | DELAYB | R/W  | 0h    | Minimum dead band delay on PWMB in terms of SYSCLK cycles. For delay value of 0, user should configure MINDBCFG[ENABLEA/B] = '0'. If MINDBCFG[ENABLEA/B] = '1' and MINDBDLY[DELAYA/B]='0' then delay is '1' cycle is applied. |
| 15:0  | DELAYA | R/W  | 0h    | Minimum dead band delay on PWMA in terms of SYSCLK cycles. For delay value of 0, user should configure MINDBCFG[ENABLEA/B] = '0'. If MINDBCFG[ENABLEA/B] = '1' and MINDBDLY[DELAYA/B]='0' then delay is '1' cycle is applied. |

### 3.7.2.172 EPWM\_LUTCTLA Register

#### 1 EPWM\_LUTCTLA Register (Offset = C20h) [reset = 1h]

LUT control register on PWMA.

Return to [Summary Table](#)

**Table 3-1327. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0C20h       |
| EPWM0_G1      | 5004 0C20h       |
| EPWM0_G2      | 5008 0C20h       |
| EPWM0_G3      | 500C 0C20h       |
| EPWM1_G0      | 5000 1C20h       |
| EPWM1_G1      | 5004 1C20h       |
| EPWM1_G2      | 5008 1C20h       |
| EPWM1_G3      | 500C 1C20h       |
| EPWM2_G0      | 5000 2C20h       |
| EPWM2_G1      | 5004 2C20h       |
| EPWM2_G2      | 5008 2C20h       |
| EPWM2_G3      | 500C 2C20h       |
| EPWM3_G0      | 5000 3C20h       |
| EPWM3_G1      | 5004 3C20h       |
| EPWM3_G2      | 5008 3C20h       |
| EPWM3_G3      | 500C 3C20h       |
| EPWM4_G0      | 5000 4C20h       |
| EPWM4_G1      | 5004 4C20h       |
| EPWM4_G2      | 5008 4C20h       |
| EPWM4_G3      | 500C 4C20h       |
| EPWM5_G0      | 5000 5C20h       |
| EPWM5_G1      | 5004 5C20h       |
| EPWM5_G2      | 5008 5C20h       |
| EPWM5_G3      | 500C 5C20h       |
| EPWM6_G0      | 5000 6C20h       |
| EPWM6_G1      | 5004 6C20h       |
| EPWM6_G2      | 5008 6C20h       |
| EPWM6_G3      | 500C 6C20h       |
| EPWM7_G0      | 5000 7C20h       |
| EPWM7_G1      | 5004 7C20h       |
| EPWM7_G2      | 5008 7C20h       |
| EPWM7_G3      | 500C 7C20h       |
| EPWM8_G0      | 5000 8C20h       |
| EPWM8_G1      | 5004 8C20h       |
| EPWM8_G2      | 5008 8C20h       |
| EPWM8_G3      | 500C 8C20h       |
| EPWM9_G0      | 5000 9C20h       |
| EPWM9_G1      | 5004 9C20h       |
| EPWM9_G2      | 5008 9C20h       |

**Table 3-1327. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9C20h       |
| EPWM10_G0     | 5000 AC20h       |
| EPWM10_G1     | 5004 AC20h       |
| EPWM10_G2     | 5008 AC20h       |
| EPWM10_G3     | 500C AC20h       |
| EPWM11_G0     | 5000 BC20h       |
| EPWM11_G1     | 5004 BC20h       |
| EPWM11_G2     | 5008 BC20h       |
| EPWM11_G3     | 500C BC20h       |
| EPWM12_G0     | 5000 CC20h       |
| EPWM12_G1     | 5004 CC20h       |
| EPWM12_G2     | 5008 CC20h       |
| EPWM12_G3     | 500C CC20h       |
| EPWM13_G0     | 5000 DC20h       |
| EPWM13_G1     | 5004 DC20h       |
| EPWM13_G2     | 5008 DC20h       |
| EPWM13_G3     | 500C DC20h       |
| EPWM14_G0     | 5000 EC20h       |
| EPWM14_G1     | 5004 EC20h       |
| EPWM14_G2     | 5008 EC20h       |
| EPWM14_G3     | 500C EC20h       |
| EPWM15_G0     | 5000 FC20h       |
| EPWM15_G1     | 5004 FC20h       |
| EPWM15_G2     | 5008 FC20h       |
| EPWM15_G3     | 500C FC20h       |
| EPWM16_G0     | 5001 0C20h       |
| EPWM16_G1     | 5005 0C20h       |
| EPWM16_G2     | 5009 0C20h       |
| EPWM16_G3     | 500D 0C20h       |
| EPWM17_G0     | 5001 1C20h       |
| EPWM17_G1     | 5005 1C20h       |
| EPWM17_G2     | 5009 1C20h       |
| EPWM17_G3     | 500D 1C20h       |
| EPWM18_G0     | 5001 2C20h       |
| EPWM18_G1     | 5005 2C20h       |
| EPWM18_G2     | 5009 2C20h       |
| EPWM18_G3     | 500D 2C20h       |
| EPWM19_G0     | 5001 3C20h       |
| EPWM19_G1     | 5005 3C20h       |
| EPWM19_G2     | 5009 3C20h       |
| EPWM19_G3     | 500D 3C20h       |
| EPWM20_G0     | 5001 4C20h       |
| EPWM20_G1     | 5005 4C20h       |
| EPWM20_G2     | 5009 4C20h       |
| EPWM20_G3     | 500D 4C20h       |

**Table 3-1327. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5C20h       |
| EPWM21_G1     | 5005 5C20h       |
| EPWM21_G2     | 5009 5C20h       |
| EPWM21_G3     | 500D 5C20h       |
| EPWM22_G0     | 5001 6C20h       |
| EPWM22_G1     | 5005 6C20h       |
| EPWM22_G2     | 5009 6C20h       |
| EPWM22_G3     | 500D 6C20h       |
| EPWM23_G0     | 5001 7C20h       |
| EPWM23_G1     | 5005 7C20h       |
| EPWM23_G2     | 5009 7C20h       |
| EPWM23_G3     | 500D 7C20h       |
| EPWM24_G0     | 5001 8C20h       |
| EPWM24_G1     | 5005 8C20h       |
| EPWM24_G2     | 5009 8C20h       |
| EPWM24_G3     | 500D 8C20h       |
| EPWM25_G0     | 5001 9C20h       |
| EPWM25_G1     | 5005 9C20h       |
| EPWM25_G2     | 5009 9C20h       |
| EPWM25_G3     | 500D 9C20h       |
| EPWM26_G0     | 5001 AC20h       |
| EPWM26_G1     | 5005 AC20h       |
| EPWM26_G2     | 5009 AC20h       |
| EPWM26_G3     | 500D AC20h       |
| EPWM27_G0     | 5001 BC20h       |
| EPWM27_G1     | 5005 BC20h       |
| EPWM27_G2     | 5009 BC20h       |
| EPWM27_G3     | 500D BC20h       |
| EPWM28_G0     | 5001 CC20h       |
| EPWM28_G1     | 5005 CC20h       |
| EPWM28_G2     | 5009 CC20h       |
| EPWM28_G3     | 500D CC20h       |
| EPWM29_G0     | 5001 DC20h       |
| EPWM29_G1     | 5005 DC20h       |
| EPWM29_G2     | 5009 DC20h       |
| EPWM29_G3     | 500D DC20h       |
| EPWM30_G0     | 5001 EC20h       |
| EPWM30_G1     | 5005 EC20h       |
| EPWM30_G2     | 5009 EC20h       |
| EPWM30_G3     | 500D EC20h       |
| EPWM31_G0     | 5001 FC20h       |
| EPWM31_G1     | 5005 FC20h       |
| EPWM31_G2     | 5009 FC20h       |
| EPWM31_G3     | 500D FC20h       |

**Figure 3-423. EPWM\_LUTCTLA Name Register**

|            |         |         |         |            |         |         |         |
|------------|---------|---------|---------|------------|---------|---------|---------|
| 31         | 30      | 29      | 28      | 27         | 26      | 25      | 24      |
| RESERVED_3 |         |         |         |            |         |         |         |
| R          |         |         |         |            |         |         |         |
| 0h         |         |         |         |            |         |         |         |
| 23         | 22      | 21      | 20      | 19         | 18      | 17      | 16      |
| LUTDEC7    | LUTDEC6 | LUTDEC5 | LUTDEC4 | LUTDEC3    | LUTDEC2 | LUTDEC1 | LUTDEC0 |
| R/W        | R/W     | R/W     | R/W     | R/W        | R/W     | R/W     | R/W     |
| 0h         | 0h      | 0h      | 0h      | 0h         | 0h      | 0h      | 0h      |
| 15         | 14      | 13      | 12      | 11         | 10      | 9       | 8       |
| RESERVED_2 |         |         |         |            |         |         |         |
| R          |         |         |         |            |         |         |         |
| 0h         |         |         |         |            |         |         |         |
| 7          | 6       | 5       | 4       | 3          | 2       | 1       | 0       |
| SELXBAR    |         |         |         | RESERVED_1 |         |         | BYPASS  |
| R/W        |         |         |         | R          |         |         | R/W     |
| 0h         |         |         |         | 0h         |         |         | 1h      |

**Table 3-1329. EPWM\_LUTCTLA Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                        |
|-------|------------|------|-------|--------------------------------------------------------------------|
| 31:24 | RESERVED_3 | R    | 0h    | Reserved                                                           |
| 23    | LUTDEC7    | R/W  | 0h    | 0 : Force 0<br>1 : Force 1                                         |
| 22    | LUTDEC6    | R/W  | 0h    | 0 : Force 0<br>1 : Force 1                                         |
| 21    | LUTDEC5    | R/W  | 0h    | 0 : Force 0<br>1 : Force 1                                         |
| 20    | LUTDEC4    | R/W  | 0h    | 0 : Force 0<br>1 : Force 1                                         |
| 19    | LUTDEC3    | R/W  | 0h    | 0 : Force 0<br>1 : Force 1                                         |
| 18    | LUTDEC2    | R/W  | 0h    | 0 : Force 0<br>1 : Force 1                                         |
| 17    | LUTDEC1    | R/W  | 0h    | 0 : Force 0<br>1 : Force 1                                         |
| 16    | LUTDEC0    | R/W  | 0h    | 0 : Force 0<br>1 : Force 1                                         |
| 15:8  | RESERVED_2 | R    | 0h    | Reserved                                                           |
| 7:4   | SELXBAR    | R/W  | 0h    | Selects one of the 16 outputs of ICSSXBAR to feed into IN3 of LUTA |
| 3:1   | RESERVED_1 | R    | 0h    | Reserved                                                           |
| 0     | BYPASS     | R/W  | 1h    | 1 : Bypass LUT logic on PWMA<br>0 : PWMA driven by LUTA            |



### 3.7.2.173 EPWM\_LUTCTLB Register

#### 1 EPWM\_LUTCTLB Register (Offset = C24h) [reset = 1h]

LUT control register on PWMB.

Return to [Summary Table](#)

**Table 3-1330. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM0_G0      | 5000 0C24h       |
| EPWM0_G1      | 5004 0C24h       |
| EPWM0_G2      | 5008 0C24h       |
| EPWM0_G3      | 500C 0C24h       |
| EPWM1_G0      | 5000 1C24h       |
| EPWM1_G1      | 5004 1C24h       |
| EPWM1_G2      | 5008 1C24h       |
| EPWM1_G3      | 500C 1C24h       |
| EPWM2_G0      | 5000 2C24h       |
| EPWM2_G1      | 5004 2C24h       |
| EPWM2_G2      | 5008 2C24h       |
| EPWM2_G3      | 500C 2C24h       |
| EPWM3_G0      | 5000 3C24h       |
| EPWM3_G1      | 5004 3C24h       |
| EPWM3_G2      | 5008 3C24h       |
| EPWM3_G3      | 500C 3C24h       |
| EPWM4_G0      | 5000 4C24h       |
| EPWM4_G1      | 5004 4C24h       |
| EPWM4_G2      | 5008 4C24h       |
| EPWM4_G3      | 500C 4C24h       |
| EPWM5_G0      | 5000 5C24h       |
| EPWM5_G1      | 5004 5C24h       |
| EPWM5_G2      | 5008 5C24h       |
| EPWM5_G3      | 500C 5C24h       |
| EPWM6_G0      | 5000 6C24h       |
| EPWM6_G1      | 5004 6C24h       |
| EPWM6_G2      | 5008 6C24h       |
| EPWM6_G3      | 500C 6C24h       |
| EPWM7_G0      | 5000 7C24h       |
| EPWM7_G1      | 5004 7C24h       |
| EPWM7_G2      | 5008 7C24h       |
| EPWM7_G3      | 500C 7C24h       |
| EPWM8_G0      | 5000 8C24h       |
| EPWM8_G1      | 5004 8C24h       |
| EPWM8_G2      | 5008 8C24h       |
| EPWM8_G3      | 500C 8C24h       |
| EPWM9_G0      | 5000 9C24h       |
| EPWM9_G1      | 5004 9C24h       |
| EPWM9_G2      | 5008 9C24h       |

**Table 3-1330. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM9_G3      | 500C 9C24h       |
| EPWM10_G0     | 5000 AC24h       |
| EPWM10_G1     | 5004 AC24h       |
| EPWM10_G2     | 5008 AC24h       |
| EPWM10_G3     | 500C AC24h       |
| EPWM11_G0     | 5000 BC24h       |
| EPWM11_G1     | 5004 BC24h       |
| EPWM11_G2     | 5008 BC24h       |
| EPWM11_G3     | 500C BC24h       |
| EPWM12_G0     | 5000 CC24h       |
| EPWM12_G1     | 5004 CC24h       |
| EPWM12_G2     | 5008 CC24h       |
| EPWM12_G3     | 500C CC24h       |
| EPWM13_G0     | 5000 DC24h       |
| EPWM13_G1     | 5004 DC24h       |
| EPWM13_G2     | 5008 DC24h       |
| EPWM13_G3     | 500C DC24h       |
| EPWM14_G0     | 5000 EC24h       |
| EPWM14_G1     | 5004 EC24h       |
| EPWM14_G2     | 5008 EC24h       |
| EPWM14_G3     | 500C EC24h       |
| EPWM15_G0     | 5000 FC24h       |
| EPWM15_G1     | 5004 FC24h       |
| EPWM15_G2     | 5008 FC24h       |
| EPWM15_G3     | 500C FC24h       |
| EPWM16_G0     | 5001 0C24h       |
| EPWM16_G1     | 5005 0C24h       |
| EPWM16_G2     | 5009 0C24h       |
| EPWM16_G3     | 500D 0C24h       |
| EPWM17_G0     | 5001 1C24h       |
| EPWM17_G1     | 5005 1C24h       |
| EPWM17_G2     | 5009 1C24h       |
| EPWM17_G3     | 500D 1C24h       |
| EPWM18_G0     | 5001 2C24h       |
| EPWM18_G1     | 5005 2C24h       |
| EPWM18_G2     | 5009 2C24h       |
| EPWM18_G3     | 500D 2C24h       |
| EPWM19_G0     | 5001 3C24h       |
| EPWM19_G1     | 5005 3C24h       |
| EPWM19_G2     | 5009 3C24h       |
| EPWM19_G3     | 500D 3C24h       |
| EPWM20_G0     | 5001 4C24h       |
| EPWM20_G1     | 5005 4C24h       |
| EPWM20_G2     | 5009 4C24h       |
| EPWM20_G3     | 500D 4C24h       |

**Table 3-1330. Instance Table (continued)**

| Instance Name | Physical Address |
|---------------|------------------|
| EPWM21_G0     | 5001 5C24h       |
| EPWM21_G1     | 5005 5C24h       |
| EPWM21_G2     | 5009 5C24h       |
| EPWM21_G3     | 500D 5C24h       |
| EPWM22_G0     | 5001 6C24h       |
| EPWM22_G1     | 5005 6C24h       |
| EPWM22_G2     | 5009 6C24h       |
| EPWM22_G3     | 500D 6C24h       |
| EPWM23_G0     | 5001 7C24h       |
| EPWM23_G1     | 5005 7C24h       |
| EPWM23_G2     | 5009 7C24h       |
| EPWM23_G3     | 500D 7C24h       |
| EPWM24_G0     | 5001 8C24h       |
| EPWM24_G1     | 5005 8C24h       |
| EPWM24_G2     | 5009 8C24h       |
| EPWM24_G3     | 500D 8C24h       |
| EPWM25_G0     | 5001 9C24h       |
| EPWM25_G1     | 5005 9C24h       |
| EPWM25_G2     | 5009 9C24h       |
| EPWM25_G3     | 500D 9C24h       |
| EPWM26_G0     | 5001 AC24h       |
| EPWM26_G1     | 5005 AC24h       |
| EPWM26_G2     | 5009 AC24h       |
| EPWM26_G3     | 500D AC24h       |
| EPWM27_G0     | 5001 BC24h       |
| EPWM27_G1     | 5005 BC24h       |
| EPWM27_G2     | 5009 BC24h       |
| EPWM27_G3     | 500D BC24h       |
| EPWM28_G0     | 5001 CC24h       |
| EPWM28_G1     | 5005 CC24h       |
| EPWM28_G2     | 5009 CC24h       |
| EPWM28_G3     | 500D CC24h       |
| EPWM29_G0     | 5001 DC24h       |
| EPWM29_G1     | 5005 DC24h       |
| EPWM29_G2     | 5009 DC24h       |
| EPWM29_G3     | 500D DC24h       |
| EPWM30_G0     | 5001 EC24h       |
| EPWM30_G1     | 5005 EC24h       |
| EPWM30_G2     | 5009 EC24h       |
| EPWM30_G3     | 500D EC24h       |
| EPWM31_G0     | 5001 FC24h       |
| EPWM31_G1     | 5005 FC24h       |
| EPWM31_G2     | 5009 FC24h       |
| EPWM31_G3     | 500D FC24h       |

**Figure 3-424. EPWM\_LUTCTLB Name Register**

|            |         |         |         |            |         |         |         |
|------------|---------|---------|---------|------------|---------|---------|---------|
| 31         | 30      | 29      | 28      | 27         | 26      | 25      | 24      |
| RESERVED_3 |         |         |         |            |         |         |         |
| R          |         |         |         |            |         |         |         |
| 0h         |         |         |         |            |         |         |         |
| 23         | 22      | 21      | 20      | 19         | 18      | 17      | 16      |
| LUTDEC7    | LUTDEC6 | LUTDEC5 | LUTDEC4 | LUTDEC3    | LUTDEC2 | LUTDEC1 | LUTDEC0 |
| R/W        | R/W     | R/W     | R/W     | R/W        | R/W     | R/W     | R/W     |
| 0h         | 0h      | 0h      | 0h      | 0h         | 0h      | 0h      | 0h      |
| 15         | 14      | 13      | 12      | 11         | 10      | 9       | 8       |
| RESERVED_2 |         |         |         |            |         |         |         |
| R          |         |         |         |            |         |         |         |
| 0h         |         |         |         |            |         |         |         |
| 7          | 6       | 5       | 4       | 3          | 2       | 1       | 0       |
| SELXBAR    |         |         |         | RESERVED_1 |         |         | BYPASS  |
| R/W        |         |         |         | R          |         |         | R/W     |
| 0h         |         |         |         | 0h         |         |         | 1h      |

**Table 3-1332. EPWM\_LUTCTLB Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                        |
|-------|------------|------|-------|--------------------------------------------------------------------|
| 31:24 | RESERVED_3 | R    | 0h    | Reserved                                                           |
| 23    | LUTDEC7    | R/W  | 0h    | 0 : Force 0<br>1 : Force 1                                         |
| 22    | LUTDEC6    | R/W  | 0h    | 0 : Force 0<br>1 : Force 1                                         |
| 21    | LUTDEC5    | R/W  | 0h    | 0 : Force 0<br>1 : Force 1                                         |
| 20    | LUTDEC4    | R/W  | 0h    | 0 : Force 0<br>1 : Force 1                                         |
| 19    | LUTDEC3    | R/W  | 0h    | 0 : Force 0<br>1 : Force 1                                         |
| 18    | LUTDEC2    | R/W  | 0h    | 0 : Force 0<br>1 : Force 1                                         |
| 17    | LUTDEC1    | R/W  | 0h    | 0 : Force 0<br>1 : Force 1                                         |
| 16    | LUTDEC0    | R/W  | 0h    | 0 : Force 0<br>1 : Force 1                                         |
| 15:8  | RESERVED_2 | R    | 0h    | Reserved                                                           |
| 7:4   | SELXBAR    | R/W  | 0h    | Selects one of the 16 outputs of ICSSXBAR to feed into IN3 of LUTB |
| 3:1   | RESERVED_1 | R    | 0h    | Reserved                                                           |
| 0     | BYPASS     | R/W  | 1h    | 1 : Bypass LUT logic on PWMB<br>0 : PWMB driven by LUTB            |

## 3.8 EQEP

### EQEP

#### 3.8.1 EQEP Summaries

#### EQEP Summaries

**Table 3-1333. EQEP Registers, Base Address=5027 0000h, Length=4096**

| Offset | Length | Register Name                  | EQEP0 Physical Address | EQEP1 Physical Address | EQEP2 Physical Address |
|--------|--------|--------------------------------|------------------------|------------------------|------------------------|
| 0h     | 32     | <a href="#">EQEP_QPOSCNT</a>   | 5027 0000h             | 5027 1000h             | 5027 2000h             |
| 4h     | 32     | <a href="#">EQEP_QPOSINIT</a>  | 5027 0004h             | 5027 1004h             | 5027 2004h             |
| 8h     | 32     | <a href="#">EQEP_QPOSMAX</a>   | 5027 0008h             | 5027 1008h             | 5027 2008h             |
| Ch     | 32     | <a href="#">EQEP_QPOSCMP</a>   | 5027 000Ch             | 5027 100Ch             | 5027 200Ch             |
| 10h    | 32     | <a href="#">EQEP_QPOSILAT</a>  | 5027 0010h             | 5027 1010h             | 5027 2010h             |
| 14h    | 32     | <a href="#">EQEP_QPOSSLAT</a>  | 5027 0014h             | 5027 1014h             | 5027 2014h             |
| 18h    | 32     | <a href="#">EQEP_QPOSLAT</a>   | 5027 0018h             | 5027 1018h             | 5027 2018h             |
| 1Ch    | 32     | <a href="#">EQEP_QUTMR</a>     | 5027 001Ch             | 5027 101Ch             | 5027 201Ch             |
| 20h    | 32     | <a href="#">EQEP_QUPRD</a>     | 5027 0020h             | 5027 1020h             | 5027 2020h             |
| 24h    | 16     | <a href="#">EQEP_QWDTMR</a>    | 5027 0024h             | 5027 1024h             | 5027 2024h             |
| 26h    | 16     | <a href="#">EQEP_QWDPRD</a>    | 5027 0026h             | 5027 1026h             | 5027 2026h             |
| 28h    | 16     | <a href="#">EQEP_QDECCTL</a>   | 5027 0028h             | 5027 1028h             | 5027 2028h             |
| 2Ah    | 16     | <a href="#">EQEP_QEPCTL</a>    | 5027 002Ah             | 5027 102Ah             | 5027 202Ah             |
| 2Ch    | 16     | <a href="#">EQEP_QCAPCTL</a>   | 5027 002Ch             | 5027 102Ch             | 5027 202Ch             |
| 2Eh    | 16     | <a href="#">EQEP_QPOSCTL</a>   | 5027 002Eh             | 5027 102Eh             | 5027 202Eh             |
| 30h    | 16     | <a href="#">EQEP_QEINT</a>     | 5027 0030h             | 5027 1030h             | 5027 2030h             |
| 32h    | 16     | <a href="#">EQEP_QFLG</a>      | 5027 0032h             | 5027 1032h             | 5027 2032h             |
| 34h    | 16     | <a href="#">EQEP_QCLR</a>      | 5027 0034h             | 5027 1034h             | 5027 2034h             |
| 36h    | 16     | <a href="#">EQEP_QFRC</a>      | 5027 0036h             | 5027 1036h             | 5027 2036h             |
| 38h    | 16     | <a href="#">EQEP_QEPSTS</a>    | 5027 0038h             | 5027 1038h             | 5027 2038h             |
| 3Ah    | 16     | <a href="#">EQEP_QCTMR</a>     | 5027 003Ah             | 5027 103Ah             | 5027 203Ah             |
| 3Ch    | 16     | <a href="#">EQEP_QCPRD</a>     | 5027 003Ch             | 5027 103Ch             | 5027 203Ch             |
| 3Eh    | 16     | <a href="#">EQEP_QCTMRLAT</a>  | 5027 003Eh             | 5027 103Eh             | 5027 203Eh             |
| 40h    | 16     | <a href="#">EQEP_QCPRDLAT</a>  | 5027 0040h             | 5027 1040h             | 5027 2040h             |
| 60h    | 32     | <a href="#">EQEP_REV</a>       | 5027 0060h             | 5027 1060h             | 5027 2060h             |
| 68h    | 32     | <a href="#">EQEP_QMACTRL</a>   | 5027 0068h             | 5027 1068h             | 5027 2068h             |
| 6Ch    | 32     | <a href="#">EQEP_QEPSRCSEL</a> | 5027 006Ch             | 5027 106Ch             | 5027 206Ch             |

#### 3.8.2 EQEP Registers

#### EQEP Registers

### 3.8.2.1 EQEP\_QPOSCNT Register

#### 1 EQEP\_QPOSCNT Register (Offset = 0h) [reset = 0h]

Position Counter .

Return to [Summary Table](#)

**Table 3-1334. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EQEP0         | 5027 0000h       |
| EQEP1         | 5027 1000h       |
| EQEP2         | 5027 2000h       |

**Figure 3-425. EQEP\_QPOSCNT Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| QPOSCNT |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| QPOSCNT |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QPOSCNT |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QPOSCNT |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 3-1336. EQEP\_QPOSCNT Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|---------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | QPOSCNT | R/W  | 0h    | <p>Position Counter</p> <p>This 32-bit position counter register counts up/down on every eQEP pulse based on direction input. This counter acts as a position integrator whose count value is proportional to position from a give reference point. This Register acts as a Read ONLY register while counter is counting up/down.</p> <p>Note: It is recommended to only write to the position counter register [QPOSCNT] during initialization, i.e. when the eQEP position counter is disabled [QPEN bit of QEPCTL is zero]. Once the position counter is enabled [QPEN bit is one], Writing to the eQEP position counter register [QPOSCNT] may cause unexpected results.</p> |

### 3.8.2.2 EQEP\_QPOSINIT Register

#### 1 EQEP\_QPOSINIT Register (Offset = 4h) [reset = 0h]

Position Counter Init .

Return to [Summary Table](#)

**Table 3-1337. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EQEP0         | 5027 0004h       |
| EQEP1         | 5027 1004h       |
| EQEP2         | 5027 2004h       |

**Figure 3-426. EQEP\_QPOSINIT Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| QPOSINIT |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| QPOSINIT |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QPOSINIT |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QPOSINIT |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 3-1339. EQEP\_QPOSINIT Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                        |
|------|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | QPOSINIT | R/W  | 0h    | Position Counter Init<br>This register contains the position value that is used to initialize the position counter based on external strobe or index event. The position counter can be initialized through software. Writes to this register should always be full 32-bit writes. |

### 3.8.2.3 EQEP\_QPOSMAX Register

#### 1 EQEP\_QPOSMAX Register (Offset = 8h) [reset = 0h]

Maximum Position Count .

Return to [Summary Table](#)

**Table 3-1340. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EQEP0         | 5027 0008h       |
| EQEP1         | 5027 1008h       |
| EQEP2         | 5027 2008h       |

**Figure 3-427. EQEP\_QPOSMAX Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| QPOSMAX |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| QPOSMAX |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QPOSMAX |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QPOSMAX |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 3-1342. EQEP\_QPOSMAX Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                       |
|------|---------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | QPOSMAX | R/W  | 0h    | Maximum Position Count<br>This register contains the maximum position counter value. Writes to this register should always be full 32-bit writes. |



### 3.8.2.4 EQEP\_QPOSCMP Register

#### 1 EQEP\_QPOSCMP Register (Offset = Ch) [reset = 0h]

Position Compare .

Return to [Summary Table](#)

**Table 3-1343. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EQEP0         | 5027 000Ch       |
| EQEP1         | 5027 100Ch       |
| EQEP2         | 5027 200Ch       |

**Figure 3-428. EQEP\_QPOSCMP Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| QPOSCMP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| QPOSCMP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QPOSCMP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QPOSCMP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 3-1345. EQEP\_QPOSCMP Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                |
|------|---------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | QPOSCMP | R/W  | 0h    | Position Compare<br>The position-compare value in this register is compared with the position counter [QPOSCNT] to generate sync output and/or interrupt on compare match. |

### 3.8.2.5 EQEP\_QPOSILAT Register

#### 1 EQEP\_QPOSILAT Register (Offset = 10h) [reset = 0h]

Index Position Latch .

Return to [Summary Table](#)

**Table 3-1346. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EQEP0         | 5027 0010h       |
| EQEP1         | 5027 1010h       |
| EQEP2         | 5027 2010h       |

**Figure 3-429. EQEP\_QPOSILAT Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| QPOSILAT |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| QPOSILAT |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QPOSILAT |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QPOSILAT |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 3-1348. EQEP\_QPOSILAT Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                            |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | QPOSILAT | R    | 0h    | Index Position Latch<br>The position-counter value is latched into this register on an index event as defined by the QEPCTL[IEL] bits. |

### 3.8.2.6 EQEP\_QPOSSLAT Register

#### 1 EQEP\_QPOSSLAT Register (Offset = 14h) [reset = 0h]

Strobe Position Latch.

Return to [Summary Table](#)

**Table 3-1349. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EQEP0         | 5027 0014h       |
| EQEP1         | 5027 1014h       |
| EQEP2         | 5027 2014h       |

**Figure 3-430. EQEP\_QPOSSLAT Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| QPOSSLAT |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| QPOSSLAT |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QPOSSLAT |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QPOSSLAT |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 3-1351. EQEP\_QPOSSLAT Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                             |
|------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | QPOSSLAT | R    | 0h    | Strobe Position Latch<br>The position-counter value is latched into this register on a strobe event as defined by the QEPCTL[SEL] bits. |

### 3.8.2.7 EQEP\_QPOSLAT Register

#### 1 EQEP\_QPOSLAT Register (Offset = 18h) [reset = 0h]

Position Latch .

Return to [Summary Table](#)

**Table 3-1352. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EQEP0         | 5027 0018h       |
| EQEP1         | 5027 1018h       |
| EQEP2         | 5027 2018h       |

**Figure 3-431. EQEP\_QPOSLAT Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| QPOSLAT |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| QPOSLAT |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QPOSLAT |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QPOSLAT |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 3-1354. EQEP\_QPOSLAT Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                          |
|------|---------|------|-------|------------------------------------------------------------------------------------------------------|
| 31:0 | QPOSLAT | R    | 0h    | Position Latch<br>The position-counter value is latched into this register on a unit time out event. |

### 3.8.2.8 EQEP\_QUTMR Register

#### 1 EQEP\_QUTMR Register (Offset = 1Ch) [reset = 0h]

QEP Unit Timer .

Return to [Summary Table](#)

**Table 3-1355. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EQEP0         | 5027 001Ch       |
| EQEP1         | 5027 101Ch       |
| EQEP2         | 5027 201Ch       |

**Figure 3-432. EQEP\_QUTMR Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| QUTMR |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| QUTMR |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUTMR |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUTMR |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 3-1357. EQEP\_QUTMR Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                |
|------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | QUTMR | R/W  | 0h    | QEP Unit Timer<br>This register acts as time base for unit time event generation. When this timer value matches the unit time period value a unit time event is generated. |

### 3.8.2.9 EQEP\_QUPRD Register

#### 1 EQEP\_QUPRD Register (Offset = 20h) [reset = 0h]

QEP Unit Period .

Return to [Summary Table](#)

**Table 3-1358. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EQEP0         | 5027 0020h       |
| EQEP1         | 5027 1020h       |
| EQEP2         | 5027 2020h       |

**Figure 3-433. EQEP\_QUPRD Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| QUPRD |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| QUPRD |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUPRD |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUPRD |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 3-1360. EQEP\_QUPRD Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                    |
|------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | QUPRD | R/W  | 0h    | QEP Unit Period<br>This register contains the period count for the unit timer to generate periodic unit time events. These events latch the eQEP position information at periodic intervals and optionally generate an interrupt. Writes to this register should always be full 32-bit writes. |

### 3.8.2.10 EQEP\_QWDTMR Register

#### 1 EQEP\_QWDTMR Register (Offset = 24h) [reset = 0h]

QEP Watchdog Timer .

Return to [Summary Table](#)

**Table 3-1361. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EQEP0         | 5027 0024h       |
| EQEP1         | 5027 1024h       |
| EQEP2         | 5027 2024h       |

**Figure 3-434. EQEP\_QWDTMR Name Register**

|        |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| QWDTMR |    |    |    |    |    |   |   |
| R/W    |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |
| 7      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| QWDTMR |    |    |    |    |    |   |   |
| R/W    |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |

**Table 3-1363. EQEP\_QWDTMR Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                     |
|------|--------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | QWDTMR | R/W  | 0h    | QEP Watchdog Timer<br>This register acts as time base for the watchdog to detect motor stalls. When this timer value matches with the watchdog's period value a watchdog timeout interrupt is generated. This register is reset upon edge transition in quadrature-clock indicating the motion. |

### 3.8.2.11 EQEP\_QWDPRD Register

#### 1 EQEP\_QWDPRD Register (Offset = 26h) [reset = 0h]

QEP Watchdog Period .

Return to [Summary Table](#)

**Table 3-1364. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EQEP0         | 5027 0026h       |
| EQEP1         | 5027 1026h       |
| EQEP2         | 5027 2026h       |

**Figure 3-435. EQEP\_QWDPRD Name Register**

|        |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| QWDPRD |    |    |    |    |    |   |   |
| R/W    |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |
| 7      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| QWDPRD |    |    |    |    |    |   |   |
| R/W    |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |

**Table 3-1366. EQEP\_QWDPRD Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                                                                                                              |
|------|--------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | QWDPRD | R/W  | 0h    | QEP Watchdog Period<br>This register contains the time-out count for the eQEP peripheral watch dog timer.<br>When the watchdog timer value matches the watchdog period value, a watchdog timeout interrupt is generated. |



### 3.8.2.12 EQEP\_QDECCTL Register

#### 1 EQEP\_QDECCTL Register (Offset = 28h) [reset = 0h]

Quadrature Decoder Control .

Return to [Summary Table](#)

**Table 3-1367. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EQEP0         | 5027 0028h       |
| EQEP1         | 5027 1028h       |
| EQEP2         | 5027 2028h       |

**Figure 3-436. EQEP\_QDECCTL Name Register**

| 15   | 14  | 13   | 12         | 11  | 10   | 9     | 8      |
|------|-----|------|------------|-----|------|-------|--------|
| QSRC |     | SOEN | SPSEL      | XCR | SWAP | IGATE | QAP    |
| R/W  |     | R/W  | R/W        | R/W | R/W  | R/W   | R/W    |
| 0h   |     | 0h   | 0h         | 0h  | 0h   | 0h    | 0h     |
| 7    | 6   | 5    | 4          | 3   | 2    | 1     | 0      |
| QBP  | QIP | QSP  | RESERVED_1 |     |      |       | QIDIRE |
| R/W  | R/W | R/W  | R          |     |      |       | R/W    |
| 0h   | 0h  | 0h   | 0h         |     |      |       | 0h     |

**Table 3-1369. EQEP\_QDECCTL Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                      |
|-------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | QSRC  | R/W  | 0h    | Position-counter source selection                                                                                                |
| 13    | SOEN  | R/W  | 0h    | Sync output-enable<br>0 Disable position-compare sync output<br>1 Enable position-compare sync output                            |
| 12    | SPSEL | R/W  | 0h    | Sync output pin selection<br>0 Index pin is used for sync output<br>1 Strobe pin is used for sync output                         |
| 11    | XCR   | R/W  | 0h    | External Clock Rate<br>0 2x resolution: Count the rising/falling edge<br>1 1x resolution: Count the rising edge only             |
| 10    | SWAP  | R/W  | 0h    | CLK/DIR Signal Source for Position Counter<br>0 Quadrature-clock inputs are not swapped<br>1 Quadrature-clock inputs are swapped |
| 9     | IGATE | R/W  | 0h    | Index pulse gating option<br>0 Disable gating of Index pulse<br>1 Gate the index pin with strobe                                 |
| 8     | QAP   | R/W  | 0h    | QEPA input polarity<br>0 No effect<br>1 Negates QEPA input                                                                       |
| 7     | QBP   | R/W  | 0h    | QEPB input polarity<br>0 No effect<br>1 Negates QEPB input                                                                       |
| 6     | QIP   | R/W  | 0h    | QEPI input polarity<br>0 No effect<br>1 Negates QEPI input                                                                       |

**Table 3-1369. EQEP\_QDECCTL Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                 |
|-----|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 5   | QSP        | R/W  | 0h    | QEPS input polarity<br>0 No effect<br>1 Negates QEPS input                                                                  |
| 4:1 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                    |
| 0   | QIDIRE     | R/W  | 0h    | 0 - Compatible mode, Behavior same as existing devices<br>1 - Enhancement for Direction change during Index will be enabled |

### 3.8.2.13 EQEP\_QEPCTL Register

#### 1 EQEP\_QEPCTL Register (Offset = 2Ah) [reset = 0h]

QEP Control .

Return to [Summary Table](#)

**Table 3-1370. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EQEP0         | 5027 002Ah       |
| EQEP1         | 5027 102Ah       |
| EQEP2         | 5027 202Ah       |

**Figure 3-437. EQEP\_QEPCTL Name Register**

| 15        | 14  | 13   | 12 | 11   | 10   | 9   | 8   |
|-----------|-----|------|----|------|------|-----|-----|
| FREE_SOFT |     | PCRM |    | SEI  |      | IEI |     |
| R/W       |     | R/W  |    | R/W  |      | R/W |     |
| 0h        |     | 0h   |    | 0h   |      | 0h  |     |
| 7         | 6   | 5    | 4  | 3    | 2    | 1   | 0   |
| SWI       | SEL | IEL  |    | QPEN | QCLM | UTE | WDE |
| R/W       | R/W | R/W  |    | R/W  | R/W  | R/W | R/W |
| 0h        | 0h  | 0h   |    | 0h   | 0h   | 0h  | 0h  |

**Table 3-1372. EQEP\_QEPCTL Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|-----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | FREE_SOFT | R/W  | 0h    | <p>Emulation mode</p> <p>0 QPOSNT behavior Position counter stops immediately on emulation suspend 0h (R/W) = QWDTMR behavior Watchdog counter stops immediately 0h (R/W) = QUTMR behavior Unit timer stops immediately 0h (R/W) = QCTMR behavior Capture Timer stops immediately</p> <p>1 QPOSNT behavior Position counter continues to count until the rollover 1h (R/W) = QWDTMR behavior Watchdog counter counts until WD period match roll over 1h (R/W) = QUTMR behavior Unit timer counts until period rollover 1h (R/W) = QCTMR behavior Capture Timer counts until next unit period event</p> <p>2 QPOSNT behavior Position counter is unaffected by emulation suspend 2h (R/W) = QWDTMR behavior Watchdog counter is unaffected by emulation suspend 2h (R/W) = QUTMR behavior Unit timer is unaffected by emulation suspend 2h (R/W) = QCTMR behavior Capture Timer is unaffected by emulation suspend</p> <p>3 Same as FREE_SOFT_2</p> |
| 13:12 | PCRM      | R/W  | 0h    | <p>Position counter reset</p> <p>0 Position counter reset on an index event</p> <p>1 Position counter reset on the maximum position</p> <p>2 Position counter reset on the first index event</p> <p>3 Position counter reset on a unit time event</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

**Table 3-1372. EQEP\_QEPCTL Register Field Descriptions (continued)**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11:10 | SEI   | R/W  | 0h    | Strobe event initialization of position counter<br>0 Does nothing (action disabled)<br>1 Does nothing (action disabled)<br>2 Initializes the position counter on rising edge of the QEPS signal<br>3 Clockwise Direction: Initializes the position counter on the rising edge of QEPS strobe Counter Clockwise Direction: Initializes the position counter on the falling edge of QEPS strobe                                                                                                    |
| 9:8   | IEI   | R/W  | 0h    | Index event init of position count<br>0 Do nothing (action disabled)<br>1 Do nothing (action disabled)<br>2 Initializes the position counter on the rising edge of the QEPI signal (QPOSCNT = QPOSINIT)<br>3 Initializes the position counter on the falling edge of QEPI signal (QPOSCNT = QPOSINIT)                                                                                                                                                                                            |
| 7     | SWI   | R/W  | 0h    | Software init position counter<br>0 Do nothing (action disabled)<br>1 Initialize position counter (QPOSCNT=QPOSINIT). This bit is not cleared automatically                                                                                                                                                                                                                                                                                                                                      |
| 6     | SEL   | R/W  | 0h    | Strobe event latch of position counter<br>0 The position counter is latched on the rising edge of QEPS strobe (QPOSSLAT = POSCNT). Latching on the falling edge can be done by inverting the strobe input using the QSP bit in the QDECCTL register<br>1 Clockwise Direction: Position counter is latched on rising edge of QEPS strobe Counter Clockwise Direction: Position counter is latched on falling edge of QEPS strobe                                                                  |
| 5:4   | IEL   | R/W  | 0h    | Index event latch of position counter [software index marker]<br>0 Reserved<br>1 Latches position counter on rising edge of the index signal<br>2 Latches position counter on falling edge of the index signal<br>3 Software index marker. Latches the position counter and quadrature direction flag on index event marker. The position counter is latched to the QPOSILAT register and the direction flag is latched in the QEPSTS[QDLF] bit. This mode is useful for software index marking. |
| 3     | QPEN  | R/W  | 0h    | Quadrature position counter enable/software reset<br>0 Reset the eQEP peripheral internal operating flags/read-only registers. Control/configuration registers are not disturbed by a software reset. When QPEN is disabled, some flags in the QFLG register do not get reset or cleared and show the actual state of that flag.<br>1 eQEP position counter is enabled                                                                                                                           |

**Table 3-1372. EQEP\_QEPCTL Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                         |
|-----|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | QCLM  | R/W  | 0h    | QEP capture latch mode<br>0 Latch on position counter read by CPU. Capture timer and capture period values are latched into QCTMRLAT and QCPRDLAT registers when CPU reads the QPOSCNT register.<br>1 Latch on unit time out. Position counter, capture timer and capture period values are latched into QPOSLAT, QCTMRLAT and QCPRDLAT registers on unit time out. |
| 1   | UTE   | R/W  | 0h    | QEP unit timer enable<br>0 Disable eQEP unit timer<br>1 Enable unit timer                                                                                                                                                                                                                                                                                           |
| 0   | WDE   | R/W  | 0h    | QEP watchdog enable<br>0 Disable the eQEP watchdog timer<br>1 Enable the eQEP watchdog timer                                                                                                                                                                                                                                                                        |

### 3.8.2.14 EQEP\_QCAPCTL Register

#### 1 EQEP\_QCAPCTL Register (Offset = 2Ch) [reset = 0h]

Qaudrature Capture Control .

Return to [Summary Table](#)

**Table 3-1373. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EQEP0         | 5027 002Ch       |
| EQEP1         | 5027 102Ch       |
| EQEP2         | 5027 202Ch       |

**Figure 3-438. EQEP\_QCAPCTL Name Register**

|            |            |    |    |      |    |   |   |
|------------|------------|----|----|------|----|---|---|
| 15         | 14         | 13 | 12 | 11   | 10 | 9 | 8 |
| CEN        | RESERVED_1 |    |    |      |    |   |   |
| R/W        | R          |    |    |      |    |   |   |
| 0h         | 0h         |    |    |      |    |   |   |
| 7          | 6          | 5  | 4  | 3    | 2  | 1 | 0 |
| RESERVED_1 | CCPS       |    |    | UPPS |    |   |   |
| R          | R/W        |    |    | R/W  |    |   |   |
| 0h         | 0h         |    |    | 0h   |    |   |   |

**Table 3-1375. EQEP\_QCAPCTL Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                            |
|------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | CEN        | R/W  | 0h    | Enable eQEP capture<br>0 eQEP capture unit is disabled<br>1 eQEP capture unit is enabled                                                                                                                                                                                                                                                                               |
| 14:7 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                               |
| 6:4  | CCPS       | R/W  | 0h    | EQEP capture timer clock prescaler<br>0 CAPCLK = SYSCLKOUT/1<br>1 CAPCLK = SYSCLKOUT/2<br>2 CAPCLK = SYSCLKOUT/4<br>3 CAPCLK = SYSCLKOUT/8<br>4 CAPCLK = SYSCLKOUT/16<br>5 CAPCLK = SYSCLKOUT/32<br>6 CAPCLK = SYSCLKOUT/64<br>7 CAPCLK = SYSCLKOUT/128                                                                                                                |
| 3:0  | UPPS       | R/W  | 0h    | Unit position event prescaler<br>0 UPEVNT = QCLK/1<br>1 UPEVNT = QCLK/2<br>2 UPEVNT = QCLK/4<br>3 UPEVNT = QCLK/8<br>4 UPEVNT = QCLK/16<br>5 UPEVNT = QCLK/32<br>6 UPEVNT = QCLK/64<br>7 UPEVNT = QCLK/128<br>8 UPEVNT = QCLK/256<br>9 UPEVNT = QCLK/512<br>10 UPEVNT = QCLK/1024<br>11 UPEVNT = QCLK/2048<br>12 Reserved<br>13 Reserved<br>14 Reserved<br>15 Reserved |

### 3.8.2.15 EQEP\_QPOSCTL Register

#### 1 EQEP\_QPOSCTL Register (Offset = 2Eh) [reset = 0h]

Position Compare Control .

Return to [Summary Table](#)

**Table 3-1376. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EQEP0         | 5027 002Eh       |
| EQEP1         | 5027 102Eh       |
| EQEP2         | 5027 202Eh       |

**Figure 3-439. EQEP\_QPOSCTL Name Register**

| 15     | 14     | 13    | 12  | 11    | 10 | 9 | 8 |
|--------|--------|-------|-----|-------|----|---|---|
| PCSHDW | PCLOAD | PCPOL | PCE | PCSPW |    |   |   |
| R/W    | R/W    | R/W   | R/W | R/W   |    |   |   |
| 0h     | 0h     | 0h    | 0h  | 0h    |    |   |   |
| 7      | 6      | 5     | 4   | 3     | 2  | 1 | 0 |
| PCSPW  |        |       |     |       |    |   |   |
| R/W    |        |       |     |       |    |   |   |
| 0h     |        |       |     |       |    |   |   |

**Table 3-1378. EQEP\_QPOSCTL Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                                     |
|------|--------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | PCSHDW | R/W  | 0h    | Position compare of shadow enable<br>0 Shadow disabled, load Immediate<br>1 Shadow enabled                                                      |
| 14   | PCLOAD | R/W  | 0h    | Position compare of shadow load<br>0 Load on QPOSCNT = 0<br>1 Load when QPOSCNT = QPOSCMP                                                       |
| 13   | PCPOL  | R/W  | 0h    | Polarity of sync output<br>0 Active HIGH pulse output<br>1 Active LOW pulse output                                                              |
| 12   | PCE    | R/W  | 0h    | Position compare enable/disable<br>0 Disable position compare unit<br>1 Enable position compare unit                                            |
| 11:0 | PCSPW  | R/W  | 0h    | Select-position-compare sync output pulse width<br>0 1 * 4 * SYSCLKOUT cycles<br>1 2 * 4 * SYSCLKOUT cycles<br>4095 4096 * 4 * SYSCLKOUT cycles |

### 3.8.2.16 EQEP\_QEINT Register

#### 1 EQEP\_QEINT Register (Offset = 30h) [reset = 0h]

QEP Interrupt Control .

Return to [Summary Table](#)

**Table 3-1379. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EQEP0         | 5027 0030h       |
| EQEP1         | 5027 1030h       |
| EQEP2         | 5027 2030h       |

**Figure 3-440. EQEP\_QEINT Name Register**

| 15         | 14  | 13  | 12   | 11  | 10  | 9   | 8          |
|------------|-----|-----|------|-----|-----|-----|------------|
| RESERVED_2 |     |     | QMAE | UTO | IEL | SEL | PCM        |
| R          |     |     | R/W  | R/W | R/W | R/W | R/W        |
| 0h         |     |     | 0h   | 0h  | 0h  | 0h  | 0h         |
| 7          | 6   | 5   | 4    | 3   | 2   | 1   | 0          |
| PCR        | PCO | PCU | WTO  | QDC | QPE | PCE | RESERVED_1 |
| R/W        | R/W | R/W | R/W  | R/W | R/W | R/W | R          |
| 0h         | 0h  | 0h  | 0h   | 0h  | 0h  | 0h  | 0h         |

**Table 3-1381. EQEP\_QEINT Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                      |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------|
| 15:13 | RESERVED_2 | R    | 0h    | Reserved                                                                                         |
| 12    | QMAE       | R/W  | 0h    | QMA Error Interrupt enable<br>0 Interrupt is disabled<br>1 Interrupt is enabled                  |
| 11    | UTO        | R/W  | 0h    | Unit time out interrupt enable<br>0 Interrupt is disabled<br>1 Interrupt is enabled              |
| 10    | IEL        | R/W  | 0h    | Index event latch interrupt enable<br>0 Interrupt is disabled<br>1 Interrupt is enabled          |
| 9     | SEL        | R/W  | 0h    | Strobe event latch interrupt enable<br>0 Interrupt is disabled<br>1 Interrupt is enabled         |
| 8     | PCM        | R/W  | 0h    | Position-compare match interrupt enable<br>0 Interrupt is disabled<br>1 Interrupt is enabled     |
| 7     | PCR        | R/W  | 0h    | Position-compare ready interrupt enable<br>0 Interrupt is disabled<br>1 Interrupt is enabled     |
| 6     | PCO        | R/W  | 0h    | Position counter overflow interrupt enable<br>0 Interrupt is disabled<br>1 Interrupt is enabled  |
| 5     | PCU        | R/W  | 0h    | Position counter underflow interrupt enable<br>0 Interrupt is disabled<br>1 Interrupt is enabled |



**Table 3-1381. EQEP\_QEINT Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                 |
|-----|------------|------|-------|-------------------------------------------------------------------------------------------------------------|
| 4   | WTO        | R/W  | 0h    | Watchdog time out interrupt enable<br>0      Interrupt is disabled<br>1      Interrupt is enabled           |
| 3   | QDC        | R/W  | 0h    | Quadrature direction change interrupt enable<br>0      Interrupt is disabled<br>1      Interrupt is enabled |
| 2   | QPE        | R/W  | 0h    | Quadrature phase error interrupt enable<br>0      Interrupt is disabled<br>1      Interrupt is enabled      |
| 1   | PCE        | R/W  | 0h    | Position counter error interrupt enable<br>0      Interrupt is disabled<br>1      Interrupt is enabled      |
| 0   | RESERVED_1 | R    | 0h    | Reserved                                                                                                    |

### 3.8.2.17 EQEP\_QFLG Register

#### 1 EQEP\_QFLG Register (Offset = 32h) [reset = 0h]

QEP Interrupt Flag .

Return to [Summary Table](#)

**Table 3-1382. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EQEP0         | 5027 0032h       |
| EQEP1         | 5027 1032h       |
| EQEP2         | 5027 2032h       |

**Figure 3-441. EQEP\_QFLG Name Register**

| 15         | 14  | 13  | 12   | 11  | 10  | 9   | 8   |
|------------|-----|-----|------|-----|-----|-----|-----|
| RESERVED_1 |     |     | QMAE | UTO | IEL | SEL | PCM |
| R          |     |     | R    | R   | R   | R   | R   |
| 0h         |     |     | 0h   | 0h  | 0h  | 0h  | 0h  |
| 7          | 6   | 5   | 4    | 3   | 2   | 1   | 0   |
| PCR        | PCO | PCU | WTO  | QDC | PHE | PCE | INT |
| R          | R   | R   | R    | R   | R   | R   | R   |
| 0h         | 0h  | 0h  | 0h   | 0h  | 0h  | 0h  | 0h  |

**Table 3-1384. EQEP\_QFLG Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                 |
|-------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                    |
| 12    | QMAE       | R    | 0h    | QMA Error interrupt flag<br>0 No interrupt generated<br>1 Interrupt was generated                                                                                           |
| 11    | UTO        | R    | 0h    | Unit time out interrupt flag<br>0 No interrupt generated<br>1 Set by eQEP unit timer period match                                                                           |
| 10    | IEL        | R    | 0h    | Index event latch interrupt flag<br>0 No interrupt generated<br>1 This bit is set after latching the QPOSCNT to QPOSILAT                                                    |
| 9     | SEL        | R    | 0h    | Strobe event latch interrupt flag<br>0 No interrupt generated<br>1 This bit is set after latching the QPOSCNT to QPOSSLAT                                                   |
| 8     | PCM        | R    | 0h    | EQEP compare match event interrupt flag<br>0 No interrupt generated<br>1 This bit is set on position-compare match                                                          |
| 7     | PCR        | R    | 0h    | Position-compare ready interrupt flag<br>0 No interrupt generated<br>1 This bit is set after transferring the shadow register value to the active position compare register |
| 6     | PCO        | R    | 0h    | Position counter overflow interrupt flag<br>0 No interrupt generated<br>1 This bit is set on position counter overflow.                                                     |

**Table 3-1384. EQEP\_QFLG Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                               |
|-----|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------|
| 5   | PCU   | R    | 0h    | Position counter underflow interrupt flag<br>0 No interrupt generated<br>1 This bit is set on position counter underflow. |
| 4   | WTO   | R    | 0h    | Watchdog timeout interrupt flag<br>0 No interrupt generated<br>1 Set by watchdog timeout                                  |
| 3   | QDC   | R    | 0h    | Quadrature direction change interrupt flag<br>0 No interrupt generated<br>1 Interrupt was generated                       |
| 2   | PHE   | R    | 0h    | Quadrature phase error interrupt flag<br>0 No interrupt generated<br>1 Set on simultaneous transition of QEPA and QEPB    |
| 1   | PCE   | R    | 0h    | Position counter error interrupt flag<br>0 No interrupt generated<br>1 Position counter error                             |
| 0   | INT   | R    | 0h    | Global interrupt status flag<br>0 No interrupt generated<br>1 Interrupt was generated                                     |

### 3.8.2.18 EQEP\_QCLR Register

#### 1 EQEP\_QCLR Register (Offset = 34h) [reset = 0h]

QEP Interrupt Clear .

Return to [Summary Table](#)

**Table 3-1385. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EQEP0         | 5027 0034h       |
| EQEP1         | 5027 1034h       |
| EQEP2         | 5027 2034h       |

**Figure 3-442. EQEP\_QCLR Name Register**

| 15         | 14     | 13     | 12     | 11     | 10     | 9      | 8      |
|------------|--------|--------|--------|--------|--------|--------|--------|
| RESERVED_1 |        |        | QMAE   | UTO    | IEL    | SEL    | PCM    |
| R          |        |        | R/W1TS | R/W1TS | R/W1TS | R/W1TS | R/W1TS |
| 0h         |        |        | 0h     | 0h     | 0h     | 0h     | 0h     |
| 7          | 6      | 5      | 4      | 3      | 2      | 1      | 0      |
| PCR        | PCO    | PCU    | WTO    | QDC    | PHE    | PCE    | INT    |
| R/W1TS     | R/W1TS | R/W1TS | R/W1TS | R/W1TS | R/W1TS | R/W1TS | R/W1TS |
| 0h         | 0h     | 0h     | 0h     | 0h     | 0h     | 0h     | 0h     |

**Table 3-1387. EQEP\_QCLR Register Field Descriptions**

| Bit   | Field      | Type   | Reset | Description                                                                                   |
|-------|------------|--------|-------|-----------------------------------------------------------------------------------------------|
| 15:13 | RESERVED_1 | R      | 0h    | Reserved                                                                                      |
| 12    | QMAE       | R/W1TS | 0h    | Clear QMA Error interrupt flag<br>0 No effect<br>1 Clears the interrupt flag                  |
| 11    | UTO        | R/W1TS | 0h    | Clear unit time out interrupt flag<br>0 No effect<br>1 Clears the interrupt flag              |
| 10    | IEL        | R/W1TS | 0h    | Clear index event latch interrupt flag<br>0 No effect<br>1 Clears the interrupt flag          |
| 9     | SEL        | R/W1TS | 0h    | Clear strobe event latch interrupt flag<br>0 No effect<br>1 Clears the interrupt flag         |
| 8     | PCM        | R/W1TS | 0h    | Clear eQEP compare match event interrupt flag<br>0 No effect<br>1 Clears the interrupt flag   |
| 7     | PCR        | R/W1TS | 0h    | Clear position-compare ready interrupt flag<br>0 No effect<br>1 Clears the interrupt flag     |
| 6     | PCO        | R/W1TS | 0h    | Clear position counter overflow interrupt flag<br>0 No effect<br>1 Clears the interrupt flag  |
| 5     | PCU        | R/W1TS | 0h    | Clear position counter underflow interrupt flag<br>0 No effect<br>1 Clears the interrupt flag |

**Table 3-1387. EQEP\_QCLR Register Field Descriptions (continued)**

| Bit | Field | Type   | Reset | Description                                                                                    |
|-----|-------|--------|-------|------------------------------------------------------------------------------------------------|
| 4   | WTO   | R/W1TS | 0h    | Clear watchdog timeout interrupt flag<br>0 No effect<br>1 Clears the interrupt flag            |
| 3   | QDC   | R/W1TS | 0h    | Clear quadrature direction change interrupt flag<br>0 No effect<br>1 Clears the interrupt flag |
| 2   | PHE   | R/W1TS | 0h    | Clear quadrature phase error interrupt flag<br>0 No effect<br>1 Clears the interrupt flag      |
| 1   | PCE   | R/W1TS | 0h    | Clear position counter error interrupt flag<br>0 No effect<br>1 Clears the interrupt flag      |
| 0   | INT   | R/W1TS | 0h    | Global interrupt clear flag<br>0 No effect<br>1 Clears the interrupt flag                      |

### 3.8.2.19 EQEP\_QFRC Register

#### 1 EQEP\_QFRC Register (Offset = 36h) [reset = 0h]

QEP Interrupt Force .

Return to [Summary Table](#)

**Table 3-1388. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EQEP0         | 5027 0036h       |
| EQEP1         | 5027 1036h       |
| EQEP2         | 5027 2036h       |

**Figure 3-443. EQEP\_QFRC Name Register**

| 15         | 14  | 13  | 12   | 11  | 10  | 9   | 8          |
|------------|-----|-----|------|-----|-----|-----|------------|
| RESERVED_2 |     |     | QMAE | UTO | IEL | SEL | PCM        |
| R          |     |     | R/W  | R/W | R/W | R/W | R/W        |
| 0h         |     |     | 0h   | 0h  | 0h  | 0h  | 0h         |
| 7          | 6   | 5   | 4    | 3   | 2   | 1   | 0          |
| PCR        | PCO | PCU | WTO  | QDC | PHE | PCE | RESERVED_1 |
| R/W        | R/W | R/W | R/W  | R/W | R/W | R/W | R          |
| 0h         | 0h  | 0h  | 0h   | 0h  | 0h  | 0h  | 0h         |

**Table 3-1390. EQEP\_QFRC Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                        |
|-------|------------|------|-------|------------------------------------------------------------------------------------|
| 15:13 | RESERVED_2 | R    | 0h    | Reserved                                                                           |
| 12    | QMAE       | R/W  | 0h    | Force QMA error interrupt<br>0 No effect<br>1 Force the interrupt                  |
| 11    | UTO        | R/W  | 0h    | Force unit time out interrupt<br>0 No effect<br>1 Force the interrupt              |
| 10    | IEL        | R/W  | 0h    | Force index event latch interrupt<br>0 No effect<br>1 Force the interrupt          |
| 9     | SEL        | R/W  | 0h    | Force strobe event latch interrupt<br>0 No effect<br>1 Force the interrupt         |
| 8     | PCM        | R/W  | 0h    | Force position-compare match interrupt<br>0 No effect<br>1 Force the interrupt     |
| 7     | PCR        | R/W  | 0h    | Force position-compare ready interrupt<br>0 No effect<br>1 Force the interrupt     |
| 6     | PCO        | R/W  | 0h    | Force position counter overflow interrupt<br>0 No effect<br>1 Force the interrupt  |
| 5     | PCU        | R/W  | 0h    | Force position counter underflow interrupt<br>0 No effect<br>1 Force the interrupt |

**Table 3-1390. EQEP\_QFRC Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                         |
|-----|------------|------|-------|-------------------------------------------------------------------------------------|
| 4   | WTO        | R/W  | 0h    | Force watchdog time out interrupt<br>0 No effect<br>1 Force the interrupt           |
| 3   | QDC        | R/W  | 0h    | Force quadrature direction change interrupt<br>0 No effect<br>1 Force the interrupt |
| 2   | PHE        | R/W  | 0h    | Force quadrature phase error interrupt<br>0 No effect<br>1 Force the interrupt      |
| 1   | PCE        | R/W  | 0h    | Force position counter error interrupt<br>0 No effect<br>1 Force the interrupt      |
| 0   | RESERVED_1 | R    | 0h    | Reserved                                                                            |

### 3.8.2.20 EQEP\_QEPSTS Register

#### 1 EQEP\_QEPSTS Register (Offset = 38h) [reset = 80h]

QEP Status .

Return to [Summary Table](#)

**Table 3-1391. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EQEP0         | 5027 0038h       |
| EQEP1         | 5027 1038h       |
| EQEP2         | 5027 2038h       |

**Figure 3-444. EQEP\_QEPSTS Name Register**

| 15         | 14   | 13  | 12   | 11     | 10     | 9      | 8    |
|------------|------|-----|------|--------|--------|--------|------|
| RESERVED_1 |      |     |      |        |        |        |      |
| R          |      |     |      |        |        |        |      |
| 0h         |      |     |      |        |        |        |      |
| 7          | 6    | 5   | 4    | 3      | 2      | 1      | 0    |
| UPEVNT     | FIDF | QDF | QDLF | COEF   | CDEF   | FIMF   | PCEF |
| R/W1TS     | R    | R   | R    | R/W1TS | R/W1TS | R/W1TS | R    |
| 1h         | 0h   | 0h  | 0h   | 0h     | 0h     | 0h     | 0h   |

**Table 3-1393. EQEP\_QEPSTS Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                      |
|------|------------|--------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                                                                                         |
| 7    | UPEVNT     | R/W1TS | 1h    | Unit position event flag<br>0 No unit position event detected<br>1 Unit position event detected. Write 1 to clear                                                                                                                                                |
| 6    | FIDF       | R      | 0h    | Direction on the first index marker<br>Status of the direction is latched on the first index event marker.<br>0 Counter-clockwise rotation (or reverse movement) on the first index event<br>1 Clockwise rotation (or forward movement) on the first index event |
| 5    | QDF        | R      | 0h    | Quadrature direction flag<br>0 Counter-clockwise rotation (or reverse movement)<br>1 Clockwise rotation (or forward movement)                                                                                                                                    |
| 4    | QDLF       | R      | 0h    | EQEP direction latch flag<br>0 Counter-clockwise rotation (or reverse movement) on index event marker<br>1 Clockwise rotation (or forward movement) on index event marker                                                                                        |
| 3    | COEF       | R/W1TS | 0h    | Capture overflow error flag<br>0 Overflow has not occurred.<br>1 Overflow occurred in eQEP Capture timer (QEPCTMR). This bit is cleared by writing a '1'.                                                                                                        |
| 2    | CDEF       | R/W1TS | 0h    | Capture direction error flag<br>0 Capture direction error has not occurred.<br>1 Direction change occurred between the capture position event. This bit is cleared by writing a '1'.                                                                             |



**Table 3-1393. EQEP\_QEPSTS Register Field Descriptions (continued)**

| Bit | Field | Type   | Reset | Description                                                                                                                                                                         |
|-----|-------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | FIMF  | R/W1TS | 0h    | First index marker flag<br>0 First index pulse has not occurred.<br>1 Set by first occurrence of index pulse. This bit is cleared by writing a '1'.                                 |
| 0   | PCEF  | R      | 0h    | Position counter error flag.<br>This bit is not sticky and it is updated for every index event.<br>0 No error occurred during the last index transition<br>1 Position counter error |

### 3.8.2.21 EQEP\_QCTMR Register

#### 1 EQEP\_QCTMR Register (Offset = 3Ah) [reset = 0h]

QEP Capture Timer .

Return to [Summary Table](#)

**Table 3-1394. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EQEP0         | 5027 003Ah       |
| EQEP1         | 5027 103Ah       |
| EQEP2         | 5027 203Ah       |

**Figure 3-445. EQEP\_QCTMR Name Register**

|       |    |    |    |    |    |   |   |
|-------|----|----|----|----|----|---|---|
| 15    | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| QCTMR |    |    |    |    |    |   |   |
| R/W   |    |    |    |    |    |   |   |
| 0h    |    |    |    |    |    |   |   |
| 7     | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| QCTMR |    |    |    |    |    |   |   |
| R/W   |    |    |    |    |    |   |   |
| 0h    |    |    |    |    |    |   |   |

**Table 3-1396. EQEP\_QCTMR Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                             |
|------|-------|------|-------|---------------------------------------------------------|
| 15:0 | QCTMR | R/W  | 0h    | This register provides time base for edge capture unit. |

### 3.8.2.22 EQEP\_QCPRD Register

#### 1 EQEP\_QCPRD Register (Offset = 3Ch) [reset = 0h]

QEP Capture Period .

Return to [Summary Table](#)

**Table 3-1397. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EQEP0         | 5027 003Ch       |
| EQEP1         | 5027 103Ch       |
| EQEP2         | 5027 203Ch       |

**Figure 3-446. EQEP\_QCPRD Name Register**

|       |    |    |    |    |    |   |   |
|-------|----|----|----|----|----|---|---|
| 15    | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| QCPRD |    |    |    |    |    |   |   |
| R/W   |    |    |    |    |    |   |   |
| 0h    |    |    |    |    |    |   |   |
| 7     | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| QCPRD |    |    |    |    |    |   |   |
| R/W   |    |    |    |    |    |   |   |
| 0h    |    |    |    |    |    |   |   |

**Table 3-1399. EQEP\_QCPRD Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                 |
|------|-------|------|-------|---------------------------------------------------------------------------------------------|
| 15:0 | QCPRD | R/W  | 0h    | This register holds the period count value between the last successive eQEP position events |

### 3.8.2.23 EQEP\_QCTMRLAT Register

#### 1 EQEP\_QCTMRLAT Register (Offset = 3Eh) [reset = 0h]

QEP Capture Latch .

Return to [Summary Table](#)

**Table 3-1400. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EQEP0         | 5027 003Eh       |
| EQEP1         | 5027 103Eh       |
| EQEP2         | 5027 203Eh       |

**Figure 3-447. EQEP\_QCTMRLAT Name Register**

|          |    |    |    |    |    |   |   |
|----------|----|----|----|----|----|---|---|
| 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| QCTMRLAT |    |    |    |    |    |   |   |
| R        |    |    |    |    |    |   |   |
| 0h       |    |    |    |    |    |   |   |
| 7        | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| QCTMRLAT |    |    |    |    |    |   |   |
| R        |    |    |    |    |    |   |   |
| 0h       |    |    |    |    |    |   |   |

**Table 3-1402. EQEP\_QCTMRLAT Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                               |
|------|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | QCTMRLAT | R    | 0h    | The eQEP capture timer value can be latched into this register on two events viz., unit timeout event, Reading the eQEP position counter. |

### 3.8.2.24 EQEP\_QCPRDLAT Register

#### 1 EQEP\_QCPRDLAT Register (Offset = 40h) [reset = 0h]

QEP Capture Period Latch .

Return to [Summary Table](#)

**Table 3-1403. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EQEP0         | 5027 0040h       |
| EQEP1         | 5027 1040h       |
| EQEP2         | 5027 2040h       |

**Figure 3-448. EQEP\_QCPRDLAT Name Register**

|          |    |    |    |    |    |   |   |
|----------|----|----|----|----|----|---|---|
| 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| QCPRDLAT |    |    |    |    |    |   |   |
| R        |    |    |    |    |    |   |   |
| 0h       |    |    |    |    |    |   |   |
| 7        | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| QCPRDLAT |    |    |    |    |    |   |   |
| R        |    |    |    |    |    |   |   |
| 0h       |    |    |    |    |    |   |   |

**Table 3-1405. EQEP\_QCPRDLAT Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                            |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | QCPRDLAT | R    | 0h    | EQEP capture period value can be latched into this register on two events viz., unit timeout event, Reading the eQEP position counter. |

### 3.8.2.25 EQEP\_REV Register

#### 1 EQEP\_REV Register (Offset = 60h) [reset = 11h]

QEP Revision Number.

Return to [Summary Table](#)

**Table 3-1406. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EQEP0         | 5027 0060h       |
| EQEP1         | 5027 1060h       |
| EQEP2         | 5027 2060h       |

**Figure 3-449. EQEP\_REV Name Register**

|            |    |       |    |    |       |    |    |
|------------|----|-------|----|----|-------|----|----|
| 31         | 30 | 29    | 28 | 27 | 26    | 25 | 24 |
| RESERVED_1 |    |       |    |    |       |    |    |
| R          |    |       |    |    |       |    |    |
| 0h         |    |       |    |    |       |    |    |
| 23         | 22 | 21    | 20 | 19 | 18    | 17 | 16 |
| RESERVED_1 |    |       |    |    |       |    |    |
| R          |    |       |    |    |       |    |    |
| 0h         |    |       |    |    |       |    |    |
| 15         | 14 | 13    | 12 | 11 | 10    | 9  | 8  |
| RESERVED_1 |    |       |    |    |       |    |    |
| R          |    |       |    |    |       |    |    |
| 0h         |    |       |    |    |       |    |    |
| 7          | 6  | 5     | 4  | 3  | 2     | 1  | 0  |
| RESERVED_1 |    | MINOR |    |    | MAJOR |    |    |
| R          |    | R     |    |    | R     |    |    |
| 0h         |    | 2h    |    |    | 1h    |    |    |

**Table 3-1408. EQEP\_REV Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                     |
|------|------------|------|-------|-----------------------------------------------------------------|
| 31:6 | RESERVED_1 | R    | 0h    | Reserved                                                        |
| 5:3  | MINOR      | R    | 2h    | This field specifies the Minor Revision number for the eQEP IP. |
| 2:0  | MAJOR      | R    | 1h    | This field specifies the Major Revision number for the eQEP IP. |

### 3.8.2.26 EQEP\_QMACTRL Register

#### 1 EQEP\_QMACTRL Register (Offset = 68h) [reset = 0h]

QMA Control register.

Return to [Summary Table](#)

**Table 3-1409. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EQEP0         | 5027 0068h       |
| EQEP1         | 5027 1068h       |
| EQEP2         | 5027 2068h       |

**Figure 3-450. EQEP\_QMACTRL Name Register**

|            |    |    |    |    |      |    |    |
|------------|----|----|----|----|------|----|----|
| 31         | 30 | 29 | 28 | 27 | 26   | 25 | 24 |
| RESERVED_1 |    |    |    |    |      |    |    |
| R          |    |    |    |    |      |    |    |
| 0h         |    |    |    |    |      |    |    |
| 23         | 22 | 21 | 20 | 19 | 18   | 17 | 16 |
| RESERVED_1 |    |    |    |    |      |    |    |
| R          |    |    |    |    |      |    |    |
| 0h         |    |    |    |    |      |    |    |
| 15         | 14 | 13 | 12 | 11 | 10   | 9  | 8  |
| RESERVED_1 |    |    |    |    |      |    |    |
| R          |    |    |    |    |      |    |    |
| 0h         |    |    |    |    |      |    |    |
| 7          | 6  | 5  | 4  | 3  | 2    | 1  | 0  |
| RESERVED_1 |    |    |    |    | MODE |    |    |
| R          |    |    |    |    | R/W  |    |    |
| 0h         |    |    |    |    | 0h   |    |    |

**Table 3-1411. EQEP\_QMACTRL Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                    |
|------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                       |
| 2:0  | MODE       | R/W  | 0h    | Select Mode for QMA mode:<br>000 : QMA Module is bypassed.<br>001 : QMA Mode-1 operation selected<br>010 : QMA Mode-2 operation selected<br>011 : QMA Module is bypassed [reserved]<br>1xx : QMA Module is bypassed [reserved] |

### 3.8.2.27 EQEP\_QEPSRCSEL Register

#### 1 EQEP\_QEPSRCSEL Register (Offset = 6Ch) [reset = 0h]

QEP Source Select Register.

Return to [Summary Table](#)

**Table 3-1412. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EQEP0         | 5027 006Ch       |
| EQEP1         | 5027 106Ch       |
| EQEP2         | 5027 206Ch       |

**Figure 3-451. EQEP\_QEPSRCSEL Name Register**

|            |    |    |    |         |    |    |    |
|------------|----|----|----|---------|----|----|----|
| 31         | 30 | 29 | 28 | 27      | 26 | 25 | 24 |
| RESERVED_4 |    |    |    | QEPSSEL |    |    |    |
| R          |    |    |    | R/W     |    |    |    |
| 0h         |    |    |    | 0h      |    |    |    |
| 23         | 22 | 21 | 20 | 19      | 18 | 17 | 16 |
| RESERVED_3 |    |    |    | QEPISEL |    |    |    |
| R          |    |    |    | R/W     |    |    |    |
| 0h         |    |    |    | 0h      |    |    |    |
| 15         | 14 | 13 | 12 | 11      | 10 | 9  | 8  |
| RESERVED_2 |    |    |    | QEPBSEL |    |    |    |
| R          |    |    |    | R/W     |    |    |    |
| 0h         |    |    |    | 0h      |    |    |    |
| 7          | 6  | 5  | 4  | 3       | 2  | 1  | 0  |
| RESERVED_1 |    |    |    | QEPASEL |    |    |    |
| R          |    |    |    | R/W     |    |    |    |
| 0h         |    |    |    | 0h      |    |    |    |

**Table 3-1414. EQEP\_QEPSRCSEL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                 |
|-------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED_4 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                    |
| 28:24 | QEPSSEL    | R/W  | 0h    | QEP Strobe source select:<br>0x0 : Reserved<br>0x1 : Device Pin<br>0x2 : PWMXBAR.Out[0]<br>0x3 : PWMXBAR.Out[1]<br>...<br>0x1F : PWMXBAR.Out[29]<br>Note: eQEP needs to be disabled before configuring these bits as it can lead to unexpected behavior if eQEP is running. |
| 23:21 | RESERVED_3 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                    |
| 20:16 | QEPISEL    | R/W  | 0h    | QEP Index source select:<br>0x0 : Reserved<br>0x1 : Device Pin<br>0x2 : PWMXBAR.Out[0]<br>0x3 : PWMXBAR.Out[1]<br>...<br>0x1F : PWMXBAR.Out[29]<br>Note: eQEP needs to be disabled before configuring these bits as it can lead to unexpected behavior if eQEP is running.  |
| 15:13 | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                    |



**Table 3-1414. EQEP\_QEPSRCSEL Register Field Descriptions (continued)**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                           |
|------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12:8 | QEPBSEL    | R/W  | 0h    | QEPB source select:<br>0x0 : Reserved<br>0x1 : Device Pin<br>0x2 : PWMXBAR.Out[0]<br>0x3 : PWMXBAR.Out[1]<br>...<br>0x1F : PWMXBAR.Out[29]<br>Note: eQEP needs to be disabled before configuring these bits as it can lead to unexpected behavior if eQEP is running. |
| 7:5  | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                              |
| 4:0  | QEPASEL    | R/W  | 0h    | QEPA source select:<br>0x0 : Reserved<br>0x1 : Device Pin<br>0x2 : PWMXBAR.Out[0]<br>0x3 : PWMXBAR.Out[1]<br>...<br>0x1F : PWMXBAR.Out[29]<br>Note: eQEP needs to be disabled before configuring these bits as it can lead to unexpected behavior if eQEP is running. |

## 3.9 FSI\_RX

### FSI\_RX

#### 3.9.1 FSI\_RX Summaries

#### FSI\_RX Summaries

**Table 3-1415. FSI\_RX\_CFG Registers, Base Address=5029 0000h, Length=4096**

| Offset | Length | Register Name                  | FSI_RX0 Physical Address | FSI_RX1 Physical Address | FSI_RX2 Physical Address |
|--------|--------|--------------------------------|--------------------------|--------------------------|--------------------------|
| 0h     | 16     | FSI_RX_CFG_RX_MASTER_CTRL_ALTC | 5029 0000h               | 5029 1000h               | 502B 0000h               |
| 8h     | 16     | FSI_RX_CFG_RX_OPER_CTRL        | 5029 0008h               | 5029 1008h               | 502B 0008h               |
| Ch     | 16     | FSI_RX_CFG_RX_FRAME_INFO       | 5029 000Ch               | 5029 100Ch               | 502B 000Ch               |
| Eh     | 16     | FSI_RX_CFG_RX_FRAME_TAG_UDATA  | 5029 000Eh               | 5029 100Eh               | 502B 000Eh               |
| 10h    | 16     | FSI_RX_CFG_RX_DMA_CTRL         | 5029 0010h               | 5029 1010h               | 502B 0010h               |
| 14h    | 16     | FSI_RX_CFG_RX_EVT_STS_ALT1     | 5029 0014h               | 5029 1014h               | 502B 0014h               |
| 16h    | 16     | FSI_RX_CFG_RX_CRC_INFO         | 5029 0016h               | 5029 1016h               | 502B 0016h               |
| 18h    | 16     | FSI_RX_CFG_RX_EVT_CLR_ALT1     | 5029 0018h               | 5029 1018h               | 502B 0018h               |
| 1Ah    | 16     | FSI_RX_CFG_RX_EVT_FRC_ALT1     | 5029 001Ah               | 5029 101Ah               | 502B 001Ah               |
| 1Ch    | 16     | FSI_RX_CFG_RX_BUF_PTR_LOAD     | 5029 001Ch               | 5029 101Ch               | 502B 001Ch               |
| 1Eh    | 16     | FSI_RX_CFG_RX_BUF_PTR_STS      | 5029 001Eh               | 5029 101Eh               | 502B 001Eh               |
| 20h    | 16     | FSI_RX_CFG_RX_FRAME_WD_CTRL    | 5029 0020h               | 5029 1020h               | 502B 0020h               |
| 24h    | 32     | FSI_RX_CFG_RX_FRAME_WD_REF     | 5029 0024h               | 5029 1024h               | 502B 0024h               |
| 28h    | 32     | FSI_RX_CFG_RX_FRAME_WD_CNT     | 5029 0028h               | 5029 1028h               | 502B 0028h               |
| 2Ch    | 16     | FSI_RX_CFG_RX_PING_WD_CTRL     | 5029 002Ch               | 5029 102Ch               | 502B 002Ch               |
| 2Eh    | 16     | FSI_RX_CFG_RX_PING_TAG         | 5029 002Eh               | 5029 102Eh               | 502B 002Eh               |
| 30h    | 32     | FSI_RX_CFG_RX_PING_WD_REF      | 5029 0030h               | 5029 1030h               | 502B 0030h               |
| 34h    | 32     | FSI_RX_CFG_RX_PING_WD_CNT      | 5029 0034h               | 5029 1034h               | 502B 0034h               |
| 38h    | 16     | FSI_RX_CFG_RX_INT1_CTRL_AL T1  | 5029 0038h               | 5029 1038h               | 502B 0038h               |
| 3Ah    | 16     | FSI_RX_CFG_RX_INT2_CTRL_AL T1  | 5029 003Ah               | 5029 103Ah               | 502B 003Ah               |
| 3Ch    | 16     | FSI_RX_CFG_RX_LOCK_CTRL        | 5029 003Ch               | 5029 103Ch               | 502B 003Ch               |
| 40h    | 32     | FSI_RX_CFG_RX_ECC_DATA         | 5029 0040h               | 5029 1040h               | 502B 0040h               |
| 44h    | 16     | FSI_RX_CFG_RX_ECC_VAL          | 5029 0044h               | 5029 1044h               | 502B 0044h               |
| 48h    | 32     | FSI_RX_CFG_RX_ECC_SEC_DATA     | 5029 0048h               | 5029 1048h               | 502B 0048h               |
| 4Ch    | 16     | FSI_RX_CFG_RX_ECC_LOG          | 5029 004Ch               | 5029 104Ch               | 502B 004Ch               |
| 50h    | 16     | FSI_RX_CFG_RX_FRAME_TAG_CMP    | 5029 0050h               | 5029 1050h               | 502B 0050h               |

**Table 3-1415. FSI\_RX\_CFG Registers, Base Address=5029 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                               | FSI_RX0 Physical Address | FSI_RX1 Physical Address | FSI_RX2 Physical Address |
|--------|--------|---------------------------------------------|--------------------------|--------------------------|--------------------------|
| 52h    | 16     | <a href="#">FSI_RX_CFG_RX_PING_TAG_CM_P</a> | 5029 0052h               | 5029 1052h               | 502B 0052h               |
| 58h    | 32     | <a href="#">FSI_RX_CFG_RX_TRIG_CTRL_0</a>   | 5029 0058h               | 5029 1058h               | 502B 0058h               |
| 5Ch    | 32     | <a href="#">FSI_RX_CFG_RX_TRIG_WIDTH_0</a>  | 5029 005Ch               | 5029 105Ch               | 502B 005Ch               |
| 60h    | 16     | <a href="#">FSI_RX_CFG_RX_DLYLINE_CTRL</a>  | 5029 0060h               | 5029 1060h               | 502B 0060h               |
| 64h    | 32     | <a href="#">FSI_RX_CFG_RX_TRIG_CTRL_1</a>   | 5029 0064h               | 5029 1064h               | 502B 0064h               |
| 68h    | 32     | <a href="#">FSI_RX_CFG_RX_TRIG_CTRL_2</a>   | 5029 0068h               | 5029 1068h               | 502B 0068h               |
| 6Ch    | 32     | <a href="#">FSI_RX_CFG_RX_TRIG_CTRL_3</a>   | 5029 006Ch               | 5029 106Ch               | 502B 006Ch               |
| 70h    | 32     | <a href="#">FSI_RX_CFG_RX_VIS_1</a>         | 5029 0070h               | 5029 1070h               | 502B 0070h               |
| 74h    | 16     | <a href="#">FSI_RX_CFG_RX_UDATA_FILTER</a>  | 5029 0074h               | 5029 1074h               | 502B 0074h               |
| 80h    | 16     | <a href="#">FSI_RX_CFG_RX_BUF_BASE_J</a>    | 5029 0080h + formula     | 5029 1080h + formula     | 502B 0080h + formula     |

**Table 3-1416. FSI\_RX\_CFG Registers, Base Address=5029 0000h, Length=4096**

| Offset | Length | Register Name                                  | FSI_RX3 Physical Address |
|--------|--------|------------------------------------------------|--------------------------|
| 0h     | 16     | <a href="#">FSI_RX_CFG_RX_MASTER_CTRL_ALTC</a> | 502B 1000h               |
| 8h     | 16     | <a href="#">FSI_RX_CFG_RX_OPER_CTRL</a>        | 502B 1008h               |
| Ch     | 16     | <a href="#">FSI_RX_CFG_RX_FRAME_INFO</a>       | 502B 100Ch               |
| Eh     | 16     | <a href="#">FSI_RX_CFG_RX_FRAME_TAG_UDATA</a>  | 502B 100Eh               |
| 10h    | 16     | <a href="#">FSI_RX_CFG_RX_DMA_CTRL</a>         | 502B 1010h               |
| 14h    | 16     | <a href="#">FSI_RX_CFG_RX_EVT_STS_ALT1</a>     | 502B 1014h               |
| 16h    | 16     | <a href="#">FSI_RX_CFG_RX_CRC_INFO</a>         | 502B 1016h               |
| 18h    | 16     | <a href="#">FSI_RX_CFG_RX_EVT_CLR_ALT1</a>     | 502B 1018h               |
| 1Ah    | 16     | <a href="#">FSI_RX_CFG_RX_EVT_FRC_ALT1</a>     | 502B 101Ah               |
| 1Ch    | 16     | <a href="#">FSI_RX_CFG_RX_BUF_PTR_LOAD</a>     | 502B 101Ch               |
| 1Eh    | 16     | <a href="#">FSI_RX_CFG_RX_BUF_PTR_STS</a>      | 502B 101Eh               |
| 20h    | 16     | <a href="#">FSI_RX_CFG_RX_FRAME_WD_CTRL</a>    | 502B 1020h               |
| 24h    | 32     | <a href="#">FSI_RX_CFG_RX_FRAME_WD_REF</a>     | 502B 1024h               |
| 28h    | 32     | <a href="#">FSI_RX_CFG_RX_FRAME_WD_CNT</a>     | 502B 1028h               |
| 2Ch    | 16     | <a href="#">FSI_RX_CFG_RX_PING_WD_CTRL</a>     | 502B 102Ch               |
| 2Eh    | 16     | <a href="#">FSI_RX_CFG_RX_PING_TAG</a>         | 502B 102Eh               |
| 30h    | 32     | <a href="#">FSI_RX_CFG_RX_PING_WD_REF</a>      | 502B 1030h               |
| 34h    | 32     | <a href="#">FSI_RX_CFG_RX_PING_WD_CNT</a>      | 502B 1034h               |
| 38h    | 16     | <a href="#">FSI_RX_CFG_RX_INT1_CTRL_ALT1</a>   | 502B 1038h               |
| 3Ah    | 16     | <a href="#">FSI_RX_CFG_RX_INT2_CTRL_ALT1</a>   | 502B 103Ah               |
| 3Ch    | 16     | <a href="#">FSI_RX_CFG_RX_LOCK_CTRL</a>        | 502B 103Ch               |
| 40h    | 32     | <a href="#">FSI_RX_CFG_RX_ECC_DATA</a>         | 502B 1040h               |
| 44h    | 16     | <a href="#">FSI_RX_CFG_RX_ECC_VAL</a>          | 502B 1044h               |
| 48h    | 32     | <a href="#">FSI_RX_CFG_RX_ECC_SEC_DATA</a>     | 502B 1048h               |
| 4Ch    | 16     | <a href="#">FSI_RX_CFG_RX_ECC_LOG</a>          | 502B 104Ch               |
| 50h    | 16     | <a href="#">FSI_RX_CFG_RX_FRAME_TAG_CMP</a>    | 502B 1050h               |
| 52h    | 16     | <a href="#">FSI_RX_CFG_RX_PING_TAG_CMP</a>     | 502B 1052h               |
| 58h    | 32     | <a href="#">FSI_RX_CFG_RX_TRIG_CTRL_0</a>      | 502B 1058h               |
| 5Ch    | 32     | <a href="#">FSI_RX_CFG_RX_TRIG_WIDTH_0</a>     | 502B 105Ch               |

**Table 3-1416. FSI\_RX\_CFG Registers, Base Address=5029 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                              | FSI_RX3 Physical Address |
|--------|--------|--------------------------------------------|--------------------------|
| 60h    | 16     | <a href="#">FSI_RX_CFG_RX_DLYLINE_CTRL</a> | 502B 1060h               |
| 64h    | 32     | <a href="#">FSI_RX_CFG_RX_TRIG_CTRL_1</a>  | 502B 1064h               |
| 68h    | 32     | <a href="#">FSI_RX_CFG_RX_TRIG_CTRL_2</a>  | 502B 1068h               |
| 6Ch    | 32     | <a href="#">FSI_RX_CFG_RX_TRIG_CTRL_3</a>  | 502B 106Ch               |
| 70h    | 32     | <a href="#">FSI_RX_CFG_RX_VIS_1</a>        | 502B 1070h               |
| 74h    | 16     | <a href="#">FSI_RX_CFG_RX_UDATA_FILTER</a> | 502B 1074h               |
| 80h    | 16     | <a href="#">FSI_RX_CFG_RX_BUF_BASE_J</a>   | 502B 1080h + formula     |

### 3.9.2 FSI\_RX Registers

#### FSI\_RX Registers

### 3.9.2.1 FSI\_RX\_CFG\_RX\_MASTER\_CTRL\_ALTC Register

#### 1 FSI\_RX\_CFG\_RX\_MASTER\_CTRL\_ALTC Register (Offset = 0h) [reset = 0h]

Receive master control register.

Return to [Summary Table](#)

**Table 3-1417. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 0000h       |
| FSI_RX1       | 5029 1000h       |
| FSI_RX2       | 502B 0000h       |
| FSI_RX3       | 502B 1000h       |

**Figure 3-452. FSI\_RX\_CFG\_RX\_MASTER\_CTRL\_ALTC Name Register**

|            |    |    |                |               |             |              |          |
|------------|----|----|----------------|---------------|-------------|--------------|----------|
| 15         | 14 | 13 | 12             | 11            | 10          | 9            | 8        |
| KEY        |    |    |                |               |             |              |          |
| W          |    |    |                |               |             |              |          |
| 0h         |    |    |                |               |             |              |          |
| 7          | 6  | 5  | 4              | 3             | 2           | 1            | 0        |
| RESERVED_1 |    |    | DATA_FILTER_EN | INPUT_ISOLATE | SPI_PAIRING | INT_LOOPBACK | CORE_RST |
| R          |    |    | R/W            | R/W           | R/W         | R/W          | R/W      |
| 0h         |    |    | 0h             | 0h            | 0h          | 0h           | 0h       |

**Table 3-1419. FSI\_RX\_CFG\_RX\_MASTER\_CTRL\_ALTC Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|------|----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | KEY            | W    | 0h    | Write Key.<br>In order to write to this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after Writing, so it must be written again for every change to this register.                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 7:5  | RESERVED_1     | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 4    | DATA_FILTER_EN | R/W  | 0h    | Data Filter Enable Bit.<br>0h[R/W] = Data filtering is disabled.<br>1h[R/W] = Data filtering is enabled.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 3    | INPUT_ISOLATE  | R/W  | 0h    | When set to 1, the FSI RX inputs [RXCLK, RXD0 and RXD1] will be isolated from what is driven from the device pins and will be held at inactive level of '1'. This isolation facilitates the user to switch the RX inputs to a different set of device pins and hence any potential glitch that could occur during the process of switching will not effect the RX module itself.                                                                                                                                                                                                                                                                                                   |
| 2    | SPI_PAIRING    | R/W  | 0h    | Clock Pairing for SPI-like Behavior Enable bit<br>This bit enables the internal clock pairing with the FSI TX module. This feature internally connects the TXCLK to RXCLK allowing the FSI TX module, acting as a SPI master, to clock data into the receiver and out of the transmitter like a standard SPI module. This configuration is valid when the Module is in SPI mode only [RX_OPER_CTRL.SPI_MODE = 1]<br>0h[R/W] = SPI clock pairing is not enabled.<br>1h[R/W] = SPI clock pairing is enabled. The RXCLK will be internally connected to the TXCLK of the corresponding FSI module.<br>Note: The KEY field must contain 0xA5 for any write to this bit to take effect. |

**Table 3-1419. FSI\_RX\_CFG\_RX\_MASTER\_CTRL\_ALTC Register Field Descriptions (continued)**

| Bit | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|--------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | INT_LOOPBACK | R/W  | 0h    | <p>Internal Loopback Enable bit</p> <p>This bit enables the internal loopback functionality of the FSI receiver. By enabling this bit, a mux will select the signals coming directly from the corresponding FSI transmitter module rather than from the pins.</p> <p>0h[R/W] = Internal loopback is disabled. The FSI RX module will receive signals coming from the pins.</p> <p>1h[R/W] = Internal loopback is enabled. The FSI RX module will receive signals from the directly from FSI TX module rather than the pins.</p> <p>Note: The KEY field must contain 0xA5 for any write to this bit to take effect.</p> |
| 0   | CORE_RST     | R/W  | 0h    | <p>Receiver Controller Core Reset bit</p> <p>This bit controls the receiver master core reset. In order to receive any frame, this bit must be cleared.</p> <p>Note: For reset to take effect, the FSI RX module must be held in reset for at least 4 SYSCLK cycles.</p> <p>0h[R/W] = Receiver core is not in reset and can receive frames.</p> <p>1h[R/W] = Receiver core is held in reset.</p> <p>Note: The KEY field must contain 0xA5 for any write to this bit to take effect.</p>                                                                                                                                |

### 3.9.2.2 FSI\_RX\_CFG\_RX\_OPER\_CTRL Register

#### 1 FSI\_RX\_CFG\_RX\_OPER\_CTRL Register (Offset = 8h) [reset = 0h]

Receive operation control register.

Return to [Summary Table](#)

**Table 3-1420. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 0008h       |
| FSI_RX1       | 5029 1008h       |
| FSI_RX2       | 502B 0008h       |
| FSI_RX3       | 502B 1008h       |

**Figure 3-453. FSI\_RX\_CFG\_RX\_OPER\_CTRL Name Register**

| 15         | 14      | 13 | 12 | 11 | 10       | 9          | 8                |
|------------|---------|----|----|----|----------|------------|------------------|
| RESERVED_1 |         |    |    |    |          |            | PING_WD_RST_MODE |
| R          |         |    |    |    |          |            | R/W              |
| 0h         |         |    |    |    |          |            | 0h               |
| 7          | 6       | 5  | 4  | 3  | 2        | 1          | 0                |
| ECC_SEL    | N_WORDS |    |    |    | SPI_MODE | DATA_WIDTH |                  |
| R/W        | R/W     |    |    |    | R/W      | R/W        |                  |
| 0h         | 0h      |    |    |    | 0h       | 0h         |                  |

**Table 3-1422. FSI\_RX\_CFG\_RX\_OPER\_CTRL Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:9 | RESERVED_1       | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 8    | PING_WD_RST_MODE | R/W  | 0h    | Ping Watchdog Timeout Mode Select bit<br>This bit selects the mode by which the ping watchdog counter is reset. The watchdog counter can be reset and restarted only by ping frames or by any received frame.<br>0h[R/W] = The ping watchdog counter will reset and restart only by ping frames.<br>1h[R/W] = The ping watchdog counter will reset and restart by any received frame.                                                                                                                                |
| 7    | ECC_SEL          | R/W  | 0h    | ECC Data Width Select bit<br>This bit selects between whether the ECC computation is done on 16-bit or 32-bit words.<br>0h[R/W] = 32-bit ECC is used.<br>1h[R/W] = 16-bit ECC is used.                                                                                                                                                                                                                                                                                                                               |
| 6:3  | N_WORDS          | R/W  | 0h    | Number of Words to Receive<br>This field defines the number of words which will be received in a DATA_N_WORD frame. This is a user-defined field that must match the corresponding field in the transmitter. Set this bitfield to be one less than the number of words to be received. This value is only applicable when the frame type received is DATA_N_WORD.<br>0h[R/W] = 1 data word frame [16-bit data].<br>1h[R/W] = 2 data word frame [32-bit data].<br>..<br>Fh [R/W] = 16 data word frame [256-bit data]. |

**Table 3-1422. FSI\_RX\_CFG\_RX\_OPER\_CTRL Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | SPI_MODE   | R/W  | 0h    | <p>SPI Mode Enable bit</p> <p>This bit enables and disables the SPI compatibility mode of the FSI RX. The received data must be formatted as an FSI frame in order for the data to properly be received. SPI compatibility mode will allow FSI RX to receive data that is sent using SPI signal format. Refer to the applicable section in the FSI TRM chapter for more information.</p> <p>0h[R/W] = FSI is in normal mode of operation.</p> <p>1h[R/W] = FSI is operating in SPI compatibility mode.</p> |
| 1:0 | DATA_WIDTH | R/W  | 0h    | <p>Receive Data Width Select bit</p> <p>These bits decide the number of data lines used for receiving data.</p> <p>0h[R/W] = Data will be received on one data line, RXD0.</p> <p>1h[R/W] = Data will be received on two data lines, RXD0 and RXD1.</p> <p>2h</p> <p>3h[R/W] = Reserved</p>                                                                                                                                                                                                                |



### 3.9.2.3 FSI\_RX\_CFG\_RX\_FRAME\_INFO Register

#### 1 FSI\_RX\_CFG\_RX\_FRAME\_INFO Register (Offset = Ch) [reset = 0h]

Receive frame control register.

Return to [Summary Table](#)

**Table 3-1423. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 000Ch       |
| FSI_RX1       | 5029 100Ch       |
| FSI_RX2       | 502B 000Ch       |
| FSI_RX3       | 502B 100Ch       |

**Figure 3-454. FSI\_RX\_CFG\_RX\_FRAME\_INFO Name Register**

|            |    |    |    |            |    |   |   |
|------------|----|----|----|------------|----|---|---|
| 15         | 14 | 13 | 12 | 11         | 10 | 9 | 8 |
| RESERVED_1 |    |    |    |            |    |   |   |
| R          |    |    |    |            |    |   |   |
| 0h         |    |    |    |            |    |   |   |
| 7          | 6  | 5  | 4  | 3          | 2  | 1 | 0 |
| RESERVED_1 |    |    |    | FRAME_TYPE |    |   |   |
| R          |    |    |    | R          |    |   |   |
| 0h         |    |    |    | 0h         |    |   |   |

**Table 3-1425. FSI\_RX\_CFG\_RX\_FRAME\_INFO Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:4 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 3:0  | FRAME_TYPE | R    | 0h    | <p>Received Frame Type</p> <p>This field indicates the type of frame that was successfully received last.</p> <p>0000b[R/W] = A ping frame was received</p> <p>0100b[R/W] = A DATA_1_WORD frame was received [16-bit data].</p> <p>0101b[R/W] = A DATA_2_WORD frame was received [32-bit data].</p> <p>0110b[R/W] = A DATA_4_WORD frame was received [64-bit data].</p> <p>0111b[R/W] = A DATA_6_WORD frame was received [96-bit data].</p> <p>0011b[R/W] = A DATA_N_WORD frame was received. The N_WORD field will determine the number of words [1 to 16] to be sent. The number of words received must equal the value programmed in RX_OPER_CTRL.N_WORDS.</p> <p>1111b[R/W] = An error frame was received. This frame can be used during error conditions or any condition where the transmitter wants to signal the receiver for attention. However, the user software is at liberty to use this for any purpose.</p> <p>0001b</p> <p>0010b and</p> <p>1000bthrough</p> <p>1110bare Reserved and should not be used.</p> |

### 3.9.2.4 FSI\_RX\_CFG\_RX\_FRAME\_TAG\_UDATA Register

#### 1 FSI\_RX\_CFG\_RX\_FRAME\_TAG\_UDATA Register (Offset = Eh) [reset = 0h]

Receive frame tag and user data register.

Return to [Summary Table](#)

**Table 3-1426. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 000Eh       |
| FSI_RX1       | 5029 100Eh       |
| FSI_RX2       | 502B 000Eh       |
| FSI_RX3       | 502B 100Eh       |

**Figure 3-455. FSI\_RX\_CFG\_RX\_FRAME\_TAG\_UDATA Name Register**

|            |    |    |           |    |    |      |   |
|------------|----|----|-----------|----|----|------|---|
| 15         | 14 | 13 | 12        | 11 | 10 | 9    | 8 |
| USER_DATA  |    |    |           |    |    |      |   |
| R          |    |    |           |    |    |      |   |
| 0h         |    |    |           |    |    |      |   |
| 7          | 6  | 5  | 4         | 3  | 2  | 1    | 0 |
| RESERVED_1 |    |    | FRAME_TAG |    |    | ZERO |   |
| R          |    |    | R         |    |    | R    |   |
| 0h         |    |    | 0h        |    |    | 0h   |   |

**Table 3-1428. FSI\_RX\_CFG\_RX\_FRAME\_TAG\_UDATA Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                            |
|------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | USER_DATA  | R    | 0h    | Received User Data<br>This field contains the 8-bit user data field of the last successfully received frame.                                                                                                                                           |
| 7:5  | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                               |
| 4:1  | FRAME_TAG  | R    | 0h    | Received Frame Tag<br>This field contains the 4-bit frame tag from the last successfully received frame. This is intentionally shifted into bits 4:1 so that the register can be used as a 32-bit address index based on the received tag.             |
| 0    | ZERO       | R    | 0h    | Zero bit<br>This bit will always read as 0. This is intentionally provided to create a 32-bit offset if required. Using the FRAME_TAG and ZERO bits of this register [bits 4:0], application software can directly index into an array of 32-bit data. |

### 3.9.2.5 FSI\_RX\_CFG\_RX\_DMA\_CTRL Register

#### 1 FSI\_RX\_CFG\_RX\_DMA\_CTRL Register (Offset = 10h) [reset = 0h]

Receive DMA event control register.

Return to [Summary Table](#)

**Table 3-1429. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 0010h       |
| FSI_RX1       | 5029 1010h       |
| FSI_RX2       | 502B 0010h       |
| FSI_RX3       | 502B 1010h       |

**Figure 3-456. FSI\_RX\_CFG\_RX\_DMA\_CTRL Name Register**

|            |    |    |    |    |    |   |            |
|------------|----|----|----|----|----|---|------------|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8          |
| RESERVED_1 |    |    |    |    |    |   |            |
| R          |    |    |    |    |    |   |            |
| 0h         |    |    |    |    |    |   |            |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0          |
| RESERVED_1 |    |    |    |    |    |   | DMA_EVT_EN |
| R          |    |    |    |    |    |   | R/W        |
| 0h         |    |    |    |    |    |   | 0h         |

**Table 3-1431. FSI\_RX\_CFG\_RX\_DMA\_CTRL Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:1 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                           |
| 0    | DMA_EVT_EN | R/W  | 0h    | <p>DMA Event Enable bit</p> <p>This bit will enable a DMA Event to be generated upon the completion of a frame reception.</p> <p>0h[R/W] = A DMA event will not be generated.</p> <p>1h[R/W] = A DMA event will be generated upon the reception of a frame.</p> <p>Note: The DMA event will only be generated for data frames.</p> |

### 3.9.2.6 FSI\_RX\_CFG\_RX\_EVT\_STS\_ALT1 Register

#### 1 FSI\_RX\_CFG\_RX\_EVT\_STS\_ALT1 Register (Offset = 14h) [reset = 0h]

Receive event and error status flag register.

Return to [Summary Table](#)

**Table 3-1432. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 0014h       |
| FSI_RX1       | 5029 1014h       |
| FSI_RX2       | 502B 0014h       |
| FSI_RX3       | 502B 1014h       |

**Figure 3-457. FSI\_RX\_CFG\_RX\_EVT\_STS\_ALT1 Name Register**

| 15            | 14              | 13             | 12             | 11         | 10             | 9                | 8               |
|---------------|-----------------|----------------|----------------|------------|----------------|------------------|-----------------|
| RESERVED_1    | ERROR_TAG_MATCH | DATA_TAG_MATCH | PING_TAG_MATCH | DATA_FRAME | FRAME_OVERFLOW | PING_FRAME       | ERR_FRAME       |
| R             | R               | R              | R              | R          | R              | R                | R               |
| 0h            | 0h              | 0h             | 0h             | 0h         | 0h             | 0h               | 0h              |
| 7             | 6               | 5              | 4              | 3          | 2              | 1                | 0               |
| BUF_UNDERFLOW | FRAME_DONE      | BUF_OVERRUN    | EOF_ERR        | TYPE_ERR   | CRC_ERR        | FRAME_WD_TIMEOUT | PING_WD_TIMEOUT |
| R             | R               | R              | R              | R          | R              | R                | R               |
| 0h            | 0h              | 0h             | 0h             | 0h         | 0h             | 0h               | 0h              |

**Table 3-1434. FSI\_RX\_CFG\_RX\_EVT\_STS\_ALT1 Register Field Descriptions**

| Bit | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                      |
|-----|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | RESERVED_1      | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                         |
| 14  | ERROR_TAG_MATCH | R    | 0h    | Error Tag Match Flag<br>This bit indicates that an error frame was received with a tag comparison matching the masked tag reference. Software can also force this bit to get set by Writing to the RX_EVT_FRC register.<br>0h[R] = No tag-matched error frame received.<br>1h[R] = A tag-matched error frame has been received.<br>To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. |
| 13  | DATA_TAG_MATCH  | R    | 0h    | Data Tag Match Flag<br>This bit indicates that a dataframe was received with a tag comparison matching the masked tag reference. Software can also force this bit to get set by Writing to the RX_EVT_FRC register.<br>0h[R] = No tag-matched data frame received.<br>1h[R] = A tag-matched data frame has been received.<br>To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.       |
| 12  | PING_TAG_MATCH  | R    | 0h    | Ping Tag Match Flag<br>This bit indicates that a ping frame was received with a tag comparison matching the masked tag reference. Software can also force this bit to get set by Writing to the RX_EVT_FRC register.<br>0h[R] = No tag-matched ping frame received.<br>1h[R] = A tag-matched ping frame has been received.<br>To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.      |

**Table 3-1434. FSI\_RX\_CFG\_RX\_EVT\_STS\_ALT1 Register Field Descriptions (continued)**

| Bit | Field         | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-----|---------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11  | DATA_FRAME    | R    | 0h    | <p>Data Frame Received Flag</p> <p>This bit indicates that an data frame has been received. Software can also force this bit to get set by Writing to the RX_EVT_FRC register.</p> <p>0h[R] = No data frame has been received.</p> <p>1h[R] = A data frame has been received.</p> <p>To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.</p>                                                                                                                                           |
| 10  | FRAME_OVERRUN | R    | 0h    | <p>Frame Overrun Flag</p> <p>This bit indicates that a frame overrun condition has occurred. This bit gets set to 1 when a new DATA/ERROR frame is received and the corresponding DATA_FRAME_RCVD/ERROR_FRAME_RCVD flag is still set to 1. Software can also force this bit to get set by Writing to the RX_EVT_FRC register.</p> <p>0h[R] = Frame overrun has not occurred.</p> <p>1h[R] = Frame overrun has occurred.</p> <p>To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.</p> |
| 9   | PING_FRAME    | R    | 0h    | <p>Ping Frame Received Flag</p> <p>This bit indicates that an ping frame has been received. Software can also force this bit to get set by Writing to the RX_EVT_FRC register.</p> <p>0h[R] = No ping frame has been received.</p> <p>1h[R] = A ping frame has been received.</p> <p>To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.</p>                                                                                                                                           |
| 8   | ERR_FRAME     | R    | 0h    | <p>Error Frame Received Flag</p> <p>This bit indicates that an error frame has been received. Software can also force this bit to get set by Writing to the RX_EVT_FRC register.</p> <p>0h[R] = No error frame has been received.</p> <p>1h[R] = An error frame has been received.</p> <p>To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.</p>                                                                                                                                      |
| 7   | BUF_UNDERRUN  | R    | 0h    | <p>Receive Buffer Underrun Flag</p> <p>This bit indicates that a buffer underrun condition has occurred in the receive buffer. This will happen when software reads the buffer which is empty and has no valid data. Software can also force this bit to get set by Writing to the RX_EVT_FRC register.</p> <p>0h[R] = Receive Buffer Underrun has not occurred.</p> <p>1h[R] = Receive Buffer Underrun has occurred.</p> <p>To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.</p>   |
| 6   | FRAME_DONE    | R    | 0h    | <p>Frame Done Flag</p> <p>This bit indicates that a frame has been successfully received without error. Software can also force this bit to get set by Writing to the RX_EVT_FRC register.</p> <p>0h[R] = No frame has been successfully received.</p> <p>1h[R] = A frame has been successfully received.</p> <p>To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.</p>                                                                                                               |
| 5   | BUF_OVERRUN   | R    | 0h    | <p>Receive Buffer Overrun Flag</p> <p>This bit indicates that a buffer overrun condition has occurred in the receive buffer. Software can also force this bit to get set by Writing to the RX_EVT_FRC register.</p> <p>0h[R] = Receive buffer overrun has not occurred.</p> <p>1h[R] = Receive buffer overrun has occurred.</p> <p>To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.</p>                                                                                             |

**Table 3-1434. FSI\_RX\_CFG\_RX\_EVT\_STS\_ALT1 Register Field Descriptions (continued)**

| Bit | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                               |
|-----|-------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | EOF_ERR     | R    | 0h    | End-of-Frame Error Flag<br>This bit indicates that an invalid end-of-frame bit pattern has been received. Software can also force this bit to get set by Writing to the RX_EVT_FRC register.<br>0h[R] = Invalid end-of-frame has not been received.<br>1h[R] = Invalid end-of-frame has been received<br>To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.                                    |
| 3   | TYPE_ERR    | R    | 0h    | Frame Type Error Flag<br>This bit indicates that an invalid frame type has been received. Software can also force this bit to get set by Writing to the RX_EVT_FRC register.<br>0h[R] = Invalid frame type has not been received.<br>1h[R] = Invalid frame type has been received<br>To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.                                                        |
| 2   | CRC_ERR     | R    | 0h    | CRC Error Flag<br>This bit indicates that a CRC error has occurred. A CRC error will be generated on a data frame where the received CRC and the computed CRC do not match. Software can also force this bit to get set by Writing to the RX_EVT_FRC register.<br>0h[R] = CRC error has not occurred.<br>1h[R] = CRC error has occurred.<br>To clear this bit, write to the corresponding bit in the RX_EVT_CLR register. |
| 1   | FRAME_WD_TO | R    | 0h    | Frame Watchdog Timeout Flag<br>This bit indicates that the frame watchdog timer has timed out. Software can also force this bit to get set by Writing to the RX_EVT_FRC register.<br>0h[R] = Frame watchdog timeout has not occurred.<br>1h[R] = Frame watchdog timeout has occurred.<br>To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.                                                    |
| 0   | PING_WD_TO  | R    | 0h    | Ping Watchdog Timeout Flag<br>This bit indicates that the ping watchdog timer has timed out. Software can also force this bit to get set by Writing to the RX_EVT_FRC register.<br>0h[R] = Ping watchdog timeout has not occurred.<br>1h[R] = Ping watchdog timeout has occurred.<br>To clear this bit, write to the corresponding bit in the RX_EVT_CLR register.                                                        |

### 3.9.2.7 FSI\_RX\_CFG\_RX\_CRC\_INFO Register

#### 1 FSI\_RX\_CFG\_RX\_CRC\_INFO Register (Offset = 16h) [reset = 0h]

Receive CRC info of received and computed CRC.

Return to [Summary Table](#)

**Table 3-1435. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 0016h       |
| FSI_RX1       | 5029 1016h       |
| FSI_RX2       | 502B 0016h       |
| FSI_RX3       | 502B 1016h       |

**Figure 3-458. FSI\_RX\_CFG\_RX\_CRC\_INFO Name Register**

|          |    |    |    |    |    |   |   |
|----------|----|----|----|----|----|---|---|
| 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CALC_CRC |    |    |    |    |    |   |   |
| R        |    |    |    |    |    |   |   |
| 0h       |    |    |    |    |    |   |   |
| 7        | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| RX_CRC   |    |    |    |    |    |   |   |
| R        |    |    |    |    |    |   |   |
| 0h       |    |    |    |    |    |   |   |

**Table 3-1437. FSI\_RX\_CFG\_RX\_CRC\_INFO Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                    |
|------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | CALC_CRC | R    | 0h    | Hardware Calculated CRC Value<br>This bitfield contains the CRC value that was calculated on the last received data. The contents of this bitfield are valid only when data frames are received.<br>Note: The contents of this bitfield are invalid for ping and error frames. |
| 7:0  | RX_CRC   | R    | 0h    | Received CRC Value<br>This bitfield contains the CRC value that was last received a frame. The contents of this bitfield are valid only when data frames are received.<br>Note: The contents of this bitfield are invalid for ping and error frames.                           |

### 3.9.2.8 FSI\_RX\_CFG\_RX\_EVT\_CLR\_ALT1 Register

#### 1 FSI\_RX\_CFG\_RX\_EVT\_CLR\_ALT1 Register (Offset = 18h) [reset = 0h]

Receive event and error clear register.

Return to [Summary Table](#)

**Table 3-1438. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 0018h       |
| FSI_RX1       | 5029 1018h       |
| FSI_RX2       | 502B 0018h       |
| FSI_RX3       | 502B 1018h       |

**Figure 3-459. FSI\_RX\_CFG\_RX\_EVT\_CLR\_ALT1 Name Register**

| 15           | 14              | 13             | 12             | 11         | 10             | 9           | 8          |
|--------------|-----------------|----------------|----------------|------------|----------------|-------------|------------|
| RESERVED_1   | ERROR_TAG_MATCH | DATA_TAG_MATCH | PING_TAG_MATCH | DATA_FRAME | FRAME_OVERFLOW | PING_FRAME  | ERR_FRAME  |
| R            | W               | W              | W              | W          | W              | W           | W          |
| 0h           | 0h              | 0h             | 0h             | 0h         | 0h             | 0h          | 0h         |
| 7            | 6               | 5              | 4              | 3          | 2              | 1           | 0          |
| BUF_UNDERRUN | FRAME_DONE      | BUF_OVERRUN    | EOF_ERR        | TYPE_ERR   | CRC_ERR        | FRAME_WDT_O | PING_WDT_O |
| W            | W               | W              | W              | W          | W              | W           | W          |
| 0h           | 0h              | 0h             | 0h             | 0h         | 0h             | 0h          | 0h         |

**Table 3-1440. FSI\_RX\_CFG\_RX\_EVT\_CLR\_ALT1 Register Field Descriptions**

| Bit | Field           | Type | Reset | Description                                                                                                                                                                                                                                                          |
|-----|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | RESERVED_1      | R    | 0h    | Reserved                                                                                                                                                                                                                                                             |
| 14  | ERROR_TAG_MATCH | W    | 0h    | Error Tag Match Flag Clear bit<br>This bit clears the corresponding bit in the RX_EVT_STS register.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.     |
| 13  | DATA_TAG_MATCH  | W    | 0h    | Data Tag Match Flag Clear bit<br>This bit clears the corresponding bit in the RX_EVT_STS register.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.      |
| 12  | PING_TAG_MATCH  | W    | 0h    | Ping Tag Match Flag Clear bit<br>This bit clears the corresponding bit in the RX_EVT_STS register.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.      |
| 11  | DATA_FRAME      | W    | 0h    | Data Frame Received Flag Clear bit<br>This bit clears the corresponding bit in the RX_EVT_STS register.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. |
| 10  | FRAME_OVERRUN   | W    | 0h    | Frame Overrun Flag Clear bit<br>This bit clears the corresponding bit in the RX_EVT_STS register.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.       |



**Table 3-1440. FSI\_RX\_CFG\_RX\_EVT\_CLR\_ALT1 Register Field Descriptions (continued)**

| Bit | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                  |
|-----|--------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9   | PING_FRAME   | W    | 0h    | Ping Frame Received Flag Clear bit<br>This bit clears the corresponding bit in the RX_EVT_STS register.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.         |
| 8   | ERR_FRAME    | W    | 0h    | Error Frame Received Flag Clear bit<br>This bit clears the corresponding bit in the RX_EVT_STS register.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.        |
| 7   | BUF_UNDERRUN | W    | 0h    | Receive Buffer Underrun Flag Clear bit<br>This bit clears the corresponding bit in the RX_EVT_STS register.<br>0h[R/W] = Writing a 0 to this bit will have no effect.<br>1h[R/W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0. |
| 6   | FRAME_DONE   | W    | 0h    | Frame Done Flag Clear bit<br>This bit clears the corresponding bit in the RX_EVT_STS register.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.                  |
| 5   | BUF_OVERRUN  | W    | 0h    | Receive Buffer Overrun Flag Clear bit<br>This bit clears the corresponding bit in the RX_EVT_STS register.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.      |
| 4   | EOF_ERR      | W    | 0h    | End-of-Frame Error Flag Clear bit<br>This bit clears the corresponding bit in the RX_EVT_STS register.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.          |
| 3   | TYPE_ERR     | W    | 0h    | Frame Type Error Flag Clear bit<br>This bit clears the corresponding bit in the RX_EVT_STS register.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.            |
| 2   | CRC_ERR      | W    | 0h    | CRC Error Flag Clear bit<br>This bit clears the corresponding bit in the RX_EVT_STS register.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.                   |
| 1   | FRAME_WD_TO  | W    | 0h    | Frame Watchdog Timeout Flag Clear bit<br>This bit clears the corresponding bit in the RX_EVT_STS register.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.      |
| 0   | PING_WD_TO   | W    | 0h    | Ping Watchdog Timeout Flag Clear bit<br>This bit clears the corresponding bit in the RX_EVT_STS register.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Writing a 1 to this bit will clear the corresponding bit in the RX_EVT_STS register to 0.       |

### 3.9.2.9 FSI\_RX\_CFG\_RX\_EVT\_FRC\_ALT1 Register

#### 1 FSI\_RX\_CFG\_RX\_EVT\_FRC\_ALT1 Register (Offset = 1Ah) [reset = 0h]

Receive event and error flag force register.

Return to [Summary Table](#)

**Table 3-1441. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 001Ah       |
| FSI_RX1       | 5029 101Ah       |
| FSI_RX2       | 502B 001Ah       |
| FSI_RX3       | 502B 101Ah       |

**Figure 3-460. FSI\_RX\_CFG\_RX\_EVT\_FRC\_ALT1 Name Register**

| 15            | 14              | 13             | 12             | 11         | 10             | 9                | 8               |
|---------------|-----------------|----------------|----------------|------------|----------------|------------------|-----------------|
| RESERVED_1    | ERROR_TAG_MATCH | DATA_TAG_MATCH | PING_TAG_MATCH | DATA_FRAME | FRAME_OVERFLOW | PING_FRAME       | ERR_FRAME       |
| R             | W               | W              | W              | W          | W              | W                | W               |
| 0h            | 0h              | 0h             | 0h             | 0h         | 0h             | 0h               | 0h              |
| 7             | 6               | 5              | 4              | 3          | 2              | 1                | 0               |
| BUF_UNDERFLOW | FRAME_DONE      | BUF_OVERFLOW   | EOF_ERR        | TYPE_ERR   | CRC_ERR        | FRAME_WD_TIMEOUT | PING_WD_TIMEOUT |
| W             | W               | W              | W              | W          | W              | W                | W               |
| 0h            | 0h              | 0h             | 0h             | 0h         | 0h             | 0h               | 0h              |

**Table 3-1443. FSI\_RX\_CFG\_RX\_EVT\_FRC\_ALT1 Register Field Descriptions**

| Bit | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                   |
|-----|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | RESERVED_1      | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                      |
| 14  | ERROR_TAG_MATCH | W    | 0h    | Error Tag Match Flag Force bit<br>This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Force the corresponding bit in the RX_EVT_STS Register.     |
| 13  | DATA_TAG_MATCH  | W    | 0h    | Data Tag Match Flag Force bit<br>This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Force the corresponding bit in the RX_EVT_STS Register.      |
| 12  | PING_TAG_MATCH  | W    | 0h    | Ping Tag Match Flag Force bit<br>This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Force the corresponding bit in the RX_EVT_STS Register.      |
| 11  | DATA_FRAME      | W    | 0h    | Data Frame Received Flag Force bit<br>This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Force the corresponding bit in the RX_EVT_STS Register. |

**Table 3-1443. FSI\_RX\_CFG\_RX\_EVT\_FRC\_ALT1 Register Field Descriptions (continued)**

| Bit | Field         | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                       |
|-----|---------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | FRAME_OVERRUN | W    | 0h    | Frame Overrun Flag Force bit<br>This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Force the corresponding bit in the RX_EVT_STS Register.           |
| 9   | PING_FRAME    | W    | 0h    | Ping Frame Received Flag Force bit<br>This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Force the corresponding bit in the RX_EVT_STS Register.     |
| 8   | ERR_FRAME     | W    | 0h    | Error Frame Received Flag Force bit<br>This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Force the corresponding bit in the RX_EVT_STS Register.    |
| 7   | BUF_UNDERRUN  | W    | 0h    | Receive Buffer Underrun Flag Force bit<br>This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Force the corresponding bit in the RX_EVT_STS Register. |
| 6   | FRAME_DONE    | W    | 0h    | Frame Done Flag Force bit<br>This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Force the corresponding bit in the RX_EVT_STS Register.              |
| 5   | BUF_OVERRUN   | W    | 0h    | Receive Buffer Overrun Flag Force bit<br>This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Force the corresponding bit in the RX_EVT_STS Register.  |
| 4   | EOF_ERR       | W    | 0h    | End-of-Frame Error Flag Force bit<br>This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Force the corresponding bit in the RX_EVT_STS Register.      |
| 3   | TYPE_ERR      | W    | 0h    | Frame Type Error Flag Force bit<br>This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Force the corresponding bit in the RX_EVT_STS Register.        |
| 2   | CRC_ERR       | W    | 0h    | CRC Error Flag Force bit<br>This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Force the corresponding bit in the RX_EVT_STS Register.               |
| 1   | FRAME_WD_TO   | W    | 0h    | Frame Watchdog Timeout Flag Force bit<br>This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Force the corresponding bit in the RX_EVT_STS Register.  |

**Table 3-1443. FSI\_RX\_CFG\_RX\_EVT\_FRC\_ALT1 Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|-----|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | PING_WD_TO | W    | 0h    | <p>Ping Watchdog Timeout Flag Force bit</p> <p>This bit will cause the corresponding bit in the RX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR.</p> <p>0h[W] = Writing a 0 to this bit will have no effect.</p> <p>1h[W] = Force the corresponding bit in the RX_EVT_STS Register.</p> |

### 3.9.2.10 FSI\_RX\_CFG\_RX\_BUF\_PTR\_LOAD Register

#### 1 FSI\_RX\_CFG\_RX\_BUF\_PTR\_LOAD Register (Offset = 1Ch) [reset = 0h]

Receive buffer pointer load register.

Return to [Summary Table](#)

**Table 3-1444. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 001Ch       |
| FSI_RX1       | 5029 101Ch       |
| FSI_RX2       | 502B 001Ch       |
| FSI_RX3       | 502B 101Ch       |

**Figure 3-461. FSI\_RX\_CFG\_RX\_BUF\_PTR\_LOAD Name Register**

|            |    |    |    |              |    |   |   |
|------------|----|----|----|--------------|----|---|---|
| 15         | 14 | 13 | 12 | 11           | 10 | 9 | 8 |
| RESERVED_1 |    |    |    |              |    |   |   |
| R          |    |    |    |              |    |   |   |
| 0h         |    |    |    |              |    |   |   |
| 7          | 6  | 5  | 4  | 3            | 2  | 1 | 0 |
| RESERVED_1 |    |    |    | BUF_PTR_LOAD |    |   |   |
| R          |    |    |    | R/W          |    |   |   |
| 0h         |    |    |    | 0h           |    |   |   |

**Table 3-1446. FSI\_RX\_CFG\_RX\_BUF\_PTR\_LOAD Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|--------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:4 | RESERVED_1   | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 3:0  | BUF_PTR_LOAD | R/W  | 0h    | Buffer Pointer Load.<br>This is the value to be loaded into the receive word pointer when written. This is to allow software to force the receiver to start storing the received data starting at a specific location in the buffer.<br>NOTE: The value of the CURR_BUF_PTR in the RX_BUF_PTR_STS will not get reflected immediately. This will take effect only when there is a valid receive operation with incoming clocks after [3 RXCLK + 3 SYCLK] cycles. |

### 3.9.2.11 FSI\_RX\_CFG\_RX\_BUF\_PTR\_STS Register

#### 1 FSI\_RX\_CFG\_RX\_BUF\_PTR\_STS Register (Offset = 1Eh) [reset = 0h]

Receive buffer pointer status register.

Return to [Summary Table](#)

**Table 3-1447. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 001Eh       |
| FSI_RX1       | 5029 101Eh       |
| FSI_RX2       | 502B 001Eh       |
| FSI_RX3       | 502B 101Eh       |

**Figure 3-462. FSI\_RX\_CFG\_RX\_BUF\_PTR\_STS Name Register**

| 15         | 14 | 13 | 12 | 11            | 10 | 9 | 8 |
|------------|----|----|----|---------------|----|---|---|
| RESERVED_2 |    |    |    | CURR_WORD_CNT |    |   |   |
| R          |    |    |    | R             |    |   |   |
| 0h         |    |    |    | 0h            |    |   |   |
| 7          | 6  | 5  | 4  | 3             | 2  | 1 | 0 |
| RESERVED_1 |    |    |    | CURR_BUF_PTR  |    |   |   |
| R          |    |    |    | R             |    |   |   |
| 0h         |    |    |    | 0h            |    |   |   |

**Table 3-1449. FSI\_RX\_CFG\_RX\_BUF\_PTR\_STS Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                      |
|-------|---------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | RESERVED_2    | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                         |
| 12:8  | CURR_WORD_CNT | R    | 0h    | Words Available in the Receive Buffer<br>This bitfield indicates the number of valid data words present in the receive buffer that have not been read by the application software. This bitfield is only valid when there is no active transfer.<br>Note: This value will not be valid if there has been a buffer overrun or underrun condition. |
| 7:4   | RESERVED_1    | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                         |
| 3:0   | CURR_BUF_PTR  | R    | 0h    | Current Buffer Pointer Index<br>This bitfield will show the current index of the buffer pointer. This value is only valid when there is no active transmission.                                                                                                                                                                                  |

### 3.9.2.12 FSI\_RX\_CFG\_RX\_FRAME\_WD\_CTRL Register

#### 1 FSI\_RX\_CFG\_RX\_FRAME\_WD\_CTRL Register (Offset = 20h) [reset = 0h]

Receive frame watchdog control register.

Return to [Summary Table](#)

**Table 3-1450. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 0020h       |
| FSI_RX1       | 5029 1020h       |
| FSI_RX2       | 502B 0020h       |
| FSI_RX3       | 502B 1020h       |

**Figure 3-463. FSI\_RX\_CFG\_RX\_FRAME\_WD\_CTRL Name Register**

|            |    |    |    |    |    |             |                  |
|------------|----|----|----|----|----|-------------|------------------|
| 15         | 14 | 13 | 12 | 11 | 10 | 9           | 8                |
| RESERVED_1 |    |    |    |    |    |             |                  |
| R          |    |    |    |    |    |             |                  |
| 0h         |    |    |    |    |    |             |                  |
| 7          | 6  | 5  | 4  | 3  | 2  | 1           | 0                |
| RESERVED_1 |    |    |    |    |    | FRAME_WD_EN | FRAME_WD_CNT_RST |
| R          |    |    |    |    |    | R/W         | R/W              |
| 0h         |    |    |    |    |    | 0h          | 0h               |

**Table 3-1452. FSI\_RX\_CFG\_RX\_FRAME\_WD\_CTRL Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:2 | RESERVED_1       | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 1    | FRAME_WD_EN      | R/W  | 0h    | Frame Watchdog Counter Enable bit<br>This bit will enable or disable the frame watchdog counter. The counter [RX_FRAME_WD_CNT] will begin counting from 0 when a valid start-of-frame pattern is received. When the reference value [RX_FRAME_WD_REF] is reached, it will generate a frame watchdog timeout event [RX_EVT_STS.FRAME_WD_TO] and the counter value will reset to 0 and continue counting on the next valid start-of-frame.<br>0h[R/W] = The frame watchdog counter is disabled and not running.<br>1h[R/W] = The frame watchdog counter logic is enabled and running. |
| 0    | FRAME_WD_CNT_RST | R/W  | 0h    | Frame Watchdog Counter Reset bit<br>This bit will reset the frame watchdog counter to 0. Writing a 1 to this bit will reset the frame watchdog counter to 0. The counter will stay in reset as long as this bit is set to 1. This bit needs to be cleared to 0 to use the counter<br>0h[R/W] = Clear the FRAME_WD_CNT_RST.<br>1h[W] = The frame watchdog counter will be reset to 0.                                                                                                                                                                                                |

### 3.9.2.13 FSI\_RX\_CFG\_RX\_FRAME\_WD\_REF Register

#### 1 FSI\_RX\_CFG\_RX\_FRAME\_WD\_REF Register (Offset = 24h) [reset = 0h]

Receive frame watchdog counter reference.

Return to [Summary Table](#)

**Table 3-1453. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 0024h       |
| FSI_RX1       | 5029 1024h       |
| FSI_RX2       | 502B 0024h       |
| FSI_RX3       | 502B 1024h       |

**Figure 3-464. FSI\_RX\_CFG\_RX\_FRAME\_WD\_REF Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FRAME_WD_REF |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FRAME_WD_REF |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FRAME_WD_REF |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FRAME_WD_REF |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 3-1455. FSI\_RX\_CFG\_RX\_FRAME\_WD\_REF Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                                                                                                                                                                         |
|------|--------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | FRAME_WD_REF | R/W  | 0h    | Frame Watchdog Counter Reference Value<br>This is the 32-bit reference value for the frame watchdog timeout counter. The counter will count up starting from 0 at a valid start-of-frame pattern and continue counting until this value is reached. |



### 3.9.2.14 FSI\_RX\_CFG\_RX\_FRAME\_WD\_CNT Register

#### 1 FSI\_RX\_CFG\_RX\_FRAME\_WD\_CNT Register (Offset = 28h) [reset = 0h]

Receive frame watchdog current count.

Return to [Summary Table](#)

**Table 3-1456. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 0028h       |
| FSI_RX1       | 5029 1028h       |
| FSI_RX2       | 502B 0028h       |
| FSI_RX3       | 502B 1028h       |

**Figure 3-465. FSI\_RX\_CFG\_RX\_FRAME\_WD\_CNT Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FRAME_WD_CNT |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FRAME_WD_CNT |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FRAME_WD_CNT |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FRAME_WD_CNT |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 3-1458. FSI\_RX\_CFG\_RX\_FRAME\_WD\_CNT Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                             |
|------|--------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | FRAME_WD_CNT | R    | 0h    | Frame Watchdog Counter Value<br>This is the 32-bit read-only register which shows the current value of the frame watchdog counter. This counter is reset to 0 in a variety of ways: A write to FRME_WD_CNT_RST, a match with FRAME_WD_REF, or the reception of a successful data frame. |

### 3.9.2.15 FSI\_RX\_CFG\_RX\_PING\_WD\_CTRL Register

#### 1 FSI\_RX\_CFG\_RX\_PING\_WD\_CTRL Register (Offset = 2Ch) [reset = 0h]

Receive ping watchdog control register.

Return to [Summary Table](#)

**Table 3-1459. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 002Ch       |
| FSI_RX1       | 5029 102Ch       |
| FSI_RX2       | 502B 002Ch       |
| FSI_RX3       | 502B 102Ch       |

**Figure 3-466. FSI\_RX\_CFG\_RX\_PING\_WD\_CTRL Name Register**

|            |    |    |    |    |    |            |             |
|------------|----|----|----|----|----|------------|-------------|
| 15         | 14 | 13 | 12 | 11 | 10 | 9          | 8           |
| RESERVED_1 |    |    |    |    |    |            |             |
| R          |    |    |    |    |    |            |             |
| 0h         |    |    |    |    |    |            |             |
| 7          | 6  | 5  | 4  | 3  | 2  | 1          | 0           |
| RESERVED_1 |    |    |    |    |    | PING_WD_EN | PING_WD_RST |
| R          |    |    |    |    |    | R/W        | R/W         |
| 0h         |    |    |    |    |    | 0h         | 0h          |

**Table 3-1461. FSI\_RX\_CFG\_RX\_PING\_WD\_CTRL Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------|-------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:2 | RESERVED_1  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 1    | PING_WD_EN  | R/W  | 0h    | <p>Ping Watchdog Counter Enable bit</p> <p>This bit will enable or disable the ping watchdog counter. The counter [RX_PING_WD_CNT] will begin counting from 0 when it is enabled. When the reference value [RX_PING_WD_REF] is reached, it will generate a ping watchdog timeout event [RX_EVT_STS.PING_WD_TO] and the counter value will reset to 0, and resume counting</p> <p>0h[R/W] = The ping watchdog counter is disabled and not running.</p> <p>1h[R/W] = The ping watchdog counter logic is enabled and running.</p> |
| 0    | PING_WD_RST | R/W  | 0h    | <p>Ping Watchdog Counter Reset bit</p> <p>This bit will reset the ping watchdog counter to 0. Writing a 1 to this bit will reset the ping watchdog counter to 0. The counter will stay in reset as long as this bit is set to 1. This bit needs to be cleared to 0 to use the counter</p> <p>0h[R/W] = Clear the PING_WD_RST.</p> <p>1h[W] = The ping watchdog counter will be reset to 0.</p>                                                                                                                                 |

### 3.9.2.16 FSI\_RX\_CFG\_RX\_PING\_TAG Register

#### 1 FSI\_RX\_CFG\_RX\_PING\_TAG Register (Offset = 2Eh) [reset = 0h]

Receive ping tag register.

Return to [Summary Table](#)

**Table 3-1462. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 002Eh       |
| FSI_RX1       | 5029 102Eh       |
| FSI_RX2       | 502B 002Eh       |
| FSI_RX3       | 502B 102Eh       |

**Figure 3-467. FSI\_RX\_CFG\_RX\_PING\_TAG Name Register**

|            |    |    |    |          |    |   |      |
|------------|----|----|----|----------|----|---|------|
| 15         | 14 | 13 | 12 | 11       | 10 | 9 | 8    |
| RESERVED_1 |    |    |    |          |    |   |      |
| R          |    |    |    |          |    |   |      |
| 0h         |    |    |    |          |    |   |      |
| 7          | 6  | 5  | 4  | 3        | 2  | 1 | 0    |
| RESERVED_1 |    |    |    | PING_TAG |    |   | ZERO |
| R          |    |    |    | R        |    |   | R    |
| 0h         |    |    |    | 0h       |    |   | 0h   |

**Table 3-1464. FSI\_RX\_CFG\_RX\_PING\_TAG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                           |
|------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:5 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                              |
| 4:1  | PING_TAG   | R    | 0h    | Received Ping Frame Tag<br>This field contains the 4-bit frame tag from the last successfully received ping frame. This is intentionally shifted into bits 4:1 so that the register can be used as a 32-bit address index based on the received tag.  |
| 0    | ZERO       | R    | 0h    | Zero bit<br>This bit will always read as 0. This is intentionally provided to create a 32-bit offset if required. Using the PING_TAG and ZERO bits of this register [bits 4:0], application software can directly index into an array of 32-bit data. |

### 3.9.2.17 FSI\_RX\_CFG\_RX\_PING\_WD\_REF Register

#### 1 FSI\_RX\_CFG\_RX\_PING\_WD\_REF Register (Offset = 30h) [reset = 0h]

Receive ping watchdog counter reference.

Return to [Summary Table](#)

**Table 3-1465. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 0030h       |
| FSI_RX1       | 5029 1030h       |
| FSI_RX2       | 502B 0030h       |
| FSI_RX3       | 502B 1030h       |

**Figure 3-468. FSI\_RX\_CFG\_RX\_PING\_WD\_REF Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PING_WD_REF |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PING_WD_REF |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PING_WD_REF |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PING_WD_REF |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 3-1467. FSI\_RX\_CFG\_RX\_PING\_WD\_REF Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                                                                     |
|------|-------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PING_WD_REF | R/W  | 0h    | Ping Watchdog Counter Reference Value<br>This is the 32-bit reference value for the ping watchdog timeout counter. The counter will count up starting from 0 and continue counting until this value is reached. |

### 3.9.2.18 FSI\_RX\_CFG\_RX\_PING\_WD\_CNT Register

#### 1 FSI\_RX\_CFG\_RX\_PING\_WD\_CNT Register (Offset = 34h) [reset = 0h]

Receive pingwatchdog current count.

Return to [Summary Table](#)

**Table 3-1468. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 0034h       |
| FSI_RX1       | 5029 1034h       |
| FSI_RX2       | 502B 0034h       |
| FSI_RX3       | 502B 1034h       |

**Figure 3-469. FSI\_RX\_CFG\_RX\_PING\_WD\_CNT Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PING_WD_CNT |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PING_WD_CNT |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PING_WD_CNT |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PING_WD_CNT |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 3-1470. FSI\_RX\_CFG\_RX\_PING\_WD\_CNT Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                                                                                                                           |
|------|-------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PING_WD_CNT | R    | 0h    | Ping Watchdog Counter Value<br>This is the 32-bit read-only register which shows the current value of the ping watchdog counter. This counter is reset to 0 in a variety of ways: A write to PING_WD_RST, a match with PING_WD_REF, or the reception of a ping frame. |

### 3.9.2.19 FSI\_RX\_CFG\_RX\_INT1\_CTRL\_ALT1 Register

#### 1 FSI\_RX\_CFG\_RX\_INT1\_CTRL\_ALT1 Register (Offset = 38h) [reset = 0h]

Receive interrupt control register for RX\_INT1.

Return to [Summary Table](#)

**Table 3-1471. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 0038h       |
| FSI_RX1       | 5029 1038h       |
| FSI_RX2       | 502B 0038h       |
| FSI_RX3       | 502B 1038h       |

**Figure 3-470. FSI\_RX\_CFG\_RX\_INT1\_CTRL\_ALT1 Name Register**

| 15               | 14                      | 13                     | 12                     | 11                 | 10                    | 9                   | 8                   |
|------------------|-------------------------|------------------------|------------------------|--------------------|-----------------------|---------------------|---------------------|
| RESERVED_1       | INT1_EN_ERROR_TAG_MATCH | INT1_EN_DATA_TAG_MATCH | INT1_EN_PING_TAG_MATCH | INT1_EN_DATA_FRAME | INT1_EN_FRAME_OVERRUN | INT1_EN_PING_FRAME  | INT1_EN_ERROR_FRAME |
| R                | R/W                     | R/W                    | R/W                    | R/W                | R/W                   | R/W                 | R/W                 |
| 0h               | 0h                      | 0h                     | 0h                     | 0h                 | 0h                    | 0h                  | 0h                  |
| 7                | 6                       | 5                      | 4                      | 3                  | 2                     | 1                   | 0                   |
| INT1_EN_UNDERRUN | INT1_EN_FRAME_DONE      | INT1_EN_OVERRUN        | INT1_EN_EOF_ERR        | INT1_EN_TYPE_ERR   | INT1_EN_CRC_ERR       | INT1_EN_FRAME_WD_TO | INT1_EN_PING_WD_TO  |
| R/W              | R/W                     | R/W                    | R/W                    | R/W                | R/W                   | R/W                 | R/W                 |
| 0h               | 0h                      | 0h                     | 0h                     | 0h                 | 0h                    | 0h                  | 0h                  |

**Table 3-1473. FSI\_RX\_CFG\_RX\_INT1\_CTRL\_ALT1 Register Field Descriptions**

| Bit | Field                   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-----|-------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | RESERVED_1              | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 14  | INT1_EN_ERROR_TAG_MATCH | R/W  | 0h    | Enable Error Frame Received with Tag Match Interrupt to INT1 bit<br>This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT1.<br>1h[R/W] = An error frame received with matching tag will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register |
| 13  | INT1_EN_DATA_TAG_MATCH  | R/W  | 0h    | Enable Data Frame Received with Tag Match Interrupt to INT1 bit<br>This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT1.<br>1h[R/W] = A data frame received with matching tag will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register    |
| 12  | INT1_EN_PING_TAG_MATCH  | R/W  | 0h    | Enable Ping Frame Received with Tag Match Interrupt to INT1 bit<br>This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT1.<br>1h[R/W] = A ping frame received with matching tag will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register    |

**Table 3-1473. FSI\_RX\_CFG\_RX\_INT1\_CTRL\_ALT1 Register Field Descriptions (continued)**

| Bit | Field                  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                     |
|-----|------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11  | INT1_EN_DATA_FRAME     | R/W  | 0h    | Enable Data Frame Received Interrupt to INT1 bit<br>This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT1.<br>1h[R/W] = A data frame received event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register       |
| 10  | INT1_EN_FRAME_OVERFLOW | R/W  | 0h    | Enable Frame Overflow Interrupt to INT1 bit<br>This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT1.<br>1h[R/W] = A frame overflow event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register                 |
| 9   | INT1_EN_PING_FRAME     | R/W  | 0h    | Enable Ping Frame Received Interrupt to INT1 bit<br>This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT1.<br>1h[R/W] = A ping frame received event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register       |
| 8   | INT1_EN_ERR_FRAME      | R/W  | 0h    | Enable ERROR Frame Received Interrupt to INT1 bit<br>This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT1.<br>1h[R/W] = A error frame received event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register     |
| 7   | INT1_EN_UNDERRUN       | R/W  | 0h    | Enable Buffer Underrun Interrupt to INT1 bit<br>This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT1.<br>1h[R/W] = A buffer underrun event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register               |
| 6   | INT1_EN_FRAME_DONE     | R/W  | 0h    | Enable Frame Done Interrupt to INT1 bit<br>This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT1.<br>1h[R/W] = A frame done event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register                         |
| 5   | INT1_EN_OVERRUN        | R/W  | 0h    | Enable Receive Buffer Overrun Interrupt to INT1 bit<br>This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT1.<br>1h[R/W] = A receive buffer overrun event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register |
| 4   | INT1_EN_EOF_ERR        | R/W  | 0h    | Enable End-of-Frame Error Interrupt to INT1 bit<br>This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT1.<br>1h[R/W] = An end-of-frame error event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register        |

**Table 3-1473. FSI\_RX\_CFG\_RX\_INT1\_CTRL\_ALT1 Register Field Descriptions (continued)**

| Bit | Field                   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                     |
|-----|-------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3   | INT1_EN_TYPE_ERR        | R/W  | 0h    | Enable Frame Type Error Interrupt to INT1 bit<br>This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT1.<br>1h[R/W] = A frame type error event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register             |
| 2   | INT1_EN_CRC_ERR         | R/W  | 0h    | Enable CRC Error Interrupt to INT1 bit<br>This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT1.<br>1h[R/W] = A CRC error will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register                                 |
| 1   | INT1_EN_FRAME_WD_T<br>O | R/W  | 0h    | Enable Frame Watchdog Timeout Interrupt to INT1 bit<br>This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT1.<br>1h[R/W] = A frame watchdog timeout event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register |
| 0   | INT1_EN_PING_WD_TO      | R/W  | 0h    | Enable Ping Watchdog Timeout Interrupt to INT1 bit<br>This is an enable register which decides whether an interrupt [RX_INT1] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT1.<br>1h[R/W] = A ping watchdog timeout event will trigger an interrupt on RX_INT1. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register   |



### 3.9.2.20 FSI\_RX\_CFG\_RX\_INT2\_CTRL\_ALT1 Register

#### 1 FSI\_RX\_CFG\_RX\_INT2\_CTRL\_ALT1 Register (Offset = 3Ah) [reset = 0h]

Receive interrupt control register for RX\_INT2.

Return to [Summary Table](#)

**Table 3-1474. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 003Ah       |
| FSI_RX1       | 5029 103Ah       |
| FSI_RX2       | 502B 003Ah       |
| FSI_RX3       | 502B 103Ah       |

**Figure 3-471. FSI\_RX\_CFG\_RX\_INT2\_CTRL\_ALT1 Name Register**

| 15                   | 14                              | 13                         | 12                         | 11                     | 10                        | 9                       | 8                      |
|----------------------|---------------------------------|----------------------------|----------------------------|------------------------|---------------------------|-------------------------|------------------------|
| RESERVED_1           | INT2_EN_ERR<br>OR_TAG_MAT<br>CH | INT2_EN_DATA<br>_TAG_MATCH | INT2_EN_PING<br>_TAG_MATCH | INT2_EN_DATA<br>_FRAME | INT2_EN_FRA<br>ME_OVERRUN | INT2_EN_PING<br>_FRAME  | INT2_EN_ERR<br>_FRAME  |
| R                    | R/W                             | R/W                        | R/W                        | R/W                    | R/W                       | R/W                     | R/W                    |
| 0h                   | 0h                              | 0h                         | 0h                         | 0h                     | 0h                        | 0h                      | 0h                     |
| 7                    | 6                               | 5                          | 4                          | 3                      | 2                         | 1                       | 0                      |
| INT2_EN_UND<br>ERRUN | INT2_EN_FRA<br>ME_DONE          | INT2_EN_OVE<br>RRUN        | INT2_EN_EOF<br>_ERR        | INT2_EN_TYP<br>E_ERR   | INT2_EN_CRC<br>_ERR       | INT2_EN_FRA<br>ME_WD_TO | INT2_EN_PING<br>_WD_TO |
| R/W                  | R/W                             | R/W                        | R/W                        | R/W                    | R/W                       | R/W                     | R/W                    |
| 0h                   | 0h                              | 0h                         | 0h                         | 0h                     | 0h                        | 0h                      | 0h                     |

**Table 3-1476. FSI\_RX\_CFG\_RX\_INT2\_CTRL\_ALT1 Register Field Descriptions**

| Bit | Field                   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-----|-------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | RESERVED_1              | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 14  | INT2_EN_ERROR_TAG_MATCH | R/W  | 0h    | Enable Error Frame Received with Tag Match Interrupt to INT2 bit<br>This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT2.<br>1h[R/W] = An error frame received with matching tag will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register |
| 13  | INT2_EN_DATA_TAG_MATCH  | R/W  | 0h    | Enable Data Frame Received with Tag Match Interrupt to INT2 bit<br>This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT2.<br>1h[R/W] = A data frame received with matching tag will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register    |
| 12  | INT2_EN_PING_TAG_MATCH  | R/W  | 0h    | Enable Ping Frame Received with Tag Match Interrupt to INT2 bit<br>This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT2.<br>1h[R/W] = A ping frame received with matching tag will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register    |

**Table 3-1476. FSI\_RX\_CFG\_RX\_INT2\_CTRL\_ALT1 Register Field Descriptions (continued)**

| Bit | Field                  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                 |
|-----|------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11  | INT2_EN_DATA_FRAME     | R/W  | 0h    | Enable Data Frame Received Interrupt to INT2 bit<br>This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT2.<br>1h[R/W] = A data frame received event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register   |
| 10  | INT2_EN_FRAME_OVERFLOW | R/W  | 0h    | Enable Frame Overflow Interrupt to INT2 bit<br>This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT2.<br>1h[R/W] = A frame overflow event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register             |
| 9   | INT2_EN_PING_FRAME     | R/W  | 0h    | Enable Ping Frame Received Interrupt to INT2 bit<br>This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT2.<br>1h[R/W] = A ping frame received event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register   |
| 8   | INT2_EN_ERR_FRAME      | R/W  | 0h    | Enable Error Frame Received Interrupt to INT2 bit<br>This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT2.<br>1h[R/W] = A error frame received event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register |
| 7   | INT2_EN_UNDERRUN       | R/W  | 0h    | Enable Buffer Underrun Interrupt to INT2 bit<br>This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT2.<br>1h[R/W] = A buffer underrun event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register           |
| 6   | INT2_EN_FRAME_DONE     | R/W  | 0h    | Enable Frame Done Interrupt to INT2 bit<br>This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT2.<br>1h[R/W] = A frame done event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register                     |
| 5   | INT2_EN_OVERRUN        | R/W  | 0h    | Enable Buffer Overrun Interrupt to INT2 bit<br>This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT2.<br>1h[R/W] = A buffer overrun event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register             |
| 4   | INT2_EN_EOF_ERR        | R/W  | 0h    | Enable End-of-Frame Error Interrupt to INT2 bit<br>This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT2.<br>1h[R/W] = An end-of-frame error event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register    |

**Table 3-1476. FSI\_RX\_CFG\_RX\_INT2\_CTRL\_ALT1 Register Field Descriptions (continued)**

| Bit | Field                   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                     |
|-----|-------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3   | INT2_EN_TYPE_ERR        | R/W  | 0h    | Enable Frame Type Error Interrupt to INT2 bit<br>This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT2.<br>1h[R/W] = A frame type error event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register             |
| 2   | INT2_EN_CRC_ERR         | R/W  | 0h    | Enable CRC Error Interrupt to INT2 bit<br>This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT2.<br>1h[R/W] = A CRC error will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register                                 |
| 1   | INT2_EN_FRAME_WD_T<br>O | R/W  | 0h    | Enable Frame Watchdog Timeout Interrupt to INT2 bit<br>This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT2.<br>1h[R/W] = A frame watchdog timeout event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register |
| 0   | INT2_EN_PING_WD_TO      | R/W  | 0h    | Enable Ping Watchdog Timeout Interrupt to INT2 bit<br>This is an enable register which decides whether an interrupt [RX_INT2] will be generated on the enabled event.<br>0h[R/W] = This event will not trigger an interrupt on RX_INT2.<br>1h[R/W] = A ping watchdog timeout event will trigger an interrupt on RX_INT2. The event itself will be latched in the corresponding bit in the RX_EVT_STS Register   |

### 3.9.2.21 FSI\_RX\_CFG\_RX\_LOCK\_CTRL Register

#### 1 FSI\_RX\_CFG\_RX\_LOCK\_CTRL Register (Offset = 3Ch) [reset = 0h]

Receive lock control register.

Return to [Summary Table](#)

**Table 3-1477. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 003Ch       |
| FSI_RX1       | 5029 103Ch       |
| FSI_RX2       | 502B 003Ch       |
| FSI_RX3       | 502B 103Ch       |

**Figure 3-472. FSI\_RX\_CFG\_RX\_LOCK\_CTRL Name Register**

|            |    |    |    |    |    |   |      |
|------------|----|----|----|----|----|---|------|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8    |
| KEY        |    |    |    |    |    |   |      |
| W          |    |    |    |    |    |   |      |
| 0h         |    |    |    |    |    |   |      |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0    |
| RESERVED_1 |    |    |    |    |    |   | LOCK |
| R          |    |    |    |    |    |   | R/W  |
| 0h         |    |    |    |    |    |   | 0h   |

**Table 3-1479. FSI\_RX\_CFG\_RX\_LOCK\_CTRL Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | KEY        | W    | 0h    | Write Key.<br>In order to write to this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after Writing, so it must be written again for every change to this register.                                                                                                                                                                                                                                                                                                                                                        |
| 7:1  | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 0    | LOCK       | R/W  | 0h    | Control Register Lock Enable bit<br>This bit locks the contents of all the receive control registers that support a lock protection. Once locked, further writes will not take effect until SYSRS unlocks the register. Once set, further writes even to this bit will be ignored.<br>0h[R/W] = Receive control registers can be modified and are not locked.<br>1h[R/W] = Receive control registers are locked and cannot be modified until this bit is cleared by SYSRS. Any further writes to this bit are ignored.<br>Note: The KEY field must contain 0xA5 for any write to this bit to take effect. |

### 3.9.2.22 FSI\_RX\_CFG\_RX\_ECC\_DATA Register

#### 1 FSI\_RX\_CFG\_RX\_ECC\_DATA Register (Offset = 40h) [reset = 0h]

Receive ECC data register.

Return to [Summary Table](#)

**Table 3-1480. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 0040h       |
| FSI_RX1       | 5029 1040h       |
| FSI_RX2       | 502B 0040h       |
| FSI_RX3       | 502B 1040h       |

**Figure 3-473. FSI\_RX\_CFG\_RX\_ECC\_DATA Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DATA_HIGH |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DATA_HIGH |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DATA_LOW  |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DATA_LOW  |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 3-1482. FSI\_RX\_CFG\_RX\_ECC\_DATA Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                |
|-------|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | DATA_HIGH | R/W  | 0h    | Upper 16 bits of ECC Data<br>Writing to this bitfield will cause the ECC logic to compute the ECC[SEC-DED] the entire 32-bit register and update TX_ECC_VAL register with the results. Software should write to these 16 bits of the register in a 32-bit write when needing to compute ECC for 32-bits for the full TX_ECC_DATA register. |
| 15:0  | DATA_LOW  | R/W  | 0h    | Lower 16 bits of ECC Data<br>Writing to this bitfield will cause the ECC logic to compute the ECC[SEC-DED] for these 16 bits and update the TX_ECC_VAL register with the results. Software should write to these register bits as a 16-bit write when needing to compute ECC for 16-bits.                                                  |

### 3.9.2.23 FSI\_RX\_CFG\_RX\_ECC\_VAL Register

#### 1 FSI\_RX\_CFG\_RX\_ECC\_VAL Register (Offset = 44h) [reset = 0h]

Receive ECC value register.

Return to [Summary Table](#)

**Table 3-1483. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 0044h       |
| FSI_RX1       | 5029 1044h       |
| FSI_RX2       | 502B 0044h       |
| FSI_RX3       | 502B 1044h       |

**Figure 3-474. FSI\_RX\_CFG\_RX\_ECC\_VAL Name Register**

|            |         |    |    |    |    |   |   |
|------------|---------|----|----|----|----|---|---|
| 15         | 14      | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED_1 |         |    |    |    |    |   |   |
| R          |         |    |    |    |    |   |   |
| 0h         |         |    |    |    |    |   |   |
| 7          | 6       | 5  | 4  | 3  | 2  | 1 | 0 |
| RESERVED_1 | ECC_VAL |    |    |    |    |   |   |
| R          | R/W     |    |    |    |    |   |   |
| 0h         | 0h      |    |    |    |    |   |   |

**Table 3-1485. FSI\_RX\_CFG\_RX\_ECC\_VAL Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                           |
|------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:7 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                              |
| 6:0  | ECC_VAL    | R/W  | 0h    | ECC Value for SEC-DED check<br>This field contains the ECC value to be used for SEC-DED either for 16-bit or 32-bit data in the RX_ECC_DATA register. |

### 3.9.2.24 FSI\_RX\_CFG\_RX\_ECC\_SEC\_DATA Register

#### 1 FSI\_RX\_CFG\_RX\_ECC\_SEC\_DATA Register (Offset = 48h) [reset = 0h]

Receive ECC corrected data register.

Return to [Summary Table](#)

**Table 3-1486. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 0048h       |
| FSI_RX1       | 5029 1048h       |
| FSI_RX2       | 502B 0048h       |
| FSI_RX3       | 502B 1048h       |

**Figure 3-475. FSI\_RX\_CFG\_RX\_ECC\_SEC\_DATA Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SEC_DATA |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SEC_DATA |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SEC_DATA |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SEC_DATA |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 3-1488. FSI\_RX\_CFG\_RX\_ECC\_SEC\_DATA Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                           |
|------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | SEC_DATA | R    | 0h    | ECC Single Error Corrected Data<br>The ECC corrected data will be available in this register. This value is valid only when there are no bit errors, or a single bit error was detected. Otherwise, the contents of this register are invalid and should not be used. |

### 3.9.2.25 FSI\_RX\_CFG\_RX\_ECC\_LOG Register

#### 1 FSI\_RX\_CFG\_RX\_ECC\_LOG Register (Offset = 4Ch) [reset = 3h]

Receive ECC log and status register.

Return to [Summary Table](#)

**Table 3-1489. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 004Ch       |
| FSI_RX1       | 5029 104Ch       |
| FSI_RX2       | 502B 004Ch       |
| FSI_RX3       | 502B 104Ch       |

**Figure 3-476. FSI\_RX\_CFG\_RX\_ECC\_LOG Name Register**

|            |    |    |    |    |    |     |     |
|------------|----|----|----|----|----|-----|-----|
| 15         | 14 | 13 | 12 | 11 | 10 | 9   | 8   |
| RESERVED_1 |    |    |    |    |    |     |     |
| R          |    |    |    |    |    |     |     |
| 0h         |    |    |    |    |    |     |     |
| 7          | 6  | 5  | 4  | 3  | 2  | 1   | 0   |
| RESERVED_1 |    |    |    |    |    | MBE | SBE |
| R          |    |    |    |    |    | R   | R   |
| 0h         |    |    |    |    |    | 1h  | 1h  |

**Table 3-1491. FSI\_RX\_CFG\_RX\_ECC\_LOG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:2 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 1    | MBE        | R    | 1h    | Multiple Bit Errors Detected<br>This bit indicates the occurrence of multiple bit errors. The data is corrupted and cannot be corrected. If this bit is set, the data present in RX_ECC_SEC_DATA is invalid and should not be used.<br>0h[R] Multiple Bit Errors were not detected. Check the SBE bit for single bit errors.<br>1h[R] Multiple Bit Errors were detected. The data is not able to be corrected. The value present in RX_ECC_SEC_DATA is invalid and should not be used. |
| 0    | SBE        | R    | 1h    | Single Bit Error Detected<br>This bit indicates the occurrence of a single bit error in the data. The data is autocorrected and placed into the RX_ECC_SEC_DATA register. This bit is valid only if MBE is 0.<br>0h[R] No bit errors were detected. The value in RX_ECC_SEC_DATA is correct.<br>1h[R] A single bit error was detected and corrected. The corrected data is present in RX_ECC_SEC_DATA.                                                                                 |



### 3.9.2.26 FSI\_RX\_CFG\_RX\_FRAME\_TAG\_CMP Register

#### 1 FSI\_RX\_CFG\_RX\_FRAME\_TAG\_CMP Register (Offset = 50h) [reset = 0h]

Receive frame tag compare register.

Return to [Summary Table](#)

**Table 3-1492. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 0050h       |
| FSI_RX1       | 5029 1050h       |
| FSI_RX2       | 502B 0050h       |
| FSI_RX3       | 502B 1050h       |

**Figure 3-477. FSI\_RX\_CFG\_RX\_FRAME\_TAG\_CMP Name Register**

| 15         | 14 | 13 | 12 | 11      | 10 | 9            | 8      |
|------------|----|----|----|---------|----|--------------|--------|
| RESERVED_1 |    |    |    |         |    | BROADCAST_EN | CMP_EN |
| R          |    |    |    |         |    | R/W          | R/W    |
| 0h         |    |    |    |         |    | 0h           | 0h     |
| 7          | 6  | 5  | 4  | 3       | 2  | 1            | 0      |
| TAG_MASK   |    |    |    | TAG_REF |    |              |        |
| R/W        |    |    |    | R/W     |    |              |        |
| 0h         |    |    |    | 0h      |    |              |        |

**Table 3-1494. FSI\_RX\_CFG\_RX\_FRAME\_TAG\_CMP Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|--------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1   | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 9     | BROADCAST_EN | R/W  | 0h    | Broadcast Enable bit<br>This will enable the reception of a ping frame broadcast. When this bit is set, bit 3 of the received tag will be treated as a broadcast notification. If bit 3 of the received tag is set to 1, a ping tag match event will be triggered regardless of the. A match caused by the comparison of TAG_MASK and TAG_REF will still be considered a match and the frame tag match event will be triggered as normal. This bit only takes effect only if CMP_EN is set to 1.<br>0h[R/W] Broadcast frame match disabled.<br>1h[R/W] Broadcast frame match enabled. |
| 8     | CMP_EN       | R/W  | 0h    | Frame Tag Compare Enable bit<br>Set this bit to enable the comparison of an incoming frame tag and the value stored in the frame tag reference. A match caused by the comparison of TAG_MASK, TAG_REF, and the incoming frame tag will trigger the appropriate frame tag match event.<br>0h[R/W] Frame tag comparison is disabled.<br>1h[R/W] Frame tag comparison is enabled.                                                                                                                                                                                                        |
| 7:4   | TAG_MASK     | R/W  | 0h    | Frame Tag Mask<br>Any bit position in this register set to 0 will be used in the comparison of the incoming frame tag and the value stored in TAG_REF. A bit position set to 1 will be ignored in the tag comparison. This mask value is used only for non-ping frames.                                                                                                                                                                                                                                                                                                               |
| 3:0   | TAG_REF      | R/W  | 0h    | Frame Tag Reference<br>The reference tag to check against when comparing the TAG_MASK and the incoming frame tag. This reference value is used only for non-ping frames.                                                                                                                                                                                                                                                                                                                                                                                                              |

### 3.9.2.27 FSI\_RX\_CFG\_RX\_PING\_TAG\_CMP Register

#### 1 FSI\_RX\_CFG\_RX\_PING\_TAG\_CMP Register (Offset = 52h) [reset = 0h]

Receive ping tag compare register.

Return to [Summary Table](#)

**Table 3-1495. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 0052h       |
| FSI_RX1       | 5029 1052h       |
| FSI_RX2       | 502B 0052h       |
| FSI_RX3       | 502B 1052h       |

**Figure 3-478. FSI\_RX\_CFG\_RX\_PING\_TAG\_CMP Name Register**

| 15         | 14 | 13 | 12 | 11      | 10 | 9            | 8      |
|------------|----|----|----|---------|----|--------------|--------|
| RESERVED_1 |    |    |    |         |    | BROADCAST_EN | CMP_EN |
| R          |    |    |    |         |    | R/W          | R/W    |
| 0h         |    |    |    |         |    | 0h           | 0h     |
| 7          | 6  | 5  | 4  | 3       | 2  | 1            | 0      |
| TAG_MASK   |    |    |    | TAG_REF |    |              |        |
| R/W        |    |    |    | R/W     |    |              |        |
| 0h         |    |    |    | 0h      |    |              |        |

**Table 3-1497. FSI\_RX\_CFG\_RX\_PING\_TAG\_CMP Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1   | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 9     | BROADCAST_EN | R/W  | 0h    | Broadcast Enable bit<br>This will enable the reception of a ping frame broadcast. When this bit is set, bit 3 of the received tag will be treated as a broadcast notification. If bit 3 of the received tag is set to 1, a ping tag match event will be triggered regardless of the. A match caused by the comparison of TAG_MASK and TAG_REF will still be considered a match and the ping tag match event will be triggered as normal<br>This bit only takes effect only if CMP_EN is set to 1.<br>0h[R/W] Broadcast frame match disabled.<br>1h[R/W] Broadcast frame match enabled. |
| 8     | CMP_EN       | R/W  | 0h    | Ping Tag Compare Enable bit<br>Set this bit to enable the comparison of an incoming ping tag and the value stored in the ping tag reference. A match caused by the comparison of TAG_MASK, TAG_REF, and the incoming ping tag will trigger a ping frame tag match event.<br>0h[R/W] Ping tag comparison is disabled.<br>1h[R/W] Ping tag comparison is enabled.                                                                                                                                                                                                                        |
| 7:4   | TAG_MASK     | R/W  | 0h    | Ping Tag Mask<br>Any bit position in this register set to 0 will be used in the comparison of the incoming ping frame tag and the value stored in TAG_REF. A bit position set to 1 will be ignored in the tag comparison.<br>This mask value is used only for ping frames.                                                                                                                                                                                                                                                                                                             |
| 3:0   | TAG_REF      | R/W  | 0h    | Ping Tag Reference<br>The reference tag to check against when comparing the TAG_MASK and the incoming ping tag.<br>This reference value is used only for ping frames.                                                                                                                                                                                                                                                                                                                                                                                                                  |

### 3.9.2.28 FSI\_RX\_CFG\_RX\_TRIG\_CTRL\_0 Register

#### 1 FSI\_RX\_CFG\_RX\_TRIG\_CTRL\_0 Register (Offset = 58h) [reset = 0h]

Receive Trigger Control register 0

Return to [Summary Table](#)

**Table 3-1498. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 0058h       |
| FSI_RX1       | 5029 1058h       |
| FSI_RX2       | 502B 0058h       |
| FSI_RX3       | 502B 1058h       |

**Figure 3-479. FSI\_RX\_CFG\_RX\_TRIG\_CTRL\_0 Name Register**

|             |    |    |          |    |    |         |    |
|-------------|----|----|----------|----|----|---------|----|
| 31          | 30 | 29 | 28       | 27 | 26 | 25      | 24 |
| RX_TRIG_DLY |    |    |          |    |    |         |    |
| R/W         |    |    |          |    |    |         |    |
| 0h          |    |    |          |    |    |         |    |
| 23          | 22 | 21 | 20       | 19 | 18 | 17      | 16 |
| RX_TRIG_DLY |    |    |          |    |    |         |    |
| R/W         |    |    |          |    |    |         |    |
| 0h          |    |    |          |    |    |         |    |
| 15          | 14 | 13 | 12       | 11 | 10 | 9       | 8  |
| RX_TRIG_DLY |    |    |          |    |    |         |    |
| R/W         |    |    |          |    |    |         |    |
| 0h          |    |    |          |    |    |         |    |
| 7           | 6  | 5  | 4        | 3  | 2  | 1       | 0  |
| RESERVED_1  |    |    | TRIG_SEL |    |    | TRIG_EN |    |
| R           |    |    | R/W      |    |    | R/W     |    |
| 0h          |    |    | 0h       |    |    | 0h      |    |

**Table 3-1500. FSI\_RX\_CFG\_RX\_TRIG\_CTRL\_0 Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                                                                                                                             |
|------|-------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RX_TRIG_DLY | R/W  | 0h    | This is the 24 bit count of the trigger delay in SYSCLK cycles. If enabled, the Trigger-1 output of the trigger module will generate a 3 SYSCLK wide trigger pulse after the selected input trigger source sees a rising edge with a delay defined by this 24-bt value. |
| 7:5  | RESERVED_1  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                |
| 4:1  | TRIG_SEL    | R/W  | 0h    | This is the mux Select Value which selects which of the inputs will be used as the trigger source.                                                                                                                                                                      |
| 0    | TRIG_EN     | R/W  | 0h    | This is the enable for the RX output trigger generation. The output triggers will be generated only if this bit is set to 1. If this bit is 0, then no trigger will be generated by this module.                                                                        |

### 3.9.2.29 FSI\_RX\_CFG\_RX\_TRIG\_WIDTH\_0 Register

#### 1 FSI\_RX\_CFG\_RX\_TRIG\_WIDTH\_0 Register (Offset = 5Ch) [reset = 0h]

Receive Trigger Width register 0

Return to [Summary Table](#)

**Table 3-1501. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 005Ch       |
| FSI_RX1       | 5029 105Ch       |
| FSI_RX2       | 502B 005Ch       |
| FSI_RX3       | 502B 105Ch       |

**Figure 3-480. FSI\_RX\_CFG\_RX\_TRIG\_WIDTH\_0 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_1    |    |    |    |    |    |    |    |
| R             |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_1    |    |    |    |    |    |    |    |
| R             |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RX_TRIG_WIDTH |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RX_TRIG_WIDTH |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 3-1503. FSI\_RX\_CFG\_RX\_TRIG\_WIDTH\_0 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                      |
|-------|---------------|------|-------|--------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED_1    | R    | 0h    | Reserved                                                                                         |
| 15:0  | RX_TRIG_WIDTH | R/W  | 0h    | This register decides the width[in SYSCLK cycles] of wide pulse output of the RX trigger module. |

### 3.9.2.30 FSI\_RX\_CFG\_RX\_DLYLINE\_CTRL Register

#### 1 FSI\_RX\_CFG\_RX\_DLYLINE\_CTRL Register (Offset = 60h) [reset = 0h]

Receive delay line control register.

Return to [Summary Table](#)

**Table 3-1504. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 0060h       |
| FSI_RX1       | 5029 1060h       |
| FSI_RX2       | 502B 0060h       |
| FSI_RX3       | 502B 1060h       |

**Figure 3-481. FSI\_RX\_CFG\_RX\_DLYLINE\_CTRL Name Register**

| 15         | 14       | 13 | 12        | 11 | 10 | 9        | 8 |
|------------|----------|----|-----------|----|----|----------|---|
| RESERVED_1 | RXD1_DLY |    |           |    |    | RXD0_DLY |   |
| R          | R/W      |    |           |    |    | R/W      |   |
| 0h         | 0h       |    |           |    |    | 0h       |   |
| 7          | 6        | 5  | 4         | 3  | 2  | 1        | 0 |
| RXD0_DLY   |          |    | RXCLK_DLY |    |    |          |   |
| R/W        |          |    | R/W       |    |    |          |   |
| 0h         |          |    | 0h        |    |    |          |   |

**Table 3-1506. FSI\_RX\_CFG\_RX\_DLYLINE\_CTRL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 14:10 | RXD1_DLY   | R/W  | 0h    | Delay Line Tap Select for RXD1<br>This bitfield selects the number of delay elements inserted into the RXD1 path from the pin boundary to the receiver core.<br>0h[R/W] Zero delay elements are included in the RXD1 path. RXD1 is taken directly from the pin.<br>1h[R/W] One delay element is included in the RXD1 path.<br>2h[R/W] Two delay elements are included in the RXD1 path.<br>...<br>1Fh [R/W] 31 delay elements are included in the RXD1 path, the maximum.        |
| 9:5   | RXD0_DLY   | R/W  | 0h    | Delay Line Tap Select for RXD0<br>This bitfield selects the number of delay elements inserted into the RXD0 path from the pin boundary to the receiver core.<br>0h[R/W] Zero delay elements are included in the RXD0 path. RXD0 is taken directly from the pin.<br>1h[R/W] One delay element is included in the RXD0 path.<br>2h[R/W] Two delay elements are included in the RXD0 path.<br>...<br>1Fh [R/W] 31 delay elements are included in the RXD0 path, the maximum.        |
| 4:0   | RXCLK_DLY  | R/W  | 0h    | Delay Line Tap Select for RXCLK<br>This bitfield selects the number of delay elements inserted into the RXCLK path from the pin boundary to the receiver core.<br>0h[R/W] Zero delay elements are included in the RXCLK path. RXCLK is taken directly from the pin.<br>1h[R/W] One delay element is included in the RXCLK path.<br>2h[R/W] Two delay elements are included in the RXCLK path.<br>...<br>1Fh [R/W] 31 delay elements are included in the RXCLK path, the maximum. |

### 3.9.2.31 FSI\_RX\_CFG\_RX\_TRIG\_CTRL\_1 Register

#### 1 FSI\_RX\_CFG\_RX\_TRIG\_CTRL\_1 Register (Offset = 64h) [reset = 0h]

Receive Trigger Control register 1

Return to [Summary Table](#)

**Table 3-1507. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 0064h       |
| FSI_RX1       | 5029 1064h       |
| FSI_RX2       | 502B 0064h       |
| FSI_RX3       | 502B 1064h       |

**Figure 3-482. FSI\_RX\_CFG\_RX\_TRIG\_CTRL\_1 Name Register**

|             |    |    |          |    |    |         |    |
|-------------|----|----|----------|----|----|---------|----|
| 31          | 30 | 29 | 28       | 27 | 26 | 25      | 24 |
| RX_TRIG_DLY |    |    |          |    |    |         |    |
| R/W         |    |    |          |    |    |         |    |
| 0h          |    |    |          |    |    |         |    |
| 23          | 22 | 21 | 20       | 19 | 18 | 17      | 16 |
| RX_TRIG_DLY |    |    |          |    |    |         |    |
| R/W         |    |    |          |    |    |         |    |
| 0h          |    |    |          |    |    |         |    |
| 15          | 14 | 13 | 12       | 11 | 10 | 9       | 8  |
| RX_TRIG_DLY |    |    |          |    |    |         |    |
| R/W         |    |    |          |    |    |         |    |
| 0h          |    |    |          |    |    |         |    |
| 7           | 6  | 5  | 4        | 3  | 2  | 1       | 0  |
| RESERVED_1  |    |    | TRIG_SEL |    |    | TRIG_EN |    |
| R           |    |    | R/W      |    |    | R/W     |    |
| 0h          |    |    | 0h       |    |    | 0h      |    |

**Table 3-1509. FSI\_RX\_CFG\_RX\_TRIG\_CTRL\_1 Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                                                                                                                              |
|------|-------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RX_TRIG_DLY | R/W  | 0h    | This is the 24 bit count of the trigger delay in SYSCLK cycles. If enabled, the Trigger-1 output of the trigger module will generate a 3 SYSCLK wide trigger pulse after the selected input trigger source sees a rising edge with a delay defined by this 24-bit value. |
| 7:5  | RESERVED_1  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                 |
| 4:1  | TRIG_SEL    | R/W  | 0h    | This is the mux Select Value which selects which of the inputs will be used as the trigger source.                                                                                                                                                                       |
| 0    | TRIG_EN     | R/W  | 0h    | This is the enable for the RX output trigger generation. The output triggers will be generated only if this bit is set to 1. If this bit is 0, then no trigger will be generated by this module.                                                                         |

### 3.9.2.32 FSI\_RX\_CFG\_RX\_TRIG\_CTRL\_2 Register

#### 1 FSI\_RX\_CFG\_RX\_TRIG\_CTRL\_2 Register (Offset = 68h) [reset = 0h]

Receive Trigger Control register 2

Return to [Summary Table](#)

**Table 3-1510. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 0068h       |
| FSI_RX1       | 5029 1068h       |
| FSI_RX2       | 502B 0068h       |
| FSI_RX3       | 502B 1068h       |

**Figure 3-483. FSI\_RX\_CFG\_RX\_TRIG\_CTRL\_2 Name Register**

|             |    |    |          |    |    |         |    |
|-------------|----|----|----------|----|----|---------|----|
| 31          | 30 | 29 | 28       | 27 | 26 | 25      | 24 |
| RX_TRIG_DLY |    |    |          |    |    |         |    |
| R/W         |    |    |          |    |    |         |    |
| 0h          |    |    |          |    |    |         |    |
| 23          | 22 | 21 | 20       | 19 | 18 | 17      | 16 |
| RX_TRIG_DLY |    |    |          |    |    |         |    |
| R/W         |    |    |          |    |    |         |    |
| 0h          |    |    |          |    |    |         |    |
| 15          | 14 | 13 | 12       | 11 | 10 | 9       | 8  |
| RX_TRIG_DLY |    |    |          |    |    |         |    |
| R/W         |    |    |          |    |    |         |    |
| 0h          |    |    |          |    |    |         |    |
| 7           | 6  | 5  | 4        | 3  | 2  | 1       | 0  |
| RESERVED_1  |    |    | TRIG_SEL |    |    | TRIG_EN |    |
| R           |    |    | R/W      |    |    | R/W     |    |
| 0h          |    |    | 0h       |    |    | 0h      |    |

**Table 3-1512. FSI\_RX\_CFG\_RX\_TRIG\_CTRL\_2 Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                                                                                                                              |
|------|-------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RX_TRIG_DLY | R/W  | 0h    | This is the 24 bit count of the trigger delay in SYSCLK cycles. If enabled, the Trigger-1 output of the trigger module will generate a 3 SYSCLK wide trigger pulse after the selected input trigger source sees a rising edge with a delay defined by this 24-bit value. |
| 7:5  | RESERVED_1  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                 |
| 4:1  | TRIG_SEL    | R/W  | 0h    | This is the mux Select Value which selects which of the inputs will be used as the trigger source.                                                                                                                                                                       |
| 0    | TRIG_EN     | R/W  | 0h    | This is the enable for the RX output trigger generation. The output triggers will be generated only if this bit is set to 1. If this bit is 0, then no trigger will be generated by this module.                                                                         |

### 3.9.2.33 FSI\_RX\_CFG\_RX\_TRIG\_CTRL\_3 Register

#### 1 FSI\_RX\_CFG\_RX\_TRIG\_CTRL\_3 Register (Offset = 6Ch) [reset = 0h]

Receive Trigger Control register 3

Return to [Summary Table](#)

**Table 3-1513. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 006Ch       |
| FSI_RX1       | 5029 106Ch       |
| FSI_RX2       | 502B 006Ch       |
| FSI_RX3       | 502B 106Ch       |

**Figure 3-484. FSI\_RX\_CFG\_RX\_TRIG\_CTRL\_3 Name Register**

|             |    |    |          |    |    |         |    |
|-------------|----|----|----------|----|----|---------|----|
| 31          | 30 | 29 | 28       | 27 | 26 | 25      | 24 |
| RX_TRIG_DLY |    |    |          |    |    |         |    |
| R/W         |    |    |          |    |    |         |    |
| 0h          |    |    |          |    |    |         |    |
| 23          | 22 | 21 | 20       | 19 | 18 | 17      | 16 |
| RX_TRIG_DLY |    |    |          |    |    |         |    |
| R/W         |    |    |          |    |    |         |    |
| 0h          |    |    |          |    |    |         |    |
| 15          | 14 | 13 | 12       | 11 | 10 | 9       | 8  |
| RX_TRIG_DLY |    |    |          |    |    |         |    |
| R/W         |    |    |          |    |    |         |    |
| 0h          |    |    |          |    |    |         |    |
| 7           | 6  | 5  | 4        | 3  | 2  | 1       | 0  |
| RESERVED_1  |    |    | TRIG_SEL |    |    | TRIG_EN |    |
| R           |    |    | R/W      |    |    | R/W     |    |
| 0h          |    |    | 0h       |    |    | 0h      |    |

**Table 3-1515. FSI\_RX\_CFG\_RX\_TRIG\_CTRL\_3 Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                                                                                                                              |
|------|-------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RX_TRIG_DLY | R/W  | 0h    | This is the 24 bit count of the trigger delay in SYSCLK cycles. If enabled, the Trigger-1 output of the trigger module will generate a 3 SYSCLK wide trigger pulse after the selected input trigger source sees a rising edge with a delay defined by this 24-bit value. |
| 7:5  | RESERVED_1  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                 |
| 4:1  | TRIG_SEL    | R/W  | 0h    | This is the mux Select Value which selects which of the inputs will be used as the trigger source.                                                                                                                                                                       |
| 0    | TRIG_EN     | R/W  | 0h    | This is the enable for the RX output trigger generation. The output triggers will be generated only if this bit is set to 1. If this bit is 0, then no trigger will be generated by this module.                                                                         |



### 3.9.2.34 FSI\_RX\_CFG\_RX\_VIS\_1 Register

#### 1 FSI\_RX\_CFG\_RX\_VIS\_1 Register (Offset = 70h) [reset = 0h]

Receive debug visibility register 1

Return to [Summary Table](#)

**Table 3-1516. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 0070h       |
| FSI_RX1       | 5029 1070h       |
| FSI_RX2       | 502B 0070h       |
| FSI_RX3       | 502B 1070h       |

**Figure 3-485. FSI\_RX\_CFG\_RX\_VIS\_1 Name Register**

|            |    |    |    |             |            |    |    |
|------------|----|----|----|-------------|------------|----|----|
| 31         | 30 | 29 | 28 | 27          | 26         | 25 | 24 |
| RESERVED_2 |    |    |    |             |            |    |    |
| R          |    |    |    |             |            |    |    |
| 0h         |    |    |    |             |            |    |    |
| 23         | 22 | 21 | 20 | 19          | 18         | 17 | 16 |
| RESERVED_2 |    |    |    |             |            |    |    |
| R          |    |    |    |             |            |    |    |
| 0h         |    |    |    |             |            |    |    |
| 15         | 14 | 13 | 12 | 11          | 10         | 9  | 8  |
| RESERVED_2 |    |    |    |             |            |    |    |
| R          |    |    |    |             |            |    |    |
| 0h         |    |    |    |             |            |    |    |
| 7          | 6  | 5  | 4  | 3           | 2          | 1  | 0  |
| RESERVED_2 |    |    |    | RX_CORE_STS | RESERVED_1 |    |    |
| R          |    |    |    | R           | R          |    |    |
| 0h         |    |    |    | 0h          | 0h         |    |    |

**Table 3-1518. FSI\_RX\_CFG\_RX\_VIS\_1 Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|-------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED_2  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 3    | RX_CORE_STS | R    | 0h    | Receiver Core Status bit<br>This bit indicates the status of the receiver core. If this bit is set, the receiver should undergo a reset and subsequent resynchronization with the transmitter. This bit will be always be set when the receiver has detected and end of frame error or a frame type error. This bit can also be set if the receiver becomes corrupted due to noise on the signal lines. If the receiver has experienced a ping watchdog or frame watchdog timeout, this bit should be read to determine if the cause was due to a corrupt transaction, thus putting the receiver core into an unrecoverable state.<br>Only a soft reset will reset the receiver core and thus reset this bit.<br>0h[R] The receiver core is operating normally.<br>1h[R] The receiver core has entered into an error state and should be reset. |
| 2:0  | RESERVED_1  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

### 3.9.2.35 FSI\_RX\_CFG\_RX\_UDATA\_FILTER Register

#### 1 FSI\_RX\_CFG\_RX\_UDATA\_FILTER Register (Offset = 74h) [reset = 0h]

Receive User Data Filter Control register.

Return to [Summary Table](#)

**Table 3-1519. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_RX0       | 5029 0074h       |
| FSI_RX1       | 5029 1074h       |
| FSI_RX2       | 502B 0074h       |
| FSI_RX3       | 502B 1074h       |

**Figure 3-486. FSI\_RX\_CFG\_RX\_UDATA\_FILTER Name Register**

|            |    |    |    |    |    |   |   |
|------------|----|----|----|----|----|---|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| UDATA_MASK |    |    |    |    |    |   |   |
| R/W        |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| UDATA_REG  |    |    |    |    |    |   |   |
| R/W        |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |

**Table 3-1521. FSI\_RX\_CFG\_RX\_UDATA\_FILTER Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                          |
|------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | UDATA_MASK | R/W  | 0h    | Bit Mask to be used for comparing the USERDATA field when filtering is enabled. Every bit that is '1' in this register will be masked for comparison. If a bit position is '1', then it will be considered a successful match for that bit position. |
| 7:0  | UDATA_REG  | R/W  | 0h    | Reference to be used for comparing the USERDATA field when filtering is enabled.                                                                                                                                                                     |

### 3.9.2.36 FSI\_RX\_CFG\_RX\_BUF\_BASE\_j Register

#### 1 FSI\_RX\_CFG\_RX\_BUF\_BASE\_j Register (Offset = 80h + formula) [reset = 0h]

Base address for receive data buffer.

Return to [Summary Table](#)

Offset = (j \* 2h); where j = 0 to 15d

**Table 3-1522. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| FSI_RX0       | 5029 0080h + formula |
| FSI_RX1       | 5029 1080h + formula |
| FSI_RX2       | 502B 0080h + formula |
| FSI_RX3       | 502B 1080h + formula |

**Figure 3-487. FSI\_RX\_CFG\_RX\_BUF\_BASE\_j Name Register**

|              |    |    |    |    |    |   |   |
|--------------|----|----|----|----|----|---|---|
| 15           | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| BASE_ADDRESS |    |    |    |    |    |   |   |
| R            |    |    |    |    |    |   |   |
| 0h           |    |    |    |    |    |   |   |
| 7            | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| BASE_ADDRESS |    |    |    |    |    |   |   |
| R            |    |    |    |    |    |   |   |
| 0h           |    |    |    |    |    |   |   |

**Table 3-1524. FSI\_RX\_CFG\_RX\_BUF\_BASE\_j Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                                   |
|------|--------------|------|-------|---------------------------------------------------------------------------------------------------------------|
| 15:0 | BASE_ADDRESS | R    | 0h    | Receive Data Buffer Base Address<br>This is the base address of the 16-word data buffer used by the receiver. |

## 3.10 FSI\_TX

### FSI\_TX

#### 3.10.1 FSI\_TX Summaries

#### FSI\_TX Summaries

**Table 3-1525. FSI\_TX\_CFG Registers, Base Address=5028 0000h, Length=4096**

| Offset | Length | Register Name                                   | FSI_TX0 Physical Address | FSI_TX1 Physical Address | FSI_TX2 Physical Address |
|--------|--------|-------------------------------------------------|--------------------------|--------------------------|--------------------------|
| 0h     | 16     | <a href="#">FSI_TX_CFG_TX_MASTER_CTRL</a>       | 5028 0000h               | 5028 1000h               | 502A 0000h               |
| 4h     | 16     | <a href="#">FSI_TX_CFG_TX_CLK_CTRL</a>          | 5028 0004h               | 5028 1004h               | 502A 0004h               |
| 8h     | 16     | <a href="#">FSI_TX_CFG_TX_OPER_CTRL_LO_ALT2</a> | 5028 0008h               | 5028 1008h               | 502A 0008h               |
| Ah     | 16     | <a href="#">FSI_TX_CFG_TX_OPER_CTRL_HI_ALT1</a> | 5028 000Ah               | 5028 100Ah               | 502A 000Ah               |
| Ch     | 16     | <a href="#">FSI_TX_CFG_TX_FRAME_CTRL</a>        | 5028 000Ch               | 5028 100Ch               | 502A 000Ch               |
| Eh     | 16     | <a href="#">FSI_TX_CFG_TX_FRAME_TAG_UDATA</a>   | 5028 000Eh               | 5028 100Eh               | 502A 000Eh               |
| 10h    | 16     | <a href="#">FSI_TX_CFG_TX_BUF_PTR_LOAD</a>      | 5028 0010h               | 5028 1010h               | 502A 0010h               |
| 12h    | 16     | <a href="#">FSI_TX_CFG_TX_BUF_PTR_STS</a>       | 5028 0012h               | 5028 1012h               | 502A 0012h               |
| 14h    | 16     | <a href="#">FSI_TX_CFG_TX_PING_CTRL_AL_T1</a>   | 5028 0014h               | 5028 1014h               | 502A 0014h               |
| 16h    | 16     | <a href="#">FSI_TX_CFG_TX_PING_TAG</a>          | 5028 0016h               | 5028 1016h               | 502A 0016h               |
| 18h    | 32     | <a href="#">FSI_TX_CFG_TX_PING_TO_REF</a>       | 5028 0018h               | 5028 1018h               | 502A 0018h               |
| 1Ch    | 32     | <a href="#">FSI_TX_CFG_TX_PING_TO_CNT</a>       | 5028 001Ch               | 5028 101Ch               | 502A 001Ch               |
| 20h    | 16     | <a href="#">FSI_TX_CFG_TX_INT_CTRL</a>          | 5028 0020h               | 5028 1020h               | 502A 0020h               |
| 22h    | 16     | <a href="#">FSI_TX_CFG_TX_DMA_CTRL</a>          | 5028 0022h               | 5028 1022h               | 502A 0022h               |
| 24h    | 16     | <a href="#">FSI_TX_CFG_TX_LOCK_CTRL</a>         | 5028 0024h               | 5028 1024h               | 502A 0024h               |
| 28h    | 16     | <a href="#">FSI_TX_CFG_TX_EVT_STS</a>           | 5028 0028h               | 5028 1028h               | 502A 0028h               |
| 2Ch    | 16     | <a href="#">FSI_TX_CFG_TX_EVT_CLR</a>           | 5028 002Ch               | 5028 102Ch               | 502A 002Ch               |
| 2Eh    | 16     | <a href="#">FSI_TX_CFG_TX_EVT_FRC</a>           | 5028 002Eh               | 5028 102Eh               | 502A 002Eh               |
| 30h    | 16     | <a href="#">FSI_TX_CFG_TX_USER_CRC</a>          | 5028 0030h               | 5028 1030h               | 502A 0030h               |
| 40h    | 32     | <a href="#">FSI_TX_CFG_TX_ECC_DATA</a>          | 5028 0040h               | 5028 1040h               | 502A 0040h               |
| 44h    | 16     | <a href="#">FSI_TX_CFG_TX_ECC_VAL</a>           | 5028 0044h               | 5028 1044h               | 502A 0044h               |
| 48h    | 16     | <a href="#">FSI_TX_CFG_TX_DLYLINE_CTRL</a>      | 5028 0048h               | 5028 1048h               | 502A 0048h               |
| 80h    | 16     | <a href="#">FSI_TX_CFG_TX_BUF_BASE_J</a>        | 5028 0080h + formula     | 5028 1080h + formula     | 502A 0080h + formula     |

**Table 3-1526. FSI\_TX\_CFG Registers, Base Address=5028 0000h, Length=4096**

| Offset | Length | Register Name                                   | FSI_TX3 Physical Address |
|--------|--------|-------------------------------------------------|--------------------------|
| 0h     | 16     | <a href="#">FSI_TX_CFG_TX_MASTER_CTRL</a>       | 502A 1000h               |
| 4h     | 16     | <a href="#">FSI_TX_CFG_TX_CLK_CTRL</a>          | 502A 1004h               |
| 8h     | 16     | <a href="#">FSI_TX_CFG_TX_OPER_CTRL_LO_ALT2</a> | 502A 1008h               |
| Ah     | 16     | <a href="#">FSI_TX_CFG_TX_OPER_CTRL_HI_ALT1</a> | 502A 100Ah               |
| Ch     | 16     | <a href="#">FSI_TX_CFG_TX_FRAME_CTRL</a>        | 502A 100Ch               |
| Eh     | 16     | <a href="#">FSI_TX_CFG_TX_FRAME_TAG_UDATA</a>   | 502A 100Eh               |
| 10h    | 16     | <a href="#">FSI_TX_CFG_TX_BUF_PTR_LOAD</a>      | 502A 1010h               |

**Table 3-1526. FSI\_TX\_CFG Registers, Base Address=5028 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                                | FSI_TX3 Physical Address |
|--------|--------|----------------------------------------------|--------------------------|
| 12h    | 16     | <a href="#">FSI_TX_CFG_TX_BUF_PTR_STS</a>    | 502A 1012h               |
| 14h    | 16     | <a href="#">FSI_TX_CFG_TX_PING_CTRL_ALT1</a> | 502A 1014h               |
| 16h    | 16     | <a href="#">FSI_TX_CFG_TX_PING_TAG</a>       | 502A 1016h               |
| 18h    | 32     | <a href="#">FSI_TX_CFG_TX_PING_TO_REF</a>    | 502A 1018h               |
| 1Ch    | 32     | <a href="#">FSI_TX_CFG_TX_PING_TO_CNT</a>    | 502A 101Ch               |
| 20h    | 16     | <a href="#">FSI_TX_CFG_TX_INT_CTRL</a>       | 502A 1020h               |
| 22h    | 16     | <a href="#">FSI_TX_CFG_TX_DMA_CTRL</a>       | 502A 1022h               |
| 24h    | 16     | <a href="#">FSI_TX_CFG_TX_LOCK_CTRL</a>      | 502A 1024h               |
| 28h    | 16     | <a href="#">FSI_TX_CFG_TX_EVT_STS</a>        | 502A 1028h               |
| 2Ch    | 16     | <a href="#">FSI_TX_CFG_TX_EVT_CLR</a>        | 502A 102Ch               |
| 2Eh    | 16     | <a href="#">FSI_TX_CFG_TX_EVT_FRC</a>        | 502A 102Eh               |
| 30h    | 16     | <a href="#">FSI_TX_CFG_TX_USER_CRC</a>       | 502A 1030h               |
| 40h    | 32     | <a href="#">FSI_TX_CFG_TX_ECC_DATA</a>       | 502A 1040h               |
| 44h    | 16     | <a href="#">FSI_TX_CFG_TX_ECC_VAL</a>        | 502A 1044h               |
| 48h    | 16     | <a href="#">FSI_TX_CFG_TX_DLYLINE_CTRL</a>   | 502A 1048h               |
| 80h    | 16     | <a href="#">FSI_TX_CFG_TX_BUF_BASE_J</a>     | 502A 1080h + formula     |

### 3.10.2 FSI\_TX Registers

#### FSI\_TX Registers

### 3.10.2.1 FSI\_TX\_CFG\_TX\_MASTER\_CTRL Register

#### 1 FSI\_TX\_CFG\_TX\_MASTER\_CTRL Register (Offset = 0h) [reset = 0h]

Transmit master control register.

Return to [Summary Table](#)

**Table 3-1527. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_TX0       | 5028 0000h       |
| FSI_TX1       | 5028 1000h       |
| FSI_TX2       | 502A 0000h       |
| FSI_TX3       | 502A 1000h       |

**Figure 3-488. FSI\_TX\_CFG\_TX\_MASTER\_CTRL Name Register**

|            |    |    |    |    |    |       |          |
|------------|----|----|----|----|----|-------|----------|
| 15         | 14 | 13 | 12 | 11 | 10 | 9     | 8        |
| KEY        |    |    |    |    |    |       |          |
| W          |    |    |    |    |    |       |          |
| 0h         |    |    |    |    |    |       |          |
| 7          | 6  | 5  | 4  | 3  | 2  | 1     | 0        |
| RESERVED_1 |    |    |    |    |    | FLUSH | CORE_RST |
| R          |    |    |    |    |    | R/W   | R/W      |
| 0h         |    |    |    |    |    | 0h    | 0h       |

**Table 3-1529. FSI\_TX\_CFG\_TX\_MASTER\_CTRL Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | KEY        | W    | 0h    | Write Key<br>In order to write to any bit in this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after Writing, so it must be written again for every change to this register.                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 7:2  | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 1    | FLUSH      | R/W  | 0h    | Flush Operation Start bit<br>This bit will cause the transmitter to initiate a flush pattern of a single toggle on the TXD0 and TXD1 followed by five full cycles of TXCLK. This bit should be written only when the CORE_RST bit is 0 and the clock to the Transmitter core is turned on.<br>0h[R/W] = Clear this bit.<br>1h[R/W] = Setting this bit will Initiate flush sequence.<br>To properly execute a flush sequence, Set FLUSH to 1, wait for five TXCLK cycles then clear FLUSH to 0.<br>Note: The KEY field must contain 0xA5 for any write to this bit to take effect. The software must keep this bit set to 1 for at least five TXCLK cycles before setting it back to 0. |
| 0    | CORE_RST   | R/W  | 0h    | Transmitter Master Core Reset bit<br>This bit controls the transmitter master core reset. In order to send any frame, this bit must be cleared.<br>0h[R/W] = Transmitter core is not in reset and can transmit frames.<br>1h[R/W] = Transmitter core is held in reset.<br>Note: The KEY field must contain 0xA5 for any write to this bit to take effect.                                                                                                                                                                                                                                                                                                                              |

### 3.10.2.2 FSI\_TX\_CFG\_TX\_CLK\_CTRL Register

#### 1 FSI\_TX\_CFG\_TX\_CLK\_CTRL Register (Offset = 4h) [reset = 0h]

Transmit clock control register.

Return to [Summary Table](#)

**Table 3-1530. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_TX0       | 5028 0004h       |
| FSI_TX1       | 5028 1004h       |
| FSI_TX2       | 502A 0004h       |
| FSI_TX3       | 502A 1004h       |

**Figure 3-489. FSI\_TX\_CFG\_TX\_CLK\_CTRL Name Register**

| 15           | 14 | 13 | 12 | 11 | 10 | 9            | 8       |
|--------------|----|----|----|----|----|--------------|---------|
| RESERVED_1   |    |    |    |    |    | PRESCALE_VAL |         |
| R            |    |    |    |    |    | R/W          |         |
| 0h           |    |    |    |    |    | 0h           |         |
| 7            | 6  | 5  | 4  | 3  | 2  | 1            | 0       |
| PRESCALE_VAL |    |    |    |    |    | CLK_EN       | CLK_RST |
| R/W          |    |    |    |    |    | R/W          | R/W     |
| 0h           |    |    |    |    |    | 0h           | 0h      |

**Table 3-1532. FSI\_TX\_CFG\_TX\_CLK\_CTRL Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|--------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED_1   | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 9:2   | PRESCALE_VAL | R/W  | 0h    | <p>Clock Divider Prescale Value</p> <p>The input clock is divided by this 8-bit value and fed into the transmitter core. This divided clock is the rate at which TXCLK will operate.</p> <p>0h[R/W] = Reserved</p> <p>1h[R/W] = Input clock / 1</p> <p>2h[R/W] = Input clock / 2</p> <p>3h[R/W] = Input clock / 3</p> <p>4h[R/W] = Input clock / 4</p> <p>...</p> <p>FFh [R/W] = Input clock / 255</p> <p>TXCLKIN = Input clock / PRESCALE_VAL</p> <p>In FSI mode: TXCLK = TXCLKIN / 2</p> <p>In SPI mode: TXCLK = TXCLKIN</p> |
| 1     | CLK_EN       | R/W  | 0h    | <p>Clock Divider Enable bit</p> <p>This bit will enable and disable the input clock divider and start the clock to the transmitter core.</p> <p>0h[R/W] = The input clock divider is not enabled and the clock is not connected to the transmitter core.</p> <p>1h[R/W] = The input clock to the transmitter core is being divided by the PRESCALE_VAL and enabled.</p>                                                                                                                                                        |
| 0     | CLK_RST      | R/W  | 0h    | <p>Clock Divider Reset bit</p> <p>This bit will reset the clock counter in the clock divider.</p> <p>0h[R/W] = The clock divider is set based on the value in PRESCALE_VAL. The input clock will be divided by PRESCALE_VAL if CLK_EN is set.</p> <p>1h[R/W] = The clock divider will be reset to 0 and will stay reset until software writes a 0 to this bit.</p>                                                                                                                                                             |

### 3.10.2.3 FSI\_TX\_CFG\_TX\_OPER\_CTRL\_LO\_ALT2 Register

#### 1 FSI\_TX\_CFG\_TX\_OPER\_CTRL\_LO\_ALT2 Register (Offset = 8h) [reset = 0h]

Transmit operation control register low.

Return to [Summary Table](#)

**Table 3-1533. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_TX0       | 5028 0008h       |
| FSI_TX1       | 5028 1008h       |
| FSI_TX2       | 502A 0008h       |
| FSI_TX3       | 502A 1008h       |

**Figure 3-490. FSI\_TX\_CFG\_TX\_OPER\_CTRL\_LO\_ALT2 Name Register**

| 15           | 14     | 13         | 12 | 11 | 10         | 9          | 8          |
|--------------|--------|------------|----|----|------------|------------|------------|
| RESERVED_1   |        |            |    |    | SEL_TDM_IN | TDM_ENABLE | SEL_PLLCLK |
| R            |        |            |    |    | R/W        | R/W        | R/W        |
| 0h           |        |            |    |    | 0h         | 0h         | 0h         |
| 7            | 6      | 5          | 4  | 3  | 2          | 1          | 0          |
| PING_TO_MODE | SW_CRC | START_MODE |    |    | SPI_MODE   | DATA_WIDTH |            |
| R/W          | R/W    | R/W        |    |    | R/W        | R/W        |            |
| 0h           | 0h     | 0h         |    |    | 0h         | 0h         |            |

**Table 3-1535. FSI\_TX\_CFG\_TX\_OPER\_CTRL\_LO\_ALT2 Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                   |
|-------|--------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | RESERVED_1   | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                      |
| 10    | SEL_TDM_IN   | R/W  | 0h    | Input TDM port Select bit<br>This bit selects the input port for the transmitter core between the TDM input pins or the RX module.<br>When this bit is '0', the inputs selected for TDM are from the TDM input pins.<br>When this bit is '1', then inputs selected for TDM are from the RX module.                                            |
| 9     | TDM_ENABLE   | R/W  | 0h    | Transmit TDM Mode Enable bit.<br>This bit enables the TDM Mode for multi-slave TDM operation.<br>0h[R/W] Transmit TDM Mode is not enabled.<br>1h[R/W] Transmit TDM Mode is enabled.                                                                                                                                                           |
| 8     | SEL_PLLCLK   | R/W  | 0h    | Input Clock Select bit<br>This bit selects the input clock source for the transmitter core.<br>0h[R/W] = SYSCLK is the source of the transmitter clock into the clock prescaler.<br>1h[R/W] = PLLRAWCLK is the source of the transmitter core clock into the clock prescaler.                                                                 |
| 7     | PING_TO_MODE | R/W  | 0h    | Ping Counter Reset Mode Select bit<br>This bit selects when the ping counter will reset.<br>0h[R/W] = The ping counter will reset and restart only on hardware initiated ping frames, when ping counter has timed out.<br>1h[R/W] = The ping counter will reset and restart on any software initiated frame as well as a ping counter timeout |
| 6     | SW_CRC       | R/W  | 0h    | CRC Source Select bit<br>This bit selects the source of the CRC value that is transmitted.<br>0h[R/W] = The transmitted CRC value is computed by hardware.<br>1h[R/W] = The transmitted CRC value is sourced from the value programmed in the TX_USER_CRC register.                                                                           |



**Table 3-1535. FSI\_TX\_CFG\_TX\_OPER\_CTRL\_LO\_ALT2 Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5:3 | START_MODE | R/W  | 0h    | <p>Transmission Start Mode Select bit</p> <p>These bits select the method by which a new frame transmission is started.</p> <p>0h[R/W] = Only a software write to TX_FRAME_CTRL.START initiate a new transmission.</p> <p>1h[R/W] = The configured external trigger will initiate a new transmission.</p> <p>2h[R/W] = Either Writing to TX_FRAME_CTRL.START or the TX_FRAME_TAG_UDATA register will initiate a new transmission.</p> <p>All other combinations of bits are illegal and reserved for future use.</p> |
| 2   | SPI_MODE   | R/W  | 0h    | <p>SPI Mode Select bit</p> <p>This bit enables and disables SPI compatibility mode.</p> <p>0h[R/W] = FSI is in normal mode of operation.</p> <p>1h[R/W] = FSI is operating in SPI compatibility mode.</p>                                                                                                                                                                                                                                                                                                            |
| 1:0 | DATA_WIDTH | R/W  | 0h    | <p>Transmit Data Width Select bits</p> <p>These bits define the number of data lines used by the transmitter.</p> <p>0h[R/W] = Data will be transmitted on one data line [TXD0]</p> <p>1h[R/W] = Data will be transmitted on two data lines [TXD0 and TXD1]. The format of the data is described in the FSI_TX TRM chapter.</p> <p>2h</p> <p>3h[R/W] = Reserved</p>                                                                                                                                                  |

### 3.10.2.4 FSI\_TX\_CFG\_TX\_OPER\_CTRL\_HI\_ALT1 Register

#### 1 FSI\_TX\_CFG\_TX\_OPER\_CTRL\_HI\_ALT1 Register (Offset = Ah) [reset = 0h]

Transmit operation control register high.

Return to [Summary Table](#)

**Table 3-1536. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_TX0       | 5028 000Ah       |
| FSI_TX1       | 5028 100Ah       |
| FSI_TX2       | 502A 000Ah       |
| FSI_TX3       | 502A 100Ah       |

**Figure 3-491. FSI\_TX\_CFG\_TX\_OPER\_CTRL\_HI\_ALT1 Name Register**

|              |         |           |            |              |    |   |   |
|--------------|---------|-----------|------------|--------------|----|---|---|
| 15           | 14      | 13        | 12         | 11           | 10 | 9 | 8 |
| RESERVED_2   |         |           |            | EXT_TRIG_SEL |    |   |   |
| R            |         |           |            | R/W          |    |   |   |
| 0h           |         |           |            | 0h           |    |   |   |
| 7            | 6       | 5         | 4          | 3            | 2  | 1 | 0 |
| EXT_TRIG_SEL | ECC_SEL | FORCE_ERR | RESERVED_1 |              |    |   |   |
| R/W          | R/W     | R/W       | R          |              |    |   |   |
| 0h           | 0h      | 0h        | 0h         |              |    |   |   |

**Table 3-1538. FSI\_TX\_CFG\_TX\_OPER\_CTRL\_HI\_ALT1 Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|--------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | RESERVED_2   | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 12:7  | EXT_TRIG_SEL | R/W  | 0h    | External Trigger Select bit<br>These bits define which of the 64 external inputs will be used as the source for the external input trigger.<br>00h[R/W] = Trigger 1 is the source.<br>01h[R/W] = Trigger 2 is the source.<br>02h[R/W] = Trigger 3 is the source.<br>...<br>3Fh [R/W] = Trigger 64 is the source.                                                                                                                                                                                                                        |
| 6     | ECC_SEL      | R/W  | 0h    | ECC Data Width Select bit<br>This bit selects between 16-bit and 32-bit ECC computation.<br>0h[R/W] = 32-bit ECC is used.<br>1h[R/W] = 16-bit ECC is used.                                                                                                                                                                                                                                                                                                                                                                              |
| 5     | FORCE_ERR    | R/W  | 0h    | Error Frame Force bit<br>This bit will force the the CRC value of the transmitted data frame to 0 whenever there is a buffer overrun or underrun condition. This can be used to force a corrupted CRC as the data is not guaranteed to be reliable. The receiver will treat the data as invalid and can handle this as needed.<br>Note: DO NOT use FORCE_ERR if using the SW CRC mode [FSI Transmit].<br>0h[R/W] = The CRC will not be forced to 0.<br>1h[R/W] = The CRC will be forced to 0 in a buffer overrun or underrun condition. |
| 4:0   | RESERVED_1   | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

### 3.10.2.5 FSI\_TX\_CFG\_TX\_FRAME\_CTRL Register

#### 1 FSI\_TX\_CFG\_TX\_FRAME\_CTRL Register (Offset = Ch) [reset = 0h]

Transmit frame control register.

Return to [Summary Table](#)

**Table 3-1539. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_TX0       | 5028 000Ch       |
| FSI_TX1       | 5028 100Ch       |
| FSI_TX2       | 502A 000Ch       |
| FSI_TX3       | 502A 100Ch       |

**Figure 3-492. FSI\_TX\_CFG\_TX\_FRAME\_CTRL Name Register**

|         |            |    |    |            |    |   |   |
|---------|------------|----|----|------------|----|---|---|
| 15      | 14         | 13 | 12 | 11         | 10 | 9 | 8 |
| START   | RESERVED_1 |    |    |            |    |   |   |
| R/W     | R          |    |    |            |    |   |   |
| 0h      | 0h         |    |    |            |    |   |   |
| 7       | 6          | 5  | 4  | 3          | 2  | 1 | 0 |
| N_WORDS |            |    |    | FRAME_TYPE |    |   |   |
| R/W     |            |    |    | R/W        |    |   |   |
| 0h      |            |    |    | 0h         |    |   |   |

**Table 3-1541. FSI\_TX\_CFG\_TX\_FRAME\_CTRL Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | START      | R/W  | 0h    | Start Transmission bit<br>This bit will cause the FSI to start transmitting the next frame.<br>0h[R/W] = Writing a 0 to this bit will have no effect.<br>1h[R/W] = Start the next transmission. This bit will be cleared by hardware.                                                                                                                                                                                                               |
| 14:8 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 7:4  | N_WORDS    | R/W  | 0h    | Number of Words to be Transmitted<br>This field defines the number of words which will be transmitted in a DATA_N_WORD frame. This is a user-defined field that must match the corresponding field in the receiver. Set this bitfield to be one less than the number of words to be transmitted.<br>0h[R/W] = 1 data word frame [16-bit data].<br>1h[R/W] = 2 data word frame [32-bit data].<br>..<br>Fh [R/W] = 16 data word frame [256-bit data]. |

**Table 3-1541. FSI\_TX\_CFG\_TX\_FRAME\_CTRL Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-----|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0 | FRAME_TYPE | R/W  | 0h    | <p>Transmit Frame Type</p> <p>This field determines the type of frame that will be transmitted next.</p> <p>0000b[R/W] = Ping Frame. This frame can be sent either by software or automatically by hardware.</p> <p>0100b[R/W] = DATA_1_WORD Frame. One word data frame [16-bit data].</p> <p>0101b[R/W] = DATA_2_WORD Frame. Two word data frame [32-bit data].</p> <p>0110b[R/W] = DATA_4_WORD Frame. Four word data frame [64-bit data].</p> <p>0111b[R/W] = DATA_6_WORD Frame. Six word data frame [96-bit data].</p> <p>0011b[R/W] = DATA_N_WORD Frame. The N_WORDS field will determine the number of words [1 to 16] to be sent. Both the transmitter and receiver must have the same value programmed.</p> <p>1111b[R/W] = Error Frame. This frame can be used during error conditions or any condition where the transmitter wants to notify the receiver of a high priority status. However, the user software is at liberty to use this for any purpose.</p> <p>0001b<br/>0010b and<br/>1000bthrough<br/>1110bare Reserved and should not be used.</p> |

### 3.10.2.6 FSI\_TX\_CFG\_TX\_FRAME\_TAG\_UDATA Register

#### 1 FSI\_TX\_CFG\_TX\_FRAME\_TAG\_UDATA Register (Offset = Eh) [reset = 0h]

Transmit frame tag and user data register.

Return to [Summary Table](#)

**Table 3-1542. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_TX0       | 5028 000Eh       |
| FSI_TX1       | 5028 100Eh       |
| FSI_TX2       | 502A 000Eh       |
| FSI_TX3       | 502A 100Eh       |

**Figure 3-493. FSI\_TX\_CFG\_TX\_FRAME\_TAG\_UDATA Name Register**

|            |    |    |    |           |    |   |   |
|------------|----|----|----|-----------|----|---|---|
| 15         | 14 | 13 | 12 | 11        | 10 | 9 | 8 |
| USER_DATA  |    |    |    |           |    |   |   |
| R/W        |    |    |    |           |    |   |   |
| 0h         |    |    |    |           |    |   |   |
| 7          | 6  | 5  | 4  | 3         | 2  | 1 | 0 |
| RESERVED_1 |    |    |    | FRAME_TAG |    |   |   |
| R          |    |    |    | R/W       |    |   |   |
| 0h         |    |    |    | 0h        |    |   |   |

**Table 3-1544. FSI\_TX\_CFG\_TX\_FRAME\_TAG\_UDATA Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                  |
|------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | USER_DATA  | R/W  | 0h    | User Data bits<br>This is a user-defined value that will be loaded into the the user data phase of the frame. This 8-bit value can be used by the receiver for any application need. This value will not impact any hardware behavior.                                                                                                                                                       |
| 7:4  | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                     |
| 3:0  | FRAME_TAG  | R/W  | 0h    | This will be used only for software initiated transmissions.<br>Frame tag bits<br>This is a user-defined value that will be loaded into the frame tag phase of the next transmission. The receiver may use the frame tag for any application need. This value will not impact any hardware behavior<br>For external triggers do not use this register. Use the TX_PING_TAG register instead. |

### 3.10.2.7 FSI\_TX\_CFG\_TX\_BUF\_PTR\_LOAD Register

#### 1 FSI\_TX\_CFG\_TX\_BUF\_PTR\_LOAD Register (Offset = 10h) [reset = 0h]

Transmit buffer pointer control load register.

Return to [Summary Table](#)

**Table 3-1545. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_TX0       | 5028 0010h       |
| FSI_TX1       | 5028 1010h       |
| FSI_TX2       | 502A 0010h       |
| FSI_TX3       | 502A 1010h       |

**Figure 3-494. FSI\_TX\_CFG\_TX\_BUF\_PTR\_LOAD Name Register**

|            |    |    |    |              |    |   |   |
|------------|----|----|----|--------------|----|---|---|
| 15         | 14 | 13 | 12 | 11           | 10 | 9 | 8 |
| RESERVED_1 |    |    |    |              |    |   |   |
| R          |    |    |    |              |    |   |   |
| 0h         |    |    |    |              |    |   |   |
| 7          | 6  | 5  | 4  | 3            | 2  | 1 | 0 |
| RESERVED_1 |    |    |    | BUF_PTR_LOAD |    |   |   |
| R          |    |    |    | R/W          |    |   |   |
| 0h         |    |    |    | 0h           |    |   |   |

**Table 3-1547. FSI\_TX\_CFG\_TX\_BUF\_PTR\_LOAD Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|--------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:4 | RESERVED_1   | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 3:0  | BUF_PTR_LOAD | R/W  | 0h    | Buffer Pointer Load bits<br>These bits are used to force the transmit buffer pointer to a desired index within the transmit buffer. The next transmission will begin picking data from this index and increment appropriately. This value will be reflected in TX_BUF_PTR_STS only after a minimum 3 SYSCLK cycles + 3 TXCLK cycles.<br>This value should not be written while there is an active transmission as it may corrupt the ongoing frame or other undefined behavior. |

### 3.10.2.8 FSI\_TX\_CFG\_TX\_BUF\_PTR\_STS Register

#### 1 FSI\_TX\_CFG\_TX\_BUF\_PTR\_STS Register (Offset = 12h) [reset = 0h]

Transmit buffer pointer control status register.

Return to [Summary Table](#)

**Table 3-1548. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_TX0       | 5028 0012h       |
| FSI_TX1       | 5028 1012h       |
| FSI_TX2       | 502A 0012h       |
| FSI_TX3       | 502A 1012h       |

**Figure 3-495. FSI\_TX\_CFG\_TX\_BUF\_PTR\_STS Name Register**

|            |    |    |    |               |    |   |   |
|------------|----|----|----|---------------|----|---|---|
| 15         | 14 | 13 | 12 | 11            | 10 | 9 | 8 |
| RESERVED_2 |    |    |    | CURR_WORD_CNT |    |   |   |
| R          |    |    |    | R             |    |   |   |
| 0h         |    |    |    | 0h            |    |   |   |
| 7          | 6  | 5  | 4  | 3             | 2  | 1 | 0 |
| RESERVED_1 |    |    |    | CURR_BUF_PTR  |    |   |   |
| R          |    |    |    | R             |    |   |   |
| 0h         |    |    |    | 0h            |    |   |   |

**Table 3-1550. FSI\_TX\_CFG\_TX\_BUF\_PTR\_STS Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                                                                                                                                                                                 |
|-------|---------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | RESERVED_2    | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                    |
| 12:8  | CURR_WORD_CNT | R    | 0h    | Words Remaining in the transmit buffer<br>This value indicates the number of words present in the data buffer which have not yet been transmitted. This value is only valid when there is no active transmission.<br>Note: This value will not be valid if there is a buffer overrun or underrun condition. |
| 7:4   | RESERVED_1    | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                    |
| 3:0   | CURR_BUF_PTR  | R    | 0h    | Current Buffer Pointer Index<br>This bitfield will show the current index of the buffer pointer. This value is only valid when there is no active transmission.                                                                                                                                             |

### 3.10.2.9 FSI\_TX\_CFG\_TX\_PING\_CTRL\_ALT1 Register

#### 1 FSI\_TX\_CFG\_TX\_PING\_CTRL\_ALT1 Register (Offset = 14h) [reset = 0h]

Transmit ping control register.

Return to [Summary Table](#)

**Table 3-1551. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_TX0       | 5028 0014h       |
| FSI_TX1       | 5028 1014h       |
| FSI_TX2       | 502A 0014h       |
| FSI_TX3       | 502A 1014h       |

**Figure 3-496. FSI\_TX\_CFG\_TX\_PING\_CTRL\_ALT1 Name Register**

|              |    |    |    |             |    |          |              |
|--------------|----|----|----|-------------|----|----------|--------------|
| 15           | 14 | 13 | 12 | 11          | 10 | 9        | 8            |
| RESERVED_1   |    |    |    |             |    |          | EXT_TRIG_SEL |
| R            |    |    |    |             |    |          | R/W          |
| 0h           |    |    |    |             |    |          | 0h           |
| 7            | 6  | 5  | 4  | 3           | 2  | 1        | 0            |
| EXT_TRIG_SEL |    |    |    | EXT_TRIG_EN |    | TIMER_EN | CNT_RST      |
| R/W          |    |    |    | R/W         |    | R/W      | R/W          |
| 0h           |    |    |    | 0h          |    | 0h       | 0h           |

**Table 3-1553. FSI\_TX\_CFG\_TX\_PING\_CTRL\_ALT1 Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|------|--------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:9 | RESERVED_1   | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 8:3  | EXT_TRIG_SEL | R/W  | 0h    | External Trigger Select bits<br>This bitfield will select one of the 64 external trigger inputs to as the source to generate a ping frame. A ping frame will only be generated if the EXT_TRIG_EN bit is set.<br>0h[R/W] = Trigger 1 will be used to generate a ping frame.<br>1h[R/W] = Trigger 2 will be used to generate a ping frame.<br>..<br>3Fh [R/W] = Trigger 64 will be used to generate a ping frame.                                                                         |
| 2    | EXT_TRIG_EN  | R/W  | 0h    | External Trigger Enable bit<br>This bit will allow the external trigger logic to generate a ping frame.<br>0h[R/W] = External triggers will not be used to generate ping frames.<br>1h[R/W] = The selected external trigger [selected by EXT_TRIG_SEL bits] will be able to generate a ping frame. The ping timer will be ignored if this bit is set.                                                                                                                                    |
| 1    | TIMER_EN     | R/W  | 0h    | Ping Timer Enable bit<br>This bit will enable the ping timer for generating periodic ping frames.<br>0h[R/W] = The ping timer is disabled and will not generate ping frames.<br>1h[R/W] = The ping timer is enabled and can be used to generate ping frames. Once the timer count reaches the value set by the TX_PING_TO_REF register, it will initiate a ping frame transmission.<br>Note: If the ping timer is used, EXT_TRIG_EN should not be set as it will override this function. |



**Table 3-1553. FSI\_TX\_CFG\_TX\_PING\_CTRL\_ALT1 Register Field Descriptions (continued)**

| Bit | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                    |
|-----|---------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | CNT_RST | R/W  | 0h    | <p>Ping Counter Reset bit</p> <p>Writing a 1 to this bit will reset the ping counter to 0. The counter will stay in reset as long as this bit is set to 1. This bit needs to be cleared to 0 to use the counter.</p> <p>0h[R/W] = Clear the CNT_RST.</p> <p>1h[R/W] = The ping counter will be reset to 0.</p> |

### 3.10.2.10 FSI\_TX\_CFG\_TX\_PING\_TAG Register

#### 1 FSI\_TX\_CFG\_TX\_PING\_TAG Register (Offset = 16h) [reset = 0h]

Transmit ping tag register.

Return to [Summary Table](#)

**Table 3-1554. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_TX0       | 5028 0016h       |
| FSI_TX1       | 5028 1016h       |
| FSI_TX2       | 502A 0016h       |
| FSI_TX3       | 502A 1016h       |

**Figure 3-497. FSI\_TX\_CFG\_TX\_PING\_TAG Name Register**

|            |    |    |    |     |    |   |   |
|------------|----|----|----|-----|----|---|---|
| 15         | 14 | 13 | 12 | 11  | 10 | 9 | 8 |
| RESERVED_1 |    |    |    |     |    |   |   |
| R          |    |    |    |     |    |   |   |
| 0h         |    |    |    |     |    |   |   |
| 7          | 6  | 5  | 4  | 3   | 2  | 1 | 0 |
| RESERVED_1 |    |    |    | TAG |    |   |   |
| R          |    |    |    | R/W |    |   |   |
| 0h         |    |    |    | 0h  |    |   |   |

**Table 3-1556. FSI\_TX\_CFG\_TX\_PING\_TAG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                              |
|------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:4 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                 |
| 3:0  | TAG        | R/W  | 0h    | Ping Frame Tag<br>This field contains a 4-bit tag which will be sent in any ping frame that is initiated by an external trigger or the ping timer. This field is user-defined and can be set based on the application requirement. If a ping frame is generated manually, the transmitted tag will be from TX_FRAME_TAG_UDATA.FRAME_TAG, not this value. |

### 3.10.2.11 FSI\_TX\_CFG\_TX\_PING\_TO\_REF Register

#### 1 FSI\_TX\_CFG\_TX\_PING\_TO\_REF Register (Offset = 18h) [reset = 0h]

Transmit ping timeout counter reference.

Return to [Summary Table](#)

**Table 3-1557. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_TX0       | 5028 0018h       |
| FSI_TX1       | 5028 1018h       |
| FSI_TX2       | 502A 0018h       |
| FSI_TX3       | 502A 1018h       |

**Figure 3-498. FSI\_TX\_CFG\_TX\_PING\_TO\_REF Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TO_REF |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TO_REF |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TO_REF |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TO_REF |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 3-1559. FSI\_TX\_CFG\_TX\_PING\_TO\_REF Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                      |
|------|--------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | TO_REF | R/W  | 0h    | Ping Timer Reference Value.<br>This is the 32-bit reference value for the ping timer. The timer will increment the counter starting from 0. When the reference value is reached, it will generate a timeout event, triggering a ping frame transmission. The counter will then reset to 0 and continue counting. |

### 3.10.2.12 FSI\_TX\_CFG\_TX\_PING\_TO\_CNT Register

#### 1 FSI\_TX\_CFG\_TX\_PING\_TO\_CNT Register (Offset = 1Ch) [reset = 0h]

Transmit ping timeout current count.

Return to [Summary Table](#)

**Table 3-1560. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_TX0       | 5028 001Ch       |
| FSI_TX1       | 5028 101Ch       |
| FSI_TX2       | 502A 001Ch       |
| FSI_TX3       | 502A 101Ch       |

**Figure 3-499. FSI\_TX\_CFG\_TX\_PING\_TO\_CNT Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TO_CNT |    |    |    |    |    |    |    |
| R      |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TO_CNT |    |    |    |    |    |    |    |
| R      |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TO_CNT |    |    |    |    |    |    |    |
| R      |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TO_CNT |    |    |    |    |    |    |    |
| R      |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 3-1562. FSI\_TX\_CFG\_TX\_PING\_TO\_CNT Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                |
|------|--------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | TO_CNT | R    | 0h    | Ping Timer Counter Value<br>This register contains the current value of the ping timer counter. After reset, this counter will increment until it reaches the reference value [TX_PING_TO_REF], at which point it generates a ping frame transmission. After this point, the counter will reset to 0 and continue counting. This is a free-running counter |

### 3.10.2.13 FSI\_TX\_CFG\_TX\_INT\_CTRL Register

#### 1 FSI\_TX\_CFG\_TX\_INT\_CTRL Register (Offset = 20h) [reset = 0h]

Transmit interrupt event control register.

Return to [Summary Table](#)

**Table 3-1563. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_TX0       | 5028 0020h       |
| FSI_TX1       | 5028 1020h       |
| FSI_TX2       | 502A 0020h       |
| FSI_TX3       | 502A 1020h       |

**Figure 3-500. FSI\_TX\_CFG\_TX\_INT\_CTRL Name Register**

| 15         | 14 | 13 | 12 | 11              | 10                  | 9                    | 8                  |
|------------|----|----|----|-----------------|---------------------|----------------------|--------------------|
| RESERVED_2 |    |    |    | INT2_EN_PING_TO | INT2_EN_BUF_OVERRUN | INT2_EN_BUF_UNDERRUN | INT2_EN_FRAME_DONE |
| R          |    |    |    | R/W             | R/W                 | R/W                  | R/W                |
| 0h         |    |    |    | 0h              | 0h                  | 0h                   | 0h                 |
| 7          | 6  | 5  | 4  | 3               | 2                   | 1                    | 0                  |
| RESERVED_1 |    |    |    | INT1_EN_PING_TO | INT1_EN_BUF_OVERRUN | INT1_EN_BUF_UNDERRUN | INT1_EN_FRAME_DONE |
| R          |    |    |    | R/W             | R/W                 | R/W                  | R/W                |
| 0h         |    |    |    | 0h              | 0h                  | 0h                   | 0h                 |

**Table 3-1565. FSI\_TX\_CFG\_TX\_INT\_CTRL Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description                                                                                                                                                                                                                                                       |
|-------|----------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | RESERVED_2           | R    | 0h    | Reserved                                                                                                                                                                                                                                                          |
| 11    | INT2_EN_PING_TO      | R/W  | 0h    | Enable PING Timer Interrupt to INT2<br>This bit allows the event to generate an interrupt on the INT2 line.<br>0h[R/W] = This event will not trigger an interrupt on TX_INT2.<br>1h[R/W] = The ping timer event will trigger an interrupt on TX_INT2.             |
| 10    | INT2_EN_BUF_OVERRUN  | R/W  | 0h    | Enable Buffer Overrun Interrupt to INT2<br>This bit allows the event to generate an interrupt on the INT2 line.<br>0h[R/W] = This event will not trigger an interrupt on TX_INT2.<br>1h[R/W] = A Buffer Overrun condition will trigger an interrupt on TX_INT2.   |
| 9     | INT2_EN_BUF_UNDERRUN | R/W  | 0h    | Enable Buffer Underrun Interrupt to INT2<br>This bit allows the event to generate an interrupt on the INT2 line.<br>0h[R/W] = This event will not trigger an interrupt on TX_INT2.<br>1h[R/W] = A Buffer Underrun condition will trigger an interrupt on TX_INT2. |
| 8     | INT2_EN_FRAME_DONE   | R/W  | 0h    | Enable Frame Done interrupt to INT2<br>This bit allows the event to generate an interrupt on the INT2 line.<br>0h[R/W] = This event will not trigger an interrupt on TX_INT2.<br>1h[R/W] = A Frame Done event will trigger an interrupt on TX_INT2.               |
| 7:4   | RESERVED_1           | R    | 0h    | Reserved                                                                                                                                                                                                                                                          |
| 3     | INT1_EN_PING_TO      | R/W  | 0h    | Enable Ping Timer Interrupt to INT1<br>This bit allows the event to generate an interrupt on the INT1 line.<br>0h[R/W] = This event will not trigger an interrupt on TX_INT1.<br>1h[R/W] = The ping timer event will trigger an interrupt on TX_INT1.             |

**Table 3-1565. FSI\_TX\_CFG\_TX\_INT\_CTRL Register Field Descriptions (continued)**

| Bit | Field                | Type | Reset | Description                                                                                                                                                                                                                                                       |
|-----|----------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | INT1_EN_BUF_OVERRUN  | R/W  | 0h    | Enable Buffer Overrun Interrupt to INT1<br>This bit allows the event to generate an interrupt on the INT1 line.<br>0h[R/W] = This event will not trigger an interrupt on TX_INT1.<br>1h[R/W] = A Buffer Overrun condition will trigger an interrupt on TX_INT1.   |
| 1   | INT1_EN_BUF_UNDERRUN | R/W  | 0h    | Enable Buffer Underrun Interrupt to INT1<br>This bit allows the event to generate an interrupt on the INT1 line.<br>0h[R/W] = This event will not trigger an interrupt on TX_INT1.<br>1h[R/W] = A Buffer Underrun condition will trigger an interrupt on TX_INT1. |
| 0   | INT1_EN_FRAME_DONE   | R/W  | 0h    | Enable Frame Done interrupt to INT1<br>This bit allows the event to generate an interrupt on the INT1 line.<br>0h[R/W] = This event will not trigger an interrupt on TX_INT1.<br>1h[R/W] = A Frame Done event will trigger an interrupt on TX_INT1.               |

### 3.10.2.14 FSI\_TX\_CFG\_TX\_DMA\_CTRL Register

#### 1 FSI\_TX\_CFG\_TX\_DMA\_CTRL Register (Offset = 22h) [reset = 0h]

Transmit DMA event control register.

Return to [Summary Table](#)

**Table 3-1566. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_TX0       | 5028 0022h       |
| FSI_TX1       | 5028 1022h       |
| FSI_TX2       | 502A 0022h       |
| FSI_TX3       | 502A 1022h       |

**Figure 3-501. FSI\_TX\_CFG\_TX\_DMA\_CTRL Name Register**

|            |    |    |    |    |    |   |            |
|------------|----|----|----|----|----|---|------------|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8          |
| RESERVED_1 |    |    |    |    |    |   |            |
| R          |    |    |    |    |    |   |            |
| 0h         |    |    |    |    |    |   |            |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0          |
| RESERVED_1 |    |    |    |    |    |   | DMA_EVT_EN |
| R          |    |    |    |    |    |   | R/W        |
| 0h         |    |    |    |    |    |   | 0h         |

**Table 3-1568. FSI\_TX\_CFG\_TX\_DMA\_CTRL Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                      |
|------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:1 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                         |
| 0    | DMA_EVT_EN | R/W  | 0h    | <p>DMA Event Enable bit</p> <p>This bit will enable the DMA event to be generated upon the completion of a transmit frame.</p> <p>0h[R/W] = A DMA event will not be generated.</p> <p>1h[R/W] = A DMA event will be generated upon the completion of a transmitted frame.</p> <p>Note: The DMA event will only be generated for data frames.</p> |

### 3.10.2.15 FSI\_TX\_CFG\_TX\_LOCK\_CTRL Register

#### 1 FSI\_TX\_CFG\_TX\_LOCK\_CTRL Register (Offset = 24h) [reset = 0h]

Transmit lock control register.

Return to [Summary Table](#)

**Table 3-1569. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_TX0       | 5028 0024h       |
| FSI_TX1       | 5028 1024h       |
| FSI_TX2       | 502A 0024h       |
| FSI_TX3       | 502A 1024h       |

**Figure 3-502. FSI\_TX\_CFG\_TX\_LOCK\_CTRL Name Register**

|            |    |    |    |    |    |   |      |
|------------|----|----|----|----|----|---|------|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8    |
| KEY        |    |    |    |    |    |   |      |
| W          |    |    |    |    |    |   |      |
| 0h         |    |    |    |    |    |   |      |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0    |
| RESERVED_1 |    |    |    |    |    |   | LOCK |
| R          |    |    |    |    |    |   | R/W  |
| 0h         |    |    |    |    |    |   | 0h   |

**Table 3-1571. FSI\_TX\_CFG\_TX\_LOCK\_CTRL Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | KEY        | W    | 0h    | Write Key<br>In order to write to this register, 0xA5 must be written to this field at the same time. Otherwise, writes are ignored. The key is cleared immediately after Writing, so it must be written again for every change to this register.                                                                                                                                                                                                                                                                                                                                                            |
| 7:1  | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 0    | LOCK       | R/W  | 0h    | Control Register Lock Enable bit<br>This bit locks the contents of all the transmit control registers that support a lock protection. Once locked, further writes will not take effect until a SYSRS has reset this register. Once set, further writes to this bit will be ignored.<br>0h[R/W] = Transmit control registers can be modified and are not locked.<br>1h[R/W] = Transmit control registers are locked and cannot be modified until this bit is cleared by SYSRS. Any further writes to this bit are ignored.<br>Note: The KEY field must contain 0xA5 for any write to this bit to take effect. |



### 3.10.2.16 FSI\_TX\_CFG\_TX\_EVT\_STS Register

#### 1 FSI\_TX\_CFG\_TX\_EVT\_STS Register (Offset = 28h) [reset = 0h]

Transmit event and error status flag register.

Return to [Summary Table](#)

**Table 3-1572. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_TX0       | 5028 0028h       |
| FSI_TX1       | 5028 1028h       |
| FSI_TX2       | 502A 0028h       |
| FSI_TX3       | 502A 1028h       |

**Figure 3-503. FSI\_TX\_CFG\_TX\_EVT\_STS Name Register**

|            |    |    |    |                    |                 |                  |            |
|------------|----|----|----|--------------------|-----------------|------------------|------------|
| 15         | 14 | 13 | 12 | 11                 | 10              | 9                | 8          |
| RESERVED_1 |    |    |    |                    |                 |                  |            |
| R          |    |    |    |                    |                 |                  |            |
| 0h         |    |    |    |                    |                 |                  |            |
| 7          | 6  | 5  | 4  | 3                  | 2               | 1                | 0          |
| RESERVED_1 |    |    |    | PING_TRIGGE<br>RED | BUF_OVERRU<br>N | BUF_UNDERR<br>UN | FRAME_DONE |
| R          |    |    |    | R                  | R               | R                | R          |
| 0h         |    |    |    | 0h                 | 0h              | 0h               | 0h         |

**Table 3-1574. FSI\_TX\_CFG\_TX\_EVT\_STS Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:4 | RESERVED_1     | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 3    | PING_TRIGGERED | R    | 0h    | <p>Ping Frame Triggered Flag Bit</p> <p>This bit indicates that a ping frame has been triggered. This bit is set by hardware when either the ping timer or an external trigger event have occurred. Software can also force this bit to get set by Writing to the TX_EVT_FRC register.</p> <p>0h[R] = A ping frame has not been triggered.</p> <p>1h[R] = A ping frame has been triggered by either the ping timer or external trigger.</p> <p>To clear this bit, write to the corresponding bit in the TX_EVT_CLR register.</p> |
| 2    | BUF_OVERRUN    | R    | 0h    | <p>Buffer Overrun Flag Bit</p> <p>This bit indicates that buffer overrun has occurred. Software can also force this bit to get set by Writing to the TX_EVT_FRC register.</p> <p>0h[R] = Buffer Overrun has not occurred.</p> <p>1h[R] = Buffer Overrun has occurred.</p> <p>To clear this bit, write to the corresponding bit in the TX_EVT_CLR register.</p>                                                                                                                                                                   |
| 1    | BUF_UNDERRUN   | R    | 0h    | <p>Buffer Underrun Flag Bit</p> <p>This bit indicates that buffer underrun has occurred. Software can also force this bit to get set by Writing to the TX_EVT_FRC register.</p> <p>0h[R] = Buffer Underrun has not occurred.</p> <p>1h[R] = Buffer Underrun has occurred.</p> <p>To clear this bit, write to the corresponding bit in the TX_EVT_CLR register.</p>                                                                                                                                                               |

**Table 3-1574. FSI\_TX\_CFG\_TX\_EVT\_STS Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | FRAME_DONE | R    | 0h    | <p>Frame Done Flag Bit</p> <p>This bit indicates a Frame Done condition. This bit is set by hardware when a frame transmission has been completed. Software can also force this bit to get set by Writing to the TX_EVT_FRC register.</p> <p>0h[R] = Frame Done condition has not occurred.</p> <p>1h[R] = Frame Done condition has occurred.</p> <p>To clear this bit, write to the corresponding bit in the TX_EVT_CLR register.</p> |

### 3.10.2.17 FSI\_TX\_CFG\_TX\_EVT\_CLR Register

#### 1 FSI\_TX\_CFG\_TX\_EVT\_CLR Register (Offset = 2Ch) [reset = 0h]

Transmit event and error clear register.

Return to [Summary Table](#)

**Table 3-1575. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_TX0       | 5028 002Ch       |
| FSI_TX1       | 5028 102Ch       |
| FSI_TX2       | 502A 002Ch       |
| FSI_TX3       | 502A 102Ch       |

**Figure 3-504. FSI\_TX\_CFG\_TX\_EVT\_CLR Name Register**

|            |    |    |    |                |             |              |            |
|------------|----|----|----|----------------|-------------|--------------|------------|
| 15         | 14 | 13 | 12 | 11             | 10          | 9            | 8          |
| RESERVED_1 |    |    |    |                |             |              |            |
| R          |    |    |    |                |             |              |            |
| 0h         |    |    |    |                |             |              |            |
| 7          | 6  | 5  | 4  | 3              | 2           | 1            | 0          |
| RESERVED_1 |    |    |    | PING_TRIGGERED | BUF_OVERRUN | BUF_UNDERRUN | FRAME_DONE |
| R          |    |    |    | W              | W           | W            | W          |
| 0h         |    |    |    | 0h             | 0h          | 0h           | 0h         |

**Table 3-1577. FSI\_TX\_CFG\_TX\_EVT\_CLR Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|------|----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:4 | RESERVED_1     | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 3    | PING_TRIGGERED | W    | 0h    | Ping Frame Triggered Flag Clear bit<br>This bit clears the corresponding bit in the TX_EVT_STS register.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0.<br>Note: This bit may not always be cleared when Writing to the corresponding TX_EVT_CLR bit. If PING_TIMEOUT MODE is configured to be 0, a hardware ping timeout may occur when another frame is actively being transmitted. In this case, if this bit still shows as 1 after the clear bit is written then the ping frame has been triggered but not serviced. This bit does not indicate that the ping frame has been completely sent, only that it has been triggered by the timeout event. |
| 2    | BUF_OVERRUN    | W    | 0h    | Buffer Overrun Flag Clear bit<br>This bit clears the corresponding bit in the TX_EVT_STS register.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 1    | BUF_UNDERRUN   | W    | 0h    | Buffer Underrun Flag Clear bit<br>This bit clears the corresponding bit in the TX_EVT_STS register.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 0    | FRAME_DONE     | W    | 0h    | Frame Done Flag Clear bit<br>This bit clears the corresponding bit in the TX_EVT_STS register.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Writing a 1 to this bit will clear the corresponding bit in the TX_EVT_STS register to 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

### 3.10.2.18 FSI\_TX\_CFG\_TX\_EVT\_FRC Register

#### 1 FSI\_TX\_CFG\_TX\_EVT\_FRC Register (Offset = 2Eh) [reset = 0h]

Transmit event and error flag force register.

Return to [Summary Table](#)

**Table 3-1578. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_TX0       | 5028 002Eh       |
| FSI_TX1       | 5028 102Eh       |
| FSI_TX2       | 502A 002Eh       |
| FSI_TX3       | 502A 102Eh       |

**Figure 3-505. FSI\_TX\_CFG\_TX\_EVT\_FRC Name Register**

|            |    |    |    |                |             |              |            |
|------------|----|----|----|----------------|-------------|--------------|------------|
| 15         | 14 | 13 | 12 | 11             | 10          | 9            | 8          |
| RESERVED_1 |    |    |    |                |             |              |            |
| R          |    |    |    |                |             |              |            |
| 0h         |    |    |    |                |             |              |            |
| 7          | 6  | 5  | 4  | 3              | 2           | 1            | 0          |
| RESERVED_1 |    |    |    | PING_TRIGGERED | BUF_OVERRUN | BUF_UNDERRUN | FRAME_DONE |
| R          |    |    |    | W              | W           | W            | W          |
| 0h         |    |    |    | 0h             | 0h          | 0h           | 0h         |

**Table 3-1580. FSI\_TX\_CFG\_TX\_EVT\_FRC Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                         |
|------|----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:4 | RESERVED_1     | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                            |
| 3    | PING_TRIGGERED | W    | 0h    | Ping Frame Triggered Flag Force bit<br>This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Force the corresponding flag bit in the TX_EVT_STS Register. |
| 2    | BUF_OVERRUN    | W    | 0h    | Buffer Overrun Flag Force bit<br>This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR.<br>0h[R/W] = Writing a 0 to this bit will have no effect.<br>1h[R/W] = Force the corresponding flag bit in the TX_EVT_STS Register.   |
| 1    | BUF_UNDERRUN   | W    | 0h    | Buffer Underrun Flag Force bit<br>This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Force the corresponding flag bit in the TX_EVT_STS Register.      |
| 0    | FRAME_DONE     | W    | 0h    | Frame Done Flag Force bit<br>This bit will cause the corresponding bit in the TX_EVT_STS register to get set. The purpose of this register is to allow software to simulate the effect of the event and test the associated software/ISR.<br>0h[W] = Writing a 0 to this bit will have no effect.<br>1h[W] = Force the corresponding flag bit in the TX_EVT_STS Register.           |

### 3.10.2.19 FSI\_TX\_CFG\_TX\_USER\_CRC Register

#### 1 FSI\_TX\_CFG\_TX\_USER\_CRC Register (Offset = 30h) [reset = 0h]

Transmit user-defined CRC register.

Return to [Summary Table](#)

**Table 3-1581. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_TX0       | 5028 0030h       |
| FSI_TX1       | 5028 1030h       |
| FSI_TX2       | 502A 0030h       |
| FSI_TX3       | 502A 1030h       |

**Figure 3-506. FSI\_TX\_CFG\_TX\_USER\_CRC Name Register**

|            |    |    |    |    |    |   |   |
|------------|----|----|----|----|----|---|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED_1 |    |    |    |    |    |   |   |
| R          |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| USER_CRC   |    |    |    |    |    |   |   |
| R/W        |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |

**Table 3-1583. FSI\_TX\_CFG\_TX\_USER\_CRC Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                 |
|------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                    |
| 7:0  | USER_CRC   | R/W  | 0h    | User-defined CRC<br>This register contains the 8-bit CRC value to be transmitted in the next frame if the transmission is set for user-defined CRC option [TX_OPER_CTRL_LO.SW_CRC = 1]. This register is ignored if the hardware CRC generation is enabled. |

### 3.10.2.20 FSI\_TX\_CFG\_TX\_ECC\_DATA Register

#### 1 FSI\_TX\_CFG\_TX\_ECC\_DATA Register (Offset = 40h) [reset = 0h]

Transmit ECC data register.

Return to [Summary Table](#)

**Table 3-1584. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_TX0       | 5028 0040h       |
| FSI_TX1       | 5028 1040h       |
| FSI_TX2       | 502A 0040h       |
| FSI_TX3       | 502A 1040h       |

**Figure 3-507. FSI\_TX\_CFG\_TX\_ECC\_DATA Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DATA_HIGH |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DATA_HIGH |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DATA_LOW  |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DATA_LOW  |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 3-1586. FSI\_TX\_CFG\_TX\_ECC\_DATA Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                |
|-------|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | DATA_HIGH | R/W  | 0h    | Upper 16 bits of ECC Data<br>Writing to this bitfield will cause the ECC logic to compute the ECC[SEC-DED] the entire 32-bit register and update TX_ECC_VAL register with the results. Software should write to these 16 bits of the register in a 32-bit write when needing to compute ECC for 32-bits for the full TX_ECC_DATA register. |
| 15:0  | DATA_LOW  | R/W  | 0h    | Lower 16 bits of ECC Data<br>Writing to this bitfield will cause the ECC logic to compute the ECC[SEC-DED] for these 16 bits and update the TX_ECC_VAL register with the results. Software should write to these register bits as a 16-bit write when needing to compute ECC for 16-bits.                                                  |

### 3.10.2.21 FSI\_TX\_CFG\_TX\_ECC\_VAL Register

#### 1 FSI\_TX\_CFG\_TX\_ECC\_VAL Register (Offset = 44h) [reset = Ch]

Transmit ECC value register.

Return to [Summary Table](#)

**Table 3-1587. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_TX0       | 5028 0044h       |
| FSI_TX1       | 5028 1044h       |
| FSI_TX2       | 502A 0044h       |
| FSI_TX3       | 502A 1044h       |

**Figure 3-508. FSI\_TX\_CFG\_TX\_ECC\_VAL Name Register**

|            |         |    |    |    |    |   |   |
|------------|---------|----|----|----|----|---|---|
| 15         | 14      | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED_1 |         |    |    |    |    |   |   |
| R          |         |    |    |    |    |   |   |
| 0h         |         |    |    |    |    |   |   |
| 7          | 6       | 5  | 4  | 3  | 2  | 1 | 0 |
| RESERVED_1 | ECC_VAL |    |    |    |    |   |   |
| R          | R       |    |    |    |    |   |   |
| 0h         | Ch      |    |    |    |    |   |   |

**Table 3-1589. FSI\_TX\_CFG\_TX\_ECC\_VAL Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                  |
|------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 15:7 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                     |
| 6:0  | ECC_VAL    | R    | Ch    | Computed ECC Value<br>This field contains the ECC value computed using SEC-DED either for 16-bit or 32-bit data in the TX_ECC_DATA register. |

### 3.10.2.22 FSI\_TX\_CFG\_TX\_DLYLINE\_CTRL Register

#### 1 FSI\_TX\_CFG\_TX\_DLYLINE\_CTRL Register (Offset = 48h) [reset = 0h]

Transmit delay Line control register.

Return to [Summary Table](#)

**Table 3-1590. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| FSI_TX0       | 5028 0048h       |
| FSI_TX1       | 5028 1048h       |
| FSI_TX2       | 502A 0048h       |
| FSI_TX3       | 502A 1048h       |

**Figure 3-509. FSI\_TX\_CFG\_TX\_DLYLINE\_CTRL Name Register**

| 15         | 14       | 13 | 12        | 11 | 10 | 9        | 8 |
|------------|----------|----|-----------|----|----|----------|---|
| RESERVED_1 | TXD1_DLY |    |           |    |    | TXD0_DLY |   |
| R          | R/W      |    |           |    |    | R/W      |   |
| 0h         | 0h       |    |           |    |    | 0h       |   |
| 7          | 6        | 5  | 4         | 3  | 2  | 1        | 0 |
| TXD0_DLY   |          |    | TXCLK_DLY |    |    |          |   |
| R/W        |          |    | R/W       |    |    |          |   |
| 0h         |          |    | 0h        |    |    |          |   |

**Table 3-1592. FSI\_TX\_CFG\_TX\_DLYLINE\_CTRL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 14:10 | TXD1_DLY   | R/W  | 0h    | Delay Line Tap Select for TXD1<br>This bitfield selects the number of delay elements inserted into the TXD1 path from the pin boundary to the receiver core.<br>0h[R/W] Zero delay elements are included in the TXD1 path. TXD1 is taken directly from the pin.<br>1h[R/W] One delay element is included in the TXD1 path.<br>2h[R/W] Two delay elements are included in the TXD1 path.<br>...<br>1Fh [R/W] 31 delay elements are included in the TXD1 path, the maximum.        |
| 9:5   | TXD0_DLY   | R/W  | 0h    | Delay Line Tap Select for TXD0<br>This bitfield selects the number of delay elements inserted into the TXD0 path from the pin boundary to the receiver core.<br>0h[R/W] Zero delay elements are included in the TXD0 path. TXD0 is taken directly from the pin.<br>1h[R/W] One delay element is included in the TXD0 path.<br>2h[R/W] Two delay elements are included in the TXD0 path.<br>...<br>1Fh [R/W] 31 delay elements are included in the TXD0 path, the maximum.        |
| 4:0   | TXCLK_DLY  | R/W  | 0h    | Delay Line Tap Select for TXCLK<br>This bitfield selects the number of delay elements inserted into the TXCLK path from the pin boundary to the receiver core.<br>0h[R/W] Zero delay elements are included in the TXCLK path. TXCLK is taken directly from the pin.<br>1h[R/W] One delay element is included in the TXCLK path.<br>2h[R/W] Two delay elements are included in the TXCLK path.<br>...<br>1Fh [R/W] 31 delay elements are included in the TXCLK path, the maximum. |



### 3.10.2.23 FSI\_TX\_CFG\_TX\_BUF\_BASE\_j Register

#### 1 FSI\_TX\_CFG\_TX\_BUF\_BASE\_j Register (Offset = 80h + formula) [reset = 0h]

Base address for transmit buffer.

Return to [Summary Table](#)

Offset = (j \* 2h); where j = 0 to 15d

**Table 3-1593. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| FSI_TX0       | 5028 0080h + formula |
| FSI_TX1       | 5028 1080h + formula |
| FSI_TX2       | 502A 0080h + formula |
| FSI_TX3       | 502A 1080h + formula |

**Figure 3-510. FSI\_TX\_CFG\_TX\_BUF\_BASE\_j Name Register**

|              |    |    |    |    |    |   |   |
|--------------|----|----|----|----|----|---|---|
| 15           | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| BASE_ADDRESS |    |    |    |    |    |   |   |
| R/W          |    |    |    |    |    |   |   |
| 0h           |    |    |    |    |    |   |   |
| 7            | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| BASE_ADDRESS |    |    |    |    |    |   |   |
| R/W          |    |    |    |    |    |   |   |
| 0h           |    |    |    |    |    |   |   |

**Table 3-1595. FSI\_TX\_CFG\_TX\_BUF\_BASE\_j Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                                       |
|------|--------------|------|-------|-------------------------------------------------------------------------------------------------------------------|
| 15:0 | BASE_ADDRESS | R/W  | 0h    | Transmit Data Buffer Base Address<br>This is the base address of the 16-word data buffer used by the transmitter. |

## 3.11 OTTOCAL

### OTTOCAL

#### 3.11.1 OTTOCAL Summaries

#### OTTOCAL Summaries

**Table 3-1596. OTTOCAL Registers, Base Address=502E 0000h, Length=4096**

| Offset | Length | Register Name                   | OTTOCAL0 Physical Address | OTTOCAL1 Physical Address | OTTOCAL2 Physical Address |
|--------|--------|---------------------------------|---------------------------|---------------------------|---------------------------|
| 42h    | 16     | <a href="#">OTTOCAL_HRPWR</a>   | 502E 0042h                | 502E 1042h                | 502E 2042h                |
| 4Ch    | 16     | <a href="#">OTTOCAL_HRMSTEP</a> | 502E 004Ch                | 502E 104Ch                | 502E 204Ch                |

**Table 3-1597. OTTOCAL Registers, Base Address=502E 0000h, Length=4096**

| Offset | Length | Register Name                   | OTTOCAL3 Physical Address |
|--------|--------|---------------------------------|---------------------------|
| 42h    | 16     | <a href="#">OTTOCAL_HRPWR</a>   | 502E 3042h                |
| 4Ch    | 16     | <a href="#">OTTOCAL_HRMSTEP</a> | 502E 304Ch                |

#### 3.11.2 OTTOCAL Registers

#### OTTOCAL Registers

### 3.11.2.1 OTTOCAL\_HRPWR Register

#### 1 OTTOCAL\_HRPWR Register (Offset = 42h) [reset = 0h]

HRPWM Power Register

This register is only accessible on EPWM modules with HRPWM capabilities.

Return to [Summary Table](#)

**Table 3-1598. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| OTTOCAL0      | 502E 0042h       |
| OTTOCAL1      | 502E 1042h       |
| OTTOCAL2      | 502E 2042h       |
| OTTOCAL3      | 502E 3042h       |

**Figure 3-511. OTTOCAL\_HRPWR Name Register**

| 15       | 14         | 13     | 12     | 11       | 10      | 9      | 8 |
|----------|------------|--------|--------|----------|---------|--------|---|
| CALPWRON | RESERVED_1 |        |        |          |         | CALSEL |   |
| R/W      | R          |        |        |          |         | R/W    |   |
| 0h       | 0h         |        |        |          |         | 0h     |   |
| 7        | 6          | 5      | 4      | 3        | 2       | 1      | 0 |
| CALSEL   | TESTSEL    | CALSTS | CNTSEL | CALSTART | CALMODE |        |   |
| R/W      | R/W        | R      | R/W    | R/W      | R/W     |        |   |
| 0h       | 0h         | 0h     | 0h     | 0h       | 0h      | 0h     |   |

**Table 3-1600. OTTOCAL\_HRPWR Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                         |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | CALPWRON   | R/W  | 0h    | MEP Calibration Power Bits [only available on ePWM1]<br>0:Disables MEP calibration logic in the HRPWM and reduces power consumption.<br>1:Enables MEP calibration logic             |
| 14:10 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                            |
| 9:6   | CALSEL     | R/W  | 0h    | EPWM Delay Line Selection for Calibration:                                                                                                                                          |
| 5     | TESTSEL    | R/W  | 0h    | Test Mode Select Bit: This bit selects if a dummy delay is added in Oscillator Calibration mode to help reducing frequency when small delays are used:                              |
| 4     | CALSTS     | R    | 0h    | Calibration Status Bit: This bit, when set to 1, indicates that calibration is in progress. It is set to 0 when:                                                                    |
| 3     | CNTSEL     | R/W  | 0h    | Counter Select Bit: Functionality of this bit has changed. When HRCNT0 or HRCNT1 reaches 0xFFFF, both counters are frozen. This bit will have an effect on when calibration starts: |
| 2     | CALSTART   | R/W  | 0h    | Calibration Start/Stop Bit:                                                                                                                                                         |
| 1:0   | CALMODE    | R/W  | 0h    | Note: CALMODE bits in HRPWM Module. Not used here.                                                                                                                                  |

### 3.11.2.2 OTTOCAL\_HRMSTEP Register

#### 1 OTTOCAL\_HRMSTEP Register (Offset = 4Ch) [reset = 0h]

##### HRPWM MEP Step Register

This register is only accessible on EPWM modules with HRPWM capabilities. Only 16 bit accesses are allowed for this register. Debugger access in 32 bit mode may display incorrect values.

Return to [Summary Table](#)

**Table 3-1601. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| OTTOCAL0      | 502E 004Ch       |
| OTTOCAL1      | 502E 104Ch       |
| OTTOCAL2      | 502E 204Ch       |
| OTTOCAL3      | 502E 304Ch       |

**Figure 3-512. OTTOCAL\_HRMSTEP Name Register**

|            |    |    |    |    |    |   |   |
|------------|----|----|----|----|----|---|---|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED_1 |    |    |    |    |    |   |   |
| R          |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| HRMSTEP    |    |    |    |    |    |   |   |
| R/W        |    |    |    |    |    |   |   |
| 0h         |    |    |    |    |    |   |   |

**Table 3-1603. OTTOCAL\_HRMSTEP Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 7:0  | HRMSTEP    | R/W  | 0h    | High Resolution MEP Step<br>When auto-conversion is enabled [HRCNFG[AUTOCONV] = 1], This 8-bit field contains the MEP_ScaleFactor [number of MEP steps per coarse steps] used by the hardware to automatically convert the value in the CMPAHR, CMPBHR, DBFEDHR, DBREDHR, TBPHSHR, or TBPRDHR register to a scaled micro-edge delay on the high-resolution ePWM output. The value in this register is written by the SFO calibration software at the end of each calibration run. |

## 3.12 SDFM

### SDFM

#### 3.12.1 SDFM Summaries

#### SDFM Summaries

**Table 3-1604. SDFM Registers, Base Address=5026 8000h, Length=4096**

| Offset | Length | Register Name                    | SDFM0 Physical Address | SDFM1 Physical Address |
|--------|--------|----------------------------------|------------------------|------------------------|
| 0h     | 32     | <a href="#">SDFM_SDIFLG</a>      | 5026 8000h             | 5026 9000h             |
| 4h     | 32     | <a href="#">SDFM_SDIFLGCLR</a>   | 5026 8004h             | 5026 9004h             |
| 8h     | 16     | <a href="#">SDFM_SDCTL</a>       | 5026 8008h             | 5026 9008h             |
| Ch     | 16     | <a href="#">SDFM_SDMFILEN</a>    | 5026 800Ch             | 5026 900Ch             |
| Eh     | 16     | <a href="#">SDFM_SDSTATUS</a>    | 5026 800Eh             | 5026 900Eh             |
| 20h    | 16     | <a href="#">SDFM_SDCTLPARM1</a>  | 5026 8020h             | 5026 9020h             |
| 22h    | 16     | <a href="#">SDFM_SDDFPARM1</a>   | 5026 8022h             | 5026 9022h             |
| 24h    | 16     | <a href="#">SDFM_SDDPARM1</a>    | 5026 8024h             | 5026 9024h             |
| 26h    | 16     | <a href="#">SDFM_SDFLT1CMPH1</a> | 5026 8026h             | 5026 9026h             |
| 28h    | 16     | <a href="#">SDFM_SDFLT1CMPL1</a> | 5026 8028h             | 5026 9028h             |
| 2Ah    | 16     | <a href="#">SDFM_SDCPARM1</a>    | 5026 802Ah             | 5026 902Ah             |
| 2Ch    | 32     | <a href="#">SDFM_SDDATA1</a>     | 5026 802Ch             | 5026 902Ch             |
| 30h    | 32     | <a href="#">SDFM_SDDATFIFO1</a>  | 5026 8030h             | 5026 9030h             |
| 34h    | 16     | <a href="#">SDFM_SDCDATA1</a>    | 5026 8034h             | 5026 9034h             |
| 36h    | 16     | <a href="#">SDFM_SDFLT1CMPH2</a> | 5026 8036h             | 5026 9036h             |
| 38h    | 16     | <a href="#">SDFM_SDFLT1CMPHZ</a> | 5026 8038h             | 5026 9038h             |
| 3Ah    | 16     | <a href="#">SDFM_SDFIFOCTL1</a>  | 5026 803Ah             | 5026 903Ah             |
| 3Ch    | 16     | <a href="#">SDFM_SDSYNC1</a>     | 5026 803Ch             | 5026 903Ch             |
| 3Eh    | 16     | <a href="#">SDFM_SDFLT1CMPL2</a> | 5026 803Eh             | 5026 903Eh             |
| 40h    | 16     | <a href="#">SDFM_SDCTLPARM2</a>  | 5026 8040h             | 5026 9040h             |
| 42h    | 16     | <a href="#">SDFM_SDDFPARM2</a>   | 5026 8042h             | 5026 9042h             |
| 44h    | 16     | <a href="#">SDFM_SDDPARM2</a>    | 5026 8044h             | 5026 9044h             |
| 46h    | 16     | <a href="#">SDFM_SDFLT2CMPH1</a> | 5026 8046h             | 5026 9046h             |
| 48h    | 16     | <a href="#">SDFM_SDFLT2CMPL1</a> | 5026 8048h             | 5026 9048h             |
| 4Ah    | 16     | <a href="#">SDFM_SDCPARM2</a>    | 5026 804Ah             | 5026 904Ah             |
| 4Ch    | 32     | <a href="#">SDFM_SDDATA2</a>     | 5026 804Ch             | 5026 904Ch             |
| 50h    | 32     | <a href="#">SDFM_SDDATFIFO2</a>  | 5026 8050h             | 5026 9050h             |
| 54h    | 16     | <a href="#">SDFM_SDCDATA2</a>    | 5026 8054h             | 5026 9054h             |
| 56h    | 16     | <a href="#">SDFM_SDFLT2CMPH2</a> | 5026 8056h             | 5026 9056h             |
| 58h    | 16     | <a href="#">SDFM_SDFLT2CMPHZ</a> | 5026 8058h             | 5026 9058h             |
| 5Ah    | 16     | <a href="#">SDFM_SDFIFOCTL2</a>  | 5026 805Ah             | 5026 905Ah             |
| 5Ch    | 16     | <a href="#">SDFM_SDSYNC2</a>     | 5026 805Ch             | 5026 905Ch             |
| 5Eh    | 16     | <a href="#">SDFM_SDFLT2CMPL2</a> | 5026 805Eh             | 5026 905Eh             |
| 60h    | 16     | <a href="#">SDFM_SDCTLPARM3</a>  | 5026 8060h             | 5026 9060h             |
| 62h    | 16     | <a href="#">SDFM_SDDFPARM3</a>   | 5026 8062h             | 5026 9062h             |
| 64h    | 16     | <a href="#">SDFM_SDDPARM3</a>    | 5026 8064h             | 5026 9064h             |
| 66h    | 16     | <a href="#">SDFM_SDFLT3CMPH1</a> | 5026 8066h             | 5026 9066h             |
| 68h    | 16     | <a href="#">SDFM_SDFLT3CMPL1</a> | 5026 8068h             | 5026 9068h             |

**Table 3-1604. SDFM Registers, Base Address=5026 8000h, Length=4096 (continued)**

| Offset | Length | Register Name                             | SDFM0 Physical Address | SDFM1 Physical Address |
|--------|--------|-------------------------------------------|------------------------|------------------------|
| 6Ah    | 16     | <a href="#">SDFM_SDCPARM3</a>             | 5026 806Ah             | 5026 906Ah             |
| 6Ch    | 32     | <a href="#">SDFM_SDDATA3</a>              | 5026 806Ch             | 5026 906Ch             |
| 70h    | 32     | <a href="#">SDFM_SDDATFIFO3</a>           | 5026 8070h             | 5026 9070h             |
| 74h    | 16     | <a href="#">SDFM_SDCDATA3</a>             | 5026 8074h             | 5026 9074h             |
| 76h    | 16     | <a href="#">SDFM_SDFLT3CMPH2</a>          | 5026 8076h             | 5026 9076h             |
| 78h    | 16     | <a href="#">SDFM_SDFLT3CMPHZ</a>          | 5026 8078h             | 5026 9078h             |
| 7Ah    | 16     | <a href="#">SDFM_SDFIFOCTL3</a>           | 5026 807Ah             | 5026 907Ah             |
| 7Ch    | 16     | <a href="#">SDFM_SDSYNC3</a>              | 5026 807Ch             | 5026 907Ch             |
| 7Eh    | 16     | <a href="#">SDFM_SDFLT3CMPL2</a>          | 5026 807Eh             | 5026 907Eh             |
| 80h    | 16     | <a href="#">SDFM_SDCTLPARM4</a>           | 5026 8080h             | 5026 9080h             |
| 82h    | 16     | <a href="#">SDFM_SDDFPARM4</a>            | 5026 8082h             | 5026 9082h             |
| 84h    | 16     | <a href="#">SDFM_SDDPARM4</a>             | 5026 8084h             | 5026 9084h             |
| 86h    | 16     | <a href="#">SDFM_SDFLT4CMPH1</a>          | 5026 8086h             | 5026 9086h             |
| 88h    | 16     | <a href="#">SDFM_SDFLT4CMPL1</a>          | 5026 8088h             | 5026 9088h             |
| 8Ah    | 16     | <a href="#">SDFM_SDCPARM4</a>             | 5026 808Ah             | 5026 908Ah             |
| 8Ch    | 32     | <a href="#">SDFM_SDDATA4</a>              | 5026 808Ch             | 5026 908Ch             |
| 90h    | 32     | <a href="#">SDFM_SDDATFIFO4</a>           | 5026 8090h             | 5026 9090h             |
| 94h    | 16     | <a href="#">SDFM_SDCDATA4</a>             | 5026 8094h             | 5026 9094h             |
| 96h    | 16     | <a href="#">SDFM_SDFLT4CMPH2</a>          | 5026 8096h             | 5026 9096h             |
| 98h    | 16     | <a href="#">SDFM_SDFLT4CMPHZ</a>          | 5026 8098h             | 5026 9098h             |
| 9Ah    | 16     | <a href="#">SDFM_SDFIFOCTL4</a>           | 5026 809Ah             | 5026 909Ah             |
| 9Ch    | 16     | <a href="#">SDFM_SDSYNC4</a>              | 5026 809Ch             | 5026 909Ch             |
| 9Eh    | 16     | <a href="#">SDFM_SDFLT4CMPL2</a>          | 5026 809Eh             | 5026 909Eh             |
| C0h    | 16     | <a href="#">SDFM_SDCOMP1CTL</a>           | 5026 80C0h             | 5026 90C0h             |
| C2h    | 16     | <a href="#">SDFM_SDCOMP1EVT2FLTCTL</a>    | 5026 80C2h             | 5026 90C2h             |
| C4h    | 16     | <a href="#">SDFM_SDCOMP1EVT2FLTCLKCTL</a> | 5026 80C4h             | 5026 90C4h             |
| C6h    | 16     | <a href="#">SDFM_SDCOMP1EVT1FLTCTL</a>    | 5026 80C6h             | 5026 90C6h             |
| C8h    | 16     | <a href="#">SDFM_SDCOMP1EVT1FLTCLKCTL</a> | 5026 80C8h             | 5026 90C8h             |
| CEh    | 16     | <a href="#">SDFM_SDCOMP1LOCK</a>          | 5026 80CEh             | 5026 90CEh             |
| D0h    | 16     | <a href="#">SDFM_SDCOMP2CTL</a>           | 5026 80D0h             | 5026 90D0h             |
| D2h    | 16     | <a href="#">SDFM_SDCOMP2EVT2FLTCTL</a>    | 5026 80D2h             | 5026 90D2h             |
| D4h    | 16     | <a href="#">SDFM_SDCOMP2EVT2FLTCLKCTL</a> | 5026 80D4h             | 5026 90D4h             |
| D6h    | 16     | <a href="#">SDFM_SDCOMP2EVT1FLTCTL</a>    | 5026 80D6h             | 5026 90D6h             |
| D8h    | 16     | <a href="#">SDFM_SDCOMP2EVT1FLTCLKCTL</a> | 5026 80D8h             | 5026 90D8h             |
| DEh    | 16     | <a href="#">SDFM_SDCOMP2LOCK</a>          | 5026 80DEh             | 5026 90DEh             |
| E0h    | 16     | <a href="#">SDFM_SDCOMP3CTL</a>           | 5026 80E0h             | 5026 90E0h             |
| E2h    | 16     | <a href="#">SDFM_SDCOMP3EVT2FLTCTL</a>    | 5026 80E2h             | 5026 90E2h             |
| E4h    | 16     | <a href="#">SDFM_SDCOMP3EVT2FLTCLKCTL</a> | 5026 80E4h             | 5026 90E4h             |
| E6h    | 16     | <a href="#">SDFM_SDCOMP3EVT1FLTCTL</a>    | 5026 80E6h             | 5026 90E6h             |
| E8h    | 16     | <a href="#">SDFM_SDCOMP3EVT1FLTCLKCTL</a> | 5026 80E8h             | 5026 90E8h             |
| EEh    | 16     | <a href="#">SDFM_SDCOMP3LOCK</a>          | 5026 80EEh             | 5026 90EEh             |
| F0h    | 16     | <a href="#">SDFM_SDCOMP4CTL</a>           | 5026 80F0h             | 5026 90F0h             |
| F2h    | 16     | <a href="#">SDFM_SDCOMP4EVT2FLTCTL</a>    | 5026 80F2h             | 5026 90F2h             |
| F4h    | 16     | <a href="#">SDFM_SDCOMP4EVT2FLTCLKCTL</a> | 5026 80F4h             | 5026 90F4h             |
| F6h    | 16     | <a href="#">SDFM_SDCOMP4EVT1FLTCTL</a>    | 5026 80F6h             | 5026 90F6h             |

**Table 3-1604. SDFM Registers, Base Address=5026 8000h, Length=4096 (continued)**

| Offset | Length | Register Name                             | SDFM0 Physical Address | SDFM1 Physical Address |
|--------|--------|-------------------------------------------|------------------------|------------------------|
| F8h    | 16     | <a href="#">SDFM_SDCOMP4EVT1FLTCLKCTL</a> | 5026 80F8h             | 5026 90F8h             |
| FEh    | 16     | <a href="#">SDFM_SDCOMP4LOCK</a>          | 5026 80FEh             | 5026 90FEh             |

### 3.12.2 SDFM Registers

#### SDFM Registers

### 3.12.2.1 SDFM\_SDIFLG Register

#### 1 SDFM\_SDIFLG Register (Offset = 0h) [reset = 0h]

SD Interrupt Flag Register.

Return to [Summary Table](#)

**Table 3-1605. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8000h       |
| SDFM1         | 5026 9000h       |

**Figure 3-513. SDFM\_SDIFLG Name Register**

|                    |                    |                    |                    |                    |                    |                    |                    |
|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| 31                 | 30                 | 29                 | 28                 | 27                 | 26                 | 25                 | 24                 |
| MIF                | RESERVED_1         |                    |                    |                    |                    |                    |                    |
| R                  | R                  |                    |                    |                    |                    |                    |                    |
| 0h                 | 0h                 |                    |                    |                    |                    |                    |                    |
| 23                 | 22                 | 21                 | 20                 | 19                 | 18                 | 17                 | 16                 |
| SDFINT4            | SDFINT3            | SDFINT2            | SDFINT1            | SDFOVF4            | SDFOVF3            | SDFOVF2            | SDFOVF1            |
| R                  | R                  | R                  | R                  | R                  | R                  | R                  | R                  |
| 0h                 | 0h                 | 0h                 | 0h                 | 0h                 | 0h                 | 0h                 | 0h                 |
| 15                 | 14                 | 13                 | 12                 | 11                 | 10                 | 9                  | 8                  |
| AF4                | AF3                | AF2                | AF1                | MF4                | MF3                | MF2                | MF1                |
| R                  | R                  | R                  | R                  | R                  | R                  | R                  | R                  |
| 0h                 | 0h                 | 0h                 | 0h                 | 0h                 | 0h                 | 0h                 | 0h                 |
| 7                  | 6                  | 5                  | 4                  | 3                  | 2                  | 1                  | 0                  |
| FLT4_FLG_CE<br>VT2 | FLT4_FLG_CE<br>VT1 | FLT3_FLG_CE<br>VT2 | FLT3_FLG_CE<br>VT1 | FLT2_FLG_CE<br>VT2 | FLT2_FLG_CE<br>VT1 | FLT1_FLG_CE<br>VT2 | FLT1_FLG_CE<br>VT1 |
| R                  | R                  | R                  | R                  | R                  | R                  | R                  | R                  |
| 0h                 | 0h                 | 0h                 | 0h                 | 0h                 | 0h                 | 0h                 | 0h                 |

**Table 3-1607. SDFM\_SDIFLG Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                       |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | MIF        | R    | 0h    | Set whenever any "error" interrupt [MF1-4, IFL1-4, IFH1-4, SDFOVF1-4] is active                                                                   |
| 30:24 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                          |
| 23    | SDFINT4    | R    | 0h    | SDFIFO data ready interrupt for Ch4                                                                                                               |
| 22    | SDFINT3    | R    | 0h    | SDFIFO data ready interrupt for Ch3                                                                                                               |
| 21    | SDFINT2    | R    | 0h    | SDFIFO data ready interrupt for Ch2                                                                                                               |
| 20    | SDFINT1    | R    | 0h    | SDFIFO data ready interrupt for Ch1<br>0: SDFIFO data ready interrupt has NOT occurred<br>1: SDFIFO data ready interrupt has occurred             |
| 19    | SDFOVF4    | R    | 0h    | FIFO Overflow Flag for Ch4                                                                                                                        |
| 18    | SDFOVF3    | R    | 0h    | FIFO Overflow Flag for Ch3                                                                                                                        |
| 17    | SDFOVF2    | R    | 0h    | FIFO Overflow Flag for Ch2                                                                                                                        |
| 16    | SDFOVF1    | R    | 0h    | FIFO Overflow Flag for Ch1<br>0 - FIFO has not overflowed<br>1 - FIFO overflowed. # words received in FIFO ' FIFO depth [16],<br>NEW word is lost |
| 15    | AF4        | R    | 0h    | Acknowledge flag for Filter 4<br>0: No new data available for Filter [in non-FIFO mode]<br>1: New data available for Filter [in non-FIFO mode]    |



**Table 3-1607. SDFM\_SDIFLG Register Field Descriptions (continued)**

| Bit | Field           | Type | Reset | Description                                                                                                                                  |
|-----|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 14  | AF3             | R    | 0h    | Acknowledge flag for Filter 3<br>0:No new data available for Filter [in non-FIFO mode]<br>1:New data available for Filter [in non-FIFO mode] |
| 13  | AF2             | R    | 0h    | Acknowledge flag for Filter 2<br>0:No new data available for Filter [in non-FIFO mode]<br>1:New data available for Filter [in non-FIFO mode] |
| 12  | AF1             | R    | 0h    | Acknowledge flag for Filter 1<br>0:No new data available for Filter [in non-FIFO mode]<br>1:New data available for Filter [in non-FIFO mode] |
| 11  | MF4             | R    | 0h    | Modulator Failure for Filter 4<br>0:Modulator is operating normally for Filter<br>1:Modulator failure for Filter                             |
| 10  | MF3             | R    | 0h    | Modulator Failure for Filter 3<br>0:Modulator is operating normally for Filter<br>1:Modulator failure for Filter                             |
| 9   | MF2             | R    | 0h    | Modulator Failure for Filter 2<br>0:Modulator is operating normally for Filter<br>1:Modulator failure for Filter                             |
| 8   | MF1             | R    | 0h    | Modulator Failure for Filter 1<br>0:Modulator is operating normally for Filter<br>1:Modulator failure for Filter                             |
| 7   | FLT4_FLG_C EVT2 | R    | 0h    | CEVT2 Interrupt flag for filter4<br>0:CEVT2 event has not occurred<br>1:CEVT2 event has occurred                                             |
| 6   | FLT4_FLG_C EVT1 | R    | 0h    | CEVT1 Interrupt flag for filter4<br>0:CEVT1 event has not occurred<br>1:CEVT1 event has occurred                                             |
| 5   | FLT3_FLG_C EVT2 | R    | 0h    | CEVT2 Interrupt flag for filter3<br>0:CEVT2 event has not occurred<br>1:CEVT2 event has occurred                                             |
| 4   | FLT3_FLG_C EVT1 | R    | 0h    | CEVT1 Interrupt flag for filter3<br>0:CEVT1 event has not occurred<br>1:CEVT1 event has occurred                                             |
| 3   | FLT2_FLG_C EVT2 | R    | 0h    | CEVT2 Interrupt flag for filter2<br>0:CEVT2 event has not occurred<br>1:CEVT2 event has occurred                                             |
| 2   | FLT2_FLG_C EVT1 | R    | 0h    | CEVT1 Interrupt flag for filter2<br>0:CEVT1 event has not occurred<br>1:CEVT1 event has occurred                                             |
| 1   | FLT1_FLG_C EVT2 | R    | 0h    | CEVT2 Interrupt flag for filter1<br>0:CEVT2 event has not occurred<br>1:CEVT2 event has occurred                                             |
| 0   | FLT1_FLG_C EVT1 | R    | 0h    | CEVT1 Interrupt flag for filter1<br>0:CEVT1 event has not occurred<br>1:CEVT1 event has occurred                                             |

### 3.12.2.2 SDFM\_SDIFLGCLR Register

#### 1 SDFM\_SDIFLGCLR Register (Offset = 4h) [reset = 0h]

SD Module Interrupt Flag Clear Bits:

Writing a "1" will clear the respective flag bit in the SDIFLG register.

Writes of "0" are ignored.

Note: If user writes a "1" to clear a bit on the same cycle that the hardware is trying to set the bit to "1", then hardware has priority and the bit will not be cleared.

Return to [Summary Table](#)

**Table 3-1608. Instance Table**

| Instance Name | Physical Address  |
|---------------|-------------------|
| <b>SDFM0</b>  | <b>5026 8004h</b> |
| <b>SDFM1</b>  | <b>5026 9004h</b> |

**Figure 3-514. SDFM\_SDIFLGCLR Name Register**

|                    |                    |                    |                    |                    |                    |                    |                    |
|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| 31                 | 30                 | 29                 | 28                 | 27                 | 26                 | 25                 | 24                 |
| MIF                | RESERVED_1         |                    |                    |                    |                    |                    |                    |
| R/W1TS             | R                  |                    |                    |                    |                    |                    |                    |
| 0h                 | 0h                 |                    |                    |                    |                    |                    |                    |
| 23                 | 22                 | 21                 | 20                 | 19                 | 18                 | 17                 | 16                 |
| SDFINT4            | SDFINT3            | SDFINT2            | SDFINT1            | SDFOVF4            | SDFOVF3            | SDFOVF2            | SDFOVF1            |
| R/W1TS             | R/W1TS             | R/W1TS             | R/W1TS             | R/W1TS             | R/W1TS             | R/W1TS             | R/W1TS             |
| 0h                 | 0h                 | 0h                 | 0h                 | 0h                 | 0h                 | 0h                 | 0h                 |
| 15                 | 14                 | 13                 | 12                 | 11                 | 10                 | 9                  | 8                  |
| AF4                | AF3                | AF2                | AF1                | MF4                | MF3                | MF2                | MF1                |
| R/W1TS             | R/W1TS             | R/W1TS             | R/W1TS             | R/W1TS             | R/W1TS             | R/W1TS             | R/W1TS             |
| 0h                 | 0h                 | 0h                 | 0h                 | 0h                 | 0h                 | 0h                 | 0h                 |
| 7                  | 6                  | 5                  | 4                  | 3                  | 2                  | 1                  | 0                  |
| FLT4_FLG_CE<br>VT2 | FLT4_FLG_CE<br>VT1 | FLT3_FLG_CE<br>VT2 | FLT3_FLG_CE<br>VT1 | FLT2_FLG_CE<br>VT2 | FLT2_FLG_CE<br>VT1 | FLT1_FLG_CE<br>VT2 | FLT1_FLG_CE<br>VT1 |
| R/W1TS             | R/W1TS             | R/W1TS             | R/W1TS             | R/W1TS             | R/W1TS             | R/W1TS             | R/W1TS             |
| 0h                 | 0h                 | 0h                 | 0h                 | 0h                 | 0h                 | 0h                 | 0h                 |

**Table 3-1610. SDFM\_SDIFLGCLR Register Field Descriptions**

| Bit   | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                                                                               |
|-------|------------|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | MIF        | R/W1TS | 0h    | Flag-clear bit for SDFM Master Interrupt flag.<br>Writing a 1 to clear MIF flag in SDIFLG register<br>Writes of "0" are ignored.<br>Note: If the MIF flag is cleared and other Interrupts are still pending, MIF will again be set to 1 on the following SysClk cycle, and the INT output will be reasserted [pulsed low] |
| 30:24 | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                  |
| 23    | SDFINT4    | R/W1TS | 0h    | SDFIFO data ready Interrupt flag-clear bit for Ch4                                                                                                                                                                                                                                                                        |
| 22    | SDFINT3    | R/W1TS | 0h    | SDFIFO data ready Interrupt flag-clear bit for Ch3                                                                                                                                                                                                                                                                        |
| 21    | SDFINT2    | R/W1TS | 0h    | SDFIFO data ready Interrupt flag-clear bit for Ch2                                                                                                                                                                                                                                                                        |
| 20    | SDFINT1    | R/W1TS | 0h    | SDFIFO data ready Interrupt flag-clear bit for Ch1                                                                                                                                                                                                                                                                        |
| 19    | SDFOVF4    | R/W1TS | 0h    | SDFIFO overflow clear Ch4                                                                                                                                                                                                                                                                                                 |
| 18    | SDFOVF3    | R/W1TS | 0h    | SDFIFO overflow clear Ch3                                                                                                                                                                                                                                                                                                 |
| 17    | SDFOVF2    | R/W1TS | 0h    | SDFIFO overflow clear Ch2                                                                                                                                                                                                                                                                                                 |

**Table 3-1610. SDFM\_SDIFLGCLR Register Field Descriptions (continued)**

| Bit | Field          | Type   | Reset | Description                                      |
|-----|----------------|--------|-------|--------------------------------------------------|
| 16  | SDFFOVF1       | R/W1TS | 0h    | SDFIFO overflow clear Ch1                        |
| 15  | AF4            | R/W1TS | 0h    | Flag-clear bit for Acknowledge flag for Filter 4 |
| 14  | AF3            | R/W1TS | 0h    | Flag Clear bit for AF3                           |
| 13  | AF2            | R/W1TS | 0h    | Flag Clear bit for AF2                           |
| 12  | AF1            | R/W1TS | 0h    | Flag Clear bit for AF1                           |
| 11  | MF4            | R/W1TS | 0h    | Flag Clear bit for MF4                           |
| 10  | MF3            | R/W1TS | 0h    | Flag Clear bit for MF3                           |
| 9   | MF2            | R/W1TS | 0h    | Flag Clear bit for MF2                           |
| 8   | MF1            | R/W1TS | 0h    | Flag Clear bit for MF1                           |
| 7   | FLT4_FLG_CEVT2 | R/W1TS | 0h    | Flag Clear bit for FLT4_FLG_CEVT2                |
| 6   | FLT4_FLG_CEVT1 | R/W1TS | 0h    | Flag Clear bit for FLT4_FLG_CEVT1                |
| 5   | FLT3_FLG_CEVT2 | R/W1TS | 0h    | Flag Clear bit for FLT3_FLG_CEVT2                |
| 4   | FLT3_FLG_CEVT1 | R/W1TS | 0h    | Flag Clear bit for FLT3_FLG_CEVT1                |
| 3   | FLT2_FLG_CEVT2 | R/W1TS | 0h    | Flag Clear bit for FLT2_FLG_CEVT2                |
| 2   | FLT2_FLG_CEVT1 | R/W1TS | 0h    | Flag Clear bit for FLT2_FLG_CEVT1                |
| 1   | FLT1_FLG_CEVT2 | R/W1TS | 0h    | Flag Clear bit for FLT1_FLG_CEVT2                |
| 0   | FLT1_FLG_CEVT1 | R/W1TS | 0h    | Flag Clear bit for FLT1_FLG_CEVT1                |

### 3.12.2.3 SDFM\_SDCTL Register

#### 1 SDFM\_SDCTL Register (Offset = 8h) [reset = 0h]

SD Control Register.

Return to [Summary Table](#)

**Table 3-1611. Instance Table**

| Instance Name | Physical Address  |
|---------------|-------------------|
| <b>SDFM0</b>  | <b>5026 8008h</b> |
| <b>SDFM1</b>  | <b>5026 9008h</b> |

**Figure 3-515. SDFM\_SDCTL Name Register**

| 15         | 14         | 13  | 12         | 11     | 10     | 9      | 8      |
|------------|------------|-----|------------|--------|--------|--------|--------|
| RESERVED_3 | RESERVED_2 | MIE | RESERVED_1 |        |        |        |        |
| R          | R          | R/W | R          |        |        |        |        |
| 0h         | 0h         | 0h  | 0h         |        |        |        |        |
| 7          | 6          | 5   | 4          | 3      | 2      | 1      | 0      |
| RESERVED_1 |            |     |            | HZ4    | HZ3    | HZ2    | HZ1    |
| R          |            |     |            | R/W1TS | R/W1TS | R/W1TS | R/W1TS |
| 0h         |            |     |            | 0h     | 0h     | 0h     | 0h     |

**Table 3-1613. SDFM\_SDCTL Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                    |
|------|------------|--------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | RESERVED_3 | R      | 0h    | Reserved                                                                                                                                       |
| 14   | RESERVED_2 | R      | 0h    | Reserved                                                                                                                                       |
| 13   | MIE        | R/W    | 0h    | Master SDy_ERR interrupt enable<br>0:SDy_ERR Interrupt and interrupt flags are disabled<br>1:SDy_ERR Interrupt and interrupt flags are enabled |
| 12:4 | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                       |
| 3    | HZ4        | R/W1TS | 0h    | Flag Clear bit for HZ4                                                                                                                         |
| 2    | HZ3        | R/W1TS | 0h    | Flag Clear bit for HZ3                                                                                                                         |
| 1    | HZ2        | R/W1TS | 0h    | Flag Clear bit for HZ2                                                                                                                         |
| 0    | HZ1        | R/W1TS | 0h    | Flag Clear bit for HZ1                                                                                                                         |

### 3.12.2.4 SDFM\_SDMFILEN Register

#### 1 SDFM\_SDMFILEN Register (Offset = Ch) [reset = 0h]

SD Master Filter Enable.

Return to [Summary Table](#)

**Table 3-1614. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 800Ch       |
| SDFM1         | 5026 900Ch       |

**Figure 3-516. SDFM\_SDMFILEN Name Register**

| 15         | 14         | 13 | 12         | 11         | 10         | 9          | 8          |
|------------|------------|----|------------|------------|------------|------------|------------|
| RESERVED_7 |            |    | RESERVED_6 | MFE        | RESERVED_5 | RESERVED_4 | RESERVED_3 |
| R          |            |    | R          | R/W        | R          | R          | R          |
| 0h         |            |    | 0h         | 0h         | 0h         | 0h         | 0h         |
| 7          | 6          | 5  | 4          | 3          | 2          | 1          | 0          |
| RESERVED_3 | RESERVED_2 |    |            | RESERVED_1 |            |            |            |
| R          | R          |    |            | R          |            |            |            |
| 0h         | 0h         |    |            | 0h         |            |            |            |

**Table 3-1616. SDFM\_SDMFILEN Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                          |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | RESERVED_7 | R    | 0h    | Reserved                                                                                                                                                             |
| 12    | RESERVED_6 | R    | 0h    | Reserved                                                                                                                                                             |
| 11    | MFE        | R/W  | 0h    | Master Filter Enable<br>0:All the four data filter units of SDFM module are disabled. All FIFOs are cleared<br>1:Data filter units can be enabled if bit FEN is '1'. |
| 10    | RESERVED_5 | R    | 0h    | Reserved                                                                                                                                                             |
| 9     | RESERVED_4 | R    | 0h    | Reserved                                                                                                                                                             |
| 8:7   | RESERVED_3 | R    | 0h    | Reserved                                                                                                                                                             |
| 6:4   | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                             |
| 3:0   | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                             |

### 3.12.2.5 SDFM\_SDSTATUS Register

#### 1 SDFM\_SDSTATUS Register (Offset = Eh) [reset = 0h]

SD Status Register.

Return to [Summary Table](#)

**Table 3-1617. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 800Eh       |
| SDFM1         | 5026 900Eh       |

**Figure 3-517. SDFM\_SDSTATUS Name Register**

| 15         | 14         | 13         | 12         | 11         | 10         | 9          | 8          |
|------------|------------|------------|------------|------------|------------|------------|------------|
| RESERVED_9 | RESERVED_8 | RESERVED_7 | RESERVED_6 | RESERVED_5 | RESERVED_4 | RESERVED_3 | RESERVED_2 |
| R          | R          | R          | R          | R          | R          | R          | R          |
| 0h         | 0h         | 0h         | 0h         | 0h         | 0h         | 0h         | 0h         |
| 7          | 6          | 5          | 4          | 3          | 2          | 1          | 0          |
| RESERVED_1 |            |            |            | HZ4        | HZ3        | HZ2        | HZ1        |
| R          |            |            |            | R          | R          | R          | R          |
| 0h         |            |            |            | 0h         | 0h         | 0h         | 0h         |

**Table 3-1619. SDFM\_SDSTATUS Register Field Descriptions**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                         |
|-----|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | RESERVED_9 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                            |
| 14  | RESERVED_8 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                            |
| 13  | RESERVED_7 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                            |
| 12  | RESERVED_6 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                            |
| 11  | RESERVED_5 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                            |
| 10  | RESERVED_4 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                            |
| 9   | RESERVED_3 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                            |
| 8   | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                            |
| 7:4 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                            |
| 3   | HZ4        | R    | 0h    | High-level Threshold crossing [Z] flag Ch4<br>Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator IFHx flag, it does not have the ability to generate an interrupt.<br>0:Comparator filter output ' SDCMPHZ4.HLTZ<br>1:Comparator filter output '= SDCMPHZ4.HLTZ |
| 2   | HZ3        | R    | 0h    | High-level Threshold crossing [Z] flag Ch3<br>Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator IFHx flag, it does not have the ability to generate an interrupt.<br>0:Comparator filter output ' SDCMPHZ3.HLTZ<br>1:Comparator filter output '= SDCMPHZ3.HLTZ |
| 1   | HZ2        | R    | 0h    | High-level Threshold crossing [Z] flag Ch2<br>Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator IFHx flag, it does not have the ability to generate an interrupt.<br>0:Comparator filter output ' SDCMPHZ2.HLTZ<br>1:Comparator filter output '= SDCMPHZ2.HLTZ |

**Table 3-1619. SDFM\_SDSTATUS Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                         |
|-----|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | HZ1   | R    | 0h    | High-level Threshold crossing [Z] flag Ch1<br>Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator IFHx flag, it does not have the ability to generate an interrupt.<br>0:Comparator filter output ' SDCMPHZ1.HLTZ<br>1:Comparator filter output '= SDCMPHZ1.HLTZ |

### 3.12.2.6 SDFM\_SDCTLPARM1 Register

#### 1 SDFM\_SDCTLPARM1 Register (Offset = 20h) [reset = 0h]

Control Parameter Register for Ch1.

Return to [Summary Table](#)

**Table 3-1620. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8020h       |
| SDFM1         | 5026 9020h       |

**Figure 3-518. SDFM\_SDCTLPARM1 Name Register**

|            |            |            |           |          |            |     |   |
|------------|------------|------------|-----------|----------|------------|-----|---|
| 15         | 14         | 13         | 12        | 11       | 10         | 9   | 8 |
| RESERVED_4 |            |            |           |          |            |     |   |
| R          |            |            |           |          |            |     |   |
| 0h         |            |            |           |          |            |     |   |
| 7          | 6          | 5          | 4         | 3        | 2          | 1   | 0 |
| RESERVED_3 | SDDATASYNC | RESERVED_2 | SDCLKSYNC | SDCLKSEL | RESERVED_1 | MOD |   |
| R          | R/W        | R          | R/W       | R/W      | R/W        | R/W |   |
| 0h         | 0h         | 0h         | 0h        | 0h       | 0h         | 0h  |   |

**Table 3-1622. SDFM\_SDCTLPARM1 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                           |
|------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED_4 | R    | 0h    | Reserved                                                                                                                              |
| 7    | RESERVED_3 | R    | 0h    | Reserved                                                                                                                              |
| 6    | SDDATASYNC | R/W  | 0h    | 0: SD Data is not passed through a synchronizer.<br>1:SD Data is passed through a synchronizer.                                       |
| 5    | RESERVED_2 | R    | 0h    | Reserved                                                                                                                              |
| 4    | SDCLKSYNC  | R/W  | 0h    | 0: SD Clock is not passed through a synchronizer.<br>1:SD Clock is passed through a synchronizer.                                     |
| 3    | SDCLKSEL   | R/W  | 0h    | SD1 Clock source select.<br>0:Clock source to SDFM filter is its channel clock.<br>1:Clock source to SDFM filter is SD1 filter clock. |
| 2    | RESERVED_1 | R/W  | 0h    | Reserved                                                                                                                              |
| 1:0  | MOD        | R/W  | 0h    | Modulator clock modes<br>0:Mode<br>0:Modulator clock running at 1x data rate<br>1:Reserved<br>2:Reserved<br>3:Reserved                |



### 3.12.2.7 SDFM\_SDDFPARM1 Register

#### 1 SDFM\_SDDFPARM1 Register (Offset = 22h) [reset = 0h]

Data Filter Parameter Register for Ch1.

Return to [Summary Table](#)

**Table 3-1623. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8022h       |
| SDFM1         | 5026 9022h       |

**Figure 3-519. SDFM\_SDDFPARM1 Name Register**

|            |    |    |          |     |    |     |     |
|------------|----|----|----------|-----|----|-----|-----|
| 15         | 14 | 13 | 12       | 11  | 10 | 9   | 8   |
| RESERVED_1 |    |    | SDSYNCEN | SST |    | AE  | FEN |
| R          |    |    | R/W      | R/W |    | R/W | R/W |
| 0h         |    |    | 0h       | 0h  |    | 0h  | 0h  |
| 7          | 6  | 5  | 4        | 3   | 2  | 1   | 0   |
| DOSR       |    |    |          |     |    |     |     |
| R/W        |    |    |          |     |    |     |     |
| 0h         |    |    |          |     |    |     |     |

**Table 3-1625. SDFM\_SDDFPARM1 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                       |
|-------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                          |
| 12    | SDSYNCEN   | R/W  | 0h    | PWM synchronization [SDSYNC] of data filter<br>0:PWM synchronization of data filter is disabled<br>1:PWM synchronization of data filter is enabled<br>Note: SDSYNCS.SYNCSEL bits define which PWM signal is used to synchronize PWMs                                              |
| 11:10 | SST        | R/W  | 0h    | Data filter structure<br>00:Data filter runs with a Sincfast structure<br>01:Data filter runs with a Sinc1 structure<br>10:Data filter runs with a Sinc2 structure<br>11:Data filter runs with a Sinc3 structure                                                                  |
| 9     | AE         | R/W  | 0h    | Data filter Acknowledge Enable<br>0:Acknowledge flag is disabled for the particular filter<br>1:Acknowledge flag is enabled for the particular filter                                                                                                                             |
| 8     | FEN        | R/W  | 0h    | Filter Enable<br>0: The data filter is disabled and no data is produced<br>1: The data filter is enabled and data are produced in the data filter<br>Note: When filter is disabled, DOSR counter held in reset, filter data erased. Also resets FIFO pointers and clears the FIFO |
| 7:0   | DOSR       | R/W  | 0h    | Data filter Oversampling ratio<br>The actual oversampling ratio of data filter is DOSR + 1<br>These bits set the oversampling ratio of the data filter.<br>0x0FF represents an oversampling ratio of 256.                                                                         |

### 3.12.2.8 SDFM\_SDDPARM1 Register

#### 1 SDFM\_SDDPARM1 Register (Offset = 24h) [reset = 0h]

Data Parameter Register for Ch1.

Return to [Summary Table](#)

**Table 3-1626. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8024h       |
| SDFM1         | 5026 9024h       |

**Figure 3-520. SDFM\_SDDPARM1 Name Register**

|    |    |     |    |    |     |   |            |
|----|----|-----|----|----|-----|---|------------|
| 15 | 14 | 13  | 12 | 11 | 10  | 9 | 8          |
|    |    | SH  |    |    | DR  |   | RESERVED_1 |
|    |    | R/W |    |    | R/W |   | R          |
|    |    | 0h  |    |    | 0h  |   | 0h         |
| 7  | 6  | 5   | 4  | 3  | 2   | 1 | 0          |
|    |    |     |    |    |     |   | RESERVED_1 |
|    |    |     |    |    |     |   | R          |
|    |    |     |    |    |     |   | 0h         |

**Table 3-1628. SDFM\_SDDPARM1 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                      |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | SH         | R/W  | 0h    | Shift Control<br>These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen. |
| 10    | DR         | R/W  | 0h    | Data filter Data representation<br>0:Data stored in<br>16b2's complement<br>1:Data stored in<br>32b2's complement                |
| 9:0   | RESERVED_1 | R    | 0h    | Reserved                                                                                                                         |

### 3.12.2.9 SDFM\_SDFLT1CMPH1 Register

#### 1 SDFM\_SDFLT1CMPH1 Register (Offset = 26h) [reset = 7FFFh]

High-level Threshold Register for Ch1.

Return to [Summary Table](#)

**Table 3-1629. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8026h       |
| SDFM1         | 5026 9026h       |

**Figure 3-521. SDFM\_SDFLT1CMPH1 Name Register**

|            |       |    |    |    |    |   |   |
|------------|-------|----|----|----|----|---|---|
| 15         | 14    | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED_1 | HLT   |    |    |    |    |   |   |
| R          | R/W   |    |    |    |    |   |   |
| 0h         | 7FFFh |    |    |    |    |   |   |
| 7          | 6     | 5  | 4  | 3  | 2  | 1 | 0 |
| HLT        |       |    |    |    |    |   |   |
| R/W        |       |    |    |    |    |   |   |
| 7FFFh      |       |    |    |    |    |   |   |

**Table 3-1631. SDFM\_SDFLT1CMPH1 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                     |
|------|------------|------|-------|-----------------------------------------------------------------|
| 15   | RESERVED_1 | R    | 0h    | Reserved                                                        |
| 14:0 | HLT        | R/W  | 7FFFh | Unsigned high-level threshold for the comparator filter output. |

### 3.12.2.10 SDFM\_SDFLT1CMPL1 Register

#### 1 SDFM\_SDFLT1CMPL1 Register (Offset = 28h) [reset = 0h]

Low-level Threshold Register for Ch1.

Return to [Summary Table](#)

**Table 3-1632. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8028h       |
| SDFM1         | 5026 9028h       |

**Figure 3-522. SDFM\_SDFLT1CMPL1 Name Register**

|            |     |    |    |    |    |   |   |
|------------|-----|----|----|----|----|---|---|
| 15         | 14  | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED_1 | LLT |    |    |    |    |   |   |
| R          | R/W |    |    |    |    |   |   |
| 0h         | 0h  |    |    |    |    |   |   |
| 7          | 6   | 5  | 4  | 3  | 2  | 1 | 0 |
| LLT        |     |    |    |    |    |   |   |
| R/W        |     |    |    |    |    |   |   |
| 0h         |     |    |    |    |    |   |   |

**Table 3-1634. SDFM\_SDFLT1CMPL1 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                    |
|------|------------|------|-------|----------------------------------------------------------------|
| 15   | RESERVED_1 | R    | 0h    | Reserved                                                       |
| 14:0 | LLT        | R/W  | 0h    | Unsigned low-level threshold for the comparator filter output. |

### 3.12.2.11 SDFM\_SDCPARM1 Register

#### 1 SDFM\_SDCPARM1 Register (Offset = 2Ah) [reset = 0h]

Comparator Filter Parameter Register for Ch1.

Return to [Summary Table](#)

**Table 3-1635. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 802Ah       |
| SDFM1         | 5026 902Ah       |

**Figure 3-523. SDFM\_SDCPARM1 Name Register**

|          |          |          |          |    |      |      |         |
|----------|----------|----------|----------|----|------|------|---------|
| 15       | 14       | 13       | 12       | 11 | 10   | 9    | 8       |
| CEVT2SEL |          | CEN      | CEVT1SEL |    | HZEN | MFIE | CS1_CS0 |
| R/W      |          | R/W      | R/W      |    | R/W  | R/W  | R/W     |
| 0h       |          | 0h       | 0h       |    | 0h   | 0h   | 0h      |
| 7        | 6        | 5        | 4        | 3  | 2    | 1    | 0       |
| CS1_CS0  | EN_CEVT2 | EN_CEVT1 |          |    | COSR |      |         |
| R/W      | R/W      | R/W      |          |    | R/W  |      |         |
| 0h       | 0h       | 0h       |          |    | 0h   |      |         |

**Table 3-1637. SDFM\_SDCPARM1 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                    |
|-------|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | CEVT2SEL | R/W  | 0h    | Comparator Event2 Select<br>00: COMPL1<br>01:COMPL1 OR COMPH1<br>10:COMPL2<br>11:COMPL2 OR COMPH2                                                                                                                                              |
| 13    | CEN      | R/W  | 0h    | Comparator Filter enable<br>0:Disable comparator filter<br>1:Enable comparator filter                                                                                                                                                          |
| 12:11 | CEVT1SEL | R/W  | 0h    | Comparator Event1 Select<br>00: COMPH1<br>01:COMPL1 OR COMPH1<br>10:COMPH2<br>11:COMPL2 OR COMPH2                                                                                                                                              |
| 10    | HZEN     | R/W  | 0h    | High level [Z] Threshold crossing output enable<br>0:Disable Higher level Threshold [Z] crossing<br>1:Enable Higher level Threshold [Z] crossing                                                                                               |
| 9     | MFIE     | R/W  | 0h    | Modulator Failure Interrupt Enable<br>0:Disable modulator failure interrupt and its flag<br>1:Enable modulator failure interrupt and its flag                                                                                                  |
| 8:7   | CS1_CS0  | R/W  | 0h    | Comparator filter structure<br>00:Comparator filter runs with a sincfast structure<br>01:Comparator filter runs with a Sinc1 structure<br>10:Comparator filter runs with a Sinc2 structure<br>11:Comparator filter runs with a Sinc3 structure |
| 6     | EN_CEVT2 | R/W  | 0h    | CEVT2 interrupt enable<br>0:Disable CEVT2 interrupt<br>1:Enable CEVT2 interrupt                                                                                                                                                                |
| 5     | EN_CEVT1 | R/W  | 0h    | CEVT1 interrupt enable<br>0:Disable CEVT1 interrupt<br>1:Enable CEVT1 interrupt                                                                                                                                                                |

**Table 3-1637. SDFM\_SDCPARM1 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                           |
|-----|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | COSR  | R/W  | 0h    | Comparator Oversampling ratio.<br>The actual rate is COSR + 1.<br>These bits set the oversampling ratio of the filter.<br>0x1F represents an oversampling ratio of 32 |

### 3.12.2.12 SDFM\_SDDATA1 Register

#### 1 SDFM\_SDDATA1 Register (Offset = 2Ch) [reset = 0h]

Data Filter Data Register (16 or 32bit) for Ch1.

Return to [Summary Table](#)

**Table 3-1638. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 802Ch       |
| SDFM1         | 5026 902Ch       |

**Figure 3-524. SDFM\_SDDATA1 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DATA32HI |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DATA32HI |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DATA16   |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DATA16   |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 3-1640. SDFM\_SDDATA1 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                             |
|-------|----------|------|-------|---------------------------------------------------------|
| 31:16 | DATA32HI | R    | 0h    | Hi-order<br>16bin<br>32bmode, 16-bit Data in<br>16bmode |
| 15:0  | DATA16   | R    | 0h    | Lo-order<br>16bin<br>32bmode                            |

### 3.12.2.13 SDFM\_SDDATFIFO1 Register

#### 1 SDFM\_SDDATFIFO1 Register (Offset = 30h) [reset = 0h]

Filter Data FIFO Output(32b) for Ch1.

Return to [Summary Table](#)

**Table 3-1641. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8030h       |
| SDFM1         | 5026 9030h       |

**Figure 3-525. SDFM\_SDDATFIFO1 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DATA32HI |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DATA32HI |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DATA16   |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DATA16   |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 3-1643. SDFM\_SDDATFIFO1 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                             |
|-------|----------|------|-------|---------------------------------------------------------|
| 31:16 | DATA32HI | R    | 0h    | Hi-order<br>16bin<br>32bmode, 16-bit Data in<br>16bmode |
| 15:0  | DATA16   | R    | 0h    | Lo-order<br>16bin<br>32bmode                            |



### 3.12.2.14 SDFM\_SDCDATA1 Register

#### 1 SDFM\_SDCDATA1 Register (Offset = 34h) [reset = 0h]

Comparator Filter Data Register (16b) for Ch1.

Return to [Summary Table](#)

**Table 3-1644. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8034h       |
| SDFM1         | 5026 9034h       |

**Figure 3-526. SDFM\_SDCDATA1 Name Register**

|        |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DATA16 |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |
| 7      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| DATA16 |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |

**Table 3-1646. SDFM\_SDCDATA1 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                      |
|------|--------|------|-------|----------------------------------|
| 15:0 | DATA16 | R    | 0h    | Comparator Data output - 16bonly |

### 3.12.2.15 SDFM\_SDFLT1CMPH2 Register

#### 1 SDFM\_SDFLT1CMPH2 Register (Offset = 36h) [reset = 7FFFh]

Second high level threshold for CH1.

Return to [Summary Table](#)

**Table 3-1647. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8036h       |
| SDFM1         | 5026 9036h       |

**Figure 3-527. SDFM\_SDFLT1CMPH2 Name Register**

|            |       |    |    |    |    |   |   |
|------------|-------|----|----|----|----|---|---|
| 15         | 14    | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED_1 | HLT2  |    |    |    |    |   |   |
| R          | R/W   |    |    |    |    |   |   |
| 0h         | 7FFFh |    |    |    |    |   |   |
| 7          | 6     | 5  | 4  | 3  | 2  | 1 | 0 |
| HLT2       |       |    |    |    |    |   |   |
| R/W        |       |    |    |    |    |   |   |
| 7FFFh      |       |    |    |    |    |   |   |

**Table 3-1649. SDFM\_SDFLT1CMPH2 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                            |
|------|------------|------|-------|------------------------------------------------------------------------|
| 15   | RESERVED_1 | R    | 0h    | Reserved                                                               |
| 14:0 | HLT2       | R/W  | 7FFFh | Second Unsigned high-level threshold for the comparator filter output. |

### 3.12.2.16 SDFM\_SDFLT1CMPHZ Register

#### 1 SDFM\_SDFLT1CMPHZ Register (Offset = 38h) [reset = 0h]

High-level (Z) Threshold Register for Ch1.

Return to [Summary Table](#)

**Table 3-1650. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8038h       |
| SDFM1         | 5026 9038h       |

**Figure 3-528. SDFM\_SDFLT1CMPHZ Name Register**

|            |      |    |    |    |    |   |   |
|------------|------|----|----|----|----|---|---|
| 15         | 14   | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED_1 | HLTZ |    |    |    |    |   |   |
| R          | R/W  |    |    |    |    |   |   |
| 0h         | 0h   |    |    |    |    |   |   |
| 7          | 6    | 5  | 4  | 3  | 2  | 1 | 0 |
| HLTZ       |      |    |    |    |    |   |   |
| R/W        |      |    |    |    |    |   |   |
| 0h         |      |    |    |    |    |   |   |

**Table 3-1652. SDFM\_SDFLT1CMPHZ Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                |
|------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                   |
| 14:0 | HLTZ       | R/W  | 0h    | Unsigned High-level threshold [Z] for the comparator filter output. Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator SDCMPHx, it does not have the ability to generate an interrupt. |

### 3.12.2.17 SDFM\_SDFIFOCTL1 Register

#### 1 SDFM\_SDFIFOCTL1 Register (Offset = 3Ah) [reset = 0h]

FIFO Control Register for Ch1.

Return to [Summary Table](#)

**Table 3-1653. Instance Table**

| Instance Name | Physical Address  |
|---------------|-------------------|
| <b>SDFM0</b>  | <b>5026 803Ah</b> |
| <b>SDFM1</b>  | <b>5026 903Ah</b> |

**Figure 3-529. SDFM\_SDFIFOCTL1 Name Register**

|        |          |            |        |            |        |   |   |
|--------|----------|------------|--------|------------|--------|---|---|
| 15     | 14       | 13         | 12     | 11         | 10     | 9 | 8 |
| OVFIEN | DRINTSEL | FFEN       | FFIEN  | RESERVED_2 | SDFFST |   |   |
| R/W    | R/W      | R/W        | R/W    | R          | R      |   |   |
| 0h     | 0h       | 0h         | 0h     | 0h         | 0h     |   |   |
| 7      | 6        | 5          | 4      | 3          | 2      | 1 | 0 |
| SDFFST |          | RESERVED_1 | SDFFIL |            |        |   |   |
| R      |          | R          | R/W    |            |        |   |   |
| 0h     |          | 0h         | 0h     |            |        |   |   |

**Table 3-1655. SDFM\_SDFIFOCTL1 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                       |
|------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | OVFIEN     | R/W  | 0h    | SDFIFO Overflow interrupt enable<br>0: SDFIFO Overflow condition will not generate an interrupt<br>1: SDFIFO overflow condition generates an interrupt on SDy_ERR |
| 14   | DRINTSEL   | R/W  | 0h    | Data-Ready Interrupt [DRINT] source select<br>0 = AF1 [Select non-FIFO data-ready interrupt]<br>1 = SDFINT1 [Select FIFO data-ready interrupt]                    |
| 13   | FFEN       | R/W  | 0h    | SDFIFO Enable<br>0: Disable FIFO operation<br>1: Enable FIFO operation<br>Note: When FIFO is disabled, FIFO contents are cleared                                  |
| 12   | FFIEN      | R/W  | 0h    | SDFIFO data ready Interrupt Enable                                                                                                                                |
| 11   | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                          |
| 10:6 | SDFFST     | R    | 0h    | SDFIFO Status<br>00000 FIFO empty<br>00001 FIFO has 1 word<br>.....<br>10000 FIFO has 16 words                                                                    |
| 5    | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                          |
| 4:0  | SDFFIL     | R/W  | 0h    | SDFIFO interrupt level bits<br>The FIFO will generate an interrupt when the FIFO status [SDFFST] != FIFO level [SDFFIL]                                           |

### 3.12.2.18 SDFM\_SDSYNC1 Register

#### 1 SDFM\_SDSYNC1 Register (Offset = 3Ch) [reset = 400h]

SD Filter Sync control for Ch1.

Return to [Summary Table](#)

**Table 3-1656. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 803Ch       |
| SDFM1         | 5026 903Ch       |

**Figure 3-530. SDFM\_SDSYNC1 Name Register**

| 15         | 14       | 13      | 12 | 11 | 10       | 9           | 8        |
|------------|----------|---------|----|----|----------|-------------|----------|
| RESERVED_1 |          |         |    |    | WTSCLREN | FFSYNCCLREN | WTSYNCLR |
| R          |          |         |    |    | R/W      | R/W         | R/W      |
| 0h         |          |         |    |    | 1h       | 0h          | 0h       |
| 7          | 6        | 5       | 4  | 3  | 2        | 1           | 0        |
| WTSYNFLG   | WTSYNCEN | SYNCSEL |    |    |          |             |          |
| R          | R/W      | R/W     |    |    |          |             |          |
| 0h         | 0h       | 0h      |    |    |          |             |          |

**Table 3-1658. SDFM\_SDSYNC1 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                              |
|-------|-------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | RESERVED_1  | R    | 0h    | Reserved                                                                                                                                                                 |
| 10    | WTSCLREN    | R/W  | 1h    | WTSYNFLG Clear-on-FIFOINT Enable<br>0:WTSYNFLG can only be cleared manually [using WTSYNCLR bit]<br>1:WTSYNFLG is cleared automatically on SDFINT                        |
| 9     | FFSYNCCLREN | R/W  | 0h    | FIFO Clear-on-SDSYNC Enable<br>0:SDFIFO is not automatically cleared upon receiving SDSYNC<br>1:SDFIFO is automatically cleared upon receiving SDSYNC                    |
| 8     | WTSYNCLR    | R/W  | 0h    | Wait-for-Sync Flag Clear [always reads 0]<br>0:Write of 0 has no effect<br>1:Write of 1 clears WTSYNFLG                                                                  |
| 7     | WTSYNFLG    | R    | 0h    | Wait-for-Sync Flag<br>0:SDSYNC event has not occurred<br>1:SDSYNC event occurred.                                                                                        |
| 6     | WTSYNCEN    | R/W  | 0h    | Wait-for-Sync Enable<br>0:Incoming Data written to SDFIFO on every Data-Ready [DR] Event<br>1:Incoming Data written to SDFIFO on DR event only after SDSYNC event occurs |
| 5:0   | SYNCSEL     | R/W  | 0h    | Defines source for the SDSYNC Input on this channel<br>Refer SDSYNcx.SYNCSEL table                                                                                       |

### 3.12.2.19 SDFM\_SDFLT1CMPL2 Register

#### 1 SDFM\_SDFLT1CMPL2 Register (Offset = 3Eh) [reset = 0h]

Second low level threshold for CH1.

Return to [Summary Table](#)

**Table 3-1659. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 803Eh       |
| SDFM1         | 5026 903Eh       |

**Figure 3-531. SDFM\_SDFLT1CMPL2 Name Register**

|            |      |    |    |    |    |   |   |
|------------|------|----|----|----|----|---|---|
| 15         | 14   | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED_1 | LLT2 |    |    |    |    |   |   |
| R          | R/W  |    |    |    |    |   |   |
| 0h         | 0h   |    |    |    |    |   |   |
| 7          | 6    | 5  | 4  | 3  | 2  | 1 | 0 |
| LLT2       |      |    |    |    |    |   |   |
| R/W        |      |    |    |    |    |   |   |
| 0h         |      |    |    |    |    |   |   |

**Table 3-1661. SDFM\_SDFLT1CMPL2 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                           |
|------|------------|------|-------|-----------------------------------------------------------------------|
| 15   | RESERVED_1 | R    | 0h    | Reserved                                                              |
| 14:0 | LLT2       | R/W  | 0h    | Second Unsigned low-level threshold for the comparator filter output. |

### 3.12.2.20 SDFM\_SDCTLPARM2 Register

#### 1 SDFM\_SDCTLPARM2 Register (Offset = 40h) [reset = 0h]

Control Parameter Register for Ch2.

Return to [Summary Table](#)

**Table 3-1662. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8040h       |
| SDFM1         | 5026 9040h       |

**Figure 3-532. SDFM\_SDCTLPARM2 Name Register**

|            |            |            |           |          |            |     |   |
|------------|------------|------------|-----------|----------|------------|-----|---|
| 15         | 14         | 13         | 12        | 11       | 10         | 9   | 8 |
| RESERVED_4 |            |            |           |          |            |     |   |
| R          |            |            |           |          |            |     |   |
| 0h         |            |            |           |          |            |     |   |
| 7          | 6          | 5          | 4         | 3        | 2          | 1   | 0 |
| RESERVED_3 | SDDATASYNC | RESERVED_2 | SDCLKSYNC | SDCLKSEL | RESERVED_1 | MOD |   |
| R          | R/W        | R          | R/W       | R/W      | R/W        | R/W |   |
| 0h         | 0h         | 0h         | 0h        | 0h       | 0h         | 0h  |   |

**Table 3-1664. SDFM\_SDCTLPARM2 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                           |
|------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED_4 | R    | 0h    | Reserved                                                                                                                              |
| 7    | RESERVED_3 | R    | 0h    | Reserved                                                                                                                              |
| 6    | SDDATASYNC | R/W  | 0h    | 0: SD Data is not passed through a synchronizer.<br>1:SD Data is passed through a synchronizer.                                       |
| 5    | RESERVED_2 | R    | 0h    | Reserved                                                                                                                              |
| 4    | SDCLKSYNC  | R/W  | 0h    | 0: SD Clock is not passed through a synchronizer.<br>1:SD Clock is passed through a synchronizer.                                     |
| 3    | SDCLKSEL   | R/W  | 0h    | SD2 Clock source select.<br>0:Clock source to SDFM filter is its channel clock.<br>1:Clock source to SDFM filter is SD1 filter clock. |
| 2    | RESERVED_1 | R/W  | 0h    | Reserved                                                                                                                              |
| 1:0  | MOD        | R/W  | 0h    | Modulator clock modes<br>0:Mode<br>0:Modulator clock running at 1x data rate<br>1:Reserved<br>2:Reserved<br>3:Reserved                |

### 3.12.2.21 SDFM\_SDDFPARM2 Register

#### 1 SDFM\_SDDFPARM2 Register (Offset = 42h) [reset = 0h]

Data Filter Parameter Register for Ch2.

Return to [Summary Table](#)

**Table 3-1665. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8042h       |
| SDFM1         | 5026 9042h       |

**Figure 3-533. SDFM\_SDDFPARM2 Name Register**

| 15         | 14 | 13 | 12       | 11  | 10 | 9   | 8   |
|------------|----|----|----------|-----|----|-----|-----|
| RESERVED_1 |    |    | SDSYNCEN | SST |    | AE  | FEN |
| R          |    |    | R/W      | R/W |    | R/W | R/W |
| 0h         |    |    | 0h       | 0h  |    | 0h  | 0h  |
| 7          | 6  | 5  | 4        | 3   | 2  | 1   | 0   |
| DOSR       |    |    |          |     |    |     |     |
| R/W        |    |    |          |     |    |     |     |
| 0h         |    |    |          |     |    |     |     |

**Table 3-1667. SDFM\_SDDFPARM2 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                       |
|-------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                          |
| 12    | SDSYNCEN   | R/W  | 0h    | PWM synchronization [SDSYNC] of data filter<br>0:PWM synchronization of data filter is disabled<br>1:PWM synchronization of data filter is enabled<br>Note: SDSYNCx.SYNCSEL bits define which PWM signal is used to synchronize PWMs                                              |
| 11:10 | SST        | R/W  | 0h    | Data filter structure<br>00:Data filter runs with a Sincfast structure<br>01:Data filter runs with a Sinc1 structure<br>10:Data filter runs with a Sinc2 structure<br>11:Data filter runs with a Sinc3 structure                                                                  |
| 9     | AE         | R/W  | 0h    | Data filter Acknowledge Enable<br>0:Acknowledge flag is disabled for the particular filter<br>1:Acknowledge flag is enabled for the particular filter                                                                                                                             |
| 8     | FEN        | R/W  | 0h    | Filter Enable<br>0: The data filter is disabled and no data is produced<br>1: The data filter is enabled and data are produced in the data filter<br>Note: When filter is disabled, DOSR counter held in reset, filter data erased. Also resets FIFO pointers and clears the FIFO |
| 7:0   | DOSR       | R/W  | 0h    | Data filter Oversampling ratio<br>The actual oversampling ratio of data filter is DOSR + 1<br>These bits set the oversampling ratio of the data filter.<br>0x0FF represents an oversampling ratio of 256.                                                                         |



### 3.12.2.22 SDFM\_SDDPARM2 Register

#### 1 SDFM\_SDDPARM2 Register (Offset = 44h) [reset = 0h]

Data Parameter Register for Ch2.

Return to [Summary Table](#)

**Table 3-1668. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8044h       |
| SDFM1         | 5026 9044h       |

**Figure 3-534. SDFM\_SDDPARM2 Name Register**

|    |    |     |    |    |     |   |            |
|----|----|-----|----|----|-----|---|------------|
| 15 | 14 | 13  | 12 | 11 | 10  | 9 | 8          |
|    |    | SH  |    |    | DR  |   | RESERVED_1 |
|    |    | R/W |    |    | R/W |   | R          |
|    |    | 0h  |    |    | 0h  |   | 0h         |
| 7  | 6  | 5   | 4  | 3  | 2   | 1 | 0          |
|    |    |     |    |    |     |   | RESERVED_1 |
|    |    |     |    |    |     |   | R          |
|    |    |     |    |    |     |   | 0h         |

**Table 3-1670. SDFM\_SDDPARM2 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                      |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | SH         | R/W  | 0h    | Shift Control<br>These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen. |
| 10    | DR         | R/W  | 0h    | Data filter Data representation<br>0:Data stored in<br>16b2's complement<br>1:Data stored in<br>32b2's complement                |
| 9:0   | RESERVED_1 | R    | 0h    | Reserved                                                                                                                         |

### 3.12.2.23 SDFM\_SDFLT2CMPH1 Register

#### 1 SDFM\_SDFLT2CMPH1 Register (Offset = 46h) [reset = 7FFFh]

High-level Threshold Register for Ch2.

Return to [Summary Table](#)

**Table 3-1671. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8046h       |
| SDFM1         | 5026 9046h       |

**Figure 3-535. SDFM\_SDFLT2CMPH1 Name Register**

|            |       |    |    |    |    |   |   |
|------------|-------|----|----|----|----|---|---|
| 15         | 14    | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED_1 | HLT   |    |    |    |    |   |   |
| R          | R/W   |    |    |    |    |   |   |
| 0h         | 7FFFh |    |    |    |    |   |   |
| 7          | 6     | 5  | 4  | 3  | 2  | 1 | 0 |
| HLT        |       |    |    |    |    |   |   |
| R/W        |       |    |    |    |    |   |   |
| 7FFFh      |       |    |    |    |    |   |   |

**Table 3-1673. SDFM\_SDFLT2CMPH1 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                     |
|------|------------|------|-------|-----------------------------------------------------------------|
| 15   | RESERVED_1 | R    | 0h    | Reserved                                                        |
| 14:0 | HLT        | R/W  | 7FFFh | Unsigned high-level threshold for the comparator filter output. |

### 3.12.2.24 SDFM\_SDFLT2CMPL1 Register

#### 1 SDFM\_SDFLT2CMPL1 Register (Offset = 48h) [reset = 0h]

Low-level Threshold Register for Ch2.

Return to [Summary Table](#)

**Table 3-1674. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8048h       |
| SDFM1         | 5026 9048h       |

**Figure 3-536. SDFM\_SDFLT2CMPL1 Name Register**

|            |     |    |    |    |    |   |   |
|------------|-----|----|----|----|----|---|---|
| 15         | 14  | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED_1 | LLT |    |    |    |    |   |   |
| R          | R/W |    |    |    |    |   |   |
| 0h         | 0h  |    |    |    |    |   |   |
| 7          | 6   | 5  | 4  | 3  | 2  | 1 | 0 |
| LLT        |     |    |    |    |    |   |   |
| R/W        |     |    |    |    |    |   |   |
| 0h         |     |    |    |    |    |   |   |

**Table 3-1676. SDFM\_SDFLT2CMPL1 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                    |
|------|------------|------|-------|----------------------------------------------------------------|
| 15   | RESERVED_1 | R    | 0h    | Reserved                                                       |
| 14:0 | LLT        | R/W  | 0h    | Unsigned low-level threshold for the comparator filter output. |

### 3.12.2.25 SDFM\_SDCPARM2 Register

#### 1 SDFM\_SDCPARM2 Register (Offset = 4Ah) [reset = 0h]

Comparator Filter Parameter Register for Ch2.

Return to [Summary Table](#)

**Table 3-1677. Instance Table**

| Instance Name | Physical Address  |
|---------------|-------------------|
| <b>SDFM0</b>  | <b>5026 804Ah</b> |
| <b>SDFM1</b>  | <b>5026 904Ah</b> |

**Figure 3-537. SDFM\_SDCPARM2 Name Register**

| 15       |  | 14       |  | 13       |  | 12       |  | 11 |  | 10   |  | 9    |  | 8       |  |
|----------|--|----------|--|----------|--|----------|--|----|--|------|--|------|--|---------|--|
| CEVT2SEL |  |          |  | CEN      |  | CEVT1SEL |  |    |  | HZEN |  | MFIE |  | CS1_CS0 |  |
| R/W      |  |          |  | R/W      |  | R/W      |  |    |  | R/W  |  | R/W  |  | R/W     |  |
| 0h       |  |          |  | 0h       |  | 0h       |  |    |  | 0h   |  | 0h   |  | 0h      |  |
| 7        |  | 6        |  | 5        |  | 4        |  | 3  |  | 2    |  | 1    |  | 0       |  |
| CS1_CS0  |  | EN_CEVT2 |  | EN_CEVT1 |  | COSR     |  |    |  |      |  |      |  |         |  |
| R/W      |  | R/W      |  | R/W      |  | R/W      |  |    |  |      |  |      |  |         |  |
| 0h       |  | 0h       |  | 0h       |  | 0h       |  |    |  |      |  |      |  |         |  |

**Table 3-1679. SDFM\_SDCPARM2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                    |
|-------|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | CEVT2SEL | R/W  | 0h    | Comparator Event2 Select<br>00: COMPL1<br>01:COMPL1 OR COMPH1<br>10:COMPL2<br>11:COMPL2 OR COMPH2                                                                                                                                              |
| 13    | CEN      | R/W  | 0h    | Comparator Filter enable<br>0:Disable comparator filter<br>1:Enable comparator filter                                                                                                                                                          |
| 12:11 | CEVT1SEL | R/W  | 0h    | Comparator Event1 Select<br>00: COMPH1<br>01:COMPL1 OR COMPH1<br>10:COMPH2<br>11:COMPL2 OR COMPH2                                                                                                                                              |
| 10    | HZEN     | R/W  | 0h    | High level [Z] Threshold crossing output enable<br>0:Disable Higher level Threshold [Z] crossing<br>1:Enable Higher level Threshold [Z] crossing                                                                                               |
| 9     | MFIE     | R/W  | 0h    | Modulator Failure Interrupt Enable<br>0:Disable modulator failure interrupt and its flag<br>1:Enable modulator failure interrupt and its flag                                                                                                  |
| 8:7   | CS1_CS0  | R/W  | 0h    | Comparator filter structure<br>00:Comparator filter runs with a sincfast structure<br>01:Comparator filter runs with a Sinc1 structure<br>10:Comparator filter runs with a Sinc2 structure<br>11:Comparator filter runs with a Sinc3 structure |
| 6     | EN_CEVT2 | R/W  | 0h    | CEVT2 interrupt enable<br>0:Disable CEVT2 interrupt<br>1:Enable CEVT2 interrupt                                                                                                                                                                |
| 5     | EN_CEVT1 | R/W  | 0h    | CEVT1 interrupt enable<br>0:Disable CEVT1 interrupt<br>1:Enable CEVT1 interrupt                                                                                                                                                                |

**Table 3-1679. SDFM\_SDCPARM2 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                           |
|-----|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | COSR  | R/W  | 0h    | Comparator Oversampling ratio.<br>The actual rate is COSR + 1.<br>These bits set the oversampling ratio of the filter.<br>0x1F represents an oversampling ratio of 32 |

### 3.12.2.26 SDFM\_SDDATA2 Register

#### 1 SDFM\_SDDATA2 Register (Offset = 4Ch) [reset = 0h]

Data Filter Data Register (16 or 32bit) for Ch2.

Return to [Summary Table](#)

**Table 3-1680. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 804Ch       |
| SDFM1         | 5026 904Ch       |

**Figure 3-538. SDFM\_SDDATA2 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DATA32HI |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DATA32HI |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DATA16   |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DATA16   |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 3-1682. SDFM\_SDDATA2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                             |
|-------|----------|------|-------|---------------------------------------------------------|
| 31:16 | DATA32HI | R    | 0h    | Hi-order<br>16bin<br>32bmode, 16-bit Data in<br>16bmode |
| 15:0  | DATA16   | R    | 0h    | Lo-order<br>16bin<br>32bmode                            |

### 3.12.2.27 SDFM\_SDDATFIFO2 Register

#### 1 SDFM\_SDDATFIFO2 Register (Offset = 50h) [reset = 0h]

Filter Data FIFO Output(32b) for Ch2.

Return to [Summary Table](#)

**Table 3-1683. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8050h       |
| SDFM1         | 5026 9050h       |

**Figure 3-539. SDFM\_SDDATFIFO2 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DATA32HI |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DATA32HI |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DATA16   |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DATA16   |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 3-1685. SDFM\_SDDATFIFO2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                             |
|-------|----------|------|-------|---------------------------------------------------------|
| 31:16 | DATA32HI | R    | 0h    | Hi-order<br>16bin<br>32bmode, 16-bit Data in<br>16bmode |
| 15:0  | DATA16   | R    | 0h    | Lo-order<br>16bin<br>32bmode                            |

### 3.12.2.28 SDFM\_SDCDATA2 Register

#### 1 SDFM\_SDCDATA2 Register (Offset = 54h) [reset = 0h]

Comparator Filter Data Register (16b) for Ch2.

Return to [Summary Table](#)

**Table 3-1686. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8054h       |
| SDFM1         | 5026 9054h       |

**Figure 3-540. SDFM\_SDCDATA2 Name Register**

|        |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DATA16 |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |
| 7      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| DATA16 |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |

**Table 3-1688. SDFM\_SDCDATA2 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                      |
|------|--------|------|-------|----------------------------------|
| 15:0 | DATA16 | R    | 0h    | Comparator Data output - 16bonly |



### 3.12.2.29 SDFM\_SDFLT2CMPH2 Register

#### 1 SDFM\_SDFLT2CMPH2 Register (Offset = 56h) [reset = 7FFFh]

Second high level threshold for CH2.

Return to [Summary Table](#)

**Table 3-1689. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8056h       |
| SDFM1         | 5026 9056h       |

**Figure 3-541. SDFM\_SDFLT2CMPH2 Name Register**

|            |       |    |    |    |    |   |   |
|------------|-------|----|----|----|----|---|---|
| 15         | 14    | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED_1 | HLT2  |    |    |    |    |   |   |
| R          | R/W   |    |    |    |    |   |   |
| 0h         | 7FFFh |    |    |    |    |   |   |
| 7          | 6     | 5  | 4  | 3  | 2  | 1 | 0 |
| HLT2       |       |    |    |    |    |   |   |
| R/W        |       |    |    |    |    |   |   |
| 7FFFh      |       |    |    |    |    |   |   |

**Table 3-1691. SDFM\_SDFLT2CMPH2 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                            |
|------|------------|------|-------|------------------------------------------------------------------------|
| 15   | RESERVED_1 | R    | 0h    | Reserved                                                               |
| 14:0 | HLT2       | R/W  | 7FFFh | Second Unsigned high-level threshold for the comparator filter output. |

### 3.12.2.30 SDFM\_SDFLT2CMPHZ Register

#### 1 SDFM\_SDFLT2CMPHZ Register (Offset = 58h) [reset = 0h]

High-level (Z) Threshold Register for Ch2.

Return to [Summary Table](#)

**Table 3-1692. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8058h       |
| SDFM1         | 5026 9058h       |

**Figure 3-542. SDFM\_SDFLT2CMPHZ Name Register**

|            |    |    |    |    |    |   |      |
|------------|----|----|----|----|----|---|------|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8    |
| RESERVED_1 |    |    |    |    |    |   | HLTZ |
| R          |    |    |    |    |    |   | R/W  |
| 0h         |    |    |    |    |    |   | 0h   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0    |
|            |    |    |    |    |    |   | HLTZ |
|            |    |    |    |    |    |   | R/W  |
|            |    |    |    |    |    |   | 0h   |

**Table 3-1694. SDFM\_SDFLT2CMPHZ Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                |
|------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                   |
| 14:0 | HLTZ       | R/W  | 0h    | Unsigned High-level threshold [Z] for the comparator filter output. Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator SDCMPHx, it does not have the ability to generate an interrupt. |

### 3.12.2.31 SDFM\_SDFIFOCTL2 Register

#### 1 SDFM\_SDFIFOCTL2 Register (Offset = 5Ah) [reset = 0h]

FIFO Control Register for Ch2.

Return to [Summary Table](#)

**Table 3-1695. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 805Ah       |
| SDFM1         | 5026 905Ah       |

**Figure 3-543. SDFM\_SDFIFOCTL2 Name Register**

| 15     | 14       | 13         | 12     | 11         | 10    | 9 | 8 |
|--------|----------|------------|--------|------------|-------|---|---|
| OVFIEN | DRINTSEL | FFEN       | FFIEN  | RESERVED_2 | SDFST |   |   |
| R/W    | R/W      | R/W        | R/W    | R          | R     |   |   |
| 0h     | 0h       | 0h         | 0h     | 0h         | 0h    |   |   |
| 7      | 6        | 5          | 4      | 3          | 2     | 1 | 0 |
| SDFST  |          | RESERVED_1 | SDFFIL |            |       |   |   |
| R      |          | R          | R/W    |            |       |   |   |
| 0h     |          | 0h         | 0h     |            |       |   |   |

**Table 3-1697. SDFM\_SDFIFOCTL2 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                       |
|------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | OVFIEN     | R/W  | 0h    | SDFIFO Overflow interrupt enable<br>0: SDFIFO Overflow condition will not generate an interrupt<br>1: SDFIFO overflow condition generates an interrupt on SDy_ERR |
| 14   | DRINTSEL   | R/W  | 0h    | Data-Ready Interrupt [DRINT] source select<br>0 = AF1 [Select non-FIFO data-ready interrupt]<br>1 = SDFINT1 [Select FIFO data-ready interrupt]                    |
| 13   | FFEN       | R/W  | 0h    | SDFIFO Enable<br>0: Disable FIFO operation<br>1: Enable FIFO operation<br>Note: When FIFO is disabled, FIFO contents are cleared                                  |
| 12   | FFIEN      | R/W  | 0h    | SDFIFO data ready Interrupt Enable                                                                                                                                |
| 11   | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                          |
| 10:6 | SDFST      | R    | 0h    | SDFIFO Status<br>00000 FIFO empty<br>00001 FIFO has 1 word<br>.....<br>10000 FIFO has 16 words                                                                    |
| 5    | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                          |
| 4:0  | SDFFIL     | R/W  | 0h    | SDFIFO interrupt level bits<br>The FIFO will generate an interrupt when the FIFO status [SDFST] != FIFO level [SDFFIL]                                            |

### 3.12.2.32 SDFM\_SDSYNC2 Register

#### 1 SDFM\_SDSYNC2 Register (Offset = 5Ch) [reset = 400h]

SD Filter Sync control for Ch2.

Return to [Summary Table](#)

**Table 3-1698. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 805Ch       |
| SDFM1         | 5026 905Ch       |

**Figure 3-544. SDFM\_SDSYNC2 Name Register**

| 15         | 14       | 13      | 12 | 11 | 10       | 9           | 8        |
|------------|----------|---------|----|----|----------|-------------|----------|
| RESERVED_1 |          |         |    |    | WTSCLREN | FFSYNCCLREN | WTSYNCLR |
| R          |          |         |    |    | R/W      | R/W         | R/W      |
| 0h         |          |         |    |    | 1h       | 0h          | 0h       |
| 7          | 6        | 5       | 4  | 3  | 2        | 1           | 0        |
| WTSYNFLG   | WTSYNCEN | SYNCSEL |    |    |          |             |          |
| R          | R/W      | R/W     |    |    |          |             |          |
| 0h         | 0h       | 0h      |    |    |          |             |          |

**Table 3-1700. SDFM\_SDSYNC2 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                              |
|-------|-------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | RESERVED_1  | R    | 0h    | Reserved                                                                                                                                                                 |
| 10    | WTSCLREN    | R/W  | 1h    | WTSYNFLG Clear-on-FIFOINT Enable<br>0:WTSYNFLG can only be cleared manually [using WTSYNCLR bit]<br>1:WTSYNFLG is cleared automatically on SDFINT                        |
| 9     | FFSYNCCLREN | R/W  | 0h    | FIFO Clear-on-SDSYNC Enable<br>0:SDFIFO is not automatically cleared upon receiving SDSYNC<br>1:SDFIFO is automatically cleared upon receiving SDSYNC                    |
| 8     | WTSYNCLR    | R/W  | 0h    | Wait-for-Sync Flag Clear [always reads 0]<br>0:Write of 0 has no effect<br>1:Write of 1 clears WTSYNFLG                                                                  |
| 7     | WTSYNFLG    | R    | 0h    | Wait-for-Sync Flag<br>0:SDSYNC event has not occurred<br>1:SDSYNC event occurred.                                                                                        |
| 6     | WTSYNCEN    | R/W  | 0h    | Wait-for-Sync Enable<br>0:Incoming Data written to SDFIFO on every Data-Ready [DR] Event<br>1:Incoming Data written to SDFIFO on DR event only after SDSYNC event occurs |
| 5:0   | SYNCSEL     | R/W  | 0h    | Defines source for the SDSYNC Input on this channel<br>Refer SDSYNcx.SYNCSEL table                                                                                       |

### 3.12.2.33 SDFM\_SDFLT2CMPL2 Register

#### 1 SDFM\_SDFLT2CMPL2 Register (Offset = 5Eh) [reset = 0h]

Second low level threshold for CH2.

Return to [Summary Table](#)

**Table 3-1701. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 805Eh       |
| SDFM1         | 5026 905Eh       |

**Figure 3-545. SDFM\_SDFLT2CMPL2 Name Register**

|            |      |    |    |    |    |   |   |
|------------|------|----|----|----|----|---|---|
| 15         | 14   | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED_1 | LLT2 |    |    |    |    |   |   |
| R          | R/W  |    |    |    |    |   |   |
| 0h         | 0h   |    |    |    |    |   |   |
| 7          | 6    | 5  | 4  | 3  | 2  | 1 | 0 |
| LLT2       |      |    |    |    |    |   |   |
| R/W        |      |    |    |    |    |   |   |
| 0h         |      |    |    |    |    |   |   |

**Table 3-1703. SDFM\_SDFLT2CMPL2 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                           |
|------|------------|------|-------|-----------------------------------------------------------------------|
| 15   | RESERVED_1 | R    | 0h    | Reserved                                                              |
| 14:0 | LLT2       | R/W  | 0h    | Second Unsigned low-level threshold for the comparator filter output. |

### 3.12.2.34 SDFM\_SDCTLPARM3 Register

#### 1 SDFM\_SDCTLPARM3 Register (Offset = 60h) [reset = 0h]

Control Parameter Register for Ch3.

Return to [Summary Table](#)

**Table 3-1704. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8060h       |
| SDFM1         | 5026 9060h       |

**Figure 3-546. SDFM\_SDCTLPARM3 Name Register**

|            |            |            |           |          |            |     |   |
|------------|------------|------------|-----------|----------|------------|-----|---|
| 15         | 14         | 13         | 12        | 11       | 10         | 9   | 8 |
| RESERVED_4 |            |            |           |          |            |     |   |
| R          |            |            |           |          |            |     |   |
| 0h         |            |            |           |          |            |     |   |
| 7          | 6          | 5          | 4         | 3        | 2          | 1   | 0 |
| RESERVED_3 | SDDATASYNC | RESERVED_2 | SDCLKSYNC | SDCLKSEL | RESERVED_1 | MOD |   |
| R          | R/W        | R          | R/W       | R/W      | R/W        | R/W |   |
| 0h         | 0h         | 0h         | 0h        | 0h       | 0h         | 0h  |   |

**Table 3-1706. SDFM\_SDCTLPARM3 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                           |
|------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED_4 | R    | 0h    | Reserved                                                                                                                              |
| 7    | RESERVED_3 | R    | 0h    | Reserved                                                                                                                              |
| 6    | SDDATASYNC | R/W  | 0h    | 0: SD Data is not passed through a synchronizer.<br>1:SD Data is passed through a synchronizer.                                       |
| 5    | RESERVED_2 | R    | 0h    | Reserved                                                                                                                              |
| 4    | SDCLKSYNC  | R/W  | 0h    | 0: SD Clock is not passed through a synchronizer.<br>1:SD Clock is passed through a synchronizer.                                     |
| 3    | SDCLKSEL   | R/W  | 0h    | SD3 Clock source select.<br>0:Clock source to SDFM filter is its channel clock.<br>1:Clock source to SDFM filter is SD1 filter clock. |
| 2    | RESERVED_1 | R/W  | 0h    | Reserved                                                                                                                              |
| 1:0  | MOD        | R/W  | 0h    | Modulator clock modes<br>0:Mode<br>0:Modulator clock running at 1x data rate<br>1:Reserved<br>2:Reserved<br>3:Reserved                |

### 3.12.2.35 SDFM\_SDDFPARM3 Register

#### 1 SDFM\_SDDFPARM3 Register (Offset = 62h) [reset = 0h]

Data Filter Parameter Register for Ch3.

Return to [Summary Table](#)

**Table 3-1707. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8062h       |
| SDFM1         | 5026 9062h       |

**Figure 3-547. SDFM\_SDDFPARM3 Name Register**

| 15         | 14 | 13 | 12       | 11  | 10 | 9   | 8   |
|------------|----|----|----------|-----|----|-----|-----|
| RESERVED_1 |    |    | SDSYNCEN | SST |    | AE  | FEN |
| R          |    |    | R/W      | R/W |    | R/W | R/W |
| 0h         |    |    | 0h       | 0h  |    | 0h  | 0h  |
| 7          | 6  | 5  | 4        | 3   | 2  | 1   | 0   |
| DOSR       |    |    |          |     |    |     |     |
| R/W        |    |    |          |     |    |     |     |
| 0h         |    |    |          |     |    |     |     |

**Table 3-1709. SDFM\_SDDFPARM3 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                       |
|-------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                          |
| 12    | SDSYNCEN   | R/W  | 0h    | PWM synchronization [SDSYNC] of data filter<br>0: PWM synchronization of data filter is disabled<br>1: PWM synchronization of data filter is enabled<br>Note: SDSYNCS.SYNCSEL bits define which PWM signal is used to synchronize PWMs                                            |
| 11:10 | SST        | R/W  | 0h    | Data filter structure<br>00: Data filter runs with a Sincfast structure<br>01: Data filter runs with a Sinc1 structure<br>10: Data filter runs with a Sinc2 structure<br>11: Data filter runs with a Sinc3 structure                                                              |
| 9     | AE         | R/W  | 0h    | Data filter Acknowledge Enable<br>0: Acknowledge flag is disabled for the particular filter<br>1: Acknowledge flag is enabled for the particular filter                                                                                                                           |
| 8     | FEN        | R/W  | 0h    | Filter Enable<br>0: The data filter is disabled and no data is produced<br>1: The data filter is enabled and data are produced in the data filter<br>Note: When filter is disabled, DOSR counter held in reset, filter data erased. Also resets FIFO pointers and clears the FIFO |
| 7:0   | DOSR       | R/W  | 0h    | Data filter Oversampling ratio<br>The actual oversampling ratio of data filter is DOSR + 1<br>These bits set the oversampling ratio of the data filter.<br>0x0FF represents an oversampling ratio of 256.                                                                         |

### 3.12.2.36 SDFM\_SDDPARM3 Register

#### 1 SDFM\_SDDPARM3 Register (Offset = 64h) [reset = 0h]

Data Parameter Register for Ch3.

Return to [Summary Table](#)

**Table 3-1710. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8064h       |
| SDFM1         | 5026 9064h       |

**Figure 3-548. SDFM\_SDDPARM3 Name Register**

|    |    |     |    |    |     |   |            |
|----|----|-----|----|----|-----|---|------------|
| 15 | 14 | 13  | 12 | 11 | 10  | 9 | 8          |
|    |    | SH  |    |    | DR  |   | RESERVED_1 |
|    |    | R/W |    |    | R/W |   | R          |
|    |    | 0h  |    |    | 0h  |   | 0h         |
| 7  | 6  | 5   | 4  | 3  | 2   | 1 | 0          |
|    |    |     |    |    |     |   | RESERVED_1 |
|    |    |     |    |    |     |   | R          |
|    |    |     |    |    |     |   | 0h         |

**Table 3-1712. SDFM\_SDDPARM3 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                      |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | SH         | R/W  | 0h    | Shift Control<br>These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen. |
| 10    | DR         | R/W  | 0h    | Data filter Data representation<br>0:Data stored in<br>16b2's complement<br>1:Data stored in<br>32b2's complement                |
| 9:0   | RESERVED_1 | R    | 0h    | Reserved                                                                                                                         |



### 3.12.2.37 SDFM\_SDFLT3CMPH1 Register

#### 1 SDFM\_SDFLT3CMPH1 Register (Offset = 66h) [reset = 7FFFh]

High-level Threshold Register for Ch3.

Return to [Summary Table](#)

**Table 3-1713. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8066h       |
| SDFM1         | 5026 9066h       |

**Figure 3-549. SDFM\_SDFLT3CMPH1 Name Register**

|            |       |    |    |    |    |   |   |
|------------|-------|----|----|----|----|---|---|
| 15         | 14    | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED_1 | HLT   |    |    |    |    |   |   |
| R          | R/W   |    |    |    |    |   |   |
| 0h         | 7FFFh |    |    |    |    |   |   |
| 7          | 6     | 5  | 4  | 3  | 2  | 1 | 0 |
| HLT        |       |    |    |    |    |   |   |
| R/W        |       |    |    |    |    |   |   |
| 7FFFh      |       |    |    |    |    |   |   |

**Table 3-1715. SDFM\_SDFLT3CMPH1 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                     |
|------|------------|------|-------|-----------------------------------------------------------------|
| 15   | RESERVED_1 | R    | 0h    | Reserved                                                        |
| 14:0 | HLT        | R/W  | 7FFFh | Unsigned high-level threshold for the comparator filter output. |

### 3.12.2.38 SDFM\_SDFLT3CMPL1 Register

#### 1 SDFM\_SDFLT3CMPL1 Register (Offset = 68h) [reset = 0h]

Low-level Threshold Register for Ch3.

Return to [Summary Table](#)

**Table 3-1716. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8068h       |
| SDFM1         | 5026 9068h       |

**Figure 3-550. SDFM\_SDFLT3CMPL1 Name Register**

|            |     |    |    |    |    |   |   |
|------------|-----|----|----|----|----|---|---|
| 15         | 14  | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED_1 | LLT |    |    |    |    |   |   |
| R          | R/W |    |    |    |    |   |   |
| 0h         | 0h  |    |    |    |    |   |   |
| 7          | 6   | 5  | 4  | 3  | 2  | 1 | 0 |
| LLT        |     |    |    |    |    |   |   |
| R/W        |     |    |    |    |    |   |   |
| 0h         |     |    |    |    |    |   |   |

**Table 3-1718. SDFM\_SDFLT3CMPL1 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                    |
|------|------------|------|-------|----------------------------------------------------------------|
| 15   | RESERVED_1 | R    | 0h    | Reserved                                                       |
| 14:0 | LLT        | R/W  | 0h    | Unsigned low-level threshold for the comparator filter output. |

### 3.12.2.39 SDFM\_SDCPARM3 Register

#### 1 SDFM\_SDCPARM3 Register (Offset = 6Ah) [reset = 0h]

Comparator Filter Parameter Register for Ch3.

Return to [Summary Table](#)

**Table 3-1719. Instance Table**

| Instance Name | Physical Address  |
|---------------|-------------------|
| <b>SDFM0</b>  | <b>5026 806Ah</b> |
| <b>SDFM1</b>  | <b>5026 906Ah</b> |

**Figure 3-551. SDFM\_SDCPARM3 Name Register**

|          |          |          |      |      |         |     |     |
|----------|----------|----------|------|------|---------|-----|-----|
| 15       | 14       | 13       | 12   | 11   | 10      | 9   | 8   |
| CEVT2SEL | CEN      | CEVT1SEL | HZEN | MFIE | CS1_CS0 |     |     |
| R/W      | R/W      | R/W      | R/W  | R/W  | R/W     | R/W | R/W |
| 0h       | 0h       | 0h       | 0h   | 0h   | 0h      | 0h  | 0h  |
| 7        | 6        | 5        | 4    | 3    | 2       | 1   | 0   |
| CS1_CS0  | EN_CEVT2 | EN_CEVT1 | COSR |      |         |     |     |
| R/W      | R/W      | R/W      | R/W  |      |         |     |     |
| 0h       | 0h       | 0h       | 0h   |      |         |     |     |

**Table 3-1721. SDFM\_SDCPARM3 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                    |
|-------|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | CEVT2SEL | R/W  | 0h    | Comparator Event2 Select<br>00: COMPL1<br>01:COMPL1 OR COMPH1<br>10:COMPL2<br>11:COMPL2 OR COMPH2                                                                                                                                              |
| 13    | CEN      | R/W  | 0h    | Comparator Filter enable<br>0:Disable comparator filter<br>1:Enable comparator filter                                                                                                                                                          |
| 12:11 | CEVT1SEL | R/W  | 0h    | Comparator Event1 Select<br>00: COMPH1<br>01:COMPL1 OR COMPH1<br>10:COMPH2<br>11:COMPL2 OR COMPH2                                                                                                                                              |
| 10    | HZEN     | R/W  | 0h    | High level [Z] Threshold crossing output enable<br>0:Disable Higher level Threshold [Z] crossing<br>1:Enable Higher level Threshold [Z] crossing                                                                                               |
| 9     | MFIE     | R/W  | 0h    | Modulator Failure Interrupt Enable<br>0:Disable modulator failure interrupt and its flag<br>1:Enable modulator failure interrupt and its flag                                                                                                  |
| 8:7   | CS1_CS0  | R/W  | 0h    | Comparator filter structure<br>00:Comparator filter runs with a sincfast structure<br>01:Comparator filter runs with a Sinc1 structure<br>10:Comparator filter runs with a Sinc2 structure<br>11:Comparator filter runs with a Sinc3 structure |
| 6     | EN_CEVT2 | R/W  | 0h    | CEVT2 interrupt enable<br>0:Disable CEVT2 interrupt<br>1:Enable CEVT2 interrupt                                                                                                                                                                |
| 5     | EN_CEVT1 | R/W  | 0h    | CEVT1 interrupt enable<br>0:Disable CEVT1 interrupt<br>1:Enable CEVT1 interrupt                                                                                                                                                                |

**Table 3-1721. SDFM\_SDCPARM3 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                           |
|-----|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | COSR  | R/W  | 0h    | Comparator Oversampling ratio.<br>The actual rate is COSR + 1.<br>These bits set the oversampling ratio of the filter.<br>0x1F represents an oversampling ratio of 32 |

### 3.12.2.40 SDFM\_SDDATA3 Register

#### 1 SDFM\_SDDATA3 Register (Offset = 6Ch) [reset = 0h]

Data Filter Data Register (16 or 32bit) for Ch3.

Return to [Summary Table](#)

**Table 3-1722. Instance Table**

| Instance Name | Physical Address  |
|---------------|-------------------|
| <b>SDFM0</b>  | <b>5026 806Ch</b> |
| <b>SDFM1</b>  | <b>5026 906Ch</b> |

**Figure 3-552. SDFM\_SDDATA3 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DATA32HI |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DATA32HI |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DATA16   |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DATA16   |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 3-1724. SDFM\_SDDATA3 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                             |
|-------|----------|------|-------|---------------------------------------------------------|
| 31:16 | DATA32HI | R    | 0h    | Hi-order<br>16bin<br>32bmode, 16-bit Data in<br>16bmode |
| 15:0  | DATA16   | R    | 0h    | Lo-order<br>16bin<br>32bmode                            |

### 3.12.2.41 SDFM\_SDDATFIFO3 Register

#### 1 SDFM\_SDDATFIFO3 Register (Offset = 70h) [reset = 0h]

Filter Data FIFO Output(32b) for Ch3.

Return to [Summary Table](#)

**Table 3-1725. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8070h       |
| SDFM1         | 5026 9070h       |

**Figure 3-553. SDFM\_SDDATFIFO3 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DATA32HI |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DATA32HI |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DATA16   |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DATA16   |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 3-1727. SDFM\_SDDATFIFO3 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                             |
|-------|----------|------|-------|---------------------------------------------------------|
| 31:16 | DATA32HI | R    | 0h    | Hi-order<br>16bin<br>32bmode, 16-bit Data in<br>16bmode |
| 15:0  | DATA16   | R    | 0h    | Lo-order<br>16bin<br>32bmode                            |

### 3.12.2.42 SDFM\_SDCDATA3 Register

#### 1 SDFM\_SDCDATA3 Register (Offset = 74h) [reset = 0h]

Comparator Filter Data Register (16b) for Ch3.

Return to [Summary Table](#)

**Table 3-1728. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8074h       |
| SDFM1         | 5026 9074h       |

**Figure 3-554. SDFM\_SDCDATA3 Name Register**

|        |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DATA16 |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |
| 7      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| DATA16 |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |

**Table 3-1730. SDFM\_SDCDATA3 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                      |
|------|--------|------|-------|----------------------------------|
| 15:0 | DATA16 | R    | 0h    | Comparator Data output - 16bonly |

### 3.12.2.43 SDFM\_SDFLT3CMPH2 Register

#### 1 SDFM\_SDFLT3CMPH2 Register (Offset = 76h) [reset = 7FFFh]

Second high level threshold for CH3.

Return to [Summary Table](#)

**Table 3-1731. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8076h       |
| SDFM1         | 5026 9076h       |

**Figure 3-555. SDFM\_SDFLT3CMPH2 Name Register**

|            |       |    |    |    |    |   |   |
|------------|-------|----|----|----|----|---|---|
| 15         | 14    | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED_1 | HLT2  |    |    |    |    |   |   |
| R          | R/W   |    |    |    |    |   |   |
| 0h         | 7FFFh |    |    |    |    |   |   |
| 7          | 6     | 5  | 4  | 3  | 2  | 1 | 0 |
| HLT2       |       |    |    |    |    |   |   |
| R/W        |       |    |    |    |    |   |   |
| 7FFFh      |       |    |    |    |    |   |   |

**Table 3-1733. SDFM\_SDFLT3CMPH2 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                            |
|------|------------|------|-------|------------------------------------------------------------------------|
| 15   | RESERVED_1 | R    | 0h    | Reserved                                                               |
| 14:0 | HLT2       | R/W  | 7FFFh | Second Unsigned high-level threshold for the comparator filter output. |



### 3.12.2.44 SDFM\_SDFLT3CMPHZ Register

#### 1 SDFM\_SDFLT3CMPHZ Register (Offset = 78h) [reset = 0h]

High-level (Z) Threshold Register for Ch3.

Return to [Summary Table](#)

**Table 3-1734. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8078h       |
| SDFM1         | 5026 9078h       |

**Figure 3-556. SDFM\_SDFLT3CMPHZ Name Register**

|            |      |    |    |    |    |   |   |
|------------|------|----|----|----|----|---|---|
| 15         | 14   | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED_1 | HLTZ |    |    |    |    |   |   |
| R          | R/W  |    |    |    |    |   |   |
| 0h         | 0h   |    |    |    |    |   |   |
| 7          | 6    | 5  | 4  | 3  | 2  | 1 | 0 |
| HLTZ       |      |    |    |    |    |   |   |
| R/W        |      |    |    |    |    |   |   |
| 0h         |      |    |    |    |    |   |   |

**Table 3-1736. SDFM\_SDFLT3CMPHZ Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                |
|------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                   |
| 14:0 | HLTZ       | R/W  | 0h    | Unsigned High-level threshold [Z] for the comparator filter output. Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator SDCMPHx, it does not have the ability to generate an interrupt. |

### 3.12.2.45 SDFM\_SDFIFOCTL3 Register

#### 1 SDFM\_SDFIFOCTL3 Register (Offset = 7Ah) [reset = 0h]

FIFO Control Register for Ch3.

Return to [Summary Table](#)

**Table 3-1737. Instance Table**

| Instance Name | Physical Address  |
|---------------|-------------------|
| <b>SDFM0</b>  | <b>5026 807Ah</b> |
| <b>SDFM1</b>  | <b>5026 907Ah</b> |

**Figure 3-557. SDFM\_SDFIFOCTL3 Name Register**

|        |          |            |        |            |       |   |   |
|--------|----------|------------|--------|------------|-------|---|---|
| 15     | 14       | 13         | 12     | 11         | 10    | 9 | 8 |
| OVFIEN | DRINTSEL | FFEN       | FFIEN  | RESERVED_2 | SDFST |   |   |
| R/W    | R/W      | R/W        | R/W    | R          | R     |   |   |
| 0h     | 0h       | 0h         | 0h     | 0h         | 0h    |   |   |
| 7      | 6        | 5          | 4      | 3          | 2     | 1 | 0 |
| SDFST  |          | RESERVED_1 | SDFFIL |            |       |   |   |
| R      |          | R          | R/W    |            |       |   |   |
| 0h     |          | 0h         | 0h     |            |       |   |   |

**Table 3-1739. SDFM\_SDFIFOCTL3 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                       |
|------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | OVFIEN     | R/W  | 0h    | SDFIFO Overflow interrupt enable<br>0: SDFIFO Overflow condition will not generate an interrupt<br>1: SDFIFO overflow condition generates an interrupt on SDy_ERR |
| 14   | DRINTSEL   | R/W  | 0h    | Data-Ready Interrupt [DRINT] source select<br>0 = AF1 [Select non-FIFO data-ready interrupt]<br>1 = SDFINT1 [Select FIFO data-ready interrupt]                    |
| 13   | FFEN       | R/W  | 0h    | SDFIFO Enable<br>0: Disable FIFO operation<br>1: Enable FIFO operation<br>Note: When FIFO is disabled, FIFO contents are cleared                                  |
| 12   | FFIEN      | R/W  | 0h    | SDFIFO data ready Interrupt Enable                                                                                                                                |
| 11   | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                          |
| 10:6 | SDFST      | R    | 0h    | SDFIFO Status<br>00000 FIFO empty<br>00001 FIFO has 1 word<br>.....<br>10000 FIFO has 16 words                                                                    |
| 5    | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                          |
| 4:0  | SDFFIL     | R/W  | 0h    | SDFIFO interrupt level bits<br>The FIFO will generate an interrupt when the FIFO status [SDFST] != FIFO level [SDFFIL]                                            |

### 3.12.2.46 SDFM\_SDSYNC3 Register

#### 1 SDFM\_SDSYNC3 Register (Offset = 7Ch) [reset = 400h]

SD Filter Sync control for Ch3.

Return to [Summary Table](#)

**Table 3-1740. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 807Ch       |
| SDFM1         | 5026 907Ch       |

**Figure 3-558. SDFM\_SDSYNC3 Name Register**

| 15         | 14       | 13      | 12 | 11 | 10       | 9           | 8        |
|------------|----------|---------|----|----|----------|-------------|----------|
| RESERVED_1 |          |         |    |    | WTSCLREN | FFSYNCCLREN | WTSYNCLR |
| R          |          |         |    |    | R/W      | R/W         | R/W      |
| 0h         |          |         |    |    | 1h       | 0h          | 0h       |
| 7          | 6        | 5       | 4  | 3  | 2        | 1           | 0        |
| WTSYNFLG   | WTSYNCEN | SYNCSEL |    |    |          |             |          |
| R          | R/W      | R/W     |    |    |          |             |          |
| 0h         | 0h       | 0h      |    |    |          |             |          |

**Table 3-1742. SDFM\_SDSYNC3 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                              |
|-------|-------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | RESERVED_1  | R    | 0h    | Reserved                                                                                                                                                                 |
| 10    | WTSCLREN    | R/W  | 1h    | WTSYNFLG Clear-on-FIFOINT Enable<br>0:WTSYNFLG can only be cleared manually [using WTSYNCLR bit]<br>1:WTSYNFLG is cleared automatically on SDFINT                        |
| 9     | FFSYNCCLREN | R/W  | 0h    | FIFO Clear-on-SDSYNC Enable<br>0:SDFIFO is not automatically cleared upon receiving SDSYNC<br>1:SDFIFO is automatically cleared upon receiving SDSYNC                    |
| 8     | WTSYNCLR    | R/W  | 0h    | Wait-for-Sync Flag Clear [always reads 0]<br>0:Write of 0 has no effect<br>1:Write of 1 clears WTSYNFLG                                                                  |
| 7     | WTSYNFLG    | R    | 0h    | Wait-for-Sync Flag<br>0:SDSYNC event has not occurred<br>1:SDSYNC event occurred.                                                                                        |
| 6     | WTSYNCEN    | R/W  | 0h    | Wait-for-Sync Enable<br>0:Incoming Data written to SDFIFO on every Data-Ready [DR] Event<br>1:Incoming Data written to SDFIFO on DR event only after SDSYNC event occurs |
| 5:0   | SYNCSEL     | R/W  | 0h    | Defines source for the SDSYNC Input on this channel<br>Refer SDSYNcx.SYNCSEL table                                                                                       |

### 3.12.2.47 SDFM\_SDFLT3CMPL2 Register

#### 1 SDFM\_SDFLT3CMPL2 Register (Offset = 7Eh) [reset = 0h]

Second low level threshold for CH3.

Return to [Summary Table](#)

**Table 3-1743. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 807Eh       |
| SDFM1         | 5026 907Eh       |

**Figure 3-559. SDFM\_SDFLT3CMPL2 Name Register**

|            |    |    |    |    |    |   |      |
|------------|----|----|----|----|----|---|------|
| 15         | 14 | 13 | 12 | 11 | 10 | 9 | 8    |
| RESERVED_1 |    |    |    |    |    |   | LLT2 |
| R          |    |    |    |    |    |   | R/W  |
| 0h         |    |    |    |    |    |   | 0h   |
| 7          | 6  | 5  | 4  | 3  | 2  | 1 | 0    |
|            |    |    |    |    |    |   | LLT2 |
|            |    |    |    |    |    |   | R/W  |
|            |    |    |    |    |    |   | 0h   |

**Table 3-1745. SDFM\_SDFLT3CMPL2 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                           |
|------|------------|------|-------|-----------------------------------------------------------------------|
| 15   | RESERVED_1 | R    | 0h    | Reserved                                                              |
| 14:0 | LLT2       | R/W  | 0h    | Second Unsigned low-level threshold for the comparator filter output. |

### 3.12.2.48 SDFM\_SDCTLPARM4 Register

#### 1 SDFM\_SDCTLPARM4 Register (Offset = 80h) [reset = 0h]

Control Parameter Register for Ch4.

Return to [Summary Table](#)

**Table 3-1746. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8080h       |
| SDFM1         | 5026 9080h       |

**Figure 3-560. SDFM\_SDCTLPARM4 Name Register**

|            |            |            |           |          |            |     |   |
|------------|------------|------------|-----------|----------|------------|-----|---|
| 15         | 14         | 13         | 12        | 11       | 10         | 9   | 8 |
| RESERVED_4 |            |            |           |          |            |     |   |
| R          |            |            |           |          |            |     |   |
| 0h         |            |            |           |          |            |     |   |
| 7          | 6          | 5          | 4         | 3        | 2          | 1   | 0 |
| RESERVED_3 | SDDATASYNC | RESERVED_2 | SDCLKSYNC | SDCLKSEL | RESERVED_1 | MOD |   |
| R          | R/W        | R          | R/W       | R/W      | R/W        | R/W |   |
| 0h         | 0h         | 0h         | 0h        | 0h       | 0h         | 0h  |   |

**Table 3-1748. SDFM\_SDCTLPARM4 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                           |
|------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | RESERVED_4 | R    | 0h    | Reserved                                                                                                                              |
| 7    | RESERVED_3 | R    | 0h    | Reserved                                                                                                                              |
| 6    | SDDATASYNC | R/W  | 0h    | 0: SD Data is not passed through a synchronizer.<br>1:SD Data is passed through a synchronizer.                                       |
| 5    | RESERVED_2 | R    | 0h    | Reserved                                                                                                                              |
| 4    | SDCLKSYNC  | R/W  | 0h    | 0: SD Clock is not passed through a synchronizer.<br>1:SD Clock is passed through a synchronizer.                                     |
| 3    | SDCLKSEL   | R/W  | 0h    | SD4 Clock source select.<br>0:Clock source to SDFM filter is its channel clock.<br>1:Clock source to SDFM filter is SD1 filter clock. |
| 2    | RESERVED_1 | R/W  | 0h    | Reserved                                                                                                                              |
| 1:0  | MOD        | R/W  | 0h    | Modulator clock modes<br>0:Mode<br>0:Modulator clock running at 1x data rate<br>1:Reserved<br>2:Reserved<br>3:Reserved                |

### 3.12.2.49 SDFM\_SDDFPARM4 Register

#### 1 SDFM\_SDDFPARM4 Register (Offset = 82h) [reset = 0h]

Data Filter Parameter Register for Ch4.

Return to [Summary Table](#)

**Table 3-1749. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8082h       |
| SDFM1         | 5026 9082h       |

**Figure 3-561. SDFM\_SDDFPARM4 Name Register**

| 15         | 14 | 13 | 12       | 11  | 10 | 9   | 8   |
|------------|----|----|----------|-----|----|-----|-----|
| RESERVED_1 |    |    | SDSYNCEN | SST |    | AE  | FEN |
| R          |    |    | R/W      | R/W |    | R/W | R/W |
| 0h         |    |    | 0h       | 0h  |    | 0h  | 0h  |
| 7          | 6  | 5  | 4        | 3   | 2  | 1   | 0   |
| DOSR       |    |    |          |     |    |     |     |
| R/W        |    |    |          |     |    |     |     |
| 0h         |    |    |          |     |    |     |     |

**Table 3-1751. SDFM\_SDDFPARM4 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                       |
|-------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                          |
| 12    | SDSYNCEN   | R/W  | 0h    | PWM synchronization [SDSYNC] of data filter<br>0: PWM synchronization of data filter is disabled<br>1: PWM synchronization of data filter is enabled<br>Note: SDSYNCS.SYNCSEL bits define which PWM signal is used to synchronize PWMs                                            |
| 11:10 | SST        | R/W  | 0h    | Data filter structure<br>00: Data filter runs with a Sincfast structure<br>01: Data filter runs with a Sinc1 structure<br>10: Data filter runs with a Sinc2 structure<br>11: Data filter runs with a Sinc3 structure                                                              |
| 9     | AE         | R/W  | 0h    | Data filter Acknowledge Enable<br>0: Acknowledge flag is disabled for the particular filter<br>1: Acknowledge flag is enabled for the particular filter                                                                                                                           |
| 8     | FEN        | R/W  | 0h    | Filter Enable<br>0: The data filter is disabled and no data is produced<br>1: The data filter is enabled and data are produced in the data filter<br>Note: When filter is disabled, DOSR counter held in reset, filter data erased. Also resets FIFO pointers and clears the FIFO |
| 7:0   | DOSR       | R/W  | 0h    | Data filter Oversampling ratio<br>The actual oversampling ratio of data filter is DOSR + 1<br>These bits set the oversampling ratio of the data filter.<br>0x0FF represents an oversampling ratio of 256.                                                                         |

### 3.12.2.50 SDFM\_SDDPARM4 Register

#### 1 SDFM\_SDDPARM4 Register (Offset = 84h) [reset = 0h]

Data Parameter Register for Ch4.

Return to [Summary Table](#)

**Table 3-1752. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8084h       |
| SDFM1         | 5026 9084h       |

**Figure 3-562. SDFM\_SDDPARM4 Name Register**

|    |    |     |    |    |     |   |            |
|----|----|-----|----|----|-----|---|------------|
| 15 | 14 | 13  | 12 | 11 | 10  | 9 | 8          |
|    |    | SH  |    |    | DR  |   | RESERVED_1 |
|    |    | R/W |    |    | R/W |   | R          |
|    |    | 0h  |    |    | 0h  |   | 0h         |
| 7  | 6  | 5   | 4  | 3  | 2   | 1 | 0          |
|    |    |     |    |    |     |   | RESERVED_1 |
|    |    |     |    |    |     |   | R          |
|    |    |     |    |    |     |   | 0h         |

**Table 3-1754. SDFM\_SDDPARM4 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                      |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | SH         | R/W  | 0h    | Shift Control<br>These bits indicate by how many bits the 16-bit window is shifted up when 16-bit data representation is chosen. |
| 10    | DR         | R/W  | 0h    | Data filter Data representation<br>0:Data stored in<br>16b2's complement<br>1:Data stored in<br>32b2's complement                |
| 9:0   | RESERVED_1 | R    | 0h    | Reserved                                                                                                                         |

### 3.12.2.51 SDFM\_SDFLT4CMPH1 Register

#### 1 SDFM\_SDFLT4CMPH1 Register (Offset = 86h) [reset = 7FFFh]

High-level Threshold Register for Ch4.

Return to [Summary Table](#)

**Table 3-1755. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8086h       |
| SDFM1         | 5026 9086h       |

**Figure 3-563. SDFM\_SDFLT4CMPH1 Name Register**

|            |    |    |    |       |    |   |   |
|------------|----|----|----|-------|----|---|---|
| 15         | 14 | 13 | 12 | 11    | 10 | 9 | 8 |
| RESERVED_1 |    |    |    | HLT   |    |   |   |
| R          |    |    |    | R/W   |    |   |   |
| 0h         |    |    |    | 7FFFh |    |   |   |
| 7          | 6  | 5  | 4  | 3     | 2  | 1 | 0 |
|            |    |    |    | HLT   |    |   |   |
|            |    |    |    | R/W   |    |   |   |
|            |    |    |    | 7FFFh |    |   |   |

**Table 3-1757. SDFM\_SDFLT4CMPH1 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                     |
|------|------------|------|-------|-----------------------------------------------------------------|
| 15   | RESERVED_1 | R    | 0h    | Reserved                                                        |
| 14:0 | HLT        | R/W  | 7FFFh | Unsigned high-level threshold for the comparator filter output. |



### 3.12.2.52 SDFM\_SDFLT4CMPL1 Register

#### 1 SDFM\_SDFLT4CMPL1 Register (Offset = 88h) [reset = 0h]

Low-level Threshold Register for Ch4.

Return to [Summary Table](#)

**Table 3-1758. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8088h       |
| SDFM1         | 5026 9088h       |

**Figure 3-564. SDFM\_SDFLT4CMPL1 Name Register**

|            |    |    |    |     |    |   |   |
|------------|----|----|----|-----|----|---|---|
| 15         | 14 | 13 | 12 | 11  | 10 | 9 | 8 |
| RESERVED_1 |    |    |    | LLT |    |   |   |
| R          |    |    |    | R/W |    |   |   |
| 0h         |    |    |    | 0h  |    |   |   |
| 7          | 6  | 5  | 4  | 3   | 2  | 1 | 0 |
|            |    |    |    | LLT |    |   |   |
|            |    |    |    | R/W |    |   |   |
|            |    |    |    | 0h  |    |   |   |

**Table 3-1760. SDFM\_SDFLT4CMPL1 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                    |
|------|------------|------|-------|----------------------------------------------------------------|
| 15   | RESERVED_1 | R    | 0h    | Reserved                                                       |
| 14:0 | LLT        | R/W  | 0h    | Unsigned low-level threshold for the comparator filter output. |

### 3.12.2.53 SDFM\_SDCPARM4 Register

#### 1 SDFM\_SDCPARM4 Register (Offset = 8Ah) [reset = 0h]

Comparator Filter Parameter Register for Ch4.

Return to [Summary Table](#)

**Table 3-1761. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 808Ah       |
| SDFM1         | 5026 908Ah       |

**Figure 3-565. SDFM\_SDCPARM4 Name Register**

|          |           |           |          |    |      |      |         |
|----------|-----------|-----------|----------|----|------|------|---------|
| 15       | 14        | 13        | 12       | 11 | 10   | 9    | 8       |
| CEVT2SEL |           | CEN       | CEVT1SEL |    | HZEN | MFIE | CS1_CS0 |
| R/W      |           | R/W       | R/W      |    | R/W  | R/W  | R/W     |
| 0h       |           | 0h        | 0h       |    | 0h   | 0h   | 0h      |
| 7        | 6         | 5         | 4        | 3  | 2    | 1    | 0       |
| CS1_CS0  | EN_C EVT2 | EN_C EVT1 |          |    | COSR |      |         |
| R/W      | R/W       | R/W       |          |    | R/W  |      |         |
| 0h       | 0h        | 0h        |          |    | 0h   |      |         |

**Table 3-1763. SDFM\_SDCPARM4 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                    |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | CEVT2SEL  | R/W  | 0h    | Comparator Event2 Select<br>00: COMPL1<br>01:COMPL1 OR COMPH1<br>10:COMPL2<br>11:COMPL2 OR COMPH2                                                                                                                                              |
| 13    | CEN       | R/W  | 0h    | Comparator Filter enable<br>0:Disable comparator filter<br>1:Enable comparator filter                                                                                                                                                          |
| 12:11 | CEVT1SEL  | R/W  | 0h    | Comparator Event1 Select<br>00: COMPH1<br>01:COMPL1 OR COMPH1<br>10:COMPH2<br>11:COMPL2 OR COMPH2                                                                                                                                              |
| 10    | HZEN      | R/W  | 0h    | High level [Z] Threshold crossing output enable<br>0:Disable Higher level Threshold [Z] crossing<br>1:Enable Higher level Threshold [Z] crossing                                                                                               |
| 9     | MFIE      | R/W  | 0h    | Modulator Failure Interrupt Enable<br>0:Disable modulator failure interrupt and its flag<br>1:Enable modulator failure interrupt and its flag                                                                                                  |
| 8:7   | CS1_CS0   | R/W  | 0h    | Comparator filter structure<br>00:Comparator filter runs with a sincfast structure<br>01:Comparator filter runs with a Sinc1 structure<br>10:Comparator filter runs with a Sinc2 structure<br>11:Comparator filter runs with a Sinc3 structure |
| 6     | EN_C EVT2 | R/W  | 0h    | CEVT2 interrupt enable<br>0:Disable CEVT2 interrupt<br>1:Enable CEVT2 interrupt                                                                                                                                                                |
| 5     | EN_C EVT1 | R/W  | 0h    | CEVT1 interrupt enable<br>0:Disable CEVT1 interrupt<br>1:Enable CEVT1 interrupt                                                                                                                                                                |

**Table 3-1763. SDFM\_SDCPARM4 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                           |
|-----|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | COSR  | R/W  | 0h    | Comparator Oversampling ratio.<br>The actual rate is COSR + 1.<br>These bits set the oversampling ratio of the filter.<br>0x1F represents an oversampling ratio of 32 |

### 3.12.2.54 SDFM\_SDDATA4 Register

#### 1 SDFM\_SDDATA4 Register (Offset = 8Ch) [reset = 0h]

Data Filter Data Register (16 or 32bit) for Ch4.

Return to [Summary Table](#)

**Table 3-1764. Instance Table**

| Instance Name | Physical Address  |
|---------------|-------------------|
| <b>SDFM0</b>  | <b>5026 808Ch</b> |
| <b>SDFM1</b>  | <b>5026 908Ch</b> |

**Figure 3-566. SDFM\_SDDATA4 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DATA32HI |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DATA32HI |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DATA16   |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DATA16   |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 3-1766. SDFM\_SDDATA4 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                             |
|-------|----------|------|-------|---------------------------------------------------------|
| 31:16 | DATA32HI | R    | 0h    | Hi-order<br>16bin<br>32bmode, 16-bit Data in<br>16bmode |
| 15:0  | DATA16   | R    | 0h    | Lo-order<br>16bin<br>32bmode                            |

### 3.12.2.55 SDFM\_SDDATFIFO4 Register

#### 1 SDFM\_SDDATFIFO4 Register (Offset = 90h) [reset = 0h]

Filter Data FIFO Output(32b) for Ch4.

Return to [Summary Table](#)

**Table 3-1767. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8090h       |
| SDFM1         | 5026 9090h       |

**Figure 3-567. SDFM\_SDDATFIFO4 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DATA32HI |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DATA32HI |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DATA16   |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DATA16   |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 3-1769. SDFM\_SDDATFIFO4 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                             |
|-------|----------|------|-------|---------------------------------------------------------|
| 31:16 | DATA32HI | R    | 0h    | Hi-order<br>16bin<br>32bmode, 16-bit Data in<br>16bmode |
| 15:0  | DATA16   | R    | 0h    | Lo-order<br>16bin<br>32bmode                            |

### 3.12.2.56 SDFM\_SDCDATA4 Register

#### 1 SDFM\_SDCDATA4 Register (Offset = 94h) [reset = 0h]

Comparator Filter Data Register (16b) for Ch4.

Return to [Summary Table](#)

**Table 3-1770. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8094h       |
| SDFM1         | 5026 9094h       |

**Figure 3-568. SDFM\_SDCDATA4 Name Register**

|        |    |    |    |    |    |   |   |
|--------|----|----|----|----|----|---|---|
| 15     | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DATA16 |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |
| 7      | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| DATA16 |    |    |    |    |    |   |   |
| R      |    |    |    |    |    |   |   |
| 0h     |    |    |    |    |    |   |   |

**Table 3-1772. SDFM\_SDCDATA4 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                      |
|------|--------|------|-------|----------------------------------|
| 15:0 | DATA16 | R    | 0h    | Comparator Data output - 16bonly |

### 3.12.2.57 SDFM\_SDFLT4CMPH2 Register

#### 1 SDFM\_SDFLT4CMPH2 Register (Offset = 96h) [reset = 7FFFh]

Second high level threshold for CH4.

Return to [Summary Table](#)

**Table 3-1773. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8096h       |
| SDFM1         | 5026 9096h       |

**Figure 3-569. SDFM\_SDFLT4CMPH2 Name Register**

|            |       |    |    |    |    |   |   |
|------------|-------|----|----|----|----|---|---|
| 15         | 14    | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED_1 | HLT2  |    |    |    |    |   |   |
| R          | R/W   |    |    |    |    |   |   |
| 0h         | 7FFFh |    |    |    |    |   |   |
| 7          | 6     | 5  | 4  | 3  | 2  | 1 | 0 |
| HLT2       |       |    |    |    |    |   |   |
| R/W        |       |    |    |    |    |   |   |
| 7FFFh      |       |    |    |    |    |   |   |

**Table 3-1775. SDFM\_SDFLT4CMPH2 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                            |
|------|------------|------|-------|------------------------------------------------------------------------|
| 15   | RESERVED_1 | R    | 0h    | Reserved                                                               |
| 14:0 | HLT2       | R/W  | 7FFFh | Second Unsigned high-level threshold for the comparator filter output. |

### 3.12.2.58 SDFM\_SDFLT4CMPHZ Register

#### 1 SDFM\_SDFLT4CMPHZ Register (Offset = 98h) [reset = 0h]

High-level (Z) Threshold Register for Ch4.

Return to [Summary Table](#)

**Table 3-1776. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 8098h       |
| SDFM1         | 5026 9098h       |

**Figure 3-570. SDFM\_SDFLT4CMPHZ Name Register**

|            |      |    |    |    |    |   |   |
|------------|------|----|----|----|----|---|---|
| 15         | 14   | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED_1 | HLTZ |    |    |    |    |   |   |
| R          | R/W  |    |    |    |    |   |   |
| 0h         | 0h   |    |    |    |    |   |   |
| 7          | 6    | 5  | 4  | 3  | 2  | 1 | 0 |
| HLTZ       |      |    |    |    |    |   |   |
| R/W        |      |    |    |    |    |   |   |
| 0h         |      |    |    |    |    |   |   |

**Table 3-1778. SDFM\_SDFLT4CMPHZ Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                |
|------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                   |
| 14:0 | HLTZ       | R/W  | 0h    | Unsigned High-level threshold [Z] for the comparator filter output. Primarily intended for detecting "zero"-crossing events. Unlike the primary comparator SDCMPHx, it does not have the ability to generate an interrupt. |



### 3.12.2.59 SDFM\_SDFIFOCTL4 Register

#### 1 SDFM\_SDFIFOCTL4 Register (Offset = 9Ah) [reset = 0h]

FIFO Control Register for Ch4.

Return to [Summary Table](#)

**Table 3-1779. Instance Table**

| Instance Name | Physical Address  |
|---------------|-------------------|
| <b>SDFM0</b>  | <b>5026 809Ah</b> |
| <b>SDFM1</b>  | <b>5026 909Ah</b> |

**Figure 3-571. SDFM\_SDFIFOCTL4 Name Register**

|        |          |            |        |            |        |   |   |
|--------|----------|------------|--------|------------|--------|---|---|
| 15     | 14       | 13         | 12     | 11         | 10     | 9 | 8 |
| OVFIEN | DRINTSEL | FFEN       | FFIEN  | RESERVED_2 | SDFFST |   |   |
| R/W    | R/W      | R/W        | R/W    | R          | R      |   |   |
| 0h     | 0h       | 0h         | 0h     | 0h         | 0h     |   |   |
| 7      | 6        | 5          | 4      | 3          | 2      | 1 | 0 |
| SDFFST |          | RESERVED_1 | SDFFIL |            |        |   |   |
| R      |          | R          | R/W    |            |        |   |   |
| 0h     |          | 0h         | 0h     |            |        |   |   |

**Table 3-1781. SDFM\_SDFIFOCTL4 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                       |
|------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | OVFIEN     | R/W  | 0h    | SDFIFO Overflow interrupt enable<br>0: SDFIFO Overflow condition will not generate an interrupt<br>1: SDFIFO overflow condition generates an interrupt on SDy_ERR |
| 14   | DRINTSEL   | R/W  | 0h    | Data-Ready Interrupt [DRINT] source select<br>0 = AF1 [Select non-FIFO data-ready interrupt]<br>1 = SDFINT1 [Select FIFO data-ready interrupt]                    |
| 13   | FFEN       | R/W  | 0h    | SDFIFO Enable<br>0: Disable FIFO operation<br>1: Enable FIFO operation<br>Note: When FIFO is disabled, FIFO contents are cleared                                  |
| 12   | FFIEN      | R/W  | 0h    | SDFIFO data ready Interrupt Enable                                                                                                                                |
| 11   | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                          |
| 10:6 | SDFFST     | R    | 0h    | SDFIFO Status<br>00000 FIFO empty<br>00001 FIFO has 1 word<br>.....<br>10000 FIFO has 16 words                                                                    |
| 5    | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                          |
| 4:0  | SDFFIL     | R/W  | 0h    | SDFIFO interrupt level bits<br>The FIFO will generate an interrupt when the FIFO status [SDFFST] != FIFO level [SDFFIL]                                           |

### 3.12.2.60 SDFM\_SDSYNC4 Register

#### 1 SDFM\_SDSYNC4 Register (Offset = 9Ch) [reset = 400h]

SD Filter Sync control for Ch4.

Return to [Summary Table](#)

**Table 3-1782. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 809Ch       |
| SDFM1         | 5026 909Ch       |

**Figure 3-572. SDFM\_SDSYNC4 Name Register**

| 15         | 14      | 13      | 12 | 11 | 10       | 9          | 8        |
|------------|---------|---------|----|----|----------|------------|----------|
| RESERVED_1 |         |         |    |    | WTSCLREN | FFSYNCLREN | WTSYNCLR |
| R          |         |         |    |    | R/W      | R/W        | R/W      |
| 0h         |         |         |    |    | 1h       | 0h         | 0h       |
| 7          | 6       | 5       | 4  | 3  | 2        | 1          | 0        |
| WTSYNFLG   | WTSYNEN | SYNCSEL |    |    |          |            |          |
| R          | R/W     | R/W     |    |    |          |            |          |
| 0h         | 0h      | 0h      |    |    |          |            |          |

**Table 3-1784. SDFM\_SDSYNC4 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                              |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:11 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                 |
| 10    | WTSCLREN   | R/W  | 1h    | WTSYNFLG Clear-on-FIFOINT Enable<br>0:WTSYNFLG can only be cleared manually [using WTSYNCLR bit]<br>1:WTSYNFLG is cleared automatically on SDFINT                        |
| 9     | FFSYNCLREN | R/W  | 0h    | FIFO Clear-on-SDSYNC Enable<br>0:SDFIFO is not automatically cleared upon receiving SDSYNC<br>1:SDFIFO is automatically cleared upon receiving SDSYNC                    |
| 8     | WTSYNCLR   | R/W  | 0h    | Wait-for-Sync Flag Clear [always reads 0]<br>0:Write of 0 has no effect<br>1:Write of 1 clears WTSYNFLG                                                                  |
| 7     | WTSYNFLG   | R    | 0h    | Wait-for-Sync Flag<br>0:SDSYNC event has not occurred<br>1:SDSYNC event occurred.                                                                                        |
| 6     | WTSYNEN    | R/W  | 0h    | Wait-for-Sync Enable<br>0:Incoming Data written to SDFIFO on every Data-Ready [DR] Event<br>1:Incoming Data written to SDFIFO on DR event only after SDSYNC event occurs |
| 5:0   | SYNCSEL    | R/W  | 0h    | Defines source for the SDSYNC Input on this channel<br>Refer SDSYNcx.SYNCSEL table                                                                                       |

### 3.12.2.61 SDFM\_SDFLT4CMPL2 Register

#### 1 SDFM\_SDFLT4CMPL2 Register (Offset = 9Eh) [reset = 0h]

Second low level threshold for CH4.

Return to [Summary Table](#)

**Table 3-1785. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 809Eh       |
| SDFM1         | 5026 909Eh       |

**Figure 3-573. SDFM\_SDFLT4CMPL2 Name Register**

|            |      |    |    |    |    |   |   |
|------------|------|----|----|----|----|---|---|
| 15         | 14   | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED_1 | LLT2 |    |    |    |    |   |   |
| R          | R/W  |    |    |    |    |   |   |
| 0h         | 0h   |    |    |    |    |   |   |
| 7          | 6    | 5  | 4  | 3  | 2  | 1 | 0 |
| LLT2       |      |    |    |    |    |   |   |
| R/W        |      |    |    |    |    |   |   |
| 0h         |      |    |    |    |    |   |   |

**Table 3-1787. SDFM\_SDFLT4CMPL2 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                           |
|------|------------|------|-------|-----------------------------------------------------------------------|
| 15   | RESERVED_1 | R    | 0h    | Reserved                                                              |
| 14:0 | LLT2       | R/W  | 0h    | Second Unsigned low-level threshold for the comparator filter output. |

### 3.12.2.62 SDFM\_SDCOMP1CTL Register

#### 1 SDFM\_SDCOMP1CTL Register (Offset = C0h) [reset = 0h]

SD Comparator event filter1 Control Register.

Return to [Summary Table](#)

**Table 3-1788. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 80C0h       |
| SDFM1         | 5026 90C0h       |

**Figure 3-574. SDFM\_SDCOMP1CTL Name Register**

| 15          | 14         | 13         | 12              | 11         | 10         | 9 | 8 |
|-------------|------------|------------|-----------------|------------|------------|---|---|
| RESERVED_10 | RESERVED_9 | RESERVED_8 | CEVT2DIGFILTSEL | RESERVED_7 | RESERVED_6 |   |   |
| R           | R          | R          | R/W             | R          | R          |   |   |
| 0h          | 0h         | 0h         | 0h              | 0h         | 0h         |   |   |
| 7           | 6          | 5          | 4               | 3          | 2          | 1 | 0 |
| RESERVED_5  | RESERVED_4 | RESERVED_3 | CEVT1DIGFILTSEL | RESERVED_2 | RESERVED_1 |   |   |
| R           | R          | R          | R/W             | R          | R          |   |   |
| 0h          | 0h         | 0h         | 0h              | 0h         | 0h         |   |   |

**Table 3-1790. SDFM\_SDCOMP1CTL Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                      |
|-------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | RESERVED_10     | R    | 0h    | Reserved                                                                                                                                         |
| 14    | RESERVED_9      | R    | 0h    | Reserved                                                                                                                                         |
| 13:12 | RESERVED_8      | R    | 0h    | Reserved                                                                                                                                         |
| 11:10 | CEVT2DIGFILTSEL | R/W  | 0h    | High comparator COMPH source select.<br>0 CEVT2 output drives COMPLOUT<br>1 Reserved<br>2 Output of digital filter drives COMPLOUT<br>3 Reserved |
| 9     | RESERVED_7      | R    | 0h    | Reserved                                                                                                                                         |
| 8     | RESERVED_6      | R    | 0h    | Reserved                                                                                                                                         |
| 7     | RESERVED_5      | R    | 0h    | Reserved                                                                                                                                         |
| 6     | RESERVED_4      | R    | 0h    | Reserved                                                                                                                                         |
| 5:4   | RESERVED_3      | R    | 0h    | Reserved                                                                                                                                         |
| 3:2   | CEVT1DIGFILTSEL | R/W  | 0h    | High comparator COMPH source select.<br>0 CEVT1 output drives COMPHOUT<br>1 Reserved<br>2 Output of digital filter drives COMPHOUT<br>3 Reserved |
| 1     | RESERVED_2      | R    | 0h    | Reserved                                                                                                                                         |
| 0     | RESERVED_1      | R    | 0h    | Reserved                                                                                                                                         |

### 3.12.2.63 SDFM\_SDCOMP1EVT2FLTCTL Register

#### 1 SDFM\_SDCOMP1EVT2FLTCTL Register (Offset = C2h) [reset = 0h]

COMPL/CEVT2 Digital filter1 Control Register.

Return to [Summary Table](#)

**Table 3-1791. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 80C2h       |
| SDFM1         | 5026 90C2h       |

**Figure 3-575. SDFM\_SDCOMP1EVT2FLTCTL Name Register**

| 15      | 14         | 13     | 12 | 11         | 10 | 9 | 8       |
|---------|------------|--------|----|------------|----|---|---------|
| FILINIT | RESERVED_2 | THRESH |    |            |    |   | SAMPWIN |
| R/W1TS  | R          | R/W    |    |            |    |   | R/W     |
| 0h      | 0h         | 0h     |    |            |    |   | 0h      |
| 7       | 6          | 5      | 4  | 3          | 2  | 1 | 0       |
| SAMPWIN |            |        |    | RESERVED_1 |    |   |         |
| R/W     |            |        |    | R          |    |   |         |
| 0h      |            |        |    | 0h         |    |   |         |

**Table 3-1793. SDFM\_SDCOMP1EVT2FLTCTL Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                       |
|------|------------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | FILINIT    | R/W1TS | 0h    | Low filter initialization.<br>0 No effect<br>1 Initialize all samples to the filter input value                                                                   |
| 14   | RESERVED_2 | R      | 0h    | Reserved                                                                                                                                                          |
| 13:9 | THRESH     | R/W    | 0h    | Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. |
| 8:4  | SAMPWIN    | R/W    | 0h    | Low filter sample window size. Number of samples to monitor is SAMPWIN+1.                                                                                         |
| 3:0  | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                          |

### 3.12.2.64 SDFM\_SDCOMP1EVT2FLTCLKCTL Register

#### 1 SDFM\_SDCOMP1EVT2FLTCLKCTL Register (Offset = C4h) [reset = 0h]

COMPL/CEVT2 Digital filter1 Clock Control Register.

Return to [Summary Table](#)

**Table 3-1794. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 80C4h       |
| SDFM1         | 5026 90C4h       |

**Figure 3-576. SDFM\_SDCOMP1EVT2FLTCLKCTL Name Register**

|             |    |    |    |    |    |             |   |
|-------------|----|----|----|----|----|-------------|---|
| 15          | 14 | 13 | 12 | 11 | 10 | 9           | 8 |
| RESERVED_1  |    |    |    |    |    | CLKPRESCALE |   |
| R           |    |    |    |    |    | R/W         |   |
| 0h          |    |    |    |    |    | 0h          |   |
| 7           | 6  | 5  | 4  | 3  | 2  | 1           | 0 |
| CLKPRESCALE |    |    |    |    |    |             |   |
| R/W         |    |    |    |    |    |             |   |
| 0h          |    |    |    |    |    |             |   |

**Table 3-1796. SDFM\_SDCOMP1EVT2FLTCLKCTL Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                |
|-------|-------------|------|-------|----------------------------------------------------------------------------|
| 15:10 | RESERVED_1  | R    | 0h    | Reserved                                                                   |
| 9:0   | CLKPRESCALE | R/W  | 0h    | Low filter sample clock prescale. Number of system clocks between samples. |

### 3.12.2.65 SDFM\_SDCOMP1EVT1FLTCTL Register

#### 1 SDFM\_SDCOMP1EVT1FLTCTL Register (Offset = C6h) [reset = 0h]

COMP/CEVT1 Digital filter1 Control Register.

Return to [Summary Table](#)

**Table 3-1797. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 80C6h       |
| SDFM1         | 5026 90C6h       |

**Figure 3-577. SDFM\_SDCOMP1EVT1FLTCTL Name Register**

| 15      | 14         | 13     | 12 | 11         | 10 | 9 | 8       |
|---------|------------|--------|----|------------|----|---|---------|
| FILINIT | RESERVED_2 | THRESH |    |            |    |   | SAMPWIN |
| R/W1TS  | R          | R/W    |    |            |    |   | R/W     |
| 0h      | 0h         | 0h     |    |            |    |   | 0h      |
| 7       | 6          | 5      | 4  | 3          | 2  | 1 | 0       |
| SAMPWIN |            |        |    | RESERVED_1 |    |   |         |
| R/W     |            |        |    | R          |    |   |         |
| 0h      |            |        |    | 0h         |    |   |         |

**Table 3-1799. SDFM\_SDCOMP1EVT1FLTCTL Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                        |
|------|------------|--------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | FILINIT    | R/W1TS | 0h    | High filter initialization.<br>0 No effect<br>1 Initialize all samples to the filter input value                                                                   |
| 14   | RESERVED_2 | R      | 0h    | Reserved                                                                                                                                                           |
| 13:9 | THRESH     | R/W    | 0h    | High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. |
| 8:4  | SAMPWIN    | R/W    | 0h    | High filter sample window size. Number of samples to monitor is SAMPWIN+1.                                                                                         |
| 3:0  | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                           |

### 3.12.2.66 SDFM\_SDCOMP1EVT1FLTCLKCTL Register

#### 1 SDFM\_SDCOMP1EVT1FLTCLKCTL Register (Offset = C8h) [reset = 0h]

COMP/CEVT1 Digital filter1 Clock Control Register.

Return to [Summary Table](#)

**Table 3-1800. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 80C8h       |
| SDFM1         | 5026 90C8h       |

**Figure 3-578. SDFM\_SDCOMP1EVT1FLTCLKCTL Name Register**

|             |    |    |    |    |    |             |   |
|-------------|----|----|----|----|----|-------------|---|
| 15          | 14 | 13 | 12 | 11 | 10 | 9           | 8 |
| RESERVED_1  |    |    |    |    |    | CLKPRESCALE |   |
| R           |    |    |    |    |    | R/W         |   |
| 0h          |    |    |    |    |    | 0h          |   |
| 7           | 6  | 5  | 4  | 3  | 2  | 1           | 0 |
| CLKPRESCALE |    |    |    |    |    |             |   |
| R/W         |    |    |    |    |    |             |   |
| 0h          |    |    |    |    |    |             |   |

**Table 3-1802. SDFM\_SDCOMP1EVT1FLTCLKCTL Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                 |
|-------|-------------|------|-------|-----------------------------------------------------------------------------|
| 15:10 | RESERVED_1  | R    | 0h    | Reserved                                                                    |
| 9:0   | CLKPRESCALE | R/W  | 0h    | High filter sample clock prescale. Number of system clocks between samples. |



### 3.12.2.67 SDFM\_SDCOMP1LOCK Register

#### 1 SDFM\_SDCOMP1LOCK Register (Offset = CEh) [reset = 0h]

SD compartor event filter1 Lock Register.

Return to [Summary Table](#)

**Table 3-1803. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 80CEh       |
| SDFM1         | 5026 90CEh       |

**Figure 3-579. SDFM\_SDCOMP1LOCK Name Register**

|            |    |    |            |        |            |            |            |
|------------|----|----|------------|--------|------------|------------|------------|
| 15         | 14 | 13 | 12         | 11     | 10         | 9          | 8          |
| RESERVED_4 |    |    |            |        |            |            |            |
| R          |    |    |            |        |            |            |            |
| 0h         |    |    |            |        |            |            |            |
| 7          | 6  | 5  | 4          | 3      | 2          | 1          | 0          |
| RESERVED_4 |    |    | RESERVED_3 | COMP   | RESERVED_2 | RESERVED_1 | SDCOMP1CTL |
| R          |    |    | R          | R/W1TS | R          | R          | R/W1TS     |
| 0h         |    |    | 0h         | 0h     | 0h         | 0h         | 0h         |

**Table 3-1805. SDFM\_SDCOMP1LOCK Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                                                                   |
|------|------------|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:5 | RESERVED_4 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                      |
| 4    | RESERVED_3 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                      |
| 3    | COMP       | R/W1TS | 0h    | Lock write-access to the SDCOMP1EVT1/2FLTCTL and COMP1FILCLKCTL registers.<br>0 SDCOMP1EVT1/2FLTCTL and SDCOMP1EVT1/2FLTCLKCTL registers are not locked. Write 0 to this bit has no effect.<br>1 SDCOMP1EVT1/2FLTCTL and SDCOMP1EVT1/2FLTCLKCTL registers are locked. Only a system reset can clear this bit. |
| 2    | RESERVED_2 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                      |
| 1    | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                      |
| 0    | SDCOMP1CTL | R/W1TS | 0h    | Lock write-access to the SDCOMP1CTL register.<br>0 SDCOMP1CTL register is not locked. Write 0 to this bit has no effect.<br>1 SDCOMP1CTL register is locked. Only a system reset can clear this bit.                                                                                                          |

### 3.12.2.68 SDFM\_SDCOMP2CTL Register

#### 1 SDFM\_SDCOMP2CTL Register (Offset = D0h) [reset = 0h]

SD Comparator event filter2 Control Register.

Return to [Summary Table](#)

**Table 3-1806. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 80D0h       |
| SDFM1         | 5026 90D0h       |

**Figure 3-580. SDFM\_SDCOMP2CTL Name Register**

| 15          | 14         | 13         | 12              | 11         | 10         | 9 | 8 |
|-------------|------------|------------|-----------------|------------|------------|---|---|
| RESERVED_10 | RESERVED_9 | RESERVED_8 | CEVT2DIGFILTSEL | RESERVED_7 | RESERVED_6 |   |   |
| R           | R          | R          | R/W             | R          | R          |   |   |
| 0h          | 0h         | 0h         | 0h              | 0h         | 0h         |   |   |
| 7           | 6          | 5          | 4               | 3          | 2          | 1 | 0 |
| RESERVED_5  | RESERVED_4 | RESERVED_3 | CEVT1DIGFILTSEL | RESERVED_2 | RESERVED_1 |   |   |
| R           | R          | R          | R/W             | R          | R          |   |   |
| 0h          | 0h         | 0h         | 0h              | 0h         | 0h         |   |   |

**Table 3-1808. SDFM\_SDCOMP2CTL Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                      |
|-------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | RESERVED_10     | R    | 0h    | Reserved                                                                                                                                         |
| 14    | RESERVED_9      | R    | 0h    | Reserved                                                                                                                                         |
| 13:12 | RESERVED_8      | R    | 0h    | Reserved                                                                                                                                         |
| 11:10 | CEVT2DIGFILTSEL | R/W  | 0h    | High comparator COMPH source select.<br>0 CEVT2 output drives COMPLOUT<br>1 Reserved<br>2 Output of digital filter drives COMPLOUT<br>3 Reserved |
| 9     | RESERVED_7      | R    | 0h    | Reserved                                                                                                                                         |
| 8     | RESERVED_6      | R    | 0h    | Reserved                                                                                                                                         |
| 7     | RESERVED_5      | R    | 0h    | Reserved                                                                                                                                         |
| 6     | RESERVED_4      | R    | 0h    | Reserved                                                                                                                                         |
| 5:4   | RESERVED_3      | R    | 0h    | Reserved                                                                                                                                         |
| 3:2   | CEVT1DIGFILTSEL | R/W  | 0h    | High comparator COMPH source select.<br>0 CEVT1 output drives COMPHOUT<br>1 Reserved<br>2 Output of digital filter drives COMPHOUT<br>3 Reserved |
| 1     | RESERVED_2      | R    | 0h    | Reserved                                                                                                                                         |
| 0     | RESERVED_1      | R    | 0h    | Reserved                                                                                                                                         |

### 3.12.2.69 SDFM\_SDCOMP2EVT2FLTCTL Register

#### 1 SDFM\_SDCOMP2EVT2FLTCTL Register (Offset = D2h) [reset = 0h]

COMPL/CEVT2 Digital filter2 Control Register.

Return to [Summary Table](#)

**Table 3-1809. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 80D2h       |
| SDFM1         | 5026 90D2h       |

**Figure 3-581. SDFM\_SDCOMP2EVT2FLTCTL Name Register**

| 15      | 14         | 13     | 12 | 11         | 10 | 9 | 8       |
|---------|------------|--------|----|------------|----|---|---------|
| FILINIT | RESERVED_2 | THRESH |    |            |    |   | SAMPWIN |
| R/W1TS  | R          | R/W    |    |            |    |   | R/W     |
| 0h      | 0h         | 0h     |    |            |    |   | 0h      |
| 7       | 6          | 5      | 4  | 3          | 2  | 1 | 0       |
| SAMPWIN |            |        |    | RESERVED_1 |    |   |         |
| R/W     |            |        |    | R          |    |   |         |
| 0h      |            |        |    | 0h         |    |   |         |

**Table 3-1811. SDFM\_SDCOMP2EVT2FLTCTL Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                       |
|------|------------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | FILINIT    | R/W1TS | 0h    | Low filter initialization.<br>0 No effect<br>1 Initialize all samples to the filter input value                                                                   |
| 14   | RESERVED_2 | R      | 0h    | Reserved                                                                                                                                                          |
| 13:9 | THRESH     | R/W    | 0h    | Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. |
| 8:4  | SAMPWIN    | R/W    | 0h    | Low filter sample window size. Number of samples to monitor is SAMPWIN+1.                                                                                         |
| 3:0  | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                          |

### 3.12.2.70 SDFM\_SDCOMP2EVT2FLTCLKCTL Register

#### 1 SDFM\_SDCOMP2EVT2FLTCLKCTL Register (Offset = D4h) [reset = 0h]

COMPL/CEVT2 Digital filter2 Clock Control Register.

Return to [Summary Table](#)

**Table 3-1812. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 80D4h       |
| SDFM1         | 5026 90D4h       |

**Figure 3-582. SDFM\_SDCOMP2EVT2FLTCLKCTL Name Register**

|             |    |    |    |    |    |             |   |
|-------------|----|----|----|----|----|-------------|---|
| 15          | 14 | 13 | 12 | 11 | 10 | 9           | 8 |
| RESERVED_1  |    |    |    |    |    | CLKPRESCALE |   |
| R           |    |    |    |    |    | R/W         |   |
| 0h          |    |    |    |    |    | 0h          |   |
| 7           | 6  | 5  | 4  | 3  | 2  | 1           | 0 |
| CLKPRESCALE |    |    |    |    |    |             |   |
| R/W         |    |    |    |    |    |             |   |
| 0h          |    |    |    |    |    |             |   |

**Table 3-1814. SDFM\_SDCOMP2EVT2FLTCLKCTL Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                |
|-------|-------------|------|-------|----------------------------------------------------------------------------|
| 15:10 | RESERVED_1  | R    | 0h    | Reserved                                                                   |
| 9:0   | CLKPRESCALE | R/W  | 0h    | Low filter sample clock prescale. Number of system clocks between samples. |

### 3.12.2.71 SDFM\_SDCOMP2EVT1FLTCTL Register

#### 1 SDFM\_SDCOMP2EVT1FLTCTL Register (Offset = D6h) [reset = 0h]

COMP/CEVT1 Digital filter2 Control Register.

Return to [Summary Table](#)

**Table 3-1815. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 80D6h       |
| SDFM1         | 5026 90D6h       |

**Figure 3-583. SDFM\_SDCOMP2EVT1FLTCTL Name Register**

| 15      | 14         | 13     | 12 | 11         | 10 | 9 | 8       |
|---------|------------|--------|----|------------|----|---|---------|
| FILINIT | RESERVED_2 | THRESH |    |            |    |   | SAMPWIN |
| R/W1TS  | R          | R/W    |    |            |    |   | R/W     |
| 0h      | 0h         | 0h     |    |            |    |   | 0h      |
| 7       | 6          | 5      | 4  | 3          | 2  | 1 | 0       |
| SAMPWIN |            |        |    | RESERVED_1 |    |   |         |
| R/W     |            |        |    | R          |    |   |         |
| 0h      |            |        |    | 0h         |    |   |         |

**Table 3-1817. SDFM\_SDCOMP2EVT1FLTCTL Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                        |
|------|------------|--------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | FILINIT    | R/W1TS | 0h    | High filter initialization.<br>0 No effect<br>1 Initialize all samples to the filter input value                                                                   |
| 14   | RESERVED_2 | R      | 0h    | Reserved                                                                                                                                                           |
| 13:9 | THRESH     | R/W    | 0h    | High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. |
| 8:4  | SAMPWIN    | R/W    | 0h    | High filter sample window size. Number of samples to monitor is SAMPWIN+1.                                                                                         |
| 3:0  | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                           |

### 3.12.2.72 SDFM\_SDCOMP2EVT1FLTCLKCTL Register

#### 1 SDFM\_SDCOMP2EVT1FLTCLKCTL Register (Offset = D8h) [reset = 0h]

COMP/CEVT1 Digital filter2 Clock Control Register.

Return to [Summary Table](#)

**Table 3-1818. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 80D8h       |
| SDFM1         | 5026 90D8h       |

**Figure 3-584. SDFM\_SDCOMP2EVT1FLTCLKCTL Name Register**

|             |    |    |    |    |    |             |   |
|-------------|----|----|----|----|----|-------------|---|
| 15          | 14 | 13 | 12 | 11 | 10 | 9           | 8 |
| RESERVED_1  |    |    |    |    |    | CLKPRESCALE |   |
| R           |    |    |    |    |    | R/W         |   |
| 0h          |    |    |    |    |    | 0h          |   |
| 7           | 6  | 5  | 4  | 3  | 2  | 1           | 0 |
| CLKPRESCALE |    |    |    |    |    |             |   |
| R/W         |    |    |    |    |    |             |   |
| 0h          |    |    |    |    |    |             |   |

**Table 3-1820. SDFM\_SDCOMP2EVT1FLTCLKCTL Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                 |
|-------|-------------|------|-------|-----------------------------------------------------------------------------|
| 15:10 | RESERVED_1  | R    | 0h    | Reserved                                                                    |
| 9:0   | CLKPRESCALE | R/W  | 0h    | High filter sample clock prescale. Number of system clocks between samples. |

### 3.12.2.73 SDFM\_SDCOMP2LOCK Register

#### 1 SDFM\_SDCOMP2LOCK Register (Offset = DEh) [reset = 0h]

SD compartor event filter2 Lock Register.

Return to [Summary Table](#)

**Table 3-1821. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 80DEh       |
| SDFM1         | 5026 90DEh       |

**Figure 3-585. SDFM\_SDCOMP2LOCK Name Register**

|            |    |    |            |        |            |            |            |
|------------|----|----|------------|--------|------------|------------|------------|
| 15         | 14 | 13 | 12         | 11     | 10         | 9          | 8          |
| RESERVED_4 |    |    |            |        |            |            |            |
| R          |    |    |            |        |            |            |            |
| 0h         |    |    |            |        |            |            |            |
| 7          | 6  | 5  | 4          | 3      | 2          | 1          | 0          |
| RESERVED_4 |    |    | RESERVED_3 | COMP   | RESERVED_2 | RESERVED_1 | SDCOMP2CTL |
| R          |    |    | R          | R/W1TS | R          | R          | R/W1TS     |
| 0h         |    |    | 0h         | 0h     | 0h         | 0h         | 0h         |

**Table 3-1823. SDFM\_SDCOMP2LOCK Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                                                                   |
|------|------------|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:5 | RESERVED_4 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                      |
| 4    | RESERVED_3 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                      |
| 3    | COMP       | R/W1TS | 0h    | Lock write-access to the SDCOMP2EVT1/2FLTCTL and COMP2FILCLKCTL registers.<br>0 SDCOMP2EVT1/2FLTCTL and SDCOMP2EVT1/2FLTCLKCTL registers are not locked. Write 0 to this bit has no effect.<br>1 SDCOMP2EVT1/2FLTCTL and SDCOMP2EVT1/2FLTCLKCTL registers are locked. Only a system reset can clear this bit. |
| 2    | RESERVED_2 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                      |
| 1    | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                      |
| 0    | SDCOMP2CTL | R/W1TS | 0h    | Lock write-access to the SDCOMP2CTL register.<br>0 SDCOMP2CTL register is not locked. Write 0 to this bit has no effect.<br>1 SDCOMP2CTL register is locked. Only a system reset can clear this bit.                                                                                                          |

### 3.12.2.74 SDFM\_SDCOMP3CTL Register

#### 1 SDFM\_SDCOMP3CTL Register (Offset = E0h) [reset = 0h]

SD Comparator event filter3 Control Register.

Return to [Summary Table](#)

**Table 3-1824. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 80E0h       |
| SDFM1         | 5026 90E0h       |

**Figure 3-586. SDFM\_SDCOMP3CTL Name Register**

| 15          | 14         | 13         | 12              | 11         | 10         | 9 | 8 |
|-------------|------------|------------|-----------------|------------|------------|---|---|
| RESERVED_10 | RESERVED_9 | RESERVED_8 | CEVT2DIGFILTSEL | RESERVED_7 | RESERVED_6 |   |   |
| R           | R          | R          | R/W             | R          | R          |   |   |
| 0h          | 0h         | 0h         | 0h              | 0h         | 0h         |   |   |
| 7           | 6          | 5          | 4               | 3          | 2          | 1 | 0 |
| RESERVED_5  | RESERVED_4 | RESERVED_3 | CEVT1DIGFILTSEL | RESERVED_2 | RESERVED_1 |   |   |
| R           | R          | R          | R/W             | R          | R          |   |   |
| 0h          | 0h         | 0h         | 0h              | 0h         | 0h         |   |   |

**Table 3-1826. SDFM\_SDCOMP3CTL Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                      |
|-------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | RESERVED_10     | R    | 0h    | Reserved                                                                                                                                         |
| 14    | RESERVED_9      | R    | 0h    | Reserved                                                                                                                                         |
| 13:12 | RESERVED_8      | R    | 0h    | Reserved                                                                                                                                         |
| 11:10 | CEVT2DIGFILTSEL | R/W  | 0h    | High comparator COMPH source select.<br>0 CEVT2 output drives COMPLOUT<br>1 Reserved<br>2 Output of digital filter drives COMPLOUT<br>3 Reserved |
| 9     | RESERVED_7      | R    | 0h    | Reserved                                                                                                                                         |
| 8     | RESERVED_6      | R    | 0h    | Reserved                                                                                                                                         |
| 7     | RESERVED_5      | R    | 0h    | Reserved                                                                                                                                         |
| 6     | RESERVED_4      | R    | 0h    | Reserved                                                                                                                                         |
| 5:4   | RESERVED_3      | R    | 0h    | Reserved                                                                                                                                         |
| 3:2   | CEVT1DIGFILTSEL | R/W  | 0h    | High comparator COMPH source select.<br>0 CEVT1 output drives COMPHOUT<br>1 Reserved<br>2 Output of digital filter drives COMPHOUT<br>3 Reserved |
| 1     | RESERVED_2      | R    | 0h    | Reserved                                                                                                                                         |
| 0     | RESERVED_1      | R    | 0h    | Reserved                                                                                                                                         |



### 3.12.2.75 SDFM\_SDCOMP3EVT2FLTCTL Register

#### 1 SDFM\_SDCOMP3EVT2FLTCTL Register (Offset = E2h) [reset = 0h]

COMPL/CEVT2 Digital filter3 Control Register.

Return to [Summary Table](#)

**Table 3-1827. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 80E2h       |
| SDFM1         | 5026 90E2h       |

**Figure 3-587. SDFM\_SDCOMP3EVT2FLTCTL Name Register**

| 15      | 14         | 13     | 12 | 11         | 10 | 9 | 8       |
|---------|------------|--------|----|------------|----|---|---------|
| FILINIT | RESERVED_2 | THRESH |    |            |    |   | SAMPWIN |
| R/W1TS  | R          | R/W    |    |            |    |   | R/W     |
| 0h      | 0h         | 0h     |    |            |    |   | 0h      |
| 7       | 6          | 5      | 4  | 3          | 2  | 1 | 0       |
| SAMPWIN |            |        |    | RESERVED_1 |    |   |         |
| R/W     |            |        |    | R          |    |   |         |
| 0h      |            |        |    | 0h         |    |   |         |

**Table 3-1829. SDFM\_SDCOMP3EVT2FLTCTL Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                       |
|------|------------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | FILINIT    | R/W1TS | 0h    | Low filter initialization.<br>0 No effect<br>1 Initialize all samples to the filter input value                                                                   |
| 14   | RESERVED_2 | R      | 0h    | Reserved                                                                                                                                                          |
| 13:9 | THRESH     | R/W    | 0h    | Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. |
| 8:4  | SAMPWIN    | R/W    | 0h    | Low filter sample window size. Number of samples to monitor is SAMPWIN+1.                                                                                         |
| 3:0  | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                          |

### 3.12.2.76 SDFM\_SDCOMP3EVT2FLTCLKCTL Register

#### 1 SDFM\_SDCOMP3EVT2FLTCLKCTL Register (Offset = E4h) [reset = 0h]

COMPL/CEVT2 Digital filter3 Clock Control Register.

Return to [Summary Table](#)

**Table 3-1830. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 80E4h       |
| SDFM1         | 5026 90E4h       |

**Figure 3-588. SDFM\_SDCOMP3EVT2FLTCLKCTL Name Register**

|             |    |    |    |    |    |             |   |
|-------------|----|----|----|----|----|-------------|---|
| 15          | 14 | 13 | 12 | 11 | 10 | 9           | 8 |
| RESERVED_1  |    |    |    |    |    | CLKPRESCALE |   |
| R           |    |    |    |    |    | R/W         |   |
| 0h          |    |    |    |    |    | 0h          |   |
| 7           | 6  | 5  | 4  | 3  | 2  | 1           | 0 |
| CLKPRESCALE |    |    |    |    |    |             |   |
| R/W         |    |    |    |    |    |             |   |
| 0h          |    |    |    |    |    |             |   |

**Table 3-1832. SDFM\_SDCOMP3EVT2FLTCLKCTL Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                |
|-------|-------------|------|-------|----------------------------------------------------------------------------|
| 15:10 | RESERVED_1  | R    | 0h    | Reserved                                                                   |
| 9:0   | CLKPRESCALE | R/W  | 0h    | Low filter sample clock prescale. Number of system clocks between samples. |

### 3.12.2.77 SDFM\_SDCOMP3EVT1FLTCTL Register

#### 1 SDFM\_SDCOMP3EVT1FLTCTL Register (Offset = E6h) [reset = 0h]

COMP/CEVT1 Digital filter3 Control Register.

Return to [Summary Table](#)

**Table 3-1833. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 80E6h       |
| SDFM1         | 5026 90E6h       |

**Figure 3-589. SDFM\_SDCOMP3EVT1FLTCTL Name Register**

| 15      | 14         | 13     | 12 | 11         | 10 | 9 | 8       |
|---------|------------|--------|----|------------|----|---|---------|
| FILINIT | RESERVED_2 | THRESH |    |            |    |   | SAMPWIN |
| R/W1TS  | R          | R/W    |    |            |    |   | R/W     |
| 0h      | 0h         | 0h     |    |            |    |   | 0h      |
| 7       | 6          | 5      | 4  | 3          | 2  | 1 | 0       |
| SAMPWIN |            |        |    | RESERVED_1 |    |   |         |
| R/W     |            |        |    | R          |    |   |         |
| 0h      |            |        |    | 0h         |    |   |         |

**Table 3-1835. SDFM\_SDCOMP3EVT1FLTCTL Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                        |
|------|------------|--------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | FILINIT    | R/W1TS | 0h    | High filter initialization.<br>0 No effect<br>1 Initialize all samples to the filter input value                                                                   |
| 14   | RESERVED_2 | R      | 0h    | Reserved                                                                                                                                                           |
| 13:9 | THRESH     | R/W    | 0h    | High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. |
| 8:4  | SAMPWIN    | R/W    | 0h    | High filter sample window size. Number of samples to monitor is SAMPWIN+1.                                                                                         |
| 3:0  | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                           |

### 3.12.2.78 SDFM\_SDCOMP3EVT1FLTCLKCTL Register

#### 1 SDFM\_SDCOMP3EVT1FLTCLKCTL Register (Offset = E8h) [reset = 0h]

COMP/CEVT1 Digital filter3 Clock Control Register.

Return to [Summary Table](#)

**Table 3-1836. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 80E8h       |
| SDFM1         | 5026 90E8h       |

**Figure 3-590. SDFM\_SDCOMP3EVT1FLTCLKCTL Name Register**

|             |    |    |    |    |    |             |   |
|-------------|----|----|----|----|----|-------------|---|
| 15          | 14 | 13 | 12 | 11 | 10 | 9           | 8 |
| RESERVED_1  |    |    |    |    |    | CLKPRESCALE |   |
| R           |    |    |    |    |    | R/W         |   |
| 0h          |    |    |    |    |    | 0h          |   |
| 7           | 6  | 5  | 4  | 3  | 2  | 1           | 0 |
| CLKPRESCALE |    |    |    |    |    |             |   |
| R/W         |    |    |    |    |    |             |   |
| 0h          |    |    |    |    |    |             |   |

**Table 3-1838. SDFM\_SDCOMP3EVT1FLTCLKCTL Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                 |
|-------|-------------|------|-------|-----------------------------------------------------------------------------|
| 15:10 | RESERVED_1  | R    | 0h    | Reserved                                                                    |
| 9:0   | CLKPRESCALE | R/W  | 0h    | High filter sample clock prescale. Number of system clocks between samples. |

### 3.12.2.79 SDFM\_SDCOMP3LOCK Register

#### 1 SDFM\_SDCOMP3LOCK Register (Offset = EEh) [reset = 0h]

SD compartor event filter3 Lock Register.

Return to [Summary Table](#)

**Table 3-1839. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 80EEh       |
| SDFM1         | 5026 90EEh       |

**Figure 3-591. SDFM\_SDCOMP3LOCK Name Register**

|            |    |    |            |        |            |            |            |
|------------|----|----|------------|--------|------------|------------|------------|
| 15         | 14 | 13 | 12         | 11     | 10         | 9          | 8          |
| RESERVED_4 |    |    |            |        |            |            |            |
| R          |    |    |            |        |            |            |            |
| 0h         |    |    |            |        |            |            |            |
| 7          | 6  | 5  | 4          | 3      | 2          | 1          | 0          |
| RESERVED_4 |    |    | RESERVED_3 | COMP   | RESERVED_2 | RESERVED_1 | SDCOMP3CTL |
| R          |    |    | R          | R/W1TS | R          | R          | R/W1TS     |
| 0h         |    |    | 0h         | 0h     | 0h         | 0h         | 0h         |

**Table 3-1841. SDFM\_SDCOMP3LOCK Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                                                                   |
|------|------------|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:5 | RESERVED_4 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                      |
| 4    | RESERVED_3 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                      |
| 3    | COMP       | R/W1TS | 0h    | Lock write-access to the SDCOMP3EVT1/2FLTCTL and COMP3FILCLKCTL registers.<br>0 SDCOMP3EVT1/2FLTCTL and SDCOMP3EVT1/2FLTCLKCTL registers are not locked. Write 0 to this bit has no effect.<br>1 SDCOMP3EVT1/2FLTCTL and SDCOMP3EVT1/2FLTCLKCTL registers are locked. Only a system reset can clear this bit. |
| 2    | RESERVED_2 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                      |
| 1    | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                      |
| 0    | SDCOMP3CTL | R/W1TS | 0h    | Lock write-access to the SDCOMP3CTL register.<br>0 SDCOMP3CTL register is not locked. Write 0 to this bit has no effect.<br>1 SDCOMP3CTL register is locked. Only a system reset can clear this bit.                                                                                                          |

### 3.12.2.80 SDFM\_SDCOMP4CTL Register

#### 1 SDFM\_SDCOMP4CTL Register (Offset = F0h) [reset = 0h]

SD Comparator event filter4 Control Register.

Return to [Summary Table](#)

**Table 3-1842. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 80F0h       |
| SDFM1         | 5026 90F0h       |

**Figure 3-592. SDFM\_SDCOMP4CTL Name Register**

| 15          | 14         | 13         | 12              | 11         | 10         | 9 | 8 |
|-------------|------------|------------|-----------------|------------|------------|---|---|
| RESERVED_10 | RESERVED_9 | RESERVED_8 | CEVT2DIGFILTSEL | RESERVED_7 | RESERVED_6 |   |   |
| R           | R          | R          | R/W             | R          | R          |   |   |
| 0h          | 0h         | 0h         | 0h              | 0h         | 0h         |   |   |
| 7           | 6          | 5          | 4               | 3          | 2          | 1 | 0 |
| RESERVED_5  | RESERVED_4 | RESERVED_3 | CEVT1DIGFILTSEL | RESERVED_2 | RESERVED_1 |   |   |
| R           | R          | R          | R/W             | R          | R          |   |   |
| 0h          | 0h         | 0h         | 0h              | 0h         | 0h         |   |   |

**Table 3-1844. SDFM\_SDCOMP4CTL Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                      |
|-------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | RESERVED_10     | R    | 0h    | Reserved                                                                                                                                         |
| 14    | RESERVED_9      | R    | 0h    | Reserved                                                                                                                                         |
| 13:12 | RESERVED_8      | R    | 0h    | Reserved                                                                                                                                         |
| 11:10 | CEVT2DIGFILTSEL | R/W  | 0h    | High comparator COMPH source select.<br>0 CEVT2 output drives COMPLOUT<br>1 Reserved<br>2 Output of digital filter drives COMPLOUT<br>3 Reserved |
| 9     | RESERVED_7      | R    | 0h    | Reserved                                                                                                                                         |
| 8     | RESERVED_6      | R    | 0h    | Reserved                                                                                                                                         |
| 7     | RESERVED_5      | R    | 0h    | Reserved                                                                                                                                         |
| 6     | RESERVED_4      | R    | 0h    | Reserved                                                                                                                                         |
| 5:4   | RESERVED_3      | R    | 0h    | Reserved                                                                                                                                         |
| 3:2   | CEVT1DIGFILTSEL | R/W  | 0h    | High comparator COMPH source select.<br>0 CEVT1 output drives COMPHOUT<br>1 Reserved<br>2 Output of digital filter drives COMPHOUT<br>3 Reserved |
| 1     | RESERVED_2      | R    | 0h    | Reserved                                                                                                                                         |
| 0     | RESERVED_1      | R    | 0h    | Reserved                                                                                                                                         |

### 3.12.2.81 SDFM\_SDCOMP4EVT2FLTCTL Register

#### 1 SDFM\_SDCOMP4EVT2FLTCTL Register (Offset = F2h) [reset = 0h]

COMPL/CEVT2 Digital filter4 Control Register.

Return to [Summary Table](#)

**Table 3-1845. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 80F2h       |
| SDFM1         | 5026 90F2h       |

**Figure 3-593. SDFM\_SDCOMP4EVT2FLTCTL Name Register**

| 15      | 14         | 13     | 12 | 11         | 10 | 9 | 8       |
|---------|------------|--------|----|------------|----|---|---------|
| FILINIT | RESERVED_2 | THRESH |    |            |    |   | SAMPWIN |
| R/W1TS  | R          | R/W    |    |            |    |   | R/W     |
| 0h      | 0h         | 0h     |    |            |    |   | 0h      |
| 7       | 6          | 5      | 4  | 3          | 2  | 1 | 0       |
| SAMPWIN |            |        |    | RESERVED_1 |    |   |         |
| R/W     |            |        |    | R          |    |   |         |
| 0h      |            |        |    | 0h         |    |   |         |

**Table 3-1847. SDFM\_SDCOMP4EVT2FLTCTL Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                       |
|------|------------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | FILINIT    | R/W1TS | 0h    | Low filter initialization.<br>0 No effect<br>1 Initialize all samples to the filter input value                                                                   |
| 14   | RESERVED_2 | R      | 0h    | Reserved                                                                                                                                                          |
| 13:9 | THRESH     | R/W    | 0h    | Low filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. |
| 8:4  | SAMPWIN    | R/W    | 0h    | Low filter sample window size. Number of samples to monitor is SAMPWIN+1.                                                                                         |
| 3:0  | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                          |

### 3.12.2.82 SDFM\_SDCOMP4EVT2FLTCLKCTL Register

#### 1 SDFM\_SDCOMP4EVT2FLTCLKCTL Register (Offset = F4h) [reset = 0h]

COMPL/CEVT2 Digital filter4 Clock Control Register.

Return to [Summary Table](#)

**Table 3-1848. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 80F4h       |
| SDFM1         | 5026 90F4h       |

**Figure 3-594. SDFM\_SDCOMP4EVT2FLTCLKCTL Name Register**

|             |    |    |    |    |    |             |   |
|-------------|----|----|----|----|----|-------------|---|
| 15          | 14 | 13 | 12 | 11 | 10 | 9           | 8 |
| RESERVED_1  |    |    |    |    |    | CLKPRESCALE |   |
| R           |    |    |    |    |    | R/W         |   |
| 0h          |    |    |    |    |    | 0h          |   |
| 7           | 6  | 5  | 4  | 3  | 2  | 1           | 0 |
| CLKPRESCALE |    |    |    |    |    |             |   |
| R/W         |    |    |    |    |    |             |   |
| 0h          |    |    |    |    |    |             |   |

**Table 3-1850. SDFM\_SDCOMP4EVT2FLTCLKCTL Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                |
|-------|-------------|------|-------|----------------------------------------------------------------------------|
| 15:10 | RESERVED_1  | R    | 0h    | Reserved                                                                   |
| 9:0   | CLKPRESCALE | R/W  | 0h    | Low filter sample clock prescale. Number of system clocks between samples. |



### 3.12.2.83 SDFM\_SDCOMP4EVT1FLTCTL Register

#### 1 SDFM\_SDCOMP4EVT1FLTCTL Register (Offset = F6h) [reset = 0h]

COMP/CEVT1 Digital filter4 Control Register.

Return to [Summary Table](#)

**Table 3-1851. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 80F6h       |
| SDFM1         | 5026 90F6h       |

**Figure 3-595. SDFM\_SDCOMP4EVT1FLTCTL Name Register**

| 15      | 14         | 13     | 12 | 11         | 10 | 9 | 8       |
|---------|------------|--------|----|------------|----|---|---------|
| FILINIT | RESERVED_2 | THRESH |    |            |    |   | SAMPWIN |
| R/W1TS  | R          | R/W    |    |            |    |   | R/W     |
| 0h      | 0h         | 0h     |    |            |    |   | 0h      |
| 7       | 6          | 5      | 4  | 3          | 2  | 1 | 0       |
| SAMPWIN |            |        |    | RESERVED_1 |    |   |         |
| R/W     |            |        |    | R          |    |   |         |
| 0h      |            |        |    | 0h         |    |   |         |

**Table 3-1853. SDFM\_SDCOMP4EVT1FLTCTL Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                        |
|------|------------|--------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | FILINIT    | R/W1TS | 0h    | High filter initialization.<br>0 No effect<br>1 Initialize all samples to the filter input value                                                                   |
| 14   | RESERVED_2 | R      | 0h    | Reserved                                                                                                                                                           |
| 13:9 | THRESH     | R/W    | 0h    | High filter majority voting threshold. At least THRESH samples of the opposite state must appear within the sample window in order for the output to change state. |
| 8:4  | SAMPWIN    | R/W    | 0h    | High filter sample window size. Number of samples to monitor is SAMPWIN+1.                                                                                         |
| 3:0  | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                           |

### 3.12.2.84 SDFM\_SDCOMP4EVT1FLTCLKCTL Register

#### 1 SDFM\_SDCOMP4EVT1FLTCLKCTL Register (Offset = F8h) [reset = 0h]

COMP4/CEVT1 Digital filter4 Clock Control Register.

Return to [Summary Table](#)

**Table 3-1854. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 80F8h       |
| SDFM1         | 5026 90F8h       |

**Figure 3-596. SDFM\_SDCOMP4EVT1FLTCLKCTL Name Register**

|             |    |    |    |    |    |             |   |
|-------------|----|----|----|----|----|-------------|---|
| 15          | 14 | 13 | 12 | 11 | 10 | 9           | 8 |
| RESERVED_1  |    |    |    |    |    | CLKPRESCALE |   |
| R           |    |    |    |    |    | R/W         |   |
| 0h          |    |    |    |    |    | 0h          |   |
| 7           | 6  | 5  | 4  | 3  | 2  | 1           | 0 |
| CLKPRESCALE |    |    |    |    |    |             |   |
| R/W         |    |    |    |    |    |             |   |
| 0h          |    |    |    |    |    |             |   |

**Table 3-1856. SDFM\_SDCOMP4EVT1FLTCLKCTL Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                 |
|-------|-------------|------|-------|-----------------------------------------------------------------------------|
| 15:10 | RESERVED_1  | R    | 0h    | Reserved                                                                    |
| 9:0   | CLKPRESCALE | R/W  | 0h    | High filter sample clock prescale. Number of system clocks between samples. |

### 3.12.2.85 SDFM\_SDCOMP4LOCK Register

#### 1 SDFM\_SDCOMP4LOCK Register (Offset = FEh) [reset = 0h]

SD compartor event filter4 Lock Register.

Return to [Summary Table](#)

**Table 3-1857. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SDFM0         | 5026 80FEh       |
| SDFM1         | 5026 90FEh       |

**Figure 3-597. SDFM\_SDCOMP4LOCK Name Register**

|            |    |    |            |        |            |            |            |
|------------|----|----|------------|--------|------------|------------|------------|
| 15         | 14 | 13 | 12         | 11     | 10         | 9          | 8          |
| RESERVED_4 |    |    |            |        |            |            |            |
| R          |    |    |            |        |            |            |            |
| 0h         |    |    |            |        |            |            |            |
| 7          | 6  | 5  | 4          | 3      | 2          | 1          | 0          |
| RESERVED_4 |    |    | RESERVED_3 | COMP   | RESERVED_2 | RESERVED_1 | SDCOMP4CTL |
| R          |    |    | R          | R/W1TS | R          | R          | R/W1TS     |
| 0h         |    |    | 0h         | 0h     | 0h         | 0h         | 0h         |

**Table 3-1859. SDFM\_SDCOMP4LOCK Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                                                                   |
|------|------------|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:5 | RESERVED_4 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                      |
| 4    | RESERVED_3 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                      |
| 3    | COMP       | R/W1TS | 0h    | Lock write-access to the SDCOMP4EVT1/2FLTCTL and COMP4FILCLKCTL registers.<br>0 SDCOMP4EVT1/2FLTCTL and SDCOMP4EVT1/2FLTCLKCTL registers are not locked. Write 0 to this bit has no effect.<br>1 SDCOMP4EVT1/2FLTCTL and SDCOMP4EVT1/2FLTCLKCTL registers are locked. Only a system reset can clear this bit. |
| 2    | RESERVED_2 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                      |
| 1    | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                      |
| 0    | SDCOMP4CTL | R/W1TS | 0h    | Lock write-access to the SDCOMP4CTL register.<br>0 SDCOMP4CTL register is not locked. Write 0 to this bit has no effect.<br>1 SDCOMP4CTL register is locked. Only a system reset can clear this bit.                                                                                                          |

### 3.13 CONTROLSS\_DMAXBAR

#### CONTROLSS\_DMAXBAR

##### 3.13.1 CONTROLSS\_DMAXBAR Summaries

#### CONTROLSS\_DMAXBAR Summaries

**Table 3-1860. CONTROLSS Registers, Base Address=502D 6000h, Length=1024**

| Offset | Length | Register Name                           | CONTROLSS_DMAXBAR Physical Address |
|--------|--------|-----------------------------------------|------------------------------------|
| 100h   | 32     | <a href="#">CONTROLSS_DMAXBAR0_GSEL</a> | 502D 6100h                         |
| 104h   | 32     | <a href="#">CONTROLSS_DMAXBAR0_G0</a>   | 502D 6104h                         |
| 108h   | 32     | <a href="#">CONTROLSS_DMAXBAR0_G1</a>   | 502D 6108h                         |
| 10Ch   | 32     | <a href="#">CONTROLSS_DMAXBAR0_G2</a>   | 502D 610Ch                         |
| 110h   | 32     | <a href="#">CONTROLSS_DMAXBAR0_G3</a>   | 502D 6110h                         |
| 114h   | 32     | <a href="#">CONTROLSS_DMAXBAR0_G4</a>   | 502D 6114h                         |
| 118h   | 32     | <a href="#">CONTROLSS_DMAXBAR0_G5</a>   | 502D 6118h                         |
| 140h   | 32     | <a href="#">CONTROLSS_DMAXBAR1_GSEL</a> | 502D 6140h                         |
| 144h   | 32     | <a href="#">CONTROLSS_DMAXBAR1_G0</a>   | 502D 6144h                         |
| 148h   | 32     | <a href="#">CONTROLSS_DMAXBAR1_G1</a>   | 502D 6148h                         |
| 14Ch   | 32     | <a href="#">CONTROLSS_DMAXBAR1_G2</a>   | 502D 614Ch                         |
| 150h   | 32     | <a href="#">CONTROLSS_DMAXBAR1_G3</a>   | 502D 6150h                         |
| 154h   | 32     | <a href="#">CONTROLSS_DMAXBAR1_G4</a>   | 502D 6154h                         |
| 158h   | 32     | <a href="#">CONTROLSS_DMAXBAR1_G5</a>   | 502D 6158h                         |
| 180h   | 32     | <a href="#">CONTROLSS_DMAXBAR2_GSEL</a> | 502D 6180h                         |
| 184h   | 32     | <a href="#">CONTROLSS_DMAXBAR2_G0</a>   | 502D 6184h                         |
| 188h   | 32     | <a href="#">CONTROLSS_DMAXBAR2_G1</a>   | 502D 6188h                         |
| 18Ch   | 32     | <a href="#">CONTROLSS_DMAXBAR2_G2</a>   | 502D 618Ch                         |
| 190h   | 32     | <a href="#">CONTROLSS_DMAXBAR2_G3</a>   | 502D 6190h                         |
| 194h   | 32     | <a href="#">CONTROLSS_DMAXBAR2_G4</a>   | 502D 6194h                         |
| 198h   | 32     | <a href="#">CONTROLSS_DMAXBAR2_G5</a>   | 502D 6198h                         |
| 1C0h   | 32     | <a href="#">CONTROLSS_DMAXBAR3_GSEL</a> | 502D 61C0h                         |
| 1C4h   | 32     | <a href="#">CONTROLSS_DMAXBAR3_G0</a>   | 502D 61C4h                         |
| 1C8h   | 32     | <a href="#">CONTROLSS_DMAXBAR3_G1</a>   | 502D 61C8h                         |
| 1CCh   | 32     | <a href="#">CONTROLSS_DMAXBAR3_G2</a>   | 502D 61CCh                         |
| 1D0h   | 32     | <a href="#">CONTROLSS_DMAXBAR3_G3</a>   | 502D 61D0h                         |
| 1D4h   | 32     | <a href="#">CONTROLSS_DMAXBAR3_G4</a>   | 502D 61D4h                         |
| 1D8h   | 32     | <a href="#">CONTROLSS_DMAXBAR3_G5</a>   | 502D 61D8h                         |
| 200h   | 32     | <a href="#">CONTROLSS_DMAXBAR4_GSEL</a> | 502D 6200h                         |
| 204h   | 32     | <a href="#">CONTROLSS_DMAXBAR4_G0</a>   | 502D 6204h                         |
| 208h   | 32     | <a href="#">CONTROLSS_DMAXBAR4_G1</a>   | 502D 6208h                         |
| 20Ch   | 32     | <a href="#">CONTROLSS_DMAXBAR4_G2</a>   | 502D 620Ch                         |
| 210h   | 32     | <a href="#">CONTROLSS_DMAXBAR4_G3</a>   | 502D 6210h                         |
| 214h   | 32     | <a href="#">CONTROLSS_DMAXBAR4_G4</a>   | 502D 6214h                         |
| 218h   | 32     | <a href="#">CONTROLSS_DMAXBAR4_G5</a>   | 502D 6218h                         |
| 240h   | 32     | <a href="#">CONTROLSS_DMAXBAR5_GSEL</a> | 502D 6240h                         |
| 244h   | 32     | <a href="#">CONTROLSS_DMAXBAR5_G0</a>   | 502D 6244h                         |

**Table 3-1860. CONTROLSS Registers, Base Address=502D 6000h, Length=1024 (continued)**

| Offset | Length | Register Name                            | CONTROLSS_DMAXBAR Physical Address |
|--------|--------|------------------------------------------|------------------------------------|
| 248h   | 32     | <a href="#">CONTROLSS_DMAXBAR5_G1</a>    | 502D 6248h                         |
| 24Ch   | 32     | <a href="#">CONTROLSS_DMAXBAR5_G2</a>    | 502D 624Ch                         |
| 250h   | 32     | <a href="#">CONTROLSS_DMAXBAR5_G3</a>    | 502D 6250h                         |
| 254h   | 32     | <a href="#">CONTROLSS_DMAXBAR5_G4</a>    | 502D 6254h                         |
| 258h   | 32     | <a href="#">CONTROLSS_DMAXBAR5_G5</a>    | 502D 6258h                         |
| 280h   | 32     | <a href="#">CONTROLSS_DMAXBAR6_GSEL</a>  | 502D 6280h                         |
| 284h   | 32     | <a href="#">CONTROLSS_DMAXBAR6_G0</a>    | 502D 6284h                         |
| 288h   | 32     | <a href="#">CONTROLSS_DMAXBAR6_G1</a>    | 502D 6288h                         |
| 28Ch   | 32     | <a href="#">CONTROLSS_DMAXBAR6_G2</a>    | 502D 628Ch                         |
| 290h   | 32     | <a href="#">CONTROLSS_DMAXBAR6_G3</a>    | 502D 6290h                         |
| 294h   | 32     | <a href="#">CONTROLSS_DMAXBAR6_G4</a>    | 502D 6294h                         |
| 298h   | 32     | <a href="#">CONTROLSS_DMAXBAR6_G5</a>    | 502D 6298h                         |
| 2C0h   | 32     | <a href="#">CONTROLSS_DMAXBAR7_GSEL</a>  | 502D 62C0h                         |
| 2C4h   | 32     | <a href="#">CONTROLSS_DMAXBAR7_G0</a>    | 502D 62C4h                         |
| 2C8h   | 32     | <a href="#">CONTROLSS_DMAXBAR7_G1</a>    | 502D 62C8h                         |
| 2CCh   | 32     | <a href="#">CONTROLSS_DMAXBAR7_G2</a>    | 502D 62CCh                         |
| 2D0h   | 32     | <a href="#">CONTROLSS_DMAXBAR7_G3</a>    | 502D 62D0h                         |
| 2D4h   | 32     | <a href="#">CONTROLSS_DMAXBAR7_G4</a>    | 502D 62D4h                         |
| 2D8h   | 32     | <a href="#">CONTROLSS_DMAXBAR7_G5</a>    | 502D 62D8h                         |
| 300h   | 32     | <a href="#">CONTROLSS_DMAXBAR8_GSEL</a>  | 502D 6300h                         |
| 304h   | 32     | <a href="#">CONTROLSS_DMAXBAR8_G0</a>    | 502D 6304h                         |
| 308h   | 32     | <a href="#">CONTROLSS_DMAXBAR8_G1</a>    | 502D 6308h                         |
| 30Ch   | 32     | <a href="#">CONTROLSS_DMAXBAR8_G2</a>    | 502D 630Ch                         |
| 310h   | 32     | <a href="#">CONTROLSS_DMAXBAR8_G3</a>    | 502D 6310h                         |
| 314h   | 32     | <a href="#">CONTROLSS_DMAXBAR8_G4</a>    | 502D 6314h                         |
| 318h   | 32     | <a href="#">CONTROLSS_DMAXBAR8_G5</a>    | 502D 6318h                         |
| 340h   | 32     | <a href="#">CONTROLSS_DMAXBAR9_GSEL</a>  | 502D 6340h                         |
| 344h   | 32     | <a href="#">CONTROLSS_DMAXBAR9_G0</a>    | 502D 6344h                         |
| 348h   | 32     | <a href="#">CONTROLSS_DMAXBAR9_G1</a>    | 502D 6348h                         |
| 34Ch   | 32     | <a href="#">CONTROLSS_DMAXBAR9_G2</a>    | 502D 634Ch                         |
| 350h   | 32     | <a href="#">CONTROLSS_DMAXBAR9_G3</a>    | 502D 6350h                         |
| 354h   | 32     | <a href="#">CONTROLSS_DMAXBAR9_G4</a>    | 502D 6354h                         |
| 358h   | 32     | <a href="#">CONTROLSS_DMAXBAR9_G5</a>    | 502D 6358h                         |
| 380h   | 32     | <a href="#">CONTROLSS_DMAXBAR10_GSEL</a> | 502D 6380h                         |
| 384h   | 32     | <a href="#">CONTROLSS_DMAXBAR10_G0</a>   | 502D 6384h                         |
| 388h   | 32     | <a href="#">CONTROLSS_DMAXBAR10_G1</a>   | 502D 6388h                         |
| 38Ch   | 32     | <a href="#">CONTROLSS_DMAXBAR10_G2</a>   | 502D 638Ch                         |
| 390h   | 32     | <a href="#">CONTROLSS_DMAXBAR10_G3</a>   | 502D 6390h                         |
| 394h   | 32     | <a href="#">CONTROLSS_DMAXBAR10_G4</a>   | 502D 6394h                         |
| 398h   | 32     | <a href="#">CONTROLSS_DMAXBAR10_G5</a>   | 502D 6398h                         |
| 3C0h   | 32     | <a href="#">CONTROLSS_DMAXBAR11_GSEL</a> | 502D 63C0h                         |
| 3C4h   | 32     | <a href="#">CONTROLSS_DMAXBAR11_G0</a>   | 502D 63C4h                         |
| 3C8h   | 32     | <a href="#">CONTROLSS_DMAXBAR11_G1</a>   | 502D 63C8h                         |
| 3CCh   | 32     | <a href="#">CONTROLSS_DMAXBAR11_G2</a>   | 502D 63CCh                         |

**Table 3-1860. CONTROLSS Registers, Base Address=502D 6000h, Length=1024 (continued)**

| Offset | Length | Register Name                            | CONTROLSS_DMAXBAR Physical Address |
|--------|--------|------------------------------------------|------------------------------------|
| 3D0h   | 32     | <a href="#">CONTROLSS_DMAXBAR11_G3</a>   | 502D 63D0h                         |
| 3D4h   | 32     | <a href="#">CONTROLSS_DMAXBAR11_G4</a>   | 502D 63D4h                         |
| 3D8h   | 32     | <a href="#">CONTROLSS_DMAXBAR11_G5</a>   | 502D 63D8h                         |
| 400h   | 32     | <a href="#">CONTROLSS_DMAXBAR12_GSEL</a> | 502D 6400h                         |
| 404h   | 32     | <a href="#">CONTROLSS_DMAXBAR12_G0</a>   | 502D 6404h                         |
| 408h   | 32     | <a href="#">CONTROLSS_DMAXBAR12_G1</a>   | 502D 6408h                         |
| 40Ch   | 32     | <a href="#">CONTROLSS_DMAXBAR12_G2</a>   | 502D 640Ch                         |
| 410h   | 32     | <a href="#">CONTROLSS_DMAXBAR12_G3</a>   | 502D 6410h                         |
| 414h   | 32     | <a href="#">CONTROLSS_DMAXBAR12_G4</a>   | 502D 6414h                         |
| 418h   | 32     | <a href="#">CONTROLSS_DMAXBAR12_G5</a>   | 502D 6418h                         |
| 440h   | 32     | <a href="#">CONTROLSS_DMAXBAR13_GSEL</a> | 502D 6440h                         |
| 444h   | 32     | <a href="#">CONTROLSS_DMAXBAR13_G0</a>   | 502D 6444h                         |
| 448h   | 32     | <a href="#">CONTROLSS_DMAXBAR13_G1</a>   | 502D 6448h                         |
| 44Ch   | 32     | <a href="#">CONTROLSS_DMAXBAR13_G2</a>   | 502D 644Ch                         |
| 450h   | 32     | <a href="#">CONTROLSS_DMAXBAR13_G3</a>   | 502D 6450h                         |
| 454h   | 32     | <a href="#">CONTROLSS_DMAXBAR13_G4</a>   | 502D 6454h                         |
| 458h   | 32     | <a href="#">CONTROLSS_DMAXBAR13_G5</a>   | 502D 6458h                         |
| 480h   | 32     | <a href="#">CONTROLSS_DMAXBAR14_GSEL</a> | 502D 6480h                         |
| 484h   | 32     | <a href="#">CONTROLSS_DMAXBAR14_G0</a>   | 502D 6484h                         |
| 488h   | 32     | <a href="#">CONTROLSS_DMAXBAR14_G1</a>   | 502D 6488h                         |
| 48Ch   | 32     | <a href="#">CONTROLSS_DMAXBAR14_G2</a>   | 502D 648Ch                         |
| 490h   | 32     | <a href="#">CONTROLSS_DMAXBAR14_G3</a>   | 502D 6490h                         |
| 494h   | 32     | <a href="#">CONTROLSS_DMAXBAR14_G4</a>   | 502D 6494h                         |
| 498h   | 32     | <a href="#">CONTROLSS_DMAXBAR14_G5</a>   | 502D 6498h                         |
| 4C0h   | 32     | <a href="#">CONTROLSS_DMAXBAR15_GSEL</a> | 502D 64C0h                         |
| 4C4h   | 32     | <a href="#">CONTROLSS_DMAXBAR15_G0</a>   | 502D 64C4h                         |
| 4C8h   | 32     | <a href="#">CONTROLSS_DMAXBAR15_G1</a>   | 502D 64C8h                         |
| 4CCh   | 32     | <a href="#">CONTROLSS_DMAXBAR15_G2</a>   | 502D 64CCh                         |
| 4D0h   | 32     | <a href="#">CONTROLSS_DMAXBAR15_G3</a>   | 502D 64D0h                         |
| 4D4h   | 32     | <a href="#">CONTROLSS_DMAXBAR15_G4</a>   | 502D 64D4h                         |
| 4D8h   | 32     | <a href="#">CONTROLSS_DMAXBAR15_G5</a>   | 502D 64D8h                         |

### 3.13.2 CONTROLSS\_DMAXBAR Registers

#### CONTROLSS\_DMAXBAR Registers

### 3.13.2.1 CONTROLSS\_DMAXBAR0\_GSEL Register

#### 1 CONTROLSS\_DMAXBAR0\_GSEL Register (Offset = 100h) [reset = 0h]

Group Select register to select between G0-G5.

Return to [Summary Table](#)

**Table 3-1861. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6100h       |

**Figure 3-598. CONTROLSS\_DMAXBAR0\_GSEL Name Register**

|          |    |    |    |    |                    |    |    |
|----------|----|----|----|----|--------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                 | 25 | 24 |
| RESERVED |    |    |    |    |                    |    |    |
| NONE     |    |    |    |    |                    |    |    |
| 0h       |    |    |    |    |                    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                 | 17 | 16 |
| RESERVED |    |    |    |    |                    |    |    |
| NONE     |    |    |    |    |                    |    |    |
| 0h       |    |    |    |    |                    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                 | 9  | 8  |
| RESERVED |    |    |    |    |                    |    |    |
| NONE     |    |    |    |    |                    |    |    |
| 0h       |    |    |    |    |                    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                  | 1  | 0  |
| RESERVED |    |    |    |    | DMAXBAR0_GSEL_GSEL |    |    |
| NONE     |    |    |    |    | R/W                |    |    |
| 0h       |    |    |    |    | 0h                 |    |    |

**Table 3-1863. CONTROLSS\_DMAXBAR0\_GSEL Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                  |
|------|--------------------|------|-------|--------------------------------------------------------------|
| 31:3 | RESERVED           | NONE | 0h    | Reserved                                                     |
| 2:0  | DMAXBAR0_GSEL_GSEL | R/W  | 0h    | Select input source:<br>0:G0 selected<br>..<br>5:G5 selected |

### 3.13.2.2 CONTROLSS\_DMAXBAR0\_G0 Register

#### 1 CONTROLSS\_DMAXBAR0\_G0 Register (Offset = 104h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1864. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6104h       |

**Figure 3-599. CONTROLSS\_DMAXBAR0\_G0 Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR0_G0_SEL |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 3-1866. CONTROLSS\_DMAXBAR0\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                              |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED        | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR0_G0_SEL | R/W  | 0h    | EPWM SOCA to corresponding XBAR<br>1:PWMx.SOCA is selected<br>0:PWMx.SOCA is de-selected |



### 3.13.2.3 CONTROLSS\_DMAXBAR0\_G1 Register

#### 1 CONTROLSS\_DMAXBAR0\_G1 Register (Offset = 108h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1867. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6108h       |

**Figure 3-600. CONTROLSS\_DMAXBAR0\_G1 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR0_G1_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-1869. CONTROLSS\_DMAXBAR0\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                              |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED        | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR0_G1_SEL | R/W  | 0h    | EPWM SOCB to corresponding XBAR<br>1:PWMx.SOCB is selected<br>0:PWMx.SOCB is de-selected |

### 3.13.2.4 CONTROLSS\_DMAXBAR0\_G2 Register

#### 1 CONTROLSS\_DMAXBAR0\_G2 Register (Offset = 10Ch) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1870. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 610Ch       |

**Figure 3-601. CONTROLSS\_DMAXBAR0\_G2 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR0_G2_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-1872. CONTROLSS\_DMAXBAR0\_G2 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:5 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-1872. CONTROLSS\_DMAXBAR0\_G2 Register Field Descriptions (continued)**

| Bit | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | DMAXBAR0_G2_SEL | R/W  | 0h    | ADC DMA requests to corresponding XBAR<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.13.2.5 CONTROLSS\_DMAXBAR0\_G3 Register

#### 1 CONTROLSS\_DMAXBAR0\_G3 Register (Offset = 110h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1873. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6110h       |

**Figure 3-602. CONTROLSS\_DMAXBAR0\_G3 Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR0_G3_SEL |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 3-1875. CONTROLSS\_DMAXBAR0\_G3 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                         |
| 3:0  | DMAXBAR0_G3_SEL | R/W  | 0h    | FSI DMA requests to corresponding XBAR<br>0:FSIRX0.RX_DMA_EVT<br>1; FSIRX0_DMATRIG1<br>2:FSIRX0_DMATRIG2<br>3:FSIRX1.RX_DMA_EVT<br>4; FSIRX1_DMATRIG1<br>5:FSIRX1_DMATRIG2<br>6:FSIRX2.RX_DMA_EVT<br>7; FSIRX2_DMATRIG1<br>8:FSIRX2_DMATRIG2<br>9:FSIRX3.RX_DMA_EVT<br>10; FSIRX3_DMATRIG1<br>11:FSIRX3_DMATRIG2<br>12:FSITX0.TX_DMA_EVT<br>13:FSITX1.TX_DMA_EVT<br>14:FSITX2.TX_DMA_EVT<br>15:FSITX3.TX_DMA_EVT |

### 3.13.2.6 CONTROLSS\_DMAXBAR0\_G4 Register

#### 1 CONTROLSS\_DMAXBAR0\_G4 Register (Offset = 114h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1876. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6114h       |

**Figure 3-603. CONTROLSS\_DMAXBAR0\_G4 Name Register**

|          |    |    |    |    |                 |    |    |
|----------|----|----|----|----|-----------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26              | 25 | 24 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 23       | 22 | 21 | 20 | 19 | 18              | 17 | 16 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 15       | 14 | 13 | 12 | 11 | 10              | 9  | 8  |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 7        | 6  | 5  | 4  | 3  | 2               | 1  | 0  |
| RESERVED |    |    |    |    | DMAXBAR0_G4_SEL |    |    |
| NONE     |    |    |    |    | R/W             |    |    |
| 0h       |    |    |    |    | 0h              |    |    |

**Table 3-1878. CONTROLSS\_DMAXBAR0\_G4 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                     |
|------|-----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                        |
| 2:0  | DMAXBAR0_G4_SEL | R/W  | 0h    | SDFM DMA requests to corresponding XBAR<br>0:SD0.FILT1.DRINT<br>1:SD0.FILT2.DRINT<br>2:SD0.FILT3.DRINT<br>3:SD0.FILT4.DRINT<br>4:SD1.FILT1.DRINT<br>5:SD1.FILT2.DRINT<br>6:SD1.FILT3.DRINT<br>7:SD1.FILT4.DRINT |

### 3.13.2.7 CONTROLSS\_DMAXBAR0\_G5 Register

#### 1 CONTROLSS\_DMAXBAR0\_G5 Register (Offset = 118h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1879. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6118h       |

**Figure 3-604. CONTROLSS\_DMAXBAR0\_G5 Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR0_G5_SEL |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 3-1881. CONTROLSS\_DMAXBAR0\_G5 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                              |
| 3:0  | DMAXBAR0_G5_SEL | R/W  | 0h    | ECAP DMA requests to corresponding XBAR<br>0:ECAP0.DMA_INT<br>1:ECAP1.DMA_INT<br>2:ECAP2.DMA_INT<br>3:ECAP3.DMA_INT<br>4:ECAP4.DMA_INT<br>5:ECAP5.DMA_INT<br>6:ECAP6.DMA_INT<br>7:ECAP7.DMA_INT<br>8:ECAP8.DMA_INT<br>9:ECAP9.DMA_INT |

### 3.13.2.8 CONTROLSS\_DMAXBAR1\_GSEL Register

#### 1 CONTROLSS\_DMAXBAR1\_GSEL Register (Offset = 140h) [reset = 0h]

Group Select register to select between G0-G5.

Return to [Summary Table](#)

**Table 3-1882. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6140h       |

**Figure 3-605. CONTROLSS\_DMAXBAR1\_GSEL Name Register**

|          |    |    |    |    |                    |    |    |
|----------|----|----|----|----|--------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                 | 25 | 24 |
| RESERVED |    |    |    |    |                    |    |    |
| NONE     |    |    |    |    |                    |    |    |
| 0h       |    |    |    |    |                    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                 | 17 | 16 |
| RESERVED |    |    |    |    |                    |    |    |
| NONE     |    |    |    |    |                    |    |    |
| 0h       |    |    |    |    |                    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                 | 9  | 8  |
| RESERVED |    |    |    |    |                    |    |    |
| NONE     |    |    |    |    |                    |    |    |
| 0h       |    |    |    |    |                    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                  | 1  | 0  |
| RESERVED |    |    |    |    | DMAXBAR1_GSEL_GSEL |    |    |
| NONE     |    |    |    |    | R/W                |    |    |
| 0h       |    |    |    |    | 0h                 |    |    |

**Table 3-1884. CONTROLSS\_DMAXBAR1\_GSEL Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                  |
|------|--------------------|------|-------|--------------------------------------------------------------|
| 31:3 | RESERVED           | NONE | 0h    | Reserved                                                     |
| 2:0  | DMAXBAR1_GSEL_GSEL | R/W  | 0h    | Select input source:<br>0:G0 selected<br>..<br>5:G5 selected |

### 3.13.2.9 CONTROLSS\_DMAXBAR1\_G0 Register

#### 1 CONTROLSS\_DMAXBAR1\_G0 Register (Offset = 144h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1885. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6144h       |

**Figure 3-606. CONTROLSS\_DMAXBAR1\_G0 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR1_G0_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-1887. CONTROLSS\_DMAXBAR1\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                              |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED        | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR1_G0_SEL | R/W  | 0h    | EPWM SOCA to corresponding XBAR<br>1:PWMx.SOCA is selected<br>0:PWMx.SOCA is de-selected |



### 3.13.2.10 CONTROLSS\_DMAXBAR1\_G1 Register

#### 1 CONTROLSS\_DMAXBAR1\_G1 Register (Offset = 148h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1888. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6148h       |

**Figure 3-607. CONTROLSS\_DMAXBAR1\_G1 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR1_G1_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-1890. CONTROLSS\_DMAXBAR1\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                              |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED        | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR1_G1_SEL | R/W  | 0h    | EPWM SOCB to corresponding XBAR<br>1:PWMx.SOCB is selected<br>0:PWMx.SOCB is de-selected |

### 3.13.2.11 CONTROLSS\_DMAXBAR1\_G2 Register

#### 1 CONTROLSS\_DMAXBAR1\_G2 Register (Offset = 14Ch) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1891. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 614Ch       |

**Figure 3-608. CONTROLSS\_DMAXBAR1\_G2 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR1_G2_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-1893. CONTROLSS\_DMAXBAR1\_G2 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:5 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-1893. CONTROLSS\_DMAXBAR1\_G2 Register Field Descriptions (continued)**

| Bit | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | DMAXBAR1_G2_SEL | R/W  | 0h    | ADC DMA requests to corresponding XBAR<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.13.2.12 CONTROLSS\_DMAXBAR1\_G3 Register

#### 1 CONTROLSS\_DMAXBAR1\_G3 Register (Offset = 150h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1894. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6150h       |

**Figure 3-609. CONTROLSS\_DMAXBAR1\_G3 Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR1_G3_SEL |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 3-1896. CONTROLSS\_DMAXBAR1\_G3 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                         |
| 3:0  | DMAXBAR1_G3_SEL | R/W  | 0h    | FSI DMA requests to corresponding XBAR<br>0:FSIRX0.RX_DMA_EVT<br>1; FSIRX0_DMATRIG1<br>2:FSIRX0_DMATRIG2<br>3:FSIRX1.RX_DMA_EVT<br>4; FSIRX1_DMATRIG1<br>5:FSIRX1_DMATRIG2<br>6:FSIRX2.RX_DMA_EVT<br>7; FSIRX2_DMATRIG1<br>8:FSIRX2_DMATRIG2<br>9:FSIRX3.RX_DMA_EVT<br>10; FSIRX3_DMATRIG1<br>11:FSIRX3_DMATRIG2<br>12:FSITX0.TX_DMA_EVT<br>13:FSITX1.TX_DMA_EVT<br>14:FSITX2.TX_DMA_EVT<br>15:FSITX3.TX_DMA_EVT |

### 3.13.2.13 CONTROLSS\_DMAXBAR1\_G4 Register

#### 1 CONTROLSS\_DMAXBAR1\_G4 Register (Offset = 154h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1897. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6154h       |

**Figure 3-610. CONTROLSS\_DMAXBAR1\_G4 Name Register**

|          |    |    |    |    |                 |    |    |
|----------|----|----|----|----|-----------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26              | 25 | 24 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 23       | 22 | 21 | 20 | 19 | 18              | 17 | 16 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 15       | 14 | 13 | 12 | 11 | 10              | 9  | 8  |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 7        | 6  | 5  | 4  | 3  | 2               | 1  | 0  |
| RESERVED |    |    |    |    | DMAXBAR1_G4_SEL |    |    |
| NONE     |    |    |    |    | R/W             |    |    |
| 0h       |    |    |    |    | 0h              |    |    |

**Table 3-1899. CONTROLSS\_DMAXBAR1\_G4 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                     |
|------|-----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                        |
| 2:0  | DMAXBAR1_G4_SEL | R/W  | 0h    | SDFM DMA requests to corresponding XBAR<br>0:SD0.FILT1.DRINT<br>1:SD0.FILT2.DRINT<br>2:SD0.FILT3.DRINT<br>3:SD0.FILT4.DRINT<br>4:SD1.FILT1.DRINT<br>5:SD1.FILT2.DRINT<br>6:SD1.FILT3.DRINT<br>7:SD1.FILT4.DRINT |

### 3.13.2.14 CONTROLSS\_DMAXBAR1\_G5 Register

#### 1 CONTROLSS\_DMAXBAR1\_G5 Register (Offset = 158h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1900. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6158h       |

**Figure 3-611. CONTROLSS\_DMAXBAR1\_G5 Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR1_G5_SEL |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 3-1902. CONTROLSS\_DMAXBAR1\_G5 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                              |
| 3:0  | DMAXBAR1_G5_SEL | R/W  | 0h    | ECAP DMA requests to corresponding XBAR<br>0:ECAP0.DMA_INT<br>1:ECAP1.DMA_INT<br>2:ECAP2.DMA_INT<br>3:ECAP3.DMA_INT<br>4:ECAP4.DMA_INT<br>5:ECAP5.DMA_INT<br>6:ECAP6.DMA_INT<br>7:ECAP7.DMA_INT<br>8:ECAP8.DMA_INT<br>9:ECAP9.DMA_INT |

### 3.13.2.15 CONTROLSS\_DMAXBAR2\_GSEL Register

#### 1 CONTROLSS\_DMAXBAR2\_GSEL Register (Offset = 180h) [reset = 0h]

Group Select register to select between G0-G5.

Return to [Summary Table](#)

**Table 3-1903. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6180h       |

**Figure 3-612. CONTROLSS\_DMAXBAR2\_GSEL Name Register**

|          |    |    |    |                    |    |    |    |
|----------|----|----|----|--------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 23       | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 15       | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 7        | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR2_GSEL_GSEL |    |    |    |
| NONE     |    |    |    | R/W                |    |    |    |
| 0h       |    |    |    | 0h                 |    |    |    |

**Table 3-1905. CONTROLSS\_DMAXBAR2\_GSEL Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                  |
|------|--------------------|------|-------|--------------------------------------------------------------|
| 31:3 | RESERVED           | NONE | 0h    | Reserved                                                     |
| 2:0  | DMAXBAR2_GSEL_GSEL | R/W  | 0h    | Select input source:<br>0:G0 selected<br>..<br>5:G5 selected |

### 3.13.2.16 CONTROLSS\_DMAXBAR2\_G0 Register

#### 1 CONTROLSS\_DMAXBAR2\_G0 Register (Offset = 184h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1906. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6184h       |

**Figure 3-613. CONTROLSS\_DMAXBAR2\_G0 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR2_G0_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-1908. CONTROLSS\_DMAXBAR2\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                              |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED        | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR2_G0_SEL | R/W  | 0h    | EPWM SOCA to corresponding XBAR<br>1:PWMx.SOCA is selected<br>0:PWMx.SOCA is de-selected |



### 3.13.2.17 CONTROLSS\_DMAXBAR2\_G1 Register

#### 1 CONTROLSS\_DMAXBAR2\_G1 Register (Offset = 188h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1909. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6188h       |

**Figure 3-614. CONTROLSS\_DMAXBAR2\_G1 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR2_G1_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-1911. CONTROLSS\_DMAXBAR2\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                              |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED        | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR2_G1_SEL | R/W  | 0h    | EPWM SOCB to corresponding XBAR<br>1:PWMx.SOCB is selected<br>0:PWMx.SOCB is de-selected |

### 3.13.2.18 CONTROLSS\_DMAXBAR2\_G2 Register

#### 1 CONTROLSS\_DMAXBAR2\_G2 Register (Offset = 18Ch) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1912. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 618Ch       |

**Figure 3-615. CONTROLSS\_DMAXBAR2\_G2 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR2_G2_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-1914. CONTROLSS\_DMAXBAR2\_G2 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:5 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-1914. CONTROLSS\_DMAXBAR2\_G2 Register Field Descriptions (continued)**

| Bit | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | DMAXBAR2_G2_SEL | R/W  | 0h    | ADC DMA requests to corresponding XBAR<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.13.2.19 CONTROLSS\_DMAXBAR2\_G3 Register

#### 1 CONTROLSS\_DMAXBAR2\_G3 Register (Offset = 190h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1915. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6190h       |

**Figure 3-616. CONTROLSS\_DMAXBAR2\_G3 Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR2_G3_SEL |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 3-1917. CONTROLSS\_DMAXBAR2\_G3 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                         |
| 3:0  | DMAXBAR2_G3_SEL | R/W  | 0h    | FSI DMA requests to corresponding XBAR<br>0:FSIRX0.RX_DMA_EVT<br>1; FSIRX0_DMATRIG1<br>2:FSIRX0_DMATRIG2<br>3:FSIRX1.RX_DMA_EVT<br>4; FSIRX1_DMATRIG1<br>5:FSIRX1_DMATRIG2<br>6:FSIRX2.RX_DMA_EVT<br>7; FSIRX2_DMATRIG1<br>8:FSIRX2_DMATRIG2<br>9:FSIRX3.RX_DMA_EVT<br>10; FSIRX3_DMATRIG1<br>11:FSIRX3_DMATRIG2<br>12:FSITX0.TX_DMA_EVT<br>13:FSITX1.TX_DMA_EVT<br>14:FSITX2.TX_DMA_EVT<br>15:FSITX3.TX_DMA_EVT |

### 3.13.2.20 CONTROLSS\_DMAXBAR2\_G4 Register

#### 1 CONTROLSS\_DMAXBAR2\_G4 Register (Offset = 194h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1918. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6194h       |

**Figure 3-617. CONTROLSS\_DMAXBAR2\_G4 Name Register**

|          |    |    |    |    |                 |    |    |
|----------|----|----|----|----|-----------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26              | 25 | 24 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 23       | 22 | 21 | 20 | 19 | 18              | 17 | 16 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 15       | 14 | 13 | 12 | 11 | 10              | 9  | 8  |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 7        | 6  | 5  | 4  | 3  | 2               | 1  | 0  |
| RESERVED |    |    |    |    | DMAXBAR2_G4_SEL |    |    |
| NONE     |    |    |    |    | R/W             |    |    |
| 0h       |    |    |    |    | 0h              |    |    |

**Table 3-1920. CONTROLSS\_DMAXBAR2\_G4 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                     |
|------|-----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                        |
| 2:0  | DMAXBAR2_G4_SEL | R/W  | 0h    | SDFM DMA requests to corresponding XBAR<br>0:SD0.FILT1.DRINT<br>1:SD0.FILT2.DRINT<br>2:SD0.FILT3.DRINT<br>3:SD0.FILT4.DRINT<br>4:SD1.FILT1.DRINT<br>5:SD1.FILT2.DRINT<br>6:SD1.FILT3.DRINT<br>7:SD1.FILT4.DRINT |

### 3.13.2.21 CONTROLSS\_DMAXBAR2\_G5 Register

#### 1 CONTROLSS\_DMAXBAR2\_G5 Register (Offset = 198h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1921. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6198h       |

**Figure 3-618. CONTROLSS\_DMAXBAR2\_G5 Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR2_G5_SEL |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 3-1923. CONTROLSS\_DMAXBAR2\_G5 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                              |
| 3:0  | DMAXBAR2_G5_SEL | R/W  | 0h    | ECAP DMA requests to corresponding XBAR<br>0:ECAP0.DMA_INT<br>1:ECAP1.DMA_INT<br>2:ECAP2.DMA_INT<br>3:ECAP3.DMA_INT<br>4:ECAP4.DMA_INT<br>5:ECAP5.DMA_INT<br>6:ECAP6.DMA_INT<br>7:ECAP7.DMA_INT<br>8:ECAP8.DMA_INT<br>9:ECAP9.DMA_INT |

### 3.13.2.22 CONTROLSS\_DMAXBAR3\_GSEL Register

#### 1 CONTROLSS\_DMAXBAR3\_GSEL Register (Offset = 1C0h) [reset = 0h]

Group Select register to select between G0-G5.

Return to [Summary Table](#)

**Table 3-1924. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 61C0h       |

**Figure 3-619. CONTROLSS\_DMAXBAR3\_GSEL Name Register**

|          |    |    |    |                    |    |    |    |
|----------|----|----|----|--------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 23       | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 15       | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 7        | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR3_GSEL_GSEL |    |    |    |
| NONE     |    |    |    | R/W                |    |    |    |
| 0h       |    |    |    | 0h                 |    |    |    |

**Table 3-1926. CONTROLSS\_DMAXBAR3\_GSEL Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                  |
|------|--------------------|------|-------|--------------------------------------------------------------|
| 31:3 | RESERVED           | NONE | 0h    | Reserved                                                     |
| 2:0  | DMAXBAR3_GSEL_GSEL | R/W  | 0h    | Select input source:<br>0:G0 selected<br>..<br>5:G5 selected |

### 3.13.2.23 CONTROLSS\_DMAXBAR3\_G0 Register

#### 1 CONTROLSS\_DMAXBAR3\_G0 Register (Offset = 1C4h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1927. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 61C4h       |

**Figure 3-620. CONTROLSS\_DMAXBAR3\_G0 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR3_G0_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-1929. CONTROLSS\_DMAXBAR3\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                              |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED        | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR3_G0_SEL | R/W  | 0h    | EPWM SOCA to corresponding XBAR<br>1:PWMx.SOCA is selected<br>0:PWMx.SOCA is de-selected |



### 3.13.2.24 CONTROLSS\_DMAXBAR3\_G1 Register

#### 1 CONTROLSS\_DMAXBAR3\_G1 Register (Offset = 1C8h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1930. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 61C8h       |

**Figure 3-621. CONTROLSS\_DMAXBAR3\_G1 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR3_G1_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-1932. CONTROLSS\_DMAXBAR3\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                              |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED        | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR3_G1_SEL | R/W  | 0h    | EPWM SOCB to corresponding XBAR<br>1:PWMx.SOCB is selected<br>0:PWMx.SOCB is de-selected |

### 3.13.2.25 CONTROLSS\_DMAXBAR3\_G2 Register

#### 1 CONTROLSS\_DMAXBAR3\_G2 Register (Offset = 1CCh) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1933. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 61CCh       |

**Figure 3-622. CONTROLSS\_DMAXBAR3\_G2 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR3_G2_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-1935. CONTROLSS\_DMAXBAR3\_G2 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:5 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-1935. CONTROLSS\_DMAXBAR3\_G2 Register Field Descriptions (continued)**

| Bit | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | DMAXBAR3_G2_SEL | R/W  | 0h    | ADC DMA requests to corresponding XBAR<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.13.2.26 CONTROLSS\_DMAXBAR3\_G3 Register

#### 1 CONTROLSS\_DMAXBAR3\_G3 Register (Offset = 1D0h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1936. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 61D0h       |

**Figure 3-623. CONTROLSS\_DMAXBAR3\_G3 Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR3_G3_SEL |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 3-1938. CONTROLSS\_DMAXBAR3\_G3 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                         |
| 3:0  | DMAXBAR3_G3_SEL | R/W  | 0h    | FSI DMA requests to corresponding XBAR<br>0:FSIRX0.RX_DMA_EVT<br>1; FSIRX0_DMATRIG1<br>2:FSIRX0_DMATRIG2<br>3:FSIRX1.RX_DMA_EVT<br>4; FSIRX1_DMATRIG1<br>5:FSIRX1_DMATRIG2<br>6:FSIRX2.RX_DMA_EVT<br>7; FSIRX2_DMATRIG1<br>8:FSIRX2_DMATRIG2<br>9:FSIRX3.RX_DMA_EVT<br>10; FSIRX3_DMATRIG1<br>11:FSIRX3_DMATRIG2<br>12:FSITX0.TX_DMA_EVT<br>13:FSITX1.TX_DMA_EVT<br>14:FSITX2.TX_DMA_EVT<br>15:FSITX3.TX_DMA_EVT |

### 3.13.2.27 CONTROLSS\_DMAXBAR3\_G4 Register

#### 1 CONTROLSS\_DMAXBAR3\_G4 Register (Offset = 1D4h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1939. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 61D4h       |

**Figure 3-624. CONTROLSS\_DMAXBAR3\_G4 Name Register**

|          |    |    |    |    |                 |    |    |
|----------|----|----|----|----|-----------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26              | 25 | 24 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 23       | 22 | 21 | 20 | 19 | 18              | 17 | 16 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 15       | 14 | 13 | 12 | 11 | 10              | 9  | 8  |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 7        | 6  | 5  | 4  | 3  | 2               | 1  | 0  |
| RESERVED |    |    |    |    | DMAXBAR3_G4_SEL |    |    |
| NONE     |    |    |    |    | R/W             |    |    |
| 0h       |    |    |    |    | 0h              |    |    |

**Table 3-1941. CONTROLSS\_DMAXBAR3\_G4 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                     |
|------|-----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                        |
| 2:0  | DMAXBAR3_G4_SEL | R/W  | 0h    | SDFM DMA requests to corresponding XBAR<br>0:SD0.FILT1.DRINT<br>1:SD0.FILT2.DRINT<br>2:SD0.FILT3.DRINT<br>3:SD0.FILT4.DRINT<br>4:SD1.FILT1.DRINT<br>5:SD1.FILT2.DRINT<br>6:SD1.FILT3.DRINT<br>7:SD1.FILT4.DRINT |

### 3.13.2.28 CONTROLSS\_DMAXBAR3\_G5 Register

#### 1 CONTROLSS\_DMAXBAR3\_G5 Register (Offset = 1D8h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1942. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 61D8h       |

**Figure 3-625. CONTROLSS\_DMAXBAR3\_G5 Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR3_G5_SEL |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 3-1944. CONTROLSS\_DMAXBAR3\_G5 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                              |
| 3:0  | DMAXBAR3_G5_SEL | R/W  | 0h    | ECAP DMA requests to corresponding XBAR<br>0:ECAP0.DMA_INT<br>1:ECAP1.DMA_INT<br>2:ECAP2.DMA_INT<br>3:ECAP3.DMA_INT<br>4:ECAP4.DMA_INT<br>5:ECAP5.DMA_INT<br>6:ECAP6.DMA_INT<br>7:ECAP7.DMA_INT<br>8:ECAP8.DMA_INT<br>9:ECAP9.DMA_INT |

### 3.13.2.29 CONTROLSS\_DMAXBAR4\_GSEL Register

#### 1 CONTROLSS\_DMAXBAR4\_GSEL Register (Offset = 200h) [reset = 0h]

Group Select register to select between G0-G5.

Return to [Summary Table](#)

**Table 3-1945. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6200h       |

**Figure 3-626. CONTROLSS\_DMAXBAR4\_GSEL Name Register**

|          |    |    |    |    |                    |    |    |
|----------|----|----|----|----|--------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                 | 25 | 24 |
| RESERVED |    |    |    |    |                    |    |    |
| NONE     |    |    |    |    |                    |    |    |
| 0h       |    |    |    |    |                    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                 | 17 | 16 |
| RESERVED |    |    |    |    |                    |    |    |
| NONE     |    |    |    |    |                    |    |    |
| 0h       |    |    |    |    |                    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                 | 9  | 8  |
| RESERVED |    |    |    |    |                    |    |    |
| NONE     |    |    |    |    |                    |    |    |
| 0h       |    |    |    |    |                    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                  | 1  | 0  |
| RESERVED |    |    |    |    | DMAXBAR4_GSEL_GSEL |    |    |
| NONE     |    |    |    |    | R/W                |    |    |
| 0h       |    |    |    |    | 0h                 |    |    |

**Table 3-1947. CONTROLSS\_DMAXBAR4\_GSEL Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                  |
|------|--------------------|------|-------|--------------------------------------------------------------|
| 31:3 | RESERVED           | NONE | 0h    | Reserved                                                     |
| 2:0  | DMAXBAR4_GSEL_GSEL | R/W  | 0h    | Select input source:<br>0:G0 selected<br>..<br>5:G5 selected |

### 3.13.2.30 CONTROLSS\_DMAXBAR4\_G0 Register

#### 1 CONTROLSS\_DMAXBAR4\_G0 Register (Offset = 204h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1948. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6204h       |

**Figure 3-627. CONTROLSS\_DMAXBAR4\_G0 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR4_G0_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-1950. CONTROLSS\_DMAXBAR4\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                              |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED        | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR4_G0_SEL | R/W  | 0h    | EPWM SOCA to corresponding XBAR<br>1:PWMx.SOCA is selected<br>0:PWMx.SOCA is de-selected |



### 3.13.2.31 CONTROLSS\_DMAXBAR4\_G1 Register

#### 1 CONTROLSS\_DMAXBAR4\_G1 Register (Offset = 208h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1951. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6208h       |

**Figure 3-628. CONTROLSS\_DMAXBAR4\_G1 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR4_G1_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-1953. CONTROLSS\_DMAXBAR4\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                              |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED        | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR4_G1_SEL | R/W  | 0h    | EPWM SOCB to corresponding XBAR<br>1:PWMx.SOCB is selected<br>0:PWMx.SOCB is de-selected |

### 3.13.2.32 CONTROLSS\_DMAXBAR4\_G2 Register

#### 1 CONTROLSS\_DMAXBAR4\_G2 Register (Offset = 20Ch) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1954. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 620Ch       |

**Figure 3-629. CONTROLSS\_DMAXBAR4\_G2 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR4_G2_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-1956. CONTROLSS\_DMAXBAR4\_G2 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:5 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-1956. CONTROLSS\_DMAXBAR4\_G2 Register Field Descriptions (continued)**

| Bit | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | DMAXBAR4_G2_SEL | R/W  | 0h    | ADC DMA requests to corresponding XBAR<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.13.2.33 CONTROLSS\_DMAXBAR4\_G3 Register

#### 1 CONTROLSS\_DMAXBAR4\_G3 Register (Offset = 210h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1957. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6210h       |

**Figure 3-630. CONTROLSS\_DMAXBAR4\_G3 Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR4_G3_SEL |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 3-1959. CONTROLSS\_DMAXBAR4\_G3 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                         |
| 3:0  | DMAXBAR4_G3_SEL | R/W  | 0h    | FSI DMA requests to corresponding XBAR<br>0:FSIRX0.RX_DMA_EVT<br>1; FSIRX0_DMATRIG1<br>2:FSIRX0_DMATRIG2<br>3:FSIRX1.RX_DMA_EVT<br>4; FSIRX1_DMATRIG1<br>5:FSIRX1_DMATRIG2<br>6:FSIRX2.RX_DMA_EVT<br>7; FSIRX2_DMATRIG1<br>8:FSIRX2_DMATRIG2<br>9:FSIRX3.RX_DMA_EVT<br>10; FSIRX3_DMATRIG1<br>11:FSIRX3_DMATRIG2<br>12:FSITX0.TX_DMA_EVT<br>13:FSITX1.TX_DMA_EVT<br>14:FSITX2.TX_DMA_EVT<br>15:FSITX3.TX_DMA_EVT |

### 3.13.2.34 CONTROLSS\_DMAXBAR4\_G4 Register

#### 1 CONTROLSS\_DMAXBAR4\_G4 Register (Offset = 214h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1960. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6214h       |

**Figure 3-631. CONTROLSS\_DMAXBAR4\_G4 Name Register**

|          |    |    |    |    |                 |    |    |
|----------|----|----|----|----|-----------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26              | 25 | 24 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 23       | 22 | 21 | 20 | 19 | 18              | 17 | 16 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 15       | 14 | 13 | 12 | 11 | 10              | 9  | 8  |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 7        | 6  | 5  | 4  | 3  | 2               | 1  | 0  |
| RESERVED |    |    |    |    | DMAXBAR4_G4_SEL |    |    |
| NONE     |    |    |    |    | R/W             |    |    |
| 0h       |    |    |    |    | 0h              |    |    |

**Table 3-1962. CONTROLSS\_DMAXBAR4\_G4 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                     |
|------|-----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                        |
| 2:0  | DMAXBAR4_G4_SEL | R/W  | 0h    | SDFM DMA requests to corresponding XBAR<br>0:SD0.FILT1.DRINT<br>1:SD0.FILT2.DRINT<br>2:SD0.FILT3.DRINT<br>3:SD0.FILT4.DRINT<br>4:SD1.FILT1.DRINT<br>5:SD1.FILT2.DRINT<br>6:SD1.FILT3.DRINT<br>7:SD1.FILT4.DRINT |

### 3.13.2.35 CONTROLSS\_DMAXBAR4\_G5 Register

#### 1 CONTROLSS\_DMAXBAR4\_G5 Register (Offset = 218h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1963. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6218h       |

**Figure 3-632. CONTROLSS\_DMAXBAR4\_G5 Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR4_G5_SEL |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 3-1965. CONTROLSS\_DMAXBAR4\_G5 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                              |
| 3:0  | DMAXBAR4_G5_SEL | R/W  | 0h    | ECAP DMA requests to corresponding XBAR<br>0:ECAP0.DMA_INT<br>1:ECAP1.DMA_INT<br>2:ECAP2.DMA_INT<br>3:ECAP3.DMA_INT<br>4:ECAP4.DMA_INT<br>5:ECAP5.DMA_INT<br>6:ECAP6.DMA_INT<br>7:ECAP7.DMA_INT<br>8:ECAP8.DMA_INT<br>9:ECAP9.DMA_INT |

### 3.13.2.36 CONTROLSS\_DMAXBAR5\_GSEL Register

#### 1 CONTROLSS\_DMAXBAR5\_GSEL Register (Offset = 240h) [reset = 0h]

Group Select register to select between G0-G5.

Return to [Summary Table](#)

**Table 3-1966. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6240h       |

**Figure 3-633. CONTROLSS\_DMAXBAR5\_GSEL Name Register**

|          |    |    |    |    |                    |    |    |
|----------|----|----|----|----|--------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                 | 25 | 24 |
| RESERVED |    |    |    |    |                    |    |    |
| NONE     |    |    |    |    |                    |    |    |
| 0h       |    |    |    |    |                    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                 | 17 | 16 |
| RESERVED |    |    |    |    |                    |    |    |
| NONE     |    |    |    |    |                    |    |    |
| 0h       |    |    |    |    |                    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                 | 9  | 8  |
| RESERVED |    |    |    |    |                    |    |    |
| NONE     |    |    |    |    |                    |    |    |
| 0h       |    |    |    |    |                    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                  | 1  | 0  |
| RESERVED |    |    |    |    | DMAXBAR5_GSEL_GSEL |    |    |
| NONE     |    |    |    |    | R/W                |    |    |
| 0h       |    |    |    |    | 0h                 |    |    |

**Table 3-1968. CONTROLSS\_DMAXBAR5\_GSEL Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                  |
|------|--------------------|------|-------|--------------------------------------------------------------|
| 31:3 | RESERVED           | NONE | 0h    | Reserved                                                     |
| 2:0  | DMAXBAR5_GSEL_GSEL | R/W  | 0h    | Select input source:<br>0:G0 selected<br>..<br>5:G5 selected |

### 3.13.2.37 CONTROLSS\_DMAXBAR5\_G0 Register

#### 1 CONTROLSS\_DMAXBAR5\_G0 Register (Offset = 244h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1969. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6244h       |

**Figure 3-634. CONTROLSS\_DMAXBAR5\_G0 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR5_G0_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-1971. CONTROLSS\_DMAXBAR5\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                              |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED        | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR5_G0_SEL | R/W  | 0h    | EPWM SOCA to corresponding XBAR<br>1:PWMx.SOCA is selected<br>0:PWMx.SOCA is de-selected |



### 3.13.2.38 CONTROLSS\_DMAXBAR5\_G1 Register

#### 1 CONTROLSS\_DMAXBAR5\_G1 Register (Offset = 248h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1972. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6248h       |

**Figure 3-635. CONTROLSS\_DMAXBAR5\_G1 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR5_G1_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-1974. CONTROLSS\_DMAXBAR5\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                              |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED        | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR5_G1_SEL | R/W  | 0h    | EPWM SOCB to corresponding XBAR<br>1:PWMx.SOCB is selected<br>0:PWMx.SOCB is de-selected |

### 3.13.2.39 CONTROLSS\_DMAXBAR5\_G2 Register

#### 1 CONTROLSS\_DMAXBAR5\_G2 Register (Offset = 24Ch) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1975. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 624Ch       |

**Figure 3-636. CONTROLSS\_DMAXBAR5\_G2 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR5_G2_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-1977. CONTROLSS\_DMAXBAR5\_G2 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:5 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-1977. CONTROLSS\_DMAXBAR5\_G2 Register Field Descriptions (continued)**

| Bit | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | DMAXBAR5_G2_SEL | R/W  | 0h    | ADC DMA requests to corresponding XBAR<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.13.2.40 CONTROLSS\_DMAXBAR5\_G3 Register

#### 1 CONTROLSS\_DMAXBAR5\_G3 Register (Offset = 250h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1978. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6250h       |

**Figure 3-637. CONTROLSS\_DMAXBAR5\_G3 Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR5_G3_SEL |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 3-1980. CONTROLSS\_DMAXBAR5\_G3 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                         |
| 3:0  | DMAXBAR5_G3_SEL | R/W  | 0h    | FSI DMA requests to corresponding XBAR<br>0:FSIRX0.RX_DMA_EVT<br>1; FSIRX0_DMATRIG1<br>2:FSIRX0_DMATRIG2<br>3:FSIRX1.RX_DMA_EVT<br>4; FSIRX1_DMATRIG1<br>5:FSIRX1_DMATRIG2<br>6:FSIRX2.RX_DMA_EVT<br>7; FSIRX2_DMATRIG1<br>8:FSIRX2_DMATRIG2<br>9:FSIRX3.RX_DMA_EVT<br>10; FSIRX3_DMATRIG1<br>11:FSIRX3_DMATRIG2<br>12:FSITX0.TX_DMA_EVT<br>13:FSITX1.TX_DMA_EVT<br>14:FSITX2.TX_DMA_EVT<br>15:FSITX3.TX_DMA_EVT |

### 3.13.2.41 CONTROLSS\_DMAXBAR5\_G4 Register

#### 1 CONTROLSS\_DMAXBAR5\_G4 Register (Offset = 254h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1981. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6254h       |

**Figure 3-638. CONTROLSS\_DMAXBAR5\_G4 Name Register**

|          |    |    |    |    |                 |    |    |
|----------|----|----|----|----|-----------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26              | 25 | 24 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 23       | 22 | 21 | 20 | 19 | 18              | 17 | 16 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 15       | 14 | 13 | 12 | 11 | 10              | 9  | 8  |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 7        | 6  | 5  | 4  | 3  | 2               | 1  | 0  |
| RESERVED |    |    |    |    | DMAXBAR5_G4_SEL |    |    |
| NONE     |    |    |    |    | R/W             |    |    |
| 0h       |    |    |    |    | 0h              |    |    |

**Table 3-1983. CONTROLSS\_DMAXBAR5\_G4 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                     |
|------|-----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                        |
| 2:0  | DMAXBAR5_G4_SEL | R/W  | 0h    | SDFM DMA requests to corresponding XBAR<br>0:SD0.FILT1.DRINT<br>1:SD0.FILT2.DRINT<br>2:SD0.FILT3.DRINT<br>3:SD0.FILT4.DRINT<br>4:SD1.FILT1.DRINT<br>5:SD1.FILT2.DRINT<br>6:SD1.FILT3.DRINT<br>7:SD1.FILT4.DRINT |

### 3.13.2.42 CONTROLSS\_DMAXBAR5\_G5 Register

#### 1 CONTROLSS\_DMAXBAR5\_G5 Register (Offset = 258h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1984. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6258h       |

**Figure 3-639. CONTROLSS\_DMAXBAR5\_G5 Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR5_G5_SEL |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 3-1986. CONTROLSS\_DMAXBAR5\_G5 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                              |
| 3:0  | DMAXBAR5_G5_SEL | R/W  | 0h    | ECAP DMA requests to corresponding XBAR<br>0:ECAP0.DMA_INT<br>1:ECAP1.DMA_INT<br>2:ECAP2.DMA_INT<br>3:ECAP3.DMA_INT<br>4:ECAP4.DMA_INT<br>5:ECAP5.DMA_INT<br>6:ECAP6.DMA_INT<br>7:ECAP7.DMA_INT<br>8:ECAP8.DMA_INT<br>9:ECAP9.DMA_INT |

### 3.13.2.43 CONTROLSS\_DMAXBAR6\_GSEL Register

#### 1 CONTROLSS\_DMAXBAR6\_GSEL Register (Offset = 280h) [reset = 0h]

Group Select register to select between G0-G5.

Return to [Summary Table](#)

**Table 3-1987. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6280h       |

**Figure 3-640. CONTROLSS\_DMAXBAR6\_GSEL Name Register**

|          |    |    |    |    |                    |    |    |
|----------|----|----|----|----|--------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                 | 25 | 24 |
| RESERVED |    |    |    |    |                    |    |    |
| NONE     |    |    |    |    |                    |    |    |
| 0h       |    |    |    |    |                    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                 | 17 | 16 |
| RESERVED |    |    |    |    |                    |    |    |
| NONE     |    |    |    |    |                    |    |    |
| 0h       |    |    |    |    |                    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                 | 9  | 8  |
| RESERVED |    |    |    |    |                    |    |    |
| NONE     |    |    |    |    |                    |    |    |
| 0h       |    |    |    |    |                    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                  | 1  | 0  |
| RESERVED |    |    |    |    | DMAXBAR6_GSEL_GSEL |    |    |
| NONE     |    |    |    |    | R/W                |    |    |
| 0h       |    |    |    |    | 0h                 |    |    |

**Table 3-1989. CONTROLSS\_DMAXBAR6\_GSEL Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                  |
|------|--------------------|------|-------|--------------------------------------------------------------|
| 31:3 | RESERVED           | NONE | 0h    | Reserved                                                     |
| 2:0  | DMAXBAR6_GSEL_GSEL | R/W  | 0h    | Select input source:<br>0:G0 selected<br>..<br>5:G5 selected |

### 3.13.2.44 CONTROLSS\_DMAXBAR6\_G0 Register

#### 1 CONTROLSS\_DMAXBAR6\_G0 Register (Offset = 284h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1990. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6284h       |

**Figure 3-641. CONTROLSS\_DMAXBAR6\_G0 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR6_G0_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-1992. CONTROLSS\_DMAXBAR6\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                              |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED        | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR6_G0_SEL | R/W  | 0h    | EPWM SOCA to corresponding XBAR<br>1:PWMx.SOCA is selected<br>0:PWMx.SOCA is de-selected |



### 3.13.2.45 CONTROLSS\_DMAXBAR6\_G1 Register

#### 1 CONTROLSS\_DMAXBAR6\_G1 Register (Offset = 288h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1993. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6288h       |

**Figure 3-642. CONTROLSS\_DMAXBAR6\_G1 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR6_G1_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-1995. CONTROLSS\_DMAXBAR6\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                              |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED        | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR6_G1_SEL | R/W  | 0h    | EPWM SOCB to corresponding XBAR<br>1:PWMx.SOCB is selected<br>0:PWMx.SOCB is de-selected |

### 3.13.2.46 CONTROLSS\_DMAXBAR6\_G2 Register

#### 1 CONTROLSS\_DMAXBAR6\_G2 Register (Offset = 28Ch) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1996. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 628Ch       |

**Figure 3-643. CONTROLSS\_DMAXBAR6\_G2 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR6_G2_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-1998. CONTROLSS\_DMAXBAR6\_G2 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:5 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-1998. CONTROLSS\_DMAXBAR6\_G2 Register Field Descriptions (continued)**

| Bit | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | DMAXBAR6_G2_SEL | R/W  | 0h    | ADC DMA requests to corresponding XBAR<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.13.2.47 CONTROLSS\_DMAXBAR6\_G3 Register

#### 1 CONTROLSS\_DMAXBAR6\_G3 Register (Offset = 290h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-1999. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6290h       |

**Figure 3-644. CONTROLSS\_DMAXBAR6\_G3 Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR6_G3_SEL |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 3-2001. CONTROLSS\_DMAXBAR6\_G3 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                         |
| 3:0  | DMAXBAR6_G3_SEL | R/W  | 0h    | FSI DMA requests to corresponding XBAR<br>0:FSIRX0.RX_DMA_EVT<br>1; FSIRX0_DMATRIG1<br>2:FSIRX0_DMATRIG2<br>3:FSIRX1.RX_DMA_EVT<br>4; FSIRX1_DMATRIG1<br>5:FSIRX1_DMATRIG2<br>6:FSIRX2.RX_DMA_EVT<br>7; FSIRX2_DMATRIG1<br>8:FSIRX2_DMATRIG2<br>9:FSIRX3.RX_DMA_EVT<br>10; FSIRX3_DMATRIG1<br>11:FSIRX3_DMATRIG2<br>12:FSITX0.TX_DMA_EVT<br>13:FSITX1.TX_DMA_EVT<br>14:FSITX2.TX_DMA_EVT<br>15:FSITX3.TX_DMA_EVT |

### 3.13.2.48 CONTROLSS\_DMAXBAR6\_G4 Register

#### 1 CONTROLSS\_DMAXBAR6\_G4 Register (Offset = 294h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2002. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6294h       |

**Figure 3-645. CONTROLSS\_DMAXBAR6\_G4 Name Register**

|          |    |    |    |    |                 |    |    |
|----------|----|----|----|----|-----------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26              | 25 | 24 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 23       | 22 | 21 | 20 | 19 | 18              | 17 | 16 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 15       | 14 | 13 | 12 | 11 | 10              | 9  | 8  |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 7        | 6  | 5  | 4  | 3  | 2               | 1  | 0  |
| RESERVED |    |    |    |    | DMAXBAR6_G4_SEL |    |    |
| NONE     |    |    |    |    | R/W             |    |    |
| 0h       |    |    |    |    | 0h              |    |    |

**Table 3-2004. CONTROLSS\_DMAXBAR6\_G4 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                     |
|------|-----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                        |
| 2:0  | DMAXBAR6_G4_SEL | R/W  | 0h    | SDFM DMA requests to corresponding XBAR<br>0:SD0.FILT1.DRINT<br>1:SD0.FILT2.DRINT<br>2:SD0.FILT3.DRINT<br>3:SD0.FILT4.DRINT<br>4:SD1.FILT1.DRINT<br>5:SD1.FILT2.DRINT<br>6:SD1.FILT3.DRINT<br>7:SD1.FILT4.DRINT |

### 3.13.2.49 CONTROLSS\_DMAXBAR6\_G5 Register

#### 1 CONTROLSS\_DMAXBAR6\_G5 Register (Offset = 298h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2005. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6298h       |

**Figure 3-646. CONTROLSS\_DMAXBAR6\_G5 Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR6_G5_SEL |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 3-2007. CONTROLSS\_DMAXBAR6\_G5 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                              |
| 3:0  | DMAXBAR6_G5_SEL | R/W  | 0h    | ECAP DMA requests to corresponding XBAR<br>0:ECAP0.DMA_INT<br>1:ECAP1.DMA_INT<br>2:ECAP2.DMA_INT<br>3:ECAP3.DMA_INT<br>4:ECAP4.DMA_INT<br>5:ECAP5.DMA_INT<br>6:ECAP6.DMA_INT<br>7:ECAP7.DMA_INT<br>8:ECAP8.DMA_INT<br>9:ECAP9.DMA_INT |

### 3.13.2.50 CONTROLSS\_DMAXBAR7\_GSEL Register

#### 1 CONTROLSS\_DMAXBAR7\_GSEL Register (Offset = 2C0h) [reset = 0h]

Group Select register to select between G0-G5.

Return to [Summary Table](#)

**Table 3-2008. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 62C0h       |

**Figure 3-647. CONTROLSS\_DMAXBAR7\_GSEL Name Register**

|          |    |    |    |    |                    |    |    |
|----------|----|----|----|----|--------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                 | 25 | 24 |
| RESERVED |    |    |    |    |                    |    |    |
| NONE     |    |    |    |    |                    |    |    |
| 0h       |    |    |    |    |                    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                 | 17 | 16 |
| RESERVED |    |    |    |    |                    |    |    |
| NONE     |    |    |    |    |                    |    |    |
| 0h       |    |    |    |    |                    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                 | 9  | 8  |
| RESERVED |    |    |    |    |                    |    |    |
| NONE     |    |    |    |    |                    |    |    |
| 0h       |    |    |    |    |                    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                  | 1  | 0  |
| RESERVED |    |    |    |    | DMAXBAR7_GSEL_GSEL |    |    |
| NONE     |    |    |    |    | R/W                |    |    |
| 0h       |    |    |    |    | 0h                 |    |    |

**Table 3-2010. CONTROLSS\_DMAXBAR7\_GSEL Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                  |
|------|--------------------|------|-------|--------------------------------------------------------------|
| 31:3 | RESERVED           | NONE | 0h    | Reserved                                                     |
| 2:0  | DMAXBAR7_GSEL_GSEL | R/W  | 0h    | Select input source:<br>0:G0 selected<br>..<br>5:G5 selected |

### 3.13.2.51 CONTROLSS\_DMAXBAR7\_G0 Register

#### 1 CONTROLSS\_DMAXBAR7\_G0 Register (Offset = 2C4h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2011. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 62C4h       |

**Figure 3-648. CONTROLSS\_DMAXBAR7\_G0 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR7_G0_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-2013. CONTROLSS\_DMAXBAR7\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                              |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED        | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR7_G0_SEL | R/W  | 0h    | EPWM SOCA to corresponding XBAR<br>1:PWMx.SOCA is selected<br>0:PWMx.SOCA is de-selected |



### 3.13.2.52 CONTROLSS\_DMAXBAR7\_G1 Register

#### 1 CONTROLSS\_DMAXBAR7\_G1 Register (Offset = 2C8h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2014. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 62C8h       |

**Figure 3-649. CONTROLSS\_DMAXBAR7\_G1 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR7_G1_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-2016. CONTROLSS\_DMAXBAR7\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                              |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED        | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR7_G1_SEL | R/W  | 0h    | EPWM SOCB to corresponding XBAR<br>1:PWMx.SOCB is selected<br>0:PWMx.SOCB is de-selected |

### 3.13.2.53 CONTROLSS\_DMAXBAR7\_G2 Register

#### 1 CONTROLSS\_DMAXBAR7\_G2 Register (Offset = 2CCh) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2017. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 62CCh       |

**Figure 3-650. CONTROLSS\_DMAXBAR7\_G2 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR7_G2_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-2019. CONTROLSS\_DMAXBAR7\_G2 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:5 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-2019. CONTROLSS\_DMAXBAR7\_G2 Register Field Descriptions (continued)**

| Bit | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | DMAXBAR7_G2_SEL | R/W  | 0h    | ADC DMA requests to corresponding XBAR<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.13.2.54 CONTROLSS\_DMAXBAR7\_G3 Register

#### 1 CONTROLSS\_DMAXBAR7\_G3 Register (Offset = 2D0h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2020. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 62D0h       |

**Figure 3-651. CONTROLSS\_DMAXBAR7\_G3 Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR7_G3_SEL |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 3-2022. CONTROLSS\_DMAXBAR7\_G3 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                         |
| 3:0  | DMAXBAR7_G3_SEL | R/W  | 0h    | FSI DMA requests to corresponding XBAR<br>0:FSIRX0.RX_DMA_EVT<br>1; FSIRX0_DMATRIG1<br>2:FSIRX0_DMATRIG2<br>3:FSIRX1.RX_DMA_EVT<br>4; FSIRX1_DMATRIG1<br>5:FSIRX1_DMATRIG2<br>6:FSIRX2.RX_DMA_EVT<br>7; FSIRX2_DMATRIG1<br>8:FSIRX2_DMATRIG2<br>9:FSIRX3.RX_DMA_EVT<br>10; FSIRX3_DMATRIG1<br>11:FSIRX3_DMATRIG2<br>12:FSITX0.TX_DMA_EVT<br>13:FSITX1.TX_DMA_EVT<br>14:FSITX2.TX_DMA_EVT<br>15:FSITX3.TX_DMA_EVT |

### 3.13.2.55 CONTROLSS\_DMAXBAR7\_G4 Register

#### 1 CONTROLSS\_DMAXBAR7\_G4 Register (Offset = 2D4h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2023. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 62D4h       |

**Figure 3-652. CONTROLSS\_DMAXBAR7\_G4 Name Register**

|          |    |    |    |    |                 |    |    |
|----------|----|----|----|----|-----------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26              | 25 | 24 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 23       | 22 | 21 | 20 | 19 | 18              | 17 | 16 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 15       | 14 | 13 | 12 | 11 | 10              | 9  | 8  |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 7        | 6  | 5  | 4  | 3  | 2               | 1  | 0  |
| RESERVED |    |    |    |    | DMAXBAR7_G4_SEL |    |    |
| NONE     |    |    |    |    | R/W             |    |    |
| 0h       |    |    |    |    | 0h              |    |    |

**Table 3-2025. CONTROLSS\_DMAXBAR7\_G4 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                     |
|------|-----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                        |
| 2:0  | DMAXBAR7_G4_SEL | R/W  | 0h    | SDFM DMA requests to corresponding XBAR<br>0:SD0.FILT1.DRINT<br>1:SD0.FILT2.DRINT<br>2:SD0.FILT3.DRINT<br>3:SD0.FILT4.DRINT<br>4:SD1.FILT1.DRINT<br>5:SD1.FILT2.DRINT<br>6:SD1.FILT3.DRINT<br>7:SD1.FILT4.DRINT |

### 3.13.2.56 CONTROLSS\_DMAXBAR7\_G5 Register

#### 1 CONTROLSS\_DMAXBAR7\_G5 Register (Offset = 2D8h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2026. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 62D8h       |

**Figure 3-653. CONTROLSS\_DMAXBAR7\_G5 Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR7_G5_SEL |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 3-2028. CONTROLSS\_DMAXBAR7\_G5 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                              |
| 3:0  | DMAXBAR7_G5_SEL | R/W  | 0h    | ECAP DMA requests to corresponding XBAR<br>0:ECAP0.DMA_INT<br>1:ECAP1.DMA_INT<br>2:ECAP2.DMA_INT<br>3:ECAP3.DMA_INT<br>4:ECAP4.DMA_INT<br>5:ECAP5.DMA_INT<br>6:ECAP6.DMA_INT<br>7:ECAP7.DMA_INT<br>8:ECAP8.DMA_INT<br>9:ECAP9.DMA_INT |

### 3.13.2.57 CONTROLSS\_DMAXBAR8\_GSEL Register

#### 1 CONTROLSS\_DMAXBAR8\_GSEL Register (Offset = 300h) [reset = 0h]

Group Select register to select between G0-G5.

Return to [Summary Table](#)

**Table 3-2029. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6300h       |

**Figure 3-654. CONTROLSS\_DMAXBAR8\_GSEL Name Register**

|          |    |    |    |                    |    |    |    |
|----------|----|----|----|--------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 23       | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 15       | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 7        | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR8_GSEL_GSEL |    |    |    |
| NONE     |    |    |    | R/W                |    |    |    |
| 0h       |    |    |    | 0h                 |    |    |    |

**Table 3-2031. CONTROLSS\_DMAXBAR8\_GSEL Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                  |
|------|--------------------|------|-------|--------------------------------------------------------------|
| 31:3 | RESERVED           | NONE | 0h    | Reserved                                                     |
| 2:0  | DMAXBAR8_GSEL_GSEL | R/W  | 0h    | Select input source:<br>0:G0 selected<br>..<br>5:G5 selected |

### 3.13.2.58 CONTROLSS\_DMAXBAR8\_G0 Register

#### 1 CONTROLSS\_DMAXBAR8\_G0 Register (Offset = 304h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2032. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6304h       |

**Figure 3-655. CONTROLSS\_DMAXBAR8\_G0 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR8_G0_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-2034. CONTROLSS\_DMAXBAR8\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                              |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED        | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR8_G0_SEL | R/W  | 0h    | EPWM SOCA to corresponding XBAR<br>1:PWMx.SOCA is selected<br>0:PWMx.SOCA is de-selected |



### 3.13.2.59 CONTROLSS\_DMAXBAR8\_G1 Register

#### 1 CONTROLSS\_DMAXBAR8\_G1 Register (Offset = 308h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2035. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6308h       |

**Figure 3-656. CONTROLSS\_DMAXBAR8\_G1 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR8_G1_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-2037. CONTROLSS\_DMAXBAR8\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                              |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED        | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR8_G1_SEL | R/W  | 0h    | EPWM SOCB to corresponding XBAR<br>1:PWMx.SOCB is selected<br>0:PWMx.SOCB is de-selected |

### 3.13.2.60 CONTROLSS\_DMAXBAR8\_G2 Register

#### 1 CONTROLSS\_DMAXBAR8\_G2 Register (Offset = 30Ch) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2038. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 630Ch       |

**Figure 3-657. CONTROLSS\_DMAXBAR8\_G2 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR8_G2_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-2040. CONTROLSS\_DMAXBAR8\_G2 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:5 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-2040. CONTROLSS\_DMAXBAR8\_G2 Register Field Descriptions (continued)**

| Bit | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | DMAXBAR8_G2_SEL | R/W  | 0h    | ADC DMA requests to corresponding XBAR<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.13.2.61 CONTROLSS\_DMAXBAR8\_G3 Register

#### 1 CONTROLSS\_DMAXBAR8\_G3 Register (Offset = 310h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2041. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6310h       |

**Figure 3-658. CONTROLSS\_DMAXBAR8\_G3 Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR8_G3_SEL |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 3-2043. CONTROLSS\_DMAXBAR8\_G3 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                         |
| 3:0  | DMAXBAR8_G3_SEL | R/W  | 0h    | FSI DMA requests to corresponding XBAR<br>0:FSIRX0.RX_DMA_EVT<br>1; FSIRX0_DMATRIG1<br>2:FSIRX0_DMATRIG2<br>3:FSIRX1.RX_DMA_EVT<br>4; FSIRX1_DMATRIG1<br>5:FSIRX1_DMATRIG2<br>6:FSIRX2.RX_DMA_EVT<br>7; FSIRX2_DMATRIG1<br>8:FSIRX2_DMATRIG2<br>9:FSIRX3.RX_DMA_EVT<br>10; FSIRX3_DMATRIG1<br>11:FSIRX3_DMATRIG2<br>12:FSITX0.TX_DMA_EVT<br>13:FSITX1.TX_DMA_EVT<br>14:FSITX2.TX_DMA_EVT<br>15:FSITX3.TX_DMA_EVT |

### 3.13.2.62 CONTROLSS\_DMAXBAR8\_G4 Register

#### 1 CONTROLSS\_DMAXBAR8\_G4 Register (Offset = 314h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2044. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6314h       |

**Figure 3-659. CONTROLSS\_DMAXBAR8\_G4 Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR8_G4_SEL |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 3-2046. CONTROLSS\_DMAXBAR8\_G4 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                     |
|------|-----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                        |
| 2:0  | DMAXBAR8_G4_SEL | R/W  | 0h    | SDFM DMA requests to corresponding XBAR<br>0:SD0.FILT1.DRINT<br>1:SD0.FILT2.DRINT<br>2:SD0.FILT3.DRINT<br>3:SD0.FILT4.DRINT<br>4:SD1.FILT1.DRINT<br>5:SD1.FILT2.DRINT<br>6:SD1.FILT3.DRINT<br>7:SD1.FILT4.DRINT |

### 3.13.2.63 CONTROLSS\_DMAXBAR8\_G5 Register

#### 1 CONTROLSS\_DMAXBAR8\_G5 Register (Offset = 318h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2047. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6318h       |

**Figure 3-660. CONTROLSS\_DMAXBAR8\_G5 Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR8_G5_SEL |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 3-2049. CONTROLSS\_DMAXBAR8\_G5 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                              |
| 3:0  | DMAXBAR8_G5_SEL | R/W  | 0h    | ECAP DMA requests to corresponding XBAR<br>0:ECAP0.DMA_INT<br>1:ECAP1.DMA_INT<br>2:ECAP2.DMA_INT<br>3:ECAP3.DMA_INT<br>4:ECAP4.DMA_INT<br>5:ECAP5.DMA_INT<br>6:ECAP6.DMA_INT<br>7:ECAP7.DMA_INT<br>8:ECAP8.DMA_INT<br>9:ECAP9.DMA_INT |

### 3.13.2.64 CONTROLSS\_DMAXBAR9\_GSEL Register

#### 1 CONTROLSS\_DMAXBAR9\_GSEL Register (Offset = 340h) [reset = 0h]

Group Select register to select between G0-G5.

Return to [Summary Table](#)

**Table 3-2050. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6340h       |

**Figure 3-661. CONTROLSS\_DMAXBAR9\_GSEL Name Register**

|          |    |    |    |                    |    |    |    |
|----------|----|----|----|--------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 23       | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 15       | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 7        | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR9_GSEL_GSEL |    |    |    |
| NONE     |    |    |    | R/W                |    |    |    |
| 0h       |    |    |    | 0h                 |    |    |    |

**Table 3-2052. CONTROLSS\_DMAXBAR9\_GSEL Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                  |
|------|--------------------|------|-------|--------------------------------------------------------------|
| 31:3 | RESERVED           | NONE | 0h    | Reserved                                                     |
| 2:0  | DMAXBAR9_GSEL_GSEL | R/W  | 0h    | Select input source:<br>0:G0 selected<br>..<br>5:G5 selected |

### 3.13.2.65 CONTROLSS\_DMAXBAR9\_G0 Register

#### 1 CONTROLSS\_DMAXBAR9\_G0 Register (Offset = 344h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2053. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6344h       |

**Figure 3-662. CONTROLSS\_DMAXBAR9\_G0 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR9_G0_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-2055. CONTROLSS\_DMAXBAR9\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                              |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED        | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR9_G0_SEL | R/W  | 0h    | EPWM SOCA to corresponding XBAR<br>1:PWMx.SOCA is selected<br>0:PWMx.SOCA is de-selected |



### 3.13.2.66 CONTROLSS\_DMAXBAR9\_G1 Register

#### 1 CONTROLSS\_DMAXBAR9\_G1 Register (Offset = 348h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2056. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6348h       |

**Figure 3-663. CONTROLSS\_DMAXBAR9\_G1 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR9_G1_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-2058. CONTROLSS\_DMAXBAR9\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                              |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED        | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR9_G1_SEL | R/W  | 0h    | EPWM SOCB to corresponding XBAR<br>1:PWMx.SOCB is selected<br>0:PWMx.SOCB is de-selected |

### 3.13.2.67 CONTROLSS\_DMAXBAR9\_G2 Register

#### 1 CONTROLSS\_DMAXBAR9\_G2 Register (Offset = 34Ch) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2059. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 634Ch       |

**Figure 3-664. CONTROLSS\_DMAXBAR9\_G2 Name Register**

|          |    |    |                 |    |    |    |    |
|----------|----|----|-----------------|----|----|----|----|
| 31       | 30 | 29 | 28              | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 23       | 22 | 21 | 20              | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 15       | 14 | 13 | 12              | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                 |    |    |    |    |
| NONE     |    |    |                 |    |    |    |    |
| 0h       |    |    |                 |    |    |    |    |
| 7        | 6  | 5  | 4               | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR9_G2_SEL |    |    |    |    |
| NONE     |    |    | R/W             |    |    |    |    |
| 0h       |    |    | 0h              |    |    |    |    |

**Table 3-2061. CONTROLSS\_DMAXBAR9\_G2 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:5 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-2061. CONTROLSS\_DMAXBAR9\_G2 Register Field Descriptions (continued)**

| Bit | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | DMAXBAR9_G2_SEL | R/W  | 0h    | ADC DMA requests to corresponding XBAR<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.13.2.68 CONTROLSS\_DMAXBAR9\_G3 Register

#### 1 CONTROLSS\_DMAXBAR9\_G3 Register (Offset = 350h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2062. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6350h       |

**Figure 3-665. CONTROLSS\_DMAXBAR9\_G3 Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR9_G3_SEL |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 3-2064. CONTROLSS\_DMAXBAR9\_G3 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                         |
| 3:0  | DMAXBAR9_G3_SEL | R/W  | 0h    | FSI DMA requests to corresponding XBAR<br>0:FSIRX0.RX_DMA_EVT<br>1; FSIRX0_DMATRIG1<br>2:FSIRX0_DMATRIG2<br>3:FSIRX1.RX_DMA_EVT<br>4; FSIRX1_DMATRIG1<br>5:FSIRX1_DMATRIG2<br>6:FSIRX2.RX_DMA_EVT<br>7; FSIRX2_DMATRIG1<br>8:FSIRX2_DMATRIG2<br>9:FSIRX3.RX_DMA_EVT<br>10; FSIRX3_DMATRIG1<br>11:FSIRX3_DMATRIG2<br>12:FSITX0.TX_DMA_EVT<br>13:FSITX1.TX_DMA_EVT<br>14:FSITX2.TX_DMA_EVT<br>15:FSITX3.TX_DMA_EVT |

### 3.13.2.69 CONTROLSS\_DMAXBAR9\_G4 Register

#### 1 CONTROLSS\_DMAXBAR9\_G4 Register (Offset = 354h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2065. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6354h       |

**Figure 3-666. CONTROLSS\_DMAXBAR9\_G4 Name Register**

|          |    |    |    |    |                 |    |    |
|----------|----|----|----|----|-----------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26              | 25 | 24 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 23       | 22 | 21 | 20 | 19 | 18              | 17 | 16 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 15       | 14 | 13 | 12 | 11 | 10              | 9  | 8  |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 7        | 6  | 5  | 4  | 3  | 2               | 1  | 0  |
| RESERVED |    |    |    |    | DMAXBAR9_G4_SEL |    |    |
| NONE     |    |    |    |    | R/W             |    |    |
| 0h       |    |    |    |    | 0h              |    |    |

**Table 3-2067. CONTROLSS\_DMAXBAR9\_G4 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                     |
|------|-----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                        |
| 2:0  | DMAXBAR9_G4_SEL | R/W  | 0h    | SDFM DMA requests to corresponding XBAR<br>0:SD0.FILT1.DRINT<br>1:SD0.FILT2.DRINT<br>2:SD0.FILT3.DRINT<br>3:SD0.FILT4.DRINT<br>4:SD1.FILT1.DRINT<br>5:SD1.FILT2.DRINT<br>6:SD1.FILT3.DRINT<br>7:SD1.FILT4.DRINT |

### 3.13.2.70 CONTROLSS\_DMAXBAR9\_G5 Register

#### 1 CONTROLSS\_DMAXBAR9\_G5 Register (Offset = 358h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2068. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6358h       |

**Figure 3-667. CONTROLSS\_DMAXBAR9\_G5 Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR9_G5_SEL |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 3-2070. CONTROLSS\_DMAXBAR9\_G5 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                              |
| 3:0  | DMAXBAR9_G5_SEL | R/W  | 0h    | ECAP DMA requests to corresponding XBAR<br>0:ECAP0.DMA_INT<br>1:ECAP1.DMA_INT<br>2:ECAP2.DMA_INT<br>3:ECAP3.DMA_INT<br>4:ECAP4.DMA_INT<br>5:ECAP5.DMA_INT<br>6:ECAP6.DMA_INT<br>7:ECAP7.DMA_INT<br>8:ECAP8.DMA_INT<br>9:ECAP9.DMA_INT |

### 3.13.2.71 CONTROLSS\_DMAXBAR10\_GSEL Register

#### 1 CONTROLSS\_DMAXBAR10\_GSEL Register (Offset = 380h) [reset = 0h]

Group Select register to select between G0-G5.

Return to [Summary Table](#)

**Table 3-2071. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6380h       |

**Figure 3-668. CONTROLSS\_DMAXBAR10\_GSEL Name Register**

|          |    |    |    |                     |    |    |    |
|----------|----|----|----|---------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED |    |    |    |                     |    |    |    |
| NONE     |    |    |    |                     |    |    |    |
| 0h       |    |    |    |                     |    |    |    |
| 23       | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED |    |    |    |                     |    |    |    |
| NONE     |    |    |    |                     |    |    |    |
| 0h       |    |    |    |                     |    |    |    |
| 15       | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| RESERVED |    |    |    |                     |    |    |    |
| NONE     |    |    |    |                     |    |    |    |
| 0h       |    |    |    |                     |    |    |    |
| 7        | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR10_GSEL_GSEL |    |    |    |
| NONE     |    |    |    | R/W                 |    |    |    |
| 0h       |    |    |    | 0h                  |    |    |    |

**Table 3-2073. CONTROLSS\_DMAXBAR10\_GSEL Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                  |
|------|---------------------|------|-------|--------------------------------------------------------------|
| 31:3 | RESERVED            | NONE | 0h    | Reserved                                                     |
| 2:0  | DMAXBAR10_GSEL_GSEL | R/W  | 0h    | Select input source:<br>0:G0 selected<br>..<br>5:G5 selected |

### 3.13.2.72 CONTROLSS\_DMAXBAR10\_G0 Register

#### 1 CONTROLSS\_DMAXBAR10\_G0 Register (Offset = 384h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2074. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6384h       |

**Figure 3-669. CONTROLSS\_DMAXBAR10\_G0 Name Register**

|          |    |    |                  |    |    |    |    |
|----------|----|----|------------------|----|----|----|----|
| 31       | 30 | 29 | 28               | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 23       | 22 | 21 | 20               | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 15       | 14 | 13 | 12               | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 7        | 6  | 5  | 4                | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR10_G0_SEL |    |    |    |    |
| NONE     |    |    | R/W              |    |    |    |    |
| 0h       |    |    | 0h               |    |    |    |    |

**Table 3-2076. CONTROLSS\_DMAXBAR10\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                              |
|------|------------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED         | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR10_G0_SEL | R/W  | 0h    | EPWM SOCA to corresponding XBAR<br>1:PWMx.SOCA is selected<br>0:PWMx.SOCA is de-selected |



### 3.13.2.73 CONTROLSS\_DMAXBAR10\_G1 Register

#### 1 CONTROLSS\_DMAXBAR10\_G1 Register (Offset = 388h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2077. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6388h       |

**Figure 3-670. CONTROLSS\_DMAXBAR10\_G1 Name Register**

|          |    |    |                  |    |    |    |    |
|----------|----|----|------------------|----|----|----|----|
| 31       | 30 | 29 | 28               | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 23       | 22 | 21 | 20               | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 15       | 14 | 13 | 12               | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 7        | 6  | 5  | 4                | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR10_G1_SEL |    |    |    |    |
| NONE     |    |    | R/W              |    |    |    |    |
| 0h       |    |    | 0h               |    |    |    |    |

**Table 3-2079. CONTROLSS\_DMAXBAR10\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                              |
|------|------------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED         | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR10_G1_SEL | R/W  | 0h    | EPWM SOCB to corresponding XBAR<br>1:PWMx.SOCB is selected<br>0:PWMx.SOCB is de-selected |

### 3.13.2.74 CONTROLSS\_DMAXBAR10\_G2 Register

#### 1 CONTROLSS\_DMAXBAR10\_G2 Register (Offset = 38Ch) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2080. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 638Ch       |

**Figure 3-671. CONTROLSS\_DMAXBAR10\_G2 Name Register**

|          |    |    |                  |    |    |    |    |
|----------|----|----|------------------|----|----|----|----|
| 31       | 30 | 29 | 28               | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 23       | 22 | 21 | 20               | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 15       | 14 | 13 | 12               | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 7        | 6  | 5  | 4                | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR10_G2_SEL |    |    |    |    |
| NONE     |    |    | R/W              |    |    |    |    |
| 0h       |    |    | 0h               |    |    |    |    |

**Table 3-2082. CONTROLSS\_DMAXBAR10\_G2 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:5 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-2082. CONTROLSS\_DMAXBAR10\_G2 Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | DMAXBAR10_G2_SEL | R/W  | 0h    | ADC DMA requests to corresponding XBAR<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.13.2.75 CONTROLSS\_DMAXBAR10\_G3 Register

#### 1 CONTROLSS\_DMAXBAR10\_G3 Register (Offset = 390h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2083. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6390h       |

**Figure 3-672. CONTROLSS\_DMAXBAR10\_G3 Name Register**

|          |    |    |    |                  |    |    |    |
|----------|----|----|----|------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 23       | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 15       | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 7        | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR10_G3_SEL |    |    |    |
| NONE     |    |    |    | R/W              |    |    |    |
| 0h       |    |    |    | 0h               |    |    |    |

**Table 3-2085. CONTROLSS\_DMAXBAR10\_G3 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                         |
| 3:0  | DMAXBAR10_G3_SEL | R/W  | 0h    | FSI DMA requests to corresponding XBAR<br>0:FSIRX0.RX_DMA_EVT<br>1: FSIRX0_DMATRIG1<br>2:FSIRX0_DMATRIG2<br>3:FSIRX1.RX_DMA_EVT<br>4: FSIRX1_DMATRIG1<br>5:FSIRX1_DMATRIG2<br>6:FSIRX2.RX_DMA_EVT<br>7: FSIRX2_DMATRIG1<br>8:FSIRX2_DMATRIG2<br>9:FSIRX3.RX_DMA_EVT<br>10: FSIRX3_DMATRIG1<br>11:FSIRX3_DMATRIG2<br>12:FSITX0.TX_DMA_EVT<br>13:FSITX1.TX_DMA_EVT<br>14:FSITX2.TX_DMA_EVT<br>15:FSITX3.TX_DMA_EVT |

### 3.13.2.76 CONTROLSS\_DMAXBAR10\_G4 Register

#### 1 CONTROLSS\_DMAXBAR10\_G4 Register (Offset = 394h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2086. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6394h       |

**Figure 3-673. CONTROLSS\_DMAXBAR10\_G4 Name Register**

|          |    |    |    |    |                  |    |    |
|----------|----|----|----|----|------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26               | 25 | 24 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18               | 17 | 16 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10               | 9  | 8  |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                | 1  | 0  |
| RESERVED |    |    |    |    | DMAXBAR10_G4_SEL |    |    |
| NONE     |    |    |    |    | R/W              |    |    |
| 0h       |    |    |    |    | 0h               |    |    |

**Table 3-2088. CONTROLSS\_DMAXBAR10\_G4 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                     |
|------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                        |
| 2:0  | DMAXBAR10_G4_SEL | R/W  | 0h    | SDFM DMA requests to corresponding XBAR<br>0:SD0.FILT1.DRINT<br>1:SD0.FILT2.DRINT<br>2:SD0.FILT3.DRINT<br>3:SD0.FILT4.DRINT<br>4:SD1.FILT1.DRINT<br>5:SD1.FILT2.DRINT<br>6:SD1.FILT3.DRINT<br>7:SD1.FILT4.DRINT |

### 3.13.2.77 CONTROLSS\_DMAXBAR10\_G5 Register

#### 1 CONTROLSS\_DMAXBAR10\_G5 Register (Offset = 398h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2089. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6398h       |

**Figure 3-674. CONTROLSS\_DMAXBAR10\_G5 Name Register**

|          |    |    |    |                  |    |    |    |
|----------|----|----|----|------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 23       | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 15       | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 7        | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR10_G5_SEL |    |    |    |
| NONE     |    |    |    | R/W              |    |    |    |
| 0h       |    |    |    | 0h               |    |    |    |

**Table 3-2091. CONTROLSS\_DMAXBAR10\_G5 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                           |
|------|------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                              |
| 3:0  | DMAXBAR10_G5_SEL | R/W  | 0h    | ECAP DMA requests to corresponding XBAR<br>0:ECAP0.DMA_INT<br>1:ECAP1.DMA_INT<br>2:ECAP2.DMA_INT<br>3:ECAP3.DMA_INT<br>4:ECAP4.DMA_INT<br>5:ECAP5.DMA_INT<br>6:ECAP6.DMA_INT<br>7:ECAP7.DMA_INT<br>8:ECAP8.DMA_INT<br>9:ECAP9.DMA_INT |

### 3.13.2.78 CONTROLSS\_DMAXBAR11\_GSEL Register

#### 1 CONTROLSS\_DMAXBAR11\_GSEL Register (Offset = 3C0h) [reset = 0h]

Group Select register to select between G0-G5.

Return to [Summary Table](#)

**Table 3-2092. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 63C0h       |

**Figure 3-675. CONTROLSS\_DMAXBAR11\_GSEL Name Register**

|          |    |    |    |    |                     |    |    |
|----------|----|----|----|----|---------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                  | 25 | 24 |
| RESERVED |    |    |    |    |                     |    |    |
| NONE     |    |    |    |    |                     |    |    |
| 0h       |    |    |    |    |                     |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                  | 17 | 16 |
| RESERVED |    |    |    |    |                     |    |    |
| NONE     |    |    |    |    |                     |    |    |
| 0h       |    |    |    |    |                     |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                  | 9  | 8  |
| RESERVED |    |    |    |    |                     |    |    |
| NONE     |    |    |    |    |                     |    |    |
| 0h       |    |    |    |    |                     |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                   | 1  | 0  |
| RESERVED |    |    |    |    | DMAXBAR11_GSEL_GSEL |    |    |
| NONE     |    |    |    |    | R/W                 |    |    |
| 0h       |    |    |    |    | 0h                  |    |    |

**Table 3-2094. CONTROLSS\_DMAXBAR11\_GSEL Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                  |
|------|---------------------|------|-------|--------------------------------------------------------------|
| 31:3 | RESERVED            | NONE | 0h    | Reserved                                                     |
| 2:0  | DMAXBAR11_GSEL_GSEL | R/W  | 0h    | Select input source:<br>0:G0 selected<br>..<br>5:G5 selected |

### 3.13.2.79 CONTROLSS\_DMAXBAR11\_G0 Register

#### 1 CONTROLSS\_DMAXBAR11\_G0 Register (Offset = 3C4h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2095. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 63C4h       |

**Figure 3-676. CONTROLSS\_DMAXBAR11\_G0 Name Register**

|          |    |    |                  |    |    |    |    |
|----------|----|----|------------------|----|----|----|----|
| 31       | 30 | 29 | 28               | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 23       | 22 | 21 | 20               | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 15       | 14 | 13 | 12               | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 7        | 6  | 5  | 4                | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR11_G0_SEL |    |    |    |    |
| NONE     |    |    | R/W              |    |    |    |    |
| 0h       |    |    | 0h               |    |    |    |    |

**Table 3-2097. CONTROLSS\_DMAXBAR11\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                              |
|------|------------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED         | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR11_G0_SEL | R/W  | 0h    | EPWM SOCA to corresponding XBAR<br>1:PWMx.SOCA is selected<br>0:PWMx.SOCA is de-selected |



### 3.13.2.80 CONTROLSS\_DMAXBAR11\_G1 Register

#### 1 CONTROLSS\_DMAXBAR11\_G1 Register (Offset = 3C8h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2098. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 63C8h       |

**Figure 3-677. CONTROLSS\_DMAXBAR11\_G1 Name Register**

|          |    |    |                  |    |    |    |    |
|----------|----|----|------------------|----|----|----|----|
| 31       | 30 | 29 | 28               | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 23       | 22 | 21 | 20               | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 15       | 14 | 13 | 12               | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 7        | 6  | 5  | 4                | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR11_G1_SEL |    |    |    |    |
| NONE     |    |    | R/W              |    |    |    |    |
| 0h       |    |    | 0h               |    |    |    |    |

**Table 3-2100. CONTROLSS\_DMAXBAR11\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                              |
|------|------------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED         | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR11_G1_SEL | R/W  | 0h    | EPWM SOCB to corresponding XBAR<br>1:PWMx.SOCB is selected<br>0:PWMx.SOCB is de-selected |

### 3.13.2.81 CONTROLSS\_DMAXBAR11\_G2 Register

#### 1 CONTROLSS\_DMAXBAR11\_G2 Register (Offset = 3CCh) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2101. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 63CCh       |

**Figure 3-678. CONTROLSS\_DMAXBAR11\_G2 Name Register**

|          |    |    |                  |    |    |    |    |
|----------|----|----|------------------|----|----|----|----|
| 31       | 30 | 29 | 28               | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 23       | 22 | 21 | 20               | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 15       | 14 | 13 | 12               | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 7        | 6  | 5  | 4                | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR11_G2_SEL |    |    |    |    |
| NONE     |    |    | R/W              |    |    |    |    |
| 0h       |    |    | 0h               |    |    |    |    |

**Table 3-2103. CONTROLSS\_DMAXBAR11\_G2 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:5 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-2103. CONTROLSS\_DMAXBAR11\_G2 Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | DMAXBAR11_G2_SEL | R/W  | 0h    | ADC DMA requests to corresponding XBAR<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.13.2.82 CONTROLSS\_DMAXBAR11\_G3 Register

#### 1 CONTROLSS\_DMAXBAR11\_G3 Register (Offset = 3D0h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2104. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 63D0h       |

**Figure 3-679. CONTROLSS\_DMAXBAR11\_G3 Name Register**

|          |    |    |    |                  |    |    |    |
|----------|----|----|----|------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 23       | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 15       | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 7        | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR11_G3_SEL |    |    |    |
| NONE     |    |    |    | R/W              |    |    |    |
| 0h       |    |    |    | 0h               |    |    |    |

**Table 3-2106. CONTROLSS\_DMAXBAR11\_G3 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                         |
| 3:0  | DMAXBAR11_G3_SEL | R/W  | 0h    | FSI DMA requests to corresponding XBAR<br>0:FSIRX0.RX_DMA_EVT<br>1; FSIRX0_DMATRIG1<br>2:FSIRX0_DMATRIG2<br>3:FSIRX1.RX_DMA_EVT<br>4; FSIRX1_DMATRIG1<br>5:FSIRX1_DMATRIG2<br>6:FSIRX2.RX_DMA_EVT<br>7; FSIRX2_DMATRIG1<br>8:FSIRX2_DMATRIG2<br>9:FSIRX3.RX_DMA_EVT<br>10; FSIRX3_DMATRIG1<br>11:FSIRX3_DMATRIG2<br>12:FSITX0.TX_DMA_EVT<br>13:FSITX1.TX_DMA_EVT<br>14:FSITX2.TX_DMA_EVT<br>15:FSITX3.TX_DMA_EVT |

### 3.13.2.83 CONTROLSS\_DMAXBAR11\_G4 Register

#### 1 CONTROLSS\_DMAXBAR11\_G4 Register (Offset = 3D4h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2107. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 63D4h       |

**Figure 3-680. CONTROLSS\_DMAXBAR11\_G4 Name Register**

|          |    |    |    |    |                  |    |    |
|----------|----|----|----|----|------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26               | 25 | 24 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18               | 17 | 16 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10               | 9  | 8  |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                | 1  | 0  |
| RESERVED |    |    |    |    | DMAXBAR11_G4_SEL |    |    |
| NONE     |    |    |    |    | R/W              |    |    |
| 0h       |    |    |    |    | 0h               |    |    |

**Table 3-2109. CONTROLSS\_DMAXBAR11\_G4 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                     |
|------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                        |
| 2:0  | DMAXBAR11_G4_SEL | R/W  | 0h    | SDFM DMA requests to corresponding XBAR<br>0:SD0.FILT1.DRINT<br>1:SD0.FILT2.DRINT<br>2:SD0.FILT3.DRINT<br>3:SD0.FILT4.DRINT<br>4:SD1.FILT1.DRINT<br>5:SD1.FILT2.DRINT<br>6:SD1.FILT3.DRINT<br>7:SD1.FILT4.DRINT |

### 3.13.2.84 CONTROLSS\_DMAXBAR11\_G5 Register

#### 1 CONTROLSS\_DMAXBAR11\_G5 Register (Offset = 3D8h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2110. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 63D8h       |

**Figure 3-681. CONTROLSS\_DMAXBAR11\_G5 Name Register**

|          |    |    |    |                  |    |    |    |
|----------|----|----|----|------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 23       | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 15       | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 7        | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR11_G5_SEL |    |    |    |
| NONE     |    |    |    | R/W              |    |    |    |
| 0h       |    |    |    | 0h               |    |    |    |

**Table 3-2112. CONTROLSS\_DMAXBAR11\_G5 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                           |
|------|------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                              |
| 3:0  | DMAXBAR11_G5_SEL | R/W  | 0h    | ECAP DMA requests to corresponding XBAR<br>0:ECAP0.DMA_INT<br>1:ECAP1.DMA_INT<br>2:ECAP2.DMA_INT<br>3:ECAP3.DMA_INT<br>4:ECAP4.DMA_INT<br>5:ECAP5.DMA_INT<br>6:ECAP6.DMA_INT<br>7:ECAP7.DMA_INT<br>8:ECAP8.DMA_INT<br>9:ECAP9.DMA_INT |

### 3.13.2.85 CONTROLSS\_DMAXBAR12\_GSEL Register

#### 1 CONTROLSS\_DMAXBAR12\_GSEL Register (Offset = 400h) [reset = 0h]

Group Select register to select between G0-G5.

Return to [Summary Table](#)

**Table 3-2113. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6400h       |

**Figure 3-682. CONTROLSS\_DMAXBAR12\_GSEL Name Register**

|          |    |    |    |                     |    |    |    |
|----------|----|----|----|---------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED |    |    |    |                     |    |    |    |
| NONE     |    |    |    |                     |    |    |    |
| 0h       |    |    |    |                     |    |    |    |
| 23       | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED |    |    |    |                     |    |    |    |
| NONE     |    |    |    |                     |    |    |    |
| 0h       |    |    |    |                     |    |    |    |
| 15       | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| RESERVED |    |    |    |                     |    |    |    |
| NONE     |    |    |    |                     |    |    |    |
| 0h       |    |    |    |                     |    |    |    |
| 7        | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR12_GSEL_GSEL |    |    |    |
| NONE     |    |    |    | R/W                 |    |    |    |
| 0h       |    |    |    | 0h                  |    |    |    |

**Table 3-2115. CONTROLSS\_DMAXBAR12\_GSEL Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                  |
|------|---------------------|------|-------|--------------------------------------------------------------|
| 31:3 | RESERVED            | NONE | 0h    | Reserved                                                     |
| 2:0  | DMAXBAR12_GSEL_GSEL | R/W  | 0h    | Select input source:<br>0:G0 selected<br>..<br>5:G5 selected |

### 3.13.2.86 CONTROLSS\_DMAXBAR12\_G0 Register

#### 1 CONTROLSS\_DMAXBAR12\_G0 Register (Offset = 404h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2116. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6404h       |

**Figure 3-683. CONTROLSS\_DMAXBAR12\_G0 Name Register**

|          |    |    |                  |    |    |    |    |
|----------|----|----|------------------|----|----|----|----|
| 31       | 30 | 29 | 28               | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 23       | 22 | 21 | 20               | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 15       | 14 | 13 | 12               | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 7        | 6  | 5  | 4                | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR12_G0_SEL |    |    |    |    |
| NONE     |    |    | R/W              |    |    |    |    |
| 0h       |    |    | 0h               |    |    |    |    |

**Table 3-2118. CONTROLSS\_DMAXBAR12\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                              |
|------|------------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED         | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR12_G0_SEL | R/W  | 0h    | EPWM SOCA to corresponding XBAR<br>1:PWMx.SOCA is selected<br>0:PWMx.SOCA is de-selected |



### 3.13.2.87 CONTROLSS\_DMAXBAR12\_G1 Register

#### 1 CONTROLSS\_DMAXBAR12\_G1 Register (Offset = 408h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2119. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6408h       |

**Figure 3-684. CONTROLSS\_DMAXBAR12\_G1 Name Register**

|          |    |    |    |                  |    |    |    |
|----------|----|----|----|------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 23       | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 15       | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 7        | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR12_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W              |    |    |    |
| 0h       |    |    |    | 0h               |    |    |    |

**Table 3-2121. CONTROLSS\_DMAXBAR12\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                              |
|------|------------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED         | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR12_G1_SEL | R/W  | 0h    | EPWM SOCB to corresponding XBAR<br>1:PWMx.SOCB is selected<br>0:PWMx.SOCB is de-selected |

### 3.13.2.88 CONTROLSS\_DMAXBAR12\_G2 Register

#### 1 CONTROLSS\_DMAXBAR12\_G2 Register (Offset = 40Ch) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2122. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 640Ch       |

**Figure 3-685. CONTROLSS\_DMAXBAR12\_G2 Name Register**

|          |    |    |                  |    |    |    |    |
|----------|----|----|------------------|----|----|----|----|
| 31       | 30 | 29 | 28               | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 23       | 22 | 21 | 20               | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 15       | 14 | 13 | 12               | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 7        | 6  | 5  | 4                | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR12_G2_SEL |    |    |    |    |
| NONE     |    |    | R/W              |    |    |    |    |
| 0h       |    |    | 0h               |    |    |    |    |

**Table 3-2124. CONTROLSS\_DMAXBAR12\_G2 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:5 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-2124. CONTROLSS\_DMAXBAR12\_G2 Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | DMAXBAR12_G2_SEL | R/W  | 0h    | ADC DMA requests to corresponding XBAR<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.13.2.89 CONTROLSS\_DMAXBAR12\_G3 Register

#### 1 CONTROLSS\_DMAXBAR12\_G3 Register (Offset = 410h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2125. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6410h       |

**Figure 3-686. CONTROLSS\_DMAXBAR12\_G3 Name Register**

|          |    |    |    |                  |    |    |    |
|----------|----|----|----|------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 23       | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 15       | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 7        | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR12_G3_SEL |    |    |    |
| NONE     |    |    |    | R/W              |    |    |    |
| 0h       |    |    |    | 0h               |    |    |    |

**Table 3-2127. CONTROLSS\_DMAXBAR12\_G3 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                         |
| 3:0  | DMAXBAR12_G3_SEL | R/W  | 0h    | FSI DMA requests to corresponding XBAR<br>0:FSIRX0.RX_DMA_EVT<br>1; FSIRX0_DMATRIG1<br>2:FSIRX0_DMATRIG2<br>3:FSIRX1.RX_DMA_EVT<br>4; FSIRX1_DMATRIG1<br>5:FSIRX1_DMATRIG2<br>6:FSIRX2.RX_DMA_EVT<br>7; FSIRX2_DMATRIG1<br>8:FSIRX2_DMATRIG2<br>9:FSIRX3.RX_DMA_EVT<br>10; FSIRX3_DMATRIG1<br>11:FSIRX3_DMATRIG2<br>12:FSITX0.TX_DMA_EVT<br>13:FSITX1.TX_DMA_EVT<br>14:FSITX2.TX_DMA_EVT<br>15:FSITX3.TX_DMA_EVT |

### 3.13.2.90 CONTROLSS\_DMAXBAR12\_G4 Register

#### 1 CONTROLSS\_DMAXBAR12\_G4 Register (Offset = 414h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2128. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6414h       |

**Figure 3-687. CONTROLSS\_DMAXBAR12\_G4 Name Register**

|          |    |    |    |    |                  |    |    |
|----------|----|----|----|----|------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26               | 25 | 24 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18               | 17 | 16 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10               | 9  | 8  |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                | 1  | 0  |
| RESERVED |    |    |    |    | DMAXBAR12_G4_SEL |    |    |
| NONE     |    |    |    |    | R/W              |    |    |
| 0h       |    |    |    |    | 0h               |    |    |

**Table 3-2130. CONTROLSS\_DMAXBAR12\_G4 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                     |
|------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                        |
| 2:0  | DMAXBAR12_G4_SEL | R/W  | 0h    | SDFM DMA requests to corresponding XBAR<br>0:SD0.FILT1.DRINT<br>1:SD0.FILT2.DRINT<br>2:SD0.FILT3.DRINT<br>3:SD0.FILT4.DRINT<br>4:SD1.FILT1.DRINT<br>5:SD1.FILT2.DRINT<br>6:SD1.FILT3.DRINT<br>7:SD1.FILT4.DRINT |

### 3.13.2.91 CONTROLSS\_DMAXBAR12\_G5 Register

#### 1 CONTROLSS\_DMAXBAR12\_G5 Register (Offset = 418h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2131. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6418h       |

**Figure 3-688. CONTROLSS\_DMAXBAR12\_G5 Name Register**

|          |    |    |    |                  |    |    |    |
|----------|----|----|----|------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 23       | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 15       | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 7        | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR12_G5_SEL |    |    |    |
| NONE     |    |    |    | R/W              |    |    |    |
| 0h       |    |    |    | 0h               |    |    |    |

**Table 3-2133. CONTROLSS\_DMAXBAR12\_G5 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                           |
|------|------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                              |
| 3:0  | DMAXBAR12_G5_SEL | R/W  | 0h    | ECAP DMA requests to corresponding XBAR<br>0:ECAP0.DMA_INT<br>1:ECAP1.DMA_INT<br>2:ECAP2.DMA_INT<br>3:ECAP3.DMA_INT<br>4:ECAP4.DMA_INT<br>5:ECAP5.DMA_INT<br>6:ECAP6.DMA_INT<br>7:ECAP7.DMA_INT<br>8:ECAP8.DMA_INT<br>9:ECAP9.DMA_INT |

### 3.13.2.92 CONTROLSS\_DMAXBAR13\_GSEL Register

#### 1 CONTROLSS\_DMAXBAR13\_GSEL Register (Offset = 440h) [reset = 0h]

Group Select register to select between G0-G5.

Return to [Summary Table](#)

**Table 3-2134. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6440h       |

**Figure 3-689. CONTROLSS\_DMAXBAR13\_GSEL Name Register**

|          |    |    |    |    |                     |    |    |
|----------|----|----|----|----|---------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                  | 25 | 24 |
| RESERVED |    |    |    |    |                     |    |    |
| NONE     |    |    |    |    |                     |    |    |
| 0h       |    |    |    |    |                     |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                  | 17 | 16 |
| RESERVED |    |    |    |    |                     |    |    |
| NONE     |    |    |    |    |                     |    |    |
| 0h       |    |    |    |    |                     |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                  | 9  | 8  |
| RESERVED |    |    |    |    |                     |    |    |
| NONE     |    |    |    |    |                     |    |    |
| 0h       |    |    |    |    |                     |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                   | 1  | 0  |
| RESERVED |    |    |    |    | DMAXBAR13_GSEL_GSEL |    |    |
| NONE     |    |    |    |    | R/W                 |    |    |
| 0h       |    |    |    |    | 0h                  |    |    |

**Table 3-2136. CONTROLSS\_DMAXBAR13\_GSEL Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                  |
|------|---------------------|------|-------|--------------------------------------------------------------|
| 31:3 | RESERVED            | NONE | 0h    | Reserved                                                     |
| 2:0  | DMAXBAR13_GSEL_GSEL | R/W  | 0h    | Select input source:<br>0:G0 selected<br>..<br>5:G5 selected |

### 3.13.2.93 CONTROLSS\_DMAXBAR13\_G0 Register

#### 1 CONTROLSS\_DMAXBAR13\_G0 Register (Offset = 444h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2137. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6444h       |

**Figure 3-690. CONTROLSS\_DMAXBAR13\_G0 Name Register**

|          |    |    |                  |    |    |    |    |
|----------|----|----|------------------|----|----|----|----|
| 31       | 30 | 29 | 28               | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 23       | 22 | 21 | 20               | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 15       | 14 | 13 | 12               | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 7        | 6  | 5  | 4                | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR13_G0_SEL |    |    |    |    |
| NONE     |    |    | R/W              |    |    |    |    |
| 0h       |    |    | 0h               |    |    |    |    |

**Table 3-2139. CONTROLSS\_DMAXBAR13\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                              |
|------|------------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED         | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR13_G0_SEL | R/W  | 0h    | EPWM SOCA to corresponding XBAR<br>1:PWMx.SOCA is selected<br>0:PWMx.SOCA is de-selected |



### 3.13.2.94 CONTROLSS\_DMAXBAR13\_G1 Register

#### 1 CONTROLSS\_DMAXBAR13\_G1 Register (Offset = 448h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2140. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6448h       |

**Figure 3-691. CONTROLSS\_DMAXBAR13\_G1 Name Register**

|          |    |    |                  |    |    |    |    |
|----------|----|----|------------------|----|----|----|----|
| 31       | 30 | 29 | 28               | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 23       | 22 | 21 | 20               | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 15       | 14 | 13 | 12               | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 7        | 6  | 5  | 4                | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR13_G1_SEL |    |    |    |    |
| NONE     |    |    | R/W              |    |    |    |    |
| 0h       |    |    | 0h               |    |    |    |    |

**Table 3-2142. CONTROLSS\_DMAXBAR13\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                              |
|------|------------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED         | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR13_G1_SEL | R/W  | 0h    | EPWM SOCB to corresponding XBAR<br>1:PWMx.SOCB is selected<br>0:PWMx.SOCB is de-selected |

### 3.13.2.95 CONTROLSS\_DMAXBAR13\_G2 Register

#### 1 CONTROLSS\_DMAXBAR13\_G2 Register (Offset = 44Ch) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2143. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 644Ch       |

**Figure 3-692. CONTROLSS\_DMAXBAR13\_G2 Name Register**

|          |    |    |                  |    |    |    |    |
|----------|----|----|------------------|----|----|----|----|
| 31       | 30 | 29 | 28               | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 23       | 22 | 21 | 20               | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 15       | 14 | 13 | 12               | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 7        | 6  | 5  | 4                | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR13_G2_SEL |    |    |    |    |
| NONE     |    |    | R/W              |    |    |    |    |
| 0h       |    |    | 0h               |    |    |    |    |

**Table 3-2145. CONTROLSS\_DMAXBAR13\_G2 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:5 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-2145. CONTROLSS\_DMAXBAR13\_G2 Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | DMAXBAR13_G2_SEL | R/W  | 0h    | ADC DMA requests to corresponding XBAR<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.13.2.96 CONTROLSS\_DMAXBAR13\_G3 Register

#### 1 CONTROLSS\_DMAXBAR13\_G3 Register (Offset = 450h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2146. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6450h       |

**Figure 3-693. CONTROLSS\_DMAXBAR13\_G3 Name Register**

|          |    |    |    |                  |    |    |    |
|----------|----|----|----|------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 23       | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 15       | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 7        | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR13_G3_SEL |    |    |    |
| NONE     |    |    |    | R/W              |    |    |    |
| 0h       |    |    |    | 0h               |    |    |    |

**Table 3-2148. CONTROLSS\_DMAXBAR13\_G3 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                         |
| 3:0  | DMAXBAR13_G3_SEL | R/W  | 0h    | FSI DMA requests to corresponding XBAR<br>0:FSIRX0.RX_DMA_EVT<br>1; FSIRX0_DMATRIG1<br>2:FSIRX0_DMATRIG2<br>3:FSIRX1.RX_DMA_EVT<br>4; FSIRX1_DMATRIG1<br>5:FSIRX1_DMATRIG2<br>6:FSIRX2.RX_DMA_EVT<br>7; FSIRX2_DMATRIG1<br>8:FSIRX2_DMATRIG2<br>9:FSIRX3.RX_DMA_EVT<br>10; FSIRX3_DMATRIG1<br>11:FSIRX3_DMATRIG2<br>12:FSITX0.TX_DMA_EVT<br>13:FSITX1.TX_DMA_EVT<br>14:FSITX2.TX_DMA_EVT<br>15:FSITX3.TX_DMA_EVT |

### 3.13.2.97 CONTROLSS\_DMAXBAR13\_G4 Register

#### 1 CONTROLSS\_DMAXBAR13\_G4 Register (Offset = 454h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2149. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6454h       |

**Figure 3-694. CONTROLSS\_DMAXBAR13\_G4 Name Register**

|          |    |    |    |    |                  |    |    |
|----------|----|----|----|----|------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26               | 25 | 24 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18               | 17 | 16 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10               | 9  | 8  |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                | 1  | 0  |
| RESERVED |    |    |    |    | DMAXBAR13_G4_SEL |    |    |
| NONE     |    |    |    |    | R/W              |    |    |
| 0h       |    |    |    |    | 0h               |    |    |

**Table 3-2151. CONTROLSS\_DMAXBAR13\_G4 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                     |
|------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                        |
| 2:0  | DMAXBAR13_G4_SEL | R/W  | 0h    | SDFM DMA requests to corresponding XBAR<br>0:SD0.FILT1.DRINT<br>1:SD0.FILT2.DRINT<br>2:SD0.FILT3.DRINT<br>3:SD0.FILT4.DRINT<br>4:SD1.FILT1.DRINT<br>5:SD1.FILT2.DRINT<br>6:SD1.FILT3.DRINT<br>7:SD1.FILT4.DRINT |

### 3.13.2.98 CONTROLSS\_DMAXBAR13\_G5 Register

#### 1 CONTROLSS\_DMAXBAR13\_G5 Register (Offset = 458h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2152. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6458h       |

**Figure 3-695. CONTROLSS\_DMAXBAR13\_G5 Name Register**

|          |    |    |    |                  |    |    |    |
|----------|----|----|----|------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 23       | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 15       | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 7        | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR13_G5_SEL |    |    |    |
| NONE     |    |    |    | R/W              |    |    |    |
| 0h       |    |    |    | 0h               |    |    |    |

**Table 3-2154. CONTROLSS\_DMAXBAR13\_G5 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                           |
|------|------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                              |
| 3:0  | DMAXBAR13_G5_SEL | R/W  | 0h    | ECAP DMA requests to corresponding XBAR<br>0:ECAP0.DMA_INT<br>1:ECAP1.DMA_INT<br>2:ECAP2.DMA_INT<br>3:ECAP3.DMA_INT<br>4:ECAP4.DMA_INT<br>5:ECAP5.DMA_INT<br>6:ECAP6.DMA_INT<br>7:ECAP7.DMA_INT<br>8:ECAP8.DMA_INT<br>9:ECAP9.DMA_INT |

### 3.13.2.99 CONTROLSS\_DMAXBAR14\_GSEL Register

#### 1 CONTROLSS\_DMAXBAR14\_GSEL Register (Offset = 480h) [reset = 0h]

Group Select register to select between G0-G5.

Return to [Summary Table](#)

**Table 3-2155. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6480h       |

**Figure 3-696. CONTROLSS\_DMAXBAR14\_GSEL Name Register**

|          |    |    |    |                     |    |    |    |
|----------|----|----|----|---------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED |    |    |    |                     |    |    |    |
| NONE     |    |    |    |                     |    |    |    |
| 0h       |    |    |    |                     |    |    |    |
| 23       | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED |    |    |    |                     |    |    |    |
| NONE     |    |    |    |                     |    |    |    |
| 0h       |    |    |    |                     |    |    |    |
| 15       | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| RESERVED |    |    |    |                     |    |    |    |
| NONE     |    |    |    |                     |    |    |    |
| 0h       |    |    |    |                     |    |    |    |
| 7        | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR14_GSEL_GSEL |    |    |    |
| NONE     |    |    |    | R/W                 |    |    |    |
| 0h       |    |    |    | 0h                  |    |    |    |

**Table 3-2157. CONTROLSS\_DMAXBAR14\_GSEL Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                  |
|------|---------------------|------|-------|--------------------------------------------------------------|
| 31:3 | RESERVED            | NONE | 0h    | Reserved                                                     |
| 2:0  | DMAXBAR14_GSEL_GSEL | R/W  | 0h    | Select input source:<br>0:G0 selected<br>..<br>5:G5 selected |

### 3.13.2.100 CONTROLSS\_DMAXBAR14\_G0 Register

#### 1 CONTROLSS\_DMAXBAR14\_G0 Register (Offset = 484h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2158. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6484h       |

**Figure 3-697. CONTROLSS\_DMAXBAR14\_G0 Name Register**

|          |    |    |                  |    |    |    |    |
|----------|----|----|------------------|----|----|----|----|
| 31       | 30 | 29 | 28               | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 23       | 22 | 21 | 20               | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 15       | 14 | 13 | 12               | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 7        | 6  | 5  | 4                | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR14_G0_SEL |    |    |    |    |
| NONE     |    |    | R/W              |    |    |    |    |
| 0h       |    |    | 0h               |    |    |    |    |

**Table 3-2160. CONTROLSS\_DMAXBAR14\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                              |
|------|------------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED         | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR14_G0_SEL | R/W  | 0h    | EPWM SOCA to corresponding XBAR<br>1:PWMx.SOCA is selected<br>0:PWMx.SOCA is de-selected |



### 3.13.2.101 CONTROLSS\_DMAXBAR14\_G1 Register

#### 1 CONTROLSS\_DMAXBAR14\_G1 Register (Offset = 488h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2161. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6488h       |

**Figure 3-698. CONTROLSS\_DMAXBAR14\_G1 Name Register**

|          |    |    |                  |    |    |    |    |
|----------|----|----|------------------|----|----|----|----|
| 31       | 30 | 29 | 28               | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 23       | 22 | 21 | 20               | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 15       | 14 | 13 | 12               | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 7        | 6  | 5  | 4                | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR14_G1_SEL |    |    |    |    |
| NONE     |    |    | R/W              |    |    |    |    |
| 0h       |    |    | 0h               |    |    |    |    |

**Table 3-2163. CONTROLSS\_DMAXBAR14\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                              |
|------|------------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED         | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR14_G1_SEL | R/W  | 0h    | EPWM SOCB to corresponding XBAR<br>1:PWMx.SOCB is selected<br>0:PWMx.SOCB is de-selected |

### 3.13.2.102 CONTROLSS\_DMAXBAR14\_G2 Register

#### 1 CONTROLSS\_DMAXBAR14\_G2 Register (Offset = 48Ch) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2164. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 648Ch       |

**Figure 3-699. CONTROLSS\_DMAXBAR14\_G2 Name Register**

|          |    |    |                  |    |    |    |    |
|----------|----|----|------------------|----|----|----|----|
| 31       | 30 | 29 | 28               | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 23       | 22 | 21 | 20               | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 15       | 14 | 13 | 12               | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 7        | 6  | 5  | 4                | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR14_G2_SEL |    |    |    |    |
| NONE     |    |    | R/W              |    |    |    |    |
| 0h       |    |    | 0h               |    |    |    |    |

**Table 3-2166. CONTROLSS\_DMAXBAR14\_G2 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:5 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-2166. CONTROLSS\_DMAXBAR14\_G2 Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | DMAXBAR14_G2_SEL | R/W  | 0h    | ADC DMA requests to corresponding XBAR<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.13.2.103 CONTROLSS\_DMAXBAR14\_G3 Register

#### 1 CONTROLSS\_DMAXBAR14\_G3 Register (Offset = 490h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2167. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6490h       |

**Figure 3-700. CONTROLSS\_DMAXBAR14\_G3 Name Register**

|          |    |    |    |                  |    |    |    |
|----------|----|----|----|------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 23       | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 15       | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 7        | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR14_G3_SEL |    |    |    |
| NONE     |    |    |    | R/W              |    |    |    |
| 0h       |    |    |    | 0h               |    |    |    |

**Table 3-2169. CONTROLSS\_DMAXBAR14\_G3 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                         |
| 3:0  | DMAXBAR14_G3_SEL | R/W  | 0h    | FSI DMA requests to corresponding XBAR<br>0:FSIRX0.RX_DMA_EVT<br>1; FSIRX0_DMATRIG1<br>2:FSIRX0_DMATRIG2<br>3:FSIRX1.RX_DMA_EVT<br>4; FSIRX1_DMATRIG1<br>5:FSIRX1_DMATRIG2<br>6:FSIRX2.RX_DMA_EVT<br>7; FSIRX2_DMATRIG1<br>8:FSIRX2_DMATRIG2<br>9:FSIRX3.RX_DMA_EVT<br>10; FSIRX3_DMATRIG1<br>11:FSIRX3_DMATRIG2<br>12:FSITX0.TX_DMA_EVT<br>13:FSITX1.TX_DMA_EVT<br>14:FSITX2.TX_DMA_EVT<br>15:FSITX3.TX_DMA_EVT |

### 3.13.2.104 CONTROLSS\_DMAXBAR14\_G4 Register

#### 1 CONTROLSS\_DMAXBAR14\_G4 Register (Offset = 494h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2170. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6494h       |

**Figure 3-701. CONTROLSS\_DMAXBAR14\_G4 Name Register**

|          |    |    |    |    |                  |    |    |
|----------|----|----|----|----|------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26               | 25 | 24 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18               | 17 | 16 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10               | 9  | 8  |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                | 1  | 0  |
| RESERVED |    |    |    |    | DMAXBAR14_G4_SEL |    |    |
| NONE     |    |    |    |    | R/W              |    |    |
| 0h       |    |    |    |    | 0h               |    |    |

**Table 3-2172. CONTROLSS\_DMAXBAR14\_G4 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                     |
|------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                        |
| 2:0  | DMAXBAR14_G4_SEL | R/W  | 0h    | SDFM DMA requests to corresponding XBAR<br>0:SD0.FILT1.DRINT<br>1:SD0.FILT2.DRINT<br>2:SD0.FILT3.DRINT<br>3:SD0.FILT4.DRINT<br>4:SD1.FILT1.DRINT<br>5:SD1.FILT2.DRINT<br>6:SD1.FILT3.DRINT<br>7:SD1.FILT4.DRINT |

### 3.13.2.105 CONTROLSS\_DMAXBAR14\_G5 Register

#### 1 CONTROLSS\_DMAXBAR14\_G5 Register (Offset = 498h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2173. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 6498h       |

**Figure 3-702. CONTROLSS\_DMAXBAR14\_G5 Name Register**

|          |    |    |    |                  |    |    |    |
|----------|----|----|----|------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 23       | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 15       | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 7        | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR14_G5_SEL |    |    |    |
| NONE     |    |    |    | R/W              |    |    |    |
| 0h       |    |    |    | 0h               |    |    |    |

**Table 3-2175. CONTROLSS\_DMAXBAR14\_G5 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                           |
|------|------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                              |
| 3:0  | DMAXBAR14_G5_SEL | R/W  | 0h    | ECAP DMA requests to corresponding XBAR<br>0:ECAP0.DMA_INT<br>1:ECAP1.DMA_INT<br>2:ECAP2.DMA_INT<br>3:ECAP3.DMA_INT<br>4:ECAP4.DMA_INT<br>5:ECAP5.DMA_INT<br>6:ECAP6.DMA_INT<br>7:ECAP7.DMA_INT<br>8:ECAP8.DMA_INT<br>9:ECAP9.DMA_INT |

### 3.13.2.106 CONTROLSS\_DMAXBAR15\_GSEL Register

#### 1 CONTROLSS\_DMAXBAR15\_GSEL Register (Offset = 4C0h) [reset = 0h]

Group Select register to select between G0-G5.

Return to [Summary Table](#)

**Table 3-2176. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 64C0h       |

**Figure 3-703. CONTROLSS\_DMAXBAR15\_GSEL Name Register**

|          |    |    |    |                     |    |    |    |
|----------|----|----|----|---------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED |    |    |    |                     |    |    |    |
| NONE     |    |    |    |                     |    |    |    |
| 0h       |    |    |    |                     |    |    |    |
| 23       | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED |    |    |    |                     |    |    |    |
| NONE     |    |    |    |                     |    |    |    |
| 0h       |    |    |    |                     |    |    |    |
| 15       | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| RESERVED |    |    |    |                     |    |    |    |
| NONE     |    |    |    |                     |    |    |    |
| 0h       |    |    |    |                     |    |    |    |
| 7        | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR15_GSEL_GSEL |    |    |    |
| NONE     |    |    |    | R/W                 |    |    |    |
| 0h       |    |    |    | 0h                  |    |    |    |

**Table 3-2178. CONTROLSS\_DMAXBAR15\_GSEL Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                  |
|------|---------------------|------|-------|--------------------------------------------------------------|
| 31:3 | RESERVED            | NONE | 0h    | Reserved                                                     |
| 2:0  | DMAXBAR15_GSEL_GSEL | R/W  | 0h    | Select input source:<br>0:G0 selected<br>..<br>5:G5 selected |

### 3.13.2.107 CONTROLSS\_DMAXBAR15\_G0 Register

#### 1 CONTROLSS\_DMAXBAR15\_G0 Register (Offset = 4C4h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2179. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 64C4h       |

**Figure 3-704. CONTROLSS\_DMAXBAR15\_G0 Name Register**

|          |    |    |                  |    |    |    |    |
|----------|----|----|------------------|----|----|----|----|
| 31       | 30 | 29 | 28               | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 23       | 22 | 21 | 20               | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 15       | 14 | 13 | 12               | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 7        | 6  | 5  | 4                | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR15_G0_SEL |    |    |    |    |
| NONE     |    |    | R/W              |    |    |    |    |
| 0h       |    |    | 0h               |    |    |    |    |

**Table 3-2181. CONTROLSS\_DMAXBAR15\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                              |
|------|------------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED         | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR15_G0_SEL | R/W  | 0h    | EPWM SOCA to corresponding XBAR<br>1:PWMx.SOCA is selected<br>0:PWMx.SOCA is de-selected |



### 3.13.2.108 CONTROLSS\_DMAXBAR15\_G1 Register

#### 1 CONTROLSS\_DMAXBAR15\_G1 Register (Offset = 4C8h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2182. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 64C8h       |

**Figure 3-705. CONTROLSS\_DMAXBAR15\_G1 Name Register**

|          |    |    |                  |    |    |    |    |
|----------|----|----|------------------|----|----|----|----|
| 31       | 30 | 29 | 28               | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 23       | 22 | 21 | 20               | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 15       | 14 | 13 | 12               | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 7        | 6  | 5  | 4                | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR15_G1_SEL |    |    |    |    |
| NONE     |    |    | R/W              |    |    |    |    |
| 0h       |    |    | 0h               |    |    |    |    |

**Table 3-2184. CONTROLSS\_DMAXBAR15\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                              |
|------|------------------|------|-------|------------------------------------------------------------------------------------------|
| 31:5 | RESERVED         | NONE | 0h    | Reserved                                                                                 |
| 4:0  | DMAXBAR15_G1_SEL | R/W  | 0h    | EPWM SOCB to corresponding XBAR<br>1:PWMx.SOCB is selected<br>0:PWMx.SOCB is de-selected |

### 3.13.2.109 CONTROLSS\_DMAXBAR15\_G2 Register

#### 1 CONTROLSS\_DMAXBAR15\_G2 Register (Offset = 4CCh) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2185. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 64CCh       |

**Figure 3-706. CONTROLSS\_DMAXBAR15\_G2 Name Register**

|          |    |    |                  |    |    |    |    |
|----------|----|----|------------------|----|----|----|----|
| 31       | 30 | 29 | 28               | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 23       | 22 | 21 | 20               | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 15       | 14 | 13 | 12               | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                  |    |    |    |    |
| NONE     |    |    |                  |    |    |    |    |
| 0h       |    |    |                  |    |    |    |    |
| 7        | 6  | 5  | 4                | 3  | 2  | 1  | 0  |
| RESERVED |    |    | DMAXBAR15_G2_SEL |    |    |    |    |
| NONE     |    |    | R/W              |    |    |    |    |
| 0h       |    |    | 0h               |    |    |    |    |

**Table 3-2187. CONTROLSS\_DMAXBAR15\_G2 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:5 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-2187. CONTROLSS\_DMAXBAR15\_G2 Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | DMAXBAR15_G2_SEL | R/W  | 0h    | ADC DMA requests to corresponding XBAR<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.13.2.110 CONTROLSS\_DMAXBAR15\_G3 Register

#### 1 CONTROLSS\_DMAXBAR15\_G3 Register (Offset = 4D0h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2188. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 64D0h       |

**Figure 3-707. CONTROLSS\_DMAXBAR15\_G3 Name Register**

|          |    |    |    |                  |    |    |    |
|----------|----|----|----|------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 23       | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 15       | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 7        | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR15_G3_SEL |    |    |    |
| NONE     |    |    |    | R/W              |    |    |    |
| 0h       |    |    |    | 0h               |    |    |    |

**Table 3-2190. CONTROLSS\_DMAXBAR15\_G3 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                         |
| 3:0  | DMAXBAR15_G3_SEL | R/W  | 0h    | FSI DMA requests to corresponding XBAR<br>0:FSIRX0.RX_DMA_EVT<br>1: FSIRX0_DMATRIG1<br>2:FSIRX0_DMATRIG2<br>3:FSIRX1.RX_DMA_EVT<br>4: FSIRX1_DMATRIG1<br>5:FSIRX1_DMATRIG2<br>6:FSIRX2.RX_DMA_EVT<br>7: FSIRX2_DMATRIG1<br>8:FSIRX2_DMATRIG2<br>9:FSIRX3.RX_DMA_EVT<br>10: FSIRX3_DMATRIG1<br>11:FSIRX3_DMATRIG2<br>12:FSITX0.TX_DMA_EVT<br>13:FSITX1.TX_DMA_EVT<br>14:FSITX2.TX_DMA_EVT<br>15:FSITX3.TX_DMA_EVT |

### 3.13.2.111 CONTROLSS\_DMAXBAR15\_G4 Register

#### 1 CONTROLSS\_DMAXBAR15\_G4 Register (Offset = 4D4h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2191. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 64D4h       |

**Figure 3-708. CONTROLSS\_DMAXBAR15\_G4 Name Register**

|          |    |    |    |    |                  |    |    |
|----------|----|----|----|----|------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26               | 25 | 24 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18               | 17 | 16 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10               | 9  | 8  |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                | 1  | 0  |
| RESERVED |    |    |    |    | DMAXBAR15_G4_SEL |    |    |
| NONE     |    |    |    |    | R/W              |    |    |
| 0h       |    |    |    |    | 0h               |    |    |

**Table 3-2193. CONTROLSS\_DMAXBAR15\_G4 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                     |
|------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                        |
| 2:0  | DMAXBAR15_G4_SEL | R/W  | 0h    | SDFM DMA requests to corresponding XBAR<br>0:SD0.FILT1.DRINT<br>1:SD0.FILT2.DRINT<br>2:SD0.FILT3.DRINT<br>3:SD0.FILT4.DRINT<br>4:SD1.FILT1.DRINT<br>5:SD1.FILT2.DRINT<br>6:SD1.FILT3.DRINT<br>7:SD1.FILT4.DRINT |

### 3.13.2.112 CONTROLSS\_DMAXBAR15\_G5 Register

#### 1 CONTROLSS\_DMAXBAR15\_G5 Register (Offset = 4D8h) [reset = 0h]

Event Select within corresponding group.

Return to [Summary Table](#)

**Table 3-2194. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_DMAXBAR | 502D 64D8h       |

**Figure 3-709. CONTROLSS\_DMAXBAR15\_G5 Name Register**

|          |    |    |    |                  |    |    |    |
|----------|----|----|----|------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 23       | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 15       | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 7        | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| RESERVED |    |    |    | DMAXBAR15_G5_SEL |    |    |    |
| NONE     |    |    |    | R/W              |    |    |    |
| 0h       |    |    |    | 0h               |    |    |    |

**Table 3-2196. CONTROLSS\_DMAXBAR15\_G5 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                           |
|------|------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                              |
| 3:0  | DMAXBAR15_G5_SEL | R/W  | 0h    | ECAP DMA requests to corresponding XBAR<br>0:ECAP0.DMA_INT<br>1:ECAP1.DMA_INT<br>2:ECAP2.DMA_INT<br>3:ECAP3.DMA_INT<br>4:ECAP4.DMA_INT<br>5:ECAP5.DMA_INT<br>6:ECAP6.DMA_INT<br>7:ECAP7.DMA_INT<br>8:ECAP8.DMA_INT<br>9:ECAP9.DMA_INT |

## 3.14 CONTROLSS\_ICLXBAR

### CONTROLSS\_ICLXBAR

#### 3.14.1 CONTROLSS\_ICLXBAR Summaries

#### CONTROLSS\_ICLXBAR Summaries

**Table 3-2197. CONTROLSS Registers, Base Address=502D 4000h, Length=1024**

| Offset | Length | Register Name                          | CONTROLSS_ICLXBAR Physical Address |
|--------|--------|----------------------------------------|------------------------------------|
| 100h   | 32     | <a href="#">CONTROLSS_ICLXBAR0_G0</a>  | 502D 4100h                         |
| 104h   | 32     | <a href="#">CONTROLSS_ICLXBAR0_G1</a>  | 502D 4104h                         |
| 108h   | 32     | <a href="#">CONTROLSS_ICLXBAR0_G2</a>  | 502D 4108h                         |
| 140h   | 32     | <a href="#">CONTROLSS_ICLXBAR1_G0</a>  | 502D 4140h                         |
| 144h   | 32     | <a href="#">CONTROLSS_ICLXBAR1_G1</a>  | 502D 4144h                         |
| 148h   | 32     | <a href="#">CONTROLSS_ICLXBAR1_G2</a>  | 502D 4148h                         |
| 180h   | 32     | <a href="#">CONTROLSS_ICLXBAR2_G0</a>  | 502D 4180h                         |
| 184h   | 32     | <a href="#">CONTROLSS_ICLXBAR2_G1</a>  | 502D 4184h                         |
| 188h   | 32     | <a href="#">CONTROLSS_ICLXBAR2_G2</a>  | 502D 4188h                         |
| 1C0h   | 32     | <a href="#">CONTROLSS_ICLXBAR3_G0</a>  | 502D 41C0h                         |
| 1C4h   | 32     | <a href="#">CONTROLSS_ICLXBAR3_G1</a>  | 502D 41C4h                         |
| 1C8h   | 32     | <a href="#">CONTROLSS_ICLXBAR3_G2</a>  | 502D 41C8h                         |
| 200h   | 32     | <a href="#">CONTROLSS_ICLXBAR4_G0</a>  | 502D 4200h                         |
| 204h   | 32     | <a href="#">CONTROLSS_ICLXBAR4_G1</a>  | 502D 4204h                         |
| 208h   | 32     | <a href="#">CONTROLSS_ICLXBAR4_G2</a>  | 502D 4208h                         |
| 240h   | 32     | <a href="#">CONTROLSS_ICLXBAR5_G0</a>  | 502D 4240h                         |
| 244h   | 32     | <a href="#">CONTROLSS_ICLXBAR5_G1</a>  | 502D 4244h                         |
| 248h   | 32     | <a href="#">CONTROLSS_ICLXBAR5_G2</a>  | 502D 4248h                         |
| 280h   | 32     | <a href="#">CONTROLSS_ICLXBAR6_G0</a>  | 502D 4280h                         |
| 284h   | 32     | <a href="#">CONTROLSS_ICLXBAR6_G1</a>  | 502D 4284h                         |
| 288h   | 32     | <a href="#">CONTROLSS_ICLXBAR6_G2</a>  | 502D 4288h                         |
| 2C0h   | 32     | <a href="#">CONTROLSS_ICLXBAR7_G0</a>  | 502D 42C0h                         |
| 2C4h   | 32     | <a href="#">CONTROLSS_ICLXBAR7_G1</a>  | 502D 42C4h                         |
| 2C8h   | 32     | <a href="#">CONTROLSS_ICLXBAR7_G2</a>  | 502D 42C8h                         |
| 300h   | 32     | <a href="#">CONTROLSS_ICLXBAR8_G0</a>  | 502D 4300h                         |
| 304h   | 32     | <a href="#">CONTROLSS_ICLXBAR8_G1</a>  | 502D 4304h                         |
| 308h   | 32     | <a href="#">CONTROLSS_ICLXBAR8_G2</a>  | 502D 4308h                         |
| 340h   | 32     | <a href="#">CONTROLSS_ICLXBAR9_G0</a>  | 502D 4340h                         |
| 344h   | 32     | <a href="#">CONTROLSS_ICLXBAR9_G1</a>  | 502D 4344h                         |
| 348h   | 32     | <a href="#">CONTROLSS_ICLXBAR9_G2</a>  | 502D 4348h                         |
| 380h   | 32     | <a href="#">CONTROLSS_ICLXBAR10_G0</a> | 502D 4380h                         |
| 384h   | 32     | <a href="#">CONTROLSS_ICLXBAR10_G1</a> | 502D 4384h                         |
| 388h   | 32     | <a href="#">CONTROLSS_ICLXBAR10_G2</a> | 502D 4388h                         |
| 3C0h   | 32     | <a href="#">CONTROLSS_ICLXBAR11_G0</a> | 502D 43C0h                         |
| 3C4h   | 32     | <a href="#">CONTROLSS_ICLXBAR11_G1</a> | 502D 43C4h                         |
| 3C8h   | 32     | <a href="#">CONTROLSS_ICLXBAR11_G2</a> | 502D 43C8h                         |
| 400h   | 32     | <a href="#">CONTROLSS_ICLXBAR12_G0</a> | 502D 4400h                         |

**Table 3-2197. CONTROLSS Registers, Base Address=502D 4000h, Length=1024 (continued)**

| Offset | Length | Register Name                          | CONTROLSS_ICLXBAR Physical Address |
|--------|--------|----------------------------------------|------------------------------------|
| 404h   | 32     | <a href="#">CONTROLSS_ICLXBAR12_G1</a> | 502D 4404h                         |
| 408h   | 32     | <a href="#">CONTROLSS_ICLXBAR12_G2</a> | 502D 4408h                         |
| 440h   | 32     | <a href="#">CONTROLSS_ICLXBAR13_G0</a> | 502D 4440h                         |
| 444h   | 32     | <a href="#">CONTROLSS_ICLXBAR13_G1</a> | 502D 4444h                         |
| 448h   | 32     | <a href="#">CONTROLSS_ICLXBAR13_G2</a> | 502D 4448h                         |
| 480h   | 32     | <a href="#">CONTROLSS_ICLXBAR14_G0</a> | 502D 4480h                         |
| 484h   | 32     | <a href="#">CONTROLSS_ICLXBAR14_G1</a> | 502D 4484h                         |
| 488h   | 32     | <a href="#">CONTROLSS_ICLXBAR14_G2</a> | 502D 4488h                         |
| 4C0h   | 32     | <a href="#">CONTROLSS_ICLXBAR15_G0</a> | 502D 44C0h                         |
| 4C4h   | 32     | <a href="#">CONTROLSS_ICLXBAR15_G1</a> | 502D 44C4h                         |
| 4C8h   | 32     | <a href="#">CONTROLSS_ICLXBAR15_G2</a> | 502D 44C8h                         |

### 3.14.2 CONTROLSS\_ICLXBAR Registers

#### CONTROLSS\_ICLXBAR Registers



### 3.14.2.1 CONTROLSS\_ICLXBAR0\_G0 Register

#### 1 CONTROLSS\_ICLXBAR0\_G0 Register (Offset = 100h) [reset = 0h]

ICL XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-2198. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4100h       |

**Figure 3-710. CONTROLSS\_ICLXBAR0\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR0_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR0_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR0_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR0_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2200. CONTROLSS\_ICLXBAR0\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR0_G0_SEL | R/W  | 0h    | ICL XBAR0 G0 input bit select. Input source is MDLx.OUTA select<br>1:MDLx.OUTA bit[x] selected<br>0:MDLx.OUTA bit[x] is de-selected |

### 3.14.2.2 CONTROLSS\_ICLXBAR0\_G1 Register

#### 1 CONTROLSS\_ICLXBAR0\_G1 Register (Offset = 104h) [reset = 0h]

ICL XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-2201. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4104h       |

**Figure 3-711. CONTROLSS\_ICLXBAR0\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR0_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR0_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR0_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR0_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2203. CONTROLSS\_ICLXBAR0\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR0_G1_SEL | R/W  | 0h    | ICL XBAR0 G1 input bit select. Input source is MDLx.OUTB select<br>1:MDLx.OUTB bit[x] selected<br>0:MDLx.OUTB bit[x] is de-selected |

### 3.14.2.3 CONTROLSS\_ICLXBAR0\_G2 Register

#### 1 CONTROLSS\_ICLXBAR0\_G2 Register (Offset = 108h) [reset = 0h]

ICL XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-2204. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4108h       |

**Figure 3-712. CONTROLSS\_ICLXBAR0\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR0_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR0_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR0_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR0_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2206. CONTROLSS\_ICLXBAR0\_G2 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR0_G2_SEL | R/W  | 0h    | ICL XBAR0 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

### 3.14.2.4 CONTROLSS\_ICLXBAR1\_G0 Register

#### 1 CONTROLSS\_ICLXBAR1\_G0 Register (Offset = 140h) [reset = 0h]

ICL XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-2207. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4140h       |

**Figure 3-713. CONTROLSS\_ICLXBAR1\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR1_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR1_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR1_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR1_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2209. CONTROLSS\_ICLXBAR1\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR1_G0_SEL | R/W  | 0h    | ICL XBAR1 G0 input bit select. Input source is MDLx.OUTA select<br>1:MDLx.OUTA bit[x] selected<br>0:MDLx.OUTA bit[x] is de-selected |

### 3.14.2.5 CONTROLSS\_ICLXBAR1\_G1 Register

#### 1 CONTROLSS\_ICLXBAR1\_G1 Register (Offset = 144h) [reset = 0h]

ICL XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-2210. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4144h       |

**Figure 3-714. CONTROLSS\_ICLXBAR1\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR1_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR1_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR1_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR1_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2212. CONTROLSS\_ICLXBAR1\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR1_G1_SEL | R/W  | 0h    | ICL XBAR1 G1 input bit select. Input source is MDLx.OUTB select<br>1:MDLx.OUTB bit[x] selected<br>0:MDLx.OUTB bit[x] is de-selected |

### 3.14.2.6 CONTROLSS\_ICLXBAR1\_G2 Register

#### 1 CONTROLSS\_ICLXBAR1\_G2 Register (Offset = 148h) [reset = 0h]

ICL XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-2213. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4148h       |

**Figure 3-715. CONTROLSS\_ICLXBAR1\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR1_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR1_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR1_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR1_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2215. CONTROLSS\_ICLXBAR1\_G2 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR1_G2_SEL | R/W  | 0h    | ICL XBAR1 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

### 3.14.2.7 CONTROLSS\_ICLXBAR2\_G0 Register

#### 1 CONTROLSS\_ICLXBAR2\_G0 Register (Offset = 180h) [reset = 0h]

ICL XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-2216. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4180h       |

**Figure 3-716. CONTROLSS\_ICLXBAR2\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR2_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR2_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR2_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR2_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2218. CONTROLSS\_ICLXBAR2\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR2_G0_SEL | R/W  | 0h    | ICL XBAR2 G0 input bit select. Input source is MDLx.OUTA select<br>1:MDLx.OUTA bit[x] selected<br>0:MDLx.OUTA bit[x] is de-selected |

### 3.14.2.8 CONTROLSS\_ICLXBAR2\_G1 Register

#### 1 CONTROLSS\_ICLXBAR2\_G1 Register (Offset = 184h) [reset = 0h]

ICL XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-2219. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4184h       |

**Figure 3-717. CONTROLSS\_ICLXBAR2\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR2_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR2_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR2_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR2_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2221. CONTROLSS\_ICLXBAR2\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR2_G1_SEL | R/W  | 0h    | ICL XBAR2 G1 input bit select. Input source is MDLx.OUTB select<br>1:MDLx.OUTB bit[x] selected<br>0:MDLx.OUTB bit[x] is de-selected |



### 3.14.2.9 CONTROLSS\_ICLXBAR2\_G2 Register

#### 1 CONTROLSS\_ICLXBAR2\_G2 Register (Offset = 188h) [reset = 0h]

ICL XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-2222. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4188h       |

**Figure 3-718. CONTROLSS\_ICLXBAR2\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR2_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR2_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR2_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR2_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2224. CONTROLSS\_ICLXBAR2\_G2 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR2_G2_SEL | R/W  | 0h    | ICL XBAR2 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

### 3.14.2.10 CONTROLSS\_ICLXBAR3\_G0 Register

#### 1 CONTROLSS\_ICLXBAR3\_G0 Register (Offset = 1C0h) [reset = 0h]

ICL XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-2225. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 41C0h       |

**Figure 3-719. CONTROLSS\_ICLXBAR3\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR3_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR3_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR3_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR3_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2227. CONTROLSS\_ICLXBAR3\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR3_G0_SEL | R/W  | 0h    | ICL XBAR3 G0 input bit select. Input source is MDLx.OUTA select<br>1:MDLx.OUTA bit[x] selected<br>0:MDLx.OUTA bit[x] is de-selected |

### 3.14.2.11 CONTROLSS\_ICLXBAR3\_G1 Register

#### 1 CONTROLSS\_ICLXBAR3\_G1 Register (Offset = 1C4h) [reset = 0h]

ICL XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-2228. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 41C4h       |

**Figure 3-720. CONTROLSS\_ICLXBAR3\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR3_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR3_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR3_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR3_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2230. CONTROLSS\_ICLXBAR3\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR3_G1_SEL | R/W  | 0h    | ICL XBAR3 G1 input bit select. Input source is MDLx.OUTB select<br>1:MDLx.OUTB bit[x] selected<br>0:MDLx.OUTB bit[x] is de-selected |

### 3.14.2.12 CONTROLSS\_ICLXBAR3\_G2 Register

#### 1 CONTROLSS\_ICLXBAR3\_G2 Register (Offset = 1C8h) [reset = 0h]

ICL XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-2231. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 41C8h       |

**Figure 3-721. CONTROLSS\_ICLXBAR3\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR3_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR3_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR3_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR3_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2233. CONTROLSS\_ICLXBAR3\_G2 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR3_G2_SEL | R/W  | 0h    | ICL XBAR3 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

### 3.14.2.13 CONTROLSS\_ICLXBAR4\_G0 Register

#### 1 CONTROLSS\_ICLXBAR4\_G0 Register (Offset = 200h) [reset = 0h]

ICL XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-2234. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4200h       |

**Figure 3-722. CONTROLSS\_ICLXBAR4\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR4_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR4_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR4_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR4_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2236. CONTROLSS\_ICLXBAR4\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR4_G0_SEL | R/W  | 0h    | ICL XBAR4 G0 input bit select. Input source is MDLx.OUTA select<br>1:MDLx.OUTA bit[x] selected<br>0:MDLx.OUTA bit[x] is de-selected |

### 3.14.2.14 CONTROLSS\_ICLXBAR4\_G1 Register

#### 1 CONTROLSS\_ICLXBAR4\_G1 Register (Offset = 204h) [reset = 0h]

ICL XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-2237. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4204h       |

**Figure 3-723. CONTROLSS\_ICLXBAR4\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR4_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR4_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR4_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR4_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2239. CONTROLSS\_ICLXBAR4\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR4_G1_SEL | R/W  | 0h    | ICL XBAR4 G1 input bit select. Input source is MDLx.OUTB select<br>1:MDLx.OUTB bit[x] selected<br>0:MDLx.OUTB bit[x] is de-selected |

### 3.14.2.15 CONTROLSS\_ICLXBAR4\_G2 Register

#### 1 CONTROLSS\_ICLXBAR4\_G2 Register (Offset = 208h) [reset = 0h]

ICL XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-2240. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4208h       |

**Figure 3-724. CONTROLSS\_ICLXBAR4\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR4_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR4_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR4_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR4_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2242. CONTROLSS\_ICLXBAR4\_G2 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR4_G2_SEL | R/W  | 0h    | ICL XBAR4 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

### 3.14.2.16 CONTROLSS\_ICLXBAR5\_G0 Register

#### 1 CONTROLSS\_ICLXBAR5\_G0 Register (Offset = 240h) [reset = 0h]

ICL XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-2243. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4240h       |

**Figure 3-725. CONTROLSS\_ICLXBAR5\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR5_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR5_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR5_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR5_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2245. CONTROLSS\_ICLXBAR5\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR5_G0_SEL | R/W  | 0h    | ICL XBAR5 G0 input bit select. Input source is MDLx.OUTA select<br>1:MDLx.OUTA bit[x] selected<br>0:MDLx.OUTA bit[x] is de-selected |



### 3.14.2.17 CONTROLSS\_ICLXBAR5\_G1 Register

#### 1 CONTROLSS\_ICLXBAR5\_G1 Register (Offset = 244h) [reset = 0h]

ICL XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-2246. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4244h       |

**Figure 3-726. CONTROLSS\_ICLXBAR5\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR5_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR5_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR5_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR5_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2248. CONTROLSS\_ICLXBAR5\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR5_G1_SEL | R/W  | 0h    | ICL XBAR5 G1 input bit select. Input source is MDLx.OUTB select<br>1:MDLx.OUTB bit[x] selected<br>0:MDLx.OUTB bit[x] is de-selected |

### 3.14.2.18 CONTROLSS\_ICLXBAR5\_G2 Register

#### 1 CONTROLSS\_ICLXBAR5\_G2 Register (Offset = 248h) [reset = 0h]

ICL XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-2249. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4248h       |

**Figure 3-727. CONTROLSS\_ICLXBAR5\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR5_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR5_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR5_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR5_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2251. CONTROLSS\_ICLXBAR5\_G2 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR5_G2_SEL | R/W  | 0h    | ICL XBAR5 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

### 3.14.2.19 CONTROLSS\_ICLXBAR6\_G0 Register

#### 1 CONTROLSS\_ICLXBAR6\_G0 Register (Offset = 280h) [reset = 0h]

ICL XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-2252. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4280h       |

**Figure 3-728. CONTROLSS\_ICLXBAR6\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR6_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR6_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR6_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR6_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2254. CONTROLSS\_ICLXBAR6\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR6_G0_SEL | R/W  | 0h    | ICL XBAR6 G0 input bit select. Input source is MDLx.OUTA select<br>1:MDLx.OUTA bit[x] selected<br>0:MDLx.OUTA bit[x] is de-selected |

### 3.14.2.20 CONTROLSS\_ICLXBAR6\_G1 Register

#### 1 CONTROLSS\_ICLXBAR6\_G1 Register (Offset = 284h) [reset = 0h]

ICL XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-2255. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4284h       |

**Figure 3-729. CONTROLSS\_ICLXBAR6\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR6_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR6_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR6_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR6_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2257. CONTROLSS\_ICLXBAR6\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR6_G1_SEL | R/W  | 0h    | ICL XBAR6 G1 input bit select. Input source is MDLx.OUTB select<br>1:MDLx.OUTB bit[x] selected<br>0:MDLx.OUTB bit[x] is de-selected |

### 3.14.2.21 CONTROLSS\_ICLXBAR6\_G2 Register

#### 1 CONTROLSS\_ICLXBAR6\_G2 Register (Offset = 288h) [reset = 0h]

ICL XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-2258. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4288h       |

**Figure 3-730. CONTROLSS\_ICLXBAR6\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR6_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR6_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR6_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR6_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2260. CONTROLSS\_ICLXBAR6\_G2 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR6_G2_SEL | R/W  | 0h    | ICL XBAR6 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

### 3.14.2.22 CONTROLSS\_ICLXBAR7\_G0 Register

#### 1 CONTROLSS\_ICLXBAR7\_G0 Register (Offset = 2C0h) [reset = 0h]

ICL XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-2261. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 42C0h       |

**Figure 3-731. CONTROLSS\_ICLXBAR7\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR7_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR7_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR7_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR7_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2263. CONTROLSS\_ICLXBAR7\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR7_G0_SEL | R/W  | 0h    | ICL XBAR7 G0 input bit select. Input source is MDLx.OUTA select<br>1:MDLx.OUTA bit[x] selected<br>0:MDLx.OUTA bit[x] is de-selected |

### 3.14.2.23 CONTROLSS\_ICLXBAR7\_G1 Register

#### 1 CONTROLSS\_ICLXBAR7\_G1 Register (Offset = 2C4h) [reset = 0h]

ICL XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-2264. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 42C4h       |

**Figure 3-732. CONTROLSS\_ICLXBAR7\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR7_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR7_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR7_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR7_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2266. CONTROLSS\_ICLXBAR7\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR7_G1_SEL | R/W  | 0h    | ICL XBAR7 G1 input bit select. Input source is MDLx.OUTB select<br>1:MDLx.OUTB bit[x] selected<br>0:MDLx.OUTB bit[x] is de-selected |

### 3.14.2.24 CONTROLSS\_ICLXBAR7\_G2 Register

#### 1 CONTROLSS\_ICLXBAR7\_G2 Register (Offset = 2C8h) [reset = 0h]

ICL XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-2267. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 42C8h       |

**Figure 3-733. CONTROLSS\_ICLXBAR7\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR7_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR7_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR7_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR7_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2269. CONTROLSS\_ICLXBAR7\_G2 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR7_G2_SEL | R/W  | 0h    | ICL XBAR7 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |



### 3.14.2.25 CONTROLSS\_ICLXBAR8\_G0 Register

#### 1 CONTROLSS\_ICLXBAR8\_G0 Register (Offset = 300h) [reset = 0h]

ICL XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-2270. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4300h       |

**Figure 3-734. CONTROLSS\_ICLXBAR8\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR8_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR8_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR8_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR8_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2272. CONTROLSS\_ICLXBAR8\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR8_G0_SEL | R/W  | 0h    | ICL XBAR8 G0 input bit select. Input source is MDLx.OUTA select<br>1:MDLx.OUTA bit[x] selected<br>0:MDLx.OUTA bit[x] is de-selected |

### 3.14.2.26 CONTROLSS\_ICLXBAR8\_G1 Register

#### 1 CONTROLSS\_ICLXBAR8\_G1 Register (Offset = 304h) [reset = 0h]

ICL XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-2273. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4304h       |

**Figure 3-735. CONTROLSS\_ICLXBAR8\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR8_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR8_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR8_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR8_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2275. CONTROLSS\_ICLXBAR8\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR8_G1_SEL | R/W  | 0h    | ICL XBAR8 G1 input bit select. Input source is MDLx.OUTB select<br>1:MDLx.OUTB bit[x] selected<br>0:MDLx.OUTB bit[x] is de-selected |

### 3.14.2.27 CONTROLSS\_ICLXBAR8\_G2 Register

#### 1 CONTROLSS\_ICLXBAR8\_G2 Register (Offset = 308h) [reset = 0h]

ICL XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-2276. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4308h       |

**Figure 3-736. CONTROLSS\_ICLXBAR8\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR8_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR8_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR8_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR8_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2278. CONTROLSS\_ICLXBAR8\_G2 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR8_G2_SEL | R/W  | 0h    | ICL XBAR8 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

### 3.14.2.28 CONTROLSS\_ICLXBAR9\_G0 Register

#### 1 CONTROLSS\_ICLXBAR9\_G0 Register (Offset = 340h) [reset = 0h]

ICL XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-2279. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4340h       |

**Figure 3-737. CONTROLSS\_ICLXBAR9\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR9_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR9_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR9_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR9_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2281. CONTROLSS\_ICLXBAR9\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR9_G0_SEL | R/W  | 0h    | ICL XBAR9 G0 input bit select. Input source is MDLx.OUTA select<br>1:MDLx.OUTA bit[x] selected<br>0:MDLx.OUTA bit[x] is de-selected |

### 3.14.2.29 CONTROLSS\_ICLXBAR9\_G1 Register

#### 1 CONTROLSS\_ICLXBAR9\_G1 Register (Offset = 344h) [reset = 0h]

ICL XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-2282. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4344h       |

**Figure 3-738. CONTROLSS\_ICLXBAR9\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR9_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR9_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR9_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR9_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2284. CONTROLSS\_ICLXBAR9\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR9_G1_SEL | R/W  | 0h    | ICL XBAR9 G1 input bit select. Input source is MDLx.OUTB select<br>1:MDLx.OUTB bit[x] selected<br>0:MDLx.OUTB bit[x] is de-selected |

### 3.14.2.30 CONTROLSS\_ICLXBAR9\_G2 Register

#### 1 CONTROLSS\_ICLXBAR9\_G2 Register (Offset = 348h) [reset = 0h]

ICL XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-2285. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4348h       |

**Figure 3-739. CONTROLSS\_ICLXBAR9\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR9_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR9_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR9_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR9_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2287. CONTROLSS\_ICLXBAR9\_G2 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR9_G2_SEL | R/W  | 0h    | ICL XBAR9 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

### 3.14.2.31 CONTROLSS\_ICLXBAR10\_G0 Register

#### 1 CONTROLSS\_ICLXBAR10\_G0 Register (Offset = 380h) [reset = 0h]

ICL XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-2288. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4380h       |

**Figure 3-740. CONTROLSS\_ICLXBAR10\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR10_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR10_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR10_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR10_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2290. CONTROLSS\_ICLXBAR10\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR10_G0_SEL | R/W  | 0h    | ICL XBAR10 G0 input bit select. Input source is MDLx.OUTA select<br>1:MDLx.OUTA bit[x] selected<br>0:MDLx.OUTA bit[x] is de-selected |

### 3.14.2.32 CONTROLSS\_ICLXBAR10\_G1 Register

#### 1 CONTROLSS\_ICLXBAR10\_G1 Register (Offset = 384h) [reset = 0h]

ICL XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-2291. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4384h       |

**Figure 3-741. CONTROLSS\_ICLXBAR10\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR10_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR10_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR10_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR10_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2293. CONTROLSS\_ICLXBAR10\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR10_G1_SEL | R/W  | 0h    | ICL XBAR10 G1 input bit select. Input source is MDLx.OUTB select<br>1:MDLx.OUTB bit[x] selected<br>0:MDLx.OUTB bit[x] is de-selected |



### 3.14.2.33 CONTROLSS\_ICLXBAR10\_G2 Register

#### 1 CONTROLSS\_ICLXBAR10\_G2 Register (Offset = 388h) [reset = 0h]

ICL XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-2294. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4388h       |

**Figure 3-742. CONTROLSS\_ICLXBAR10\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR10_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR10_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR10_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR10_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2296. CONTROLSS\_ICLXBAR10\_G2 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR10_G2_SEL | R/W  | 0h    | ICL XBAR10 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

### 3.14.2.34 CONTROLSS\_ICLXBAR11\_G0 Register

#### 1 CONTROLSS\_ICLXBAR11\_G0 Register (Offset = 3C0h) [reset = 0h]

ICL XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-2297. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 43C0h       |

**Figure 3-743. CONTROLSS\_ICLXBAR11\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR11_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR11_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR11_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR11_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2299. CONTROLSS\_ICLXBAR11\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR11_G0_SEL | R/W  | 0h    | ICL XBAR11 G0 input bit select. Input source is MDLx.OUTA select<br>1:MDLx.OUTA bit[x] selected<br>0:MDLx.OUTA bit[x] is de-selected |

### 3.14.2.35 CONTROLSS\_ICLXBAR11\_G1 Register

#### 1 CONTROLSS\_ICLXBAR11\_G1 Register (Offset = 3C4h) [reset = 0h]

ICL XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-2300. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 43C4h       |

**Figure 3-744. CONTROLSS\_ICLXBAR11\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR11_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR11_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR11_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR11_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2302. CONTROLSS\_ICLXBAR11\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                       |
|------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR11_G1_SEL | R/W  | 0h    | ICL XBAR11 G1 input bit select. Input source is MDLx.OTB select<br>1:MDLx.OTB bit[x] selected<br>0:MDLx.OTB bit[x] is de-selected |

### 3.14.2.36 CONTROLSS\_ICLXBAR11\_G2 Register

#### 1 CONTROLSS\_ICLXBAR11\_G2 Register (Offset = 3C8h) [reset = 0h]

ICL XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-2303. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 43C8h       |

**Figure 3-745. CONTROLSS\_ICLXBAR11\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR11_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR11_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR11_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR11_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2305. CONTROLSS\_ICLXBAR11\_G2 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR11_G2_SEL | R/W  | 0h    | ICL XBAR11 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

### 3.14.2.37 CONTROLSS\_ICLXBAR12\_G0 Register

#### 1 CONTROLSS\_ICLXBAR12\_G0 Register (Offset = 400h) [reset = 0h]

ICL XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-2306. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4400h       |

**Figure 3-746. CONTROLSS\_ICLXBAR12\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR12_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR12_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR12_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR12_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2308. CONTROLSS\_ICLXBAR12\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR12_G0_SEL | R/W  | 0h    | ICL XBAR12 G0 input bit select. Input source is MDLx.OUTA select<br>1:MDLx.OUTA bit[x] selected<br>0:MDLx.OUTA bit[x] is de-selected |

### 3.14.2.38 CONTROLSS\_ICLXBAR12\_G1 Register

#### 1 CONTROLSS\_ICLXBAR12\_G1 Register (Offset = 404h) [reset = 0h]

ICL XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-2309. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4404h       |

**Figure 3-747. CONTROLSS\_ICLXBAR12\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR12_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR12_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR12_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR12_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2311. CONTROLSS\_ICLXBAR12\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR12_G1_SEL | R/W  | 0h    | ICL XBAR12 G1 input bit select. Input source is MDLx.OUTB select<br>1:MDLx.OUTB bit[x] selected<br>0:MDLx.OUTB bit[x] is de-selected |

### 3.14.2.39 CONTROLSS\_ICLXBAR12\_G2 Register

#### 1 CONTROLSS\_ICLXBAR12\_G2 Register (Offset = 408h) [reset = 0h]

ICL XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-2312. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4408h       |

**Figure 3-748. CONTROLSS\_ICLXBAR12\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR12_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR12_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR12_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR12_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2314. CONTROLSS\_ICLXBAR12\_G2 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR12_G2_SEL | R/W  | 0h    | ICL XBAR12 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

### 3.14.2.40 CONTROLSS\_ICLXBAR13\_G0 Register

#### 1 CONTROLSS\_ICLXBAR13\_G0 Register (Offset = 440h) [reset = 0h]

ICL XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-2315. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4440h       |

**Figure 3-749. CONTROLSS\_ICLXBAR13\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR13_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR13_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR13_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR13_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2317. CONTROLSS\_ICLXBAR13\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR13_G0_SEL | R/W  | 0h    | ICL XBAR13 G0 input bit select. Input source is MDLx.OUTA select<br>1:MDLx.OUTA bit[x] selected<br>0:MDLx.OUTA bit[x] is de-selected |



### 3.14.2.41 CONTROLSS\_ICLXBAR13\_G1 Register

#### 1 CONTROLSS\_ICLXBAR13\_G1 Register (Offset = 444h) [reset = 0h]

ICL XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-2318. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4444h       |

**Figure 3-750. CONTROLSS\_ICLXBAR13\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR13_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR13_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR13_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR13_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2320. CONTROLSS\_ICLXBAR13\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR13_G1_SEL | R/W  | 0h    | ICL XBAR13 G1 input bit select. Input source is MDLx.OUTB select<br>1:MDLx.OUTB bit[x] selected<br>0:MDLx.OUTB bit[x] is de-selected |

### 3.14.2.42 CONTROLSS\_ICLXBAR13\_G2 Register

#### 1 CONTROLSS\_ICLXBAR13\_G2 Register (Offset = 448h) [reset = 0h]

ICL XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-2321. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4448h       |

**Figure 3-751. CONTROLSS\_ICLXBAR13\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR13_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR13_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR13_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR13_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2323. CONTROLSS\_ICLXBAR13\_G2 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR13_G2_SEL | R/W  | 0h    | ICL XBAR13 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

### 3.14.2.43 CONTROLSS\_ICLXBAR14\_G0 Register

#### 1 CONTROLSS\_ICLXBAR14\_G0 Register (Offset = 480h) [reset = 0h]

ICL XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-2324. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4480h       |

**Figure 3-752. CONTROLSS\_ICLXBAR14\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR14_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR14_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR14_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR14_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2326. CONTROLSS\_ICLXBAR14\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR14_G0_SEL | R/W  | 0h    | ICL XBAR14 G0 input bit select. Input source is MDLx.OUTA select<br>1:MDLx.OUTA bit[x] selected<br>0:MDLx.OUTA bit[x] is de-selected |

### 3.14.2.44 CONTROLSS\_ICLXBAR14\_G1 Register

#### 1 CONTROLSS\_ICLXBAR14\_G1 Register (Offset = 484h) [reset = 0h]

ICL XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-2327. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4484h       |

**Figure 3-753. CONTROLSS\_ICLXBAR14\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR14_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR14_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR14_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR14_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2329. CONTROLSS\_ICLXBAR14\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR14_G1_SEL | R/W  | 0h    | ICL XBAR14 G1 input bit select. Input source is MDLx.OUTB select<br>1:MDLx.OUTB bit[x] selected<br>0:MDLx.OUTB bit[x] is de-selected |

### 3.14.2.45 CONTROLSS\_ICLXBAR14\_G2 Register

#### 1 CONTROLSS\_ICLXBAR14\_G2 Register (Offset = 488h) [reset = 0h]

ICL XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-2330. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 4488h       |

**Figure 3-754. CONTROLSS\_ICLXBAR14\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR14_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR14_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR14_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR14_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2332. CONTROLSS\_ICLXBAR14\_G2 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR14_G2_SEL | R/W  | 0h    | ICL XBAR14 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

### 3.14.2.46 CONTROLSS\_ICLXBAR15\_G0 Register

#### 1 CONTROLSS\_ICLXBAR15\_G0 Register (Offset = 4C0h) [reset = 0h]

ICL XBAR 15 Input Select .

Return to [Summary Table](#)

**Table 3-2333. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 44C0h       |

**Figure 3-755. CONTROLSS\_ICLXBAR15\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR15_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR15_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR15_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR15_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2335. CONTROLSS\_ICLXBAR15\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR15_G0_SEL | R/W  | 0h    | ICL XBAR15 G0 input bit select. Input source is MDLx.OUTA select<br>1:MDLx.OUTA bit[x] selected<br>0:MDLx.OUTA bit[x] is de-selected |

### 3.14.2.47 CONTROLSS\_ICLXBAR15\_G1 Register

#### 1 CONTROLSS\_ICLXBAR15\_G1 Register (Offset = 4C4h) [reset = 0h]

ICL XBAR 15 Input Select .

Return to [Summary Table](#)

**Table 3-2336. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 44C4h       |

**Figure 3-756. CONTROLSS\_ICLXBAR15\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR15_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR15_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR15_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR15_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2338. CONTROLSS\_ICLXBAR15\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR15_G1_SEL | R/W  | 0h    | ICL XBAR15 G1 input bit select. Input source is MDLx.OUTB select<br>1:MDLx.OUTB bit[x] selected<br>0:MDLx.OUTB bit[x] is de-selected |

### 3.14.2.48 CONTROLSS\_ICLXBAR15\_G2 Register

#### 1 CONTROLSS\_ICLXBAR15\_G2 Register (Offset = 4C8h) [reset = 0h]

ICL XBAR 15 Input Select .

Return to [Summary Table](#)

**Table 3-2339. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_ICLXBAR | 502D 44C8h       |

**Figure 3-757. CONTROLSS\_ICLXBAR15\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICLXBAR15_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICLXBAR15_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICLXBAR15_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICLXBAR15_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2341. CONTROLSS\_ICLXBAR15\_G2 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ICLXBAR15_G2_SEL | R/W  | 0h    | ICL XBAR15 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |



## 3.15 CONTROLSS\_INPUTXBAR

### CONTROLSS\_INPUTXBAR

#### 3.15.1 CONTROLSS\_INPUTXBAR Summaries

#### CONTROLSS\_INPUTXBAR Summaries

**Table 3-2342. CONTROLSS Registers, Base Address=502D 0000h, Length=2048**

| Offset | Length | Register Name                              | CONTROLSS_INPUTXBAR Physical Address |
|--------|--------|--------------------------------------------|--------------------------------------|
| 100h   | 32     | <a href="#">CONTROLSS_INPUTXBAR0_GSEL</a>  | 502D 0100h                           |
| 104h   | 32     | <a href="#">CONTROLSS_INPUTXBAR0_G0</a>    | 502D 0104h                           |
| 108h   | 32     | <a href="#">CONTROLSS_INPUTXBAR0_G1</a>    | 502D 0108h                           |
| 140h   | 32     | <a href="#">CONTROLSS_INPUTXBAR1_GSEL</a>  | 502D 0140h                           |
| 144h   | 32     | <a href="#">CONTROLSS_INPUTXBAR1_G0</a>    | 502D 0144h                           |
| 148h   | 32     | <a href="#">CONTROLSS_INPUTXBAR1_G1</a>    | 502D 0148h                           |
| 180h   | 32     | <a href="#">CONTROLSS_INPUTXBAR2_GSEL</a>  | 502D 0180h                           |
| 184h   | 32     | <a href="#">CONTROLSS_INPUTXBAR2_G0</a>    | 502D 0184h                           |
| 188h   | 32     | <a href="#">CONTROLSS_INPUTXBAR2_G1</a>    | 502D 0188h                           |
| 1C0h   | 32     | <a href="#">CONTROLSS_INPUTXBAR3_GSEL</a>  | 502D 01C0h                           |
| 1C4h   | 32     | <a href="#">CONTROLSS_INPUTXBAR3_G0</a>    | 502D 01C4h                           |
| 1C8h   | 32     | <a href="#">CONTROLSS_INPUTXBAR3_G1</a>    | 502D 01C8h                           |
| 200h   | 32     | <a href="#">CONTROLSS_INPUTXBAR4_GSEL</a>  | 502D 0200h                           |
| 204h   | 32     | <a href="#">CONTROLSS_INPUTXBAR4_G0</a>    | 502D 0204h                           |
| 208h   | 32     | <a href="#">CONTROLSS_INPUTXBAR4_G1</a>    | 502D 0208h                           |
| 240h   | 32     | <a href="#">CONTROLSS_INPUTXBAR5_GSEL</a>  | 502D 0240h                           |
| 244h   | 32     | <a href="#">CONTROLSS_INPUTXBAR5_G0</a>    | 502D 0244h                           |
| 248h   | 32     | <a href="#">CONTROLSS_INPUTXBAR5_G1</a>    | 502D 0248h                           |
| 280h   | 32     | <a href="#">CONTROLSS_INPUTXBAR6_GSEL</a>  | 502D 0280h                           |
| 284h   | 32     | <a href="#">CONTROLSS_INPUTXBAR6_G0</a>    | 502D 0284h                           |
| 288h   | 32     | <a href="#">CONTROLSS_INPUTXBAR6_G1</a>    | 502D 0288h                           |
| 2C0h   | 32     | <a href="#">CONTROLSS_INPUTXBAR7_GSEL</a>  | 502D 02C0h                           |
| 2C4h   | 32     | <a href="#">CONTROLSS_INPUTXBAR7_G0</a>    | 502D 02C4h                           |
| 2C8h   | 32     | <a href="#">CONTROLSS_INPUTXBAR7_G1</a>    | 502D 02C8h                           |
| 300h   | 32     | <a href="#">CONTROLSS_INPUTXBAR8_GSEL</a>  | 502D 0300h                           |
| 304h   | 32     | <a href="#">CONTROLSS_INPUTXBAR8_G0</a>    | 502D 0304h                           |
| 308h   | 32     | <a href="#">CONTROLSS_INPUTXBAR8_G1</a>    | 502D 0308h                           |
| 340h   | 32     | <a href="#">CONTROLSS_INPUTXBAR9_GSEL</a>  | 502D 0340h                           |
| 344h   | 32     | <a href="#">CONTROLSS_INPUTXBAR9_G0</a>    | 502D 0344h                           |
| 348h   | 32     | <a href="#">CONTROLSS_INPUTXBAR9_G1</a>    | 502D 0348h                           |
| 380h   | 32     | <a href="#">CONTROLSS_INPUTXBAR10_GSEL</a> | 502D 0380h                           |
| 384h   | 32     | <a href="#">CONTROLSS_INPUTXBAR10_G0</a>   | 502D 0384h                           |
| 388h   | 32     | <a href="#">CONTROLSS_INPUTXBAR10_G1</a>   | 502D 0388h                           |
| 3C0h   | 32     | <a href="#">CONTROLSS_INPUTXBAR11_GSEL</a> | 502D 03C0h                           |
| 3C4h   | 32     | <a href="#">CONTROLSS_INPUTXBAR11_G0</a>   | 502D 03C4h                           |
| 3C8h   | 32     | <a href="#">CONTROLSS_INPUTXBAR11_G1</a>   | 502D 03C8h                           |
| 400h   | 32     | <a href="#">CONTROLSS_INPUTXBAR12_GSEL</a> | 502D 0400h                           |

**Table 3-2342. CONTROLSS Registers, Base Address=502D 0000h, Length=2048 (continued)**

| Offset | Length | Register Name                              | CONTROLSS_INPUTXBAR Physical Address |
|--------|--------|--------------------------------------------|--------------------------------------|
| 404h   | 32     | <a href="#">CONTROLSS_INPUTXBAR12_G0</a>   | 502D 0404h                           |
| 408h   | 32     | <a href="#">CONTROLSS_INPUTXBAR12_G1</a>   | 502D 0408h                           |
| 440h   | 32     | <a href="#">CONTROLSS_INPUTXBAR13_GSEL</a> | 502D 0440h                           |
| 444h   | 32     | <a href="#">CONTROLSS_INPUTXBAR13_G0</a>   | 502D 0444h                           |
| 448h   | 32     | <a href="#">CONTROLSS_INPUTXBAR13_G1</a>   | 502D 0448h                           |
| 480h   | 32     | <a href="#">CONTROLSS_INPUTXBAR14_GSEL</a> | 502D 0480h                           |
| 484h   | 32     | <a href="#">CONTROLSS_INPUTXBAR14_G0</a>   | 502D 0484h                           |
| 488h   | 32     | <a href="#">CONTROLSS_INPUTXBAR14_G1</a>   | 502D 0488h                           |
| 4C0h   | 32     | <a href="#">CONTROLSS_INPUTXBAR15_GSEL</a> | 502D 04C0h                           |
| 4C4h   | 32     | <a href="#">CONTROLSS_INPUTXBAR15_G0</a>   | 502D 04C4h                           |
| 4C8h   | 32     | <a href="#">CONTROLSS_INPUTXBAR15_G1</a>   | 502D 04C8h                           |
| 500h   | 32     | <a href="#">CONTROLSS_INPUTXBAR16_GSEL</a> | 502D 0500h                           |
| 504h   | 32     | <a href="#">CONTROLSS_INPUTXBAR16_G0</a>   | 502D 0504h                           |
| 508h   | 32     | <a href="#">CONTROLSS_INPUTXBAR16_G1</a>   | 502D 0508h                           |
| 540h   | 32     | <a href="#">CONTROLSS_INPUTXBAR17_GSEL</a> | 502D 0540h                           |
| 544h   | 32     | <a href="#">CONTROLSS_INPUTXBAR17_G0</a>   | 502D 0544h                           |
| 548h   | 32     | <a href="#">CONTROLSS_INPUTXBAR17_G1</a>   | 502D 0548h                           |
| 580h   | 32     | <a href="#">CONTROLSS_INPUTXBAR18_GSEL</a> | 502D 0580h                           |
| 584h   | 32     | <a href="#">CONTROLSS_INPUTXBAR18_G0</a>   | 502D 0584h                           |
| 588h   | 32     | <a href="#">CONTROLSS_INPUTXBAR18_G1</a>   | 502D 0588h                           |
| 5C0h   | 32     | <a href="#">CONTROLSS_INPUTXBAR19_GSEL</a> | 502D 05C0h                           |
| 5C4h   | 32     | <a href="#">CONTROLSS_INPUTXBAR19_G0</a>   | 502D 05C4h                           |
| 5C8h   | 32     | <a href="#">CONTROLSS_INPUTXBAR19_G1</a>   | 502D 05C8h                           |
| 600h   | 32     | <a href="#">CONTROLSS_INPUTXBAR20_GSEL</a> | 502D 0600h                           |
| 604h   | 32     | <a href="#">CONTROLSS_INPUTXBAR20_G0</a>   | 502D 0604h                           |
| 608h   | 32     | <a href="#">CONTROLSS_INPUTXBAR20_G1</a>   | 502D 0608h                           |
| 640h   | 32     | <a href="#">CONTROLSS_INPUTXBAR21_GSEL</a> | 502D 0640h                           |
| 644h   | 32     | <a href="#">CONTROLSS_INPUTXBAR21_G0</a>   | 502D 0644h                           |
| 648h   | 32     | <a href="#">CONTROLSS_INPUTXBAR21_G1</a>   | 502D 0648h                           |
| 680h   | 32     | <a href="#">CONTROLSS_INPUTXBAR22_GSEL</a> | 502D 0680h                           |
| 684h   | 32     | <a href="#">CONTROLSS_INPUTXBAR22_G0</a>   | 502D 0684h                           |
| 688h   | 32     | <a href="#">CONTROLSS_INPUTXBAR22_G1</a>   | 502D 0688h                           |
| 6C0h   | 32     | <a href="#">CONTROLSS_INPUTXBAR23_GSEL</a> | 502D 06C0h                           |
| 6C4h   | 32     | <a href="#">CONTROLSS_INPUTXBAR23_G0</a>   | 502D 06C4h                           |
| 6C8h   | 32     | <a href="#">CONTROLSS_INPUTXBAR23_G1</a>   | 502D 06C8h                           |
| 700h   | 32     | <a href="#">CONTROLSS_INPUTXBAR24_GSEL</a> | 502D 0700h                           |
| 704h   | 32     | <a href="#">CONTROLSS_INPUTXBAR24_G0</a>   | 502D 0704h                           |
| 708h   | 32     | <a href="#">CONTROLSS_INPUTXBAR24_G1</a>   | 502D 0708h                           |
| 740h   | 32     | <a href="#">CONTROLSS_INPUTXBAR25_GSEL</a> | 502D 0740h                           |
| 744h   | 32     | <a href="#">CONTROLSS_INPUTXBAR25_G0</a>   | 502D 0744h                           |
| 748h   | 32     | <a href="#">CONTROLSS_INPUTXBAR25_G1</a>   | 502D 0748h                           |
| 780h   | 32     | <a href="#">CONTROLSS_INPUTXBAR26_GSEL</a> | 502D 0780h                           |
| 784h   | 32     | <a href="#">CONTROLSS_INPUTXBAR26_G0</a>   | 502D 0784h                           |
| 788h   | 32     | <a href="#">CONTROLSS_INPUTXBAR26_G1</a>   | 502D 0788h                           |

**Table 3-2342. CONTROLSS Registers, Base Address=502D 0000h, Length=2048 (continued)**

| Offset | Length | Register Name                              | CONTROLSS_INPUTXBAR Physical Address |
|--------|--------|--------------------------------------------|--------------------------------------|
| 7C0h   | 32     | <a href="#">CONTROLSS_INPUTXBAR27_GSEL</a> | 502D 07C0h                           |
| 7C4h   | 32     | <a href="#">CONTROLSS_INPUTXBAR27_G0</a>   | 502D 07C4h                           |
| 7C8h   | 32     | <a href="#">CONTROLSS_INPUTXBAR27_G1</a>   | 502D 07C8h                           |
| 800h   | 32     | <a href="#">CONTROLSS_INPUTXBAR28_GSEL</a> | 502D 0800h                           |
| 804h   | 32     | <a href="#">CONTROLSS_INPUTXBAR28_G0</a>   | 502D 0804h                           |
| 808h   | 32     | <a href="#">CONTROLSS_INPUTXBAR28_G1</a>   | 502D 0808h                           |
| 840h   | 32     | <a href="#">CONTROLSS_INPUTXBAR29_GSEL</a> | 502D 0840h                           |
| 844h   | 32     | <a href="#">CONTROLSS_INPUTXBAR29_G0</a>   | 502D 0844h                           |
| 848h   | 32     | <a href="#">CONTROLSS_INPUTXBAR29_G1</a>   | 502D 0848h                           |
| 880h   | 32     | <a href="#">CONTROLSS_INPUTXBAR30_GSEL</a> | 502D 0880h                           |
| 884h   | 32     | <a href="#">CONTROLSS_INPUTXBAR30_G0</a>   | 502D 0884h                           |
| 888h   | 32     | <a href="#">CONTROLSS_INPUTXBAR30_G1</a>   | 502D 0888h                           |
| 8C0h   | 32     | <a href="#">CONTROLSS_INPUTXBAR31_GSEL</a> | 502D 08C0h                           |
| 8C4h   | 32     | <a href="#">CONTROLSS_INPUTXBAR31_G0</a>   | 502D 08C4h                           |
| 8C8h   | 32     | <a href="#">CONTROLSS_INPUTXBAR31_G1</a>   | 502D 08C8h                           |

### 3.15.2 CONTROLSS\_INPUTXBAR Registers

#### CONTROLSS\_INPUTXBAR Registers

### 3.15.2.1 CONTROLSS\_INPUTXBAR0\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR0\_GSEL Register (Offset = 100h) [reset = 0h]

INPUT XBAR0 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2343. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0100h       |

**Figure 3-758. CONTROLSS\_INPUTXBAR0\_GSEL Name Register**

|          |    |    |    |    |    |    |                      |
|----------|----|----|----|----|----|----|----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                   |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                   |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                    |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                    |
| RESERVED |    |    |    |    |    |    | INPUTXBAR0_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                  |
| 0h       |    |    |    |    |    |    | 0h                   |

**Table 3-2345. CONTROLSS\_INPUTXBAR0\_GSEL Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                  |
|------|----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED             | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR0_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.2 CONTROLSS\_INPUTXBAR0\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR0\_G0 Register (Offset = 104h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2346. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0104h       |

**Figure 3-759. CONTROLSS\_INPUTXBAR0\_G0 Name Register**

|                   |    |    |    |    |    |    |    |
|-------------------|----|----|----|----|----|----|----|
| 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR0_G0_SEL |    |    |    |    |    |    |    |
| R/W               |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |

**Table 3-2348. CONTROLSS\_INPUTXBAR0\_G0 Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                                                      |
|------|-------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED          | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR0_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.3 CONTROLSS\_INPUTXBAR0\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR0\_G1 Register (Offset = 108h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2349. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0108h       |

**Figure 3-760. CONTROLSS\_INPUTXBAR0\_G1 Name Register**

|          |    |    |                   |    |    |    |    |
|----------|----|----|-------------------|----|----|----|----|
| 31       | 30 | 29 | 28                | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                   |    |    |    |    |
| NONE     |    |    |                   |    |    |    |    |
| 0h       |    |    |                   |    |    |    |    |
| 23       | 22 | 21 | 20                | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                   |    |    |    |    |
| NONE     |    |    |                   |    |    |    |    |
| 0h       |    |    |                   |    |    |    |    |
| 15       | 14 | 13 | 12                | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                   |    |    |    |    |
| NONE     |    |    |                   |    |    |    |    |
| 0h       |    |    |                   |    |    |    |    |
| 7        | 6  | 5  | 4                 | 3  | 2  | 1  | 0  |
| RESERVED |    |    | INPUTXBAR0_G1_SEL |    |    |    |    |
| NONE     |    |    | R/W               |    |    |    |    |
| 0h       |    |    | 0h                |    |    |    |    |

**Table 3-2351. CONTROLSS\_INPUTXBAR0\_G1 Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                                                        |
|------|-------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED          | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR0_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

### 3.15.2.4 CONTROLSS\_INPUTXBAR1\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR1\_GSEL Register (Offset = 140h) [reset = 0h]

INPUT XBAR1 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2352. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0140h       |

**Figure 3-761. CONTROLSS\_INPUTXBAR1\_GSEL Name Register**

|          |    |    |    |    |    |    |                      |
|----------|----|----|----|----|----|----|----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                   |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                   |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                    |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                    |
| RESERVED |    |    |    |    |    |    | INPUTXBAR1_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                  |
| 0h       |    |    |    |    |    |    | 0h                   |

**Table 3-2354. CONTROLSS\_INPUTXBAR1\_GSEL Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                  |
|------|----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED             | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR1_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.5 CONTROLSS\_INPUTXBAR1\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR1\_G0 Register (Offset = 144h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2355. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0144h       |

**Figure 3-762. CONTROLSS\_INPUTXBAR1\_G0 Name Register**

|                   |    |    |    |    |    |    |    |
|-------------------|----|----|----|----|----|----|----|
| 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR1_G0_SEL |    |    |    |    |    |    |    |
| R/W               |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |

**Table 3-2357. CONTROLSS\_INPUTXBAR1\_G0 Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                                                      |
|------|-------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED          | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR1_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |



### 3.15.2.6 CONTROLSS\_INPUTXBAR1\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR1\_G1 Register (Offset = 148h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2358. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0148h       |

**Figure 3-763. CONTROLSS\_INPUTXBAR1\_G1 Name Register**

|          |    |    |    |                   |    |    |    |
|----------|----|----|----|-------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                | 26 | 25 | 24 |
| RESERVED |    |    |    |                   |    |    |    |
| NONE     |    |    |    |                   |    |    |    |
| 0h       |    |    |    |                   |    |    |    |
| 23       | 22 | 21 | 20 | 19                | 18 | 17 | 16 |
| RESERVED |    |    |    |                   |    |    |    |
| NONE     |    |    |    |                   |    |    |    |
| 0h       |    |    |    |                   |    |    |    |
| 15       | 14 | 13 | 12 | 11                | 10 | 9  | 8  |
| RESERVED |    |    |    |                   |    |    |    |
| NONE     |    |    |    |                   |    |    |    |
| 0h       |    |    |    |                   |    |    |    |
| 7        | 6  | 5  | 4  | 3                 | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR1_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W               |    |    |    |
| 0h       |    |    |    | 0h                |    |    |    |

**Table 3-2360. CONTROLSS\_INPUTXBAR1\_G1 Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                                                        |
|------|-------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED          | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR1_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

### 3.15.2.7 CONTROLSS\_INPUTXBAR2\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR2\_GSEL Register (Offset = 180h) [reset = 0h]

INPUT XBAR2 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2361. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0180h       |

**Figure 3-764. CONTROLSS\_INPUTXBAR2\_GSEL Name Register**

|          |    |    |    |    |    |    |                      |
|----------|----|----|----|----|----|----|----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                   |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                   |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                    |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                    |
| RESERVED |    |    |    |    |    |    | INPUTXBAR2_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                  |
| 0h       |    |    |    |    |    |    | 0h                   |

**Table 3-2363. CONTROLSS\_INPUTXBAR2\_GSEL Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                  |
|------|----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED             | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR2_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.8 CONTROLSS\_INPUTXBAR2\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR2\_G0 Register (Offset = 184h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2364. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0184h       |

**Figure 3-765. CONTROLSS\_INPUTXBAR2\_G0 Name Register**

|                   |    |    |    |    |    |    |    |
|-------------------|----|----|----|----|----|----|----|
| 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR2_G0_SEL |    |    |    |    |    |    |    |
| R/W               |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |

**Table 3-2366. CONTROLSS\_INPUTXBAR2\_G0 Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                                                      |
|------|-------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED          | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR2_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.9 CONTROLSS\_INPUTXBAR2\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR2\_G1 Register (Offset = 188h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2367. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0188h       |

**Figure 3-766. CONTROLSS\_INPUTXBAR2\_G1 Name Register**

|          |    |    |    |                   |    |    |    |
|----------|----|----|----|-------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                | 26 | 25 | 24 |
| RESERVED |    |    |    |                   |    |    |    |
| NONE     |    |    |    |                   |    |    |    |
| 0h       |    |    |    |                   |    |    |    |
| 23       | 22 | 21 | 20 | 19                | 18 | 17 | 16 |
| RESERVED |    |    |    |                   |    |    |    |
| NONE     |    |    |    |                   |    |    |    |
| 0h       |    |    |    |                   |    |    |    |
| 15       | 14 | 13 | 12 | 11                | 10 | 9  | 8  |
| RESERVED |    |    |    |                   |    |    |    |
| NONE     |    |    |    |                   |    |    |    |
| 0h       |    |    |    |                   |    |    |    |
| 7        | 6  | 5  | 4  | 3                 | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR2_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W               |    |    |    |
| 0h       |    |    |    | 0h                |    |    |    |

**Table 3-2369. CONTROLSS\_INPUTXBAR2\_G1 Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                                                        |
|------|-------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED          | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR2_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

### 3.15.2.10 CONTROLSS\_INPUTXBAR3\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR3\_GSEL Register (Offset = 1C0h) [reset = 0h]

INPUT XBAR3 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2370. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 01C0h       |

**Figure 3-767. CONTROLSS\_INPUTXBAR3\_GSEL Name Register**

|          |    |    |    |    |    |    |                      |
|----------|----|----|----|----|----|----|----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                   |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                   |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                    |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                    |
| RESERVED |    |    |    |    |    |    | INPUTXBAR3_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                  |
| 0h       |    |    |    |    |    |    | 0h                   |

**Table 3-2372. CONTROLSS\_INPUTXBAR3\_GSEL Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                  |
|------|----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED             | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR3_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.11 CONTROLSS\_INPUTXBAR3\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR3\_G0 Register (Offset = 1C4h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2373. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 01C4h       |

**Figure 3-768. CONTROLSS\_INPUTXBAR3\_G0 Name Register**

|                   |    |    |    |    |    |    |    |
|-------------------|----|----|----|----|----|----|----|
| 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR3_G0_SEL |    |    |    |    |    |    |    |
| R/W               |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |

**Table 3-2375. CONTROLSS\_INPUTXBAR3\_G0 Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                                                      |
|------|-------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED          | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR3_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.12 CONTROLSS\_INPUTXBAR3\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR3\_G1 Register (Offset = 1C8h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2376. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 01C8h       |

**Figure 3-769. CONTROLSS\_INPUTXBAR3\_G1 Name Register**

|          |    |    |    |                   |    |    |    |
|----------|----|----|----|-------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                | 26 | 25 | 24 |
| RESERVED |    |    |    |                   |    |    |    |
| NONE     |    |    |    |                   |    |    |    |
| 0h       |    |    |    |                   |    |    |    |
| 23       | 22 | 21 | 20 | 19                | 18 | 17 | 16 |
| RESERVED |    |    |    |                   |    |    |    |
| NONE     |    |    |    |                   |    |    |    |
| 0h       |    |    |    |                   |    |    |    |
| 15       | 14 | 13 | 12 | 11                | 10 | 9  | 8  |
| RESERVED |    |    |    |                   |    |    |    |
| NONE     |    |    |    |                   |    |    |    |
| 0h       |    |    |    |                   |    |    |    |
| 7        | 6  | 5  | 4  | 3                 | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR3_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W               |    |    |    |
| 0h       |    |    |    | 0h                |    |    |    |

**Table 3-2378. CONTROLSS\_INPUTXBAR3\_G1 Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                                                        |
|------|-------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED          | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR3_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

### 3.15.2.13 CONTROLSS\_INPUTXBAR4\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR4\_GSEL Register (Offset = 200h) [reset = 0h]

INPUT XBAR4 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2379. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0200h       |

**Figure 3-770. CONTROLSS\_INPUTXBAR4\_GSEL Name Register**

|          |    |    |    |    |    |    |                      |
|----------|----|----|----|----|----|----|----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                   |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                   |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                    |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                    |
| RESERVED |    |    |    |    |    |    | INPUTXBAR4_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                  |
| 0h       |    |    |    |    |    |    | 0h                   |

**Table 3-2381. CONTROLSS\_INPUTXBAR4\_GSEL Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                  |
|------|----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED             | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR4_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |



### 3.15.2.14 CONTROLSS\_INPUTXBAR4\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR4\_G0 Register (Offset = 204h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2382. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0204h       |

**Figure 3-771. CONTROLSS\_INPUTXBAR4\_G0 Name Register**

|                   |    |    |    |    |    |    |    |
|-------------------|----|----|----|----|----|----|----|
| 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR4_G0_SEL |    |    |    |    |    |    |    |
| R/W               |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |

**Table 3-2384. CONTROLSS\_INPUTXBAR4\_G0 Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                                                      |
|------|-------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED          | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR4_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.15 CONTROLSS\_INPUTXBAR4\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR4\_G1 Register (Offset = 208h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2385. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0208h       |

**Figure 3-772. CONTROLSS\_INPUTXBAR4\_G1 Name Register**

|          |    |    |    |                   |    |    |    |
|----------|----|----|----|-------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                | 26 | 25 | 24 |
| RESERVED |    |    |    |                   |    |    |    |
| NONE     |    |    |    |                   |    |    |    |
| 0h       |    |    |    |                   |    |    |    |
| 23       | 22 | 21 | 20 | 19                | 18 | 17 | 16 |
| RESERVED |    |    |    |                   |    |    |    |
| NONE     |    |    |    |                   |    |    |    |
| 0h       |    |    |    |                   |    |    |    |
| 15       | 14 | 13 | 12 | 11                | 10 | 9  | 8  |
| RESERVED |    |    |    |                   |    |    |    |
| NONE     |    |    |    |                   |    |    |    |
| 0h       |    |    |    |                   |    |    |    |
| 7        | 6  | 5  | 4  | 3                 | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR4_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W               |    |    |    |
| 0h       |    |    |    | 0h                |    |    |    |

**Table 3-2387. CONTROLSS\_INPUTXBAR4\_G1 Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                                                        |
|------|-------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED          | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR4_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

### 3.15.2.16 CONTROLSS\_INPUTXBAR5\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR5\_GSEL Register (Offset = 240h) [reset = 0h]

INPUT XBAR5 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2388. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0240h       |

**Figure 3-773. CONTROLSS\_INPUTXBAR5\_GSEL Name Register**

|          |    |    |    |    |    |    |                      |
|----------|----|----|----|----|----|----|----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                   |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                   |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                    |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                    |
| RESERVED |    |    |    |    |    |    | INPUTXBAR5_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                  |
| 0h       |    |    |    |    |    |    | 0h                   |

**Table 3-2390. CONTROLSS\_INPUTXBAR5\_GSEL Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                  |
|------|----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED             | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR5_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.17 CONTROLSS\_INPUTXBAR5\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR5\_G0 Register (Offset = 244h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2391. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0244h       |

**Figure 3-774. CONTROLSS\_INPUTXBAR5\_G0 Name Register**

|                   |    |    |    |    |    |    |    |
|-------------------|----|----|----|----|----|----|----|
| 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR5_G0_SEL |    |    |    |    |    |    |    |
| R/W               |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |

**Table 3-2393. CONTROLSS\_INPUTXBAR5\_G0 Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                                                      |
|------|-------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED          | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR5_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.18 CONTROLSS\_INPUTXBAR5\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR5\_G1 Register (Offset = 248h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2394. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0248h       |

**Figure 3-775. CONTROLSS\_INPUTXBAR5\_G1 Name Register**

|          |    |    |    |                   |    |    |    |
|----------|----|----|----|-------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                | 26 | 25 | 24 |
| RESERVED |    |    |    |                   |    |    |    |
| NONE     |    |    |    |                   |    |    |    |
| 0h       |    |    |    |                   |    |    |    |
| 23       | 22 | 21 | 20 | 19                | 18 | 17 | 16 |
| RESERVED |    |    |    |                   |    |    |    |
| NONE     |    |    |    |                   |    |    |    |
| 0h       |    |    |    |                   |    |    |    |
| 15       | 14 | 13 | 12 | 11                | 10 | 9  | 8  |
| RESERVED |    |    |    |                   |    |    |    |
| NONE     |    |    |    |                   |    |    |    |
| 0h       |    |    |    |                   |    |    |    |
| 7        | 6  | 5  | 4  | 3                 | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR5_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W               |    |    |    |
| 0h       |    |    |    | 0h                |    |    |    |

**Table 3-2396. CONTROLSS\_INPUTXBAR5\_G1 Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                                                        |
|------|-------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED          | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR5_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

### 3.15.2.19 CONTROLSS\_INPUTXBAR6\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR6\_GSEL Register (Offset = 280h) [reset = 0h]

INPUT XBAR6 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2397. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0280h       |

**Figure 3-776. CONTROLSS\_INPUTXBAR6\_GSEL Name Register**

|          |    |    |    |    |    |    |                      |
|----------|----|----|----|----|----|----|----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                   |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                   |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                    |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                    |
| RESERVED |    |    |    |    |    |    | INPUTXBAR6_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                  |
| 0h       |    |    |    |    |    |    | 0h                   |

**Table 3-2399. CONTROLSS\_INPUTXBAR6\_GSEL Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                  |
|------|----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED             | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR6_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.20 CONTROLSS\_INPUTXBAR6\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR6\_G0 Register (Offset = 284h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2400. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0284h       |

**Figure 3-777. CONTROLSS\_INPUTXBAR6\_G0 Name Register**

|                   |    |    |    |    |    |    |    |
|-------------------|----|----|----|----|----|----|----|
| 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR6_G0_SEL |    |    |    |    |    |    |    |
| R/W               |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |

**Table 3-2402. CONTROLSS\_INPUTXBAR6\_G0 Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                                                      |
|------|-------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED          | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR6_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.21 CONTROLSS\_INPUTXBAR6\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR6\_G1 Register (Offset = 288h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2403. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0288h       |

**Figure 3-778. CONTROLSS\_INPUTXBAR6\_G1 Name Register**

|          |    |    |    |                   |    |    |    |
|----------|----|----|----|-------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                | 26 | 25 | 24 |
| RESERVED |    |    |    |                   |    |    |    |
| NONE     |    |    |    |                   |    |    |    |
| 0h       |    |    |    |                   |    |    |    |
| 23       | 22 | 21 | 20 | 19                | 18 | 17 | 16 |
| RESERVED |    |    |    |                   |    |    |    |
| NONE     |    |    |    |                   |    |    |    |
| 0h       |    |    |    |                   |    |    |    |
| 15       | 14 | 13 | 12 | 11                | 10 | 9  | 8  |
| RESERVED |    |    |    |                   |    |    |    |
| NONE     |    |    |    |                   |    |    |    |
| 0h       |    |    |    |                   |    |    |    |
| 7        | 6  | 5  | 4  | 3                 | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR6_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W               |    |    |    |
| 0h       |    |    |    | 0h                |    |    |    |

**Table 3-2405. CONTROLSS\_INPUTXBAR6\_G1 Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                                                        |
|------|-------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED          | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR6_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |



### 3.15.2.22 CONTROLSS\_INPUTXBAR7\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR7\_GSEL Register (Offset = 2C0h) [reset = 0h]

INPUT XBAR7 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2406. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 02C0h       |

**Figure 3-779. CONTROLSS\_INPUTXBAR7\_GSEL Name Register**

|          |    |    |    |    |    |    |                      |
|----------|----|----|----|----|----|----|----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                   |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                   |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                    |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                    |
| RESERVED |    |    |    |    |    |    | INPUTXBAR7_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                  |
| 0h       |    |    |    |    |    |    | 0h                   |

**Table 3-2408. CONTROLSS\_INPUTXBAR7\_GSEL Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                  |
|------|----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED             | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR7_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.23 CONTROLSS\_INPUTXBAR7\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR7\_G0 Register (Offset = 2C4h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2409. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 02C4h       |

**Figure 3-780. CONTROLSS\_INPUTXBAR7\_G0 Name Register**

|                   |    |    |    |    |    |    |    |
|-------------------|----|----|----|----|----|----|----|
| 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR7_G0_SEL |    |    |    |    |    |    |    |
| R/W               |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |

**Table 3-2411. CONTROLSS\_INPUTXBAR7\_G0 Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                                                      |
|------|-------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED          | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR7_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.24 CONTROLSS\_INPUTXBAR7\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR7\_G1 Register (Offset = 2C8h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2412. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 02C8h       |

**Figure 3-781. CONTROLSS\_INPUTXBAR7\_G1 Name Register**

|          |    |    |                   |    |    |    |    |
|----------|----|----|-------------------|----|----|----|----|
| 31       | 30 | 29 | 28                | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                   |    |    |    |    |
| NONE     |    |    |                   |    |    |    |    |
| 0h       |    |    |                   |    |    |    |    |
| 23       | 22 | 21 | 20                | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                   |    |    |    |    |
| NONE     |    |    |                   |    |    |    |    |
| 0h       |    |    |                   |    |    |    |    |
| 15       | 14 | 13 | 12                | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                   |    |    |    |    |
| NONE     |    |    |                   |    |    |    |    |
| 0h       |    |    |                   |    |    |    |    |
| 7        | 6  | 5  | 4                 | 3  | 2  | 1  | 0  |
| RESERVED |    |    | INPUTXBAR7_G1_SEL |    |    |    |    |
| NONE     |    |    | R/W               |    |    |    |    |
| 0h       |    |    | 0h                |    |    |    |    |

**Table 3-2414. CONTROLSS\_INPUTXBAR7\_G1 Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                                                        |
|------|-------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED          | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR7_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

### 3.15.2.25 CONTROLSS\_INPUTXBAR8\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR8\_GSEL Register (Offset = 300h) [reset = 0h]

INPUT XBAR8 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2415. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0300h       |

**Figure 3-782. CONTROLSS\_INPUTXBAR8\_GSEL Name Register**

|          |    |    |    |    |    |    |                      |
|----------|----|----|----|----|----|----|----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                   |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                   |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                    |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                    |
| RESERVED |    |    |    |    |    |    | INPUTXBAR8_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                  |
| 0h       |    |    |    |    |    |    | 0h                   |

**Table 3-2417. CONTROLSS\_INPUTXBAR8\_GSEL Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                  |
|------|----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED             | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR8_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.26 CONTROLSS\_INPUTXBAR8\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR8\_G0 Register (Offset = 304h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2418. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0304h       |

**Figure 3-783. CONTROLSS\_INPUTXBAR8\_G0 Name Register**

|                   |    |    |    |    |    |    |    |
|-------------------|----|----|----|----|----|----|----|
| 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR8_G0_SEL |    |    |    |    |    |    |    |
| R/W               |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |

**Table 3-2420. CONTROLSS\_INPUTXBAR8\_G0 Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                                                      |
|------|-------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED          | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR8_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.27 CONTROLSS\_INPUTXBAR8\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR8\_G1 Register (Offset = 308h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2421. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0308h       |

**Figure 3-784. CONTROLSS\_INPUTXBAR8\_G1 Name Register**

|          |    |    |                   |    |    |    |    |
|----------|----|----|-------------------|----|----|----|----|
| 31       | 30 | 29 | 28                | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                   |    |    |    |    |
| NONE     |    |    |                   |    |    |    |    |
| 0h       |    |    |                   |    |    |    |    |
| 23       | 22 | 21 | 20                | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                   |    |    |    |    |
| NONE     |    |    |                   |    |    |    |    |
| 0h       |    |    |                   |    |    |    |    |
| 15       | 14 | 13 | 12                | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                   |    |    |    |    |
| NONE     |    |    |                   |    |    |    |    |
| 0h       |    |    |                   |    |    |    |    |
| 7        | 6  | 5  | 4                 | 3  | 2  | 1  | 0  |
| RESERVED |    |    | INPUTXBAR8_G1_SEL |    |    |    |    |
| NONE     |    |    | R/W               |    |    |    |    |
| 0h       |    |    | 0h                |    |    |    |    |

**Table 3-2423. CONTROLSS\_INPUTXBAR8\_G1 Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                                                        |
|------|-------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED          | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR8_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

### 3.15.2.28 CONTROLSS\_INPUTXBAR9\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR9\_GSEL Register (Offset = 340h) [reset = 0h]

INPUT XBAR9 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2424. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0340h       |

**Figure 3-785. CONTROLSS\_INPUTXBAR9\_GSEL Name Register**

|          |    |    |    |    |    |    |                      |
|----------|----|----|----|----|----|----|----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                   |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                   |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                    |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                    |
| RESERVED |    |    |    |    |    |    | INPUTXBAR9_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                  |
| 0h       |    |    |    |    |    |    | 0h                   |

**Table 3-2426. CONTROLSS\_INPUTXBAR9\_GSEL Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                  |
|------|----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED             | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR9_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.29 CONTROLSS\_INPUTXBAR9\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR9\_G0 Register (Offset = 344h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2427. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0344h       |

**Figure 3-786. CONTROLSS\_INPUTXBAR9\_G0 Name Register**

|                   |    |    |    |    |    |    |    |
|-------------------|----|----|----|----|----|----|----|
| 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR9_G0_SEL |    |    |    |    |    |    |    |
| R/W               |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |

**Table 3-2429. CONTROLSS\_INPUTXBAR9\_G0 Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                                                      |
|------|-------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED          | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR9_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |



### 3.15.2.30 CONTROLSS\_INPUTXBAR9\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR9\_G1 Register (Offset = 348h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2430. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0348h       |

**Figure 3-787. CONTROLSS\_INPUTXBAR9\_G1 Name Register**

|          |    |    |    |                   |    |    |    |
|----------|----|----|----|-------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                | 26 | 25 | 24 |
| RESERVED |    |    |    |                   |    |    |    |
| NONE     |    |    |    |                   |    |    |    |
| 0h       |    |    |    |                   |    |    |    |
| 23       | 22 | 21 | 20 | 19                | 18 | 17 | 16 |
| RESERVED |    |    |    |                   |    |    |    |
| NONE     |    |    |    |                   |    |    |    |
| 0h       |    |    |    |                   |    |    |    |
| 15       | 14 | 13 | 12 | 11                | 10 | 9  | 8  |
| RESERVED |    |    |    |                   |    |    |    |
| NONE     |    |    |    |                   |    |    |    |
| 0h       |    |    |    |                   |    |    |    |
| 7        | 6  | 5  | 4  | 3                 | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR9_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W               |    |    |    |
| 0h       |    |    |    | 0h                |    |    |    |

**Table 3-2432. CONTROLSS\_INPUTXBAR9\_G1 Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                                                        |
|------|-------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED          | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR9_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

### 3.15.2.31 CONTROLSS\_INPUTXBAR10\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR10\_GSEL Register (Offset = 380h) [reset = 0h]

INPUT XBAR10 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2433. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0380h       |

**Figure 3-788. CONTROLSS\_INPUTXBAR10\_GSEL Name Register**

|          |    |    |    |    |    |    |                       |
|----------|----|----|----|----|----|----|-----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                     |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                     |
| RESERVED |    |    |    |    |    |    | INPUTXBAR10_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                   |
| 0h       |    |    |    |    |    |    | 0h                    |

**Table 3-2435. CONTROLSS\_INPUTXBAR10\_GSEL Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                  |
|------|-----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED              | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR10_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.32 CONTROLSS\_INPUTXBAR10\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR10\_G0 Register (Offset = 384h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2436. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0384h       |

**Figure 3-789. CONTROLSS\_INPUTXBAR10\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR10_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-2438. CONTROLSS\_INPUTXBAR10\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                      |
|------|--------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED           | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR10_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.33 CONTROLSS\_INPUTXBAR10\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR10\_G1 Register (Offset = 388h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2439. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0388h       |

**Figure 3-790. CONTROLSS\_INPUTXBAR10\_G1 Name Register**

|          |    |    |    |                    |    |    |    |
|----------|----|----|----|--------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 23       | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 15       | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 7        | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR10_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W                |    |    |    |
| 0h       |    |    |    | 0h                 |    |    |    |

**Table 3-2441. CONTROLSS\_INPUTXBAR10\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                        |
|------|--------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED           | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR10_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

### 3.15.2.34 CONTROLSS\_INPUTXBAR11\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR11\_GSEL Register (Offset = 3C0h) [reset = 0h]

INPUT XBAR11 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2442. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 03C0h       |

**Figure 3-791. CONTROLSS\_INPUTXBAR11\_GSEL Name Register**

|          |    |    |    |    |    |    |                       |
|----------|----|----|----|----|----|----|-----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                     |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                     |
| RESERVED |    |    |    |    |    |    | INPUTXBAR11_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                   |
| 0h       |    |    |    |    |    |    | 0h                    |

**Table 3-2444. CONTROLSS\_INPUTXBAR11\_GSEL Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                  |
|------|-----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED              | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR11_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.35 CONTROLSS\_INPUTXBAR11\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR11\_G0 Register (Offset = 3C4h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2445. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 03C4h       |

**Figure 3-792. CONTROLSS\_INPUTXBAR11\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR11_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-2447. CONTROLSS\_INPUTXBAR11\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                      |
|------|--------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED           | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR11_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.36 CONTROLSS\_INPUTXBAR11\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR11\_G1 Register (Offset = 3C8h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2448. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 03C8h       |

**Figure 3-793. CONTROLSS\_INPUTXBAR11\_G1 Name Register**

|          |    |    |    |                    |    |    |    |
|----------|----|----|----|--------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 23       | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 15       | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 7        | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR11_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W                |    |    |    |
| 0h       |    |    |    | 0h                 |    |    |    |

**Table 3-2450. CONTROLSS\_INPUTXBAR11\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                        |
|------|--------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED           | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR11_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

### 3.15.2.37 CONTROLSS\_INPUTXBAR12\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR12\_GSEL Register (Offset = 400h) [reset = 0h]

INPUT XBAR12 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2451. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0400h       |

**Figure 3-794. CONTROLSS\_INPUTXBAR12\_GSEL Name Register**

|          |    |    |    |    |    |    |                       |
|----------|----|----|----|----|----|----|-----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                     |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                     |
| RESERVED |    |    |    |    |    |    | INPUTXBAR12_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                   |
| 0h       |    |    |    |    |    |    | 0h                    |

**Table 3-2453. CONTROLSS\_INPUTXBAR12\_GSEL Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                  |
|------|-----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED              | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR12_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |



### 3.15.2.38 CONTROLSS\_INPUTXBAR12\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR12\_G0 Register (Offset = 404h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2454. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0404h       |

**Figure 3-795. CONTROLSS\_INPUTXBAR12\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR12_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-2456. CONTROLSS\_INPUTXBAR12\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                      |
|------|--------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED           | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR12_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.39 CONTROLSS\_INPUTXBAR12\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR12\_G1 Register (Offset = 408h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2457. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0408h       |

**Figure 3-796. CONTROLSS\_INPUTXBAR12\_G1 Name Register**

|          |    |    |    |                    |    |    |    |
|----------|----|----|----|--------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 23       | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 15       | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 7        | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR12_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W                |    |    |    |
| 0h       |    |    |    | 0h                 |    |    |    |

**Table 3-2459. CONTROLSS\_INPUTXBAR12\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                        |
|------|--------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED           | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR12_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

### 3.15.2.40 CONTROLSS\_INPUTXBAR13\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR13\_GSEL Register (Offset = 440h) [reset = 0h]

INPUT XBAR13 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2460. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0440h       |

**Figure 3-797. CONTROLSS\_INPUTXBAR13\_GSEL Name Register**

|          |    |    |    |    |    |    |                       |
|----------|----|----|----|----|----|----|-----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                     |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                     |
| RESERVED |    |    |    |    |    |    | INPUTXBAR13_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                   |
| 0h       |    |    |    |    |    |    | 0h                    |

**Table 3-2462. CONTROLSS\_INPUTXBAR13\_GSEL Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                  |
|------|-----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED              | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR13_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.41 CONTROLSS\_INPUTXBAR13\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR13\_G0 Register (Offset = 444h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2463. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0444h       |

**Figure 3-798. CONTROLSS\_INPUTXBAR13\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR13_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-2465. CONTROLSS\_INPUTXBAR13\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                      |
|------|--------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED           | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR13_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.42 CONTROLSS\_INPUTXBAR13\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR13\_G1 Register (Offset = 448h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2466. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0448h       |

**Figure 3-799. CONTROLSS\_INPUTXBAR13\_G1 Name Register**

|          |    |    |    |                    |    |    |    |
|----------|----|----|----|--------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 23       | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 15       | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 7        | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR13_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W                |    |    |    |
| 0h       |    |    |    | 0h                 |    |    |    |

**Table 3-2468. CONTROLSS\_INPUTXBAR13\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                        |
|------|--------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED           | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR13_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

### 3.15.2.43 CONTROLSS\_INPUTXBAR14\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR14\_GSEL Register (Offset = 480h) [reset = 0h]

INPUT XBAR14 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2469. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0480h       |

**Figure 3-800. CONTROLSS\_INPUTXBAR14\_GSEL Name Register**

|          |    |    |    |    |    |    |                       |
|----------|----|----|----|----|----|----|-----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                     |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                     |
| RESERVED |    |    |    |    |    |    | INPUTXBAR14_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                   |
| 0h       |    |    |    |    |    |    | 0h                    |

**Table 3-2471. CONTROLSS\_INPUTXBAR14\_GSEL Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                  |
|------|-----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED              | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR14_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.44 CONTROLSS\_INPUTXBAR14\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR14\_G0 Register (Offset = 484h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2472. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0484h       |

**Figure 3-801. CONTROLSS\_INPUTXBAR14\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR14_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-2474. CONTROLSS\_INPUTXBAR14\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                      |
|------|--------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED           | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR14_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.45 CONTROLSS\_INPUTXBAR14\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR14\_G1 Register (Offset = 488h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2475. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0488h       |

**Figure 3-802. CONTROLSS\_INPUTXBAR14\_G1 Name Register**

|          |    |    |    |                    |    |    |    |
|----------|----|----|----|--------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 23       | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 15       | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 7        | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR14_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W                |    |    |    |
| 0h       |    |    |    | 0h                 |    |    |    |

**Table 3-2477. CONTROLSS\_INPUTXBAR14\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                        |
|------|--------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED           | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR14_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |



### 3.15.2.46 CONTROLSS\_INPUTXBAR15\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR15\_GSEL Register (Offset = 4C0h) [reset = 0h]

INPUT XBAR15 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2478. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 04C0h       |

**Figure 3-803. CONTROLSS\_INPUTXBAR15\_GSEL Name Register**

|          |    |    |    |    |    |    |                       |
|----------|----|----|----|----|----|----|-----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                     |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                     |
| RESERVED |    |    |    |    |    |    | INPUTXBAR15_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                   |
| 0h       |    |    |    |    |    |    | 0h                    |

**Table 3-2480. CONTROLSS\_INPUTXBAR15\_GSEL Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                  |
|------|-----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED              | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR15_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.47 CONTROLSS\_INPUTXBAR15\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR15\_G0 Register (Offset = 4C4h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2481. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 04C4h       |

**Figure 3-804. CONTROLSS\_INPUTXBAR15\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR15_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-2483. CONTROLSS\_INPUTXBAR15\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                      |
|------|--------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED           | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR15_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.48 CONTROLSS\_INPUTXBAR15\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR15\_G1 Register (Offset = 4C8h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2484. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 04C8h       |

**Figure 3-805. CONTROLSS\_INPUTXBAR15\_G1 Name Register**

|          |    |    |    |                    |    |    |    |
|----------|----|----|----|--------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 23       | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 15       | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 7        | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR15_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W                |    |    |    |
| 0h       |    |    |    | 0h                 |    |    |    |

**Table 3-2486. CONTROLSS\_INPUTXBAR15\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                        |
|------|--------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED           | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR15_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

### 3.15.2.49 CONTROLSS\_INPUTXBAR16\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR16\_GSEL Register (Offset = 500h) [reset = 0h]

INPUT XBAR16 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2487. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0500h       |

**Figure 3-806. CONTROLSS\_INPUTXBAR16\_GSEL Name Register**

|          |    |    |    |    |    |    |                       |
|----------|----|----|----|----|----|----|-----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                     |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                     |
| RESERVED |    |    |    |    |    |    | INPUTXBAR16_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                   |
| 0h       |    |    |    |    |    |    | 0h                    |

**Table 3-2489. CONTROLSS\_INPUTXBAR16\_GSEL Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                  |
|------|-----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED              | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR16_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.50 CONTROLSS\_INPUTXBAR16\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR16\_G0 Register (Offset = 504h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2490. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0504h       |

**Figure 3-807. CONTROLSS\_INPUTXBAR16\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR16_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-2492. CONTROLSS\_INPUTXBAR16\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                      |
|------|--------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED           | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR16_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.51 CONTROLSS\_INPUTXBAR16\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR16\_G1 Register (Offset = 508h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2493. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0508h       |

**Figure 3-808. CONTROLSS\_INPUTXBAR16\_G1 Name Register**

|          |    |    |    |                    |    |    |    |
|----------|----|----|----|--------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 23       | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 15       | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 7        | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR16_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W                |    |    |    |
| 0h       |    |    |    | 0h                 |    |    |    |

**Table 3-2495. CONTROLSS\_INPUTXBAR16\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                        |
|------|--------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED           | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR16_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

### 3.15.2.52 CONTROLSS\_INPUTXBAR17\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR17\_GSEL Register (Offset = 540h) [reset = 0h]

INPUT XBAR17 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2496. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0540h       |

**Figure 3-809. CONTROLSS\_INPUTXBAR17\_GSEL Name Register**

|          |    |    |    |    |    |    |                       |
|----------|----|----|----|----|----|----|-----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                     |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                     |
| RESERVED |    |    |    |    |    |    | INPUTXBAR17_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                   |
| 0h       |    |    |    |    |    |    | 0h                    |

**Table 3-2498. CONTROLSS\_INPUTXBAR17\_GSEL Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                  |
|------|-----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED              | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR17_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.53 CONTROLSS\_INPUTXBAR17\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR17\_G0 Register (Offset = 544h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2499. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0544h       |

**Figure 3-810. CONTROLSS\_INPUTXBAR17\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR17_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-2501. CONTROLSS\_INPUTXBAR17\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                      |
|------|--------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED           | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR17_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |



### 3.15.2.54 CONTROLSS\_INPUTXBAR17\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR17\_G1 Register (Offset = 548h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2502. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0548h       |

**Figure 3-811. CONTROLSS\_INPUTXBAR17\_G1 Name Register**

|          |    |    |    |                    |    |    |    |
|----------|----|----|----|--------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 23       | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 15       | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 7        | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR17_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W                |    |    |    |
| 0h       |    |    |    | 0h                 |    |    |    |

**Table 3-2504. CONTROLSS\_INPUTXBAR17\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                        |
|------|--------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED           | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR17_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

### 3.15.2.55 CONTROLSS\_INPUTXBAR18\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR18\_GSEL Register (Offset = 580h) [reset = 0h]

INPUT XBAR18 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2505. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0580h       |

**Figure 3-812. CONTROLSS\_INPUTXBAR18\_GSEL Name Register**

|          |    |    |    |    |    |    |                       |
|----------|----|----|----|----|----|----|-----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                     |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                     |
| RESERVED |    |    |    |    |    |    | INPUTXBAR18_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                   |
| 0h       |    |    |    |    |    |    | 0h                    |

**Table 3-2507. CONTROLSS\_INPUTXBAR18\_GSEL Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                  |
|------|-----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED              | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR18_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.56 CONTROLSS\_INPUTXBAR18\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR18\_G0 Register (Offset = 584h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2508. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0584h       |

**Figure 3-813. CONTROLSS\_INPUTXBAR18\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR18_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-2510. CONTROLSS\_INPUTXBAR18\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                      |
|------|--------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED           | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR18_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.57 CONTROLSS\_INPUTXBAR18\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR18\_G1 Register (Offset = 588h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2511. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0588h       |

**Figure 3-814. CONTROLSS\_INPUTXBAR18\_G1 Name Register**

|          |    |    |    |                    |    |    |    |
|----------|----|----|----|--------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 23       | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 15       | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 7        | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR18_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W                |    |    |    |
| 0h       |    |    |    | 0h                 |    |    |    |

**Table 3-2513. CONTROLSS\_INPUTXBAR18\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                        |
|------|--------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED           | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR18_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

### 3.15.2.58 CONTROLSS\_INPUTXBAR19\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR19\_GSEL Register (Offset = 5C0h) [reset = 0h]

INPUT XBAR19 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2514. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 05C0h       |

**Figure 3-815. CONTROLSS\_INPUTXBAR19\_GSEL Name Register**

|          |    |    |    |    |    |    |                       |
|----------|----|----|----|----|----|----|-----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                     |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                     |
| RESERVED |    |    |    |    |    |    | INPUTXBAR19_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                   |
| 0h       |    |    |    |    |    |    | 0h                    |

**Table 3-2516. CONTROLSS\_INPUTXBAR19\_GSEL Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                  |
|------|-----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED              | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR19_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.59 CONTROLSS\_INPUTXBAR19\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR19\_G0 Register (Offset = 5C4h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2517. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 05C4h       |

**Figure 3-816. CONTROLSS\_INPUTXBAR19\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR19_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-2519. CONTROLSS\_INPUTXBAR19\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                      |
|------|--------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED           | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR19_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.60 CONTROLSS\_INPUTXBAR19\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR19\_G1 Register (Offset = 5C8h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2520. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 05C8h       |

**Figure 3-817. CONTROLSS\_INPUTXBAR19\_G1 Name Register**

|          |    |    |    |                    |    |    |    |
|----------|----|----|----|--------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 23       | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 15       | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 7        | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR19_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W                |    |    |    |
| 0h       |    |    |    | 0h                 |    |    |    |

**Table 3-2522. CONTROLSS\_INPUTXBAR19\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                        |
|------|--------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED           | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR19_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

### 3.15.2.61 CONTROLSS\_INPUTXBAR20\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR20\_GSEL Register (Offset = 600h) [reset = 0h]

INPUT XBAR20 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2523. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0600h       |

**Figure 3-818. CONTROLSS\_INPUTXBAR20\_GSEL Name Register**

|          |    |    |    |    |    |    |                       |
|----------|----|----|----|----|----|----|-----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                     |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                     |
| RESERVED |    |    |    |    |    |    | INPUTXBAR20_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                   |
| 0h       |    |    |    |    |    |    | 0h                    |

**Table 3-2525. CONTROLSS\_INPUTXBAR20\_GSEL Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                  |
|------|-----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED              | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR20_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |



### 3.15.2.62 CONTROLSS\_INPUTXBAR20\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR20\_G0 Register (Offset = 604h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2526. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0604h       |

**Figure 3-819. CONTROLSS\_INPUTXBAR20\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR20_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-2528. CONTROLSS\_INPUTXBAR20\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                      |
|------|--------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED           | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR20_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.63 CONTROLSS\_INPUTXBAR20\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR20\_G1 Register (Offset = 608h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2529. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0608h       |

**Figure 3-820. CONTROLSS\_INPUTXBAR20\_G1 Name Register**

|          |    |    |                    |    |    |    |    |
|----------|----|----|--------------------|----|----|----|----|
| 31       | 30 | 29 | 28                 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |                    |    |    |    |    |
| NONE     |    |    |                    |    |    |    |    |
| 0h       |    |    |                    |    |    |    |    |
| 23       | 22 | 21 | 20                 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |                    |    |    |    |    |
| NONE     |    |    |                    |    |    |    |    |
| 0h       |    |    |                    |    |    |    |    |
| 15       | 14 | 13 | 12                 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |                    |    |    |    |    |
| NONE     |    |    |                    |    |    |    |    |
| 0h       |    |    |                    |    |    |    |    |
| 7        | 6  | 5  | 4                  | 3  | 2  | 1  | 0  |
| RESERVED |    |    | INPUTXBAR20_G1_SEL |    |    |    |    |
| NONE     |    |    | R/W                |    |    |    |    |
| 0h       |    |    | 0h                 |    |    |    |    |

**Table 3-2531. CONTROLSS\_INPUTXBAR20\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                        |
|------|--------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED           | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR20_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

### 3.15.2.64 CONTROLSS\_INPUTXBAR21\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR21\_GSEL Register (Offset = 640h) [reset = 0h]

INPUT XBAR21 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2532. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0640h       |

**Figure 3-821. CONTROLSS\_INPUTXBAR21\_GSEL Name Register**

|          |    |    |    |    |    |    |                       |
|----------|----|----|----|----|----|----|-----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                     |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                     |
| RESERVED |    |    |    |    |    |    | INPUTXBAR21_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                   |
| 0h       |    |    |    |    |    |    | 0h                    |

**Table 3-2534. CONTROLSS\_INPUTXBAR21\_GSEL Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                  |
|------|-----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED              | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR21_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.65 CONTROLSS\_INPUTXBAR21\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR21\_G0 Register (Offset = 644h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2535. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0644h       |

**Figure 3-822. CONTROLSS\_INPUTXBAR21\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR21_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-2537. CONTROLSS\_INPUTXBAR21\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                      |
|------|--------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED           | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR21_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.66 CONTROLSS\_INPUTXBAR21\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR21\_G1 Register (Offset = 648h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2538. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0648h       |

**Figure 3-823. CONTROLSS\_INPUTXBAR21\_G1 Name Register**

|          |    |    |    |                    |    |    |    |
|----------|----|----|----|--------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 23       | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 15       | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 7        | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR21_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W                |    |    |    |
| 0h       |    |    |    | 0h                 |    |    |    |

**Table 3-2540. CONTROLSS\_INPUTXBAR21\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                        |
|------|--------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED           | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR21_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

### 3.15.2.67 CONTROLSS\_INPUTXBAR22\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR22\_GSEL Register (Offset = 680h) [reset = 0h]

INPUT XBAR22 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2541. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0680h       |

**Figure 3-824. CONTROLSS\_INPUTXBAR22\_GSEL Name Register**

|          |    |    |    |    |    |    |                       |
|----------|----|----|----|----|----|----|-----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                     |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                     |
| RESERVED |    |    |    |    |    |    | INPUTXBAR22_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                   |
| 0h       |    |    |    |    |    |    | 0h                    |

**Table 3-2543. CONTROLSS\_INPUTXBAR22\_GSEL Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                  |
|------|-----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED              | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR22_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.68 CONTROLSS\_INPUTXBAR22\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR22\_G0 Register (Offset = 684h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2544. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0684h       |

**Figure 3-825. CONTROLSS\_INPUTXBAR22\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR22_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-2546. CONTROLSS\_INPUTXBAR22\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                      |
|------|--------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED           | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR22_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.69 CONTROLSS\_INPUTXBAR22\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR22\_G1 Register (Offset = 688h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2547. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0688h       |

**Figure 3-826. CONTROLSS\_INPUTXBAR22\_G1 Name Register**

|          |    |    |    |                    |    |    |    |
|----------|----|----|----|--------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 23       | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 15       | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 7        | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR22_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W                |    |    |    |
| 0h       |    |    |    | 0h                 |    |    |    |

**Table 3-2549. CONTROLSS\_INPUTXBAR22\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                        |
|------|--------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED           | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR22_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |



### 3.15.2.70 CONTROLSS\_INPUTXBAR23\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR23\_GSEL Register (Offset = 6C0h) [reset = 0h]

INPUT XBAR23 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2550. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 06C0h       |

**Figure 3-827. CONTROLSS\_INPUTXBAR23\_GSEL Name Register**

|          |    |    |    |    |    |    |                       |
|----------|----|----|----|----|----|----|-----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                     |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                     |
| RESERVED |    |    |    |    |    |    | INPUTXBAR23_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                   |
| 0h       |    |    |    |    |    |    | 0h                    |

**Table 3-2552. CONTROLSS\_INPUTXBAR23\_GSEL Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                  |
|------|-----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED              | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR23_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.71 CONTROLSS\_INPUTXBAR23\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR23\_G0 Register (Offset = 6C4h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2553. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 06C4h       |

**Figure 3-828. CONTROLSS\_INPUTXBAR23\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR23_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-2555. CONTROLSS\_INPUTXBAR23\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                      |
|------|--------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED           | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR23_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.72 CONTROLSS\_INPUTXBAR23\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR23\_G1 Register (Offset = 6C8h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2556. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 06C8h       |

**Figure 3-829. CONTROLSS\_INPUTXBAR23\_G1 Name Register**

|          |    |    |    |                    |    |    |    |
|----------|----|----|----|--------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 23       | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 15       | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 7        | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR23_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W                |    |    |    |
| 0h       |    |    |    | 0h                 |    |    |    |

**Table 3-2558. CONTROLSS\_INPUTXBAR23\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                        |
|------|--------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED           | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR23_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

### 3.15.2.73 CONTROLSS\_INPUTXBAR24\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR24\_GSEL Register (Offset = 700h) [reset = 0h]

INPUT XBAR24 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2559. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0700h       |

**Figure 3-830. CONTROLSS\_INPUTXBAR24\_GSEL Name Register**

|          |    |    |    |    |    |    |                       |
|----------|----|----|----|----|----|----|-----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                     |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                     |
| RESERVED |    |    |    |    |    |    | INPUTXBAR24_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                   |
| 0h       |    |    |    |    |    |    | 0h                    |

**Table 3-2561. CONTROLSS\_INPUTXBAR24\_GSEL Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                  |
|------|-----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED              | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR24_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.74 CONTROLSS\_INPUTXBAR24\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR24\_G0 Register (Offset = 704h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2562. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0704h       |

**Figure 3-831. CONTROLSS\_INPUTXBAR24\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR24_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-2564. CONTROLSS\_INPUTXBAR24\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                      |
|------|--------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED           | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR24_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.75 CONTROLSS\_INPUTXBAR24\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR24\_G1 Register (Offset = 708h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2565. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0708h       |

**Figure 3-832. CONTROLSS\_INPUTXBAR24\_G1 Name Register**

|          |    |    |    |                    |    |    |    |
|----------|----|----|----|--------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 23       | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 15       | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 7        | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR24_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W                |    |    |    |
| 0h       |    |    |    | 0h                 |    |    |    |

**Table 3-2567. CONTROLSS\_INPUTXBAR24\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                        |
|------|--------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED           | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR24_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

### 3.15.2.76 CONTROLSS\_INPUTXBAR25\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR25\_GSEL Register (Offset = 740h) [reset = 0h]

INPUT XBAR25 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2568. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0740h       |

**Figure 3-833. CONTROLSS\_INPUTXBAR25\_GSEL Name Register**

|          |    |    |    |    |    |    |                       |
|----------|----|----|----|----|----|----|-----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                     |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                     |
| RESERVED |    |    |    |    |    |    | INPUTXBAR25_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                   |
| 0h       |    |    |    |    |    |    | 0h                    |

**Table 3-2570. CONTROLSS\_INPUTXBAR25\_GSEL Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                  |
|------|-----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED              | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR25_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.77 CONTROLSS\_INPUTXBAR25\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR25\_G0 Register (Offset = 744h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2571. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0744h       |

**Figure 3-834. CONTROLSS\_INPUTXBAR25\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR25_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-2573. CONTROLSS\_INPUTXBAR25\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                      |
|------|--------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED           | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR25_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |



### 3.15.2.78 CONTROLSS\_INPUTXBAR25\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR25\_G1 Register (Offset = 748h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2574. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0748h       |

**Figure 3-835. CONTROLSS\_INPUTXBAR25\_G1 Name Register**

|          |    |    |    |                    |    |    |    |
|----------|----|----|----|--------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 23       | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 15       | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 7        | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR25_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W                |    |    |    |
| 0h       |    |    |    | 0h                 |    |    |    |

**Table 3-2576. CONTROLSS\_INPUTXBAR25\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                        |
|------|--------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED           | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR25_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

### 3.15.2.79 CONTROLSS\_INPUTXBAR26\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR26\_GSEL Register (Offset = 780h) [reset = 0h]

INPUT XBAR26 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2577. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0780h       |

**Figure 3-836. CONTROLSS\_INPUTXBAR26\_GSEL Name Register**

|          |    |    |    |    |    |    |                       |
|----------|----|----|----|----|----|----|-----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                     |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                     |
| RESERVED |    |    |    |    |    |    | INPUTXBAR26_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                   |
| 0h       |    |    |    |    |    |    | 0h                    |

**Table 3-2579. CONTROLSS\_INPUTXBAR26\_GSEL Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                  |
|------|-----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED              | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR26_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.80 CONTROLSS\_INPUTXBAR26\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR26\_G0 Register (Offset = 784h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2580. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0784h       |

**Figure 3-837. CONTROLSS\_INPUTXBAR26\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR26_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-2582. CONTROLSS\_INPUTXBAR26\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                      |
|------|--------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED           | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR26_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.81 CONTROLSS\_INPUTXBAR26\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR26\_G1 Register (Offset = 788h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2583. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0788h       |

**Figure 3-838. CONTROLSS\_INPUTXBAR26\_G1 Name Register**

|          |    |    |    |                    |    |    |    |
|----------|----|----|----|--------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 23       | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 15       | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 7        | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR26_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W                |    |    |    |
| 0h       |    |    |    | 0h                 |    |    |    |

**Table 3-2585. CONTROLSS\_INPUTXBAR26\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                        |
|------|--------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED           | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR26_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

### 3.15.2.82 CONTROLSS\_INPUTXBAR27\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR27\_GSEL Register (Offset = 7C0h) [reset = 0h]

INPUT XBAR27 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2586. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 07C0h       |

**Figure 3-839. CONTROLSS\_INPUTXBAR27\_GSEL Name Register**

|          |    |    |    |    |    |    |                       |
|----------|----|----|----|----|----|----|-----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                     |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                     |
| RESERVED |    |    |    |    |    |    | INPUTXBAR27_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                   |
| 0h       |    |    |    |    |    |    | 0h                    |

**Table 3-2588. CONTROLSS\_INPUTXBAR27\_GSEL Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                  |
|------|-----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED              | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR27_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.83 CONTROLSS\_INPUTXBAR27\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR27\_G0 Register (Offset = 7C4h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2589. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 07C4h       |

**Figure 3-840. CONTROLSS\_INPUTXBAR27\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR27_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-2591. CONTROLSS\_INPUTXBAR27\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                      |
|------|--------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED           | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR27_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.84 CONTROLSS\_INPUTXBAR27\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR27\_G1 Register (Offset = 7C8h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2592. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 07C8h       |

**Figure 3-841. CONTROLSS\_INPUTXBAR27\_G1 Name Register**

|          |    |    |    |                    |    |    |    |
|----------|----|----|----|--------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 23       | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 15       | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 7        | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR27_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W                |    |    |    |
| 0h       |    |    |    | 0h                 |    |    |    |

**Table 3-2594. CONTROLSS\_INPUTXBAR27\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                        |
|------|--------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED           | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR27_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

### 3.15.2.85 CONTROLSS\_INPUTXBAR28\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR28\_GSEL Register (Offset = 800h) [reset = 0h]

INPUT XBAR28 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2595. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0800h       |

**Figure 3-842. CONTROLSS\_INPUTXBAR28\_GSEL Name Register**

|          |    |    |    |    |    |    |                       |
|----------|----|----|----|----|----|----|-----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                     |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                     |
| RESERVED |    |    |    |    |    |    | INPUTXBAR28_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                   |
| 0h       |    |    |    |    |    |    | 0h                    |

**Table 3-2597. CONTROLSS\_INPUTXBAR28\_GSEL Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                  |
|------|-----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED              | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR28_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |



### 3.15.2.86 CONTROLSS\_INPUTXBAR28\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR28\_G0 Register (Offset = 804h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2598. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0804h       |

**Figure 3-843. CONTROLSS\_INPUTXBAR28\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR28_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-2600. CONTROLSS\_INPUTXBAR28\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                      |
|------|--------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED           | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR28_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.87 CONTROLSS\_INPUTXBAR28\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR28\_G1 Register (Offset = 808h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2601. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0808h       |

**Figure 3-844. CONTROLSS\_INPUTXBAR28\_G1 Name Register**

|          |    |    |    |                    |    |    |    |
|----------|----|----|----|--------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 23       | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 15       | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 7        | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR28_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W                |    |    |    |
| 0h       |    |    |    | 0h                 |    |    |    |

**Table 3-2603. CONTROLSS\_INPUTXBAR28\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                        |
|------|--------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED           | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR28_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

### 3.15.2.88 CONTROLSS\_INPUTXBAR29\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR29\_GSEL Register (Offset = 840h) [reset = 0h]

INPUT XBAR29 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2604. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0840h       |

**Figure 3-845. CONTROLSS\_INPUTXBAR29\_GSEL Name Register**

|          |    |    |    |    |    |    |                       |
|----------|----|----|----|----|----|----|-----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                     |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                     |
| RESERVED |    |    |    |    |    |    | INPUTXBAR29_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                   |
| 0h       |    |    |    |    |    |    | 0h                    |

**Table 3-2606. CONTROLSS\_INPUTXBAR29\_GSEL Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                  |
|------|-----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED              | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR29_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.89 CONTROLSS\_INPUTXBAR29\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR29\_G0 Register (Offset = 844h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2607. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0844h       |

**Figure 3-846. CONTROLSS\_INPUTXBAR29\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR29_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-2609. CONTROLSS\_INPUTXBAR29\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                      |
|------|--------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED           | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR29_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.90 CONTROLSS\_INPUTXBAR29\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR29\_G1 Register (Offset = 848h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2610. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0848h       |

**Figure 3-847. CONTROLSS\_INPUTXBAR29\_G1 Name Register**

|          |    |    |    |                    |    |    |    |
|----------|----|----|----|--------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 23       | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 15       | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 7        | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR29_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W                |    |    |    |
| 0h       |    |    |    | 0h                 |    |    |    |

**Table 3-2612. CONTROLSS\_INPUTXBAR29\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                        |
|------|--------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED           | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR29_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

### 3.15.2.91 CONTROLSS\_INPUTXBAR30\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR30\_GSEL Register (Offset = 880h) [reset = 0h]

INPUT XBAR30 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2613. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0880h       |

**Figure 3-848. CONTROLSS\_INPUTXBAR30\_GSEL Name Register**

|          |    |    |    |    |    |    |                       |
|----------|----|----|----|----|----|----|-----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                     |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                     |
| RESERVED |    |    |    |    |    |    | INPUTXBAR30_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                   |
| 0h       |    |    |    |    |    |    | 0h                    |

**Table 3-2615. CONTROLSS\_INPUTXBAR30\_GSEL Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                  |
|------|-----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED              | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR30_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.92 CONTROLSS\_INPUTXBAR30\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR30\_G0 Register (Offset = 884h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2616. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0884h       |

**Figure 3-849. CONTROLSS\_INPUTXBAR30\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR30_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-2618. CONTROLSS\_INPUTXBAR30\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                      |
|------|--------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED           | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR30_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.93 CONTROLSS\_INPUTXBAR30\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR30\_G1 Register (Offset = 888h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2619. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 0888h       |

**Figure 3-850. CONTROLSS\_INPUTXBAR30\_G1 Name Register**

|          |    |    |    |                    |    |    |    |
|----------|----|----|----|--------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 23       | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 15       | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 7        | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR30_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W                |    |    |    |
| 0h       |    |    |    | 0h                 |    |    |    |

**Table 3-2621. CONTROLSS\_INPUTXBAR30\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                        |
|------|--------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED           | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR30_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |



### 3.15.2.94 CONTROLSS\_INPUTXBAR31\_GSEL Register

#### 1 CONTROLSS\_INPUTXBAR31\_GSEL Register (Offset = 8C0h) [reset = 0h]

INPUT XBAR31 Input Select

0 : GPI

1: ICSS GPO port.

Return to [Summary Table](#)

**Table 3-2622. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 08C0h       |

**Figure 3-851. CONTROLSS\_INPUTXBAR31\_GSEL Name Register**

|          |    |    |    |    |    |    |                       |
|----------|----|----|----|----|----|----|-----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                    |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                     |
| RESERVED |    |    |    |    |    |    |                       |
| NONE     |    |    |    |    |    |    |                       |
| 0h       |    |    |    |    |    |    |                       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                     |
| RESERVED |    |    |    |    |    |    | INPUTXBAR31_GSEL_GSEL |
| NONE     |    |    |    |    |    |    | R/W                   |
| 0h       |    |    |    |    |    |    | 0h                    |

**Table 3-2624. CONTROLSS\_INPUTXBAR31\_GSEL Register Field Descriptions**

| Bit  | Field                 | Type | Reset | Description                                                  |
|------|-----------------------|------|-------|--------------------------------------------------------------|
| 31:1 | RESERVED              | NONE | 0h    | Reserved                                                     |
| 0    | INPUTXBAR31_GSEL_GSEL | R/W  | 0h    | Select input source Group:<br>0 G0 selected<br>1 G1 selected |

### 3.15.2.95 CONTROLSS\_INPUTXBAR31\_G0 Register

#### 1 CONTROLSS\_INPUTXBAR31\_G0 Register (Offset = 8C4h) [reset = 0h]

Input GPI XBAR selection - valid inputs are GPI[143:0].

Return to [Summary Table](#)

**Table 3-2625. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 08C4h       |

**Figure 3-852. CONTROLSS\_INPUTXBAR31\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INPUTXBAR31_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-2627. CONTROLSS\_INPUTXBAR31\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                      |
|------|--------------------|------|-------|------------------------------------------------------------------|
| 31:8 | RESERVED           | NONE | 0h    | Reserved                                                         |
| 7:0  | INPUTXBAR31_G0_SEL | R/W  | 0h    | Select input source:<br>0 G0.0 selected<br>..<br>x G0.x selected |

### 3.15.2.96 CONTROLSS\_INPUTXBAR31\_G1 Register

#### 1 CONTROLSS\_INPUTXBAR31\_G1 Register (Offset = 8C8h) [reset = 0h]

ICSS GPO port selection - ICSS GPO[31:0].

Return to [Summary Table](#)

**Table 3-2628. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| CONTROLSS_INPUTXBAR | 502D 08C8h       |

**Figure 3-853. CONTROLSS\_INPUTXBAR31\_G1 Name Register**

|          |    |    |    |                    |    |    |    |
|----------|----|----|----|--------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 23       | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 15       | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED |    |    |    |                    |    |    |    |
| NONE     |    |    |    |                    |    |    |    |
| 0h       |    |    |    |                    |    |    |    |
| 7        | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| RESERVED |    |    |    | INPUTXBAR31_G1_SEL |    |    |    |
| NONE     |    |    |    | R/W                |    |    |    |
| 0h       |    |    |    | 0h                 |    |    |    |

**Table 3-2630. CONTROLSS\_INPUTXBAR31\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                        |
|------|--------------------|------|-------|--------------------------------------------------------------------|
| 31:5 | RESERVED           | NONE | 0h    | Reserved                                                           |
| 4:0  | INPUTXBAR31_G1_SEL | R/W  | 0h    | Select input source:<br>0 G1.0 selected<br>..<br>31 G1.31 selected |

## 3.16 CONTROLSS\_INTXBAR

### CONTROLSS\_INTXBAR

#### 3.16.1 CONTROLSS\_INTXBAR Summaries

#### CONTROLSS\_INTXBAR Summaries

**Table 3-2631. CONTROLSS Registers, Base Address=502D 5000h, Length=2048**

| Offset | Length | Register Name                         | CONTROLSS_INTXBAR Physical Address |
|--------|--------|---------------------------------------|------------------------------------|
| 100h   | 32     | <a href="#">CONTROLSS_INTXBAR0_G0</a> | 502D 5100h                         |
| 104h   | 32     | <a href="#">CONTROLSS_INTXBAR0_G1</a> | 502D 5104h                         |
| 108h   | 32     | <a href="#">CONTROLSS_INTXBAR0_G2</a> | 502D 5108h                         |
| 10Ch   | 32     | <a href="#">CONTROLSS_INTXBAR0_G3</a> | 502D 510Ch                         |
| 110h   | 32     | <a href="#">CONTROLSS_INTXBAR0_G4</a> | 502D 5110h                         |
| 114h   | 32     | <a href="#">CONTROLSS_INTXBAR0_G5</a> | 502D 5114h                         |
| 118h   | 32     | <a href="#">CONTROLSS_INTXBAR0_G6</a> | 502D 5118h                         |
| 140h   | 32     | <a href="#">CONTROLSS_INTXBAR1_G0</a> | 502D 5140h                         |
| 144h   | 32     | <a href="#">CONTROLSS_INTXBAR1_G1</a> | 502D 5144h                         |
| 148h   | 32     | <a href="#">CONTROLSS_INTXBAR1_G2</a> | 502D 5148h                         |
| 14Ch   | 32     | <a href="#">CONTROLSS_INTXBAR1_G3</a> | 502D 514Ch                         |
| 150h   | 32     | <a href="#">CONTROLSS_INTXBAR1_G4</a> | 502D 5150h                         |
| 154h   | 32     | <a href="#">CONTROLSS_INTXBAR1_G5</a> | 502D 5154h                         |
| 158h   | 32     | <a href="#">CONTROLSS_INTXBAR1_G6</a> | 502D 5158h                         |
| 180h   | 32     | <a href="#">CONTROLSS_INTXBAR2_G0</a> | 502D 5180h                         |
| 184h   | 32     | <a href="#">CONTROLSS_INTXBAR2_G1</a> | 502D 5184h                         |
| 188h   | 32     | <a href="#">CONTROLSS_INTXBAR2_G2</a> | 502D 5188h                         |
| 18Ch   | 32     | <a href="#">CONTROLSS_INTXBAR2_G3</a> | 502D 518Ch                         |
| 190h   | 32     | <a href="#">CONTROLSS_INTXBAR2_G4</a> | 502D 5190h                         |
| 194h   | 32     | <a href="#">CONTROLSS_INTXBAR2_G5</a> | 502D 5194h                         |
| 198h   | 32     | <a href="#">CONTROLSS_INTXBAR2_G6</a> | 502D 5198h                         |
| 1C0h   | 32     | <a href="#">CONTROLSS_INTXBAR3_G0</a> | 502D 51C0h                         |
| 1C4h   | 32     | <a href="#">CONTROLSS_INTXBAR3_G1</a> | 502D 51C4h                         |
| 1C8h   | 32     | <a href="#">CONTROLSS_INTXBAR3_G2</a> | 502D 51C8h                         |
| 1CCh   | 32     | <a href="#">CONTROLSS_INTXBAR3_G3</a> | 502D 51CCh                         |
| 1D0h   | 32     | <a href="#">CONTROLSS_INTXBAR3_G4</a> | 502D 51D0h                         |
| 1D4h   | 32     | <a href="#">CONTROLSS_INTXBAR3_G5</a> | 502D 51D4h                         |
| 1D8h   | 32     | <a href="#">CONTROLSS_INTXBAR3_G6</a> | 502D 51D8h                         |
| 200h   | 32     | <a href="#">CONTROLSS_INTXBAR4_G0</a> | 502D 5200h                         |
| 204h   | 32     | <a href="#">CONTROLSS_INTXBAR4_G1</a> | 502D 5204h                         |
| 208h   | 32     | <a href="#">CONTROLSS_INTXBAR4_G2</a> | 502D 5208h                         |
| 20Ch   | 32     | <a href="#">CONTROLSS_INTXBAR4_G3</a> | 502D 520Ch                         |
| 210h   | 32     | <a href="#">CONTROLSS_INTXBAR4_G4</a> | 502D 5210h                         |
| 214h   | 32     | <a href="#">CONTROLSS_INTXBAR4_G5</a> | 502D 5214h                         |
| 218h   | 32     | <a href="#">CONTROLSS_INTXBAR4_G6</a> | 502D 5218h                         |
| 240h   | 32     | <a href="#">CONTROLSS_INTXBAR5_G0</a> | 502D 5240h                         |
| 244h   | 32     | <a href="#">CONTROLSS_INTXBAR5_G1</a> | 502D 5244h                         |

**Table 3-2631. CONTROLSS Registers, Base Address=502D 5000h, Length=2048 (continued)**

| Offset | Length | Register Name                          | CONTROLSS_INTXBAR Physical Address |
|--------|--------|----------------------------------------|------------------------------------|
| 248h   | 32     | <a href="#">CONTROLSS_INTXBAR5_G2</a>  | 502D 5248h                         |
| 24Ch   | 32     | <a href="#">CONTROLSS_INTXBAR5_G3</a>  | 502D 524Ch                         |
| 250h   | 32     | <a href="#">CONTROLSS_INTXBAR5_G4</a>  | 502D 5250h                         |
| 254h   | 32     | <a href="#">CONTROLSS_INTXBAR5_G5</a>  | 502D 5254h                         |
| 258h   | 32     | <a href="#">CONTROLSS_INTXBAR5_G6</a>  | 502D 5258h                         |
| 280h   | 32     | <a href="#">CONTROLSS_INTXBAR6_G0</a>  | 502D 5280h                         |
| 284h   | 32     | <a href="#">CONTROLSS_INTXBAR6_G1</a>  | 502D 5284h                         |
| 288h   | 32     | <a href="#">CONTROLSS_INTXBAR6_G2</a>  | 502D 5288h                         |
| 28Ch   | 32     | <a href="#">CONTROLSS_INTXBAR6_G3</a>  | 502D 528Ch                         |
| 290h   | 32     | <a href="#">CONTROLSS_INTXBAR6_G4</a>  | 502D 5290h                         |
| 294h   | 32     | <a href="#">CONTROLSS_INTXBAR6_G5</a>  | 502D 5294h                         |
| 298h   | 32     | <a href="#">CONTROLSS_INTXBAR6_G6</a>  | 502D 5298h                         |
| 2C0h   | 32     | <a href="#">CONTROLSS_INTXBAR7_G0</a>  | 502D 52C0h                         |
| 2C4h   | 32     | <a href="#">CONTROLSS_INTXBAR7_G1</a>  | 502D 52C4h                         |
| 2C8h   | 32     | <a href="#">CONTROLSS_INTXBAR7_G2</a>  | 502D 52C8h                         |
| 2CCh   | 32     | <a href="#">CONTROLSS_INTXBAR7_G3</a>  | 502D 52CCh                         |
| 2D0h   | 32     | <a href="#">CONTROLSS_INTXBAR7_G4</a>  | 502D 52D0h                         |
| 2D4h   | 32     | <a href="#">CONTROLSS_INTXBAR7_G5</a>  | 502D 52D4h                         |
| 2D8h   | 32     | <a href="#">CONTROLSS_INTXBAR7_G6</a>  | 502D 52D8h                         |
| 300h   | 32     | <a href="#">CONTROLSS_INTXBAR8_G0</a>  | 502D 5300h                         |
| 304h   | 32     | <a href="#">CONTROLSS_INTXBAR8_G1</a>  | 502D 5304h                         |
| 308h   | 32     | <a href="#">CONTROLSS_INTXBAR8_G2</a>  | 502D 5308h                         |
| 30Ch   | 32     | <a href="#">CONTROLSS_INTXBAR8_G3</a>  | 502D 530Ch                         |
| 310h   | 32     | <a href="#">CONTROLSS_INTXBAR8_G4</a>  | 502D 5310h                         |
| 314h   | 32     | <a href="#">CONTROLSS_INTXBAR8_G5</a>  | 502D 5314h                         |
| 318h   | 32     | <a href="#">CONTROLSS_INTXBAR8_G6</a>  | 502D 5318h                         |
| 340h   | 32     | <a href="#">CONTROLSS_INTXBAR9_G0</a>  | 502D 5340h                         |
| 344h   | 32     | <a href="#">CONTROLSS_INTXBAR9_G1</a>  | 502D 5344h                         |
| 348h   | 32     | <a href="#">CONTROLSS_INTXBAR9_G2</a>  | 502D 5348h                         |
| 34Ch   | 32     | <a href="#">CONTROLSS_INTXBAR9_G3</a>  | 502D 534Ch                         |
| 350h   | 32     | <a href="#">CONTROLSS_INTXBAR9_G4</a>  | 502D 5350h                         |
| 354h   | 32     | <a href="#">CONTROLSS_INTXBAR9_G5</a>  | 502D 5354h                         |
| 358h   | 32     | <a href="#">CONTROLSS_INTXBAR9_G6</a>  | 502D 5358h                         |
| 380h   | 32     | <a href="#">CONTROLSS_INTXBAR10_G0</a> | 502D 5380h                         |
| 384h   | 32     | <a href="#">CONTROLSS_INTXBAR10_G1</a> | 502D 5384h                         |
| 388h   | 32     | <a href="#">CONTROLSS_INTXBAR10_G2</a> | 502D 5388h                         |
| 38Ch   | 32     | <a href="#">CONTROLSS_INTXBAR10_G3</a> | 502D 538Ch                         |
| 390h   | 32     | <a href="#">CONTROLSS_INTXBAR10_G4</a> | 502D 5390h                         |
| 394h   | 32     | <a href="#">CONTROLSS_INTXBAR10_G5</a> | 502D 5394h                         |
| 398h   | 32     | <a href="#">CONTROLSS_INTXBAR10_G6</a> | 502D 5398h                         |
| 3C0h   | 32     | <a href="#">CONTROLSS_INTXBAR11_G0</a> | 502D 53C0h                         |
| 3C4h   | 32     | <a href="#">CONTROLSS_INTXBAR11_G1</a> | 502D 53C4h                         |
| 3C8h   | 32     | <a href="#">CONTROLSS_INTXBAR11_G2</a> | 502D 53C8h                         |
| 3CCh   | 32     | <a href="#">CONTROLSS_INTXBAR11_G3</a> | 502D 53CCh                         |

**Table 3-2631. CONTROLSS Registers, Base Address=502D 5000h, Length=2048 (continued)**

| Offset | Length | Register Name                          | CONTROLSS_INTXBAR Physical Address |
|--------|--------|----------------------------------------|------------------------------------|
| 3D0h   | 32     | <a href="#">CONTROLSS_INTXBAR11_G4</a> | 502D 53D0h                         |
| 3D4h   | 32     | <a href="#">CONTROLSS_INTXBAR11_G5</a> | 502D 53D4h                         |
| 3D8h   | 32     | <a href="#">CONTROLSS_INTXBAR11_G6</a> | 502D 53D8h                         |
| 400h   | 32     | <a href="#">CONTROLSS_INTXBAR12_G0</a> | 502D 5400h                         |
| 404h   | 32     | <a href="#">CONTROLSS_INTXBAR12_G1</a> | 502D 5404h                         |
| 408h   | 32     | <a href="#">CONTROLSS_INTXBAR12_G2</a> | 502D 5408h                         |
| 40Ch   | 32     | <a href="#">CONTROLSS_INTXBAR12_G3</a> | 502D 540Ch                         |
| 410h   | 32     | <a href="#">CONTROLSS_INTXBAR12_G4</a> | 502D 5410h                         |
| 414h   | 32     | <a href="#">CONTROLSS_INTXBAR12_G5</a> | 502D 5414h                         |
| 418h   | 32     | <a href="#">CONTROLSS_INTXBAR12_G6</a> | 502D 5418h                         |
| 440h   | 32     | <a href="#">CONTROLSS_INTXBAR13_G0</a> | 502D 5440h                         |
| 444h   | 32     | <a href="#">CONTROLSS_INTXBAR13_G1</a> | 502D 5444h                         |
| 448h   | 32     | <a href="#">CONTROLSS_INTXBAR13_G2</a> | 502D 5448h                         |
| 44Ch   | 32     | <a href="#">CONTROLSS_INTXBAR13_G3</a> | 502D 544Ch                         |
| 450h   | 32     | <a href="#">CONTROLSS_INTXBAR13_G4</a> | 502D 5450h                         |
| 454h   | 32     | <a href="#">CONTROLSS_INTXBAR13_G5</a> | 502D 5454h                         |
| 458h   | 32     | <a href="#">CONTROLSS_INTXBAR13_G6</a> | 502D 5458h                         |
| 480h   | 32     | <a href="#">CONTROLSS_INTXBAR14_G0</a> | 502D 5480h                         |
| 484h   | 32     | <a href="#">CONTROLSS_INTXBAR14_G1</a> | 502D 5484h                         |
| 488h   | 32     | <a href="#">CONTROLSS_INTXBAR14_G2</a> | 502D 5488h                         |
| 48Ch   | 32     | <a href="#">CONTROLSS_INTXBAR14_G3</a> | 502D 548Ch                         |
| 490h   | 32     | <a href="#">CONTROLSS_INTXBAR14_G4</a> | 502D 5490h                         |
| 494h   | 32     | <a href="#">CONTROLSS_INTXBAR14_G5</a> | 502D 5494h                         |
| 498h   | 32     | <a href="#">CONTROLSS_INTXBAR14_G6</a> | 502D 5498h                         |
| 4C0h   | 32     | <a href="#">CONTROLSS_INTXBAR15_G0</a> | 502D 54C0h                         |
| 4C4h   | 32     | <a href="#">CONTROLSS_INTXBAR15_G1</a> | 502D 54C4h                         |
| 4C8h   | 32     | <a href="#">CONTROLSS_INTXBAR15_G2</a> | 502D 54C8h                         |
| 4CCh   | 32     | <a href="#">CONTROLSS_INTXBAR15_G3</a> | 502D 54CCh                         |
| 4D0h   | 32     | <a href="#">CONTROLSS_INTXBAR15_G4</a> | 502D 54D0h                         |
| 4D4h   | 32     | <a href="#">CONTROLSS_INTXBAR15_G5</a> | 502D 54D4h                         |
| 4D8h   | 32     | <a href="#">CONTROLSS_INTXBAR15_G6</a> | 502D 54D8h                         |
| 500h   | 32     | <a href="#">CONTROLSS_INTXBAR16_G0</a> | 502D 5500h                         |
| 504h   | 32     | <a href="#">CONTROLSS_INTXBAR16_G1</a> | 502D 5504h                         |
| 508h   | 32     | <a href="#">CONTROLSS_INTXBAR16_G2</a> | 502D 5508h                         |
| 50Ch   | 32     | <a href="#">CONTROLSS_INTXBAR16_G3</a> | 502D 550Ch                         |
| 510h   | 32     | <a href="#">CONTROLSS_INTXBAR16_G4</a> | 502D 5510h                         |
| 514h   | 32     | <a href="#">CONTROLSS_INTXBAR16_G5</a> | 502D 5514h                         |
| 518h   | 32     | <a href="#">CONTROLSS_INTXBAR16_G6</a> | 502D 5518h                         |
| 540h   | 32     | <a href="#">CONTROLSS_INTXBAR17_G0</a> | 502D 5540h                         |
| 544h   | 32     | <a href="#">CONTROLSS_INTXBAR17_G1</a> | 502D 5544h                         |
| 548h   | 32     | <a href="#">CONTROLSS_INTXBAR17_G2</a> | 502D 5548h                         |
| 54Ch   | 32     | <a href="#">CONTROLSS_INTXBAR17_G3</a> | 502D 554Ch                         |
| 550h   | 32     | <a href="#">CONTROLSS_INTXBAR17_G4</a> | 502D 5550h                         |
| 554h   | 32     | <a href="#">CONTROLSS_INTXBAR17_G5</a> | 502D 5554h                         |

**Table 3-2631. CONTROLSS Registers, Base Address=502D 5000h, Length=2048 (continued)**

| Offset | Length | Register Name                          | CONTROLSS_INTXBAR Physical Address |
|--------|--------|----------------------------------------|------------------------------------|
| 558h   | 32     | <a href="#">CONTROLSS_INTXBAR17_G6</a> | 502D 5558h                         |
| 580h   | 32     | <a href="#">CONTROLSS_INTXBAR18_G0</a> | 502D 5580h                         |
| 584h   | 32     | <a href="#">CONTROLSS_INTXBAR18_G1</a> | 502D 5584h                         |
| 588h   | 32     | <a href="#">CONTROLSS_INTXBAR18_G2</a> | 502D 5588h                         |
| 58Ch   | 32     | <a href="#">CONTROLSS_INTXBAR18_G3</a> | 502D 558Ch                         |
| 590h   | 32     | <a href="#">CONTROLSS_INTXBAR18_G4</a> | 502D 5590h                         |
| 594h   | 32     | <a href="#">CONTROLSS_INTXBAR18_G5</a> | 502D 5594h                         |
| 598h   | 32     | <a href="#">CONTROLSS_INTXBAR18_G6</a> | 502D 5598h                         |
| 5C0h   | 32     | <a href="#">CONTROLSS_INTXBAR19_G0</a> | 502D 55C0h                         |
| 5C4h   | 32     | <a href="#">CONTROLSS_INTXBAR19_G1</a> | 502D 55C4h                         |
| 5C8h   | 32     | <a href="#">CONTROLSS_INTXBAR19_G2</a> | 502D 55C8h                         |
| 5CCh   | 32     | <a href="#">CONTROLSS_INTXBAR19_G3</a> | 502D 55CCh                         |
| 5D0h   | 32     | <a href="#">CONTROLSS_INTXBAR19_G4</a> | 502D 55D0h                         |
| 5D4h   | 32     | <a href="#">CONTROLSS_INTXBAR19_G5</a> | 502D 55D4h                         |
| 5D8h   | 32     | <a href="#">CONTROLSS_INTXBAR19_G6</a> | 502D 55D8h                         |
| 600h   | 32     | <a href="#">CONTROLSS_INTXBAR20_G0</a> | 502D 5600h                         |
| 604h   | 32     | <a href="#">CONTROLSS_INTXBAR20_G1</a> | 502D 5604h                         |
| 608h   | 32     | <a href="#">CONTROLSS_INTXBAR20_G2</a> | 502D 5608h                         |
| 60Ch   | 32     | <a href="#">CONTROLSS_INTXBAR20_G3</a> | 502D 560Ch                         |
| 610h   | 32     | <a href="#">CONTROLSS_INTXBAR20_G4</a> | 502D 5610h                         |
| 614h   | 32     | <a href="#">CONTROLSS_INTXBAR20_G5</a> | 502D 5614h                         |
| 618h   | 32     | <a href="#">CONTROLSS_INTXBAR20_G6</a> | 502D 5618h                         |
| 640h   | 32     | <a href="#">CONTROLSS_INTXBAR21_G0</a> | 502D 5640h                         |
| 644h   | 32     | <a href="#">CONTROLSS_INTXBAR21_G1</a> | 502D 5644h                         |
| 648h   | 32     | <a href="#">CONTROLSS_INTXBAR21_G2</a> | 502D 5648h                         |
| 64Ch   | 32     | <a href="#">CONTROLSS_INTXBAR21_G3</a> | 502D 564Ch                         |
| 650h   | 32     | <a href="#">CONTROLSS_INTXBAR21_G4</a> | 502D 5650h                         |
| 654h   | 32     | <a href="#">CONTROLSS_INTXBAR21_G5</a> | 502D 5654h                         |
| 658h   | 32     | <a href="#">CONTROLSS_INTXBAR21_G6</a> | 502D 5658h                         |
| 680h   | 32     | <a href="#">CONTROLSS_INTXBAR22_G0</a> | 502D 5680h                         |
| 684h   | 32     | <a href="#">CONTROLSS_INTXBAR22_G1</a> | 502D 5684h                         |
| 688h   | 32     | <a href="#">CONTROLSS_INTXBAR22_G2</a> | 502D 5688h                         |
| 68Ch   | 32     | <a href="#">CONTROLSS_INTXBAR22_G3</a> | 502D 568Ch                         |
| 690h   | 32     | <a href="#">CONTROLSS_INTXBAR22_G4</a> | 502D 5690h                         |
| 694h   | 32     | <a href="#">CONTROLSS_INTXBAR22_G5</a> | 502D 5694h                         |
| 698h   | 32     | <a href="#">CONTROLSS_INTXBAR22_G6</a> | 502D 5698h                         |
| 6C0h   | 32     | <a href="#">CONTROLSS_INTXBAR23_G0</a> | 502D 56C0h                         |
| 6C4h   | 32     | <a href="#">CONTROLSS_INTXBAR23_G1</a> | 502D 56C4h                         |
| 6C8h   | 32     | <a href="#">CONTROLSS_INTXBAR23_G2</a> | 502D 56C8h                         |
| 6CCh   | 32     | <a href="#">CONTROLSS_INTXBAR23_G3</a> | 502D 56CCh                         |
| 6D0h   | 32     | <a href="#">CONTROLSS_INTXBAR23_G4</a> | 502D 56D0h                         |
| 6D4h   | 32     | <a href="#">CONTROLSS_INTXBAR23_G5</a> | 502D 56D4h                         |
| 6D8h   | 32     | <a href="#">CONTROLSS_INTXBAR23_G6</a> | 502D 56D8h                         |
| 700h   | 32     | <a href="#">CONTROLSS_INTXBAR24_G0</a> | 502D 5700h                         |

**Table 3-2631. CONTROLSS Registers, Base Address=502D 5000h, Length=2048 (continued)**

| Offset | Length | Register Name                          | CONTROLSS_INTXBAR Physical Address |
|--------|--------|----------------------------------------|------------------------------------|
| 704h   | 32     | <a href="#">CONTROLSS_INTXBAR24_G1</a> | 502D 5704h                         |
| 708h   | 32     | <a href="#">CONTROLSS_INTXBAR24_G2</a> | 502D 5708h                         |
| 70Ch   | 32     | <a href="#">CONTROLSS_INTXBAR24_G3</a> | 502D 570Ch                         |
| 710h   | 32     | <a href="#">CONTROLSS_INTXBAR24_G4</a> | 502D 5710h                         |
| 714h   | 32     | <a href="#">CONTROLSS_INTXBAR24_G5</a> | 502D 5714h                         |
| 718h   | 32     | <a href="#">CONTROLSS_INTXBAR24_G6</a> | 502D 5718h                         |
| 740h   | 32     | <a href="#">CONTROLSS_INTXBAR25_G0</a> | 502D 5740h                         |
| 744h   | 32     | <a href="#">CONTROLSS_INTXBAR25_G1</a> | 502D 5744h                         |
| 748h   | 32     | <a href="#">CONTROLSS_INTXBAR25_G2</a> | 502D 5748h                         |
| 74Ch   | 32     | <a href="#">CONTROLSS_INTXBAR25_G3</a> | 502D 574Ch                         |
| 750h   | 32     | <a href="#">CONTROLSS_INTXBAR25_G4</a> | 502D 5750h                         |
| 754h   | 32     | <a href="#">CONTROLSS_INTXBAR25_G5</a> | 502D 5754h                         |
| 758h   | 32     | <a href="#">CONTROLSS_INTXBAR25_G6</a> | 502D 5758h                         |
| 780h   | 32     | <a href="#">CONTROLSS_INTXBAR26_G0</a> | 502D 5780h                         |
| 784h   | 32     | <a href="#">CONTROLSS_INTXBAR26_G1</a> | 502D 5784h                         |
| 788h   | 32     | <a href="#">CONTROLSS_INTXBAR26_G2</a> | 502D 5788h                         |
| 78Ch   | 32     | <a href="#">CONTROLSS_INTXBAR26_G3</a> | 502D 578Ch                         |
| 790h   | 32     | <a href="#">CONTROLSS_INTXBAR26_G4</a> | 502D 5790h                         |
| 794h   | 32     | <a href="#">CONTROLSS_INTXBAR26_G5</a> | 502D 5794h                         |
| 798h   | 32     | <a href="#">CONTROLSS_INTXBAR26_G6</a> | 502D 5798h                         |
| 7C0h   | 32     | <a href="#">CONTROLSS_INTXBAR27_G0</a> | 502D 57C0h                         |
| 7C4h   | 32     | <a href="#">CONTROLSS_INTXBAR27_G1</a> | 502D 57C4h                         |
| 7C8h   | 32     | <a href="#">CONTROLSS_INTXBAR27_G2</a> | 502D 57C8h                         |
| 7CCh   | 32     | <a href="#">CONTROLSS_INTXBAR27_G3</a> | 502D 57CCh                         |
| 7D0h   | 32     | <a href="#">CONTROLSS_INTXBAR27_G4</a> | 502D 57D0h                         |
| 7D4h   | 32     | <a href="#">CONTROLSS_INTXBAR27_G5</a> | 502D 57D4h                         |
| 7D8h   | 32     | <a href="#">CONTROLSS_INTXBAR27_G6</a> | 502D 57D8h                         |
| 800h   | 32     | <a href="#">CONTROLSS_INTXBAR28_G0</a> | 502D 5800h                         |
| 804h   | 32     | <a href="#">CONTROLSS_INTXBAR28_G1</a> | 502D 5804h                         |
| 808h   | 32     | <a href="#">CONTROLSS_INTXBAR28_G2</a> | 502D 5808h                         |
| 80Ch   | 32     | <a href="#">CONTROLSS_INTXBAR28_G3</a> | 502D 580Ch                         |
| 810h   | 32     | <a href="#">CONTROLSS_INTXBAR28_G4</a> | 502D 5810h                         |
| 814h   | 32     | <a href="#">CONTROLSS_INTXBAR28_G5</a> | 502D 5814h                         |
| 818h   | 32     | <a href="#">CONTROLSS_INTXBAR28_G6</a> | 502D 5818h                         |
| 840h   | 32     | <a href="#">CONTROLSS_INTXBAR29_G0</a> | 502D 5840h                         |
| 844h   | 32     | <a href="#">CONTROLSS_INTXBAR29_G1</a> | 502D 5844h                         |
| 848h   | 32     | <a href="#">CONTROLSS_INTXBAR29_G2</a> | 502D 5848h                         |
| 84Ch   | 32     | <a href="#">CONTROLSS_INTXBAR29_G3</a> | 502D 584Ch                         |
| 850h   | 32     | <a href="#">CONTROLSS_INTXBAR29_G4</a> | 502D 5850h                         |
| 854h   | 32     | <a href="#">CONTROLSS_INTXBAR29_G5</a> | 502D 5854h                         |
| 858h   | 32     | <a href="#">CONTROLSS_INTXBAR29_G6</a> | 502D 5858h                         |
| 880h   | 32     | <a href="#">CONTROLSS_INTXBAR30_G0</a> | 502D 5880h                         |
| 884h   | 32     | <a href="#">CONTROLSS_INTXBAR30_G1</a> | 502D 5884h                         |
| 888h   | 32     | <a href="#">CONTROLSS_INTXBAR30_G2</a> | 502D 5888h                         |



**Table 3-2631. CONTROLSS Registers, Base Address=502D 5000h, Length=2048 (continued)**

| Offset | Length | Register Name                          | CONTROLSS_INTXBAR Physical Address |
|--------|--------|----------------------------------------|------------------------------------|
| 88Ch   | 32     | <a href="#">CONTROLSS_INTXBAR30_G3</a> | 502D 588Ch                         |
| 890h   | 32     | <a href="#">CONTROLSS_INTXBAR30_G4</a> | 502D 5890h                         |
| 894h   | 32     | <a href="#">CONTROLSS_INTXBAR30_G5</a> | 502D 5894h                         |
| 898h   | 32     | <a href="#">CONTROLSS_INTXBAR30_G6</a> | 502D 5898h                         |
| 8C0h   | 32     | <a href="#">CONTROLSS_INTXBAR31_G0</a> | 502D 58C0h                         |
| 8C4h   | 32     | <a href="#">CONTROLSS_INTXBAR31_G1</a> | 502D 58C4h                         |
| 8C8h   | 32     | <a href="#">CONTROLSS_INTXBAR31_G2</a> | 502D 58C8h                         |
| 8CCh   | 32     | <a href="#">CONTROLSS_INTXBAR31_G3</a> | 502D 58CCh                         |
| 8D0h   | 32     | <a href="#">CONTROLSS_INTXBAR31_G4</a> | 502D 58D0h                         |
| 8D4h   | 32     | <a href="#">CONTROLSS_INTXBAR31_G5</a> | 502D 58D4h                         |
| 8D8h   | 32     | <a href="#">CONTROLSS_INTXBAR31_G6</a> | 502D 58D8h                         |

### 3.16.2 CONTROLSS\_INTXBAR Registers

#### CONTROLSS\_INTXBAR Registers

### 3.16.2.1 CONTROLSS\_INTXBAR0\_G0 Register

#### 1 CONTROLSS\_INTXBAR0\_G0 Register (Offset = 100h) [reset = 0h]

INT XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-2632. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5100h       |

**Figure 3-854. CONTROLSS\_INTXBAR0\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR0_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR0_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR0_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR0_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2634. CONTROLSS\_INTXBAR0\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                     |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR0_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.2 CONTROLSS\_INTXBAR0\_G1 Register

#### 1 CONTROLSS\_INTXBAR0\_G1 Register (Offset = 104h) [reset = 0h]

INT XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-2635. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5104h       |

**Figure 3-855. CONTROLSS\_INTXBAR0\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR0_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR0_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR0_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR0_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2637. CONTROLSS\_INTXBAR0\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                           |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR0_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.3 CONTROLSS\_INTXBAR0\_G2 Register

#### 1 CONTROLSS\_INTXBAR0\_G2 Register (Offset = 108h) [reset = 0h]

INT XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-2638. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5108h       |

**Figure 3-856. CONTROLSS\_INTXBAR0\_G2 Name Register**

|                 |    |    |    |    |    |    |                 |
|-----------------|----|----|----|----|----|----|-----------------|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24              |
| RESERVED        |    |    |    |    |    |    | INTXBAR0_G2_SEL |
| NONE            |    |    |    |    |    |    | R/W             |
| 0h              |    |    |    |    |    |    | 0h              |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16              |
| INTXBAR0_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8               |
| INTXBAR0_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0               |
| INTXBAR0_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |

**Table 3-2640. CONTROLSS\_INTXBAR0\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-2640. CONTROLSS\_INTXBAR0\_G2 Register Field Descriptions (continued)**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR0_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.4 CONTROLSS\_INTXBAR0\_G3 Register

#### 1 CONTROLSS\_INTXBAR0\_G3 Register (Offset = 10Ch) [reset = 0h]

INT XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-2641. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 510Ch       |

**Figure 3-857. CONTROLSS\_INTXBAR0\_G3 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR0_G3_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR0_G3_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2643. CONTROLSS\_INTXBAR0\_G3 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR0_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.5 CONTROLSS\_INTXBAR0\_G4 Register

#### 1 CONTROLSS\_INTXBAR0\_G4 Register (Offset = 110h) [reset = 0h]

INT XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-2644. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5110h       |

**Figure 3-858. CONTROLSS\_INTXBAR0\_G4 Name Register**

|                 |    |    |    |    |    |                 |    |
|-----------------|----|----|----|----|----|-----------------|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25              | 24 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17              | 16 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9               | 8  |
| RESERVED        |    |    |    |    |    | INTXBAR0_G4_SEL |    |
| NONE            |    |    |    |    |    | R/W             |    |
| 0h              |    |    |    |    |    | 0h              |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1               | 0  |
| INTXBAR0_G4_SEL |    |    |    |    |    |                 |    |
| R/W             |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |

**Table 3-2646. CONTROLSS\_INTXBAR0\_G4 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR0_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.6 CONTROLSS\_INTXBAR0\_G5 Register

#### 1 CONTROLSS\_INTXBAR0\_G5 Register (Offset = 114h) [reset = 0h]

INT XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-2647. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5114h       |

**Figure 3-859. CONTROLSS\_INTXBAR0\_G5 Name Register**

|                 |    |    |    |    |    |                 |    |
|-----------------|----|----|----|----|----|-----------------|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25              | 24 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17              | 16 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9               | 8  |
| RESERVED        |    |    |    |    |    | INTXBAR0_G5_SEL |    |
| NONE            |    |    |    |    |    | R/W             |    |
| 0h              |    |    |    |    |    | 0h              |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1               | 0  |
| INTXBAR0_G5_SEL |    |    |    |    |    |                 |    |
| R/W             |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |

**Table 3-2649. CONTROLSS\_INTXBAR0\_G5 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                  |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR0_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.7 CONTROLSS\_INTXBAR0\_G6 Register

#### 1 CONTROLSS\_INTXBAR0\_G6 Register (Offset = 118h) [reset = 0h]

INT XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-2650. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5118h       |

**Figure 3-860. CONTROLSS\_INTXBAR0\_G6 Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | INTXBAR0_G6_SEL |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 3-2652. CONTROLSS\_INTXBAR0\_G6 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR0_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.8 CONTROLSS\_INTXBAR1\_G0 Register

#### 1 CONTROLSS\_INTXBAR1\_G0 Register (Offset = 140h) [reset = 0h]

INT XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-2653. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5140h       |

**Figure 3-861. CONTROLSS\_INTXBAR1\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR1_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR1_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR1_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR1_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2655. CONTROLSS\_INTXBAR1\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                     |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR1_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.9 CONTROLSS\_INTXBAR1\_G1 Register

#### 1 CONTROLSS\_INTXBAR1\_G1 Register (Offset = 144h) [reset = 0h]

INT XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-2656. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5144h       |

**Figure 3-862. CONTROLSS\_INTXBAR1\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR1_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR1_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR1_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR1_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2658. CONTROLSS\_INTXBAR1\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                           |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR1_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.10 CONTROLSS\_INTXBAR1\_G2 Register

#### 1 CONTROLSS\_INTXBAR1\_G2 Register (Offset = 148h) [reset = 0h]

INT XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-2659. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5148h       |

**Figure 3-863. CONTROLSS\_INTXBAR1\_G2 Name Register**

|                 |    |    |    |    |    |    |                 |
|-----------------|----|----|----|----|----|----|-----------------|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24              |
| RESERVED        |    |    |    |    |    |    | INTXBAR1_G2_SEL |
| NONE            |    |    |    |    |    |    | R/W             |
| 0h              |    |    |    |    |    |    | 0h              |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16              |
| INTXBAR1_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8               |
| INTXBAR1_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0               |
| INTXBAR1_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |

**Table 3-2661. CONTROLSS\_INTXBAR1\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-2661. CONTROLSS\_INTXBAR1\_G2 Register Field Descriptions (continued)**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR1_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.11 CONTROLSS\_INTXBAR1\_G3 Register

#### 1 CONTROLSS\_INTXBAR1\_G3 Register (Offset = 14Ch) [reset = 0h]

INT XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-2662. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 514Ch       |

**Figure 3-864. CONTROLSS\_INTXBAR1\_G3 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR1_G3_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR1_G3_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2664. CONTROLSS\_INTXBAR1\_G3 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR1_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.12 CONTROLSS\_INTXBAR1\_G4 Register

#### 1 CONTROLSS\_INTXBAR1\_G4 Register (Offset = 150h) [reset = 0h]

INT XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-2665. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5150h       |

**Figure 3-865. CONTROLSS\_INTXBAR1\_G4 Name Register**

|                 |    |    |    |    |    |                 |    |
|-----------------|----|----|----|----|----|-----------------|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25              | 24 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17              | 16 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9               | 8  |
| RESERVED        |    |    |    |    |    | INTXBAR1_G4_SEL |    |
| NONE            |    |    |    |    |    | R/W             |    |
| 0h              |    |    |    |    |    | 0h              |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1               | 0  |
| INTXBAR1_G4_SEL |    |    |    |    |    |                 |    |
| R/W             |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |

**Table 3-2667. CONTROLSS\_INTXBAR1\_G4 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR1_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.13 CONTROLSS\_INTXBAR1\_G5 Register

#### 1 CONTROLSS\_INTXBAR1\_G5 Register (Offset = 154h) [reset = 0h]

INT XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-2668. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5154h       |

**Figure 3-866. CONTROLSS\_INTXBAR1\_G5 Name Register**

|                 |    |    |    |    |    |                 |    |
|-----------------|----|----|----|----|----|-----------------|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25              | 24 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17              | 16 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9               | 8  |
| RESERVED        |    |    |    |    |    | INTXBAR1_G5_SEL |    |
| NONE            |    |    |    |    |    | R/W             |    |
| 0h              |    |    |    |    |    | 0h              |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1               | 0  |
| INTXBAR1_G5_SEL |    |    |    |    |    |                 |    |
| R/W             |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |

**Table 3-2670. CONTROLSS\_INTXBAR1\_G5 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                  |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR1_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.14 CONTROLSS\_INTXBAR1\_G6 Register

#### 1 CONTROLSS\_INTXBAR1\_G6 Register (Offset = 158h) [reset = 0h]

INT XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-2671. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5158h       |

**Figure 3-867. CONTROLSS\_INTXBAR1\_G6 Name Register**

|          |    |    |    |    |                 |    |    |
|----------|----|----|----|----|-----------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26              | 25 | 24 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 23       | 22 | 21 | 20 | 19 | 18              | 17 | 16 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 15       | 14 | 13 | 12 | 11 | 10              | 9  | 8  |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 7        | 6  | 5  | 4  | 3  | 2               | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR1_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W             |    |    |
| 0h       |    |    |    |    | 0h              |    |    |

**Table 3-2673. CONTROLSS\_INTXBAR1\_G6 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR1_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.15 CONTROLSS\_INTXBAR2\_G0 Register

#### 1 CONTROLSS\_INTXBAR2\_G0 Register (Offset = 180h) [reset = 0h]

INT XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-2674. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5180h       |

**Figure 3-868. CONTROLSS\_INTXBAR2\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR2_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR2_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR2_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR2_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2676. CONTROLSS\_INTXBAR2\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                     |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR2_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.16 CONTROLSS\_INTXBAR2\_G1 Register

#### 1 CONTROLSS\_INTXBAR2\_G1 Register (Offset = 184h) [reset = 0h]

INT XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-2677. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5184h       |

**Figure 3-869. CONTROLSS\_INTXBAR2\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR2_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR2_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR2_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR2_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2679. CONTROLSS\_INTXBAR2\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                           |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR2_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.17 CONTROLSS\_INTXBAR2\_G2 Register

#### 1 CONTROLSS\_INTXBAR2\_G2 Register (Offset = 188h) [reset = 0h]

INT XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-2680. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5188h       |

**Figure 3-870. CONTROLSS\_INTXBAR2\_G2 Name Register**

|                 |    |    |    |    |    |    |                 |
|-----------------|----|----|----|----|----|----|-----------------|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24              |
| RESERVED        |    |    |    |    |    |    | INTXBAR2_G2_SEL |
| NONE            |    |    |    |    |    |    | R/W             |
| 0h              |    |    |    |    |    |    | 0h              |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16              |
| INTXBAR2_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8               |
| INTXBAR2_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0               |
| INTXBAR2_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |

**Table 3-2682. CONTROLSS\_INTXBAR2\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-2682. CONTROLSS\_INTXBAR2\_G2 Register Field Descriptions (continued)**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR2_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.18 CONTROLSS\_INTXBAR2\_G3 Register

#### 1 CONTROLSS\_INTXBAR2\_G3 Register (Offset = 18Ch) [reset = 0h]

INT XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-2683. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 518Ch       |

**Figure 3-871. CONTROLSS\_INTXBAR2\_G3 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR2_G3_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR2_G3_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2685. CONTROLSS\_INTXBAR2\_G3 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR2_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.19 CONTROLSS\_INTXBAR2\_G4 Register

#### 1 CONTROLSS\_INTXBAR2\_G4 Register (Offset = 190h) [reset = 0h]

INT XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-2686. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5190h       |

**Figure 3-872. CONTROLSS\_INTXBAR2\_G4 Name Register**

|                 |    |    |    |    |    |                 |    |
|-----------------|----|----|----|----|----|-----------------|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25              | 24 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17              | 16 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9               | 8  |
| RESERVED        |    |    |    |    |    | INTXBAR2_G4_SEL |    |
| NONE            |    |    |    |    |    | R/W             |    |
| 0h              |    |    |    |    |    | 0h              |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1               | 0  |
| INTXBAR2_G4_SEL |    |    |    |    |    |                 |    |
| R/W             |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |

**Table 3-2688. CONTROLSS\_INTXBAR2\_G4 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR2_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.20 CONTROLSS\_INTXBAR2\_G5 Register

#### 1 CONTROLSS\_INTXBAR2\_G5 Register (Offset = 194h) [reset = 0h]

INT XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-2689. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5194h       |

**Figure 3-873. CONTROLSS\_INTXBAR2\_G5 Name Register**

|                 |    |    |    |    |    |                 |    |
|-----------------|----|----|----|----|----|-----------------|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25              | 24 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17              | 16 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9               | 8  |
| RESERVED        |    |    |    |    |    | INTXBAR2_G5_SEL |    |
| NONE            |    |    |    |    |    | R/W             |    |
| 0h              |    |    |    |    |    | 0h              |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1               | 0  |
| INTXBAR2_G5_SEL |    |    |    |    |    |                 |    |
| R/W             |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |

**Table 3-2691. CONTROLSS\_INTXBAR2\_G5 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                  |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR2_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.21 CONTROLSS\_INTXBAR2\_G6 Register

#### 1 CONTROLSS\_INTXBAR2\_G6 Register (Offset = 198h) [reset = 0h]

INT XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-2692. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5198h       |

**Figure 3-874. CONTROLSS\_INTXBAR2\_G6 Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | INTXBAR2_G6_SEL |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 3-2694. CONTROLSS\_INTXBAR2\_G6 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR2_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.22 CONTROLSS\_INTXBAR3\_G0 Register

#### 1 CONTROLSS\_INTXBAR3\_G0 Register (Offset = 1C0h) [reset = 0h]

INT XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-2695. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 51C0h       |

**Figure 3-875. CONTROLSS\_INTXBAR3\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR3_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR3_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR3_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR3_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2697. CONTROLSS\_INTXBAR3\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                     |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR3_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.23 CONTROLSS\_INTXBAR3\_G1 Register

#### 1 CONTROLSS\_INTXBAR3\_G1 Register (Offset = 1C4h) [reset = 0h]

INT XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-2698. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 51C4h       |

**Figure 3-876. CONTROLSS\_INTXBAR3\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR3_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR3_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR3_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR3_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2700. CONTROLSS\_INTXBAR3\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                           |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR3_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.24 CONTROLSS\_INTXBAR3\_G2 Register

#### 1 CONTROLSS\_INTXBAR3\_G2 Register (Offset = 1C8h) [reset = 0h]

INT XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-2701. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 51C8h       |

**Figure 3-877. CONTROLSS\_INTXBAR3\_G2 Name Register**

|                 |    |    |    |    |    |    |                 |
|-----------------|----|----|----|----|----|----|-----------------|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24              |
| RESERVED        |    |    |    |    |    |    | INTXBAR3_G2_SEL |
| NONE            |    |    |    |    |    |    | R/W             |
| 0h              |    |    |    |    |    |    | 0h              |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16              |
| INTXBAR3_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8               |
| INTXBAR3_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0               |
| INTXBAR3_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |

**Table 3-2703. CONTROLSS\_INTXBAR3\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-2703. CONTROLSS\_INTXBAR3\_G2 Register Field Descriptions (continued)**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR3_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.25 CONTROLSS\_INTXBAR3\_G3 Register

#### 1 CONTROLSS\_INTXBAR3\_G3 Register (Offset = 1CCh) [reset = 0h]

INT XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-2704. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 51CCh       |

**Figure 3-878. CONTROLSS\_INTXBAR3\_G3 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR3_G3_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR3_G3_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2706. CONTROLSS\_INTXBAR3\_G3 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR3_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.26 CONTROLSS\_INTXBAR3\_G4 Register

#### 1 CONTROLSS\_INTXBAR3\_G4 Register (Offset = 1D0h) [reset = 0h]

INT XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-2707. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 51D0h       |

**Figure 3-879. CONTROLSS\_INTXBAR3\_G4 Name Register**

|                 |    |    |    |    |    |                 |    |
|-----------------|----|----|----|----|----|-----------------|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25              | 24 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17              | 16 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9               | 8  |
| RESERVED        |    |    |    |    |    | INTXBAR3_G4_SEL |    |
| NONE            |    |    |    |    |    | R/W             |    |
| 0h              |    |    |    |    |    | 0h              |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1               | 0  |
| INTXBAR3_G4_SEL |    |    |    |    |    |                 |    |
| R/W             |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |

**Table 3-2709. CONTROLSS\_INTXBAR3\_G4 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR3_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.27 CONTROLSS\_INTXBAR3\_G5 Register

#### 1 CONTROLSS\_INTXBAR3\_G5 Register (Offset = 1D4h) [reset = 0h]

INT XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-2710. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 51D4h       |

**Figure 3-880. CONTROLSS\_INTXBAR3\_G5 Name Register**

|                 |    |    |    |    |    |                 |    |
|-----------------|----|----|----|----|----|-----------------|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25              | 24 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17              | 16 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9               | 8  |
| RESERVED        |    |    |    |    |    | INTXBAR3_G5_SEL |    |
| NONE            |    |    |    |    |    | R/W             |    |
| 0h              |    |    |    |    |    | 0h              |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1               | 0  |
| INTXBAR3_G5_SEL |    |    |    |    |    |                 |    |
| R/W             |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |

**Table 3-2712. CONTROLSS\_INTXBAR3\_G5 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                  |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR3_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.28 CONTROLSS\_INTXBAR3\_G6 Register

#### 1 CONTROLSS\_INTXBAR3\_G6 Register (Offset = 1D8h) [reset = 0h]

INT XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-2713. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 51D8h       |

**Figure 3-881. CONTROLSS\_INTXBAR3\_G6 Name Register**

|          |    |    |    |    |                 |    |    |
|----------|----|----|----|----|-----------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26              | 25 | 24 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 23       | 22 | 21 | 20 | 19 | 18              | 17 | 16 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 15       | 14 | 13 | 12 | 11 | 10              | 9  | 8  |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 7        | 6  | 5  | 4  | 3  | 2               | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR3_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W             |    |    |
| 0h       |    |    |    |    | 0h              |    |    |

**Table 3-2715. CONTROLSS\_INTXBAR3\_G6 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR3_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.29 CONTROLSS\_INTXBAR4\_G0 Register

#### 1 CONTROLSS\_INTXBAR4\_G0 Register (Offset = 200h) [reset = 0h]

INT XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-2716. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5200h       |

**Figure 3-882. CONTROLSS\_INTXBAR4\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR4_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR4_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR4_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR4_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2718. CONTROLSS\_INTXBAR4\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                     |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR4_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.30 CONTROLSS\_INTXBAR4\_G1 Register

#### 1 CONTROLSS\_INTXBAR4\_G1 Register (Offset = 204h) [reset = 0h]

INT XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-2719. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5204h       |

**Figure 3-883. CONTROLSS\_INTXBAR4\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR4_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR4_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR4_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR4_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2721. CONTROLSS\_INTXBAR4\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                           |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR4_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.31 CONTROLSS\_INTXBAR4\_G2 Register

#### 1 CONTROLSS\_INTXBAR4\_G2 Register (Offset = 208h) [reset = 0h]

INT XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-2722. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5208h       |

**Figure 3-884. CONTROLSS\_INTXBAR4\_G2 Name Register**

|                 |    |    |    |    |    |    |                 |
|-----------------|----|----|----|----|----|----|-----------------|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24              |
| RESERVED        |    |    |    |    |    |    | INTXBAR4_G2_SEL |
| NONE            |    |    |    |    |    |    | R/W             |
| 0h              |    |    |    |    |    |    | 0h              |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16              |
| INTXBAR4_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8               |
| INTXBAR4_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0               |
| INTXBAR4_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |

**Table 3-2724. CONTROLSS\_INTXBAR4\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-2724. CONTROLSS\_INTXBAR4\_G2 Register Field Descriptions (continued)**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR4_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.32 CONTROLSS\_INTXBAR4\_G3 Register

#### 1 CONTROLSS\_INTXBAR4\_G3 Register (Offset = 20Ch) [reset = 0h]

INT XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-2725. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 520Ch       |

**Figure 3-885. CONTROLSS\_INTXBAR4\_G3 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR4_G3_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR4_G3_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2727. CONTROLSS\_INTXBAR4\_G3 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR4_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.33 CONTROLSS\_INTXBAR4\_G4 Register

#### 1 CONTROLSS\_INTXBAR4\_G4 Register (Offset = 210h) [reset = 0h]

INT XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-2728. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5210h       |

**Figure 3-886. CONTROLSS\_INTXBAR4\_G4 Name Register**

|                 |    |    |    |    |    |                 |    |
|-----------------|----|----|----|----|----|-----------------|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25              | 24 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17              | 16 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9               | 8  |
| RESERVED        |    |    |    |    |    | INTXBAR4_G4_SEL |    |
| NONE            |    |    |    |    |    | R/W             |    |
| 0h              |    |    |    |    |    | 0h              |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1               | 0  |
| INTXBAR4_G4_SEL |    |    |    |    |    |                 |    |
| R/W             |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |

**Table 3-2730. CONTROLSS\_INTXBAR4\_G4 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR4_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.34 CONTROLSS\_INTXBAR4\_G5 Register

#### 1 CONTROLSS\_INTXBAR4\_G5 Register (Offset = 214h) [reset = 0h]

INT XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-2731. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5214h       |

**Figure 3-887. CONTROLSS\_INTXBAR4\_G5 Name Register**

|                 |    |    |    |    |    |                 |    |
|-----------------|----|----|----|----|----|-----------------|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25              | 24 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17              | 16 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9               | 8  |
| RESERVED        |    |    |    |    |    | INTXBAR4_G5_SEL |    |
| NONE            |    |    |    |    |    | R/W             |    |
| 0h              |    |    |    |    |    | 0h              |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1               | 0  |
| INTXBAR4_G5_SEL |    |    |    |    |    |                 |    |
| R/W             |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |

**Table 3-2733. CONTROLSS\_INTXBAR4\_G5 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                  |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR4_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.35 CONTROLSS\_INTXBAR4\_G6 Register

#### 1 CONTROLSS\_INTXBAR4\_G6 Register (Offset = 218h) [reset = 0h]

INT XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-2734. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5218h       |

**Figure 3-888. CONTROLSS\_INTXBAR4\_G6 Name Register**

|          |    |    |    |    |                 |    |    |
|----------|----|----|----|----|-----------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26              | 25 | 24 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 23       | 22 | 21 | 20 | 19 | 18              | 17 | 16 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 15       | 14 | 13 | 12 | 11 | 10              | 9  | 8  |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 7        | 6  | 5  | 4  | 3  | 2               | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR4_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W             |    |    |
| 0h       |    |    |    |    | 0h              |    |    |

**Table 3-2736. CONTROLSS\_INTXBAR4\_G6 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR4_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.36 CONTROLSS\_INTXBAR5\_G0 Register

#### 1 CONTROLSS\_INTXBAR5\_G0 Register (Offset = 240h) [reset = 0h]

INT XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-2737. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5240h       |

**Figure 3-889. CONTROLSS\_INTXBAR5\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR5_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR5_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR5_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR5_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2739. CONTROLSS\_INTXBAR5\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                     |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR5_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.37 CONTROLSS\_INTXBAR5\_G1 Register

#### 1 CONTROLSS\_INTXBAR5\_G1 Register (Offset = 244h) [reset = 0h]

INT XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-2740. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5244h       |

**Figure 3-890. CONTROLSS\_INTXBAR5\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR5_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR5_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR5_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR5_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2742. CONTROLSS\_INTXBAR5\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                           |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR5_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.38 CONTROLSS\_INTXBAR5\_G2 Register

#### 1 CONTROLSS\_INTXBAR5\_G2 Register (Offset = 248h) [reset = 0h]

INT XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-2743. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5248h       |

**Figure 3-891. CONTROLSS\_INTXBAR5\_G2 Name Register**

|                 |    |    |    |    |    |    |                 |
|-----------------|----|----|----|----|----|----|-----------------|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24              |
| RESERVED        |    |    |    |    |    |    | INTXBAR5_G2_SEL |
| NONE            |    |    |    |    |    |    | R/W             |
| 0h              |    |    |    |    |    |    | 0h              |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16              |
| INTXBAR5_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8               |
| INTXBAR5_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0               |
| INTXBAR5_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |

**Table 3-2745. CONTROLSS\_INTXBAR5\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-2745. CONTROLSS\_INTXBAR5\_G2 Register Field Descriptions (continued)**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR5_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.39 CONTROLSS\_INTXBAR5\_G3 Register

#### 1 CONTROLSS\_INTXBAR5\_G3 Register (Offset = 24Ch) [reset = 0h]

INT XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-2746. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 524Ch       |

**Figure 3-892. CONTROLSS\_INTXBAR5\_G3 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR5_G3_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR5_G3_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2748. CONTROLSS\_INTXBAR5\_G3 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR5_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.40 CONTROLSS\_INTXBAR5\_G4 Register

#### 1 CONTROLSS\_INTXBAR5\_G4 Register (Offset = 250h) [reset = 0h]

INT XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-2749. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5250h       |

**Figure 3-893. CONTROLSS\_INTXBAR5\_G4 Name Register**

|                 |    |    |    |    |    |                 |    |
|-----------------|----|----|----|----|----|-----------------|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25              | 24 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17              | 16 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9               | 8  |
| RESERVED        |    |    |    |    |    | INTXBAR5_G4_SEL |    |
| NONE            |    |    |    |    |    | R/W             |    |
| 0h              |    |    |    |    |    | 0h              |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1               | 0  |
| INTXBAR5_G4_SEL |    |    |    |    |    |                 |    |
| R/W             |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |

**Table 3-2751. CONTROLSS\_INTXBAR5\_G4 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR5_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.41 CONTROLSS\_INTXBAR5\_G5 Register

#### 1 CONTROLSS\_INTXBAR5\_G5 Register (Offset = 254h) [reset = 0h]

INT XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-2752. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5254h       |

**Figure 3-894. CONTROLSS\_INTXBAR5\_G5 Name Register**

|                 |    |    |    |    |    |                 |    |
|-----------------|----|----|----|----|----|-----------------|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25              | 24 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17              | 16 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9               | 8  |
| RESERVED        |    |    |    |    |    | INTXBAR5_G5_SEL |    |
| NONE            |    |    |    |    |    | R/W             |    |
| 0h              |    |    |    |    |    | 0h              |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1               | 0  |
| INTXBAR5_G5_SEL |    |    |    |    |    |                 |    |
| R/W             |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |

**Table 3-2754. CONTROLSS\_INTXBAR5\_G5 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                  |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR5_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.42 CONTROLSS\_INTXBAR5\_G6 Register

#### 1 CONTROLSS\_INTXBAR5\_G6 Register (Offset = 258h) [reset = 0h]

INT XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-2755. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5258h       |

**Figure 3-895. CONTROLSS\_INTXBAR5\_G6 Name Register**

|          |    |    |    |    |                 |    |    |
|----------|----|----|----|----|-----------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26              | 25 | 24 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 23       | 22 | 21 | 20 | 19 | 18              | 17 | 16 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 15       | 14 | 13 | 12 | 11 | 10              | 9  | 8  |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 7        | 6  | 5  | 4  | 3  | 2               | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR5_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W             |    |    |
| 0h       |    |    |    |    | 0h              |    |    |

**Table 3-2757. CONTROLSS\_INTXBAR5\_G6 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR5_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.43 CONTROLSS\_INTXBAR6\_G0 Register

#### 1 CONTROLSS\_INTXBAR6\_G0 Register (Offset = 280h) [reset = 0h]

INT XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-2758. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5280h       |

**Figure 3-896. CONTROLSS\_INTXBAR6\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR6_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR6_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR6_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR6_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2760. CONTROLSS\_INTXBAR6\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                     |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR6_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.44 CONTROLSS\_INTXBAR6\_G1 Register

#### 1 CONTROLSS\_INTXBAR6\_G1 Register (Offset = 284h) [reset = 0h]

INT XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-2761. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5284h       |

**Figure 3-897. CONTROLSS\_INTXBAR6\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR6_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR6_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR6_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR6_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2763. CONTROLSS\_INTXBAR6\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                           |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR6_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.45 CONTROLSS\_INTXBAR6\_G2 Register

#### 1 CONTROLSS\_INTXBAR6\_G2 Register (Offset = 288h) [reset = 0h]

INT XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-2764. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5288h       |

**Figure 3-898. CONTROLSS\_INTXBAR6\_G2 Name Register**

|                 |    |    |    |    |    |    |                 |
|-----------------|----|----|----|----|----|----|-----------------|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24              |
| RESERVED        |    |    |    |    |    |    | INTXBAR6_G2_SEL |
| NONE            |    |    |    |    |    |    | R/W             |
| 0h              |    |    |    |    |    |    | 0h              |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16              |
| INTXBAR6_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8               |
| INTXBAR6_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0               |
| INTXBAR6_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |

**Table 3-2766. CONTROLSS\_INTXBAR6\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-2766. CONTROLSS\_INTXBAR6\_G2 Register Field Descriptions (continued)**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR6_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.46 CONTROLSS\_INTXBAR6\_G3 Register

#### 1 CONTROLSS\_INTXBAR6\_G3 Register (Offset = 28Ch) [reset = 0h]

INT XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-2767. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 528Ch       |

**Figure 3-899. CONTROLSS\_INTXBAR6\_G3 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR6_G3_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR6_G3_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2769. CONTROLSS\_INTXBAR6\_G3 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR6_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.47 CONTROLSS\_INTXBAR6\_G4 Register

#### 1 CONTROLSS\_INTXBAR6\_G4 Register (Offset = 290h) [reset = 0h]

INT XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-2770. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5290h       |

**Figure 3-900. CONTROLSS\_INTXBAR6\_G4 Name Register**

|                 |    |    |    |    |    |                 |    |
|-----------------|----|----|----|----|----|-----------------|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25              | 24 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17              | 16 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9               | 8  |
| RESERVED        |    |    |    |    |    | INTXBAR6_G4_SEL |    |
| NONE            |    |    |    |    |    | R/W             |    |
| 0h              |    |    |    |    |    | 0h              |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1               | 0  |
| INTXBAR6_G4_SEL |    |    |    |    |    |                 |    |
| R/W             |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |

**Table 3-2772. CONTROLSS\_INTXBAR6\_G4 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR6_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.48 CONTROLSS\_INTXBAR6\_G5 Register

#### 1 CONTROLSS\_INTXBAR6\_G5 Register (Offset = 294h) [reset = 0h]

INT XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-2773. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5294h       |

**Figure 3-901. CONTROLSS\_INTXBAR6\_G5 Name Register**

|                 |    |    |    |    |    |                 |    |
|-----------------|----|----|----|----|----|-----------------|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25              | 24 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17              | 16 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9               | 8  |
| RESERVED        |    |    |    |    |    | INTXBAR6_G5_SEL |    |
| NONE            |    |    |    |    |    | R/W             |    |
| 0h              |    |    |    |    |    | 0h              |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1               | 0  |
| INTXBAR6_G5_SEL |    |    |    |    |    |                 |    |
| R/W             |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |

**Table 3-2775. CONTROLSS\_INTXBAR6\_G5 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                  |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR6_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.49 CONTROLSS\_INTXBAR6\_G6 Register

#### 1 CONTROLSS\_INTXBAR6\_G6 Register (Offset = 298h) [reset = 0h]

INT XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-2776. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5298h       |

**Figure 3-902. CONTROLSS\_INTXBAR6\_G6 Name Register**

|          |    |    |    |                 |    |    |    |
|----------|----|----|----|-----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 23       | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 15       | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| RESERVED |    |    |    |                 |    |    |    |
| NONE     |    |    |    |                 |    |    |    |
| 0h       |    |    |    |                 |    |    |    |
| 7        | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED |    |    |    | INTXBAR6_G6_SEL |    |    |    |
| NONE     |    |    |    | R/W             |    |    |    |
| 0h       |    |    |    | 0h              |    |    |    |

**Table 3-2778. CONTROLSS\_INTXBAR6\_G6 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR6_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.50 CONTROLSS\_INTXBAR7\_G0 Register

#### 1 CONTROLSS\_INTXBAR7\_G0 Register (Offset = 2C0h) [reset = 0h]

INT XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-2779. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 52C0h       |

**Figure 3-903. CONTROLSS\_INTXBAR7\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR7_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR7_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR7_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR7_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2781. CONTROLSS\_INTXBAR7\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                     |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR7_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.51 CONTROLSS\_INTXBAR7\_G1 Register

#### 1 CONTROLSS\_INTXBAR7\_G1 Register (Offset = 2C4h) [reset = 0h]

INT XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-2782. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 52C4h       |

**Figure 3-904. CONTROLSS\_INTXBAR7\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR7_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR7_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR7_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR7_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2784. CONTROLSS\_INTXBAR7\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                           |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR7_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.52 CONTROLSS\_INTXBAR7\_G2 Register

#### 1 CONTROLSS\_INTXBAR7\_G2 Register (Offset = 2C8h) [reset = 0h]

INT XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-2785. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 52C8h       |

**Figure 3-905. CONTROLSS\_INTXBAR7\_G2 Name Register**

|                 |    |    |    |    |    |    |                 |
|-----------------|----|----|----|----|----|----|-----------------|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24              |
| RESERVED        |    |    |    |    |    |    | INTXBAR7_G2_SEL |
| NONE            |    |    |    |    |    |    | R/W             |
| 0h              |    |    |    |    |    |    | 0h              |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16              |
| INTXBAR7_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8               |
| INTXBAR7_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0               |
| INTXBAR7_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |

**Table 3-2787. CONTROLSS\_INTXBAR7\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-2787. CONTROLSS\_INTXBAR7\_G2 Register Field Descriptions (continued)**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR7_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.53 CONTROLSS\_INTXBAR7\_G3 Register

#### 1 CONTROLSS\_INTXBAR7\_G3 Register (Offset = 2CCh) [reset = 0h]

INT XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-2788. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 52CCh       |

**Figure 3-906. CONTROLSS\_INTXBAR7\_G3 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR7_G3_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR7_G3_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2790. CONTROLSS\_INTXBAR7\_G3 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR7_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.54 CONTROLSS\_INTXBAR7\_G4 Register

#### 1 CONTROLSS\_INTXBAR7\_G4 Register (Offset = 2D0h) [reset = 0h]

INT XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-2791. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 52D0h       |

**Figure 3-907. CONTROLSS\_INTXBAR7\_G4 Name Register**

|                 |    |    |    |    |    |                 |    |
|-----------------|----|----|----|----|----|-----------------|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25              | 24 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17              | 16 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9               | 8  |
| RESERVED        |    |    |    |    |    | INTXBAR7_G4_SEL |    |
| NONE            |    |    |    |    |    | R/W             |    |
| 0h              |    |    |    |    |    | 0h              |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1               | 0  |
| INTXBAR7_G4_SEL |    |    |    |    |    |                 |    |
| R/W             |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |

**Table 3-2793. CONTROLSS\_INTXBAR7\_G4 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR7_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.55 CONTROLSS\_INTXBAR7\_G5 Register

#### 1 CONTROLSS\_INTXBAR7\_G5 Register (Offset = 2D4h) [reset = 0h]

INT XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-2794. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 52D4h       |

**Figure 3-908. CONTROLSS\_INTXBAR7\_G5 Name Register**

|                 |    |    |    |    |    |                 |    |
|-----------------|----|----|----|----|----|-----------------|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25              | 24 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17              | 16 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9               | 8  |
| RESERVED        |    |    |    |    |    | INTXBAR7_G5_SEL |    |
| NONE            |    |    |    |    |    | R/W             |    |
| 0h              |    |    |    |    |    | 0h              |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1               | 0  |
| INTXBAR7_G5_SEL |    |    |    |    |    |                 |    |
| R/W             |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |

**Table 3-2796. CONTROLSS\_INTXBAR7\_G5 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                  |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR7_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.56 CONTROLSS\_INTXBAR7\_G6 Register

#### 1 CONTROLSS\_INTXBAR7\_G6 Register (Offset = 2D8h) [reset = 0h]

INT XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-2797. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 52D8h       |

**Figure 3-909. CONTROLSS\_INTXBAR7\_G6 Name Register**

|          |    |    |    |    |                 |    |    |
|----------|----|----|----|----|-----------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26              | 25 | 24 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 23       | 22 | 21 | 20 | 19 | 18              | 17 | 16 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 15       | 14 | 13 | 12 | 11 | 10              | 9  | 8  |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 7        | 6  | 5  | 4  | 3  | 2               | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR7_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W             |    |    |
| 0h       |    |    |    |    | 0h              |    |    |

**Table 3-2799. CONTROLSS\_INTXBAR7\_G6 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR7_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.57 CONTROLSS\_INTXBAR8\_G0 Register

#### 1 CONTROLSS\_INTXBAR8\_G0 Register (Offset = 300h) [reset = 0h]

INT XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-2800. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5300h       |

**Figure 3-910. CONTROLSS\_INTXBAR8\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR8_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR8_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR8_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR8_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2802. CONTROLSS\_INTXBAR8\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                     |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR8_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.58 CONTROLSS\_INTXBAR8\_G1 Register

#### 1 CONTROLSS\_INTXBAR8\_G1 Register (Offset = 304h) [reset = 0h]

INT XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-2803. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5304h       |

**Figure 3-911. CONTROLSS\_INTXBAR8\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR8_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR8_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR8_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR8_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2805. CONTROLSS\_INTXBAR8\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                           |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR8_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.59 CONTROLSS\_INTXBAR8\_G2 Register

#### 1 CONTROLSS\_INTXBAR8\_G2 Register (Offset = 308h) [reset = 0h]

INT XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-2806. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5308h       |

**Figure 3-912. CONTROLSS\_INTXBAR8\_G2 Name Register**

|                 |    |    |    |    |    |    |                 |
|-----------------|----|----|----|----|----|----|-----------------|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24              |
| RESERVED        |    |    |    |    |    |    | INTXBAR8_G2_SEL |
| NONE            |    |    |    |    |    |    | R/W             |
| 0h              |    |    |    |    |    |    | 0h              |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16              |
| INTXBAR8_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8               |
| INTXBAR8_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0               |
| INTXBAR8_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |

**Table 3-2808. CONTROLSS\_INTXBAR8\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-2808. CONTROLSS\_INTXBAR8\_G2 Register Field Descriptions (continued)**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR8_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.60 CONTROLSS\_INTXBAR8\_G3 Register

#### 1 CONTROLSS\_INTXBAR8\_G3 Register (Offset = 30Ch) [reset = 0h]

INT XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-2809. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 530Ch       |

**Figure 3-913. CONTROLSS\_INTXBAR8\_G3 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR8_G3_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR8_G3_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2811. CONTROLSS\_INTXBAR8\_G3 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR8_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.61 CONTROLSS\_INTXBAR8\_G4 Register

#### 1 CONTROLSS\_INTXBAR8\_G4 Register (Offset = 310h) [reset = 0h]

INT XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-2812. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5310h       |

**Figure 3-914. CONTROLSS\_INTXBAR8\_G4 Name Register**

|                 |    |    |    |    |    |                 |    |
|-----------------|----|----|----|----|----|-----------------|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25              | 24 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17              | 16 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9               | 8  |
| RESERVED        |    |    |    |    |    | INTXBAR8_G4_SEL |    |
| NONE            |    |    |    |    |    | R/W             |    |
| 0h              |    |    |    |    |    | 0h              |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1               | 0  |
| INTXBAR8_G4_SEL |    |    |    |    |    |                 |    |
| R/W             |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |

**Table 3-2814. CONTROLSS\_INTXBAR8\_G4 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR8_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.62 CONTROLSS\_INTXBAR8\_G5 Register

#### 1 CONTROLSS\_INTXBAR8\_G5 Register (Offset = 314h) [reset = 0h]

INT XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-2815. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5314h       |

**Figure 3-915. CONTROLSS\_INTXBAR8\_G5 Name Register**

|                 |    |    |    |    |    |                 |    |
|-----------------|----|----|----|----|----|-----------------|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25              | 24 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17              | 16 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9               | 8  |
| RESERVED        |    |    |    |    |    | INTXBAR8_G5_SEL |    |
| NONE            |    |    |    |    |    | R/W             |    |
| 0h              |    |    |    |    |    | 0h              |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1               | 0  |
| INTXBAR8_G5_SEL |    |    |    |    |    |                 |    |
| R/W             |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |

**Table 3-2817. CONTROLSS\_INTXBAR8\_G5 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                  |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR8_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.63 CONTROLSS\_INTXBAR8\_G6 Register

#### 1 CONTROLSS\_INTXBAR8\_G6 Register (Offset = 318h) [reset = 0h]

INT XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-2818. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5318h       |

**Figure 3-916. CONTROLSS\_INTXBAR8\_G6 Name Register**

|          |    |    |    |    |                 |    |    |
|----------|----|----|----|----|-----------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26              | 25 | 24 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 23       | 22 | 21 | 20 | 19 | 18              | 17 | 16 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 15       | 14 | 13 | 12 | 11 | 10              | 9  | 8  |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 7        | 6  | 5  | 4  | 3  | 2               | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR8_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W             |    |    |
| 0h       |    |    |    |    | 0h              |    |    |

**Table 3-2820. CONTROLSS\_INTXBAR8\_G6 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR8_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.64 CONTROLSS\_INTXBAR9\_G0 Register

#### 1 CONTROLSS\_INTXBAR9\_G0 Register (Offset = 340h) [reset = 0h]

INT XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-2821. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5340h       |

**Figure 3-917. CONTROLSS\_INTXBAR9\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR9_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR9_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR9_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR9_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2823. CONTROLSS\_INTXBAR9\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                     |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR9_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.65 CONTROLSS\_INTXBAR9\_G1 Register

#### 1 CONTROLSS\_INTXBAR9\_G1 Register (Offset = 344h) [reset = 0h]

INT XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-2824. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5344h       |

**Figure 3-918. CONTROLSS\_INTXBAR9\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR9_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR9_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR9_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR9_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2826. CONTROLSS\_INTXBAR9\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                           |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR9_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.66 CONTROLSS\_INTXBAR9\_G2 Register

#### 1 CONTROLSS\_INTXBAR9\_G2 Register (Offset = 348h) [reset = 0h]

INT XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-2827. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5348h       |

**Figure 3-919. CONTROLSS\_INTXBAR9\_G2 Name Register**

|                 |    |    |    |    |    |    |                 |
|-----------------|----|----|----|----|----|----|-----------------|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24              |
| RESERVED        |    |    |    |    |    |    | INTXBAR9_G2_SEL |
| NONE            |    |    |    |    |    |    | R/W             |
| 0h              |    |    |    |    |    |    | 0h              |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16              |
| INTXBAR9_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8               |
| INTXBAR9_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0               |
| INTXBAR9_G2_SEL |    |    |    |    |    |    |                 |
| R/W             |    |    |    |    |    |    |                 |
| 0h              |    |    |    |    |    |    |                 |

**Table 3-2829. CONTROLSS\_INTXBAR9\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-2829. CONTROLSS\_INTXBAR9\_G2 Register Field Descriptions (continued)**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR9_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.67 CONTROLSS\_INTXBAR9\_G3 Register

#### 1 CONTROLSS\_INTXBAR9\_G3 Register (Offset = 34Ch) [reset = 0h]

INT XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-2830. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 534Ch       |

**Figure 3-920. CONTROLSS\_INTXBAR9\_G3 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR9_G3_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR9_G3_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-2832. CONTROLSS\_INTXBAR9\_G3 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR9_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.68 CONTROLSS\_INTXBAR9\_G4 Register

#### 1 CONTROLSS\_INTXBAR9\_G4 Register (Offset = 350h) [reset = 0h]

INT XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-2833. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5350h       |

**Figure 3-921. CONTROLSS\_INTXBAR9\_G4 Name Register**

|                 |    |    |    |    |    |                 |    |
|-----------------|----|----|----|----|----|-----------------|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25              | 24 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17              | 16 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9               | 8  |
| RESERVED        |    |    |    |    |    | INTXBAR9_G4_SEL |    |
| NONE            |    |    |    |    |    | R/W             |    |
| 0h              |    |    |    |    |    | 0h              |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1               | 0  |
| INTXBAR9_G4_SEL |    |    |    |    |    |                 |    |
| R/W             |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |

**Table 3-2835. CONTROLSS\_INTXBAR9\_G4 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR9_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.69 CONTROLSS\_INTXBAR9\_G5 Register

#### 1 CONTROLSS\_INTXBAR9\_G5 Register (Offset = 354h) [reset = 0h]

INT XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-2836. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5354h       |

**Figure 3-922. CONTROLSS\_INTXBAR9\_G5 Name Register**

|                 |    |    |    |    |    |                 |    |
|-----------------|----|----|----|----|----|-----------------|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25              | 24 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17              | 16 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9               | 8  |
| RESERVED        |    |    |    |    |    | INTXBAR9_G5_SEL |    |
| NONE            |    |    |    |    |    | R/W             |    |
| 0h              |    |    |    |    |    | 0h              |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1               | 0  |
| INTXBAR9_G5_SEL |    |    |    |    |    |                 |    |
| R/W             |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |

**Table 3-2838. CONTROLSS\_INTXBAR9\_G5 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                  |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR9_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.70 CONTROLSS\_INTXBAR9\_G6 Register

#### 1 CONTROLSS\_INTXBAR9\_G6 Register (Offset = 358h) [reset = 0h]

INT XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-2839. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5358h       |

**Figure 3-923. CONTROLSS\_INTXBAR9\_G6 Name Register**

|          |    |    |    |    |                 |    |    |
|----------|----|----|----|----|-----------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26              | 25 | 24 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 23       | 22 | 21 | 20 | 19 | 18              | 17 | 16 |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 15       | 14 | 13 | 12 | 11 | 10              | 9  | 8  |
| RESERVED |    |    |    |    |                 |    |    |
| NONE     |    |    |    |    |                 |    |    |
| 0h       |    |    |    |    |                 |    |    |
| 7        | 6  | 5  | 4  | 3  | 2               | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR9_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W             |    |    |
| 0h       |    |    |    |    | 0h              |    |    |

**Table 3-2841. CONTROLSS\_INTXBAR9\_G6 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED        | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR9_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.71 CONTROLSS\_INTXBAR10\_G0 Register

#### 1 CONTROLSS\_INTXBAR10\_G0 Register (Offset = 380h) [reset = 0h]

INT XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-2842. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5380h       |

**Figure 3-924. CONTROLSS\_INTXBAR10\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR10_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR10_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR10_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR10_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2844. CONTROLSS\_INTXBAR10\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR10_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.72 CONTROLSS\_INTXBAR10\_G1 Register

#### 1 CONTROLSS\_INTXBAR10\_G1 Register (Offset = 384h) [reset = 0h]

INT XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-2845. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5384h       |

**Figure 3-925. CONTROLSS\_INTXBAR10\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR10_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR10_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR10_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR10_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2847. CONTROLSS\_INTXBAR10\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                           |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR10_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.73 CONTROLSS\_INTXBAR10\_G2 Register

#### 1 CONTROLSS\_INTXBAR10\_G2 Register (Offset = 388h) [reset = 0h]

INT XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-2848. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5388h       |

**Figure 3-926. CONTROLSS\_INTXBAR10\_G2 Name Register**

|                  |    |    |    |    |    |    |                  |
|------------------|----|----|----|----|----|----|------------------|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24               |
| RESERVED         |    |    |    |    |    |    | INTXBAR10_G2_SEL |
| NONE             |    |    |    |    |    |    | R/W              |
| 0h               |    |    |    |    |    |    | 0h               |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16               |
| INTXBAR10_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8                |
| INTXBAR10_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0                |
| INTXBAR10_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |

**Table 3-2850. CONTROLSS\_INTXBAR10\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-2850. CONTROLSS\_INTXBAR10\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR10_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.74 CONTROLSS\_INTXBAR10\_G3 Register

#### 1 CONTROLSS\_INTXBAR10\_G3 Register (Offset = 38Ch) [reset = 0h]

INT XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-2851. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 538Ch       |

**Figure 3-927. CONTROLSS\_INTXBAR10\_G3 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR10_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR10_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2853. CONTROLSS\_INTXBAR10\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR10_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.75 CONTROLSS\_INTXBAR10\_G4 Register

#### 1 CONTROLSS\_INTXBAR10\_G4 Register (Offset = 390h) [reset = 0h]

INT XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-2854. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5390h       |

**Figure 3-928. CONTROLSS\_INTXBAR10\_G4 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR10_G4_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR10_G4_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-2856. CONTROLSS\_INTXBAR10\_G4 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR10_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.76 CONTROLSS\_INTXBAR10\_G5 Register

#### 1 CONTROLSS\_INTXBAR10\_G5 Register (Offset = 394h) [reset = 0h]

INT XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-2857. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5394h       |

**Figure 3-929. CONTROLSS\_INTXBAR10\_G5 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR10_G5_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR10_G5_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-2859. CONTROLSS\_INTXBAR10\_G5 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR10_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.77 CONTROLSS\_INTXBAR10\_G6 Register

#### 1 CONTROLSS\_INTXBAR10\_G6 Register (Offset = 398h) [reset = 0h]

INT XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-2860. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5398h       |

**Figure 3-930. CONTROLSS\_INTXBAR10\_G6 Name Register**

|          |    |    |    |    |                  |    |    |
|----------|----|----|----|----|------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26               | 25 | 24 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18               | 17 | 16 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10               | 9  | 8  |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR10_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W              |    |    |
| 0h       |    |    |    |    | 0h               |    |    |

**Table 3-2862. CONTROLSS\_INTXBAR10\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                         |
|------|------------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR10_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.78 CONTROLSS\_INTXBAR11\_G0 Register

#### 1 CONTROLSS\_INTXBAR11\_G0 Register (Offset = 3C0h) [reset = 0h]

INT XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-2863. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 53C0h       |

**Figure 3-931. CONTROLSS\_INTXBAR11\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR11_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR11_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR11_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR11_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2865. CONTROLSS\_INTXBAR11\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR11_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.79 CONTROLSS\_INTXBAR11\_G1 Register

#### 1 CONTROLSS\_INTXBAR11\_G1 Register (Offset = 3C4h) [reset = 0h]

INT XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-2866. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 53C4h       |

**Figure 3-932. CONTROLSS\_INTXBAR11\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR11_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR11_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR11_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR11_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2868. CONTROLSS\_INTXBAR11\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                           |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR11_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.80 CONTROLSS\_INTXBAR11\_G2 Register

#### 1 CONTROLSS\_INTXBAR11\_G2 Register (Offset = 3C8h) [reset = 0h]

INT XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-2869. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 53C8h       |

**Figure 3-933. CONTROLSS\_INTXBAR11\_G2 Name Register**

|                  |    |    |    |    |    |    |                  |
|------------------|----|----|----|----|----|----|------------------|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24               |
| RESERVED         |    |    |    |    |    |    | INTXBAR11_G2_SEL |
| NONE             |    |    |    |    |    |    | R/W              |
| 0h               |    |    |    |    |    |    | 0h               |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16               |
| INTXBAR11_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8                |
| INTXBAR11_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0                |
| INTXBAR11_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |

**Table 3-2871. CONTROLSS\_INTXBAR11\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-2871. CONTROLSS\_INTXBAR11\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR11_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.81 CONTROLSS\_INTXBAR11\_G3 Register

#### 1 CONTROLSS\_INTXBAR11\_G3 Register (Offset = 3CCh) [reset = 0h]

INT XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-2872. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 53CCh       |

**Figure 3-934. CONTROLSS\_INTXBAR11\_G3 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR11_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR11_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2874. CONTROLSS\_INTXBAR11\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR11_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.82 CONTROLSS\_INTXBAR11\_G4 Register

#### 1 CONTROLSS\_INTXBAR11\_G4 Register (Offset = 3D0h) [reset = 0h]

INT XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-2875. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 53D0h       |

**Figure 3-935. CONTROLSS\_INTXBAR11\_G4 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR11_G4_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR11_G4_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-2877. CONTROLSS\_INTXBAR11\_G4 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR11_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.83 CONTROLSS\_INTXBAR11\_G5 Register

#### 1 CONTROLSS\_INTXBAR11\_G5 Register (Offset = 3D4h) [reset = 0h]

INT XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-2878. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 53D4h       |

**Figure 3-936. CONTROLSS\_INTXBAR11\_G5 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR11_G5_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR11_G5_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-2880. CONTROLSS\_INTXBAR11\_G5 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR11_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.84 CONTROLSS\_INTXBAR11\_G6 Register

#### 1 CONTROLSS\_INTXBAR11\_G6 Register (Offset = 3D8h) [reset = 0h]

INT XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-2881. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 53D8h       |

**Figure 3-937. CONTROLSS\_INTXBAR11\_G6 Name Register**

|          |    |    |    |    |                  |    |    |
|----------|----|----|----|----|------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26               | 25 | 24 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18               | 17 | 16 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10               | 9  | 8  |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR11_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W              |    |    |
| 0h       |    |    |    |    | 0h               |    |    |

**Table 3-2883. CONTROLSS\_INTXBAR11\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                         |
|------|------------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR11_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.85 CONTROLSS\_INTXBAR12\_G0 Register

#### 1 CONTROLSS\_INTXBAR12\_G0 Register (Offset = 400h) [reset = 0h]

INT XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-2884. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5400h       |

**Figure 3-938. CONTROLSS\_INTXBAR12\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR12_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR12_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR12_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR12_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2886. CONTROLSS\_INTXBAR12\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR12_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.86 CONTROLSS\_INTXBAR12\_G1 Register

#### 1 CONTROLSS\_INTXBAR12\_G1 Register (Offset = 404h) [reset = 0h]

INT XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-2887. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5404h       |

**Figure 3-939. CONTROLSS\_INTXBAR12\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR12_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR12_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR12_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR12_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2889. CONTROLSS\_INTXBAR12\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                           |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR12_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.87 CONTROLSS\_INTXBAR12\_G2 Register

#### 1 CONTROLSS\_INTXBAR12\_G2 Register (Offset = 408h) [reset = 0h]

INT XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-2890. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5408h       |

**Figure 3-940. CONTROLSS\_INTXBAR12\_G2 Name Register**

|                  |    |    |    |    |    |    |                  |
|------------------|----|----|----|----|----|----|------------------|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24               |
| RESERVED         |    |    |    |    |    |    | INTXBAR12_G2_SEL |
| NONE             |    |    |    |    |    |    | R/W              |
| 0h               |    |    |    |    |    |    | 0h               |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16               |
| INTXBAR12_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8                |
| INTXBAR12_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0                |
| INTXBAR12_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |

**Table 3-2892. CONTROLSS\_INTXBAR12\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-2892. CONTROLSS\_INTXBAR12\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR12_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.88 CONTROLSS\_INTXBAR12\_G3 Register

#### 1 CONTROLSS\_INTXBAR12\_G3 Register (Offset = 40Ch) [reset = 0h]

INT XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-2893. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 540Ch       |

**Figure 3-941. CONTROLSS\_INTXBAR12\_G3 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR12_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR12_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2895. CONTROLSS\_INTXBAR12\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR12_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.89 CONTROLSS\_INTXBAR12\_G4 Register

#### 1 CONTROLSS\_INTXBAR12\_G4 Register (Offset = 410h) [reset = 0h]

INT XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-2896. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5410h       |

**Figure 3-942. CONTROLSS\_INTXBAR12\_G4 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR12_G4_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR12_G4_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-2898. CONTROLSS\_INTXBAR12\_G4 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR12_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.90 CONTROLSS\_INTXBAR12\_G5 Register

#### 1 CONTROLSS\_INTXBAR12\_G5 Register (Offset = 414h) [reset = 0h]

INT XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-2899. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5414h       |

**Figure 3-943. CONTROLSS\_INTXBAR12\_G5 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR12_G5_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR12_G5_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-2901. CONTROLSS\_INTXBAR12\_G5 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR12_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.91 CONTROLSS\_INTXBAR12\_G6 Register

#### 1 CONTROLSS\_INTXBAR12\_G6 Register (Offset = 418h) [reset = 0h]

INT XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-2902. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5418h       |

**Figure 3-944. CONTROLSS\_INTXBAR12\_G6 Name Register**

|          |    |    |    |    |                  |    |    |
|----------|----|----|----|----|------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26               | 25 | 24 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18               | 17 | 16 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10               | 9  | 8  |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR12_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W              |    |    |
| 0h       |    |    |    |    | 0h               |    |    |

**Table 3-2904. CONTROLSS\_INTXBAR12\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                         |
|------|------------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR12_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.92 CONTROLSS\_INTXBAR13\_G0 Register

#### 1 CONTROLSS\_INTXBAR13\_G0 Register (Offset = 440h) [reset = 0h]

INT XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-2905. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5440h       |

**Figure 3-945. CONTROLSS\_INTXBAR13\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR13_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR13_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR13_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR13_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2907. CONTROLSS\_INTXBAR13\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR13_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.93 CONTROLSS\_INTXBAR13\_G1 Register

#### 1 CONTROLSS\_INTXBAR13\_G1 Register (Offset = 444h) [reset = 0h]

INT XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-2908. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5444h       |

**Figure 3-946. CONTROLSS\_INTXBAR13\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR13_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR13_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR13_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR13_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2910. CONTROLSS\_INTXBAR13\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                           |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR13_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.94 CONTROLSS\_INTXBAR13\_G2 Register

#### 1 CONTROLSS\_INTXBAR13\_G2 Register (Offset = 448h) [reset = 0h]

INT XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-2911. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5448h       |

**Figure 3-947. CONTROLSS\_INTXBAR13\_G2 Name Register**

|                  |    |    |    |    |    |    |                  |
|------------------|----|----|----|----|----|----|------------------|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24               |
| RESERVED         |    |    |    |    |    |    | INTXBAR13_G2_SEL |
| NONE             |    |    |    |    |    |    | R/W              |
| 0h               |    |    |    |    |    |    | 0h               |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16               |
| INTXBAR13_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8                |
| INTXBAR13_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0                |
| INTXBAR13_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |

**Table 3-2913. CONTROLSS\_INTXBAR13\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-2913. CONTROLSS\_INTXBAR13\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR13_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.95 CONTROLSS\_INTXBAR13\_G3 Register

#### 1 CONTROLSS\_INTXBAR13\_G3 Register (Offset = 44Ch) [reset = 0h]

INT XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-2914. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 544Ch       |

**Figure 3-948. CONTROLSS\_INTXBAR13\_G3 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR13_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR13_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2916. CONTROLSS\_INTXBAR13\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR13_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.96 CONTROLSS\_INTXBAR13\_G4 Register

#### 1 CONTROLSS\_INTXBAR13\_G4 Register (Offset = 450h) [reset = 0h]

INT XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-2917. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5450h       |

**Figure 3-949. CONTROLSS\_INTXBAR13\_G4 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR13_G4_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR13_G4_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-2919. CONTROLSS\_INTXBAR13\_G4 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR13_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.97 CONTROLSS\_INTXBAR13\_G5 Register

#### 1 CONTROLSS\_INTXBAR13\_G5 Register (Offset = 454h) [reset = 0h]

INT XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-2920. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5454h       |

**Figure 3-950. CONTROLSS\_INTXBAR13\_G5 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR13_G5_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR13_G5_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-2922. CONTROLSS\_INTXBAR13\_G5 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR13_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.98 CONTROLSS\_INTXBAR13\_G6 Register

#### 1 CONTROLSS\_INTXBAR13\_G6 Register (Offset = 458h) [reset = 0h]

INT XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-2923. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5458h       |

**Figure 3-951. CONTROLSS\_INTXBAR13\_G6 Name Register**

|          |    |    |    |    |                  |    |    |
|----------|----|----|----|----|------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26               | 25 | 24 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18               | 17 | 16 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10               | 9  | 8  |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR13_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W              |    |    |
| 0h       |    |    |    |    | 0h               |    |    |

**Table 3-2925. CONTROLSS\_INTXBAR13\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                         |
|------|------------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR13_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.99 CONTROLSS\_INTXBAR14\_G0 Register

#### 1 CONTROLSS\_INTXBAR14\_G0 Register (Offset = 480h) [reset = 0h]

INT XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-2926. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5480h       |

**Figure 3-952. CONTROLSS\_INTXBAR14\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR14_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR14_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR14_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR14_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2928. CONTROLSS\_INTXBAR14\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR14_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.100 CONTROLSS\_INTXBAR14\_G1 Register

#### 1 CONTROLSS\_INTXBAR14\_G1 Register (Offset = 484h) [reset = 0h]

INT XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-2929. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5484h       |

**Figure 3-953. CONTROLSS\_INTXBAR14\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR14_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR14_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR14_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR14_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2931. CONTROLSS\_INTXBAR14\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                           |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR14_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.101 CONTROLSS\_INTXBAR14\_G2 Register

#### 1 CONTROLSS\_INTXBAR14\_G2 Register (Offset = 488h) [reset = 0h]

INT XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-2932. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5488h       |

**Figure 3-954. CONTROLSS\_INTXBAR14\_G2 Name Register**

|                  |    |    |    |    |    |    |                  |
|------------------|----|----|----|----|----|----|------------------|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24               |
| RESERVED         |    |    |    |    |    |    | INTXBAR14_G2_SEL |
| NONE             |    |    |    |    |    |    | R/W              |
| 0h               |    |    |    |    |    |    | 0h               |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16               |
| INTXBAR14_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8                |
| INTXBAR14_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0                |
| INTXBAR14_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |

**Table 3-2934. CONTROLSS\_INTXBAR14\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-2934. CONTROLSS\_INTXBAR14\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR14_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.102 CONTROLSS\_INTXBAR14\_G3 Register

#### 1 CONTROLSS\_INTXBAR14\_G3 Register (Offset = 48Ch) [reset = 0h]

INT XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-2935. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 548Ch       |

**Figure 3-955. CONTROLSS\_INTXBAR14\_G3 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR14_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR14_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2937. CONTROLSS\_INTXBAR14\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR14_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.103 CONTROLSS\_INTXBAR14\_G4 Register

#### 1 CONTROLSS\_INTXBAR14\_G4 Register (Offset = 490h) [reset = 0h]

INT XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-2938. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5490h       |

**Figure 3-956. CONTROLSS\_INTXBAR14\_G4 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR14_G4_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR14_G4_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-2940. CONTROLSS\_INTXBAR14\_G4 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR14_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.104 CONTROLSS\_INTXBAR14\_G5 Register

#### 1 CONTROLSS\_INTXBAR14\_G5 Register (Offset = 494h) [reset = 0h]

INT XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-2941. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5494h       |

**Figure 3-957. CONTROLSS\_INTXBAR14\_G5 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR14_G5_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR14_G5_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-2943. CONTROLSS\_INTXBAR14\_G5 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR14_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.105 CONTROLSS\_INTXBAR14\_G6 Register

#### 1 CONTROLSS\_INTXBAR14\_G6 Register (Offset = 498h) [reset = 0h]

INT XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-2944. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5498h       |

**Figure 3-958. CONTROLSS\_INTXBAR14\_G6 Name Register**

|          |    |    |    |    |                  |    |    |
|----------|----|----|----|----|------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26               | 25 | 24 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18               | 17 | 16 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10               | 9  | 8  |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR14_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W              |    |    |
| 0h       |    |    |    |    | 0h               |    |    |

**Table 3-2946. CONTROLSS\_INTXBAR14\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                         |
|------|------------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR14_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.106 CONTROLSS\_INTXBAR15\_G0 Register

#### 1 CONTROLSS\_INTXBAR15\_G0 Register (Offset = 4C0h) [reset = 0h]

INT XBAR 15 Input Select.

Return to [Summary Table](#)

**Table 3-2947. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 54C0h       |

**Figure 3-959. CONTROLSS\_INTXBAR15\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR15_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR15_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR15_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR15_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2949. CONTROLSS\_INTXBAR15\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR15_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.107 CONTROLSS\_INTXBAR15\_G1 Register

#### 1 CONTROLSS\_INTXBAR15\_G1 Register (Offset = 4C4h) [reset = 0h]

INT XBAR 15 Input Select.

Return to [Summary Table](#)

**Table 3-2950. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 54C4h       |

**Figure 3-960. CONTROLSS\_INTXBAR15\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR15_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR15_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR15_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR15_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2952. CONTROLSS\_INTXBAR15\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                           |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR15_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.108 CONTROLSS\_INTXBAR15\_G2 Register

#### 1 CONTROLSS\_INTXBAR15\_G2 Register (Offset = 4C8h) [reset = 0h]

INT XBAR 15 Input Select.

Return to [Summary Table](#)

**Table 3-2953. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 54C8h       |

**Figure 3-961. CONTROLSS\_INTXBAR15\_G2 Name Register**

|                  |    |    |    |    |    |    |                  |
|------------------|----|----|----|----|----|----|------------------|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24               |
| RESERVED         |    |    |    |    |    |    | INTXBAR15_G2_SEL |
| NONE             |    |    |    |    |    |    | R/W              |
| 0h               |    |    |    |    |    |    | 0h               |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16               |
| INTXBAR15_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8                |
| INTXBAR15_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0                |
| INTXBAR15_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |

**Table 3-2955. CONTROLSS\_INTXBAR15\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-2955. CONTROLSS\_INTXBAR15\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR15_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.109 CONTROLSS\_INTXBAR15\_G3 Register

#### 1 CONTROLSS\_INTXBAR15\_G3 Register (Offset = 4CCh) [reset = 0h]

INT XBAR 15 Input Select.

Return to [Summary Table](#)

**Table 3-2956. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 54CCh       |

**Figure 3-962. CONTROLSS\_INTXBAR15\_G3 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR15_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR15_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2958. CONTROLSS\_INTXBAR15\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR15_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.110 CONTROLSS\_INTXBAR15\_G4 Register

#### 1 CONTROLSS\_INTXBAR15\_G4 Register (Offset = 4D0h) [reset = 0h]

INT XBAR 15 Input Select.

Return to [Summary Table](#)

**Table 3-2959. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 54D0h       |

**Figure 3-963. CONTROLSS\_INTXBAR15\_G4 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR15_G4_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR15_G4_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-2961. CONTROLSS\_INTXBAR15\_G4 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR15_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.111 CONTROLSS\_INTXBAR15\_G5 Register

#### 1 CONTROLSS\_INTXBAR15\_G5 Register (Offset = 4D4h) [reset = 0h]

INT XBAR 15 Input Select.

Return to [Summary Table](#)

**Table 3-2962. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 54D4h       |

**Figure 3-964. CONTROLSS\_INTXBAR15\_G5 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR15_G5_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR15_G5_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-2964. CONTROLSS\_INTXBAR15\_G5 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR15_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.112 CONTROLSS\_INTXBAR15\_G6 Register

#### 1 CONTROLSS\_INTXBAR15\_G6 Register (Offset = 4D8h) [reset = 0h]

INT XBAR 15 Input Select.

Return to [Summary Table](#)

**Table 3-2965. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 54D8h       |

**Figure 3-965. CONTROLSS\_INTXBAR15\_G6 Name Register**

|          |    |    |    |    |                  |    |    |
|----------|----|----|----|----|------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26               | 25 | 24 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18               | 17 | 16 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10               | 9  | 8  |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR15_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W              |    |    |
| 0h       |    |    |    |    | 0h               |    |    |

**Table 3-2967. CONTROLSS\_INTXBAR15\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                         |
|------|------------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR15_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.113 CONTROLSS\_INTXBAR16\_G0 Register

#### 1 CONTROLSS\_INTXBAR16\_G0 Register (Offset = 500h) [reset = 0h]

INT XBAR 16 Input Select.

Return to [Summary Table](#)

**Table 3-2968. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5500h       |

**Figure 3-966. CONTROLSS\_INTXBAR16\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR16_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR16_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR16_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR16_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2970. CONTROLSS\_INTXBAR16\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR16_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.114 CONTROLSS\_INTXBAR16\_G1 Register

#### 1 CONTROLSS\_INTXBAR16\_G1 Register (Offset = 504h) [reset = 0h]

INT XBAR 16 Input Select.

Return to [Summary Table](#)

**Table 3-2971. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5504h       |

**Figure 3-967. CONTROLSS\_INTXBAR16\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR16_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR16_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR16_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR16_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2973. CONTROLSS\_INTXBAR16\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                           |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR16_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.115 CONTROLSS\_INTXBAR16\_G2 Register

#### 1 CONTROLSS\_INTXBAR16\_G2 Register (Offset = 508h) [reset = 0h]

INT XBAR 16 Input Select.

Return to [Summary Table](#)

**Table 3-2974. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5508h       |

**Figure 3-968. CONTROLSS\_INTXBAR16\_G2 Name Register**

|                  |    |    |    |    |    |    |                  |
|------------------|----|----|----|----|----|----|------------------|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24               |
| RESERVED         |    |    |    |    |    |    | INTXBAR16_G2_SEL |
| NONE             |    |    |    |    |    |    | R/W              |
| 0h               |    |    |    |    |    |    | 0h               |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16               |
| INTXBAR16_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8                |
| INTXBAR16_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0                |
| INTXBAR16_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |

**Table 3-2976. CONTROLSS\_INTXBAR16\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-2976. CONTROLSS\_INTXBAR16\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR16_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.116 CONTROLSS\_INTXBAR16\_G3 Register

#### 1 CONTROLSS\_INTXBAR16\_G3 Register (Offset = 50Ch) [reset = 0h]

INT XBAR 16 Input Select.

Return to [Summary Table](#)

**Table 3-2977. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 550Ch       |

**Figure 3-969. CONTROLSS\_INTXBAR16\_G3 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR16_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR16_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2979. CONTROLSS\_INTXBAR16\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR16_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.117 CONTROLSS\_INTXBAR16\_G4 Register

#### 1 CONTROLSS\_INTXBAR16\_G4 Register (Offset = 510h) [reset = 0h]

INT XBAR 16 Input Select.

Return to [Summary Table](#)

**Table 3-2980. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5510h       |

**Figure 3-970. CONTROLSS\_INTXBAR16\_G4 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR16_G4_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR16_G4_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-2982. CONTROLSS\_INTXBAR16\_G4 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR16_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.118 CONTROLSS\_INTXBAR16\_G5 Register

#### 1 CONTROLSS\_INTXBAR16\_G5 Register (Offset = 514h) [reset = 0h]

INT XBAR 16 Input Select.

Return to [Summary Table](#)

**Table 3-2983. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5514h       |

**Figure 3-971. CONTROLSS\_INTXBAR16\_G5 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR16_G5_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR16_G5_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-2985. CONTROLSS\_INTXBAR16\_G5 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR16_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.119 CONTROLSS\_INTXBAR16\_G6 Register

#### 1 CONTROLSS\_INTXBAR16\_G6 Register (Offset = 518h) [reset = 0h]

INT XBAR 16 Input Select.

Return to [Summary Table](#)

**Table 3-2986. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5518h       |

**Figure 3-972. CONTROLSS\_INTXBAR16\_G6 Name Register**

|          |    |    |    |    |                  |    |    |
|----------|----|----|----|----|------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26               | 25 | 24 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18               | 17 | 16 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10               | 9  | 8  |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR16_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W              |    |    |
| 0h       |    |    |    |    | 0h               |    |    |

**Table 3-2988. CONTROLSS\_INTXBAR16\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                         |
|------|------------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR16_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.120 CONTROLSS\_INTXBAR17\_G0 Register

#### 1 CONTROLSS\_INTXBAR17\_G0 Register (Offset = 540h) [reset = 0h]

INT XBAR 17 Input Select.

Return to [Summary Table](#)

**Table 3-2989. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5540h       |

**Figure 3-973. CONTROLSS\_INTXBAR17\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR17_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR17_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR17_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR17_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2991. CONTROLSS\_INTXBAR17\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR17_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.121 CONTROLSS\_INTXBAR17\_G1 Register

#### 1 CONTROLSS\_INTXBAR17\_G1 Register (Offset = 544h) [reset = 0h]

INT XBAR 17 Input Select.

Return to [Summary Table](#)

**Table 3-2992. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5544h       |

**Figure 3-974. CONTROLSS\_INTXBAR17\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR17_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR17_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR17_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR17_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-2994. CONTROLSS\_INTXBAR17\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                           |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR17_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.122 CONTROLSS\_INTXBAR17\_G2 Register

#### 1 CONTROLSS\_INTXBAR17\_G2 Register (Offset = 548h) [reset = 0h]

INT XBAR 17 Input Select.

Return to [Summary Table](#)

**Table 3-2995. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5548h       |

**Figure 3-975. CONTROLSS\_INTXBAR17\_G2 Name Register**

|                  |    |    |    |    |    |    |                  |
|------------------|----|----|----|----|----|----|------------------|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24               |
| RESERVED         |    |    |    |    |    |    | INTXBAR17_G2_SEL |
| NONE             |    |    |    |    |    |    | R/W              |
| 0h               |    |    |    |    |    |    | 0h               |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16               |
| INTXBAR17_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8                |
| INTXBAR17_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0                |
| INTXBAR17_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |

**Table 3-2997. CONTROLSS\_INTXBAR17\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-2997. CONTROLSS\_INTXBAR17\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR17_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.123 CONTROLSS\_INTXBAR17\_G3 Register

#### 1 CONTROLSS\_INTXBAR17\_G3 Register (Offset = 54Ch) [reset = 0h]

INT XBAR 17 Input Select.

Return to [Summary Table](#)

**Table 3-2998. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 554Ch       |

**Figure 3-976. CONTROLSS\_INTXBAR17\_G3 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR17_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR17_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3000. CONTROLSS\_INTXBAR17\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR17_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.124 CONTROLSS\_INTXBAR17\_G4 Register

#### 1 CONTROLSS\_INTXBAR17\_G4 Register (Offset = 550h) [reset = 0h]

INT XBAR 17 Input Select.

Return to [Summary Table](#)

**Table 3-3001. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5550h       |

**Figure 3-977. CONTROLSS\_INTXBAR17\_G4 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR17_G4_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR17_G4_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3003. CONTROLSS\_INTXBAR17\_G4 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR17_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.125 CONTROLSS\_INTXBAR17\_G5 Register

#### 1 CONTROLSS\_INTXBAR17\_G5 Register (Offset = 554h) [reset = 0h]

INT XBAR 17 Input Select.

Return to [Summary Table](#)

**Table 3-3004. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5554h       |

**Figure 3-978. CONTROLSS\_INTXBAR17\_G5 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR17_G5_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR17_G5_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3006. CONTROLSS\_INTXBAR17\_G5 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR17_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.126 CONTROLSS\_INTXBAR17\_G6 Register

#### 1 CONTROLSS\_INTXBAR17\_G6 Register (Offset = 558h) [reset = 0h]

INT XBAR 17 Input Select.

Return to [Summary Table](#)

**Table 3-3007. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5558h       |

**Figure 3-979. CONTROLSS\_INTXBAR17\_G6 Name Register**

|          |    |    |    |    |                  |    |    |
|----------|----|----|----|----|------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26               | 25 | 24 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18               | 17 | 16 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10               | 9  | 8  |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR17_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W              |    |    |
| 0h       |    |    |    |    | 0h               |    |    |

**Table 3-3009. CONTROLSS\_INTXBAR17\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                         |
|------|------------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR17_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.127 CONTROLSS\_INTXBAR18\_G0 Register

#### 1 CONTROLSS\_INTXBAR18\_G0 Register (Offset = 580h) [reset = 0h]

INT XBAR 18 Input Select.

Return to [Summary Table](#)

**Table 3-3010. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5580h       |

**Figure 3-980. CONTROLSS\_INTXBAR18\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR18_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR18_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR18_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR18_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3012. CONTROLSS\_INTXBAR18\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR18_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.128 CONTROLSS\_INTXBAR18\_G1 Register

#### 1 CONTROLSS\_INTXBAR18\_G1 Register (Offset = 584h) [reset = 0h]

INT XBAR 18 Input Select.

Return to [Summary Table](#)

**Table 3-3013. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5584h       |

**Figure 3-981. CONTROLSS\_INTXBAR18\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR18_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR18_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR18_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR18_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3015. CONTROLSS\_INTXBAR18\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                           |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR18_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.129 CONTROLSS\_INTXBAR18\_G2 Register

#### 1 CONTROLSS\_INTXBAR18\_G2 Register (Offset = 588h) [reset = 0h]

INT XBAR 18 Input Select.

Return to [Summary Table](#)

**Table 3-3016. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5588h       |

**Figure 3-982. CONTROLSS\_INTXBAR18\_G2 Name Register**

|                  |    |    |    |    |    |    |                  |
|------------------|----|----|----|----|----|----|------------------|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24               |
| RESERVED         |    |    |    |    |    |    | INTXBAR18_G2_SEL |
| NONE             |    |    |    |    |    |    | R/W              |
| 0h               |    |    |    |    |    |    | 0h               |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16               |
| INTXBAR18_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8                |
| INTXBAR18_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0                |
| INTXBAR18_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |

**Table 3-3018. CONTROLSS\_INTXBAR18\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3018. CONTROLSS\_INTXBAR18\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR18_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.130 CONTROLSS\_INTXBAR18\_G3 Register

#### 1 CONTROLSS\_INTXBAR18\_G3 Register (Offset = 58Ch) [reset = 0h]

INT XBAR 18 Input Select.

Return to [Summary Table](#)

**Table 3-3019. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 558Ch       |

**Figure 3-983. CONTROLSS\_INTXBAR18\_G3 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR18_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR18_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3021. CONTROLSS\_INTXBAR18\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR18_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.131 CONTROLSS\_INTXBAR18\_G4 Register

#### 1 CONTROLSS\_INTXBAR18\_G4 Register (Offset = 590h) [reset = 0h]

INT XBAR 18 Input Select.

Return to [Summary Table](#)

**Table 3-3022. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5590h       |

**Figure 3-984. CONTROLSS\_INTXBAR18\_G4 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR18_G4_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR18_G4_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3024. CONTROLSS\_INTXBAR18\_G4 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR18_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.132 CONTROLSS\_INTXBAR18\_G5 Register

#### 1 CONTROLSS\_INTXBAR18\_G5 Register (Offset = 594h) [reset = 0h]

INT XBAR 18 Input Select.

Return to [Summary Table](#)

**Table 3-3025. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5594h       |

**Figure 3-985. CONTROLSS\_INTXBAR18\_G5 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR18_G5_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR18_G5_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3027. CONTROLSS\_INTXBAR18\_G5 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR18_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.133 CONTROLSS\_INTXBAR18\_G6 Register

#### 1 CONTROLSS\_INTXBAR18\_G6 Register (Offset = 598h) [reset = 0h]

INT XBAR 18 Input Select.

Return to [Summary Table](#)

**Table 3-3028. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5598h       |

**Figure 3-986. CONTROLSS\_INTXBAR18\_G6 Name Register**

|          |    |    |    |    |                  |    |    |
|----------|----|----|----|----|------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26               | 25 | 24 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18               | 17 | 16 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10               | 9  | 8  |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR18_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W              |    |    |
| 0h       |    |    |    |    | 0h               |    |    |

**Table 3-3030. CONTROLSS\_INTXBAR18\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                         |
|------|------------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR18_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.134 CONTROLSS\_INTXBAR19\_G0 Register

#### 1 CONTROLSS\_INTXBAR19\_G0 Register (Offset = 5C0h) [reset = 0h]

INT XBAR 19 Input Select.

Return to [Summary Table](#)

**Table 3-3031. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 55C0h       |

**Figure 3-987. CONTROLSS\_INTXBAR19\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR19_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR19_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR19_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR19_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3033. CONTROLSS\_INTXBAR19\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR19_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.135 CONTROLSS\_INTXBAR19\_G1 Register

#### 1 CONTROLSS\_INTXBAR19\_G1 Register (Offset = 5C4h) [reset = 0h]

INT XBAR 19 Input Select.

Return to [Summary Table](#)

**Table 3-3034. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 55C4h       |

**Figure 3-988. CONTROLSS\_INTXBAR19\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR19_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR19_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR19_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR19_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3036. CONTROLSS\_INTXBAR19\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                           |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR19_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.136 CONTROLSS\_INTXBAR19\_G2 Register

#### 1 CONTROLSS\_INTXBAR19\_G2 Register (Offset = 5C8h) [reset = 0h]

INT XBAR 19 Input Select.

Return to [Summary Table](#)

**Table 3-3037. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 55C8h       |

**Figure 3-989. CONTROLSS\_INTXBAR19\_G2 Name Register**

|                  |    |    |    |    |    |    |                  |
|------------------|----|----|----|----|----|----|------------------|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24               |
| RESERVED         |    |    |    |    |    |    | INTXBAR19_G2_SEL |
| NONE             |    |    |    |    |    |    | R/W              |
| 0h               |    |    |    |    |    |    | 0h               |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16               |
| INTXBAR19_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8                |
| INTXBAR19_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0                |
| INTXBAR19_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |

**Table 3-3039. CONTROLSS\_INTXBAR19\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3039. CONTROLSS\_INTXBAR19\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR19_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.137 CONTROLSS\_INTXBAR19\_G3 Register

#### 1 CONTROLSS\_INTXBAR19\_G3 Register (Offset = 5CCh) [reset = 0h]

INT XBAR 19 Input Select.

Return to [Summary Table](#)

**Table 3-3040. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 55CCh       |

**Figure 3-990. CONTROLSS\_INTXBAR19\_G3 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR19_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR19_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3042. CONTROLSS\_INTXBAR19\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR19_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.138 CONTROLSS\_INTXBAR19\_G4 Register

#### 1 CONTROLSS\_INTXBAR19\_G4 Register (Offset = 5D0h) [reset = 0h]

INT XBAR 19 Input Select.

Return to [Summary Table](#)

**Table 3-3043. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 55D0h       |

**Figure 3-991. CONTROLSS\_INTXBAR19\_G4 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR19_G4_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR19_G4_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3045. CONTROLSS\_INTXBAR19\_G4 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR19_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.139 CONTROLSS\_INTXBAR19\_G5 Register

#### 1 CONTROLSS\_INTXBAR19\_G5 Register (Offset = 5D4h) [reset = 0h]

INT XBAR 19 Input Select.

Return to [Summary Table](#)

**Table 3-3046. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 55D4h       |

**Figure 3-992. CONTROLSS\_INTXBAR19\_G5 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR19_G5_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR19_G5_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3048. CONTROLSS\_INTXBAR19\_G5 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR19_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.140 CONTROLSS\_INTXBAR19\_G6 Register

#### 1 CONTROLSS\_INTXBAR19\_G6 Register (Offset = 5D8h) [reset = 0h]

INT XBAR 19 Input Select.

Return to [Summary Table](#)

**Table 3-3049. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 55D8h       |

**Figure 3-993. CONTROLSS\_INTXBAR19\_G6 Name Register**

|          |    |    |    |    |                  |    |    |
|----------|----|----|----|----|------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26               | 25 | 24 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18               | 17 | 16 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10               | 9  | 8  |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR19_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W              |    |    |
| 0h       |    |    |    |    | 0h               |    |    |

**Table 3-3051. CONTROLSS\_INTXBAR19\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                         |
|------|------------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR19_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.141 CONTROLSS\_INTXBAR20\_G0 Register

#### 1 CONTROLSS\_INTXBAR20\_G0 Register (Offset = 600h) [reset = 0h]

INT XBAR 20 Input Select.

Return to [Summary Table](#)

**Table 3-3052. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5600h       |

**Figure 3-994. CONTROLSS\_INTXBAR20\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR20_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR20_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR20_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR20_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3054. CONTROLSS\_INTXBAR20\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR20_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.142 CONTROLSS\_INTXBAR20\_G1 Register

#### 1 CONTROLSS\_INTXBAR20\_G1 Register (Offset = 604h) [reset = 0h]

INT XBAR 20 Input Select.

Return to [Summary Table](#)

**Table 3-3055. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5604h       |

**Figure 3-995. CONTROLSS\_INTXBAR20\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR20_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR20_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR20_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR20_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3057. CONTROLSS\_INTXBAR20\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                           |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR20_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.143 CONTROLSS\_INTXBAR20\_G2 Register

#### 1 CONTROLSS\_INTXBAR20\_G2 Register (Offset = 608h) [reset = 0h]

INT XBAR 20 Input Select.

Return to [Summary Table](#)

**Table 3-3058. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5608h       |

**Figure 3-996. CONTROLSS\_INTXBAR20\_G2 Name Register**

|                  |    |    |    |    |    |    |                  |
|------------------|----|----|----|----|----|----|------------------|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24               |
| RESERVED         |    |    |    |    |    |    | INTXBAR20_G2_SEL |
| NONE             |    |    |    |    |    |    | R/W              |
| 0h               |    |    |    |    |    |    | 0h               |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16               |
| INTXBAR20_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8                |
| INTXBAR20_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0                |
| INTXBAR20_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |

**Table 3-3060. CONTROLSS\_INTXBAR20\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3060. CONTROLSS\_INTXBAR20\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR20_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.144 CONTROLSS\_INTXBAR20\_G3 Register

#### 1 CONTROLSS\_INTXBAR20\_G3 Register (Offset = 60Ch) [reset = 0h]

INT XBAR 20 Input Select.

Return to [Summary Table](#)

**Table 3-3061. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 560Ch       |

**Figure 3-997. CONTROLSS\_INTXBAR20\_G3 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR20_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR20_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3063. CONTROLSS\_INTXBAR20\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR20_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.145 CONTROLSS\_INTXBAR20\_G4 Register

#### 1 CONTROLSS\_INTXBAR20\_G4 Register (Offset = 610h) [reset = 0h]

INT XBAR 20 Input Select.

Return to [Summary Table](#)

**Table 3-3064. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5610h       |

**Figure 3-998. CONTROLSS\_INTXBAR20\_G4 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR20_G4_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR20_G4_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3066. CONTROLSS\_INTXBAR20\_G4 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR20_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.146 CONTROLSS\_INTXBAR20\_G5 Register

#### 1 CONTROLSS\_INTXBAR20\_G5 Register (Offset = 614h) [reset = 0h]

INT XBAR 20 Input Select.

Return to [Summary Table](#)

**Table 3-3067. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5614h       |

**Figure 3-999. CONTROLSS\_INTXBAR20\_G5 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR20_G5_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR20_G5_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3069. CONTROLSS\_INTXBAR20\_G5 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR20_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.147 CONTROLSS\_INTXBAR20\_G6 Register

#### 1 CONTROLSS\_INTXBAR20\_G6 Register (Offset = 618h) [reset = 0h]

INT XBAR 20 Input Select.

Return to [Summary Table](#)

**Table 3-3070. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5618h       |

**Figure 3-1000. CONTROLSS\_INTXBAR20\_G6 Name Register**

|          |    |    |    |    |                  |    |    |
|----------|----|----|----|----|------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26               | 25 | 24 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18               | 17 | 16 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10               | 9  | 8  |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR20_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W              |    |    |
| 0h       |    |    |    |    | 0h               |    |    |

**Table 3-3072. CONTROLSS\_INTXBAR20\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                         |
|------|------------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR20_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.148 CONTROLSS\_INTXBAR21\_G0 Register

#### 1 CONTROLSS\_INTXBAR21\_G0 Register (Offset = 640h) [reset = 0h]

INT XBAR 21 Input Select.

Return to [Summary Table](#)

**Table 3-3073. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5640h       |

**Figure 3-1001. CONTROLSS\_INTXBAR21\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR21_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR21_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR21_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR21_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3075. CONTROLSS\_INTXBAR21\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR21_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.149 CONTROLSS\_INTXBAR21\_G1 Register

#### 1 CONTROLSS\_INTXBAR21\_G1 Register (Offset = 644h) [reset = 0h]

INT XBAR 21 Input Select.

Return to [Summary Table](#)

**Table 3-3076. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5644h       |

**Figure 3-1002. CONTROLSS\_INTXBAR21\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR21_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR21_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR21_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR21_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3078. CONTROLSS\_INTXBAR21\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                           |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR21_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.150 CONTROLSS\_INTXBAR21\_G2 Register

#### 1 CONTROLSS\_INTXBAR21\_G2 Register (Offset = 648h) [reset = 0h]

INT XBAR 21 Input Select.

Return to [Summary Table](#)

**Table 3-3079. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5648h       |

**Figure 3-1003. CONTROLSS\_INTXBAR21\_G2 Name Register**

|                  |    |    |    |    |    |    |                  |
|------------------|----|----|----|----|----|----|------------------|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24               |
| RESERVED         |    |    |    |    |    |    | INTXBAR21_G2_SEL |
| NONE             |    |    |    |    |    |    | R/W              |
| 0h               |    |    |    |    |    |    | 0h               |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16               |
| INTXBAR21_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8                |
| INTXBAR21_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0                |
| INTXBAR21_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |

**Table 3-3081. CONTROLSS\_INTXBAR21\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3081. CONTROLSS\_INTXBAR21\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR21_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.151 CONTROLSS\_INTXBAR21\_G3 Register

#### 1 CONTROLSS\_INTXBAR21\_G3 Register (Offset = 64Ch) [reset = 0h]

INT XBAR 21 Input Select.

Return to [Summary Table](#)

**Table 3-3082. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 564Ch       |

**Figure 3-1004. CONTROLSS\_INTXBAR21\_G3 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR21_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR21_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3084. CONTROLSS\_INTXBAR21\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR21_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.152 CONTROLSS\_INTXBAR21\_G4 Register

#### 1 CONTROLSS\_INTXBAR21\_G4 Register (Offset = 650h) [reset = 0h]

INT XBAR 21 Input Select.

Return to [Summary Table](#)

**Table 3-3085. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5650h       |

**Figure 3-1005. CONTROLSS\_INTXBAR21\_G4 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR21_G4_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR21_G4_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3087. CONTROLSS\_INTXBAR21\_G4 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR21_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.153 CONTROLSS\_INTXBAR21\_G5 Register

#### 1 CONTROLSS\_INTXBAR21\_G5 Register (Offset = 654h) [reset = 0h]

INT XBAR 21 Input Select.

Return to [Summary Table](#)

**Table 3-3088. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5654h       |

**Figure 3-1006. CONTROLSS\_INTXBAR21\_G5 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR21_G5_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR21_G5_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3090. CONTROLSS\_INTXBAR21\_G5 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR21_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.154 CONTROLSS\_INTXBAR21\_G6 Register

#### 1 CONTROLSS\_INTXBAR21\_G6 Register (Offset = 658h) [reset = 0h]

INT XBAR 21 Input Select.

Return to [Summary Table](#)

**Table 3-3091. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5658h       |

**Figure 3-1007. CONTROLSS\_INTXBAR21\_G6 Name Register**

|          |    |    |    |    |                  |    |    |
|----------|----|----|----|----|------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26               | 25 | 24 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18               | 17 | 16 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10               | 9  | 8  |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR21_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W              |    |    |
| 0h       |    |    |    |    | 0h               |    |    |

**Table 3-3093. CONTROLSS\_INTXBAR21\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                         |
|------|------------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR21_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.155 CONTROLSS\_INTXBAR22\_G0 Register

#### 1 CONTROLSS\_INTXBAR22\_G0 Register (Offset = 680h) [reset = 0h]

INT XBAR 22 Input Select.

Return to [Summary Table](#)

**Table 3-3094. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5680h       |

**Figure 3-1008. CONTROLSS\_INTXBAR22\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR22_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR22_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR22_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR22_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3096. CONTROLSS\_INTXBAR22\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR22_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.156 CONTROLSS\_INTXBAR22\_G1 Register

#### 1 CONTROLSS\_INTXBAR22\_G1 Register (Offset = 684h) [reset = 0h]

INT XBAR 22 Input Select.

Return to [Summary Table](#)

**Table 3-3097. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5684h       |

**Figure 3-1009. CONTROLSS\_INTXBAR22\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR22_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR22_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR22_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR22_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3099. CONTROLSS\_INTXBAR22\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                           |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR22_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.157 CONTROLSS\_INTXBAR22\_G2 Register

#### 1 CONTROLSS\_INTXBAR22\_G2 Register (Offset = 688h) [reset = 0h]

INT XBAR 22 Input Select.

Return to [Summary Table](#)

**Table 3-3100. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5688h       |

**Figure 3-1010. CONTROLSS\_INTXBAR22\_G2 Name Register**

|                  |    |    |    |    |    |    |                  |
|------------------|----|----|----|----|----|----|------------------|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24               |
| RESERVED         |    |    |    |    |    |    | INTXBAR22_G2_SEL |
| NONE             |    |    |    |    |    |    | R/W              |
| 0h               |    |    |    |    |    |    | 0h               |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16               |
| INTXBAR22_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8                |
| INTXBAR22_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0                |
| INTXBAR22_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |

**Table 3-3102. CONTROLSS\_INTXBAR22\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3102. CONTROLSS\_INTXBAR22\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR22_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.158 CONTROLSS\_INTXBAR22\_G3 Register

#### 1 CONTROLSS\_INTXBAR22\_G3 Register (Offset = 68Ch) [reset = 0h]

INT XBAR 22 Input Select.

Return to [Summary Table](#)

**Table 3-3103. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 568Ch       |

**Figure 3-1011. CONTROLSS\_INTXBAR22\_G3 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR22_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR22_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3105. CONTROLSS\_INTXBAR22\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR22_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.159 CONTROLSS\_INTXBAR22\_G4 Register

#### 1 CONTROLSS\_INTXBAR22\_G4 Register (Offset = 690h) [reset = 0h]

INT XBAR 22 Input Select.

Return to [Summary Table](#)

**Table 3-3106. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5690h       |

**Figure 3-1012. CONTROLSS\_INTXBAR22\_G4 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR22_G4_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR22_G4_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3108. CONTROLSS\_INTXBAR22\_G4 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR22_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.160 CONTROLSS\_INTXBAR22\_G5 Register

#### 1 CONTROLSS\_INTXBAR22\_G5 Register (Offset = 694h) [reset = 0h]

INT XBAR 22 Input Select.

Return to [Summary Table](#)

**Table 3-3109. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5694h       |

**Figure 3-1013. CONTROLSS\_INTXBAR22\_G5 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR22_G5_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR22_G5_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3111. CONTROLSS\_INTXBAR22\_G5 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR22_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.161 CONTROLSS\_INTXBAR22\_G6 Register

#### 1 CONTROLSS\_INTXBAR22\_G6 Register (Offset = 698h) [reset = 0h]

INT XBAR 22 Input Select.

Return to [Summary Table](#)

**Table 3-3112. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5698h       |

**Figure 3-1014. CONTROLSS\_INTXBAR22\_G6 Name Register**

|          |    |    |    |    |                  |    |    |
|----------|----|----|----|----|------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26               | 25 | 24 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18               | 17 | 16 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10               | 9  | 8  |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR22_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W              |    |    |
| 0h       |    |    |    |    | 0h               |    |    |

**Table 3-3114. CONTROLSS\_INTXBAR22\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                         |
|------|------------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR22_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.162 CONTROLSS\_INTXBAR23\_G0 Register

#### 1 CONTROLSS\_INTXBAR23\_G0 Register (Offset = 6C0h) [reset = 0h]

INT XBAR 23 Input Select.

Return to [Summary Table](#)

**Table 3-3115. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 56C0h       |

**Figure 3-1015. CONTROLSS\_INTXBAR23\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR23_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR23_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR23_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR23_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3117. CONTROLSS\_INTXBAR23\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR23_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.163 CONTROLSS\_INTXBAR23\_G1 Register

#### 1 CONTROLSS\_INTXBAR23\_G1 Register (Offset = 6C4h) [reset = 0h]

INT XBAR 23 Input Select.

Return to [Summary Table](#)

**Table 3-3118. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 56C4h       |

**Figure 3-1016. CONTROLSS\_INTXBAR23\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR23_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR23_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR23_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR23_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3120. CONTROLSS\_INTXBAR23\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                           |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR23_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.164 CONTROLSS\_INTXBAR23\_G2 Register

#### 1 CONTROLSS\_INTXBAR23\_G2 Register (Offset = 6C8h) [reset = 0h]

INT XBAR 23 Input Select.

Return to [Summary Table](#)

**Table 3-3121. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 56C8h       |

**Figure 3-1017. CONTROLSS\_INTXBAR23\_G2 Name Register**

|                  |    |    |    |    |    |    |                  |
|------------------|----|----|----|----|----|----|------------------|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24               |
| RESERVED         |    |    |    |    |    |    | INTXBAR23_G2_SEL |
| NONE             |    |    |    |    |    |    | R/W              |
| 0h               |    |    |    |    |    |    | 0h               |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16               |
| INTXBAR23_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8                |
| INTXBAR23_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0                |
| INTXBAR23_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |

**Table 3-3123. CONTROLSS\_INTXBAR23\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3123. CONTROLSS\_INTXBAR23\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR23_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.165 CONTROLSS\_INTXBAR23\_G3 Register

#### 1 CONTROLSS\_INTXBAR23\_G3 Register (Offset = 6CCh) [reset = 0h]

INT XBAR 23 Input Select.

Return to [Summary Table](#)

**Table 3-3124. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 56CCh       |

**Figure 3-1018. CONTROLSS\_INTXBAR23\_G3 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR23_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR23_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3126. CONTROLSS\_INTXBAR23\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR23_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.166 CONTROLSS\_INTXBAR23\_G4 Register

#### 1 CONTROLSS\_INTXBAR23\_G4 Register (Offset = 6D0h) [reset = 0h]

INT XBAR 23 Input Select.

Return to [Summary Table](#)

**Table 3-3127. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 56D0h       |

**Figure 3-1019. CONTROLSS\_INTXBAR23\_G4 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR23_G4_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR23_G4_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3129. CONTROLSS\_INTXBAR23\_G4 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR23_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.167 CONTROLSS\_INTXBAR23\_G5 Register

#### 1 CONTROLSS\_INTXBAR23\_G5 Register (Offset = 6D4h) [reset = 0h]

INT XBAR 23 Input Select.

Return to [Summary Table](#)

**Table 3-3130. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 56D4h       |

**Figure 3-1020. CONTROLSS\_INTXBAR23\_G5 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR23_G5_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR23_G5_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3132. CONTROLSS\_INTXBAR23\_G5 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR23_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.168 CONTROLSS\_INTXBAR23\_G6 Register

#### 1 CONTROLSS\_INTXBAR23\_G6 Register (Offset = 6D8h) [reset = 0h]

INT XBAR 23 Input Select.

Return to [Summary Table](#)

**Table 3-3133. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 56D8h       |

**Figure 3-1021. CONTROLSS\_INTXBAR23\_G6 Name Register**

|          |    |    |    |    |                  |    |    |
|----------|----|----|----|----|------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26               | 25 | 24 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18               | 17 | 16 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10               | 9  | 8  |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR23_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W              |    |    |
| 0h       |    |    |    |    | 0h               |    |    |

**Table 3-3135. CONTROLSS\_INTXBAR23\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                         |
|------|------------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR23_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.169 CONTROLSS\_INTXBAR24\_G0 Register

#### 1 CONTROLSS\_INTXBAR24\_G0 Register (Offset = 700h) [reset = 0h]

INT XBAR 24 Input Select.

Return to [Summary Table](#)

**Table 3-3136. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5700h       |

**Figure 3-1022. CONTROLSS\_INTXBAR24\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR24_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR24_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR24_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR24_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3138. CONTROLSS\_INTXBAR24\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR24_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.170 CONTROLSS\_INTXBAR24\_G1 Register

#### 1 CONTROLSS\_INTXBAR24\_G1 Register (Offset = 704h) [reset = 0h]

INT XBAR 24 Input Select.

Return to [Summary Table](#)

**Table 3-3139. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5704h       |

**Figure 3-1023. CONTROLSS\_INTXBAR24\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR24_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR24_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR24_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR24_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3141. CONTROLSS\_INTXBAR24\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                           |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR24_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.171 CONTROLSS\_INTXBAR24\_G2 Register

#### 1 CONTROLSS\_INTXBAR24\_G2 Register (Offset = 708h) [reset = 0h]

INT XBAR 24 Input Select.

Return to [Summary Table](#)

**Table 3-3142. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5708h       |

**Figure 3-1024. CONTROLSS\_INTXBAR24\_G2 Name Register**

|                  |    |    |    |    |    |    |                  |
|------------------|----|----|----|----|----|----|------------------|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24               |
| RESERVED         |    |    |    |    |    |    | INTXBAR24_G2_SEL |
| NONE             |    |    |    |    |    |    | R/W              |
| 0h               |    |    |    |    |    |    | 0h               |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16               |
| INTXBAR24_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8                |
| INTXBAR24_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0                |
| INTXBAR24_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |

**Table 3-3144. CONTROLSS\_INTXBAR24\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3144. CONTROLSS\_INTXBAR24\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR24_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.172 CONTROLSS\_INTXBAR24\_G3 Register

#### 1 CONTROLSS\_INTXBAR24\_G3 Register (Offset = 70Ch) [reset = 0h]

INT XBAR 24 Input Select.

Return to [Summary Table](#)

**Table 3-3145. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 570Ch       |

**Figure 3-1025. CONTROLSS\_INTXBAR24\_G3 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR24_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR24_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3147. CONTROLSS\_INTXBAR24\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR24_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.173 CONTROLSS\_INTXBAR24\_G4 Register

#### 1 CONTROLSS\_INTXBAR24\_G4 Register (Offset = 710h) [reset = 0h]

INT XBAR 24 Input Select.

Return to [Summary Table](#)

**Table 3-3148. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5710h       |

**Figure 3-1026. CONTROLSS\_INTXBAR24\_G4 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR24_G4_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR24_G4_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3150. CONTROLSS\_INTXBAR24\_G4 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR24_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.174 CONTROLSS\_INTXBAR24\_G5 Register

#### 1 CONTROLSS\_INTXBAR24\_G5 Register (Offset = 714h) [reset = 0h]

INT XBAR 24 Input Select.

Return to [Summary Table](#)

**Table 3-3151. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5714h       |

**Figure 3-1027. CONTROLSS\_INTXBAR24\_G5 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR24_G5_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR24_G5_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3153. CONTROLSS\_INTXBAR24\_G5 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR24_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.175 CONTROLSS\_INTXBAR24\_G6 Register

#### 1 CONTROLSS\_INTXBAR24\_G6 Register (Offset = 718h) [reset = 0h]

INT XBAR 24 Input Select.

Return to [Summary Table](#)

**Table 3-3154. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5718h       |

**Figure 3-1028. CONTROLSS\_INTXBAR24\_G6 Name Register**

|          |    |    |    |    |                  |    |    |
|----------|----|----|----|----|------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26               | 25 | 24 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18               | 17 | 16 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10               | 9  | 8  |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR24_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W              |    |    |
| 0h       |    |    |    |    | 0h               |    |    |

**Table 3-3156. CONTROLSS\_INTXBAR24\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                         |
|------|------------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR24_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.176 CONTROLSS\_INTXBAR25\_G0 Register

#### 1 CONTROLSS\_INTXBAR25\_G0 Register (Offset = 740h) [reset = 0h]

INT XBAR 25 Input Select.

Return to [Summary Table](#)

**Table 3-3157. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5740h       |

**Figure 3-1029. CONTROLSS\_INTXBAR25\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR25_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR25_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR25_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR25_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3159. CONTROLSS\_INTXBAR25\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR25_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.177 CONTROLSS\_INTXBAR25\_G1 Register

#### 1 CONTROLSS\_INTXBAR25\_G1 Register (Offset = 744h) [reset = 0h]

INT XBAR 25 Input Select.

Return to [Summary Table](#)

**Table 3-3160. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5744h       |

**Figure 3-1030. CONTROLSS\_INTXBAR25\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR25_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR25_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR25_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR25_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3162. CONTROLSS\_INTXBAR25\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                           |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR25_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.178 CONTROLSS\_INTXBAR25\_G2 Register

#### 1 CONTROLSS\_INTXBAR25\_G2 Register (Offset = 748h) [reset = 0h]

INT XBAR 25 Input Select.

Return to [Summary Table](#)

**Table 3-3163. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5748h       |

**Figure 3-1031. CONTROLSS\_INTXBAR25\_G2 Name Register**

|                  |    |    |    |    |    |    |                  |
|------------------|----|----|----|----|----|----|------------------|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24               |
| RESERVED         |    |    |    |    |    |    | INTXBAR25_G2_SEL |
| NONE             |    |    |    |    |    |    | R/W              |
| 0h               |    |    |    |    |    |    | 0h               |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16               |
| INTXBAR25_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8                |
| INTXBAR25_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0                |
| INTXBAR25_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |

**Table 3-3165. CONTROLSS\_INTXBAR25\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3165. CONTROLSS\_INTXBAR25\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR25_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.179 CONTROLSS\_INTXBAR25\_G3 Register

#### 1 CONTROLSS\_INTXBAR25\_G3 Register (Offset = 74Ch) [reset = 0h]

INT XBAR 25 Input Select.

Return to [Summary Table](#)

**Table 3-3166. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 574Ch       |

**Figure 3-1032. CONTROLSS\_INTXBAR25\_G3 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR25_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR25_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3168. CONTROLSS\_INTXBAR25\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR25_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.180 CONTROLSS\_INTXBAR25\_G4 Register

#### 1 CONTROLSS\_INTXBAR25\_G4 Register (Offset = 750h) [reset = 0h]

INT XBAR 25 Input Select.

Return to [Summary Table](#)

**Table 3-3169. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5750h       |

**Figure 3-1033. CONTROLSS\_INTXBAR25\_G4 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR25_G4_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR25_G4_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3171. CONTROLSS\_INTXBAR25\_G4 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR25_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.181 CONTROLSS\_INTXBAR25\_G5 Register

#### 1 CONTROLSS\_INTXBAR25\_G5 Register (Offset = 754h) [reset = 0h]

INT XBAR 25 Input Select.

Return to [Summary Table](#)

**Table 3-3172. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5754h       |

**Figure 3-1034. CONTROLSS\_INTXBAR25\_G5 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR25_G5_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR25_G5_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3174. CONTROLSS\_INTXBAR25\_G5 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR25_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.182 CONTROLSS\_INTXBAR25\_G6 Register

#### 1 CONTROLSS\_INTXBAR25\_G6 Register (Offset = 758h) [reset = 0h]

INT XBAR 25 Input Select.

Return to [Summary Table](#)

**Table 3-3175. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5758h       |

**Figure 3-1035. CONTROLSS\_INTXBAR25\_G6 Name Register**

|          |    |    |    |    |                  |    |    |
|----------|----|----|----|----|------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26               | 25 | 24 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18               | 17 | 16 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10               | 9  | 8  |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR25_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W              |    |    |
| 0h       |    |    |    |    | 0h               |    |    |

**Table 3-3177. CONTROLSS\_INTXBAR25\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                         |
|------|------------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR25_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.183 CONTROLSS\_INTXBAR26\_G0 Register

#### 1 CONTROLSS\_INTXBAR26\_G0 Register (Offset = 780h) [reset = 0h]

INT XBAR 26 Input Select.

Return to [Summary Table](#)

**Table 3-3178. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5780h       |

**Figure 3-1036. CONTROLSS\_INTXBAR26\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR26_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR26_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR26_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR26_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3180. CONTROLSS\_INTXBAR26\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR26_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.184 CONTROLSS\_INTXBAR26\_G1 Register

#### 1 CONTROLSS\_INTXBAR26\_G1 Register (Offset = 784h) [reset = 0h]

INT XBAR 26 Input Select.

Return to [Summary Table](#)

**Table 3-3181. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5784h       |

**Figure 3-1037. CONTROLSS\_INTXBAR26\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR26_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR26_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR26_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR26_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3183. CONTROLSS\_INTXBAR26\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                           |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR26_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.185 CONTROLSS\_INTXBAR26\_G2 Register

#### 1 CONTROLSS\_INTXBAR26\_G2 Register (Offset = 788h) [reset = 0h]

INT XBAR 26 Input Select.

Return to [Summary Table](#)

**Table 3-3184. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5788h       |

**Figure 3-1038. CONTROLSS\_INTXBAR26\_G2 Name Register**

|                  |    |    |    |    |    |    |                  |
|------------------|----|----|----|----|----|----|------------------|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24               |
| RESERVED         |    |    |    |    |    |    | INTXBAR26_G2_SEL |
| NONE             |    |    |    |    |    |    | R/W              |
| 0h               |    |    |    |    |    |    | 0h               |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16               |
| INTXBAR26_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8                |
| INTXBAR26_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0                |
| INTXBAR26_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |

**Table 3-3186. CONTROLSS\_INTXBAR26\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3186. CONTROLSS\_INTXBAR26\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR26_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.186 CONTROLSS\_INTXBAR26\_G3 Register

#### 1 CONTROLSS\_INTXBAR26\_G3 Register (Offset = 78Ch) [reset = 0h]

INT XBAR 26 Input Select.

Return to [Summary Table](#)

**Table 3-3187. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 578Ch       |

**Figure 3-1039. CONTROLSS\_INTXBAR26\_G3 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR26_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR26_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3189. CONTROLSS\_INTXBAR26\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR26_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.187 CONTROLSS\_INTXBAR26\_G4 Register

#### 1 CONTROLSS\_INTXBAR26\_G4 Register (Offset = 790h) [reset = 0h]

INT XBAR 26 Input Select.

Return to [Summary Table](#)

**Table 3-3190. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5790h       |

**Figure 3-1040. CONTROLSS\_INTXBAR26\_G4 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR26_G4_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR26_G4_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3192. CONTROLSS\_INTXBAR26\_G4 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR26_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.188 CONTROLSS\_INTXBAR26\_G5 Register

#### 1 CONTROLSS\_INTXBAR26\_G5 Register (Offset = 794h) [reset = 0h]

INT XBAR 26 Input Select.

Return to [Summary Table](#)

**Table 3-3193. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5794h       |

**Figure 3-1041. CONTROLSS\_INTXBAR26\_G5 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR26_G5_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR26_G5_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3195. CONTROLSS\_INTXBAR26\_G5 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR26_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.189 CONTROLSS\_INTXBAR26\_G6 Register

#### 1 CONTROLSS\_INTXBAR26\_G6 Register (Offset = 798h) [reset = 0h]

INT XBAR 26 Input Select.

Return to [Summary Table](#)

**Table 3-3196. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5798h       |

**Figure 3-1042. CONTROLSS\_INTXBAR26\_G6 Name Register**

|          |    |    |    |    |                  |    |    |
|----------|----|----|----|----|------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26               | 25 | 24 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18               | 17 | 16 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10               | 9  | 8  |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR26_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W              |    |    |
| 0h       |    |    |    |    | 0h               |    |    |

**Table 3-3198. CONTROLSS\_INTXBAR26\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                         |
|------|------------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR26_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.190 CONTROLSS\_INTXBAR27\_G0 Register

#### 1 CONTROLSS\_INTXBAR27\_G0 Register (Offset = 7C0h) [reset = 0h]

INT XBAR 27 Input Select.

Return to [Summary Table](#)

**Table 3-3199. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 57C0h       |

**Figure 3-1043. CONTROLSS\_INTXBAR27\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR27_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR27_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR27_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR27_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3201. CONTROLSS\_INTXBAR27\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR27_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.191 CONTROLSS\_INTXBAR27\_G1 Register

#### 1 CONTROLSS\_INTXBAR27\_G1 Register (Offset = 7C4h) [reset = 0h]

INT XBAR 27 Input Select.

Return to [Summary Table](#)

**Table 3-3202. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 57C4h       |

**Figure 3-1044. CONTROLSS\_INTXBAR27\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR27_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR27_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR27_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR27_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3204. CONTROLSS\_INTXBAR27\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                           |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR27_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.192 CONTROLSS\_INTXBAR27\_G2 Register

#### 1 CONTROLSS\_INTXBAR27\_G2 Register (Offset = 7C8h) [reset = 0h]

INT XBAR 27 Input Select.

Return to [Summary Table](#)

**Table 3-3205. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 57C8h       |

**Figure 3-1045. CONTROLSS\_INTXBAR27\_G2 Name Register**

|                  |    |    |    |    |    |    |                  |
|------------------|----|----|----|----|----|----|------------------|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24               |
| RESERVED         |    |    |    |    |    |    | INTXBAR27_G2_SEL |
| NONE             |    |    |    |    |    |    | R/W              |
| 0h               |    |    |    |    |    |    | 0h               |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16               |
| INTXBAR27_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8                |
| INTXBAR27_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0                |
| INTXBAR27_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |

**Table 3-3207. CONTROLSS\_INTXBAR27\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3207. CONTROLSS\_INTXBAR27\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR27_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.193 CONTROLSS\_INTXBAR27\_G3 Register

#### 1 CONTROLSS\_INTXBAR27\_G3 Register (Offset = 7CCh) [reset = 0h]

INT XBAR 27 Input Select.

Return to [Summary Table](#)

**Table 3-3208. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 57CCh       |

**Figure 3-1046. CONTROLSS\_INTXBAR27\_G3 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR27_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR27_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3210. CONTROLSS\_INTXBAR27\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR27_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.194 CONTROLSS\_INTXBAR27\_G4 Register

#### 1 CONTROLSS\_INTXBAR27\_G4 Register (Offset = 7D0h) [reset = 0h]

INT XBAR 27 Input Select.

Return to [Summary Table](#)

**Table 3-3211. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 57D0h       |

**Figure 3-1047. CONTROLSS\_INTXBAR27\_G4 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR27_G4_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR27_G4_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3213. CONTROLSS\_INTXBAR27\_G4 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR27_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.195 CONTROLSS\_INTXBAR27\_G5 Register

#### 1 CONTROLSS\_INTXBAR27\_G5 Register (Offset = 7D4h) [reset = 0h]

INT XBAR 27 Input Select.

Return to [Summary Table](#)

**Table 3-3214. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 57D4h       |

**Figure 3-1048. CONTROLSS\_INTXBAR27\_G5 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR27_G5_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR27_G5_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3216. CONTROLSS\_INTXBAR27\_G5 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR27_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.196 CONTROLSS\_INTXBAR27\_G6 Register

#### 1 CONTROLSS\_INTXBAR27\_G6 Register (Offset = 7D8h) [reset = 0h]

INT XBAR 27 Input Select.

Return to [Summary Table](#)

**Table 3-3217. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 57D8h       |

**Figure 3-1049. CONTROLSS\_INTXBAR27\_G6 Name Register**

|          |    |    |    |    |                  |    |    |
|----------|----|----|----|----|------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26               | 25 | 24 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18               | 17 | 16 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10               | 9  | 8  |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR27_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W              |    |    |
| 0h       |    |    |    |    | 0h               |    |    |

**Table 3-3219. CONTROLSS\_INTXBAR27\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                         |
|------|------------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR27_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.197 CONTROLSS\_INTXBAR28\_G0 Register

#### 1 CONTROLSS\_INTXBAR28\_G0 Register (Offset = 800h) [reset = 0h]

INT XBAR 28 Input Select.

Return to [Summary Table](#)

**Table 3-3220. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5800h       |

**Figure 3-1050. CONTROLSS\_INTXBAR28\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR28_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR28_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR28_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR28_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3222. CONTROLSS\_INTXBAR28\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR28_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.198 CONTROLSS\_INTXBAR28\_G1 Register

#### 1 CONTROLSS\_INTXBAR28\_G1 Register (Offset = 804h) [reset = 0h]

INT XBAR 28 Input Select.

Return to [Summary Table](#)

**Table 3-3223. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5804h       |

**Figure 3-1051. CONTROLSS\_INTXBAR28\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR28_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR28_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR28_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR28_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3225. CONTROLSS\_INTXBAR28\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                           |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR28_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.199 CONTROLSS\_INTXBAR28\_G2 Register

#### 1 CONTROLSS\_INTXBAR28\_G2 Register (Offset = 808h) [reset = 0h]

INT XBAR 28 Input Select.

Return to [Summary Table](#)

**Table 3-3226. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5808h       |

**Figure 3-1052. CONTROLSS\_INTXBAR28\_G2 Name Register**

|                  |    |    |    |    |    |    |                  |
|------------------|----|----|----|----|----|----|------------------|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24               |
| RESERVED         |    |    |    |    |    |    | INTXBAR28_G2_SEL |
| NONE             |    |    |    |    |    |    | R/W              |
| 0h               |    |    |    |    |    |    | 0h               |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16               |
| INTXBAR28_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8                |
| INTXBAR28_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0                |
| INTXBAR28_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |

**Table 3-3228. CONTROLSS\_INTXBAR28\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3228. CONTROLSS\_INTXBAR28\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR28_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.200 CONTROLSS\_INTXBAR28\_G3 Register

#### 1 CONTROLSS\_INTXBAR28\_G3 Register (Offset = 80Ch) [reset = 0h]

INT XBAR 28 Input Select.

Return to [Summary Table](#)

**Table 3-3229. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 580Ch       |

**Figure 3-1053. CONTROLSS\_INTXBAR28\_G3 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR28_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR28_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3231. CONTROLSS\_INTXBAR28\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR28_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.201 CONTROLSS\_INTXBAR28\_G4 Register

#### 1 CONTROLSS\_INTXBAR28\_G4 Register (Offset = 810h) [reset = 0h]

INT XBAR 28 Input Select.

Return to [Summary Table](#)

**Table 3-3232. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5810h       |

**Figure 3-1054. CONTROLSS\_INTXBAR28\_G4 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR28_G4_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR28_G4_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3234. CONTROLSS\_INTXBAR28\_G4 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR28_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.202 CONTROLSS\_INTXBAR28\_G5 Register

#### 1 CONTROLSS\_INTXBAR28\_G5 Register (Offset = 814h) [reset = 0h]

INT XBAR 28 Input Select.

Return to [Summary Table](#)

**Table 3-3235. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5814h       |

**Figure 3-1055. CONTROLSS\_INTXBAR28\_G5 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR28_G5_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR28_G5_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3237. CONTROLSS\_INTXBAR28\_G5 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR28_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.203 CONTROLSS\_INTXBAR28\_G6 Register

#### 1 CONTROLSS\_INTXBAR28\_G6 Register (Offset = 818h) [reset = 0h]

INT XBAR 28 Input Select.

Return to [Summary Table](#)

**Table 3-3238. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5818h       |

**Figure 3-1056. CONTROLSS\_INTXBAR28\_G6 Name Register**

|          |    |    |    |    |                  |    |    |
|----------|----|----|----|----|------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26               | 25 | 24 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18               | 17 | 16 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10               | 9  | 8  |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR28_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W              |    |    |
| 0h       |    |    |    |    | 0h               |    |    |

**Table 3-3240. CONTROLSS\_INTXBAR28\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                         |
|------|------------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR28_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.204 CONTROLSS\_INTXBAR29\_G0 Register

#### 1 CONTROLSS\_INTXBAR29\_G0 Register (Offset = 840h) [reset = 0h]

INT XBAR 29 Input Select.

Return to [Summary Table](#)

**Table 3-3241. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5840h       |

**Figure 3-1057. CONTROLSS\_INTXBAR29\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR29_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR29_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR29_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR29_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3243. CONTROLSS\_INTXBAR29\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR29_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.205 CONTROLSS\_INTXBAR29\_G1 Register

#### 1 CONTROLSS\_INTXBAR29\_G1 Register (Offset = 844h) [reset = 0h]

INT XBAR 29 Input Select.

Return to [Summary Table](#)

**Table 3-3244. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5844h       |

**Figure 3-1058. CONTROLSS\_INTXBAR29\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR29_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR29_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR29_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR29_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3246. CONTROLSS\_INTXBAR29\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                           |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR29_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.206 CONTROLSS\_INTXBAR29\_G2 Register

#### 1 CONTROLSS\_INTXBAR29\_G2 Register (Offset = 848h) [reset = 0h]

INT XBAR 29 Input Select.

Return to [Summary Table](#)

**Table 3-3247. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5848h       |

**Figure 3-1059. CONTROLSS\_INTXBAR29\_G2 Name Register**

|                  |    |    |    |    |    |    |                  |
|------------------|----|----|----|----|----|----|------------------|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24               |
| RESERVED         |    |    |    |    |    |    | INTXBAR29_G2_SEL |
| NONE             |    |    |    |    |    |    | R/W              |
| 0h               |    |    |    |    |    |    | 0h               |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16               |
| INTXBAR29_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8                |
| INTXBAR29_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0                |
| INTXBAR29_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |

**Table 3-3249. CONTROLSS\_INTXBAR29\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3249. CONTROLSS\_INTXBAR29\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR29_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.207 CONTROLSS\_INTXBAR29\_G3 Register

#### 1 CONTROLSS\_INTXBAR29\_G3 Register (Offset = 84Ch) [reset = 0h]

INT XBAR 29 Input Select.

Return to [Summary Table](#)

**Table 3-3250. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 584Ch       |

**Figure 3-1060. CONTROLSS\_INTXBAR29\_G3 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR29_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR29_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3252. CONTROLSS\_INTXBAR29\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR29_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.208 CONTROLSS\_INTXBAR29\_G4 Register

#### 1 CONTROLSS\_INTXBAR29\_G4 Register (Offset = 850h) [reset = 0h]

INT XBAR 29 Input Select.

Return to [Summary Table](#)

**Table 3-3253. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5850h       |

**Figure 3-1061. CONTROLSS\_INTXBAR29\_G4 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR29_G4_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR29_G4_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3255. CONTROLSS\_INTXBAR29\_G4 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR29_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.209 CONTROLSS\_INTXBAR29\_G5 Register

#### 1 CONTROLSS\_INTXBAR29\_G5 Register (Offset = 854h) [reset = 0h]

INT XBAR 29 Input Select.

Return to [Summary Table](#)

**Table 3-3256. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5854h       |

**Figure 3-1062. CONTROLSS\_INTXBAR29\_G5 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR29_G5_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR29_G5_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3258. CONTROLSS\_INTXBAR29\_G5 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR29_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.210 CONTROLSS\_INTXBAR29\_G6 Register

#### 1 CONTROLSS\_INTXBAR29\_G6 Register (Offset = 858h) [reset = 0h]

INT XBAR 29 Input Select.

Return to [Summary Table](#)

**Table 3-3259. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5858h       |

**Figure 3-1063. CONTROLSS\_INTXBAR29\_G6 Name Register**

|          |    |    |    |    |                  |    |    |
|----------|----|----|----|----|------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26               | 25 | 24 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18               | 17 | 16 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10               | 9  | 8  |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR29_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W              |    |    |
| 0h       |    |    |    |    | 0h               |    |    |

**Table 3-3261. CONTROLSS\_INTXBAR29\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                         |
|------|------------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR29_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.211 CONTROLSS\_INTXBAR30\_G0 Register

#### 1 CONTROLSS\_INTXBAR30\_G0 Register (Offset = 880h) [reset = 0h]

INT XBAR 30 Input Select.

Return to [Summary Table](#)

**Table 3-3262. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5880h       |

**Figure 3-1064. CONTROLSS\_INTXBAR30\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR30_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR30_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR30_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR30_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3264. CONTROLSS\_INTXBAR30\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR30_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.212 CONTROLSS\_INTXBAR30\_G1 Register

#### 1 CONTROLSS\_INTXBAR30\_G1 Register (Offset = 884h) [reset = 0h]

INT XBAR 30 Input Select.

Return to [Summary Table](#)

**Table 3-3265. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5884h       |

**Figure 3-1065. CONTROLSS\_INTXBAR30\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR30_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR30_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR30_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR30_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3267. CONTROLSS\_INTXBAR30\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                           |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR30_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.213 CONTROLSS\_INTXBAR30\_G2 Register

#### 1 CONTROLSS\_INTXBAR30\_G2 Register (Offset = 888h) [reset = 0h]

INT XBAR 30 Input Select.

Return to [Summary Table](#)

**Table 3-3268. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5888h       |

**Figure 3-1066. CONTROLSS\_INTXBAR30\_G2 Name Register**

|                  |    |    |    |    |    |    |                  |
|------------------|----|----|----|----|----|----|------------------|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24               |
| RESERVED         |    |    |    |    |    |    | INTXBAR30_G2_SEL |
| NONE             |    |    |    |    |    |    | R/W              |
| 0h               |    |    |    |    |    |    | 0h               |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16               |
| INTXBAR30_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8                |
| INTXBAR30_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0                |
| INTXBAR30_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |

**Table 3-3270. CONTROLSS\_INTXBAR30\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3270. CONTROLSS\_INTXBAR30\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR30_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.214 CONTROLSS\_INTXBAR30\_G3 Register

#### 1 CONTROLSS\_INTXBAR30\_G3 Register (Offset = 88Ch) [reset = 0h]

INT XBAR 30 Input Select.

Return to [Summary Table](#)

**Table 3-3271. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 588Ch       |

**Figure 3-1067. CONTROLSS\_INTXBAR30\_G3 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR30_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR30_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3273. CONTROLSS\_INTXBAR30\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR30_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.215 CONTROLSS\_INTXBAR30\_G4 Register

#### 1 CONTROLSS\_INTXBAR30\_G4 Register (Offset = 890h) [reset = 0h]

INT XBAR 30 Input Select.

Return to [Summary Table](#)

**Table 3-3274. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5890h       |

**Figure 3-1068. CONTROLSS\_INTXBAR30\_G4 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR30_G4_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR30_G4_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3276. CONTROLSS\_INTXBAR30\_G4 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR30_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.216 CONTROLSS\_INTXBAR30\_G5 Register

#### 1 CONTROLSS\_INTXBAR30\_G5 Register (Offset = 894h) [reset = 0h]

INT XBAR 30 Input Select.

Return to [Summary Table](#)

**Table 3-3277. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5894h       |

**Figure 3-1069. CONTROLSS\_INTXBAR30\_G5 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR30_G5_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR30_G5_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3279. CONTROLSS\_INTXBAR30\_G5 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR30_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.217 CONTROLSS\_INTXBAR30\_G6 Register

#### 1 CONTROLSS\_INTXBAR30\_G6 Register (Offset = 898h) [reset = 0h]

INT XBAR 30 Input Select.

Return to [Summary Table](#)

**Table 3-3280. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 5898h       |

**Figure 3-1070. CONTROLSS\_INTXBAR30\_G6 Name Register**

|          |    |    |    |                  |    |    |    |
|----------|----|----|----|------------------|----|----|----|
| 31       | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 23       | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 15       | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| RESERVED |    |    |    |                  |    |    |    |
| NONE     |    |    |    |                  |    |    |    |
| 0h       |    |    |    |                  |    |    |    |
| 7        | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| RESERVED |    |    |    | INTXBAR30_G6_SEL |    |    |    |
| NONE     |    |    |    | R/W              |    |    |    |
| 0h       |    |    |    | 0h               |    |    |    |

**Table 3-3282. CONTROLSS\_INTXBAR30\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                         |
|------|------------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR30_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

### 3.16.2.218 CONTROLSS\_INTXBAR31\_G0 Register

#### 1 CONTROLSS\_INTXBAR31\_G0 Register (Offset = 8C0h) [reset = 0h]

INT XBAR 31 Input Select.

Return to [Summary Table](#)

**Table 3-3283. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 58C0h       |

**Figure 3-1071. CONTROLSS\_INTXBAR31\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR31_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR31_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR31_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR31_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3285. CONTROLSS\_INTXBAR31\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR31_G0_SEL | R/W  | 0h    | EPWM INT interrupt to corresponding XBAR<br>1:PWMx.INT is selected<br>0:PWMx.INT is de-selected |

### 3.16.2.219 CONTROLSS\_INTXBAR31\_G1 Register

#### 1 CONTROLSS\_INTXBAR31\_G1 Register (Offset = 8C4h) [reset = 0h]

INT XBAR 31 Input Select.

Return to [Summary Table](#)

**Table 3-3286. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 58C4h       |

**Figure 3-1072. CONTROLSS\_INTXBAR31\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| INTXBAR31_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| INTXBAR31_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR31_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR31_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3288. CONTROLSS\_INTXBAR31\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                           |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | INTXBAR31_G1_SEL | R/W  | 0h    | EPWM TZINT interrupt to corresponding XBAR<br>1:PWMx.TZINT is selected<br>0:PWMx.TZINT is de-selected |

### 3.16.2.220 CONTROLSS\_INTXBAR31\_G2 Register

#### 1 CONTROLSS\_INTXBAR31\_G2 Register (Offset = 8C8h) [reset = 0h]

INT XBAR 31 Input Select.

Return to [Summary Table](#)

**Table 3-3289. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 58C8h       |

**Figure 3-1073. CONTROLSS\_INTXBAR31\_G2 Name Register**

|                  |    |    |    |    |    |    |                  |
|------------------|----|----|----|----|----|----|------------------|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24               |
| RESERVED         |    |    |    |    |    |    | INTXBAR31_G2_SEL |
| NONE             |    |    |    |    |    |    | R/W              |
| 0h               |    |    |    |    |    |    | 0h               |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16               |
| INTXBAR31_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8                |
| INTXBAR31_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0                |
| INTXBAR31_G2_SEL |    |    |    |    |    |    |                  |
| R/W              |    |    |    |    |    |    |                  |
| 0h               |    |    |    |    |    |    |                  |

**Table 3-3291. CONTROLSS\_INTXBAR31\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:25 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3291. CONTROLSS\_INTXBAR31\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24:0 | INTXBAR31_G2_SEL | R/W  | 0h    | Corresponding INT XBAR G2 Input Select<br>0:ADC0.INT1<br>1:ADC0.INT2<br>2:ADC0.INT3<br>3:ADC0.INT4<br>4:ADC0.EVTINT<br>5:ADC1.INT1<br>6:ADC1.INT2<br>7:ADC1.INT3<br>8:ADC1.INT4<br>9:ADC1.EVTINT<br>10:ADC2.INT1<br>11:ADC2.INT2<br>12:ADC2.INT3<br>13:ADC2.INT4<br>14:ADC2.EVTINT<br>15:ADC3.INT1<br>16:ADC3.INT2<br>17:ADC3.INT3<br>18:ADC3.INT4<br>19:ADC3.EVTINT<br>20:ADC4.INT1<br>21:ADC4.INT2<br>22:ADC4.INT3<br>23:ADC4.INT4<br>24:ADC4.EVTINT |

### 3.16.2.221 CONTROLSS\_INTXBAR31\_G3 Register

#### 1 CONTROLSS\_INTXBAR31\_G3 Register (Offset = 8CCh) [reset = 0h]

INT XBAR 31 Input Select.

Return to [Summary Table](#)

**Table 3-3292. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 58CCh       |

**Figure 3-1074. CONTROLSS\_INTXBAR31\_G3 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| INTXBAR31_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| INTXBAR31_G3_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3294. CONTROLSS\_INTXBAR31\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | INTXBAR31_G3_SEL | R/W  | 0h    | Corresponding INT XBAR G3 Input Select<br>0:FSIRX0.INT1N<br>1:FSIRX0.INT2N<br>2:FSIRX1.INT1N<br>3:FSIRX1.INT2N<br>4:FSIRX2.INT1N<br>5:FSIRX2.INT2N<br>6:FSIRX3.INT1N<br>7:FSIRX3.INT2N<br>8:FSITX0.INT1N<br>9:FSITX0.INT2N<br>10:FSITX1.INT1N<br>11:FSITX1.INT2N<br>12:FSITX2.INT1N<br>13:FSITX2.INT2N<br>14:FSITX3.INT1N<br>15:FSITX3.INT2N |

### 3.16.2.222 CONTROLSS\_INTXBAR31\_G4 Register

#### 1 CONTROLSS\_INTXBAR31\_G4 Register (Offset = 8D0h) [reset = 0h]

INT XBAR 31 Input Select.

Return to [Summary Table](#)

**Table 3-3295. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 58D0h       |

**Figure 3-1075. CONTROLSS\_INTXBAR31\_G4 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR31_G4_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR31_G4_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3297. CONTROLSS\_INTXBAR31\_G4 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 9:0   | INTXBAR31_G4_SEL | R/W  | 0h    | Corresponding INT XBAR G4 Input Select<br>0:SD0.ERR<br>1:SD0.FILT1.DRINT<br>2:SD0.FILT2.DRINT<br>3:SD0.FILT3.DRINT<br>4:SD0.FILT4.DRINT<br>5:SD1.ERR<br>6:SD1.FILT1.DRINT<br>7:SD1.FILT2.DRINT<br>8:SD1.FILT3.DRINT<br>9:SD1.FILT4.DRINT |

### 3.16.2.223 CONTROLSS\_INTXBAR31\_G5 Register

#### 1 CONTROLSS\_INTXBAR31\_G5 Register (Offset = 8D4h) [reset = 0h]

INT XBAR 31 Input Select.

Return to [Summary Table](#)

**Table 3-3298. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 58D4h       |

**Figure 3-1076. CONTROLSS\_INTXBAR31\_G5 Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | INTXBAR31_G5_SEL |    |
| NONE             |    |    |    |    |    | R/W              |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| INTXBAR31_G5_SEL |    |    |    |    |    |                  |    |
| R/W              |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 3-3300. CONTROLSS\_INTXBAR31\_G5 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                     |
| 9:0   | INTXBAR31_G5_SEL | R/W  | 0h    | Corresponding INT XBAR G5 Input Select<br>0:ECAP0.INT<br>1:ECAP1.INT<br>2:ECAP2.INT<br>3:ECAP3.INT<br>4:ECAP4.INT<br>5:ECAP5.INT<br>6:ECAP6.INT<br>7:ECAP7.INT<br>8:ECAP8.INT<br>9:ECAP9.INT |



### 3.16.2.224 CONTROLSS\_INTXBAR31\_G6 Register

#### 1 CONTROLSS\_INTXBAR31\_G6 Register (Offset = 8D8h) [reset = 0h]

INT XBAR 31 Input Select.

Return to [Summary Table](#)

**Table 3-3301. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_INTXBAR | 502D 58D8h       |

**Figure 3-1077. CONTROLSS\_INTXBAR31\_G6 Name Register**

|          |    |    |    |    |                  |    |    |
|----------|----|----|----|----|------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26               | 25 | 24 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 23       | 22 | 21 | 20 | 19 | 18               | 17 | 16 |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 15       | 14 | 13 | 12 | 11 | 10               | 9  | 8  |
| RESERVED |    |    |    |    |                  |    |    |
| NONE     |    |    |    |    |                  |    |    |
| 0h       |    |    |    |    |                  |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                | 1  | 0  |
| RESERVED |    |    |    |    | INTXBAR31_G6_SEL |    |    |
| NONE     |    |    |    |    | R/W              |    |    |
| 0h       |    |    |    |    | 0h               |    |    |

**Table 3-3303. CONTROLSS\_INTXBAR31\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                         |
|------|------------------|------|-------|-------------------------------------------------------------------------------------|
| 31:3 | RESERVED         | NONE | 0h    | Reserved                                                                            |
| 2:0  | INTXBAR31_G6_SEL | R/W  | 0h    | Corresponding INT XBAR G6 Input Select<br>0:EQEP0.INT<br>1:EQEP1.INT<br>2:EQEP2.INT |

## 3.17 CONTROLSS\_MDLXBAR

### CONTROLSS\_MDLXBAR

#### 3.17.1 CONTROLSS\_MDLXBAR Summaries

#### CONTROLSS\_MDLXBAR Summaries

**Table 3-3304. CONTROLSS Registers, Base Address=502D 3000h, Length=1024**

| Offset | Length | Register Name                          | CONTROLSS_MDLXBAR Physical Address |
|--------|--------|----------------------------------------|------------------------------------|
| 100h   | 32     | <a href="#">CONTROLSS_MDLXBAR0_G0</a>  | 502D 3100h                         |
| 104h   | 32     | <a href="#">CONTROLSS_MDLXBAR0_G1</a>  | 502D 3104h                         |
| 108h   | 32     | <a href="#">CONTROLSS_MDLXBAR0_G2</a>  | 502D 3108h                         |
| 140h   | 32     | <a href="#">CONTROLSS_MDLXBAR1_G0</a>  | 502D 3140h                         |
| 144h   | 32     | <a href="#">CONTROLSS_MDLXBAR1_G1</a>  | 502D 3144h                         |
| 148h   | 32     | <a href="#">CONTROLSS_MDLXBAR1_G2</a>  | 502D 3148h                         |
| 180h   | 32     | <a href="#">CONTROLSS_MDLXBAR2_G0</a>  | 502D 3180h                         |
| 184h   | 32     | <a href="#">CONTROLSS_MDLXBAR2_G1</a>  | 502D 3184h                         |
| 188h   | 32     | <a href="#">CONTROLSS_MDLXBAR2_G2</a>  | 502D 3188h                         |
| 1C0h   | 32     | <a href="#">CONTROLSS_MDLXBAR3_G0</a>  | 502D 31C0h                         |
| 1C4h   | 32     | <a href="#">CONTROLSS_MDLXBAR3_G1</a>  | 502D 31C4h                         |
| 1C8h   | 32     | <a href="#">CONTROLSS_MDLXBAR3_G2</a>  | 502D 31C8h                         |
| 200h   | 32     | <a href="#">CONTROLSS_MDLXBAR4_G0</a>  | 502D 3200h                         |
| 204h   | 32     | <a href="#">CONTROLSS_MDLXBAR4_G1</a>  | 502D 3204h                         |
| 208h   | 32     | <a href="#">CONTROLSS_MDLXBAR4_G2</a>  | 502D 3208h                         |
| 240h   | 32     | <a href="#">CONTROLSS_MDLXBAR5_G0</a>  | 502D 3240h                         |
| 244h   | 32     | <a href="#">CONTROLSS_MDLXBAR5_G1</a>  | 502D 3244h                         |
| 248h   | 32     | <a href="#">CONTROLSS_MDLXBAR5_G2</a>  | 502D 3248h                         |
| 280h   | 32     | <a href="#">CONTROLSS_MDLXBAR6_G0</a>  | 502D 3280h                         |
| 284h   | 32     | <a href="#">CONTROLSS_MDLXBAR6_G1</a>  | 502D 3284h                         |
| 288h   | 32     | <a href="#">CONTROLSS_MDLXBAR6_G2</a>  | 502D 3288h                         |
| 2C0h   | 32     | <a href="#">CONTROLSS_MDLXBAR7_G0</a>  | 502D 32C0h                         |
| 2C4h   | 32     | <a href="#">CONTROLSS_MDLXBAR7_G1</a>  | 502D 32C4h                         |
| 2C8h   | 32     | <a href="#">CONTROLSS_MDLXBAR7_G2</a>  | 502D 32C8h                         |
| 300h   | 32     | <a href="#">CONTROLSS_MDLXBAR8_G0</a>  | 502D 3300h                         |
| 304h   | 32     | <a href="#">CONTROLSS_MDLXBAR8_G1</a>  | 502D 3304h                         |
| 308h   | 32     | <a href="#">CONTROLSS_MDLXBAR8_G2</a>  | 502D 3308h                         |
| 340h   | 32     | <a href="#">CONTROLSS_MDLXBAR9_G0</a>  | 502D 3340h                         |
| 344h   | 32     | <a href="#">CONTROLSS_MDLXBAR9_G1</a>  | 502D 3344h                         |
| 348h   | 32     | <a href="#">CONTROLSS_MDLXBAR9_G2</a>  | 502D 3348h                         |
| 380h   | 32     | <a href="#">CONTROLSS_MDLXBAR10_G0</a> | 502D 3380h                         |
| 384h   | 32     | <a href="#">CONTROLSS_MDLXBAR10_G1</a> | 502D 3384h                         |
| 388h   | 32     | <a href="#">CONTROLSS_MDLXBAR10_G2</a> | 502D 3388h                         |
| 3C0h   | 32     | <a href="#">CONTROLSS_MDLXBAR11_G0</a> | 502D 33C0h                         |
| 3C4h   | 32     | <a href="#">CONTROLSS_MDLXBAR11_G1</a> | 502D 33C4h                         |
| 3C8h   | 32     | <a href="#">CONTROLSS_MDLXBAR11_G2</a> | 502D 33C8h                         |
| 400h   | 32     | <a href="#">CONTROLSS_MDLXBAR12_G0</a> | 502D 3400h                         |

**Table 3-3304. CONTROLSS Registers, Base Address=502D 3000h, Length=1024 (continued)**

| Offset | Length | Register Name                          | CONTROLSS_MDLXBAR Physical Address |
|--------|--------|----------------------------------------|------------------------------------|
| 404h   | 32     | <a href="#">CONTROLSS_MDLXBAR12_G1</a> | 502D 3404h                         |
| 408h   | 32     | <a href="#">CONTROLSS_MDLXBAR12_G2</a> | 502D 3408h                         |
| 440h   | 32     | <a href="#">CONTROLSS_MDLXBAR13_G0</a> | 502D 3440h                         |
| 444h   | 32     | <a href="#">CONTROLSS_MDLXBAR13_G1</a> | 502D 3444h                         |
| 448h   | 32     | <a href="#">CONTROLSS_MDLXBAR13_G2</a> | 502D 3448h                         |
| 480h   | 32     | <a href="#">CONTROLSS_MDLXBAR14_G0</a> | 502D 3480h                         |
| 484h   | 32     | <a href="#">CONTROLSS_MDLXBAR14_G1</a> | 502D 3484h                         |
| 488h   | 32     | <a href="#">CONTROLSS_MDLXBAR14_G2</a> | 502D 3488h                         |
| 4C0h   | 32     | <a href="#">CONTROLSS_MDLXBAR15_G0</a> | 502D 34C0h                         |
| 4C4h   | 32     | <a href="#">CONTROLSS_MDLXBAR15_G1</a> | 502D 34C4h                         |
| 4C8h   | 32     | <a href="#">CONTROLSS_MDLXBAR15_G2</a> | 502D 34C8h                         |

### 3.17.2 CONTROLSS\_MDLXBAR Registers

#### CONTROLSS\_MDLXBAR Registers

### 3.17.2.1 CONTROLSS\_MDLXBAR0\_G0 Register

#### 1 CONTROLSS\_MDLXBAR0\_G0 Register (Offset = 100h) [reset = 0h]

MDL XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-3305. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3100h       |

**Figure 3-1078. CONTROLSS\_MDLXBAR0\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR0_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR0_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR0_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR0_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3307. CONTROLSS\_MDLXBAR0\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR0_G0_SEL | R/W  | 0h    | MDL XBAR0 G0 input bit select. Input source is PWMA sclk select<br>1:PWMA sclk bit[x] selected<br>0:PWMA sclk bit[x] is de-selected |

### 3.17.2.2 CONTROLSS\_MDLXBAR0\_G1 Register

#### 1 CONTROLSS\_MDLXBAR0\_G1 Register (Offset = 104h) [reset = 0h]

MDL XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-3308. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3104h       |

**Figure 3-1079. CONTROLSS\_MDLXBAR0\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR0_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR0_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR0_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR0_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3310. CONTROLSS\_MDLXBAR0\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR0_G1_SEL | R/W  | 0h    | MDL XBAR0 G1 input bit select. Input source is PWMB sclk select<br>1:PWMB sclk bit[x] selected<br>0:PWMB sclk bit[x] is de-selected |

### 3.17.2.3 CONTROLSS\_MDLXBAR0\_G2 Register

#### 1 CONTROLSS\_MDLXBAR0\_G2 Register (Offset = 108h) [reset = 0h]

MDL XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-3311. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3108h       |

**Figure 3-1080. CONTROLSS\_MDLXBAR0\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR0_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR0_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR0_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR0_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3313. CONTROLSS\_MDLXBAR0\_G2 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR0_G2_SEL | R/W  | 0h    | MDL XBAR0 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

### 3.17.2.4 CONTROLSS\_MDLXBAR1\_G0 Register

#### 1 CONTROLSS\_MDLXBAR1\_G0 Register (Offset = 140h) [reset = 0h]

MDL XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-3314. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3140h       |

**Figure 3-1081. CONTROLSS\_MDLXBAR1\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR1_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR1_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR1_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR1_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3316. CONTROLSS\_MDLXBAR1\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR1_G0_SEL | R/W  | 0h    | MDL XBAR1 G0 input bit select. Input source is PWMA sclk select<br>1:PWMA sclk bit[x] selected<br>0:PWMA sclk bit[x] is de-selected |

### 3.17.2.5 CONTROLSS\_MDLXBAR1\_G1 Register

#### 1 CONTROLSS\_MDLXBAR1\_G1 Register (Offset = 144h) [reset = 0h]

MDL XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-3317. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3144h       |

**Figure 3-1082. CONTROLSS\_MDLXBAR1\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR1_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR1_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR1_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR1_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3319. CONTROLSS\_MDLXBAR1\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR1_G1_SEL | R/W  | 0h    | MDL XBAR1 G1 input bit select. Input source is PWMB sclk select<br>1:PWMB sclk bit[x] selected<br>0:PWMB sclk bit[x] is de-selected |



### 3.17.2.6 CONTROLSS\_MDLXBAR1\_G2 Register

#### 1 CONTROLSS\_MDLXBAR1\_G2 Register (Offset = 148h) [reset = 0h]

MDL XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-3320. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3148h       |

**Figure 3-1083. CONTROLSS\_MDLXBAR1\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR1_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR1_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR1_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR1_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3322. CONTROLSS\_MDLXBAR1\_G2 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR1_G2_SEL | R/W  | 0h    | MDL XBAR1 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

### 3.17.2.7 CONTROLSS\_MDLXBAR2\_G0 Register

#### 1 CONTROLSS\_MDLXBAR2\_G0 Register (Offset = 180h) [reset = 0h]

MDL XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-3323. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3180h       |

**Figure 3-1084. CONTROLSS\_MDLXBAR2\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR2_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR2_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR2_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR2_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3325. CONTROLSS\_MDLXBAR2\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR2_G0_SEL | R/W  | 0h    | MDL XBAR2 G0 input bit select. Input source is PWMA sclk select<br>1:PWMA sclk bit[x] selected<br>0:PWMA sclk bit[x] is de-selected |

### 3.17.2.8 CONTROLSS\_MDLXBAR2\_G1 Register

#### 1 CONTROLSS\_MDLXBAR2\_G1 Register (Offset = 184h) [reset = 0h]

MDL XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-3326. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3184h       |

**Figure 3-1085. CONTROLSS\_MDLXBAR2\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR2_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR2_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR2_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR2_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3328. CONTROLSS\_MDLXBAR2\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR2_G1_SEL | R/W  | 0h    | MDL XBAR2 G1 input bit select. Input source is PWMB sclk select<br>1:PWMB sclk bit[x] selected<br>0:PWMB sclk bit[x] is de-selected |

### 3.17.2.9 CONTROLSS\_MDLXBAR2\_G2 Register

#### 1 CONTROLSS\_MDLXBAR2\_G2 Register (Offset = 188h) [reset = 0h]

MDL XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-3329. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3188h       |

**Figure 3-1086. CONTROLSS\_MDLXBAR2\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR2_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR2_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR2_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR2_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3331. CONTROLSS\_MDLXBAR2\_G2 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR2_G2_SEL | R/W  | 0h    | MDL XBAR2 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

### 3.17.2.10 CONTROLSS\_MDLXBAR3\_G0 Register

#### 1 CONTROLSS\_MDLXBAR3\_G0 Register (Offset = 1C0h) [reset = 0h]

MDL XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-3332. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 31C0h       |

**Figure 3-1087. CONTROLSS\_MDLXBAR3\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR3_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR3_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR3_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR3_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3334. CONTROLSS\_MDLXBAR3\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR3_G0_SEL | R/W  | 0h    | MDL XBAR3 G0 input bit select. Input source is PWMA sclk select<br>1:PWMA sclk bit[x] selected<br>0:PWMA sclk bit[x] is de-selected |

### 3.17.2.11 CONTROLSS\_MDLXBAR3\_G1 Register

#### 1 CONTROLSS\_MDLXBAR3\_G1 Register (Offset = 1C4h) [reset = 0h]

MDL XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-3335. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 31C4h       |

**Figure 3-1088. CONTROLSS\_MDLXBAR3\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR3_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR3_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR3_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR3_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3337. CONTROLSS\_MDLXBAR3\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR3_G1_SEL | R/W  | 0h    | MDL XBAR3 G1 input bit select. Input source is PWMB sclk select<br>1:PWMB sclk bit[x] selected<br>0:PWMB sclk bit[x] is de-selected |

### 3.17.2.12 CONTROLSS\_MDLXBAR3\_G2 Register

#### 1 CONTROLSS\_MDLXBAR3\_G2 Register (Offset = 1C8h) [reset = 0h]

MDL XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-3338. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 31C8h       |

**Figure 3-1089. CONTROLSS\_MDLXBAR3\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR3_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR3_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR3_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR3_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3340. CONTROLSS\_MDLXBAR3\_G2 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR3_G2_SEL | R/W  | 0h    | MDL XBAR3 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

### 3.17.2.13 CONTROLSS\_MDLXBAR4\_G0 Register

#### 1 CONTROLSS\_MDLXBAR4\_G0 Register (Offset = 200h) [reset = 0h]

MDL XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-3341. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3200h       |

**Figure 3-1090. CONTROLSS\_MDLXBAR4\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR4_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR4_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR4_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR4_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3343. CONTROLSS\_MDLXBAR4\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR4_G0_SEL | R/W  | 0h    | MDL XBAR4 G0 input bit select. Input source is PWMA sclk select<br>1:PWMA sclk bit[x] selected<br>0:PWMA sclk bit[x] is de-selected |



### 3.17.2.14 CONTROLSS\_MDLXBAR4\_G1 Register

#### 1 CONTROLSS\_MDLXBAR4\_G1 Register (Offset = 204h) [reset = 0h]

MDL XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-3344. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3204h       |

**Figure 3-1091. CONTROLSS\_MDLXBAR4\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR4_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR4_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR4_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR4_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3346. CONTROLSS\_MDLXBAR4\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR4_G1_SEL | R/W  | 0h    | MDL XBAR4 G1 input bit select. Input source is PWMB sclk select<br>1:PWMB sclk bit[x] selected<br>0:PWMB sclk bit[x] is de-selected |

### 3.17.2.15 CONTROLSS\_MDLXBAR4\_G2 Register

#### 1 CONTROLSS\_MDLXBAR4\_G2 Register (Offset = 208h) [reset = 0h]

MDL XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-3347. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3208h       |

**Figure 3-1092. CONTROLSS\_MDLXBAR4\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR4_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR4_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR4_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR4_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3349. CONTROLSS\_MDLXBAR4\_G2 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR4_G2_SEL | R/W  | 0h    | MDL XBAR4 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

### 3.17.2.16 CONTROLSS\_MDLXBAR5\_G0 Register

#### 1 CONTROLSS\_MDLXBAR5\_G0 Register (Offset = 240h) [reset = 0h]

MDL XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-3350. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3240h       |

**Figure 3-1093. CONTROLSS\_MDLXBAR5\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR5_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR5_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR5_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR5_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3352. CONTROLSS\_MDLXBAR5\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR5_G0_SEL | R/W  | 0h    | MDL XBAR5 G0 input bit select. Input source is PWMA sclk select<br>1:PWMA sclk bit[x] selected<br>0:PWMA sclk bit[x] is de-selected |

### 3.17.2.17 CONTROLSS\_MDLXBAR5\_G1 Register

#### 1 CONTROLSS\_MDLXBAR5\_G1 Register (Offset = 244h) [reset = 0h]

MDL XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-3353. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3244h       |

**Figure 3-1094. CONTROLSS\_MDLXBAR5\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR5_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR5_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR5_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR5_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3355. CONTROLSS\_MDLXBAR5\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR5_G1_SEL | R/W  | 0h    | MDL XBAR5 G1 input bit select. Input source is PWMB sclk select<br>1:PWMB sclk bit[x] selected<br>0:PWMB sclk bit[x] is de-selected |

### 3.17.2.18 CONTROLSS\_MDLXBAR5\_G2 Register

#### 1 CONTROLSS\_MDLXBAR5\_G2 Register (Offset = 248h) [reset = 0h]

MDL XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-3356. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3248h       |

**Figure 3-1095. CONTROLSS\_MDLXBAR5\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR5_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR5_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR5_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR5_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3358. CONTROLSS\_MDLXBAR5\_G2 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR5_G2_SEL | R/W  | 0h    | MDL XBAR5 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

### 3.17.2.19 CONTROLSS\_MDLXBAR6\_G0 Register

#### 1 CONTROLSS\_MDLXBAR6\_G0 Register (Offset = 280h) [reset = 0h]

MDL XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-3359. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3280h       |

**Figure 3-1096. CONTROLSS\_MDLXBAR6\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR6_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR6_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR6_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR6_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3361. CONTROLSS\_MDLXBAR6\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR6_G0_SEL | R/W  | 0h    | MDL XBAR6 G0 input bit select. Input source is PWMA sclk select<br>1:PWMA sclk bit[x] selected<br>0:PWMA sclk bit[x] is de-selected |

### 3.17.2.20 CONTROLSS\_MDLXBAR6\_G1 Register

#### 1 CONTROLSS\_MDLXBAR6\_G1 Register (Offset = 284h) [reset = 0h]

MDL XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-3362. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3284h       |

**Figure 3-1097. CONTROLSS\_MDLXBAR6\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR6_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR6_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR6_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR6_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3364. CONTROLSS\_MDLXBAR6\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR6_G1_SEL | R/W  | 0h    | MDL XBAR6 G1 input bit select. Input source is PWMB sclk select<br>1:PWMB sclk bit[x] selected<br>0:PWMB sclk bit[x] is de-selected |

### 3.17.2.21 CONTROLSS\_MDLXBAR6\_G2 Register

#### 1 CONTROLSS\_MDLXBAR6\_G2 Register (Offset = 288h) [reset = 0h]

MDL XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-3365. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3288h       |

**Figure 3-1098. CONTROLSS\_MDLXBAR6\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR6_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR6_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR6_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR6_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3367. CONTROLSS\_MDLXBAR6\_G2 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR6_G2_SEL | R/W  | 0h    | MDL XBAR6 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |



### 3.17.2.22 CONTROLSS\_MDLXBAR7\_G0 Register

#### 1 CONTROLSS\_MDLXBAR7\_G0 Register (Offset = 2C0h) [reset = 0h]

MDL XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-3368. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 32C0h       |

**Figure 3-1099. CONTROLSS\_MDLXBAR7\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR7_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR7_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR7_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR7_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3370. CONTROLSS\_MDLXBAR7\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR7_G0_SEL | R/W  | 0h    | MDL XBAR7 G0 input bit select. Input source is PWMA sclk select<br>1:PWMA sclk bit[x] selected<br>0:PWMA sclk bit[x] is de-selected |

### 3.17.2.23 CONTROLSS\_MDLXBAR7\_G1 Register

#### 1 CONTROLSS\_MDLXBAR7\_G1 Register (Offset = 2C4h) [reset = 0h]

MDL XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-3371. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 32C4h       |

**Figure 3-1100. CONTROLSS\_MDLXBAR7\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR7_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR7_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR7_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR7_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3373. CONTROLSS\_MDLXBAR7\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR7_G1_SEL | R/W  | 0h    | MDL XBAR7 G1 input bit select. Input source is PWMB sclk select<br>1:PWMB sclk bit[x] selected<br>0:PWMB sclk bit[x] is de-selected |

### 3.17.2.24 CONTROLSS\_MDLXBAR7\_G2 Register

#### 1 CONTROLSS\_MDLXBAR7\_G2 Register (Offset = 2C8h) [reset = 0h]

MDL XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-3374. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 32C8h       |

**Figure 3-1101. CONTROLSS\_MDLXBAR7\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR7_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR7_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR7_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR7_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3376. CONTROLSS\_MDLXBAR7\_G2 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR7_G2_SEL | R/W  | 0h    | MDL XBAR7 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

### 3.17.2.25 CONTROLSS\_MDLXBAR8\_G0 Register

#### 1 CONTROLSS\_MDLXBAR8\_G0 Register (Offset = 300h) [reset = 0h]

MDL XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-3377. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3300h       |

**Figure 3-1102. CONTROLSS\_MDLXBAR8\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR8_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR8_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR8_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR8_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3379. CONTROLSS\_MDLXBAR8\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR8_G0_SEL | R/W  | 0h    | MDL XBAR8 G0 input bit select. Input source is PWMA sclk select<br>1:PWMA sclk bit[x] selected<br>0:PWMA sclk bit[x] is de-selected |

### 3.17.2.26 CONTROLSS\_MDLXBAR8\_G1 Register

#### 1 CONTROLSS\_MDLXBAR8\_G1 Register (Offset = 304h) [reset = 0h]

MDL XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-3380. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3304h       |

**Figure 3-1103. CONTROLSS\_MDLXBAR8\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR8_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR8_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR8_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR8_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3382. CONTROLSS\_MDLXBAR8\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR8_G1_SEL | R/W  | 0h    | MDL XBAR8 G1 input bit select. Input source is PWMB sclk select<br>1:PWMB sclk bit[x] selected<br>0:PWMB sclk bit[x] is de-selected |

### 3.17.2.27 CONTROLSS\_MDLXBAR8\_G2 Register

#### 1 CONTROLSS\_MDLXBAR8\_G2 Register (Offset = 308h) [reset = 0h]

MDL XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-3383. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3308h       |

**Figure 3-1104. CONTROLSS\_MDLXBAR8\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR8_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR8_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR8_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR8_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3385. CONTROLSS\_MDLXBAR8\_G2 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR8_G2_SEL | R/W  | 0h    | MDL XBAR8 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

### 3.17.2.28 CONTROLSS\_MDLXBAR9\_G0 Register

#### 1 CONTROLSS\_MDLXBAR9\_G0 Register (Offset = 340h) [reset = 0h]

MDL XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-3386. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3340h       |

**Figure 3-1105. CONTROLSS\_MDLXBAR9\_G0 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR9_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR9_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR9_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR9_G0_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3388. CONTROLSS\_MDLXBAR9\_G0 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR9_G0_SEL | R/W  | 0h    | MDL XBAR9 G0 input bit select. Input source is PWMA sclk select<br>1:PWMA sclk bit[x] selected<br>0:PWMA sclk bit[x] is de-selected |

### 3.17.2.29 CONTROLSS\_MDLXBAR9\_G1 Register

#### 1 CONTROLSS\_MDLXBAR9\_G1 Register (Offset = 344h) [reset = 0h]

MDL XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-3389. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3344h       |

**Figure 3-1106. CONTROLSS\_MDLXBAR9\_G1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR9_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR9_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR9_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR9_G1_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3391. CONTROLSS\_MDLXBAR9\_G1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR9_G1_SEL | R/W  | 0h    | MDL XBAR9 G1 input bit select. Input source is PWMB sclk select<br>1:PWMB sclk bit[x] selected<br>0:PWMB sclk bit[x] is de-selected |



### 3.17.2.30 CONTROLSS\_MDLXBAR9\_G2 Register

#### 1 CONTROLSS\_MDLXBAR9\_G2 Register (Offset = 348h) [reset = 0h]

MDL XBAR 9 Input Select.

Return to [Summary Table](#)
**Table 3-3392. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3348h       |

**Figure 3-1107. CONTROLSS\_MDLXBAR9\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR9_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR9_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR9_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR9_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-3394. CONTROLSS\_MDLXBAR9\_G2 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR9_G2_SEL | R/W  | 0h    | MDL XBAR9 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

### 3.17.2.31 CONTROLSS\_MDLXBAR10\_G0 Register

#### 1 CONTROLSS\_MDLXBAR10\_G0 Register (Offset = 380h) [reset = 0h]

MDL XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-3395. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3380h       |

**Figure 3-1108. CONTROLSS\_MDLXBAR10\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR10_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR10_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR10_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR10_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3397. CONTROLSS\_MDLXBAR10\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR10_G0_SEL | R/W  | 0h    | MDL XBAR10 G0 input bit select. Input source is PWMA sclk select<br>1:PWMA sclk bit[x] selected<br>0:PWMA sclk bit[x] is de-selected |

### 3.17.2.32 CONTROLSS\_MDLXBAR10\_G1 Register

#### 1 CONTROLSS\_MDLXBAR10\_G1 Register (Offset = 384h) [reset = 0h]

MDL XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-3398. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3384h       |

**Figure 3-1109. CONTROLSS\_MDLXBAR10\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR10_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR10_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR10_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR10_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3400. CONTROLSS\_MDLXBAR10\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR10_G1_SEL | R/W  | 0h    | MDL XBAR10 G1 input bit select. Input source is PWMB sclk select<br>1:PWMB sclk bit[x] selected<br>0:PWMB sclk bit[x] is de-selected |

### 3.17.2.33 CONTROLSS\_MDLXBAR10\_G2 Register

#### 1 CONTROLSS\_MDLXBAR10\_G2 Register (Offset = 388h) [reset = 0h]

MDL XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-3401. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3388h       |

**Figure 3-1110. CONTROLSS\_MDLXBAR10\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR10_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR10_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR10_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR10_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3403. CONTROLSS\_MDLXBAR10\_G2 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR10_G2_SEL | R/W  | 0h    | MDL XBAR10 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

### 3.17.2.34 CONTROLSS\_MDLXBAR11\_G0 Register

#### 1 CONTROLSS\_MDLXBAR11\_G0 Register (Offset = 3C0h) [reset = 0h]

MDL XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-3404. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 33C0h       |

**Figure 3-1111. CONTROLSS\_MDLXBAR11\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR11_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR11_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR11_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR11_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3406. CONTROLSS\_MDLXBAR11\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR11_G0_SEL | R/W  | 0h    | MDL XBAR11 G0 input bit select. Input source is PWMA sclk select<br>1:PWMA sclk bit[x] selected<br>0:PWMA sclk bit[x] is de-selected |

### 3.17.2.35 CONTROLSS\_MDLXBAR11\_G1 Register

#### 1 CONTROLSS\_MDLXBAR11\_G1 Register (Offset = 3C4h) [reset = 0h]

MDL XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-3407. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 33C4h       |

**Figure 3-1112. CONTROLSS\_MDLXBAR11\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR11_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR11_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR11_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR11_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3409. CONTROLSS\_MDLXBAR11\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR11_G1_SEL | R/W  | 0h    | MDL XBAR11 G1 input bit select. Input source is PWMB sclk select<br>1:PWMB sclk bit[x] selected<br>0:PWMB sclk bit[x] is de-selected |

### 3.17.2.36 CONTROLSS\_MDLXBAR11\_G2 Register

#### 1 CONTROLSS\_MDLXBAR11\_G2 Register (Offset = 3C8h) [reset = 0h]

MDL XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-3410. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 33C8h       |

**Figure 3-1113. CONTROLSS\_MDLXBAR11\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR11_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR11_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR11_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR11_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3412. CONTROLSS\_MDLXBAR11\_G2 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR11_G2_SEL | R/W  | 0h    | MDL XBAR11 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

### 3.17.2.37 CONTROLSS\_MDLXBAR12\_G0 Register

#### 1 CONTROLSS\_MDLXBAR12\_G0 Register (Offset = 400h) [reset = 0h]

MDL XBAR 12 Input Select.

Return to [Summary Table](#)
**Table 3-3413. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3400h       |

**Figure 3-1114. CONTROLSS\_MDLXBAR12\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR12_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR12_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR12_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR12_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3415. CONTROLSS\_MDLXBAR12\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR12_G0_SEL | R/W  | 0h    | MDL XBAR12 G0 input bit select. Input source is PWMA sclk select<br>1:PWMA sclk bit[x] selected<br>0:PWMA sclk bit[x] is de-selected |



### 3.17.2.38 CONTROLSS\_MDLXBAR12\_G1 Register

#### 1 CONTROLSS\_MDLXBAR12\_G1 Register (Offset = 404h) [reset = 0h]

MDL XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-3416. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3404h       |

**Figure 3-1115. CONTROLSS\_MDLXBAR12\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR12_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR12_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR12_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR12_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3418. CONTROLSS\_MDLXBAR12\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR12_G1_SEL | R/W  | 0h    | MDL XBAR12 G1 input bit select. Input source is PWMB sclk select<br>1:PWMB sclk bit[x] selected<br>0:PWMB sclk bit[x] is de-selected |

### 3.17.2.39 CONTROLSS\_MDLXBAR12\_G2 Register

#### 1 CONTROLSS\_MDLXBAR12\_G2 Register (Offset = 408h) [reset = 0h]

MDL XBAR 12 Input Select.

Return to [Summary Table](#)
**Table 3-3419. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3408h       |

**Figure 3-1116. CONTROLSS\_MDLXBAR12\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR12_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR12_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR12_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR12_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3421. CONTROLSS\_MDLXBAR12\_G2 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR12_G2_SEL | R/W  | 0h    | MDL XBAR12 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

### 3.17.2.40 CONTROLSS\_MDLXBAR13\_G0 Register

#### 1 CONTROLSS\_MDLXBAR13\_G0 Register (Offset = 440h) [reset = 0h]

MDL XBAR 13 Input Select.

Return to [Summary Table](#)
**Table 3-3422. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3440h       |

**Figure 3-1117. CONTROLSS\_MDLXBAR13\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR13_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR13_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR13_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR13_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3424. CONTROLSS\_MDLXBAR13\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR13_G0_SEL | R/W  | 0h    | MDL XBAR13 G0 input bit select. Input source is PWMA sclk select<br>1:PWMA sclk bit[x] selected<br>0:PWMA sclk bit[x] is de-selected |

### 3.17.2.41 CONTROLSS\_MDLXBAR13\_G1 Register

#### 1 CONTROLSS\_MDLXBAR13\_G1 Register (Offset = 444h) [reset = 0h]

MDL XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-3425. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3444h       |

**Figure 3-1118. CONTROLSS\_MDLXBAR13\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR13_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR13_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR13_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR13_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3427. CONTROLSS\_MDLXBAR13\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR13_G1_SEL | R/W  | 0h    | MDL XBAR13 G1 input bit select. Input source is PWMB sclk select<br>1:PWMB sclk bit[x] selected<br>0:PWMB sclk bit[x] is de-selected |

### 3.17.2.42 CONTROLSS\_MDLXBAR13\_G2 Register

#### 1 CONTROLSS\_MDLXBAR13\_G2 Register (Offset = 448h) [reset = 0h]

MDL XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-3428. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3448h       |

**Figure 3-1119. CONTROLSS\_MDLXBAR13\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR13_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR13_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR13_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR13_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3430. CONTROLSS\_MDLXBAR13\_G2 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR13_G2_SEL | R/W  | 0h    | MDL XBAR13 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

### 3.17.2.43 CONTROLSS\_MDLXBAR14\_G0 Register

#### 1 CONTROLSS\_MDLXBAR14\_G0 Register (Offset = 480h) [reset = 0h]

MDL XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-3431. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3480h       |

**Figure 3-1120. CONTROLSS\_MDLXBAR14\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR14_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR14_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR14_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR14_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3433. CONTROLSS\_MDLXBAR14\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR14_G0_SEL | R/W  | 0h    | MDL XBAR14 G0 input bit select. Input source is PWMA sclk select<br>1:PWMA sclk bit[x] selected<br>0:PWMA sclk bit[x] is de-selected |

### 3.17.2.44 CONTROLSS\_MDLXBAR14\_G1 Register

#### 1 CONTROLSS\_MDLXBAR14\_G1 Register (Offset = 484h) [reset = 0h]

MDL XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-3434. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3484h       |

**Figure 3-1121. CONTROLSS\_MDLXBAR14\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR14_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR14_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR14_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR14_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3436. CONTROLSS\_MDLXBAR14\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR14_G1_SEL | R/W  | 0h    | MDL XBAR14 G1 input bit select. Input source is PWMB sclk select<br>1:PWMB sclk bit[x] selected<br>0:PWMB sclk bit[x] is de-selected |

### 3.17.2.45 CONTROLSS\_MDLXBAR14\_G2 Register

#### 1 CONTROLSS\_MDLXBAR14\_G2 Register (Offset = 488h) [reset = 0h]

MDL XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-3437. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 3488h       |

**Figure 3-1122. CONTROLSS\_MDLXBAR14\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR14_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR14_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR14_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR14_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3439. CONTROLSS\_MDLXBAR14\_G2 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR14_G2_SEL | R/W  | 0h    | MDL XBAR14 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |



### 3.17.2.46 CONTROLSS\_MDLXBAR15\_G0 Register

#### 1 CONTROLSS\_MDLXBAR15\_G0 Register (Offset = 4C0h) [reset = 0h]

MDL XBAR 15 Input Select .

Return to [Summary Table](#)

**Table 3-3440. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 34C0h       |

**Figure 3-1123. CONTROLSS\_MDLXBAR15\_G0 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR15_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR15_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR15_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR15_G0_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3442. CONTROLSS\_MDLXBAR15\_G0 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR15_G0_SEL | R/W  | 0h    | MDL XBAR15 G0 input bit select. Input source is PWMA sclk select<br>1:PWMA sclk bit[x] selected<br>0:PWMA sclk bit[x] is de-selected |

### 3.17.2.47 CONTROLSS\_MDLXBAR15\_G1 Register

#### 1 CONTROLSS\_MDLXBAR15\_G1 Register (Offset = 4C4h) [reset = 0h]

MDL XBAR 15 Input Select .

Return to [Summary Table](#)
**Table 3-3443. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 34C4h       |

**Figure 3-1124. CONTROLSS\_MDLXBAR15\_G1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR15_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR15_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR15_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR15_G1_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3445. CONTROLSS\_MDLXBAR15\_G1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR15_G1_SEL | R/W  | 0h    | MDL XBAR15 G1 input bit select. Input source is PWMB sclk select<br>1:PWMB sclk bit[x] selected<br>0:PWMB sclk bit[x] is de-selected |

### 3.17.2.48 CONTROLSS\_MDLXBAR15\_G2 Register

#### 1 CONTROLSS\_MDLXBAR15\_G2 Register (Offset = 4C8h) [reset = 0h]

MDL XBAR 15 Input Select .

Return to [Summary Table](#)

**Table 3-3446. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_MDLXBAR | 502D 34C8h       |

**Figure 3-1125. CONTROLSS\_MDLXBAR15\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MDLXBAR15_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MDLXBAR15_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MDLXBAR15_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MDLXBAR15_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-3448. CONTROLSS\_MDLXBAR15\_G2 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MDLXBAR15_G2_SEL | R/W  | 0h    | MDL XBAR15 G2 input bit select. Input source is ICSS GPO select<br>y=0 when x =0 to 15, y=1 when x=16 to 31<br>1:ICSS_PORT[y].GPO[x] selected.<br>0:ICSS_PORT[y].GPO[x] is de-selected |

## 3.18 CONTROLSS\_OUTPUTXBAR

### CONTROLSS\_OUTPUTXBAR

#### 3.18.1 CONTROLSS\_OUTPUTXBAR Summaries

#### CONTROLSS\_OUTPUTXBAR Summaries

**Table 3-3449. CONTROLSS Registers, Base Address=502D 8000h, Length=1024**

| Offset | Length | Register Name                                   | CONTROLSS_OUTPUTXBAR Physical Address |
|--------|--------|-------------------------------------------------|---------------------------------------|
| 10h    | 32     | <a href="#">CONTROLSS_OUTPUTXBAR_STATUS</a>     | 502D 8010h                            |
| 14h    | 32     | <a href="#">CONTROLSS_OUTPUTXBAR_FLAGINVERT</a> | 502D 8014h                            |
| 18h    | 32     | <a href="#">CONTROLSS_OUTPUTXBAR_FLAG</a>       | 502D 8018h                            |
| 1Ch    | 32     | <a href="#">CONTROLSS_OUTPUTXBAR_FLAG_CLR</a>   | 502D 801Ch                            |
| 20h    | 32     | <a href="#">CONTROLSS_OUTPUTXBAR_FLAGFORCE</a>  | 502D 8020h                            |
| 24h    | 32     | <a href="#">CONTROLSS_OUTPUTXBAR_OUTLATCH</a>   | 502D 8024h                            |
| 28h    | 32     | <a href="#">CONTROLSS_OUTPUTXBAR_OUTSTRETCH</a> | 502D 8028h                            |
| 2Ch    | 32     | <a href="#">CONTROLSS_OUTPUTXBAR_OUTLENGTH</a>  | 502D 802Ch                            |
| 30h    | 32     | <a href="#">CONTROLSS_OUTPUTXBAR_OUTINVERT</a>  | 502D 8030h                            |
| 100h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR0_G0</a>        | 502D 8100h                            |
| 104h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR0_G1</a>        | 502D 8104h                            |
| 108h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR0_G2</a>        | 502D 8108h                            |
| 10Ch   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR0_G3</a>        | 502D 810Ch                            |
| 110h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR0_G4</a>        | 502D 8110h                            |
| 114h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR0_G5</a>        | 502D 8114h                            |
| 118h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR0_G6</a>        | 502D 8118h                            |
| 11Ch   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR0_G7</a>        | 502D 811Ch                            |
| 120h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR0_G8</a>        | 502D 8120h                            |
| 124h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR0_G9</a>        | 502D 8124h                            |
| 128h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR0_G10</a>       | 502D 8128h                            |
| 140h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR1_G0</a>        | 502D 8140h                            |
| 144h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR1_G1</a>        | 502D 8144h                            |
| 148h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR1_G2</a>        | 502D 8148h                            |
| 14Ch   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR1_G3</a>        | 502D 814Ch                            |
| 150h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR1_G4</a>        | 502D 8150h                            |
| 154h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR1_G5</a>        | 502D 8154h                            |
| 158h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR1_G6</a>        | 502D 8158h                            |
| 15Ch   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR1_G7</a>        | 502D 815Ch                            |
| 160h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR1_G8</a>        | 502D 8160h                            |
| 164h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR1_G9</a>        | 502D 8164h                            |
| 168h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR1_G10</a>       | 502D 8168h                            |
| 180h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR2_G0</a>        | 502D 8180h                            |
| 184h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR2_G1</a>        | 502D 8184h                            |
| 188h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR2_G2</a>        | 502D 8188h                            |
| 18Ch   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR2_G3</a>        | 502D 818Ch                            |
| 190h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR2_G4</a>        | 502D 8190h                            |
| 194h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR2_G5</a>        | 502D 8194h                            |

**Table 3-3449. CONTROLSS Registers, Base Address=502D 8000h, Length=1024 (continued)**

| Offset | Length | Register Name                             | CONTROLSS_OUTPUTXBAR Physical Address |
|--------|--------|-------------------------------------------|---------------------------------------|
| 198h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR2_G6</a>  | 502D 8198h                            |
| 19Ch   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR2_G7</a>  | 502D 819Ch                            |
| 1A0h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR2_G8</a>  | 502D 81A0h                            |
| 1A4h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR2_G9</a>  | 502D 81A4h                            |
| 1A8h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR2_G10</a> | 502D 81A8h                            |
| 1C0h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR3_G0</a>  | 502D 81C0h                            |
| 1C4h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR3_G1</a>  | 502D 81C4h                            |
| 1C8h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR3_G2</a>  | 502D 81C8h                            |
| 1CCh   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR3_G3</a>  | 502D 81CCh                            |
| 1D0h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR3_G4</a>  | 502D 81D0h                            |
| 1D4h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR3_G5</a>  | 502D 81D4h                            |
| 1D8h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR3_G6</a>  | 502D 81D8h                            |
| 1DCh   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR3_G7</a>  | 502D 81DCh                            |
| 1E0h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR3_G8</a>  | 502D 81E0h                            |
| 1E4h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR3_G9</a>  | 502D 81E4h                            |
| 1E8h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR3_G10</a> | 502D 81E8h                            |
| 200h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR4_G0</a>  | 502D 8200h                            |
| 204h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR4_G1</a>  | 502D 8204h                            |
| 208h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR4_G2</a>  | 502D 8208h                            |
| 20Ch   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR4_G3</a>  | 502D 820Ch                            |
| 210h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR4_G4</a>  | 502D 8210h                            |
| 214h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR4_G5</a>  | 502D 8214h                            |
| 218h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR4_G6</a>  | 502D 8218h                            |
| 21Ch   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR4_G7</a>  | 502D 821Ch                            |
| 220h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR4_G8</a>  | 502D 8220h                            |
| 224h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR4_G9</a>  | 502D 8224h                            |
| 228h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR4_G10</a> | 502D 8228h                            |
| 240h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR5_G0</a>  | 502D 8240h                            |
| 244h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR5_G1</a>  | 502D 8244h                            |
| 248h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR5_G2</a>  | 502D 8248h                            |
| 24Ch   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR5_G3</a>  | 502D 824Ch                            |
| 250h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR5_G4</a>  | 502D 8250h                            |
| 254h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR5_G5</a>  | 502D 8254h                            |
| 258h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR5_G6</a>  | 502D 8258h                            |
| 25Ch   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR5_G7</a>  | 502D 825Ch                            |
| 260h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR5_G8</a>  | 502D 8260h                            |
| 264h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR5_G9</a>  | 502D 8264h                            |
| 268h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR5_G10</a> | 502D 8268h                            |
| 280h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR6_G0</a>  | 502D 8280h                            |
| 284h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR6_G1</a>  | 502D 8284h                            |
| 288h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR6_G2</a>  | 502D 8288h                            |
| 28Ch   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR6_G3</a>  | 502D 828Ch                            |
| 290h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR6_G4</a>  | 502D 8290h                            |
| 294h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR6_G5</a>  | 502D 8294h                            |

**Table 3-3449. CONTROLSS Registers, Base Address=502D 8000h, Length=1024 (continued)**

| Offset | Length | Register Name                             | CONTROLSS_OUTPUTXBAR Physical Address |
|--------|--------|-------------------------------------------|---------------------------------------|
| 298h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR6_G6</a>  | 502D 8298h                            |
| 29Ch   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR6_G7</a>  | 502D 829Ch                            |
| 2A0h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR6_G8</a>  | 502D 82A0h                            |
| 2A4h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR6_G9</a>  | 502D 82A4h                            |
| 2A8h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR6_G10</a> | 502D 82A8h                            |
| 2C0h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR7_G0</a>  | 502D 82C0h                            |
| 2C4h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR7_G1</a>  | 502D 82C4h                            |
| 2C8h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR7_G2</a>  | 502D 82C8h                            |
| 2CCh   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR7_G3</a>  | 502D 82CCh                            |
| 2D0h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR7_G4</a>  | 502D 82D0h                            |
| 2D4h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR7_G5</a>  | 502D 82D4h                            |
| 2D8h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR7_G6</a>  | 502D 82D8h                            |
| 2DCh   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR7_G7</a>  | 502D 82DCh                            |
| 2E0h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR7_G8</a>  | 502D 82E0h                            |
| 2E4h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR7_G9</a>  | 502D 82E4h                            |
| 2E8h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR7_G10</a> | 502D 82E8h                            |
| 300h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR8_G0</a>  | 502D 8300h                            |
| 304h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR8_G1</a>  | 502D 8304h                            |
| 308h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR8_G2</a>  | 502D 8308h                            |
| 30Ch   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR8_G3</a>  | 502D 830Ch                            |
| 310h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR8_G4</a>  | 502D 8310h                            |
| 314h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR8_G5</a>  | 502D 8314h                            |
| 318h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR8_G6</a>  | 502D 8318h                            |
| 31Ch   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR8_G7</a>  | 502D 831Ch                            |
| 320h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR8_G8</a>  | 502D 8320h                            |
| 324h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR8_G9</a>  | 502D 8324h                            |
| 328h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR8_G10</a> | 502D 8328h                            |
| 340h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR9_G0</a>  | 502D 8340h                            |
| 344h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR9_G1</a>  | 502D 8344h                            |
| 348h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR9_G2</a>  | 502D 8348h                            |
| 34Ch   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR9_G3</a>  | 502D 834Ch                            |
| 350h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR9_G4</a>  | 502D 8350h                            |
| 354h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR9_G5</a>  | 502D 8354h                            |
| 358h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR9_G6</a>  | 502D 8358h                            |
| 35Ch   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR9_G7</a>  | 502D 835Ch                            |
| 360h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR9_G8</a>  | 502D 8360h                            |
| 364h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR9_G9</a>  | 502D 8364h                            |
| 368h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR9_G10</a> | 502D 8368h                            |
| 380h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR10_G0</a> | 502D 8380h                            |
| 384h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR10_G1</a> | 502D 8384h                            |
| 388h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR10_G2</a> | 502D 8388h                            |
| 38Ch   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR10_G3</a> | 502D 838Ch                            |
| 390h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR10_G4</a> | 502D 8390h                            |
| 394h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR10_G5</a> | 502D 8394h                            |

**Table 3-3449. CONTROLSS Registers, Base Address=502D 8000h, Length=1024 (continued)**

| Offset | Length | Register Name                              | CONTROLSS_OUTPUTXBAR Physical Address |
|--------|--------|--------------------------------------------|---------------------------------------|
| 398h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR10_G6</a>  | 502D 8398h                            |
| 39Ch   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR10_G7</a>  | 502D 839Ch                            |
| 3A0h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR10_G8</a>  | 502D 83A0h                            |
| 3A4h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR10_G9</a>  | 502D 83A4h                            |
| 3A8h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR10_G10</a> | 502D 83A8h                            |
| 3C0h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR11_G0</a>  | 502D 83C0h                            |
| 3C4h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR11_G1</a>  | 502D 83C4h                            |
| 3C8h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR11_G2</a>  | 502D 83C8h                            |
| 3CCh   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR11_G3</a>  | 502D 83CCh                            |
| 3D0h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR11_G4</a>  | 502D 83D0h                            |
| 3D4h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR11_G5</a>  | 502D 83D4h                            |
| 3D8h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR11_G6</a>  | 502D 83D8h                            |
| 3DCh   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR11_G7</a>  | 502D 83DCh                            |
| 3E0h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR11_G8</a>  | 502D 83E0h                            |
| 3E4h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR11_G9</a>  | 502D 83E4h                            |
| 3E8h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR11_G10</a> | 502D 83E8h                            |
| 400h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR12_G0</a>  | 502D 8400h                            |
| 404h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR12_G1</a>  | 502D 8404h                            |
| 408h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR12_G2</a>  | 502D 8408h                            |
| 40Ch   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR12_G3</a>  | 502D 840Ch                            |
| 410h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR12_G4</a>  | 502D 8410h                            |
| 414h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR12_G5</a>  | 502D 8414h                            |
| 418h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR12_G6</a>  | 502D 8418h                            |
| 41Ch   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR12_G7</a>  | 502D 841Ch                            |
| 420h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR12_G8</a>  | 502D 8420h                            |
| 424h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR12_G9</a>  | 502D 8424h                            |
| 428h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR12_G10</a> | 502D 8428h                            |
| 440h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR13_G0</a>  | 502D 8440h                            |
| 444h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR13_G1</a>  | 502D 8444h                            |
| 448h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR13_G2</a>  | 502D 8448h                            |
| 44Ch   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR13_G3</a>  | 502D 844Ch                            |
| 450h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR13_G4</a>  | 502D 8450h                            |
| 454h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR13_G5</a>  | 502D 8454h                            |
| 458h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR13_G6</a>  | 502D 8458h                            |
| 45Ch   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR13_G7</a>  | 502D 845Ch                            |
| 460h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR13_G8</a>  | 502D 8460h                            |
| 464h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR13_G9</a>  | 502D 8464h                            |
| 468h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR13_G10</a> | 502D 8468h                            |
| 480h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR14_G0</a>  | 502D 8480h                            |
| 484h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR14_G1</a>  | 502D 8484h                            |
| 488h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR14_G2</a>  | 502D 8488h                            |
| 48Ch   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR14_G3</a>  | 502D 848Ch                            |
| 490h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR14_G4</a>  | 502D 8490h                            |
| 494h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR14_G5</a>  | 502D 8494h                            |

**Table 3-3449. CONTROLSS Registers, Base Address=502D 8000h, Length=1024 (continued)**

| Offset | Length | Register Name                              | CONTROLSS_OUTPUTXBAR Physical Address |
|--------|--------|--------------------------------------------|---------------------------------------|
| 498h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR14_G6</a>  | 502D 8498h                            |
| 49Ch   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR14_G7</a>  | 502D 849Ch                            |
| 4A0h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR14_G8</a>  | 502D 84A0h                            |
| 4A4h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR14_G9</a>  | 502D 84A4h                            |
| 4A8h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR14_G10</a> | 502D 84A8h                            |
| 4C0h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR15_G0</a>  | 502D 84C0h                            |
| 4C4h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR15_G1</a>  | 502D 84C4h                            |
| 4C8h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR15_G2</a>  | 502D 84C8h                            |
| 4CCh   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR15_G3</a>  | 502D 84CCh                            |
| 4D0h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR15_G4</a>  | 502D 84D0h                            |
| 4D4h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR15_G5</a>  | 502D 84D4h                            |
| 4D8h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR15_G6</a>  | 502D 84D8h                            |
| 4DCh   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR15_G7</a>  | 502D 84DCh                            |
| 4E0h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR15_G8</a>  | 502D 84E0h                            |
| 4E4h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR15_G9</a>  | 502D 84E4h                            |
| 4E8h   | 32     | <a href="#">CONTROLSS_OUTPUTXBAR15_G10</a> | 502D 84E8h                            |

### 3.18.2 CONTROLSS\_OUTPUTXBAR Registers

#### CONTROLSS\_OUTPUTXBAR Registers



### 3.18.2.1 CONTROLSS\_OUTPUTXBAR\_STATUS Register

#### 1 CONTROLSS\_OUTPUTXBAR\_STATUS Register (Offset = 10h) [reset = 0h]

Output Signal Status.

Return to [Summary Table](#)

**Table 3-3450. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8010h       |

**Figure 3-1126. CONTROLSS\_OUTPUTXBAR\_STATUS Name Register**

|                       |    |    |    |    |    |    |    |
|-----------------------|----|----|----|----|----|----|----|
| 31                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED              |    |    |    |    |    |    |    |
| NONE                  |    |    |    |    |    |    |    |
| 0h                    |    |    |    |    |    |    |    |
| 23                    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED              |    |    |    |    |    |    |    |
| NONE                  |    |    |    |    |    |    |    |
| 0h                    |    |    |    |    |    |    |    |
| 15                    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR_STATUS_STS |    |    |    |    |    |    |    |
| R                     |    |    |    |    |    |    |    |
| 0h                    |    |    |    |    |    |    |    |
| 7                     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR_STATUS_STS |    |    |    |    |    |    |    |
| R                     |    |    |    |    |    |    |    |
| 0h                    |    |    |    |    |    |    |    |

**Table 3-3452. CONTROLSS\_OUTPUTXBAR\_STATUS Register Field Descriptions**

| Bit   | Field                 | Type | Reset | Description |
|-------|-----------------------|------|-------|-------------|
| 31:16 | RESERVED              | NONE | 0h    | Reserved    |
| 15:0  | OUTPUTXBAR_STATUS_STS | R    | 0h    | Status      |

### 3.18.2.2 CONTROLSS\_OUTPUTXBAR\_FLAGINVERT Register

#### 1 CONTROLSS\_OUTPUTXBAR\_FLAGINVERT Register (Offset = 14h) [reset = 0h]

Output Signal Invert Before Latch.

Return to [Summary Table](#)

**Table 3-3453. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8014h       |

**Figure 3-1127. CONTROLSS\_OUTPUTXBAR\_FLAGINVERT Name Register**

|                              |    |    |    |    |    |    |    |
|------------------------------|----|----|----|----|----|----|----|
| 31                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                     |    |    |    |    |    |    |    |
| NONE                         |    |    |    |    |    |    |    |
| 0h                           |    |    |    |    |    |    |    |
| 23                           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                     |    |    |    |    |    |    |    |
| NONE                         |    |    |    |    |    |    |    |
| 0h                           |    |    |    |    |    |    |    |
| 15                           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR_FLAGINVERT_INVERT |    |    |    |    |    |    |    |
| R/W                          |    |    |    |    |    |    |    |
| 0h                           |    |    |    |    |    |    |    |
| 7                            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR_FLAGINVERT_INVERT |    |    |    |    |    |    |    |
| R/W                          |    |    |    |    |    |    |    |
| 0h                           |    |    |    |    |    |    |    |

**Table 3-3455. CONTROLSS\_OUTPUTXBAR\_FLAGINVERT Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description |
|-------|------------------------------|------|-------|-------------|
| 31:16 | RESERVED                     | NONE | 0h    | Reserved    |
| 15:0  | OUTPUTXBAR_FLAGINVERT_INVERT | R/W  | 0h    | FlagInvert  |

### 3.18.2.3 CONTROLSS\_OUTPUTXBAR\_FLAG Register

#### 1 CONTROLSS\_OUTPUTXBAR\_FLAG Register (Offset = 18h) [reset = 0h]

Output Signal Latched Flag.

Return to [Summary Table](#)

**Table 3-3456. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8018h       |

**Figure 3-1128. CONTROLSS\_OUTPUTXBAR\_FLAG Name Register**

|                       |                       |                       |                       |                       |                       |                      |                      |
|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|----------------------|----------------------|
| 31                    | 30                    | 29                    | 28                    | 27                    | 26                    | 25                   | 24                   |
| RESERVED              |                       |                       |                       |                       |                       |                      |                      |
| NONE                  |                       |                       |                       |                       |                       |                      |                      |
| 0h                    |                       |                       |                       |                       |                       |                      |                      |
| 23                    | 22                    | 21                    | 20                    | 19                    | 18                    | 17                   | 16                   |
| RESERVED              |                       |                       |                       |                       |                       |                      |                      |
| NONE                  |                       |                       |                       |                       |                       |                      |                      |
| 0h                    |                       |                       |                       |                       |                       |                      |                      |
| 15                    | 14                    | 13                    | 12                    | 11                    | 10                    | 9                    | 8                    |
| OUTPUTXBAR_FLAG_BIT15 | OUTPUTXBAR_FLAG_BIT14 | OUTPUTXBAR_FLAG_BIT13 | OUTPUTXBAR_FLAG_BIT12 | OUTPUTXBAR_FLAG_BIT11 | OUTPUTXBAR_FLAG_BIT10 | OUTPUTXBAR_FLAG_BIT9 | OUTPUTXBAR_FLAG_BIT8 |
| R/W                   | R/W                   | R/W                   | R/W                   | R/W                   | R/W                   | R/W                  | R/W                  |
| 0h                    | 0h                    | 0h                    | 0h                    | 0h                    | 0h                    | 0h                   | 0h                   |
| 7                     | 6                     | 5                     | 4                     | 3                     | 2                     | 1                    | 0                    |
| OUTPUTXBAR_FLAG_BIT7  | OUTPUTXBAR_FLAG_BIT6  | OUTPUTXBAR_FLAG_BIT5  | OUTPUTXBAR_FLAG_BIT4  | OUTPUTXBAR_FLAG_BIT3  | OUTPUTXBAR_FLAG_BIT2  | OUTPUTXBAR_FLAG_BIT1 | OUTPUTXBAR_FLAG_BIT0 |
| R/W                   | R/W                   | R/W                   | R/W                   | R/W                   | R/W                   | R/W                  | R/W                  |
| 0h                    | 0h                    | 0h                    | 0h                    | 0h                    | 0h                    | 0h                   | 0h                   |

**Table 3-3458. CONTROLSS\_OUTPUTXBAR\_FLAG Register Field Descriptions**

| Bit   | Field                 | Type | Reset | Description      |
|-------|-----------------------|------|-------|------------------|
| 31:16 | RESERVED              | NONE | 0h    | Reserved         |
| 15    | OUTPUTXBAR_FLAG_BIT15 | R/W  | 0h    | Output XBAR flag |
| 14    | OUTPUTXBAR_FLAG_BIT14 | R/W  | 0h    | Output XBAR flag |
| 13    | OUTPUTXBAR_FLAG_BIT13 | R/W  | 0h    | Output XBAR flag |
| 12    | OUTPUTXBAR_FLAG_BIT12 | R/W  | 0h    | Output XBAR flag |
| 11    | OUTPUTXBAR_FLAG_BIT11 | R/W  | 0h    | Output XBAR flag |
| 10    | OUTPUTXBAR_FLAG_BIT10 | R/W  | 0h    | Output XBAR flag |
| 9     | OUTPUTXBAR_FLAG_BIT9  | R/W  | 0h    | Output XBAR flag |
| 8     | OUTPUTXBAR_FLAG_BIT8  | R/W  | 0h    | Output XBAR flag |
| 7     | OUTPUTXBAR_FLAG_BIT7  | R/W  | 0h    | Output XBAR flag |

**Table 3-3458. CONTROLSS\_OUTPUTXBAR\_FLAG Register Field Descriptions (continued)**

| Bit | Field                | Type | Reset | Description      |
|-----|----------------------|------|-------|------------------|
| 6   | OUTPUTXBAR_FLAG_BIT6 | R/W  | 0h    | Output XBAR flag |
| 5   | OUTPUTXBAR_FLAG_BIT5 | R/W  | 0h    | Output XBAR flag |
| 4   | OUTPUTXBAR_FLAG_BIT4 | R/W  | 0h    | Output XBAR flag |
| 3   | OUTPUTXBAR_FLAG_BIT3 | R/W  | 0h    | Output XBAR flag |
| 2   | OUTPUTXBAR_FLAG_BIT2 | R/W  | 0h    | Output XBAR flag |
| 1   | OUTPUTXBAR_FLAG_BIT1 | R/W  | 0h    | Output XBAR flag |
| 0   | OUTPUTXBAR_FLAG_BIT0 | R/W  | 0h    | Output XBAR flag |

### 3.18.2.4 CONTROLSS\_OUTPUTXBAR\_FLAG\_CLR Register

#### 1 CONTROLSS\_OUTPUTXBAR\_FLAG\_CLR Register (Offset = 1Ch) [reset = 0h]

Output Signal Latched Flag Clear.

Return to [Summary Table](#)

**Table 3-3459. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 801Ch       |

**Figure 3-1129. CONTROLSS\_OUTPUTXBAR\_FLAG\_CLR Name Register**

|                           |                           |                           |                           |                           |                           |                          |                          |
|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|--------------------------|--------------------------|
| 31                        | 30                        | 29                        | 28                        | 27                        | 26                        | 25                       | 24                       |
| RESERVED                  |                           |                           |                           |                           |                           |                          |                          |
| NONE                      |                           |                           |                           |                           |                           |                          |                          |
| 0h                        |                           |                           |                           |                           |                           |                          |                          |
| 23                        | 22                        | 21                        | 20                        | 19                        | 18                        | 17                       | 16                       |
| RESERVED                  |                           |                           |                           |                           |                           |                          |                          |
| NONE                      |                           |                           |                           |                           |                           |                          |                          |
| 0h                        |                           |                           |                           |                           |                           |                          |                          |
| 15                        | 14                        | 13                        | 12                        | 11                        | 10                        | 9                        | 8                        |
| OUTPUTXBAR_FLAG_CLR_BIT15 | OUTPUTXBAR_FLAG_CLR_BIT14 | OUTPUTXBAR_FLAG_CLR_BIT13 | OUTPUTXBAR_FLAG_CLR_BIT12 | OUTPUTXBAR_FLAG_CLR_BIT11 | OUTPUTXBAR_FLAG_CLR_BIT10 | OUTPUTXBAR_FLAG_CLR_BIT9 | OUTPUTXBAR_FLAG_CLR_BIT8 |
| R/W                       | R/W                       | R/W                       | R/W                       | R/W                       | R/W                       | R/W                      | R/W                      |
| 0h                        | 0h                        | 0h                        | 0h                        | 0h                        | 0h                        | 0h                       | 0h                       |
| 7                         | 6                         | 5                         | 4                         | 3                         | 2                         | 1                        | 0                        |
| OUTPUTXBAR_FLAG_CLR_BIT7  | OUTPUTXBAR_FLAG_CLR_BIT6  | OUTPUTXBAR_FLAG_CLR_BIT5  | OUTPUTXBAR_FLAG_CLR_BIT4  | OUTPUTXBAR_FLAG_CLR_BIT3  | OUTPUTXBAR_FLAG_CLR_BIT2  | OUTPUTXBAR_FLAG_CLR_BIT1 | OUTPUTXBAR_FLAG_CLR_BIT0 |
| R/W                       | R/W                       | R/W                       | R/W                       | R/W                       | R/W                       | R/W                      | R/W                      |
| 0h                        | 0h                        | 0h                        | 0h                        | 0h                        | 0h                        | 0h                       | 0h                       |

**Table 3-3461. CONTROLSS\_OUTPUTXBAR\_FLAG\_CLR Register Field Descriptions**

| Bit   | Field                     | Type | Reset | Description            |
|-------|---------------------------|------|-------|------------------------|
| 31:16 | RESERVED                  | NONE | 0h    | Reserved               |
| 15    | OUTPUTXBAR_FLAG_CLR_BIT15 | R/W  | 0h    | Output XBAR flag clear |
| 14    | OUTPUTXBAR_FLAG_CLR_BIT14 | R/W  | 0h    | Output XBAR flag clear |
| 13    | OUTPUTXBAR_FLAG_CLR_BIT13 | R/W  | 0h    | Output XBAR flag clear |
| 12    | OUTPUTXBAR_FLAG_CLR_BIT12 | R/W  | 0h    | Output XBAR flag clear |
| 11    | OUTPUTXBAR_FLAG_CLR_BIT11 | R/W  | 0h    | Output XBAR flag clear |
| 10    | OUTPUTXBAR_FLAG_CLR_BIT10 | R/W  | 0h    | Output XBAR flag clear |
| 9     | OUTPUTXBAR_FLAG_CLR_BIT9  | R/W  | 0h    | Output XBAR flag clear |
| 8     | OUTPUTXBAR_FLAG_CLR_BIT8  | R/W  | 0h    | Output XBAR flag clear |

**Table 3-3461. CONTROLSS\_OUTPUTXBAR\_FLAG\_CLR Register Field Descriptions (continued)**

| Bit | Field                    | Type | Reset | Description            |
|-----|--------------------------|------|-------|------------------------|
| 7   | OUTPUTXBAR_FLAG_CLR_BIT7 | R/W  | 0h    | Output XBAR flag clear |
| 6   | OUTPUTXBAR_FLAG_CLR_BIT6 | R/W  | 0h    | Output XBAR flag clear |
| 5   | OUTPUTXBAR_FLAG_CLR_BIT5 | R/W  | 0h    | Output XBAR flag clear |
| 4   | OUTPUTXBAR_FLAG_CLR_BIT4 | R/W  | 0h    | Output XBAR flag clear |
| 3   | OUTPUTXBAR_FLAG_CLR_BIT3 | R/W  | 0h    | Output XBAR flag clear |
| 2   | OUTPUTXBAR_FLAG_CLR_BIT2 | R/W  | 0h    | Output XBAR flag clear |
| 1   | OUTPUTXBAR_FLAG_CLR_BIT1 | R/W  | 0h    | Output XBAR flag clear |
| 0   | OUTPUTXBAR_FLAG_CLR_BIT0 | R/W  | 0h    | Output XBAR flag clear |

### 3.18.2.5 CONTROLSS\_OUTPUTXBAR\_FLAGFORCE Register

#### 1 CONTROLSS\_OUTPUTXBAR\_FLAGFORCE Register (Offset = 20h) [reset = 0h]

Output Signal Latched Flag Force.

Return to [Summary Table](#)

**Table 3-3462. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8020h       |

**Figure 3-1130. CONTROLSS\_OUTPUTXBAR\_FLAGFORCE Name Register**

|                          |    |    |    |    |    |    |    |
|--------------------------|----|----|----|----|----|----|----|
| 31                       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                 |    |    |    |    |    |    |    |
| NONE                     |    |    |    |    |    |    |    |
| 0h                       |    |    |    |    |    |    |    |
| 23                       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                 |    |    |    |    |    |    |    |
| NONE                     |    |    |    |    |    |    |    |
| 0h                       |    |    |    |    |    |    |    |
| 15                       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR_FLAGFORCE_FRC |    |    |    |    |    |    |    |
| R/W                      |    |    |    |    |    |    |    |
| 0h                       |    |    |    |    |    |    |    |
| 7                        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR_FLAGFORCE_FRC |    |    |    |    |    |    |    |
| R/W                      |    |    |    |    |    |    |    |
| 0h                       |    |    |    |    |    |    |    |

**Table 3-3464. CONTROLSS\_OUTPUTXBAR\_FLAGFORCE Register Field Descriptions**

| Bit   | Field                    | Type | Reset | Description |
|-------|--------------------------|------|-------|-------------|
| 31:16 | RESERVED                 | NONE | 0h    | Reserved    |
| 15:0  | OUTPUTXBAR_FLAGFORCE_FRC | R/W  | 0h    | FlagForce   |

### 3.18.2.6 CONTROLSS\_OUTPUTXBAR\_OUTLATCH Register

#### 1 CONTROLSS\_OUTPUTXBAR\_OUTLATCH Register (Offset = 24h) [reset = 0h]

Output Signal Select Latch.

Return to [Summary Table](#)

**Table 3-3465. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8024h       |

**Figure 3-1131. CONTROLSS\_OUTPUTXBAR\_OUTLATCH Name Register**

|                              |    |    |    |    |    |    |    |
|------------------------------|----|----|----|----|----|----|----|
| 31                           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                     |    |    |    |    |    |    |    |
| NONE                         |    |    |    |    |    |    |    |
| 0h                           |    |    |    |    |    |    |    |
| 23                           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                     |    |    |    |    |    |    |    |
| NONE                         |    |    |    |    |    |    |    |
| 0h                           |    |    |    |    |    |    |    |
| 15                           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR_OUTLATCH_LATCHSEL |    |    |    |    |    |    |    |
| R/W                          |    |    |    |    |    |    |    |
| 0h                           |    |    |    |    |    |    |    |
| 7                            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR_OUTLATCH_LATCHSEL |    |    |    |    |    |    |    |
| R/W                          |    |    |    |    |    |    |    |
| 0h                           |    |    |    |    |    |    |    |

**Table 3-3467. CONTROLSS\_OUTPUTXBAR\_OUTLATCH Register Field Descriptions**

| Bit   | Field                        | Type | Reset | Description |
|-------|------------------------------|------|-------|-------------|
| 31:16 | RESERVED                     | NONE | 0h    | Reserved    |
| 15:0  | OUTPUTXBAR_OUTLATCH_LATCHSEL | R/W  | 0h    | OutLatch    |



### 3.18.2.7 CONTROLSS\_OUTPUTXBAR\_OUTSTRETCH Register

#### 1 CONTROLSS\_OUTPUTXBAR\_OUTSTRETCH Register (Offset = 28h) [reset = 0h]

Output Signal Stretched Pulse Version Select.

Return to [Summary Table](#)

**Table 3-3468. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8028h       |

**Figure 3-1132. CONTROLSS\_OUTPUTXBAR\_OUTSTRETCH Name Register**

|                                  |    |    |    |    |    |    |    |
|----------------------------------|----|----|----|----|----|----|----|
| 31                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                         |    |    |    |    |    |    |    |
| NONE                             |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 23                               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                         |    |    |    |    |    |    |    |
| NONE                             |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 15                               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR_OUTSTRETCH_STRETCHSEL |    |    |    |    |    |    |    |
| R/W                              |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |
| 7                                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR_OUTSTRETCH_STRETCHSEL |    |    |    |    |    |    |    |
| R/W                              |    |    |    |    |    |    |    |
| 0h                               |    |    |    |    |    |    |    |

**Table 3-3470. CONTROLSS\_OUTPUTXBAR\_OUTSTRETCH Register Field Descriptions**

| Bit   | Field                            | Type | Reset | Description |
|-------|----------------------------------|------|-------|-------------|
| 31:16 | RESERVED                         | NONE | 0h    | Reserved    |
| 15:0  | OUTPUTXBAR_OUTSTRETCH_STRETCHSEL | R/W  | 0h    | OutStretch  |

### 3.18.2.8 CONTROLSS\_OUTPUTXBAR\_OUTLENGTH Register

#### 1 CONTROLSS\_OUTPUTXBAR\_OUTLENGTH Register (Offset = 2Ch) [reset = 0h]

Output Signal Stretched Pulse Length Select.

Return to [Summary Table](#)

**Table 3-3471. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 802Ch       |

**Figure 3-1133. CONTROLSS\_OUTPUTXBAR\_OUTLENGTH Name Register**

|                                |    |    |    |    |    |    |    |
|--------------------------------|----|----|----|----|----|----|----|
| 31                             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                       |    |    |    |    |    |    |    |
| NONE                           |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |
| 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                       |    |    |    |    |    |    |    |
| NONE                           |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |
| 15                             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR_OUTLENGTH_LENGTHSEL |    |    |    |    |    |    |    |
| R/W                            |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |
| 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR_OUTLENGTH_LENGTHSEL |    |    |    |    |    |    |    |
| R/W                            |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |

**Table 3-3473. CONTROLSS\_OUTPUTXBAR\_OUTLENGTH Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description |
|-------|--------------------------------|------|-------|-------------|
| 31:16 | RESERVED                       | NONE | 0h    | Reserved    |
| 15:0  | OUTPUTXBAR_OUTLENGTH_LENGTHSEL | R/W  | 0h    | OutLength   |

### 3.18.2.9 CONTROLSS\_OUTPUTXBAR\_OUTINVERT Register

#### 1 CONTROLSS\_OUTPUTXBAR\_OUTINVERT Register (Offset = 30h) [reset = 0h]

Output Signal Invert Select.

Return to [Summary Table](#)

**Table 3-3474. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8030h       |

**Figure 3-1134. CONTROLSS\_OUTPUTXBAR\_OUTINVERT Name Register**

|                                |    |    |    |    |    |    |    |
|--------------------------------|----|----|----|----|----|----|----|
| 31                             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED                       |    |    |    |    |    |    |    |
| NONE                           |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |
| 23                             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED                       |    |    |    |    |    |    |    |
| NONE                           |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |
| 15                             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR_OUTINVERT_OUTINVERT |    |    |    |    |    |    |    |
| R/W                            |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |
| 7                              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR_OUTINVERT_OUTINVERT |    |    |    |    |    |    |    |
| R/W                            |    |    |    |    |    |    |    |
| 0h                             |    |    |    |    |    |    |    |

**Table 3-3476. CONTROLSS\_OUTPUTXBAR\_OUTINVERT Register Field Descriptions**

| Bit   | Field                          | Type | Reset | Description |
|-------|--------------------------------|------|-------|-------------|
| 31:16 | RESERVED                       | NONE | 0h    | Reserved    |
| 15:0  | OUTPUTXBAR_OUTINVERT_OUTINVERT | R/W  | 0h    | OutInvert   |

### 3.18.2.10 CONTROLSS\_OUTPUTXBAR0\_G0 Register

#### 1 CONTROLSS\_OUTPUTXBAR0\_G0 Register (Offset = 100h) [reset = 0h]

OUTPUT XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-3477. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8100h       |

**Figure 3-1135. CONTROLSS\_OUTPUTXBAR0\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR0_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR0_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR0_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR0_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3479. CONTROLSS\_OUTPUTXBAR0\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                       |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR0_G0_SEL | R/W  | 0h    | G0: PWM XBAR0 G0 input bit select. Input source is PWM[x].TRIPOUT<br>1:PWM[x] TRIPOUT selected<br>0:PWM[x] TRIPOUT is de-selected |

### 3.18.2.11 CONTROLSS\_OUTPUTXBAR0\_G1 Register

#### 1 CONTROLSS\_OUTPUTXBAR0\_G1 Register (Offset = 104h) [reset = 0h]

OUTPUT XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-3480. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8104h       |

**Figure 3-1136. CONTROLSS\_OUTPUTXBAR0\_G1 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR0_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR0_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR0_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR0_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3482. CONTROLSS\_OUTPUTXBAR0\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR0_G1_SEL | R/W  | 0h    | G1: OUTPUT XBAR0 G1 input bit select. Input source is PWM[x].SOCA<br>1:PWM[x] SOCA selected<br>0:PWM[x] SOCA is de-selected |

### 3.18.2.12 CONTROLSS\_OUTPUTXBAR0\_G2 Register

#### 1 CONTROLSS\_OUTPUTXBAR0\_G2 Register (Offset = 108h) [reset = 0h]

OUTPUT XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-3483. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8108h       |

**Figure 3-1137. CONTROLSS\_OUTPUTXBAR0\_G2 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR0_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR0_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR0_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR0_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3485. CONTROLSS\_OUTPUTXBAR0\_G2 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR0_G2_SEL | R/W  | 0h    | G2: OUTPUT XBAR0 G2 input bit select. Input source is PWM[x].SOCB<br>1:PWM[x] SOCB selected<br>0:PWM[x] SOCB is de-selected |

### 3.18.2.13 CONTROLSS\_OUTPUTXBAR0\_G3 Register

#### 1 CONTROLSS\_OUTPUTXBAR0\_G3 Register (Offset = 10Ch) [reset = 0h]

OUTPUT XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-3486. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 810Ch       |

**Figure 3-1138. CONTROLSS\_OUTPUTXBAR0\_G3 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR0_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR0_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR0_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR0_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3488. CONTROLSS\_OUTPUTXBAR0\_G3 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                       |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR0_G3_SEL | R/W  | 0h    | G3: OUTPUT XBAR0 G3 input bit select. Input source is DEL[x].ACTIVE<br>1:DEL[x] ACTIVE selected<br>0:DEL[x] ACTIVE is de-selected |

### 3.18.2.14 CONTROLSS\_OUTPUTXBAR0\_G4 Register

#### 1 CONTROLSS\_OUTPUTXBAR0\_G4 Register (Offset = 110h) [reset = 0h]

OUTPUT XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-3489. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8110h       |

**Figure 3-1139. CONTROLSS\_OUTPUTXBAR0\_G4 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR0_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR0_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR0_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR0_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3491. CONTROLSS\_OUTPUTXBAR0\_G4 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR0_G4_SEL | R/W  | 0h    | G4: OUTPUT XBAR0 G4 input bit select. Input source is DEL[x].TRIP<br>1:DEL[x] TRIP selected<br>0:DEL[x] TRIP is de-selected |



### 3.18.2.15 CONTROLSS\_OUTPUTXBAR0\_G5 Register

#### 1 CONTROLSS\_OUTPUTXBAR0\_G5 Register (Offset = 114h) [reset = 0h]

OUTPUT XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-3492. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8114h       |

**Figure 3-1140. CONTROLSS\_OUTPUTXBAR0\_G5 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR0_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR0_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR0_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3494. CONTROLSS\_OUTPUTXBAR0\_G5 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3494. CONTROLSS\_OUTPUTXBAR0\_G5 Register Field Descriptions (continued)**

| Bit  | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------|--------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | OUTPUTXBAR0_G5_SEL | R/W  | 0h    | G5: OUTPUT XBAR0 G5 input bit select.<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.18.2.16 CONTROLSS\_OUTPUTXBAR0\_G6 Register

#### 1 CONTROLSS\_OUTPUTXBAR0\_G6 Register (Offset = 118h) [reset = 0h]

OUTPUT XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-3495. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8118h       |

**Figure 3-1141. CONTROLSS\_OUTPUTXBAR0\_G6 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR0_G6_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR0_G6_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR0_G6_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3497. CONTROLSS\_OUTPUTXBAR0\_G6 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 19:0  | OUTPUTXBAR0_G6_SEL | R/W  | 0h    | G6: OUTPUT XBAR0 G6 Input Select<br>0: CMPSSA0.CTRIPOUTL<br>1: CMPSSA0.CTRIPOUTH<br>2: CMPSSA1.CTRIPOUTL<br>3: CMPSSA1.CTRIPOUTH<br>4: CMPSSA2.CTRIPOUTL<br>5: CMPSSA2.CTRIPOUTH<br>6: CMPSSA3.CTRIPOUTL<br>7: CMPSSA3.CTRIPOUTH<br>8: CMPSSA4.CTRIPOUTL<br>9: CMPSSA4.CTRIPOUTH<br>10: CMPSSA5.CTRIPOUTL<br>11: CMPSSA5.CTRIPOUTH<br>12: CMPSSA6.CTRIPOUTL<br>13: CMPSSA6.CTRIPOUTH<br>14: CMPSSA7.CTRIPOUTL<br>15: CMPSSA7.CTRIPOUTH<br>16: CMPSSA8.CTRIPOUTL<br>17: CMPSSA8.CTRIPOUTH<br>18: CMPSSA9.CTRIPOUTL<br>19: CMPSSA9.CTRIPOUTH |

### 3.18.2.17 CONTROLSS\_OUTPUTXBAR0\_G7 Register

#### 1 CONTROLSS\_OUTPUTXBAR0\_G7 Register (Offset = 11Ch) [reset = 0h]

OUTPUT XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-3498. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 811Ch       |

**Figure 3-1142. CONTROLSS\_OUTPUTXBAR0\_G7 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR0_G7_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR0_G7_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR0_G7_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3500. CONTROLSS\_OUTPUTXBAR0\_G7 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 19:0  | OUTPUTXBAR0_G7_SEL | R/W  | 0h    | G7: OUTPUT XBAR0 G7 Input Select<br>0: CMPSSB0.CTRIPOUTL<br>1: CMPSSB0.CTRIPOUTH<br>2: CMPSSB1.CTRIPOUTL<br>3: CMPSSB1.CTRIPOUTH<br>4: CMPSSB2.CTRIPOUTL<br>5: CMPSSB2.CTRIPOUTH<br>6: CMPSSB3.CTRIPOUTL<br>7: CMPSSB3.CTRIPOUTH<br>8: CMPSSB4.CTRIPOUTL<br>9: CMPSSB4.CTRIPOUTH<br>10: CMPSSB5.CTRIPOUTL<br>11: CMPSSB5.CTRIPOUTH<br>12: CMPSSB6.CTRIPOUTL<br>13: CMPSSB6.CTRIPOUTH<br>14: CMPSSB7.CTRIPOUTL<br>15: CMPSSB7.CTRIPOUTH<br>16: CMPSSB8.CTRIPOUTL<br>17: CMPSSB8.CTRIPOUTH<br>18: CMPSSB9.CTRIPOUTL<br>19: CMPSSB9.CTRIPOUTH |

### 3.18.2.18 CONTROLSS\_OUTPUTXBAR0\_G8 Register

#### 1 CONTROLSS\_OUTPUTXBAR0\_G8 Register (Offset = 120h) [reset = 0h]

OUTPUT XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-3501. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8120h       |

**Figure 3-1143. CONTROLSS\_OUTPUTXBAR0\_G8 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR0_G8_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR0_G8_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR0_G8_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3503. CONTROLSS\_OUTPUTXBAR0\_G8 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                            |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                               |
| 19:0  | OUTPUTXBAR0_G8_SEL | R/W  | 0h    | G8: OUTPUT XBAR0 G8 Input Select<br>0:ADC0.EVT1<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.18.2.19 CONTROLSS\_OUTPUTXBAR0\_G9 Register

#### 1 CONTROLSS\_OUTPUTXBAR0\_G9 Register (Offset = 124h) [reset = 0h]

OUTPUT XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-3504. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8124h       |

**Figure 3-1144. CONTROLSS\_OUTPUTXBAR0\_G9 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR0_G9_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR0_G9_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR0_G9_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3506. CONTROLSS\_OUTPUTXBAR0\_G9 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                               |
| 19:0  | OUTPUTXBAR0_G9_SEL | R/W  | 0h    | G9: OUTPUT XBAR0 G9 Input Select<br>0:PWMSyncOutXBAR.SYNCOU0<br>1:PWMSyncOutXBAR.SYNCOU1<br>2:PWMSyncOutXBAR.SYNCOU2<br>3:PWMSyncOutXBAR.SYNCOU3<br>4:EQEP0.I_OUT<br>5:EQEP0.S_OUT<br>6:EQEP1.I_OUT<br>7:EQEP1.S_OUT<br>8:EQEP2.I_OUT<br>9:EQEP2.S_OUT<br>10:ECAP0.OUT<br>11:ECAP1.OUT<br>12:ECAP2.OUT<br>13:ECAP3.OUT<br>14:ECAP4.OUT<br>15:ECAP5.OUT<br>16:ECAP6.OUT<br>17:ECAP7.OUT<br>18:ECAP8.OUT<br>19:ECAP9.OUT |

### 3.18.2.20 CONTROLSS\_OUTPUTXBAR0\_G10 Register

#### 1 CONTROLSS\_OUTPUTXBAR0\_G10 Register (Offset = 128h) [reset = 0h]

OUTPUT XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-3507. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8128h       |

**Figure 3-1145. CONTROLSS\_OUTPUTXBAR0\_G10 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR0_G10_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR0_G10_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3509. CONTROLSS\_OUTPUTXBAR0\_G10 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                   |
|-------|---------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                      |
| 15:0  | OUTPUTXBAR0_G10_SEL | R/W  | 0h    | G10: OUTPUT XBAR0 G10 Input Select<br>3<br>0:FSIRX0.RX_TRIG0<br>7<br>4:FSIRX1.RX_TRIG0<br>11<br>8:FSIRX2.RX_TRIG0<br>15<br>12:FSIRX3.RX_TRIG0 |

### 3.18.2.21 CONTROLSS\_OUTPUTXBAR1\_G0 Register

#### 1 CONTROLSS\_OUTPUTXBAR1\_G0 Register (Offset = 140h) [reset = 0h]

OUTPUT XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-3510. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8140h       |

**Figure 3-1146. CONTROLSS\_OUTPUTXBAR1\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR1_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR1_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR1_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR1_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3512. CONTROLSS\_OUTPUTXBAR1\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                       |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR1_G0_SEL | R/W  | 0h    | G0: PWM XBAR1 G0 input bit select. Input source is PWM[x].TRIPOUT<br>1:PWM[x] TRIPOUT selected<br>0:PWM[x] TRIPOUT is de-selected |



### 3.18.2.22 CONTROLSS\_OUTPUTXBAR1\_G1 Register

#### 1 CONTROLSS\_OUTPUTXBAR1\_G1 Register (Offset = 144h) [reset = 0h]

OUTPUT XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-3513. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8144h       |

**Figure 3-1147. CONTROLSS\_OUTPUTXBAR1\_G1 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR1_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR1_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR1_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR1_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3515. CONTROLSS\_OUTPUTXBAR1\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR1_G1_SEL | R/W  | 0h    | G1: OUTPUT XBAR1 G1 input bit select. Input source is PWM[x].SOCA<br>1:PWM[x] SOCA selected<br>0:PWM[x] SOCA is de-selected |

### 3.18.2.23 CONTROLSS\_OUTPUTXBAR1\_G2 Register

#### 1 CONTROLSS\_OUTPUTXBAR1\_G2 Register (Offset = 148h) [reset = 0h]

OUTPUT XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-3516. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8148h       |

**Figure 3-1148. CONTROLSS\_OUTPUTXBAR1\_G2 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR1_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR1_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR1_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR1_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3518. CONTROLSS\_OUTPUTXBAR1\_G2 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR1_G2_SEL | R/W  | 0h    | G2: OUTPUT XBAR1 G2 input bit select. Input source is PWM[x].SOCB<br>1:PWM[x] SOCB selected<br>0:PWM[x] SOCB is de-selected |

### 3.18.2.24 CONTROLSS\_OUTPUTXBAR1\_G3 Register

#### 1 CONTROLSS\_OUTPUTXBAR1\_G3 Register (Offset = 14Ch) [reset = 0h]

OUTPUT XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-3519. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 814Ch       |

**Figure 3-1149. CONTROLSS\_OUTPUTXBAR1\_G3 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR1_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR1_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR1_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR1_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3521. CONTROLSS\_OUTPUTXBAR1\_G3 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                       |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR1_G3_SEL | R/W  | 0h    | G3: OUTPUT XBAR1 G3 input bit select. Input source is DEL[x].ACTIVE<br>1:DEL[x] ACTIVE selected<br>0:DEL[x] ACTIVE is de-selected |

### 3.18.2.25 CONTROLSS\_OUTPUTXBAR1\_G4 Register

#### 1 CONTROLSS\_OUTPUTXBAR1\_G4 Register (Offset = 150h) [reset = 0h]

OUTPUT XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-3522. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8150h       |

**Figure 3-1150. CONTROLSS\_OUTPUTXBAR1\_G4 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR1_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR1_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR1_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR1_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3524. CONTROLSS\_OUTPUTXBAR1\_G4 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR1_G4_SEL | R/W  | 0h    | G4: OUTPUT XBAR1 G4 input bit select. Input source is DEL[x].TRIP<br>1:DEL[x] TRIP selected<br>0:DEL[x] TRIP is de-selected |

### 3.18.2.26 CONTROLSS\_OUTPUTXBAR1\_G5 Register

#### 1 CONTROLSS\_OUTPUTXBAR1\_G5 Register (Offset = 154h) [reset = 0h]

OUTPUT XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-3525. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8154h       |

**Figure 3-1151. CONTROLSS\_OUTPUTXBAR1\_G5 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR1_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR1_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR1_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3527. CONTROLSS\_OUTPUTXBAR1\_G5 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3527. CONTROLSS\_OUTPUTXBAR1\_G5 Register Field Descriptions (continued)**

| Bit  | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------|--------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | OUTPUTXBAR1_G5_SEL | R/W  | 0h    | G5: OUTPUT XBAR1 G5 input bit select.<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.18.2.27 CONTROLSS\_OUTPUTXBAR1\_G6 Register

#### 1 CONTROLSS\_OUTPUTXBAR1\_G6 Register (Offset = 158h) [reset = 0h]

OUTPUT XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-3528. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8158h       |

**Figure 3-1152. CONTROLSS\_OUTPUTXBAR1\_G6 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR1_G6_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR1_G6_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR1_G6_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3530. CONTROLSS\_OUTPUTXBAR1\_G6 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 19:0  | OUTPUTXBAR1_G6_SEL | R/W  | 0h    | G6: OUTPUT XBAR1 G6 Input Select<br>0: CMPSSA0.CTRIPOUTL<br>1: CMPSSA0.CTRIPOUTH<br>2: CMPSSA1.CTRIPOUTL<br>3: CMPSSA1.CTRIPOUTH<br>4: CMPSSA2.CTRIPOUTL<br>5: CMPSSA2.CTRIPOUTH<br>6: CMPSSA3.CTRIPOUTL<br>7: CMPSSA3.CTRIPOUTH<br>8: CMPSSA4.CTRIPOUTL<br>9: CMPSSA4.CTRIPOUTH<br>10: CMPSSA5.CTRIPOUTL<br>11: CMPSSA5.CTRIPOUTH<br>12: CMPSSA6.CTRIPOUTL<br>13: CMPSSA6.CTRIPOUTH<br>14: CMPSSA7.CTRIPOUTL<br>15: CMPSSA7.CTRIPOUTH<br>16: CMPSSA8.CTRIPOUTL<br>17: CMPSSA8.CTRIPOUTH<br>18: CMPSSA9.CTRIPOUTL<br>19: CMPSSA9.CTRIPOUTH |

### 3.18.2.28 CONTROLSS\_OUTPUTXBAR1\_G7 Register

#### 1 CONTROLSS\_OUTPUTXBAR1\_G7 Register (Offset = 15Ch) [reset = 0h]

OUTPUT XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-3531. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 815Ch       |

**Figure 3-1153. CONTROLSS\_OUTPUTXBAR1\_G7 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR1_G7_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR1_G7_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR1_G7_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3533. CONTROLSS\_OUTPUTXBAR1\_G7 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 19:0  | OUTPUTXBAR1_G7_SEL | R/W  | 0h    | G7: OUTPUT XBAR1 G7 Input Select<br>0: CMPSSB0.CTRIPOUTL<br>1: CMPSSB0.CTRIPOUTH<br>2: CMPSSB1.CTRIPOUTL<br>3: CMPSSB1.CTRIPOUTH<br>4: CMPSSB2.CTRIPOUTL<br>5: CMPSSB2.CTRIPOUTH<br>6: CMPSSB3.CTRIPOUTL<br>7: CMPSSB3.CTRIPOUTH<br>8: CMPSSB4.CTRIPOUTL<br>9: CMPSSB4.CTRIPOUTH<br>10: CMPSSB5.CTRIPOUTL<br>11: CMPSSB5.CTRIPOUTH<br>12: CMPSSB6.CTRIPOUTL<br>13: CMPSSB6.CTRIPOUTH<br>14: CMPSSB7.CTRIPOUTL<br>15: CMPSSB7.CTRIPOUTH<br>16: CMPSSB8.CTRIPOUTL<br>17: CMPSSB8.CTRIPOUTH<br>18: CMPSSB9.CTRIPOUTL<br>19: CMPSSB9.CTRIPOUTH |



### 3.18.2.29 CONTROLSS\_OUTPUTXBAR1\_G8 Register

#### 1 CONTROLSS\_OUTPUTXBAR1\_G8 Register (Offset = 160h) [reset = 0h]

OUTPUT XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-3534. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8160h       |

**Figure 3-1154. CONTROLSS\_OUTPUTXBAR1\_G8 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR1_G8_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR1_G8_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR1_G8_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3536. CONTROLSS\_OUTPUTXBAR1\_G8 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                            |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                               |
| 19:0  | OUTPUTXBAR1_G8_SEL | R/W  | 0h    | G8: OUTPUT XBAR1 G8 Input Select<br>0:ADC0.EVT1<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.18.2.30 CONTROLSS\_OUTPUTXBAR1\_G9 Register

#### 1 CONTROLSS\_OUTPUTXBAR1\_G9 Register (Offset = 164h) [reset = 0h]

OUTPUT XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-3537. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8164h       |

**Figure 3-1155. CONTROLSS\_OUTPUTXBAR1\_G9 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR1_G9_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR1_G9_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR1_G9_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3539. CONTROLSS\_OUTPUTXBAR1\_G9 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                               |
| 19:0  | OUTPUTXBAR1_G9_SEL | R/W  | 0h    | G9: OUTPUT XBAR1 G9 Input Select<br>0:PWMSyncOutXBAR.SYNCOU0<br>1:PWMSyncOutXBAR.SYNCOU1<br>2:PWMSyncOutXBAR.SYNCOU2<br>3:PWMSyncOutXBAR.SYNCOU3<br>4:EQEP0.I_OUT<br>5:EQEP0.S_OUT<br>6:EQEP1.I_OUT<br>7:EQEP1.S_OUT<br>8:EQEP2.I_OUT<br>9:EQEP2.S_OUT<br>10:ECAP0.OUT<br>11:ECAP1.OUT<br>12:ECAP2.OUT<br>13:ECAP3.OUT<br>14:ECAP4.OUT<br>15:ECAP5.OUT<br>16:ECAP6.OUT<br>17:ECAP7.OUT<br>18:ECAP8.OUT<br>19:ECAP9.OUT |

### 3.18.2.31 CONTROLSS\_OUTPUTXBAR1\_G10 Register

#### 1 CONTROLSS\_OUTPUTXBAR1\_G10 Register (Offset = 168h) [reset = 0h]

OUTPUT XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-3540. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8168h       |

**Figure 3-1156. CONTROLSS\_OUTPUTXBAR1\_G10 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR1_G10_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR1_G10_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3542. CONTROLSS\_OUTPUTXBAR1\_G10 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                   |
|-------|---------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                      |
| 15:0  | OUTPUTXBAR1_G10_SEL | R/W  | 0h    | G10: OUTPUT XBAR1 G10 Input Select<br>3<br>0:FSIRX0.RX_TRIG0<br>7<br>4:FSIRX1.RX_TRIG0<br>11<br>8:FSIRX2.RX_TRIG0<br>15<br>12:FSIRX3.RX_TRIG0 |

### 3.18.2.32 CONTROLSS\_OUTPUTXBAR2\_G0 Register

#### 1 CONTROLSS\_OUTPUTXBAR2\_G0 Register (Offset = 180h) [reset = 0h]

OUTPUT XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-3543. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8180h       |

**Figure 3-1157. CONTROLSS\_OUTPUTXBAR2\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR2_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR2_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR2_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR2_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3545. CONTROLSS\_OUTPUTXBAR2\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                       |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR2_G0_SEL | R/W  | 0h    | G0: PWM XBAR2 G0 input bit select. Input source is PWM[x].TRIPOUT<br>1:PWM[x] TRIPOUT selected<br>0:PWM[x] TRIPOUT is de-selected |

### 3.18.2.33 CONTROLSS\_OUTPUTXBAR2\_G1 Register

#### 1 CONTROLSS\_OUTPUTXBAR2\_G1 Register (Offset = 184h) [reset = 0h]

OUTPUT XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-3546. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8184h       |

**Figure 3-1158. CONTROLSS\_OUTPUTXBAR2\_G1 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR2_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR2_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR2_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR2_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3548. CONTROLSS\_OUTPUTXBAR2\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR2_G1_SEL | R/W  | 0h    | G1: OUTPUT XBAR2 G1 input bit select. Input source is PWM[x].SOCA<br>1:PWM[x] SOCA selected<br>0:PWM[x] SOCA is de-selected |

### 3.18.2.34 CONTROLSS\_OUTPUTXBAR2\_G2 Register

#### 1 CONTROLSS\_OUTPUTXBAR2\_G2 Register (Offset = 188h) [reset = 0h]

OUTPUT XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-3549. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8188h       |

**Figure 3-1159. CONTROLSS\_OUTPUTXBAR2\_G2 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR2_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR2_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR2_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR2_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3551. CONTROLSS\_OUTPUTXBAR2\_G2 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR2_G2_SEL | R/W  | 0h    | G2: OUTPUT XBAR2 G2 input bit select. Input source is PWM[x].SOCB<br>1:PWM[x] SOCB selected<br>0:PWM[x] SOCB is de-selected |

### 3.18.2.35 CONTROLSS\_OUTPUTXBAR2\_G3 Register

#### 1 CONTROLSS\_OUTPUTXBAR2\_G3 Register (Offset = 18Ch) [reset = 0h]

OUTPUT XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-3552. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 818Ch       |

**Figure 3-1160. CONTROLSS\_OUTPUTXBAR2\_G3 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR2_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR2_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR2_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR2_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3554. CONTROLSS\_OUTPUTXBAR2\_G3 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                       |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR2_G3_SEL | R/W  | 0h    | G3: OUTPUT XBAR2 G3 input bit select. Input source is DEL[x].ACTIVE<br>1:DEL[x] ACTIVE selected<br>0:DEL[x] ACTIVE is de-selected |

### 3.18.2.36 CONTROLSS\_OUTPUTXBAR2\_G4 Register

#### 1 CONTROLSS\_OUTPUTXBAR2\_G4 Register (Offset = 190h) [reset = 0h]

OUTPUT XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-3555. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8190h       |

**Figure 3-1161. CONTROLSS\_OUTPUTXBAR2\_G4 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR2_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR2_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR2_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR2_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3557. CONTROLSS\_OUTPUTXBAR2\_G4 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR2_G4_SEL | R/W  | 0h    | G4: OUTPUT XBAR2 G4 input bit select. Input source is DEL[x].TRIP<br>1:DEL[x] TRIP selected<br>0:DEL[x] TRIP is de-selected |



### 3.18.2.37 CONTROLSS\_OUTPUTXBAR2\_G5 Register

#### 1 CONTROLSS\_OUTPUTXBAR2\_G5 Register (Offset = 194h) [reset = 0h]

OUTPUT XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-3558. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8194h       |

**Figure 3-1162. CONTROLSS\_OUTPUTXBAR2\_G5 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR2_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR2_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR2_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3560. CONTROLSS\_OUTPUTXBAR2\_G5 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3560. CONTROLSS\_OUTPUTXBAR2\_G5 Register Field Descriptions (continued)**

| Bit  | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------|--------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | OUTPUTXBAR2_G5_SEL | R/W  | 0h    | G5: OUTPUT XBAR2 G5 input bit select.<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.18.2.38 CONTROLSS\_OUTPUTXBAR2\_G6 Register

#### 1 CONTROLSS\_OUTPUTXBAR2\_G6 Register (Offset = 198h) [reset = 0h]

OUTPUT XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-3561. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8198h       |

**Figure 3-1163. CONTROLSS\_OUTPUTXBAR2\_G6 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR2_G6_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR2_G6_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR2_G6_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3563. CONTROLSS\_OUTPUTXBAR2\_G6 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 19:0  | OUTPUTXBAR2_G6_SEL | R/W  | 0h    | G6: OUTPUT XBAR2 G6 Input Select<br>0: CMPSSA0.CTRIPOUTL<br>1: CMPSSA0.CTRIPOUTH<br>2: CMPSSA1.CTRIPOUTL<br>3: CMPSSA1.CTRIPOUTH<br>4: CMPSSA2.CTRIPOUTL<br>5: CMPSSA2.CTRIPOUTH<br>6: CMPSSA3.CTRIPOUTL<br>7: CMPSSA3.CTRIPOUTH<br>8: CMPSSA4.CTRIPOUTL<br>9: CMPSSA4.CTRIPOUTH<br>10: CMPSSA5.CTRIPOUTL<br>11: CMPSSA5.CTRIPOUTH<br>12: CMPSSA6.CTRIPOUTL<br>13: CMPSSA6.CTRIPOUTH<br>14: CMPSSA7.CTRIPOUTL<br>15: CMPSSA7.CTRIPOUTH<br>16: CMPSSA8.CTRIPOUTL<br>17: CMPSSA8.CTRIPOUTH<br>18: CMPSSA9.CTRIPOUTL<br>19: CMPSSA9.CTRIPOUTH |

### 3.18.2.39 CONTROLSS\_OUTPUTXBAR2\_G7 Register

#### 1 CONTROLSS\_OUTPUTXBAR2\_G7 Register (Offset = 19Ch) [reset = 0h]

OUTPUT XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-3564. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 819Ch       |

**Figure 3-1164. CONTROLSS\_OUTPUTXBAR2\_G7 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR2_G7_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR2_G7_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR2_G7_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3566. CONTROLSS\_OUTPUTXBAR2\_G7 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 19:0  | OUTPUTXBAR2_G7_SEL | R/W  | 0h    | G7: OUTPUT XBAR2 G7 Input Select<br>0: CMPSSB0.CTRIPOUTL<br>1: CMPSSB0.CTRIPOUTH<br>2: CMPSSB1.CTRIPOUTL<br>3: CMPSSB1.CTRIPOUTH<br>4: CMPSSB2.CTRIPOUTL<br>5: CMPSSB2.CTRIPOUTH<br>6: CMPSSB3.CTRIPOUTL<br>7: CMPSSB3.CTRIPOUTH<br>8: CMPSSB4.CTRIPOUTL<br>9: CMPSSB4.CTRIPOUTH<br>10: CMPSSB5.CTRIPOUTL<br>11: CMPSSB5.CTRIPOUTH<br>12: CMPSSB6.CTRIPOUTL<br>13: CMPSSB6.CTRIPOUTH<br>14: CMPSSB7.CTRIPOUTL<br>15: CMPSSB7.CTRIPOUTH<br>16: CMPSSB8.CTRIPOUTL<br>17: CMPSSB8.CTRIPOUTH<br>18: CMPSSB9.CTRIPOUTL<br>19: CMPSSB9.CTRIPOUTH |

### 3.18.2.40 CONTROLSS\_OUTPUTXBAR2\_G8 Register

#### 1 CONTROLSS\_OUTPUTXBAR2\_G8 Register (Offset = 1A0h) [reset = 0h]

OUTPUT XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-3567. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 81A0h       |

**Figure 3-1165. CONTROLSS\_OUTPUTXBAR2\_G8 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR2_G8_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR2_G8_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR2_G8_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3569. CONTROLSS\_OUTPUTXBAR2\_G8 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                            |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                               |
| 19:0  | OUTPUTXBAR2_G8_SEL | R/W  | 0h    | G8: OUTPUT XBAR2 G8 Input Select<br>0:ADC0.EVT1<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.18.2.41 CONTROLSS\_OUTPUTXBAR2\_G9 Register

#### 1 CONTROLSS\_OUTPUTXBAR2\_G9 Register (Offset = 1A4h) [reset = 0h]

OUTPUT XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-3570. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 81A4h       |

**Figure 3-1166. CONTROLSS\_OUTPUTXBAR2\_G9 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR2_G9_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR2_G9_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR2_G9_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3572. CONTROLSS\_OUTPUTXBAR2\_G9 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                               |
| 19:0  | OUTPUTXBAR2_G9_SEL | R/W  | 0h    | G9: OUTPUT XBAR2 G9 Input Select<br>0:PWMSyncOutXBAR.SYNCOU0<br>1:PWMSyncOutXBAR.SYNCOU1<br>2:PWMSyncOutXBAR.SYNCOU2<br>3:PWMSyncOutXBAR.SYNCOU3<br>4:EQEP0.I_OUT<br>5:EQEP0.S_OUT<br>6:EQEP1.I_OUT<br>7:EQEP1.S_OUT<br>8:EQEP2.I_OUT<br>9:EQEP2.S_OUT<br>10:ECAP0.OUT<br>11:ECAP1.OUT<br>12:ECAP2.OUT<br>13:ECAP3.OUT<br>14:ECAP4.OUT<br>15:ECAP5.OUT<br>16:ECAP6.OUT<br>17:ECAP7.OUT<br>18:ECAP8.OUT<br>19:ECAP9.OUT |

### 3.18.2.42 CONTROLSS\_OUTPUTXBAR2\_G10 Register

#### 1 CONTROLSS\_OUTPUTXBAR2\_G10 Register (Offset = 1A8h) [reset = 0h]

OUTPUT XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-3573. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 81A8h       |

**Figure 3-1167. CONTROLSS\_OUTPUTXBAR2\_G10 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR2_G10_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR2_G10_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3575. CONTROLSS\_OUTPUTXBAR2\_G10 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                   |
|-------|---------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                      |
| 15:0  | OUTPUTXBAR2_G10_SEL | R/W  | 0h    | G10: OUTPUT XBAR2 G10 Input Select<br>3<br>0:FSIRX0.RX_TRIG0<br>7<br>4:FSIRX1.RX_TRIG0<br>11<br>8:FSIRX2.RX_TRIG0<br>15<br>12:FSIRX3.RX_TRIG0 |

### 3.18.2.43 CONTROLSS\_OUTPUTXBAR3\_G0 Register

#### 1 CONTROLSS\_OUTPUTXBAR3\_G0 Register (Offset = 1C0h) [reset = 0h]

OUTPUT XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-3576. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 81C0h       |

**Figure 3-1168. CONTROLSS\_OUTPUTXBAR3\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR3_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR3_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR3_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR3_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3578. CONTROLSS\_OUTPUTXBAR3\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                       |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR3_G0_SEL | R/W  | 0h    | G0: PWM XBAR3 G0 input bit select. Input source is PWM[x].TRIPOUT<br>1:PWM[x] TRIPOUT selected<br>0:PWM[x] TRIPOUT is de-selected |



### 3.18.2.44 CONTROLSS\_OUTPUTXBAR3\_G1 Register

#### 1 CONTROLSS\_OUTPUTXBAR3\_G1 Register (Offset = 1C4h) [reset = 0h]

OUTPUT XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-3579. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 81C4h       |

**Figure 3-1169. CONTROLSS\_OUTPUTXBAR3\_G1 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR3_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR3_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR3_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR3_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3581. CONTROLSS\_OUTPUTXBAR3\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR3_G1_SEL | R/W  | 0h    | G1: OUTPUT XBAR3 G1 input bit select. Input source is PWM[x].SOCA<br>1:PWM[x] SOCA selected<br>0:PWM[x] SOCA is de-selected |

### 3.18.2.45 CONTROLSS\_OUTPUTXBAR3\_G2 Register

#### 1 CONTROLSS\_OUTPUTXBAR3\_G2 Register (Offset = 1C8h) [reset = 0h]

OUTPUT XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-3582. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 81C8h       |

**Figure 3-1170. CONTROLSS\_OUTPUTXBAR3\_G2 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR3_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR3_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR3_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR3_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3584. CONTROLSS\_OUTPUTXBAR3\_G2 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR3_G2_SEL | R/W  | 0h    | G2: OUTPUT XBAR3 G2 input bit select. Input source is PWM[x].SOCB<br>1:PWM[x] SOCB selected<br>0:PWM[x] SOCB is de-selected |

### 3.18.2.46 CONTROLSS\_OUTPUTXBAR3\_G3 Register

#### 1 CONTROLSS\_OUTPUTXBAR3\_G3 Register (Offset = 1CCh) [reset = 0h]

OUTPUT XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-3585. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 81CCh       |

**Figure 3-1171. CONTROLSS\_OUTPUTXBAR3\_G3 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR3_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR3_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR3_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR3_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3587. CONTROLSS\_OUTPUTXBAR3\_G3 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                       |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR3_G3_SEL | R/W  | 0h    | G3: OUTPUT XBAR3 G3 input bit select. Input source is DEL[x].ACTIVE<br>1:DEL[x] ACTIVE selected<br>0:DEL[x] ACTIVE is de-selected |

### 3.18.2.47 CONTROLSS\_OUTPUTXBAR3\_G4 Register

#### 1 CONTROLSS\_OUTPUTXBAR3\_G4 Register (Offset = 1D0h) [reset = 0h]

OUTPUT XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-3588. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 81D0h       |

**Figure 3-1172. CONTROLSS\_OUTPUTXBAR3\_G4 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR3_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR3_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR3_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR3_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3590. CONTROLSS\_OUTPUTXBAR3\_G4 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR3_G4_SEL | R/W  | 0h    | G4: OUTPUT XBAR3 G4 input bit select. Input source is DEL[x].TRIP<br>1:DEL[x] TRIP selected<br>0:DEL[x] TRIP is de-selected |

### 3.18.2.48 CONTROLSS\_OUTPUTXBAR3\_G5 Register

#### 1 CONTROLSS\_OUTPUTXBAR3\_G5 Register (Offset = 1D4h) [reset = 0h]

OUTPUT XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-3591. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 81D4h       |

**Figure 3-1173. CONTROLSS\_OUTPUTXBAR3\_G5 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR3_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR3_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR3_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3593. CONTROLSS\_OUTPUTXBAR3\_G5 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3593. CONTROLSS\_OUTPUTXBAR3\_G5 Register Field Descriptions (continued)**

| Bit  | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------|--------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | OUTPUTXBAR3_G5_SEL | R/W  | 0h    | G5: OUTPUT XBAR3 G5 input bit select.<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.18.2.49 CONTROLSS\_OUTPUTXBAR3\_G6 Register

#### 1 CONTROLSS\_OUTPUTXBAR3\_G6 Register (Offset = 1D8h) [reset = 0h]

OUTPUT XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-3594. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 81D8h       |

**Figure 3-1174. CONTROLSS\_OUTPUTXBAR3\_G6 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR3_G6_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR3_G6_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR3_G6_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3596. CONTROLSS\_OUTPUTXBAR3\_G6 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 19:0  | OUTPUTXBAR3_G6_SEL | R/W  | 0h    | G6: OUTPUT XBAR3 G6 Input Select<br>0: CMPSSA0.CTRIPOUTL<br>1: CMPSSA0.CTRIPOUTH<br>2: CMPSSA1.CTRIPOUTL<br>3: CMPSSA1.CTRIPOUTH<br>4: CMPSSA2.CTRIPOUTL<br>5: CMPSSA2.CTRIPOUTH<br>6: CMPSSA3.CTRIPOUTL<br>7: CMPSSA3.CTRIPOUTH<br>8: CMPSSA4.CTRIPOUTL<br>9: CMPSSA4.CTRIPOUTH<br>10: CMPSSA5.CTRIPOUTL<br>11: CMPSSA5.CTRIPOUTH<br>12: CMPSSA6.CTRIPOUTL<br>13: CMPSSA6.CTRIPOUTH<br>14: CMPSSA7.CTRIPOUTL<br>15: CMPSSA7.CTRIPOUTH<br>16: CMPSSA8.CTRIPOUTL<br>17: CMPSSA8.CTRIPOUTH<br>18: CMPSSA9.CTRIPOUTL<br>19: CMPSSA9.CTRIPOUTH |

### 3.18.2.50 CONTROLSS\_OUTPUTXBAR3\_G7 Register

#### 1 CONTROLSS\_OUTPUTXBAR3\_G7 Register (Offset = 1DCh) [reset = 0h]

OUTPUT XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-3597. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 81DCh       |

**Figure 3-1175. CONTROLSS\_OUTPUTXBAR3\_G7 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR3_G7_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR3_G7_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR3_G7_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3599. CONTROLSS\_OUTPUTXBAR3\_G7 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 19:0  | OUTPUTXBAR3_G7_SEL | R/W  | 0h    | G7: OUTPUT XBAR3 G7 Input Select<br>0: CMPSSB0.CTRIPOUTL<br>1: CMPSSB0.CTRIPOUTH<br>2: CMPSSB1.CTRIPOUTL<br>3: CMPSSB1.CTRIPOUTH<br>4: CMPSSB2.CTRIPOUTL<br>5: CMPSSB2.CTRIPOUTH<br>6: CMPSSB3.CTRIPOUTL<br>7: CMPSSB3.CTRIPOUTH<br>8: CMPSSB4.CTRIPOUTL<br>9: CMPSSB4.CTRIPOUTH<br>10: CMPSSB5.CTRIPOUTL<br>11: CMPSSB5.CTRIPOUTH<br>12: CMPSSB6.CTRIPOUTL<br>13: CMPSSB6.CTRIPOUTH<br>14: CMPSSB7.CTRIPOUTL<br>15: CMPSSB7.CTRIPOUTH<br>16: CMPSSB8.CTRIPOUTL<br>17: CMPSSB8.CTRIPOUTH<br>18: CMPSSB9.CTRIPOUTL<br>19: CMPSSB9.CTRIPOUTH |



### 3.18.2.51 CONTROLSS\_OUTPUTXBAR3\_G8 Register

#### 1 CONTROLSS\_OUTPUTXBAR3\_G8 Register (Offset = 1E0h) [reset = 0h]

OUTPUT XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-3600. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 81E0h       |

**Figure 3-1176. CONTROLSS\_OUTPUTXBAR3\_G8 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR3_G8_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR3_G8_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR3_G8_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3602. CONTROLSS\_OUTPUTXBAR3\_G8 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                            |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                               |
| 19:0  | OUTPUTXBAR3_G8_SEL | R/W  | 0h    | G8: OUTPUT XBAR3 G8 Input Select<br>0:ADC0.EVT1<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.18.2.52 CONTROLSS\_OUTPUTXBAR3\_G9 Register

#### 1 CONTROLSS\_OUTPUTXBAR3\_G9 Register (Offset = 1E4h) [reset = 0h]

OUTPUT XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-3603. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 81E4h       |

**Figure 3-1177. CONTROLSS\_OUTPUTXBAR3\_G9 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR3_G9_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR3_G9_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR3_G9_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3605. CONTROLSS\_OUTPUTXBAR3\_G9 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                               |
| 19:0  | OUTPUTXBAR3_G9_SEL | R/W  | 0h    | G9: OUTPUT XBAR3 G9 Input Select<br>0:PWMSyncOutXBAR.SYNCOU0<br>1:PWMSyncOutXBAR.SYNCOU1<br>2:PWMSyncOutXBAR.SYNCOU2<br>3:PWMSyncOutXBAR.SYNCOU3<br>4:EQEP0.I_OUT<br>5:EQEP0.S_OUT<br>6:EQEP1.I_OUT<br>7:EQEP1.S_OUT<br>8:EQEP2.I_OUT<br>9:EQEP2.S_OUT<br>10:ECAP0.OUT<br>11:ECAP1.OUT<br>12:ECAP2.OUT<br>13:ECAP3.OUT<br>14:ECAP4.OUT<br>15:ECAP5.OUT<br>16:ECAP6.OUT<br>17:ECAP7.OUT<br>18:ECAP8.OUT<br>19:ECAP9.OUT |

### 3.18.2.53 CONTROLSS\_OUTPUTXBAR3\_G10 Register

#### 1 CONTROLSS\_OUTPUTXBAR3\_G10 Register (Offset = 1E8h) [reset = 0h]

OUTPUT XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-3606. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 81E8h       |

**Figure 3-1178. CONTROLSS\_OUTPUTXBAR3\_G10 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR3_G10_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR3_G10_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3608. CONTROLSS\_OUTPUTXBAR3\_G10 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                   |
|-------|---------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                      |
| 15:0  | OUTPUTXBAR3_G10_SEL | R/W  | 0h    | G10: OUTPUT XBAR3 G10 Input Select<br>3<br>0:FSIRX0.RX_TRIG0<br>7<br>4:FSIRX1.RX_TRIG0<br>11<br>8:FSIRX2.RX_TRIG0<br>15<br>12:FSIRX3.RX_TRIG0 |

### 3.18.2.54 CONTROLSS\_OUTPUTXBAR4\_G0 Register

#### 1 CONTROLSS\_OUTPUTXBAR4\_G0 Register (Offset = 200h) [reset = 0h]

OUTPUT XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-3609. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8200h       |

**Figure 3-1179. CONTROLSS\_OUTPUTXBAR4\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR4_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR4_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR4_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR4_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3611. CONTROLSS\_OUTPUTXBAR4\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                       |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR4_G0_SEL | R/W  | 0h    | G0: PWM XBAR4 G0 input bit select. Input source is PWM[x].TRIPOUT<br>1:PWM[x] TRIPOUT selected<br>0:PWM[x] TRIPOUT is de-selected |

### 3.18.2.55 CONTROLSS\_OUTPUTXBAR4\_G1 Register

#### 1 CONTROLSS\_OUTPUTXBAR4\_G1 Register (Offset = 204h) [reset = 0h]

OUTPUT XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-3612. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8204h       |

**Figure 3-1180. CONTROLSS\_OUTPUTXBAR4\_G1 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR4_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR4_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR4_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR4_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3614. CONTROLSS\_OUTPUTXBAR4\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR4_G1_SEL | R/W  | 0h    | G1: OUTPUT XBAR4 G1 input bit select. Input source is PWM[x].SOCA<br>1:PWM[x] SOCA selected<br>0:PWM[x] SOCA is de-selected |

### 3.18.2.56 CONTROLSS\_OUTPUTXBAR4\_G2 Register

#### 1 CONTROLSS\_OUTPUTXBAR4\_G2 Register (Offset = 208h) [reset = 0h]

OUTPUT XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-3615. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8208h       |

**Figure 3-1181. CONTROLSS\_OUTPUTXBAR4\_G2 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR4_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR4_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR4_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR4_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3617. CONTROLSS\_OUTPUTXBAR4\_G2 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR4_G2_SEL | R/W  | 0h    | G2: OUTPUT XBAR4 G2 input bit select. Input source is PWM[x].SOCB<br>1:PWM[x] SOCB selected<br>0:PWM[x] SOCB is de-selected |

### 3.18.2.57 CONTROLSS\_OUTPUTXBAR4\_G3 Register

#### 1 CONTROLSS\_OUTPUTXBAR4\_G3 Register (Offset = 20Ch) [reset = 0h]

OUTPUT XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-3618. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 820Ch       |

**Figure 3-1182. CONTROLSS\_OUTPUTXBAR4\_G3 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR4_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR4_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR4_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR4_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3620. CONTROLSS\_OUTPUTXBAR4\_G3 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                       |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR4_G3_SEL | R/W  | 0h    | G3: OUTPUT XBAR4 G3 input bit select. Input source is DEL[x].ACTIVE<br>1:DEL[x] ACTIVE selected<br>0:DEL[x] ACTIVE is de-selected |

### 3.18.2.58 CONTROLSS\_OUTPUTXBAR4\_G4 Register

#### 1 CONTROLSS\_OUTPUTXBAR4\_G4 Register (Offset = 210h) [reset = 0h]

OUTPUT XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-3621. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8210h       |

**Figure 3-1183. CONTROLSS\_OUTPUTXBAR4\_G4 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR4_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR4_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR4_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR4_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3623. CONTROLSS\_OUTPUTXBAR4\_G4 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR4_G4_SEL | R/W  | 0h    | G4: OUTPUT XBAR4 G4 input bit select. Input source is DEL[x].TRIP<br>1:DEL[x] TRIP selected<br>0:DEL[x] TRIP is de-selected |



### 3.18.2.59 CONTROLSS\_OUTPUTXBAR4\_G5 Register

#### 1 CONTROLSS\_OUTPUTXBAR4\_G5 Register (Offset = 214h) [reset = 0h]

OUTPUT XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-3624. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8214h       |

**Figure 3-1184. CONTROLSS\_OUTPUTXBAR4\_G5 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR4_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR4_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR4_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3626. CONTROLSS\_OUTPUTXBAR4\_G5 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3626. CONTROLSS\_OUTPUTXBAR4\_G5 Register Field Descriptions (continued)**

| Bit  | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------|--------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | OUTPUTXBAR4_G5_SEL | R/W  | 0h    | G5: OUTPUT XBAR4 G5 input bit select.<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.18.2.60 CONTROLSS\_OUTPUTXBAR4\_G6 Register

#### 1 CONTROLSS\_OUTPUTXBAR4\_G6 Register (Offset = 218h) [reset = 0h]

OUTPUT XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-3627. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8218h       |

**Figure 3-1185. CONTROLSS\_OUTPUTXBAR4\_G6 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR4_G6_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR4_G6_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR4_G6_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3629. CONTROLSS\_OUTPUTXBAR4\_G6 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 19:0  | OUTPUTXBAR4_G6_SEL | R/W  | 0h    | G6: OUTPUT XBAR4 G6 Input Select<br>0: CMPSSA0.CTRIPOUTL<br>1: CMPSSA0.CTRIPOUTH<br>2: CMPSSA1.CTRIPOUTL<br>3: CMPSSA1.CTRIPOUTH<br>4: CMPSSA2.CTRIPOUTL<br>5: CMPSSA2.CTRIPOUTH<br>6: CMPSSA3.CTRIPOUTL<br>7: CMPSSA3.CTRIPOUTH<br>8: CMPSSA4.CTRIPOUTL<br>9: CMPSSA4.CTRIPOUTH<br>10: CMPSSA5.CTRIPOUTL<br>11: CMPSSA5.CTRIPOUTH<br>12: CMPSSA6.CTRIPOUTL<br>13: CMPSSA6.CTRIPOUTH<br>14: CMPSSA7.CTRIPOUTL<br>15: CMPSSA7.CTRIPOUTH<br>16: CMPSSA8.CTRIPOUTL<br>17: CMPSSA8.CTRIPOUTH<br>18: CMPSSA9.CTRIPOUTL<br>19: CMPSSA9.CTRIPOUTH |

### 3.18.2.61 CONTROLSS\_OUTPUTXBAR4\_G7 Register

#### 1 CONTROLSS\_OUTPUTXBAR4\_G7 Register (Offset = 21Ch) [reset = 0h]

OUTPUT XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-3630. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 821Ch       |

**Figure 3-1186. CONTROLSS\_OUTPUTXBAR4\_G7 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR4_G7_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR4_G7_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR4_G7_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3632. CONTROLSS\_OUTPUTXBAR4\_G7 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 19:0  | OUTPUTXBAR4_G7_SEL | R/W  | 0h    | G7: OUTPUT XBAR4 G7 Input Select<br>0: CMPSSB0.CTRIPOUTL<br>1: CMPSSB0.CTRIPOUTH<br>2: CMPSSB1.CTRIPOUTL<br>3: CMPSSB1.CTRIPOUTH<br>4: CMPSSB2.CTRIPOUTL<br>5: CMPSSB2.CTRIPOUTH<br>6: CMPSSB3.CTRIPOUTL<br>7: CMPSSB3.CTRIPOUTH<br>8: CMPSSB4.CTRIPOUTL<br>9: CMPSSB4.CTRIPOUTH<br>10: CMPSSB5.CTRIPOUTL<br>11: CMPSSB5.CTRIPOUTH<br>12: CMPSSB6.CTRIPOUTL<br>13: CMPSSB6.CTRIPOUTH<br>14: CMPSSB7.CTRIPOUTL<br>15: CMPSSB7.CTRIPOUTH<br>16: CMPSSB8.CTRIPOUTL<br>17: CMPSSB8.CTRIPOUTH<br>18: CMPSSB9.CTRIPOUTL<br>19: CMPSSB9.CTRIPOUTH |

### 3.18.2.62 CONTROLSS\_OUTPUTXBAR4\_G8 Register

#### 1 CONTROLSS\_OUTPUTXBAR4\_G8 Register (Offset = 220h) [reset = 0h]

OUTPUT XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-3633. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8220h       |

**Figure 3-1187. CONTROLSS\_OUTPUTXBAR4\_G8 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR4_G8_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR4_G8_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR4_G8_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3635. CONTROLSS\_OUTPUTXBAR4\_G8 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                            |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                               |
| 19:0  | OUTPUTXBAR4_G8_SEL | R/W  | 0h    | G8: OUTPUT XBAR4 G8 Input Select<br>0:ADC0.EVT1<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.18.2.63 CONTROLSS\_OUTPUTXBAR4\_G9 Register

#### 1 CONTROLSS\_OUTPUTXBAR4\_G9 Register (Offset = 224h) [reset = 0h]

OUTPUT XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-3636. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8224h       |

**Figure 3-1188. CONTROLSS\_OUTPUTXBAR4\_G9 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR4_G9_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR4_G9_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR4_G9_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3638. CONTROLSS\_OUTPUTXBAR4\_G9 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                               |
| 19:0  | OUTPUTXBAR4_G9_SEL | R/W  | 0h    | G9: OUTPUT XBAR4 G9 Input Select<br>0:PWMSyncOutXBAR.SYNCOU0<br>1:PWMSyncOutXBAR.SYNCOU1<br>2:PWMSyncOutXBAR.SYNCOU2<br>3:PWMSyncOutXBAR.SYNCOU3<br>4:EQEP0.I_OUT<br>5:EQEP0.S_OUT<br>6:EQEP1.I_OUT<br>7:EQEP1.S_OUT<br>8:EQEP2.I_OUT<br>9:EQEP2.S_OUT<br>10:ECAP0.OUT<br>11:ECAP1.OUT<br>12:ECAP2.OUT<br>13:ECAP3.OUT<br>14:ECAP4.OUT<br>15:ECAP5.OUT<br>16:ECAP6.OUT<br>17:ECAP7.OUT<br>18:ECAP8.OUT<br>19:ECAP9.OUT |

### 3.18.2.64 CONTROLSS\_OUTPUTXBAR4\_G10 Register

#### 1 CONTROLSS\_OUTPUTXBAR4\_G10 Register (Offset = 228h) [reset = 0h]

OUTPUT XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-3639. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8228h       |

**Figure 3-1189. CONTROLSS\_OUTPUTXBAR4\_G10 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR4_G10_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR4_G10_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3641. CONTROLSS\_OUTPUTXBAR4\_G10 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                   |
|-------|---------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                      |
| 15:0  | OUTPUTXBAR4_G10_SEL | R/W  | 0h    | G10: OUTPUT XBAR4 G10 Input Select<br>3<br>0:FSIRX0.RX_TRIG0<br>7<br>4:FSIRX1.RX_TRIG0<br>11<br>8:FSIRX2.RX_TRIG0<br>15<br>12:FSIRX3.RX_TRIG0 |

### 3.18.2.65 CONTROLSS\_OUTPUTXBAR5\_G0 Register

#### 1 CONTROLSS\_OUTPUTXBAR5\_G0 Register (Offset = 240h) [reset = 0h]

OUTPUT XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-3642. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8240h       |

**Figure 3-1190. CONTROLSS\_OUTPUTXBAR5\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR5_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR5_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR5_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR5_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3644. CONTROLSS\_OUTPUTXBAR5\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                       |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR5_G0_SEL | R/W  | 0h    | G0: PWM XBAR5 G0 input bit select. Input source is PWM[x].TRIPOUT<br>1:PWM[x] TRIPOUT selected<br>0:PWM[x] TRIPOUT is de-selected |



### 3.18.2.66 CONTROLSS\_OUTPUTXBAR5\_G1 Register

#### 1 CONTROLSS\_OUTPUTXBAR5\_G1 Register (Offset = 244h) [reset = 0h]

OUTPUT XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-3645. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8244h       |

**Figure 3-1191. CONTROLSS\_OUTPUTXBAR5\_G1 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR5_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR5_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR5_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR5_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3647. CONTROLSS\_OUTPUTXBAR5\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR5_G1_SEL | R/W  | 0h    | G1: OUTPUT XBAR5 G1 input bit select. Input source is PWM[x].SOCA<br>1:PWM[x] SOCA selected<br>0:PWM[x] SOCA is de-selected |

### 3.18.2.67 CONTROLSS\_OUTPUTXBAR5\_G2 Register

#### 1 CONTROLSS\_OUTPUTXBAR5\_G2 Register (Offset = 248h) [reset = 0h]

OUTPUT XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-3648. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8248h       |

**Figure 3-1192. CONTROLSS\_OUTPUTXBAR5\_G2 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR5_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR5_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR5_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR5_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3650. CONTROLSS\_OUTPUTXBAR5\_G2 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR5_G2_SEL | R/W  | 0h    | G2: OUTPUT XBAR5 G2 input bit select. Input source is PWM[x].SOCB<br>1:PWM[x] SOCB selected<br>0:PWM[x] SOCB is de-selected |

### 3.18.2.68 CONTROLSS\_OUTPUTXBAR5\_G3 Register

#### 1 CONTROLSS\_OUTPUTXBAR5\_G3 Register (Offset = 24Ch) [reset = 0h]

OUTPUT XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-3651. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 824Ch       |

**Figure 3-1193. CONTROLSS\_OUTPUTXBAR5\_G3 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR5_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR5_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR5_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR5_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3653. CONTROLSS\_OUTPUTXBAR5\_G3 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                       |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR5_G3_SEL | R/W  | 0h    | G3: OUTPUT XBAR5 G3 input bit select. Input source is DEL[x].ACTIVE<br>1:DEL[x] ACTIVE selected<br>0:DEL[x] ACTIVE is de-selected |

### 3.18.2.69 CONTROLSS\_OUTPUTXBAR5\_G4 Register

#### 1 CONTROLSS\_OUTPUTXBAR5\_G4 Register (Offset = 250h) [reset = 0h]

OUTPUT XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-3654. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8250h       |

**Figure 3-1194. CONTROLSS\_OUTPUTXBAR5\_G4 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR5_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR5_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR5_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR5_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3656. CONTROLSS\_OUTPUTXBAR5\_G4 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR5_G4_SEL | R/W  | 0h    | G4: OUTPUT XBAR5 G4 input bit select. Input source is DEL[x].TRIP<br>1:DEL[x] TRIP selected<br>0:DEL[x] TRIP is de-selected |

### 3.18.2.70 CONTROLSS\_OUTPUTXBAR5\_G5 Register

#### 1 CONTROLSS\_OUTPUTXBAR5\_G5 Register (Offset = 254h) [reset = 0h]

OUTPUT XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-3657. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8254h       |

**Figure 3-1195. CONTROLSS\_OUTPUTXBAR5\_G5 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR5_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR5_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR5_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3659. CONTROLSS\_OUTPUTXBAR5\_G5 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3659. CONTROLSS\_OUTPUTXBAR5\_G5 Register Field Descriptions (continued)**

| Bit  | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------|--------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | OUTPUTXBAR5_G5_SEL | R/W  | 0h    | G5: OUTPUT XBAR5 G5 input bit select.<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.18.2.71 CONTROLSS\_OUTPUTXBAR5\_G6 Register

#### 1 CONTROLSS\_OUTPUTXBAR5\_G6 Register (Offset = 258h) [reset = 0h]

OUTPUT XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-3660. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8258h       |

**Figure 3-1196. CONTROLSS\_OUTPUTXBAR5\_G6 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR5_G6_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR5_G6_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR5_G6_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3662. CONTROLSS\_OUTPUTXBAR5\_G6 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 19:0  | OUTPUTXBAR5_G6_SEL | R/W  | 0h    | G6: OUTPUT XBAR5 G6 Input Select<br>0: CMPSSA0.CTRIPOUTL<br>1: CMPSSA0.CTRIPOUTH<br>2: CMPSSA1.CTRIPOUTL<br>3: CMPSSA1.CTRIPOUTH<br>4: CMPSSA2.CTRIPOUTL<br>5: CMPSSA2.CTRIPOUTH<br>6: CMPSSA3.CTRIPOUTL<br>7: CMPSSA3.CTRIPOUTH<br>8: CMPSSA4.CTRIPOUTL<br>9: CMPSSA4.CTRIPOUTH<br>10: CMPSSA5.CTRIPOUTL<br>11: CMPSSA5.CTRIPOUTH<br>12: CMPSSA6.CTRIPOUTL<br>13: CMPSSA6.CTRIPOUTH<br>14: CMPSSA7.CTRIPOUTL<br>15: CMPSSA7.CTRIPOUTH<br>16: CMPSSA8.CTRIPOUTL<br>17: CMPSSA8.CTRIPOUTH<br>18: CMPSSA9.CTRIPOUTL<br>19: CMPSSA9.CTRIPOUTH |

### 3.18.2.72 CONTROLSS\_OUTPUTXBAR5\_G7 Register

#### 1 CONTROLSS\_OUTPUTXBAR5\_G7 Register (Offset = 25Ch) [reset = 0h]

OUTPUT XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-3663. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 825Ch       |

**Figure 3-1197. CONTROLSS\_OUTPUTXBAR5\_G7 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR5_G7_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR5_G7_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR5_G7_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3665. CONTROLSS\_OUTPUTXBAR5\_G7 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 19:0  | OUTPUTXBAR5_G7_SEL | R/W  | 0h    | G7: OUTPUT XBAR5 G7 Input Select<br>0: CMPSSB0.CTRIPOUTL<br>1: CMPSSB0.CTRIPOUTH<br>2: CMPSSB1.CTRIPOUTL<br>3: CMPSSB1.CTRIPOUTH<br>4: CMPSSB2.CTRIPOUTL<br>5: CMPSSB2.CTRIPOUTH<br>6: CMPSSB3.CTRIPOUTL<br>7: CMPSSB3.CTRIPOUTH<br>8: CMPSSB4.CTRIPOUTL<br>9: CMPSSB4.CTRIPOUTH<br>10: CMPSSB5.CTRIPOUTL<br>11: CMPSSB5.CTRIPOUTH<br>12: CMPSSB6.CTRIPOUTL<br>13: CMPSSB6.CTRIPOUTH<br>14: CMPSSB7.CTRIPOUTL<br>15: CMPSSB7.CTRIPOUTH<br>16: CMPSSB8.CTRIPOUTL<br>17: CMPSSB8.CTRIPOUTH<br>18: CMPSSB9.CTRIPOUTL<br>19: CMPSSB9.CTRIPOUTH |



### 3.18.2.73 CONTROLSS\_OUTPUTXBAR5\_G8 Register

#### 1 CONTROLSS\_OUTPUTXBAR5\_G8 Register (Offset = 260h) [reset = 0h]

OUTPUT XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-3666. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8260h       |

**Figure 3-1198. CONTROLSS\_OUTPUTXBAR5\_G8 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR5_G8_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR5_G8_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR5_G8_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3668. CONTROLSS\_OUTPUTXBAR5\_G8 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                            |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                               |
| 19:0  | OUTPUTXBAR5_G8_SEL | R/W  | 0h    | G8: OUTPUT XBAR5 G8 Input Select<br>0:ADC0.EVT1<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.18.2.74 CONTROLSS\_OUTPUTXBAR5\_G9 Register

#### 1 CONTROLSS\_OUTPUTXBAR5\_G9 Register (Offset = 264h) [reset = 0h]

OUTPUT XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-3669. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8264h       |

**Figure 3-1199. CONTROLSS\_OUTPUTXBAR5\_G9 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR5_G9_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR5_G9_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR5_G9_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3671. CONTROLSS\_OUTPUTXBAR5\_G9 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                               |
| 19:0  | OUTPUTXBAR5_G9_SEL | R/W  | 0h    | G9: OUTPUT XBAR5 G9 Input Select<br>0:PWMSyncOutXBAR.SYNCOU0<br>1:PWMSyncOutXBAR.SYNCOU1<br>2:PWMSyncOutXBAR.SYNCOU2<br>3:PWMSyncOutXBAR.SYNCOU3<br>4:EQEP0.I_OUT<br>5:EQEP0.S_OUT<br>6:EQEP1.I_OUT<br>7:EQEP1.S_OUT<br>8:EQEP2.I_OUT<br>9:EQEP2.S_OUT<br>10:ECAP0.OUT<br>11:ECAP1.OUT<br>12:ECAP2.OUT<br>13:ECAP3.OUT<br>14:ECAP4.OUT<br>15:ECAP5.OUT<br>16:ECAP6.OUT<br>17:ECAP7.OUT<br>18:ECAP8.OUT<br>19:ECAP9.OUT |

### 3.18.2.75 CONTROLSS\_OUTPUTXBAR5\_G10 Register

#### 1 CONTROLSS\_OUTPUTXBAR5\_G10 Register (Offset = 268h) [reset = 0h]

OUTPUT XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-3672. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8268h       |

**Figure 3-1200. CONTROLSS\_OUTPUTXBAR5\_G10 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR5_G10_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR5_G10_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3674. CONTROLSS\_OUTPUTXBAR5\_G10 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                   |
|-------|---------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                      |
| 15:0  | OUTPUTXBAR5_G10_SEL | R/W  | 0h    | G10: OUTPUT XBAR5 G10 Input Select<br>3<br>0:FSIRX0.RX_TRIG0<br>7<br>4:FSIRX1.RX_TRIG0<br>11<br>8:FSIRX2.RX_TRIG0<br>15<br>12:FSIRX3.RX_TRIG0 |

### 3.18.2.76 CONTROLSS\_OUTPUTXBAR6\_G0 Register

#### 1 CONTROLSS\_OUTPUTXBAR6\_G0 Register (Offset = 280h) [reset = 0h]

OUTPUT XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-3675. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8280h       |

**Figure 3-1201. CONTROLSS\_OUTPUTXBAR6\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR6_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR6_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR6_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR6_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3677. CONTROLSS\_OUTPUTXBAR6\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                       |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR6_G0_SEL | R/W  | 0h    | G0: PWM XBAR6 G0 input bit select. Input source is PWM[x].TRIPOUT<br>1:PWM[x] TRIPOUT selected<br>0:PWM[x] TRIPOUT is de-selected |

### 3.18.2.77 CONTROLSS\_OUTPUTXBAR6\_G1 Register

#### 1 CONTROLSS\_OUTPUTXBAR6\_G1 Register (Offset = 284h) [reset = 0h]

OUTPUT XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-3678. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8284h       |

**Figure 3-1202. CONTROLSS\_OUTPUTXBAR6\_G1 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR6_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR6_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR6_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR6_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3680. CONTROLSS\_OUTPUTXBAR6\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR6_G1_SEL | R/W  | 0h    | G1: OUTPUT XBAR6 G1 input bit select. Input source is PWM[x].SOCA<br>1:PWM[x] SOCA selected<br>0:PWM[x] SOCA is de-selected |

### 3.18.2.78 CONTROLSS\_OUTPUTXBAR6\_G2 Register

#### 1 CONTROLSS\_OUTPUTXBAR6\_G2 Register (Offset = 288h) [reset = 0h]

OUTPUT XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-3681. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8288h       |

**Figure 3-1203. CONTROLSS\_OUTPUTXBAR6\_G2 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR6_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR6_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR6_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR6_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3683. CONTROLSS\_OUTPUTXBAR6\_G2 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR6_G2_SEL | R/W  | 0h    | G2: OUTPUT XBAR6 G2 input bit select. Input source is PWM[x].SOCB<br>1:PWM[x] SOCB selected<br>0:PWM[x] SOCB is de-selected |

### 3.18.2.79 CONTROLSS\_OUTPUTXBAR6\_G3 Register

#### 1 CONTROLSS\_OUTPUTXBAR6\_G3 Register (Offset = 28Ch) [reset = 0h]

OUTPUT XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-3684. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 828Ch       |

**Figure 3-1204. CONTROLSS\_OUTPUTXBAR6\_G3 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR6_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR6_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR6_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR6_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3686. CONTROLSS\_OUTPUTXBAR6\_G3 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                       |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR6_G3_SEL | R/W  | 0h    | G3: OUTPUT XBAR6 G3 input bit select. Input source is DEL[x].ACTIVE<br>1:DEL[x] ACTIVE selected<br>0:DEL[x] ACTIVE is de-selected |

### 3.18.2.80 CONTROLSS\_OUTPUTXBAR6\_G4 Register

#### 1 CONTROLSS\_OUTPUTXBAR6\_G4 Register (Offset = 290h) [reset = 0h]

OUTPUT XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-3687. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8290h       |

**Figure 3-1205. CONTROLSS\_OUTPUTXBAR6\_G4 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR6_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR6_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR6_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR6_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3689. CONTROLSS\_OUTPUTXBAR6\_G4 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR6_G4_SEL | R/W  | 0h    | G4: OUTPUT XBAR6 G4 input bit select. Input source is DEL[x].TRIP<br>1:DEL[x] TRIP selected<br>0:DEL[x] TRIP is de-selected |



### 3.18.2.81 CONTROLSS\_OUTPUTXBAR6\_G5 Register

#### 1 CONTROLSS\_OUTPUTXBAR6\_G5 Register (Offset = 294h) [reset = 0h]

OUTPUT XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-3690. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8294h       |

**Figure 3-1206. CONTROLSS\_OUTPUTXBAR6\_G5 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR6_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR6_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR6_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3692. CONTROLSS\_OUTPUTXBAR6\_G5 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3692. CONTROLSS\_OUTPUTXBAR6\_G5 Register Field Descriptions (continued)**

| Bit  | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------|--------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | OUTPUTXBAR6_G5_SEL | R/W  | 0h    | G5: OUTPUT XBAR6 G5 input bit select.<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.18.2.82 CONTROLSS\_OUTPUTXBAR6\_G6 Register

#### 1 CONTROLSS\_OUTPUTXBAR6\_G6 Register (Offset = 298h) [reset = 0h]

OUTPUT XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-3693. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8298h       |

**Figure 3-1207. CONTROLSS\_OUTPUTXBAR6\_G6 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR6_G6_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR6_G6_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR6_G6_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3695. CONTROLSS\_OUTPUTXBAR6\_G6 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 19:0  | OUTPUTXBAR6_G6_SEL | R/W  | 0h    | G6: OUTPUT XBAR6 G6 Input Select<br>0: CMPSSA0.CTRIPOUTL<br>1: CMPSSA0.CTRIPOUTH<br>2: CMPSSA1.CTRIPOUTL<br>3: CMPSSA1.CTRIPOUTH<br>4: CMPSSA2.CTRIPOUTL<br>5: CMPSSA2.CTRIPOUTH<br>6: CMPSSA3.CTRIPOUTL<br>7: CMPSSA3.CTRIPOUTH<br>8: CMPSSA4.CTRIPOUTL<br>9: CMPSSA4.CTRIPOUTH<br>10: CMPSSA5.CTRIPOUTL<br>11: CMPSSA5.CTRIPOUTH<br>12: CMPSSA6.CTRIPOUTL<br>13: CMPSSA6.CTRIPOUTH<br>14: CMPSSA7.CTRIPOUTL<br>15: CMPSSA7.CTRIPOUTH<br>16: CMPSSA8.CTRIPOUTL<br>17: CMPSSA8.CTRIPOUTH<br>18: CMPSSA9.CTRIPOUTL<br>19: CMPSSA9.CTRIPOUTH |

### 3.18.2.83 CONTROLSS\_OUTPUTXBAR6\_G7 Register

#### 1 CONTROLSS\_OUTPUTXBAR6\_G7 Register (Offset = 29Ch) [reset = 0h]

OUTPUT XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-3696. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 829Ch       |

**Figure 3-1208. CONTROLSS\_OUTPUTXBAR6\_G7 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR6_G7_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR6_G7_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR6_G7_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3698. CONTROLSS\_OUTPUTXBAR6\_G7 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 19:0  | OUTPUTXBAR6_G7_SEL | R/W  | 0h    | G7: OUTPUT XBAR6 G7 Input Select<br>0: CMPSSB0.CTRIPOUTL<br>1: CMPSSB0.CTRIPOUTH<br>2: CMPSSB1.CTRIPOUTL<br>3: CMPSSB1.CTRIPOUTH<br>4: CMPSSB2.CTRIPOUTL<br>5: CMPSSB2.CTRIPOUTH<br>6: CMPSSB3.CTRIPOUTL<br>7: CMPSSB3.CTRIPOUTH<br>8: CMPSSB4.CTRIPOUTL<br>9: CMPSSB4.CTRIPOUTH<br>10: CMPSSB5.CTRIPOUTL<br>11: CMPSSB5.CTRIPOUTH<br>12: CMPSSB6.CTRIPOUTL<br>13: CMPSSB6.CTRIPOUTH<br>14: CMPSSB7.CTRIPOUTL<br>15: CMPSSB7.CTRIPOUTH<br>16: CMPSSB8.CTRIPOUTL<br>17: CMPSSB8.CTRIPOUTH<br>18: CMPSSB9.CTRIPOUTL<br>19: CMPSSB9.CTRIPOUTH |

### 3.18.2.84 CONTROLSS\_OUTPUTXBAR6\_G8 Register

#### 1 CONTROLSS\_OUTPUTXBAR6\_G8 Register (Offset = 2A0h) [reset = 0h]

OUTPUT XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-3699. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 82A0h       |

**Figure 3-1209. CONTROLSS\_OUTPUTXBAR6\_G8 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR6_G8_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR6_G8_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR6_G8_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3701. CONTROLSS\_OUTPUTXBAR6\_G8 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                            |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                               |
| 19:0  | OUTPUTXBAR6_G8_SEL | R/W  | 0h    | G8: OUTPUT XBAR6 G8 Input Select<br>0:ADC0.EVT1<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.18.2.85 CONTROLSS\_OUTPUTXBAR6\_G9 Register

#### 1 CONTROLSS\_OUTPUTXBAR6\_G9 Register (Offset = 2A4h) [reset = 0h]

OUTPUT XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-3702. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 82A4h       |

**Figure 3-1210. CONTROLSS\_OUTPUTXBAR6\_G9 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR6_G9_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR6_G9_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR6_G9_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3704. CONTROLSS\_OUTPUTXBAR6\_G9 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                               |
| 19:0  | OUTPUTXBAR6_G9_SEL | R/W  | 0h    | G9: OUTPUT XBAR6 G9 Input Select<br>0:PWMSyncOutXBAR.SYNCOU0<br>1:PWMSyncOutXBAR.SYNCOU1<br>2:PWMSyncOutXBAR.SYNCOU2<br>3:PWMSyncOutXBAR.SYNCOU3<br>4:EQEP0.I_OUT<br>5:EQEP0.S_OUT<br>6:EQEP1.I_OUT<br>7:EQEP1.S_OUT<br>8:EQEP2.I_OUT<br>9:EQEP2.S_OUT<br>10:ECAP0.OUT<br>11:ECAP1.OUT<br>12:ECAP2.OUT<br>13:ECAP3.OUT<br>14:ECAP4.OUT<br>15:ECAP5.OUT<br>16:ECAP6.OUT<br>17:ECAP7.OUT<br>18:ECAP8.OUT<br>19:ECAP9.OUT |

### 3.18.2.86 CONTROLSS\_OUTPUTXBAR6\_G10 Register

#### 1 CONTROLSS\_OUTPUTXBAR6\_G10 Register (Offset = 2A8h) [reset = 0h]

OUTPUT XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-3705. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 82A8h       |

**Figure 3-1211. CONTROLSS\_OUTPUTXBAR6\_G10 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR6_G10_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR6_G10_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3707. CONTROLSS\_OUTPUTXBAR6\_G10 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                   |
|-------|---------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                      |
| 15:0  | OUTPUTXBAR6_G10_SEL | R/W  | 0h    | G10: OUTPUT XBAR6 G10 Input Select<br>3<br>0:FSIRX0.RX_TRIG0<br>7<br>4:FSIRX1.RX_TRIG0<br>11<br>8:FSIRX2.RX_TRIG0<br>15<br>12:FSIRX3.RX_TRIG0 |

### 3.18.2.87 CONTROLSS\_OUTPUTXBAR7\_G0 Register

#### 1 CONTROLSS\_OUTPUTXBAR7\_G0 Register (Offset = 2C0h) [reset = 0h]

OUTPUT XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-3708. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 82C0h       |

**Figure 3-1212. CONTROLSS\_OUTPUTXBAR7\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR7_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR7_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR7_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR7_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3710. CONTROLSS\_OUTPUTXBAR7\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                       |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR7_G0_SEL | R/W  | 0h    | G0: PWM XBAR7 G0 input bit select. Input source is PWM[x].TRIPOUT<br>1:PWM[x] TRIPOUT selected<br>0:PWM[x] TRIPOUT is de-selected |



### 3.18.2.88 CONTROLSS\_OUTPUTXBAR7\_G1 Register

#### 1 CONTROLSS\_OUTPUTXBAR7\_G1 Register (Offset = 2C4h) [reset = 0h]

OUTPUT XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-3711. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 82C4h       |

**Figure 3-1213. CONTROLSS\_OUTPUTXBAR7\_G1 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR7_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR7_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR7_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR7_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3713. CONTROLSS\_OUTPUTXBAR7\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR7_G1_SEL | R/W  | 0h    | G1: OUTPUT XBAR7 G1 input bit select. Input source is PWM[x].SOCA<br>1:PWM[x] SOCA selected<br>0:PWM[x] SOCA is de-selected |

### 3.18.2.89 CONTROLSS\_OUTPUTXBAR7\_G2 Register

#### 1 CONTROLSS\_OUTPUTXBAR7\_G2 Register (Offset = 2C8h) [reset = 0h]

OUTPUT XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-3714. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 82C8h       |

**Figure 3-1214. CONTROLSS\_OUTPUTXBAR7\_G2 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR7_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR7_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR7_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR7_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3716. CONTROLSS\_OUTPUTXBAR7\_G2 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR7_G2_SEL | R/W  | 0h    | G2: OUTPUT XBAR7 G2 input bit select. Input source is PWM[x].SOCB<br>1:PWM[x] SOCB selected<br>0:PWM[x] SOCB is de-selected |

### 3.18.2.90 CONTROLSS\_OUTPUTXBAR7\_G3 Register

#### 1 CONTROLSS\_OUTPUTXBAR7\_G3 Register (Offset = 2CCh) [reset = 0h]

OUTPUT XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-3717. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 82CCh       |

**Figure 3-1215. CONTROLSS\_OUTPUTXBAR7\_G3 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR7_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR7_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR7_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR7_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3719. CONTROLSS\_OUTPUTXBAR7\_G3 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                       |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR7_G3_SEL | R/W  | 0h    | G3: OUTPUT XBAR7 G3 input bit select. Input source is DEL[x].ACTIVE<br>1:DEL[x] ACTIVE selected<br>0:DEL[x] ACTIVE is de-selected |

### 3.18.2.91 CONTROLSS\_OUTPUTXBAR7\_G4 Register

#### 1 CONTROLSS\_OUTPUTXBAR7\_G4 Register (Offset = 2D0h) [reset = 0h]

OUTPUT XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-3720. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 82D0h       |

**Figure 3-1216. CONTROLSS\_OUTPUTXBAR7\_G4 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR7_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR7_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR7_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR7_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3722. CONTROLSS\_OUTPUTXBAR7\_G4 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR7_G4_SEL | R/W  | 0h    | G4: OUTPUT XBAR7 G4 input bit select. Input source is DEL[x].TRIP<br>1:DEL[x] TRIP selected<br>0:DEL[x] TRIP is de-selected |

### 3.18.2.92 CONTROLSS\_OUTPUTXBAR7\_G5 Register

#### 1 CONTROLSS\_OUTPUTXBAR7\_G5 Register (Offset = 2D4h) [reset = 0h]

OUTPUT XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-3723. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 82D4h       |

**Figure 3-1217. CONTROLSS\_OUTPUTXBAR7\_G5 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR7_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR7_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR7_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3725. CONTROLSS\_OUTPUTXBAR7\_G5 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3725. CONTROLSS\_OUTPUTXBAR7\_G5 Register Field Descriptions (continued)**

| Bit  | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------|--------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | OUTPUTXBAR7_G5_SEL | R/W  | 0h    | G5: OUTPUT XBAR7 G5 input bit select.<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.18.2.93 CONTROLSS\_OUTPUTXBAR7\_G6 Register

#### 1 CONTROLSS\_OUTPUTXBAR7\_G6 Register (Offset = 2D8h) [reset = 0h]

OUTPUT XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-3726. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 82D8h       |

**Figure 3-1218. CONTROLSS\_OUTPUTXBAR7\_G6 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR7_G6_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR7_G6_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR7_G6_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3728. CONTROLSS\_OUTPUTXBAR7\_G6 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 19:0  | OUTPUTXBAR7_G6_SEL | R/W  | 0h    | G6: OUTPUT XBAR7 G6 Input Select<br>0: CMPSSA0.CTRIPOUTL<br>1: CMPSSA0.CTRIPOUTH<br>2: CMPSSA1.CTRIPOUTL<br>3: CMPSSA1.CTRIPOUTH<br>4: CMPSSA2.CTRIPOUTL<br>5: CMPSSA2.CTRIPOUTH<br>6: CMPSSA3.CTRIPOUTL<br>7: CMPSSA3.CTRIPOUTH<br>8: CMPSSA4.CTRIPOUTL<br>9: CMPSSA4.CTRIPOUTH<br>10: CMPSSA5.CTRIPOUTL<br>11: CMPSSA5.CTRIPOUTH<br>12: CMPSSA6.CTRIPOUTL<br>13: CMPSSA6.CTRIPOUTH<br>14: CMPSSA7.CTRIPOUTL<br>15: CMPSSA7.CTRIPOUTH<br>16: CMPSSA8.CTRIPOUTL<br>17: CMPSSA8.CTRIPOUTH<br>18: CMPSSA9.CTRIPOUTL<br>19: CMPSSA9.CTRIPOUTH |

### 3.18.2.94 CONTROLSS\_OUTPUTXBAR7\_G7 Register

#### 1 CONTROLSS\_OUTPUTXBAR7\_G7 Register (Offset = 2DCh) [reset = 0h]

OUTPUT XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-3729. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 82DCh       |

**Figure 3-1219. CONTROLSS\_OUTPUTXBAR7\_G7 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR7_G7_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR7_G7_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR7_G7_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3731. CONTROLSS\_OUTPUTXBAR7\_G7 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 19:0  | OUTPUTXBAR7_G7_SEL | R/W  | 0h    | G7: OUTPUT XBAR7 G7 Input Select<br>0: CMPSSB0.CTRIPOUTL<br>1: CMPSSB0.CTRIPOUTH<br>2: CMPSSB1.CTRIPOUTL<br>3: CMPSSB1.CTRIPOUTH<br>4: CMPSSB2.CTRIPOUTL<br>5: CMPSSB2.CTRIPOUTH<br>6: CMPSSB3.CTRIPOUTL<br>7: CMPSSB3.CTRIPOUTH<br>8: CMPSSB4.CTRIPOUTL<br>9: CMPSSB4.CTRIPOUTH<br>10: CMPSSB5.CTRIPOUTL<br>11: CMPSSB5.CTRIPOUTH<br>12: CMPSSB6.CTRIPOUTL<br>13: CMPSSB6.CTRIPOUTH<br>14: CMPSSB7.CTRIPOUTL<br>15: CMPSSB7.CTRIPOUTH<br>16: CMPSSB8.CTRIPOUTL<br>17: CMPSSB8.CTRIPOUTH<br>18: CMPSSB9.CTRIPOUTL<br>19: CMPSSB9.CTRIPOUTH |



### 3.18.2.95 CONTROLSS\_OUTPUTXBAR7\_G8 Register

#### 1 CONTROLSS\_OUTPUTXBAR7\_G8 Register (Offset = 2E0h) [reset = 0h]

OUTPUT XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-3732. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 82E0h       |

**Figure 3-1220. CONTROLSS\_OUTPUTXBAR7\_G8 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR7_G8_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR7_G8_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR7_G8_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3734. CONTROLSS\_OUTPUTXBAR7\_G8 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                            |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                               |
| 19:0  | OUTPUTXBAR7_G8_SEL | R/W  | 0h    | G8: OUTPUT XBAR7 G8 Input Select<br>0:ADC0.EVT1<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.18.2.96 CONTROLSS\_OUTPUTXBAR7\_G9 Register

#### 1 CONTROLSS\_OUTPUTXBAR7\_G9 Register (Offset = 2E4h) [reset = 0h]

OUTPUT XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-3735. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 82E4h       |

**Figure 3-1221. CONTROLSS\_OUTPUTXBAR7\_G9 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR7_G9_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR7_G9_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR7_G9_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3737. CONTROLSS\_OUTPUTXBAR7\_G9 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                               |
| 19:0  | OUTPUTXBAR7_G9_SEL | R/W  | 0h    | G9: OUTPUT XBAR7 G9 Input Select<br>0:PWMSyncOutXBAR.SYNCOU0<br>1:PWMSyncOutXBAR.SYNCOU1<br>2:PWMSyncOutXBAR.SYNCOU2<br>3:PWMSyncOutXBAR.SYNCOU3<br>4:EQEP0.I_OUT<br>5:EQEP0.S_OUT<br>6:EQEP1.I_OUT<br>7:EQEP1.S_OUT<br>8:EQEP2.I_OUT<br>9:EQEP2.S_OUT<br>10:ECAP0.OUT<br>11:ECAP1.OUT<br>12:ECAP2.OUT<br>13:ECAP3.OUT<br>14:ECAP4.OUT<br>15:ECAP5.OUT<br>16:ECAP6.OUT<br>17:ECAP7.OUT<br>18:ECAP8.OUT<br>19:ECAP9.OUT |

### 3.18.2.97 CONTROLSS\_OUTPUTXBAR7\_G10 Register

#### 1 CONTROLSS\_OUTPUTXBAR7\_G10 Register (Offset = 2E8h) [reset = 0h]

OUTPUT XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-3738. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 82E8h       |

**Figure 3-1222. CONTROLSS\_OUTPUTXBAR7\_G10 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR7_G10_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR7_G10_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3740. CONTROLSS\_OUTPUTXBAR7\_G10 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                   |
|-------|---------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                      |
| 15:0  | OUTPUTXBAR7_G10_SEL | R/W  | 0h    | G10: OUTPUT XBAR7 G10 Input Select<br>3<br>0:FSIRX0.RX_TRIG0<br>7<br>4:FSIRX1.RX_TRIG0<br>11<br>8:FSIRX2.RX_TRIG0<br>15<br>12:FSIRX3.RX_TRIG0 |

### 3.18.2.98 CONTROLSS\_OUTPUTXBAR8\_G0 Register

#### 1 CONTROLSS\_OUTPUTXBAR8\_G0 Register (Offset = 300h) [reset = 0h]

OUTPUT XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-3741. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8300h       |

**Figure 3-1223. CONTROLSS\_OUTPUTXBAR8\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR8_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR8_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR8_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR8_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3743. CONTROLSS\_OUTPUTXBAR8\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                       |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR8_G0_SEL | R/W  | 0h    | G0: PWM XBAR8 G0 input bit select. Input source is PWM[x].TRIPOUT<br>1:PWM[x] TRIPOUT selected<br>0:PWM[x] TRIPOUT is de-selected |

### 3.18.2.99 CONTROLSS\_OUTPUTXBAR8\_G1 Register

#### 1 CONTROLSS\_OUTPUTXBAR8\_G1 Register (Offset = 304h) [reset = 0h]

OUTPUT XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-3744. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8304h       |

**Figure 3-1224. CONTROLSS\_OUTPUTXBAR8\_G1 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR8_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR8_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR8_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR8_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3746. CONTROLSS\_OUTPUTXBAR8\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR8_G1_SEL | R/W  | 0h    | G1: OUTPUT XBAR8 G1 input bit select. Input source is PWM[x].SOCA<br>1:PWM[x] SOCA selected<br>0:PWM[x] SOCA is de-selected |

### 3.18.2.100 CONTROLSS\_OUTPUTXBAR8\_G2 Register

#### 1 CONTROLSS\_OUTPUTXBAR8\_G2 Register (Offset = 308h) [reset = 0h]

OUTPUT XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-3747. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8308h       |

**Figure 3-1225. CONTROLSS\_OUTPUTXBAR8\_G2 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR8_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR8_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR8_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR8_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3749. CONTROLSS\_OUTPUTXBAR8\_G2 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR8_G2_SEL | R/W  | 0h    | G2: OUTPUT XBAR8 G2 input bit select. Input source is PWM[x].SOCB<br>1:PWM[x] SOCB selected<br>0:PWM[x] SOCB is de-selected |

### 3.18.2.101 CONTROLSS\_OUTPUTXBAR8\_G3 Register

#### 1 CONTROLSS\_OUTPUTXBAR8\_G3 Register (Offset = 30Ch) [reset = 0h]

OUTPUT XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-3750. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 830Ch       |

**Figure 3-1226. CONTROLSS\_OUTPUTXBAR8\_G3 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR8_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR8_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR8_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR8_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3752. CONTROLSS\_OUTPUTXBAR8\_G3 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                       |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR8_G3_SEL | R/W  | 0h    | G3: OUTPUT XBAR8 G3 input bit select. Input source is DEL[x].ACTIVE<br>1:DEL[x] ACTIVE selected<br>0:DEL[x] ACTIVE is de-selected |

### 3.18.2.102 CONTROLSS\_OUTPUTXBAR8\_G4 Register

#### 1 CONTROLSS\_OUTPUTXBAR8\_G4 Register (Offset = 310h) [reset = 0h]

OUTPUT XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-3753. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8310h       |

**Figure 3-1227. CONTROLSS\_OUTPUTXBAR8\_G4 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR8_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR8_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR8_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR8_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3755. CONTROLSS\_OUTPUTXBAR8\_G4 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR8_G4_SEL | R/W  | 0h    | G4: OUTPUT XBAR8 G4 input bit select. Input source is DEL[x].TRIP<br>1:DEL[x] TRIP selected<br>0:DEL[x] TRIP is de-selected |



### 3.18.2.103 CONTROLSS\_OUTPUTXBAR8\_G5 Register

#### 1 CONTROLSS\_OUTPUTXBAR8\_G5 Register (Offset = 314h) [reset = 0h]

OUTPUT XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-3756. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8314h       |

**Figure 3-1228. CONTROLSS\_OUTPUTXBAR8\_G5 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR8_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR8_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR8_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3758. CONTROLSS\_OUTPUTXBAR8\_G5 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3758. CONTROLSS\_OUTPUTXBAR8\_G5 Register Field Descriptions (continued)**

| Bit  | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------|--------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | OUTPUTXBAR8_G5_SEL | R/W  | 0h    | G5: OUTPUT XBAR8 G5 input bit select.<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.18.2.104 CONTROLSS\_OUTPUTXBAR8\_G6 Register

#### 1 CONTROLSS\_OUTPUTXBAR8\_G6 Register (Offset = 318h) [reset = 0h]

OUTPUT XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-3759. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8318h       |

**Figure 3-1229. CONTROLSS\_OUTPUTXBAR8\_G6 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR8_G6_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR8_G6_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR8_G6_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3761. CONTROLSS\_OUTPUTXBAR8\_G6 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 19:0  | OUTPUTXBAR8_G6_SEL | R/W  | 0h    | G6: OUTPUT XBAR8 G6 Input Select<br>0: CMPSSA0.CTRIPOUTL<br>1: CMPSSA0.CTRIPOUTH<br>2: CMPSSA1.CTRIPOUTL<br>3: CMPSSA1.CTRIPOUTH<br>4: CMPSSA2.CTRIPOUTL<br>5: CMPSSA2.CTRIPOUTH<br>6: CMPSSA3.CTRIPOUTL<br>7: CMPSSA3.CTRIPOUTH<br>8: CMPSSA4.CTRIPOUTL<br>9: CMPSSA4.CTRIPOUTH<br>10: CMPSSA5.CTRIPOUTL<br>11: CMPSSA5.CTRIPOUTH<br>12: CMPSSA6.CTRIPOUTL<br>13: CMPSSA6.CTRIPOUTH<br>14: CMPSSA7.CTRIPOUTL<br>15: CMPSSA7.CTRIPOUTH<br>16: CMPSSA8.CTRIPOUTL<br>17: CMPSSA8.CTRIPOUTH<br>18: CMPSSA9.CTRIPOUTL<br>19: CMPSSA9.CTRIPOUTH |

### 3.18.2.105 CONTROLSS\_OUTPUTXBAR8\_G7 Register

#### 1 CONTROLSS\_OUTPUTXBAR8\_G7 Register (Offset = 31Ch) [reset = 0h]

OUTPUT XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-3762. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 831Ch       |

**Figure 3-1230. CONTROLSS\_OUTPUTXBAR8\_G7 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR8_G7_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR8_G7_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR8_G7_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3764. CONTROLSS\_OUTPUTXBAR8\_G7 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 19:0  | OUTPUTXBAR8_G7_SEL | R/W  | 0h    | G7: OUTPUT XBAR8 G7 Input Select<br>0: CMPSSB0.CTRIPOUTL<br>1: CMPSSB0.CTRIPOUTH<br>2: CMPSSB1.CTRIPOUTL<br>3: CMPSSB1.CTRIPOUTH<br>4: CMPSSB2.CTRIPOUTL<br>5: CMPSSB2.CTRIPOUTH<br>6: CMPSSB3.CTRIPOUTL<br>7: CMPSSB3.CTRIPOUTH<br>8: CMPSSB4.CTRIPOUTL<br>9: CMPSSB4.CTRIPOUTH<br>10: CMPSSB5.CTRIPOUTL<br>11: CMPSSB5.CTRIPOUTH<br>12: CMPSSB6.CTRIPOUTL<br>13: CMPSSB6.CTRIPOUTH<br>14: CMPSSB7.CTRIPOUTL<br>15: CMPSSB7.CTRIPOUTH<br>16: CMPSSB8.CTRIPOUTL<br>17: CMPSSB8.CTRIPOUTH<br>18: CMPSSB9.CTRIPOUTL<br>19: CMPSSB9.CTRIPOUTH |

### 3.18.2.106 CONTROLSS\_OUTPUTXBAR8\_G8 Register

#### 1 CONTROLSS\_OUTPUTXBAR8\_G8 Register (Offset = 320h) [reset = 0h]

OUTPUT XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-3765. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8320h       |

**Figure 3-1231. CONTROLSS\_OUTPUTXBAR8\_G8 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR8_G8_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR8_G8_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR8_G8_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3767. CONTROLSS\_OUTPUTXBAR8\_G8 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                            |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                               |
| 19:0  | OUTPUTXBAR8_G8_SEL | R/W  | 0h    | G8: OUTPUT XBAR8 G8 Input Select<br>0:ADC0.EVT1<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.18.2.107 CONTROLSS\_OUTPUTXBAR8\_G9 Register

#### 1 CONTROLSS\_OUTPUTXBAR8\_G9 Register (Offset = 324h) [reset = 0h]

OUTPUT XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-3768. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8324h       |

**Figure 3-1232. CONTROLSS\_OUTPUTXBAR8\_G9 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR8_G9_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR8_G9_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR8_G9_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3770. CONTROLSS\_OUTPUTXBAR8\_G9 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                               |
| 19:0  | OUTPUTXBAR8_G9_SEL | R/W  | 0h    | G9: OUTPUT XBAR8 G9 Input Select<br>0:PWMSyncOutXBAR.SYNCOU0<br>1:PWMSyncOutXBAR.SYNCOU1<br>2:PWMSyncOutXBAR.SYNCOU2<br>3:PWMSyncOutXBAR.SYNCOU3<br>4:EQEP0.I_OUT<br>5:EQEP0.S_OUT<br>6:EQEP1.I_OUT<br>7:EQEP1.S_OUT<br>8:EQEP2.I_OUT<br>9:EQEP2.S_OUT<br>10:ECAP0.OUT<br>11:ECAP1.OUT<br>12:ECAP2.OUT<br>13:ECAP3.OUT<br>14:ECAP4.OUT<br>15:ECAP5.OUT<br>16:ECAP6.OUT<br>17:ECAP7.OUT<br>18:ECAP8.OUT<br>19:ECAP9.OUT |

### 3.18.2.108 CONTROLSS\_OUTPUTXBAR8\_G10 Register

#### 1 CONTROLSS\_OUTPUTXBAR8\_G10 Register (Offset = 328h) [reset = 0h]

OUTPUT XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-3771. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8328h       |

**Figure 3-1233. CONTROLSS\_OUTPUTXBAR8\_G10 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR8_G10_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR8_G10_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3773. CONTROLSS\_OUTPUTXBAR8\_G10 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                   |
|-------|---------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                      |
| 15:0  | OUTPUTXBAR8_G10_SEL | R/W  | 0h    | G10: OUTPUT XBAR8 G10 Input Select<br>3<br>0:FSIRX0.RX_TRIG0<br>7<br>4:FSIRX1.RX_TRIG0<br>11<br>8:FSIRX2.RX_TRIG0<br>15<br>12:FSIRX3.RX_TRIG0 |

### 3.18.2.109 CONTROLSS\_OUTPUTXBAR9\_G0 Register

#### 1 CONTROLSS\_OUTPUTXBAR9\_G0 Register (Offset = 340h) [reset = 0h]

OUTPUT XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-3774. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8340h       |

**Figure 3-1234. CONTROLSS\_OUTPUTXBAR9\_G0 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR9_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR9_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR9_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR9_G0_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3776. CONTROLSS\_OUTPUTXBAR9\_G0 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                       |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR9_G0_SEL | R/W  | 0h    | G0: PWM XBAR9 G0 input bit select. Input source is PWM[x].TRIPOUT<br>1:PWM[x] TRIPOUT selected<br>0:PWM[x] TRIPOUT is de-selected |



### 3.18.2.110 CONTROLSS\_OUTPUTXBAR9\_G1 Register

#### 1 CONTROLSS\_OUTPUTXBAR9\_G1 Register (Offset = 344h) [reset = 0h]

OUTPUT XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-3777. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8344h       |

**Figure 3-1235. CONTROLSS\_OUTPUTXBAR9\_G1 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR9_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR9_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR9_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR9_G1_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3779. CONTROLSS\_OUTPUTXBAR9\_G1 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR9_G1_SEL | R/W  | 0h    | G1: OUTPUT XBAR9 G1 input bit select. Input source is PWM[x].SOCA<br>1:PWM[x] SOCA selected<br>0:PWM[x] SOCA is de-selected |

### 3.18.2.111 CONTROLSS\_OUTPUTXBAR9\_G2 Register

#### 1 CONTROLSS\_OUTPUTXBAR9\_G2 Register (Offset = 348h) [reset = 0h]

OUTPUT XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-3780. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8348h       |

**Figure 3-1236. CONTROLSS\_OUTPUTXBAR9\_G2 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR9_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR9_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR9_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR9_G2_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3782. CONTROLSS\_OUTPUTXBAR9\_G2 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR9_G2_SEL | R/W  | 0h    | G2: OUTPUT XBAR9 G2 input bit select. Input source is PWM[x].SOCB<br>1:PWM[x] SOCB selected<br>0:PWM[x] SOCB is de-selected |

### 3.18.2.112 CONTROLSS\_OUTPUTXBAR9\_G3 Register

#### 1 CONTROLSS\_OUTPUTXBAR9\_G3 Register (Offset = 34Ch) [reset = 0h]

OUTPUT XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-3783. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 834Ch       |

**Figure 3-1237. CONTROLSS\_OUTPUTXBAR9\_G3 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR9_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR9_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR9_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR9_G3_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3785. CONTROLSS\_OUTPUTXBAR9\_G3 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                       |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR9_G3_SEL | R/W  | 0h    | G3: OUTPUT XBAR9 G3 input bit select. Input source is DEL[x].ACTIVE<br>1:DEL[x] ACTIVE selected<br>0:DEL[x] ACTIVE is de-selected |

### 3.18.2.113 CONTROLSS\_OUTPUTXBAR9\_G4 Register

#### 1 CONTROLSS\_OUTPUTXBAR9\_G4 Register (Offset = 350h) [reset = 0h]

OUTPUT XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-3786. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8350h       |

**Figure 3-1238. CONTROLSS\_OUTPUTXBAR9\_G4 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR9_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR9_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR9_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR9_G4_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3788. CONTROLSS\_OUTPUTXBAR9\_G4 Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                 |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR9_G4_SEL | R/W  | 0h    | G4: OUTPUT XBAR9 G4 input bit select. Input source is DEL[x].TRIP<br>1:DEL[x] TRIP selected<br>0:DEL[x] TRIP is de-selected |

### 3.18.2.114 CONTROLSS\_OUTPUTXBAR9\_G5 Register

#### 1 CONTROLSS\_OUTPUTXBAR9\_G5 Register (Offset = 354h) [reset = 0h]

OUTPUT XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-3789. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8354h       |

**Figure 3-1239. CONTROLSS\_OUTPUTXBAR9\_G5 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR9_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR9_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR9_G5_SEL |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 3-3791. CONTROLSS\_OUTPUTXBAR9\_G5 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3791. CONTROLSS\_OUTPUTXBAR9\_G5 Register Field Descriptions (continued)**

| Bit  | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------|--------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | OUTPUTXBAR9_G5_SEL | R/W  | 0h    | G5: OUTPUT XBAR9 G5 input bit select.<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.18.2.115 CONTROLSS\_OUTPUTXBAR9\_G6 Register

#### 1 CONTROLSS\_OUTPUTXBAR9\_G6 Register (Offset = 358h) [reset = 0h]

OUTPUT XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-3792. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8358h       |

**Figure 3-1240. CONTROLSS\_OUTPUTXBAR9\_G6 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR9_G6_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR9_G6_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR9_G6_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3794. CONTROLSS\_OUTPUTXBAR9\_G6 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 19:0  | OUTPUTXBAR9_G6_SEL | R/W  | 0h    | G6: OUTPUT XBAR9 G6 Input Select<br>0: CMPSSA0.CTRIPOUTL<br>1: CMPSSA0.CTRIPOUTH<br>2: CMPSSA1.CTRIPOUTL<br>3: CMPSSA1.CTRIPOUTH<br>4: CMPSSA2.CTRIPOUTL<br>5: CMPSSA2.CTRIPOUTH<br>6: CMPSSA3.CTRIPOUTL<br>7: CMPSSA3.CTRIPOUTH<br>8: CMPSSA4.CTRIPOUTL<br>9: CMPSSA4.CTRIPOUTH<br>10: CMPSSA5.CTRIPOUTL<br>11: CMPSSA5.CTRIPOUTH<br>12: CMPSSA6.CTRIPOUTL<br>13: CMPSSA6.CTRIPOUTH<br>14: CMPSSA7.CTRIPOUTL<br>15: CMPSSA7.CTRIPOUTH<br>16: CMPSSA8.CTRIPOUTL<br>17: CMPSSA8.CTRIPOUTH<br>18: CMPSSA9.CTRIPOUTL<br>19: CMPSSA9.CTRIPOUTH |

### 3.18.2.116 CONTROLSS\_OUTPUTXBAR9\_G7 Register

#### 1 CONTROLSS\_OUTPUTXBAR9\_G7 Register (Offset = 35Ch) [reset = 0h]

OUTPUT XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-3795. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 835Ch       |

**Figure 3-1241. CONTROLSS\_OUTPUTXBAR9\_G7 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR9_G7_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR9_G7_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR9_G7_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3797. CONTROLSS\_OUTPUTXBAR9\_G7 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 19:0  | OUTPUTXBAR9_G7_SEL | R/W  | 0h    | G7: OUTPUT XBAR9 G7 Input Select<br>0: CMPSSB0.CTRIPOUTL<br>1: CMPSSB0.CTRIPOUTH<br>2: CMPSSB1.CTRIPOUTL<br>3: CMPSSB1.CTRIPOUTH<br>4: CMPSSB2.CTRIPOUTL<br>5: CMPSSB2.CTRIPOUTH<br>6: CMPSSB3.CTRIPOUTL<br>7: CMPSSB3.CTRIPOUTH<br>8: CMPSSB4.CTRIPOUTL<br>9: CMPSSB4.CTRIPOUTH<br>10: CMPSSB5.CTRIPOUTL<br>11: CMPSSB5.CTRIPOUTH<br>12: CMPSSB6.CTRIPOUTL<br>13: CMPSSB6.CTRIPOUTH<br>14: CMPSSB7.CTRIPOUTL<br>15: CMPSSB7.CTRIPOUTH<br>16: CMPSSB8.CTRIPOUTL<br>17: CMPSSB8.CTRIPOUTH<br>18: CMPSSB9.CTRIPOUTL<br>19: CMPSSB9.CTRIPOUTH |



### 3.18.2.117 CONTROLSS\_OUTPUTXBAR9\_G8 Register

#### 1 CONTROLSS\_OUTPUTXBAR9\_G8 Register (Offset = 360h) [reset = 0h]

OUTPUT XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-3798. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8360h       |

**Figure 3-1242. CONTROLSS\_OUTPUTXBAR9\_G8 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR9_G8_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR9_G8_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR9_G8_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3800. CONTROLSS\_OUTPUTXBAR9\_G8 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                            |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                               |
| 19:0  | OUTPUTXBAR9_G8_SEL | R/W  | 0h    | G8: OUTPUT XBAR9 G8 Input Select<br>0:ADC0.EVT1<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.18.2.118 CONTROLSS\_OUTPUTXBAR9\_G9 Register

#### 1 CONTROLSS\_OUTPUTXBAR9\_G9 Register (Offset = 364h) [reset = 0h]

OUTPUT XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-3801. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8364h       |

**Figure 3-1243. CONTROLSS\_OUTPUTXBAR9\_G9 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED           |    |    |    |                    |    |    |    |
| NONE               |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED           |    |    |    | OUTPUTXBAR9_G9_SEL |    |    |    |
| NONE               |    |    |    | R/W                |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| OUTPUTXBAR9_G9_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| OUTPUTXBAR9_G9_SEL |    |    |    |                    |    |    |    |
| R/W                |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 3-3803. CONTROLSS\_OUTPUTXBAR9\_G9 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|--------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                               |
| 19:0  | OUTPUTXBAR9_G9_SEL | R/W  | 0h    | G9: OUTPUT XBAR9 G9 Input Select<br>0:PWMSyncOutXBAR.SYNCOU0<br>1:PWMSyncOutXBAR.SYNCOU1<br>2:PWMSyncOutXBAR.SYNCOU2<br>3:PWMSyncOutXBAR.SYNCOU3<br>4:EQEP0.I_OUT<br>5:EQEP0.S_OUT<br>6:EQEP1.I_OUT<br>7:EQEP1.S_OUT<br>8:EQEP2.I_OUT<br>9:EQEP2.S_OUT<br>10:ECAP0.OUT<br>11:ECAP1.OUT<br>12:ECAP2.OUT<br>13:ECAP3.OUT<br>14:ECAP4.OUT<br>15:ECAP5.OUT<br>16:ECAP6.OUT<br>17:ECAP7.OUT<br>18:ECAP8.OUT<br>19:ECAP9.OUT |

### 3.18.2.119 CONTROLSS\_OUTPUTXBAR9\_G10 Register

#### 1 CONTROLSS\_OUTPUTXBAR9\_G10 Register (Offset = 368h) [reset = 0h]

OUTPUT XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-3804. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8368h       |

**Figure 3-1244. CONTROLSS\_OUTPUTXBAR9\_G10 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR9_G10_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR9_G10_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3806. CONTROLSS\_OUTPUTXBAR9\_G10 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                   |
|-------|---------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                      |
| 15:0  | OUTPUTXBAR9_G10_SEL | R/W  | 0h    | G10: OUTPUT XBAR9 G10 Input Select<br>3<br>0:FSIRX0.RX_TRIG0<br>7<br>4:FSIRX1.RX_TRIG0<br>11<br>8:FSIRX2.RX_TRIG0<br>15<br>12:FSIRX3.RX_TRIG0 |

### 3.18.2.120 CONTROLSS\_OUTPUTXBAR10\_G0 Register

#### 1 CONTROLSS\_OUTPUTXBAR10\_G0 Register (Offset = 380h) [reset = 0h]

OUTPUT XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-3807. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8380h       |

**Figure 3-1245. CONTROLSS\_OUTPUTXBAR10\_G0 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR10_G0_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR10_G0_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR10_G0_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR10_G0_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3809. CONTROLSS\_OUTPUTXBAR10\_G0 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                        |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR10_G0_SEL | R/W  | 0h    | G0: PWM XBAR10 G0 input bit select. Input source is PWM[x].TRIPOUT<br>1:PWM[x] TRIPOUT selected<br>0:PWM[x] TRIPOUT is de-selected |

### 3.18.2.121 CONTROLSS\_OUTPUTXBAR10\_G1 Register

#### 1 CONTROLSS\_OUTPUTXBAR10\_G1 Register (Offset = 384h) [reset = 0h]

OUTPUT XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-3810. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8384h       |

**Figure 3-1246. CONTROLSS\_OUTPUTXBAR10\_G1 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR10_G1_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR10_G1_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR10_G1_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR10_G1_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3812. CONTROLSS\_OUTPUTXBAR10\_G1 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                  |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR10_G1_SEL | R/W  | 0h    | G1: OUTPUT XBAR10 G1 input bit select. Input source is PWM[x].SOCA<br>1:PWM[x] SOCA selected<br>0:PWM[x] SOCA is de-selected |

### 3.18.2.122 CONTROLSS\_OUTPUTXBAR10\_G2 Register

#### 1 CONTROLSS\_OUTPUTXBAR10\_G2 Register (Offset = 388h) [reset = 0h]

OUTPUT XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-3813. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8388h       |

**Figure 3-1247. CONTROLSS\_OUTPUTXBAR10\_G2 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR10_G2_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR10_G2_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR10_G2_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR10_G2_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3815. CONTROLSS\_OUTPUTXBAR10\_G2 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                  |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR10_G2_SEL | R/W  | 0h    | G2: OUTPUT XBAR10 G2 input bit select. Input source is PWM[x].SOCB<br>1:PWM[x] SOCB selected<br>0:PWM[x] SOCB is de-selected |

### 3.18.2.123 CONTROLSS\_OUTPUTXBAR10\_G3 Register

#### 1 CONTROLSS\_OUTPUTXBAR10\_G3 Register (Offset = 38Ch) [reset = 0h]

OUTPUT XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-3816. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 838Ch       |

**Figure 3-1248. CONTROLSS\_OUTPUTXBAR10\_G3 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR10_G3_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR10_G3_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR10_G3_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR10_G3_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3818. CONTROLSS\_OUTPUTXBAR10\_G3 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                        |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR10_G3_SEL | R/W  | 0h    | G3: OUTPUT XBAR10 G3 input bit select. Input source is DEL[x].ACTIVE<br>1:DEL[x] ACTIVE selected<br>0:DEL[x] ACTIVE is de-selected |

### 3.18.2.124 CONTROLSS\_OUTPUTXBAR10\_G4 Register

#### 1 CONTROLSS\_OUTPUTXBAR10\_G4 Register (Offset = 390h) [reset = 0h]

OUTPUT XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-3819. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8390h       |

**Figure 3-1249. CONTROLSS\_OUTPUTXBAR10\_G4 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR10_G4_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR10_G4_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR10_G4_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR10_G4_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3821. CONTROLSS\_OUTPUTXBAR10\_G4 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                  |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR10_G4_SEL | R/W  | 0h    | G4: OUTPUT XBAR10 G4 input bit select. Input source is DEL[x].TRIP<br>1:DEL[x] TRIP selected<br>0:DEL[x] TRIP is de-selected |



### 3.18.2.125 CONTROLSS\_OUTPUTXBAR10\_G5 Register

#### 1 CONTROLSS\_OUTPUTXBAR10\_G5 Register (Offset = 394h) [reset = 0h]

OUTPUT XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-3822. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8394h       |

**Figure 3-1250. CONTROLSS\_OUTPUTXBAR10\_G5 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR10_G5_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR10_G5_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR10_G5_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3824. CONTROLSS\_OUTPUTXBAR10\_G5 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3824. CONTROLSS\_OUTPUTXBAR10\_G5 Register Field Descriptions (continued)**

| Bit  | Field                   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|-------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | OUTPUTXBAR10_G5_SE<br>L | R/W  | 0h    | G5: OUTPUT XBAR10 G5 input bit select.<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.18.2.126 CONTROLSS\_OUTPUTXBAR10\_G6 Register

#### 1 CONTROLSS\_OUTPUTXBAR10\_G6 Register (Offset = 398h) [reset = 0h]

OUTPUT XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-3825. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8398h       |

**Figure 3-1251. CONTROLSS\_OUTPUTXBAR10\_G6 Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    | OUTPUTXBAR10_G6_SEL |    |    |    |
| NONE                |    |    |    | R/W                 |    |    |    |
| 0h                  |    |    |    | 0h                  |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| OUTPUTXBAR10_G6_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| OUTPUTXBAR10_G6_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |

**Table 3-3827. CONTROLSS\_OUTPUTXBAR10\_G6 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 19:0  | OUTPUTXBAR10_G6_SEL | R/W  | 0h    | G6: OUTPUT XBAR10 G6 Input Select<br>0: CMPSSA0.CTRIPOUTL<br>1: CMPSSA0.CTRIPOUTH<br>2: CMPSSA1.CTRIPOUTL<br>3: CMPSSA1.CTRIPOUTH<br>4: CMPSSA2.CTRIPOUTL<br>5: CMPSSA2.CTRIPOUTH<br>6: CMPSSA3.CTRIPOUTL<br>7: CMPSSA3.CTRIPOUTH<br>8: CMPSSA4.CTRIPOUTL<br>9: CMPSSA4.CTRIPOUTH<br>10: CMPSSA5.CTRIPOUTL<br>11: CMPSSA5.CTRIPOUTH<br>12: CMPSSA6.CTRIPOUTL<br>13: CMPSSA6.CTRIPOUTH<br>14: CMPSSA7.CTRIPOUTL<br>15: CMPSSA7.CTRIPOUTH<br>16: CMPSSA8.CTRIPOUTL<br>17: CMPSSA8.CTRIPOUTH<br>18: CMPSSA9.CTRIPOUTL<br>19: CMPSSA9.CTRIPOUTH |

### 3.18.2.127 CONTROLSS\_OUTPUTXBAR10\_G7 Register

#### 1 CONTROLSS\_OUTPUTXBAR10\_G7 Register (Offset = 39Ch) [reset = 0h]

OUTPUT XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-3828. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 839Ch       |

**Figure 3-1252. CONTROLSS\_OUTPUTXBAR10\_G7 Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    | OUTPUTXBAR10_G7_SEL |    |    |    |
| NONE                |    |    |    | R/W                 |    |    |    |
| 0h                  |    |    |    | 0h                  |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| OUTPUTXBAR10_G7_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| OUTPUTXBAR10_G7_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |

**Table 3-3830. CONTROLSS\_OUTPUTXBAR10\_G7 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 19:0  | OUTPUTXBAR10_G7_SEL | R/W  | 0h    | G7: OUTPUT XBAR10 G7 Input Select<br>0: CMPSSB0.CTRIPOUTL<br>1: CMPSSB0.CTRIPOUTH<br>2: CMPSSB1.CTRIPOUTL<br>3: CMPSSB1.CTRIPOUTH<br>4: CMPSSB2.CTRIPOUTL<br>5: CMPSSB2.CTRIPOUTH<br>6: CMPSSB3.CTRIPOUTL<br>7: CMPSSB3.CTRIPOUTH<br>8: CMPSSB4.CTRIPOUTL<br>9: CMPSSB4.CTRIPOUTH<br>10: CMPSSB5.CTRIPOUTL<br>11: CMPSSB5.CTRIPOUTH<br>12: CMPSSB6.CTRIPOUTL<br>13: CMPSSB6.CTRIPOUTH<br>14: CMPSSB7.CTRIPOUTL<br>15: CMPSSB7.CTRIPOUTH<br>16: CMPSSB8.CTRIPOUTL<br>17: CMPSSB8.CTRIPOUTH<br>18: CMPSSB9.CTRIPOUTL<br>19: CMPSSB9.CTRIPOUTH |

### 3.18.2.128 CONTROLSS\_OUTPUTXBAR10\_G8 Register

#### 1 CONTROLSS\_OUTPUTXBAR10\_G8 Register (Offset = 3A0h) [reset = 0h]

OUTPUT XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-3831. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 83A0h       |

**Figure 3-1253. CONTROLSS\_OUTPUTXBAR10\_G8 Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    | OUTPUTXBAR10_G8_SEL |    |    |    |
| NONE                |    |    |    | R/W                 |    |    |    |
| 0h                  |    |    |    | 0h                  |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| OUTPUTXBAR10_G8_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| OUTPUTXBAR10_G8_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |

**Table 3-3833. CONTROLSS\_OUTPUTXBAR10\_G8 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                             |
|-------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | OUTPUTXBAR10_G8_SEL | R/W  | 0h    | G8: OUTPUT XBAR10 G8 Input Select<br>0:ADC0.EVT1<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.18.2.129 CONTROLSS\_OUTPUTXBAR10\_G9 Register

#### 1 CONTROLSS\_OUTPUTXBAR10\_G9 Register (Offset = 3A4h) [reset = 0h]

OUTPUT XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-3834. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 83A4h       |

**Figure 3-1254. CONTROLSS\_OUTPUTXBAR10\_G9 Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    | OUTPUTXBAR10_G9_SEL |    |    |    |
| NONE                |    |    |    | R/W                 |    |    |    |
| 0h                  |    |    |    | 0h                  |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| OUTPUTXBAR10_G9_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| OUTPUTXBAR10_G9_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |

**Table 3-3836. CONTROLSS\_OUTPUTXBAR10\_G9 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|---------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | OUTPUTXBAR10_G9_SEL | R/W  | 0h    | G9: OUTPUT XBAR10 G9 Input Select<br>0:PWMSyncOutXBAR.SYNCOU0<br>1:PWMSyncOutXBAR.SYNCOU1<br>2:PWMSyncOutXBAR.SYNCOU2<br>3:PWMSyncOutXBAR.SYNCOU3<br>4:EQEP0.I_OUT<br>5:EQEP0.S_OUT<br>6:EQEP1.I_OUT<br>7:EQEP1.S_OUT<br>8:EQEP2.I_OUT<br>9:EQEP2.S_OUT<br>10:ECAP0.OUT<br>11:ECAP1.OUT<br>12:ECAP2.OUT<br>13:ECAP3.OUT<br>14:ECAP4.OUT<br>15:ECAP5.OUT<br>16:ECAP6.OUT<br>17:ECAP7.OUT<br>18:ECAP8.OUT<br>19:ECAP9.OUT |

### 3.18.2.130 CONTROLSS\_OUTPUTXBAR10\_G10 Register

#### 1 CONTROLSS\_OUTPUTXBAR10\_G10 Register (Offset = 3A8h) [reset = 0h]

OUTPUT XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-3837. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 83A8h       |

**Figure 3-1255. CONTROLSS\_OUTPUTXBAR10\_G10 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR10_G10_SEL |    |    |    |    |    |    |    |
| R/W                  |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR10_G10_SEL |    |    |    |    |    |    |    |
| R/W                  |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 3-3839. CONTROLSS\_OUTPUTXBAR10\_G10 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description                                                                                                                                    |
|-------|----------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED             | NONE | 0h    | Reserved                                                                                                                                       |
| 15:0  | OUTPUTXBAR10_G10_SEL | R/W  | 0h    | G10: OUTPUT XBAR10 G10 Input Select<br>3<br>0:FSIRX0.RX_TRIG0<br>7<br>4:FSIRX1.RX_TRIG0<br>11<br>8:FSIRX2.RX_TRIG0<br>15<br>12:FSIRX3.RX_TRIG0 |

### 3.18.2.131 CONTROLSS\_OUTPUTXBAR11\_G0 Register

#### 1 CONTROLSS\_OUTPUTXBAR11\_G0 Register (Offset = 3C0h) [reset = 0h]

OUTPUT XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-3840. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 83C0h       |

**Figure 3-1256. CONTROLSS\_OUTPUTXBAR11\_G0 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR11_G0_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR11_G0_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR11_G0_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR11_G0_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3842. CONTROLSS\_OUTPUTXBAR11\_G0 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                        |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR11_G0_SEL | R/W  | 0h    | G0: PWM XBAR11 G0 input bit select. Input source is PWM[x].TRIPOUT<br>1:PWM[x] TRIPOUT selected<br>0:PWM[x] TRIPOUT is de-selected |



### 3.18.2.132 CONTROLSS\_OUTPUTXBAR11\_G1 Register

#### 1 CONTROLSS\_OUTPUTXBAR11\_G1 Register (Offset = 3C4h) [reset = 0h]

OUTPUT XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-3843. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 83C4h       |

**Figure 3-1257. CONTROLSS\_OUTPUTXBAR11\_G1 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR11_G1_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR11_G1_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR11_G1_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR11_G1_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3845. CONTROLSS\_OUTPUTXBAR11\_G1 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                  |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR11_G1_SEL | R/W  | 0h    | G1: OUTPUT XBAR11 G1 input bit select. Input source is PWM[x].SOCA<br>1:PWM[x] SOCA selected<br>0:PWM[x] SOCA is de-selected |

### 3.18.2.133 CONTROLSS\_OUTPUTXBAR11\_G2 Register

#### 1 CONTROLSS\_OUTPUTXBAR11\_G2 Register (Offset = 3C8h) [reset = 0h]

OUTPUT XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-3846. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 83C8h       |

**Figure 3-1258. CONTROLSS\_OUTPUTXBAR11\_G2 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR11_G2_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR11_G2_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR11_G2_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR11_G2_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3848. CONTROLSS\_OUTPUTXBAR11\_G2 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                  |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR11_G2_SEL | R/W  | 0h    | G2: OUTPUT XBAR11 G2 input bit select. Input source is PWM[x].SOCB<br>1:PWM[x] SOCB selected<br>0:PWM[x] SOCB is de-selected |

### 3.18.2.134 CONTROLSS\_OUTPUTXBAR11\_G3 Register

#### 1 CONTROLSS\_OUTPUTXBAR11\_G3 Register (Offset = 3CCh) [reset = 0h]

OUTPUT XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-3849. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 83CCh       |

**Figure 3-1259. CONTROLSS\_OUTPUTXBAR11\_G3 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR11_G3_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR11_G3_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR11_G3_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR11_G3_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3851. CONTROLSS\_OUTPUTXBAR11\_G3 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                        |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR11_G3_SEL | R/W  | 0h    | G3: OUTPUT XBAR11 G3 input bit select. Input source is DEL[x].ACTIVE<br>1:DEL[x] ACTIVE selected<br>0:DEL[x] ACTIVE is de-selected |

### 3.18.2.135 CONTROLSS\_OUTPUTXBAR11\_G4 Register

#### 1 CONTROLSS\_OUTPUTXBAR11\_G4 Register (Offset = 3D0h) [reset = 0h]

OUTPUT XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-3852. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 83D0h       |

**Figure 3-1260. CONTROLSS\_OUTPUTXBAR11\_G4 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR11_G4_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR11_G4_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR11_G4_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR11_G4_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3854. CONTROLSS\_OUTPUTXBAR11\_G4 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                  |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR11_G4_SEL | R/W  | 0h    | G4: OUTPUT XBAR11 G4 input bit select. Input source is DEL[x].TRIP<br>1:DEL[x] TRIP selected<br>0:DEL[x] TRIP is de-selected |

### 3.18.2.136 CONTROLSS\_OUTPUTXBAR11\_G5 Register

#### 1 CONTROLSS\_OUTPUTXBAR11\_G5 Register (Offset = 3D4h) [reset = 0h]

OUTPUT XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-3855. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 83D4h       |

**Figure 3-1261. CONTROLSS\_OUTPUTXBAR11\_G5 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR11_G5_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR11_G5_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR11_G5_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3857. CONTROLSS\_OUTPUTXBAR11\_G5 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3857. CONTROLSS\_OUTPUTXBAR11\_G5 Register Field Descriptions (continued)**

| Bit  | Field                   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|-------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | OUTPUTXBAR11_G5_SE<br>L | R/W  | 0h    | G5: OUTPUT XBAR11 G5 input bit select.<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.18.2.137 CONTROLSS\_OUTPUTXBAR11\_G6 Register

#### 1 CONTROLSS\_OUTPUTXBAR11\_G6 Register (Offset = 3D8h) [reset = 0h]

OUTPUT XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-3858. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 83D8h       |

**Figure 3-1262. CONTROLSS\_OUTPUTXBAR11\_G6 Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    | OUTPUTXBAR11_G6_SEL |    |    |    |
| NONE                |    |    |    | R/W                 |    |    |    |
| 0h                  |    |    |    | 0h                  |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| OUTPUTXBAR11_G6_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| OUTPUTXBAR11_G6_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |

**Table 3-3860. CONTROLSS\_OUTPUTXBAR11\_G6 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 19:0  | OUTPUTXBAR11_G6_SEL | R/W  | 0h    | G6: OUTPUT XBAR11 G6 Input Select<br>0: CMPSSA0.CTRIPOUTL<br>1: CMPSSA0.CTRIPOUTH<br>2: CMPSSA1.CTRIPOUTL<br>3: CMPSSA1.CTRIPOUTH<br>4: CMPSSA2.CTRIPOUTL<br>5: CMPSSA2.CTRIPOUTH<br>6: CMPSSA3.CTRIPOUTL<br>7: CMPSSA3.CTRIPOUTH<br>8: CMPSSA4.CTRIPOUTL<br>9: CMPSSA4.CTRIPOUTH<br>10: CMPSSA5.CTRIPOUTL<br>11: CMPSSA5.CTRIPOUTH<br>12: CMPSSA6.CTRIPOUTL<br>13: CMPSSA6.CTRIPOUTH<br>14: CMPSSA7.CTRIPOUTL<br>15: CMPSSA7.CTRIPOUTH<br>16: CMPSSA8.CTRIPOUTL<br>17: CMPSSA8.CTRIPOUTH<br>18: CMPSSA9.CTRIPOUTL<br>19: CMPSSA9.CTRIPOUTH |

### 3.18.2.138 CONTROLSS\_OUTPUTXBAR11\_G7 Register

#### 1 CONTROLSS\_OUTPUTXBAR11\_G7 Register (Offset = 3DCh) [reset = 0h]

OUTPUT XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-3861. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 83DCh       |

**Figure 3-1263. CONTROLSS\_OUTPUTXBAR11\_G7 Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    | OUTPUTXBAR11_G7_SEL |    |    |    |
| NONE                |    |    |    | R/W                 |    |    |    |
| 0h                  |    |    |    | 0h                  |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| OUTPUTXBAR11_G7_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| OUTPUTXBAR11_G7_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |

**Table 3-3863. CONTROLSS\_OUTPUTXBAR11\_G7 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 19:0  | OUTPUTXBAR11_G7_SEL | R/W  | 0h    | G7: OUTPUT XBAR11 G7 Input Select<br>0: CMPSSB0.CTRIPOUTL<br>1: CMPSSB0.CTRIPOUTH<br>2: CMPSSB1.CTRIPOUTL<br>3: CMPSSB1.CTRIPOUTH<br>4: CMPSSB2.CTRIPOUTL<br>5: CMPSSB2.CTRIPOUTH<br>6: CMPSSB3.CTRIPOUTL<br>7: CMPSSB3.CTRIPOUTH<br>8: CMPSSB4.CTRIPOUTL<br>9: CMPSSB4.CTRIPOUTH<br>10: CMPSSB5.CTRIPOUTL<br>11: CMPSSB5.CTRIPOUTH<br>12: CMPSSB6.CTRIPOUTL<br>13: CMPSSB6.CTRIPOUTH<br>14: CMPSSB7.CTRIPOUTL<br>15: CMPSSB7.CTRIPOUTH<br>16: CMPSSB8.CTRIPOUTL<br>17: CMPSSB8.CTRIPOUTH<br>18: CMPSSB9.CTRIPOUTL<br>19: CMPSSB9.CTRIPOUTH |



### 3.18.2.139 CONTROLSS\_OUTPUTXBAR11\_G8 Register

#### 1 CONTROLSS\_OUTPUTXBAR11\_G8 Register (Offset = 3E0h) [reset = 0h]

OUTPUT XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-3864. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 83E0h       |

**Figure 3-1264. CONTROLSS\_OUTPUTXBAR11\_G8 Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    | OUTPUTXBAR11_G8_SEL |    |    |    |
| NONE                |    |    |    | R/W                 |    |    |    |
| 0h                  |    |    |    | 0h                  |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| OUTPUTXBAR11_G8_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| OUTPUTXBAR11_G8_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |

**Table 3-3866. CONTROLSS\_OUTPUTXBAR11\_G8 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                             |
|-------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | OUTPUTXBAR11_G8_SEL | R/W  | 0h    | G8: OUTPUT XBAR11 G8 Input Select<br>0:ADC0.EVT1<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.18.2.140 CONTROLSS\_OUTPUTXBAR11\_G9 Register

#### 1 CONTROLSS\_OUTPUTXBAR11\_G9 Register (Offset = 3E4h) [reset = 0h]

OUTPUT XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-3867. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 83E4h       |

**Figure 3-1265. CONTROLSS\_OUTPUTXBAR11\_G9 Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    | OUTPUTXBAR11_G9_SEL |    |    |    |
| NONE                |    |    |    | R/W                 |    |    |    |
| 0h                  |    |    |    | 0h                  |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| OUTPUTXBAR11_G9_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| OUTPUTXBAR11_G9_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |

**Table 3-3869. CONTROLSS\_OUTPUTXBAR11\_G9 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|---------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | OUTPUTXBAR11_G9_SEL | R/W  | 0h    | G9: OUTPUT XBAR11 G9 Input Select<br>0:PWMSyncOutXBAR.SYNCOU0<br>1:PWMSyncOutXBAR.SYNCOU1<br>2:PWMSyncOutXBAR.SYNCOU2<br>3:PWMSyncOutXBAR.SYNCOU3<br>4:EQEP0.I_OUT<br>5:EQEP0.S_OUT<br>6:EQEP1.I_OUT<br>7:EQEP1.S_OUT<br>8:EQEP2.I_OUT<br>9:EQEP2.S_OUT<br>10:ECAP0.OUT<br>11:ECAP1.OUT<br>12:ECAP2.OUT<br>13:ECAP3.OUT<br>14:ECAP4.OUT<br>15:ECAP5.OUT<br>16:ECAP6.OUT<br>17:ECAP7.OUT<br>18:ECAP8.OUT<br>19:ECAP9.OUT |

### 3.18.2.141 CONTROLSS\_OUTPUTXBAR11\_G10 Register

#### 1 CONTROLSS\_OUTPUTXBAR11\_G10 Register (Offset = 3E8h) [reset = 0h]

OUTPUT XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-3870. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 83E8h       |

**Figure 3-1266. CONTROLSS\_OUTPUTXBAR11\_G10 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR11_G10_SEL |    |    |    |    |    |    |    |
| R/W                  |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR11_G10_SEL |    |    |    |    |    |    |    |
| R/W                  |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 3-3872. CONTROLSS\_OUTPUTXBAR11\_G10 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description                                                                                                                                    |
|-------|----------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED             | NONE | 0h    | Reserved                                                                                                                                       |
| 15:0  | OUTPUTXBAR11_G10_SEL | R/W  | 0h    | G10: OUTPUT XBAR11 G10 Input Select<br>3<br>0:FSIRX0.RX_TRIG0<br>7<br>4:FSIRX1.RX_TRIG0<br>11<br>8:FSIRX2.RX_TRIG0<br>15<br>12:FSIRX3.RX_TRIG0 |

### 3.18.2.142 CONTROLSS\_OUTPUTXBAR12\_G0 Register

#### 1 CONTROLSS\_OUTPUTXBAR12\_G0 Register (Offset = 400h) [reset = 0h]

OUTPUT XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-3873. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8400h       |

**Figure 3-1267. CONTROLSS\_OUTPUTXBAR12\_G0 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR12_G0_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR12_G0_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR12_G0_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR12_G0_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3875. CONTROLSS\_OUTPUTXBAR12\_G0 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                        |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR12_G0_SEL | R/W  | 0h    | G0: PWM XBAR12 G0 input bit select. Input source is PWM[x].TRIPOUT<br>1:PWM[x] TRIPOUT selected<br>0:PWM[x] TRIPOUT is de-selected |

### 3.18.2.143 CONTROLSS\_OUTPUTXBAR12\_G1 Register

#### 1 CONTROLSS\_OUTPUTXBAR12\_G1 Register (Offset = 404h) [reset = 0h]

OUTPUT XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-3876. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8404h       |

**Figure 3-1268. CONTROLSS\_OUTPUTXBAR12\_G1 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR12_G1_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR12_G1_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR12_G1_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR12_G1_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3878. CONTROLSS\_OUTPUTXBAR12\_G1 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                  |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR12_G1_SEL | R/W  | 0h    | G1: OUTPUT XBAR12 G1 input bit select. Input source is PWM[x].SOCA<br>1:PWM[x] SOCA selected<br>0:PWM[x] SOCA is de-selected |

### 3.18.2.144 CONTROLSS\_OUTPUTXBAR12\_G2 Register

#### 1 CONTROLSS\_OUTPUTXBAR12\_G2 Register (Offset = 408h) [reset = 0h]

OUTPUT XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-3879. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8408h       |

**Figure 3-1269. CONTROLSS\_OUTPUTXBAR12\_G2 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR12_G2_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR12_G2_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR12_G2_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR12_G2_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3881. CONTROLSS\_OUTPUTXBAR12\_G2 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                  |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR12_G2_SEL | R/W  | 0h    | G2: OUTPUT XBAR12 G2 input bit select. Input source is PWM[x].SOCB<br>1:PWM[x] SOCB selected<br>0:PWM[x] SOCB is de-selected |

### 3.18.2.145 CONTROLSS\_OUTPUTXBAR12\_G3 Register

#### 1 CONTROLSS\_OUTPUTXBAR12\_G3 Register (Offset = 40Ch) [reset = 0h]

OUTPUT XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-3882. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 840Ch       |

**Figure 3-1270. CONTROLSS\_OUTPUTXBAR12\_G3 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR12_G3_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR12_G3_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR12_G3_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR12_G3_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3884. CONTROLSS\_OUTPUTXBAR12\_G3 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                        |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR12_G3_SEL | R/W  | 0h    | G3: OUTPUT XBAR12 G3 input bit select. Input source is DEL[x].ACTIVE<br>1:DEL[x] ACTIVE selected<br>0:DEL[x] ACTIVE is de-selected |

### 3.18.2.146 CONTROLSS\_OUTPUTXBAR12\_G4 Register

#### 1 CONTROLSS\_OUTPUTXBAR12\_G4 Register (Offset = 410h) [reset = 0h]

OUTPUT XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-3885. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8410h       |

**Figure 3-1271. CONTROLSS\_OUTPUTXBAR12\_G4 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR12_G4_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR12_G4_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR12_G4_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR12_G4_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3887. CONTROLSS\_OUTPUTXBAR12\_G4 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                  |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR12_G4_SEL | R/W  | 0h    | G4: OUTPUT XBAR12 G4 input bit select. Input source is DEL[x].TRIP<br>1:DEL[x] TRIP selected<br>0:DEL[x] TRIP is de-selected |



### 3.18.2.147 CONTROLSS\_OUTPUTXBAR12\_G5 Register

#### 1 CONTROLSS\_OUTPUTXBAR12\_G5 Register (Offset = 414h) [reset = 0h]

OUTPUT XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-3888. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8414h       |

**Figure 3-1272. CONTROLSS\_OUTPUTXBAR12\_G5 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR12_G5_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR12_G5_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR12_G5_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3890. CONTROLSS\_OUTPUTXBAR12\_G5 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3890. CONTROLSS\_OUTPUTXBAR12\_G5 Register Field Descriptions (continued)**

| Bit  | Field                   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|-------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | OUTPUTXBAR12_G5_SE<br>L | R/W  | 0h    | G5: OUTPUT XBAR12 G5 input bit select.<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.18.2.148 CONTROLSS\_OUTPUTXBAR12\_G6 Register

#### 1 CONTROLSS\_OUTPUTXBAR12\_G6 Register (Offset = 418h) [reset = 0h]

OUTPUT XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-3891. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8418h       |

**Figure 3-1273. CONTROLSS\_OUTPUTXBAR12\_G6 Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    | OUTPUTXBAR12_G6_SEL |    |    |    |
| NONE                |    |    |    | R/W                 |    |    |    |
| 0h                  |    |    |    | 0h                  |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| OUTPUTXBAR12_G6_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| OUTPUTXBAR12_G6_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |

**Table 3-3893. CONTROLSS\_OUTPUTXBAR12\_G6 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 19:0  | OUTPUTXBAR12_G6_SEL | R/W  | 0h    | G6: OUTPUT XBAR12 G6 Input Select<br>0: CMPSSA0.CTRIPOUTL<br>1: CMPSSA0.CTRIPOUTH<br>2: CMPSSA1.CTRIPOUTL<br>3: CMPSSA1.CTRIPOUTH<br>4: CMPSSA2.CTRIPOUTL<br>5: CMPSSA2.CTRIPOUTH<br>6: CMPSSA3.CTRIPOUTL<br>7: CMPSSA3.CTRIPOUTH<br>8: CMPSSA4.CTRIPOUTL<br>9: CMPSSA4.CTRIPOUTH<br>10: CMPSSA5.CTRIPOUTL<br>11: CMPSSA5.CTRIPOUTH<br>12: CMPSSA6.CTRIPOUTL<br>13: CMPSSA6.CTRIPOUTH<br>14: CMPSSA7.CTRIPOUTL<br>15: CMPSSA7.CTRIPOUTH<br>16: CMPSSA8.CTRIPOUTL<br>17: CMPSSA8.CTRIPOUTH<br>18: CMPSSA9.CTRIPOUTL<br>19: CMPSSA9.CTRIPOUTH |

### 3.18.2.149 CONTROLSS\_OUTPUTXBAR12\_G7 Register

#### 1 CONTROLSS\_OUTPUTXBAR12\_G7 Register (Offset = 41Ch) [reset = 0h]

OUTPUT XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-3894. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 841Ch       |

**Figure 3-1274. CONTROLSS\_OUTPUTXBAR12\_G7 Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    | OUTPUTXBAR12_G7_SEL |    |    |    |
| NONE                |    |    |    | R/W                 |    |    |    |
| 0h                  |    |    |    | 0h                  |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| OUTPUTXBAR12_G7_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| OUTPUTXBAR12_G7_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |

**Table 3-3896. CONTROLSS\_OUTPUTXBAR12\_G7 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 19:0  | OUTPUTXBAR12_G7_SEL | R/W  | 0h    | G7: OUTPUT XBAR12 G7 Input Select<br>0: CMPSSB0.CTRIPOUTL<br>1: CMPSSB0.CTRIPOUTH<br>2: CMPSSB1.CTRIPOUTL<br>3: CMPSSB1.CTRIPOUTH<br>4: CMPSSB2.CTRIPOUTL<br>5: CMPSSB2.CTRIPOUTH<br>6: CMPSSB3.CTRIPOUTL<br>7: CMPSSB3.CTRIPOUTH<br>8: CMPSSB4.CTRIPOUTL<br>9: CMPSSB4.CTRIPOUTH<br>10: CMPSSB5.CTRIPOUTL<br>11: CMPSSB5.CTRIPOUTH<br>12: CMPSSB6.CTRIPOUTL<br>13: CMPSSB6.CTRIPOUTH<br>14: CMPSSB7.CTRIPOUTL<br>15: CMPSSB7.CTRIPOUTH<br>16: CMPSSB8.CTRIPOUTL<br>17: CMPSSB8.CTRIPOUTH<br>18: CMPSSB9.CTRIPOUTL<br>19: CMPSSB9.CTRIPOUTH |

### 3.18.2.150 CONTROLSS\_OUTPUTXBAR12\_G8 Register

#### 1 CONTROLSS\_OUTPUTXBAR12\_G8 Register (Offset = 420h) [reset = 0h]

OUTPUT XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-3897. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8420h       |

**Figure 3-1275. CONTROLSS\_OUTPUTXBAR12\_G8 Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    | OUTPUTXBAR12_G8_SEL |    |    |    |
| NONE                |    |    |    | R/W                 |    |    |    |
| 0h                  |    |    |    | 0h                  |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| OUTPUTXBAR12_G8_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| OUTPUTXBAR12_G8_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |

**Table 3-3899. CONTROLSS\_OUTPUTXBAR12\_G8 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                             |
|-------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | OUTPUTXBAR12_G8_SEL | R/W  | 0h    | G8: OUTPUT XBAR12 G8 Input Select<br>0:ADC0.EVT1<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.18.2.151 CONTROLSS\_OUTPUTXBAR12\_G9 Register

#### 1 CONTROLSS\_OUTPUTXBAR12\_G9 Register (Offset = 424h) [reset = 0h]

OUTPUT XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-3900. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8424h       |

**Figure 3-1276. CONTROLSS\_OUTPUTXBAR12\_G9 Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    | OUTPUTXBAR12_G9_SEL |    |    |    |
| NONE                |    |    |    | R/W                 |    |    |    |
| 0h                  |    |    |    | 0h                  |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| OUTPUTXBAR12_G9_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| OUTPUTXBAR12_G9_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |

**Table 3-3902. CONTROLSS\_OUTPUTXBAR12\_G9 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|---------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | OUTPUTXBAR12_G9_SEL | R/W  | 0h    | G9: OUTPUT XBAR12 G9 Input Select<br>0:PWMSyncOutXBAR.SYNCOU0<br>1:PWMSyncOutXBAR.SYNCOU1<br>2:PWMSyncOutXBAR.SYNCOU2<br>3:PWMSyncOutXBAR.SYNCOU3<br>4:EQEP0.I_OUT<br>5:EQEP0.S_OUT<br>6:EQEP1.I_OUT<br>7:EQEP1.S_OUT<br>8:EQEP2.I_OUT<br>9:EQEP2.S_OUT<br>10:ECAP0.OUT<br>11:ECAP1.OUT<br>12:ECAP2.OUT<br>13:ECAP3.OUT<br>14:ECAP4.OUT<br>15:ECAP5.OUT<br>16:ECAP6.OUT<br>17:ECAP7.OUT<br>18:ECAP8.OUT<br>19:ECAP9.OUT |

### 3.18.2.152 CONTROLSS\_OUTPUTXBAR12\_G10 Register

#### 1 CONTROLSS\_OUTPUTXBAR12\_G10 Register (Offset = 428h) [reset = 0h]

OUTPUT XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-3903. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8428h       |

**Figure 3-1277. CONTROLSS\_OUTPUTXBAR12\_G10 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR12_G10_SEL |    |    |    |    |    |    |    |
| R/W                  |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR12_G10_SEL |    |    |    |    |    |    |    |
| R/W                  |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 3-3905. CONTROLSS\_OUTPUTXBAR12\_G10 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description                                                                                                                                    |
|-------|----------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED             | NONE | 0h    | Reserved                                                                                                                                       |
| 15:0  | OUTPUTXBAR12_G10_SEL | R/W  | 0h    | G10: OUTPUT XBAR12 G10 Input Select<br>3<br>0:FSIRX0.RX_TRIG0<br>7<br>4:FSIRX1.RX_TRIG0<br>11<br>8:FSIRX2.RX_TRIG0<br>15<br>12:FSIRX3.RX_TRIG0 |

### 3.18.2.153 CONTROLSS\_OUTPUTXBAR13\_G0 Register

#### 1 CONTROLSS\_OUTPUTXBAR13\_G0 Register (Offset = 440h) [reset = 0h]

OUTPUT XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-3906. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8440h       |

**Figure 3-1278. CONTROLSS\_OUTPUTXBAR13\_G0 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR13_G0_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR13_G0_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR13_G0_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR13_G0_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3908. CONTROLSS\_OUTPUTXBAR13\_G0 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                        |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR13_G0_SEL | R/W  | 0h    | G0: PWM XBAR13 G0 input bit select. Input source is PWM[x].TRIPOUT<br>1:PWM[x] TRIPOUT selected<br>0:PWM[x] TRIPOUT is de-selected |



### 3.18.2.154 CONTROLSS\_OUTPUTXBAR13\_G1 Register

#### 1 CONTROLSS\_OUTPUTXBAR13\_G1 Register (Offset = 444h) [reset = 0h]

OUTPUT XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-3909. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8444h       |

**Figure 3-1279. CONTROLSS\_OUTPUTXBAR13\_G1 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR13_G1_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR13_G1_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR13_G1_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR13_G1_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3911. CONTROLSS\_OUTPUTXBAR13\_G1 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                  |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR13_G1_SEL | R/W  | 0h    | G1: OUTPUT XBAR13 G1 input bit select. Input source is PWM[x].SOCA<br>1:PWM[x] SOCA selected<br>0:PWM[x] SOCA is de-selected |

### 3.18.2.155 CONTROLSS\_OUTPUTXBAR13\_G2 Register

#### 1 CONTROLSS\_OUTPUTXBAR13\_G2 Register (Offset = 448h) [reset = 0h]

OUTPUT XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-3912. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8448h       |

**Figure 3-1280. CONTROLSS\_OUTPUTXBAR13\_G2 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR13_G2_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR13_G2_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR13_G2_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR13_G2_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3914. CONTROLSS\_OUTPUTXBAR13\_G2 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                  |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR13_G2_SEL | R/W  | 0h    | G2: OUTPUT XBAR13 G2 input bit select. Input source is PWM[x].SOCB<br>1:PWM[x] SOCB selected<br>0:PWM[x] SOCB is de-selected |

### 3.18.2.156 CONTROLSS\_OUTPUTXBAR13\_G3 Register

#### 1 CONTROLSS\_OUTPUTXBAR13\_G3 Register (Offset = 44Ch) [reset = 0h]

OUTPUT XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-3915. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 844Ch       |

**Figure 3-1281. CONTROLSS\_OUTPUTXBAR13\_G3 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR13_G3_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR13_G3_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR13_G3_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR13_G3_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3917. CONTROLSS\_OUTPUTXBAR13\_G3 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                        |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR13_G3_SEL | R/W  | 0h    | G3: OUTPUT XBAR13 G3 input bit select. Input source is DEL[x].ACTIVE<br>1:DEL[x] ACTIVE selected<br>0:DEL[x] ACTIVE is de-selected |

### 3.18.2.157 CONTROLSS\_OUTPUTXBAR13\_G4 Register

#### 1 CONTROLSS\_OUTPUTXBAR13\_G4 Register (Offset = 450h) [reset = 0h]

OUTPUT XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-3918. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8450h       |

**Figure 3-1282. CONTROLSS\_OUTPUTXBAR13\_G4 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR13_G4_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR13_G4_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR13_G4_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR13_G4_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3920. CONTROLSS\_OUTPUTXBAR13\_G4 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                  |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR13_G4_SEL | R/W  | 0h    | G4: OUTPUT XBAR13 G4 input bit select. Input source is DEL[x].TRIP<br>1:DEL[x] TRIP selected<br>0:DEL[x] TRIP is de-selected |

### 3.18.2.158 CONTROLSS\_OUTPUTXBAR13\_G5 Register

#### 1 CONTROLSS\_OUTPUTXBAR13\_G5 Register (Offset = 454h) [reset = 0h]

OUTPUT XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-3921. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8454h       |

**Figure 3-1283. CONTROLSS\_OUTPUTXBAR13\_G5 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR13_G5_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR13_G5_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR13_G5_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3923. CONTROLSS\_OUTPUTXBAR13\_G5 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3923. CONTROLSS\_OUTPUTXBAR13\_G5 Register Field Descriptions (continued)**

| Bit  | Field                   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|-------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | OUTPUTXBAR13_G5_SE<br>L | R/W  | 0h    | G5: OUTPUT XBAR13 G5 input bit select.<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.18.2.159 CONTROLSS\_OUTPUTXBAR13\_G6 Register

#### 1 CONTROLSS\_OUTPUTXBAR13\_G6 Register (Offset = 458h) [reset = 0h]

OUTPUT XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-3924. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8458h       |

**Figure 3-1284. CONTROLSS\_OUTPUTXBAR13\_G6 Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    | OUTPUTXBAR13_G6_SEL |    |    |    |
| NONE                |    |    |    | R/W                 |    |    |    |
| 0h                  |    |    |    | 0h                  |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| OUTPUTXBAR13_G6_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| OUTPUTXBAR13_G6_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |

**Table 3-3926. CONTROLSS\_OUTPUTXBAR13\_G6 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 19:0  | OUTPUTXBAR13_G6_SEL | R/W  | 0h    | G6: OUTPUT XBAR13 G6 Input Select<br>0: CMPSSA0.CTRIPOUTL<br>1: CMPSSA0.CTRIPOUTH<br>2: CMPSSA1.CTRIPOUTL<br>3: CMPSSA1.CTRIPOUTH<br>4: CMPSSA2.CTRIPOUTL<br>5: CMPSSA2.CTRIPOUTH<br>6: CMPSSA3.CTRIPOUTL<br>7: CMPSSA3.CTRIPOUTH<br>8: CMPSSA4.CTRIPOUTL<br>9: CMPSSA4.CTRIPOUTH<br>10: CMPSSA5.CTRIPOUTL<br>11: CMPSSA5.CTRIPOUTH<br>12: CMPSSA6.CTRIPOUTL<br>13: CMPSSA6.CTRIPOUTH<br>14: CMPSSA7.CTRIPOUTL<br>15: CMPSSA7.CTRIPOUTH<br>16: CMPSSA8.CTRIPOUTL<br>17: CMPSSA8.CTRIPOUTH<br>18: CMPSSA9.CTRIPOUTL<br>19: CMPSSA9.CTRIPOUTH |

### 3.18.2.160 CONTROLSS\_OUTPUTXBAR13\_G7 Register

#### 1 CONTROLSS\_OUTPUTXBAR13\_G7 Register (Offset = 45Ch) [reset = 0h]

OUTPUT XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-3927. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 845Ch       |

**Figure 3-1285. CONTROLSS\_OUTPUTXBAR13\_G7 Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    | OUTPUTXBAR13_G7_SEL |    |    |    |
| NONE                |    |    |    | R/W                 |    |    |    |
| 0h                  |    |    |    | 0h                  |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| OUTPUTXBAR13_G7_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| OUTPUTXBAR13_G7_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |

**Table 3-3929. CONTROLSS\_OUTPUTXBAR13\_G7 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 19:0  | OUTPUTXBAR13_G7_SEL | R/W  | 0h    | G7: OUTPUT XBAR13 G7 Input Select<br>0: CMPSSB0.CTRIPOUTL<br>1: CMPSSB0.CTRIPOUTH<br>2: CMPSSB1.CTRIPOUTL<br>3: CMPSSB1.CTRIPOUTH<br>4: CMPSSB2.CTRIPOUTL<br>5: CMPSSB2.CTRIPOUTH<br>6: CMPSSB3.CTRIPOUTL<br>7: CMPSSB3.CTRIPOUTH<br>8: CMPSSB4.CTRIPOUTL<br>9: CMPSSB4.CTRIPOUTH<br>10: CMPSSB5.CTRIPOUTL<br>11: CMPSSB5.CTRIPOUTH<br>12: CMPSSB6.CTRIPOUTL<br>13: CMPSSB6.CTRIPOUTH<br>14: CMPSSB7.CTRIPOUTL<br>15: CMPSSB7.CTRIPOUTH<br>16: CMPSSB8.CTRIPOUTL<br>17: CMPSSB8.CTRIPOUTH<br>18: CMPSSB9.CTRIPOUTL<br>19: CMPSSB9.CTRIPOUTH |



### 3.18.2.161 CONTROLSS\_OUTPUTXBAR13\_G8 Register

#### 1 CONTROLSS\_OUTPUTXBAR13\_G8 Register (Offset = 460h) [reset = 0h]

OUTPUT XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-3930. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8460h       |

**Figure 3-1286. CONTROLSS\_OUTPUTXBAR13\_G8 Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    | OUTPUTXBAR13_G8_SEL |    |    |    |
| NONE                |    |    |    | R/W                 |    |    |    |
| 0h                  |    |    |    | 0h                  |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| OUTPUTXBAR13_G8_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| OUTPUTXBAR13_G8_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |

**Table 3-3932. CONTROLSS\_OUTPUTXBAR13\_G8 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                             |
|-------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | OUTPUTXBAR13_G8_SEL | R/W  | 0h    | G8: OUTPUT XBAR13 G8 Input Select<br>0:ADC0.EVT1<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.18.2.162 CONTROLSS\_OUTPUTXBAR13\_G9 Register

#### 1 CONTROLSS\_OUTPUTXBAR13\_G9 Register (Offset = 464h) [reset = 0h]

OUTPUT XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-3933. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8464h       |

**Figure 3-1287. CONTROLSS\_OUTPUTXBAR13\_G9 Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    | OUTPUTXBAR13_G9_SEL |    |    |    |
| NONE                |    |    |    | R/W                 |    |    |    |
| 0h                  |    |    |    | 0h                  |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| OUTPUTXBAR13_G9_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| OUTPUTXBAR13_G9_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |

**Table 3-3935. CONTROLSS\_OUTPUTXBAR13\_G9 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|---------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | OUTPUTXBAR13_G9_SEL | R/W  | 0h    | G9: OUTPUT XBAR13 G9 Input Select<br>0:PWMSyncOutXBAR.SYNCOU0<br>1:PWMSyncOutXBAR.SYNCOU1<br>2:PWMSyncOutXBAR.SYNCOU2<br>3:PWMSyncOutXBAR.SYNCOU3<br>4:EQEP0.I_OUT<br>5:EQEP0.S_OUT<br>6:EQEP1.I_OUT<br>7:EQEP1.S_OUT<br>8:EQEP2.I_OUT<br>9:EQEP2.S_OUT<br>10:ECAP0.OUT<br>11:ECAP1.OUT<br>12:ECAP2.OUT<br>13:ECAP3.OUT<br>14:ECAP4.OUT<br>15:ECAP5.OUT<br>16:ECAP6.OUT<br>17:ECAP7.OUT<br>18:ECAP8.OUT<br>19:ECAP9.OUT |

### 3.18.2.163 CONTROLSS\_OUTPUTXBAR13\_G10 Register

#### 1 CONTROLSS\_OUTPUTXBAR13\_G10 Register (Offset = 468h) [reset = 0h]

OUTPUT XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-3936. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8468h       |

**Figure 3-1288. CONTROLSS\_OUTPUTXBAR13\_G10 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR13_G10_SEL |    |    |    |    |    |    |    |
| R/W                  |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR13_G10_SEL |    |    |    |    |    |    |    |
| R/W                  |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 3-3938. CONTROLSS\_OUTPUTXBAR13\_G10 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description                                                                                                                                    |
|-------|----------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED             | NONE | 0h    | Reserved                                                                                                                                       |
| 15:0  | OUTPUTXBAR13_G10_SEL | R/W  | 0h    | G10: OUTPUT XBAR13 G10 Input Select<br>3<br>0:FSIRX0.RX_TRIG0<br>7<br>4:FSIRX1.RX_TRIG0<br>11<br>8:FSIRX2.RX_TRIG0<br>15<br>12:FSIRX3.RX_TRIG0 |

### 3.18.2.164 CONTROLSS\_OUTPUTXBAR14\_G0 Register

#### 1 CONTROLSS\_OUTPUTXBAR14\_G0 Register (Offset = 480h) [reset = 0h]

OUTPUT XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-3939. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8480h       |

**Figure 3-1289. CONTROLSS\_OUTPUTXBAR14\_G0 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR14_G0_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR14_G0_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR14_G0_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR14_G0_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3941. CONTROLSS\_OUTPUTXBAR14\_G0 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                        |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR14_G0_SEL | R/W  | 0h    | G0: PWM XBAR14 G0 input bit select. Input source is PWM[x].TRIPOUT<br>1:PWM[x] TRIPOUT selected<br>0:PWM[x] TRIPOUT is de-selected |

### 3.18.2.165 CONTROLSS\_OUTPUTXBAR14\_G1 Register

#### 1 CONTROLSS\_OUTPUTXBAR14\_G1 Register (Offset = 484h) [reset = 0h]

OUTPUT XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-3942. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8484h       |

**Figure 3-1290. CONTROLSS\_OUTPUTXBAR14\_G1 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR14_G1_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR14_G1_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR14_G1_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR14_G1_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3944. CONTROLSS\_OUTPUTXBAR14\_G1 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                  |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR14_G1_SEL | R/W  | 0h    | G1: OUTPUT XBAR14 G1 input bit select. Input source is PWM[x].SOCA<br>1:PWM[x] SOCA selected<br>0:PWM[x] SOCA is de-selected |

### 3.18.2.166 CONTROLSS\_OUTPUTXBAR14\_G2 Register

#### 1 CONTROLSS\_OUTPUTXBAR14\_G2 Register (Offset = 488h) [reset = 0h]

OUTPUT XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-3945. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8488h       |

**Figure 3-1291. CONTROLSS\_OUTPUTXBAR14\_G2 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR14_G2_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR14_G2_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR14_G2_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR14_G2_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3947. CONTROLSS\_OUTPUTXBAR14\_G2 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                  |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR14_G2_SEL | R/W  | 0h    | G2: OUTPUT XBAR14 G2 input bit select. Input source is PWM[x].SOCB<br>1:PWM[x] SOCB selected<br>0:PWM[x] SOCB is de-selected |

### 3.18.2.167 CONTROLSS\_OUTPUTXBAR14\_G3 Register

#### 1 CONTROLSS\_OUTPUTXBAR14\_G3 Register (Offset = 48Ch) [reset = 0h]

OUTPUT XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-3948. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 848Ch       |

**Figure 3-1292. CONTROLSS\_OUTPUTXBAR14\_G3 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR14_G3_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR14_G3_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR14_G3_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR14_G3_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3950. CONTROLSS\_OUTPUTXBAR14\_G3 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                        |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR14_G3_SEL | R/W  | 0h    | G3: OUTPUT XBAR14 G3 input bit select. Input source is DEL[x].ACTIVE<br>1:DEL[x] ACTIVE selected<br>0:DEL[x] ACTIVE is de-selected |

### 3.18.2.168 CONTROLSS\_OUTPUTXBAR14\_G4 Register

#### 1 CONTROLSS\_OUTPUTXBAR14\_G4 Register (Offset = 490h) [reset = 0h]

OUTPUT XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-3951. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8490h       |

**Figure 3-1293. CONTROLSS\_OUTPUTXBAR14\_G4 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR14_G4_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR14_G4_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR14_G4_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR14_G4_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3953. CONTROLSS\_OUTPUTXBAR14\_G4 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                  |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR14_G4_SEL | R/W  | 0h    | G4: OUTPUT XBAR14 G4 input bit select. Input source is DEL[x].TRIP<br>1:DEL[x] TRIP selected<br>0:DEL[x] TRIP is de-selected |



### 3.18.2.169 CONTROLSS\_OUTPUTXBAR14\_G5 Register

#### 1 CONTROLSS\_OUTPUTXBAR14\_G5 Register (Offset = 494h) [reset = 0h]

OUTPUT XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-3954. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8494h       |

**Figure 3-1294. CONTROLSS\_OUTPUTXBAR14\_G5 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR14_G5_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR14_G5_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR14_G5_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3956. CONTROLSS\_OUTPUTXBAR14\_G5 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3956. CONTROLSS\_OUTPUTXBAR14\_G5 Register Field Descriptions (continued)**

| Bit  | Field                   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|-------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | OUTPUTXBAR14_G5_SE<br>L | R/W  | 0h    | G5: OUTPUT XBAR14 G5 input bit select.<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.18.2.170 CONTROLSS\_OUTPUTXBAR14\_G6 Register

#### 1 CONTROLSS\_OUTPUTXBAR14\_G6 Register (Offset = 498h) [reset = 0h]

OUTPUT XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-3957. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 8498h       |

**Figure 3-1295. CONTROLSS\_OUTPUTXBAR14\_G6 Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    | OUTPUTXBAR14_G6_SEL |    |    |    |
| NONE                |    |    |    | R/W                 |    |    |    |
| 0h                  |    |    |    | 0h                  |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| OUTPUTXBAR14_G6_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| OUTPUTXBAR14_G6_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |

**Table 3-3959. CONTROLSS\_OUTPUTXBAR14\_G6 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 19:0  | OUTPUTXBAR14_G6_SEL | R/W  | 0h    | G6: OUTPUT XBAR14 G6 Input Select<br>0: CMPSSA0.CTRIPOUTL<br>1: CMPSSA0.CTRIPOUTH<br>2: CMPSSA1.CTRIPOUTL<br>3: CMPSSA1.CTRIPOUTH<br>4: CMPSSA2.CTRIPOUTL<br>5: CMPSSA2.CTRIPOUTH<br>6: CMPSSA3.CTRIPOUTL<br>7: CMPSSA3.CTRIPOUTH<br>8: CMPSSA4.CTRIPOUTL<br>9: CMPSSA4.CTRIPOUTH<br>10: CMPSSA5.CTRIPOUTL<br>11: CMPSSA5.CTRIPOUTH<br>12: CMPSSA6.CTRIPOUTL<br>13: CMPSSA6.CTRIPOUTH<br>14: CMPSSA7.CTRIPOUTL<br>15: CMPSSA7.CTRIPOUTH<br>16: CMPSSA8.CTRIPOUTL<br>17: CMPSSA8.CTRIPOUTH<br>18: CMPSSA9.CTRIPOUTL<br>19: CMPSSA9.CTRIPOUTH |

### 3.18.2.171 CONTROLSS\_OUTPUTXBAR14\_G7 Register

#### 1 CONTROLSS\_OUTPUTXBAR14\_G7 Register (Offset = 49Ch) [reset = 0h]

OUTPUT XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-3960. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 849Ch       |

**Figure 3-1296. CONTROLSS\_OUTPUTXBAR14\_G7 Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    | OUTPUTXBAR14_G7_SEL |    |    |    |
| NONE                |    |    |    | R/W                 |    |    |    |
| 0h                  |    |    |    | 0h                  |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| OUTPUTXBAR14_G7_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| OUTPUTXBAR14_G7_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |

**Table 3-3962. CONTROLSS\_OUTPUTXBAR14\_G7 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 19:0  | OUTPUTXBAR14_G7_SEL | R/W  | 0h    | G7: OUTPUT XBAR14 G7 Input Select<br>0: CMPSSB0.CTRIPOUTL<br>1: CMPSSB0.CTRIPOUTH<br>2: CMPSSB1.CTRIPOUTL<br>3: CMPSSB1.CTRIPOUTH<br>4: CMPSSB2.CTRIPOUTL<br>5: CMPSSB2.CTRIPOUTH<br>6: CMPSSB3.CTRIPOUTL<br>7: CMPSSB3.CTRIPOUTH<br>8: CMPSSB4.CTRIPOUTL<br>9: CMPSSB4.CTRIPOUTH<br>10: CMPSSB5.CTRIPOUTL<br>11: CMPSSB5.CTRIPOUTH<br>12: CMPSSB6.CTRIPOUTL<br>13: CMPSSB6.CTRIPOUTH<br>14: CMPSSB7.CTRIPOUTL<br>15: CMPSSB7.CTRIPOUTH<br>16: CMPSSB8.CTRIPOUTL<br>17: CMPSSB8.CTRIPOUTH<br>18: CMPSSB9.CTRIPOUTL<br>19: CMPSSB9.CTRIPOUTH |

### 3.18.2.172 CONTROLSS\_OUTPUTXBAR14\_G8 Register

#### 1 CONTROLSS\_OUTPUTXBAR14\_G8 Register (Offset = 4A0h) [reset = 0h]

OUTPUT XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-3963. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 84A0h       |

**Figure 3-1297. CONTROLSS\_OUTPUTXBAR14\_G8 Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    | OUTPUTXBAR14_G8_SEL |    |    |    |
| NONE                |    |    |    | R/W                 |    |    |    |
| 0h                  |    |    |    | 0h                  |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| OUTPUTXBAR14_G8_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| OUTPUTXBAR14_G8_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |

**Table 3-3965. CONTROLSS\_OUTPUTXBAR14\_G8 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                             |
|-------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | OUTPUTXBAR14_G8_SEL | R/W  | 0h    | G8: OUTPUT XBAR14 G8 Input Select<br>0:ADC0.EVT1<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.18.2.173 CONTROLSS\_OUTPUTXBAR14\_G9 Register

#### 1 CONTROLSS\_OUTPUTXBAR14\_G9 Register (Offset = 4A4h) [reset = 0h]

OUTPUT XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-3966. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 84A4h       |

**Figure 3-1298. CONTROLSS\_OUTPUTXBAR14\_G9 Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    | OUTPUTXBAR14_G9_SEL |    |    |    |
| NONE                |    |    |    | R/W                 |    |    |    |
| 0h                  |    |    |    | 0h                  |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| OUTPUTXBAR14_G9_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| OUTPUTXBAR14_G9_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |

**Table 3-3968. CONTROLSS\_OUTPUTXBAR14\_G9 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|---------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | OUTPUTXBAR14_G9_SEL | R/W  | 0h    | G9: OUTPUT XBAR14 G9 Input Select<br>0:PWMSyncOutXBAR.SYNCOU0<br>1:PWMSyncOutXBAR.SYNCOU1<br>2:PWMSyncOutXBAR.SYNCOU2<br>3:PWMSyncOutXBAR.SYNCOU3<br>4:EQEP0.I_OUT<br>5:EQEP0.S_OUT<br>6:EQEP1.I_OUT<br>7:EQEP1.S_OUT<br>8:EQEP2.I_OUT<br>9:EQEP2.S_OUT<br>10:ECAP0.OUT<br>11:ECAP1.OUT<br>12:ECAP2.OUT<br>13:ECAP3.OUT<br>14:ECAP4.OUT<br>15:ECAP5.OUT<br>16:ECAP6.OUT<br>17:ECAP7.OUT<br>18:ECAP8.OUT<br>19:ECAP9.OUT |

### 3.18.2.174 CONTROLSS\_OUTPUTXBAR14\_G10 Register

#### 1 CONTROLSS\_OUTPUTXBAR14\_G10 Register (Offset = 4A8h) [reset = 0h]

OUTPUT XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-3969. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 84A8h       |

**Figure 3-1299. CONTROLSS\_OUTPUTXBAR14\_G10 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR14_G10_SEL |    |    |    |    |    |    |    |
| R/W                  |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR14_G10_SEL |    |    |    |    |    |    |    |
| R/W                  |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 3-3971. CONTROLSS\_OUTPUTXBAR14\_G10 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description                                                                                                                                    |
|-------|----------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED             | NONE | 0h    | Reserved                                                                                                                                       |
| 15:0  | OUTPUTXBAR14_G10_SEL | R/W  | 0h    | G10: OUTPUT XBAR14 G10 Input Select<br>3<br>0:FSIRX0.RX_TRIG0<br>7<br>4:FSIRX1.RX_TRIG0<br>11<br>8:FSIRX2.RX_TRIG0<br>15<br>12:FSIRX3.RX_TRIG0 |

### 3.18.2.175 CONTROLSS\_OUTPUTXBAR15\_G0 Register

#### 1 CONTROLSS\_OUTPUTXBAR15\_G0 Register (Offset = 4C0h) [reset = 0h]

OUTPUT XBAR 15 Input Select.

Return to [Summary Table](#)

**Table 3-3972. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 84C0h       |

**Figure 3-1300. CONTROLSS\_OUTPUTXBAR15\_G0 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR15_G0_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR15_G0_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR15_G0_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR15_G0_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3974. CONTROLSS\_OUTPUTXBAR15\_G0 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                        |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR15_G0_SEL | R/W  | 0h    | G0: PWM XBAR15 G0 input bit select. Input source is PWM[x].TRIPOUT<br>1:PWM[x] TRIPOUT selected<br>0:PWM[x] TRIPOUT is de-selected |



### 3.18.2.176 CONTROLSS\_OUTPUTXBAR15\_G1 Register

#### 1 CONTROLSS\_OUTPUTXBAR15\_G1 Register (Offset = 4C4h) [reset = 0h]

OUTPUT XBAR 15 Input Select.

Return to [Summary Table](#)

**Table 3-3975. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 84C4h       |

**Figure 3-1301. CONTROLSS\_OUTPUTXBAR15\_G1 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR15_G1_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR15_G1_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR15_G1_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR15_G1_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3977. CONTROLSS\_OUTPUTXBAR15\_G1 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                  |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR15_G1_SEL | R/W  | 0h    | G1: OUTPUT XBAR15 G1 input bit select. Input source is PWM[x].SOCA<br>1:PWM[x] SOCA selected<br>0:PWM[x] SOCA is de-selected |

### 3.18.2.177 CONTROLSS\_OUTPUTXBAR15\_G2 Register

#### 1 CONTROLSS\_OUTPUTXBAR15\_G2 Register (Offset = 4C8h) [reset = 0h]

OUTPUT XBAR 15 Input Select.

Return to [Summary Table](#)

**Table 3-3978. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 84C8h       |

**Figure 3-1302. CONTROLSS\_OUTPUTXBAR15\_G2 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR15_G2_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR15_G2_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR15_G2_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR15_G2_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3980. CONTROLSS\_OUTPUTXBAR15\_G2 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                  |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR15_G2_SEL | R/W  | 0h    | G2: OUTPUT XBAR15 G2 input bit select. Input source is PWM[x].SOCB<br>1:PWM[x] SOCB selected<br>0:PWM[x] SOCB is de-selected |

### 3.18.2.178 CONTROLSS\_OUTPUTXBAR15\_G3 Register

#### 1 CONTROLSS\_OUTPUTXBAR15\_G3 Register (Offset = 4CCh) [reset = 0h]

OUTPUT XBAR 15 Input Select.

Return to [Summary Table](#)

**Table 3-3981. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 84CCh       |

**Figure 3-1303. CONTROLSS\_OUTPUTXBAR15\_G3 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR15_G3_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR15_G3_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR15_G3_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR15_G3_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3983. CONTROLSS\_OUTPUTXBAR15\_G3 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                        |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR15_G3_SEL | R/W  | 0h    | G3: OUTPUT XBAR15 G3 input bit select. Input source is DEL[x].ACTIVE<br>1:DEL[x] ACTIVE selected<br>0:DEL[x] ACTIVE is de-selected |

### 3.18.2.179 CONTROLSS\_OUTPUTXBAR15\_G4 Register

#### 1 CONTROLSS\_OUTPUTXBAR15\_G4 Register (Offset = 4D0h) [reset = 0h]

OUTPUT XBAR 15 Input Select.

Return to [Summary Table](#)

**Table 3-3984. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 84D0h       |

**Figure 3-1304. CONTROLSS\_OUTPUTXBAR15\_G4 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUTPUTXBAR15_G4_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR15_G4_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR15_G4_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR15_G4_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3986. CONTROLSS\_OUTPUTXBAR15\_G4 Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                                                                                                                  |
|------|---------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | OUTPUTXBAR15_G4_SEL | R/W  | 0h    | G4: OUTPUT XBAR15 G4 input bit select. Input source is DEL[x].TRIP<br>1:DEL[x] TRIP selected<br>0:DEL[x] TRIP is de-selected |

### 3.18.2.180 CONTROLSS\_OUTPUTXBAR15\_G5 Register

#### 1 CONTROLSS\_OUTPUTXBAR15\_G5 Register (Offset = 4D4h) [reset = 0h]

OUTPUT XBAR 15 Input Select.

Return to [Summary Table](#)

**Table 3-3987. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 84D4h       |

**Figure 3-1305. CONTROLSS\_OUTPUTXBAR15\_G5 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUTPUTXBAR15_G5_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR15_G5_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR15_G5_SEL |    |    |    |    |    |    |    |
| R/W                 |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 3-3989. CONTROLSS\_OUTPUTXBAR15\_G5 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-3989. CONTROLSS\_OUTPUTXBAR15\_G5 Register Field Descriptions (continued)**

| Bit  | Field                   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|-------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | OUTPUTXBAR15_G5_SE<br>L | R/W  | 0h    | G5: OUTPUT XBAR15 G5 input bit select.<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.18.2.181 CONTROLSS\_OUTPUTXBAR15\_G6 Register

#### 1 CONTROLSS\_OUTPUTXBAR15\_G6 Register (Offset = 4D8h) [reset = 0h]

OUTPUT XBAR 15 Input Select.

Return to [Summary Table](#)

**Table 3-3990. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 84D8h       |

**Figure 3-1306. CONTROLSS\_OUTPUTXBAR15\_G6 Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    | OUTPUTXBAR15_G6_SEL |    |    |    |
| NONE                |    |    |    | R/W                 |    |    |    |
| 0h                  |    |    |    | 0h                  |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| OUTPUTXBAR15_G6_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| OUTPUTXBAR15_G6_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |

**Table 3-3992. CONTROLSS\_OUTPUTXBAR15\_G6 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 19:0  | OUTPUTXBAR15_G6_SEL | R/W  | 0h    | G6: OUTPUT XBAR15 G6 Input Select<br>0: CMPSSA0.CTRIPOUTL<br>1: CMPSSA0.CTRIPOUTH<br>2: CMPSSA1.CTRIPOUTL<br>3: CMPSSA1.CTRIPOUTH<br>4: CMPSSA2.CTRIPOUTL<br>5: CMPSSA2.CTRIPOUTH<br>6: CMPSSA3.CTRIPOUTL<br>7: CMPSSA3.CTRIPOUTH<br>8: CMPSSA4.CTRIPOUTL<br>9: CMPSSA4.CTRIPOUTH<br>10: CMPSSA5.CTRIPOUTL<br>11: CMPSSA5.CTRIPOUTH<br>12: CMPSSA6.CTRIPOUTL<br>13: CMPSSA6.CTRIPOUTH<br>14: CMPSSA7.CTRIPOUTL<br>15: CMPSSA7.CTRIPOUTH<br>16: CMPSSA8.CTRIPOUTL<br>17: CMPSSA8.CTRIPOUTH<br>18: CMPSSA9.CTRIPOUTL<br>19: CMPSSA9.CTRIPOUTH |

### 3.18.2.182 CONTROLSS\_OUTPUTXBAR15\_G7 Register

#### 1 CONTROLSS\_OUTPUTXBAR15\_G7 Register (Offset = 4DCh) [reset = 0h]

OUTPUT XBAR 15 Input Select.

Return to [Summary Table](#)

**Table 3-3993. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 84DCh       |

**Figure 3-1307. CONTROLSS\_OUTPUTXBAR15\_G7 Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    | OUTPUTXBAR15_G7_SEL |    |    |    |
| NONE                |    |    |    | R/W                 |    |    |    |
| 0h                  |    |    |    | 0h                  |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| OUTPUTXBAR15_G7_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| OUTPUTXBAR15_G7_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |

**Table 3-3995. CONTROLSS\_OUTPUTXBAR15\_G7 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 19:0  | OUTPUTXBAR15_G7_SEL | R/W  | 0h    | G7: OUTPUT XBAR15 G7 Input Select<br>0: CMPSSB0.CTRIPOUTL<br>1: CMPSSB0.CTRIPOUTH<br>2: CMPSSB1.CTRIPOUTL<br>3: CMPSSB1.CTRIPOUTH<br>4: CMPSSB2.CTRIPOUTL<br>5: CMPSSB2.CTRIPOUTH<br>6: CMPSSB3.CTRIPOUTL<br>7: CMPSSB3.CTRIPOUTH<br>8: CMPSSB4.CTRIPOUTL<br>9: CMPSSB4.CTRIPOUTH<br>10: CMPSSB5.CTRIPOUTL<br>11: CMPSSB5.CTRIPOUTH<br>12: CMPSSB6.CTRIPOUTL<br>13: CMPSSB6.CTRIPOUTH<br>14: CMPSSB7.CTRIPOUTL<br>15: CMPSSB7.CTRIPOUTH<br>16: CMPSSB8.CTRIPOUTL<br>17: CMPSSB8.CTRIPOUTH<br>18: CMPSSB9.CTRIPOUTL<br>19: CMPSSB9.CTRIPOUTH |



### 3.18.2.183 CONTROLSS\_OUTPUTXBAR15\_G8 Register

#### 1 CONTROLSS\_OUTPUTXBAR15\_G8 Register (Offset = 4E0h) [reset = 0h]

OUTPUT XBAR 15 Input Select.

Return to [Summary Table](#)

**Table 3-3996. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 84E0h       |

**Figure 3-1308. CONTROLSS\_OUTPUTXBAR15\_G8 Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    | OUTPUTXBAR15_G8_SEL |    |    |    |
| NONE                |    |    |    | R/W                 |    |    |    |
| 0h                  |    |    |    | 0h                  |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| OUTPUTXBAR15_G8_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| OUTPUTXBAR15_G8_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |

**Table 3-3998. CONTROLSS\_OUTPUTXBAR15\_G8 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                             |
|-------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | OUTPUTXBAR15_G8_SEL | R/W  | 0h    | G8: OUTPUT XBAR15 G8 Input Select<br>0:ADC0.EVT1<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.18.2.184 CONTROLSS\_OUTPUTXBAR15\_G9 Register

#### 1 CONTROLSS\_OUTPUTXBAR15\_G9 Register (Offset = 4E4h) [reset = 0h]

OUTPUT XBAR 15 Input Select.

Return to [Summary Table](#)

**Table 3-3999. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 84E4h       |

**Figure 3-1309. CONTROLSS\_OUTPUTXBAR15\_G9 Name Register**

|                     |    |    |    |                     |    |    |    |
|---------------------|----|----|----|---------------------|----|----|----|
| 31                  | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED            |    |    |    |                     |    |    |    |
| NONE                |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 23                  | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED            |    |    |    | OUTPUTXBAR15_G9_SEL |    |    |    |
| NONE                |    |    |    | R/W                 |    |    |    |
| 0h                  |    |    |    | 0h                  |    |    |    |
| 15                  | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| OUTPUTXBAR15_G9_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |
| 7                   | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| OUTPUTXBAR15_G9_SEL |    |    |    |                     |    |    |    |
| R/W                 |    |    |    |                     |    |    |    |
| 0h                  |    |    |    |                     |    |    |    |

**Table 3-4001. CONTROLSS\_OUTPUTXBAR15\_G9 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|---------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | OUTPUTXBAR15_G9_SEL | R/W  | 0h    | G9: OUTPUT XBAR15 G9 Input Select<br>0:PWMSyncOutXBAR.SYNCOU0<br>1:PWMSyncOutXBAR.SYNCOU1<br>2:PWMSyncOutXBAR.SYNCOU2<br>3:PWMSyncOutXBAR.SYNCOU3<br>4:EQEP0.I_OUT<br>5:EQEP0.S_OUT<br>6:EQEP1.I_OUT<br>7:EQEP1.S_OUT<br>8:EQEP2.I_OUT<br>9:EQEP2.S_OUT<br>10:ECAP0.OUT<br>11:ECAP1.OUT<br>12:ECAP2.OUT<br>13:ECAP3.OUT<br>14:ECAP4.OUT<br>15:ECAP5.OUT<br>16:ECAP6.OUT<br>17:ECAP7.OUT<br>18:ECAP8.OUT<br>19:ECAP9.OUT |

### 3.18.2.185 CONTROLSS\_OUTPUTXBAR15\_G10 Register

#### 1 CONTROLSS\_OUTPUTXBAR15\_G10 Register (Offset = 4E8h) [reset = 0h]

OUTPUT XBAR 15 Input Select.

Return to [Summary Table](#)

**Table 3-4002. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| CONTROLSS_OUTPUTXBAR | 502D 84E8h       |

**Figure 3-1310. CONTROLSS\_OUTPUTXBAR15\_G10 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUTPUTXBAR15_G10_SEL |    |    |    |    |    |    |    |
| R/W                  |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUTPUTXBAR15_G10_SEL |    |    |    |    |    |    |    |
| R/W                  |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 3-4004. CONTROLSS\_OUTPUTXBAR15\_G10 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description                                                                                                                                    |
|-------|----------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED             | NONE | 0h    | Reserved                                                                                                                                       |
| 15:0  | OUTPUTXBAR15_G10_SEL | R/W  | 0h    | G10: OUTPUT XBAR15 G10 Input Select<br>3<br>0:FSIRX0.RX_TRIG0<br>7<br>4:FSIRX1.RX_TRIG0<br>11<br>8:FSIRX2.RX_TRIG0<br>15<br>12:FSIRX3.RX_TRIG0 |

## 3.19 CONTROLSS\_PWMSYNCOUXTBAR

### CONTROLSS\_PWMSYNCOUXTBAR

#### 3.19.1 CONTROLSS\_PWMSYNCOUXTBAR Summaries

#### CONTROLSS\_PWMSYNCOUXTBAR Summaries

**Table 3-4005. CONTROLSS Registers, Base Address=502D 2000h, Length=2048**

| Offset | Length | Register Name                                | CONTROLSS_PWMSYNCOUXTBAR<br>Physical Address |
|--------|--------|----------------------------------------------|----------------------------------------------|
| 100h   | 32     | <a href="#">CONTROLSS_PWMSYNCOUXTBAR0_G0</a> | 502D 2100h                                   |
| 140h   | 32     | <a href="#">CONTROLSS_PWMSYNCOUXTBAR1_G0</a> | 502D 2140h                                   |
| 180h   | 32     | <a href="#">CONTROLSS_PWMSYNCOUXTBAR2_G0</a> | 502D 2180h                                   |
| 1C0h   | 32     | <a href="#">CONTROLSS_PWMSYNCOUXTBAR3_G0</a> | 502D 21C0h                                   |

#### 3.19.2 CONTROLSS\_PWMSYNCOUXTBAR Registers

#### CONTROLSS\_PWMSYNCOUXTBAR Registers

### 3.19.2.1 CONTROLSS\_PWMSYNCOUXTBAR0\_G0 Register

#### 1 CONTROLSS\_PWMSYNCOUXTBAR0\_G0 Register (Offset = 100h) [reset = 0h]

EPWM pwmsyncout XBAR0 select.

Return to [Summary Table](#)

**Table 3-4006. Instance Table**

| Instance Name            | Physical Address |
|--------------------------|------------------|
| CONTROLSS_PWMSYNCOUXTBAR | 502D 2100h       |

**Figure 3-1311. CONTROLSS\_PWMSYNCOUXTBAR0\_G0 Name Register**

|                        |    |    |    |    |    |    |    |
|------------------------|----|----|----|----|----|----|----|
| 31                     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMSYNCOUXTBAR0_G0_SEL |    |    |    |    |    |    |    |
| R/W                    |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |
| 23                     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMSYNCOUXTBAR0_G0_SEL |    |    |    |    |    |    |    |
| R/W                    |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |
| 15                     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMSYNCOUXTBAR0_G0_SEL |    |    |    |    |    |    |    |
| R/W                    |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |
| 7                      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMSYNCOUXTBAR0_G0_SEL |    |    |    |    |    |    |    |
| R/W                    |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |

**Table 3-4008. CONTROLSS\_PWMSYNCOUXTBAR0\_G0 Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                                                  |
|------|------------------------|------|-------|----------------------------------------------------------------------------------------------|
| 31:0 | PWMSYNCOUXTBAR0_G0_SEL | R/W  | 0h    | EPWM pwmsyncout XBAR0 select<br>1:PWM[x] SYNCOUT selected<br>0:PWM[x] SYNCOUT is de-selected |

### 3.19.2.2 CONTROLSS\_PWMSYNCOUXTBAR1\_G0 Register

#### 1 CONTROLSS\_PWMSYNCOUXTBAR1\_G0 Register (Offset = 140h) [reset = 0h]

EPWM pwmsyncout XBAR1 select.

Return to [Summary Table](#)

**Table 3-4009. Instance Table**

| Instance Name            | Physical Address |
|--------------------------|------------------|
| CONTROLSS_PWMSYNCOUXTBAR | 502D 2140h       |

**Figure 3-1312. CONTROLSS\_PWMSYNCOUXTBAR1\_G0 Name Register**

|                        |    |    |    |    |    |    |    |
|------------------------|----|----|----|----|----|----|----|
| 31                     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMSYNCOUXTBAR1_G0_SEL |    |    |    |    |    |    |    |
| R/W                    |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |
| 23                     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMSYNCOUXTBAR1_G0_SEL |    |    |    |    |    |    |    |
| R/W                    |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |
| 15                     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMSYNCOUXTBAR1_G0_SEL |    |    |    |    |    |    |    |
| R/W                    |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |
| 7                      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMSYNCOUXTBAR1_G0_SEL |    |    |    |    |    |    |    |
| R/W                    |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |

**Table 3-4011. CONTROLSS\_PWMSYNCOUXTBAR1\_G0 Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                                                  |
|------|------------------------|------|-------|----------------------------------------------------------------------------------------------|
| 31:0 | PWMSYNCOUXTBAR1_G0_SEL | R/W  | 0h    | EPWM pwmsyncout XBAR1 select<br>1:PWM[x] SYNCOUT selected<br>0:PWM[x] SYNCOUT is de-selected |

### 3.19.2.3 CONTROLSS\_PWMSYNCOUXTBAR2\_G0 Register

#### 1 CONTROLSS\_PWMSYNCOUXTBAR2\_G0 Register (Offset = 180h) [reset = 0h]

EPWM pwmsyncout XBAR2 select.

Return to [Summary Table](#)

**Table 3-4012. Instance Table**

| Instance Name            | Physical Address |
|--------------------------|------------------|
| CONTROLSS_PWMSYNCOUXTBAR | 502D 2180h       |

**Figure 3-1313. CONTROLSS\_PWMSYNCOUXTBAR2\_G0 Name Register**

|                        |    |    |    |    |    |    |    |
|------------------------|----|----|----|----|----|----|----|
| 31                     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMSYNCOUXTBAR2_G0_SEL |    |    |    |    |    |    |    |
| R/W                    |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |
| 23                     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMSYNCOUXTBAR2_G0_SEL |    |    |    |    |    |    |    |
| R/W                    |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |
| 15                     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMSYNCOUXTBAR2_G0_SEL |    |    |    |    |    |    |    |
| R/W                    |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |
| 7                      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMSYNCOUXTBAR2_G0_SEL |    |    |    |    |    |    |    |
| R/W                    |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |

**Table 3-4014. CONTROLSS\_PWMSYNCOUXTBAR2\_G0 Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                                                  |
|------|------------------------|------|-------|----------------------------------------------------------------------------------------------|
| 31:0 | PWMSYNCOUXTBAR2_G0_SEL | R/W  | 0h    | EPWM pwmsyncout XBAR2 select<br>1:PWM[x] SYNCOUT selected<br>0:PWM[x] SYNCOUT is de-selected |

### 3.19.2.4 CONTROLSS\_PWMSYNCOUXTBAR3\_G0 Register

#### 1 CONTROLSS\_PWMSYNCOUXTBAR3\_G0 Register (Offset = 1C0h) [reset = 0h]

EPWM pwmsyncout XBAR3 select.

Return to [Summary Table](#)

**Table 3-4015. Instance Table**

| Instance Name                | Physical Address |
|------------------------------|------------------|
| CONTROLSS_PWMSYNCOUXTBAR3_G0 | 502D 21C0h       |

**Figure 3-1314. CONTROLSS\_PWMSYNCOUXTBAR3\_G0 Name Register**

|                        |    |    |    |    |    |    |    |
|------------------------|----|----|----|----|----|----|----|
| 31                     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMSYNCOUXTBAR3_G0_SEL |    |    |    |    |    |    |    |
| R/W                    |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |
| 23                     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMSYNCOUXTBAR3_G0_SEL |    |    |    |    |    |    |    |
| R/W                    |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |
| 15                     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMSYNCOUXTBAR3_G0_SEL |    |    |    |    |    |    |    |
| R/W                    |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |
| 7                      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMSYNCOUXTBAR3_G0_SEL |    |    |    |    |    |    |    |
| R/W                    |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |

**Table 3-4017. CONTROLSS\_PWMSYNCOUXTBAR3\_G0 Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                                                  |
|------|------------------------|------|-------|----------------------------------------------------------------------------------------------|
| 31:0 | PWMSYNCOUXTBAR3_G0_SEL | R/W  | 0h    | EPWM pwmsyncout XBAR3 select<br>1:PWM[x] SYNCOUT selected<br>0:PWM[x] SYNCOUT is de-selected |



## 3.20 CONTROLSS\_PWMXBAR

### CONTROLSS\_PWMXBAR

#### 3.20.1 CONTROLSS\_PWMXBAR Summaries

#### CONTROLSS\_PWMXBAR Summaries

**Table 3-4018. CONTROLSS Registers, Base Address=502D 1000h, Length=2048**

| Offset | Length | Register Name                                | CONTROLSS_PWMXBAR Physical Address |
|--------|--------|----------------------------------------------|------------------------------------|
| 10h    | 32     | <a href="#">CONTROLSS_PWMXBAR_STATUS</a>     | 502D 1010h                         |
| 14h    | 32     | <a href="#">CONTROLSS_PWMXBAR_FLAGINVERT</a> | 502D 1014h                         |
| 18h    | 32     | <a href="#">CONTROLSS_PWMXBAR_FLAG</a>       | 502D 1018h                         |
| 1Ch    | 32     | <a href="#">CONTROLSS_PWMXBAR_FLAG_CLR</a>   | 502D 101Ch                         |
| 100h   | 32     | <a href="#">CONTROLSS_PWMXBAR0_G0</a>        | 502D 1100h                         |
| 104h   | 32     | <a href="#">CONTROLSS_PWMXBAR0_G1</a>        | 502D 1104h                         |
| 108h   | 32     | <a href="#">CONTROLSS_PWMXBAR0_G2</a>        | 502D 1108h                         |
| 10Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR0_G3</a>        | 502D 110Ch                         |
| 110h   | 32     | <a href="#">CONTROLSS_PWMXBAR0_G4</a>        | 502D 1110h                         |
| 114h   | 32     | <a href="#">CONTROLSS_PWMXBAR0_G5</a>        | 502D 1114h                         |
| 118h   | 32     | <a href="#">CONTROLSS_PWMXBAR0_G6</a>        | 502D 1118h                         |
| 11Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR0_G7</a>        | 502D 111Ch                         |
| 120h   | 32     | <a href="#">CONTROLSS_PWMXBAR0_G8</a>        | 502D 1120h                         |
| 140h   | 32     | <a href="#">CONTROLSS_PWMXBAR1_G0</a>        | 502D 1140h                         |
| 144h   | 32     | <a href="#">CONTROLSS_PWMXBAR1_G1</a>        | 502D 1144h                         |
| 148h   | 32     | <a href="#">CONTROLSS_PWMXBAR1_G2</a>        | 502D 1148h                         |
| 14Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR1_G3</a>        | 502D 114Ch                         |
| 150h   | 32     | <a href="#">CONTROLSS_PWMXBAR1_G4</a>        | 502D 1150h                         |
| 154h   | 32     | <a href="#">CONTROLSS_PWMXBAR1_G5</a>        | 502D 1154h                         |
| 158h   | 32     | <a href="#">CONTROLSS_PWMXBAR1_G6</a>        | 502D 1158h                         |
| 15Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR1_G7</a>        | 502D 115Ch                         |
| 160h   | 32     | <a href="#">CONTROLSS_PWMXBAR1_G8</a>        | 502D 1160h                         |
| 180h   | 32     | <a href="#">CONTROLSS_PWMXBAR2_G0</a>        | 502D 1180h                         |
| 184h   | 32     | <a href="#">CONTROLSS_PWMXBAR2_G1</a>        | 502D 1184h                         |
| 188h   | 32     | <a href="#">CONTROLSS_PWMXBAR2_G2</a>        | 502D 1188h                         |
| 18Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR2_G3</a>        | 502D 118Ch                         |
| 190h   | 32     | <a href="#">CONTROLSS_PWMXBAR2_G4</a>        | 502D 1190h                         |
| 194h   | 32     | <a href="#">CONTROLSS_PWMXBAR2_G5</a>        | 502D 1194h                         |
| 198h   | 32     | <a href="#">CONTROLSS_PWMXBAR2_G6</a>        | 502D 1198h                         |
| 19Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR2_G7</a>        | 502D 119Ch                         |
| 1A0h   | 32     | <a href="#">CONTROLSS_PWMXBAR2_G8</a>        | 502D 11A0h                         |
| 1C0h   | 32     | <a href="#">CONTROLSS_PWMXBAR3_G0</a>        | 502D 11C0h                         |
| 1C4h   | 32     | <a href="#">CONTROLSS_PWMXBAR3_G1</a>        | 502D 11C4h                         |
| 1C8h   | 32     | <a href="#">CONTROLSS_PWMXBAR3_G2</a>        | 502D 11C8h                         |
| 1CCh   | 32     | <a href="#">CONTROLSS_PWMXBAR3_G3</a>        | 502D 11CCh                         |
| 1D0h   | 32     | <a href="#">CONTROLSS_PWMXBAR3_G4</a>        | 502D 11D0h                         |
| 1D4h   | 32     | <a href="#">CONTROLSS_PWMXBAR3_G5</a>        | 502D 11D4h                         |

**Table 3-4018. CONTROLSS Registers, Base Address=502D 1000h, Length=2048 (continued)**

| Offset | Length | Register Name                         | CONTROLSS_PWMXBAR Physical Address |
|--------|--------|---------------------------------------|------------------------------------|
| 1D8h   | 32     | <a href="#">CONTROLSS_PWMXBAR3_G6</a> | 502D 11D8h                         |
| 1DCh   | 32     | <a href="#">CONTROLSS_PWMXBAR3_G7</a> | 502D 11DCh                         |
| 1E0h   | 32     | <a href="#">CONTROLSS_PWMXBAR3_G8</a> | 502D 11E0h                         |
| 200h   | 32     | <a href="#">CONTROLSS_PWMXBAR4_G0</a> | 502D 1200h                         |
| 204h   | 32     | <a href="#">CONTROLSS_PWMXBAR4_G1</a> | 502D 1204h                         |
| 208h   | 32     | <a href="#">CONTROLSS_PWMXBAR4_G2</a> | 502D 1208h                         |
| 20Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR4_G3</a> | 502D 120Ch                         |
| 210h   | 32     | <a href="#">CONTROLSS_PWMXBAR4_G4</a> | 502D 1210h                         |
| 214h   | 32     | <a href="#">CONTROLSS_PWMXBAR4_G5</a> | 502D 1214h                         |
| 218h   | 32     | <a href="#">CONTROLSS_PWMXBAR4_G6</a> | 502D 1218h                         |
| 21Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR4_G7</a> | 502D 121Ch                         |
| 220h   | 32     | <a href="#">CONTROLSS_PWMXBAR4_G8</a> | 502D 1220h                         |
| 240h   | 32     | <a href="#">CONTROLSS_PWMXBAR5_G0</a> | 502D 1240h                         |
| 244h   | 32     | <a href="#">CONTROLSS_PWMXBAR5_G1</a> | 502D 1244h                         |
| 248h   | 32     | <a href="#">CONTROLSS_PWMXBAR5_G2</a> | 502D 1248h                         |
| 24Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR5_G3</a> | 502D 124Ch                         |
| 250h   | 32     | <a href="#">CONTROLSS_PWMXBAR5_G4</a> | 502D 1250h                         |
| 254h   | 32     | <a href="#">CONTROLSS_PWMXBAR5_G5</a> | 502D 1254h                         |
| 258h   | 32     | <a href="#">CONTROLSS_PWMXBAR5_G6</a> | 502D 1258h                         |
| 25Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR5_G7</a> | 502D 125Ch                         |
| 260h   | 32     | <a href="#">CONTROLSS_PWMXBAR5_G8</a> | 502D 1260h                         |
| 280h   | 32     | <a href="#">CONTROLSS_PWMXBAR6_G0</a> | 502D 1280h                         |
| 284h   | 32     | <a href="#">CONTROLSS_PWMXBAR6_G1</a> | 502D 1284h                         |
| 288h   | 32     | <a href="#">CONTROLSS_PWMXBAR6_G2</a> | 502D 1288h                         |
| 28Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR6_G3</a> | 502D 128Ch                         |
| 290h   | 32     | <a href="#">CONTROLSS_PWMXBAR6_G4</a> | 502D 1290h                         |
| 294h   | 32     | <a href="#">CONTROLSS_PWMXBAR6_G5</a> | 502D 1294h                         |
| 298h   | 32     | <a href="#">CONTROLSS_PWMXBAR6_G6</a> | 502D 1298h                         |
| 29Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR6_G7</a> | 502D 129Ch                         |
| 2A0h   | 32     | <a href="#">CONTROLSS_PWMXBAR6_G8</a> | 502D 12A0h                         |
| 2C0h   | 32     | <a href="#">CONTROLSS_PWMXBAR7_G0</a> | 502D 12C0h                         |
| 2C4h   | 32     | <a href="#">CONTROLSS_PWMXBAR7_G1</a> | 502D 12C4h                         |
| 2C8h   | 32     | <a href="#">CONTROLSS_PWMXBAR7_G2</a> | 502D 12C8h                         |
| 2CCh   | 32     | <a href="#">CONTROLSS_PWMXBAR7_G3</a> | 502D 12CCh                         |
| 2D0h   | 32     | <a href="#">CONTROLSS_PWMXBAR7_G4</a> | 502D 12D0h                         |
| 2D4h   | 32     | <a href="#">CONTROLSS_PWMXBAR7_G5</a> | 502D 12D4h                         |
| 2D8h   | 32     | <a href="#">CONTROLSS_PWMXBAR7_G6</a> | 502D 12D8h                         |
| 2DCh   | 32     | <a href="#">CONTROLSS_PWMXBAR7_G7</a> | 502D 12DCh                         |
| 2E0h   | 32     | <a href="#">CONTROLSS_PWMXBAR7_G8</a> | 502D 12E0h                         |
| 300h   | 32     | <a href="#">CONTROLSS_PWMXBAR8_G0</a> | 502D 1300h                         |
| 304h   | 32     | <a href="#">CONTROLSS_PWMXBAR8_G1</a> | 502D 1304h                         |
| 308h   | 32     | <a href="#">CONTROLSS_PWMXBAR8_G2</a> | 502D 1308h                         |
| 30Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR8_G3</a> | 502D 130Ch                         |
| 310h   | 32     | <a href="#">CONTROLSS_PWMXBAR8_G4</a> | 502D 1310h                         |

**Table 3-4018. CONTROLSS Registers, Base Address=502D 1000h, Length=2048 (continued)**

| Offset | Length | Register Name                          | CONTROLSS_PWMXBAR Physical Address |
|--------|--------|----------------------------------------|------------------------------------|
| 314h   | 32     | <a href="#">CONTROLSS_PWMXBAR8_G5</a>  | 502D 1314h                         |
| 318h   | 32     | <a href="#">CONTROLSS_PWMXBAR8_G6</a>  | 502D 1318h                         |
| 31Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR8_G7</a>  | 502D 131Ch                         |
| 320h   | 32     | <a href="#">CONTROLSS_PWMXBAR8_G8</a>  | 502D 1320h                         |
| 340h   | 32     | <a href="#">CONTROLSS_PWMXBAR9_G0</a>  | 502D 1340h                         |
| 344h   | 32     | <a href="#">CONTROLSS_PWMXBAR9_G1</a>  | 502D 1344h                         |
| 348h   | 32     | <a href="#">CONTROLSS_PWMXBAR9_G2</a>  | 502D 1348h                         |
| 34Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR9_G3</a>  | 502D 134Ch                         |
| 350h   | 32     | <a href="#">CONTROLSS_PWMXBAR9_G4</a>  | 502D 1350h                         |
| 354h   | 32     | <a href="#">CONTROLSS_PWMXBAR9_G5</a>  | 502D 1354h                         |
| 358h   | 32     | <a href="#">CONTROLSS_PWMXBAR9_G6</a>  | 502D 1358h                         |
| 35Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR9_G7</a>  | 502D 135Ch                         |
| 360h   | 32     | <a href="#">CONTROLSS_PWMXBAR9_G8</a>  | 502D 1360h                         |
| 380h   | 32     | <a href="#">CONTROLSS_PWMXBAR10_G0</a> | 502D 1380h                         |
| 384h   | 32     | <a href="#">CONTROLSS_PWMXBAR10_G1</a> | 502D 1384h                         |
| 388h   | 32     | <a href="#">CONTROLSS_PWMXBAR10_G2</a> | 502D 1388h                         |
| 38Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR10_G3</a> | 502D 138Ch                         |
| 390h   | 32     | <a href="#">CONTROLSS_PWMXBAR10_G4</a> | 502D 1390h                         |
| 394h   | 32     | <a href="#">CONTROLSS_PWMXBAR10_G5</a> | 502D 1394h                         |
| 398h   | 32     | <a href="#">CONTROLSS_PWMXBAR10_G6</a> | 502D 1398h                         |
| 39Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR10_G7</a> | 502D 139Ch                         |
| 3A0h   | 32     | <a href="#">CONTROLSS_PWMXBAR10_G8</a> | 502D 13A0h                         |
| 3C0h   | 32     | <a href="#">CONTROLSS_PWMXBAR11_G0</a> | 502D 13C0h                         |
| 3C4h   | 32     | <a href="#">CONTROLSS_PWMXBAR11_G1</a> | 502D 13C4h                         |
| 3C8h   | 32     | <a href="#">CONTROLSS_PWMXBAR11_G2</a> | 502D 13C8h                         |
| 3CCh   | 32     | <a href="#">CONTROLSS_PWMXBAR11_G3</a> | 502D 13CCh                         |
| 3D0h   | 32     | <a href="#">CONTROLSS_PWMXBAR11_G4</a> | 502D 13D0h                         |
| 3D4h   | 32     | <a href="#">CONTROLSS_PWMXBAR11_G5</a> | 502D 13D4h                         |
| 3D8h   | 32     | <a href="#">CONTROLSS_PWMXBAR11_G6</a> | 502D 13D8h                         |
| 3DCh   | 32     | <a href="#">CONTROLSS_PWMXBAR11_G7</a> | 502D 13DCh                         |
| 3E0h   | 32     | <a href="#">CONTROLSS_PWMXBAR11_G8</a> | 502D 13E0h                         |
| 400h   | 32     | <a href="#">CONTROLSS_PWMXBAR12_G0</a> | 502D 1400h                         |
| 404h   | 32     | <a href="#">CONTROLSS_PWMXBAR12_G1</a> | 502D 1404h                         |
| 408h   | 32     | <a href="#">CONTROLSS_PWMXBAR12_G2</a> | 502D 1408h                         |
| 40Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR12_G3</a> | 502D 140Ch                         |
| 410h   | 32     | <a href="#">CONTROLSS_PWMXBAR12_G4</a> | 502D 1410h                         |
| 414h   | 32     | <a href="#">CONTROLSS_PWMXBAR12_G5</a> | 502D 1414h                         |
| 418h   | 32     | <a href="#">CONTROLSS_PWMXBAR12_G6</a> | 502D 1418h                         |
| 41Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR12_G7</a> | 502D 141Ch                         |
| 420h   | 32     | <a href="#">CONTROLSS_PWMXBAR12_G8</a> | 502D 1420h                         |
| 440h   | 32     | <a href="#">CONTROLSS_PWMXBAR13_G0</a> | 502D 1440h                         |
| 444h   | 32     | <a href="#">CONTROLSS_PWMXBAR13_G1</a> | 502D 1444h                         |
| 448h   | 32     | <a href="#">CONTROLSS_PWMXBAR13_G2</a> | 502D 1448h                         |
| 44Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR13_G3</a> | 502D 144Ch                         |

**Table 3-4018. CONTROLSS Registers, Base Address=502D 1000h, Length=2048 (continued)**

| Offset | Length | Register Name                          | CONTROLSS_PWMXBAR Physical Address |
|--------|--------|----------------------------------------|------------------------------------|
| 450h   | 32     | <a href="#">CONTROLSS_PWMXBAR13_G4</a> | 502D 1450h                         |
| 454h   | 32     | <a href="#">CONTROLSS_PWMXBAR13_G5</a> | 502D 1454h                         |
| 458h   | 32     | <a href="#">CONTROLSS_PWMXBAR13_G6</a> | 502D 1458h                         |
| 45Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR13_G7</a> | 502D 145Ch                         |
| 460h   | 32     | <a href="#">CONTROLSS_PWMXBAR13_G8</a> | 502D 1460h                         |
| 480h   | 32     | <a href="#">CONTROLSS_PWMXBAR14_G0</a> | 502D 1480h                         |
| 484h   | 32     | <a href="#">CONTROLSS_PWMXBAR14_G1</a> | 502D 1484h                         |
| 488h   | 32     | <a href="#">CONTROLSS_PWMXBAR14_G2</a> | 502D 1488h                         |
| 48Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR14_G3</a> | 502D 148Ch                         |
| 490h   | 32     | <a href="#">CONTROLSS_PWMXBAR14_G4</a> | 502D 1490h                         |
| 494h   | 32     | <a href="#">CONTROLSS_PWMXBAR14_G5</a> | 502D 1494h                         |
| 498h   | 32     | <a href="#">CONTROLSS_PWMXBAR14_G6</a> | 502D 1498h                         |
| 49Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR14_G7</a> | 502D 149Ch                         |
| 4A0h   | 32     | <a href="#">CONTROLSS_PWMXBAR14_G8</a> | 502D 14A0h                         |
| 4C0h   | 32     | <a href="#">CONTROLSS_PWMXBAR15_G0</a> | 502D 14C0h                         |
| 4C4h   | 32     | <a href="#">CONTROLSS_PWMXBAR15_G1</a> | 502D 14C4h                         |
| 4C8h   | 32     | <a href="#">CONTROLSS_PWMXBAR15_G2</a> | 502D 14C8h                         |
| 4CCh   | 32     | <a href="#">CONTROLSS_PWMXBAR15_G3</a> | 502D 14CCh                         |
| 4D0h   | 32     | <a href="#">CONTROLSS_PWMXBAR15_G4</a> | 502D 14D0h                         |
| 4D4h   | 32     | <a href="#">CONTROLSS_PWMXBAR15_G5</a> | 502D 14D4h                         |
| 4D8h   | 32     | <a href="#">CONTROLSS_PWMXBAR15_G6</a> | 502D 14D8h                         |
| 4DCh   | 32     | <a href="#">CONTROLSS_PWMXBAR15_G7</a> | 502D 14DCh                         |
| 4E0h   | 32     | <a href="#">CONTROLSS_PWMXBAR15_G8</a> | 502D 14E0h                         |
| 500h   | 32     | <a href="#">CONTROLSS_PWMXBAR16_G0</a> | 502D 1500h                         |
| 504h   | 32     | <a href="#">CONTROLSS_PWMXBAR16_G1</a> | 502D 1504h                         |
| 508h   | 32     | <a href="#">CONTROLSS_PWMXBAR16_G2</a> | 502D 1508h                         |
| 50Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR16_G3</a> | 502D 150Ch                         |
| 510h   | 32     | <a href="#">CONTROLSS_PWMXBAR16_G4</a> | 502D 1510h                         |
| 514h   | 32     | <a href="#">CONTROLSS_PWMXBAR16_G5</a> | 502D 1514h                         |
| 518h   | 32     | <a href="#">CONTROLSS_PWMXBAR16_G6</a> | 502D 1518h                         |
| 51Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR16_G7</a> | 502D 151Ch                         |
| 520h   | 32     | <a href="#">CONTROLSS_PWMXBAR16_G8</a> | 502D 1520h                         |
| 540h   | 32     | <a href="#">CONTROLSS_PWMXBAR17_G0</a> | 502D 1540h                         |
| 544h   | 32     | <a href="#">CONTROLSS_PWMXBAR17_G1</a> | 502D 1544h                         |
| 548h   | 32     | <a href="#">CONTROLSS_PWMXBAR17_G2</a> | 502D 1548h                         |
| 54Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR17_G3</a> | 502D 154Ch                         |
| 550h   | 32     | <a href="#">CONTROLSS_PWMXBAR17_G4</a> | 502D 1550h                         |
| 554h   | 32     | <a href="#">CONTROLSS_PWMXBAR17_G5</a> | 502D 1554h                         |
| 558h   | 32     | <a href="#">CONTROLSS_PWMXBAR17_G6</a> | 502D 1558h                         |
| 55Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR17_G7</a> | 502D 155Ch                         |
| 560h   | 32     | <a href="#">CONTROLSS_PWMXBAR17_G8</a> | 502D 1560h                         |
| 580h   | 32     | <a href="#">CONTROLSS_PWMXBAR18_G0</a> | 502D 1580h                         |
| 584h   | 32     | <a href="#">CONTROLSS_PWMXBAR18_G1</a> | 502D 1584h                         |
| 588h   | 32     | <a href="#">CONTROLSS_PWMXBAR18_G2</a> | 502D 1588h                         |

**Table 3-4018. CONTROLSS Registers, Base Address=502D 1000h, Length=2048 (continued)**

| Offset | Length | Register Name                          | CONTROLSS_PWMXBAR Physical Address |
|--------|--------|----------------------------------------|------------------------------------|
| 58Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR18_G3</a> | 502D 158Ch                         |
| 590h   | 32     | <a href="#">CONTROLSS_PWMXBAR18_G4</a> | 502D 1590h                         |
| 594h   | 32     | <a href="#">CONTROLSS_PWMXBAR18_G5</a> | 502D 1594h                         |
| 598h   | 32     | <a href="#">CONTROLSS_PWMXBAR18_G6</a> | 502D 1598h                         |
| 59Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR18_G7</a> | 502D 159Ch                         |
| 5A0h   | 32     | <a href="#">CONTROLSS_PWMXBAR18_G8</a> | 502D 15A0h                         |
| 5C0h   | 32     | <a href="#">CONTROLSS_PWMXBAR19_G0</a> | 502D 15C0h                         |
| 5C4h   | 32     | <a href="#">CONTROLSS_PWMXBAR19_G1</a> | 502D 15C4h                         |
| 5C8h   | 32     | <a href="#">CONTROLSS_PWMXBAR19_G2</a> | 502D 15C8h                         |
| 5CCh   | 32     | <a href="#">CONTROLSS_PWMXBAR19_G3</a> | 502D 15CCh                         |
| 5D0h   | 32     | <a href="#">CONTROLSS_PWMXBAR19_G4</a> | 502D 15D0h                         |
| 5D4h   | 32     | <a href="#">CONTROLSS_PWMXBAR19_G5</a> | 502D 15D4h                         |
| 5D8h   | 32     | <a href="#">CONTROLSS_PWMXBAR19_G6</a> | 502D 15D8h                         |
| 5DCh   | 32     | <a href="#">CONTROLSS_PWMXBAR19_G7</a> | 502D 15DCh                         |
| 5E0h   | 32     | <a href="#">CONTROLSS_PWMXBAR19_G8</a> | 502D 15E0h                         |
| 600h   | 32     | <a href="#">CONTROLSS_PWMXBAR20_G0</a> | 502D 1600h                         |
| 604h   | 32     | <a href="#">CONTROLSS_PWMXBAR20_G1</a> | 502D 1604h                         |
| 608h   | 32     | <a href="#">CONTROLSS_PWMXBAR20_G2</a> | 502D 1608h                         |
| 60Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR20_G3</a> | 502D 160Ch                         |
| 610h   | 32     | <a href="#">CONTROLSS_PWMXBAR20_G4</a> | 502D 1610h                         |
| 614h   | 32     | <a href="#">CONTROLSS_PWMXBAR20_G5</a> | 502D 1614h                         |
| 618h   | 32     | <a href="#">CONTROLSS_PWMXBAR20_G6</a> | 502D 1618h                         |
| 61Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR20_G7</a> | 502D 161Ch                         |
| 620h   | 32     | <a href="#">CONTROLSS_PWMXBAR20_G8</a> | 502D 1620h                         |
| 640h   | 32     | <a href="#">CONTROLSS_PWMXBAR21_G0</a> | 502D 1640h                         |
| 644h   | 32     | <a href="#">CONTROLSS_PWMXBAR21_G1</a> | 502D 1644h                         |
| 648h   | 32     | <a href="#">CONTROLSS_PWMXBAR21_G2</a> | 502D 1648h                         |
| 64Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR21_G3</a> | 502D 164Ch                         |
| 650h   | 32     | <a href="#">CONTROLSS_PWMXBAR21_G4</a> | 502D 1650h                         |
| 654h   | 32     | <a href="#">CONTROLSS_PWMXBAR21_G5</a> | 502D 1654h                         |
| 658h   | 32     | <a href="#">CONTROLSS_PWMXBAR21_G6</a> | 502D 1658h                         |
| 65Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR21_G7</a> | 502D 165Ch                         |
| 660h   | 32     | <a href="#">CONTROLSS_PWMXBAR21_G8</a> | 502D 1660h                         |
| 680h   | 32     | <a href="#">CONTROLSS_PWMXBAR22_G0</a> | 502D 1680h                         |
| 684h   | 32     | <a href="#">CONTROLSS_PWMXBAR22_G1</a> | 502D 1684h                         |
| 688h   | 32     | <a href="#">CONTROLSS_PWMXBAR22_G2</a> | 502D 1688h                         |
| 68Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR22_G3</a> | 502D 168Ch                         |
| 690h   | 32     | <a href="#">CONTROLSS_PWMXBAR22_G4</a> | 502D 1690h                         |
| 694h   | 32     | <a href="#">CONTROLSS_PWMXBAR22_G5</a> | 502D 1694h                         |
| 698h   | 32     | <a href="#">CONTROLSS_PWMXBAR22_G6</a> | 502D 1698h                         |
| 69Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR22_G7</a> | 502D 169Ch                         |
| 6A0h   | 32     | <a href="#">CONTROLSS_PWMXBAR22_G8</a> | 502D 16A0h                         |
| 6C0h   | 32     | <a href="#">CONTROLSS_PWMXBAR23_G0</a> | 502D 16C0h                         |
| 6C4h   | 32     | <a href="#">CONTROLSS_PWMXBAR23_G1</a> | 502D 16C4h                         |

**Table 3-4018. CONTROLSS Registers, Base Address=502D 1000h, Length=2048 (continued)**

| Offset | Length | Register Name                          | CONTROLSS_PWMXBAR Physical Address |
|--------|--------|----------------------------------------|------------------------------------|
| 6C8h   | 32     | <a href="#">CONTROLSS_PWMXBAR23_G2</a> | 502D 16C8h                         |
| 6CCh   | 32     | <a href="#">CONTROLSS_PWMXBAR23_G3</a> | 502D 16CCh                         |
| 6D0h   | 32     | <a href="#">CONTROLSS_PWMXBAR23_G4</a> | 502D 16D0h                         |
| 6D4h   | 32     | <a href="#">CONTROLSS_PWMXBAR23_G5</a> | 502D 16D4h                         |
| 6D8h   | 32     | <a href="#">CONTROLSS_PWMXBAR23_G6</a> | 502D 16D8h                         |
| 6DCh   | 32     | <a href="#">CONTROLSS_PWMXBAR23_G7</a> | 502D 16DCh                         |
| 6E0h   | 32     | <a href="#">CONTROLSS_PWMXBAR23_G8</a> | 502D 16E0h                         |
| 700h   | 32     | <a href="#">CONTROLSS_PWMXBAR24_G0</a> | 502D 1700h                         |
| 704h   | 32     | <a href="#">CONTROLSS_PWMXBAR24_G1</a> | 502D 1704h                         |
| 708h   | 32     | <a href="#">CONTROLSS_PWMXBAR24_G2</a> | 502D 1708h                         |
| 70Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR24_G3</a> | 502D 170Ch                         |
| 710h   | 32     | <a href="#">CONTROLSS_PWMXBAR24_G4</a> | 502D 1710h                         |
| 714h   | 32     | <a href="#">CONTROLSS_PWMXBAR24_G5</a> | 502D 1714h                         |
| 718h   | 32     | <a href="#">CONTROLSS_PWMXBAR24_G6</a> | 502D 1718h                         |
| 71Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR24_G7</a> | 502D 171Ch                         |
| 720h   | 32     | <a href="#">CONTROLSS_PWMXBAR24_G8</a> | 502D 1720h                         |
| 740h   | 32     | <a href="#">CONTROLSS_PWMXBAR25_G0</a> | 502D 1740h                         |
| 744h   | 32     | <a href="#">CONTROLSS_PWMXBAR25_G1</a> | 502D 1744h                         |
| 748h   | 32     | <a href="#">CONTROLSS_PWMXBAR25_G2</a> | 502D 1748h                         |
| 74Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR25_G3</a> | 502D 174Ch                         |
| 750h   | 32     | <a href="#">CONTROLSS_PWMXBAR25_G4</a> | 502D 1750h                         |
| 754h   | 32     | <a href="#">CONTROLSS_PWMXBAR25_G5</a> | 502D 1754h                         |
| 758h   | 32     | <a href="#">CONTROLSS_PWMXBAR25_G6</a> | 502D 1758h                         |
| 75Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR25_G7</a> | 502D 175Ch                         |
| 760h   | 32     | <a href="#">CONTROLSS_PWMXBAR25_G8</a> | 502D 1760h                         |
| 780h   | 32     | <a href="#">CONTROLSS_PWMXBAR26_G0</a> | 502D 1780h                         |
| 784h   | 32     | <a href="#">CONTROLSS_PWMXBAR26_G1</a> | 502D 1784h                         |
| 788h   | 32     | <a href="#">CONTROLSS_PWMXBAR26_G2</a> | 502D 1788h                         |
| 78Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR26_G3</a> | 502D 178Ch                         |
| 790h   | 32     | <a href="#">CONTROLSS_PWMXBAR26_G4</a> | 502D 1790h                         |
| 794h   | 32     | <a href="#">CONTROLSS_PWMXBAR26_G5</a> | 502D 1794h                         |
| 798h   | 32     | <a href="#">CONTROLSS_PWMXBAR26_G6</a> | 502D 1798h                         |
| 79Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR26_G7</a> | 502D 179Ch                         |
| 7A0h   | 32     | <a href="#">CONTROLSS_PWMXBAR26_G8</a> | 502D 17A0h                         |
| 7C0h   | 32     | <a href="#">CONTROLSS_PWMXBAR27_G0</a> | 502D 17C0h                         |
| 7C4h   | 32     | <a href="#">CONTROLSS_PWMXBAR27_G1</a> | 502D 17C4h                         |
| 7C8h   | 32     | <a href="#">CONTROLSS_PWMXBAR27_G2</a> | 502D 17C8h                         |
| 7CCh   | 32     | <a href="#">CONTROLSS_PWMXBAR27_G3</a> | 502D 17CCh                         |
| 7D0h   | 32     | <a href="#">CONTROLSS_PWMXBAR27_G4</a> | 502D 17D0h                         |
| 7D4h   | 32     | <a href="#">CONTROLSS_PWMXBAR27_G5</a> | 502D 17D4h                         |
| 7D8h   | 32     | <a href="#">CONTROLSS_PWMXBAR27_G6</a> | 502D 17D8h                         |
| 7DCh   | 32     | <a href="#">CONTROLSS_PWMXBAR27_G7</a> | 502D 17DCh                         |
| 7E0h   | 32     | <a href="#">CONTROLSS_PWMXBAR27_G8</a> | 502D 17E0h                         |
| 800h   | 32     | <a href="#">CONTROLSS_PWMXBAR28_G0</a> | 502D 1800h                         |

**Table 3-4018. CONTROLSS Registers, Base Address=502D 1000h, Length=2048 (continued)**

| Offset | Length | Register Name                          | CONTROLSS_PWMXBAR Physical Address |
|--------|--------|----------------------------------------|------------------------------------|
| 804h   | 32     | <a href="#">CONTROLSS_PWMXBAR28_G1</a> | 502D 1804h                         |
| 808h   | 32     | <a href="#">CONTROLSS_PWMXBAR28_G2</a> | 502D 1808h                         |
| 80Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR28_G3</a> | 502D 180Ch                         |
| 810h   | 32     | <a href="#">CONTROLSS_PWMXBAR28_G4</a> | 502D 1810h                         |
| 814h   | 32     | <a href="#">CONTROLSS_PWMXBAR28_G5</a> | 502D 1814h                         |
| 818h   | 32     | <a href="#">CONTROLSS_PWMXBAR28_G6</a> | 502D 1818h                         |
| 81Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR28_G7</a> | 502D 181Ch                         |
| 820h   | 32     | <a href="#">CONTROLSS_PWMXBAR28_G8</a> | 502D 1820h                         |
| 840h   | 32     | <a href="#">CONTROLSS_PWMXBAR29_G0</a> | 502D 1840h                         |
| 844h   | 32     | <a href="#">CONTROLSS_PWMXBAR29_G1</a> | 502D 1844h                         |
| 848h   | 32     | <a href="#">CONTROLSS_PWMXBAR29_G2</a> | 502D 1848h                         |
| 84Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR29_G3</a> | 502D 184Ch                         |
| 850h   | 32     | <a href="#">CONTROLSS_PWMXBAR29_G4</a> | 502D 1850h                         |
| 854h   | 32     | <a href="#">CONTROLSS_PWMXBAR29_G5</a> | 502D 1854h                         |
| 858h   | 32     | <a href="#">CONTROLSS_PWMXBAR29_G6</a> | 502D 1858h                         |
| 85Ch   | 32     | <a href="#">CONTROLSS_PWMXBAR29_G7</a> | 502D 185Ch                         |
| 860h   | 32     | <a href="#">CONTROLSS_PWMXBAR29_G8</a> | 502D 1860h                         |

### 3.20.2 CONTROLSS\_PWMXBAR Registers

#### CONTROLSS\_PWMXBAR Registers

### 3.20.2.1 CONTROLSS\_PWMXBAR\_STATUS Register

#### 1 CONTROLSS\_PWMXBAR\_STATUS Register (Offset = 10h) [reset = 0h]

Output Signal Status.

Return to [Summary Table](#)

**Table 3-4019. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1010h       |

**Figure 3-1315. CONTROLSS\_PWMXBAR\_STATUS Name Register**

|                    |    |                    |    |    |    |    |    |
|--------------------|----|--------------------|----|----|----|----|----|
| 31                 | 30 | 29                 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    | PWMXBAR_STATUS_STS |    |    |    |    |    |
| NONE               |    | R                  |    |    |    |    |    |
| 0h                 |    | 0h                 |    |    |    |    |    |
| 23                 | 22 | 21                 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR_STATUS_STS |    |                    |    |    |    |    |    |
| R                  |    |                    |    |    |    |    |    |
| 0h                 |    |                    |    |    |    |    |    |
| 15                 | 14 | 13                 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR_STATUS_STS |    |                    |    |    |    |    |    |
| R                  |    |                    |    |    |    |    |    |
| 0h                 |    |                    |    |    |    |    |    |
| 7                  | 6  | 5                  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR_STATUS_STS |    |                    |    |    |    |    |    |
| R                  |    |                    |    |    |    |    |    |
| 0h                 |    |                    |    |    |    |    |    |

**Table 3-4021. CONTROLSS\_PWMXBAR\_STATUS Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description          |
|-------|--------------------|------|-------|----------------------|
| 31:30 | RESERVED           | NONE | 0h    | Reserved             |
| 29:0  | PWMXBAR_STATUS_STS | R    | 0h    | Output Signal Status |



### 3.20.2.2 CONTROLSS\_PWMXBAR\_FLAGINVERT Register

#### 1 CONTROLSS\_PWMXBAR\_FLAGINVERT Register (Offset = 14h) [reset = 0h]

Output Signal Invert Before Latch.

Return to [Summary Table](#)

**Table 3-4022. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1014h       |

**Figure 3-1316. CONTROLSS\_PWMXBAR\_FLAGINVERT Name Register**

|                           |    |                           |    |    |    |    |    |
|---------------------------|----|---------------------------|----|----|----|----|----|
| 31                        | 30 | 29                        | 28 | 27 | 26 | 25 | 24 |
| RESERVED                  |    | PWMXBAR_FLAGINVERT_INVERT |    |    |    |    |    |
| NONE                      |    | R/W                       |    |    |    |    |    |
| 0h                        |    | 0h                        |    |    |    |    |    |
| 23                        | 22 | 21                        | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR_FLAGINVERT_INVERT |    |                           |    |    |    |    |    |
| R/W                       |    |                           |    |    |    |    |    |
| 0h                        |    |                           |    |    |    |    |    |
| 15                        | 14 | 13                        | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR_FLAGINVERT_INVERT |    |                           |    |    |    |    |    |
| R/W                       |    |                           |    |    |    |    |    |
| 0h                        |    |                           |    |    |    |    |    |
| 7                         | 6  | 5                         | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR_FLAGINVERT_INVERT |    |                           |    |    |    |    |    |
| R/W                       |    |                           |    |    |    |    |    |
| 0h                        |    |                           |    |    |    |    |    |

**Table 3-4024. CONTROLSS\_PWMXBAR\_FLAGINVERT Register Field Descriptions**

| Bit   | Field                     | Type | Reset | Description                       |
|-------|---------------------------|------|-------|-----------------------------------|
| 31:30 | RESERVED                  | NONE | 0h    | Reserved                          |
| 29:0  | PWMXBAR_FLAGINVERT_INVERT | R/W  | 0h    | Output Signal Invert Before Latch |

### 3.20.2.3 CONTROLSS\_PWMXBAR\_FLAG Register

#### 1 CONTROLSS\_PWMXBAR\_FLAG Register (Offset = 18h) [reset = 0h]

Output Signal Latched Flag.

Return to [Summary Table](#)

**Table 3-4025. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1018h       |

**Figure 3-1317. CONTROLSS\_PWMXBAR\_FLAG Name Register**

| 31                     | 30                     | 29                     | 28                     | 27                     | 26                     | 25                     | 24                     |
|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|
| RESERVED               | PWMXBAR_FL<br>AG_BIT29 | PWMXBAR_FL<br>AG_BIT28 | PWMXBAR_FL<br>AG_BIT27 | PWMXBAR_FL<br>AG_BIT26 | PWMXBAR_FL<br>AG_BIT25 | PWMXBAR_FL<br>AG_BIT24 |                        |
| NONE                   | R/W                    | R/W                    | R/W                    | R/W                    | R/W                    | R/W                    | R/W                    |
| 0h                     | 0h                     | 0h                     | 0h                     | 0h                     | 0h                     | 0h                     | 0h                     |
| 23                     | 22                     | 21                     | 20                     | 19                     | 18                     | 17                     | 16                     |
| PWMXBAR_FL<br>AG_BIT23 | PWMXBAR_FL<br>AG_BIT22 | PWMXBAR_FL<br>AG_BIT21 | PWMXBAR_FL<br>AG_BIT20 | PWMXBAR_FL<br>AG_BIT19 | PWMXBAR_FL<br>AG_BIT18 | PWMXBAR_FL<br>AG_BIT17 | PWMXBAR_FL<br>AG_BIT16 |
| R/W                    | R/W                    | R/W                    | R/W                    | R/W                    | R/W                    | R/W                    | R/W                    |
| 0h                     | 0h                     | 0h                     | 0h                     | 0h                     | 0h                     | 0h                     | 0h                     |
| 15                     | 14                     | 13                     | 12                     | 11                     | 10                     | 9                      | 8                      |
| PWMXBAR_FL<br>AG_BIT15 | PWMXBAR_FL<br>AG_BIT14 | PWMXBAR_FL<br>AG_BIT13 | PWMXBAR_FL<br>AG_BIT12 | PWMXBAR_FL<br>AG_BIT11 | PWMXBAR_FL<br>AG_BIT10 | PWMXBAR_FL<br>AG_BIT9  | PWMXBAR_FL<br>AG_BIT8  |
| R/W                    | R/W                    | R/W                    | R/W                    | R/W                    | R/W                    | R/W                    | R/W                    |
| 0h                     | 0h                     | 0h                     | 0h                     | 0h                     | 0h                     | 0h                     | 0h                     |
| 7                      | 6                      | 5                      | 4                      | 3                      | 2                      | 1                      | 0                      |
| PWMXBAR_FL<br>AG_BIT7  | PWMXBAR_FL<br>AG_BIT6  | PWMXBAR_FL<br>AG_BIT5  | PWMXBAR_FL<br>AG_BIT4  | PWMXBAR_FL<br>AG_BIT3  | PWMXBAR_FL<br>AG_BIT2  | PWMXBAR_FL<br>AG_BIT1  | PWMXBAR_FL<br>AG_BIT0  |
| R/W                    | R/W                    | R/W                    | R/W                    | R/W                    | R/W                    | R/W                    | R/W                    |
| 0h                     | 0h                     | 0h                     | 0h                     | 0h                     | 0h                     | 0h                     | 0h                     |

**Table 3-4027. CONTROLSS\_PWMXBAR\_FLAG Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                |
|-------|--------------------|------|-------|----------------------------|
| 31:30 | RESERVED           | NONE | 0h    | Reserved                   |
| 29    | PWMXBAR_FLAG_BIT29 | R/W  | 0h    | Output Signal Latched Flag |
| 28    | PWMXBAR_FLAG_BIT28 | R/W  | 0h    | Output Signal Latched Flag |
| 27    | PWMXBAR_FLAG_BIT27 | R/W  | 0h    | Output Signal Latched Flag |
| 26    | PWMXBAR_FLAG_BIT26 | R/W  | 0h    | Output Signal Latched Flag |
| 25    | PWMXBAR_FLAG_BIT25 | R/W  | 0h    | Output Signal Latched Flag |
| 24    | PWMXBAR_FLAG_BIT24 | R/W  | 0h    | Output Signal Latched Flag |
| 23    | PWMXBAR_FLAG_BIT23 | R/W  | 0h    | Output Signal Latched Flag |
| 22    | PWMXBAR_FLAG_BIT22 | R/W  | 0h    | Output Signal Latched Flag |
| 21    | PWMXBAR_FLAG_BIT21 | R/W  | 0h    | Output Signal Latched Flag |
| 20    | PWMXBAR_FLAG_BIT20 | R/W  | 0h    | Output Signal Latched Flag |
| 19    | PWMXBAR_FLAG_BIT19 | R/W  | 0h    | Output Signal Latched Flag |
| 18    | PWMXBAR_FLAG_BIT18 | R/W  | 0h    | Output Signal Latched Flag |
| 17    | PWMXBAR_FLAG_BIT17 | R/W  | 0h    | Output Signal Latched Flag |
| 16    | PWMXBAR_FLAG_BIT16 | R/W  | 0h    | Output Signal Latched Flag |

**Table 3-4027. CONTROLSS\_PWMXBAR\_FLAG Register Field Descriptions (continued)**

| Bit | Field              | Type | Reset | Description                |
|-----|--------------------|------|-------|----------------------------|
| 15  | PWMXBAR_FLAG_BIT15 | R/W  | 0h    | Output Signal Latched Flag |
| 14  | PWMXBAR_FLAG_BIT14 | R/W  | 0h    | Output Signal Latched Flag |
| 13  | PWMXBAR_FLAG_BIT13 | R/W  | 0h    | Output Signal Latched Flag |
| 12  | PWMXBAR_FLAG_BIT12 | R/W  | 0h    | Output Signal Latched Flag |
| 11  | PWMXBAR_FLAG_BIT11 | R/W  | 0h    | Output Signal Latched Flag |
| 10  | PWMXBAR_FLAG_BIT10 | R/W  | 0h    | Output Signal Latched Flag |
| 9   | PWMXBAR_FLAG_BIT9  | R/W  | 0h    | Output Signal Latched Flag |
| 8   | PWMXBAR_FLAG_BIT8  | R/W  | 0h    | Output Signal Latched Flag |
| 7   | PWMXBAR_FLAG_BIT7  | R/W  | 0h    | Output Signal Latched Flag |
| 6   | PWMXBAR_FLAG_BIT6  | R/W  | 0h    | Output Signal Latched Flag |
| 5   | PWMXBAR_FLAG_BIT5  | R/W  | 0h    | Output Signal Latched Flag |
| 4   | PWMXBAR_FLAG_BIT4  | R/W  | 0h    | Output Signal Latched Flag |
| 3   | PWMXBAR_FLAG_BIT3  | R/W  | 0h    | Output Signal Latched Flag |
| 2   | PWMXBAR_FLAG_BIT2  | R/W  | 0h    | Output Signal Latched Flag |
| 1   | PWMXBAR_FLAG_BIT1  | R/W  | 0h    | Output Signal Latched Flag |
| 0   | PWMXBAR_FLAG_BIT0  | R/W  | 0h    | Output Signal Latched Flag |

### 3.20.2.4 CONTROLSS\_PWMXBAR\_FLAG\_CLR Register

#### 1 CONTROLSS\_PWMXBAR\_FLAG\_CLR Register (Offset = 1Ch) [reset = 0h]

Output Signal Latched Flag Clear.

Return to [Summary Table](#)

**Table 3-4028. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 101Ch       |

**Figure 3-1318. CONTROLSS\_PWMXBAR\_FLAG\_CLR Name Register**

| 31                         | 30                         | 29                         | 28                         | 27                         | 26                         | 25                         | 24                         |
|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| RESERVED                   | PWMXBAR_FL<br>AG_CLR_BIT29 | PWMXBAR_FL<br>AG_CLR_BIT28 | PWMXBAR_FL<br>AG_CLR_BIT27 | PWMXBAR_FL<br>AG_CLR_BIT26 | PWMXBAR_FL<br>AG_CLR_BIT25 | PWMXBAR_FL<br>AG_CLR_BIT24 |                            |
| NONE                       | R/W                        | R/W                        | R/W                        | R/W                        | R/W                        | R/W                        | R/W                        |
| 0h                         | 0h                         | 0h                         | 0h                         | 0h                         | 0h                         | 0h                         | 0h                         |
| 23                         | 22                         | 21                         | 20                         | 19                         | 18                         | 17                         | 16                         |
| PWMXBAR_FL<br>AG_CLR_BIT23 | PWMXBAR_FL<br>AG_CLR_BIT22 | PWMXBAR_FL<br>AG_CLR_BIT21 | PWMXBAR_FL<br>AG_CLR_BIT20 | PWMXBAR_FL<br>AG_CLR_BIT19 | PWMXBAR_FL<br>AG_CLR_BIT18 | PWMXBAR_FL<br>AG_CLR_BIT17 | PWMXBAR_FL<br>AG_CLR_BIT16 |
| R/W                        | R/W                        | R/W                        | R/W                        | R/W                        | R/W                        | R/W                        | R/W                        |
| 0h                         | 0h                         | 0h                         | 0h                         | 0h                         | 0h                         | 0h                         | 0h                         |
| 15                         | 14                         | 13                         | 12                         | 11                         | 10                         | 9                          | 8                          |
| PWMXBAR_FL<br>AG_CLR_BIT15 | PWMXBAR_FL<br>AG_CLR_BIT14 | PWMXBAR_FL<br>AG_CLR_BIT13 | PWMXBAR_FL<br>AG_CLR_BIT12 | PWMXBAR_FL<br>AG_CLR_BIT11 | PWMXBAR_FL<br>AG_CLR_BIT10 | PWMXBAR_FL<br>AG_CLR_BIT9  | PWMXBAR_FL<br>AG_CLR_BIT8  |
| R/W                        | R/W                        | R/W                        | R/W                        | R/W                        | R/W                        | R/W                        | R/W                        |
| 0h                         | 0h                         | 0h                         | 0h                         | 0h                         | 0h                         | 0h                         | 0h                         |
| 7                          | 6                          | 5                          | 4                          | 3                          | 2                          | 1                          | 0                          |
| PWMXBAR_FL<br>AG_CLR_BIT7  | PWMXBAR_FL<br>AG_CLR_BIT6  | PWMXBAR_FL<br>AG_CLR_BIT5  | PWMXBAR_FL<br>AG_CLR_BIT4  | PWMXBAR_FL<br>AG_CLR_BIT3  | PWMXBAR_FL<br>AG_CLR_BIT2  | PWMXBAR_FL<br>AG_CLR_BIT1  | PWMXBAR_FL<br>AG_CLR_BIT0  |
| R/W                        | R/W                        | R/W                        | R/W                        | R/W                        | R/W                        | R/W                        | R/W                        |
| 0h                         | 0h                         | 0h                         | 0h                         | 0h                         | 0h                         | 0h                         | 0h                         |

**Table 3-4030. CONTROLSS\_PWMXBAR\_FLAG\_CLR Register Field Descriptions**

| Bit   | Field                  | Type | Reset | Description                      |
|-------|------------------------|------|-------|----------------------------------|
| 31:30 | RESERVED               | NONE | 0h    | Reserved                         |
| 29    | PWMXBAR_FLAG_CLR_BIT29 | R/W  | 0h    | Output Signal Latched Flag Clear |
| 28    | PWMXBAR_FLAG_CLR_BIT28 | R/W  | 0h    | Output Signal Latched Flag Clear |
| 27    | PWMXBAR_FLAG_CLR_BIT27 | R/W  | 0h    | Output Signal Latched Flag Clear |
| 26    | PWMXBAR_FLAG_CLR_BIT26 | R/W  | 0h    | Output Signal Latched Flag Clear |
| 25    | PWMXBAR_FLAG_CLR_BIT25 | R/W  | 0h    | Output Signal Latched Flag Clear |
| 24    | PWMXBAR_FLAG_CLR_BIT24 | R/W  | 0h    | Output Signal Latched Flag Clear |
| 23    | PWMXBAR_FLAG_CLR_BIT23 | R/W  | 0h    | Output Signal Latched Flag Clear |
| 22    | PWMXBAR_FLAG_CLR_BIT22 | R/W  | 0h    | Output Signal Latched Flag Clear |

**Table 3-4030. CONTROLSS\_PWMXBAR\_FLAG\_CLR Register Field Descriptions (continued)**

| Bit | Field                  | Type | Reset | Description                      |
|-----|------------------------|------|-------|----------------------------------|
| 21  | PWMXBAR_FLAG_CLR_BIT21 | R/W  | 0h    | Output Signal Latched Flag Clear |
| 20  | PWMXBAR_FLAG_CLR_BIT20 | R/W  | 0h    | Output Signal Latched Flag Clear |
| 19  | PWMXBAR_FLAG_CLR_BIT19 | R/W  | 0h    | Output Signal Latched Flag Clear |
| 18  | PWMXBAR_FLAG_CLR_BIT18 | R/W  | 0h    | Output Signal Latched Flag Clear |
| 17  | PWMXBAR_FLAG_CLR_BIT17 | R/W  | 0h    | Output Signal Latched Flag Clear |
| 16  | PWMXBAR_FLAG_CLR_BIT16 | R/W  | 0h    | Output Signal Latched Flag Clear |
| 15  | PWMXBAR_FLAG_CLR_BIT15 | R/W  | 0h    | Output Signal Latched Flag Clear |
| 14  | PWMXBAR_FLAG_CLR_BIT14 | R/W  | 0h    | Output Signal Latched Flag Clear |
| 13  | PWMXBAR_FLAG_CLR_BIT13 | R/W  | 0h    | Output Signal Latched Flag Clear |
| 12  | PWMXBAR_FLAG_CLR_BIT12 | R/W  | 0h    | Output Signal Latched Flag Clear |
| 11  | PWMXBAR_FLAG_CLR_BIT11 | R/W  | 0h    | Output Signal Latched Flag Clear |
| 10  | PWMXBAR_FLAG_CLR_BIT10 | R/W  | 0h    | Output Signal Latched Flag Clear |
| 9   | PWMXBAR_FLAG_CLR_BIT9  | R/W  | 0h    | Output Signal Latched Flag Clear |
| 8   | PWMXBAR_FLAG_CLR_BIT8  | R/W  | 0h    | Output Signal Latched Flag Clear |
| 7   | PWMXBAR_FLAG_CLR_BIT7  | R/W  | 0h    | Output Signal Latched Flag Clear |
| 6   | PWMXBAR_FLAG_CLR_BIT6  | R/W  | 0h    | Output Signal Latched Flag Clear |
| 5   | PWMXBAR_FLAG_CLR_BIT5  | R/W  | 0h    | Output Signal Latched Flag Clear |
| 4   | PWMXBAR_FLAG_CLR_BIT4  | R/W  | 0h    | Output Signal Latched Flag Clear |
| 3   | PWMXBAR_FLAG_CLR_BIT3  | R/W  | 0h    | Output Signal Latched Flag Clear |
| 2   | PWMXBAR_FLAG_CLR_BIT2  | R/W  | 0h    | Output Signal Latched Flag Clear |
| 1   | PWMXBAR_FLAG_CLR_BIT1  | R/W  | 0h    | Output Signal Latched Flag Clear |
| 0   | PWMXBAR_FLAG_CLR_BIT0  | R/W  | 0h    | Output Signal Latched Flag Clear |

### 3.20.2.5 CONTROLSS\_PWMXBAR0\_G0 Register

#### 1 CONTROLSS\_PWMXBAR0\_G0 Register (Offset = 100h) [reset = 0h]

PWM XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-4031. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1100h       |

**Figure 3-1319. CONTROLSS\_PWMXBAR0\_G0 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR0_G0_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR0_G0_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR0_G0_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4033. CONTROLSS\_PWMXBAR0\_G0 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | PWMXBAR0_G0_SEL | R/W  | 0h    | PWM XBAR0 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |

### 3.20.2.6 CONTROLSS\_PWMXBAR0\_G1 Register

#### 1 CONTROLSS\_PWMXBAR0\_G1 Register (Offset = 104h) [reset = 0h]

PWM XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-4034. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1104h       |

**Figure 3-1320. CONTROLSS\_PWMXBAR0\_G1 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR0_G1_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR0_G1_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR0_G1_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4036. CONTROLSS\_PWMXBAR0\_G1 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | PWMXBAR0_G1_SEL | R/W  | 0h    | PWM XBAR0 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.7 CONTROLSS\_PWMXBAR0\_G2 Register

#### 1 CONTROLSS\_PWMXBAR0\_G2 Register (Offset = 108h) [reset = 0h]

PWM XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-4037. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1108h       |

**Figure 3-1321. CONTROLSS\_PWMXBAR0\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR0_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR0_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR0_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4039. CONTROLSS\_PWMXBAR0\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |



**Table 3-4039. CONTROLSS\_PWMXBAR0\_G2 Register Field Descriptions (continued)**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR0_G2_SEL | R/W  | 0h    | PWM XBAR0 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.8 CONTROLSS\_PWMXBAR0\_G3 Register

#### 1 CONTROLSS\_PWMXBAR0\_G3 Register (Offset = 10Ch) [reset = 0h]

PWM XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-4040. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 110Ch       |

**Figure 3-1322. CONTROLSS\_PWMXBAR0\_G3 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR0_G3_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR0_G3_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR0_G3_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4042. CONTROLSS\_PWMXBAR0\_G3 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                      |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                         |
| 19:0  | PWMXBAR0_G3_SEL | R/W  | 0h    | PWM XBAR0 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.20.2.9 CONTROLSS\_PWMXBAR0\_G4 Register

#### 1 CONTROLSS\_PWMXBAR0\_G4 Register (Offset = 110h) [reset = 0h]

PWM XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-4043. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1110h       |

**Figure 3-1323. CONTROLSS\_PWMXBAR0\_G4 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR0_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR0_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR0_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR0_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4045. CONTROLSS\_PWMXBAR0\_G4 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                    |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR0_G4_SEL | R/W  | 0h    | PWM XBAR0 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.10 CONTROLSS\_PWMXBAR0\_G5 Register

#### 1 CONTROLSS\_PWMXBAR0\_G5 Register (Offset = 114h) [reset = 0h]

PWM XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-4046. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1114h       |

**Figure 3-1324. CONTROLSS\_PWMXBAR0\_G5 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR0_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR0_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR0_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR0_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4048. CONTROLSS\_PWMXBAR0\_G5 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR0_G5_SEL | R/W  | 0h    | PWM XBAR0 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |

### 3.20.2.11 CONTROLSS\_PWMXBAR0\_G6 Register

#### 1 CONTROLSS\_PWMXBAR0\_G6 Register (Offset = 118h) [reset = 0h]

PWM XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-4049. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1118h       |

**Figure 3-1325. CONTROLSS\_PWMXBAR0\_G6 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR0_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR0_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR0_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR0_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4051. CONTROLSS\_PWMXBAR0\_G6 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR0_G6_SEL | R/W  | 0h    | PWM XBAR0 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.12 CONTROLSS\_PWMXBAR0\_G7 Register

#### 1 CONTROLSS\_PWMXBAR0\_G7 Register (Offset = 11Ch) [reset = 0h]

PWM XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-4052. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 111Ch       |

**Figure 3-1326. CONTROLSS\_PWMXBAR0\_G7 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR0_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR0_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR0_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR0_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4054. CONTROLSS\_PWMXBAR0\_G7 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                 |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR0_G7_SEL | R/W  | 0h    | PWM XBAR0 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |

### 3.20.2.13 CONTROLSS\_PWMXBAR0\_G8 Register

#### 1 CONTROLSS\_PWMXBAR0\_G8 Register (Offset = 120h) [reset = 0h]

PWM XBAR 0 Input Select.

Return to [Summary Table](#)

**Table 3-4055. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1120h       |

**Figure 3-1327. CONTROLSS\_PWMXBAR0\_G8 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    | PWMXBAR0_G8_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| PWMXBAR0_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR0_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR0_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4057. CONTROLSS\_PWMXBAR0\_G8 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                       |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                          |
| 28:0  | PWMXBAR0_G8_SEL | R/W  | 0h    | PWM XBAR0 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.14 CONTROLSS\_PWMXBAR1\_G0 Register

#### 1 CONTROLSS\_PWMXBAR1\_G0 Register (Offset = 140h) [reset = 0h]

PWM XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-4058. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1140h       |

**Figure 3-1328. CONTROLSS\_PWMXBAR1\_G0 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR1_G0_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR1_G0_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR1_G0_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4060. CONTROLSS\_PWMXBAR1\_G0 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | PWMXBAR1_G0_SEL | R/W  | 0h    | PWM XBAR1 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |



### 3.20.2.15 CONTROLSS\_PWMXBAR1\_G1 Register

#### 1 CONTROLSS\_PWMXBAR1\_G1 Register (Offset = 144h) [reset = 0h]

PWM XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-4061. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1144h       |

**Figure 3-1329. CONTROLSS\_PWMXBAR1\_G1 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR1_G1_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR1_G1_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR1_G1_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4063. CONTROLSS\_PWMXBAR1\_G1 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | PWMXBAR1_G1_SEL | R/W  | 0h    | PWM XBAR1 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.16 CONTROLSS\_PWMXBAR1\_G2 Register

#### 1 CONTROLSS\_PWMXBAR1\_G2 Register (Offset = 148h) [reset = 0h]

PWM XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-4064. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1148h       |

**Figure 3-1330. CONTROLSS\_PWMXBAR1\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR1_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR1_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR1_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4066. CONTROLSS\_PWMXBAR1\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-4066. CONTROLSS\_PWMXBAR1\_G2 Register Field Descriptions (continued)**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR1_G2_SEL | R/W  | 0h    | PWM XBAR1 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.17 CONTROLSS\_PWMXBAR1\_G3 Register

#### 1 CONTROLSS\_PWMXBAR1\_G3 Register (Offset = 14Ch) [reset = 0h]

PWM XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-4067. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 114Ch       |

**Figure 3-1331. CONTROLSS\_PWMXBAR1\_G3 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR1_G3_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR1_G3_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR1_G3_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4069. CONTROLSS\_PWMXBAR1\_G3 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                      |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                         |
| 19:0  | PWMXBAR1_G3_SEL | R/W  | 0h    | PWM XBAR1 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.20.2.18 CONTROLSS\_PWMXBAR1\_G4 Register

#### 1 CONTROLSS\_PWMXBAR1\_G4 Register (Offset = 150h) [reset = 0h]

PWM XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-4070. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1150h       |

**Figure 3-1332. CONTROLSS\_PWMXBAR1\_G4 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR1_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR1_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR1_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR1_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4072. CONTROLSS\_PWMXBAR1\_G4 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                    |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR1_G4_SEL | R/W  | 0h    | PWM XBAR1 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.19 CONTROLSS\_PWMXBAR1\_G5 Register

#### 1 CONTROLSS\_PWMXBAR1\_G5 Register (Offset = 154h) [reset = 0h]

PWM XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-4073. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1154h       |

**Figure 3-1333. CONTROLSS\_PWMXBAR1\_G5 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR1_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR1_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR1_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR1_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4075. CONTROLSS\_PWMXBAR1\_G5 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR1_G5_SEL | R/W  | 0h    | PWM XBAR1 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |

### 3.20.2.20 CONTROLSS\_PWMXBAR1\_G6 Register

#### 1 CONTROLSS\_PWMXBAR1\_G6 Register (Offset = 158h) [reset = 0h]

PWM XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-4076. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1158h       |

**Figure 3-1334. CONTROLSS\_PWMXBAR1\_G6 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR1_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR1_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR1_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR1_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4078. CONTROLSS\_PWMXBAR1\_G6 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR1_G6_SEL | R/W  | 0h    | PWM XBAR1 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.21 CONTROLSS\_PWMXBAR1\_G7 Register

#### 1 CONTROLSS\_PWMXBAR1\_G7 Register (Offset = 15Ch) [reset = 0h]

PWM XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-4079. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 115Ch       |

**Figure 3-1335. CONTROLSS\_PWMXBAR1\_G7 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR1_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR1_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR1_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR1_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4081. CONTROLSS\_PWMXBAR1\_G7 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                 |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR1_G7_SEL | R/W  | 0h    | PWM XBAR1 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |



### 3.20.2.22 CONTROLSS\_PWMXBAR1\_G8 Register

#### 1 CONTROLSS\_PWMXBAR1\_G8 Register (Offset = 160h) [reset = 0h]

PWM XBAR 1 Input Select.

Return to [Summary Table](#)

**Table 3-4082. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1160h       |

**Figure 3-1336. CONTROLSS\_PWMXBAR1\_G8 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    | PWMXBAR1_G8_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| PWMXBAR1_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR1_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR1_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4084. CONTROLSS\_PWMXBAR1\_G8 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                       |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                          |
| 28:0  | PWMXBAR1_G8_SEL | R/W  | 0h    | PWM XBAR1 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.23 CONTROLSS\_PWMXBAR2\_G0 Register

#### 1 CONTROLSS\_PWMXBAR2\_G0 Register (Offset = 180h) [reset = 0h]

PWM XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-4085. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1180h       |

**Figure 3-1337. CONTROLSS\_PWMXBAR2\_G0 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR2_G0_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR2_G0_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR2_G0_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4087. CONTROLSS\_PWMXBAR2\_G0 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | PWMXBAR2_G0_SEL | R/W  | 0h    | PWM XBAR2 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |

### 3.20.2.24 CONTROLSS\_PWMXBAR2\_G1 Register

#### 1 CONTROLSS\_PWMXBAR2\_G1 Register (Offset = 184h) [reset = 0h]

PWM XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-4088. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1184h       |

**Figure 3-1338. CONTROLSS\_PWMXBAR2\_G1 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR2_G1_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR2_G1_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR2_G1_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4090. CONTROLSS\_PWMXBAR2\_G1 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | PWMXBAR2_G1_SEL | R/W  | 0h    | PWM XBAR2 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.25 CONTROLSS\_PWMXBAR2\_G2 Register

#### 1 CONTROLSS\_PWMXBAR2\_G2 Register (Offset = 188h) [reset = 0h]

PWM XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-4091. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1188h       |

**Figure 3-1339. CONTROLSS\_PWMXBAR2\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR2_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR2_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR2_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4093. CONTROLSS\_PWMXBAR2\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-4093. CONTROLSS\_PWMXBAR2\_G2 Register Field Descriptions (continued)**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR2_G2_SEL | R/W  | 0h    | PWM XBAR2 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.26 CONTROLSS\_PWMXBAR2\_G3 Register

#### 1 CONTROLSS\_PWMXBAR2\_G3 Register (Offset = 18Ch) [reset = 0h]

PWM XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-4094. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 118Ch       |

**Figure 3-1340. CONTROLSS\_PWMXBAR2\_G3 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR2_G3_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR2_G3_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR2_G3_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4096. CONTROLSS\_PWMXBAR2\_G3 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                      |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                         |
| 19:0  | PWMXBAR2_G3_SEL | R/W  | 0h    | PWM XBAR2 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.20.2.27 CONTROLSS\_PWMXBAR2\_G4 Register

#### 1 CONTROLSS\_PWMXBAR2\_G4 Register (Offset = 190h) [reset = 0h]

PWM XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-4097. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1190h       |

**Figure 3-1341. CONTROLSS\_PWMXBAR2\_G4 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR2_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR2_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR2_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR2_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4099. CONTROLSS\_PWMXBAR2\_G4 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                    |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR2_G4_SEL | R/W  | 0h    | PWM XBAR2 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.28 CONTROLSS\_PWMXBAR2\_G5 Register

#### 1 CONTROLSS\_PWMXBAR2\_G5 Register (Offset = 194h) [reset = 0h]

PWM XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-4100. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1194h       |

**Figure 3-1342. CONTROLSS\_PWMXBAR2\_G5 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR2_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR2_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR2_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR2_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4102. CONTROLSS\_PWMXBAR2\_G5 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR2_G5_SEL | R/W  | 0h    | PWM XBAR2 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |



### 3.20.2.29 CONTROLSS\_PWMXBAR2\_G6 Register

#### 1 CONTROLSS\_PWMXBAR2\_G6 Register (Offset = 198h) [reset = 0h]

PWM XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-4103. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1198h       |

**Figure 3-1343. CONTROLSS\_PWMXBAR2\_G6 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR2_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR2_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR2_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR2_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4105. CONTROLSS\_PWMXBAR2\_G6 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR2_G6_SEL | R/W  | 0h    | PWM XBAR2 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.30 CONTROLSS\_PWMXBAR2\_G7 Register

#### 1 CONTROLSS\_PWMXBAR2\_G7 Register (Offset = 19Ch) [reset = 0h]

PWM XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-4106. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 119Ch       |

**Figure 3-1344. CONTROLSS\_PWMXBAR2\_G7 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR2_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR2_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR2_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR2_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4108. CONTROLSS\_PWMXBAR2\_G7 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                 |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR2_G7_SEL | R/W  | 0h    | PWM XBAR2 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |

### 3.20.2.31 CONTROLSS\_PWMXBAR2\_G8 Register

#### 1 CONTROLSS\_PWMXBAR2\_G8 Register (Offset = 1A0h) [reset = 0h]

PWM XBAR 2 Input Select.

Return to [Summary Table](#)

**Table 3-4109. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 11A0h       |

**Figure 3-1345. CONTROLSS\_PWMXBAR2\_G8 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    | PWMXBAR2_G8_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| PWMXBAR2_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR2_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR2_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4111. CONTROLSS\_PWMXBAR2\_G8 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                       |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                          |
| 28:0  | PWMXBAR2_G8_SEL | R/W  | 0h    | PWM XBAR2 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.32 CONTROLSS\_PWMXBAR3\_G0 Register

#### 1 CONTROLSS\_PWMXBAR3\_G0 Register (Offset = 1C0h) [reset = 0h]

PWM XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-4112. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 11C0h       |

**Figure 3-1346. CONTROLSS\_PWMXBAR3\_G0 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR3_G0_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR3_G0_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR3_G0_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4114. CONTROLSS\_PWMXBAR3\_G0 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | PWMXBAR3_G0_SEL | R/W  | 0h    | PWM XBAR3 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |

### 3.20.2.33 CONTROLSS\_PWMXBAR3\_G1 Register

#### 1 CONTROLSS\_PWMXBAR3\_G1 Register (Offset = 1C4h) [reset = 0h]

PWM XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-4115. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 11C4h       |

**Figure 3-1347. CONTROLSS\_PWMXBAR3\_G1 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR3_G1_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR3_G1_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR3_G1_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4117. CONTROLSS\_PWMXBAR3\_G1 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | PWMXBAR3_G1_SEL | R/W  | 0h    | PWM XBAR3 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.34 CONTROLSS\_PWMXBAR3\_G2 Register

#### 1 CONTROLSS\_PWMXBAR3\_G2 Register (Offset = 1C8h) [reset = 0h]

PWM XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-4118. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 11C8h       |

**Figure 3-1348. CONTROLSS\_PWMXBAR3\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR3_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR3_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR3_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4120. CONTROLSS\_PWMXBAR3\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-4120. CONTROLSS\_PWMXBAR3\_G2 Register Field Descriptions (continued)**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR3_G2_SEL | R/W  | 0h    | PWM XBAR3 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.35 CONTROLSS\_PWMXBAR3\_G3 Register

#### 1 CONTROLSS\_PWMXBAR3\_G3 Register (Offset = 1CCh) [reset = 0h]

PWM XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-4121. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 11CCh       |

**Figure 3-1349. CONTROLSS\_PWMXBAR3\_G3 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR3_G3_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR3_G3_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR3_G3_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4123. CONTROLSS\_PWMXBAR3\_G3 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                      |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                         |
| 19:0  | PWMXBAR3_G3_SEL | R/W  | 0h    | PWM XBAR3 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |



### 3.20.2.36 CONTROLSS\_PWMXBAR3\_G4 Register

#### 1 CONTROLSS\_PWMXBAR3\_G4 Register (Offset = 1D0h) [reset = 0h]

PWM XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-4124. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 11D0h       |

**Figure 3-1350. CONTROLSS\_PWMXBAR3\_G4 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR3_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR3_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR3_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR3_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4126. CONTROLSS\_PWMXBAR3\_G4 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                    |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR3_G4_SEL | R/W  | 0h    | PWM XBAR3 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.37 CONTROLSS\_PWMXBAR3\_G5 Register

#### 1 CONTROLSS\_PWMXBAR3\_G5 Register (Offset = 1D4h) [reset = 0h]

PWM XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-4127. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 11D4h       |

**Figure 3-1351. CONTROLSS\_PWMXBAR3\_G5 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR3_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR3_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR3_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR3_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4129. CONTROLSS\_PWMXBAR3\_G5 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR3_G5_SEL | R/W  | 0h    | PWM XBAR3 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |

### 3.20.2.38 CONTROLSS\_PWMXBAR3\_G6 Register

#### 1 CONTROLSS\_PWMXBAR3\_G6 Register (Offset = 1D8h) [reset = 0h]

PWM XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-4130. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 11D8h       |

**Figure 3-1352. CONTROLSS\_PWMXBAR3\_G6 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR3_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR3_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR3_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR3_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4132. CONTROLSS\_PWMXBAR3\_G6 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR3_G6_SEL | R/W  | 0h    | PWM XBAR3 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.39 CONTROLSS\_PWMXBAR3\_G7 Register

#### 1 CONTROLSS\_PWMXBAR3\_G7 Register (Offset = 1DCh) [reset = 0h]

PWM XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-4133. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 11DCh       |

**Figure 3-1353. CONTROLSS\_PWMXBAR3\_G7 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR3_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR3_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR3_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR3_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4135. CONTROLSS\_PWMXBAR3\_G7 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                 |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR3_G7_SEL | R/W  | 0h    | PWM XBAR3 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |

### 3.20.2.40 CONTROLSS\_PWMXBAR3\_G8 Register

#### 1 CONTROLSS\_PWMXBAR3\_G8 Register (Offset = 1E0h) [reset = 0h]

PWM XBAR 3 Input Select.

Return to [Summary Table](#)

**Table 3-4136. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 11E0h       |

**Figure 3-1354. CONTROLSS\_PWMXBAR3\_G8 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    | PWMXBAR3_G8_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| PWMXBAR3_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR3_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR3_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4138. CONTROLSS\_PWMXBAR3\_G8 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                       |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                          |
| 28:0  | PWMXBAR3_G8_SEL | R/W  | 0h    | PWM XBAR3 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.41 CONTROLSS\_PWMXBAR4\_G0 Register

#### 1 CONTROLSS\_PWMXBAR4\_G0 Register (Offset = 200h) [reset = 0h]

PWM XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-4139. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1200h       |

**Figure 3-1355. CONTROLSS\_PWMXBAR4\_G0 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR4_G0_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR4_G0_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR4_G0_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4141. CONTROLSS\_PWMXBAR4\_G0 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | PWMXBAR4_G0_SEL | R/W  | 0h    | PWM XBAR4 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |

### 3.20.2.42 CONTROLSS\_PWMXBAR4\_G1 Register

#### 1 CONTROLSS\_PWMXBAR4\_G1 Register (Offset = 204h) [reset = 0h]

PWM XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-4142. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1204h       |

**Figure 3-1356. CONTROLSS\_PWMXBAR4\_G1 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR4_G1_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR4_G1_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR4_G1_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4144. CONTROLSS\_PWMXBAR4\_G1 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | PWMXBAR4_G1_SEL | R/W  | 0h    | PWM XBAR4 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.43 CONTROLSS\_PWMXBAR4\_G2 Register

#### 1 CONTROLSS\_PWMXBAR4\_G2 Register (Offset = 208h) [reset = 0h]

PWM XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-4145. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1208h       |

**Figure 3-1357. CONTROLSS\_PWMXBAR4\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR4_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR4_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR4_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4147. CONTROLSS\_PWMXBAR4\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |



**Table 3-4147. CONTROLSS\_PWMXBAR4\_G2 Register Field Descriptions (continued)**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR4_G2_SEL | R/W  | 0h    | PWM XBAR4 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.44 CONTROLSS\_PWMXBAR4\_G3 Register

#### 1 CONTROLSS\_PWMXBAR4\_G3 Register (Offset = 20Ch) [reset = 0h]

PWM XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-4148. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 120Ch       |

**Figure 3-1358. CONTROLSS\_PWMXBAR4\_G3 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR4_G3_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR4_G3_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR4_G3_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4150. CONTROLSS\_PWMXBAR4\_G3 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                      |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                         |
| 19:0  | PWMXBAR4_G3_SEL | R/W  | 0h    | PWM XBAR4 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.20.2.45 CONTROLSS\_PWMXBAR4\_G4 Register

#### 1 CONTROLSS\_PWMXBAR4\_G4 Register (Offset = 210h) [reset = 0h]

PWM XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-4151. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1210h       |

**Figure 3-1359. CONTROLSS\_PWMXBAR4\_G4 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR4_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR4_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR4_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR4_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4153. CONTROLSS\_PWMXBAR4\_G4 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                    |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR4_G4_SEL | R/W  | 0h    | PWM XBAR4 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.46 CONTROLSS\_PWMXBAR4\_G5 Register

#### 1 CONTROLSS\_PWMXBAR4\_G5 Register (Offset = 214h) [reset = 0h]

PWM XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-4154. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1214h       |

**Figure 3-1360. CONTROLSS\_PWMXBAR4\_G5 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR4_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR4_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR4_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR4_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4156. CONTROLSS\_PWMXBAR4\_G5 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR4_G5_SEL | R/W  | 0h    | PWM XBAR4 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |

### 3.20.2.47 CONTROLSS\_PWMXBAR4\_G6 Register

#### 1 CONTROLSS\_PWMXBAR4\_G6 Register (Offset = 218h) [reset = 0h]

PWM XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-4157. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1218h       |

**Figure 3-1361. CONTROLSS\_PWMXBAR4\_G6 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR4_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR4_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR4_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR4_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4159. CONTROLSS\_PWMXBAR4\_G6 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR4_G6_SEL | R/W  | 0h    | PWM XBAR4 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.48 CONTROLSS\_PWMXBAR4\_G7 Register

#### 1 CONTROLSS\_PWMXBAR4\_G7 Register (Offset = 21Ch) [reset = 0h]

PWM XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-4160. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 121Ch       |

**Figure 3-1362. CONTROLSS\_PWMXBAR4\_G7 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR4_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR4_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR4_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR4_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4162. CONTROLSS\_PWMXBAR4\_G7 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                 |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR4_G7_SEL | R/W  | 0h    | PWM XBAR4 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |

### 3.20.2.49 CONTROLSS\_PWMXBAR4\_G8 Register

#### 1 CONTROLSS\_PWMXBAR4\_G8 Register (Offset = 220h) [reset = 0h]

PWM XBAR 4 Input Select.

Return to [Summary Table](#)

**Table 3-4163. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1220h       |

**Figure 3-1363. CONTROLSS\_PWMXBAR4\_G8 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    | PWMXBAR4_G8_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| PWMXBAR4_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR4_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR4_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4165. CONTROLSS\_PWMXBAR4\_G8 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                       |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                          |
| 28:0  | PWMXBAR4_G8_SEL | R/W  | 0h    | PWM XBAR4 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.50 CONTROLSS\_PWMXBAR5\_G0 Register

#### 1 CONTROLSS\_PWMXBAR5\_G0 Register (Offset = 240h) [reset = 0h]

PWM XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-4166. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1240h       |

**Figure 3-1364. CONTROLSS\_PWMXBAR5\_G0 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR5_G0_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR5_G0_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR5_G0_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4168. CONTROLSS\_PWMXBAR5\_G0 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | PWMXBAR5_G0_SEL | R/W  | 0h    | PWM XBAR5 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |



### 3.20.2.51 CONTROLSS\_PWMXBAR5\_G1 Register

#### 1 CONTROLSS\_PWMXBAR5\_G1 Register (Offset = 244h) [reset = 0h]

PWM XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-4169. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1244h       |

**Figure 3-1365. CONTROLSS\_PWMXBAR5\_G1 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR5_G1_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR5_G1_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR5_G1_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4171. CONTROLSS\_PWMXBAR5\_G1 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | PWMXBAR5_G1_SEL | R/W  | 0h    | PWM XBAR5 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.52 CONTROLSS\_PWMXBAR5\_G2 Register

#### 1 CONTROLSS\_PWMXBAR5\_G2 Register (Offset = 248h) [reset = 0h]

PWM XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-4172. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1248h       |

**Figure 3-1366. CONTROLSS\_PWMXBAR5\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR5_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR5_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR5_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4174. CONTROLSS\_PWMXBAR5\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-4174. CONTROLSS\_PWMXBAR5\_G2 Register Field Descriptions (continued)**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR5_G2_SEL | R/W  | 0h    | PWM XBAR5 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.53 CONTROLSS\_PWMXBAR5\_G3 Register

#### 1 CONTROLSS\_PWMXBAR5\_G3 Register (Offset = 24Ch) [reset = 0h]

PWM XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-4175. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 124Ch       |

**Figure 3-1367. CONTROLSS\_PWMXBAR5\_G3 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR5_G3_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR5_G3_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR5_G3_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4177. CONTROLSS\_PWMXBAR5\_G3 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                      |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                         |
| 19:0  | PWMXBAR5_G3_SEL | R/W  | 0h    | PWM XBAR5 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.20.2.54 CONTROLSS\_PWMXBAR5\_G4 Register

#### 1 CONTROLSS\_PWMXBAR5\_G4 Register (Offset = 250h) [reset = 0h]

PWM XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-4178. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1250h       |

**Figure 3-1368. CONTROLSS\_PWMXBAR5\_G4 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR5_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR5_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR5_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR5_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4180. CONTROLSS\_PWMXBAR5\_G4 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                    |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR5_G4_SEL | R/W  | 0h    | PWM XBAR5 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.55 CONTROLSS\_PWMXBAR5\_G5 Register

#### 1 CONTROLSS\_PWMXBAR5\_G5 Register (Offset = 254h) [reset = 0h]

PWM XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-4181. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1254h       |

**Figure 3-1369. CONTROLSS\_PWMXBAR5\_G5 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR5_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR5_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR5_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR5_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4183. CONTROLSS\_PWMXBAR5\_G5 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR5_G5_SEL | R/W  | 0h    | PWM XBAR5 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |

### 3.20.2.56 CONTROLSS\_PWMXBAR5\_G6 Register

#### 1 CONTROLSS\_PWMXBAR5\_G6 Register (Offset = 258h) [reset = 0h]

PWM XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-4184. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1258h       |

**Figure 3-1370. CONTROLSS\_PWMXBAR5\_G6 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR5_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR5_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR5_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR5_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4186. CONTROLSS\_PWMXBAR5\_G6 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR5_G6_SEL | R/W  | 0h    | PWM XBAR5 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.57 CONTROLSS\_PWMXBAR5\_G7 Register

#### 1 CONTROLSS\_PWMXBAR5\_G7 Register (Offset = 25Ch) [reset = 0h]

PWM XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-4187. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 125Ch       |

**Figure 3-1371. CONTROLSS\_PWMXBAR5\_G7 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR5_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR5_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR5_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR5_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4189. CONTROLSS\_PWMXBAR5\_G7 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                 |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR5_G7_SEL | R/W  | 0h    | PWM XBAR5 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |



### 3.20.2.58 CONTROLSS\_PWMXBAR5\_G8 Register

#### 1 CONTROLSS\_PWMXBAR5\_G8 Register (Offset = 260h) [reset = 0h]

PWM XBAR 5 Input Select.

Return to [Summary Table](#)

**Table 3-4190. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1260h       |

**Figure 3-1372. CONTROLSS\_PWMXBAR5\_G8 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    | PWMXBAR5_G8_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| PWMXBAR5_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR5_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR5_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4192. CONTROLSS\_PWMXBAR5\_G8 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                       |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                          |
| 28:0  | PWMXBAR5_G8_SEL | R/W  | 0h    | PWM XBAR5 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.59 CONTROLSS\_PWMXBAR6\_G0 Register

#### 1 CONTROLSS\_PWMXBAR6\_G0 Register (Offset = 280h) [reset = 0h]

PWM XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-4193. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1280h       |

**Figure 3-1373. CONTROLSS\_PWMXBAR6\_G0 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR6_G0_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR6_G0_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR6_G0_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4195. CONTROLSS\_PWMXBAR6\_G0 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | PWMXBAR6_G0_SEL | R/W  | 0h    | PWM XBAR6 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |

### 3.20.2.60 CONTROLSS\_PWMXBAR6\_G1 Register

#### 1 CONTROLSS\_PWMXBAR6\_G1 Register (Offset = 284h) [reset = 0h]

PWM XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-4196. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1284h       |

**Figure 3-1374. CONTROLSS\_PWMXBAR6\_G1 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR6_G1_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR6_G1_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR6_G1_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4198. CONTROLSS\_PWMXBAR6\_G1 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | PWMXBAR6_G1_SEL | R/W  | 0h    | PWM XBAR6 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.61 CONTROLSS\_PWMXBAR6\_G2 Register

#### 1 CONTROLSS\_PWMXBAR6\_G2 Register (Offset = 288h) [reset = 0h]

PWM XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-4199. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1288h       |

**Figure 3-1375. CONTROLSS\_PWMXBAR6\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR6_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR6_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR6_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4201. CONTROLSS\_PWMXBAR6\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-4201. CONTROLSS\_PWMXBAR6\_G2 Register Field Descriptions (continued)**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR6_G2_SEL | R/W  | 0h    | PWM XBAR6 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.62 CONTROLSS\_PWMXBAR6\_G3 Register

#### 1 CONTROLSS\_PWMXBAR6\_G3 Register (Offset = 28Ch) [reset = 0h]

PWM XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-4202. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 128Ch       |

**Figure 3-1376. CONTROLSS\_PWMXBAR6\_G3 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR6_G3_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR6_G3_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR6_G3_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4204. CONTROLSS\_PWMXBAR6\_G3 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                      |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                         |
| 19:0  | PWMXBAR6_G3_SEL | R/W  | 0h    | PWM XBAR6 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.20.2.63 CONTROLSS\_PWMXBAR6\_G4 Register

#### 1 CONTROLSS\_PWMXBAR6\_G4 Register (Offset = 290h) [reset = 0h]

PWM XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-4205. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1290h       |

**Figure 3-1377. CONTROLSS\_PWMXBAR6\_G4 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR6_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR6_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR6_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR6_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4207. CONTROLSS\_PWMXBAR6\_G4 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                    |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR6_G4_SEL | R/W  | 0h    | PWM XBAR6 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.64 CONTROLSS\_PWMXBAR6\_G5 Register

#### 1 CONTROLSS\_PWMXBAR6\_G5 Register (Offset = 294h) [reset = 0h]

PWM XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-4208. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1294h       |

**Figure 3-1378. CONTROLSS\_PWMXBAR6\_G5 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR6_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR6_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR6_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR6_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4210. CONTROLSS\_PWMXBAR6\_G5 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR6_G5_SEL | R/W  | 0h    | PWM XBAR6 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |



### 3.20.2.65 CONTROLSS\_PWMXBAR6\_G6 Register

#### 1 CONTROLSS\_PWMXBAR6\_G6 Register (Offset = 298h) [reset = 0h]

PWM XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-4211. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1298h       |

**Figure 3-1379. CONTROLSS\_PWMXBAR6\_G6 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR6_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR6_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR6_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR6_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4213. CONTROLSS\_PWMXBAR6\_G6 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR6_G6_SEL | R/W  | 0h    | PWM XBAR6 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.66 CONTROLSS\_PWMXBAR6\_G7 Register

#### 1 CONTROLSS\_PWMXBAR6\_G7 Register (Offset = 29Ch) [reset = 0h]

PWM XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-4214. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 129Ch       |

**Figure 3-1380. CONTROLSS\_PWMXBAR6\_G7 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR6_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR6_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR6_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR6_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4216. CONTROLSS\_PWMXBAR6\_G7 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                 |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR6_G7_SEL | R/W  | 0h    | PWM XBAR6 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |

### 3.20.2.67 CONTROLSS\_PWMXBAR6\_G8 Register

#### 1 CONTROLSS\_PWMXBAR6\_G8 Register (Offset = 2A0h) [reset = 0h]

PWM XBAR 6 Input Select.

Return to [Summary Table](#)

**Table 3-4217. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 12A0h       |

**Figure 3-1381. CONTROLSS\_PWMXBAR6\_G8 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    | PWMXBAR6_G8_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| PWMXBAR6_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR6_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR6_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4219. CONTROLSS\_PWMXBAR6\_G8 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                       |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                          |
| 28:0  | PWMXBAR6_G8_SEL | R/W  | 0h    | PWM XBAR6 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.68 CONTROLSS\_PWMXBAR7\_G0 Register

#### 1 CONTROLSS\_PWMXBAR7\_G0 Register (Offset = 2C0h) [reset = 0h]

PWM XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-4220. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 12C0h       |

**Figure 3-1382. CONTROLSS\_PWMXBAR7\_G0 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR7_G0_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR7_G0_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR7_G0_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4222. CONTROLSS\_PWMXBAR7\_G0 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | PWMXBAR7_G0_SEL | R/W  | 0h    | PWM XBAR7 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |

### 3.20.2.69 CONTROLSS\_PWMXBAR7\_G1 Register

#### 1 CONTROLSS\_PWMXBAR7\_G1 Register (Offset = 2C4h) [reset = 0h]

PWM XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-4223. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 12C4h       |

**Figure 3-1383. CONTROLSS\_PWMXBAR7\_G1 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR7_G1_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR7_G1_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR7_G1_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4225. CONTROLSS\_PWMXBAR7\_G1 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | PWMXBAR7_G1_SEL | R/W  | 0h    | PWM XBAR7 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.70 CONTROLSS\_PWMXBAR7\_G2 Register

#### 1 CONTROLSS\_PWMXBAR7\_G2 Register (Offset = 2C8h) [reset = 0h]

PWM XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-4226. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 12C8h       |

**Figure 3-1384. CONTROLSS\_PWMXBAR7\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR7_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR7_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR7_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4228. CONTROLSS\_PWMXBAR7\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-4228. CONTROLSS\_PWMXBAR7\_G2 Register Field Descriptions (continued)**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR7_G2_SEL | R/W  | 0h    | PWM XBAR7 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.71 CONTROLSS\_PWMXBAR7\_G3 Register

#### 1 CONTROLSS\_PWMXBAR7\_G3 Register (Offset = 2CCh) [reset = 0h]

PWM XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-4229. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 12CCh       |

**Figure 3-1385. CONTROLSS\_PWMXBAR7\_G3 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR7_G3_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR7_G3_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR7_G3_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4231. CONTROLSS\_PWMXBAR7\_G3 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                      |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                         |
| 19:0  | PWMXBAR7_G3_SEL | R/W  | 0h    | PWM XBAR7 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |



### 3.20.2.72 CONTROLSS\_PWMXBAR7\_G4 Register

#### 1 CONTROLSS\_PWMXBAR7\_G4 Register (Offset = 2D0h) [reset = 0h]

PWM XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-4232. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 12D0h       |

**Figure 3-1386. CONTROLSS\_PWMXBAR7\_G4 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR7_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR7_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR7_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR7_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4234. CONTROLSS\_PWMXBAR7\_G4 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                    |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR7_G4_SEL | R/W  | 0h    | PWM XBAR7 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.73 CONTROLSS\_PWMXBAR7\_G5 Register

#### 1 CONTROLSS\_PWMXBAR7\_G5 Register (Offset = 2D4h) [reset = 0h]

PWM XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-4235. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 12D4h       |

**Figure 3-1387. CONTROLSS\_PWMXBAR7\_G5 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR7_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR7_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR7_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR7_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4237. CONTROLSS\_PWMXBAR7\_G5 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR7_G5_SEL | R/W  | 0h    | PWM XBAR7 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |

### 3.20.2.74 CONTROLSS\_PWMXBAR7\_G6 Register

#### 1 CONTROLSS\_PWMXBAR7\_G6 Register (Offset = 2D8h) [reset = 0h]

PWM XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-4238. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 12D8h       |

**Figure 3-1388. CONTROLSS\_PWMXBAR7\_G6 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR7_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR7_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR7_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR7_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4240. CONTROLSS\_PWMXBAR7\_G6 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR7_G6_SEL | R/W  | 0h    | PWM XBAR7 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.75 CONTROLSS\_PWMXBAR7\_G7 Register

#### 1 CONTROLSS\_PWMXBAR7\_G7 Register (Offset = 2DCh) [reset = 0h]

PWM XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-4241. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 12DCh       |

**Figure 3-1389. CONTROLSS\_PWMXBAR7\_G7 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR7_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR7_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR7_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR7_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4243. CONTROLSS\_PWMXBAR7\_G7 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                 |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR7_G7_SEL | R/W  | 0h    | PWM XBAR7 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |

### 3.20.2.76 CONTROLSS\_PWMXBAR7\_G8 Register

#### 1 CONTROLSS\_PWMXBAR7\_G8 Register (Offset = 2E0h) [reset = 0h]

PWM XBAR 7 Input Select.

Return to [Summary Table](#)

**Table 3-4244. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 12E0h       |

**Figure 3-1390. CONTROLSS\_PWMXBAR7\_G8 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    | PWMXBAR7_G8_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| PWMXBAR7_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR7_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR7_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4246. CONTROLSS\_PWMXBAR7\_G8 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                       |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                          |
| 28:0  | PWMXBAR7_G8_SEL | R/W  | 0h    | PWM XBAR7 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.77 CONTROLSS\_PWMXBAR8\_G0 Register

#### 1 CONTROLSS\_PWMXBAR8\_G0 Register (Offset = 300h) [reset = 0h]

PWM XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-4247. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1300h       |

**Figure 3-1391. CONTROLSS\_PWMXBAR8\_G0 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR8_G0_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR8_G0_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR8_G0_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4249. CONTROLSS\_PWMXBAR8\_G0 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | PWMXBAR8_G0_SEL | R/W  | 0h    | PWM XBAR8 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |

### 3.20.2.78 CONTROLSS\_PWMXBAR8\_G1 Register

#### 1 CONTROLSS\_PWMXBAR8\_G1 Register (Offset = 304h) [reset = 0h]

PWM XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-4250. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1304h       |

**Figure 3-1392. CONTROLSS\_PWMXBAR8\_G1 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR8_G1_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR8_G1_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR8_G1_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4252. CONTROLSS\_PWMXBAR8\_G1 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | PWMXBAR8_G1_SEL | R/W  | 0h    | PWM XBAR8 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.79 CONTROLSS\_PWMXBAR8\_G2 Register

#### 1 CONTROLSS\_PWMXBAR8\_G2 Register (Offset = 308h) [reset = 0h]

PWM XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-4253. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1308h       |

**Figure 3-1393. CONTROLSS\_PWMXBAR8\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR8_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR8_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR8_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4255. CONTROLSS\_PWMXBAR8\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |



**Table 3-4255. CONTROLSS\_PWMXBAR8\_G2 Register Field Descriptions (continued)**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR8_G2_SEL | R/W  | 0h    | PWM XBAR8 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.80 CONTROLSS\_PWMXBAR8\_G3 Register

#### 1 CONTROLSS\_PWMXBAR8\_G3 Register (Offset = 30Ch) [reset = 0h]

PWM XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-4256. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 130Ch       |

**Figure 3-1394. CONTROLSS\_PWMXBAR8\_G3 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR8_G3_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR8_G3_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR8_G3_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4258. CONTROLSS\_PWMXBAR8\_G3 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                      |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                         |
| 19:0  | PWMXBAR8_G3_SEL | R/W  | 0h    | PWM XBAR8 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.20.2.81 CONTROLSS\_PWMXBAR8\_G4 Register

#### 1 CONTROLSS\_PWMXBAR8\_G4 Register (Offset = 310h) [reset = 0h]

PWM XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-4259. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1310h       |

**Figure 3-1395. CONTROLSS\_PWMXBAR8\_G4 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR8_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR8_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR8_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR8_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4261. CONTROLSS\_PWMXBAR8\_G4 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                    |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR8_G4_SEL | R/W  | 0h    | PWM XBAR8 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.82 CONTROLSS\_PWMXBAR8\_G5 Register

#### 1 CONTROLSS\_PWMXBAR8\_G5 Register (Offset = 314h) [reset = 0h]

PWM XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-4262. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1314h       |

**Figure 3-1396. CONTROLSS\_PWMXBAR8\_G5 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR8_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR8_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR8_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR8_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4264. CONTROLSS\_PWMXBAR8\_G5 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR8_G5_SEL | R/W  | 0h    | PWM XBAR8 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |

### 3.20.2.83 CONTROLSS\_PWMXBAR8\_G6 Register

#### 1 CONTROLSS\_PWMXBAR8\_G6 Register (Offset = 318h) [reset = 0h]

PWM XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-4265. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1318h       |

**Figure 3-1397. CONTROLSS\_PWMXBAR8\_G6 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR8_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR8_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR8_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR8_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4267. CONTROLSS\_PWMXBAR8\_G6 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR8_G6_SEL | R/W  | 0h    | PWM XBAR8 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.84 CONTROLSS\_PWMXBAR8\_G7 Register

#### 1 CONTROLSS\_PWMXBAR8\_G7 Register (Offset = 31Ch) [reset = 0h]

PWM XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-4268. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 131Ch       |

**Figure 3-1398. CONTROLSS\_PWMXBAR8\_G7 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR8_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR8_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR8_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR8_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4270. CONTROLSS\_PWMXBAR8\_G7 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                 |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR8_G7_SEL | R/W  | 0h    | PWM XBAR8 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |

### 3.20.2.85 CONTROLSS\_PWMXBAR8\_G8 Register

#### 1 CONTROLSS\_PWMXBAR8\_G8 Register (Offset = 320h) [reset = 0h]

PWM XBAR 8 Input Select.

Return to [Summary Table](#)

**Table 3-4271. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1320h       |

**Figure 3-1399. CONTROLSS\_PWMXBAR8\_G8 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    | PWMXBAR8_G8_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| PWMXBAR8_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR8_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR8_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4273. CONTROLSS\_PWMXBAR8\_G8 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                       |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                          |
| 28:0  | PWMXBAR8_G8_SEL | R/W  | 0h    | PWM XBAR8 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.86 CONTROLSS\_PWMXBAR9\_G0 Register

#### 1 CONTROLSS\_PWMXBAR9\_G0 Register (Offset = 340h) [reset = 0h]

PWM XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-4274. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1340h       |

**Figure 3-1400. CONTROLSS\_PWMXBAR9\_G0 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR9_G0_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR9_G0_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR9_G0_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4276. CONTROLSS\_PWMXBAR9\_G0 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | PWMXBAR9_G0_SEL | R/W  | 0h    | PWM XBAR9 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |



### 3.20.2.87 CONTROLSS\_PWMXBAR9\_G1 Register

#### 1 CONTROLSS\_PWMXBAR9\_G1 Register (Offset = 344h) [reset = 0h]

PWM XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-4277. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1344h       |

**Figure 3-1401. CONTROLSS\_PWMXBAR9\_G1 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR9_G1_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR9_G1_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR9_G1_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4279. CONTROLSS\_PWMXBAR9\_G1 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 19:0  | PWMXBAR9_G1_SEL | R/W  | 0h    | PWM XBAR9 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.88 CONTROLSS\_PWMXBAR9\_G2 Register

#### 1 CONTROLSS\_PWMXBAR9\_G2 Register (Offset = 348h) [reset = 0h]

PWM XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-4280. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1348h       |

**Figure 3-1402. CONTROLSS\_PWMXBAR9\_G2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR9_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR9_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR9_G2_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4282. CONTROLSS\_PWMXBAR9\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-4282. CONTROLSS\_PWMXBAR9\_G2 Register Field Descriptions (continued)**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR9_G2_SEL | R/W  | 0h    | PWM XBAR9 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.89 CONTROLSS\_PWMXBAR9\_G3 Register

#### 1 CONTROLSS\_PWMXBAR9\_G3 Register (Offset = 34Ch) [reset = 0h]

PWM XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-4283. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 134Ch       |

**Figure 3-1403. CONTROLSS\_PWMXBAR9\_G3 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    | PWMXBAR9_G3_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR9_G3_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR9_G3_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4285. CONTROLSS\_PWMXBAR9\_G3 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                      |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                         |
| 19:0  | PWMXBAR9_G3_SEL | R/W  | 0h    | PWM XBAR9 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.20.2.90 CONTROLSS\_PWMXBAR9\_G4 Register

#### 1 CONTROLSS\_PWMXBAR9\_G4 Register (Offset = 350h) [reset = 0h]

PWM XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-4286. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1350h       |

**Figure 3-1404. CONTROLSS\_PWMXBAR9\_G4 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR9_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR9_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR9_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR9_G4_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4288. CONTROLSS\_PWMXBAR9\_G4 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                    |
|------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR9_G4_SEL | R/W  | 0h    | PWM XBAR9 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.91 CONTROLSS\_PWMXBAR9\_G5 Register

#### 1 CONTROLSS\_PWMXBAR9\_G5 Register (Offset = 354h) [reset = 0h]

PWM XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-4289. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1354h       |

**Figure 3-1405. CONTROLSS\_PWMXBAR9\_G5 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR9_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR9_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR9_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR9_G5_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4291. CONTROLSS\_PWMXBAR9\_G5 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                         |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR9_G5_SEL | R/W  | 0h    | PWM XBAR9 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |

### 3.20.2.92 CONTROLSS\_PWMXBAR9\_G6 Register

#### 1 CONTROLSS\_PWMXBAR9\_G6 Register (Offset = 358h) [reset = 0h]

PWM XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-4292. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1358h       |

**Figure 3-1406. CONTROLSS\_PWMXBAR9\_G6 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR9_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR9_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR9_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR9_G6_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4294. CONTROLSS\_PWMXBAR9\_G6 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR9_G6_SEL | R/W  | 0h    | PWM XBAR9 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.93 CONTROLSS\_PWMXBAR9\_G7 Register

#### 1 CONTROLSS\_PWMXBAR9\_G7 Register (Offset = 35Ch) [reset = 0h]

PWM XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-4295. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 135Ch       |

**Figure 3-1407. CONTROLSS\_PWMXBAR9\_G7 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR9_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR9_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR9_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR9_G7_SEL |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 3-4297. CONTROLSS\_PWMXBAR9\_G7 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                 |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR9_G7_SEL | R/W  | 0h    | PWM XBAR9 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |



### 3.20.2.94 CONTROLSS\_PWMXBAR9\_G8 Register

#### 1 CONTROLSS\_PWMXBAR9\_G8 Register (Offset = 360h) [reset = 0h]

PWM XBAR 9 Input Select.

Return to [Summary Table](#)

**Table 3-4298. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1360h       |

**Figure 3-1408. CONTROLSS\_PWMXBAR9\_G8 Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    | PWMXBAR9_G8_SEL |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 0h              |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| PWMXBAR9_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| PWMXBAR9_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| PWMXBAR9_G8_SEL |    |    |    |                 |    |    |    |
| R/W             |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |

**Table 3-4300. CONTROLSS\_PWMXBAR9\_G8 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                       |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                          |
| 28:0  | PWMXBAR9_G8_SEL | R/W  | 0h    | PWM XBAR9 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.95 CONTROLSS\_PWMXBAR10\_G0 Register

#### 1 CONTROLSS\_PWMXBAR10\_G0 Register (Offset = 380h) [reset = 0h]

PWM XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-4301. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1380h       |

**Figure 3-1409. CONTROLSS\_PWMXBAR10\_G0 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR10_G0_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR10_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR10_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4303. CONTROLSS\_PWMXBAR10\_G0 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR10_G0_SEL | R/W  | 0h    | PWM XBAR10 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |

### 3.20.2.96 CONTROLSS\_PWMXBAR10\_G1 Register

#### 1 CONTROLSS\_PWMXBAR10\_G1 Register (Offset = 384h) [reset = 0h]

PWM XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-4304. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1384h       |

**Figure 3-1410. CONTROLSS\_PWMXBAR10\_G1 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR10_G1_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR10_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR10_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4306. CONTROLSS\_PWMXBAR10\_G1 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR10_G1_SEL | R/W  | 0h    | PWM XBAR10 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.97 CONTROLSS\_PWMXBAR10\_G2 Register

#### 1 CONTROLSS\_PWMXBAR10\_G2 Register (Offset = 388h) [reset = 0h]

PWM XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-4307. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1388h       |

**Figure 3-1411. CONTROLSS\_PWMXBAR10\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR10_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR10_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR10_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4309. CONTROLSS\_PWMXBAR10\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-4309. CONTROLSS\_PWMXBAR10\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR10_G2_SEL | R/W  | 0h    | PWM XBAR10 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.98 CONTROLSS\_PWMXBAR10\_G3 Register

#### 1 CONTROLSS\_PWMXBAR10\_G3 Register (Offset = 38Ch) [reset = 0h]

PWM XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-4310. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 138Ch       |

**Figure 3-1412. CONTROLSS\_PWMXBAR10\_G3 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR10_G3_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR10_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR10_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4312. CONTROLSS\_PWMXBAR10\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                       |
|-------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                          |
| 19:0  | PWMXBAR10_G3_SEL | R/W  | 0h    | PWM XBAR10 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.20.2.99 CONTROLSS\_PWMXBAR10\_G4 Register

#### 1 CONTROLSS\_PWMXBAR10\_G4 Register (Offset = 390h) [reset = 0h]

PWM XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-4313. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1390h       |

**Figure 3-1413. CONTROLSS\_PWMXBAR10\_G4 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR10_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR10_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR10_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR10_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4315. CONTROLSS\_PWMXBAR10\_G4 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR10_G4_SEL | R/W  | 0h    | PWM XBAR10 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.100 CONTROLSS\_PWMXBAR10\_G5 Register

#### 1 CONTROLSS\_PWMXBAR10\_G5 Register (Offset = 394h) [reset = 0h]

PWM XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-4316. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1394h       |

**Figure 3-1414. CONTROLSS\_PWMXBAR10\_G5 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR10_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR10_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR10_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR10_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4318. CONTROLSS\_PWMXBAR10\_G5 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR10_G5_SEL | R/W  | 0h    | PWM XBAR10 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |



### 3.20.2.101 CONTROLSS\_PWMXBAR10\_G6 Register

#### 1 CONTROLSS\_PWMXBAR10\_G6 Register (Offset = 398h) [reset = 0h]

PWM XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-4319. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1398h       |

**Figure 3-1415. CONTROLSS\_PWMXBAR10\_G6 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR10_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR10_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR10_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR10_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4321. CONTROLSS\_PWMXBAR10\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR10_G6_SEL | R/W  | 0h    | PWM XBAR10 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.102 CONTROLSS\_PWMXBAR10\_G7 Register

#### 1 CONTROLSS\_PWMXBAR10\_G7 Register (Offset = 39Ch) [reset = 0h]

PWM XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-4322. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 139Ch       |

**Figure 3-1416. CONTROLSS\_PWMXBAR10\_G7 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR10_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR10_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR10_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR10_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4324. CONTROLSS\_PWMXBAR10\_G7 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                  |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR10_G7_SEL | R/W  | 0h    | PWM XBAR10 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |

### 3.20.2.103 CONTROLSS\_PWMXBAR10\_G8 Register

#### 1 CONTROLSS\_PWMXBAR10\_G8 Register (Offset = 3A0h) [reset = 0h]

PWM XBAR 10 Input Select.

Return to [Summary Table](#)

**Table 3-4325. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 13A0h       |

**Figure 3-1417. CONTROLSS\_PWMXBAR10\_G8 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    | PWMXBAR10_G8_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| PWMXBAR10_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR10_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR10_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4327. CONTROLSS\_PWMXBAR10\_G8 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                        |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                           |
| 28:0  | PWMXBAR10_G8_SEL | R/W  | 0h    | PWM XBAR10 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.104 CONTROLSS\_PWMXBAR11\_G0 Register

#### 1 CONTROLSS\_PWMXBAR11\_G0 Register (Offset = 3C0h) [reset = 0h]

PWM XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-4328. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 13C0h       |

**Figure 3-1418. CONTROLSS\_PWMXBAR11\_G0 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR11_G0_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR11_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR11_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4330. CONTROLSS\_PWMXBAR11\_G0 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR11_G0_SEL | R/W  | 0h    | PWM XBAR11 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |

### 3.20.2.105 CONTROLSS\_PWMXBAR11\_G1 Register

#### 1 CONTROLSS\_PWMXBAR11\_G1 Register (Offset = 3C4h) [reset = 0h]

PWM XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-4331. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 13C4h       |

**Figure 3-1419. CONTROLSS\_PWMXBAR11\_G1 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR11_G1_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR11_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR11_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4333. CONTROLSS\_PWMXBAR11\_G1 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR11_G1_SEL | R/W  | 0h    | PWM XBAR11 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.106 CONTROLSS\_PWMXBAR11\_G2 Register

#### 1 CONTROLSS\_PWMXBAR11\_G2 Register (Offset = 3C8h) [reset = 0h]

PWM XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-4334. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 13C8h       |

**Figure 3-1420. CONTROLSS\_PWMXBAR11\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR11_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR11_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR11_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4336. CONTROLSS\_PWMXBAR11\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-4336. CONTROLSS\_PWMXBAR11\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR11_G2_SEL | R/W  | 0h    | PWM XBAR11 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.107 CONTROLSS\_PWMXBAR11\_G3 Register

#### 1 CONTROLSS\_PWMXBAR11\_G3 Register (Offset = 3CCh) [reset = 0h]

PWM XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-4337. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 13CCh       |

**Figure 3-1421. CONTROLSS\_PWMXBAR11\_G3 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR11_G3_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR11_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR11_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4339. CONTROLSS\_PWMXBAR11\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                       |
|-------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                          |
| 19:0  | PWMXBAR11_G3_SEL | R/W  | 0h    | PWM XBAR11 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |



### 3.20.2.108 CONTROLSS\_PWMXBAR11\_G4 Register

#### 1 CONTROLSS\_PWMXBAR11\_G4 Register (Offset = 3D0h) [reset = 0h]

PWM XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-4340. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 13D0h       |

**Figure 3-1422. CONTROLSS\_PWMXBAR11\_G4 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR11_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR11_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR11_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR11_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4342. CONTROLSS\_PWMXBAR11\_G4 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR11_G4_SEL | R/W  | 0h    | PWM XBAR11 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.109 CONTROLSS\_PWMXBAR11\_G5 Register

#### 1 CONTROLSS\_PWMXBAR11\_G5 Register (Offset = 3D4h) [reset = 0h]

PWM XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-4343. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 13D4h       |

**Figure 3-1423. CONTROLSS\_PWMXBAR11\_G5 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR11_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR11_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR11_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR11_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4345. CONTROLSS\_PWMXBAR11\_G5 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR11_G5_SEL | R/W  | 0h    | PWM XBAR11 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |

### 3.20.2.110 CONTROLSS\_PWMXBAR11\_G6 Register

#### 1 CONTROLSS\_PWMXBAR11\_G6 Register (Offset = 3D8h) [reset = 0h]

PWM XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-4346. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 13D8h       |

**Figure 3-1424. CONTROLSS\_PWMXBAR11\_G6 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR11_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR11_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR11_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR11_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4348. CONTROLSS\_PWMXBAR11\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR11_G6_SEL | R/W  | 0h    | PWM XBAR11 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.111 CONTROLSS\_PWMXBAR11\_G7 Register

#### 1 CONTROLSS\_PWMXBAR11\_G7 Register (Offset = 3DCh) [reset = 0h]

PWM XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-4349. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 13DCh       |

**Figure 3-1425. CONTROLSS\_PWMXBAR11\_G7 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR11_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR11_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR11_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR11_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4351. CONTROLSS\_PWMXBAR11\_G7 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                  |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR11_G7_SEL | R/W  | 0h    | PWM XBAR11 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |

### 3.20.2.112 CONTROLSS\_PWMXBAR11\_G8 Register

#### 1 CONTROLSS\_PWMXBAR11\_G8 Register (Offset = 3E0h) [reset = 0h]

PWM XBAR 11 Input Select.

Return to [Summary Table](#)

**Table 3-4352. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 13E0h       |

**Figure 3-1426. CONTROLSS\_PWMXBAR11\_G8 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    | PWMXBAR11_G8_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| PWMXBAR11_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR11_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR11_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4354. CONTROLSS\_PWMXBAR11\_G8 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                        |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                           |
| 28:0  | PWMXBAR11_G8_SEL | R/W  | 0h    | PWM XBAR11 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.113 CONTROLSS\_PWMXBAR12\_G0 Register

#### 1 CONTROLSS\_PWMXBAR12\_G0 Register (Offset = 400h) [reset = 0h]

PWM XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-4355. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1400h       |

**Figure 3-1427. CONTROLSS\_PWMXBAR12\_G0 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR12_G0_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR12_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR12_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4357. CONTROLSS\_PWMXBAR12\_G0 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR12_G0_SEL | R/W  | 0h    | PWM XBAR12 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |

### 3.20.2.114 CONTROLSS\_PWMXBAR12\_G1 Register

#### 1 CONTROLSS\_PWMXBAR12\_G1 Register (Offset = 404h) [reset = 0h]

PWM XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-4358. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1404h       |

**Figure 3-1428. CONTROLSS\_PWMXBAR12\_G1 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR12_G1_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR12_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR12_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4360. CONTROLSS\_PWMXBAR12\_G1 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR12_G1_SEL | R/W  | 0h    | PWM XBAR12 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.115 CONTROLSS\_PWMXBAR12\_G2 Register

#### 1 CONTROLSS\_PWMXBAR12\_G2 Register (Offset = 408h) [reset = 0h]

PWM XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-4361. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1408h       |

**Figure 3-1429. CONTROLSS\_PWMXBAR12\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR12_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR12_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR12_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4363. CONTROLSS\_PWMXBAR12\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |



**Table 3-4363. CONTROLSS\_PWMXBAR12\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR12_G2_SEL | R/W  | 0h    | PWM XBAR12 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.116 CONTROLSS\_PWMXBAR12\_G3 Register

#### 1 CONTROLSS\_PWMXBAR12\_G3 Register (Offset = 40Ch) [reset = 0h]

PWM XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-4364. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 140Ch       |

**Figure 3-1430. CONTROLSS\_PWMXBAR12\_G3 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR12_G3_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR12_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR12_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4366. CONTROLSS\_PWMXBAR12\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                       |
|-------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                          |
| 19:0  | PWMXBAR12_G3_SEL | R/W  | 0h    | PWM XBAR12 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.20.2.117 CONTROLSS\_PWMXBAR12\_G4 Register

#### 1 CONTROLSS\_PWMXBAR12\_G4 Register (Offset = 410h) [reset = 0h]

PWM XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-4367. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1410h       |

**Figure 3-1431. CONTROLSS\_PWMXBAR12\_G4 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR12_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR12_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR12_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR12_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4369. CONTROLSS\_PWMXBAR12\_G4 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR12_G4_SEL | R/W  | 0h    | PWM XBAR12 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.118 CONTROLSS\_PWMXBAR12\_G5 Register

#### 1 CONTROLSS\_PWMXBAR12\_G5 Register (Offset = 414h) [reset = 0h]

PWM XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-4370. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1414h       |

**Figure 3-1432. CONTROLSS\_PWMXBAR12\_G5 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR12_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR12_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR12_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR12_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4372. CONTROLSS\_PWMXBAR12\_G5 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR12_G5_SEL | R/W  | 0h    | PWM XBAR12 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |

### 3.20.2.119 CONTROLSS\_PWMXBAR12\_G6 Register

#### 1 CONTROLSS\_PWMXBAR12\_G6 Register (Offset = 418h) [reset = 0h]

PWM XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-4373. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1418h       |

**Figure 3-1433. CONTROLSS\_PWMXBAR12\_G6 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR12_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR12_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR12_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR12_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4375. CONTROLSS\_PWMXBAR12\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR12_G6_SEL | R/W  | 0h    | PWM XBAR12 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.120 CONTROLSS\_PWMXBAR12\_G7 Register

#### 1 CONTROLSS\_PWMXBAR12\_G7 Register (Offset = 41Ch) [reset = 0h]

PWM XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-4376. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 141Ch       |

**Figure 3-1434. CONTROLSS\_PWMXBAR12\_G7 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR12_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR12_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR12_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR12_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4378. CONTROLSS\_PWMXBAR12\_G7 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                  |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR12_G7_SEL | R/W  | 0h    | PWM XBAR12 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |

### 3.20.2.121 CONTROLSS\_PWMXBAR12\_G8 Register

#### 1 CONTROLSS\_PWMXBAR12\_G8 Register (Offset = 420h) [reset = 0h]

PWM XBAR 12 Input Select.

Return to [Summary Table](#)

**Table 3-4379. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1420h       |

**Figure 3-1435. CONTROLSS\_PWMXBAR12\_G8 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    | PWMXBAR12_G8_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| PWMXBAR12_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR12_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR12_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4381. CONTROLSS\_PWMXBAR12\_G8 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                        |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                           |
| 28:0  | PWMXBAR12_G8_SEL | R/W  | 0h    | PWM XBAR12 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.122 CONTROLSS\_PWMXBAR13\_G0 Register

#### 1 CONTROLSS\_PWMXBAR13\_G0 Register (Offset = 440h) [reset = 0h]

PWM XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-4382. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1440h       |

**Figure 3-1436. CONTROLSS\_PWMXBAR13\_G0 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR13_G0_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR13_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR13_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4384. CONTROLSS\_PWMXBAR13\_G0 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR13_G0_SEL | R/W  | 0h    | PWM XBAR13 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |



### 3.20.2.123 CONTROLSS\_PWMXBAR13\_G1 Register

#### 1 CONTROLSS\_PWMXBAR13\_G1 Register (Offset = 444h) [reset = 0h]

PWM XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-4385. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1444h       |

**Figure 3-1437. CONTROLSS\_PWMXBAR13\_G1 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR13_G1_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR13_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR13_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4387. CONTROLSS\_PWMXBAR13\_G1 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR13_G1_SEL | R/W  | 0h    | PWM XBAR13 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.124 CONTROLSS\_PWMXBAR13\_G2 Register

#### 1 CONTROLSS\_PWMXBAR13\_G2 Register (Offset = 448h) [reset = 0h]

PWM XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-4388. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1448h       |

**Figure 3-1438. CONTROLSS\_PWMXBAR13\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR13_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR13_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR13_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4390. CONTROLSS\_PWMXBAR13\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-4390. CONTROLSS\_PWMXBAR13\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR13_G2_SEL | R/W  | 0h    | PWM XBAR13 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.125 CONTROLSS\_PWMXBAR13\_G3 Register

#### 1 CONTROLSS\_PWMXBAR13\_G3 Register (Offset = 44Ch) [reset = 0h]

PWM XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-4391. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 144Ch       |

**Figure 3-1439. CONTROLSS\_PWMXBAR13\_G3 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR13_G3_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR13_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR13_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4393. CONTROLSS\_PWMXBAR13\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                       |
|-------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                          |
| 19:0  | PWMXBAR13_G3_SEL | R/W  | 0h    | PWM XBAR13 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.20.2.126 CONTROLSS\_PWMXBAR13\_G4 Register

#### 1 CONTROLSS\_PWMXBAR13\_G4 Register (Offset = 450h) [reset = 0h]

PWM XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-4394. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1450h       |

**Figure 3-1440. CONTROLSS\_PWMXBAR13\_G4 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR13_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR13_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR13_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR13_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4396. CONTROLSS\_PWMXBAR13\_G4 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR13_G4_SEL | R/W  | 0h    | PWM XBAR13 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.127 CONTROLSS\_PWMXBAR13\_G5 Register

#### 1 CONTROLSS\_PWMXBAR13\_G5 Register (Offset = 454h) [reset = 0h]

PWM XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-4397. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1454h       |

**Figure 3-1441. CONTROLSS\_PWMXBAR13\_G5 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR13_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR13_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR13_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR13_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4399. CONTROLSS\_PWMXBAR13\_G5 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR13_G5_SEL | R/W  | 0h    | PWM XBAR13 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |

### 3.20.2.128 CONTROLSS\_PWMXBAR13\_G6 Register

#### 1 CONTROLSS\_PWMXBAR13\_G6 Register (Offset = 458h) [reset = 0h]

PWM XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-4400. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1458h       |

**Figure 3-1442. CONTROLSS\_PWMXBAR13\_G6 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR13_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR13_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR13_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR13_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4402. CONTROLSS\_PWMXBAR13\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR13_G6_SEL | R/W  | 0h    | PWM XBAR13 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.129 CONTROLSS\_PWMXBAR13\_G7 Register

#### 1 CONTROLSS\_PWMXBAR13\_G7 Register (Offset = 45Ch) [reset = 0h]

PWM XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-4403. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 145Ch       |

**Figure 3-1443. CONTROLSS\_PWMXBAR13\_G7 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR13_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR13_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR13_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR13_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4405. CONTROLSS\_PWMXBAR13\_G7 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                  |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR13_G7_SEL | R/W  | 0h    | PWM XBAR13 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |



### 3.20.2.130 CONTROLSS\_PWMXBAR13\_G8 Register

#### 1 CONTROLSS\_PWMXBAR13\_G8 Register (Offset = 460h) [reset = 0h]

PWM XBAR 13 Input Select.

Return to [Summary Table](#)

**Table 3-4406. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1460h       |

**Figure 3-1444. CONTROLSS\_PWMXBAR13\_G8 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    | PWMXBAR13_G8_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| PWMXBAR13_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR13_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR13_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4408. CONTROLSS\_PWMXBAR13\_G8 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                        |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                           |
| 28:0  | PWMXBAR13_G8_SEL | R/W  | 0h    | PWM XBAR13 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.131 CONTROLSS\_PWMXBAR14\_G0 Register

#### 1 CONTROLSS\_PWMXBAR14\_G0 Register (Offset = 480h) [reset = 0h]

PWM XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-4409. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1480h       |

**Figure 3-1445. CONTROLSS\_PWMXBAR14\_G0 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR14_G0_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR14_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR14_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4411. CONTROLSS\_PWMXBAR14\_G0 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR14_G0_SEL | R/W  | 0h    | PWM XBAR14 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |

### 3.20.2.132 CONTROLSS\_PWMXBAR14\_G1 Register

#### 1 CONTROLSS\_PWMXBAR14\_G1 Register (Offset = 484h) [reset = 0h]

PWM XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-4412. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1484h       |

**Figure 3-1446. CONTROLSS\_PWMXBAR14\_G1 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR14_G1_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR14_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR14_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4414. CONTROLSS\_PWMXBAR14\_G1 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR14_G1_SEL | R/W  | 0h    | PWM XBAR14 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.133 CONTROLSS\_PWMXBAR14\_G2 Register

#### 1 CONTROLSS\_PWMXBAR14\_G2 Register (Offset = 488h) [reset = 0h]

PWM XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-4415. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1488h       |

**Figure 3-1447. CONTROLSS\_PWMXBAR14\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR14_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR14_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR14_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4417. CONTROLSS\_PWMXBAR14\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-4417. CONTROLSS\_PWMXBAR14\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR14_G2_SEL | R/W  | 0h    | PWM XBAR14 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.134 CONTROLSS\_PWMXBAR14\_G3 Register

#### 1 CONTROLSS\_PWMXBAR14\_G3 Register (Offset = 48Ch) [reset = 0h]

PWM XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-4418. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 148Ch       |

**Figure 3-1448. CONTROLSS\_PWMXBAR14\_G3 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR14_G3_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR14_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR14_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4420. CONTROLSS\_PWMXBAR14\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                       |
|-------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                          |
| 19:0  | PWMXBAR14_G3_SEL | R/W  | 0h    | PWM XBAR14 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.20.2.135 CONTROLSS\_PWMXBAR14\_G4 Register

#### 1 CONTROLSS\_PWMXBAR14\_G4 Register (Offset = 490h) [reset = 0h]

PWM XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-4421. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1490h       |

**Figure 3-1449. CONTROLSS\_PWMXBAR14\_G4 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR14_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR14_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR14_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR14_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4423. CONTROLSS\_PWMXBAR14\_G4 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR14_G4_SEL | R/W  | 0h    | PWM XBAR14 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.136 CONTROLSS\_PWMXBAR14\_G5 Register

#### 1 CONTROLSS\_PWMXBAR14\_G5 Register (Offset = 494h) [reset = 0h]

PWM XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-4424. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1494h       |

**Figure 3-1450. CONTROLSS\_PWMXBAR14\_G5 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR14_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR14_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR14_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR14_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4426. CONTROLSS\_PWMXBAR14\_G5 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR14_G5_SEL | R/W  | 0h    | PWM XBAR14 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |



### 3.20.2.137 CONTROLSS\_PWMXBAR14\_G6 Register

#### 1 CONTROLSS\_PWMXBAR14\_G6 Register (Offset = 498h) [reset = 0h]

PWM XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-4427. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1498h       |

**Figure 3-1451. CONTROLSS\_PWMXBAR14\_G6 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR14_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR14_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR14_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR14_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4429. CONTROLSS\_PWMXBAR14\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR14_G6_SEL | R/W  | 0h    | PWM XBAR14 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.138 CONTROLSS\_PWMXBAR14\_G7 Register

#### 1 CONTROLSS\_PWMXBAR14\_G7 Register (Offset = 49Ch) [reset = 0h]

PWM XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-4430. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 149Ch       |

**Figure 3-1452. CONTROLSS\_PWMXBAR14\_G7 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR14_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR14_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR14_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR14_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4432. CONTROLSS\_PWMXBAR14\_G7 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                  |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR14_G7_SEL | R/W  | 0h    | PWM XBAR14 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |

### 3.20.2.139 CONTROLSS\_PWMXBAR14\_G8 Register

#### 1 CONTROLSS\_PWMXBAR14\_G8 Register (Offset = 4A0h) [reset = 0h]

PWM XBAR 14 Input Select.

Return to [Summary Table](#)

**Table 3-4433. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 14A0h       |

**Figure 3-1453. CONTROLSS\_PWMXBAR14\_G8 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    | PWMXBAR14_G8_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| PWMXBAR14_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR14_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR14_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4435. CONTROLSS\_PWMXBAR14\_G8 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                        |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                           |
| 28:0  | PWMXBAR14_G8_SEL | R/W  | 0h    | PWM XBAR14 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.140 CONTROLSS\_PWMXBAR15\_G0 Register

#### 1 CONTROLSS\_PWMXBAR15\_G0 Register (Offset = 4C0h) [reset = 0h]

PWM XBAR 15 Input Select.

Return to [Summary Table](#)

**Table 3-4436. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 14C0h       |

**Figure 3-1454. CONTROLSS\_PWMXBAR15\_G0 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR15_G0_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR15_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR15_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4438. CONTROLSS\_PWMXBAR15\_G0 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR15_G0_SEL | R/W  | 0h    | PWM XBAR15 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |

### 3.20.2.141 CONTROLSS\_PWMXBAR15\_G1 Register

#### 1 CONTROLSS\_PWMXBAR15\_G1 Register (Offset = 4C4h) [reset = 0h]

PWM XBAR 15 Input Select.

Return to [Summary Table](#)

**Table 3-4439. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 14C4h       |

**Figure 3-1455. CONTROLSS\_PWMXBAR15\_G1 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR15_G1_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR15_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR15_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4441. CONTROLSS\_PWMXBAR15\_G1 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR15_G1_SEL | R/W  | 0h    | PWM XBAR15 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.142 CONTROLSS\_PWMXBAR15\_G2 Register

#### 1 CONTROLSS\_PWMXBAR15\_G2 Register (Offset = 4C8h) [reset = 0h]

PWM XBAR 15 Input Select.

Return to [Summary Table](#)

**Table 3-4442. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 14C8h       |

**Figure 3-1456. CONTROLSS\_PWMXBAR15\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR15_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR15_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR15_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4444. CONTROLSS\_PWMXBAR15\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-4444. CONTROLSS\_PWMXBAR15\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR15_G2_SEL | R/W  | 0h    | PWM XBAR15 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.143 CONTROLSS\_PWMXBAR15\_G3 Register

#### 1 CONTROLSS\_PWMXBAR15\_G3 Register (Offset = 4CCh) [reset = 0h]

PWM XBAR 15 Input Select.

Return to [Summary Table](#)

**Table 3-4445. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 14CCh       |

**Figure 3-1457. CONTROLSS\_PWMXBAR15\_G3 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR15_G3_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR15_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR15_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4447. CONTROLSS\_PWMXBAR15\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                       |
|-------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                          |
| 19:0  | PWMXBAR15_G3_SEL | R/W  | 0h    | PWM XBAR15 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |



### 3.20.2.144 CONTROLSS\_PWMXBAR15\_G4 Register

#### 1 CONTROLSS\_PWMXBAR15\_G4 Register (Offset = 4D0h) [reset = 0h]

PWM XBAR 15 Input Select.

Return to [Summary Table](#)

**Table 3-4448. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 14D0h       |

**Figure 3-1458. CONTROLSS\_PWMXBAR15\_G4 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR15_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR15_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR15_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR15_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4450. CONTROLSS\_PWMXBAR15\_G4 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR15_G4_SEL | R/W  | 0h    | PWM XBAR15 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.145 CONTROLSS\_PWMXBAR15\_G5 Register

#### 1 CONTROLSS\_PWMXBAR15\_G5 Register (Offset = 4D4h) [reset = 0h]

PWM XBAR 15 Input Select.

Return to [Summary Table](#)

**Table 3-4451. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 14D4h       |

**Figure 3-1459. CONTROLSS\_PWMXBAR15\_G5 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR15_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR15_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR15_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR15_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4453. CONTROLSS\_PWMXBAR15\_G5 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR15_G5_SEL | R/W  | 0h    | PWM XBAR15 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |

### 3.20.2.146 CONTROLSS\_PWMXBAR15\_G6 Register

#### 1 CONTROLSS\_PWMXBAR15\_G6 Register (Offset = 4D8h) [reset = 0h]

PWM XBAR 15 Input Select.

Return to [Summary Table](#)

**Table 3-4454. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 14D8h       |

**Figure 3-1460. CONTROLSS\_PWMXBAR15\_G6 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR15_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR15_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR15_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR15_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4456. CONTROLSS\_PWMXBAR15\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR15_G6_SEL | R/W  | 0h    | PWM XBAR15 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.147 CONTROLSS\_PWMXBAR15\_G7 Register

#### 1 CONTROLSS\_PWMXBAR15\_G7 Register (Offset = 4DCh) [reset = 0h]

PWM XBAR 15 Input Select.

Return to [Summary Table](#)

**Table 3-4457. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 14DCh       |

**Figure 3-1461. CONTROLSS\_PWMXBAR15\_G7 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR15_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR15_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR15_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR15_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4459. CONTROLSS\_PWMXBAR15\_G7 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                  |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR15_G7_SEL | R/W  | 0h    | PWM XBAR15 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |

### 3.20.2.148 CONTROLSS\_PWMXBAR15\_G8 Register

#### 1 CONTROLSS\_PWMXBAR15\_G8 Register (Offset = 4E0h) [reset = 0h]

PWM XBAR 15 Input Select.

Return to [Summary Table](#)

**Table 3-4460. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 14E0h       |

**Figure 3-1462. CONTROLSS\_PWMXBAR15\_G8 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    | PWMXBAR15_G8_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| PWMXBAR15_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR15_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR15_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4462. CONTROLSS\_PWMXBAR15\_G8 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                        |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                           |
| 28:0  | PWMXBAR15_G8_SEL | R/W  | 0h    | PWM XBAR15 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.149 CONTROLSS\_PWMXBAR16\_G0 Register

#### 1 CONTROLSS\_PWMXBAR16\_G0 Register (Offset = 500h) [reset = 0h]

PWM XBAR 16 Input Select.

Return to [Summary Table](#)

**Table 3-4463. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1500h       |

**Figure 3-1463. CONTROLSS\_PWMXBAR16\_G0 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR16_G0_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR16_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR16_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4465. CONTROLSS\_PWMXBAR16\_G0 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR16_G0_SEL | R/W  | 0h    | PWM XBAR16 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |

### 3.20.2.150 CONTROLSS\_PWMXBAR16\_G1 Register

#### 1 CONTROLSS\_PWMXBAR16\_G1 Register (Offset = 504h) [reset = 0h]

PWM XBAR 16 Input Select.

Return to [Summary Table](#)

**Table 3-4466. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1504h       |

**Figure 3-1464. CONTROLSS\_PWMXBAR16\_G1 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR16_G1_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR16_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR16_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4468. CONTROLSS\_PWMXBAR16\_G1 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR16_G1_SEL | R/W  | 0h    | PWM XBAR16 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.151 CONTROLSS\_PWMXBAR16\_G2 Register

#### 1 CONTROLSS\_PWMXBAR16\_G2 Register (Offset = 508h) [reset = 0h]

PWM XBAR 16 Input Select.

Return to [Summary Table](#)

**Table 3-4469. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1508h       |

**Figure 3-1465. CONTROLSS\_PWMXBAR16\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR16_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR16_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR16_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4471. CONTROLSS\_PWMXBAR16\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |



**Table 3-4471. CONTROLSS\_PWMXBAR16\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR16_G2_SEL | R/W  | 0h    | PWM XBAR16 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.152 CONTROLSS\_PWMXBAR16\_G3 Register

#### 1 CONTROLSS\_PWMXBAR16\_G3 Register (Offset = 50Ch) [reset = 0h]

PWM XBAR 16 Input Select.

Return to [Summary Table](#)

**Table 3-4472. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 150Ch       |

**Figure 3-1466. CONTROLSS\_PWMXBAR16\_G3 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR16_G3_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR16_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR16_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4474. CONTROLSS\_PWMXBAR16\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                       |
|-------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                          |
| 19:0  | PWMXBAR16_G3_SEL | R/W  | 0h    | PWM XBAR16 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.20.2.153 CONTROLSS\_PWMXBAR16\_G4 Register

#### 1 CONTROLSS\_PWMXBAR16\_G4 Register (Offset = 510h) [reset = 0h]

PWM XBAR 16 Input Select.

Return to [Summary Table](#)

**Table 3-4475. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1510h       |

**Figure 3-1467. CONTROLSS\_PWMXBAR16\_G4 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR16_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR16_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR16_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR16_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4477. CONTROLSS\_PWMXBAR16\_G4 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR16_G4_SEL | R/W  | 0h    | PWM XBAR16 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.154 CONTROLSS\_PWMXBAR16\_G5 Register

#### 1 CONTROLSS\_PWMXBAR16\_G5 Register (Offset = 514h) [reset = 0h]

PWM XBAR 16 Input Select.

Return to [Summary Table](#)

**Table 3-4478. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1514h       |

**Figure 3-1468. CONTROLSS\_PWMXBAR16\_G5 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR16_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR16_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR16_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR16_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4480. CONTROLSS\_PWMXBAR16\_G5 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR16_G5_SEL | R/W  | 0h    | PWM XBAR16 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |

### 3.20.2.155 CONTROLSS\_PWMXBAR16\_G6 Register

#### 1 CONTROLSS\_PWMXBAR16\_G6 Register (Offset = 518h) [reset = 0h]

PWM XBAR 16 Input Select.

Return to [Summary Table](#)

**Table 3-4481. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1518h       |

**Figure 3-1469. CONTROLSS\_PWMXBAR16\_G6 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR16_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR16_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR16_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR16_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4483. CONTROLSS\_PWMXBAR16\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR16_G6_SEL | R/W  | 0h    | PWM XBAR16 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.156 CONTROLSS\_PWMXBAR16\_G7 Register

#### 1 CONTROLSS\_PWMXBAR16\_G7 Register (Offset = 51Ch) [reset = 0h]

PWM XBAR 16 Input Select.

Return to [Summary Table](#)

**Table 3-4484. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 151Ch       |

**Figure 3-1470. CONTROLSS\_PWMXBAR16\_G7 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR16_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR16_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR16_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR16_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4486. CONTROLSS\_PWMXBAR16\_G7 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                  |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR16_G7_SEL | R/W  | 0h    | PWM XBAR16 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |

### 3.20.2.157 CONTROLSS\_PWMXBAR16\_G8 Register

#### 1 CONTROLSS\_PWMXBAR16\_G8 Register (Offset = 520h) [reset = 0h]

PWM XBAR 16 Input Select.

Return to [Summary Table](#)

**Table 3-4487. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1520h       |

**Figure 3-1471. CONTROLSS\_PWMXBAR16\_G8 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    | PWMXBAR16_G8_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| PWMXBAR16_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR16_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR16_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4489. CONTROLSS\_PWMXBAR16\_G8 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                        |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                           |
| 28:0  | PWMXBAR16_G8_SEL | R/W  | 0h    | PWM XBAR16 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.158 CONTROLSS\_PWMXBAR17\_G0 Register

#### 1 CONTROLSS\_PWMXBAR17\_G0 Register (Offset = 540h) [reset = 0h]

PWM XBAR 17 Input Select.

Return to [Summary Table](#)

**Table 3-4490. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1540h       |

**Figure 3-1472. CONTROLSS\_PWMXBAR17\_G0 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR17_G0_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR17_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR17_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4492. CONTROLSS\_PWMXBAR17\_G0 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR17_G0_SEL | R/W  | 0h    | PWM XBAR17 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |



### 3.20.2.159 CONTROLSS\_PWMXBAR17\_G1 Register

#### 1 CONTROLSS\_PWMXBAR17\_G1 Register (Offset = 544h) [reset = 0h]

PWM XBAR 17 Input Select.

Return to [Summary Table](#)

**Table 3-4493. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1544h       |

**Figure 3-1473. CONTROLSS\_PWMXBAR17\_G1 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR17_G1_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR17_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR17_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4495. CONTROLSS\_PWMXBAR17\_G1 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR17_G1_SEL | R/W  | 0h    | PWM XBAR17 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.160 CONTROLSS\_PWMXBAR17\_G2 Register

#### 1 CONTROLSS\_PWMXBAR17\_G2 Register (Offset = 548h) [reset = 0h]

PWM XBAR 17 Input Select.

Return to [Summary Table](#)

**Table 3-4496. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1548h       |

**Figure 3-1474. CONTROLSS\_PWMXBAR17\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR17_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR17_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR17_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4498. CONTROLSS\_PWMXBAR17\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-4498. CONTROLSS\_PWMXBAR17\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR17_G2_SEL | R/W  | 0h    | PWM XBAR17 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.161 CONTROLSS\_PWMXBAR17\_G3 Register

#### 1 CONTROLSS\_PWMXBAR17\_G3 Register (Offset = 54Ch) [reset = 0h]

PWM XBAR 17 Input Select.

Return to [Summary Table](#)

**Table 3-4499. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 154Ch       |

**Figure 3-1475. CONTROLSS\_PWMXBAR17\_G3 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR17_G3_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR17_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR17_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4501. CONTROLSS\_PWMXBAR17\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                       |
|-------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                          |
| 19:0  | PWMXBAR17_G3_SEL | R/W  | 0h    | PWM XBAR17 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.20.2.162 CONTROLSS\_PWMXBAR17\_G4 Register

#### 1 CONTROLSS\_PWMXBAR17\_G4 Register (Offset = 550h) [reset = 0h]

PWM XBAR 17 Input Select.

Return to [Summary Table](#)

**Table 3-4502. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1550h       |

**Figure 3-1476. CONTROLSS\_PWMXBAR17\_G4 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR17_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR17_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR17_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR17_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4504. CONTROLSS\_PWMXBAR17\_G4 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR17_G4_SEL | R/W  | 0h    | PWM XBAR17 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.163 CONTROLSS\_PWMXBAR17\_G5 Register

#### 1 CONTROLSS\_PWMXBAR17\_G5 Register (Offset = 554h) [reset = 0h]

PWM XBAR 17 Input Select.

Return to [Summary Table](#)

**Table 3-4505. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1554h       |

**Figure 3-1477. CONTROLSS\_PWMXBAR17\_G5 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR17_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR17_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR17_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR17_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4507. CONTROLSS\_PWMXBAR17\_G5 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR17_G5_SEL | R/W  | 0h    | PWM XBAR17 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |

### 3.20.2.164 CONTROLSS\_PWMXBAR17\_G6 Register

#### 1 CONTROLSS\_PWMXBAR17\_G6 Register (Offset = 558h) [reset = 0h]

PWM XBAR 17 Input Select.

Return to [Summary Table](#)

**Table 3-4508. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1558h       |

**Figure 3-1478. CONTROLSS\_PWMXBAR17\_G6 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR17_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR17_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR17_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR17_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4510. CONTROLSS\_PWMXBAR17\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR17_G6_SEL | R/W  | 0h    | PWM XBAR17 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.165 CONTROLSS\_PWMXBAR17\_G7 Register

#### 1 CONTROLSS\_PWMXBAR17\_G7 Register (Offset = 55Ch) [reset = 0h]

PWM XBAR 17 Input Select.

Return to [Summary Table](#)

**Table 3-4511. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 155Ch       |

**Figure 3-1479. CONTROLSS\_PWMXBAR17\_G7 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR17_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR17_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR17_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR17_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4513. CONTROLSS\_PWMXBAR17\_G7 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                  |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR17_G7_SEL | R/W  | 0h    | PWM XBAR17 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |



### 3.20.2.166 CONTROLSS\_PWMXBAR17\_G8 Register

#### 1 CONTROLSS\_PWMXBAR17\_G8 Register (Offset = 560h) [reset = 0h]

PWM XBAR 17 Input Select.

Return to [Summary Table](#)

**Table 3-4514. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1560h       |

**Figure 3-1480. CONTROLSS\_PWMXBAR17\_G8 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    | PWMXBAR17_G8_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| PWMXBAR17_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR17_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR17_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4516. CONTROLSS\_PWMXBAR17\_G8 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                        |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                           |
| 28:0  | PWMXBAR17_G8_SEL | R/W  | 0h    | PWM XBAR17 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.167 CONTROLSS\_PWMXBAR18\_G0 Register

#### 1 CONTROLSS\_PWMXBAR18\_G0 Register (Offset = 580h) [reset = 0h]

PWM XBAR 18 Input Select.

Return to [Summary Table](#)

**Table 3-4517. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1580h       |

**Figure 3-1481. CONTROLSS\_PWMXBAR18\_G0 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR18_G0_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR18_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR18_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4519. CONTROLSS\_PWMXBAR18\_G0 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR18_G0_SEL | R/W  | 0h    | PWM XBAR18 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |

### 3.20.2.168 CONTROLSS\_PWMXBAR18\_G1 Register

#### 1 CONTROLSS\_PWMXBAR18\_G1 Register (Offset = 584h) [reset = 0h]

PWM XBAR 18 Input Select.

Return to [Summary Table](#)

**Table 3-4520. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1584h       |

**Figure 3-1482. CONTROLSS\_PWMXBAR18\_G1 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR18_G1_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR18_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR18_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4522. CONTROLSS\_PWMXBAR18\_G1 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR18_G1_SEL | R/W  | 0h    | PWM XBAR18 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.169 CONTROLSS\_PWMXBAR18\_G2 Register

#### 1 CONTROLSS\_PWMXBAR18\_G2 Register (Offset = 588h) [reset = 0h]

PWM XBAR 18 Input Select.

Return to [Summary Table](#)

**Table 3-4523. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1588h       |

**Figure 3-1483. CONTROLSS\_PWMXBAR18\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR18_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR18_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR18_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4525. CONTROLSS\_PWMXBAR18\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-4525. CONTROLSS\_PWMXBAR18\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR18_G2_SEL | R/W  | 0h    | PWM XBAR18 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.170 CONTROLSS\_PWMXBAR18\_G3 Register

#### 1 CONTROLSS\_PWMXBAR18\_G3 Register (Offset = 58Ch) [reset = 0h]

PWM XBAR 18 Input Select.

Return to [Summary Table](#)

**Table 3-4526. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 158Ch       |

**Figure 3-1484. CONTROLSS\_PWMXBAR18\_G3 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR18_G3_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR18_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR18_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4528. CONTROLSS\_PWMXBAR18\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                       |
|-------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                          |
| 19:0  | PWMXBAR18_G3_SEL | R/W  | 0h    | PWM XBAR18 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.20.2.171 CONTROLSS\_PWMXBAR18\_G4 Register

#### 1 CONTROLSS\_PWMXBAR18\_G4 Register (Offset = 590h) [reset = 0h]

PWM XBAR 18 Input Select.

Return to [Summary Table](#)

**Table 3-4529. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1590h       |

**Figure 3-1485. CONTROLSS\_PWMXBAR18\_G4 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR18_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR18_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR18_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR18_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4531. CONTROLSS\_PWMXBAR18\_G4 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR18_G4_SEL | R/W  | 0h    | PWM XBAR18 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.172 CONTROLSS\_PWMXBAR18\_G5 Register

#### 1 CONTROLSS\_PWMXBAR18\_G5 Register (Offset = 594h) [reset = 0h]

PWM XBAR 18 Input Select.

Return to [Summary Table](#)

**Table 3-4532. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1594h       |

**Figure 3-1486. CONTROLSS\_PWMXBAR18\_G5 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR18_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR18_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR18_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR18_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4534. CONTROLSS\_PWMXBAR18\_G5 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR18_G5_SEL | R/W  | 0h    | PWM XBAR18 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |



### 3.20.2.173 CONTROLSS\_PWMXBAR18\_G6 Register

#### 1 CONTROLSS\_PWMXBAR18\_G6 Register (Offset = 598h) [reset = 0h]

PWM XBAR 18 Input Select.

Return to [Summary Table](#)

**Table 3-4535. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1598h       |

**Figure 3-1487. CONTROLSS\_PWMXBAR18\_G6 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR18_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR18_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR18_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR18_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4537. CONTROLSS\_PWMXBAR18\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR18_G6_SEL | R/W  | 0h    | PWM XBAR18 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.174 CONTROLSS\_PWMXBAR18\_G7 Register

#### 1 CONTROLSS\_PWMXBAR18\_G7 Register (Offset = 59Ch) [reset = 0h]

PWM XBAR 18 Input Select.

Return to [Summary Table](#)

**Table 3-4538. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 159Ch       |

**Figure 3-1488. CONTROLSS\_PWMXBAR18\_G7 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR18_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR18_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR18_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR18_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4540. CONTROLSS\_PWMXBAR18\_G7 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                  |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR18_G7_SEL | R/W  | 0h    | PWM XBAR18 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |

### 3.20.2.175 CONTROLSS\_PWMXBAR18\_G8 Register

#### 1 CONTROLSS\_PWMXBAR18\_G8 Register (Offset = 5A0h) [reset = 0h]

PWM XBAR 18 Input Select.

Return to [Summary Table](#)

**Table 3-4541. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 15A0h       |

**Figure 3-1489. CONTROLSS\_PWMXBAR18\_G8 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    | PWMXBAR18_G8_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| PWMXBAR18_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR18_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR18_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4543. CONTROLSS\_PWMXBAR18\_G8 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                        |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                           |
| 28:0  | PWMXBAR18_G8_SEL | R/W  | 0h    | PWM XBAR18 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.176 CONTROLSS\_PWMXBAR19\_G0 Register

#### 1 CONTROLSS\_PWMXBAR19\_G0 Register (Offset = 5C0h) [reset = 0h]

PWM XBAR 19 Input Select.

Return to [Summary Table](#)

**Table 3-4544. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 15C0h       |

**Figure 3-1490. CONTROLSS\_PWMXBAR19\_G0 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR19_G0_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR19_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR19_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4546. CONTROLSS\_PWMXBAR19\_G0 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR19_G0_SEL | R/W  | 0h    | PWM XBAR19 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |

### 3.20.2.177 CONTROLSS\_PWMXBAR19\_G1 Register

#### 1 CONTROLSS\_PWMXBAR19\_G1 Register (Offset = 5C4h) [reset = 0h]

PWM XBAR 19 Input Select.

Return to [Summary Table](#)

**Table 3-4547. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 15C4h       |

**Figure 3-1491. CONTROLSS\_PWMXBAR19\_G1 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR19_G1_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR19_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR19_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4549. CONTROLSS\_PWMXBAR19\_G1 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR19_G1_SEL | R/W  | 0h    | PWM XBAR19 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.178 CONTROLSS\_PWMXBAR19\_G2 Register

#### 1 CONTROLSS\_PWMXBAR19\_G2 Register (Offset = 5C8h) [reset = 0h]

PWM XBAR 19 Input Select.

Return to [Summary Table](#)

**Table 3-4550. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 15C8h       |

**Figure 3-1492. CONTROLSS\_PWMXBAR19\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR19_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR19_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR19_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4552. CONTROLSS\_PWMXBAR19\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-4552. CONTROLSS\_PWMXBAR19\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR19_G2_SEL | R/W  | 0h    | PWM XBAR19 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.179 CONTROLSS\_PWMXBAR19\_G3 Register

#### 1 CONTROLSS\_PWMXBAR19\_G3 Register (Offset = 5CCh) [reset = 0h]

PWM XBAR 19 Input Select.

Return to [Summary Table](#)

**Table 3-4553. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 15CCh       |

**Figure 3-1493. CONTROLSS\_PWMXBAR19\_G3 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR19_G3_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR19_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR19_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4555. CONTROLSS\_PWMXBAR19\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                       |
|-------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                          |
| 19:0  | PWMXBAR19_G3_SEL | R/W  | 0h    | PWM XBAR19 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |



### 3.20.2.180 CONTROLSS\_PWMXBAR19\_G4 Register

#### 1 CONTROLSS\_PWMXBAR19\_G4 Register (Offset = 5D0h) [reset = 0h]

PWM XBAR 19 Input Select.

Return to [Summary Table](#)

**Table 3-4556. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 15D0h       |

**Figure 3-1494. CONTROLSS\_PWMXBAR19\_G4 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR19_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR19_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR19_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR19_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4558. CONTROLSS\_PWMXBAR19\_G4 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR19_G4_SEL | R/W  | 0h    | PWM XBAR19 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.181 CONTROLSS\_PWMXBAR19\_G5 Register

#### 1 CONTROLSS\_PWMXBAR19\_G5 Register (Offset = 5D4h) [reset = 0h]

PWM XBAR 19 Input Select.

Return to [Summary Table](#)

**Table 3-4559. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 15D4h       |

**Figure 3-1495. CONTROLSS\_PWMXBAR19\_G5 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR19_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR19_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR19_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR19_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4561. CONTROLSS\_PWMXBAR19\_G5 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR19_G5_SEL | R/W  | 0h    | PWM XBAR19 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |

### 3.20.2.182 CONTROLSS\_PWMXBAR19\_G6 Register

#### 1 CONTROLSS\_PWMXBAR19\_G6 Register (Offset = 5D8h) [reset = 0h]

PWM XBAR 19 Input Select.

Return to [Summary Table](#)

**Table 3-4562. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 15D8h       |

**Figure 3-1496. CONTROLSS\_PWMXBAR19\_G6 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR19_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR19_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR19_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR19_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4564. CONTROLSS\_PWMXBAR19\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR19_G6_SEL | R/W  | 0h    | PWM XBAR19 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.183 CONTROLSS\_PWMXBAR19\_G7 Register

#### 1 CONTROLSS\_PWMXBAR19\_G7 Register (Offset = 5DCh) [reset = 0h]

PWM XBAR 19 Input Select.

Return to [Summary Table](#)

**Table 3-4565. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 15DCh       |

**Figure 3-1497. CONTROLSS\_PWMXBAR19\_G7 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR19_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR19_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR19_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR19_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4567. CONTROLSS\_PWMXBAR19\_G7 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                  |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR19_G7_SEL | R/W  | 0h    | PWM XBAR19 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |

### 3.20.2.184 CONTROLSS\_PWMXBAR19\_G8 Register

#### 1 CONTROLSS\_PWMXBAR19\_G8 Register (Offset = 5E0h) [reset = 0h]

PWM XBAR 19 Input Select.

Return to [Summary Table](#)

**Table 3-4568. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 15E0h       |

**Figure 3-1498. CONTROLSS\_PWMXBAR19\_G8 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    | PWMXBAR19_G8_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| PWMXBAR19_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR19_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR19_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4570. CONTROLSS\_PWMXBAR19\_G8 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                        |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                           |
| 28:0  | PWMXBAR19_G8_SEL | R/W  | 0h    | PWM XBAR19 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.185 CONTROLSS\_PWMXBAR20\_G0 Register

#### 1 CONTROLSS\_PWMXBAR20\_G0 Register (Offset = 600h) [reset = 0h]

PWM XBAR 20 Input Select.

Return to [Summary Table](#)

**Table 3-4571. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1600h       |

**Figure 3-1499. CONTROLSS\_PWMXBAR20\_G0 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR20_G0_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR20_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR20_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4573. CONTROLSS\_PWMXBAR20\_G0 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR20_G0_SEL | R/W  | 0h    | PWM XBAR20 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |

### 3.20.2.186 CONTROLSS\_PWMXBAR20\_G1 Register

#### 1 CONTROLSS\_PWMXBAR20\_G1 Register (Offset = 604h) [reset = 0h]

PWM XBAR 20 Input Select.

Return to [Summary Table](#)

**Table 3-4574. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1604h       |

**Figure 3-1500. CONTROLSS\_PWMXBAR20\_G1 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR20_G1_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR20_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR20_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4576. CONTROLSS\_PWMXBAR20\_G1 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR20_G1_SEL | R/W  | 0h    | PWM XBAR20 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.187 CONTROLSS\_PWMXBAR20\_G2 Register

#### 1 CONTROLSS\_PWMXBAR20\_G2 Register (Offset = 608h) [reset = 0h]

PWM XBAR 20 Input Select.

Return to [Summary Table](#)

**Table 3-4577. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1608h       |

**Figure 3-1501. CONTROLSS\_PWMXBAR20\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR20_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR20_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR20_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4579. CONTROLSS\_PWMXBAR20\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |



**Table 3-4579. CONTROLSS\_PWMXBAR20\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR20_G2_SEL | R/W  | 0h    | PWM XBAR20 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.188 CONTROLSS\_PWMXBAR20\_G3 Register

#### 1 CONTROLSS\_PWMXBAR20\_G3 Register (Offset = 60Ch) [reset = 0h]

PWM XBAR 20 Input Select.

Return to [Summary Table](#)

**Table 3-4580. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 160Ch       |

**Figure 3-1502. CONTROLSS\_PWMXBAR20\_G3 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR20_G3_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR20_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR20_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4582. CONTROLSS\_PWMXBAR20\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                       |
|-------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                          |
| 19:0  | PWMXBAR20_G3_SEL | R/W  | 0h    | PWM XBAR20 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.20.2.189 CONTROLSS\_PWMXBAR20\_G4 Register

#### 1 CONTROLSS\_PWMXBAR20\_G4 Register (Offset = 610h) [reset = 0h]

PWM XBAR 20 Input Select.

Return to [Summary Table](#)

**Table 3-4583. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1610h       |

**Figure 3-1503. CONTROLSS\_PWMXBAR20\_G4 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR20_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR20_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR20_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR20_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4585. CONTROLSS\_PWMXBAR20\_G4 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR20_G4_SEL | R/W  | 0h    | PWM XBAR20 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.190 CONTROLSS\_PWMXBAR20\_G5 Register

#### 1 CONTROLSS\_PWMXBAR20\_G5 Register (Offset = 614h) [reset = 0h]

PWM XBAR 20 Input Select.

Return to [Summary Table](#)

**Table 3-4586. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1614h       |

**Figure 3-1504. CONTROLSS\_PWMXBAR20\_G5 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR20_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR20_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR20_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR20_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4588. CONTROLSS\_PWMXBAR20\_G5 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR20_G5_SEL | R/W  | 0h    | PWM XBAR20 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |

### 3.20.2.191 CONTROLSS\_PWMXBAR20\_G6 Register

#### 1 CONTROLSS\_PWMXBAR20\_G6 Register (Offset = 618h) [reset = 0h]

PWM XBAR 20 Input Select.

Return to [Summary Table](#)

**Table 3-4589. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1618h       |

**Figure 3-1505. CONTROLSS\_PWMXBAR20\_G6 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR20_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR20_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR20_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR20_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4591. CONTROLSS\_PWMXBAR20\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR20_G6_SEL | R/W  | 0h    | PWM XBAR20 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.192 CONTROLSS\_PWMXBAR20\_G7 Register

#### 1 CONTROLSS\_PWMXBAR20\_G7 Register (Offset = 61Ch) [reset = 0h]

PWM XBAR 20 Input Select.

Return to [Summary Table](#)

**Table 3-4592. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 161Ch       |

**Figure 3-1506. CONTROLSS\_PWMXBAR20\_G7 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR20_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR20_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR20_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR20_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4594. CONTROLSS\_PWMXBAR20\_G7 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                  |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR20_G7_SEL | R/W  | 0h    | PWM XBAR20 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |

### 3.20.2.193 CONTROLSS\_PWMXBAR20\_G8 Register

#### 1 CONTROLSS\_PWMXBAR20\_G8 Register (Offset = 620h) [reset = 0h]

PWM XBAR 20 Input Select.

Return to [Summary Table](#)

**Table 3-4595. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1620h       |

**Figure 3-1507. CONTROLSS\_PWMXBAR20\_G8 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    | PWMXBAR20_G8_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| PWMXBAR20_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR20_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR20_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4597. CONTROLSS\_PWMXBAR20\_G8 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                        |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                           |
| 28:0  | PWMXBAR20_G8_SEL | R/W  | 0h    | PWM XBAR20 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.194 CONTROLSS\_PWMXBAR21\_G0 Register

#### 1 CONTROLSS\_PWMXBAR21\_G0 Register (Offset = 640h) [reset = 0h]

PWM XBAR 21 Input Select.

Return to [Summary Table](#)

**Table 3-4598. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1640h       |

**Figure 3-1508. CONTROLSS\_PWMXBAR21\_G0 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR21_G0_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR21_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR21_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4600. CONTROLSS\_PWMXBAR21\_G0 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR21_G0_SEL | R/W  | 0h    | PWM XBAR21 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |



### 3.20.2.195 CONTROLSS\_PWMXBAR21\_G1 Register

#### 1 CONTROLSS\_PWMXBAR21\_G1 Register (Offset = 644h) [reset = 0h]

PWM XBAR 21 Input Select.

Return to [Summary Table](#)

**Table 3-4601. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1644h       |

**Figure 3-1509. CONTROLSS\_PWMXBAR21\_G1 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR21_G1_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR21_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR21_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4603. CONTROLSS\_PWMXBAR21\_G1 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR21_G1_SEL | R/W  | 0h    | PWM XBAR21 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.196 CONTROLSS\_PWMXBAR21\_G2 Register

#### 1 CONTROLSS\_PWMXBAR21\_G2 Register (Offset = 648h) [reset = 0h]

PWM XBAR 21 Input Select.

Return to [Summary Table](#)

**Table 3-4604. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1648h       |

**Figure 3-1510. CONTROLSS\_PWMXBAR21\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR21_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR21_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR21_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4606. CONTROLSS\_PWMXBAR21\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-4606. CONTROLSS\_PWMXBAR21\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR21_G2_SEL | R/W  | 0h    | PWM XBAR21 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.197 CONTROLSS\_PWMXBAR21\_G3 Register

#### 1 CONTROLSS\_PWMXBAR21\_G3 Register (Offset = 64Ch) [reset = 0h]

PWM XBAR 21 Input Select.

Return to [Summary Table](#)

**Table 3-4607. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 164Ch       |

**Figure 3-1511. CONTROLSS\_PWMXBAR21\_G3 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR21_G3_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR21_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR21_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4609. CONTROLSS\_PWMXBAR21\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                       |
|-------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                          |
| 19:0  | PWMXBAR21_G3_SEL | R/W  | 0h    | PWM XBAR21 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.20.2.198 CONTROLSS\_PWMXBAR21\_G4 Register

#### 1 CONTROLSS\_PWMXBAR21\_G4 Register (Offset = 650h) [reset = 0h]

PWM XBAR 21 Input Select.

Return to [Summary Table](#)

**Table 3-4610. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1650h       |

**Figure 3-1512. CONTROLSS\_PWMXBAR21\_G4 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR21_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR21_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR21_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR21_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4612. CONTROLSS\_PWMXBAR21\_G4 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR21_G4_SEL | R/W  | 0h    | PWM XBAR21 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.199 CONTROLSS\_PWMXBAR21\_G5 Register

#### 1 CONTROLSS\_PWMXBAR21\_G5 Register (Offset = 654h) [reset = 0h]

PWM XBAR 21 Input Select.

Return to [Summary Table](#)

**Table 3-4613. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1654h       |

**Figure 3-1513. CONTROLSS\_PWMXBAR21\_G5 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR21_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR21_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR21_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR21_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4615. CONTROLSS\_PWMXBAR21\_G5 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR21_G5_SEL | R/W  | 0h    | PWM XBAR21 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |

### 3.20.2.200 CONTROLSS\_PWMXBAR21\_G6 Register

#### 1 CONTROLSS\_PWMXBAR21\_G6 Register (Offset = 658h) [reset = 0h]

PWM XBAR 21 Input Select.

Return to [Summary Table](#)

**Table 3-4616. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1658h       |

**Figure 3-1514. CONTROLSS\_PWMXBAR21\_G6 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR21_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR21_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR21_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR21_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4618. CONTROLSS\_PWMXBAR21\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR21_G6_SEL | R/W  | 0h    | PWM XBAR21 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.201 CONTROLSS\_PWMXBAR21\_G7 Register

#### 1 CONTROLSS\_PWMXBAR21\_G7 Register (Offset = 65Ch) [reset = 0h]

PWM XBAR 21 Input Select.

Return to [Summary Table](#)

**Table 3-4619. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 165Ch       |

**Figure 3-1515. CONTROLSS\_PWMXBAR21\_G7 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR21_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR21_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR21_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR21_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4621. CONTROLSS\_PWMXBAR21\_G7 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                  |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR21_G7_SEL | R/W  | 0h    | PWM XBAR21 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |



### 3.20.2.202 CONTROLSS\_PWMXBAR21\_G8 Register

#### 1 CONTROLSS\_PWMXBAR21\_G8 Register (Offset = 660h) [reset = 0h]

PWM XBAR 21 Input Select.

Return to [Summary Table](#)

**Table 3-4622. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1660h       |

**Figure 3-1516. CONTROLSS\_PWMXBAR21\_G8 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    | PWMXBAR21_G8_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| PWMXBAR21_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR21_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR21_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4624. CONTROLSS\_PWMXBAR21\_G8 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                        |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                           |
| 28:0  | PWMXBAR21_G8_SEL | R/W  | 0h    | PWM XBAR21 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.203 CONTROLSS\_PWMXBAR22\_G0 Register

#### 1 CONTROLSS\_PWMXBAR22\_G0 Register (Offset = 680h) [reset = 0h]

PWM XBAR 22 Input Select.

Return to [Summary Table](#)

**Table 3-4625. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1680h       |

**Figure 3-1517. CONTROLSS\_PWMXBAR22\_G0 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR22_G0_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR22_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR22_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4627. CONTROLSS\_PWMXBAR22\_G0 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR22_G0_SEL | R/W  | 0h    | PWM XBAR22 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |

### 3.20.2.204 CONTROLSS\_PWMXBAR22\_G1 Register

#### 1 CONTROLSS\_PWMXBAR22\_G1 Register (Offset = 684h) [reset = 0h]

PWM XBAR 22 Input Select.

Return to [Summary Table](#)

**Table 3-4628. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1684h       |

**Figure 3-1518. CONTROLSS\_PWMXBAR22\_G1 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR22_G1_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR22_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR22_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4630. CONTROLSS\_PWMXBAR22\_G1 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR22_G1_SEL | R/W  | 0h    | PWM XBAR22 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.205 CONTROLSS\_PWMXBAR22\_G2 Register

#### 1 CONTROLSS\_PWMXBAR22\_G2 Register (Offset = 688h) [reset = 0h]

PWM XBAR 22 Input Select.

Return to [Summary Table](#)

**Table 3-4631. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1688h       |

**Figure 3-1519. CONTROLSS\_PWMXBAR22\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR22_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR22_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR22_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4633. CONTROLSS\_PWMXBAR22\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-4633. CONTROLSS\_PWMXBAR22\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR22_G2_SEL | R/W  | 0h    | PWM XBAR22 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.206 CONTROLSS\_PWMXBAR22\_G3 Register

#### 1 CONTROLSS\_PWMXBAR22\_G3 Register (Offset = 68Ch) [reset = 0h]

PWM XBAR 22 Input Select.

Return to [Summary Table](#)

**Table 3-4634. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 168Ch       |

**Figure 3-1520. CONTROLSS\_PWMXBAR22\_G3 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR22_G3_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR22_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR22_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4636. CONTROLSS\_PWMXBAR22\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                       |
|-------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                          |
| 19:0  | PWMXBAR22_G3_SEL | R/W  | 0h    | PWM XBAR22 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.20.2.207 CONTROLSS\_PWMXBAR22\_G4 Register

#### 1 CONTROLSS\_PWMXBAR22\_G4 Register (Offset = 690h) [reset = 0h]

PWM XBAR 22 Input Select.

Return to [Summary Table](#)

**Table 3-4637. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1690h       |

**Figure 3-1521. CONTROLSS\_PWMXBAR22\_G4 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR22_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR22_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR22_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR22_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4639. CONTROLSS\_PWMXBAR22\_G4 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR22_G4_SEL | R/W  | 0h    | PWM XBAR22 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.208 CONTROLSS\_PWMXBAR22\_G5 Register

#### 1 CONTROLSS\_PWMXBAR22\_G5 Register (Offset = 694h) [reset = 0h]

PWM XBAR 22 Input Select.

Return to [Summary Table](#)

**Table 3-4640. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1694h       |

**Figure 3-1522. CONTROLSS\_PWMXBAR22\_G5 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR22_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR22_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR22_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR22_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4642. CONTROLSS\_PWMXBAR22\_G5 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR22_G5_SEL | R/W  | 0h    | PWM XBAR22 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |



### 3.20.2.209 CONTROLSS\_PWMXBAR22\_G6 Register

#### 1 CONTROLSS\_PWMXBAR22\_G6 Register (Offset = 698h) [reset = 0h]

PWM XBAR 22 Input Select.

Return to [Summary Table](#)

**Table 3-4643. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1698h       |

**Figure 3-1523. CONTROLSS\_PWMXBAR22\_G6 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR22_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR22_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR22_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR22_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4645. CONTROLSS\_PWMXBAR22\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR22_G6_SEL | R/W  | 0h    | PWM XBAR22 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.210 CONTROLSS\_PWMXBAR22\_G7 Register

#### 1 CONTROLSS\_PWMXBAR22\_G7 Register (Offset = 69Ch) [reset = 0h]

PWM XBAR 22 Input Select.

Return to [Summary Table](#)

**Table 3-4646. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 169Ch       |

**Figure 3-1524. CONTROLSS\_PWMXBAR22\_G7 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR22_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR22_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR22_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR22_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4648. CONTROLSS\_PWMXBAR22\_G7 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                  |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR22_G7_SEL | R/W  | 0h    | PWM XBAR22 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |

### 3.20.2.211 CONTROLSS\_PWMXBAR22\_G8 Register

#### 1 CONTROLSS\_PWMXBAR22\_G8 Register (Offset = 6A0h) [reset = 0h]

PWM XBAR 22 Input Select.

Return to [Summary Table](#)

**Table 3-4649. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 16A0h       |

**Figure 3-1525. CONTROLSS\_PWMXBAR22\_G8 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    | PWMXBAR22_G8_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| PWMXBAR22_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR22_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR22_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4651. CONTROLSS\_PWMXBAR22\_G8 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                        |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                           |
| 28:0  | PWMXBAR22_G8_SEL | R/W  | 0h    | PWM XBAR22 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.212 CONTROLSS\_PWMXBAR23\_G0 Register

#### 1 CONTROLSS\_PWMXBAR23\_G0 Register (Offset = 6C0h) [reset = 0h]

PWM XBAR 23 Input Select.

Return to [Summary Table](#)

**Table 3-4652. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 16C0h       |

**Figure 3-1526. CONTROLSS\_PWMXBAR23\_G0 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR23_G0_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR23_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR23_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4654. CONTROLSS\_PWMXBAR23\_G0 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR23_G0_SEL | R/W  | 0h    | PWM XBAR23 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |

### 3.20.2.213 CONTROLSS\_PWMXBAR23\_G1 Register

#### 1 CONTROLSS\_PWMXBAR23\_G1 Register (Offset = 6C4h) [reset = 0h]

PWM XBAR 23 Input Select.

Return to [Summary Table](#)

**Table 3-4655. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 16C4h       |

**Figure 3-1527. CONTROLSS\_PWMXBAR23\_G1 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR23_G1_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR23_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR23_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4657. CONTROLSS\_PWMXBAR23\_G1 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR23_G1_SEL | R/W  | 0h    | PWM XBAR23 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.214 CONTROLSS\_PWMXBAR23\_G2 Register

#### 1 CONTROLSS\_PWMXBAR23\_G2 Register (Offset = 6C8h) [reset = 0h]

PWM XBAR 23 Input Select.

Return to [Summary Table](#)

**Table 3-4658. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 16C8h       |

**Figure 3-1528. CONTROLSS\_PWMXBAR23\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR23_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR23_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR23_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4660. CONTROLSS\_PWMXBAR23\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-4660. CONTROLSS\_PWMXBAR23\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR23_G2_SEL | R/W  | 0h    | PWM XBAR23 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.215 CONTROLSS\_PWMXBAR23\_G3 Register

#### 1 CONTROLSS\_PWMXBAR23\_G3 Register (Offset = 6CCh) [reset = 0h]

PWM XBAR 23 Input Select.

Return to [Summary Table](#)

**Table 3-4661. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 16CCh       |

**Figure 3-1529. CONTROLSS\_PWMXBAR23\_G3 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR23_G3_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR23_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR23_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4663. CONTROLSS\_PWMXBAR23\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                       |
|-------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                          |
| 19:0  | PWMXBAR23_G3_SEL | R/W  | 0h    | PWM XBAR23 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |



### 3.20.2.216 CONTROLSS\_PWMXBAR23\_G4 Register

#### 1 CONTROLSS\_PWMXBAR23\_G4 Register (Offset = 6D0h) [reset = 0h]

PWM XBAR 23 Input Select.

Return to [Summary Table](#)

**Table 3-4664. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 16D0h       |

**Figure 3-1530. CONTROLSS\_PWMXBAR23\_G4 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR23_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR23_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR23_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR23_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4666. CONTROLSS\_PWMXBAR23\_G4 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR23_G4_SEL | R/W  | 0h    | PWM XBAR23 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.217 CONTROLSS\_PWMXBAR23\_G5 Register

#### 1 CONTROLSS\_PWMXBAR23\_G5 Register (Offset = 6D4h) [reset = 0h]

PWM XBAR 23 Input Select.

Return to [Summary Table](#)

**Table 3-4667. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 16D4h       |

**Figure 3-1531. CONTROLSS\_PWMXBAR23\_G5 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR23_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR23_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR23_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR23_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4669. CONTROLSS\_PWMXBAR23\_G5 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR23_G5_SEL | R/W  | 0h    | PWM XBAR23 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |

### 3.20.2.218 CONTROLSS\_PWMXBAR23\_G6 Register

#### 1 CONTROLSS\_PWMXBAR23\_G6 Register (Offset = 6D8h) [reset = 0h]

PWM XBAR 23 Input Select.

Return to [Summary Table](#)

**Table 3-4670. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 16D8h       |

**Figure 3-1532. CONTROLSS\_PWMXBAR23\_G6 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR23_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR23_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR23_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR23_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4672. CONTROLSS\_PWMXBAR23\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR23_G6_SEL | R/W  | 0h    | PWM XBAR23 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.219 CONTROLSS\_PWMXBAR23\_G7 Register

#### 1 CONTROLSS\_PWMXBAR23\_G7 Register (Offset = 6DCh) [reset = 0h]

PWM XBAR 23 Input Select.

Return to [Summary Table](#)

**Table 3-4673. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 16DCh       |

**Figure 3-1533. CONTROLSS\_PWMXBAR23\_G7 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR23_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR23_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR23_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR23_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4675. CONTROLSS\_PWMXBAR23\_G7 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                  |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR23_G7_SEL | R/W  | 0h    | PWM XBAR23 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |

### 3.20.2.220 CONTROLSS\_PWMXBAR23\_G8 Register

#### 1 CONTROLSS\_PWMXBAR23\_G8 Register (Offset = 6E0h) [reset = 0h]

PWM XBAR 23 Input Select.

Return to [Summary Table](#)

**Table 3-4676. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 16E0h       |

**Figure 3-1534. CONTROLSS\_PWMXBAR23\_G8 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    | PWMXBAR23_G8_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| PWMXBAR23_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR23_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR23_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4678. CONTROLSS\_PWMXBAR23\_G8 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                        |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                           |
| 28:0  | PWMXBAR23_G8_SEL | R/W  | 0h    | PWM XBAR23 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.221 CONTROLSS\_PWMXBAR24\_G0 Register

#### 1 CONTROLSS\_PWMXBAR24\_G0 Register (Offset = 700h) [reset = 0h]

PWM XBAR 24 Input Select.

Return to [Summary Table](#)

**Table 3-4679. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1700h       |

**Figure 3-1535. CONTROLSS\_PWMXBAR24\_G0 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR24_G0_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR24_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR24_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4681. CONTROLSS\_PWMXBAR24\_G0 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR24_G0_SEL | R/W  | 0h    | PWM XBAR24 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |

### 3.20.2.222 CONTROLSS\_PWMXBAR24\_G1 Register

#### 1 CONTROLSS\_PWMXBAR24\_G1 Register (Offset = 704h) [reset = 0h]

PWM XBAR 24 Input Select.

Return to [Summary Table](#)

**Table 3-4682. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1704h       |

**Figure 3-1536. CONTROLSS\_PWMXBAR24\_G1 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR24_G1_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR24_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR24_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4684. CONTROLSS\_PWMXBAR24\_G1 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR24_G1_SEL | R/W  | 0h    | PWM XBAR24 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.223 CONTROLSS\_PWMXBAR24\_G2 Register

#### 1 CONTROLSS\_PWMXBAR24\_G2 Register (Offset = 708h) [reset = 0h]

PWM XBAR 24 Input Select.

Return to [Summary Table](#)

**Table 3-4685. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1708h       |

**Figure 3-1537. CONTROLSS\_PWMXBAR24\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR24_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR24_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR24_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4687. CONTROLSS\_PWMXBAR24\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |



**Table 3-4687. CONTROLSS\_PWMXBAR24\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR24_G2_SEL | R/W  | 0h    | PWM XBAR24 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.224 CONTROLSS\_PWMXBAR24\_G3 Register

#### 1 CONTROLSS\_PWMXBAR24\_G3 Register (Offset = 70Ch) [reset = 0h]

PWM XBAR 24 Input Select.

Return to [Summary Table](#)

**Table 3-4688. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 170Ch       |

**Figure 3-1538. CONTROLSS\_PWMXBAR24\_G3 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR24_G3_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR24_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR24_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4690. CONTROLSS\_PWMXBAR24\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                       |
|-------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                          |
| 19:0  | PWMXBAR24_G3_SEL | R/W  | 0h    | PWM XBAR24 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.20.2.225 CONTROLSS\_PWMXBAR24\_G4 Register

#### 1 CONTROLSS\_PWMXBAR24\_G4 Register (Offset = 710h) [reset = 0h]

PWM XBAR 24 Input Select.

Return to [Summary Table](#)

**Table 3-4691. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1710h       |

**Figure 3-1539. CONTROLSS\_PWMXBAR24\_G4 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR24_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR24_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR24_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR24_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4693. CONTROLSS\_PWMXBAR24\_G4 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR24_G4_SEL | R/W  | 0h    | PWM XBAR24 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.226 CONTROLSS\_PWMXBAR24\_G5 Register

#### 1 CONTROLSS\_PWMXBAR24\_G5 Register (Offset = 714h) [reset = 0h]

PWM XBAR 24 Input Select.

Return to [Summary Table](#)

**Table 3-4694. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1714h       |

**Figure 3-1540. CONTROLSS\_PWMXBAR24\_G5 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR24_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR24_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR24_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR24_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4696. CONTROLSS\_PWMXBAR24\_G5 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR24_G5_SEL | R/W  | 0h    | PWM XBAR24 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |

### 3.20.2.227 CONTROLSS\_PWMXBAR24\_G6 Register

#### 1 CONTROLSS\_PWMXBAR24\_G6 Register (Offset = 718h) [reset = 0h]

PWM XBAR 24 Input Select.

Return to [Summary Table](#)

**Table 3-4697. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1718h       |

**Figure 3-1541. CONTROLSS\_PWMXBAR24\_G6 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR24_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR24_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR24_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR24_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4699. CONTROLSS\_PWMXBAR24\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR24_G6_SEL | R/W  | 0h    | PWM XBAR24 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.228 CONTROLSS\_PWMXBAR24\_G7 Register

#### 1 CONTROLSS\_PWMXBAR24\_G7 Register (Offset = 71Ch) [reset = 0h]

PWM XBAR 24 Input Select.

Return to [Summary Table](#)

**Table 3-4700. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 171Ch       |

**Figure 3-1542. CONTROLSS\_PWMXBAR24\_G7 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR24_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR24_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR24_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR24_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4702. CONTROLSS\_PWMXBAR24\_G7 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                  |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR24_G7_SEL | R/W  | 0h    | PWM XBAR24 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |

### 3.20.2.229 CONTROLSS\_PWMXBAR24\_G8 Register

#### 1 CONTROLSS\_PWMXBAR24\_G8 Register (Offset = 720h) [reset = 0h]

PWM XBAR 24 Input Select.

Return to [Summary Table](#)

**Table 3-4703. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1720h       |

**Figure 3-1543. CONTROLSS\_PWMXBAR24\_G8 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    | PWMXBAR24_G8_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| PWMXBAR24_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR24_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR24_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4705. CONTROLSS\_PWMXBAR24\_G8 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                        |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                           |
| 28:0  | PWMXBAR24_G8_SEL | R/W  | 0h    | PWM XBAR24 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.230 CONTROLSS\_PWMXBAR25\_G0 Register

#### 1 CONTROLSS\_PWMXBAR25\_G0 Register (Offset = 740h) [reset = 0h]

PWM XBAR 25 Input Select.

Return to [Summary Table](#)

**Table 3-4706. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1740h       |

**Figure 3-1544. CONTROLSS\_PWMXBAR25\_G0 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR25_G0_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR25_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR25_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4708. CONTROLSS\_PWMXBAR25\_G0 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR25_G0_SEL | R/W  | 0h    | PWM XBAR25 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |



### 3.20.2.231 CONTROLSS\_PWMXBAR25\_G1 Register

#### 1 CONTROLSS\_PWMXBAR25\_G1 Register (Offset = 744h) [reset = 0h]

PWM XBAR 25 Input Select.

Return to [Summary Table](#)

**Table 3-4709. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1744h       |

**Figure 3-1545. CONTROLSS\_PWMXBAR25\_G1 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR25_G1_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR25_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR25_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4711. CONTROLSS\_PWMXBAR25\_G1 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR25_G1_SEL | R/W  | 0h    | PWM XBAR25 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.232 CONTROLSS\_PWMXBAR25\_G2 Register

#### 1 CONTROLSS\_PWMXBAR25\_G2 Register (Offset = 748h) [reset = 0h]

PWM XBAR 25 Input Select.

Return to [Summary Table](#)

**Table 3-4712. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1748h       |

**Figure 3-1546. CONTROLSS\_PWMXBAR25\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR25_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR25_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR25_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4714. CONTROLSS\_PWMXBAR25\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-4714. CONTROLSS\_PWMXBAR25\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR25_G2_SEL | R/W  | 0h    | PWM XBAR25 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.233 CONTROLSS\_PWMXBAR25\_G3 Register

#### 1 CONTROLSS\_PWMXBAR25\_G3 Register (Offset = 74Ch) [reset = 0h]

PWM XBAR 25 Input Select.

Return to [Summary Table](#)

**Table 3-4715. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 174Ch       |

**Figure 3-1547. CONTROLSS\_PWMXBAR25\_G3 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR25_G3_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR25_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR25_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4717. CONTROLSS\_PWMXBAR25\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                       |
|-------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                          |
| 19:0  | PWMXBAR25_G3_SEL | R/W  | 0h    | PWM XBAR25 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.20.2.234 CONTROLSS\_PWMXBAR25\_G4 Register

#### 1 CONTROLSS\_PWMXBAR25\_G4 Register (Offset = 750h) [reset = 0h]

PWM XBAR 25 Input Select.

Return to [Summary Table](#)

**Table 3-4718. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1750h       |

**Figure 3-1548. CONTROLSS\_PWMXBAR25\_G4 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR25_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR25_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR25_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR25_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4720. CONTROLSS\_PWMXBAR25\_G4 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR25_G4_SEL | R/W  | 0h    | PWM XBAR25 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.235 CONTROLSS\_PWMXBAR25\_G5 Register

#### 1 CONTROLSS\_PWMXBAR25\_G5 Register (Offset = 754h) [reset = 0h]

PWM XBAR 25 Input Select.

Return to [Summary Table](#)

**Table 3-4721. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1754h       |

**Figure 3-1549. CONTROLSS\_PWMXBAR25\_G5 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR25_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR25_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR25_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR25_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4723. CONTROLSS\_PWMXBAR25\_G5 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR25_G5_SEL | R/W  | 0h    | PWM XBAR25 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |

### 3.20.2.236 CONTROLSS\_PWMXBAR25\_G6 Register

#### 1 CONTROLSS\_PWMXBAR25\_G6 Register (Offset = 758h) [reset = 0h]

PWM XBAR 25 Input Select.

Return to [Summary Table](#)

**Table 3-4724. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1758h       |

**Figure 3-1550. CONTROLSS\_PWMXBAR25\_G6 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR25_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR25_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR25_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR25_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4726. CONTROLSS\_PWMXBAR25\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR25_G6_SEL | R/W  | 0h    | PWM XBAR25 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.237 CONTROLSS\_PWMXBAR25\_G7 Register

#### 1 CONTROLSS\_PWMXBAR25\_G7 Register (Offset = 75Ch) [reset = 0h]

PWM XBAR 25 Input Select.

Return to [Summary Table](#)

**Table 3-4727. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 175Ch       |

**Figure 3-1551. CONTROLSS\_PWMXBAR25\_G7 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR25_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR25_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR25_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR25_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4729. CONTROLSS\_PWMXBAR25\_G7 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                  |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR25_G7_SEL | R/W  | 0h    | PWM XBAR25 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |



### 3.20.2.238 CONTROLSS\_PWMXBAR25\_G8 Register

#### 1 CONTROLSS\_PWMXBAR25\_G8 Register (Offset = 760h) [reset = 0h]

PWM XBAR 25 Input Select.

Return to [Summary Table](#)

**Table 3-4730. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1760h       |

**Figure 3-1552. CONTROLSS\_PWMXBAR25\_G8 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    | PWMXBAR25_G8_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| PWMXBAR25_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR25_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR25_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4732. CONTROLSS\_PWMXBAR25\_G8 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                        |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                           |
| 28:0  | PWMXBAR25_G8_SEL | R/W  | 0h    | PWM XBAR25 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.239 CONTROLSS\_PWMXBAR26\_G0 Register

#### 1 CONTROLSS\_PWMXBAR26\_G0 Register (Offset = 780h) [reset = 0h]

PWM XBAR 26 Input Select.

Return to [Summary Table](#)

**Table 3-4733. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1780h       |

**Figure 3-1553. CONTROLSS\_PWMXBAR26\_G0 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR26_G0_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR26_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR26_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4735. CONTROLSS\_PWMXBAR26\_G0 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR26_G0_SEL | R/W  | 0h    | PWM XBAR26 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |

### 3.20.2.240 CONTROLSS\_PWMXBAR26\_G1 Register

#### 1 CONTROLSS\_PWMXBAR26\_G1 Register (Offset = 784h) [reset = 0h]

PWM XBAR 26 Input Select.

Return to [Summary Table](#)

**Table 3-4736. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1784h       |

**Figure 3-1554. CONTROLSS\_PWMXBAR26\_G1 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR26_G1_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR26_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR26_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4738. CONTROLSS\_PWMXBAR26\_G1 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR26_G1_SEL | R/W  | 0h    | PWM XBAR26 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.241 CONTROLSS\_PWMXBAR26\_G2 Register

#### 1 CONTROLSS\_PWMXBAR26\_G2 Register (Offset = 788h) [reset = 0h]

PWM XBAR 26 Input Select.

Return to [Summary Table](#)

**Table 3-4739. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1788h       |

**Figure 3-1555. CONTROLSS\_PWMXBAR26\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR26_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR26_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR26_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4741. CONTROLSS\_PWMXBAR26\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-4741. CONTROLSS\_PWMXBAR26\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR26_G2_SEL | R/W  | 0h    | PWM XBAR26 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.242 CONTROLSS\_PWMXBAR26\_G3 Register

#### 1 CONTROLSS\_PWMXBAR26\_G3 Register (Offset = 78Ch) [reset = 0h]

PWM XBAR 26 Input Select.

Return to [Summary Table](#)

**Table 3-4742. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 178Ch       |

**Figure 3-1556. CONTROLSS\_PWMXBAR26\_G3 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR26_G3_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR26_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR26_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4744. CONTROLSS\_PWMXBAR26\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                       |
|-------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                          |
| 19:0  | PWMXBAR26_G3_SEL | R/W  | 0h    | PWM XBAR26 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.20.2.243 CONTROLSS\_PWMXBAR26\_G4 Register

#### 1 CONTROLSS\_PWMXBAR26\_G4 Register (Offset = 790h) [reset = 0h]

PWM XBAR 26 Input Select.

Return to [Summary Table](#)

**Table 3-4745. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1790h       |

**Figure 3-1557. CONTROLSS\_PWMXBAR26\_G4 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR26_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR26_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR26_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR26_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4747. CONTROLSS\_PWMXBAR26\_G4 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR26_G4_SEL | R/W  | 0h    | PWM XBAR26 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.244 CONTROLSS\_PWMXBAR26\_G5 Register

#### 1 CONTROLSS\_PWMXBAR26\_G5 Register (Offset = 794h) [reset = 0h]

PWM XBAR 26 Input Select.

Return to [Summary Table](#)

**Table 3-4748. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1794h       |

**Figure 3-1558. CONTROLSS\_PWMXBAR26\_G5 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR26_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR26_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR26_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR26_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4750. CONTROLSS\_PWMXBAR26\_G5 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR26_G5_SEL | R/W  | 0h    | PWM XBAR26 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |



### 3.20.2.245 CONTROLSS\_PWMXBAR26\_G6 Register

#### 1 CONTROLSS\_PWMXBAR26\_G6 Register (Offset = 798h) [reset = 0h]

PWM XBAR 26 Input Select.

Return to [Summary Table](#)

**Table 3-4751. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1798h       |

**Figure 3-1559. CONTROLSS\_PWMXBAR26\_G6 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR26_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR26_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR26_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR26_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4753. CONTROLSS\_PWMXBAR26\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR26_G6_SEL | R/W  | 0h    | PWM XBAR26 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.246 CONTROLSS\_PWMXBAR26\_G7 Register

#### 1 CONTROLSS\_PWMXBAR26\_G7 Register (Offset = 79Ch) [reset = 0h]

PWM XBAR 26 Input Select.

Return to [Summary Table](#)

**Table 3-4754. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 179Ch       |

**Figure 3-1560. CONTROLSS\_PWMXBAR26\_G7 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR26_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR26_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR26_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR26_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4756. CONTROLSS\_PWMXBAR26\_G7 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                  |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR26_G7_SEL | R/W  | 0h    | PWM XBAR26 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |

### 3.20.2.247 CONTROLSS\_PWMXBAR26\_G8 Register

#### 1 CONTROLSS\_PWMXBAR26\_G8 Register (Offset = 7A0h) [reset = 0h]

PWM XBAR 26 Input Select.

Return to [Summary Table](#)

**Table 3-4757. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 17A0h       |

**Figure 3-1561. CONTROLSS\_PWMXBAR26\_G8 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    | PWMXBAR26_G8_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| PWMXBAR26_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR26_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR26_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4759. CONTROLSS\_PWMXBAR26\_G8 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                        |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                           |
| 28:0  | PWMXBAR26_G8_SEL | R/W  | 0h    | PWM XBAR26 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.248 CONTROLSS\_PWMXBAR27\_G0 Register

#### 1 CONTROLSS\_PWMXBAR27\_G0 Register (Offset = 7C0h) [reset = 0h]

PWM XBAR 27 Input Select.

Return to [Summary Table](#)

**Table 3-4760. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 17C0h       |

**Figure 3-1562. CONTROLSS\_PWMXBAR27\_G0 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR27_G0_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR27_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR27_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4762. CONTROLSS\_PWMXBAR27\_G0 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR27_G0_SEL | R/W  | 0h    | PWM XBAR27 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |

### 3.20.2.249 CONTROLSS\_PWMXBAR27\_G1 Register

#### 1 CONTROLSS\_PWMXBAR27\_G1 Register (Offset = 7C4h) [reset = 0h]

PWM XBAR 27 Input Select.

Return to [Summary Table](#)

**Table 3-4763. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 17C4h       |

**Figure 3-1563. CONTROLSS\_PWMXBAR27\_G1 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR27_G1_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR27_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR27_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4765. CONTROLSS\_PWMXBAR27\_G1 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR27_G1_SEL | R/W  | 0h    | PWM XBAR27 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.250 CONTROLSS\_PWMXBAR27\_G2 Register

#### 1 CONTROLSS\_PWMXBAR27\_G2 Register (Offset = 7C8h) [reset = 0h]

PWM XBAR 27 Input Select.

Return to [Summary Table](#)

**Table 3-4766. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 17C8h       |

**Figure 3-1564. CONTROLSS\_PWMXBAR27\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR27_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR27_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR27_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4768. CONTROLSS\_PWMXBAR27\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-4768. CONTROLSS\_PWMXBAR27\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR27_G2_SEL | R/W  | 0h    | PWM XBAR27 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.251 CONTROLSS\_PWMXBAR27\_G3 Register

#### 1 CONTROLSS\_PWMXBAR27\_G3 Register (Offset = 7CCh) [reset = 0h]

PWM XBAR 27 Input Select.

Return to [Summary Table](#)

**Table 3-4769. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 17CCh       |

**Figure 3-1565. CONTROLSS\_PWMXBAR27\_G3 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR27_G3_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR27_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR27_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4771. CONTROLSS\_PWMXBAR27\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                       |
|-------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                          |
| 19:0  | PWMXBAR27_G3_SEL | R/W  | 0h    | PWM XBAR27 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |



### 3.20.2.252 CONTROLSS\_PWMXBAR27\_G4 Register

#### 1 CONTROLSS\_PWMXBAR27\_G4 Register (Offset = 7D0h) [reset = 0h]

PWM XBAR 27 Input Select.

Return to [Summary Table](#)

**Table 3-4772. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 17D0h       |

**Figure 3-1566. CONTROLSS\_PWMXBAR27\_G4 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR27_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR27_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR27_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR27_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4774. CONTROLSS\_PWMXBAR27\_G4 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR27_G4_SEL | R/W  | 0h    | PWM XBAR27 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.253 CONTROLSS\_PWMXBAR27\_G5 Register

#### 1 CONTROLSS\_PWMXBAR27\_G5 Register (Offset = 7D4h) [reset = 0h]

PWM XBAR 27 Input Select.

Return to [Summary Table](#)

**Table 3-4775. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 17D4h       |

**Figure 3-1567. CONTROLSS\_PWMXBAR27\_G5 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR27_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR27_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR27_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR27_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4777. CONTROLSS\_PWMXBAR27\_G5 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR27_G5_SEL | R/W  | 0h    | PWM XBAR27 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |

### 3.20.2.254 CONTROLSS\_PWMXBAR27\_G6 Register

#### 1 CONTROLSS\_PWMXBAR27\_G6 Register (Offset = 7D8h) [reset = 0h]

PWM XBAR 27 Input Select.

Return to [Summary Table](#)

**Table 3-4778. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 17D8h       |

**Figure 3-1568. CONTROLSS\_PWMXBAR27\_G6 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR27_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR27_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR27_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR27_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4780. CONTROLSS\_PWMXBAR27\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR27_G6_SEL | R/W  | 0h    | PWM XBAR27 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.255 CONTROLSS\_PWMXBAR27\_G7 Register

#### 1 CONTROLSS\_PWMXBAR27\_G7 Register (Offset = 7DCh) [reset = 0h]

PWM XBAR 27 Input Select.

Return to [Summary Table](#)

**Table 3-4781. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 17DCh       |

**Figure 3-1569. CONTROLSS\_PWMXBAR27\_G7 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR27_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR27_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR27_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR27_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4783. CONTROLSS\_PWMXBAR27\_G7 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                  |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR27_G7_SEL | R/W  | 0h    | PWM XBAR27 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |

### 3.20.2.256 CONTROLSS\_PWMXBAR27\_G8 Register

#### 1 CONTROLSS\_PWMXBAR27\_G8 Register (Offset = 7E0h) [reset = 0h]

PWM XBAR 27 Input Select.

Return to [Summary Table](#)

**Table 3-4784. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 17E0h       |

**Figure 3-1570. CONTROLSS\_PWMXBAR27\_G8 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    | PWMXBAR27_G8_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| PWMXBAR27_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR27_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR27_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4786. CONTROLSS\_PWMXBAR27\_G8 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                        |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                           |
| 28:0  | PWMXBAR27_G8_SEL | R/W  | 0h    | PWM XBAR27 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.257 CONTROLSS\_PWMXBAR28\_G0 Register

#### 1 CONTROLSS\_PWMXBAR28\_G0 Register (Offset = 800h) [reset = 0h]

PWM XBAR 28 Input Select.

Return to [Summary Table](#)

**Table 3-4787. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1800h       |

**Figure 3-1571. CONTROLSS\_PWMXBAR28\_G0 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR28_G0_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR28_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR28_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4789. CONTROLSS\_PWMXBAR28\_G0 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR28_G0_SEL | R/W  | 0h    | PWM XBAR28 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |

### 3.20.2.258 CONTROLSS\_PWMXBAR28\_G1 Register

#### 1 CONTROLSS\_PWMXBAR28\_G1 Register (Offset = 804h) [reset = 0h]

PWM XBAR 28 Input Select.

Return to [Summary Table](#)

**Table 3-4790. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1804h       |

**Figure 3-1572. CONTROLSS\_PWMXBAR28\_G1 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR28_G1_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR28_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR28_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4792. CONTROLSS\_PWMXBAR28\_G1 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR28_G1_SEL | R/W  | 0h    | PWM XBAR28 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.259 CONTROLSS\_PWMXBAR28\_G2 Register

#### 1 CONTROLSS\_PWMXBAR28\_G2 Register (Offset = 808h) [reset = 0h]

PWM XBAR 28 Input Select.

Return to [Summary Table](#)

**Table 3-4793. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1808h       |

**Figure 3-1573. CONTROLSS\_PWMXBAR28\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR28_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR28_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR28_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4795. CONTROLSS\_PWMXBAR28\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |



**Table 3-4795. CONTROLSS\_PWMXBAR28\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR28_G2_SEL | R/W  | 0h    | PWM XBAR28 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.260 CONTROLSS\_PWMXBAR28\_G3 Register

#### 1 CONTROLSS\_PWMXBAR28\_G3 Register (Offset = 80Ch) [reset = 0h]

PWM XBAR 28 Input Select.

Return to [Summary Table](#)

**Table 3-4796. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 180Ch       |

**Figure 3-1574. CONTROLSS\_PWMXBAR28\_G3 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR28_G3_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR28_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR28_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4798. CONTROLSS\_PWMXBAR28\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                       |
|-------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                          |
| 19:0  | PWMXBAR28_G3_SEL | R/W  | 0h    | PWM XBAR28 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.20.2.261 CONTROLSS\_PWMXBAR28\_G4 Register

#### 1 CONTROLSS\_PWMXBAR28\_G4 Register (Offset = 810h) [reset = 0h]

PWM XBAR 28 Input Select.

Return to [Summary Table](#)

**Table 3-4799. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1810h       |

**Figure 3-1575. CONTROLSS\_PWMXBAR28\_G4 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR28_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR28_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR28_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR28_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4801. CONTROLSS\_PWMXBAR28\_G4 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR28_G4_SEL | R/W  | 0h    | PWM XBAR28 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.262 CONTROLSS\_PWMXBAR28\_G5 Register

#### 1 CONTROLSS\_PWMXBAR28\_G5 Register (Offset = 814h) [reset = 0h]

PWM XBAR 28 Input Select.

Return to [Summary Table](#)

**Table 3-4802. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1814h       |

**Figure 3-1576. CONTROLSS\_PWMXBAR28\_G5 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR28_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR28_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR28_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR28_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4804. CONTROLSS\_PWMXBAR28\_G5 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR28_G5_SEL | R/W  | 0h    | PWM XBAR28 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |

### 3.20.2.263 CONTROLSS\_PWMXBAR28\_G6 Register

#### 1 CONTROLSS\_PWMXBAR28\_G6 Register (Offset = 818h) [reset = 0h]

PWM XBAR 28 Input Select.

Return to [Summary Table](#)

**Table 3-4805. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1818h       |

**Figure 3-1577. CONTROLSS\_PWMXBAR28\_G6 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR28_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR28_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR28_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR28_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4807. CONTROLSS\_PWMXBAR28\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR28_G6_SEL | R/W  | 0h    | PWM XBAR28 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.264 CONTROLSS\_PWMXBAR28\_G7 Register

#### 1 CONTROLSS\_PWMXBAR28\_G7 Register (Offset = 81Ch) [reset = 0h]

PWM XBAR 28 Input Select.

Return to [Summary Table](#)

**Table 3-4808. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 181Ch       |

**Figure 3-1578. CONTROLSS\_PWMXBAR28\_G7 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR28_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR28_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR28_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR28_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4810. CONTROLSS\_PWMXBAR28\_G7 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                  |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR28_G7_SEL | R/W  | 0h    | PWM XBAR28 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |

### 3.20.2.265 CONTROLSS\_PWMXBAR28\_G8 Register

#### 1 CONTROLSS\_PWMXBAR28\_G8 Register (Offset = 820h) [reset = 0h]

PWM XBAR 28 Input Select.

Return to [Summary Table](#)

**Table 3-4811. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1820h       |

**Figure 3-1579. CONTROLSS\_PWMXBAR28\_G8 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    | PWMXBAR28_G8_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| PWMXBAR28_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR28_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR28_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4813. CONTROLSS\_PWMXBAR28\_G8 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                        |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                           |
| 28:0  | PWMXBAR28_G8_SEL | R/W  | 0h    | PWM XBAR28 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

### 3.20.2.266 CONTROLSS\_PWMXBAR29\_G0 Register

#### 1 CONTROLSS\_PWMXBAR29\_G0 Register (Offset = 840h) [reset = 0h]

PWM XBAR 29 Input Select.

Return to [Summary Table](#)

**Table 3-4814. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1840h       |

**Figure 3-1580. CONTROLSS\_PWMXBAR29\_G0 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR29_G0_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR29_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR29_G0_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4816. CONTROLSS\_PWMXBAR29\_G0 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR29_G0_SEL | R/W  | 0h    | PWM XBAR29 G0 Input Select<br>0: CMPSSA0.CTRIPL<br>1: CMPSSA0.CTRIPH<br>2: CMPSSA1.CTRIPL<br>3: CMPSSA1.CTRIPH<br>4: CMPSSA2.CTRIPL<br>5: CMPSSA2.CTRIPH<br>6: CMPSSA3.CTRIPL<br>7: CMPSSA3.CTRIPH<br>8: CMPSSA4.CTRIPL<br>9: CMPSSA4.CTRIPH<br>10: CMPSSA5.CTRIPL<br>11: CMPSSA5.CTRIPH<br>12: CMPSSA6.CTRIPL<br>13: CMPSSA6.CTRIPH<br>14: CMPSSA7.CTRIPL<br>15: CMPSSA7.CTRIPH<br>16: CMPSSA8.CTRIPL<br>17: CMPSSA8.CTRIPH<br>18: CMPSSA9.CTRIPL<br>19: CMPSSA9.CTRIPH |



### 3.20.2.267 CONTROLSS\_PWMXBAR29\_G1 Register

#### 1 CONTROLSS\_PWMXBAR29\_G1 Register (Offset = 844h) [reset = 0h]

PWM XBAR 29 Input Select.

Return to [Summary Table](#)

**Table 3-4817. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1844h       |

**Figure 3-1581. CONTROLSS\_PWMXBAR29\_G1 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR29_G1_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR29_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR29_G1_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4819. CONTROLSS\_PWMXBAR29\_G1 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 19:0  | PWMXBAR29_G1_SEL | R/W  | 0h    | PWM XBAR29 G1 Input Select<br>0: CMPSSB0.CTRIPL<br>1: CMPSSB0.CTRIPH<br>2: CMPSSB1.CTRIPL<br>3: CMPSSB1.CTRIPH<br>4: CMPSSB2.CTRIPL<br>5: CMPSSB2.CTRIPH<br>6: CMPSSB3.CTRIPL<br>7: CMPSSB3.CTRIPH<br>8: CMPSSB4.CTRIPL<br>9: CMPSSB4.CTRIPH<br>10: CMPSSB5.CTRIPL<br>11: CMPSSB5.CTRIPH<br>12: CMPSSB6.CTRIPL<br>13: CMPSSB6.CTRIPH<br>14: CMPSSB7.CTRIPL<br>15: CMPSSB7.CTRIPH<br>16: CMPSSB8.CTRIPL<br>17: CMPSSB8.CTRIPH<br>18: CMPSSB9.CTRIPL<br>19: CMPSSB9.CTRIPH |

### 3.20.2.268 CONTROLSS\_PWMXBAR29\_G2 Register

#### 1 CONTROLSS\_PWMXBAR29\_G2 Register (Offset = 848h) [reset = 0h]

PWM XBAR 29 Input Select.

Return to [Summary Table](#)

**Table 3-4820. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1848h       |

**Figure 3-1582. CONTROLSS\_PWMXBAR29\_G2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |    |    |    |    |    |    |
| NONE             |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR29_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR29_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR29_G2_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4822. CONTROLSS\_PWMXBAR29\_G2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved    |

**Table 3-4822. CONTROLSS\_PWMXBAR29\_G2 Register Field Descriptions (continued)**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:0 | PWMXBAR29_G2_SEL | R/W  | 0h    | PWM XBAR29 G2 Input Select<br>0:SDFM0.FILT1CEVT1<br>1:SDFM0.FILT1CEVT2<br>2:SDFM0.FILT1COMPHZ<br>3:SDFM0.FILT2CEVT1<br>4:SDFM0.FILT2CEVT2<br>5:SDFM0.FILT2COMPHZ<br>6:SDFM0.FILT3CEVT1<br>7:SDFM0.FILT3CEVT2<br>8:SDFM0.FILT3COMPHZ<br>9:SDFM0.FILT4CEVT1<br>10:SDFM0.FILT4CEVT2<br>11:SDFM0.FILT4COMPHZ<br>12:SDFM1.FILT1CEVT1<br>13:SDFM1.FILT1CEVT2<br>14:SDFM1.FILT1COMPHZ<br>15:SDFM1.FILT2CEVT1<br>16:SDFM1.FILT2CEVT2<br>17:SDFM1.FILT2COMPHZ<br>18:SDFM1.FILT3CEVT1<br>19:SDFM1.FILT3CEVT2<br>20:SDFM1.FILT3COMPHZ<br>21:SDFM1.FILT4CEVT1<br>22:SDFM1.FILT4CEVT2<br>23:SDFM1.FILT4COMPHZ |

### 3.20.2.269 CONTROLSS\_PWMXBAR29\_G3 Register

#### 1 CONTROLSS\_PWMXBAR29\_G3 Register (Offset = 84Ch) [reset = 0h]

PWM XBAR 29 Input Select.

Return to [Summary Table](#)

**Table 3-4823. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 184Ch       |

**Figure 3-1583. CONTROLSS\_PWMXBAR29\_G3 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    | PWMXBAR29_G3_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR29_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR29_G3_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4825. CONTROLSS\_PWMXBAR29\_G3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                       |
|-------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                          |
| 19:0  | PWMXBAR29_G3_SEL | R/W  | 0h    | PWM XBAR29 G3 Input Select<br>1:ADC0.EVT2<br>2:ADC0.EVT3<br>3:ADC0.EVT4<br>4:ADC1.EVT1<br>5:ADC1.EVT2<br>6:ADC1.EVT3<br>7:ADC1.EVT4<br>8:ADC2.EVT1<br>9:ADC2.EVT2<br>10:ADC2.EVT3<br>11:ADC2.EVT4<br>12:ADC3.EVT1<br>13:ADC3.EVT2<br>14:ADC3.EVT3<br>15:ADC3.EVT4<br>16:ADC4.EVT1<br>17:ADC4.EVT2<br>18:ADC4.EVT3<br>19:ADC4.EVT4 |

### 3.20.2.270 CONTROLSS\_PWMXBAR29\_G4 Register

#### 1 CONTROLSS\_PWMXBAR29\_G4 Register (Offset = 850h) [reset = 0h]

PWM XBAR 29 Input Select.

Return to [Summary Table](#)

**Table 3-4826. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1850h       |

**Figure 3-1584. CONTROLSS\_PWMXBAR29\_G4 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR29_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR29_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR29_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR29_G4_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4828. CONTROLSS\_PWMXBAR29\_G4 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                     |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR29_G4_SEL | R/W  | 0h    | PWM XBAR29 G4 input bit select. Input source is INPUT XBAR.<br>1:INPUT XBAR output bit[x] selected<br>0:INPUT XBAR output bit[x] is de-selected |

### 3.20.2.271 CONTROLSS\_PWMXBAR29\_G5 Register

#### 1 CONTROLSS\_PWMXBAR29\_G5 Register (Offset = 854h) [reset = 0h]

PWM XBAR 29 Input Select.

Return to [Summary Table](#)

**Table 3-4829. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1854h       |

**Figure 3-1585. CONTROLSS\_PWMXBAR29\_G5 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR29_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR29_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR29_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR29_G5_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4831. CONTROLSS\_PWMXBAR29\_G5 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                          |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR29_G5_SEL | R/W  | 0h    | PWM XBAR29 G5 input bit select. Input source is PWM TRIPOUT.<br>1:PWM TRIPOUT bit[x] selected<br>0:PWM TRIPOUT bit[x] is de-selected |

### 3.20.2.272 CONTROLSS\_PWMXBAR29\_G6 Register

#### 1 CONTROLSS\_PWMXBAR29\_G6 Register (Offset = 858h) [reset = 0h]

PWM XBAR 29 Input Select.

Return to [Summary Table](#)

**Table 3-4832. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1858h       |

**Figure 3-1586. CONTROLSS\_PWMXBAR29\_G6 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR29_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR29_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR29_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR29_G6_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4834. CONTROLSS\_PWMXBAR29\_G6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                            |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR29_G6_SEL | R/W  | 0h    | PWM XBAR29 G6 input bit select. Input source is PWM DEL TRIP<br>1:PWM DEL TRIP bit[x] selected<br>0:PWM DEL TRIP bit[x] is de-selected |

### 3.20.2.273 CONTROLSS\_PWMXBAR29\_G7 Register

#### 1 CONTROLSS\_PWMXBAR29\_G7 Register (Offset = 85Ch) [reset = 0h]

PWM XBAR 29 Input Select.

Return to [Summary Table](#)

**Table 3-4835. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 185Ch       |

**Figure 3-1587. CONTROLSS\_PWMXBAR29\_G7 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PWMXBAR29_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PWMXBAR29_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWMXBAR29_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWMXBAR29_G7_SEL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 3-4837. CONTROLSS\_PWMXBAR29\_G7 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                  |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PWMXBAR29_G7_SEL | R/W  | 0h    | PWM XBAR29 G7 input bit select. Input source is PWM DEL ACTIVE<br>1:PWM DEL ACTIVE bit[x] selected<br>0:PWM DEL ACTIVE bit[x] is de-selected |



### 3.20.2.274 CONTROLSS\_PWMXBAR29\_G8 Register

#### 1 CONTROLSS\_PWMXBAR29\_G8 Register (Offset = 860h) [reset = 0h]

PWM XBAR 29 Input Select.

Return to [Summary Table](#)

**Table 3-4838. Instance Table**

| Instance Name     | Physical Address |
|-------------------|------------------|
| CONTROLSS_PWMXBAR | 502D 1860h       |

**Figure 3-1588. CONTROLSS\_PWMXBAR29\_G8 Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    | PWMXBAR29_G8_SEL |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| PWMXBAR29_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| PWMXBAR29_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| PWMXBAR29_G8_SEL |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 3-4840. CONTROLSS\_PWMXBAR29\_G8 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                        |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                           |
| 28:0  | PWMXBAR29_G8_SEL | R/W  | 0h    | PWM XBAR29 G8 Input Select<br>0:EQEP0.ERR<br>1:EQEP1.ERR<br>2:EQEP2.ERR<br>6<br>3:FSIRX0.RX_TRIG4<br>10<br>7:FSIRX1.RX_TRIG4<br>14<br>11:FSIRX2.RX_TRIG4<br>18<br>15:FSIRX3.RX_TRIG4<br>28<br>19:ECAP[9:0].TRIPOUT |

## 3.21 SoC\_TIMESYNC\_XBAR0

### SoC\_TIMESYNC\_XBAR0

#### 3.21.1 SoC\_TIMESYNC\_XBAR0 Summaries

#### SoC\_TIMESYNC\_XBAR0 Summaries

**Table 3-4841. SOC\_TIMESYNC\_XBAR0\_INTR\_ROUTER\_CFG Registers, Base Address=52E0 0000h, Length=1024**

| Offset | Length | Register Name                                                                    | SOC_TIMESYNC_XBAR0 Physical Address |
|--------|--------|----------------------------------------------------------------------------------|-------------------------------------|
| 0h     | 32     | <a href="#">SOC_TIMESYNC_XBAR0_INTR_ROUTER_CFG_PID</a>                           | 52E0 0000h                          |
| 4h     | 32     | <a href="#">SOC_TIMESYNC_XBAR0_INTR_ROUTER_CFG_MUXCN</a><br><a href="#">TL_J</a> | 52E0 0004h + formula                |

#### 3.21.2 SoC\_TIMESYNC\_XBAR0 Registers

#### SoC\_TIMESYNC\_XBAR0 Registers

### 3.21.2.1 SOC\_TIMESYNC\_XBAR0\_INTR\_ROUTER\_CFG\_PID Register

#### 1 SOC\_TIMESYNC\_XBAR0\_INTR\_ROUTER\_CFG\_PID Register (Offset = 0h) [reset = 66948100h]

Identification register.

Return to [Summary Table](#)

**Table 3-4842. Instance Table**

| Instance Name      | Physical Address |
|--------------------|------------------|
| SOC_TIMESYNC_XBAR0 | 52E0 0000h       |

**Figure 3-1589. SOC\_TIMESYNC\_XBAR0\_INTR\_ROUTER\_CFG\_PID Name Register**

|          |    |        |    |          |        |    |    |
|----------|----|--------|----|----------|--------|----|----|
| 31       | 30 | 29     | 28 | 27       | 26     | 25 | 24 |
| SCHEME   |    | BU     |    | FUNCTION |        |    |    |
| R        |    | R      |    | R        |        |    |    |
| 1h       |    | 2h     |    | 694h     |        |    |    |
| 23       | 22 | 21     | 20 | 19       | 18     | 17 | 16 |
| FUNCTION |    |        |    |          |        |    |    |
| R        |    |        |    |          |        |    |    |
| 694h     |    |        |    |          |        |    |    |
| 15       | 14 | 13     | 12 | 11       | 10     | 9  | 8  |
| RTLVER   |    |        |    |          | MAJREV |    |    |
| R        |    |        |    |          | R      |    |    |
| 10h      |    |        |    |          | 1h     |    |    |
| 7        | 6  | 5      | 4  | 3        | 2      | 1  | 0  |
| CUSTOM   |    | MINREV |    |          |        |    |    |
| R        |    | R      |    |          |        |    |    |
| 0h       |    | 0h     |    |          |        |    |    |

**Table 3-4844. SOC\_TIMESYNC\_XBAR0\_INTR\_ROUTER\_CFG\_PID Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description   |
|-------|----------|------|-------|---------------|
| 31:30 | SCHEME   | R    | 1h    | Scheme        |
| 29:28 | BU       | R    | 2h    | bu            |
| 27:16 | FUNCTION | R    | 694h  | function      |
| 15:11 | RTLVER   | R    | 10h   | Rtl version   |
| 10:8  | MAJREV   | R    | 1h    | major version |
| 7:6   | CUSTOM   | R    | 0h    | custom id     |
| 5:0   | MINREV   | R    | 0h    | minor version |

### 3.21.2.2 SOC\_TIMESYNC\_XBAR0\_INTR\_ROUTER\_CFG\_MUXCNTL\_j Register

**1 SOC\_TIMESYNC\_XBAR0\_INTR\_ROUTER\_CFG\_MUXCNTL\_j Register (Offset = 4h + formula) [reset = 0h]**

Interrupt mux control register.

Return to [Summary Table](#)

Offset = (j \* 4h); where j = 0 to 19d

**Table 3-4845. Instance Table**

| Instance Name      | Physical Address     |
|--------------------|----------------------|
| SOC_TIMESYNC_XBAR0 | 52E0 0004h + formula |

**Figure 3-1590. SOC\_TIMESYNC\_XBAR0\_INTR\_ROUTER\_CFG\_MUXCNTL\_j Name Register**

|          |    |    |    |          |    |    |            |
|----------|----|----|----|----------|----|----|------------|
| 31       | 30 | 29 | 28 | 27       | 26 | 25 | 24         |
| RESERVED |    |    |    |          |    |    |            |
| NONE     |    |    |    |          |    |    |            |
| 0h       |    |    |    |          |    |    |            |
| 23       | 22 | 21 | 20 | 19       | 18 | 17 | 16         |
| RESERVED |    |    |    |          |    |    | INT_ENABLE |
| NONE     |    |    |    |          |    |    | R/W        |
| 0h       |    |    |    |          |    |    | 0h         |
| 15       | 14 | 13 | 12 | 11       | 10 | 9  | 8          |
| RESERVED |    |    |    |          |    |    |            |
| NONE     |    |    |    |          |    |    |            |
| 0h       |    |    |    |          |    |    |            |
| 7        | 6  | 5  | 4  | 3        | 2  | 1  | 0          |
| RESERVED |    |    |    | MUX_CNTL |    |    |            |
| NONE     |    |    |    | R/W      |    |    |            |
| 0h       |    |    |    | 0h       |    |    |            |

**Table 3-4847. SOC\_TIMESYNC\_XBAR0\_INTR\_ROUTER\_CFG\_MUXCNTL\_j Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                           |
|-------|------------|------|-------|-------------------------------------------------------|
| 31:17 | RESERVED   | NONE | 0h    | Reserved                                              |
| 16    | INT_ENABLE | R/W  | 0h    | Interrupt j Output Enable.<br>0 Disabled<br>1 Enabled |
| 15:5  | RESERVED   | NONE | 0h    | Reserved                                              |
| 4:0   | MUX_CNTL   | R/W  | 0h    | Mux Control for Interrupt j.                          |

## 3.22 SoC\_TIMESYNC\_XBAR1

### SoC\_TIMESYNC\_XBAR1

#### 3.22.1 SoC\_TIMESYNC\_XBAR1 Summaries

#### SoC\_TIMESYNC\_XBAR1 Summaries

**Table 3-4848. SOC\_TIMESYNC\_XBAR1\_INTR\_ROUTER\_CFG Registers, Base Address=52E0 4000h, Length=2048**

| Offset | Length | Register Name                                                     | SOC_TIMESYNC_XBAR1 Physical Address |
|--------|--------|-------------------------------------------------------------------|-------------------------------------|
| 0h     | 32     | <a href="#">SOC_TIMESYNC_XBAR1_INTR_ROUTER_CFG_PID</a>            | 52E0 4000h                          |
| 4h     | 32     | <a href="#">SOC_TIMESYNC_XBAR1_INTR_ROUTER_CFG_MUXCN<br/>TL_J</a> | 52E0 4004h + formula                |

#### 3.22.2 SoC\_TIMESYNC\_XBAR1 Registers

#### SoC\_TIMESYNC\_XBAR1 Registers

### 3.22.2.1 SOC\_TIMESYNC\_XBAR1\_INTR\_ROUTER\_CFG\_PID Register

#### 1 SOC\_TIMESYNC\_XBAR1\_INTR\_ROUTER\_CFG\_PID Register (Offset = 0h) [reset = 66948100h]

Identification register.

Return to [Summary Table](#)

**Table 3-4849. Instance Table**

| Instance Name      | Physical Address |
|--------------------|------------------|
| SOC_TIMESYNC_XBAR1 | 52E0 4000h       |

**Figure 3-1591. SOC\_TIMESYNC\_XBAR1\_INTR\_ROUTER\_CFG\_PID Name Register**

|          |    |        |    |          |        |    |    |
|----------|----|--------|----|----------|--------|----|----|
| 31       | 30 | 29     | 28 | 27       | 26     | 25 | 24 |
| SCHEME   |    | BU     |    | FUNCTION |        |    |    |
| R        |    | R      |    | R        |        |    |    |
| 1h       |    | 2h     |    | 694h     |        |    |    |
| 23       | 22 | 21     | 20 | 19       | 18     | 17 | 16 |
| FUNCTION |    |        |    |          |        |    |    |
| R        |    |        |    |          |        |    |    |
| 694h     |    |        |    |          |        |    |    |
| 15       | 14 | 13     | 12 | 11       | 10     | 9  | 8  |
| RTLVER   |    |        |    |          | MAJREV |    |    |
| R        |    |        |    |          | R      |    |    |
| 10h      |    |        |    |          | 1h     |    |    |
| 7        | 6  | 5      | 4  | 3        | 2      | 1  | 0  |
| CUSTOM   |    | MINREV |    |          |        |    |    |
| R        |    | R      |    |          |        |    |    |
| 0h       |    | 0h     |    |          |        |    |    |

**Table 3-4851. SOC\_TIMESYNC\_XBAR1\_INTR\_ROUTER\_CFG\_PID Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description   |
|-------|----------|------|-------|---------------|
| 31:30 | SCHEME   | R    | 1h    | Scheme        |
| 29:28 | BU       | R    | 2h    | bu            |
| 27:16 | FUNCTION | R    | 694h  | function      |
| 15:11 | RTLVER   | R    | 10h   | Rtl version   |
| 10:8  | MAJREV   | R    | 1h    | major version |
| 7:6   | CUSTOM   | R    | 0h    | custom id     |
| 5:0   | MINREV   | R    | 0h    | minor version |

### 3.22.2.2 SOC\_TIMESYNC\_XBAR1\_INTR\_ROUTER\_CFG\_MUXCNTL\_j Register

**1 SOC\_TIMESYNC\_XBAR1\_INTR\_ROUTER\_CFG\_MUXCNTL\_j Register (Offset = 4h + formula) [reset = 0h]**

Interrupt mux control register.

Return to [Summary Table](#)

Offset = (j \* 4h); where j = 0 to 33d

**Table 3-4852. Instance Table**

| Instance Name      | Physical Address     |
|--------------------|----------------------|
| SOC_TIMESYNC_XBAR1 | 52E0 4004h + formula |

**Figure 3-1592. SOC\_TIMESYNC\_XBAR1\_INTR\_ROUTER\_CFG\_MUXCNTL\_j Name Register**

|          |    |    |    |          |    |    |            |
|----------|----|----|----|----------|----|----|------------|
| 31       | 30 | 29 | 28 | 27       | 26 | 25 | 24         |
| RESERVED |    |    |    |          |    |    |            |
| NONE     |    |    |    |          |    |    |            |
| 0h       |    |    |    |          |    |    |            |
| 23       | 22 | 21 | 20 | 19       | 18 | 17 | 16         |
| RESERVED |    |    |    |          |    |    | INT_ENABLE |
| NONE     |    |    |    |          |    |    | R/W        |
| 0h       |    |    |    |          |    |    | 0h         |
| 15       | 14 | 13 | 12 | 11       | 10 | 9  | 8          |
| RESERVED |    |    |    |          |    |    |            |
| NONE     |    |    |    |          |    |    |            |
| 0h       |    |    |    |          |    |    |            |
| 7        | 6  | 5  | 4  | 3        | 2  | 1  | 0          |
| RESERVED |    |    |    | MUX_CNTL |    |    |            |
| NONE     |    |    |    | R/W      |    |    |            |
| 0h       |    |    |    | 0h       |    |    |            |

**Table 3-4854. SOC\_TIMESYNC\_XBAR1\_INTR\_ROUTER\_CFG\_MUXCNTL\_j Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                           |
|-------|------------|------|-------|-------------------------------------------------------|
| 31:17 | RESERVED   | NONE | 0h    | Reserved                                              |
| 16    | INT_ENABLE | R/W  | 0h    | Interrupt j Output Enable.<br>0 Disabled<br>1 Enabled |
| 15:4  | RESERVED   | NONE | 0h    | Reserved                                              |
| 3:0   | MUX_CNTL   | R/W  | 0h    | Mux Control for Interrupt j.                          |

## Chapter 4

# ***Processor and Accelerator Registers***

---



The Processor and Accelerator module registers are described in the following sections.



## 4.1 R5SS

### R5SS

#### 4.1.1 R5SS Summaries

#### R5SS Summaries

**Table 4-1. TCMA\_CORE0\_ROM Registers, Base Address=0000 0000h, Length=131072**

| Offset  | Length | Register Name                        | R5SS0 Physical Address |
|---------|--------|--------------------------------------|------------------------|
| 0h      | 32     | <a href="#">TCMA_CORE0_ROM_START</a> | 0000 0000h             |
| 1FFFCCh | 32     | <a href="#">TCMA_CORE0_ROM_END</a>   | 0001 FFFCh             |

**Table 4-2. TCMA\_CORE1\_RAM Registers, Base Address=0000 0000h, Length=32768**

| Offset | Length | Register Name                        | R5SS0 Physical Address | R5SS1 Physical Address |
|--------|--------|--------------------------------------|------------------------|------------------------|
| 0h     | 32     | <a href="#">TCMA_CORE1_RAM_START</a> | 0000 0000h             | 0000 0000h             |
| 7FFCh  | 32     | <a href="#">TCMA_CORE1_RAM_END</a>   | 0000 7FFCh             | 0000 7FFCh             |

**Table 4-3. TCMA\_CORE0\_RAM Registers, Base Address=0002 0000h, Length=32768**

| Offset | Length | Register Name                        | R5SS0 Physical Address | R5SS1 Physical Address |
|--------|--------|--------------------------------------|------------------------|------------------------|
| 0h     | 32     | <a href="#">TCMA_CORE0_RAM_START</a> | 0002 0000h             | 0000 0000h             |
| 7FFCh  | 32     | <a href="#">TCMA_CORE0_RAM_END</a>   | 0002 7FFCh             | 0000 7FFCh             |

**Table 4-4. TCMB\_CORE0\_RAM Registers, Base Address=0008 0000h, Length=32768**

| Offset | Length | Register Name                        | R5SS0 Physical Address | R5SS1 Physical Address |
|--------|--------|--------------------------------------|------------------------|------------------------|
| 0h     | 32     | <a href="#">TCMB_CORE0_RAM_START</a> | 0008 0000h             | 0008 0000h             |
| 17FFCh | 32     | <a href="#">TCMB_CORE0_RAM_END</a>   | 0009 7FFCh             | 0009 7FFCh             |

**Table 4-5. TCMB\_CORE1\_RAM Registers, Base Address=0008 0000h, Length=32768**

| Offset | Length | Register Name                        | R5SS0 Physical Address | R5SS1 Physical Address |
|--------|--------|--------------------------------------|------------------------|------------------------|
| 0h     | 32     | <a href="#">TCMB_CORE1_RAM_START</a> | 0008 0000h             | 0008 0000h             |
| 17FFCh | 32     | <a href="#">TCMB_CORE1_RAM_END</a>   | 0009 7FFCh             | 0009 7FFCh             |

**Table 4-6. VIM0 Registers, Base Address=50F0 0000h, Length=16384**

| Offset | Length | Register Name                | R5SS0 Physical Address | R5SS1 Physical Address |
|--------|--------|------------------------------|------------------------|------------------------|
| 0h     | 32     | <a href="#">VIM0_PID</a>     | 50F0 0000h             | 50F0 0000h             |
| 4h     | 32     | <a href="#">VIM0_INFO</a>    | 50F0 0004h             | 50F0 0004h             |
| 8h     | 32     | <a href="#">VIM0_PRIIRQ</a>  | 50F0 0008h             | 50F0 0008h             |
| Ch     | 32     | <a href="#">VIM0_PRIFIQ</a>  | 50F0 000Ch             | 50F0 000Ch             |
| 10h    | 32     | <a href="#">VIM0_IRQGSTS</a> | 50F0 0010h             | 50F0 0010h             |
| 14h    | 32     | <a href="#">VIM0_FIQGSTS</a> | 50F0 0014h             | 50F0 0014h             |
| 18h    | 32     | <a href="#">VIM0_IRQVEC</a>  | 50F0 0018h             | 50F0 0018h             |
| 1Ch    | 32     | <a href="#">VIM0_FIQVEC</a>  | 50F0 001Ch             | 50F0 001Ch             |
| 20h    | 32     | <a href="#">VIM0_ACTIRQ</a>  | 50F0 0020h             | 50F0 0020h             |
| 24h    | 32     | <a href="#">VIM0_ACTFIQ</a>  | 50F0 0024h             | 50F0 0024h             |

**Table 4-6. VIM0 Registers, Base Address=50F0 0000h, Length=16384 (continued)**

| Offset | Length | Register Name                       | R5SS0 Physical Address | R5SS1 Physical Address |
|--------|--------|-------------------------------------|------------------------|------------------------|
| 28h    | 32     | <a href="#">VIM0_IRQPRIMSK</a>      | 50F0 0028h             | 50F0 0028h             |
| 2Ch    | 32     | <a href="#">VIM0_FIQPRIMSK</a>      | 50F0 002Ch             | 50F0 002Ch             |
| 30h    | 32     | <a href="#">VIM0_DEDVEC</a>         | 50F0 0030h             | 50F0 0030h             |
| 400h   | 32     | <a href="#">VIM0_RAW_M</a>          | 50F0 0400h             | 50F0 0400h             |
| 404h   | 32     | <a href="#">VIM0_STS_M</a>          | 50F0 0404h             | 50F0 0404h             |
| 408h   | 32     | <a href="#">VIM0_INTR_EN_SET_M</a>  | 50F0 0408h             | 50F0 0408h             |
| 40Ch   | 32     | <a href="#">VIM0_INTER_EN_CLR_M</a> | 50F0 040Ch             | 50F0 040Ch             |
| 410h   | 32     | <a href="#">VIM0_IRQSTS_M</a>       | 50F0 0410h             | 50F0 0410h             |
| 414h   | 32     | <a href="#">VIM0_FIQSTS_M</a>       | 50F0 0414h             | 50F0 0414h             |
| 418h   | 32     | <a href="#">VIM0_INTMAP_M</a>       | 50F0 0418h             | 50F0 0418h             |
| 41Ch   | 32     | <a href="#">VIM0_INTTYPE_M</a>      | 50F0 041Ch             | 50F0 041Ch             |
| 1000h  | 32     | <a href="#">VIM0_INTPRIORITY_Q</a>  | 50F0 1000h             | 50F0 1000h             |
| 2000h  | 32     | <a href="#">VIM0_INTVECTOR_Q</a>    | 50F0 2000h             | 50F0 2000h             |

**Table 4-7. VIM1 Registers, Base Address=50F0 0000h, Length=16384**

| Offset | Length | Register Name                       | R5SS0 Physical Address | R5SS1 Physical Address |
|--------|--------|-------------------------------------|------------------------|------------------------|
| 0h     | 32     | <a href="#">VIM1_PID</a>            | 50F0 0000h             | 50F0 0000h             |
| 4h     | 32     | <a href="#">VIM1_INFO</a>           | 50F0 0004h             | 50F0 0004h             |
| 8h     | 32     | <a href="#">VIM1_PRIIRQ</a>         | 50F0 0008h             | 50F0 0008h             |
| Ch     | 32     | <a href="#">VIM1_PRIFIQ</a>         | 50F0 000Ch             | 50F0 000Ch             |
| 10h    | 32     | <a href="#">VIM1_IRQGSTS</a>        | 50F0 0010h             | 50F0 0010h             |
| 14h    | 32     | <a href="#">VIM1_FIQGSTS</a>        | 50F0 0014h             | 50F0 0014h             |
| 18h    | 32     | <a href="#">VIM1_IRQVEC</a>         | 50F0 0018h             | 50F0 0018h             |
| 1Ch    | 32     | <a href="#">VIM1_FIQVEC</a>         | 50F0 001Ch             | 50F0 001Ch             |
| 20h    | 32     | <a href="#">VIM1_ACTIRQ</a>         | 50F0 0020h             | 50F0 0020h             |
| 24h    | 32     | <a href="#">VIM1_ACTFIQ</a>         | 50F0 0024h             | 50F0 0024h             |
| 28h    | 32     | <a href="#">VIM1_IRQPRIMSK</a>      | 50F0 0028h             | 50F0 0028h             |
| 2Ch    | 32     | <a href="#">VIM1_FIQPRIMSK</a>      | 50F0 002Ch             | 50F0 002Ch             |
| 30h    | 32     | <a href="#">VIM1_DEDVEC</a>         | 50F0 0030h             | 50F0 0030h             |
| 400h   | 32     | <a href="#">VIM1_RAW_M</a>          | 50F0 0400h             | 50F0 0400h             |
| 404h   | 32     | <a href="#">VIM1_STS_M</a>          | 50F0 0404h             | 50F0 0404h             |
| 408h   | 32     | <a href="#">VIM1_INTR_EN_SET_M</a>  | 50F0 0408h             | 50F0 0408h             |
| 40Ch   | 32     | <a href="#">VIM1_INTER_EN_CLR_M</a> | 50F0 040Ch             | 50F0 040Ch             |
| 410h   | 32     | <a href="#">VIM1_IRQSTS_M</a>       | 50F0 0410h             | 50F0 0410h             |
| 414h   | 32     | <a href="#">VIM1_FIQSTS_M</a>       | 50F0 0414h             | 50F0 0414h             |
| 418h   | 32     | <a href="#">VIM1_INTMAP_M</a>       | 50F0 0418h             | 50F0 0418h             |
| 41Ch   | 32     | <a href="#">VIM1_INTTYPE_M</a>      | 50F0 041Ch             | 50F0 041Ch             |
| 1000h  | 32     | <a href="#">VIM1_INTPRIORITY_Q</a>  | 50F0 1000h             | 50F0 1000h             |
| 2000h  | 32     | <a href="#">VIM1_INTVECTOR_Q</a>    | 50F0 2000h             | 50F0 2000h             |

**Table 4-8. ECC\_AGG\_CORE0 Registers, Base Address=5300 0000h, Length=1024**

| Offset | Length | Register Name                               | R5SS0 Physical Address | R5SS1 Physical Address |
|--------|--------|---------------------------------------------|------------------------|------------------------|
| 0h     | 32     | <a href="#">ECC_AGG_CORE0_AGGR_REVISION</a> | 5300 0000h             | 5300 4000h             |
| 8h     | 32     | <a href="#">ECC_AGG_CORE0_ECC_VECTOR</a>    | 5300 0008h             | 5300 4008h             |

**Table 4-8. ECC\_AGG\_CORE0 Registers, Base Address=5300 0000h, Length=1024 (continued)**

| Offset | Length | Register Name                                     | R5SS0 Physical Address | R5SS1 Physical Address |
|--------|--------|---------------------------------------------------|------------------------|------------------------|
| Ch     | 32     | <a href="#">ECC_AGG_CORE0_MISC_STATUS</a>         | 5300 000Ch             | 5300 400Ch             |
| 10h    | 32     | <a href="#">ECC_AGG_CORE0_ECC_WRAP_REVISION</a>   | 5300 0010h             | 5300 4010h             |
| 14h    | 32     | <a href="#">ECC_AGG_CORE0_CONTROL</a>             | 5300 0014h             | 5300 4014h             |
| 18h    | 32     | <a href="#">ECC_AGG_CORE0_ERROR_CTRL1</a>         | 5300 0018h             | 5300 4018h             |
| 1Ch    | 32     | <a href="#">ECC_AGG_CORE0_ERROR_CTRL2</a>         | 5300 001Ch             | 5300 401Ch             |
| 20h    | 32     | <a href="#">ECC_AGG_CORE0_ERROR_STATUS1</a>       | 5300 0020h             | 5300 4020h             |
| 24h    | 32     | <a href="#">ECC_AGG_CORE0_ERROR_STATUS2</a>       | 5300 0024h             | 5300 4024h             |
| 28h    | 32     | <a href="#">ECC_AGG_CORE0_ERROR_STATUS3</a>       | 5300 0028h             | 5300 4028h             |
| 3Ch    | 32     | <a href="#">ECC_AGG_CORE0_SEC_EOI_REG</a>         | 5300 003Ch             | 5300 403Ch             |
| 40h    | 32     | <a href="#">ECC_AGG_CORE0_SEC_STATUS_REG0</a>     | 5300 0040h             | 5300 4040h             |
| 80h    | 32     | <a href="#">ECC_AGG_CORE0_SEC_ENABLE_SET_REG0</a> | 5300 0080h             | 5300 4080h             |
| C0h    | 32     | <a href="#">ECC_AGG_CORE0_SEC_ENABLE_CLR_REG0</a> | 5300 00C0h             | 5300 40C0h             |
| 13Ch   | 32     | <a href="#">ECC_AGG_CORE0_DED_EOI_REG</a>         | 5300 013Ch             | 5300 413Ch             |
| 140h   | 32     | <a href="#">ECC_AGG_CORE0_DED_STATUS_REG0</a>     | 5300 0140h             | 5300 4140h             |
| 180h   | 32     | <a href="#">ECC_AGG_CORE0_DED_ENABLE_SET_REG0</a> | 5300 0180h             | 5300 4180h             |
| 1C0h   | 32     | <a href="#">ECC_AGG_CORE0_DED_ENABLE_CLR_REG0</a> | 5300 01C0h             | 5300 41C0h             |
| 200h   | 32     | <a href="#">ECC_AGG_CORE0_AGGR_ENABLE_SET</a>     | 5300 0200h             | 5300 4200h             |
| 204h   | 32     | <a href="#">ECC_AGG_CORE0_AGGR_ENABLE_CLR</a>     | 5300 0204h             | 5300 4204h             |
| 208h   | 32     | <a href="#">ECC_AGG_CORE0_AGGR_STATUS_SET</a>     | 5300 0208h             | 5300 4208h             |
| 20Ch   | 32     | <a href="#">ECC_AGG_CORE0_AGGR_STATUS_CLR</a>     | 5300 020Ch             | 5300 420Ch             |

**Table 4-9. ECC\_AGG\_CORE1 Registers, Base Address=5300 3000h, Length=1024**

| Offset | Length | Register Name                                     | R5SS0 Physical Address | R5SS1 Physical Address |
|--------|--------|---------------------------------------------------|------------------------|------------------------|
| 0h     | 32     | <a href="#">ECC_AGG_CORE1_AGGR_REVISION</a>       | 5300 3000h             | 5300 7000h             |
| 8h     | 32     | <a href="#">ECC_AGG_CORE1_ECC_VECTOR</a>          | 5300 3008h             | 5300 7008h             |
| Ch     | 32     | <a href="#">ECC_AGG_CORE1_MISC_STATUS</a>         | 5300 300Ch             | 5300 700Ch             |
| 10h    | 32     | <a href="#">ECC_AGG_CORE1_ECC_WRAP_REVISION</a>   | 5300 3010h             | 5300 7010h             |
| 14h    | 32     | <a href="#">ECC_AGG_CORE1_CONTROL</a>             | 5300 3014h             | 5300 7014h             |
| 18h    | 32     | <a href="#">ECC_AGG_CORE1_ERROR_CTRL1</a>         | 5300 3018h             | 5300 7018h             |
| 1Ch    | 32     | <a href="#">ECC_AGG_CORE1_ERROR_CTRL2</a>         | 5300 301Ch             | 5300 701Ch             |
| 20h    | 32     | <a href="#">ECC_AGG_CORE1_ERROR_STATUS1</a>       | 5300 3020h             | 5300 7020h             |
| 24h    | 32     | <a href="#">ECC_AGG_CORE1_ERROR_STATUS2</a>       | 5300 3024h             | 5300 7024h             |
| 28h    | 32     | <a href="#">ECC_AGG_CORE1_ERROR_STATUS3</a>       | 5300 3028h             | 5300 7028h             |
| 3Ch    | 32     | <a href="#">ECC_AGG_CORE1_SEC_EOI_REG</a>         | 5300 303Ch             | 5300 703Ch             |
| 40h    | 32     | <a href="#">ECC_AGG_CORE1_SEC_STATUS_REG0</a>     | 5300 3040h             | 5300 7040h             |
| 80h    | 32     | <a href="#">ECC_AGG_CORE1_SEC_ENABLE_SET_REG0</a> | 5300 3080h             | 5300 7080h             |
| C0h    | 32     | <a href="#">ECC_AGG_CORE1_SEC_ENABLE_CLR_REG0</a> | 5300 30C0h             | 5300 70C0h             |
| 13Ch   | 32     | <a href="#">ECC_AGG_CORE1_DED_EOI_REG</a>         | 5300 313Ch             | 5300 713Ch             |
| 140h   | 32     | <a href="#">ECC_AGG_CORE1_DED_STATUS_REG0</a>     | 5300 3140h             | 5300 7140h             |

**Table 4-9. ECC\_AGG\_CORE1 Registers, Base Address=5300 3000h, Length=1024 (continued)**

| Offset | Length | Register Name                                          | R5SS0 Physical Address | R5SS1 Physical Address |
|--------|--------|--------------------------------------------------------|------------------------|------------------------|
| 180h   | 32     | <a href="#">ECC_AGG_CORE1_DED_ENABLE_SET_R<br/>EG0</a> | 5300 3180h             | 5300 7180h             |
| 1C0h   | 32     | <a href="#">ECC_AGG_CORE1_DED_ENABLE_CLR_R<br/>EG0</a> | 5300 31C0h             | 5300 71C0h             |
| 200h   | 32     | <a href="#">ECC_AGG_CORE1_AGGR_ENABLE_SET</a>          | 5300 3200h             | 5300 7200h             |
| 204h   | 32     | <a href="#">ECC_AGG_CORE1_AGGR_ENABLE_CLR</a>          | 5300 3204h             | 5300 7204h             |
| 208h   | 32     | <a href="#">ECC_AGG_CORE1_AGGR_STATUS_SET</a>          | 5300 3208h             | 5300 7208h             |
| 20Ch   | 32     | <a href="#">ECC_AGG_CORE1_AGGR_STATUS_CLR</a>          | 5300 320Ch             | 5300 720Ch             |

**Table 4-10. CCMR Registers, Base Address=5321 0000h, Length=4096**

| Offset | Length | Register Name                    | R5SS0 Physical Address | R5SS1 Physical Address |
|--------|--------|----------------------------------|------------------------|------------------------|
| 0h     | 32     | <a href="#">CCMR_CCMSR1</a>      | 5321 0000h             | 5321 1000h             |
| 4h     | 32     | <a href="#">CCMR_CCMKEYR1</a>    | 5321 0004h             | 5321 1004h             |
| 8h     | 32     | <a href="#">CCMR_CCMSR2</a>      | 5321 0008h             | 5321 1008h             |
| Ch     | 32     | <a href="#">CCMR_CCMKEYR2</a>    | 5321 000Ch             | 5321 100Ch             |
| 10h    | 32     | <a href="#">CCMR_CCMSR3</a>      | 5321 0010h             | 5321 1010h             |
| 14h    | 32     | <a href="#">CCMR_CCMKEYR3</a>    | 5321 0014h             | 5321 1014h             |
| 18h    | 32     | <a href="#">CCMR_CCMPOLCNTRL</a> | 5321 0018h             | 5321 1018h             |

**Table 4-11. STC Registers, Base Address=5350 0000h, Length=512**

| Offset | Length | Register Name                       | R5SS0 Physical Address | R5SS1 Physical Address |
|--------|--------|-------------------------------------|------------------------|------------------------|
| 0h     | 32     | <a href="#">STC_STCGCR0</a>         | 5350 0000h             | 5351 0000h             |
| 4h     | 32     | <a href="#">STC_STCGCR1</a>         | 5350 0004h             | 5351 0004h             |
| 8h     | 32     | <a href="#">STC_STCTPR</a>          | 5350 0008h             | 5351 0008h             |
| Ch     | 32     | <a href="#">STC_STC_CADDR</a>       | 5350 000Ch             | 5351 000Ch             |
| 10h    | 32     | <a href="#">STC_STCCICR</a>         | 5350 0010h             | 5351 0010h             |
| 14h    | 32     | <a href="#">STC_STCGSTAT</a>        | 5350 0014h             | 5351 0014h             |
| 18h    | 32     | <a href="#">STC_STCFSTAT</a>        | 5350 0018h             | 5351 0018h             |
| 1Ch    | 32     | <a href="#">STC_STCSCSCR</a>        | 5350 001Ch             | 5351 001Ch             |
| 20h    | 32     | <a href="#">STC_STC_CADDR2</a>      | 5350 0020h             | 5351 0020h             |
| 24h    | 32     | <a href="#">STC_STC_CLKDIV</a>      | 5350 0024h             | 5351 0024h             |
| 28h    | 32     | <a href="#">STC_STC_SEGPLR</a>      | 5350 0028h             | 5351 0028h             |
| 2Ch    | 32     | <a href="#">STC_SEG0_START_ADDR</a> | 5350 002Ch             | 5351 002Ch             |
| 30h    | 32     | <a href="#">STC_SEG1_START_ADDR</a> | 5350 0030h             | 5351 0030h             |
| 34h    | 32     | <a href="#">STC_SEG2_START_ADDR</a> | 5350 0034h             | 5351 0034h             |
| 38h    | 32     | <a href="#">STC_SEG3_START_ADDR</a> | 5350 0038h             | 5351 0038h             |
| 3Ch    | 32     | <a href="#">STC_CORE1_CURMISR_0</a> | 5350 003Ch             | 5351 003Ch             |
| 40h    | 32     | <a href="#">STC_CORE1_CURMISR_1</a> | 5350 0040h             | 5351 0040h             |
| 44h    | 32     | <a href="#">STC_CORE1_CURMISR_2</a> | 5350 0044h             | 5351 0044h             |
| 48h    | 32     | <a href="#">STC_CORE1_CURMISR_3</a> | 5350 0048h             | 5351 0048h             |
| 4Ch    | 32     | <a href="#">STC_CORE1_CURMISR_4</a> | 5350 004Ch             | 5351 004Ch             |
| 50h    | 32     | <a href="#">STC_CORE1_CURMISR_5</a> | 5350 0050h             | 5351 0050h             |
| 54h    | 32     | <a href="#">STC_CORE1_CURMISR_6</a> | 5350 0054h             | 5351 0054h             |
| 58h    | 32     | <a href="#">STC_CORE1_CURMISR_7</a> | 5350 0058h             | 5351 0058h             |

**Table 4-11. STC Registers, Base Address=5350 0000h, Length=512 (continued)**

| Offset | Length | Register Name                        | R5SS0 Physical Address | R5SS1 Physical Address |
|--------|--------|--------------------------------------|------------------------|------------------------|
| 5Ch    | 32     | <a href="#">STC_CORE1_CURMISR_8</a>  | 5350 005Ch             | 5351 005Ch             |
| 60h    | 32     | <a href="#">STC_CORE1_CURMISR_9</a>  | 5350 0060h             | 5351 0060h             |
| 64h    | 32     | <a href="#">STC_CORE1_CURMISR_10</a> | 5350 0064h             | 5351 0064h             |
| 68h    | 32     | <a href="#">STC_CORE1_CURMISR_11</a> | 5350 0068h             | 5351 0068h             |
| 6Ch    | 32     | <a href="#">STC_CORE1_CURMISR_12</a> | 5350 006Ch             | 5351 006Ch             |
| 70h    | 32     | <a href="#">STC_CORE1_CURMISR_13</a> | 5350 0070h             | 5351 0070h             |
| 74h    | 32     | <a href="#">STC_CORE1_CURMISR_14</a> | 5350 0074h             | 5351 0074h             |
| 78h    | 32     | <a href="#">STC_CORE1_CURMISR_15</a> | 5350 0078h             | 5351 0078h             |
| 7Ch    | 32     | <a href="#">STC_CORE1_CURMISR_16</a> | 5350 007Ch             | 5351 007Ch             |
| 80h    | 32     | <a href="#">STC_CORE1_CURMISR_17</a> | 5350 0080h             | 5351 0080h             |
| 84h    | 32     | <a href="#">STC_CORE1_CURMISR_18</a> | 5350 0084h             | 5351 0084h             |
| 88h    | 32     | <a href="#">STC_CORE1_CURMISR_19</a> | 5350 0088h             | 5351 0088h             |
| 8Ch    | 32     | <a href="#">STC_CORE1_CURMISR_20</a> | 5350 008Ch             | 5351 008Ch             |
| 90h    | 32     | <a href="#">STC_CORE1_CURMISR_21</a> | 5350 0090h             | 5351 0090h             |
| 94h    | 32     | <a href="#">STC_CORE1_CURMISR_22</a> | 5350 0094h             | 5351 0094h             |
| 98h    | 32     | <a href="#">STC_CORE1_CURMISR_23</a> | 5350 0098h             | 5351 0098h             |
| 9Ch    | 32     | <a href="#">STC_CORE1_CURMISR_24</a> | 5350 009Ch             | 5351 009Ch             |
| A0h    | 32     | <a href="#">STC_CORE1_CURMISR_25</a> | 5350 00A0h             | 5351 00A0h             |
| A4h    | 32     | <a href="#">STC_CORE1_CURMISR_26</a> | 5350 00A4h             | 5351 00A4h             |
| A8h    | 32     | <a href="#">STC_CORE1_CURMISR_27</a> | 5350 00A8h             | 5351 00A8h             |
| ACh    | 32     | <a href="#">STC_CORE2_CURMISR_0</a>  | 5350 00ACh             | 5351 00ACh             |
| B0h    | 32     | <a href="#">STC_CORE2_CURMISR_1</a>  | 5350 00B0h             | 5351 00B0h             |
| B4h    | 32     | <a href="#">STC_CORE2_CURMISR_2</a>  | 5350 00B4h             | 5351 00B4h             |
| B8h    | 32     | <a href="#">STC_CORE2_CURMISR_3</a>  | 5350 00B8h             | 5351 00B8h             |
| BCh    | 32     | <a href="#">STC_CORE2_CURMISR_4</a>  | 5350 00BCh             | 5351 00BCh             |
| C0h    | 32     | <a href="#">STC_CORE2_CURMISR_5</a>  | 5350 00C0h             | 5351 00C0h             |
| C4h    | 32     | <a href="#">STC_CORE2_CURMISR_6</a>  | 5350 00C4h             | 5351 00C4h             |
| C8h    | 32     | <a href="#">STC_CORE2_CURMISR_7</a>  | 5350 00C8h             | 5351 00C8h             |
| CCh    | 32     | <a href="#">STC_CORE2_CURMISR_8</a>  | 5350 00CCh             | 5351 00CCh             |
| D0h    | 32     | <a href="#">STC_CORE2_CURMISR_9</a>  | 5350 00D0h             | 5351 00D0h             |
| D4h    | 32     | <a href="#">STC_CORE2_CURMISR_10</a> | 5350 00D4h             | 5351 00D4h             |
| D8h    | 32     | <a href="#">STC_CORE2_CURMISR_11</a> | 5350 00D8h             | 5351 00D8h             |
| DCh    | 32     | <a href="#">STC_CORE2_CURMISR_12</a> | 5350 00DCh             | 5351 00DCh             |
| E0h    | 32     | <a href="#">STC_CORE2_CURMISR_13</a> | 5350 00E0h             | 5351 00E0h             |
| E4h    | 32     | <a href="#">STC_CORE2_CURMISR_14</a> | 5350 00E4h             | 5351 00E4h             |
| E8h    | 32     | <a href="#">STC_CORE2_CURMISR_15</a> | 5350 00E8h             | 5351 00E8h             |
| ECh    | 32     | <a href="#">STC_CORE2_CURMISR_16</a> | 5350 00ECh             | 5351 00ECh             |
| F0h    | 32     | <a href="#">STC_CORE2_CURMISR_17</a> | 5350 00F0h             | 5351 00F0h             |
| F4h    | 32     | <a href="#">STC_CORE2_CURMISR_18</a> | 5350 00F4h             | 5351 00F4h             |
| F8h    | 32     | <a href="#">STC_CORE2_CURMISR_19</a> | 5350 00F8h             | 5351 00F8h             |
| FCh    | 32     | <a href="#">STC_CORE2_CURMISR_20</a> | 5350 00FCh             | 5351 00FCh             |
| 100h   | 32     | <a href="#">STC_CORE2_CURMISR_21</a> | 5350 0100h             | 5351 0100h             |
| 104h   | 32     | <a href="#">STC_CORE2_CURMISR_22</a> | 5350 0104h             | 5351 0104h             |
| 108h   | 32     | <a href="#">STC_CORE2_CURMISR_23</a> | 5350 0108h             | 5351 0108h             |
| 10Ch   | 32     | <a href="#">STC_CORE2_CURMISR_24</a> | 5350 010Ch             | 5351 010Ch             |

**Table 4-11. STC Registers, Base Address=5350 0000h, Length=512 (continued)**

| Offset | Length | Register Name                        | R5SS0 Physical Address | R5SS1 Physical Address |
|--------|--------|--------------------------------------|------------------------|------------------------|
| 110h   | 32     | <a href="#">STC_CORE2_CURMISR_25</a> | 5350 0110h             | 5351 0110h             |
| 114h   | 32     | <a href="#">STC_CORE2_CURMISR_26</a> | 5350 0114h             | 5351 0114h             |
| 118h   | 32     | <a href="#">STC_CORE2_CURMISR_27</a> | 5350 0118h             | 5351 0118h             |

**Table 4-12. ICACHE\_CORE0 Registers, Base Address=7400 0000h, Length=8388608**

| Offset  | Length | Register Name                      | R5SS0 Physical Address | R5SS1 Physical Address |
|---------|--------|------------------------------------|------------------------|------------------------|
| 0h      | 32     | <a href="#">ICACHE_CORE0_START</a> | 7400 0000h             | 7600 0000h             |
| 7FFFFCh | 32     | <a href="#">ICACHE_CORE0_END</a>   | 747F FFFCh             | 767F FFFCh             |

**Table 4-13. DCACHE\_CORE0 Registers, Base Address=7480 0000h, Length=8388608**

| Offset  | Length | Register Name                      | R5SS0 Physical Address | R5SS1 Physical Address |
|---------|--------|------------------------------------|------------------------|------------------------|
| 0h      | 32     | <a href="#">DCACHE_CORE0_START</a> | 7480 0000h             | 7680 0000h             |
| 7FFFFCh | 32     | <a href="#">DCACHE_CORE0_END</a>   | 74FF FFFCh             | 76FF FFFCh             |

**Table 4-14. ICACHE\_CORE1 Registers, Base Address=7500 0000h, Length=8388608**

| Offset  | Length | Register Name                      | R5SS0 Physical Address | R5SS1 Physical Address |
|---------|--------|------------------------------------|------------------------|------------------------|
| 0h      | 32     | <a href="#">ICACHE_CORE1_START</a> | 7500 0000h             | 7700 0000h             |
| 7FFFFCh | 32     | <a href="#">ICACHE_CORE1_END</a>   | 757F FFFCh             | 777F FFFCh             |

**Table 4-15. DCACHE\_CORE1 Registers, Base Address=7580 0000h, Length=8388608**

| Offset  | Length | Register Name                      | R5SS0 Physical Address | R5SS1 Physical Address |
|---------|--------|------------------------------------|------------------------|------------------------|
| 0h      | 32     | <a href="#">DCACHE_CORE1_START</a> | 7580 0000h             | 7780 0000h             |
| 7FFFFCh | 32     | <a href="#">DCACHE_CORE1_END</a>   | 75FF FFFCh             | 77FF FFFCh             |

**Table 4-16. TCMA\_CORE0 Registers, Base Address=7800 0000h, Length=65536**

| Offset | Length | Register Name                    | R5SS0 Physical Address | R5SS1 Physical Address |
|--------|--------|----------------------------------|------------------------|------------------------|
| 0h     | 32     | <a href="#">TCMA_CORE0_START</a> | 7800 0000h             | 7840 0000h             |
| 27FFCh | 32     | <a href="#">TCMA_CORE0_END</a>   | 7802 7FFCh             | 7842 7FFCh             |

**Table 4-17. TCMB\_CORE0 Registers, Base Address=7810 0000h, Length=65536**

| Offset  | Length | Register Name                    | R5SS0 Physical Address | R5SS1 Physical Address |
|---------|--------|----------------------------------|------------------------|------------------------|
| 0h      | 32     | <a href="#">TCMB_CORE0_START</a> | 7810 0000h             | 7850 0000h             |
| 2FFFFCh | 32     | <a href="#">TCMB_CORE0_END</a>   | 7812 FFFCh             | 7852 FFFCh             |

**Table 4-18. TCMA\_CORE1 Registers, Base Address=7820 0000h, Length=32768**

| Offset | Length | Register Name                    | R5SS0 Physical Address | R5SS1 Physical Address |
|--------|--------|----------------------------------|------------------------|------------------------|
| 0h     | 32     | <a href="#">TCMA_CORE1_START</a> | 7820 0000h             | 7860 0000h             |
| 7FFCh  | 32     | <a href="#">TCMA_CORE1_END</a>   | 7820 7FFCh             | 7860 7FFCh             |

**Table 4-19. TCMB\_CORE1 Registers, Base Address=7830 0000h, Length=32768**

| Offset | Length | Register Name                    | R5SS0 Physical Address | R5SS1 Physical Address |
|--------|--------|----------------------------------|------------------------|------------------------|
| 0h     | 32     | <a href="#">TCMB_CORE1_START</a> | 7830 0000h             | 7870 0000h             |
| 17FFCh | 32     | <a href="#">TCMB_CORE1_END</a>   | 7831 7FFCh             | 7871 7FFCh             |

#### 4.1.2 R5SS Registers

##### R5SS Registers

#### 4.1.2.1 TCMA\_CORE0\_ROM\_START Register

##### 1 TCMA\_CORE0\_ROM\_START Register (Offset = 0h) [reset = 0h]

Return to [Summary Table](#)

**Table 4-20. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 0000 0000h       |

**Figure 4-1. TCMA\_CORE0\_ROM\_START Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ROM_START |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ROM_START |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ROM_START |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ROM_START |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 4-22. TCMA\_CORE0\_ROM\_START Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                 |
|------|-----------|------|-------|---------------------------------------------|
| 31:0 | ROM_START | R    | 0h    | ROM start address of master sub system tcma |



#### 4.1.2.2 TCMA\_CORE0\_ROM\_END Register

1 TCMA\_CORE0\_ROM\_END Register (Offset = 1FFFCh) [reset = 0h]

Return to [Summary Table](#)

**Table 4-23. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 0001 FFFCh       |

**Figure 4-2. TCMA\_CORE0\_ROM\_END Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ROM_END |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ROM_END |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ROM_END |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ROM_END |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-25. TCMA\_CORE0\_ROM\_END Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                               |
|------|---------|------|-------|-------------------------------------------|
| 31:0 | ROM_END | R    | 0h    | ROM end address of master sub system tcma |

#### 4.1.2.3 TCMA\_CORE1\_RAM\_START Register

**1 TCMA\_CORE1\_RAM\_START Register (Offset = 0h) [reset = 0h]**

Return to [Summary Table](#)

**Table 4-26. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 0000 0000h       |
| R5SS1         | 0000 0000h       |

**Figure 4-3. TCMA\_CORE1\_RAM\_START Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAM_START |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM_START |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RAM_START |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RAM_START |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 4-28. TCMA\_CORE1\_RAM\_START Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                 |
|------|-----------|------|-------|---------------------------------------------|
| 31:0 | RAM_START | R/W  | 0h    | RAM start address of master sub system tcma |

#### 4.1.2.4 TCMA\_CORE1\_RAM\_END Register

**1 TCMA\_CORE1\_RAM\_END Register (Offset = 7FFCh) [reset = 0h]**

Return to [Summary Table](#)

**Table 4-29. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 0000 7FFCh       |
| R5SS1         | 0000 7FFCh       |

**Figure 4-4. TCMA\_CORE1\_RAM\_END Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAM_END |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM_END |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RAM_END |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RAM_END |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-31. TCMA\_CORE1\_RAM\_END Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                               |
|------|---------|------|-------|-------------------------------------------|
| 31:0 | RAM_END | R/W  | 0h    | RAM end address of master sub system tcma |

#### 4.1.2.5 TCMA\_CORE0\_RAM\_START Register

##### 1 TCMA\_CORE0\_RAM\_START Register (Offset = 0h) [reset = 0h]

Return to [Summary Table](#)

**Table 4-32. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 0002 0000h       |
| R5SS1         | 0000 0000h       |

**Figure 4-5. TCMA\_CORE0\_RAM\_START Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAM_START |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM_START |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RAM_START |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RAM_START |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 4-34. TCMA\_CORE0\_RAM\_START Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                 |
|------|-----------|------|-------|---------------------------------------------|
| 31:0 | RAM_START | R/W  | 0h    | RAM start address of master sub system tcma |

#### 4.1.2.6 TCMA\_CORE0\_RAM\_END Register

##### 1 TCMA\_CORE0\_RAM\_END Register (Offset = 7FFCh) [reset = 0h]

Return to [Summary Table](#)

**Table 4-35. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 0002 7FFCh       |
| R5SS1         | 0000 7FFCh       |

**Figure 4-6. TCMA\_CORE0\_RAM\_END Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAM_END |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAM_END |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RAM_END |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RAM_END |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-37. TCMA\_CORE0\_RAM\_END Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                               |
|------|---------|------|-------|-------------------------------------------|
| 31:0 | RAM_END | R/W  | 0h    | RAM end address of master sub system tcma |

#### 4.1.2.7 TCMB\_CORE0\_RAM\_START Register

**1 TCMB\_CORE0\_RAM\_START Register (Offset = 0h) [reset = 0h]**

Return to [Summary Table](#)

**Table 4-38. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 0008 0000h       |
| R5SS1         | 0008 0000h       |

**Figure 4-7. TCMB\_CORE0\_RAM\_START Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-40. TCMB\_CORE0\_RAM\_START Register Field Descriptions**

| Bit  | Field | Type | Reset | Description        |
|------|-------|------|-------|--------------------|
| 31:0 | START | R/W  | 0h    | TCMB start address |

#### 4.1.2.8 TCMB\_CORE0\_RAM\_END Register

**1 TCMB\_CORE0\_RAM\_END Register (Offset = 17FFCh) [reset = 0h]**

Return to [Summary Table](#)

**Table 4-41. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 0009 7FFCh       |
| R5SS1         | 0009 7FFCh       |

**Figure 4-8. TCMB\_CORE0\_RAM\_END Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 4-43. TCMB\_CORE0\_RAM\_END Register Field Descriptions**

| Bit  | Field | Type | Reset | Description      |
|------|-------|------|-------|------------------|
| 31:0 | END   | R/W  | 0h    | TCMB end address |

#### 4.1.2.9 TCMB\_CORE1\_RAM\_START Register

**1 TCMB\_CORE1\_RAM\_START Register (Offset = 0h) [reset = 0h]**

Return to [Summary Table](#)

**Table 4-44. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 0008 0000h       |
| R5SS1         | 0008 0000h       |

**Figure 4-9. TCMB\_CORE1\_RAM\_START Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-46. TCMB\_CORE1\_RAM\_START Register Field Descriptions**

| Bit  | Field | Type | Reset | Description        |
|------|-------|------|-------|--------------------|
| 31:0 | START | R/W  | 0h    | TCMB start address |



#### 4.1.2.10 TCMB\_CORE1\_RAM\_END Register

1 TCMB\_CORE1\_RAM\_END Register (Offset = 17FFCh) [reset = 0h]

Return to [Summary Table](#)

**Table 4-47. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 0009 7FFCh       |
| R5SS1         | 0009 7FFCh       |

**Figure 4-10. TCMB\_CORE1\_RAM\_END Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 4-49. TCMB\_CORE1\_RAM\_END Register Field Descriptions**

| Bit  | Field | Type | Reset | Description      |
|------|-------|------|-------|------------------|
| 31:0 | END   | R/W  | 0h    | TCMB end address |

#### 4.1.2.11 VIM0\_PID Register

##### 1 VIM0\_PID Register (Offset = 0h) [reset = 60900001h]

The Revision Register contains the major and minor revisions for the module.

Return to [Summary Table](#)

**Table 4-50. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0000h       |
| R5SS1         | 50F0 0000h       |

**Figure 4-11. VIM0\_PID Name Register**

|        |    |       |    |      |       |    |    |
|--------|----|-------|----|------|-------|----|----|
| 31     | 30 | 29    | 28 | 27   | 26    | 25 | 24 |
| SCHEME |    | BU    |    | FUNC |       |    |    |
| R      |    | R     |    | R    |       |    |    |
| 1h     |    | 2h    |    | 90h  |       |    |    |
| 23     | 22 | 21    | 20 | 19   | 18    | 17 | 16 |
| FUNC   |    |       |    |      |       |    |    |
| R      |    |       |    |      |       |    |    |
| 90h    |    |       |    |      |       |    |    |
| 15     | 14 | 13    | 12 | 11   | 10    | 9  | 8  |
| RTL    |    |       |    |      | MAJOR |    |    |
| R      |    |       |    |      | R     |    |    |
| 0h     |    |       |    |      | 0h    |    |    |
| 7      | 6  | 5     | 4  | 3    | 2     | 1  | 0  |
| CUSTOM |    | MINOR |    |      |       |    |    |
| R      |    | R     |    |      |       |    |    |
| 0h     |    | 1h    |    |      |       |    |    |

**Table 4-52. VIM0\_PID Register Field Descriptions**

| Bit   | Field  | Type | Reset | Description                                   |
|-------|--------|------|-------|-----------------------------------------------|
| 31:30 | SCHEME | R    | 1h    | PID register scheme                           |
| 29:28 | BU     | R    | 2h    | Business Unit: 10 = Processors                |
| 27:16 | FUNC   | R    | 90h   | Module ID                                     |
| 15:11 | RTL    | R    | 0h    | RTL revision. Will vary depending on release. |
| 10:8  | MAJOR  | R    | 0h    | Major revision                                |
| 7:6   | CUSTOM | R    | 0h    | Custom                                        |
| 5:0   | MINOR  | R    | 1h    | Minor revision                                |

#### 4.1.2.12 VIM0\_INFO Register

##### 1 VIM0\_INFO Register (Offset = 4h) [reset = 100h]

The Info Register gives the configuration Information of this VIM.

Return to [Summary Table](#)

**Table 4-53. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0004h       |
| R5SS1         | 50F0 0004h       |

**Figure 4-12. VIM0\_INFO Name Register**

|            |    |    |    |            |    |    |    |
|------------|----|----|----|------------|----|----|----|
| 31         | 30 | 29 | 28 | 27         | 26 | 25 | 24 |
| RES1       |    |    |    |            |    |    |    |
| R          |    |    |    |            |    |    |    |
| 0h         |    |    |    |            |    |    |    |
| 23         | 22 | 21 | 20 | 19         | 18 | 17 | 16 |
| RES1       |    |    |    |            |    |    |    |
| R          |    |    |    |            |    |    |    |
| 0h         |    |    |    |            |    |    |    |
| 15         | 14 | 13 | 12 | 11         | 10 | 9  | 8  |
| RES1       |    |    |    | INTERRUPTS |    |    |    |
| R          |    |    |    | R          |    |    |    |
| 0h         |    |    |    | 100h       |    |    |    |
| 7          | 6  | 5  | 4  | 3          | 2  | 1  | 0  |
| INTERRUPTS |    |    |    |            |    |    |    |
| R          |    |    |    |            |    |    |    |
| 100h       |    |    |    |            |    |    |    |

**Table 4-55. VIM0\_INFO Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                |
|-------|------------|------|-------|----------------------------|
| 31:11 | RES1       | R    | 0h    | RESERVE FIELD              |
| 10:0  | INTERRUPTS | R    | 100h  | Total number of Interrupts |

#### 4.1.2.13 VIM0\_PRIIRQ Register

##### 1 VIM0\_PRIIRQ Register (Offset = 8h) [reset = 0h]

The Prioritized IRQ Register shows the number of the highest priority pending IRQ.

Return to [Summary Table](#)

**Table 4-56. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0008h       |
| R5SS1         | 50F0 0008h       |

**Figure 4-13. VIM0\_PRIIRQ Name Register**

|       |      |    |    |     |    |     |    |
|-------|------|----|----|-----|----|-----|----|
| 31    | 30   | 29 | 28 | 27  | 26 | 25  | 24 |
| VALID | RES2 |    |    |     |    |     |    |
| R     | R    |    |    |     |    |     |    |
| 0h    | 0h   |    |    |     |    |     |    |
| 23    | 22   | 21 | 20 | 19  | 18 | 17  | 16 |
| RES2  |      |    |    | PRI |    |     |    |
| R     |      |    |    | R   |    |     |    |
| 0h    |      |    |    | 0h  |    |     |    |
| 15    | 14   | 13 | 12 | 11  | 10 | 9   | 8  |
| RES3  |      |    |    |     |    | NUM |    |
| R     |      |    |    |     |    | R   |    |
| 0h    |      |    |    |     |    | 0h  |    |
| 7     | 6    | 5  | 4  | 3   | 2  | 1   | 0  |
| NUM   |      |    |    |     |    |     |    |
| R     |      |    |    |     |    |     |    |
| 0h    |      |    |    |     |    |     |    |

**Table 4-58. VIM0\_PRIIRQ Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                        |
|-------|-------|------|-------|------------------------------------------------------------------------------------|
| 31    | VALID | R    | 0h    | Indicates that the num field is valid.                                             |
| 30:20 | RES2  | R    | 0h    | RESERVE FIELD                                                                      |
| 19:16 | PRI   | R    | 0h    | Priority of the highest priority pending IRQ. valid only if the valid flag is set. |
| 15:10 | RES3  | R    | 0h    | RESERVE FIELD                                                                      |
| 9:0   | NUM   | R    | 0h    | Number of the highest priority pending IRQ. valid only if the valid flag is set.   |

#### 4.1.2.14 VIM0\_PRIFIQ Register

##### 1 VIM0\_PRIFIQ Register (Offset = Ch) [reset = 0h]

The Prioritized FIQ Register shows the number of the highest priority pending FIQ.

Return to [Summary Table](#)

**Table 4-59. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 000Ch       |
| R5SS1         | 50F0 000Ch       |

**Figure 4-14. VIM0\_PRIFIQ Name Register**

|       |      |    |    |     |    |     |    |
|-------|------|----|----|-----|----|-----|----|
| 31    | 30   | 29 | 28 | 27  | 26 | 25  | 24 |
| VALID | RES4 |    |    |     |    |     |    |
| R     | R    |    |    |     |    |     |    |
| 0h    | 0h   |    |    |     |    |     |    |
| 23    | 22   | 21 | 20 | 19  | 18 | 17  | 16 |
| RES4  |      |    |    | PRI |    |     |    |
| R     |      |    |    | R   |    |     |    |
| 0h    |      |    |    | 0h  |    |     |    |
| 15    | 14   | 13 | 12 | 11  | 10 | 9   | 8  |
| RES5  |      |    |    |     |    | NUM |    |
| R     |      |    |    |     |    | R   |    |
| 0h    |      |    |    |     |    | 0h  |    |
| 7     | 6    | 5  | 4  | 3   | 2  | 1   | 0  |
| NUM   |      |    |    |     |    |     |    |
| R     |      |    |    |     |    |     |    |
| 0h    |      |    |    |     |    |     |    |

**Table 4-61. VIM0\_PRIFIQ Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                        |
|-------|-------|------|-------|------------------------------------------------------------------------------------|
| 31    | VALID | R    | 0h    | Indicates that the num field is valid.                                             |
| 30:20 | RES4  | R    | 0h    | RESERVE FIELD                                                                      |
| 19:16 | PRI   | R    | 0h    | Priority of the highest priority pending FIQ. valid only if the valid flag is set. |
| 15:10 | RES5  | R    | 0h    | RESERVE FIELD                                                                      |
| 9:0   | NUM   | R    | 0h    | Number of the highest priority pending FIQ. valid only if the valid flag is set.   |

#### 4.1.2.15 VIM0\_IRQGSTS Register

##### 1 VIM0\_IRQGSTS Register (Offset = 10h) [reset = 0h]

The IRQ Group Status Register indicates which groups have pending IRQ interrupts.

Return to [Summary Table](#)

**Table 4-62. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0010h       |
| R5SS1         | 50F0 0010h       |

**Figure 4-15. VIM0\_IRQGSTS Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| STS |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| STS |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| STS |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| STS |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 4-64. VIM0\_IRQGSTS Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                            |
|------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | STS   | R    | 0h    | This field indicates that one or more interrupts in Group M are mapped to IRQ, unmasked, and pending. Bit 0 corresponds to Group 0; Bit 1 corresponds to Group 1 etc. The interrupts associated with each group are $[(M*32)+31:M*32]$ |

#### 4.1.2.16 VIM0\_FIQSTS Register

##### 1 VIM0\_FIQSTS Register (Offset = 14h) [reset = 0h]

The FIQ Group Status Register indicates which groups have pending FIQ interrupts.

Return to [Summary Table](#)

**Table 4-65. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0014h       |
| R5SS1         | 50F0 0014h       |

**Figure 4-16. VIM0\_FIQSTS Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| STS |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| STS |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| STS |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| STS |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 4-67. VIM0\_FIQSTS Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                            |
|------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | STS   | R    | 0h    | This field indicates that one or more interrupts in Group M are mapped to FIQ, unmasked, and pending. Bit 0 corresponds to Group 0; Bit 1 corresponds to Group 1 etc. The interrupts associated with each group are $[(M*32)+31:M*32]$ |

#### 4.1.2.17 VIM0\_IRQVEC Register

##### 1 VIM0\_IRQVEC Register (Offset = 18h) [reset = 0h]

The IRQ Vector Address Register contains the 32-bit address of the interrupt vector for the current pending IRQ.

Return to [Summary Table](#)

**Table 4-68. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0018h       |
| R5SS1         | 50F0 0018h       |

**Figure 4-17. VIM0\_IRQVEC Name Register**

|      |    |    |    |    |    |       |    |
|------|----|----|----|----|----|-------|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25    | 24 |
| ADDR |    |    |    |    |    |       |    |
| R/W  |    |    |    |    |    |       |    |
| 0h   |    |    |    |    |    |       |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17    | 16 |
| ADDR |    |    |    |    |    |       |    |
| R/W  |    |    |    |    |    |       |    |
| 0h   |    |    |    |    |    |       |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9     | 8  |
| ADDR |    |    |    |    |    |       |    |
| R/W  |    |    |    |    |    |       |    |
| 0h   |    |    |    |    |    |       |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1     | 0  |
| ADDR |    |    |    |    |    | RES21 |    |
| R/W  |    |    |    |    |    | R     |    |
| 0h   |    |    |    |    |    | 0h    |    |

**Table 4-70. VIM0\_IRQVEC Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                |
|------|-------|------|-------|------------------------------------------------------------------------------------------------------------|
| 31:2 | ADDR  | R/W  | 0h    | Upper 30 bits of the 32-bit vector address. Only valid if the Prioritized IRQ Register valid flag is true. |
| 1:0  | RES21 | R    | 0h    | RESERVE FIELD                                                                                              |



#### 4.1.2.18 VIM0\_FIQVEC Register

##### 1 VIM0\_FIQVEC Register (Offset = 1Ch) [reset = 0h]

The FIQ Vector Address Register contains the 32-bit address of the interrupt vector for the current pending FIQ.

Return to [Summary Table](#)

**Table 4-71. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 001Ch       |
| R5SS1         | 50F0 001Ch       |

**Figure 4-18. VIM0\_FIQVEC Name Register**

|      |    |    |    |    |    |       |    |
|------|----|----|----|----|----|-------|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25    | 24 |
| ADDR |    |    |    |    |    |       |    |
| R/W  |    |    |    |    |    |       |    |
| 0h   |    |    |    |    |    |       |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17    | 16 |
| ADDR |    |    |    |    |    |       |    |
| R/W  |    |    |    |    |    |       |    |
| 0h   |    |    |    |    |    |       |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9     | 8  |
| ADDR |    |    |    |    |    |       |    |
| R/W  |    |    |    |    |    |       |    |
| 0h   |    |    |    |    |    |       |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1     | 0  |
| ADDR |    |    |    |    |    | RES22 |    |
| R/W  |    |    |    |    |    | R     |    |
| 0h   |    |    |    |    |    | 0h    |    |

**Table 4-73. VIM0\_FIQVEC Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                |
|------|-------|------|-------|------------------------------------------------------------------------------------------------------------|
| 31:2 | ADDR  | R/W  | 0h    | Upper 30 bits of the 32-bit vector address. Only valid if the Prioritized FIQ Register valid flag is true. |
| 1:0  | RES22 | R    | 0h    | RESERVE FIELD                                                                                              |

#### 4.1.2.19 VIM0\_ACTIRQ Register

##### 1 VIM0\_ACTIRQ Register (Offset = 20h) [reset = 0h]

The Active IRQ Register shows the number of the currently active IRQ.

Return to [Summary Table](#)

**Table 4-74. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0020h       |
| R5SS1         | 50F0 0020h       |

**Figure 4-19. VIM0\_ACTIRQ Name Register**

|       |      |    |    |     |    |     |    |
|-------|------|----|----|-----|----|-----|----|
| 31    | 30   | 29 | 28 | 27  | 26 | 25  | 24 |
| VALID | RES6 |    |    |     |    |     |    |
| R     | R    |    |    |     |    |     |    |
| 0h    | 0h   |    |    |     |    |     |    |
| 23    | 22   | 21 | 20 | 19  | 18 | 17  | 16 |
| RES6  |      |    |    | PRI |    |     |    |
| R     |      |    |    | R   |    |     |    |
| 0h    |      |    |    | 0h  |    |     |    |
| 15    | 14   | 13 | 12 | 11  | 10 | 9   | 8  |
| RES7  |      |    |    |     |    | NUM |    |
| R     |      |    |    |     |    | R   |    |
| 0h    |      |    |    |     |    | 0h  |    |
| 7     | 6    | 5  | 4  | 3   | 2  | 1   | 0  |
| NUM   |      |    |    |     |    |     |    |
| R     |      |    |    |     |    |     |    |
| 0h    |      |    |    |     |    |     |    |

**Table 4-76. VIM0\_ACTIRQ Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                   |
|-------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | VALID | R    | 0h    | Indicates that the num field is valid. Set when the ACTIRQ Vector Address Register is read and cleared whenever the IRQ Vector Address Register is written.   |
| 30:20 | RES6  | R    | 0h    | RESERVE FIELD                                                                                                                                                 |
| 19:16 | PRI   | R    | 0h    | Priority of the highest priority pending ACTIRQ. valid only if the valid flag is set.                                                                         |
| 15:10 | RES7  | R    | 0h    | RESERVE FIELD                                                                                                                                                 |
| 9:0   | NUM   | R    | 0h    | Number of the currently active IRQ. Loaded from the Prioritized ACTIRQ Register whenever the IRQ Vector Address is read. Valid only if the valid flag is set. |

#### 4.1.2.20 VIM0\_ACTFIQ Register

##### 1 VIM0\_ACTFIQ Register (Offset = 24h) [reset = 0h]

The Active FIQ Register shows the number of the currently active FIQ.

Return to [Summary Table](#)

**Table 4-77. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0024h       |
| R5SS1         | 50F0 0024h       |

**Figure 4-20. VIM0\_ACTFIQ Name Register**

|       |      |    |    |     |    |     |    |
|-------|------|----|----|-----|----|-----|----|
| 31    | 30   | 29 | 28 | 27  | 26 | 25  | 24 |
| VALID | RES8 |    |    |     |    |     |    |
| R     | R    |    |    |     |    |     |    |
| 0h    | 0h   |    |    |     |    |     |    |
| 23    | 22   | 21 | 20 | 19  | 18 | 17  | 16 |
| RES8  |      |    |    | PRI |    |     |    |
| R     |      |    |    | R   |    |     |    |
| 0h    |      |    |    | 0h  |    |     |    |
| 15    | 14   | 13 | 12 | 11  | 10 | 9   | 8  |
| RES9  |      |    |    |     |    | NUM |    |
| R     |      |    |    |     |    | R   |    |
| 0h    |      |    |    |     |    | 0h  |    |
| 7     | 6    | 5  | 4  | 3   | 2  | 1   | 0  |
| NUM   |      |    |    |     |    |     |    |
| R     |      |    |    |     |    |     |    |
| 0h    |      |    |    |     |    |     |    |

**Table 4-79. VIM0\_ACTFIQ Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                |
|-------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | VALID | R    | 0h    | Indicates that the num field is valid. Set when the FIQ Vector Address Register is read and cleared whenever the FIQ Vector Address Register is written.   |
| 30:20 | RES8  | R    | 0h    | RESERVE FIELD                                                                                                                                              |
| 19:16 | PRI   | R    | 0h    | Priority of the highest priority pending IRQ. valid only if the valid flag is set.                                                                         |
| 15:10 | RES9  | R    | 0h    | RESERVE FIELD                                                                                                                                              |
| 9:0   | NUM   | R    | 0h    | Number of the currently active FIQ. Loaded from teh Prioritized FIQ Register whenever the FIQ Vector Address is read. Valid only if the valid flag is set. |

#### 4.1.2.21 VIM0\_IRQPRIMSK Register

##### 1 VIM0\_IRQPRIMSK Register (Offset = 28h) [reset = FFFFh]

The IRQ Priority Mask Register allows all IRQs of a particular priority to be enabled or disabled.

Return to [Summary Table](#)

**Table 4-80. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0028h       |
| R5SS1         | 50F0 0028h       |

**Figure 4-21. VIM0\_IRQPRIMSK Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RES24 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RES24 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSK   |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSK   |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |

**Table 4-82. VIM0\_IRQPRIMSK Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                |
|-------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RES24 | R    | 0h    | RESERVE FIELD                                                                                                              |
| 15:0  | MSK   | R/W  | FFFFh | Each bit corresponds to the given priority. 1 - IRQs of this priority are enabled. 0 - IRQs of this priority are disabled. |

#### 4.1.2.22 VIM0\_FIQPRIMSK Register

##### 1 VIM0\_FIQPRIMSK Register (Offset = 2Ch) [reset = FFFFh]

The FIQ Priority Mask Register allows all FIQs of a particular priority to be enabled or disabled.

Return to [Summary Table](#)

**Table 4-83. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 002Ch       |
| R5SS1         | 50F0 002Ch       |

**Figure 4-22. VIM0\_FIQPRIMSK Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RES24 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RES24 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSK   |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSK   |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |

**Table 4-85. VIM0\_FIQPRIMSK Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                |
|-------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RES24 | R    | 0h    | RESERVE FIELD                                                                                                              |
| 15:0  | MSK   | R/W  | FFFFh | Each bit corresponds to the given priority. 1 - FIQs of this priority are enabled. 0 - FIQs of this priority are disabled. |

#### 4.1.2.23 VIM0\_DEDVEC Register

##### 1 VIM0\_DEDVEC Register (Offset = 30h) [reset = 0h]

The DED Vector Address contains a default vector address for when an uncorrectable error is detected for an active IRQ or FIQ.

Return to [Summary Table](#)

**Table 4-86. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0030h       |
| R5SS1         | 50F0 0030h       |

**Figure 4-23. VIM0\_DEDVEC Name Register**

|      |    |    |    |    |    |       |    |
|------|----|----|----|----|----|-------|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25    | 24 |
| ADDR |    |    |    |    |    |       |    |
| R/W  |    |    |    |    |    |       |    |
| 0h   |    |    |    |    |    |       |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17    | 16 |
| ADDR |    |    |    |    |    |       |    |
| R/W  |    |    |    |    |    |       |    |
| 0h   |    |    |    |    |    |       |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9     | 8  |
| ADDR |    |    |    |    |    |       |    |
| R/W  |    |    |    |    |    |       |    |
| 0h   |    |    |    |    |    |       |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1     | 0  |
| ADDR |    |    |    |    |    | RES23 |    |
| R/W  |    |    |    |    |    | R     |    |
| 0h   |    |    |    |    |    | 0h    |    |

**Table 4-88. VIM0\_DEDVEC Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                 |
|------|-------|------|-------|---------------------------------------------|
| 31:2 | ADDR  | R/W  | 0h    | Upper 30 bits of the 32-bit vector address. |
| 1:0  | RES23 | R    | 0h    | RESERVE FIELD                               |

#### 4.1.2.24 VIM0\_RAW\_M Register

##### 1 VIM0\_RAW\_M Register (Offset = 400h) [reset = 0h]

Group M Interrupt Raw Status/Set Register (M is 0 to 7) Address formula = 50F00000h + Offset + M x 20h

Return to [Summary Table](#)

**Table 4-89. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0400h       |
| R5SS1         | 50F0 0400h       |

**Figure 4-24. VIM0\_RAW\_M Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| STS |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| STS |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| STS |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| STS |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 4-91. VIM0\_RAW\_M Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                 |
|------|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | STS   | R/W  | 0h    | This is the raw status of the events in Group M. Each bit corresponds to event Q where Q = Mx32+Bit<br>Read 0 Inactive<br>Read 1 Active/Pending<br>Write 0 No effect<br>Write 1 Set to Interrupt Raw Status |

#### 4.1.2.25 VIM0\_STS\_M Register

##### 1 VIM0\_STS\_M Register (Offset = 404h) [reset = 0h]

Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) Address formula = 50F00000h + Offset + M x 20h

Return to [Summary Table](#)

**Table 4-92. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0404h       |
| R5SS1         | 50F0 0404h       |

**Figure 4-25. VIM0\_STS\_M Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 4-94. VIM0\_STS\_M Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                           |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MASK  | R/W  | 0h    | This is the masked status of the events in Group M. Each bit corresponds to event Q where Q = Mx32+Bit<br>Read 0 Inactive or Disabled<br>Read 1 Active/Pending and Enabled<br>Write 0 No effect<br>Write 1 Clear Interrupt Raw Status |



#### 4.1.2.26 VIM0\_INTR\_EN\_SET\_M Register

##### 1 VIM0\_INTR\_EN\_SET\_M Register (Offset = 408h) [reset = 0h]

Group M Interrupt Enabled Set Register (M is 0 to 7) Address formula = 50F00000h + Offset + M x 20h

Return to [Summary Table](#)

**Table 4-95. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0408h       |
| R5SS1         | 50F0 0408h       |

**Figure 4-26. VIM0\_INTR\_EN\_SET\_M Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 4-97. VIM0\_INTR\_EN\_SET\_M Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                    |
|------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MASK  | R/W  | 0h    | This field is used to enable the mask of events in Group M. Each bit corresponds to event Q where Q = Mx32+Bit<br>Read 0 Disabled<br>Read 1 Enabled<br>Write 0 No effect<br>Write 1 Set Enable |

#### 4.1.2.27 VIM0\_INTER\_EN\_CLR\_M Register

##### 1 VIM0\_INTER\_EN\_CLR\_M Register (Offset = 40Ch) [reset = 0h]

Group M Interrupt Enabled Clear Register (M is 0 to 7) Address formula = 50F00000h + Offset + M x 20h

Return to [Summary Table](#)

**Table 4-98. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 040Ch       |
| R5SS1         | 50F0 040Ch       |

**Figure 4-27. VIM0\_INTER\_EN\_CLR\_M Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 4-100. VIM0\_INTER\_EN\_CLR\_M Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                       |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MASK  | R/W  | 0h    | This field is used to disable the mask of events in Group M. Each bit corresponds to event Q where Q = Mx32+Bit<br>Read 0 Disabled<br>Read 1 Enabled<br>Write 0 No effect<br>Write 1 Clear Enable |

#### 4.1.2.28 VIM0\_IRQSTS\_M Register

##### 1 VIM0\_IRQSTS\_M Register (Offset = 410h) [reset = 0h]

Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) Address formula = 50F00000h + Offset + M x 20h

Return to [Summary Table](#)

**Table 4-101. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0410h       |
| R5SS1         | 50F0 0410h       |

**Figure 4-28. VIM0\_IRQSTS\_M Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 4-103. VIM0\_IRQSTS\_M Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                             |
|------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MASK  | R/W  | 0h    | This is the masked status of the events in group M that are mapped to IRQ Each bit corresponds to event Q where Q = Mx32+Bit<br>Read 0 Inactive, Disabled, or not an IRQ<br>Read 1 Active/Pending, Enabled, and IRQ<br>Write 0 No effect<br>Write 1 Clear Interrupt Raw Status [if IRQ] |

#### 4.1.2.29 VIM0\_FIQSTS\_M Register

##### 1 VIM0\_FIQSTS\_M Register (Offset = 414h) [reset = 0h]

Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) Address formula = 50F00000h + Offset + M x 20h

Return to [Summary Table](#)

**Table 4-104. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0414h       |
| R5SS1         | 50F0 0414h       |

**Figure 4-29. VIM0\_FIQSTS\_M Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 4-106. VIM0\_FIQSTS\_M Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                             |
|------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MASK  | R/W  | 0h    | This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+Bit<br>Read 0 Inactive, Disabled, or not an FIQ<br>Read 1 Active/Pending, Enabled, and FIQ<br>Write 0 No effect<br>Write 1 Clear Interrupt Raw Status [if FIQ] |

#### 4.1.2.30 VIM0\_INTMAP\_M Register

##### 1 VIM0\_INTMAP\_M Register (Offset = 418h) [reset = 0h]

Group M Interrupt Map Register (M is 0 to 7) Address formula = 50F00000h + Offset + M x 20h

Return to [Summary Table](#)

**Table 4-107. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0418h       |
| R5SS1         | 50F0 0418h       |

**Figure 4-30. VIM0\_INTMAP\_M Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 4-109. VIM0\_INTMAP\_M Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                          |
|------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MASK  | R/W  | 0h    | This field is used to indicate which interrupt the corresponding event influences [if enabled] for event group M. Each bit corresponds to event Q where Q = Mx32+Bit<br>0 IRQ Interrupt [default]<br>1 FIQ Interrupt |

#### 4.1.2.31 VIM0\_INTTYPE\_M Register

##### 1 VIM0\_INTTYPE\_M Register (Offset = 41Ch) [reset = 0h]

Group M Interrupt Type Map Register (M is 0 to 7) Address formula = 50F00000h + Offset + M x 20h

Return to [Summary Table](#)

**Table 4-110. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 041Ch       |
| R5SS1         | 50F0 041Ch       |

**Figure 4-31. VIM0\_INTTYPE\_M Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| VAL |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| VAL |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| VAL |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| VAL |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 4-112. VIM0\_INTTYPE\_M Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | VAL   | R/W  | 0h    | This field is used to indicate whether the source of an interrupt is a level [default] or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event. The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit<br>0 Level [default]<br>1 Pulse |

#### 4.1.2.32 VIM0\_INTPRIORITY\_Q Register

##### 1 VIM0\_INTPRIORITY\_Q Register (Offset = 1000h) [reset = Fh]

Interrupt Q Priority Register (where Q is 0 to 255) Address formula = 50F00000h + Offset + Q x 4h

Return to [Summary Table](#)

**Table 4-113. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 1000h       |
| R5SS1         | 50F0 1000h       |

**Figure 4-32. VIM0\_INTPRIORITY\_Q Name Register**

|       |    |    |    |     |    |    |    |
|-------|----|----|----|-----|----|----|----|
| 31    | 30 | 29 | 28 | 27  | 26 | 25 | 24 |
| RES19 |    |    |    |     |    |    |    |
| R     |    |    |    |     |    |    |    |
| 0h    |    |    |    |     |    |    |    |
| 23    | 22 | 21 | 20 | 19  | 18 | 17 | 16 |
| RES19 |    |    |    |     |    |    |    |
| R     |    |    |    |     |    |    |    |
| 0h    |    |    |    |     |    |    |    |
| 15    | 14 | 13 | 12 | 11  | 10 | 9  | 8  |
| RES19 |    |    |    |     |    |    |    |
| R     |    |    |    |     |    |    |    |
| 0h    |    |    |    |     |    |    |    |
| 7     | 6  | 5  | 4  | 3   | 2  | 1  | 0  |
| RES19 |    |    |    | PRI |    |    |    |
| R     |    |    |    | R/W |    |    |    |
| 0h    |    |    |    | Fh  |    |    |    |

**Table 4-115. VIM0\_INTPRIORITY\_Q Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                            |
|------|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RES19 | R    | 0h    | RESERVE FIELD                                                                                                                                                                                          |
| 3:0  | PRI   | R/W  | Fh    | This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration<br>0 Highest Priority<br>15 Lowest Priority [Default] |

#### 4.1.2.33 VIM0\_INTVECTOR\_Q Register

##### 1 VIM0\_INTVECTOR\_Q Register (Offset = 2000h) [reset = 0h]

Interrupt Q Vector Register (Q is 0 to 255) Address formula = 50F00000h + Offset + Q x 4h

Return to [Summary Table](#)

**Table 4-116. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 2000h       |
| R5SS1         | 50F0 2000h       |

**Figure 4-33. VIM0\_INTVECTOR\_Q Name Register**

|      |    |    |    |    |    |       |    |
|------|----|----|----|----|----|-------|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25    | 24 |
| ADDR |    |    |    |    |    |       |    |
| R/W  |    |    |    |    |    |       |    |
| 0h   |    |    |    |    |    |       |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17    | 16 |
| ADDR |    |    |    |    |    |       |    |
| R/W  |    |    |    |    |    |       |    |
| 0h   |    |    |    |    |    |       |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9     | 8  |
| ADDR |    |    |    |    |    |       |    |
| R/W  |    |    |    |    |    |       |    |
| 0h   |    |    |    |    |    |       |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1     | 0  |
| ADDR |    |    |    |    |    | RES20 |    |
| R/W  |    |    |    |    |    | R     |    |
| 0h   |    |    |    |    |    | 0h    |    |

**Table 4-118. VIM0\_INTVECTOR\_Q Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | ADDR  | R/W  | 0h    | This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address [Base Address + 0x18] or FIQ Vector Address [Base Address + 0x1C] and the VECADDR pin when interrupt Q is the active interrupt. Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed. Reads to this register will stall the MMR interface until the read is able to be completed at the RAM. |
| 1:0  | RES20 | R    | 0h    | Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |



#### 4.1.2.34 VIM1\_PID Register

##### 1 VIM1\_PID Register (Offset = 0h) [reset = 60900001h]

The Revision Register contains the major and minor revisions for the module.

Return to [Summary Table](#)

**Table 4-119. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0000h       |
| R5SS1         | 50F0 0000h       |

**Figure 4-34. VIM1\_PID Name Register**

|        |    |       |    |      |       |    |    |
|--------|----|-------|----|------|-------|----|----|
| 31     | 30 | 29    | 28 | 27   | 26    | 25 | 24 |
| SCHEME |    | BU    |    | FUNC |       |    |    |
| R      |    | R     |    | R    |       |    |    |
| 1h     |    | 2h    |    | 90h  |       |    |    |
| 23     | 22 | 21    | 20 | 19   | 18    | 17 | 16 |
| FUNC   |    |       |    |      |       |    |    |
| R      |    |       |    |      |       |    |    |
| 90h    |    |       |    |      |       |    |    |
| 15     | 14 | 13    | 12 | 11   | 10    | 9  | 8  |
| RTL    |    |       |    |      | MAJOR |    |    |
| R      |    |       |    |      | R     |    |    |
| 0h     |    |       |    |      | 0h    |    |    |
| 7      | 6  | 5     | 4  | 3    | 2     | 1  | 0  |
| CUSTOM |    | MINOR |    |      |       |    |    |
| R      |    | R     |    |      |       |    |    |
| 0h     |    | 1h    |    |      |       |    |    |

**Table 4-121. VIM1\_PID Register Field Descriptions**

| Bit   | Field  | Type | Reset | Description                                   |
|-------|--------|------|-------|-----------------------------------------------|
| 31:30 | SCHEME | R    | 1h    | PID register scheme                           |
| 29:28 | BU     | R    | 2h    | Business Unit: 10 = Processors                |
| 27:16 | FUNC   | R    | 90h   | Module ID                                     |
| 15:11 | RTL    | R    | 0h    | RTL revision. Will vary depending on release. |
| 10:8  | MAJOR  | R    | 0h    | Major revision                                |
| 7:6   | CUSTOM | R    | 0h    | Custom                                        |
| 5:0   | MINOR  | R    | 1h    | Minor revision                                |

#### 4.1.2.35 VIM1\_INFO Register

##### 1 VIM1\_INFO Register (Offset = 4h) [reset = 100h]

The Info Register gives the configuration Information of this VIM.

Return to [Summary Table](#)

**Table 4-122. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0004h       |
| R5SS1         | 50F0 0004h       |

**Figure 4-35. VIM1\_INFO Name Register**

|            |    |    |    |            |    |    |    |
|------------|----|----|----|------------|----|----|----|
| 31         | 30 | 29 | 28 | 27         | 26 | 25 | 24 |
| RES1       |    |    |    |            |    |    |    |
| R          |    |    |    |            |    |    |    |
| 0h         |    |    |    |            |    |    |    |
| 23         | 22 | 21 | 20 | 19         | 18 | 17 | 16 |
| RES1       |    |    |    |            |    |    |    |
| R          |    |    |    |            |    |    |    |
| 0h         |    |    |    |            |    |    |    |
| 15         | 14 | 13 | 12 | 11         | 10 | 9  | 8  |
| RES1       |    |    |    | INTERRUPTS |    |    |    |
| R          |    |    |    | R          |    |    |    |
| 0h         |    |    |    | 100h       |    |    |    |
| 7          | 6  | 5  | 4  | 3          | 2  | 1  | 0  |
| INTERRUPTS |    |    |    |            |    |    |    |
| R          |    |    |    |            |    |    |    |
| 100h       |    |    |    |            |    |    |    |

**Table 4-124. VIM1\_INFO Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                |
|-------|------------|------|-------|----------------------------|
| 31:11 | RES1       | R    | 0h    | RESERVE FIELD              |
| 10:0  | INTERRUPTS | R    | 100h  | Total number of Interrupts |

#### 4.1.2.36 VIM1\_PRIIRQ Register

##### 1 VIM1\_PRIIRQ Register (Offset = 8h) [reset = 0h]

The Prioritized IRQ Register shows the number of the highest priority pending IRQ.

Return to [Summary Table](#)

**Table 4-125. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0008h       |
| R5SS1         | 50F0 0008h       |

**Figure 4-36. VIM1\_PRIIRQ Name Register**

|       |      |    |    |     |    |     |    |
|-------|------|----|----|-----|----|-----|----|
| 31    | 30   | 29 | 28 | 27  | 26 | 25  | 24 |
| VALID | RES2 |    |    |     |    |     |    |
| R     | R    |    |    |     |    |     |    |
| 0h    | 0h   |    |    |     |    |     |    |
| 23    | 22   | 21 | 20 | 19  | 18 | 17  | 16 |
| RES2  |      |    |    | PRI |    |     |    |
| R     |      |    |    | R   |    |     |    |
| 0h    |      |    |    | 0h  |    |     |    |
| 15    | 14   | 13 | 12 | 11  | 10 | 9   | 8  |
| RES3  |      |    |    |     |    | NUM |    |
| R     |      |    |    |     |    | R   |    |
| 0h    |      |    |    |     |    | 0h  |    |
| 7     | 6    | 5  | 4  | 3   | 2  | 1   | 0  |
| NUM   |      |    |    |     |    |     |    |
| R     |      |    |    |     |    |     |    |
| 0h    |      |    |    |     |    |     |    |

**Table 4-127. VIM1\_PRIIRQ Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                        |
|-------|-------|------|-------|------------------------------------------------------------------------------------|
| 31    | VALID | R    | 0h    | Indicates that the num field is valid.                                             |
| 30:20 | RES2  | R    | 0h    | RESERVE FIELD                                                                      |
| 19:16 | PRI   | R    | 0h    | Priority of the highest priority pending IRQ. valid only if the valid flag is set. |
| 15:10 | RES3  | R    | 0h    | RESERVE FIELD                                                                      |
| 9:0   | NUM   | R    | 0h    | Number of the highest priority pending IRQ. valid only if the valid flag is set.   |

#### 4.1.2.37 VIM1\_PRIFIQ Register

##### 1 VIM1\_PRIFIQ Register (Offset = Ch) [reset = 0h]

The Prioritized FIQ Register shows the number of the highest priority pending FIQ.

Return to [Summary Table](#)

**Table 4-128. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 000Ch       |
| R5SS1         | 50F0 000Ch       |

**Figure 4-37. VIM1\_PRIFIQ Name Register**

|       |      |    |    |     |    |     |    |
|-------|------|----|----|-----|----|-----|----|
| 31    | 30   | 29 | 28 | 27  | 26 | 25  | 24 |
| VALID | RES4 |    |    |     |    |     |    |
| R     | R    |    |    |     |    |     |    |
| 0h    | 0h   |    |    |     |    |     |    |
| 23    | 22   | 21 | 20 | 19  | 18 | 17  | 16 |
| RES4  |      |    |    | PRI |    |     |    |
| R     |      |    |    | R   |    |     |    |
| 0h    |      |    |    | 0h  |    |     |    |
| 15    | 14   | 13 | 12 | 11  | 10 | 9   | 8  |
| RES5  |      |    |    |     |    | NUM |    |
| R     |      |    |    |     |    | R   |    |
| 0h    |      |    |    |     |    | 0h  |    |
| 7     | 6    | 5  | 4  | 3   | 2  | 1   | 0  |
| NUM   |      |    |    |     |    |     |    |
| R     |      |    |    |     |    |     |    |
| 0h    |      |    |    |     |    |     |    |

**Table 4-130. VIM1\_PRIFIQ Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                        |
|-------|-------|------|-------|------------------------------------------------------------------------------------|
| 31    | VALID | R    | 0h    | Indicates that the num field is valid.                                             |
| 30:20 | RES4  | R    | 0h    | RESERVE FIELD                                                                      |
| 19:16 | PRI   | R    | 0h    | Priority of the highest priority pending FIQ. valid only if the valid flag is set. |
| 15:10 | RES5  | R    | 0h    | RESERVE FIELD                                                                      |
| 9:0   | NUM   | R    | 0h    | Number of the highest priority pending FIQ. valid only if the valid flag is set.   |

#### 4.1.2.38 VIM1\_IRQGSTS Register

##### 1 VIM1\_IRQGSTS Register (Offset = 10h) [reset = 0h]

The IRQ Group Status Register indicates which groups have pending IRQ interrupts.

Return to [Summary Table](#)

**Table 4-131. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0010h       |
| R5SS1         | 50F0 0010h       |

**Figure 4-38. VIM1\_IRQGSTS Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| STS |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| STS |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| STS |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| STS |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 4-133. VIM1\_IRQGSTS Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                              |
|------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | STS   | R    | 0h    | This field indicates that one or more interrupts in Group M are mapped to IRQ, unmasked, and pending. Bit 0 corresponds to Group 0; Bit 1 corresponds to Group 1 etc. The interrupts associated with each group are $[(M*32)+31:M*32]$ . |

#### 4.1.2.39 VIM1\_FIQSTS Register

##### 1 VIM1\_FIQSTS Register (Offset = 14h) [reset = 0h]

The FIQ Group Status Register indicates which groups have pending FIQ interrupts.

Return to [Summary Table](#)

**Table 4-134. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0014h       |
| R5SS1         | 50F0 0014h       |

**Figure 4-39. VIM1\_FIQSTS Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| STS |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| STS |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| STS |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| STS |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 4-136. VIM1\_FIQSTS Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                              |
|------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | STS   | R    | 0h    | This field indicates that one or more interrupts in Group M are mapped to FIQ, unmasked, and pending. Bit 0 corresponds to Group 0; Bit 1 corresponds to Group 1 etc. The interrupts associated with each group are $[(M*32)+31:M*32]$ . |

#### 4.1.2.40 VIM1\_IRQVEC Register

##### 1 VIM1\_IRQVEC Register (Offset = 18h) [reset = 0h]

The IRQ Vector Address Register contains the 32-bit address of the interrupt vector for the current pending IRQ.

Return to [Summary Table](#)

**Table 4-137. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0018h       |
| R5SS1         | 50F0 0018h       |

**Figure 4-40. VIM1\_IRQVEC Name Register**

|      |    |    |    |    |    |       |    |
|------|----|----|----|----|----|-------|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25    | 24 |
| ADDR |    |    |    |    |    |       |    |
| R/W  |    |    |    |    |    |       |    |
| 0h   |    |    |    |    |    |       |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17    | 16 |
| ADDR |    |    |    |    |    |       |    |
| R/W  |    |    |    |    |    |       |    |
| 0h   |    |    |    |    |    |       |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9     | 8  |
| ADDR |    |    |    |    |    |       |    |
| R/W  |    |    |    |    |    |       |    |
| 0h   |    |    |    |    |    |       |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1     | 0  |
| ADDR |    |    |    |    |    | RES21 |    |
| R/W  |    |    |    |    |    | R     |    |
| 0h   |    |    |    |    |    | 0h    |    |

**Table 4-139. VIM1\_IRQVEC Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                |
|------|-------|------|-------|------------------------------------------------------------------------------------------------------------|
| 31:2 | ADDR  | R/W  | 0h    | Upper 30 bits of the 32-bit vector address. Only valid if the Prioritized IRQ Register valid flag is true. |
| 1:0  | RES21 | R    | 0h    | RESERVE FIELD                                                                                              |

#### 4.1.2.41 VIM1\_FIQVEC Register

##### 1 VIM1\_FIQVEC Register (Offset = 1Ch) [reset = 0h]

The FIQ Vector Address Register contains the 32-bit address of the interrupt vector for the current pending FIQ.

Return to [Summary Table](#)

**Table 4-140. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 001Ch       |
| R5SS1         | 50F0 001Ch       |

**Figure 4-41. VIM1\_FIQVEC Name Register**

|      |    |    |    |    |    |       |    |
|------|----|----|----|----|----|-------|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25    | 24 |
| ADDR |    |    |    |    |    |       |    |
| R/W  |    |    |    |    |    |       |    |
| 0h   |    |    |    |    |    |       |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17    | 16 |
| ADDR |    |    |    |    |    |       |    |
| R/W  |    |    |    |    |    |       |    |
| 0h   |    |    |    |    |    |       |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9     | 8  |
| ADDR |    |    |    |    |    |       |    |
| R/W  |    |    |    |    |    |       |    |
| 0h   |    |    |    |    |    |       |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1     | 0  |
| ADDR |    |    |    |    |    | RES22 |    |
| R/W  |    |    |    |    |    | R     |    |
| 0h   |    |    |    |    |    | 0h    |    |

**Table 4-142. VIM1\_FIQVEC Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                |
|------|-------|------|-------|------------------------------------------------------------------------------------------------------------|
| 31:2 | ADDR  | R/W  | 0h    | Upper 30 bits of the 32-bit vector address. Only valid if the Prioritized FIQ Register valid flag is true. |
| 1:0  | RES22 | R    | 0h    | RESERVE FIELD                                                                                              |



#### 4.1.2.42 VIM1\_ACTIRQ Register

##### 1 VIM1\_ACTIRQ Register (Offset = 20h) [reset = 0h]

The Active IRQ Register shows the number of the currently active IRQ.

Return to [Summary Table](#)

**Table 4-143. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0020h       |
| R5SS1         | 50F0 0020h       |

**Figure 4-42. VIM1\_ACTIRQ Name Register**

|       |      |    |    |     |    |     |    |
|-------|------|----|----|-----|----|-----|----|
| 31    | 30   | 29 | 28 | 27  | 26 | 25  | 24 |
| VALID | RES6 |    |    |     |    |     |    |
| R     | R    |    |    |     |    |     |    |
| 0h    | 0h   |    |    |     |    |     |    |
| 23    | 22   | 21 | 20 | 19  | 18 | 17  | 16 |
| RES6  |      |    |    | PRI |    |     |    |
| R     |      |    |    | R   |    |     |    |
| 0h    |      |    |    | 0h  |    |     |    |
| 15    | 14   | 13 | 12 | 11  | 10 | 9   | 8  |
| RES7  |      |    |    |     |    | NUM |    |
| R     |      |    |    |     |    | R   |    |
| 0h    |      |    |    |     |    | 0h  |    |
| 7     | 6    | 5  | 4  | 3   | 2  | 1   | 0  |
| NUM   |      |    |    |     |    |     |    |
| R     |      |    |    |     |    |     |    |
| 0h    |      |    |    |     |    |     |    |

**Table 4-145. VIM1\_ACTIRQ Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                |
|-------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | VALID | R    | 0h    | Indicates that the num field is valid. Set when the IRQ Vector Address Register is read and cleared whenever the IRQ Vector Address Register is written.   |
| 30:20 | RES6  | R    | 0h    | RESERVE FIELD                                                                                                                                              |
| 19:16 | PRI   | R    | 0h    | Priority of the highest priority pending IRQ. valid only if the valid flag is set.                                                                         |
| 15:10 | RES7  | R    | 0h    | RESERVE FIELD                                                                                                                                              |
| 9:0   | NUM   | R    | 0h    | Number of the currently active IRQ. Loaded from teh Prioritized IRQ Register whenever the IRQ Vector Address is read. Valid only if the valid flag is set. |

#### 4.1.2.43 VIM1\_ACTFIQ Register

##### 1 VIM1\_ACTFIQ Register (Offset = 24h) [reset = 0h]

The Active FIQ Register shows the number of the currently active FIQ.

Return to [Summary Table](#)

**Table 4-146. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0024h       |
| R5SS1         | 50F0 0024h       |

**Figure 4-43. VIM1\_ACTFIQ Name Register**

|       |      |    |    |     |    |     |    |
|-------|------|----|----|-----|----|-----|----|
| 31    | 30   | 29 | 28 | 27  | 26 | 25  | 24 |
| VALID | RES8 |    |    |     |    |     |    |
| R     | R    |    |    |     |    |     |    |
| 0h    | 0h   |    |    |     |    |     |    |
| 23    | 22   | 21 | 20 | 19  | 18 | 17  | 16 |
| RES8  |      |    |    | PRI |    |     |    |
| R     |      |    |    | R   |    |     |    |
| 0h    |      |    |    | 0h  |    |     |    |
| 15    | 14   | 13 | 12 | 11  | 10 | 9   | 8  |
| RES9  |      |    |    |     |    | NUM |    |
| R     |      |    |    |     |    | R   |    |
| 0h    |      |    |    |     |    | 0h  |    |
| 7     | 6    | 5  | 4  | 3   | 2  | 1   | 0  |
| NUM   |      |    |    |     |    |     |    |
| R     |      |    |    |     |    |     |    |
| 0h    |      |    |    |     |    |     |    |

**Table 4-148. VIM1\_ACTFIQ Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                |
|-------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | VALID | R    | 0h    | Indicates that the num field is valid. Set when the FIQ Vector Address Register is read and cleared whenever the FIQ Vector Address Register is written.   |
| 30:20 | RES8  | R    | 0h    | RESERVE FIELD                                                                                                                                              |
| 19:16 | PRI   | R    | 0h    | Priority of the highest priority pending IRQ. valid only if the valid flag is set.                                                                         |
| 15:10 | RES9  | R    | 0h    | RESERVE FIELD                                                                                                                                              |
| 9:0   | NUM   | R    | 0h    | Number of the currently active FIQ. Loaded from teh Prioritized FIQ Register whenever the FIQ Vector Address is read. Valid only if the valid flag is set. |

#### 4.1.2.44 VIM1\_IRQPRIMSK Register

##### 1 VIM1\_IRQPRIMSK Register (Offset = 28h) [reset = FFFFh]

The IRQ Priority Mask Register allows all IRQs of a particular priority to be enabled or disabled.

Return to [Summary Table](#)

**Table 4-149. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0028h       |
| R5SS1         | 50F0 0028h       |

**Figure 4-44. VIM1\_IRQPRIMSK Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RES24 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RES24 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSK   |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSK   |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |

**Table 4-151. VIM1\_IRQPRIMSK Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                |
|-------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RES24 | R    | 0h    | RESERVE FIELD                                                                                                              |
| 15:0  | MSK   | R/W  | FFFFh | Each bit corresponds to the given priority. 1 - IRQs of this priority are enabled. 0 - IRQs of this priority are disabled. |

#### 4.1.2.45 VIM1\_FIQPRIMSK Register

##### 1 VIM1\_FIQPRIMSK Register (Offset = 2Ch) [reset = FFFFh]

The FIQ Priority Mask Register allows all FIQs of a particular priority to be enabled or disabled.

Return to [Summary Table](#)

**Table 4-152. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 002Ch       |
| R5SS1         | 50F0 002Ch       |

**Figure 4-45. VIM1\_FIQPRIMSK Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RES24 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RES24 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSK   |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSK   |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |

**Table 4-154. VIM1\_FIQPRIMSK Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                |
|-------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RES24 | R    | 0h    | RESERVE FIELD                                                                                                              |
| 15:0  | MSK   | R/W  | FFFFh | Each bit corresponds to the given priority. 1 - FIQs of this priority are enabled. 0 - FIQs of this priority are disabled. |

#### 4.1.2.46 VIM1\_DEDVEC Register

##### 1 VIM1\_DEDVEC Register (Offset = 30h) [reset = 0h]

The DED Vector Address contains a default vector address for when an uncorrectable error is detected for an active IRQ or FIQ.

Return to [Summary Table](#)

**Table 4-155. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0030h       |
| R5SS1         | 50F0 0030h       |

**Figure 4-46. VIM1\_DEDVEC Name Register**

|      |    |    |    |    |    |       |    |
|------|----|----|----|----|----|-------|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25    | 24 |
| ADDR |    |    |    |    |    |       |    |
| R/W  |    |    |    |    |    |       |    |
| 0h   |    |    |    |    |    |       |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17    | 16 |
| ADDR |    |    |    |    |    |       |    |
| R/W  |    |    |    |    |    |       |    |
| 0h   |    |    |    |    |    |       |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9     | 8  |
| ADDR |    |    |    |    |    |       |    |
| R/W  |    |    |    |    |    |       |    |
| 0h   |    |    |    |    |    |       |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1     | 0  |
| ADDR |    |    |    |    |    | RES23 |    |
| R/W  |    |    |    |    |    | R     |    |
| 0h   |    |    |    |    |    | 0h    |    |

**Table 4-157. VIM1\_DEDVEC Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                 |
|------|-------|------|-------|---------------------------------------------|
| 31:2 | ADDR  | R/W  | 0h    | Upper 30 bits of the 32-bit vector address. |
| 1:0  | RES23 | R    | 0h    | RESERVE FIELD                               |

#### 4.1.2.47 VIM1\_RAW\_M Register

##### 1 VIM1\_RAW\_M Register (Offset = 400h) [reset = 0h]

Group M Interrupt Raw Status/Set Register (M is 0 to 7) Address formula = 50F00000h + Offset + M x 20h

Return to [Summary Table](#)

**Table 4-158. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0400h       |
| R5SS1         | 50F0 0400h       |

**Figure 4-47. VIM1\_RAW\_M Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| STS |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| STS |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| STS |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| STS |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 4-160. VIM1\_RAW\_M Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                |
|------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | STS   | R/W  | 0h    | This is the raw status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit<br>Read 0 Inactive<br>Read 1 Active/Pending<br>Write 0 No effect<br>Write 1 Set to Interrupt Raw Status |

#### 4.1.2.48 VIM1\_STS\_M Register

##### 1 VIM1\_STS\_M Register (Offset = 404h) [reset = 0h]

Group M Interrupt Enabled Status/Clear Register (M is 0 to 7) Address formula = 50F00000h + Offset + M x 20h

Return to [Summary Table](#)

**Table 4-161. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0404h       |
| R5SS1         | 50F0 0404h       |

**Figure 4-48. VIM1\_STS\_M Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 4-163. VIM1\_STS\_M Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                          |
|------|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MASK  | R/W  | 0h    | This is the masked status of the events in Group M Each bit corresponds to event Q where Q = Mx32+Bit<br>Read 0 Inactive or Disabled<br>Read 1 Active/Pending and Enabled<br>Write 0 No effect<br>Write 1 Clear Interrupt Raw Status |

#### 4.1.2.49 VIM1\_INTR\_EN\_SET\_M Register

##### 1 VIM1\_INTR\_EN\_SET\_M Register (Offset = 408h) [reset = 0h]

Group M Interrupt Enabled Set Register (M is 0 to 7) Address formula = 50F00000h + Offset + M x 20h

Return to [Summary Table](#)

**Table 4-164. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0408h       |
| R5SS1         | 50F0 0408h       |

**Figure 4-49. VIM1\_INTR\_EN\_SET\_M Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 4-166. VIM1\_INTR\_EN\_SET\_M Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                   |
|------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MASK  | R/W  | 0h    | This field is used to enable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+Bit<br>Read 0 Disabled<br>Read 1 Enabled<br>Write 0 No effect<br>Write 1 Set Enable |



#### 4.1.2.50 VIM1\_INTER\_EN\_CLR\_M Register

##### 1 VIM1\_INTER\_EN\_CLR\_M Register (Offset = 40Ch) [reset = 0h]

Group M Interrupt Enabled Clear Register (M is 0 to 7) Address formula = 50F00000h + Offset + M x 20h

Return to [Summary Table](#)

**Table 4-167. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 040Ch       |
| R5SS1         | 50F0 040Ch       |

**Figure 4-50. VIM1\_INTER\_EN\_CLR\_M Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 4-169. VIM1\_INTER\_EN\_CLR\_M Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                      |
|------|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MASK  | R/W  | 0h    | This field is used to disable the mask of events in Group M Each bit corresponds to event Q where Q = Mx32+Bit<br>Read 0 Disabled<br>Read 1 Enabled<br>Write 0 No effect<br>Write 1 Clear Enable |

#### 4.1.2.51 VIM1\_IRQSTS\_M Register

##### 1 VIM1\_IRQSTS\_M Register (Offset = 410h) [reset = 0h]

Group M Interrupt IRQ Enabled Status/Clear Register (M is 0 to 7) Address formula = 50F00000h + Offset + M x 20h

Return to [Summary Table](#)

**Table 4-170. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0410h       |
| R5SS1         | 50F0 0410h       |

**Figure 4-51. VIM1\_IRQSTS\_M Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 4-172. VIM1\_IRQSTS\_M Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                   |
|------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MASK  | R/W  | 0h    | This is the masked status of the events in group M that are mapped to IRQ. Each bit corresponds to event Q where Q = Mx32+Bit.<br>Read 0 Inactive, Disabled, or not an IRQ.<br>Read 1 Active/Pending, Enabled, and IRQ.<br>Write 0 No effect.<br>Write 1 Clear Interrupt Raw Status [if IRQ]. |

#### 4.1.2.52 VIM1\_FIQSTS\_M Register

##### 1 VIM1\_FIQSTS\_M Register (Offset = 414h) [reset = 0h]

Group M Interrupt FIQ Enabled Status/Clear Register (M is 0 to 7) Address formula = 50F00000h + Offset + M x 20h

Return to [Summary Table](#)

**Table 4-173. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0414h       |
| R5SS1         | 50F0 0414h       |

**Figure 4-52. VIM1\_FIQSTS\_M Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 4-175. VIM1\_FIQSTS\_M Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                             |
|------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MASK  | R/W  | 0h    | This is the masked status of the events in group M that are mapped to FIQ Each bit corresponds to event Q where Q = Mx32+Bit<br>Read 0 Inactive, Disabled, or not an FIQ<br>Read 1 Active/Pending, Enabled, and FIQ<br>Write 0 No effect<br>Write 1 Clear Interrupt Raw Status [if FIQ] |

#### 4.1.2.53 VIM1\_INTMAP\_M Register

##### 1 VIM1\_INTMAP\_M Register (Offset = 418h) [reset = 0h]

Group M Interrupt Map Register (M is 0 to 7) Address formula = 50F00000h + Offset + M x 20h

Return to [Summary Table](#)

**Table 4-176. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 0418h       |
| R5SS1         | 50F0 0418h       |

**Figure 4-53. VIM1\_INTMAP\_M Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MASK |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 4-178. VIM1\_INTMAP\_M Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                          |
|------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MASK  | R/W  | 0h    | This field is used to indicate which interrupt the corresponding event influences [if enabled] for event group M. Each bit corresponds to event Q where Q = Mx32+Bit<br>0 IRQ Interrupt [default]<br>1 FIQ Interrupt |

#### 4.1.2.54 VIM1\_INTTYPE\_M Register

##### 1 VIM1\_INTTYPE\_M Register (Offset = 41Ch) [reset = 0h]

Group M Interrupt Type Map Register (M is 0 to 7) Address formula = 50F00000h + Offset + M x 20h

Return to [Summary Table](#)

**Table 4-179. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 041Ch       |
| R5SS1         | 50F0 041Ch       |

**Figure 4-54. VIM1\_INTTYPE\_M Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| VAL |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| VAL |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| VAL |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| VAL |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 4-181. VIM1\_INTTYPE\_M Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | VAL   | R/W  | 0h    | This field is used to indicate whether the source of an interrupt is a level [default] or a pulse for event group M. This is informational so that an ISR may query this register and know whether it has to clear a pulse event or a level event [see 3.4 Interrupt Handling]. The value has no effect on how the VIM hardware functions. The input interrupts are agnostic as to whether they are pulse or level. Each bit corresponds to event Q where Q = Mx32+Bit<br>0 Level [default]<br>1 Pulse |

#### 4.1.2.55 VIM1\_INTPRIORITY\_Q Register

##### 1 VIM1\_INTPRIORITY\_Q Register (Offset = 1000h) [reset = Fh]

Interrupt Q Priority Register (where Q is 0 to 255) Address formula = 50F00000h + Offset + Q x 4h

Return to [Summary Table](#)

**Table 4-182. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 1000h       |
| R5SS1         | 50F0 1000h       |

**Figure 4-55. VIM1\_INTPRIORITY\_Q Name Register**

|       |    |    |    |     |    |    |    |
|-------|----|----|----|-----|----|----|----|
| 31    | 30 | 29 | 28 | 27  | 26 | 25 | 24 |
| RES19 |    |    |    |     |    |    |    |
| R     |    |    |    |     |    |    |    |
| 0h    |    |    |    |     |    |    |    |
| 23    | 22 | 21 | 20 | 19  | 18 | 17 | 16 |
| RES19 |    |    |    |     |    |    |    |
| R     |    |    |    |     |    |    |    |
| 0h    |    |    |    |     |    |    |    |
| 15    | 14 | 13 | 12 | 11  | 10 | 9  | 8  |
| RES19 |    |    |    |     |    |    |    |
| R     |    |    |    |     |    |    |    |
| 0h    |    |    |    |     |    |    |    |
| 7     | 6  | 5  | 4  | 3   | 2  | 1  | 0  |
| RES19 |    |    |    | PRI |    |    |    |
| R     |    |    |    | R/W |    |    |    |
| 0h    |    |    |    | Fh  |    |    |    |

**Table 4-184. VIM1\_INTPRIORITY\_Q Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                            |
|------|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RES19 | R    | 0h    | RESERVE FIELD                                                                                                                                                                                          |
| 3:0  | PRI   | R/W  | Fh    | This is the priority for interrupt Q. If two interrupts have the same priority, then whichever interrupt has the lower number Q wins arbitration<br>0 Highest Priority<br>15 Lowest Priority [Default] |

#### 4.1.2.56 VIM1\_INTVECTOR\_Q Register

##### 1 VIM1\_INTVECTOR\_Q Register (Offset = 2000h) [reset = 0h]

Interrupt Q Vector Register (Q is 0 to 255) Address formula = 50F00000h + Offset + Q x 4h

Return to [Summary Table](#)

**Table 4-185. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 50F0 2000h       |
| R5SS1         | 50F0 2000h       |

**Figure 4-56. VIM1\_INTVECTOR\_Q Name Register**

|      |    |    |    |    |    |       |    |
|------|----|----|----|----|----|-------|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25    | 24 |
| ADDR |    |    |    |    |    |       |    |
| R/W  |    |    |    |    |    |       |    |
| 0h   |    |    |    |    |    |       |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17    | 16 |
| ADDR |    |    |    |    |    |       |    |
| R/W  |    |    |    |    |    |       |    |
| 0h   |    |    |    |    |    |       |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9     | 8  |
| ADDR |    |    |    |    |    |       |    |
| R/W  |    |    |    |    |    |       |    |
| 0h   |    |    |    |    |    |       |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1     | 0  |
| ADDR |    |    |    |    |    | RES20 |    |
| R/W  |    |    |    |    |    | R     |    |
| 0h   |    |    |    |    |    | 0h    |    |

**Table 4-187. VIM1\_INTVECTOR\_Q Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | ADDR  | R/W  | 0h    | This is the 32-bit Vector Address associated with interrupt Q. It is the address that will be reflected in the IRQ Vector Address [Base Address + 0x18] or FIQ Vector Address [Base Address + 0x1C] and the VECADDR pin when interrupt Q is the active interrupt. Internally, these values are kept in a RAM. The FIQ and IRQ state machines have priority access to this RAM. Writes to this register will be piped internally, but further writes to the MMR interface may be stalled until this write has a chance to complete in the RAM. The new Vector Address will not take effect until this write completes to the RAM. In order to tell if this write has completed, software may read this register back. That read will not be able to complete unless the write has landed. Reads to this register will stall the MMR interface until the read is able to be completed at the RAM. |
| 1:0  | RES20 | R    | 0h    | Reserved. Read as 0. The lower 2 bits of the 32-bit vector address are always 0. Vector addresses must be 32-bit aligned.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

#### 4.1.2.57 ECC\_AGG\_CORE0\_AGGR\_REVISION Register

##### 1 ECC\_AGG\_CORE0\_AGGR\_REVISION Register (Offset = 0h) [reset = 66A0C200h]

The Revision Register contains the major and minor revisions for the ECC aggregator module. It does not support byte accesses.

Return to [Summary Table](#)

**Table 4-188. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 0000h       |
| R5SS1         | 5300 4000h       |

**Figure 4-57. ECC\_AGG\_CORE0\_AGGR\_REVISION Name Register**

|           |    |        |    |           |        |    |    |
|-----------|----|--------|----|-----------|--------|----|----|
| 31        | 30 | 29     | 28 | 27        | 26     | 25 | 24 |
| SCHEME    |    | BU     |    | MODULE_ID |        |    |    |
| R         |    | R      |    | R         |        |    |    |
| 1h        |    | 2h     |    | 6A0h      |        |    |    |
| 23        | 22 | 21     | 20 | 19        | 18     | 17 | 16 |
| MODULE_ID |    |        |    |           |        |    |    |
| R         |    |        |    |           |        |    |    |
| 6A0h      |    |        |    |           |        |    |    |
| 15        | 14 | 13     | 12 | 11        | 10     | 9  | 8  |
| REVRTL    |    |        |    |           | REVMAJ |    |    |
| R         |    |        |    |           | R      |    |    |
| 18h       |    |        |    |           | 2h     |    |    |
| 7         | 6  | 5      | 4  | 3         | 2      | 1  | 0  |
| CUSTOM    |    | REVMIN |    |           |        |    |    |
| R         |    | R      |    |           |        |    |    |
| 0h        |    | 0h     |    |           |        |    |    |

**Table 4-190. ECC\_AGG\_CORE0\_AGGR\_REVISION Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description    |
|-------|-----------|------|-------|----------------|
| 31:30 | SCHEME    | R    | 1h    | Scheme         |
| 29:28 | BU        | R    | 2h    | Business unit  |
| 27:16 | MODULE_ID | R    | 6A0h  | Module ID      |
| 15:11 | REVRTL    | R    | 18h   | RTL version    |
| 10:8  | REVMAJ    | R    | 2h    | Major version  |
| 7:6   | CUSTOM    | R    | 0h    | Custom version |
| 5:0   | REVMIN    | R    | 0h    | Minor version  |



#### 4.1.2.58 ECC\_AGG\_CORE0\_ECC\_VECTOR Register

##### 1 ECC\_AGG\_CORE0\_ECC\_VECTOR Register (Offset = 8h) [reset = 0h]

ECC RAM ID to select which ECC RAM to control or read status from.

Return to [Summary Table](#)

**Table 4-191. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 0008h       |
| R5SS1         | 5300 4008h       |

**Figure 4-58. ECC\_AGG\_CORE0\_ECC\_VECTOR Name Register**

|                  |          |    |    |    |            |    |                   |
|------------------|----------|----|----|----|------------|----|-------------------|
| 31               | 30       | 29 | 28 | 27 | 26         | 25 | 24                |
| RESERVED         |          |    |    |    |            |    | RD_SVBUS_D<br>ONE |
| NONE             |          |    |    |    |            |    | R                 |
| 0h               |          |    |    |    |            |    | 0h                |
| 23               | 22       | 21 | 20 | 19 | 18         | 17 | 16                |
| RD_SVBUS_ADDRESS |          |    |    |    |            |    |                   |
| R/W              |          |    |    |    |            |    |                   |
| 0h               |          |    |    |    |            |    |                   |
| 15               | 14       | 13 | 12 | 11 | 10         | 9  | 8                 |
| RD_SVBUS         | RESERVED |    |    |    | ECC_VECTOR |    |                   |
| R/W1TS           | NONE     |    |    |    | R/W        |    |                   |
| 0h               | 0h       |    |    |    | 0h         |    |                   |
| 7                | 6        | 5  | 4  | 3  | 2          | 1  | 0                 |
| ECC_VECTOR       |          |    |    |    |            |    |                   |
| R/W              |          |    |    |    |            |    |                   |
| 0h               |          |    |    |    |            |    |                   |

**Table 4-193. ECC\_AGG\_CORE0\_ECC\_VECTOR Register Field Descriptions**

| Bit   | Field            | Type   | Reset | Description                                                             |
|-------|------------------|--------|-------|-------------------------------------------------------------------------|
| 31:25 | RESERVED         | NONE   | 0h    | Reserved                                                                |
| 24    | RD_SVBUS_DONE    | R      | 0h    | Status to indicate if read on serial VBUS is complete                   |
| 23:16 | RD_SVBUS_ADDRESS | R/W    | 0h    | Read address                                                            |
| 15    | RD_SVBUS         | R/W1TS | 0h    | Write 1 to trigger a read on the serial VBUS                            |
| 14:11 | RESERVED         | NONE   | 0h    | Reserved                                                                |
| 10:0  | ECC_VECTOR       | R/W    | 0h    | Value written to select the corresponding ECC RAM for control or status |

#### 4.1.2.59 ECC\_AGG\_CORE0\_MISC\_STATUS Register

##### 1 ECC\_AGG\_CORE0\_MISC\_STATUS Register (Offset = Ch) [reset = 1Ch]

Contains misc status such as number of ECC RAMs serviced by the ECC aggregator.

Return to [Summary Table](#)

**Table 4-194. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 000Ch       |
| R5SS1         | 5300 400Ch       |

**Figure 4-59. ECC\_AGG\_CORE0\_MISC\_STATUS Name Register**

|          |    |    |    |    |          |    |    |
|----------|----|----|----|----|----------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26       | 25 | 24 |
| RESERVED |    |    |    |    |          |    |    |
| NONE     |    |    |    |    |          |    |    |
| 0h       |    |    |    |    |          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18       | 17 | 16 |
| RESERVED |    |    |    |    |          |    |    |
| NONE     |    |    |    |    |          |    |    |
| 0h       |    |    |    |    |          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10       | 9  | 8  |
| RESERVED |    |    |    |    | NUM_RAMs |    |    |
| NONE     |    |    |    |    | R        |    |    |
| 0h       |    |    |    |    | 1Ch      |    |    |
| 7        | 6  | 5  | 4  | 3  | 2        | 1  | 0  |
| NUM_RAMs |    |    |    |    |          |    |    |
| R        |    |    |    |    |          |    |    |
| 1Ch      |    |    |    |    |          |    |    |

**Table 4-196. ECC\_AGG\_CORE0\_MISC\_STATUS Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                 |
|-------|----------|------|-------|-------------------------------------------------------------|
| 31:11 | RESERVED | NONE | 0h    | Reserved                                                    |
| 10:0  | NUM_RAMs | R    | 1Ch   | Indicates the number of RAMs serviced by the ECC aggregator |

#### 4.1.2.60 ECC\_AGG\_CORE0\_ECC\_WRAP\_REVISION Register

##### 1 ECC\_AGG\_CORE0\_ECC\_WRAP\_REVISION Register (Offset = 10h) [reset = 66A40202h]

Revision parameters.

Return to [Summary Table](#)

**Table 4-197. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 0010h       |
| R5SS1         | 5300 4010h       |

**Figure 4-60. ECC\_AGG\_CORE0\_ECC\_WRAP\_REVISION Name Register**

|           |    |        |    |           |        |    |    |
|-----------|----|--------|----|-----------|--------|----|----|
| 31        | 30 | 29     | 28 | 27        | 26     | 25 | 24 |
| SCHEME    |    | BU     |    | MODULE_ID |        |    |    |
| R         |    | R      |    | R         |        |    |    |
| 1h        |    | 2h     |    | 6A4h      |        |    |    |
| 23        | 22 | 21     | 20 | 19        | 18     | 17 | 16 |
| MODULE_ID |    |        |    |           |        |    |    |
| R         |    |        |    |           |        |    |    |
| 6A4h      |    |        |    |           |        |    |    |
| 15        | 14 | 13     | 12 | 11        | 10     | 9  | 8  |
| REVRTL    |    |        |    |           | REVMaj |    |    |
| R         |    |        |    |           | R      |    |    |
| 0h        |    |        |    |           | 2h     |    |    |
| 7         | 6  | 5      | 4  | 3         | 2      | 1  | 0  |
| CUSTOM    |    | REVMIN |    |           |        |    |    |
| R         |    | R      |    |           |        |    |    |
| 0h        |    | 2h     |    |           |        |    |    |

**Table 4-199. ECC\_AGG\_CORE0\_ECC\_WRAP\_REVISION Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description    |
|-------|-----------|------|-------|----------------|
| 31:30 | SCHEME    | R    | 1h    | Scheme         |
| 29:28 | BU        | R    | 2h    | Business unit  |
| 27:16 | MODULE_ID | R    | 6A4h  | Module ID      |
| 15:11 | REVRTL    | R    | 0h    | RTL version    |
| 10:8  | REVMaj    | R    | 2h    | Major version  |
| 7:6   | CUSTOM    | R    | 0h    | Custom version |
| 5:0   | REVMIN    | R    | 2h    | Minor version  |

#### 4.1.2.61 ECC\_AGG\_CORE0\_CONTROL Register

##### 1 ECC\_AGG\_CORE0\_CONTROL Register (Offset = 14h) [reset = 187h]

ECC Control Register.

Return to [Summary Table](#)

**Table 4-200. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 0014h       |
| R5SS1         | 5300 4014h       |

**Figure 4-61. ECC\_AGG\_CORE0\_CONTROL Name Register**

|              |            |             |           |           |            |           |                     |
|--------------|------------|-------------|-----------|-----------|------------|-----------|---------------------|
| 31           | 30         | 29          | 28        | 27        | 26         | 25        | 24                  |
| RESERVED     |            |             |           |           |            |           |                     |
| NONE         |            |             |           |           |            |           |                     |
| 0h           |            |             |           |           |            |           |                     |
| 23           | 22         | 21          | 20        | 19        | 18         | 17        | 16                  |
| RESERVED     |            |             |           |           |            |           |                     |
| NONE         |            |             |           |           |            |           |                     |
| 0h           |            |             |           |           |            |           |                     |
| 15           | 14         | 13          | 12        | 11        | 10         | 9         | 8                   |
| RESERVED     |            |             |           |           |            |           | CHECK_SVBUS_TIMEOUT |
| NONE         |            |             |           |           |            |           | R/W                 |
| 0h           |            |             |           |           |            |           | 1h                  |
| 7            | 6          | 5           | 4         | 3         | 2          | 1         | 0                   |
| CHECK_PARITY | ERROR_ONCE | FORCE_N_ROW | FORCE_DED | FORCE_SEC | ENABLE_RMW | ECC_CHECK | ECC_ENABLE          |
| R/W          | R/W        | R/W         | R/W       | R/W       | R/W        | R/W       | R/W                 |
| 1h           | 0h         | 0h          | 0h        | 0h        | 1h         | 1h        | 1h                  |

**Table 4-202. ECC\_AGG\_CORE0\_CONTROL Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                    |
|------|---------------------|------|-------|--------------------------------|
| 31:9 | RESERVED            | NONE | 0h    | Reserved                       |
| 8    | CHECK_SVBUS_TIMEOUT | R/W  | 1h    | check for svbus timeout errors |
| 7    | CHECK_PARITY        | R/W  | 1h    | check for parity errors        |
| 6    | ERROR_ONCE          | R/W  | 0h    | Force Error only once          |
| 5    | FORCE_N_ROW         | R/W  | 0h    | Force Error on any RAM read    |
| 4    | FORCE_DED           | R/W  | 0h    | Force Double Bit Error         |
| 3    | FORCE_SEC           | R/W  | 0h    | Force Single Bit Error         |
| 2    | ENABLE_RMW          | R/W  | 1h    | Enable rmw                     |
| 1    | ECC_CHECK           | R/W  | 1h    | Enable ECC check               |
| 0    | ECC_ENABLE          | R/W  | 1h    | Enable ECC                     |

#### 4.1.2.62 ECC\_AGG\_CORE0\_ERROR\_CTRL1 Register

##### 1 ECC\_AGG\_CORE0\_ERROR\_CTRL1 Register (Offset = 18h) [reset = 0h]

ECC Error Control1 Register.

Return to [Summary Table](#)

**Table 4-203. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 0018h       |
| R5SS1         | 5300 4018h       |

**Figure 4-62. ECC\_AGG\_CORE0\_ERROR\_CTRL1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ECC_ROW |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ECC_ROW |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ECC_ROW |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ECC_ROW |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-205. ECC\_AGG\_CORE0\_ERROR\_CTRL1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                             |
|------|---------|------|-------|---------------------------------------------------------------------------------------------------------|
| 31:0 | ECC_ROW | R/W  | 0h    | Row address where single or double-bit error needs to be applied. This is ignored if force_n_row is set |

#### 4.1.2.63 ECC\_AGG\_CORE0\_ERROR\_CTRL2 Register

##### 1 ECC\_AGG\_CORE0\_ERROR\_CTRL2 Register (Offset = 1Ch) [reset = 0h]

ECC Error Control2 Register.

Return to [Summary Table](#)

**Table 4-206. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 001Ch       |
| R5SS1         | 5300 401Ch       |

**Figure 4-63. ECC\_AGG\_CORE0\_ERROR\_CTRL2 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ECC_BIT2 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ECC_BIT2 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ECC_BIT1 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ECC_BIT1 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-208. ECC\_AGG\_CORE0\_ERROR\_CTRL2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                              |
|-------|----------|------|-------|--------------------------------------------------------------------------|
| 31:16 | ECC_BIT2 | R/W  | 0h    | Data bit that needs to be flipped if double bit error needs to be forced |
| 15:0  | ECC_BIT1 | R/W  | 0h    | Data bit that needs to be flipped when force_sec is set                  |

#### 4.1.2.64 ECC\_AGG\_CORE0\_ERROR\_STATUS1 Register

##### 1 ECC\_AGG\_CORE0\_ERROR\_STATUS1 Register (Offset = 20h) [reset = 0h]

ECC Error Status1 Register.

Return to [Summary Table](#)

**Table 4-209. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 0020h       |
| R5SS1         | 5300 4020h       |

**Figure 4-64. ECC\_AGG\_CORE0\_ERROR\_STATUS1 Name Register**

|                  |                |    |               |             |    |             |    |
|------------------|----------------|----|---------------|-------------|----|-------------|----|
| 31               | 30             | 29 | 28            | 27          | 26 | 25          | 24 |
| ECC_BIT1         |                |    |               |             |    |             |    |
| R                |                |    |               |             |    |             |    |
| 0h               |                |    |               |             |    |             |    |
| 23               | 22             | 21 | 20            | 19          | 18 | 17          | 16 |
| ECC_BIT1         |                |    |               |             |    |             |    |
| R                |                |    |               |             |    |             |    |
| 0h               |                |    |               |             |    |             |    |
| 15               | 14             | 13 | 12            | 11          | 10 | 9           | 8  |
| CLR_CTRL_REG_ERR | CLR_PARITY_ERR |    | CLR_ECC_OTHER | CLR_ECC_DED |    | CLR_ECC_SEC |    |
| R/W1TC           | R/WD           |    | R/W1TC        | R/WD        |    | R/WD        |    |
| 0h               | 0h             |    | 0h            | 0h          |    | 0h          |    |
| 7                | 6              | 5  | 4             | 3           | 2  | 1           | 0  |
| CTR_REG_ERR      | PARITY_ERR     |    | ECC_OTHER     | ECC_DED     |    | ECC_SEC     |    |
| R/W1TS           | R/W1TS         |    | R/W1TS        | R/WI        |    | R/WI        |    |
| 0h               | 0h             |    | 0h            | 0h          |    | 0h          |    |

**Table 4-211. ECC\_AGG\_CORE0\_ERROR\_STATUS1 Register Field Descriptions**

| Bit   | Field            | Type   | Reset | Description                                                                                      |
|-------|------------------|--------|-------|--------------------------------------------------------------------------------------------------|
| 31:16 | ECC_BIT1         | R      | 0h    | Data bit that corresponds to the single-bit error                                                |
| 15    | CLR_CTRL_REG_ERR | R/W1TC | 0h    | Clear control reg Error Status, you must also re write the control register itself to clear this |
| 14:13 | CLR_PARITY_ERR   | R/WD   | 0h    | Clear parity Error Status                                                                        |
| 12    | CLR_ECC_OTHER    | R/W1TC | 0h    | Clear other Error Status                                                                         |
| 11:10 | CLR_ECC_DED      | R/WD   | 0h    | Clear Double Bit Error Status                                                                    |
| 9:8   | CLR_ECC_SEC      | R/WD   | 0h    | Clear Single Bit Error Status                                                                    |
| 7     | CTR_REG_ERR      | R/W1TS | 0h    | control register error pending, Level interrupt                                                  |
| 6:5   | PARITY_ERR       | R/W1TS | 0h    | Level parity error Error Status                                                                  |
| 4     | ECC_OTHER        | R/W1TS | 0h    | Successive single-bit errors have occurred while a writeback is still pending, Level interrupt   |
| 3:2   | ECC_DED          | R/WI   | 0h    | Level Double Bit Error Status                                                                    |
| 1:0   | ECC_SEC          | R/WI   | 0h    | Level Single Bit Error Status                                                                    |

#### 4.1.2.65 ECC\_AGG\_CORE0\_ERROR\_STATUS2 Register

##### 1 ECC\_AGG\_CORE0\_ERROR\_STATUS2 Register (Offset = 24h) [reset = 0h]

ECC Error Status2 Register.

Return to [Summary Table](#)

**Table 4-212. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 0024h       |
| R5SS1         | 5300 4024h       |

**Figure 4-65. ECC\_AGG\_CORE0\_ERROR\_STATUS2 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ECC_ROW |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ECC_ROW |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ECC_ROW |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ECC_ROW |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-214. ECC\_AGG\_CORE0\_ERROR\_STATUS2 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                   |
|------|---------|------|-------|---------------------------------------------------------------|
| 31:0 | ECC_ROW | R    | 0h    | Row address where the single or double-bit error has occurred |



#### 4.1.2.66 ECC\_AGG\_CORE0\_ERROR\_STATUS3 Register

##### 1 ECC\_AGG\_CORE0\_ERROR\_STATUS3 Register (Offset = 28h) [reset = 0h]

ECC Error Status3 Register.

Return to [Summary Table](#)

**Table 4-215. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 0028h       |
| R5SS1         | 5300 4028h       |

**Figure 4-66. ECC\_AGG\_CORE0\_ERROR\_STATUS3 Name Register**

|          |    |    |    |    |    |                       |          |
|----------|----|----|----|----|----|-----------------------|----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25                    | 24       |
| RESERVED |    |    |    |    |    |                       |          |
| NONE     |    |    |    |    |    |                       |          |
| 0h       |    |    |    |    |    |                       |          |
| 23       | 22 | 21 | 20 | 19 | 18 | 17                    | 16       |
| RESERVED |    |    |    |    |    |                       |          |
| NONE     |    |    |    |    |    |                       |          |
| 0h       |    |    |    |    |    |                       |          |
| 15       | 14 | 13 | 12 | 11 | 10 | 9                     | 8        |
| RESERVED |    |    |    |    |    | CLR_SVBUS_TIMEOUT_ERR | RESERVED |
| NONE     |    |    |    |    |    | R/W1TC                | NONE     |
| 0h       |    |    |    |    |    | 0h                    | 0h       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1                     | 0        |
| RESERVED |    |    |    |    |    | SVBUS_TIMEOUT_ERR     | WB_PEND  |
| NONE     |    |    |    |    |    | R/W1TS                | R        |
| 0h       |    |    |    |    |    | 0h                    | 0h       |

**Table 4-217. ECC\_AGG\_CORE0\_ERROR\_STATUS3 Register Field Descriptions**

| Bit   | Field                 | Type   | Reset | Description                            |
|-------|-----------------------|--------|-------|----------------------------------------|
| 31:10 | RESERVED              | NONE   | 0h    | Reserved                               |
| 9     | CLR_SVBUS_TIMEOUT_ERR | R/W1TC | 0h    | Clear svbus timeout Error Status       |
| 8:2   | RESERVED              | NONE   | 0h    | Reserved                               |
| 1     | SVBUS_TIMEOUT_ERR     | R/W1TS | 0h    | Level svbus timeout error Error Status |
| 0     | WB_PEND               | R      | 0h    | delayed write back pending Status      |

#### 4.1.2.67 ECC\_AGG\_CORE0\_SEC\_EOI\_REG Register

##### 1 ECC\_AGG\_CORE0\_SEC\_EOI\_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register.

Return to [Summary Table](#)

**Table 4-218. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 003Ch       |
| R5SS1         | 5300 403Ch       |

**Figure 4-67. ECC\_AGG\_CORE0\_SEC\_EOI\_REG Name Register**

|          |    |    |    |    |    |    |        |
|----------|----|----|----|----|----|----|--------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24     |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16     |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8      |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0      |
| RESERVED |    |    |    |    |    |    | EOI_WR |
| NONE     |    |    |    |    |    |    | R/W1TS |
| 0h       |    |    |    |    |    |    | 0h     |

**Table 4-220. ECC\_AGG\_CORE0\_SEC\_EOI\_REG Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description                                                                                                                                                                                     |
|------|----------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED | NONE   | 0h    | Reserved                                                                                                                                                                                        |
| 0    | EOI_WR   | R/W1TS | 0h    | Write of 1 to this register indicates that software has acknowledged the pending interrupt and the next interrupt can be sent to the host. The bit is self clearing and will be read as a zero. |

#### 4.1.2.68 ECC\_AGG\_CORE0\_SEC\_STATUS\_REG0 Register

##### 1 ECC\_AGG\_CORE0\_SEC\_STATUS\_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

Return to [Summary Table](#)

**Table 4-221. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 0040h       |
| R5SS1         | 5300 4040h       |

**Figure 4-68. ECC\_AGG\_CORE0\_SEC\_STATUS\_REG0 Name Register**

| 31                    | 30                    | 29                    | 28                    | 27                      | 26                   | 25                   | 24                   |
|-----------------------|-----------------------|-----------------------|-----------------------|-------------------------|----------------------|----------------------|----------------------|
| RESERVED              |                       |                       |                       | CPU0_KS_VIM_RAMECC_PEND | B1TCM0_BANK1_PEND    | B1TCM0_BANK0_PEND    | B0TCM0_BANK1_PEND    |
| NONE                  |                       |                       |                       | R/W1TS                  | R/W1TS               | R/W1TS               | R/W1TS               |
| 0h                    |                       |                       |                       | 0h                      | 0h                   | 0h                   | 0h                   |
| 23                    | 22                    | 21                    | 20                    | 19                      | 18                   | 17                   | 16                   |
| B0TCM0_BANK0_PEND     | ATCM0_BANK1_PEND      | ATCM0_BANK0_PEND      | CPU0_DDATA_RAM7_PEND  | CPU0_DDATA_RAM6_PEND    | CPU0_DDATA_RAM5_PEND | CPU0_DDATA_RAM4_PEND | CPU0_DDATA_RAM3_PEND |
| R/W1TS                | R/W1TS                | R/W1TS                | R/W1TS                | R/W1TS                  | R/W1TS               | R/W1TS               | R/W1TS               |
| 0h                    | 0h                    | 0h                    | 0h                    | 0h                      | 0h                   | 0h                   | 0h                   |
| 15                    | 14                    | 13                    | 12                    | 11                      | 10                   | 9                    | 8                    |
| CPU0_DDATA_RAM2_PEND  | CPU0_DDATA_RAM1_PEND  | CPU0_DDATA_RAM0_PEND  | CPU0_DDIRTY_RAM_PEND  | CPU0_DTAG_RAM3_PEND     | CPU0_DTAG_RAM2_PEND  | CPU0_DTAG_RAM1_PEND  | CPU0_DTAG_RAM0_PEND  |
| R/W1TS                | R/W1TS                | R/W1TS                | R/W1TS                | R/W1TS                  | R/W1TS               | R/W1TS               | R/W1TS               |
| 0h                    | 0h                    | 0h                    | 0h                    | 0h                      | 0h                   | 0h                   | 0h                   |
| 7                     | 6                     | 5                     | 4                     | 3                       | 2                    | 1                    | 0                    |
| CPU0_IDATA_BANK3_PEND | CPU0_IDATA_BANK2_PEND | CPU0_IDATA_BANK1_PEND | CPU0_IDATA_BANK0_PEND | CPU0_ITAG_RAM3_PEND     | CPU0_ITAG_RAM2_PEND  | CPU0_ITAG_RAM1_PEND  | CPU0_ITAG_RAM0_PEND  |
| R/W1TS                | R/W1TS                | R/W1TS                | R/W1TS                | R/W1TS                  | R/W1TS               | R/W1TS               | R/W1TS               |
| 0h                    | 0h                    | 0h                    | 0h                    | 0h                      | 0h                   | 0h                   | 0h                   |

**Table 4-223. ECC\_AGG\_CORE0\_SEC\_STATUS\_REG0 Register Field Descriptions**

| Bit   | Field                   | Type   | Reset | Description                                          |
|-------|-------------------------|--------|-------|------------------------------------------------------|
| 31:28 | RESERVED                | NONE   | 0h    | Reserved                                             |
| 27    | CPU0_KS_VIM_RAMECC_PEND | R/W1TS | 0h    | Interrupt Pending Status for cpu0_ks_vim_ramecc_pend |
| 26    | B1TCM0_BANK1_PEND       | R/W1TS | 0h    | Interrupt Pending Status for b1tcm0_bank1_pend       |
| 25    | B1TCM0_BANK0_PEND       | R/W1TS | 0h    | Interrupt Pending Status for b1tcm0_bank0_pend       |
| 24    | B0TCM0_BANK1_PEND       | R/W1TS | 0h    | Interrupt Pending Status for b0tcm0_bank1_pend       |
| 23    | B0TCM0_BANK0_PEND       | R/W1TS | 0h    | Interrupt Pending Status for b0tcm0_bank0_pend       |
| 22    | ATCM0_BANK1_PEND        | R/W1TS | 0h    | Interrupt Pending Status for atcm0_bank1_pend        |
| 21    | ATCM0_BANK0_PEND        | R/W1TS | 0h    | Interrupt Pending Status for atcm0_bank0_pend        |
| 20    | CPU0_DDATA_RAM7_PEND    | R/W1TS | 0h    | Interrupt Pending Status for cpu0_ddata_ram7_pend    |
| 19    | CPU0_DDATA_RAM6_PEND    | R/W1TS | 0h    | Interrupt Pending Status for cpu0_ddata_ram6_pend    |
| 18    | CPU0_DDATA_RAM5_PEND    | R/W1TS | 0h    | Interrupt Pending Status for cpu0_ddata_ram5_pend    |

**Table 4-223. ECC\_AGG\_CORE0\_SEC\_STATUS\_REG0 Register Field Descriptions (continued)**

| Bit | Field                 | Type   | Reset | Description                                        |
|-----|-----------------------|--------|-------|----------------------------------------------------|
| 17  | CPU0_DDATA_RAM4_PEND  | R/W1TS | 0h    | Interrupt Pending Status for cpu0_ddata_ram4_pend  |
| 16  | CPU0_DDATA_RAM3_PEND  | R/W1TS | 0h    | Interrupt Pending Status for cpu0_ddata_ram3_pend  |
| 15  | CPU0_DDATA_RAM2_PEND  | R/W1TS | 0h    | Interrupt Pending Status for cpu0_ddata_ram2_pend  |
| 14  | CPU0_DDATA_RAM1_PEND  | R/W1TS | 0h    | Interrupt Pending Status for cpu0_ddata_ram1_pend  |
| 13  | CPU0_DDATA_RAM0_PEND  | R/W1TS | 0h    | Interrupt Pending Status for cpu0_ddata_ram0_pend  |
| 12  | CPU0_DDIRTY_RAM_PEND  | R/W1TS | 0h    | Interrupt Pending Status for cpu0_ddirty_ram_pend  |
| 11  | CPU0_DTAG_RAM3_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu0_dtag_ram3_pend   |
| 10  | CPU0_DTAG_RAM2_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu0_dtag_ram2_pend   |
| 9   | CPU0_DTAG_RAM1_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu0_dtag_ram1_pend   |
| 8   | CPU0_DTAG_RAM0_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu0_dtag_ram0_pend   |
| 7   | CPU0_IDATA_BANK3_PEND | R/W1TS | 0h    | Interrupt Pending Status for cpu0_idata_bank3_pend |
| 6   | CPU0_IDATA_BANK2_PEND | R/W1TS | 0h    | Interrupt Pending Status for cpu0_idata_bank2_pend |
| 5   | CPU0_IDATA_BANK1_PEND | R/W1TS | 0h    | Interrupt Pending Status for cpu0_idata_bank1_pend |
| 4   | CPU0_IDATA_BANK0_PEND | R/W1TS | 0h    | Interrupt Pending Status for cpu0_idata_bank0_pend |
| 3   | CPU0_ITAG_RAM3_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu0_itag_ram3_pend   |
| 2   | CPU0_ITAG_RAM2_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu0_itag_ram2_pend   |
| 1   | CPU0_ITAG_RAM1_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu0_itag_ram1_pend   |
| 0   | CPU0_ITAG_RAM0_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu0_itag_ram0_pend   |

#### 4.1.2.69 ECC\_AGG\_CORE0\_SEC\_ENABLE\_SET\_REG0 Register

##### 1 ECC\_AGG\_CORE0\_SEC\_ENABLE\_SET\_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

Return to [Summary Table](#)

**Table 4-224. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 0080h       |
| R5SS1         | 5300 4080h       |

**Figure 4-69. ECC\_AGG\_CORE0\_SEC\_ENABLE\_SET\_REG0 Name Register**

| 31                          | 30                          | 29                          | 28                          | 27                            | 26                         | 25                         | 24                         |
|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-------------------------------|----------------------------|----------------------------|----------------------------|
| RESERVED                    |                             |                             |                             | CPU0_KS_VIM_RAMECC_ENABLE_SET | B1TCM0_BANK1_ENABLE_SET    | B1TCM0_BANK0_ENABLE_SET    | B0TCM0_BANK1_ENABLE_SET    |
| NONE                        |                             |                             |                             | R/W1TS                        | R/W1TS                     | R/W1TS                     | R/W1TS                     |
| 0h                          |                             |                             |                             | 0h                            | 0h                         | 0h                         | 0h                         |
| 23                          | 22                          | 21                          | 20                          | 19                            | 18                         | 17                         | 16                         |
| B0TCM0_BANK0_ENABLE_SET     | ATCM0_BANK1_ENABLE_SET      | ATCM0_BANK0_ENABLE_SET      | CPU0_DDATA_RAM7_ENABLE_SET  | CPU0_DDATA_RAM6_ENABLE_SET    | CPU0_DDATA_RAM5_ENABLE_SET | CPU0_DDATA_RAM4_ENABLE_SET | CPU0_DDATA_RAM3_ENABLE_SET |
| R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                        | R/W1TS                     | R/W1TS                     | R/W1TS                     |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                            | 0h                         | 0h                         | 0h                         |
| 15                          | 14                          | 13                          | 12                          | 11                            | 10                         | 9                          | 8                          |
| CPU0_DDATA_RAM2_ENABLE_SET  | CPU0_DDATA_RAM1_ENABLE_SET  | CPU0_DDATA_RAM0_ENABLE_SET  | CPU0_DDIRTY_RAM_ENABLE_SET  | CPU0_DTAG_RAM3_ENABLE_SET     | CPU0_DTAG_RAM2_ENABLE_SET  | CPU0_DTAG_RAM1_ENABLE_SET  | CPU0_DTAG_RAM0_ENABLE_SET  |
| R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                        | R/W1TS                     | R/W1TS                     | R/W1TS                     |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                            | 0h                         | 0h                         | 0h                         |
| 7                           | 6                           | 5                           | 4                           | 3                             | 2                          | 1                          | 0                          |
| CPU0_IDATA_BANK3_ENABLE_SET | CPU0_IDATA_BANK2_ENABLE_SET | CPU0_IDATA_BANK1_ENABLE_SET | CPU0_IDATA_BANK0_ENABLE_SET | CPU0_ITAG_RAM3_ENABLE_SET     | CPU0_ITAG_RAM2_ENABLE_SET  | CPU0_ITAG_RAM1_ENABLE_SET  | CPU0_ITAG_RAM0_ENABLE_SET  |
| R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                        | R/W1TS                     | R/W1TS                     | R/W1TS                     |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                            | 0h                         | 0h                         | 0h                         |

**Table 4-226. ECC\_AGG\_CORE0\_SEC\_ENABLE\_SET\_REG0 Register Field Descriptions**

| Bit   | Field                         | Type   | Reset | Description                                               |
|-------|-------------------------------|--------|-------|-----------------------------------------------------------|
| 31:28 | RESERVED                      | NONE   | 0h    | Reserved                                                  |
| 27    | CPU0_KS_VIM_RAMECC_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_ks_vim_ramecc_pend |
| 26    | B1TCM0_BANK1_ENABLE_SET       | R/W1TS | 0h    | Interrupt Enable Set Register for b1tcm0_bank1_pend       |
| 25    | B1TCM0_BANK0_ENABLE_SET       | R/W1TS | 0h    | Interrupt Enable Set Register for b1tcm0_bank0_pend       |
| 24    | B0TCM0_BANK1_ENABLE_SET       | R/W1TS | 0h    | Interrupt Enable Set Register for b0tcm0_bank1_pend       |
| 23    | B0TCM0_BANK0_ENABLE_SET       | R/W1TS | 0h    | Interrupt Enable Set Register for b0tcm0_bank0_pend       |
| 22    | ATCM0_BANK1_ENABLE_SET        | R/W1TS | 0h    | Interrupt Enable Set Register for atcm0_bank1_pend        |

**Table 4-226. ECC\_AGG\_CORE0\_SEC\_ENABLE\_SET\_REG0 Register Field Descriptions (continued)**

| Bit | Field                       | Type   | Reset | Description                                             |
|-----|-----------------------------|--------|-------|---------------------------------------------------------|
| 21  | ATCM0_BANK0_ENABLE_SET      | R/W1TS | 0h    | Interrupt Enable Set Register for atcm0_bank0_pend      |
| 20  | CPU0_DDATA_RAM7_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_ddata_ram7_pend  |
| 19  | CPU0_DDATA_RAM6_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_ddata_ram6_pend  |
| 18  | CPU0_DDATA_RAM5_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_ddata_ram5_pend  |
| 17  | CPU0_DDATA_RAM4_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_ddata_ram4_pend  |
| 16  | CPU0_DDATA_RAM3_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_ddata_ram3_pend  |
| 15  | CPU0_DDATA_RAM2_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_ddata_ram2_pend  |
| 14  | CPU0_DDATA_RAM1_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_ddata_ram1_pend  |
| 13  | CPU0_DDATA_RAM0_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_ddata_ram0_pend  |
| 12  | CPU0_DDIRTY_RAM_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_ddirty_ram_pend  |
| 11  | CPU0_DTAG_RAM3_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_dtag_ram3_pend   |
| 10  | CPU0_DTAG_RAM2_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_dtag_ram2_pend   |
| 9   | CPU0_DTAG_RAM1_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_dtag_ram1_pend   |
| 8   | CPU0_DTAG_RAM0_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_dtag_ram0_pend   |
| 7   | CPU0_IDATA_BANK3_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_idata_bank3_pend |
| 6   | CPU0_IDATA_BANK2_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_idata_bank2_pend |
| 5   | CPU0_IDATA_BANK1_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_idata_bank1_pend |
| 4   | CPU0_IDATA_BANK0_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_idata_bank0_pend |
| 3   | CPU0_ITAG_RAM3_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_itag_ram3_pend   |
| 2   | CPU0_ITAG_RAM2_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_itag_ram2_pend   |
| 1   | CPU0_ITAG_RAM1_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_itag_ram1_pend   |
| 0   | CPU0_ITAG_RAM0_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_itag_ram0_pend   |

#### 4.1.2.70 ECC\_AGG\_CORE0\_SEC\_ENABLE\_CLR\_REG0 Register

##### 1 ECC\_AGG\_CORE0\_SEC\_ENABLE\_CLR\_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to [Summary Table](#)

**Table 4-227. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 00C0h       |
| R5SS1         | 5300 40C0h       |

**Figure 4-70. ECC\_AGG\_CORE0\_SEC\_ENABLE\_CLR\_REG0 Name Register**

| 31                          | 30                          | 29                          | 28                          | 27                            | 26                         | 25                         | 24                         |
|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-------------------------------|----------------------------|----------------------------|----------------------------|
| RESERVED                    |                             |                             |                             | CPU0_KS_VIM_RAMECC_ENABLE_CLR | B1TCM0_BANK1_ENABLE_CLR    | B1TCM0_BANK0_ENABLE_CLR    | B0TCM0_BANK1_ENABLE_CLR    |
| NONE                        |                             |                             |                             | R/W1TC                        | R/W1TC                     | R/W1TC                     | R/W1TC                     |
| 0h                          |                             |                             |                             | 0h                            | 0h                         | 0h                         | 0h                         |
| 23                          | 22                          | 21                          | 20                          | 19                            | 18                         | 17                         | 16                         |
| B0TCM0_BANK0_ENABLE_CLR     | ATCM0_BANK1_ENABLE_CLR      | ATCM0_BANK0_ENABLE_CLR      | CPU0_DDATA_RAM7_ENABLE_CLR  | CPU0_DDATA_RAM6_ENABLE_CLR    | CPU0_DDATA_RAM5_ENABLE_CLR | CPU0_DDATA_RAM4_ENABLE_CLR | CPU0_DDATA_RAM3_ENABLE_CLR |
| R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                        | R/W1TC                     | R/W1TC                     | R/W1TC                     |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                            | 0h                         | 0h                         | 0h                         |
| 15                          | 14                          | 13                          | 12                          | 11                            | 10                         | 9                          | 8                          |
| CPU0_DDATA_RAM2_ENABLE_CLR  | CPU0_DDATA_RAM1_ENABLE_CLR  | CPU0_DDATA_RAM0_ENABLE_CLR  | CPU0_DDIRTY_RAM_ENABLE_CLR  | CPU0_DTAG_RAM3_ENABLE_CLR     | CPU0_DTAG_RAM2_ENABLE_CLR  | CPU0_DTAG_RAM1_ENABLE_CLR  | CPU0_DTAG_RAM0_ENABLE_CLR  |
| R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                        | R/W1TC                     | R/W1TC                     | R/W1TC                     |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                            | 0h                         | 0h                         | 0h                         |
| 7                           | 6                           | 5                           | 4                           | 3                             | 2                          | 1                          | 0                          |
| CPU0_IDATA_BANK3_ENABLE_CLR | CPU0_IDATA_BANK2_ENABLE_CLR | CPU0_IDATA_BANK1_ENABLE_CLR | CPU0_IDATA_BANK0_ENABLE_CLR | CPU0_ITAG_RAM3_ENABLE_CLR     | CPU0_ITAG_RAM2_ENABLE_CLR  | CPU0_ITAG_RAM1_ENABLE_CLR  | CPU0_ITAG_RAM0_ENABLE_CLR  |
| R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                        | R/W1TC                     | R/W1TC                     | R/W1TC                     |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                            | 0h                         | 0h                         | 0h                         |

**Table 4-229. ECC\_AGG\_CORE0\_SEC\_ENABLE\_CLR\_REG0 Register Field Descriptions**

| Bit   | Field                         | Type   | Reset | Description                                                 |
|-------|-------------------------------|--------|-------|-------------------------------------------------------------|
| 31:28 | RESERVED                      | NONE   | 0h    | Reserved                                                    |
| 27    | CPU0_KS_VIM_RAMECC_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_ks_vim_ramecc_pend |
| 26    | B1TCM0_BANK1_ENABLE_CLR       | R/W1TC | 0h    | Interrupt Enable Clear Register for b1tcm0_bank1_pend       |
| 25    | B1TCM0_BANK0_ENABLE_CLR       | R/W1TC | 0h    | Interrupt Enable Clear Register for b1tcm0_bank0_pend       |
| 24    | B0TCM0_BANK1_ENABLE_CLR       | R/W1TC | 0h    | Interrupt Enable Clear Register for b0tcm0_bank1_pend       |
| 23    | B0TCM0_BANK0_ENABLE_CLR       | R/W1TC | 0h    | Interrupt Enable Clear Register for b0tcm0_bank0_pend       |
| 22    | ATCM0_BANK1_ENABLE_CLR        | R/W1TC | 0h    | Interrupt Enable Clear Register for atcm0_bank1_pend        |

**Table 4-229. ECC\_AGG\_CORE0\_SEC\_ENABLE\_CLR\_REG0 Register Field Descriptions (continued)**

| Bit | Field                       | Type   | Reset | Description                                               |
|-----|-----------------------------|--------|-------|-----------------------------------------------------------|
| 21  | ATCM0_BANK0_ENABLE_CLR      | R/W1TC | 0h    | Interrupt Enable Clear Register for atcm0_bank0_pend      |
| 20  | CPU0_DDATA_RAM7_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_ddata_ram7_pend  |
| 19  | CPU0_DDATA_RAM6_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_ddata_ram6_pend  |
| 18  | CPU0_DDATA_RAM5_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_ddata_ram5_pend  |
| 17  | CPU0_DDATA_RAM4_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_ddata_ram4_pend  |
| 16  | CPU0_DDATA_RAM3_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_ddata_ram3_pend  |
| 15  | CPU0_DDATA_RAM2_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_ddata_ram2_pend  |
| 14  | CPU0_DDATA_RAM1_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_ddata_ram1_pend  |
| 13  | CPU0_DDATA_RAM0_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_ddata_ram0_pend  |
| 12  | CPU0_DDIRTY_RAM_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_ddirty_ram_pend  |
| 11  | CPU0_DTAG_RAM3_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_dtag_ram3_pend   |
| 10  | CPU0_DTAG_RAM2_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_dtag_ram2_pend   |
| 9   | CPU0_DTAG_RAM1_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_dtag_ram1_pend   |
| 8   | CPU0_DTAG_RAM0_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_dtag_ram0_pend   |
| 7   | CPU0_IDATA_BANK3_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_idata_bank3_pend |
| 6   | CPU0_IDATA_BANK2_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_idata_bank2_pend |
| 5   | CPU0_IDATA_BANK1_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_idata_bank1_pend |
| 4   | CPU0_IDATA_BANK0_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_idata_bank0_pend |
| 3   | CPU0_ITAG_RAM3_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_itag_ram3_pend   |
| 2   | CPU0_ITAG_RAM2_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_itag_ram2_pend   |
| 1   | CPU0_ITAG_RAM1_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_itag_ram1_pend   |
| 0   | CPU0_ITAG_RAM0_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_itag_ram0_pend   |



#### 4.1.2.71 ECC\_AGG\_CORE0\_DED\_EOI\_REG Register

##### 1 ECC\_AGG\_CORE0\_DED\_EOI\_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register.

Return to [Summary Table](#)

**Table 4-230. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 013Ch       |
| R5SS1         | 5300 413Ch       |

**Figure 4-71. ECC\_AGG\_CORE0\_DED\_EOI\_REG Name Register**

|          |    |    |    |    |    |    |        |
|----------|----|----|----|----|----|----|--------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24     |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16     |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8      |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0      |
| RESERVED |    |    |    |    |    |    | EOI_WR |
| NONE     |    |    |    |    |    |    | R/W1TS |
| 0h       |    |    |    |    |    |    | 0h     |

**Table 4-232. ECC\_AGG\_CORE0\_DED\_EOI\_REG Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description                                                                                                                                                                                     |
|------|----------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED | NONE   | 0h    | Reserved                                                                                                                                                                                        |
| 0    | EOI_WR   | R/W1TS | 0h    | Write of 1 to this register indicates that software has acknowledged the pending interrupt and the next interrupt can be sent to the host. The bit is self clearing and will be read as a zero. |

#### 4.1.2.72 ECC\_AGG\_CORE0\_DED\_STATUS\_REG0 Register

##### 1 ECC\_AGG\_CORE0\_DED\_STATUS\_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

Return to [Summary Table](#)

**Table 4-233. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 0140h       |
| R5SS1         | 5300 4140h       |

**Figure 4-72. ECC\_AGG\_CORE0\_DED\_STATUS\_REG0 Name Register**

| 31                    | 30                    | 29                    | 28                    | 27                      | 26                   | 25                   | 24                   |
|-----------------------|-----------------------|-----------------------|-----------------------|-------------------------|----------------------|----------------------|----------------------|
| RESERVED              |                       |                       |                       | CPU0_KS_VIM_RAMECC_PEND | B1TCM0_BANK1_PEND    | B1TCM0_BANK0_PEND    | B0TCM0_BANK1_PEND    |
| NONE                  |                       |                       |                       | R/W1TS                  | R/W1TS               | R/W1TS               | R/W1TS               |
| 0h                    |                       |                       |                       | 0h                      | 0h                   | 0h                   | 0h                   |
| 23                    | 22                    | 21                    | 20                    | 19                      | 18                   | 17                   | 16                   |
| B0TCM0_BANK0_PEND     | ATCM0_BANK1_PEND      | ATCM0_BANK0_PEND      | CPU0_DDATA_RAM7_PEND  | CPU0_DDATA_RAM6_PEND    | CPU0_DDATA_RAM5_PEND | CPU0_DDATA_RAM4_PEND | CPU0_DDATA_RAM3_PEND |
| R/W1TS                | R/W1TS                | R/W1TS                | R/W1TS                | R/W1TS                  | R/W1TS               | R/W1TS               | R/W1TS               |
| 0h                    | 0h                    | 0h                    | 0h                    | 0h                      | 0h                   | 0h                   | 0h                   |
| 15                    | 14                    | 13                    | 12                    | 11                      | 10                   | 9                    | 8                    |
| CPU0_DDATA_RAM2_PEND  | CPU0_DDATA_RAM1_PEND  | CPU0_DDATA_RAM0_PEND  | CPU0_DDIRTY_RAM_PEND  | CPU0_DTAG_RAM3_PEND     | CPU0_DTAG_RAM2_PEND  | CPU0_DTAG_RAM1_PEND  | CPU0_DTAG_RAM0_PEND  |
| R/W1TS                | R/W1TS                | R/W1TS                | R/W1TS                | R/W1TS                  | R/W1TS               | R/W1TS               | R/W1TS               |
| 0h                    | 0h                    | 0h                    | 0h                    | 0h                      | 0h                   | 0h                   | 0h                   |
| 7                     | 6                     | 5                     | 4                     | 3                       | 2                    | 1                    | 0                    |
| CPU0_IDATA_BANK3_PEND | CPU0_IDATA_BANK2_PEND | CPU0_IDATA_BANK1_PEND | CPU0_IDATA_BANK0_PEND | CPU0_ITAG_RAM3_PEND     | CPU0_ITAG_RAM2_PEND  | CPU0_ITAG_RAM1_PEND  | CPU0_ITAG_RAM0_PEND  |
| R/W1TS                | R/W1TS                | R/W1TS                | R/W1TS                | R/W1TS                  | R/W1TS               | R/W1TS               | R/W1TS               |
| 0h                    | 0h                    | 0h                    | 0h                    | 0h                      | 0h                   | 0h                   | 0h                   |

**Table 4-235. ECC\_AGG\_CORE0\_DED\_STATUS\_REG0 Register Field Descriptions**

| Bit   | Field                   | Type   | Reset | Description                                          |
|-------|-------------------------|--------|-------|------------------------------------------------------|
| 31:28 | RESERVED                | NONE   | 0h    | Reserved                                             |
| 27    | CPU0_KS_VIM_RAMECC_PEND | R/W1TS | 0h    | Interrupt Pending Status for cpu0_ks_vim_ramecc_pend |
| 26    | B1TCM0_BANK1_PEND       | R/W1TS | 0h    | Interrupt Pending Status for b1tcm0_bank1_pend       |
| 25    | B1TCM0_BANK0_PEND       | R/W1TS | 0h    | Interrupt Pending Status for b1tcm0_bank0_pend       |
| 24    | B0TCM0_BANK1_PEND       | R/W1TS | 0h    | Interrupt Pending Status for b0tcm0_bank1_pend       |
| 23    | B0TCM0_BANK0_PEND       | R/W1TS | 0h    | Interrupt Pending Status for b0tcm0_bank0_pend       |
| 22    | ATCM0_BANK1_PEND        | R/W1TS | 0h    | Interrupt Pending Status for atcm0_bank1_pend        |
| 21    | ATCM0_BANK0_PEND        | R/W1TS | 0h    | Interrupt Pending Status for atcm0_bank0_pend        |
| 20    | CPU0_DDATA_RAM7_PEND    | R/W1TS | 0h    | Interrupt Pending Status for cpu0_ddata_ram7_pend    |
| 19    | CPU0_DDATA_RAM6_PEND    | R/W1TS | 0h    | Interrupt Pending Status for cpu0_ddata_ram6_pend    |
| 18    | CPU0_DDATA_RAM5_PEND    | R/W1TS | 0h    | Interrupt Pending Status for cpu0_ddata_ram5_pend    |

**Table 4-235. ECC\_AGG\_CORE0\_DED\_STATUS\_REG0 Register Field Descriptions (continued)**

| Bit | Field                 | Type   | Reset | Description                                        |
|-----|-----------------------|--------|-------|----------------------------------------------------|
| 17  | CPU0_DDATA_RAM4_PEND  | R/W1TS | 0h    | Interrupt Pending Status for cpu0_ddata_ram4_pend  |
| 16  | CPU0_DDATA_RAM3_PEND  | R/W1TS | 0h    | Interrupt Pending Status for cpu0_ddata_ram3_pend  |
| 15  | CPU0_DDATA_RAM2_PEND  | R/W1TS | 0h    | Interrupt Pending Status for cpu0_ddata_ram2_pend  |
| 14  | CPU0_DDATA_RAM1_PEND  | R/W1TS | 0h    | Interrupt Pending Status for cpu0_ddata_ram1_pend  |
| 13  | CPU0_DDATA_RAM0_PEND  | R/W1TS | 0h    | Interrupt Pending Status for cpu0_ddata_ram0_pend  |
| 12  | CPU0_DDIRTY_RAM_PEND  | R/W1TS | 0h    | Interrupt Pending Status for cpu0_ddirty_ram_pend  |
| 11  | CPU0_DTAG_RAM3_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu0_dtag_ram3_pend   |
| 10  | CPU0_DTAG_RAM2_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu0_dtag_ram2_pend   |
| 9   | CPU0_DTAG_RAM1_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu0_dtag_ram1_pend   |
| 8   | CPU0_DTAG_RAM0_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu0_dtag_ram0_pend   |
| 7   | CPU0_IDATA_BANK3_PEND | R/W1TS | 0h    | Interrupt Pending Status for cpu0_idata_bank3_pend |
| 6   | CPU0_IDATA_BANK2_PEND | R/W1TS | 0h    | Interrupt Pending Status for cpu0_idata_bank2_pend |
| 5   | CPU0_IDATA_BANK1_PEND | R/W1TS | 0h    | Interrupt Pending Status for cpu0_idata_bank1_pend |
| 4   | CPU0_IDATA_BANK0_PEND | R/W1TS | 0h    | Interrupt Pending Status for cpu0_idata_bank0_pend |
| 3   | CPU0_ITAG_RAM3_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu0_itag_ram3_pend   |
| 2   | CPU0_ITAG_RAM2_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu0_itag_ram2_pend   |
| 1   | CPU0_ITAG_RAM1_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu0_itag_ram1_pend   |
| 0   | CPU0_ITAG_RAM0_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu0_itag_ram0_pend   |

#### 4.1.2.73 ECC\_AGG\_CORE0\_DED\_ENABLE\_SET\_REG0 Register

##### 1 ECC\_AGG\_CORE0\_DED\_ENABLE\_SET\_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

Return to [Summary Table](#)

**Table 4-236. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 0180h       |
| R5SS1         | 5300 4180h       |

**Figure 4-73. ECC\_AGG\_CORE0\_DED\_ENABLE\_SET\_REG0 Name Register**

| 31                          | 30                          | 29                          | 28                          | 27                            | 26                         | 25                         | 24                         |
|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-------------------------------|----------------------------|----------------------------|----------------------------|
| RESERVED                    |                             |                             |                             | CPU0_KS_VIM_RAMECC_ENABLE_SET | B1TCM0_BANK1_ENABLE_SET    | B1TCM0_BANK0_ENABLE_SET    | B0TCM0_BANK1_ENABLE_SET    |
| NONE                        |                             |                             |                             | R/W1TS                        | R/W1TS                     | R/W1TS                     | R/W1TS                     |
| 0h                          |                             |                             |                             | 0h                            | 0h                         | 0h                         | 0h                         |
| 23                          | 22                          | 21                          | 20                          | 19                            | 18                         | 17                         | 16                         |
| B0TCM0_BANK0_ENABLE_SET     | ATCM0_BANK1_ENABLE_SET      | ATCM0_BANK0_ENABLE_SET      | CPU0_DDATA_RAM7_ENABLE_SET  | CPU0_DDATA_RAM6_ENABLE_SET    | CPU0_DDATA_RAM5_ENABLE_SET | CPU0_DDATA_RAM4_ENABLE_SET | CPU0_DDATA_RAM3_ENABLE_SET |
| R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                        | R/W1TS                     | R/W1TS                     | R/W1TS                     |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                            | 0h                         | 0h                         | 0h                         |
| 15                          | 14                          | 13                          | 12                          | 11                            | 10                         | 9                          | 8                          |
| CPU0_DDATA_RAM2_ENABLE_SET  | CPU0_DDATA_RAM1_ENABLE_SET  | CPU0_DDATA_RAM0_ENABLE_SET  | CPU0_DDIRTY_RAM_ENABLE_SET  | CPU0_DTAG_RAM3_ENABLE_SET     | CPU0_DTAG_RAM2_ENABLE_SET  | CPU0_DTAG_RAM1_ENABLE_SET  | CPU0_DTAG_RAM0_ENABLE_SET  |
| R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                        | R/W1TS                     | R/W1TS                     | R/W1TS                     |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                            | 0h                         | 0h                         | 0h                         |
| 7                           | 6                           | 5                           | 4                           | 3                             | 2                          | 1                          | 0                          |
| CPU0_IDATA_BANK3_ENABLE_SET | CPU0_IDATA_BANK2_ENABLE_SET | CPU0_IDATA_BANK1_ENABLE_SET | CPU0_IDATA_BANK0_ENABLE_SET | CPU0_ITAG_RAM3_ENABLE_SET     | CPU0_ITAG_RAM2_ENABLE_SET  | CPU0_ITAG_RAM1_ENABLE_SET  | CPU0_ITAG_RAM0_ENABLE_SET  |
| R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                        | R/W1TS                     | R/W1TS                     | R/W1TS                     |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                            | 0h                         | 0h                         | 0h                         |

**Table 4-238. ECC\_AGG\_CORE0\_DED\_ENABLE\_SET\_REG0 Register Field Descriptions**

| Bit   | Field                         | Type   | Reset | Description                                               |
|-------|-------------------------------|--------|-------|-----------------------------------------------------------|
| 31:28 | RESERVED                      | NONE   | 0h    | Reserved                                                  |
| 27    | CPU0_KS_VIM_RAMECC_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_ks_vim_ramecc_pend |
| 26    | B1TCM0_BANK1_ENABLE_SET       | R/W1TS | 0h    | Interrupt Enable Set Register for b1tcm0_bank1_pend       |
| 25    | B1TCM0_BANK0_ENABLE_SET       | R/W1TS | 0h    | Interrupt Enable Set Register for b1tcm0_bank0_pend       |
| 24    | B0TCM0_BANK1_ENABLE_SET       | R/W1TS | 0h    | Interrupt Enable Set Register for b0tcm0_bank1_pend       |
| 23    | B0TCM0_BANK0_ENABLE_SET       | R/W1TS | 0h    | Interrupt Enable Set Register for b0tcm0_bank0_pend       |
| 22    | ATCM0_BANK1_ENABLE_SET        | R/W1TS | 0h    | Interrupt Enable Set Register for atcm0_bank1_pend        |

**Table 4-238. ECC\_AGG\_CORE0\_DED\_ENABLE\_SET\_REG0 Register Field Descriptions (continued)**

| Bit | Field                       | Type   | Reset | Description                                             |
|-----|-----------------------------|--------|-------|---------------------------------------------------------|
| 21  | ATCM0_BANK0_ENABLE_SET      | R/W1TS | 0h    | Interrupt Enable Set Register for atcm0_bank0_pend      |
| 20  | CPU0_DDATA_RAM7_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_ddata_ram7_pend  |
| 19  | CPU0_DDATA_RAM6_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_ddata_ram6_pend  |
| 18  | CPU0_DDATA_RAM5_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_ddata_ram5_pend  |
| 17  | CPU0_DDATA_RAM4_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_ddata_ram4_pend  |
| 16  | CPU0_DDATA_RAM3_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_ddata_ram3_pend  |
| 15  | CPU0_DDATA_RAM2_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_ddata_ram2_pend  |
| 14  | CPU0_DDATA_RAM1_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_ddata_ram1_pend  |
| 13  | CPU0_DDATA_RAM0_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_ddata_ram0_pend  |
| 12  | CPU0_DDIRTY_RAM_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_ddirty_ram_pend  |
| 11  | CPU0_DTAG_RAM3_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_dtag_ram3_pend   |
| 10  | CPU0_DTAG_RAM2_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_dtag_ram2_pend   |
| 9   | CPU0_DTAG_RAM1_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_dtag_ram1_pend   |
| 8   | CPU0_DTAG_RAM0_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_dtag_ram0_pend   |
| 7   | CPU0_IDATA_BANK3_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_idata_bank3_pend |
| 6   | CPU0_IDATA_BANK2_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_idata_bank2_pend |
| 5   | CPU0_IDATA_BANK1_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_idata_bank1_pend |
| 4   | CPU0_IDATA_BANK0_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_idata_bank0_pend |
| 3   | CPU0_ITAG_RAM3_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_itag_ram3_pend   |
| 2   | CPU0_ITAG_RAM2_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_itag_ram2_pend   |
| 1   | CPU0_ITAG_RAM1_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_itag_ram1_pend   |
| 0   | CPU0_ITAG_RAM0_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu0_itag_ram0_pend   |

#### 4.1.2.74 ECC\_AGG\_CORE0\_DED\_ENABLE\_CLR\_REG0 Register

##### 1 ECC\_AGG\_CORE0\_DED\_ENABLE\_CLR\_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to [Summary Table](#)

**Table 4-239. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 01C0h       |
| R5SS1         | 5300 41C0h       |

**Figure 4-74. ECC\_AGG\_CORE0\_DED\_ENABLE\_CLR\_REG0 Name Register**

| 31                          | 30                          | 29                          | 28                          | 27                            | 26                         | 25                         | 24                         |
|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-------------------------------|----------------------------|----------------------------|----------------------------|
| RESERVED                    |                             |                             |                             | CPU0_KS_VIM_RAMECC_ENABLE_CLR | B1TCM0_BANK1_ENABLE_CLR    | B1TCM0_BANK0_ENABLE_CLR    | B0TCM0_BANK1_ENABLE_CLR    |
| NONE                        |                             |                             |                             | R/W1TC                        | R/W1TC                     | R/W1TC                     | R/W1TC                     |
| 0h                          |                             |                             |                             | 0h                            | 0h                         | 0h                         | 0h                         |
| 23                          | 22                          | 21                          | 20                          | 19                            | 18                         | 17                         | 16                         |
| B0TCM0_BANK0_ENABLE_CLR     | ATCM0_BANK1_ENABLE_CLR      | ATCM0_BANK0_ENABLE_CLR      | CPU0_DDATA_RAM7_ENABLE_CLR  | CPU0_DDATA_RAM6_ENABLE_CLR    | CPU0_DDATA_RAM5_ENABLE_CLR | CPU0_DDATA_RAM4_ENABLE_CLR | CPU0_DDATA_RAM3_ENABLE_CLR |
| R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                        | R/W1TC                     | R/W1TC                     | R/W1TC                     |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                            | 0h                         | 0h                         | 0h                         |
| 15                          | 14                          | 13                          | 12                          | 11                            | 10                         | 9                          | 8                          |
| CPU0_DDATA_RAM2_ENABLE_CLR  | CPU0_DDATA_RAM1_ENABLE_CLR  | CPU0_DDATA_RAM0_ENABLE_CLR  | CPU0_DDIRTY_RAM_ENABLE_CLR  | CPU0_DTAG_RAM3_ENABLE_CLR     | CPU0_DTAG_RAM2_ENABLE_CLR  | CPU0_DTAG_RAM1_ENABLE_CLR  | CPU0_DTAG_RAM0_ENABLE_CLR  |
| R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                        | R/W1TC                     | R/W1TC                     | R/W1TC                     |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                            | 0h                         | 0h                         | 0h                         |
| 7                           | 6                           | 5                           | 4                           | 3                             | 2                          | 1                          | 0                          |
| CPU0_IDATA_BANK3_ENABLE_CLR | CPU0_IDATA_BANK2_ENABLE_CLR | CPU0_IDATA_BANK1_ENABLE_CLR | CPU0_IDATA_BANK0_ENABLE_CLR | CPU0_ITAG_RAM3_ENABLE_CLR     | CPU0_ITAG_RAM2_ENABLE_CLR  | CPU0_ITAG_RAM1_ENABLE_CLR  | CPU0_ITAG_RAM0_ENABLE_CLR  |
| R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                        | R/W1TC                     | R/W1TC                     | R/W1TC                     |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                            | 0h                         | 0h                         | 0h                         |

**Table 4-241. ECC\_AGG\_CORE0\_DED\_ENABLE\_CLR\_REG0 Register Field Descriptions**

| Bit   | Field                         | Type   | Reset | Description                                                 |
|-------|-------------------------------|--------|-------|-------------------------------------------------------------|
| 31:28 | RESERVED                      | NONE   | 0h    | Reserved                                                    |
| 27    | CPU0_KS_VIM_RAMECC_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_ks_vim_ramecc_pend |
| 26    | B1TCM0_BANK1_ENABLE_CLR       | R/W1TC | 0h    | Interrupt Enable Clear Register for b1tcm0_bank1_pend       |
| 25    | B1TCM0_BANK0_ENABLE_CLR       | R/W1TC | 0h    | Interrupt Enable Clear Register for b1tcm0_bank0_pend       |
| 24    | B0TCM0_BANK1_ENABLE_CLR       | R/W1TC | 0h    | Interrupt Enable Clear Register for b0tcm0_bank1_pend       |
| 23    | B0TCM0_BANK0_ENABLE_CLR       | R/W1TC | 0h    | Interrupt Enable Clear Register for b0tcm0_bank0_pend       |
| 22    | ATCM0_BANK1_ENABLE_CLR        | R/W1TC | 0h    | Interrupt Enable Clear Register for atcm0_bank1_pend        |

**Table 4-241. ECC\_AGG\_CORE0\_DED\_ENABLE\_CLR\_REG0 Register Field Descriptions (continued)**

| Bit | Field                       | Type   | Reset | Description                                               |
|-----|-----------------------------|--------|-------|-----------------------------------------------------------|
| 21  | ATCM0_BANK0_ENABLE_CLR      | R/W1TC | 0h    | Interrupt Enable Clear Register for atcm0_bank0_pend      |
| 20  | CPU0_DDATA_RAM7_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_ddata_ram7_pend  |
| 19  | CPU0_DDATA_RAM6_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_ddata_ram6_pend  |
| 18  | CPU0_DDATA_RAM5_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_ddata_ram5_pend  |
| 17  | CPU0_DDATA_RAM4_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_ddata_ram4_pend  |
| 16  | CPU0_DDATA_RAM3_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_ddata_ram3_pend  |
| 15  | CPU0_DDATA_RAM2_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_ddata_ram2_pend  |
| 14  | CPU0_DDATA_RAM1_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_ddata_ram1_pend  |
| 13  | CPU0_DDATA_RAM0_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_ddata_ram0_pend  |
| 12  | CPU0_DDIRTY_RAM_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_ddirty_ram_pend  |
| 11  | CPU0_DTAG_RAM3_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_dtag_ram3_pend   |
| 10  | CPU0_DTAG_RAM2_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_dtag_ram2_pend   |
| 9   | CPU0_DTAG_RAM1_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_dtag_ram1_pend   |
| 8   | CPU0_DTAG_RAM0_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_dtag_ram0_pend   |
| 7   | CPU0_IDATA_BANK3_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_idata_bank3_pend |
| 6   | CPU0_IDATA_BANK2_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_idata_bank2_pend |
| 5   | CPU0_IDATA_BANK1_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_idata_bank1_pend |
| 4   | CPU0_IDATA_BANK0_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_idata_bank0_pend |
| 3   | CPU0_ITAG_RAM3_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_itag_ram3_pend   |
| 2   | CPU0_ITAG_RAM2_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_itag_ram2_pend   |
| 1   | CPU0_ITAG_RAM1_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_itag_ram1_pend   |
| 0   | CPU0_ITAG_RAM0_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu0_itag_ram0_pend   |

#### 4.1.2.75 ECC\_AGG\_CORE0\_AGGR\_ENABLE\_SET Register

##### 1 ECC\_AGG\_CORE0\_AGGR\_ENABLE\_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register.

Return to [Summary Table](#)

**Table 4-242. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 0200h       |
| R5SS1         | 5300 4200h       |

**Figure 4-75. ECC\_AGG\_CORE0\_AGGR\_ENABLE\_SET Name Register**

|          |    |    |    |    |    |         |        |
|----------|----|----|----|----|----|---------|--------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25      | 24     |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 23       | 22 | 21 | 20 | 19 | 18 | 17      | 16     |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 15       | 14 | 13 | 12 | 11 | 10 | 9       | 8      |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 7        | 6  | 5  | 4  | 3  | 2  | 1       | 0      |
| RESERVED |    |    |    |    |    | TIMEOUT | PARITY |
| NONE     |    |    |    |    |    | R/W1TS  | R/W1TS |
| 0h       |    |    |    |    |    | 0h      | 0h     |

**Table 4-244. ECC\_AGG\_CORE0\_AGGR\_ENABLE\_SET Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description                                   |
|------|----------|--------|-------|-----------------------------------------------|
| 31:2 | RESERVED | NONE   | 0h    | Reserved                                      |
| 1    | TIMEOUT  | R/W1TS | 0h    | Interrupt enable set for svbus timeout errors |
| 0    | PARITY   | R/W1TS | 0h    | Interrupt enable set for parity errors        |



#### 4.1.2.76 ECC\_AGG\_CORE0\_AGGR\_ENABLE\_CLR Register

##### 1 ECC\_AGG\_CORE0\_AGGR\_ENABLE\_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register.

Return to [Summary Table](#)

**Table 4-245. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 0204h       |
| R5SS1         | 5300 4204h       |

**Figure 4-76. ECC\_AGG\_CORE0\_AGGR\_ENABLE\_CLR Name Register**

|          |    |    |    |    |    |         |        |
|----------|----|----|----|----|----|---------|--------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25      | 24     |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 23       | 22 | 21 | 20 | 19 | 18 | 17      | 16     |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 15       | 14 | 13 | 12 | 11 | 10 | 9       | 8      |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 7        | 6  | 5  | 4  | 3  | 2  | 1       | 0      |
| RESERVED |    |    |    |    |    | TIMEOUT | PARITY |
| NONE     |    |    |    |    |    | R/W1TC  | R/W1TC |
| 0h       |    |    |    |    |    | 0h      | 0h     |

**Table 4-247. ECC\_AGG\_CORE0\_AGGR\_ENABLE\_CLR Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description                                     |
|------|----------|--------|-------|-------------------------------------------------|
| 31:2 | RESERVED | NONE   | 0h    | Reserved                                        |
| 1    | TIMEOUT  | R/W1TC | 0h    | Interrupt enable clear for svbus timeout errors |
| 0    | PARITY   | R/W1TC | 0h    | Interrupt enable clear for parity errors        |

#### 4.1.2.77 ECC\_AGG\_CORE0\_AGGR\_STATUS\_SET Register

##### 1 ECC\_AGG\_CORE0\_AGGR\_STATUS\_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register.

Return to [Summary Table](#)

**Table 4-248. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 0208h       |
| R5SS1         | 5300 4208h       |

**Figure 4-77. ECC\_AGG\_CORE0\_AGGR\_STATUS\_SET Name Register**

|          |    |    |    |         |    |        |    |
|----------|----|----|----|---------|----|--------|----|
| 31       | 30 | 29 | 28 | 27      | 26 | 25     | 24 |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 23       | 22 | 21 | 20 | 19      | 18 | 17     | 16 |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 15       | 14 | 13 | 12 | 11      | 10 | 9      | 8  |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 7        | 6  | 5  | 4  | 3       | 2  | 1      | 0  |
| RESERVED |    |    |    | TIMEOUT |    | PARITY |    |
| NONE     |    |    |    | R/WI    |    | R/WI   |    |
| 0h       |    |    |    | 0h      |    | 0h     |    |

**Table 4-250. ECC\_AGG\_CORE0\_AGGR\_STATUS\_SET Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 3:2  | TIMEOUT  | R/WI | 0h    | 2-bit saturating counter of the number of timeout errors that have occurred since last cleared.<br>2'b00 - No timeout errors have occurred<br>2'b01 - 1 timeout error has occurred<br>2'b10 - 2 timeout error has occurred<br>2'b11 - 3 or more timeout errors have occurred<br>A write of a non-zero value to this register increments that many from the timeout fields. If the value written is less than the current value of the counter, then the pending level interrupt stays asserted. . If this register goes from 0 to non zero a level interrupt will be asserted as well as a pulse interrupt. If the value was non zero to non zero then the level interrupt would remain asserted, but no new pulse interrupt would be asserted. You must write the eoi register to get a new pulse interrupt. |

**Table 4-250. ECC\_AGG\_CORE0\_AGGR\_STATUS\_SET Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-----|--------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0 | PARITY | R/WI | 0h    | <p>2-bit saturating counter of the number of parity errors that have occurred since last cleared.</p> <p>2'b00 - No parity errors have occurred</p> <p>2'b01 - 1 parity error has occurred</p> <p>2'b10 - 2 parity error has occurred</p> <p>2'b11 - 3 or more parity error have occurred</p> <p>A write of a non-zero value to this register increments that many from the parity fields. If the value written is less than the current value of the counter, then the pending level interrupt stays asserted. If this register goes from 0 to non zero a level interrupt will be asserted as well as a pulse interrupt. If the value was non zero to non zero then the level interrupt would remain asserted, but no new pulse interrupt would be asserted. You must write the eoi register to get a new pulse interrupt.</p> |

#### 4.1.2.78 ECC\_AGG\_CORE0\_AGGR\_STATUS\_CLR Register

##### 1 ECC\_AGG\_CORE0\_AGGR\_STATUS\_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register.

Return to [Summary Table](#)

**Table 4-251. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 020Ch       |
| R5SS1         | 5300 420Ch       |

**Figure 4-78. ECC\_AGG\_CORE0\_AGGR\_STATUS\_CLR Name Register**

|          |    |    |    |         |    |        |    |
|----------|----|----|----|---------|----|--------|----|
| 31       | 30 | 29 | 28 | 27      | 26 | 25     | 24 |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 23       | 22 | 21 | 20 | 19      | 18 | 17     | 16 |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 15       | 14 | 13 | 12 | 11      | 10 | 9      | 8  |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 7        | 6  | 5  | 4  | 3       | 2  | 1      | 0  |
| RESERVED |    |    |    | TIMEOUT |    | PARITY |    |
| NONE     |    |    |    | R/W     |    | R/W    |    |
| 0h       |    |    |    | 0h      |    | 0h     |    |

**Table 4-253. ECC\_AGG\_CORE0\_AGGR\_STATUS\_CLR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 3:2  | TIMEOUT  | R/W  | 0h    | 2'b00 - No timeout errors have occurred<br>2'b01 - 1 timeout error has occurred<br>2'b10 - 2 timeout error has occurred<br>2'b11 - 3 or more timeout errors have occurred<br>A write of a non-zero value to this register decrements that many from the timeout fields. If the resulting written value is non zero, then the pending level interrupt stays asserted. A new pulse interrupt will not be asserted, you must write the eoi register for that to occur. If you write a value more than the counter value the result will be zero. |
| 1:0  | PARITY   | R/W  | 0h    | 2'b00 - No parity errors have occurred<br>2'b01 - 1 parity error has occurred<br>2'b10 - 2 parity error has occurred<br>2'b11 - 3 or more parity error have occurred<br>A write of a non-zero value to this register decrements that many from the parity fields. If the resulting written value is non zero, then the pending level interrupt stays asserted. A new pulse interrupt will not be asserted, you must write the eoi register for that to occur. If you write a value more than the counter value the result will be zero.       |

#### 4.1.2.79 ECC\_AGG\_CORE1\_AGGR\_REVISION Register

##### 1 ECC\_AGG\_CORE1\_AGGR\_REVISION Register (Offset = 0h) [reset = 66A0C200h]

The Revision Register contains the major and minor revisions for the ECC aggregator module. It does not support byte accesses.

Return to [Summary Table](#)

**Table 4-254. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 3000h       |
| R5SS1         | 5300 7000h       |

**Figure 4-79. ECC\_AGG\_CORE1\_AGGR\_REVISION Name Register**

|           |    |        |    |           |        |    |    |
|-----------|----|--------|----|-----------|--------|----|----|
| 31        | 30 | 29     | 28 | 27        | 26     | 25 | 24 |
| SCHEME    |    | BU     |    | MODULE_ID |        |    |    |
| R         |    | R      |    | R         |        |    |    |
| 1h        |    | 2h     |    | 6A0h      |        |    |    |
| 23        | 22 | 21     | 20 | 19        | 18     | 17 | 16 |
| MODULE_ID |    |        |    |           |        |    |    |
| R         |    |        |    |           |        |    |    |
| 6A0h      |    |        |    |           |        |    |    |
| 15        | 14 | 13     | 12 | 11        | 10     | 9  | 8  |
| REVRTL    |    |        |    |           | REVMAJ |    |    |
| R         |    |        |    |           | R      |    |    |
| 18h       |    |        |    |           | 2h     |    |    |
| 7         | 6  | 5      | 4  | 3         | 2      | 1  | 0  |
| CUSTOM    |    | REVMIN |    |           |        |    |    |
| R         |    | R      |    |           |        |    |    |
| 0h        |    | 0h     |    |           |        |    |    |

**Table 4-256. ECC\_AGG\_CORE1\_AGGR\_REVISION Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description    |
|-------|-----------|------|-------|----------------|
| 31:30 | SCHEME    | R    | 1h    | Scheme         |
| 29:28 | BU        | R    | 2h    | Business Unit  |
| 27:16 | MODULE_ID | R    | 6A0h  | Module ID      |
| 15:11 | REVRTL    | R    | 18h   | RTL version    |
| 10:8  | REVMAJ    | R    | 2h    | Major version  |
| 7:6   | CUSTOM    | R    | 0h    | Custom version |
| 5:0   | REVMIN    | R    | 0h    | Minor version  |

#### 4.1.2.80 ECC\_AGG\_CORE1\_ECC\_VECTOR Register

##### 1 ECC\_AGG\_CORE1\_ECC\_VECTOR Register (Offset = 8h) [reset = 0h]

ECC RAM ID to select which ECC RAM to control or read status from.

Return to [Summary Table](#)

**Table 4-257. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 3008h       |
| R5SS1         | 5300 7008h       |

**Figure 4-80. ECC\_AGG\_CORE1\_ECC\_VECTOR Name Register**

|                  |          |    |    |    |            |    |                   |
|------------------|----------|----|----|----|------------|----|-------------------|
| 31               | 30       | 29 | 28 | 27 | 26         | 25 | 24                |
| RESERVED         |          |    |    |    |            |    | RD_SVBUS_D<br>ONE |
| NONE             |          |    |    |    |            |    | R                 |
| 0h               |          |    |    |    |            |    | 0h                |
| 23               | 22       | 21 | 20 | 19 | 18         | 17 | 16                |
| RD_SVBUS_ADDRESS |          |    |    |    |            |    |                   |
| R/W              |          |    |    |    |            |    |                   |
| 0h               |          |    |    |    |            |    |                   |
| 15               | 14       | 13 | 12 | 11 | 10         | 9  | 8                 |
| RD_SVBUS         | RESERVED |    |    |    | ECC_VECTOR |    |                   |
| R/W1TS           | NONE     |    |    |    | R/W        |    |                   |
| 0h               | 0h       |    |    |    | 0h         |    |                   |
| 7                | 6        | 5  | 4  | 3  | 2          | 1  | 0                 |
| ECC_VECTOR       |          |    |    |    |            |    |                   |
| R/W              |          |    |    |    |            |    |                   |
| 0h               |          |    |    |    |            |    |                   |

**Table 4-259. ECC\_AGG\_CORE1\_ECC\_VECTOR Register Field Descriptions**

| Bit   | Field            | Type   | Reset | Description                                                             |
|-------|------------------|--------|-------|-------------------------------------------------------------------------|
| 31:25 | RESERVED         | NONE   | 0h    | Reserved                                                                |
| 24    | RD_SVBUS_DONE    | R      | 0h    | Status to indicate if read on serial VBUS is complete                   |
| 23:16 | RD_SVBUS_ADDRESS | R/W    | 0h    | Read address                                                            |
| 15    | RD_SVBUS         | R/W1TS | 0h    | Write 1 to trigger a read on the serial VBUS                            |
| 14:11 | RESERVED         | NONE   | 0h    | Reserved                                                                |
| 10:0  | ECC_VECTOR       | R/W    | 0h    | Value written to select the corresponding ECC RAM for control or status |

#### 4.1.2.81 ECC\_AGG\_CORE1\_MISC\_STATUS Register

##### 1 ECC\_AGG\_CORE1\_MISC\_STATUS Register (Offset = Ch) [reset = 1Ch]

Contains misc status such as number of ECC RAMs serviced by the ECC aggregator.

Return to [Summary Table](#)

**Table 4-260. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 300Ch       |
| R5SS1         | 5300 700Ch       |

**Figure 4-81. ECC\_AGG\_CORE1\_MISC\_STATUS Name Register**

|          |    |    |    |    |          |    |    |
|----------|----|----|----|----|----------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26       | 25 | 24 |
| RESERVED |    |    |    |    |          |    |    |
| NONE     |    |    |    |    |          |    |    |
| 0h       |    |    |    |    |          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18       | 17 | 16 |
| RESERVED |    |    |    |    |          |    |    |
| NONE     |    |    |    |    |          |    |    |
| 0h       |    |    |    |    |          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10       | 9  | 8  |
| RESERVED |    |    |    |    | NUM_RAMs |    |    |
| NONE     |    |    |    |    | R        |    |    |
| 0h       |    |    |    |    | 1Ch      |    |    |
| 7        | 6  | 5  | 4  | 3  | 2        | 1  | 0  |
| NUM_RAMs |    |    |    |    |          |    |    |
| R        |    |    |    |    |          |    |    |
| 1Ch      |    |    |    |    |          |    |    |

**Table 4-262. ECC\_AGG\_CORE1\_MISC\_STATUS Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                 |
|-------|----------|------|-------|-------------------------------------------------------------|
| 31:11 | RESERVED | NONE | 0h    | Reserved                                                    |
| 10:0  | NUM_RAMs | R    | 1Ch   | Indicates the number of RAMs serviced by the ECC aggregator |

#### 4.1.2.82 ECC\_AGG\_CORE1\_ECC\_WRAP\_REVISION Register

##### 1 ECC\_AGG\_CORE1\_ECC\_WRAP\_REVISION Register (Offset = 10h) [reset = 66A40202h]

Revision parameters.

Return to [Summary Table](#)

**Table 4-263. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 3010h       |
| R5SS1         | 5300 7010h       |

**Figure 4-82. ECC\_AGG\_CORE1\_ECC\_WRAP\_REVISION Name Register**

|           |    |        |    |           |        |    |    |
|-----------|----|--------|----|-----------|--------|----|----|
| 31        | 30 | 29     | 28 | 27        | 26     | 25 | 24 |
| SCHEME    |    | BU     |    | MODULE_ID |        |    |    |
| R         |    | R      |    | R         |        |    |    |
| 1h        |    | 2h     |    | 6A4h      |        |    |    |
| 23        | 22 | 21     | 20 | 19        | 18     | 17 | 16 |
| MODULE_ID |    |        |    |           |        |    |    |
| R         |    |        |    |           |        |    |    |
| 6A4h      |    |        |    |           |        |    |    |
| 15        | 14 | 13     | 12 | 11        | 10     | 9  | 8  |
| REVRTL    |    |        |    |           | REVMaj |    |    |
| R         |    |        |    |           | R      |    |    |
| 0h        |    |        |    |           | 2h     |    |    |
| 7         | 6  | 5      | 4  | 3         | 2      | 1  | 0  |
| CUSTOM    |    | REVMIN |    |           |        |    |    |
| R         |    | R      |    |           |        |    |    |
| 0h        |    | 2h     |    |           |        |    |    |

**Table 4-265. ECC\_AGG\_CORE1\_ECC\_WRAP\_REVISION Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description    |
|-------|-----------|------|-------|----------------|
| 31:30 | SCHEME    | R    | 1h    | Scheme         |
| 29:28 | BU        | R    | 2h    | bu             |
| 27:16 | MODULE_ID | R    | 6A4h  | Module ID      |
| 15:11 | REVRTL    | R    | 0h    | RTL version    |
| 10:8  | REVMaj    | R    | 2h    | Major version  |
| 7:6   | CUSTOM    | R    | 0h    | Custom version |
| 5:0   | REVMIN    | R    | 2h    | Minor version  |



#### 4.1.2.83 ECC\_AGG\_CORE1\_CONTROL Register

##### 1 ECC\_AGG\_CORE1\_CONTROL Register (Offset = 14h) [reset = 187h]

ECC Control Register.

Return to [Summary Table](#)

**Table 4-266. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 3014h       |
| R5SS1         | 5300 7014h       |

**Figure 4-83. ECC\_AGG\_CORE1\_CONTROL Name Register**

|                  |            |             |           |           |            |           |                         |
|------------------|------------|-------------|-----------|-----------|------------|-----------|-------------------------|
| 31               | 30         | 29          | 28        | 27        | 26         | 25        | 24                      |
| RESERVED         |            |             |           |           |            |           |                         |
| NONE             |            |             |           |           |            |           |                         |
| 0h               |            |             |           |           |            |           |                         |
| 23               | 22         | 21          | 20        | 19        | 18         | 17        | 16                      |
| RESERVED         |            |             |           |           |            |           |                         |
| NONE             |            |             |           |           |            |           |                         |
| 0h               |            |             |           |           |            |           |                         |
| 15               | 14         | 13          | 12        | 11        | 10         | 9         | 8                       |
| RESERVED         |            |             |           |           |            |           | CHECK_SVBU<br>S_TIMEOUT |
| NONE             |            |             |           |           |            |           | R/W                     |
| 0h               |            |             |           |           |            |           | 1h                      |
| 7                | 6          | 5           | 4         | 3         | 2          | 1         | 0                       |
| CHECK_PARIT<br>Y | ERROR_ONCE | FORCE_N_ROW | FORCE_DED | FORCE_SEC | ENABLE_RMW | ECC_CHECK | ECC_ENABLE              |
| R/W              | R/W        | R/W         | R/W       | R/W       | R/W        | R/W       | R/W                     |
| 1h               | 0h         | 0h          | 0h        | 0h        | 1h         | 1h        | 1h                      |

**Table 4-268. ECC\_AGG\_CORE1\_CONTROL Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                    |
|------|-------------------------|------|-------|--------------------------------|
| 31:9 | RESERVED                | NONE | 0h    | Reserved                       |
| 8    | CHECK_SVBU<br>S_TIMEOUT | R/W  | 1h    | check for svbus timeout errors |
| 7    | CHECK_PARITY            | R/W  | 1h    | check for parity errors        |
| 6    | ERROR_ONCE              | R/W  | 0h    | Force Error only once          |
| 5    | FORCE_N_ROW             | R/W  | 0h    | Force Error on any RAM read    |
| 4    | FORCE_DED               | R/W  | 0h    | Force Double Bit Error         |
| 3    | FORCE_SEC               | R/W  | 0h    | Force Single Bit Error         |
| 2    | ENABLE_RMW              | R/W  | 1h    | Enable rmw                     |
| 1    | ECC_CHECK               | R/W  | 1h    | Enable ECC check               |
| 0    | ECC_ENABLE              | R/W  | 1h    | Enable ECC                     |

#### 4.1.2.84 ECC\_AGG\_CORE1\_ERROR\_CTRL1 Register

##### 1 ECC\_AGG\_CORE1\_ERROR\_CTRL1 Register (Offset = 18h) [reset = 0h]

ECC Error Control1 Register.

Return to [Summary Table](#)

**Table 4-269. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 3018h       |
| R5SS1         | 5300 7018h       |

**Figure 4-84. ECC\_AGG\_CORE1\_ERROR\_CTRL1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ECC_ROW |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ECC_ROW |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ECC_ROW |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ECC_ROW |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-271. ECC\_AGG\_CORE1\_ERROR\_CTRL1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                             |
|------|---------|------|-------|---------------------------------------------------------------------------------------------------------|
| 31:0 | ECC_ROW | R/W  | 0h    | Row address where single or double-bit error needs to be applied. This is ignored if force_n_row is set |

#### 4.1.2.85 ECC\_AGG\_CORE1\_ERROR\_CTRL2 Register

##### 1 ECC\_AGG\_CORE1\_ERROR\_CTRL2 Register (Offset = 1Ch) [reset = 0h]

ECC Error Control2 Register.

Return to [Summary Table](#)

**Table 4-272. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 301Ch       |
| R5SS1         | 5300 701Ch       |

**Figure 4-85. ECC\_AGG\_CORE1\_ERROR\_CTRL2 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ECC_BIT2 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ECC_BIT2 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ECC_BIT1 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ECC_BIT1 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-274. ECC\_AGG\_CORE1\_ERROR\_CTRL2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                              |
|-------|----------|------|-------|--------------------------------------------------------------------------|
| 31:16 | ECC_BIT2 | R/W  | 0h    | Data bit that needs to be flipped if double bit error needs to be forced |
| 15:0  | ECC_BIT1 | R/W  | 0h    | Data bit that needs to be flipped when force_sec is set                  |

#### 4.1.2.86 ECC\_AGG\_CORE1\_ERROR\_STATUS1 Register

##### 1 ECC\_AGG\_CORE1\_ERROR\_STATUS1 Register (Offset = 20h) [reset = 0h]

ECC Error Status1 Register.

Return to [Summary Table](#)

**Table 4-275. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 3020h       |
| R5SS1         | 5300 7020h       |

**Figure 4-86. ECC\_AGG\_CORE1\_ERROR\_STATUS1 Name Register**

|                  |                |    |               |             |    |             |    |
|------------------|----------------|----|---------------|-------------|----|-------------|----|
| 31               | 30             | 29 | 28            | 27          | 26 | 25          | 24 |
| ECC_BIT1         |                |    |               |             |    |             |    |
| R                |                |    |               |             |    |             |    |
| 0h               |                |    |               |             |    |             |    |
| 23               | 22             | 21 | 20            | 19          | 18 | 17          | 16 |
| ECC_BIT1         |                |    |               |             |    |             |    |
| R                |                |    |               |             |    |             |    |
| 0h               |                |    |               |             |    |             |    |
| 15               | 14             | 13 | 12            | 11          | 10 | 9           | 8  |
| CLR_CTRL_REG_ERR | CLR_PARITY_ERR |    | CLR_ECC_OTHER | CLR_ECC_DED |    | CLR_ECC_SEC |    |
| R/W1TC           | R/WD           |    | R/W1TC        | R/WD        |    | R/WD        |    |
| 0h               | 0h             |    | 0h            | 0h          |    | 0h          |    |
| 7                | 6              | 5  | 4             | 3           | 2  | 1           | 0  |
| CTR_REG_ERR      | PARITY_ERR     |    | ECC_OTHER     | ECC_DED     |    | ECC_SEC     |    |
| R/W1TS           | R/W1TS         |    | R/W1TS        | R/WI        |    | R/WI        |    |
| 0h               | 0h             |    | 0h            | 0h          |    | 0h          |    |

**Table 4-277. ECC\_AGG\_CORE1\_ERROR\_STATUS1 Register Field Descriptions**

| Bit   | Field            | Type   | Reset | Description                                                                                      |
|-------|------------------|--------|-------|--------------------------------------------------------------------------------------------------|
| 31:16 | ECC_BIT1         | R      | 0h    | Data bit that corresponds to the single-bit error                                                |
| 15    | CLR_CTRL_REG_ERR | R/W1TC | 0h    | Clear control reg Error Status, you must also re write the control register itself to clear this |
| 14:13 | CLR_PARITY_ERR   | R/WD   | 0h    | Clear parity Error Status                                                                        |
| 12    | CLR_ECC_OTHER    | R/W1TC | 0h    | Clear other Error Status                                                                         |
| 11:10 | CLR_ECC_DED      | R/WD   | 0h    | Clear Double Bit Error Status                                                                    |
| 9:8   | CLR_ECC_SEC      | R/WD   | 0h    | Clear Single Bit Error Status                                                                    |
| 7     | CTR_REG_ERR      | R/W1TS | 0h    | control register error pending, Level interrupt                                                  |
| 6:5   | PARITY_ERR       | R/W1TS | 0h    | Level parity error Error Status                                                                  |
| 4     | ECC_OTHER        | R/W1TS | 0h    | Successive single-bit errors have occurred while a writeback is still pending, Level interrupt   |
| 3:2   | ECC_DED          | R/WI   | 0h    | Level Double Bit Error Status                                                                    |
| 1:0   | ECC_SEC          | R/WI   | 0h    | Level Single Bit Error Status                                                                    |

#### 4.1.2.87 ECC\_AGG\_CORE1\_ERROR\_STATUS2 Register

##### 1 ECC\_AGG\_CORE1\_ERROR\_STATUS2 Register (Offset = 24h) [reset = 0h]

ECC Error Status2 Register.

Return to [Summary Table](#)

**Table 4-278. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 3024h       |
| R5SS1         | 5300 7024h       |

**Figure 4-87. ECC\_AGG\_CORE1\_ERROR\_STATUS2 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ECC_ROW |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ECC_ROW |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ECC_ROW |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ECC_ROW |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-280. ECC\_AGG\_CORE1\_ERROR\_STATUS2 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                   |
|------|---------|------|-------|---------------------------------------------------------------|
| 31:0 | ECC_ROW | R    | 0h    | Row address where the single or double-bit error has occurred |

#### 4.1.2.88 ECC\_AGG\_CORE1\_ERROR\_STATUS3 Register

##### 1 ECC\_AGG\_CORE1\_ERROR\_STATUS3 Register (Offset = 28h) [reset = 0h]

ECC Error Status3 Register.

Return to [Summary Table](#)

**Table 4-281. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 3028h       |
| R5SS1         | 5300 7028h       |

**Figure 4-88. ECC\_AGG\_CORE1\_ERROR\_STATUS3 Name Register**

|          |    |    |    |    |    |                           |          |
|----------|----|----|----|----|----|---------------------------|----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25                        | 24       |
| RESERVED |    |    |    |    |    |                           |          |
| NONE     |    |    |    |    |    |                           |          |
| 0h       |    |    |    |    |    |                           |          |
| 23       | 22 | 21 | 20 | 19 | 18 | 17                        | 16       |
| RESERVED |    |    |    |    |    |                           |          |
| NONE     |    |    |    |    |    |                           |          |
| 0h       |    |    |    |    |    |                           |          |
| 15       | 14 | 13 | 12 | 11 | 10 | 9                         | 8        |
| RESERVED |    |    |    |    |    | CLR_SVBUS_T<br>IMEOUT_ERR | RESERVED |
| NONE     |    |    |    |    |    | R/W1TC                    | NONE     |
| 0h       |    |    |    |    |    | 0h                        | 0h       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1                         | 0        |
| RESERVED |    |    |    |    |    | SVBUS_TIMEO<br>UT_ERR     | WB_PEND  |
| NONE     |    |    |    |    |    | R/W1TS                    | R        |
| 0h       |    |    |    |    |    | 0h                        | 0h       |

**Table 4-283. ECC\_AGG\_CORE1\_ERROR\_STATUS3 Register Field Descriptions**

| Bit   | Field                 | Type   | Reset | Description                            |
|-------|-----------------------|--------|-------|----------------------------------------|
| 31:10 | RESERVED              | NONE   | 0h    | Reserved                               |
| 9     | CLR_SVBUS_TIMEOUT_ERR | R/W1TC | 0h    | Clear svbus timeout Error Status       |
| 8:2   | RESERVED              | NONE   | 0h    | Reserved                               |
| 1     | SVBUS_TIMEOUT_ERR     | R/W1TS | 0h    | Level svbus timeout error Error Status |
| 0     | WB_PEND               | R      | 0h    | delayed write back pending Status      |

#### 4.1.2.89 ECC\_AGG\_CORE1\_SEC\_EOI\_REG Register

##### 1 ECC\_AGG\_CORE1\_SEC\_EOI\_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register.

Return to [Summary Table](#)

**Table 4-284. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 303Ch       |
| R5SS1         | 5300 703Ch       |

**Figure 4-89. ECC\_AGG\_CORE1\_SEC\_EOI\_REG Name Register**

|          |    |    |    |    |    |    |        |
|----------|----|----|----|----|----|----|--------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24     |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16     |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8      |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0      |
| RESERVED |    |    |    |    |    |    | EOI_WR |
| NONE     |    |    |    |    |    |    | R/W1TS |
| 0h       |    |    |    |    |    |    | 0h     |

**Table 4-286. ECC\_AGG\_CORE1\_SEC\_EOI\_REG Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description                                                                                                                                                                                     |
|------|----------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED | NONE   | 0h    | Reserved                                                                                                                                                                                        |
| 0    | EOI_WR   | R/W1TS | 0h    | Write of 1 to this register indicates that software has acknowledged the pending interrupt and the next interrupt can be sent to the host. The bit is self clearing and will be read as a zero. |

#### 4.1.2.90 ECC\_AGG\_CORE1\_SEC\_STATUS\_REG0 Register

##### 1 ECC\_AGG\_CORE1\_SEC\_STATUS\_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

Return to [Summary Table](#)

**Table 4-287. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 3040h       |
| R5SS1         | 5300 7040h       |

**Figure 4-90. ECC\_AGG\_CORE1\_SEC\_STATUS\_REG0 Name Register**

| 31                    | 30                    | 29                    | 28                    | 27                      | 26                   | 25                   | 24                   |
|-----------------------|-----------------------|-----------------------|-----------------------|-------------------------|----------------------|----------------------|----------------------|
| RESERVED              |                       |                       |                       | CPU1_KS_VIM_RAMECC_PEND | B1TCM1_BANK1_PEND    | B1TCM1_BANK0_PEND    | B0TCM1_BANK1_PEND    |
| NONE                  |                       |                       |                       | R/W1TS                  | R/W1TS               | R/W1TS               | R/W1TS               |
| 0h                    |                       |                       |                       | 0h                      | 0h                   | 0h                   | 0h                   |
| 23                    | 22                    | 21                    | 20                    | 19                      | 18                   | 17                   | 16                   |
| B0TCM1_BANK0_PEND     | ATCM1_BANK1_PEND      | ATCM1_BANK0_PEND      | CPU1_DDATA_RAM7_PEND  | CPU1_DDATA_RAM6_PEND    | CPU1_DDATA_RAM5_PEND | CPU1_DDATA_RAM4_PEND | CPU1_DDATA_RAM3_PEND |
| R/W1TS                | R/W1TS                | R/W1TS                | R/W1TS                | R/W1TS                  | R/W1TS               | R/W1TS               | R/W1TS               |
| 0h                    | 0h                    | 0h                    | 0h                    | 0h                      | 0h                   | 0h                   | 0h                   |
| 15                    | 14                    | 13                    | 12                    | 11                      | 10                   | 9                    | 8                    |
| CPU1_DDATA_RAM2_PEND  | CPU1_DDATA_RAM1_PEND  | CPU1_DDATA_RAM0_PEND  | CPU1_DDIRTY_RAM_PEND  | CPU1_DTAG_RAM3_PEND     | CPU1_DTAG_RAM2_PEND  | CPU1_DTAG_RAM1_PEND  | CPU1_DTAG_RAM0_PEND  |
| R/W1TS                | R/W1TS                | R/W1TS                | R/W1TS                | R/W1TS                  | R/W1TS               | R/W1TS               | R/W1TS               |
| 0h                    | 0h                    | 0h                    | 0h                    | 0h                      | 0h                   | 0h                   | 0h                   |
| 7                     | 6                     | 5                     | 4                     | 3                       | 2                    | 1                    | 0                    |
| CPU1_IDATA_BANK3_PEND | CPU1_IDATA_BANK2_PEND | CPU1_IDATA_BANK1_PEND | CPU1_IDATA_BANK0_PEND | CPU1_ITAG_RAM3_PEND     | CPU1_ITAG_RAM2_PEND  | CPU1_ITAG_RAM1_PEND  | CPU1_ITAG_RAM0_PEND  |
| R/W1TS                | R/W1TS                | R/W1TS                | R/W1TS                | R/W1TS                  | R/W1TS               | R/W1TS               | R/W1TS               |
| 0h                    | 0h                    | 0h                    | 0h                    | 0h                      | 0h                   | 0h                   | 0h                   |

**Table 4-289. ECC\_AGG\_CORE1\_SEC\_STATUS\_REG0 Register Field Descriptions**

| Bit   | Field                   | Type   | Reset | Description                                          |
|-------|-------------------------|--------|-------|------------------------------------------------------|
| 31:28 | RESERVED                | NONE   | 0h    | Reserved                                             |
| 27    | CPU1_KS_VIM_RAMECC_PEND | R/W1TS | 0h    | Interrupt Pending Status for cpu1_ks_vim_ramecc_pend |
| 26    | B1TCM1_BANK1_PEND       | R/W1TS | 0h    | Interrupt Pending Status for b1tcm1_bank1_pend       |
| 25    | B1TCM1_BANK0_PEND       | R/W1TS | 0h    | Interrupt Pending Status for b1tcm1_bank0_pend       |
| 24    | B0TCM1_BANK1_PEND       | R/W1TS | 0h    | Interrupt Pending Status for b0tcm1_bank1_pend       |
| 23    | B0TCM1_BANK0_PEND       | R/W1TS | 0h    | Interrupt Pending Status for b0tcm1_bank0_pend       |
| 22    | ATCM1_BANK1_PEND        | R/W1TS | 0h    | Interrupt Pending Status for atcm1_bank1_pend        |
| 21    | ATCM1_BANK0_PEND        | R/W1TS | 0h    | Interrupt Pending Status for atcm1_bank0_pend        |
| 20    | CPU1_DDATA_RAM7_PEND    | R/W1TS | 0h    | Interrupt Pending Status for cpu1_ddata_ram7_pend    |
| 19    | CPU1_DDATA_RAM6_PEND    | R/W1TS | 0h    | Interrupt Pending Status for cpu1_ddata_ram6_pend    |
| 18    | CPU1_DDATA_RAM5_PEND    | R/W1TS | 0h    | Interrupt Pending Status for cpu1_ddata_ram5_pend    |



**Table 4-289. ECC\_AGG\_CORE1\_SEC\_STATUS\_REG0 Register Field Descriptions (continued)**

| Bit | Field                 | Type   | Reset | Description                                        |
|-----|-----------------------|--------|-------|----------------------------------------------------|
| 17  | CPU1_DDATA_RAM4_PEND  | R/W1TS | 0h    | Interrupt Pending Status for cpu1_ddata_ram4_pend  |
| 16  | CPU1_DDATA_RAM3_PEND  | R/W1TS | 0h    | Interrupt Pending Status for cpu1_ddata_ram3_pend  |
| 15  | CPU1_DDATA_RAM2_PEND  | R/W1TS | 0h    | Interrupt Pending Status for cpu1_ddata_ram2_pend  |
| 14  | CPU1_DDATA_RAM1_PEND  | R/W1TS | 0h    | Interrupt Pending Status for cpu1_ddata_ram1_pend  |
| 13  | CPU1_DDATA_RAM0_PEND  | R/W1TS | 0h    | Interrupt Pending Status for cpu1_ddata_ram0_pend  |
| 12  | CPU1_DDIRTY_RAM_PEND  | R/W1TS | 0h    | Interrupt Pending Status for cpu1_ddirty_ram_pend  |
| 11  | CPU1_DTAG_RAM3_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu1_dtag_ram3_pend   |
| 10  | CPU1_DTAG_RAM2_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu1_dtag_ram2_pend   |
| 9   | CPU1_DTAG_RAM1_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu1_dtag_ram1_pend   |
| 8   | CPU1_DTAG_RAM0_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu1_dtag_ram0_pend   |
| 7   | CPU1_IDATA_BANK3_PEND | R/W1TS | 0h    | Interrupt Pending Status for cpu1_idata_bank3_pend |
| 6   | CPU1_IDATA_BANK2_PEND | R/W1TS | 0h    | Interrupt Pending Status for cpu1_idata_bank2_pend |
| 5   | CPU1_IDATA_BANK1_PEND | R/W1TS | 0h    | Interrupt Pending Status for cpu1_idata_bank1_pend |
| 4   | CPU1_IDATA_BANK0_PEND | R/W1TS | 0h    | Interrupt Pending Status for cpu1_idata_bank0_pend |
| 3   | CPU1_ITAG_RAM3_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu1_itag_ram3_pend   |
| 2   | CPU1_ITAG_RAM2_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu1_itag_ram2_pend   |
| 1   | CPU1_ITAG_RAM1_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu1_itag_ram1_pend   |
| 0   | CPU1_ITAG_RAM0_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu1_itag_ram0_pend   |

#### 4.1.2.91 ECC\_AGG\_CORE1\_SEC\_ENABLE\_SET\_REG0 Register

##### 1 ECC\_AGG\_CORE1\_SEC\_ENABLE\_SET\_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

Return to [Summary Table](#)

**Table 4-290. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 3080h       |
| R5SS1         | 5300 7080h       |

**Figure 4-91. ECC\_AGG\_CORE1\_SEC\_ENABLE\_SET\_REG0 Name Register**

| 31                          | 30                          | 29                          | 28                          | 27                            | 26                         | 25                         | 24                         |
|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-------------------------------|----------------------------|----------------------------|----------------------------|
| RESERVED                    |                             |                             |                             | CPU1_KS_VIM_RAMECC_ENABLE_SET | B1TCM1_BANK1_ENABLE_SET    | B1TCM1_BANK0_ENABLE_SET    | B0TCM1_BANK1_ENABLE_SET    |
| NONE                        |                             |                             |                             | R/W1TS                        | R/W1TS                     | R/W1TS                     | R/W1TS                     |
| 0h                          |                             |                             |                             | 0h                            | 0h                         | 0h                         | 0h                         |
| 23                          | 22                          | 21                          | 20                          | 19                            | 18                         | 17                         | 16                         |
| B0TCM1_BANK0_ENABLE_SET     | ATCM1_BANK1_ENABLE_SET      | ATCM1_BANK0_ENABLE_SET      | CPU1_DDATA_RAM7_ENABLE_SET  | CPU1_DDATA_RAM6_ENABLE_SET    | CPU1_DDATA_RAM5_ENABLE_SET | CPU1_DDATA_RAM4_ENABLE_SET | CPU1_DDATA_RAM3_ENABLE_SET |
| R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                        | R/W1TS                     | R/W1TS                     | R/W1TS                     |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                            | 0h                         | 0h                         | 0h                         |
| 15                          | 14                          | 13                          | 12                          | 11                            | 10                         | 9                          | 8                          |
| CPU1_DDATA_RAM2_ENABLE_SET  | CPU1_DDATA_RAM1_ENABLE_SET  | CPU1_DDATA_RAM0_ENABLE_SET  | CPU1_DDIRTY_RAM_ENABLE_SET  | CPU1_DTAG_RAM3_ENABLE_SET     | CPU1_DTAG_RAM2_ENABLE_SET  | CPU1_DTAG_RAM1_ENABLE_SET  | CPU1_DTAG_RAM0_ENABLE_SET  |
| R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                        | R/W1TS                     | R/W1TS                     | R/W1TS                     |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                            | 0h                         | 0h                         | 0h                         |
| 7                           | 6                           | 5                           | 4                           | 3                             | 2                          | 1                          | 0                          |
| CPU1_IDATA_BANK3_ENABLE_SET | CPU1_IDATA_BANK2_ENABLE_SET | CPU1_IDATA_BANK1_ENABLE_SET | CPU1_IDATA_BANK0_ENABLE_SET | CPU1_ITAG_RAM3_ENABLE_SET     | CPU1_ITAG_RAM2_ENABLE_SET  | CPU1_ITAG_RAM1_ENABLE_SET  | CPU1_ITAG_RAM0_ENABLE_SET  |
| R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                        | R/W1TS                     | R/W1TS                     | R/W1TS                     |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                            | 0h                         | 0h                         | 0h                         |

**Table 4-292. ECC\_AGG\_CORE1\_SEC\_ENABLE\_SET\_REG0 Register Field Descriptions**

| Bit   | Field                         | Type   | Reset | Description                                               |
|-------|-------------------------------|--------|-------|-----------------------------------------------------------|
| 31:28 | RESERVED                      | NONE   | 0h    | Reserved                                                  |
| 27    | CPU1_KS_VIM_RAMECC_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_ks_vim_ramecc_pend |
| 26    | B1TCM1_BANK1_ENABLE_SET       | R/W1TS | 0h    | Interrupt Enable Set Register for b1tcm1_bank1_pend       |
| 25    | B1TCM1_BANK0_ENABLE_SET       | R/W1TS | 0h    | Interrupt Enable Set Register for b1tcm1_bank0_pend       |
| 24    | B0TCM1_BANK1_ENABLE_SET       | R/W1TS | 0h    | Interrupt Enable Set Register for b0tcm1_bank1_pend       |
| 23    | B0TCM1_BANK0_ENABLE_SET       | R/W1TS | 0h    | Interrupt Enable Set Register for b0tcm1_bank0_pend       |
| 22    | ATCM1_BANK1_ENABLE_SET        | R/W1TS | 0h    | Interrupt Enable Set Register for atcm1_bank1_pend        |

**Table 4-292. ECC\_AGG\_CORE1\_SEC\_ENABLE\_SET\_REG0 Register Field Descriptions (continued)**

| Bit | Field                       | Type   | Reset | Description                                             |
|-----|-----------------------------|--------|-------|---------------------------------------------------------|
| 21  | ATCM1_BANK0_ENABLE_SET      | R/W1TS | 0h    | Interrupt Enable Set Register for atcm1_bank0_pend      |
| 20  | CPU1_DDATA_RAM7_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_ddata_ram7_pend  |
| 19  | CPU1_DDATA_RAM6_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_ddata_ram6_pend  |
| 18  | CPU1_DDATA_RAM5_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_ddata_ram5_pend  |
| 17  | CPU1_DDATA_RAM4_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_ddata_ram4_pend  |
| 16  | CPU1_DDATA_RAM3_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_ddata_ram3_pend  |
| 15  | CPU1_DDATA_RAM2_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_ddata_ram2_pend  |
| 14  | CPU1_DDATA_RAM1_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_ddata_ram1_pend  |
| 13  | CPU1_DDATA_RAM0_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_ddata_ram0_pend  |
| 12  | CPU1_DDIRTY_RAM_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_ddirty_ram_pend  |
| 11  | CPU1_DTAG_RAM3_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_dtag_ram3_pend   |
| 10  | CPU1_DTAG_RAM2_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_dtag_ram2_pend   |
| 9   | CPU1_DTAG_RAM1_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_dtag_ram1_pend   |
| 8   | CPU1_DTAG_RAM0_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_dtag_ram0_pend   |
| 7   | CPU1_IDATA_BANK3_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_idata_bank3_pend |
| 6   | CPU1_IDATA_BANK2_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_idata_bank2_pend |
| 5   | CPU1_IDATA_BANK1_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_idata_bank1_pend |
| 4   | CPU1_IDATA_BANK0_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_idata_bank0_pend |
| 3   | CPU1_ITAG_RAM3_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_itag_ram3_pend   |
| 2   | CPU1_ITAG_RAM2_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_itag_ram2_pend   |
| 1   | CPU1_ITAG_RAM1_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_itag_ram1_pend   |
| 0   | CPU1_ITAG_RAM0_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_itag_ram0_pend   |

#### 4.1.2.92 ECC\_AGG\_CORE1\_SEC\_ENABLE\_CLR\_REG0 Register

##### 1 ECC\_AGG\_CORE1\_SEC\_ENABLE\_CLR\_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to [Summary Table](#)

**Table 4-293. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 30C0h       |
| R5SS1         | 5300 70C0h       |

**Figure 4-92. ECC\_AGG\_CORE1\_SEC\_ENABLE\_CLR\_REG0 Name Register**

| 31                          | 30                          | 29                          | 28                          | 27                            | 26                         | 25                         | 24                         |
|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-------------------------------|----------------------------|----------------------------|----------------------------|
| RESERVED                    |                             |                             |                             | CPU1_KS_VIM_RAMECC_ENABLE_CLR | B1TCM1_BANK1_ENABLE_CLR    | B1TCM1_BANK0_ENABLE_CLR    | B0TCM1_BANK1_ENABLE_CLR    |
| NONE                        |                             |                             |                             | R/W1TC                        | R/W1TC                     | R/W1TC                     | R/W1TC                     |
| 0h                          |                             |                             |                             | 0h                            | 0h                         | 0h                         | 0h                         |
| 23                          | 22                          | 21                          | 20                          | 19                            | 18                         | 17                         | 16                         |
| B0TCM1_BANK0_ENABLE_CLR     | ATCM1_BANK1_ENABLE_CLR      | ATCM1_BANK0_ENABLE_CLR      | CPU1_DDATA_RAM7_ENABLE_CLR  | CPU1_DDATA_RAM6_ENABLE_CLR    | CPU1_DDATA_RAM5_ENABLE_CLR | CPU1_DDATA_RAM4_ENABLE_CLR | CPU1_DDATA_RAM3_ENABLE_CLR |
| R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                        | R/W1TC                     | R/W1TC                     | R/W1TC                     |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                            | 0h                         | 0h                         | 0h                         |
| 15                          | 14                          | 13                          | 12                          | 11                            | 10                         | 9                          | 8                          |
| CPU1_DDATA_RAM2_ENABLE_CLR  | CPU1_DDATA_RAM1_ENABLE_CLR  | CPU1_DDATA_RAM0_ENABLE_CLR  | CPU1_DDIRTY_RAM_ENABLE_CLR  | CPU1_DTAG_RAM3_ENABLE_CLR     | CPU1_DTAG_RAM2_ENABLE_CLR  | CPU1_DTAG_RAM1_ENABLE_CLR  | CPU1_DTAG_RAM0_ENABLE_CLR  |
| R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                        | R/W1TC                     | R/W1TC                     | R/W1TC                     |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                            | 0h                         | 0h                         | 0h                         |
| 7                           | 6                           | 5                           | 4                           | 3                             | 2                          | 1                          | 0                          |
| CPU1_IDATA_BANK3_ENABLE_CLR | CPU1_IDATA_BANK2_ENABLE_CLR | CPU1_IDATA_BANK1_ENABLE_CLR | CPU1_IDATA_BANK0_ENABLE_CLR | CPU1_ITAG_RAM3_ENABLE_CLR     | CPU1_ITAG_RAM2_ENABLE_CLR  | CPU1_ITAG_RAM1_ENABLE_CLR  | CPU1_ITAG_RAM0_ENABLE_CLR  |
| R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                        | R/W1TC                     | R/W1TC                     | R/W1TC                     |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                            | 0h                         | 0h                         | 0h                         |

**Table 4-295. ECC\_AGG\_CORE1\_SEC\_ENABLE\_CLR\_REG0 Register Field Descriptions**

| Bit   | Field                         | Type   | Reset | Description                                                 |
|-------|-------------------------------|--------|-------|-------------------------------------------------------------|
| 31:28 | RESERVED                      | NONE   | 0h    | Reserved                                                    |
| 27    | CPU1_KS_VIM_RAMECC_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_ks_vim_ramecc_pend |
| 26    | B1TCM1_BANK1_ENABLE_CLR       | R/W1TC | 0h    | Interrupt Enable Clear Register for b1tcm1_bank1_pend       |
| 25    | B1TCM1_BANK0_ENABLE_CLR       | R/W1TC | 0h    | Interrupt Enable Clear Register for b1tcm1_bank0_pend       |
| 24    | B0TCM1_BANK1_ENABLE_CLR       | R/W1TC | 0h    | Interrupt Enable Clear Register for b0tcm1_bank1_pend       |
| 23    | B0TCM1_BANK0_ENABLE_CLR       | R/W1TC | 0h    | Interrupt Enable Clear Register for b0tcm1_bank0_pend       |
| 22    | ATCM1_BANK1_ENABLE_CLR        | R/W1TC | 0h    | Interrupt Enable Clear Register for atcm1_bank1_pend        |

**Table 4-295. ECC\_AGG\_CORE1\_SEC\_ENABLE\_CLR\_REG0 Register Field Descriptions (continued)**

| Bit | Field                       | Type   | Reset | Description                                               |
|-----|-----------------------------|--------|-------|-----------------------------------------------------------|
| 21  | ATCM1_BANK0_ENABLE_CLR      | R/W1TC | 0h    | Interrupt Enable Clear Register for atcm1_bank0_pend      |
| 20  | CPU1_DDATA_RAM7_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_ddata_ram7_pend  |
| 19  | CPU1_DDATA_RAM6_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_ddata_ram6_pend  |
| 18  | CPU1_DDATA_RAM5_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_ddata_ram5_pend  |
| 17  | CPU1_DDATA_RAM4_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_ddata_ram4_pend  |
| 16  | CPU1_DDATA_RAM3_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_ddata_ram3_pend  |
| 15  | CPU1_DDATA_RAM2_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_ddata_ram2_pend  |
| 14  | CPU1_DDATA_RAM1_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_ddata_ram1_pend  |
| 13  | CPU1_DDATA_RAM0_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_ddata_ram0_pend  |
| 12  | CPU1_DDIRTY_RAM_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_ddirty_ram_pend  |
| 11  | CPU1_DTAG_RAM3_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_dtag_ram3_pend   |
| 10  | CPU1_DTAG_RAM2_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_dtag_ram2_pend   |
| 9   | CPU1_DTAG_RAM1_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_dtag_ram1_pend   |
| 8   | CPU1_DTAG_RAM0_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_dtag_ram0_pend   |
| 7   | CPU1_IDATA_BANK3_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_idata_bank3_pend |
| 6   | CPU1_IDATA_BANK2_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_idata_bank2_pend |
| 5   | CPU1_IDATA_BANK1_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_idata_bank1_pend |
| 4   | CPU1_IDATA_BANK0_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_idata_bank0_pend |
| 3   | CPU1_ITAG_RAM3_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_itag_ram3_pend   |
| 2   | CPU1_ITAG_RAM2_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_itag_ram2_pend   |
| 1   | CPU1_ITAG_RAM1_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_itag_ram1_pend   |
| 0   | CPU1_ITAG_RAM0_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_itag_ram0_pend   |

#### 4.1.2.93 ECC\_AGG\_CORE1\_DED\_EOI\_REG Register

##### 1 ECC\_AGG\_CORE1\_DED\_EOI\_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register.

Return to [Summary Table](#)

**Table 4-296. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 313Ch       |
| R5SS1         | 5300 713Ch       |

**Figure 4-93. ECC\_AGG\_CORE1\_DED\_EOI\_REG Name Register**

|          |    |    |    |    |    |    |        |
|----------|----|----|----|----|----|----|--------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24     |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16     |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8      |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0      |
| RESERVED |    |    |    |    |    |    | EOI_WR |
| NONE     |    |    |    |    |    |    | R/W1TS |
| 0h       |    |    |    |    |    |    | 0h     |

**Table 4-298. ECC\_AGG\_CORE1\_DED\_EOI\_REG Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description                                                                                                                                                                                     |
|------|----------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED | NONE   | 0h    | Reserved                                                                                                                                                                                        |
| 0    | EOI_WR   | R/W1TS | 0h    | Write of 1 to this register indicates that software has acknowledged the pending interrupt and the next interrupt can be sent to the host. The bit is self clearing and will be read as a zero. |

#### 4.1.2.94 ECC\_AGG\_CORE1\_DED\_STATUS\_REG0 Register

##### 1 ECC\_AGG\_CORE1\_DED\_STATUS\_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

Return to [Summary Table](#)

**Table 4-299. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 3140h       |
| R5SS1         | 5300 7140h       |

**Figure 4-94. ECC\_AGG\_CORE1\_DED\_STATUS\_REG0 Name Register**

| 31                    | 30                    | 29                    | 28                    | 27                      | 26                   | 25                   | 24                   |
|-----------------------|-----------------------|-----------------------|-----------------------|-------------------------|----------------------|----------------------|----------------------|
| RESERVED              |                       |                       |                       | CPU1_KS_VIM_RAMECC_PEND | B1TCM1_BANK1_PEND    | B1TCM1_BANK0_PEND    | B0TCM1_BANK1_PEND    |
| NONE                  |                       |                       |                       | R/W1TS                  | R/W1TS               | R/W1TS               | R/W1TS               |
| 0h                    |                       |                       |                       | 0h                      | 0h                   | 0h                   | 0h                   |
| 23                    | 22                    | 21                    | 20                    | 19                      | 18                   | 17                   | 16                   |
| B0TCM1_BANK0_PEND     | ATCM1_BANK1_PEND      | ATCM1_BANK0_PEND      | CPU1_DDATA_RAM7_PEND  | CPU1_DDATA_RAM6_PEND    | CPU1_DDATA_RAM5_PEND | CPU1_DDATA_RAM4_PEND | CPU1_DDATA_RAM3_PEND |
| R/W1TS                | R/W1TS                | R/W1TS                | R/W1TS                | R/W1TS                  | R/W1TS               | R/W1TS               | R/W1TS               |
| 0h                    | 0h                    | 0h                    | 0h                    | 0h                      | 0h                   | 0h                   | 0h                   |
| 15                    | 14                    | 13                    | 12                    | 11                      | 10                   | 9                    | 8                    |
| CPU1_DDATA_RAM2_PEND  | CPU1_DDATA_RAM1_PEND  | CPU1_DDATA_RAM0_PEND  | CPU1_DDIRTY_RAM_PEND  | CPU1_DTAG_RAM3_PEND     | CPU1_DTAG_RAM2_PEND  | CPU1_DTAG_RAM1_PEND  | CPU1_DTAG_RAM0_PEND  |
| R/W1TS                | R/W1TS                | R/W1TS                | R/W1TS                | R/W1TS                  | R/W1TS               | R/W1TS               | R/W1TS               |
| 0h                    | 0h                    | 0h                    | 0h                    | 0h                      | 0h                   | 0h                   | 0h                   |
| 7                     | 6                     | 5                     | 4                     | 3                       | 2                    | 1                    | 0                    |
| CPU1_IDATA_BANK3_PEND | CPU1_IDATA_BANK2_PEND | CPU1_IDATA_BANK1_PEND | CPU1_IDATA_BANK0_PEND | CPU1_ITAG_RAM3_PEND     | CPU1_ITAG_RAM2_PEND  | CPU1_ITAG_RAM1_PEND  | CPU1_ITAG_RAM0_PEND  |
| R/W1TS                | R/W1TS                | R/W1TS                | R/W1TS                | R/W1TS                  | R/W1TS               | R/W1TS               | R/W1TS               |
| 0h                    | 0h                    | 0h                    | 0h                    | 0h                      | 0h                   | 0h                   | 0h                   |

**Table 4-301. ECC\_AGG\_CORE1\_DED\_STATUS\_REG0 Register Field Descriptions**

| Bit   | Field                   | Type   | Reset | Description                                          |
|-------|-------------------------|--------|-------|------------------------------------------------------|
| 31:28 | RESERVED                | NONE   | 0h    | Reserved                                             |
| 27    | CPU1_KS_VIM_RAMECC_PEND | R/W1TS | 0h    | Interrupt Pending Status for cpu1_ks_vim_ramecc_pend |
| 26    | B1TCM1_BANK1_PEND       | R/W1TS | 0h    | Interrupt Pending Status for b1tcm1_bank1_pend       |
| 25    | B1TCM1_BANK0_PEND       | R/W1TS | 0h    | Interrupt Pending Status for b1tcm1_bank0_pend       |
| 24    | B0TCM1_BANK1_PEND       | R/W1TS | 0h    | Interrupt Pending Status for b0tcm1_bank1_pend       |
| 23    | B0TCM1_BANK0_PEND       | R/W1TS | 0h    | Interrupt Pending Status for b0tcm1_bank0_pend       |
| 22    | ATCM1_BANK1_PEND        | R/W1TS | 0h    | Interrupt Pending Status for atcm1_bank1_pend        |
| 21    | ATCM1_BANK0_PEND        | R/W1TS | 0h    | Interrupt Pending Status for atcm1_bank0_pend        |
| 20    | CPU1_DDATA_RAM7_PEND    | R/W1TS | 0h    | Interrupt Pending Status for cpu1_ddata_ram7_pend    |
| 19    | CPU1_DDATA_RAM6_PEND    | R/W1TS | 0h    | Interrupt Pending Status for cpu1_ddata_ram6_pend    |
| 18    | CPU1_DDATA_RAM5_PEND    | R/W1TS | 0h    | Interrupt Pending Status for cpu1_ddata_ram5_pend    |

**Table 4-301. ECC\_AGG\_CORE1\_DED\_STATUS\_REG0 Register Field Descriptions (continued)**

| Bit | Field                 | Type   | Reset | Description                                        |
|-----|-----------------------|--------|-------|----------------------------------------------------|
| 17  | CPU1_DDATA_RAM4_PEND  | R/W1TS | 0h    | Interrupt Pending Status for cpu1_ddata_ram4_pend  |
| 16  | CPU1_DDATA_RAM3_PEND  | R/W1TS | 0h    | Interrupt Pending Status for cpu1_ddata_ram3_pend  |
| 15  | CPU1_DDATA_RAM2_PEND  | R/W1TS | 0h    | Interrupt Pending Status for cpu1_ddata_ram2_pend  |
| 14  | CPU1_DDATA_RAM1_PEND  | R/W1TS | 0h    | Interrupt Pending Status for cpu1_ddata_ram1_pend  |
| 13  | CPU1_DDATA_RAM0_PEND  | R/W1TS | 0h    | Interrupt Pending Status for cpu1_ddata_ram0_pend  |
| 12  | CPU1_DDIRTY_RAM_PEND  | R/W1TS | 0h    | Interrupt Pending Status for cpu1_ddirty_ram_pend  |
| 11  | CPU1_DTAG_RAM3_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu1_dtag_ram3_pend   |
| 10  | CPU1_DTAG_RAM2_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu1_dtag_ram2_pend   |
| 9   | CPU1_DTAG_RAM1_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu1_dtag_ram1_pend   |
| 8   | CPU1_DTAG_RAM0_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu1_dtag_ram0_pend   |
| 7   | CPU1_IDATA_BANK3_PEND | R/W1TS | 0h    | Interrupt Pending Status for cpu1_idata_bank3_pend |
| 6   | CPU1_IDATA_BANK2_PEND | R/W1TS | 0h    | Interrupt Pending Status for cpu1_idata_bank2_pend |
| 5   | CPU1_IDATA_BANK1_PEND | R/W1TS | 0h    | Interrupt Pending Status for cpu1_idata_bank1_pend |
| 4   | CPU1_IDATA_BANK0_PEND | R/W1TS | 0h    | Interrupt Pending Status for cpu1_idata_bank0_pend |
| 3   | CPU1_ITAG_RAM3_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu1_itag_ram3_pend   |
| 2   | CPU1_ITAG_RAM2_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu1_itag_ram2_pend   |
| 1   | CPU1_ITAG_RAM1_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu1_itag_ram1_pend   |
| 0   | CPU1_ITAG_RAM0_PEND   | R/W1TS | 0h    | Interrupt Pending Status for cpu1_itag_ram0_pend   |



#### 4.1.2.95 ECC\_AGG\_CORE1\_DED\_ENABLE\_SET\_REG0 Register

##### 1 ECC\_AGG\_CORE1\_DED\_ENABLE\_SET\_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

Return to [Summary Table](#)

**Table 4-302. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 3180h       |
| R5SS1         | 5300 7180h       |

**Figure 4-95. ECC\_AGG\_CORE1\_DED\_ENABLE\_SET\_REG0 Name Register**

| 31                          | 30                          | 29                          | 28                          | 27                            | 26                         | 25                         | 24                         |
|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-------------------------------|----------------------------|----------------------------|----------------------------|
| RESERVED                    |                             |                             |                             | CPU1_KS_VIM_RAMECC_ENABLE_SET | B1TCM1_BANK1_ENABLE_SET    | B1TCM1_BANK0_ENABLE_SET    | B0TCM1_BANK1_ENABLE_SET    |
| NONE                        |                             |                             |                             | R/W1TS                        | R/W1TS                     | R/W1TS                     | R/W1TS                     |
| 0h                          |                             |                             |                             | 0h                            | 0h                         | 0h                         | 0h                         |
| 23                          | 22                          | 21                          | 20                          | 19                            | 18                         | 17                         | 16                         |
| B0TCM1_BANK0_ENABLE_SET     | ATCM1_BANK1_ENABLE_SET      | ATCM1_BANK0_ENABLE_SET      | CPU1_DDATA_RAM7_ENABLE_SET  | CPU1_DDATA_RAM6_ENABLE_SET    | CPU1_DDATA_RAM5_ENABLE_SET | CPU1_DDATA_RAM4_ENABLE_SET | CPU1_DDATA_RAM3_ENABLE_SET |
| R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                        | R/W1TS                     | R/W1TS                     | R/W1TS                     |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                            | 0h                         | 0h                         | 0h                         |
| 15                          | 14                          | 13                          | 12                          | 11                            | 10                         | 9                          | 8                          |
| CPU1_DDATA_RAM2_ENABLE_SET  | CPU1_DDATA_RAM1_ENABLE_SET  | CPU1_DDATA_RAM0_ENABLE_SET  | CPU1_DDIRTY_RAM_ENABLE_SET  | CPU1_DTAG_RAM3_ENABLE_SET     | CPU1_DTAG_RAM2_ENABLE_SET  | CPU1_DTAG_RAM1_ENABLE_SET  | CPU1_DTAG_RAM0_ENABLE_SET  |
| R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                        | R/W1TS                     | R/W1TS                     | R/W1TS                     |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                            | 0h                         | 0h                         | 0h                         |
| 7                           | 6                           | 5                           | 4                           | 3                             | 2                          | 1                          | 0                          |
| CPU1_IDATA_BANK3_ENABLE_SET | CPU1_IDATA_BANK2_ENABLE_SET | CPU1_IDATA_BANK1_ENABLE_SET | CPU1_IDATA_BANK0_ENABLE_SET | CPU1_ITAG_RAM3_ENABLE_SET     | CPU1_ITAG_RAM2_ENABLE_SET  | CPU1_ITAG_RAM1_ENABLE_SET  | CPU1_ITAG_RAM0_ENABLE_SET  |
| R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                        | R/W1TS                     | R/W1TS                     | R/W1TS                     |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                            | 0h                         | 0h                         | 0h                         |

**Table 4-304. ECC\_AGG\_CORE1\_DED\_ENABLE\_SET\_REG0 Register Field Descriptions**

| Bit   | Field                         | Type   | Reset | Description                                               |
|-------|-------------------------------|--------|-------|-----------------------------------------------------------|
| 31:28 | RESERVED                      | NONE   | 0h    | Reserved                                                  |
| 27    | CPU1_KS_VIM_RAMECC_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_ks_vim_ramecc_pend |
| 26    | B1TCM1_BANK1_ENABLE_SET       | R/W1TS | 0h    | Interrupt Enable Set Register for b1tcm1_bank1_pend       |
| 25    | B1TCM1_BANK0_ENABLE_SET       | R/W1TS | 0h    | Interrupt Enable Set Register for b1tcm1_bank0_pend       |
| 24    | B0TCM1_BANK1_ENABLE_SET       | R/W1TS | 0h    | Interrupt Enable Set Register for b0tcm1_bank1_pend       |
| 23    | B0TCM1_BANK0_ENABLE_SET       | R/W1TS | 0h    | Interrupt Enable Set Register for b0tcm1_bank0_pend       |
| 22    | ATCM1_BANK1_ENABLE_SET        | R/W1TS | 0h    | Interrupt Enable Set Register for atcm1_bank1_pend        |

**Table 4-304. ECC\_AGG\_CORE1\_DED\_ENABLE\_SET\_REG0 Register Field Descriptions (continued)**

| Bit | Field                       | Type   | Reset | Description                                             |
|-----|-----------------------------|--------|-------|---------------------------------------------------------|
| 21  | ATCM1_BANK0_ENABLE_SET      | R/W1TS | 0h    | Interrupt Enable Set Register for atcm1_bank0_pend      |
| 20  | CPU1_DDATA_RAM7_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_ddata_ram7_pend  |
| 19  | CPU1_DDATA_RAM6_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_ddata_ram6_pend  |
| 18  | CPU1_DDATA_RAM5_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_ddata_ram5_pend  |
| 17  | CPU1_DDATA_RAM4_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_ddata_ram4_pend  |
| 16  | CPU1_DDATA_RAM3_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_ddata_ram3_pend  |
| 15  | CPU1_DDATA_RAM2_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_ddata_ram2_pend  |
| 14  | CPU1_DDATA_RAM1_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_ddata_ram1_pend  |
| 13  | CPU1_DDATA_RAM0_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_ddata_ram0_pend  |
| 12  | CPU1_DDIRTY_RAM_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_ddirty_ram_pend  |
| 11  | CPU1_DTAG_RAM3_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_dtag_ram3_pend   |
| 10  | CPU1_DTAG_RAM2_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_dtag_ram2_pend   |
| 9   | CPU1_DTAG_RAM1_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_dtag_ram1_pend   |
| 8   | CPU1_DTAG_RAM0_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_dtag_ram0_pend   |
| 7   | CPU1_IDATA_BANK3_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_idata_bank3_pend |
| 6   | CPU1_IDATA_BANK2_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_idata_bank2_pend |
| 5   | CPU1_IDATA_BANK1_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_idata_bank1_pend |
| 4   | CPU1_IDATA_BANK0_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_idata_bank0_pend |
| 3   | CPU1_ITAG_RAM3_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_itag_ram3_pend   |
| 2   | CPU1_ITAG_RAM2_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_itag_ram2_pend   |
| 1   | CPU1_ITAG_RAM1_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_itag_ram1_pend   |
| 0   | CPU1_ITAG_RAM0_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for cpu1_itag_ram0_pend   |

#### 4.1.2.96 ECC\_AGG\_CORE1\_DED\_ENABLE\_CLR\_REG0 Register

##### 1 ECC\_AGG\_CORE1\_DED\_ENABLE\_CLR\_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to [Summary Table](#)

**Table 4-305. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 31C0h       |
| R5SS1         | 5300 71C0h       |

**Figure 4-96. ECC\_AGG\_CORE1\_DED\_ENABLE\_CLR\_REG0 Name Register**

| 31                          | 30                          | 29                          | 28                          | 27                            | 26                         | 25                         | 24                         |
|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-------------------------------|----------------------------|----------------------------|----------------------------|
| RESERVED                    |                             |                             |                             | CPU1_KS_VIM_RAMECC_ENABLE_CLR | B1TCM1_BANK1_ENABLE_CLR    | B1TCM1_BANK0_ENABLE_CLR    | B0TCM1_BANK1_ENABLE_CLR    |
| NONE                        |                             |                             |                             | R/W1TC                        | R/W1TC                     | R/W1TC                     | R/W1TC                     |
| 0h                          |                             |                             |                             | 0h                            | 0h                         | 0h                         | 0h                         |
| 23                          | 22                          | 21                          | 20                          | 19                            | 18                         | 17                         | 16                         |
| B0TCM1_BANK0_ENABLE_CLR     | ATCM1_BANK1_ENABLE_CLR      | ATCM1_BANK0_ENABLE_CLR      | CPU1_DDATA_RAM7_ENABLE_CLR  | CPU1_DDATA_RAM6_ENABLE_CLR    | CPU1_DDATA_RAM5_ENABLE_CLR | CPU1_DDATA_RAM4_ENABLE_CLR | CPU1_DDATA_RAM3_ENABLE_CLR |
| R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                        | R/W1TC                     | R/W1TC                     | R/W1TC                     |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                            | 0h                         | 0h                         | 0h                         |
| 15                          | 14                          | 13                          | 12                          | 11                            | 10                         | 9                          | 8                          |
| CPU1_DDATA_RAM2_ENABLE_CLR  | CPU1_DDATA_RAM1_ENABLE_CLR  | CPU1_DDATA_RAM0_ENABLE_CLR  | CPU1_DDIRTY_RAM_ENABLE_CLR  | CPU1_DTAG_RAM3_ENABLE_CLR     | CPU1_DTAG_RAM2_ENABLE_CLR  | CPU1_DTAG_RAM1_ENABLE_CLR  | CPU1_DTAG_RAM0_ENABLE_CLR  |
| R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                        | R/W1TC                     | R/W1TC                     | R/W1TC                     |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                            | 0h                         | 0h                         | 0h                         |
| 7                           | 6                           | 5                           | 4                           | 3                             | 2                          | 1                          | 0                          |
| CPU1_IDATA_BANK3_ENABLE_CLR | CPU1_IDATA_BANK2_ENABLE_CLR | CPU1_IDATA_BANK1_ENABLE_CLR | CPU1_IDATA_BANK0_ENABLE_CLR | CPU1_ITAG_RAM3_ENABLE_CLR     | CPU1_ITAG_RAM2_ENABLE_CLR  | CPU1_ITAG_RAM1_ENABLE_CLR  | CPU1_ITAG_RAM0_ENABLE_CLR  |
| R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                        | R/W1TC                     | R/W1TC                     | R/W1TC                     |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                            | 0h                         | 0h                         | 0h                         |

**Table 4-307. ECC\_AGG\_CORE1\_DED\_ENABLE\_CLR\_REG0 Register Field Descriptions**

| Bit   | Field                         | Type   | Reset | Description                                                 |
|-------|-------------------------------|--------|-------|-------------------------------------------------------------|
| 31:28 | RESERVED                      | NONE   | 0h    | Reserved                                                    |
| 27    | CPU1_KS_VIM_RAMECC_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_ks_vim_ramecc_pend |
| 26    | B1TCM1_BANK1_ENABLE_CLR       | R/W1TC | 0h    | Interrupt Enable Clear Register for b1tcm1_bank1_pend       |
| 25    | B1TCM1_BANK0_ENABLE_CLR       | R/W1TC | 0h    | Interrupt Enable Clear Register for b1tcm1_bank0_pend       |
| 24    | B0TCM1_BANK1_ENABLE_CLR       | R/W1TC | 0h    | Interrupt Enable Clear Register for b0tcm1_bank1_pend       |
| 23    | B0TCM1_BANK0_ENABLE_CLR       | R/W1TC | 0h    | Interrupt Enable Clear Register for b0tcm1_bank0_pend       |
| 22    | ATCM1_BANK1_ENABLE_CLR        | R/W1TC | 0h    | Interrupt Enable Clear Register for atcm1_bank1_pend        |

**Table 4-307. ECC\_AGG\_CORE1\_DED\_ENABLE\_CLR\_REG0 Register Field Descriptions (continued)**

| Bit | Field                       | Type   | Reset | Description                                               |
|-----|-----------------------------|--------|-------|-----------------------------------------------------------|
| 21  | ATCM1_BANK0_ENABLE_CLR      | R/W1TC | 0h    | Interrupt Enable Clear Register for atcm1_bank0_pend      |
| 20  | CPU1_DDATA_RAM7_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_ddata_ram7_pend  |
| 19  | CPU1_DDATA_RAM6_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_ddata_ram6_pend  |
| 18  | CPU1_DDATA_RAM5_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_ddata_ram5_pend  |
| 17  | CPU1_DDATA_RAM4_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_ddata_ram4_pend  |
| 16  | CPU1_DDATA_RAM3_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_ddata_ram3_pend  |
| 15  | CPU1_DDATA_RAM2_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_ddata_ram2_pend  |
| 14  | CPU1_DDATA_RAM1_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_ddata_ram1_pend  |
| 13  | CPU1_DDATA_RAM0_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_ddata_ram0_pend  |
| 12  | CPU1_DDIRTY_RAM_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_ddirty_ram_pend  |
| 11  | CPU1_DTAG_RAM3_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_dtag_ram3_pend   |
| 10  | CPU1_DTAG_RAM2_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_dtag_ram2_pend   |
| 9   | CPU1_DTAG_RAM1_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_dtag_ram1_pend   |
| 8   | CPU1_DTAG_RAM0_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_dtag_ram0_pend   |
| 7   | CPU1_IDATA_BANK3_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_idata_bank3_pend |
| 6   | CPU1_IDATA_BANK2_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_idata_bank2_pend |
| 5   | CPU1_IDATA_BANK1_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_idata_bank1_pend |
| 4   | CPU1_IDATA_BANK0_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_idata_bank0_pend |
| 3   | CPU1_ITAG_RAM3_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_itag_ram3_pend   |
| 2   | CPU1_ITAG_RAM2_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_itag_ram2_pend   |
| 1   | CPU1_ITAG_RAM1_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_itag_ram1_pend   |
| 0   | CPU1_ITAG_RAM0_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for cpu1_itag_ram0_pend   |

#### 4.1.2.97 ECC\_AGG\_CORE1\_AGGR\_ENABLE\_SET Register

##### 1 ECC\_AGG\_CORE1\_AGGR\_ENABLE\_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register.

Return to [Summary Table](#)

**Table 4-308. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 3200h       |
| R5SS1         | 5300 7200h       |

**Figure 4-97. ECC\_AGG\_CORE1\_AGGR\_ENABLE\_SET Name Register**

|          |    |    |    |    |    |         |        |
|----------|----|----|----|----|----|---------|--------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25      | 24     |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 23       | 22 | 21 | 20 | 19 | 18 | 17      | 16     |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 15       | 14 | 13 | 12 | 11 | 10 | 9       | 8      |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 7        | 6  | 5  | 4  | 3  | 2  | 1       | 0      |
| RESERVED |    |    |    |    |    | TIMEOUT | PARITY |
| NONE     |    |    |    |    |    | R/W1TS  | R/W1TS |
| 0h       |    |    |    |    |    | 0h      | 0h     |

**Table 4-310. ECC\_AGG\_CORE1\_AGGR\_ENABLE\_SET Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description                                   |
|------|----------|--------|-------|-----------------------------------------------|
| 31:2 | RESERVED | NONE   | 0h    | Reserved                                      |
| 1    | TIMEOUT  | R/W1TS | 0h    | Interrupt enable set for svbus timeout errors |
| 0    | PARITY   | R/W1TS | 0h    | Interrupt enable set for parity errors        |

#### 4.1.2.98 ECC\_AGG\_CORE1\_AGGR\_ENABLE\_CLR Register

##### 1 ECC\_AGG\_CORE1\_AGGR\_ENABLE\_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register.

Return to [Summary Table](#)

**Table 4-311. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 3204h       |
| R5SS1         | 5300 7204h       |

**Figure 4-98. ECC\_AGG\_CORE1\_AGGR\_ENABLE\_CLR Name Register**

|          |    |    |    |    |    |         |        |
|----------|----|----|----|----|----|---------|--------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25      | 24     |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 23       | 22 | 21 | 20 | 19 | 18 | 17      | 16     |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 15       | 14 | 13 | 12 | 11 | 10 | 9       | 8      |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 7        | 6  | 5  | 4  | 3  | 2  | 1       | 0      |
| RESERVED |    |    |    |    |    | TIMEOUT | PARITY |
| NONE     |    |    |    |    |    | R/W1TC  | R/W1TC |
| 0h       |    |    |    |    |    | 0h      | 0h     |

**Table 4-313. ECC\_AGG\_CORE1\_AGGR\_ENABLE\_CLR Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description                                     |
|------|----------|--------|-------|-------------------------------------------------|
| 31:2 | RESERVED | NONE   | 0h    | Reserved                                        |
| 1    | TIMEOUT  | R/W1TC | 0h    | Interrupt enable clear for svbus timeout errors |
| 0    | PARITY   | R/W1TC | 0h    | Interrupt enable clear for parity errors        |

#### 4.1.2.99 ECC\_AGG\_CORE1\_AGGR\_STATUS\_SET Register

##### 1 ECC\_AGG\_CORE1\_AGGR\_STATUS\_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register.

Return to [Summary Table](#)

**Table 4-314. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 3208h       |
| R5SS1         | 5300 7208h       |

**Figure 4-99. ECC\_AGG\_CORE1\_AGGR\_STATUS\_SET Name Register**

|          |    |    |    |         |    |        |    |
|----------|----|----|----|---------|----|--------|----|
| 31       | 30 | 29 | 28 | 27      | 26 | 25     | 24 |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 23       | 22 | 21 | 20 | 19      | 18 | 17     | 16 |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 15       | 14 | 13 | 12 | 11      | 10 | 9      | 8  |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 7        | 6  | 5  | 4  | 3       | 2  | 1      | 0  |
| RESERVED |    |    |    | TIMEOUT |    | PARITY |    |
| NONE     |    |    |    | R/WI    |    | R/WI   |    |
| 0h       |    |    |    | 0h      |    | 0h     |    |

**Table 4-316. ECC\_AGG\_CORE1\_AGGR\_STATUS\_SET Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 3:2  | TIMEOUT  | R/WI | 0h    | 2-bit saturating counter of the number of timeout errors that have occurred since last cleared.<br>2'b00 - No timeout errors have occurred<br>2'b01 - 1 timeout error has occurred<br>2'b10 - 2 timeout error has occurred<br>2'b11 - 3 or more timeout errors have occurred<br>A write of a non-zero value to this register increments that many from the timeout fields. If the value written is less than the current value of the counter, then the pending level interrupt stays asserted. . If this register goes from 0 to non zero a level interrupt will be asserted as well as a pulse interrupt. If the value was non zero to non zero then the level interrupt would remain asserted, but no new pulse interrupt would be asserted. You must write the eoi register to get a new pulse interrupt. |

**Table 4-316. ECC\_AGG\_CORE1\_AGGR\_STATUS\_SET Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-----|--------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0 | PARITY | R/WI | 0h    | <p>2-bit saturating counter of the number of parity errors that have occurred since last cleared.</p> <p>2'b00 - No parity errors have occurred</p> <p>2'b01 - 1 parity error has occurred</p> <p>2'b10 - 2 parity error has occurred</p> <p>2'b11 - 3 or more parity error have occurred</p> <p>A write of a non-zero value to this register increments that many from the parity fields. If the value written is less than the current value of the counter, then the pending level interrupt stays asserted. If this register goes from 0 to non zero a level interrupt will be asserted as well as a pulse interrupt. If the value was non zero to non zero then the level interrupt would remain asserted, but no new pulse interrupt would be asserted. You must write the eoi register to get a new pulse interrupt.</p> |



#### 4.1.2.100 ECC\_AGG\_CORE1\_AGGR\_STATUS\_CLR Register

##### 1 ECC\_AGG\_CORE1\_AGGR\_STATUS\_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register.

Return to [Summary Table](#)

**Table 4-317. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5300 320Ch       |
| R5SS1         | 5300 720Ch       |

**Figure 4-100. ECC\_AGG\_CORE1\_AGGR\_STATUS\_CLR Name Register**

|          |    |    |    |         |    |        |    |
|----------|----|----|----|---------|----|--------|----|
| 31       | 30 | 29 | 28 | 27      | 26 | 25     | 24 |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 23       | 22 | 21 | 20 | 19      | 18 | 17     | 16 |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 15       | 14 | 13 | 12 | 11      | 10 | 9      | 8  |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 7        | 6  | 5  | 4  | 3       | 2  | 1      | 0  |
| RESERVED |    |    |    | TIMEOUT |    | PARITY |    |
| NONE     |    |    |    | R/W     |    | R/W    |    |
| 0h       |    |    |    | 0h      |    | 0h     |    |

**Table 4-319. ECC\_AGG\_CORE1\_AGGR\_STATUS\_CLR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 3:2  | TIMEOUT  | R/W  | 0h    | 2'b00 - No timeout errors have occurred<br>2'b01 - 1 timeout error has occurred<br>2'b10 - 2 timeout error has occurred<br>2'b11 - 3 or more timeout errors have occurred<br>A write of a non-zero value to this register decrements that many from the timeout fields. If the resulting written value is non zero, then the pending level interrupt stays asserted. A new pulse interrupt will not be asserted, you must write the eoi register for that to occur. If you write a value more than the counter value the result will be zero. |
| 1:0  | PARITY   | R/W  | 0h    | 2'b00 - No parity errors have occurred<br>2'b01 - 1 parity error has occurred<br>2'b10 - 2 parity error has occurred<br>2'b11 - 3 or more parity error have occurred<br>A write of a non-zero value to this register decrements that many from the parity fields. If the resulting written value is non zero, then the pending level interrupt stays asserted. A new pulse interrupt will not be asserted, you must write the eoi register for that to occur. If you write a value more than the counter value the result will be zero.       |

#### 4.1.2.101 CCMR\_CCMSR1 Register

##### 1 CCMR\_CCMSR1 Register (Offset = 0h) [reset = 0h]

CPU Compare Status Register.

Return to [Summary Table](#)

**Table 4-320. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5321 0000h       |
| R5SS1         | 5321 1000h       |

**Figure 4-101. CCMR\_CCMSR1 Name Register**

|     |    |    |    |    |    |       |       |
|-----|----|----|----|----|----|-------|-------|
| 31  | 30 | 29 | 28 | 27 | 26 | 25    | 24    |
| NU2 |    |    |    |    |    |       |       |
| NU2 |    |    |    |    |    |       |       |
| 0h  |    |    |    |    |    |       |       |
| 23  | 22 | 21 | 20 | 19 | 18 | 17    | 16    |
| NU2 |    |    |    |    |    |       | CMPE1 |
| NU2 |    |    |    |    |    |       | R/W   |
| 0h  |    |    |    |    |    |       | 0h    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9     | 8     |
| NU1 |    |    |    |    |    |       | STC1  |
| NU1 |    |    |    |    |    |       | R/W   |
| 0h  |    |    |    |    |    |       | 0h    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1     | 0     |
| NU0 |    |    |    |    |    | STET1 | STE1  |
| R/W |    |    |    |    |    | R/W   | R     |
| 0h  |    |    |    |    |    | 0h    | 0h    |

**Table 4-322. CCMR\_CCMSR1 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                          |
|-------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | NU2   | NU2  | 0h    | Reserved                                                                                                                                             |
| 16    | CMPE1 | R/W  | 0h    | Compare Error<br>0 = CPU signals are identical<br>1 = CPU signal compare mismatch<br>Writes '1' to clear this bit                                    |
| 15:9  | NU1   | NU1  | 0h    | Reserved                                                                                                                                             |
| 8     | STC1  | R/W  | 0h    | Self Test Complete<br>0 = self test on-going if self test mode asserted<br>1 = self test is complete<br>Writes have no effect                        |
| 7:2   | NU0   | R/W  | 0h    | Reserved                                                                                                                                             |
| 1     | STET1 | R/W  | 0h    | Self Test Error Type<br>0 = self test failed during Compare Match test<br>1 = self test failed during Compare mismatch test<br>Writes have no effect |
| 0     | STE1  | R    | 0h    | Self Test Error<br>0 = self test passed<br>1 = self test failed<br>Writes have no effect                                                             |

#### 4.1.2.102 CCMR\_CCMKEYR1 Register

##### 1 CCMR\_CCMKEYR1 Register (Offset = 4h) [reset = 0h]

CPU Compare Key Register.

Return to [Summary Table](#)

**Table 4-323. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5321 0004h       |
| R5SS1         | 5321 1004h       |

**Figure 4-102. CCMR\_CCMKEYR1 Name Register**

|     |    |    |    |       |    |    |    |
|-----|----|----|----|-------|----|----|----|
| 31  | 30 | 29 | 28 | 27    | 26 | 25 | 24 |
| NU3 |    |    |    |       |    |    |    |
| R/W |    |    |    |       |    |    |    |
| 0h  |    |    |    |       |    |    |    |
| 23  | 22 | 21 | 20 | 19    | 18 | 17 | 16 |
| NU3 |    |    |    |       |    |    |    |
| R/W |    |    |    |       |    |    |    |
| 0h  |    |    |    |       |    |    |    |
| 15  | 14 | 13 | 12 | 11    | 10 | 9  | 8  |
| NU3 |    |    |    |       |    |    |    |
| R/W |    |    |    |       |    |    |    |
| 0h  |    |    |    |       |    |    |    |
| 7   | 6  | 5  | 4  | 3     | 2  | 1  | 0  |
| NU3 |    |    |    | MKEY1 |    |    |    |
| R/W |    |    |    | R/W   |    |    |    |
| 0h  |    |    |    | 0h    |    |    |    |

**Table 4-325. CCMR\_CCMKEYR1 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                |
|------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------|
| 31:4 | NU3   | R/W  | 0h    | Reserved                                                                                                                   |
| 3:0  | MKEY1 | R/W  | 0h    | Mode Key<br>0000= lock step mode<br>0110= self test mode<br>1001= error forcing mode<br>1111= self test error forcing mode |

#### 4.1.2.103 CCMR\_CCMSR2 Register

##### 1 CCMR\_CCMSR2 Register (Offset = 8h) [reset = 0h]

VIM Compare Status Register.

Return to [Summary Table](#)

**Table 4-326. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5321 0008h       |
| R5SS1         | 5321 1008h       |

**Figure 4-103. CCMR\_CCMSR2 Name Register**

|     |    |    |    |    |    |       |       |
|-----|----|----|----|----|----|-------|-------|
| 31  | 30 | 29 | 28 | 27 | 26 | 25    | 24    |
| NU6 |    |    |    |    |    |       |       |
| R/W |    |    |    |    |    |       |       |
| 0h  |    |    |    |    |    |       |       |
| 23  | 22 | 21 | 20 | 19 | 18 | 17    | 16    |
| NU6 |    |    |    |    |    |       | CMPE2 |
| R/W |    |    |    |    |    |       | R/W   |
| 0h  |    |    |    |    |    |       | 0h    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9     | 8     |
| NU5 |    |    |    |    |    |       | STC2  |
| R/W |    |    |    |    |    |       | R/W   |
| 0h  |    |    |    |    |    |       | 0h    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1     | 0     |
| NU4 |    |    |    |    |    | STET2 | STE2  |
| R/W |    |    |    |    |    | R/W   | R/W   |
| 0h  |    |    |    |    |    | 0h    | 0h    |

**Table 4-328. CCMR\_CCMSR2 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                          |
|-------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | NU6   | R/W  | 0h    | Reserved                                                                                                                                             |
| 16    | CMPE2 | R/W  | 0h    | Compare Error<br>0 = VIM signals are identical<br>1 = VIM signal compare mismatch<br>Writes '1' to clear this bit                                    |
| 15:9  | NU5   | R/W  | 0h    | Reserved                                                                                                                                             |
| 8     | STC2  | R/W  | 0h    | Self Test Complete<br>0 = self test on-going if self test mode asserted<br>1 = self test is complete<br>Writes have no effect                        |
| 7:2   | NU4   | R/W  | 0h    | Reserved                                                                                                                                             |
| 1     | STET2 | R/W  | 0h    | Self Test Error Type<br>0 = self test failed during Compare Match test<br>1 = self test failed during Compare mismatch test<br>Writes have no effect |
| 0     | STE2  | R/W  | 0h    | Self Test Error<br>0 = self test passed<br>1 = self test failed<br>Writes have no effect                                                             |

#### 4.1.2.104 CCMR\_CCMKEYR2 Register

##### 1 CCMR\_CCMKEYR2 Register (Offset = Ch) [reset = 0h]

VIM Compare Key Register.

Return to [Summary Table](#)

**Table 4-329. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5321 000Ch       |
| R5SS1         | 5321 100Ch       |

**Figure 4-104. CCMR\_CCMKEYR2 Name Register**

|     |    |    |    |       |    |    |    |
|-----|----|----|----|-------|----|----|----|
| 31  | 30 | 29 | 28 | 27    | 26 | 25 | 24 |
| NU7 |    |    |    |       |    |    |    |
| R/W |    |    |    |       |    |    |    |
| 0h  |    |    |    |       |    |    |    |
| 23  | 22 | 21 | 20 | 19    | 18 | 17 | 16 |
| NU7 |    |    |    |       |    |    |    |
| R/W |    |    |    |       |    |    |    |
| 0h  |    |    |    |       |    |    |    |
| 15  | 14 | 13 | 12 | 11    | 10 | 9  | 8  |
| NU7 |    |    |    |       |    |    |    |
| R/W |    |    |    |       |    |    |    |
| 0h  |    |    |    |       |    |    |    |
| 7   | 6  | 5  | 4  | 3     | 2  | 1  | 0  |
| NU7 |    |    |    | MKEY2 |    |    |    |
| R/W |    |    |    | R/W   |    |    |    |
| 0h  |    |    |    | 0h    |    |    |    |

**Table 4-331. CCMR\_CCMKEYR2 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                |
|------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------|
| 31:4 | NU7   | R/W  | 0h    | Reserved                                                                                                                   |
| 3:0  | MKEY2 | R/W  | 0h    | Mode Key<br>0000= lock step mode<br>0110= self test mode<br>1001= error forcing mode<br>1111= self test error forcing mode |

#### 4.1.2.105 CCMR\_CCMSR3 Register

##### 1 CCMR\_CCMSR3 Register (Offset = 10h) [reset = 0h]

Inactivity Monitor Status Register.

Return to [Summary Table](#)

**Table 4-332. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5321 0010h       |
| R5SS1         | 5321 1010h       |

**Figure 4-105. CCMR\_CCMSR3 Name Register**

|      |    |    |    |    |    |       |       |
|------|----|----|----|----|----|-------|-------|
| 31   | 30 | 29 | 28 | 27 | 26 | 25    | 24    |
| NU10 |    |    |    |    |    |       |       |
| R/W  |    |    |    |    |    |       |       |
| 0h   |    |    |    |    |    |       |       |
| 23   | 22 | 21 | 20 | 19 | 18 | 17    | 16    |
| NU10 |    |    |    |    |    |       | CMPE3 |
| R/W  |    |    |    |    |    |       | R/W   |
| 0h   |    |    |    |    |    |       | 0h    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9     | 8     |
| NU9  |    |    |    |    |    |       | STC3  |
| R/W  |    |    |    |    |    |       | R/W   |
| 0h   |    |    |    |    |    |       | 0h    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1     | 0     |
| NU8  |    |    |    |    |    | STET3 | STE3  |
| R/W  |    |    |    |    |    | R/W   | R     |
| 0h   |    |    |    |    |    | 0h    | 0h    |

**Table 4-334. CCMR\_CCMSR3 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                          |
|-------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | NU10  | R/W  | 0h    | Reserved                                                                                                                                             |
| 16    | CMPE3 | R/W  | 0h    | Compare Error<br>0 = Inactivity monitor signals are identical<br>1 = Inactivity monitor signal compare mismatch<br>Writes '1' to clear this bit      |
| 15:9  | NU9   | R/W  | 0h    | Reserved                                                                                                                                             |
| 8     | STC3  | R/W  | 0h    | Self Test Complete<br>0 = self test on-going if self test mode asserted<br>1 = self test is complete<br>Writes have no effect                        |
| 7:2   | NU8   | R/W  | 0h    | Reserved                                                                                                                                             |
| 1     | STET3 | R/W  | 0h    | Self Test Error Type<br>0 = self test failed during Compare Match test<br>1 = self test failed during Compare mismatch test<br>Writes have no effect |
| 0     | STE3  | R    | 0h    | Self Test Error<br>0 = self test passed<br>1 = self test failed<br>Writes have no effect                                                             |

#### 4.1.2.106 CCMR\_CCMKEYR3 Register

##### 1 CCMR\_CCMKEYR3 Register (Offset = 14h) [reset = 0h]

Inactivity Monitor Key Register.

Return to [Summary Table](#)

**Table 4-335. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5321 0014h       |
| R5SS1         | 5321 1014h       |

**Figure 4-106. CCMR\_CCMKEYR3 Name Register**

|      |    |    |    |       |    |    |    |
|------|----|----|----|-------|----|----|----|
| 31   | 30 | 29 | 28 | 27    | 26 | 25 | 24 |
| NU11 |    |    |    |       |    |    |    |
| R/W  |    |    |    |       |    |    |    |
| 0h   |    |    |    |       |    |    |    |
| 23   | 22 | 21 | 20 | 19    | 18 | 17 | 16 |
| NU11 |    |    |    |       |    |    |    |
| R/W  |    |    |    |       |    |    |    |
| 0h   |    |    |    |       |    |    |    |
| 15   | 14 | 13 | 12 | 11    | 10 | 9  | 8  |
| NU11 |    |    |    |       |    |    |    |
| R/W  |    |    |    |       |    |    |    |
| 0h   |    |    |    |       |    |    |    |
| 7    | 6  | 5  | 4  | 3     | 2  | 1  | 0  |
| NU11 |    |    |    | MKEY3 |    |    |    |
| R/W  |    |    |    | R/W   |    |    |    |
| 0h   |    |    |    | 0h    |    |    |    |

**Table 4-337. CCMR\_CCMKEYR3 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                |
|------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------|
| 31:4 | NU11  | R/W  | 0h    | Reserved                                                                                                                   |
| 3:0  | MKEY3 | R/W  | 0h    | Mode Key<br>0000= lock step mode<br>0110= self test mode<br>1001= error forcing mode<br>1111= self test error forcing mode |

#### 4.1.2.107 CCMR\_CCMPOLCNTRL Register

##### 1 CCMR\_CCMPOLCNTRL Register (Offset = 18h) [reset = 0h]

CPU Compare Polarity Control Register.

Return to [Summary Table](#)

**Table 4-338. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5321 0018h       |
| R5SS1         | 5321 1018h       |

**Figure 4-107. CCMR\_CCMPOLCNTRL Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| NU12    |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| NU12    |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| NU12    |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| POL_INV |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-340. CCMR\_CCMPOLCNTRL Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                |
|------|---------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | NU12    | R/W  | 0h    | Reserved                                                                                                                                                                                                                                   |
| 7:0  | POL_INV | R    | 0h    | This value is used to invert the 8 XOR of the CPU1 to create compare fail in functional active compare mode.<br>User and privilege mode read = Returns current value of the POL INV<br>Privilege mode write = Update the values of POL INV |



#### 4.1.2.108 STC\_STCGCR0 Register

##### 1 STC\_STCGCR0 Register (Offset = 0h) [reset = 10120h]

Self test Global control Reg0. \*NOT BYTE ACCESSIBLE.

Return to [Summary Table](#)

**Table 4-341. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0000h       |
| R5SS1         | 5351 0000h       |

**Figure 4-108. STC\_STCGCR0 Name Register**

|                            |    |    |     |                |           |    |    |
|----------------------------|----|----|-----|----------------|-----------|----|----|
| 31                         | 30 | 29 | 28  | 27             | 26        | 25 | 24 |
| INTCOUNT_B16               |    |    |     |                |           |    |    |
| R/W                        |    |    |     |                |           |    |    |
| 1h                         |    |    |     |                |           |    |    |
| 23                         | 22 | 21 | 20  | 19             | 18        | 17 | 16 |
| INTCOUNT_B16               |    |    |     |                |           |    |    |
| R/W                        |    |    |     |                |           |    |    |
| 1h                         |    |    |     |                |           |    |    |
| 15                         | 14 | 13 | 12  | 11             | 10        | 9  | 8  |
| NU0                        |    |    |     | CAP_IDLE_CYCLE |           |    |    |
| R                          |    |    |     | R/W            |           |    |    |
| 0h                         |    |    |     | 1h             |           |    |    |
| 7                          | 6  | 5  | 4   | 3              | 2         | 1  | 0  |
| SCANEN_HIGH_CAP_IDLE_CYCLE |    |    | NU1 |                | RS_CNT_B1 |    |    |
| R/W                        |    |    | NU1 |                | R/W       |    |    |
| 1h                         |    |    | 0h  |                | 0h        |    |    |

**Table 4-343. STC\_STCGCR0 Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                    |
|-------|----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | INTCOUNT_B16   | R/W  | 1h    | Number of intervals of the self test run [RWP - Read, Priviledge Mode Write only]<br>Count of intervals that need to be covered for a specific selftest run. The selftest controller sends out complete indication once it runs all of the intervals programmed in this field.<br>INTCOUNT_B16=0 is an invalid configuration for a selftest.                   |
| 15:11 | NU0            | R    | 0h    | Reserved bits                                                                                                                                                                                                                                                                                                                                                  |
| 10:8  | CAP_IDLE_CYCLE | R/W  | 1h    | Idle cycles before and after capture clock [RWP - Read, Priviledge Mode Write only]<br>Idle Cycles before and after capture clock.<br>This value is used to insert that many idle cycles in the Capture phase. Programmable idle cycles allow implementation flexibility on SCAN_EN signal at chip level based on the size of the UUT and timing requirements. |

**Table 4-343. STC\_STCGCR0 Register Field Descriptions (continued)**

| Bit | Field                          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|--------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5 | SCANEN_HIGH_CAP_ID<br>LE_CYCLE | R/W  | 1h    | Idle cycles before and after capture clock [RWP - Read, Priviledge Mode Write only]. *NOT BYTE ACCESSIBLE<br>Idle Cycles between scan_en going high to func_clk_en generation and scan_en going high to misr_log_en generation.<br>This value is used to insert that many idle cycles in the shift clock [scan_en going high to func_clk_en generation] and misr_log_clk [scan_en going high to misr_log_en generation] generation. Programmable idle cycles allow implementation flexibility on SCAN_EN signal at chip level based on the size of the UUT and timing requirements. |
| 4:2 | NU1                            | NU1  | 0h    | Reserved bits                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 1:0 | RS_CNT_B1                      | R/W  | 0h    | Restart/Continue or preload [RWP - Read, Priviledge Mode Write only]<br>This bit specifies the selftest controller whether to continue the run from next interval onwards, restart from ROM address 0 or preload from a prescribed interval. This bit gets reset after the completion of selftest run.<br>00 = Continue NSTC run from previous interval<br>01 = Restart NSTC run from ROM address 0<br>1X = Start from segment number specified in STC_SEGPLR register                                                                                                              |

#### 4.1.2.109 STC\_STCGCR1 Register

##### 1 STC\_STCGCR1 Register (Offset = 4h) [reset = 25h]

Self test Global control Reg1.

Return to [Summary Table](#)

**Table 4-344. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0004h       |
| R5SS1         | 5351 0004h       |

**Figure 4-109. STC\_STCGCR1 Name Register**

|     |                   |              |                |    |    |               |           |
|-----|-------------------|--------------|----------------|----|----|---------------|-----------|
| 31  | 30                | 29           | 28             | 27 | 26 | 25            | 24        |
|     |                   |              | NU2            |    |    |               |           |
|     |                   |              | NU2            |    |    |               |           |
|     |                   |              | 0h             |    |    |               |           |
| 23  | 22                | 21           | 20             | 19 | 18 | 17            | 16        |
|     |                   |              | NU2            |    |    |               |           |
|     |                   |              | NU2            |    |    |               |           |
|     |                   |              | 0h             |    |    |               |           |
| 15  | 14                | 13           | 12             | 11 | 10 | 9             | 8         |
|     |                   | NU2          |                |    |    | SEG0_CORE_SEL |           |
|     |                   | NU2          |                |    |    | R/W           |           |
|     |                   | 0h           |                |    |    | 0h            |           |
| 7   | 6                 | 5            | 4              | 3  | 2  | 1             | 0         |
| NU3 | CODEC_SPREAD_MODE | LP_SCAN_MODE | ROM_ACCESS_INV |    |    |               | ST_ENA_B4 |
| R   | R/W               | R/W          | R/W            |    |    |               | R/W       |
| 0h  | 0h                | 1h           | 0h             |    |    |               | 5h        |

**Table 4-346. STC\_STCGCR1 Register Field Descriptions**

| Bit   | Field             | Type | Reset | Description                                                                                                                                                                                 |
|-------|-------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | NU2               | NU2  | 0h    | Reserved bits                                                                                                                                                                               |
| 11:8  | SEG0_CORE_SEL     | R/W  | 0h    | Selects the Segment0 CORE for self test [RWP - Read, Priviledge Mode Write only]<br>Select the Segment0 CORE for Self -Test<br>0001= Select CORE for selftest<br>Other = CORE not selected. |
| 7     | NU3               | R    | 0h    | Reserved bits                                                                                                                                                                               |
| 6     | CODEC_SPREAD_MODE | R/W  | 0h    | Codec Spread Mode control signal [RWP - Read, Priviledge Mode Write only]<br>This bit is used to configure the codec in spread / X-OR mode.<br>1 = Spread mode<br>0 = XOR mode              |
| 5     | LP_SCAN_MODE      | R/W  | 1h    | LP scan mode [RWP - Read, Priviledge Mode Write only]<br>This bit is used to decide the scan configuration:<br>1 = Operates in Low Power Scan Mode.<br>0 = Operates in Normal Scan Mode.    |
| 4     | ROM_ACCESS_INV    | R/W  | 0h    | Rom access inversion mode [RWP - Read, Priviledge Mode Write only]<br>- NOT SUPPORTED                                                                                                       |

**Table 4-346. STC\_STCGCR1 Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description                                                                                                                                           |
|-----|-----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0 | ST_ENA_B4 | R/W  | 5h    | Self test enable key [RWP - Read, Priviledge Mode Write only]<br>1010= Self test run enabled<br>All values other than<br>1010= Self test run disabled |

#### 4.1.2.110 STC\_STCTPR Register

##### 1 STC\_STCTPR Register (Offset = 8h) [reset = FFFFFFFFh]

Time out counter preload register.

Return to [Summary Table](#)

**Table 4-347. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0008h       |
| R5SS1         | 5351 0008h       |

**Figure 4-110. STC\_STCTPR Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TO_PRELOAD |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| FFFFFFFh   |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TO_PRELOAD |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| FFFFFFFh   |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TO_PRELOAD |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| FFFFFFFh   |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TO_PRELOAD |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| FFFFFFFh   |    |    |    |    |    |    |    |

**Table 4-349. STC\_STCTPR Register Field Descriptions**

| Bit  | Field      | Type | Reset    | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|------|------------|------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | TO_PRELOAD | R/W  | FFFFFFFh | Self test time out preload [RWP - Read, Priviledge Mode Write only]<br>This register contains the total number of STC clock cycles it will take before a self-test timeout error will be triggered after the initiation of the self-test run. This is a fail safe feature to avoid system hang-up situation on account of any run away self test issues. This register should be loaded with a meaningful count value for this feature to be effective.<br>This register value [preload count value] gets loaded into the self test timeout down counter whenever a self test run is initiated [ST_ENA is enabled]. and gets disabled on completion of a self test run. |

#### 4.1.2.111 STC\_STC\_CADDR Register

##### 1 STC\_STC\_CADDR Register (Offset = Ch) [reset = 0h]

Current Address register for CORE1.

Return to [Summary Table](#)

**Table 4-350. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 000Ch       |
| R5SS1         | 5351 000Ch       |

**Figure 4-111. STC\_STC\_CADDR Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ADDR |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ADDR |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ADDR |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ADDR |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 4-352. STC\_STC\_CADDR Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                       |
|------|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ADDR  | R    | 0h    | Current ROM Address for CORE1<br>This register reflects the current ROM address [for micro code load] accessed during selftest for CORE1 in case of segment0 and all the remaining n segments, where n = 1 to 3]. |

#### 4.1.2.112 STC\_STCCICR Register

##### 1 STC\_STCCICR Register (Offset = 10h) [reset = 0h]

Current Interval count register.

Return to [Summary Table](#)

**Table 4-353. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0010h       |
| R5SS1         | 5351 0010h       |

**Figure 4-112. STC\_STCCICR Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CORE2_ICOUNT |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CORE2_ICOUNT |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CORE1_ICOUNT |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CORE1_ICOUNT |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 4-355. STC\_STCCICR Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                                                                                                                                    |
|-------|--------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | CORE2_ICOUNT | R    | 0h    | Specifies the last interval number for CORE2<br>This specifies the Last executed Interval number for CORE2 of Segment0 if self test is being executed for secondary core as well. This field is applicable only for Segment 0. |
| 15:0  | CORE1_ICOUNT | R    | 0h    | Specifies the last interval number for CORE1<br>This specifies the Last executed Interval number of a self-test run.                                                                                                           |

#### 4.1.2.113 STC\_STCGSTAT Register

##### 1 STC\_STCGSTAT Register (Offset = 14h) [reset = 500h]

Global Status Register.

Return to [Summary Table](#)

**Table 4-356. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0014h       |
| R5SS1         | 5351 0014h       |

**Figure 4-113. STC\_STCGSTAT Name Register**

|     |    |    |    |           |    |           |           |
|-----|----|----|----|-----------|----|-----------|-----------|
| 31  | 30 | 29 | 28 | 27        | 26 | 25        | 24        |
| NU4 |    |    |    |           |    |           |           |
| R   |    |    |    |           |    |           |           |
| 0h  |    |    |    |           |    |           |           |
| 23  | 22 | 21 | 20 | 19        | 18 | 17        | 16        |
| NU4 |    |    |    |           |    |           |           |
| R   |    |    |    |           |    |           |           |
| 0h  |    |    |    |           |    |           |           |
| 15  | 14 | 13 | 12 | 11        | 10 | 9         | 8         |
| NU4 |    |    |    | ST_ACTIVE |    |           |           |
| R   |    |    |    | R         |    |           |           |
| 0h  |    |    |    | 5h        |    |           |           |
| 7   | 6  | 5  | 4  | 3         | 2  | 1         | 0         |
| NU5 |    |    |    |           |    | TEST_FAIL | TEST_DONE |
| R   |    |    |    |           |    | R         | R         |
| 0h  |    |    |    |           |    | 0h        | 0h        |

**Table 4-358. STC\_STCGSTAT Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                        |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | NU4       | R    | 0h    | Reserved bits                                                                                                                                                                                                                      |
| 11:8  | ST_ACTIVE | R    | 5h    | Indicates whether self test is currently active or not.<br>1010 = Self test is active<br>Others = SelfTest is not active<br>Once the self-test completes and ST_ENA_B4 key is cleared, this field will reflect the inactive value. |
| 7:2   | NU5       | R    | 0h    | Reserved bits                                                                                                                                                                                                                      |
| 1     | TEST_FAIL | R    | 0h    | Test_fail flag [RCP - Read, Clear on Writing in Priviledge Mode]<br>0 = Self test run has not failed<br>1 = SelfTest run has failed. Write Clear.                                                                                  |
| 0     | TEST_DONE | R    | 0h    | Test_done_flag [RCP - Read, Clear on Writing in Priviledge Mode]<br>0 = Not completed<br>1 = SelfTest run Completed                                                                                                                |



#### 4.1.2.114 STC\_STCFSTAT Register

##### 1 STC\_STCFSTAT Register (Offset = 18h) [reset = 0h]

Fail Status Register.

Return to [Summary Table](#)

**Table 4-359. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0018h       |
| R5SS1         | 5351 0018h       |

**Figure 4-114. STC\_STCFSTAT Name Register**

|     |    |    |         |    |          |              |              |
|-----|----|----|---------|----|----------|--------------|--------------|
| 31  | 30 | 29 | 28      | 27 | 26       | 25           | 24           |
| NU6 |    |    |         |    |          |              |              |
| R   |    |    |         |    |          |              |              |
| 0h  |    |    |         |    |          |              |              |
| 23  | 22 | 21 | 20      | 19 | 18       | 17           | 16           |
| NU6 |    |    |         |    |          |              |              |
| R   |    |    |         |    |          |              |              |
| 0h  |    |    |         |    |          |              |              |
| 15  | 14 | 13 | 12      | 11 | 10       | 9            | 8            |
| NU6 |    |    |         |    |          |              |              |
| R   |    |    |         |    |          |              |              |
| 0h  |    |    |         |    |          |              |              |
| 7   | 6  | 5  | 4       | 3  | 2        | 1            | 0            |
| NU6 |    |    | FSEG_ID |    | TO_ER_B1 | CPU2_FAIL_B1 | CPU1_FAIL_B1 |
| R   |    |    | R       |    | R        | R            | R            |
| 0h  |    |    | 0h      |    | 0h       | 0h           | 0h           |

**Table 4-361. STC\_STCFSTAT Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                        |
|------|--------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:5 | NU6          | R    | 0h    | Reserved bits                                                                                                                                                                                                                                                                                                      |
| 4:3  | FSEG_ID      | R    | 0h    | Failed Segment ID [RCP - Read, Clear on Writing in Privilege Mode]<br>This field captures the Segment number for which any of the failures like TO_ER_B1, CPU1_FAIL_B1 and CPU2_FAIL_B1 occur.<br>00 = Failure on Segment 0<br>01 = Failure on Segment 1<br>10 = Failure on Segment 2<br>11 = Failure on Segment 3 |
| 2    | TO_ER_B1     | R    | 0h    | Indicates whether self test failed because of time out error [RCP - Read, Clear on Writing in Privilege Mode]<br>0 = No time out error occurred<br>1 = SelfTest run failed due to a timeout error                                                                                                                  |
| 1    | CPU2_FAIL_B1 | R    | 0h    | Indicates whether MISR mismatch happened in CORE2 when in Segment0 mode [RCP - Read, Clear on Writing in Privilege Mode]<br>0 = No MISR mismatch for CORE2<br>1 = Self test run failed due to MISR mismatch for CORE2                                                                                              |
| 0    | CPU1_FAIL_B1 | R    | 0h    | Indicates whether MISR mismatch happened in CORE1 [RCP - Read, Clear on Writing in Privilege Mode]<br>Applicable to all segments.<br>0 = No MISR mismatch for CORE1<br>1 = Self test run failed due to MISR mismatch for CORE1                                                                                     |

#### 4.1.2.115 STC\_STCSCSCR Register

##### 1 STC\_STCSCSCR Register (Offset = 1Ch) [reset = 5h]

Signature compare Self Check Register.

Return to [Summary Table](#)

**Table 4-362. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 001Ch       |
| R5SS1         | 5351 001Ch       |

**Figure 4-115. STC\_STCSCSCR Name Register**

|     |    |    |              |                   |    |    |    |
|-----|----|----|--------------|-------------------|----|----|----|
| 31  | 30 | 29 | 28           | 27                | 26 | 25 | 24 |
| NU7 |    |    |              |                   |    |    |    |
| R   |    |    |              |                   |    |    |    |
| 0h  |    |    |              |                   |    |    |    |
| 23  | 22 | 21 | 20           | 19                | 18 | 17 | 16 |
| NU7 |    |    |              |                   |    |    |    |
| R   |    |    |              |                   |    |    |    |
| 0h  |    |    |              |                   |    |    |    |
| 15  | 14 | 13 | 12           | 11                | 10 | 9  | 8  |
| NU7 |    |    |              |                   |    |    |    |
| R   |    |    |              |                   |    |    |    |
| 0h  |    |    |              |                   |    |    |    |
| 7   | 6  | 5  | 4            | 3                 | 2  | 1  | 0  |
| NU7 |    |    | FAULT_INS_B1 | SELF_CHECK_KEY_B4 |    |    |    |
| R   |    |    | R/W          | R/W               |    |    |    |
| 0h  |    |    | 0h           | 5h                |    |    |    |

**Table 4-364. STC\_STCSCSCR Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                                                                                                                                                                                                                              |
|------|-------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:5 | NU7               | R    | 0h    | Reserved bits                                                                                                                                                                                                                            |
| 4    | FAULT_INS_B1      | R/W  | 0h    | Fault Insertion bit [RWP - Read, Priviledge Mode Write only]<br>0 = No fault insertion.<br>1 = Inserts fault in the logic unedr test which will make signature compare fail. This feature is used as diagnostic check of the STC IP.     |
| 3:0  | SELF_CHECK_KEY_B4 | R/W  | 5h    | Signature compare logic self check key enable/disable [RWP - Read, Priviledge Mode Write only]<br>1010 = Signature compare logic Self Check is enabled<br>All values other than<br>1010 = Signature compare logic Self Check is disabled |

#### 4.1.2.116 STC\_STC\_CADDR2 Register

##### 1 STC\_STC\_CADDR2 Register (Offset = 20h) [reset = 0h]

Current Address register for CORE2.

Return to [Summary Table](#)

**Table 4-365. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0020h       |
| R5SS1         | 5351 0020h       |

**Figure 4-116. STC\_STC\_CADDR2 Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ADDR |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ADDR |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ADDR |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ADDR |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 4-367. STC\_STC\_CADDR2 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                  |
|------|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ADDR  | R    | 0h    | Current ROM Address for CORE2<br>This register reflects the current ROM address[for micro code load] accessed during selftest for CORE2 in of case segment0. |

#### 4.1.2.117 STC\_STC\_CLKDIV Register

##### 1 STC\_STC\_CLKDIV Register (Offset = 24h) [reset = 0h]

Clock Divider Register.

Return to [Summary Table](#)

**Table 4-368. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0024h       |
| R5SS1         | 5351 0024h       |

**Figure 4-117. STC\_STC\_CLKDIV Name Register**

|    |    |      |    |    |    |         |    |
|----|----|------|----|----|----|---------|----|
| 31 | 30 | 29   | 28 | 27 | 26 | 25      | 24 |
|    |    | NU8  |    |    |    | CLKDIV0 |    |
|    |    | R    |    |    |    | R/W     |    |
|    |    | 0h   |    |    |    | 0h      |    |
| 23 | 22 | 21   | 20 | 19 | 18 | 17      | 16 |
|    |    | NU9  |    |    |    | CLKDIV1 |    |
|    |    | R    |    |    |    | R/W     |    |
|    |    | 0h   |    |    |    | 0h      |    |
| 15 | 14 | 13   | 12 | 11 | 10 | 9       | 8  |
|    |    | NU10 |    |    |    | CLKDIV2 |    |
|    |    | R    |    |    |    | R/W     |    |
|    |    | 0h   |    |    |    | 0h      |    |
| 7  | 6  | 5    | 4  | 3  | 2  | 1       | 0  |
|    |    | NU11 |    |    |    | CLKDIV3 |    |
|    |    | R    |    |    |    | R/W     |    |
|    |    | 0h   |    |    |    | 0h      |    |

**Table 4-370. STC\_STC\_CLKDIV Register Field Descriptions**

| Bit   | Field   | Type | Reset | Description                                                                                                                   |
|-------|---------|------|-------|-------------------------------------------------------------------------------------------------------------------------------|
| 31:27 | NU8     | R    | 0h    | Reserved bits                                                                                                                 |
| 26:24 | CLKDIV0 | R/W  | 0h    | Clock division for Seg0 [RWP - Read, Priviledge Mode Write only]<br>*NOT SUPPORTED<br>X = Division ratio is X+1 for Segment 0 |
| 23:19 | NU9     | R    | 0h    | Reserved bits                                                                                                                 |
| 18:16 | CLKDIV1 | R/W  | 0h    | Clock division for Seg1 [RWP - Read, Priviledge Mode Write only]<br>*NOT SUPPORTED<br>X = Division ratio is X+1 for Segment 1 |
| 15:11 | NU10    | R    | 0h    | Reserved bits                                                                                                                 |
| 10:8  | CLKDIV2 | R/W  | 0h    | Clock division for Seg2 [RWP - Read, Priviledge Mode Write only]<br>*NOT SUPPORTED<br>X = Division ratio is X+1 for Segment 2 |
| 7:3   | NU11    | R    | 0h    | Reserved bits                                                                                                                 |
| 2:0   | CLKDIV3 | R/W  | 0h    | Clock division for Seg3 [RWP - Read, Priviledge Mode Write only]<br>*NOT SUPPORTED<br>X = Division ratio is X+1 for Segment 3 |

#### 4.1.2.118 STC\_STC\_SEGPLR Register

##### 1 STC\_STC\_SEGPLR Register (Offset = 28h) [reset = 0h]

Segment 1st interval Preload Register.

Return to [Summary Table](#)

**Table 4-371. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0028h       |
| R5SS1         | 5351 0028h       |

**Figure 4-118. STC\_STC\_SEGPLR Name Register**

|      |    |    |    |    |    |             |    |
|------|----|----|----|----|----|-------------|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25          | 24 |
| NU12 |    |    |    |    |    |             |    |
| R    |    |    |    |    |    |             |    |
| 0h   |    |    |    |    |    |             |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17          | 16 |
| NU12 |    |    |    |    |    |             |    |
| R    |    |    |    |    |    |             |    |
| 0h   |    |    |    |    |    |             |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9           | 8  |
| NU12 |    |    |    |    |    |             |    |
| R    |    |    |    |    |    |             |    |
| 0h   |    |    |    |    |    |             |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1           | 0  |
| NU12 |    |    |    |    |    | SEGID_PLOAD |    |
| R    |    |    |    |    |    | R/W         |    |
| 0h   |    |    |    |    |    | 0h          |    |

**Table 4-373. STC\_STC\_SEGPLR Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|-------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | NU12        | R    | 0h    | Reserved bits                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 1:0  | SEGID_PLOAD | R/W  | 0h    | Segment number for which preload is to be started [RWP - Read, Privilege Mode Write only]<br>This specifies the segment for which the address of its First interval will be pre-loaded into the NSTC ROM address counter. The 1st address of each segment are defined in SEGx_START_ADDR register. The address of the 1st interval of the selected segment is loaded into the NSTC ROM address counter when the RS_CNT_B1 bits of STC_GCR0 are set to 1X<br>00 = Preload the address of the 1st interval of segment 0.<br>01 = Preload the address of the 1st interval of segment 1.<br>10 = Preload the address of the 1st interval of segment 2.<br>11 = Preload the address of the 1st interval of segment 3. |

#### 4.1.2.119 STC\_SEG0\_START\_ADDR Register

##### 1 STC\_SEG0\_START\_ADDR Register (Offset = 2Ch) [reset = 0h]

ROM Start address for Segment0.

Return to [Summary Table](#)

**Table 4-374. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 002Ch       |
| R5SS1         | 5351 002Ch       |

**Figure 4-119. STC\_SEG0\_START\_ADDR Name Register**

|                |    |    |    |                |    |    |    |
|----------------|----|----|----|----------------|----|----|----|
| 31             | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| NU13           |    |    |    |                |    |    |    |
| R              |    |    |    |                |    |    |    |
| 0h             |    |    |    |                |    |    |    |
| 23             | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| NU13           |    |    |    | SEG_START_ADDR |    |    |    |
| R              |    |    |    | R/W            |    |    |    |
| 0h             |    |    |    | 0h             |    |    |    |
| 15             | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| SEG_START_ADDR |    |    |    |                |    |    |    |
| R/W            |    |    |    |                |    |    |    |
| 0h             |    |    |    |                |    |    |    |
| 7              | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| SEG_START_ADDR |    |    |    |                |    |    |    |
| R/W            |    |    |    |                |    |    |    |
| 0h             |    |    |    |                |    |    |    |

**Table 4-376. STC\_SEG0\_START\_ADDR Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                               |
|-------|----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | NU13           | R    | 0h    | Reserved bits                                                                                                                                                                                                                                                                                                                                                                             |
| 19:0  | SEG_START_ADDR | R/W  | 0h    | Segment 0 Start Address [RWP - Read, Priviledge Mode Write only]<br>This register holds the ROM address for the start of first interval of the segment.<br>When STC_GCR0.RS_CNT_B1 field is set to [1x] PRELOAD option, this register is used to determine the ROM start address for the Segment selected in ST_SEGPLR register.<br>Valid number of bits depends on RTL parameterter ADDR |

#### 4.1.2.120 STC\_SEG1\_START\_ADDR Register

##### 1 STC\_SEG1\_START\_ADDR Register (Offset = 30h) [reset = 0h]

ROM Start address for Segment1.

Return to [Summary Table](#)

**Table 4-377. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0030h       |
| R5SS1         | 5351 0030h       |

**Figure 4-120. STC\_SEG1\_START\_ADDR Name Register**

|                |    |    |    |                |    |    |    |
|----------------|----|----|----|----------------|----|----|----|
| 31             | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| NU14           |    |    |    |                |    |    |    |
| R              |    |    |    |                |    |    |    |
| 0h             |    |    |    |                |    |    |    |
| 23             | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| NU14           |    |    |    | SEG_START_ADDR |    |    |    |
| R              |    |    |    | R/W            |    |    |    |
| 0h             |    |    |    | 0h             |    |    |    |
| 15             | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| SEG_START_ADDR |    |    |    |                |    |    |    |
| R/W            |    |    |    |                |    |    |    |
| 0h             |    |    |    |                |    |    |    |
| 7              | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| SEG_START_ADDR |    |    |    |                |    |    |    |
| R/W            |    |    |    |                |    |    |    |
| 0h             |    |    |    |                |    |    |    |

**Table 4-379. STC\_SEG1\_START\_ADDR Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | NU14           | R    | 0h    | Reserved bits                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 19:0  | SEG_START_ADDR | R/W  | 0h    | Segment 1 Start Address [RWP - Read, Priviledge Mode Write only]<br>This register holds the ROM address for the start of first interval of the segment.<br>When STC_GCR0.RS_CNT_B1 field is set to [1x] PRELOAD option, this register is used to determine the ROM start address for the Segment selected in ST_SEGPLR register.<br>Valid number of bits depends on RTL parameter ADDR.<br>This register is present only when RTL parameter NUM_SEG = 1. |

#### 4.1.2.121 STC\_SEG2\_START\_ADDR Register

##### 1 STC\_SEG2\_START\_ADDR Register (Offset = 34h) [reset = 0h]

ROM Start address for Segment2.

Return to [Summary Table](#)

**Table 4-380. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0034h       |
| R5SS1         | 5351 0034h       |

**Figure 4-121. STC\_SEG2\_START\_ADDR Name Register**

|                |    |    |    |                |    |    |    |
|----------------|----|----|----|----------------|----|----|----|
| 31             | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| NU15           |    |    |    |                |    |    |    |
| R              |    |    |    |                |    |    |    |
| 0h             |    |    |    |                |    |    |    |
| 23             | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| NU15           |    |    |    | SEG_START_ADDR |    |    |    |
| R              |    |    |    | R/W            |    |    |    |
| 0h             |    |    |    | 0h             |    |    |    |
| 15             | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| SEG_START_ADDR |    |    |    |                |    |    |    |
| R/W            |    |    |    |                |    |    |    |
| 0h             |    |    |    |                |    |    |    |
| 7              | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| SEG_START_ADDR |    |    |    |                |    |    |    |
| R/W            |    |    |    |                |    |    |    |
| 0h             |    |    |    |                |    |    |    |

**Table 4-382. STC\_SEG2\_START\_ADDR Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | NU15           | R    | 0h    | Reserved bits                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 19:0  | SEG_START_ADDR | R/W  | 0h    | Segment 2 Start Address [RWP - Read, Priviledge Mode Write only]<br>This register holds the ROM address for the start of first interval of the segment.<br>When STC_GCR0.RS_CNT_B1 field is set to [1x] PRELOAD option, this register is used to determine the ROM start address for the Segment selected in ST_SEGPLR register.<br>Valid number of bits depends on RTL parameter ADDR.<br>This register is present only when RTL parameter NUM_SEG = 2. |



#### 4.1.2.122 STC\_SEG3\_START\_ADDR Register

##### 1 STC\_SEG3\_START\_ADDR Register (Offset = 38h) [reset = 0h]

ROM Start address for Segment3.

Return to [Summary Table](#)

**Table 4-383. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0038h       |
| R5SS1         | 5351 0038h       |

**Figure 4-122. STC\_SEG3\_START\_ADDR Name Register**

|                |    |    |    |                |    |    |    |
|----------------|----|----|----|----------------|----|----|----|
| 31             | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| NU16           |    |    |    |                |    |    |    |
| R              |    |    |    |                |    |    |    |
| 0h             |    |    |    |                |    |    |    |
| 23             | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| NU16           |    |    |    | SEG_START_ADDR |    |    |    |
| R              |    |    |    | R/W            |    |    |    |
| 0h             |    |    |    | 0h             |    |    |    |
| 15             | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| SEG_START_ADDR |    |    |    |                |    |    |    |
| R/W            |    |    |    |                |    |    |    |
| 0h             |    |    |    |                |    |    |    |
| 7              | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| SEG_START_ADDR |    |    |    |                |    |    |    |
| R/W            |    |    |    |                |    |    |    |
| 0h             |    |    |    |                |    |    |    |

**Table 4-385. STC\_SEG3\_START\_ADDR Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | NU16           | R    | 0h    | Reserved bits                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 19:0  | SEG_START_ADDR | R/W  | 0h    | Segment 3 Start Address [RWP - Read, Priviledge Mode Write only]<br>This register holds the ROM address for the start of first interval of the segment.<br>When STC_GCR0.RS_CNT_B1 field is set to [1x] PRELOAD option, this register is used to determine the ROM start address for the Segment selected in ST_SEGPLR register.<br>Valid number of bits depends on RTL parameter ADDR.<br>This register is present only when RTL parameter NUM_SEG = 3. |

#### 4.1.2.123 STC\_CORE1\_CURMISR\_0 Register

##### 1 STC\_CORE1\_CURMISR\_0 Register (Offset = 3Ch) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-386. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 003Ch       |
| R5SS1         | 5351 003Ch       |

**Figure 4-123. STC\_CORE1\_CURMISR\_0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-388. STC\_CORE1\_CURMISR\_0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|---------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR0 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.124 STC\_CORE1\_CURMISR\_1 Register

##### 1 STC\_CORE1\_CURMISR\_1 Register (Offset = 40h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-389. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0040h       |
| R5SS1         | 5351 0040h       |

**Figure 4-124. STC\_CORE1\_CURMISR\_1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-391. STC\_CORE1\_CURMISR\_1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|---------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR1 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.125 STC\_CORE1\_CURMISR\_2 Register

##### 1 STC\_CORE1\_CURMISR\_2 Register (Offset = 44h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-392. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0044h       |
| R5SS1         | 5351 0044h       |

**Figure 4-125. STC\_CORE1\_CURMISR\_2 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR2 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR2 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR2 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR2 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-394. STC\_CORE1\_CURMISR\_2 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|---------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR2 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.126 STC\_CORE1\_CURMISR\_3 Register

##### 1 STC\_CORE1\_CURMISR\_3 Register (Offset = 48h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-395. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0048h       |
| R5SS1         | 5351 0048h       |

**Figure 4-126. STC\_CORE1\_CURMISR\_3 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR3 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR3 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR3 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR3 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-397. STC\_CORE1\_CURMISR\_3 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|---------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR3 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.127 STC\_CORE1\_CURMISR\_4 Register

##### 1 STC\_CORE1\_CURMISR\_4 Register (Offset = 4Ch) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-398. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 004Ch       |
| R5SS1         | 5351 004Ch       |

**Figure 4-127. STC\_CORE1\_CURMISR\_4 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR4 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR4 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR4 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR4 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-400. STC\_CORE1\_CURMISR\_4 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|---------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR4 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.128 STC\_CORE1\_CURMISR\_5 Register

##### 1 STC\_CORE1\_CURMISR\_5 Register (Offset = 50h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-401. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0050h       |
| R5SS1         | 5351 0050h       |

**Figure 4-128. STC\_CORE1\_CURMISR\_5 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR5 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR5 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR5 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR5 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-403. STC\_CORE1\_CURMISR\_5 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|---------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR5 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.129 STC\_CORE1\_CURMISR\_6 Register

##### 1 STC\_CORE1\_CURMISR\_6 Register (Offset = 54h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-404. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0054h       |
| R5SS1         | 5351 0054h       |

**Figure 4-129. STC\_CORE1\_CURMISR\_6 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR6 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR6 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR6 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR6 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-406. STC\_CORE1\_CURMISR\_6 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|---------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR6 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |



#### 4.1.2.130 STC\_CORE1\_CURMISR\_7 Register

##### 1 STC\_CORE1\_CURMISR\_7 Register (Offset = 58h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-407. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0058h       |
| R5SS1         | 5351 0058h       |

**Figure 4-130. STC\_CORE1\_CURMISR\_7 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR7 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR7 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR7 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR7 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-409. STC\_CORE1\_CURMISR\_7 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|---------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR7 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.131 STC\_CORE1\_CURMISR\_8 Register

##### 1 STC\_CORE1\_CURMISR\_8 Register (Offset = 5Ch) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-410. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 005Ch       |
| R5SS1         | 5351 005Ch       |

**Figure 4-131. STC\_CORE1\_CURMISR\_8 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR8 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR8 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR8 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR8 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-412. STC\_CORE1\_CURMISR\_8 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|---------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR8 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.132 STC\_CORE1\_CURMISR\_9 Register

##### 1 STC\_CORE1\_CURMISR\_9 Register (Offset = 60h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-413. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0060h       |
| R5SS1         | 5351 0060h       |

**Figure 4-132. STC\_CORE1\_CURMISR\_9 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR9 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR9 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR9 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR9 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-415. STC\_CORE1\_CURMISR\_9 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|---------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR9 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.133 STC\_CORE1\_CURMISR\_10 Register

##### 1 STC\_CORE1\_CURMISR\_10 Register (Offset = 64h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-416. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0064h       |
| R5SS1         | 5351 0064h       |

**Figure 4-133. STC\_CORE1\_CURMISR\_10 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR10 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR10 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR10 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR10 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-418. STC\_CORE1\_CURMISR\_10 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR10 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.134 STC\_CORE1\_CURMISR\_11 Register

##### 1 STC\_CORE1\_CURMISR\_11 Register (Offset = 68h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-419. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0068h       |
| R5SS1         | 5351 0068h       |

**Figure 4-134. STC\_CORE1\_CURMISR\_11 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR11 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR11 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR11 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR11 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-421. STC\_CORE1\_CURMISR\_11 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR11 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.135 STC\_CORE1\_CURMISR\_12 Register

##### 1 STC\_CORE1\_CURMISR\_12 Register (Offset = 6Ch) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-422. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 006Ch       |
| R5SS1         | 5351 006Ch       |

**Figure 4-135. STC\_CORE1\_CURMISR\_12 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR12 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR12 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR12 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR12 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-424. STC\_CORE1\_CURMISR\_12 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR12 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.136 STC\_CORE1\_CURMISR\_13 Register

##### 1 STC\_CORE1\_CURMISR\_13 Register (Offset = 70h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-425. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0070h       |
| R5SS1         | 5351 0070h       |

**Figure 4-136. STC\_CORE1\_CURMISR\_13 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR13 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR13 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR13 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR13 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-427. STC\_CORE1\_CURMISR\_13 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR13 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.137 STC\_CORE1\_CURMISR\_14 Register

##### 1 STC\_CORE1\_CURMISR\_14 Register (Offset = 74h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-428. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0074h       |
| R5SS1         | 5351 0074h       |

**Figure 4-137. STC\_CORE1\_CURMISR\_14 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR14 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR14 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR14 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR14 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-430. STC\_CORE1\_CURMISR\_14 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR14 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |



#### 4.1.2.138 STC\_CORE1\_CURMISR\_15 Register

##### 1 STC\_CORE1\_CURMISR\_15 Register (Offset = 78h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-431. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0078h       |
| R5SS1         | 5351 0078h       |

**Figure 4-138. STC\_CORE1\_CURMISR\_15 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR15 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR15 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR15 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR15 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-433. STC\_CORE1\_CURMISR\_15 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR15 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.139 STC\_CORE1\_CURMISR\_16 Register

##### 1 STC\_CORE1\_CURMISR\_16 Register (Offset = 7Ch) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-434. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 007Ch       |
| R5SS1         | 5351 007Ch       |

**Figure 4-139. STC\_CORE1\_CURMISR\_16 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR16 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR16 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR16 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR16 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-436. STC\_CORE1\_CURMISR\_16 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR16 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.140 STC\_CORE1\_CURMISR\_17 Register

##### 1 STC\_CORE1\_CURMISR\_17 Register (Offset = 80h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-437. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0080h       |
| R5SS1         | 5351 0080h       |

**Figure 4-140. STC\_CORE1\_CURMISR\_17 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR17 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR17 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR17 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR17 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-439. STC\_CORE1\_CURMISR\_17 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR17 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.141 STC\_CORE1\_CURMISR\_18 Register

##### 1 STC\_CORE1\_CURMISR\_18 Register (Offset = 84h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-440. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0084h       |
| R5SS1         | 5351 0084h       |

**Figure 4-141. STC\_CORE1\_CURMISR\_18 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR18 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR18 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR18 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR18 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-442. STC\_CORE1\_CURMISR\_18 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR18 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.142 STC\_CORE1\_CURMISR\_19 Register

##### 1 STC\_CORE1\_CURMISR\_19 Register (Offset = 88h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-443. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0088h       |
| R5SS1         | 5351 0088h       |

**Figure 4-142. STC\_CORE1\_CURMISR\_19 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR19 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR19 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR19 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR19 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-445. STC\_CORE1\_CURMISR\_19 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR19 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.143 STC\_CORE1\_CURMISR\_20 Register

##### 1 STC\_CORE1\_CURMISR\_20 Register (Offset = 8Ch) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-446. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 008Ch       |
| R5SS1         | 5351 008Ch       |

**Figure 4-143. STC\_CORE1\_CURMISR\_20 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR20 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR20 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR20 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR20 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-448. STC\_CORE1\_CURMISR\_20 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR20 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.144 STC\_CORE1\_CURMISR\_21 Register

##### 1 STC\_CORE1\_CURMISR\_21 Register (Offset = 90h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-449. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0090h       |
| R5SS1         | 5351 0090h       |

**Figure 4-144. STC\_CORE1\_CURMISR\_21 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR21 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR21 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR21 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR21 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-451. STC\_CORE1\_CURMISR\_21 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR21 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.145 STC\_CORE1\_CURMISR\_22 Register

##### 1 STC\_CORE1\_CURMISR\_22 Register (Offset = 94h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-452. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0094h       |
| R5SS1         | 5351 0094h       |

**Figure 4-145. STC\_CORE1\_CURMISR\_22 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR22 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR22 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR22 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR22 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-454. STC\_CORE1\_CURMISR\_22 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR22 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |



#### 4.1.2.146 STC\_CORE1\_CURMISR\_23 Register

##### 1 STC\_CORE1\_CURMISR\_23 Register (Offset = 98h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-455. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0098h       |
| R5SS1         | 5351 0098h       |

**Figure 4-146. STC\_CORE1\_CURMISR\_23 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR23 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR23 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR23 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR23 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-457. STC\_CORE1\_CURMISR\_23 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR23 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.147 STC\_CORE1\_CURMISR\_24 Register

##### 1 STC\_CORE1\_CURMISR\_24 Register (Offset = 9Ch) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-458. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 009Ch       |
| R5SS1         | 5351 009Ch       |

**Figure 4-147. STC\_CORE1\_CURMISR\_24 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR24 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR24 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR24 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR24 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-460. STC\_CORE1\_CURMISR\_24 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR24 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.148 STC\_CORE1\_CURMISR\_25 Register

##### 1 STC\_CORE1\_CURMISR\_25 Register (Offset = A0h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-461. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 00A0h       |
| R5SS1         | 5351 00A0h       |

**Figure 4-148. STC\_CORE1\_CURMISR\_25 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR25 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR25 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR25 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR25 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-463. STC\_CORE1\_CURMISR\_25 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR25 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.149 STC\_CORE1\_CURMISR\_26 Register

##### 1 STC\_CORE1\_CURMISR\_26 Register (Offset = A4h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-464. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 00A4h       |
| R5SS1         | 5351 00A4h       |

**Figure 4-149. STC\_CORE1\_CURMISR\_26 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR26 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR26 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR26 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR26 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-466. STC\_CORE1\_CURMISR\_26 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR26 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.150 STC\_CORE1\_CURMISR\_27 Register

##### 1 STC\_CORE1\_CURMISR\_27 Register (Offset = A8h) [reset = 0h]

Holds the MISR signature for CORE1.

Return to [Summary Table](#)

**Table 4-467. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 00A8h       |
| R5SS1         | 5351 00A8h       |

**Figure 4-150. STC\_CORE1\_CURMISR\_27 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C1MISR27 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C1MISR27 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C1MISR27 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C1MISR27 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-469. STC\_CORE1\_CURMISR\_27 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C1MISR27 | R    | 0h    | MISR Signature for CORE1<br>This register contains the MISR data of the current interval for CORE1 in the case of segment0 and the remaining Segments 1 to 3. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.151 STC\_CORE2\_CURMISR\_0 Register

##### 1 STC\_CORE2\_CURMISR\_0 Register (Offset = ACh) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-470. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 00ACh       |
| R5SS1         | 5351 00ACh       |

**Figure 4-151. STC\_CORE2\_CURMISR\_0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-472. STC\_CORE2\_CURMISR\_0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|---------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR0 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.152 STC\_CORE2\_CURMISR\_1 Register

##### 1 STC\_CORE2\_CURMISR\_1 Register (Offset = B0h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-473. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 00B0h       |
| R5SS1         | 5351 00B0h       |

**Figure 4-152. STC\_CORE2\_CURMISR\_1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-475. STC\_CORE2\_CURMISR\_1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|---------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR1 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.153 STC\_CORE2\_CURMISR\_2 Register

##### 1 STC\_CORE2\_CURMISR\_2 Register (Offset = B4h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-476. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 00B4h       |
| R5SS1         | 5351 00B4h       |

**Figure 4-153. STC\_CORE2\_CURMISR\_2 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR2 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR2 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR2 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR2 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-478. STC\_CORE2\_CURMISR\_2 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|---------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR2 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |



#### 4.1.2.154 STC\_CORE2\_CURMISR\_3 Register

##### 1 STC\_CORE2\_CURMISR\_3 Register (Offset = B8h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-479. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 00B8h       |
| R5SS1         | 5351 00B8h       |

**Figure 4-154. STC\_CORE2\_CURMISR\_3 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR3 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR3 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR3 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR3 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-481. STC\_CORE2\_CURMISR\_3 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|---------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR3 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.155 STC\_CORE2\_CURMISR\_4 Register

##### 1 STC\_CORE2\_CURMISR\_4 Register (Offset = BCh) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-482. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 00BCh       |
| R5SS1         | 5351 00BCh       |

**Figure 4-155. STC\_CORE2\_CURMISR\_4 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR4 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR4 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR4 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR4 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-484. STC\_CORE2\_CURMISR\_4 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|---------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR4 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.156 STC\_CORE2\_CURMISR\_5 Register

##### 1 STC\_CORE2\_CURMISR\_5 Register (Offset = C0h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-485. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 00C0h       |
| R5SS1         | 5351 00C0h       |

**Figure 4-156. STC\_CORE2\_CURMISR\_5 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR5 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR5 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR5 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR5 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-487. STC\_CORE2\_CURMISR\_5 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|---------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR5 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.157 STC\_CORE2\_CURMISR\_6 Register

##### 1 STC\_CORE2\_CURMISR\_6 Register (Offset = C4h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-488. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 00C4h       |
| R5SS1         | 5351 00C4h       |

**Figure 4-157. STC\_CORE2\_CURMISR\_6 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR6 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR6 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR6 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR6 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-490. STC\_CORE2\_CURMISR\_6 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|---------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR6 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.158 STC\_CORE2\_CURMISR\_7 Register

##### 1 STC\_CORE2\_CURMISR\_7 Register (Offset = C8h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-491. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 00C8h       |
| R5SS1         | 5351 00C8h       |

**Figure 4-158. STC\_CORE2\_CURMISR\_7 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR7 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR7 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR7 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR7 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-493. STC\_CORE2\_CURMISR\_7 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|---------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR7 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.159 STC\_CORE2\_CURMISR\_8 Register

##### 1 STC\_CORE2\_CURMISR\_8 Register (Offset = CCh) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-494. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 00CCh       |
| R5SS1         | 5351 00CCh       |

**Figure 4-159. STC\_CORE2\_CURMISR\_8 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR8 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR8 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR8 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR8 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-496. STC\_CORE2\_CURMISR\_8 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|---------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR8 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.160 STC\_CORE2\_CURMISR\_9 Register

##### 1 STC\_CORE2\_CURMISR\_9 Register (Offset = D0h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-497. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 00D0h       |
| R5SS1         | 5351 00D0h       |

**Figure 4-160. STC\_CORE2\_CURMISR\_9 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR9 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR9 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR9 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR9 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-499. STC\_CORE2\_CURMISR\_9 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|---------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR9 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.161 STC\_CORE2\_CURMISR\_10 Register

##### 1 STC\_CORE2\_CURMISR\_10 Register (Offset = D4h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-500. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 00D4h       |
| R5SS1         | 5351 00D4h       |

**Figure 4-161. STC\_CORE2\_CURMISR\_10 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR10 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR10 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR10 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR10 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-502. STC\_CORE2\_CURMISR\_10 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR10 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |



#### 4.1.2.162 STC\_CORE2\_CURMISR\_11 Register

##### 1 STC\_CORE2\_CURMISR\_11 Register (Offset = D8h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-503. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 00D8h       |
| R5SS1         | 5351 00D8h       |

**Figure 4-162. STC\_CORE2\_CURMISR\_11 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR11 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR11 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR11 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR11 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-505. STC\_CORE2\_CURMISR\_11 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR11 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.163 STC\_CORE2\_CURMISR\_12 Register

##### 1 STC\_CORE2\_CURMISR\_12 Register (Offset = DCh) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-506. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 00DCh       |
| R5SS1         | 5351 00DCh       |

**Figure 4-163. STC\_CORE2\_CURMISR\_12 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR12 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR12 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR12 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR12 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-508. STC\_CORE2\_CURMISR\_12 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR12 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.164 STC\_CORE2\_CURMISR\_13 Register

##### 1 STC\_CORE2\_CURMISR\_13 Register (Offset = E0h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-509. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 00E0h       |
| R5SS1         | 5351 00E0h       |

**Figure 4-164. STC\_CORE2\_CURMISR\_13 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR13 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR13 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR13 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR13 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-511. STC\_CORE2\_CURMISR\_13 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR13 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.165 STC\_CORE2\_CURMISR\_14 Register

##### 1 STC\_CORE2\_CURMISR\_14 Register (Offset = E4h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-512. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 00E4h       |
| R5SS1         | 5351 00E4h       |

**Figure 4-165. STC\_CORE2\_CURMISR\_14 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR14 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR14 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR14 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR14 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-514. STC\_CORE2\_CURMISR\_14 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR14 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.166 STC\_CORE2\_CURMISR\_15 Register

##### 1 STC\_CORE2\_CURMISR\_15 Register (Offset = E8h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-515. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 00E8h       |
| R5SS1         | 5351 00E8h       |

**Figure 4-166. STC\_CORE2\_CURMISR\_15 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR15 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR15 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR15 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR15 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-517. STC\_CORE2\_CURMISR\_15 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR15 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.167 STC\_CORE2\_CURMISR\_16 Register

##### 1 STC\_CORE2\_CURMISR\_16 Register (Offset = ECh) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-518. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 00ECh       |
| R5SS1         | 5351 00ECh       |

**Figure 4-167. STC\_CORE2\_CURMISR\_16 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR16 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR16 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR16 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR16 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-520. STC\_CORE2\_CURMISR\_16 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR16 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.168 STC\_CORE2\_CURMISR\_17 Register

##### 1 STC\_CORE2\_CURMISR\_17 Register (Offset = F0h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-521. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 00F0h       |
| R5SS1         | 5351 00F0h       |

**Figure 4-168. STC\_CORE2\_CURMISR\_17 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR17 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR17 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR17 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR17 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-523. STC\_CORE2\_CURMISR\_17 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR17 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.169 STC\_CORE2\_CURMISR\_18 Register

##### 1 STC\_CORE2\_CURMISR\_18 Register (Offset = F4h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-524. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 00F4h       |
| R5SS1         | 5351 00F4h       |

**Figure 4-169. STC\_CORE2\_CURMISR\_18 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR18 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR18 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR18 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR18 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-526. STC\_CORE2\_CURMISR\_18 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR18 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |



#### 4.1.2.170 STC\_CORE2\_CURMISR\_19 Register

##### 1 STC\_CORE2\_CURMISR\_19 Register (Offset = F8h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-527. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 00F8h       |
| R5SS1         | 5351 00F8h       |

**Figure 4-170. STC\_CORE2\_CURMISR\_19 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR19 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR19 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR19 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR19 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-529. STC\_CORE2\_CURMISR\_19 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR19 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.171 STC\_CORE2\_CURMISR\_20 Register

##### 1 STC\_CORE2\_CURMISR\_20 Register (Offset = FCh) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-530. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 00FCh       |
| R5SS1         | 5351 00FCh       |

**Figure 4-171. STC\_CORE2\_CURMISR\_20 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR20 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR20 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR20 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR20 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-532. STC\_CORE2\_CURMISR\_20 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR20 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.172 STC\_CORE2\_CURMISR\_21 Register

##### 1 STC\_CORE2\_CURMISR\_21 Register (Offset = 100h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-533. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0100h       |
| R5SS1         | 5351 0100h       |

**Figure 4-172. STC\_CORE2\_CURMISR\_21 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR21 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR21 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR21 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR21 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-535. STC\_CORE2\_CURMISR\_21 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR21 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.173 STC\_CORE2\_CURMISR\_22 Register

##### 1 STC\_CORE2\_CURMISR\_22 Register (Offset = 104h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-536. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0104h       |
| R5SS1         | 5351 0104h       |

**Figure 4-173. STC\_CORE2\_CURMISR\_22 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR22 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR22 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR22 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR22 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-538. STC\_CORE2\_CURMISR\_22 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR22 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.174 STC\_CORE2\_CURMISR\_23 Register

##### 1 STC\_CORE2\_CURMISR\_23 Register (Offset = 108h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-539. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0108h       |
| R5SS1         | 5351 0108h       |

**Figure 4-174. STC\_CORE2\_CURMISR\_23 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR23 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR23 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR23 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR23 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-541. STC\_CORE2\_CURMISR\_23 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR23 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.175 STC\_CORE2\_CURMISR\_24 Register

##### 1 STC\_CORE2\_CURMISR\_24 Register (Offset = 10Ch) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-542. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 010Ch       |
| R5SS1         | 5351 010Ch       |

**Figure 4-175. STC\_CORE2\_CURMISR\_24 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR24 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR24 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR24 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR24 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-544. STC\_CORE2\_CURMISR\_24 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR24 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.176 STC\_CORE2\_CURMISR\_25 Register

##### 1 STC\_CORE2\_CURMISR\_25 Register (Offset = 110h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-545. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0110h       |
| R5SS1         | 5351 0110h       |

**Figure 4-176. STC\_CORE2\_CURMISR\_25 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR25 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR25 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR25 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR25 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-547. STC\_CORE2\_CURMISR\_25 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR25 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.177 STC\_CORE2\_CURMISR\_26 Register

##### 1 STC\_CORE2\_CURMISR\_26 Register (Offset = 114h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-548. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0114h       |
| R5SS1         | 5351 0114h       |

**Figure 4-177. STC\_CORE2\_CURMISR\_26 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR26 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR26 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR26 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR26 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-550. STC\_CORE2\_CURMISR\_26 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR26 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |



#### 4.1.2.178 STC\_CORE2\_CURMISR\_27 Register

##### 1 STC\_CORE2\_CURMISR\_27 Register (Offset = 118h) [reset = 0h]

Holds the MISR signature for CORE2.

Return to [Summary Table](#)

**Table 4-551. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 5350 0118h       |
| R5SS1         | 5351 0118h       |

**Figure 4-178. STC\_CORE2\_CURMISR\_27 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| C2MISR27 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| C2MISR27 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| C2MISR27 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| C2MISR27 |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-553. STC\_CORE2\_CURMISR\_27 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                           |
|------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | C2MISR27 | R    | 0h    | MISR Signature for CORE2<br>This register contains the MISR data from the CORE2 for the current interval. This is applicable to Segment 0 alone. This value will be compared with the GOLDEN MISR value copied from ROM. This register gets reset to its default value with Power on or system reset assertion. The MISR values should be read only after the Self Test is completed. |

#### 4.1.2.179 ICACHE\_CORE0\_START Register

##### 1 ICACHE\_CORE0\_START Register (Offset = 0h) [reset = 0h]

Return to [Summary Table](#)

**Table 4-554. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 7400 0000h       |
| R5SS1         | 7600 0000h       |

**Figure 4-179. ICACHE\_CORE0\_START Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-556. ICACHE\_CORE0\_START Register Field Descriptions**

| Bit  | Field | Type | Reset | Description          |
|------|-------|------|-------|----------------------|
| 31:0 | START | R/W  | 0h    | Memory start address |

#### 4.1.2.180 ICACHE\_CORE0\_END Register

##### 1 ICACHE\_CORE0\_END Register (Offset = 7FFFFCh) [reset = 0h]

Return to [Summary Table](#)

**Table 4-557. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 747F FFFCh       |
| R5SS1         | 767F FFFCh       |

**Figure 4-180. ICACHE\_CORE0\_END Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 4-559. ICACHE\_CORE0\_END Register Field Descriptions**

| Bit  | Field | Type | Reset | Description        |
|------|-------|------|-------|--------------------|
| 31:0 | END   | R/W  | 0h    | Memory end address |

#### 4.1.2.181 DCACHE\_CORE0\_START Register

##### 1 DCACHE\_CORE0\_START Register (Offset = 0h) [reset = 0h]

Return to [Summary Table](#)

**Table 4-560. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 7480 0000h       |
| R5SS1         | 7680 0000h       |

**Figure 4-181. DCACHE\_CORE0\_START Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-562. DCACHE\_CORE0\_START Register Field Descriptions**

| Bit  | Field | Type | Reset | Description          |
|------|-------|------|-------|----------------------|
| 31:0 | START | R/W  | 0h    | Memory start address |

#### 4.1.2.182 DCACHE\_CORE0\_END Register

**1 DCACHE\_CORE0\_END Register (Offset = 7FFFFCh) [reset = 0h]**

Return to [Summary Table](#)

**Table 4-563. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 74FF FFFCh       |
| R5SS1         | 76FF FFFCh       |

**Figure 4-182. DCACHE\_CORE0\_END Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 4-565. DCACHE\_CORE0\_END Register Field Descriptions**

| Bit  | Field | Type | Reset | Description        |
|------|-------|------|-------|--------------------|
| 31:0 | END   | R/W  | 0h    | Memory end address |

#### 4.1.2.183 ICACHE\_CORE1\_START Register

##### 1 ICACHE\_CORE1\_START Register (Offset = 0h) [reset = 0h]

Return to [Summary Table](#)

**Table 4-566. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 7500 0000h       |
| R5SS1         | 7700 0000h       |

**Figure 4-183. ICACHE\_CORE1\_START Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-568. ICACHE\_CORE1\_START Register Field Descriptions**

| Bit  | Field | Type | Reset | Description          |
|------|-------|------|-------|----------------------|
| 31:0 | START | R/W  | 0h    | Memory start address |

#### 4.1.2.184 ICACHE\_CORE1\_END Register

##### 1 ICACHE\_CORE1\_END Register (Offset = 7FFFFCh) [reset = 0h]

Return to [Summary Table](#)

**Table 4-569. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 757F FFFCh       |
| R5SS1         | 777F FFFCh       |

**Figure 4-184. ICACHE\_CORE1\_END Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 4-571. ICACHE\_CORE1\_END Register Field Descriptions**

| Bit  | Field | Type | Reset | Description        |
|------|-------|------|-------|--------------------|
| 31:0 | END   | R/W  | 0h    | Memory end address |

#### 4.1.2.185 DCACHE\_CORE1\_START Register

##### 1 DCACHE\_CORE1\_START Register (Offset = 0h) [reset = 0h]

Return to [Summary Table](#)

**Table 4-572. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 7580 0000h       |
| R5SS1         | 7780 0000h       |

**Figure 4-185. DCACHE\_CORE1\_START Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-574. DCACHE\_CORE1\_START Register Field Descriptions**

| Bit  | Field | Type | Reset | Description          |
|------|-------|------|-------|----------------------|
| 31:0 | START | R/W  | 0h    | Memory start address |



#### 4.1.2.186 DCACHE\_CORE1\_END Register

**1 DCACHE\_CORE1\_END Register (Offset = 7FFFFCh) [reset = 0h]**

Return to [Summary Table](#)

**Table 4-575. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 75FF FFFCh       |
| R5SS1         | 77FF FFFCh       |

**Figure 4-186. DCACHE\_CORE1\_END Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 4-577. DCACHE\_CORE1\_END Register Field Descriptions**

| Bit  | Field | Type | Reset | Description        |
|------|-------|------|-------|--------------------|
| 31:0 | END   | R/W  | 0h    | Memory end address |

#### 4.1.2.187 TCMA\_CORE0\_START Register

**1 TCMA\_CORE0\_START Register (Offset = 0h) [reset = 0h]**

Return to [Summary Table](#)

**Table 4-578. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 7800 0000h       |
| R5SS1         | 7840 0000h       |

**Figure 4-187. TCMA\_CORE0\_START Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-580. TCMA\_CORE0\_START Register Field Descriptions**

| Bit  | Field | Type | Reset | Description        |
|------|-------|------|-------|--------------------|
| 31:0 | START | R/W  | 0h    | TCMA start address |

#### 4.1.2.188 TCMA\_CORE0\_END Register

**1 TCMA\_CORE0\_END Register (Offset = 27FFCh) [reset = 0h]**

Return to [Summary Table](#)

**Table 4-581. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 7802 7FFCh       |
| R5SS1         | 7842 7FFCh       |

**Figure 4-188. TCMA\_CORE0\_END Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 4-583. TCMA\_CORE0\_END Register Field Descriptions**

| Bit  | Field | Type | Reset | Description      |
|------|-------|------|-------|------------------|
| 31:0 | END   | R/W  | 0h    | TCMA end address |

#### 4.1.2.189 TCMB\_CORE0\_START Register

1 TCMB\_CORE0\_START Register (Offset = 0h) [reset = 0h]

Return to [Summary Table](#)

**Table 4-584. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 7810 0000h       |
| R5SS1         | 7850 0000h       |

**Figure 4-189. TCMB\_CORE0\_START Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-586. TCMB\_CORE0\_START Register Field Descriptions**

| Bit  | Field | Type | Reset | Description        |
|------|-------|------|-------|--------------------|
| 31:0 | START | R/W  | 0h    | TCMB start address |

#### 4.1.2.190 TCMB\_CORE0\_END Register

**1 TCMB\_CORE0\_END Register (Offset = 2FFFCh) [reset = 0h]**

Return to [Summary Table](#)

**Table 4-587. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 7812 FFFCh       |
| R5SS1         | 7852 FFFCh       |

**Figure 4-190. TCMB\_CORE0\_END Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 4-589. TCMB\_CORE0\_END Register Field Descriptions**

| Bit  | Field | Type | Reset | Description      |
|------|-------|------|-------|------------------|
| 31:0 | END   | R/W  | 0h    | TCMB end address |

#### 4.1.2.191 TCMA\_CORE1\_START Register

1 TCMA\_CORE1\_START Register (Offset = 0h) [reset = 0h]

Return to [Summary Table](#)

**Table 4-590. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 7820 0000h       |
| R5SS1         | 7860 0000h       |

**Figure 4-191. TCMA\_CORE1\_START Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-592. TCMA\_CORE1\_START Register Field Descriptions**

| Bit  | Field | Type | Reset | Description        |
|------|-------|------|-------|--------------------|
| 31:0 | START | R/W  | 0h    | TCMA start address |

#### 4.1.2.192 TCMA\_CORE1\_END Register

**1 TCMA\_CORE1\_END Register (Offset = 7FFCh) [reset = 0h]**

Return to [Summary Table](#)

**Table 4-593. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 7820 7FFCh       |
| R5SS1         | 7860 7FFCh       |

**Figure 4-192. TCMA\_CORE1\_END Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 4-595. TCMA\_CORE1\_END Register Field Descriptions**

| Bit  | Field | Type | Reset | Description      |
|------|-------|------|-------|------------------|
| 31:0 | END   | R/W  | 0h    | TCMA end address |

#### 4.1.2.193 TCMB\_CORE1\_START Register

1 TCMB\_CORE1\_START Register (Offset = 0h) [reset = 0h]

Return to [Summary Table](#)

**Table 4-596. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 7830 0000h       |
| R5SS1         | 7870 0000h       |

**Figure 4-193. TCMB\_CORE1\_START Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-598. TCMB\_CORE1\_START Register Field Descriptions**

| Bit  | Field | Type | Reset | Description        |
|------|-------|------|-------|--------------------|
| 31:0 | START | R/W  | 0h    | TCMB start address |



#### 4.1.2.194 TCMB\_CORE1\_END Register

**1 TCMB\_CORE1\_END Register (Offset = 17FFCh) [reset = 0h]**

Return to [Summary Table](#)

**Table 4-599. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| R5SS0         | 7831 7FFCh       |
| R5SS1         | 7871 7FFCh       |

**Figure 4-194. TCMB\_CORE1\_END Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 4-601. TCMB\_CORE1\_END Register Field Descriptions**

| Bit  | Field | Type | Reset | Description      |
|------|-------|------|-------|------------------|
| 31:0 | END   | R/W  | 0h    | TCMB end address |

## 4.2 ICSSM

### ICSSM

#### 4.2.1 ICSSM Summaries

#### ICSSM Summaries

**Table 4-602. ICSSM\_DRAM0\_SLV\_RAM Registers, Base Address=4800 0000h, Length=8192**

| Offset | Length | Register Name                                 | ICSSM0 Physical Address |
|--------|--------|-----------------------------------------------|-------------------------|
| 0h     | 32     | <a href="#">ICSSM_DRAM0_SLV_RAM_RAM_REG_J</a> | 4800 0000h + formula    |

**Table 4-603. ICSSM\_DRAM1\_SLV\_RAM Registers, Base Address=4800 2000h, Length=8192**

| Offset | Length | Register Name                                 | ICSSM0 Physical Address |
|--------|--------|-----------------------------------------------|-------------------------|
| 0h     | 32     | <a href="#">ICSSM_DRAM1_SLV_RAM_RAM_REG_J</a> | 4800 2000h + formula    |

**Table 4-604. RAT Registers, Base Address=4800 8000h, Length=4096**

| Offset | Length | Register Name                                 | ICSSM0 Physical Address |
|--------|--------|-----------------------------------------------|-------------------------|
| 0h     | 32     | <a href="#">RAT_PID</a>                       | 4800 8000h              |
| 4h     | 32     | <a href="#">RAT_CONFIG</a>                    | 4800 8004h              |
| 804h   | 32     | <a href="#">RAT_DESTINATION_ID</a>            | 4800 8804h              |
| 820h   | 32     | <a href="#">RAT_EXCEPTION_LOGGING_CONTROL</a> | 4800 8820h              |
| 824h   | 32     | <a href="#">RAT_EXCEPTION_LOGGING_HEADER0</a> | 4800 8824h              |
| 828h   | 32     | <a href="#">RAT_EXCEPTION_LOGGING_HEADER1</a> | 4800 8828h              |
| 82Ch   | 32     | <a href="#">RAT_EXCEPTION_LOGGING_DATA0</a>   | 4800 882Ch              |
| 830h   | 32     | <a href="#">RAT_EXCEPTION_LOGGING_DATA1</a>   | 4800 8830h              |
| 834h   | 32     | <a href="#">RAT_EXCEPTION_LOGGING_DATA2</a>   | 4800 8834h              |
| 838h   | 32     | <a href="#">RAT_EXCEPTION_LOGGING_DATA3</a>   | 4800 8838h              |
| 840h   | 32     | <a href="#">RAT_EXCEPTION_PEND_SET</a>        | 4800 8840h              |
| 844h   | 32     | <a href="#">RAT_EXCEPTION_PEND_CLEAR</a>      | 4800 8844h              |
| 848h   | 32     | <a href="#">RAT_EXCEPTION_ENABLE_SET</a>      | 4800 8848h              |
| 84Ch   | 32     | <a href="#">RAT_EXCEPTION_ENABLE_CLEAR</a>    | 4800 884Ch              |
| 850h   | 32     | <a href="#">RAT_EOI_REG</a>                   | 4800 8850h              |
| 20h    | 32     | <a href="#">RAT_REGION_CTRL_J</a>             | 4800 8020h + formula    |
| 24h    | 32     | <a href="#">RAT_REGION_BASE_J</a>             | 4800 8024h + formula    |
| 28h    | 32     | <a href="#">RAT_REGION_TRANS_L_J</a>          | 4800 8028h + formula    |
| 2Ch    | 32     | <a href="#">RAT_REGION_TRANS_U_J</a>          | 4800 802Ch + formula    |

**Table 4-605. RAT Registers, Base Address=4800 9000h, Length=4096**

| Offset | Length | Register Name                                 | ICSSM0 Physical Address |
|--------|--------|-----------------------------------------------|-------------------------|
| 0h     | 32     | <a href="#">RAT_PID</a>                       | 4800 9000h              |
| 4h     | 32     | <a href="#">RAT_CONFIG</a>                    | 4800 9004h              |
| 804h   | 32     | <a href="#">RAT_DESTINATION_ID</a>            | 4800 9804h              |
| 820h   | 32     | <a href="#">RAT_EXCEPTION_LOGGING_CONTROL</a> | 4800 9820h              |
| 824h   | 32     | <a href="#">RAT_EXCEPTION_LOGGING_HEADER0</a> | 4800 9824h              |
| 828h   | 32     | <a href="#">RAT_EXCEPTION_LOGGING_HEADER1</a> | 4800 9828h              |

**Table 4-605. RAT Registers, Base Address=4800 9000h, Length=4096 (continued)**

| Offset | Length | Register Name                               | ICSSM0 Physical Address |
|--------|--------|---------------------------------------------|-------------------------|
| 82Ch   | 32     | <a href="#">RAT_EXCEPTION_LOGGING_DATA0</a> | 4800 982Ch              |
| 830h   | 32     | <a href="#">RAT_EXCEPTION_LOGGING_DATA1</a> | 4800 9830h              |
| 834h   | 32     | <a href="#">RAT_EXCEPTION_LOGGING_DATA2</a> | 4800 9834h              |
| 838h   | 32     | <a href="#">RAT_EXCEPTION_LOGGING_DATA3</a> | 4800 9838h              |
| 840h   | 32     | <a href="#">RAT_EXCEPTION_PEND_SET</a>      | 4800 9840h              |
| 844h   | 32     | <a href="#">RAT_EXCEPTION_PEND_CLEAR</a>    | 4800 9844h              |
| 848h   | 32     | <a href="#">RAT_EXCEPTION_ENABLE_SET</a>    | 4800 9848h              |
| 84Ch   | 32     | <a href="#">RAT_EXCEPTION_ENABLE_CLEAR</a>  | 4800 984Ch              |
| 850h   | 32     | <a href="#">RAT_EOI_REG</a>                 | 4800 9850h              |
| 20h    | 32     | <a href="#">RAT_REGION_CTRL_J</a>           | 4800 9020h + formula    |
| 24h    | 32     | <a href="#">RAT_REGION_BASE_J</a>           | 4800 9024h + formula    |
| 28h    | 32     | <a href="#">RAT_REGION_TRANS_L_J</a>        | 4800 9028h + formula    |
| 2Ch    | 32     | <a href="#">RAT_REGION_TRANS_U_J</a>        | 4800 902Ch + formula    |

**Table 4-606. ICSSM\_RAM\_SLV\_RAM Registers, Base Address=4801 0000h, Length=32768**

| Offset | Length | Register Name                               | ICSSM0 Physical Address |
|--------|--------|---------------------------------------------|-------------------------|
| 0h     | 32     | <a href="#">ICSSM_RAM_SLV_RAM_RAM_REG_J</a> | 4801 0000h + formula    |

**Table 4-607. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV Registers, Base Address=4802 0000h, Length=8192**

| Offset | Length | Register Name                                                          | ICSSM0 Physical Address |
|--------|--------|------------------------------------------------------------------------|-------------------------|
| 0h     | 32     | <a href="#">ICSSM_PR1_ICSS_INTC_INTC_SLV_REVISION_REG</a>              | 4802 0000h              |
| 4h     | 32     | <a href="#">ICSSM_PR1_ICSS_INTC_INTC_SLV_CONTROL_REG</a>               | 4802 0004h              |
| 10h    | 32     | <a href="#">ICSSM_PR1_ICSS_INTC_INTC_SLV_GLOBAL_ENABLE_HINT_REG</a>    | 4802 0010h              |
| 1Ch    | 32     | <a href="#">ICSSM_PR1_ICSS_INTC_INTC_SLV_GLB_NEST_LEVEL_REG</a>        | 4802 001Ch              |
| 20h    | 32     | <a href="#">ICSSM_PR1_ICSS_INTC_INTC_SLV_STATUS_SET_INDEX_REG</a>      | 4802 0020h              |
| 24h    | 32     | <a href="#">ICSSM_PR1_ICSS_INTC_INTC_SLV_STATUS_CLR_INDEX_REG</a>      | 4802 0024h              |
| 28h    | 32     | <a href="#">ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_SET_INDEX_REG</a>      | 4802 0028h              |
| 2Ch    | 32     | <a href="#">ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_CLR_INDEX_REG</a>      | 4802 002Ch              |
| 34h    | 32     | <a href="#">ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_ENABLE_SET_INDEX_REG</a> | 4802 0034h              |
| 38h    | 32     | <a href="#">ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_ENABLE_CLR_INDEX_REG</a> | 4802 0038h              |
| 80h    | 32     | <a href="#">ICSSM_PR1_ICSS_INTC_INTC_SLV_GLB_PRI_INTR_REG</a>          | 4802 0080h              |
| 200h   | 32     | <a href="#">ICSSM_PR1_ICSS_INTC_INTC_SLV_RAW_STATUS_REG0</a>           | 4802 0200h              |
| 204h   | 32     | <a href="#">ICSSM_PR1_ICSS_INTC_INTC_SLV_RAW_STATUS_REG1</a>           | 4802 0204h              |
| 280h   | 32     | <a href="#">ICSSM_PR1_ICSS_INTC_INTC_SLV_ENA_STATUS_REG0</a>           | 4802 0280h              |
| 284h   | 32     | <a href="#">ICSSM_PR1_ICSS_INTC_INTC_SLV_ENA_STATUS_REG1</a>           | 4802 0284h              |

**Table 4-607. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV Registers, Base Address=4802 0000h, Length=8192  
(continued)**

| Offset | Length | Register Name                                    | ICSSM0 Physical Address |
|--------|--------|--------------------------------------------------|-------------------------|
| 300h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_REG0         | 4802 0300h              |
| 304h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_REG1         | 4802 0304h              |
| 380h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_CLR_REG<br>0 | 4802 0380h              |
| 384h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_CLR_REG<br>1 | 4802 0384h              |
| 400h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG0         | 4802 0400h              |
| 404h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG1         | 4802 0404h              |
| 408h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG2         | 4802 0408h              |
| 40Ch   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG3         | 4802 040Ch              |
| 410h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG4         | 4802 0410h              |
| 414h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG5         | 4802 0414h              |
| 418h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG6         | 4802 0418h              |
| 41Ch   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG7         | 4802 041Ch              |
| 420h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG8         | 4802 0420h              |
| 424h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG9         | 4802 0424h              |
| 428h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG10        | 4802 0428h              |
| 42Ch   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG11        | 4802 042Ch              |
| 430h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG12        | 4802 0430h              |
| 434h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG13        | 4802 0434h              |
| 438h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG14        | 4802 0438h              |
| 43Ch   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_CH_MAP_REG15        | 4802 043Ch              |
| 800h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_MAP_REG0       | 4802 0800h              |
| 804h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_MAP_REG1       | 4802 0804h              |
| 808h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_HINT_MAP_REG2       | 4802 0808h              |
| 900h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG0       | 4802 0900h              |
| 904h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG1       | 4802 0904h              |
| 908h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG2       | 4802 0908h              |
| 90Ch   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG3       | 4802 090Ch              |
| 910h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG4       | 4802 0910h              |
| 914h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG5       | 4802 0914h              |
| 918h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG6       | 4802 0918h              |
| 91Ch   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG7       | 4802 091Ch              |
| 920h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG8       | 4802 0920h              |
| 924h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_PRI_HINT_REG9       | 4802 0924h              |
| D00h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_POLARITY_REG0       | 4802 0D00h              |
| D04h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_POLARITY_REG1       | 4802 0D04h              |
| D80h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_TYPE_REG0           | 4802 0D80h              |
| D84h   | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_TYPE_REG1           | 4802 0D84h              |
| 1100h  | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG<br>0 | 4802 1100h              |
| 1104h  | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG<br>1 | 4802 1104h              |
| 1108h  | 32     | ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG<br>2 | 4802 1108h              |

**Table 4-607. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV Registers, Base Address=4802 0000h, Length=8192  
(continued)**

| Offset | Length | Register Name                                                 | ICSSM0 Physical Address |
|--------|--------|---------------------------------------------------------------|-------------------------|
| 110Ch  | 32     | <a href="#">ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG_3</a> | 4802 110Ch              |
| 1110h  | 32     | <a href="#">ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG_4</a> | 4802 1110h              |
| 1114h  | 32     | <a href="#">ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG_5</a> | 4802 1114h              |
| 1118h  | 32     | <a href="#">ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG_6</a> | 4802 1118h              |
| 111Ch  | 32     | <a href="#">ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG_7</a> | 4802 111Ch              |
| 1120h  | 32     | <a href="#">ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG_8</a> | 4802 1120h              |
| 1124h  | 32     | <a href="#">ICSSM_PR1_ICSS_INTC_INTC_SLV_NEST_LEVEL_REG_9</a> | 4802 1124h              |
| 1500h  | 32     | <a href="#">ICSSM_PR1_ICSS_INTC_INTC_SLV_ENABLE_HINT_REG0</a> | 4802 1500h              |

**Table 4-608. ICSSM\_PR1\_PROTECT\_SLV Registers, Base Address=4802 4C00h, Length=256**

| Offset | Length | Register Name                                    | ICSSM0 Physical Address |
|--------|--------|--------------------------------------------------|-------------------------|
| 0h     | 32     | <a href="#">ICSSM_PR1_PROTECT_SLV_UNLOCK_KEY</a> | 4802 4C00h              |
| 4h     | 32     | <a href="#">ICSSM_PR1_PROTECT_SLV_CFG</a>        | 4802 4C04h              |

**Table 4-609. ICSSM\_PR1\_CFG\_SLV Registers, Base Address=4802 6000h, Length=512**

| Offset | Length | Register Name                                              | ICSSM0 Physical Address |
|--------|--------|------------------------------------------------------------|-------------------------|
| 0h     | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PID_REG</a>                  | 4802 6000h              |
| 4h     | 32     | <a href="#">ICSSM_PR1_CFG_SLV_HWDIS_REG</a>                | 4802 6004h              |
| 8h     | 32     | <a href="#">ICSSM_PR1_CFG_SLV_GPCFG0_REG</a>               | 4802 6008h              |
| Ch     | 32     | <a href="#">ICSSM_PR1_CFG_SLV_GPCFG1_REG</a>               | 4802 600Ch              |
| 10h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_CGR_REG</a>                  | 4802 6010h              |
| 14h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_GPECFG0_REG</a>              | 4802 6014h              |
| 18h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_GPECFG1_REG</a>              | 4802 6018h              |
| 1Ch    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_RESET_ISO_REG</a>            | 4802 601Ch              |
| 2Ch    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_MII_RT_REG</a>               | 4802 602Ch              |
| 30h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_IEPCLK_REG</a>               | 4802 6030h              |
| 34h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_SPP_REG</a>                  | 4802 6034h              |
| 38h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_SPIN_CFG_REG</a>             | 4802 6038h              |
| 3Ch    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_CORE_SYNC_REG</a>            | 4802 603Ch              |
| 40h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_SA_MX_REG</a>                | 4802 6040h              |
| 44h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_DIV_REG</a>      | 4802 6044h              |
| 48h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG0</a>     | 4802 6048h              |
| 4Ch    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG0</a> | 4802 604Ch              |
| 50h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG1</a>     | 4802 6050h              |
| 54h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG1</a> | 4802 6054h              |
| 58h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG2</a>     | 4802 6058h              |
| 5Ch    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG2</a> | 4802 605Ch              |

**Table 4-609. ICSSM\_PR1\_CFG\_SLV Registers, Base Address=4802 6000h, Length=512 (continued)**

| Offset | Length | Register Name                                              | ICSSM0 Physical Address |
|--------|--------|------------------------------------------------------------|-------------------------|
| 60h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG3</a>     | 4802 6060h              |
| 64h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG3</a> | 4802 6064h              |
| 68h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG4</a>     | 4802 6068h              |
| 6Ch    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG4</a> | 4802 606Ch              |
| 70h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG5</a>     | 4802 6070h              |
| 74h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG5</a> | 4802 6074h              |
| 78h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG6</a>     | 4802 6078h              |
| 7Ch    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG6</a> | 4802 607Ch              |
| 80h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG7</a>     | 4802 6080h              |
| 84h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG7</a> | 4802 6084h              |
| 88h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU0_SD_CLK_SEL_REG8</a>     | 4802 6088h              |
| 8Ch    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU0_SD_SAMPLE_SIZE_REG8</a> | 4802 608Ch              |
| 90h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_DIV_REG</a>      | 4802 6090h              |
| 94h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG0</a>     | 4802 6094h              |
| 98h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG0</a> | 4802 6098h              |
| 9Ch    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG1</a>     | 4802 609Ch              |
| A0h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG1</a> | 4802 60A0h              |
| A4h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG2</a>     | 4802 60A4h              |
| A8h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG2</a> | 4802 60A8h              |
| ACh    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG3</a>     | 4802 60ACh              |
| B0h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG3</a> | 4802 60B0h              |
| B4h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG4</a>     | 4802 60B4h              |
| B8h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG4</a> | 4802 60B8h              |
| BCh    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG5</a>     | 4802 60BCh              |
| C0h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG5</a> | 4802 60C0h              |
| C4h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG6</a>     | 4802 60C4h              |
| C8h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG6</a> | 4802 60C8h              |
| CCh    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG7</a>     | 4802 60CCh              |
| D0h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG7</a> | 4802 60D0h              |
| D4h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU1_SD_CLK_SEL_REG8</a>     | 4802 60D4h              |
| D8h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU1_SD_SAMPLE_SIZE_REG8</a> | 4802 60D8h              |
| E0h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU0_ED_RX_CFG_REG</a>       | 4802 60E0h              |
| E4h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU0_ED_TX_CFG_REG</a>       | 4802 60E4h              |
| E8h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU0_ED_CH0_CFG0_REG</a>     | 4802 60E8h              |
| ECh    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU0_ED_CH0_CFG1_REG</a>     | 4802 60ECh              |
| F0h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU0_ED_CH1_CFG0_REG</a>     | 4802 60F0h              |
| F4h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU0_ED_CH1_CFG1_REG</a>     | 4802 60F4h              |
| F8h    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU0_ED_CH2_CFG0_REG</a>     | 4802 60F8h              |
| FCh    | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU0_ED_CH2_CFG1_REG</a>     | 4802 60FCh              |
| 100h   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU1_ED_RX_CFG_REG</a>       | 4802 6100h              |
| 104h   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU1_ED_TX_CFG_REG</a>       | 4802 6104h              |
| 108h   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU1_ED_CH0_CFG0_REG</a>     | 4802 6108h              |
| 10Ch   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU1_ED_CH0_CFG1_REG</a>     | 4802 610Ch              |
| 110h   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU1_ED_CH1_CFG0_REG</a>     | 4802 6110h              |
| 114h   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU1_ED_CH1_CFG1_REG</a>     | 4802 6114h              |

**Table 4-609. ICSSM\_PR1\_CFG\_SLV Registers, Base Address=4802 6000h, Length=512 (continued)**

| Offset | Length | Register Name                                          | ICSSM0 Physical Address |
|--------|--------|--------------------------------------------------------|-------------------------|
| 118h   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU1_ED_CH2_CFG0_REG</a> | 4802 6118h              |
| 11Ch   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PRU1_ED_CH2_CFG1_REG</a> | 4802 611Ch              |
| 124h   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_RTU0_POKE_EN0_REG</a>    | 4802 6124h              |
| 12Ch   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_RTU1_POKE_EN0_REG</a>    | 4802 612Ch              |
| 130h   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PWM0</a>                 | 4802 6130h              |
| 134h   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PWM1</a>                 | 4802 6134h              |
| 138h   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PWM2</a>                 | 4802 6138h              |
| 13Ch   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PWM3</a>                 | 4802 613Ch              |
| 140h   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PWM0_0</a>               | 4802 6140h              |
| 144h   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PWM0_1</a>               | 4802 6144h              |
| 148h   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PWM0_2</a>               | 4802 6148h              |
| 14Ch   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PWM1_0</a>               | 4802 614Ch              |
| 150h   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PWM1_1</a>               | 4802 6150h              |
| 154h   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PWM1_2</a>               | 4802 6154h              |
| 158h   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PWM2_0</a>               | 4802 6158h              |
| 15Ch   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PWM2_1</a>               | 4802 615Ch              |
| 160h   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PWM2_2</a>               | 4802 6160h              |
| 164h   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PWM3_0</a>               | 4802 6164h              |
| 168h   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PWM3_1</a>               | 4802 6168h              |
| 16Ch   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PWM3_2</a>               | 4802 616Ch              |
| 170h   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_SPIN_LOCK0</a>           | 4802 6170h              |
| 174h   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_SPIN_LOCK1</a>           | 4802 6174h              |
| 178h   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_CFG0</a>    | 4802 6178h              |
| 17Ch   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_STAT0</a>   | 4802 617Ch              |
| 180h   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_CFG1</a>    | 4802 6180h              |
| 184h   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_STAT1</a>   | 4802 6184h              |
| 188h   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_CFG2</a>    | 4802 6188h              |
| 18Ch   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_STAT2</a>   | 4802 618Ch              |
| 190h   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_CFG3</a>    | 4802 6190h              |
| 194h   | 32     | <a href="#">ICSSM_PR1_CFG_SLV_PA_STAT_PDSP_STAT3</a>   | 4802 6194h              |

**Table 4-610. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV Registers, Base Address=4802 8000h, Length=64**

| Offset | Length | Register Name                                       | ICSSM0 Physical Address |
|--------|--------|-----------------------------------------------------|-------------------------|
| 0h     | 32     | <a href="#">ICSSM_PR1_ICSS_UART_UART_SLV_RBR</a>    | 4802 8000h              |
| 4h     | 32     | <a href="#">ICSSM_PR1_ICSS_UART_UART_SLV_IER</a>    | 4802 8004h              |
| 8h     | 32     | <a href="#">ICSSM_PR1_ICSS_UART_UART_SLV_IIR</a>    | 4802 8008h              |
| Ch     | 32     | <a href="#">ICSSM_PR1_ICSS_UART_UART_SLV_LCR</a>    | 4802 800Ch              |
| 10h    | 32     | <a href="#">ICSSM_PR1_ICSS_UART_UART_SLV_MCR</a>    | 4802 8010h              |
| 14h    | 32     | <a href="#">ICSSM_PR1_ICSS_UART_UART_SLV_LSR</a>    | 4802 8014h              |
| 18h    | 32     | <a href="#">ICSSM_PR1_ICSS_UART_UART_SLV_MSR</a>    | 4802 8018h              |
| 1Ch    | 32     | <a href="#">ICSSM_PR1_ICSS_UART_UART_SLV_SCR</a>    | 4802 801Ch              |
| 20h    | 32     | <a href="#">ICSSM_PR1_ICSS_UART_UART_SLV_DLL</a>    | 4802 8020h              |
| 24h    | 32     | <a href="#">ICSSM_PR1_ICSS_UART_UART_SLV_DLH</a>    | 4802 8024h              |
| 28h    | 32     | <a href="#">ICSSM_PR1_ICSS_UART_UART_SLV_REVID1</a> | 4802 8028h              |

**Table 4-610. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV Registers, Base Address=4802 8000h, Length=64  
(continued)**

| Offset | Length | Register Name                                            | ICSSM0 Physical Address |
|--------|--------|----------------------------------------------------------|-------------------------|
| 30h    | 32     | <a href="#">ICSSM_PR1_ICSS_UART_UART_SLV_PWREMU_MGMT</a> | 4802 8030h              |
| 34h    | 32     | <a href="#">ICSSM_PR1_ICSS_UART_UART_SLV_MDR</a>         | 4802 8034h              |
| 0h     | 32     | <a href="#">ICSSM_PR1_ICSS_UART_UART_SLV_THR</a>         | 4802 8000h              |
| 8h     | 32     | <a href="#">ICSSM_PR1_ICSS_UART_UART_SLV_FCR</a>         | 4802 8008h              |
| 2Ch    | 32     | <a href="#">ICSSM_PR1_ICSS_UART_UART_SLV_REVID2</a>      | 4802 802Ch              |

**Table 4-611. ICSSM\_PR1\_IEP0\_SLV Registers, Base Address=4802 E000h, Length=4096**

| Offset | Length | Register Name                                        | ICSSM0 Physical Address |
|--------|--------|------------------------------------------------------|-------------------------|
| 0h     | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_GLOBAL_CFG_REG</a>    | 4802 E000h              |
| 4h     | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_GLOBAL_STATUS_REG</a> | 4802 E004h              |
| 8h     | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_COMPEN_REG</a>        | 4802 E008h              |
| Ch     | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_SLOW_COMPEN_REG</a>   | 4802 E00Ch              |
| 10h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_COUNT_REG0</a>        | 4802 E010h              |
| 14h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_COUNT_REG1</a>        | 4802 E014h              |
| 18h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAP_CFG_REG</a>       | 4802 E018h              |
| 1Ch    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAP_STATUS_REG</a>    | 4802 E01Ch              |
| 20h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR0_REG0</a>        | 4802 E020h              |
| 24h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR0_REG1</a>        | 4802 E024h              |
| 28h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR1_REG0</a>        | 4802 E028h              |
| 2Ch    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR1_REG1</a>        | 4802 E02Ch              |
| 30h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR2_REG0</a>        | 4802 E030h              |
| 34h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR2_REG1</a>        | 4802 E034h              |
| 38h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR3_REG0</a>        | 4802 E038h              |
| 3Ch    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR3_REG1</a>        | 4802 E03Ch              |
| 40h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR4_REG0</a>        | 4802 E040h              |
| 44h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR4_REG1</a>        | 4802 E044h              |
| 48h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR5_REG0</a>        | 4802 E048h              |
| 4Ch    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR5_REG1</a>        | 4802 E04Ch              |
| 50h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR6_REG0</a>        | 4802 E050h              |
| 54h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR6_REG1</a>        | 4802 E054h              |
| 58h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPF6_REG0</a>        | 4802 E058h              |
| 5Ch    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPF6_REG1</a>        | 4802 E05Ch              |
| 60h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR7_REG0</a>        | 4802 E060h              |
| 64h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR7_REG1</a>        | 4802 E064h              |
| 68h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPF7_REG0</a>        | 4802 E068h              |
| 6Ch    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPF7_REG1</a>        | 4802 E06Ch              |
| 70h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP_CFG_REG</a>       | 4802 E070h              |
| 74h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP_STATUS_REG</a>    | 4802 E074h              |
| 78h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP0_REG0</a>         | 4802 E078h              |
| 7Ch    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP0_REG1</a>         | 4802 E07Ch              |
| 80h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP1_REG0</a>         | 4802 E080h              |
| 84h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP1_REG1</a>         | 4802 E084h              |
| 88h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP2_REG0</a>         | 4802 E088h              |
| 8Ch    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP2_REG1</a>         | 4802 E08Ch              |



**Table 4-611. ICSSM\_PR1\_IEP0\_SLV Registers, Base Address=4802 E000h, Length=4096 (continued)**

| Offset | Length | Register Name                                           | ICSSM0 Physical Address |
|--------|--------|---------------------------------------------------------|-------------------------|
| 90h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP3_REG0</a>            | 4802 E090h              |
| 94h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP3_REG1</a>            | 4802 E094h              |
| 98h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP4_REG0</a>            | 4802 E098h              |
| 9Ch    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP4_REG1</a>            | 4802 E09Ch              |
| A0h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP5_REG0</a>            | 4802 E0A0h              |
| A4h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP5_REG1</a>            | 4802 E0A4h              |
| A8h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP6_REG0</a>            | 4802 E0A8h              |
| ACh    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP6_REG1</a>            | 4802 E0ACh              |
| B0h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP7_REG0</a>            | 4802 E0B0h              |
| B4h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP7_REG1</a>            | 4802 E0B4h              |
| B8h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_RXIPG0_REG</a>           | 4802 E0B8h              |
| BCh    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_RXIPG1_REG</a>           | 4802 E0BCh              |
| C0h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP8_REG0</a>            | 4802 E0C0h              |
| C4h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP8_REG1</a>            | 4802 E0C4h              |
| C8h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP9_REG0</a>            | 4802 E0C8h              |
| CCh    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP9_REG1</a>            | 4802 E0CCh              |
| D0h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP10_REG0</a>           | 4802 E0D0h              |
| D4h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP10_REG1</a>           | 4802 E0D4h              |
| D8h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP11_REG0</a>           | 4802 E0D8h              |
| DCh    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP11_REG1</a>           | 4802 E0DCh              |
| E0h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP12_REG0</a>           | 4802 E0E0h              |
| E4h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP12_REG1</a>           | 4802 E0E4h              |
| E8h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP13_REG0</a>           | 4802 E0E8h              |
| ECh    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP13_REG1</a>           | 4802 E0ECh              |
| F0h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP14_REG0</a>           | 4802 E0F0h              |
| F4h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP14_REG1</a>           | 4802 E0F4h              |
| F8h    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP15_REG0</a>           | 4802 E0F8h              |
| FCh    | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CMP15_REG1</a>           | 4802 E0FCh              |
| 100h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_COUNT_RESET_VAL_REG0</a> | 4802 E100h              |
| 104h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_COUNT_RESET_VAL_REG1</a> | 4802 E104h              |
| 108h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_PWM_REG</a>              | 4802 E108h              |
| 10Ch   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR0_BI_REG0</a>        | 4802 E10Ch              |
| 110h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR0_BI_REG1</a>        | 4802 E110h              |
| 114h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR1_BI_REG0</a>        | 4802 E114h              |
| 118h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR1_BI_REG1</a>        | 4802 E118h              |
| 11Ch   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR2_BI_REG0</a>        | 4802 E11Ch              |
| 120h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR2_BI_REG1</a>        | 4802 E120h              |
| 124h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR3_BI_REG0</a>        | 4802 E124h              |
| 128h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR3_BI_REG1</a>        | 4802 E128h              |
| 12Ch   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR4_BI_REG0</a>        | 4802 E12Ch              |
| 130h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR4_BI_REG1</a>        | 4802 E130h              |
| 134h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR5_BI_REG0</a>        | 4802 E134h              |
| 138h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR5_BI_REG1</a>        | 4802 E138h              |
| 13Ch   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR6_BI_REG0</a>        | 4802 E13Ch              |
| 140h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR6_BI_REG1</a>        | 4802 E140h              |

**Table 4-611. ICSSM\_PR1\_IEP0\_SLV Registers, Base Address=4802 E000h, Length=4096 (continued)**

| Offset | Length | Register Name                                            | ICSSM0 Physical Address |
|--------|--------|----------------------------------------------------------|-------------------------|
| 144h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPF6_BI_REG0</a>         | 4802 E144h              |
| 148h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPF6_BI_REG1</a>         | 4802 E148h              |
| 14Ch   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR7_BI_REG0</a>         | 4802 E14Ch              |
| 150h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPR7_BI_REG1</a>         | 4802 E150h              |
| 154h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPF7_BI_REG0</a>         | 4802 E154h              |
| 158h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_CAPF7_BI_REG1</a>         | 4802 E158h              |
| 180h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_SYNC_CTRL_REG</a>         | 4802 E180h              |
| 184h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_SYNC_FIRST_STAT_REG</a>   | 4802 E184h              |
| 188h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_SYNC0_STAT_REG</a>        | 4802 E188h              |
| 18Ch   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_SYNC1_STAT_REG</a>        | 4802 E18Ch              |
| 190h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_SYNC_PWIDTH_REG</a>       | 4802 E190h              |
| 194h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_SYNC0_PERIOD_REG</a>      | 4802 E194h              |
| 198h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_SYNC1_DELAY_REG</a>       | 4802 E198h              |
| 19Ch   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_SYNC_START_REG</a>        | 4802 E19Ch              |
| 200h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_WD_PREDIV_REG</a>         | 4802 E200h              |
| 204h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_PDI_WD_TIM_REG</a>        | 4802 E204h              |
| 208h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_PD_WD_TIM_REG</a>         | 4802 E208h              |
| 20Ch   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_WD_STATUS_REG</a>         | 4802 E20Ch              |
| 210h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_WD_EXP_CNT_REG</a>        | 4802 E210h              |
| 214h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_WD_CTRL_REG</a>           | 4802 E214h              |
| 300h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_DIGIO_CTRL_REG</a>        | 4802 E300h              |
| 304h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_DIGIO_STATUS_REG</a>      | 4802 E304h              |
| 308h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_DIGIO_DATA_IN_REG</a>     | 4802 E308h              |
| 30Ch   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_DIGIO_DATA_IN_RAW_REG</a> | 4802 E30Ch              |
| 310h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_DIGIO_DATA_OUT_REG</a>    | 4802 E310h              |
| 314h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_DIGIO_DATA_OUT_EN_REG</a> | 4802 E314h              |
| 318h   | 32     | <a href="#">ICSSM_PR1_IEP0_SLV_DIGIO_EXP_REG</a>         | 4802 E318h              |

**Table 4-612. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV Registers, Base Address=4803 0000h, Length=256**

| Offset | Length | Register Name                                               | ICSSM0 Physical Address |
|--------|--------|-------------------------------------------------------------|-------------------------|
| 0h     | 32     | <a href="#">ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_TSCNT</a>         | 4803 0000h              |
| 4h     | 32     | <a href="#">ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CNTPHS</a>        | 4803 0004h              |
| 8h     | 32     | <a href="#">ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CAP1</a>          | 4803 0008h              |
| Ch     | 32     | <a href="#">ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CAP2</a>          | 4803 000Ch              |
| 10h    | 32     | <a href="#">ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CAP3</a>          | 4803 0010h              |
| 14h    | 32     | <a href="#">ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_CAP4</a>          | 4803 0014h              |
| 28h    | 32     | <a href="#">ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECCTL2_ECCTL1</a> | 4803 0028h              |
| 2Ch    | 32     | <a href="#">ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECFLG_ECEINT</a>  | 4803 002Ch              |
| 30h    | 32     | <a href="#">ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECCLR</a>         | 4803 0030h              |
| 34h    | 32     | <a href="#">ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_ECFRC</a>         | 4803 0034h              |
| 5Ch    | 32     | <a href="#">ICSSM_PR1_ICSS_ECAP0_ECAP_SLV_REVID1</a>        | 4803 005Ch              |

**Table 4-613. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG Registers, Base Address=4803 2000h, Length=256**

| Offset | Length | Register Name                                      | ICSSM0 Physical Address |
|--------|--------|----------------------------------------------------|-------------------------|
| 0h     | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RXCFG0             | 4803 2000h              |
| 4h     | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RXCFG1             | 4803 2004h              |
| 10h    | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TXCFG0             | 4803 2010h              |
| 14h    | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TXCFG1             | 4803 2014h              |
| 20h    | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_CRC0            | 4803 2020h              |
| 24h    | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_CRC1            | 4803 2024h              |
| 30h    | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_IPG0            | 4803 2030h              |
| 34h    | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_IPG1            | 4803 2034h              |
| 38h    | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_PRS0               | 4803 2038h              |
| 3Ch    | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_PRS1               | 4803 203Ch              |
| 40h    | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_FRMS0           | 4803 2040h              |
| 44h    | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_FRMS1           | 4803 2044h              |
| 48h    | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_PCNT0           | 4803 2048h              |
| 4Ch    | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_PCNT1           | 4803 204Ch              |
| 50h    | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_ERR0            | 4803 2050h              |
| 54h    | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_ERR1            | 4803 2054h              |
| 60h    | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_FIFO_LEVE<br>L0 | 4803 2060h              |
| 64h    | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_RX_FIFO_LEVE<br>L1 | 4803 2064h              |
| 68h    | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_FIFO_LEVE<br>L0 | 4803 2068h              |
| 6Ch    | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_CFG_TX_FIFO_LEVE<br>L1 | 4803 206Ch              |

**Table 4-614. ICSSM\_PR1\_MDIO\_V1P7\_MDIO Registers, Base Address=4803 2400h, Length=256**

| Offset | Length | Register Name                                        | ICSSM0 Physical Address |
|--------|--------|------------------------------------------------------|-------------------------|
| 0h     | 32     | ICSSM_PR1_MDIO_V1P7_MDIO_MDIO_VERSION_REG            | 4803 2400h              |
| 4h     | 32     | ICSSM_PR1_MDIO_V1P7_MDIO_CONTROL_REG                 | 4803 2404h              |
| 8h     | 32     | ICSSM_PR1_MDIO_V1P7_MDIO_ALIVE_REG                   | 4803 2408h              |
| Ch     | 32     | ICSSM_PR1_MDIO_V1P7_MDIO_LINK_REG                    | 4803 240Ch              |
| 10h    | 32     | ICSSM_PR1_MDIO_V1P7_MDIO_LINK_INT_RAW_REG            | 4803 2410h              |
| 14h    | 32     | ICSSM_PR1_MDIO_V1P7_MDIO_LINK_INT_MASKED_R<br>EG     | 4803 2414h              |
| 18h    | 32     | ICSSM_PR1_MDIO_V1P7_MDIO_LINK_INT_MASK_SET_<br>REG   | 4803 2418h              |
| 1Ch    | 32     | ICSSM_PR1_MDIO_V1P7_MDIO_LINK_INT_MASK_CLEA<br>R_REG | 4803 241Ch              |
| 20h    | 32     | ICSSM_PR1_MDIO_V1P7_MDIO_USER_INT_RAW_REG            | 4803 2420h              |
| 24h    | 32     | ICSSM_PR1_MDIO_V1P7_MDIO_USER_INT_MASKED_R<br>EG     | 4803 2424h              |
| 28h    | 32     | ICSSM_PR1_MDIO_V1P7_MDIO_USER_INT_MASK_SET_<br>_REG  | 4803 2428h              |
| 2Ch    | 32     | ICSSM_PR1_MDIO_V1P7_MDIO_USER_INT_MASK_CLE<br>AR_REG | 4803 242Ch              |
| 30h    | 32     | ICSSM_PR1_MDIO_V1P7_MDIO_MANUAL_IF_REG               | 4803 2430h              |
| 34h    | 32     | ICSSM_PR1_MDIO_V1P7_MDIO_POLL_REG                    | 4803 2434h              |

**Table 4-614. ICSSM\_PR1\_MDIO\_V1P7\_MDIO Registers, Base Address=4803 2400h, Length=256  
(continued)**

| Offset | Length | Register Name                                          | ICSSM0 Physical Address |
|--------|--------|--------------------------------------------------------|-------------------------|
| 38h    | 32     | ICSSM_PR1_MDIO_V1P7_MDIO_POLL_EN_REG                   | 4803 2438h              |
| 3Ch    | 32     | ICSSM_PR1_MDIO_V1P7_MDIO_CLAUS45_REG                   | 4803 243Ch              |
| 40h    | 32     | ICSSM_PR1_MDIO_V1P7_MDIO_USER_ADDR0_REG                | 4803 2440h              |
| 44h    | 32     | ICSSM_PR1_MDIO_V1P7_MDIO_USER_ADDR1_REG                | 4803 2444h              |
| 80h    | 32     | ICSSM_PR1_MDIO_V1P7_MDIO_USER_GROUP_USER_ACCESS_REG_J  | 4803 2480h + formula    |
| 84h    | 32     | ICSSM_PR1_MDIO_V1P7_MDIO_USER_GROUP_USER_PHY_SEL_REG_J | 4803 2484h + formula    |

**Table 4-615. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G Registers, Base Address=4803 3000h, Length=4096**

| Offset | Length | Register Name                                         | ICSSM0 Physical Address |
|--------|--------|-------------------------------------------------------|-------------------------|
| 0h     | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_ICSS_G_CFG   | 4803 3000h              |
| 4h     | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_PREEEMPT_CFG | 4803 3004h              |
| 8h     | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_SMDT1S_CFG   | 4803 3008h              |
| Ch     | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_SMDT1C_CFG   | 4803 300Ch              |
| 10h    | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_POOL_PTR_CFG | 4803 3010h              |
| 14h    | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_TX_EARLY_EOF | 4803 3014h              |
| 18h    | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_FRAG_CNT_CFG | 4803 3018h              |
| D00h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE0       | 4803 3D00h              |
| D04h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE1       | 4803 3D04h              |
| D08h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE2       | 4803 3D08h              |
| D0Ch   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE3       | 4803 3D0Ch              |
| D10h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE4       | 4803 3D10h              |
| D14h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE5       | 4803 3D14h              |
| D18h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE6       | 4803 3D18h              |
| D1Ch   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE7       | 4803 3D1Ch              |
| D20h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE8       | 4803 3D20h              |
| D24h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE9       | 4803 3D24h              |
| D28h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE10      | 4803 3D28h              |
| D2Ch   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QUEUE11      | 4803 3D2Ch              |

**Table 4-615. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G Registers, Base Address=4803 3000h, Length=4096 (continued)**

| Offset | Length | Register Name                                                         | ICSSM0 Physical Address |
|--------|--------|-----------------------------------------------------------------------|-------------------------|
| D30h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE12</a>     | 4803 3D30h              |
| D34h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE13</a>     | 4803 3D34h              |
| D38h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE14</a>     | 4803 3D38h              |
| D3Ch   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE15</a>     | 4803 3D3Ch              |
| D40h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE16</a>     | 4803 3D40h              |
| D44h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE17</a>     | 4803 3D44h              |
| D48h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE18</a>     | 4803 3D48h              |
| D4Ch   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE19</a>     | 4803 3D4Ch              |
| D50h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE20</a>     | 4803 3D50h              |
| D54h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE21</a>     | 4803 3D54h              |
| D58h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE22</a>     | 4803 3D58h              |
| D5Ch   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE23</a>     | 4803 3D5Ch              |
| D60h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE24</a>     | 4803 3D60h              |
| D64h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE25</a>     | 4803 3D64h              |
| D68h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE26</a>     | 4803 3D68h              |
| D6Ch   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE27</a>     | 4803 3D6Ch              |
| D70h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE28</a>     | 4803 3D70h              |
| D74h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE29</a>     | 4803 3D74h              |
| D78h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE30</a>     | 4803 3D78h              |
| D7Ch   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE31</a>     | 4803 3D7Ch              |
| E00h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE_PEEK0</a> | 4803 3E00h              |
| E04h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE_PEEK1</a> | 4803 3E04h              |
| E08h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE_PEEK2</a> | 4803 3E08h              |
| E0Ch   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE_PEEK3</a> | 4803 3E0Ch              |
| E10h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE_PEEK4</a> | 4803 3E10h              |
| E14h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE_PEEK5</a> | 4803 3E14h              |

**Table 4-615. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G Registers, Base Address=4803 3000h, Length=4096 (continued)**

| Offset | Length | Register Name                                             | ICSSM0 Physical Address |
|--------|--------|-----------------------------------------------------------|-------------------------|
| E18h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU<br>EUE_PEEK6  | 4803 3E18h              |
| E1Ch   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU<br>EUE_PEEK7  | 4803 3E1Ch              |
| E20h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU<br>EUE_PEEK8  | 4803 3E20h              |
| E24h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU<br>EUE_PEEK9  | 4803 3E24h              |
| E28h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU<br>EUE_PEEK10 | 4803 3E28h              |
| E2Ch   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU<br>EUE_PEEK11 | 4803 3E2Ch              |
| E30h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU<br>EUE_PEEK12 | 4803 3E30h              |
| E34h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU<br>EUE_PEEK13 | 4803 3E34h              |
| E38h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU<br>EUE_PEEK14 | 4803 3E38h              |
| E3Ch   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU<br>EUE_PEEK15 | 4803 3E3Ch              |
| E40h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU<br>EUE_CNT0   | 4803 3E40h              |
| E44h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU<br>EUE_CNT1   | 4803 3E44h              |
| E48h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU<br>EUE_CNT2   | 4803 3E48h              |
| E4Ch   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU<br>EUE_CNT3   | 4803 3E4Ch              |
| E50h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU<br>EUE_CNT4   | 4803 3E50h              |
| E54h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU<br>EUE_CNT5   | 4803 3E54h              |
| E58h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU<br>EUE_CNT6   | 4803 3E58h              |
| E5Ch   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU<br>EUE_CNT7   | 4803 3E5Ch              |
| E60h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU<br>EUE_CNT8   | 4803 3E60h              |
| E64h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU<br>EUE_CNT9   | 4803 3E64h              |
| E68h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU<br>EUE_CNT10  | 4803 3E68h              |
| E6Ch   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU<br>EUE_CNT11  | 4803 3E6Ch              |
| E70h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU<br>EUE_CNT12  | 4803 3E70h              |
| E74h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU<br>EUE_CNT13  | 4803 3E74h              |
| E78h   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU<br>EUE_CNT14  | 4803 3E78h              |
| E7Ch   | 32     | ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU<br>EUE_CNT15  | 4803 3E7Ch              |

**Table 4-615. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G Registers, Base Address=4803 3000h, Length=4096 (continued)**

| Offset | Length | Register Name                                                         | ICSSM0 Physical Address |
|--------|--------|-----------------------------------------------------------------------|-------------------------|
| E80h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE_CNT16</a> | 4803 3E80h              |
| E84h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE_CNT17</a> | 4803 3E84h              |
| E88h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE_CNT18</a> | 4803 3E88h              |
| E8Ch   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE_CNT19</a> | 4803 3E8Ch              |
| E90h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE_CNT20</a> | 4803 3E90h              |
| E94h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE_CNT21</a> | 4803 3E94h              |
| E98h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE_CNT22</a> | 4803 3E98h              |
| E9Ch   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE_CNT23</a> | 4803 3E9Ch              |
| EA0h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE_CNT24</a> | 4803 3EA0h              |
| EA4h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE_CNT25</a> | 4803 3EA4h              |
| EA8h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE_CNT26</a> | 4803 3EA8h              |
| EACH   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE_CNT27</a> | 4803 3EACH              |
| EB0h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE_CNT28</a> | 4803 3EB0h              |
| EB4h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE_CNT29</a> | 4803 3EB4h              |
| EB8h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE_CNT30</a> | 4803 3EB8h              |
| EBCh   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE_CNT31</a> | 4803 3EBCh              |
| F40h   | 32     | <a href="#">ICSSM_PR1_MII_RT_PR1_MII_RT_G_CFG_REGS_G_QU_EUE_RESET</a> | 4803 3F40h              |

**Table 4-616. ECC\_AGGR Registers, Base Address=4810 0000h, Length=1024**

| Offset | Length | Register Name                                | ICSSM0 Physical Address |
|--------|--------|----------------------------------------------|-------------------------|
| 0h     | 32     | <a href="#">ECC_AGGR_REV</a>                 | 4810 0000h              |
| 8h     | 32     | <a href="#">ECC_AGGR_VECTOR</a>              | 4810 0008h              |
| Ch     | 32     | <a href="#">ECC_AGGR_STAT</a>                | 4810 000Ch              |
| 10h    | 32     | <a href="#">ECC_AGGR_RESERVED_SVBUS_J</a>    | 4810 0010h + formula    |
| 3Ch    | 32     | <a href="#">ECC_AGGR_SEC_EOI_REG</a>         | 4810 003Ch              |
| 40h    | 32     | <a href="#">ECC_AGGR_SEC_STATUS_REG0</a>     | 4810 0040h              |
| 80h    | 32     | <a href="#">ECC_AGGR_SEC_ENABLE_SET_REG0</a> | 4810 0080h              |
| C0h    | 32     | <a href="#">ECC_AGGR_SEC_ENABLE_CLR_REG0</a> | 4810 00C0h              |
| 13Ch   | 32     | <a href="#">ECC_AGGR_DED_EOI_REG</a>         | 4810 013Ch              |
| 140h   | 32     | <a href="#">ECC_AGGR_DED_STATUS_REG0</a>     | 4810 0140h              |
| 180h   | 32     | <a href="#">ECC_AGGR_DED_ENABLE_SET_REG0</a> | 4810 0180h              |
| 1C0h   | 32     | <a href="#">ECC_AGGR_DED_ENABLE_CLR_REG0</a> | 4810 01C0h              |

**Table 4-616. ECC\_AGGR Registers, Base Address=4810 0000h, Length=1024 (continued)**

| Offset | Length | Register Name                            | ICSSM0 Physical Address |
|--------|--------|------------------------------------------|-------------------------|
| 200h   | 32     | <a href="#">ECC_AGGR_AGGR_ENABLE_SET</a> | 4810 0200h              |
| 204h   | 32     | <a href="#">ECC_AGGR_AGGR_ENABLE_CLR</a> | 4810 0204h              |
| 208h   | 32     | <a href="#">ECC_AGGR_AGGR_STATUS_SET</a> | 4810 0208h              |
| 20Ch   | 32     | <a href="#">ECC_AGGR_AGGR_STATUS_CLR</a> | 4810 020Ch              |

## 4.2.2 ICSSM Registers

### ICSSM Registers



#### 4.2.2.1 ICSSM\_DRAM0\_SLV\_RAM\_RAM\_REG\_j Register

##### 1 ICSSM\_DRAM0\_SLV\_RAM\_RAM\_REG\_j Register (Offset = 0h + formula) [reset = 0h]

The RAM memory words provide memory mapped random access data storage.

Return to [Summary Table](#)

Offset = (j \* 4h); where j = 0 to 2047d

**Table 4-617. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ICSSM0        | 4800 0000h + formula |

**Figure 4-195. ICSSM\_DRAM0\_SLV\_RAM\_RAM\_REG\_j Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BYTE3 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BYTE2 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| BYTE1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| BYTE0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-619. ICSSM\_DRAM0\_SLV\_RAM\_RAM\_REG\_j Register Field Descriptions**

| Bit   | Field | Type | Reset | Description         |
|-------|-------|------|-------|---------------------|
| 31:24 | BYTE3 | R/W  | 0h    | This is the MS byte |
| 23:16 | BYTE2 | R/W  | 0h    | This is the UM byte |
| 15:8  | BYTE1 | R/W  | 0h    | This is the LM byte |
| 7:0   | BYTE0 | R/W  | 0h    | This is the LS byte |

#### 4.2.2.2 ICSSM\_DRAM1\_SLV\_RAM\_RAM\_REG\_j Register

##### 1 ICSSM\_DRAM1\_SLV\_RAM\_RAM\_REG\_j Register (Offset = 0h + formula) [reset = 0h]

The RAM memory words provide memory mapped random access data storage.

Return to [Summary Table](#)

Offset = (j \* 4h); where j = 0 to 2047d

**Table 4-620. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ICSSM0        | 4800 2000h + formula |

**Figure 4-196. ICSSM\_DRAM1\_SLV\_RAM\_RAM\_REG\_j Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BYTE3 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BYTE2 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| BYTE1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| BYTE0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-622. ICSSM\_DRAM1\_SLV\_RAM\_RAM\_REG\_j Register Field Descriptions**

| Bit   | Field | Type | Reset | Description         |
|-------|-------|------|-------|---------------------|
| 31:24 | BYTE3 | R/W  | 0h    | This is the MS byte |
| 23:16 | BYTE2 | R/W  | 0h    | This is the UM byte |
| 15:8  | BYTE1 | R/W  | 0h    | This is the LM byte |
| 7:0   | BYTE0 | R/W  | 0h    | This is the LS byte |

#### 4.2.2.3 RAT\_PID Register

##### 1 RAT\_PID Register (Offset = 0h) [reset = 66803100h]

The Revision Register contains the major and minor revisions for the module.

Return to [Summary Table](#)

**Table 4-623. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 9000h       |

**Figure 4-197. RAT\_PID Name Register**

|        |    |       |    |      |       |    |    |
|--------|----|-------|----|------|-------|----|----|
| 31     | 30 | 29    | 28 | 27   | 26    | 25 | 24 |
| SCHEME |    | BU    |    | FUNC |       |    |    |
| R      |    | R     |    | R    |       |    |    |
| 1h     |    | 2h    |    | 680h |       |    |    |
| 23     | 22 | 21    | 20 | 19   | 18    | 17 | 16 |
| FUNC   |    |       |    |      |       |    |    |
| R      |    |       |    |      |       |    |    |
| 680h   |    |       |    |      |       |    |    |
| 15     | 14 | 13    | 12 | 11   | 10    | 9  | 8  |
| RTL    |    |       |    |      | MAJOR |    |    |
| R      |    |       |    |      | R     |    |    |
| 6h     |    |       |    |      | 1h    |    |    |
| 7      | 6  | 5     | 4  | 3    | 2     | 1  | 0  |
| CUSTOM |    | MINOR |    |      |       |    |    |
| R      |    | R     |    |      |       |    |    |
| 0h     |    | 0h    |    |      |       |    |    |

**Table 4-625. RAT\_PID Register Field Descriptions**

| Bit   | Field  | Type | Reset | Description                                   |
|-------|--------|------|-------|-----------------------------------------------|
| 31:30 | SCHEME | R    | 1h    | PID register scheme                           |
| 29:28 | BU     | R    | 2h    | Business Unit: 10 = Processors                |
| 27:16 | FUNC   | R    | 680h  | Module ID                                     |
| 15:11 | RTL    | R    | 6h    | RTL revision. Will vary depending on release. |
| 10:8  | MAJOR  | R    | 1h    | Major revision                                |
| 7:6   | CUSTOM | R    | 0h    | Custom                                        |
| 5:0   | MINOR  | R    | 0h    | Minor revision                                |

#### 4.2.2.4 RAT\_CONFIG Register

##### 1 RAT\_CONFIG Register (Offset = 4h) [reset = 240106h]

The Config Register contains the configuration values for the module.

Return to [Summary Table](#)

**Table 4-626. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 9004h       |

**Figure 4-198. RAT\_CONFIG Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ADDR_WIDTH |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 24h        |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ADDRS      |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 1h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| REGIONS    |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 6h         |    |    |    |    |    |    |    |

**Table 4-628. RAT\_CONFIG Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description            |
|-------|------------|------|-------|------------------------|
| 31:24 | RESERVED   | NONE | 0h    | Reserved               |
| 23:16 | ADDR_WIDTH | R    | 24h   | Number of address bits |
| 15:8  | ADDRS      | R    | 1h    | Number of addresses    |
| 7:0   | REGIONS    | R    | 6h    | Number of regions      |

#### 4.2.2.5 RAT\_DESTINATION\_ID Register

##### 1 RAT\_DESTINATION\_ID Register (Offset = 804h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

Return to [Summary Table](#)

**Table 4-629. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 9804h       |

**Figure 4-199. RAT\_DESTINATION\_ID Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DEST_ID  |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-631. RAT\_DESTINATION\_ID Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description         |
|------|----------|------|-------|---------------------|
| 31:8 | RESERVED | NONE | 0h    | Reserved            |
| 7:0  | DEST_ID  | R/W  | 0h    | The destination ID. |

#### 4.2.2.6 RAT\_EXCEPTION\_LOGGING\_CONTROL Register

##### 1 RAT\_EXCEPTION\_LOGGING\_CONTROL Register (Offset = 820h) [reset = 0h]

The Exception Logging Control Register controls the exception logging.

Return to [Summary Table](#)

**Table 4-632. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 9820h       |

**Figure 4-200. RAT\_EXCEPTION\_LOGGING\_CONTROL Name Register**

|          |    |    |    |    |    |              |           |
|----------|----|----|----|----|----|--------------|-----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25           | 24        |
| RESERVED |    |    |    |    |    |              |           |
| NONE     |    |    |    |    |    |              |           |
| 0h       |    |    |    |    |    |              |           |
| 23       | 22 | 21 | 20 | 19 | 18 | 17           | 16        |
| RESERVED |    |    |    |    |    |              |           |
| NONE     |    |    |    |    |    |              |           |
| 0h       |    |    |    |    |    |              |           |
| 15       | 14 | 13 | 12 | 11 | 10 | 9            | 8         |
| RESERVED |    |    |    |    |    |              |           |
| NONE     |    |    |    |    |    |              |           |
| 0h       |    |    |    |    |    |              |           |
| 7        | 6  | 5  | 4  | 3  | 2  | 1            | 0         |
| RESERVED |    |    |    |    |    | DISABLE_INTR | DISABLE_F |
| NONE     |    |    |    |    |    | R/W          | R/W       |
| 0h       |    |    |    |    |    | 0h           | 0h        |

**Table 4-634. RAT\_EXCEPTION\_LOGGING\_CONTROL Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                          |
|------|--------------|------|-------|--------------------------------------|
| 31:2 | RESERVED     | NONE | 0h    | Reserved                             |
| 1    | DISABLE_INTR | R/W  | 0h    | Disables logging interrupt when set. |
| 0    | DISABLE_F    | R/W  | 0h    | Disables logging when set.           |

#### 4.2.2.7 RAT\_EXCEPTION\_LOGGING\_HEADER0 Register

##### 1 RAT\_EXCEPTION\_LOGGING\_HEADER0 Register (Offset = 824h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

Return to [Summary Table](#)

**Table 4-635. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 9824h       |

**Figure 4-201. RAT\_EXCEPTION\_LOGGING\_HEADER0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TYPE_F  |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SRC_ID  |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SRC_ID  |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DEST_ID |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-637. RAT\_EXCEPTION\_LOGGING\_HEADER0 Register Field Descriptions**

| Bit   | Field   | Type | Reset | Description     |
|-------|---------|------|-------|-----------------|
| 31:24 | TYPE_F  | R    | 0h    | Type. 4 = RAT.  |
| 23:8  | SRC_ID  | R    | 0h    | Source ID.      |
| 7:0   | DEST_ID | R    | 0h    | Destination ID. |

#### 4.2.2.8 RAT\_EXCEPTION\_LOGGING\_HEADER1 Register

##### 1 RAT\_EXCEPTION\_LOGGING\_HEADER1 Register (Offset = 828h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

Return to [Summary Table](#)

**Table 4-638. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 9828h       |

**Figure 4-202. RAT\_EXCEPTION\_LOGGING\_HEADER1 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| GROUP    |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CODE     |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-640. RAT\_EXCEPTION\_LOGGING\_HEADER1 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                        |
|-------|----------|------|-------|------------------------------------|
| 31:24 | GROUP    | R    | 0h    | Group.                             |
| 23:16 | CODE     | R    | 0h    | Code. 1 = Boundary crossing error. |
| 15:0  | RESERVED | NONE | 0h    | Reserved                           |



#### 4.2.2.9 RAT\_EXCEPTION\_LOGGING\_DATA0 Register

##### 1 RAT\_EXCEPTION\_LOGGING\_DATA0 Register (Offset = 82Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

Return to [Summary Table](#)

**Table 4-641. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 982Ch       |

**Figure 4-203. RAT\_EXCEPTION\_LOGGING\_DATA0 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ADDR_L |    |    |    |    |    |    |    |
| R      |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ADDR_L |    |    |    |    |    |    |    |
| R      |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ADDR_L |    |    |    |    |    |    |    |
| R      |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ADDR_L |    |    |    |    |    |    |    |
| R      |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 4-643. RAT\_EXCEPTION\_LOGGING\_DATA0 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description            |
|------|--------|------|-------|------------------------|
| 31:0 | ADDR_L | R    | 0h    | Address lower 32 bits. |

#### 4.2.2.10 RAT\_EXCEPTION\_LOGGING\_DATA1 Register

##### 1 RAT\_EXCEPTION\_LOGGING\_DATA1 Register (Offset = 830h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

Return to [Summary Table](#)

**Table 4-644. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 9830h       |

**Figure 4-204. RAT\_EXCEPTION\_LOGGING\_DATA1 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ADDR_H   |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ADDR_H   |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-646. RAT\_EXCEPTION\_LOGGING\_DATA1 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description            |
|-------|----------|------|-------|------------------------|
| 31:16 | RESERVED | NONE | 0h    | Reserved               |
| 15:0  | ADDR_H   | R    | 0h    | Address upper 12 bits. |

#### 4.2.2.11 RAT\_EXCEPTION\_LOGGING\_DATA2 Register

##### 1 RAT\_EXCEPTION\_LOGGING\_DATA2 Register (Offset = 834h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

Return to [Summary Table](#)

**Table 4-647. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 9834h       |

**Figure 4-205. RAT\_EXCEPTION\_LOGGING\_DATA2 Name Register**

|          |    |       |      |         |           |      |        |
|----------|----|-------|------|---------|-----------|------|--------|
| 31       | 30 | 29    | 28   | 27      | 26        | 25   | 24     |
| RESERVED |    |       |      | ROUTEID |           |      |        |
| NONE     |    |       |      | R       |           |      |        |
| 0h       |    |       |      | 0h      |           |      |        |
| 23       | 22 | 21    | 20   | 19      | 18        | 17   | 16     |
| ROUTEID  |    |       |      |         |           |      |        |
| R        |    |       |      |         |           |      |        |
| 0h       |    |       |      |         |           |      |        |
| 15       | 14 | 13    | 12   | 11      | 10        | 9    | 8      |
| RESERVED |    | WRITE | READ | DEBUG   | CACHEABLE | PRIV | SECURE |
| NONE     |    | R     | R    | R       | R         | R    | R      |
| 0h       |    | 0h    | 0h   | 0h      | 0h        | 0h   | 0h     |
| 7        | 6  | 5     | 4    | 3       | 2         | 1    | 0      |
| PRIV_ID  |    |       |      |         |           |      |        |
| R        |    |       |      |         |           |      |        |
| 0h       |    |       |      |         |           |      |        |

**Table 4-649. RAT\_EXCEPTION\_LOGGING\_DATA2 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description |
|-------|-----------|------|-------|-------------|
| 31:28 | RESERVED  | NONE | 0h    | Reserved    |
| 27:16 | ROUTEID   | R    | 0h    | Route ID.   |
| 15:14 | RESERVED  | NONE | 0h    | Reserved    |
| 13    | WRITE     | R    | 0h    | Write.      |
| 12    | READ      | R    | 0h    | Read.       |
| 11    | DEBUG     | R    | 0h    | Debug.      |
| 10    | CACHEABLE | R    | 0h    | Cacheable.  |
| 9     | PRIV      | R    | 0h    | Priv.       |
| 8     | SECURE    | R    | 0h    | Secure.     |
| 7:0   | PRIV_ID   | R    | 0h    | Priv ID.    |

#### 4.2.2.12 RAT\_EXCEPTION\_LOGGING\_DATA3 Register

##### 1 RAT\_EXCEPTION\_LOGGING\_DATA3 Register (Offset = 838h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data. Reading this register will clear the error pending bit.

Return to [Summary Table](#)

**Table 4-650. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 9838h       |

**Figure 4-206. RAT\_EXCEPTION\_LOGGING\_DATA3 Name Register**

|          |    |    |    |    |    |         |    |
|----------|----|----|----|----|----|---------|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25      | 24 |
| RESERVED |    |    |    |    |    |         |    |
| NONE     |    |    |    |    |    |         |    |
| 0h       |    |    |    |    |    |         |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17      | 16 |
| RESERVED |    |    |    |    |    |         |    |
| NONE     |    |    |    |    |    |         |    |
| 0h       |    |    |    |    |    |         |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9       | 8  |
| RESERVED |    |    |    |    |    | BYTECNT |    |
| NONE     |    |    |    |    |    | R       |    |
| 0h       |    |    |    |    |    | 0h      |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1       | 0  |
| BYTECNT  |    |    |    |    |    |         |    |
| R        |    |    |    |    |    |         |    |
| 0h       |    |    |    |    |    |         |    |

**Table 4-652. RAT\_EXCEPTION\_LOGGING\_DATA3 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:10 | RESERVED | NONE | 0h    | Reserved    |
| 9:0   | BYTECNT  | R    | 0h    | Byte count. |

#### 4.2.2.13 RAT\_EXCEPTION\_PEND\_SET Register

##### 1 RAT\_EXCEPTION\_PEND\_SET Register (Offset = 840h) [reset = 0h]

The Exception Logging Interrupt Pending Set Register allows to set the pend signal.

Return to [Summary Table](#)

**Table 4-653. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 9840h       |

**Figure 4-207. RAT\_EXCEPTION\_PEND\_SET Name Register**

|          |    |    |    |    |    |    |          |
|----------|----|----|----|----|----|----|----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24       |
| RESERVED |    |    |    |    |    |    |          |
| NONE     |    |    |    |    |    |    |          |
| 0h       |    |    |    |    |    |    |          |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16       |
| RESERVED |    |    |    |    |    |    |          |
| NONE     |    |    |    |    |    |    |          |
| 0h       |    |    |    |    |    |    |          |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8        |
| RESERVED |    |    |    |    |    |    |          |
| NONE     |    |    |    |    |    |    |          |
| 0h       |    |    |    |    |    |    |          |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0        |
| RESERVED |    |    |    |    |    |    | PEND_SET |
| NONE     |    |    |    |    |    |    | R/W1TS   |
| 0h       |    |    |    |    |    |    | 0h       |

**Table 4-655. RAT\_EXCEPTION\_PEND\_SET Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description                                 |
|------|----------|--------|-------|---------------------------------------------|
| 31:1 | RESERVED | NONE   | 0h    | Reserved                                    |
| 0    | PEND_SET | R/W1TS | 0h    | Write a 1 to set the exception pend signal. |

#### 4.2.2.14 RAT\_EXCEPTION\_PEND\_CLEAR Register

##### 1 RAT\_EXCEPTION\_PEND\_CLEAR Register (Offset = 844h) [reset = 0h]

The Exception Logging Interrupt Pending Clear Register allows to clear the pend signal.

Return to [Summary Table](#)

**Table 4-656. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 9844h       |

**Figure 4-208. RAT\_EXCEPTION\_PEND\_CLEAR Name Register**

|          |    |    |    |    |    |    |          |
|----------|----|----|----|----|----|----|----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24       |
| RESERVED |    |    |    |    |    |    |          |
| NONE     |    |    |    |    |    |    |          |
| 0h       |    |    |    |    |    |    |          |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16       |
| RESERVED |    |    |    |    |    |    |          |
| NONE     |    |    |    |    |    |    |          |
| 0h       |    |    |    |    |    |    |          |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8        |
| RESERVED |    |    |    |    |    |    |          |
| NONE     |    |    |    |    |    |    |          |
| 0h       |    |    |    |    |    |    |          |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0        |
| RESERVED |    |    |    |    |    |    | PEND_CLR |
| NONE     |    |    |    |    |    |    | R/W1TC   |
| 0h       |    |    |    |    |    |    | 0h       |

**Table 4-658. RAT\_EXCEPTION\_PEND\_CLEAR Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description                                   |
|------|----------|--------|-------|-----------------------------------------------|
| 31:1 | RESERVED | NONE   | 0h    | Reserved                                      |
| 0    | PEND_CLR | R/W1TC | 0h    | Write a 1 to clear the exception pend signal. |

#### 4.2.2.15 RAT\_EXCEPTION\_ENABLE\_SET Register

##### 1 RAT\_EXCEPTION\_ENABLE\_SET Register (Offset = 848h) [reset = 0h]

The Exception Logging Interrupt Enable Set Register allows to set the interrupt enable signal.

Return to [Summary Table](#)

**Table 4-659. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 9848h       |

**Figure 4-209. RAT\_EXCEPTION\_ENABLE\_SET Name Register**

|          |    |    |    |    |    |    |            |
|----------|----|----|----|----|----|----|------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24         |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16         |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8          |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0          |
| RESERVED |    |    |    |    |    |    | ENABLE_SET |
| NONE     |    |    |    |    |    |    | R/W1TS     |
| 0h       |    |    |    |    |    |    | 0h         |

**Table 4-661. RAT\_EXCEPTION\_ENABLE\_SET Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                             |
|------|------------|--------|-------|---------------------------------------------------------|
| 31:1 | RESERVED   | NONE   | 0h    | Reserved                                                |
| 0    | ENABLE_SET | R/W1TS | 0h    | Write a 1 to set the exception interrupt enable signal. |

#### 4.2.2.16 RAT\_EXCEPTION\_ENABLE\_CLEAR Register

##### 1 RAT\_EXCEPTION\_ENABLE\_CLEAR Register (Offset = 84Ch) [reset = 0h]

The Exception Logging Interrupt Enable Clear Register allows to clear the interrupt enable signal.

Return to [Summary Table](#)

**Table 4-662. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 984Ch       |

**Figure 4-210. RAT\_EXCEPTION\_ENABLE\_CLEAR Name Register**

|          |    |    |    |    |    |    |            |
|----------|----|----|----|----|----|----|------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24         |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16         |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8          |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0          |
| RESERVED |    |    |    |    |    |    | ENABLE_CLR |
| NONE     |    |    |    |    |    |    | R/W1TC     |
| 0h       |    |    |    |    |    |    | 0h         |

**Table 4-664. RAT\_EXCEPTION\_ENABLE\_CLEAR Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                               |
|------|------------|--------|-------|-----------------------------------------------------------|
| 31:1 | RESERVED   | NONE   | 0h    | Reserved                                                  |
| 0    | ENABLE_CLR | R/W1TC | 0h    | Write a 1 to clear the exception interrupt enable signal. |



#### 4.2.2.17 RAT\_EOI\_REG Register

##### 1 RAT\_EOI\_REG Register (Offset = 850h) [reset = 0h]

EOI Register.

Return to [Summary Table](#)

**Table 4-665. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 9850h       |

**Figure 4-211. RAT\_EOI\_REG Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| EOI_WR   |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| EOI_WR   |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-667. RAT\_EOI\_REG Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description  |
|-------|----------|------|-------|--------------|
| 31:16 | RESERVED | NONE | 0h    | Reserved     |
| 15:0  | EOI_WR   | R/W  | 0h    | EOI Register |

#### 4.2.2.18 RAT\_REGION\_CTRL\_J Register

##### 1 RAT\_REGION\_CTRL\_J Register (Offset = 20h) [reset = 0h]

The Control for Region a

Return to [Summary Table](#)

Offset = Base + (j \* 10h); where j = 0 to 5d

**Table 4-668. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ICSSM0        | 4800 9020h + formula |

**Figure 4-212. RAT\_REGION\_CTRL\_J Name Register**

|          |          |      |    |    |    |    |    |
|----------|----------|------|----|----|----|----|----|
| 31       | 30       | 29   | 28 | 27 | 26 | 25 | 24 |
| EN       | RESERVED |      |    |    |    |    |    |
| R/W      | NONE     |      |    |    |    |    |    |
| 0h       | 0h       |      |    |    |    |    |    |
| 23       | 22       | 21   | 20 | 19 | 18 | 17 | 16 |
| RESERVED |          |      |    |    |    |    |    |
| NONE     |          |      |    |    |    |    |    |
| 0h       |          |      |    |    |    |    |    |
| 15       | 14       | 13   | 12 | 11 | 10 | 9  | 8  |
| RESERVED |          |      |    |    |    |    |    |
| NONE     |          |      |    |    |    |    |    |
| 0h       |          |      |    |    |    |    |    |
| 7        | 6        | 5    | 4  | 3  | 2  | 1  | 0  |
| RESERVED |          | SIZE |    |    |    |    |    |
| NONE     |          | R/W  |    |    |    |    |    |
| 0h       |          | 0h   |    |    |    |    |    |

**Table 4-670. RAT\_REGION\_CTRL\_J Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                  |
|------|----------|------|-------|----------------------------------------------------------------------------------------------|
| 31   | EN       | R/W  | 0h    | Enable for the Region                                                                        |
| 30:6 | RESERVED | NONE | 0h    | Reserved                                                                                     |
| 5:0  | SIZE     | R/W  | 0h    | Size of the Region in Address Bits. 0 = 1 byte, 1 = 2B, 2 = 4B, 3 = 8B, etc. up to 32 = 4GB. |

#### 4.2.2.19 RAT\_REGION\_BASE\_J Register

##### 1 RAT\_REGION\_BASE\_J Register (Offset = 24h) [reset = 0h]

The Base Address for Region a. This is the source address for matching to a region.

Return to [Summary Table](#)

Offset = Base + (j \* 10h); where j = 0 to 5d

**Table 4-671. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ICSSM0        | 4800 9024h + formula |

**Figure 4-213. RAT\_REGION\_BASE\_J Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BASE |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BASE |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| BASE |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| BASE |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 4-673. RAT\_REGION\_BASE\_J Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                             |
|------|-------|------|-------|-------------------------------------------------------------------------|
| 31:0 | BASE  | R/W  | 0h    | Base Address for the Region. It must be aligned to the programmed size. |

#### 4.2.2.20 RAT\_REGION\_TRANS\_L\_J Register

##### 1 RAT\_REGION\_TRANS\_L\_J Register (Offset = 28h) [reset = 0h]

The Translated Lower Address Bits for Region a

Return to [Summary Table](#)

Offset = Base + (j \* 10h); where j = 0 to 5d

**Table 4-674. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ICSSM0        | 4800 9028h + formula |

**Figure 4-214. RAT\_REGION\_TRANS\_L\_J Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| LOWER |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LOWER |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| LOWER |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LOWER |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-676. RAT\_REGION\_TRANS\_L\_J Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                              |
|------|-------|------|-------|------------------------------------------------------------------------------------------|
| 31:0 | LOWER | R/W  | 0h    | Translated Lower Address Bits for the Region. It must be aligned to the programmed size. |

#### 4.2.2.21 RAT\_REGION\_TRANS\_U\_J Register

##### 1 RAT\_REGION\_TRANS\_U\_J Register (Offset = 2Ch) [reset = 0h]

The Translated Upper Address Bits for Region a

Return to [Summary Table](#)

Offset = Base + (j \* 10h); where j = 0 to 5d

**Table 4-677. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ICSSM0        | 4800 902Ch + formula |

**Figure 4-215. RAT\_REGION\_TRANS\_U\_J Name Register**

|          |    |    |    |       |    |    |    |
|----------|----|----|----|-------|----|----|----|
| 31       | 30 | 29 | 28 | 27    | 26 | 25 | 24 |
| RESERVED |    |    |    |       |    |    |    |
| NONE     |    |    |    |       |    |    |    |
| 0h       |    |    |    |       |    |    |    |
| 23       | 22 | 21 | 20 | 19    | 18 | 17 | 16 |
| RESERVED |    |    |    |       |    |    |    |
| NONE     |    |    |    |       |    |    |    |
| 0h       |    |    |    |       |    |    |    |
| 15       | 14 | 13 | 12 | 11    | 10 | 9  | 8  |
| RESERVED |    |    |    |       |    |    |    |
| NONE     |    |    |    |       |    |    |    |
| 0h       |    |    |    |       |    |    |    |
| 7        | 6  | 5  | 4  | 3     | 2  | 1  | 0  |
| RESERVED |    |    |    | UPPER |    |    |    |
| NONE     |    |    |    | R/W   |    |    |    |
| 0h       |    |    |    | 0h    |    |    |    |

**Table 4-679. RAT\_REGION\_TRANS\_U\_J Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                  |
|------|----------|------|-------|----------------------------------------------|
| 31:4 | RESERVED | NONE | 0h    | Reserved                                     |
| 3:0  | UPPER    | R/W  | 0h    | Translated Upper Address Bits for the Region |

#### 4.2.2.22 RAT\_PID Register

##### 1 RAT\_PID Register (Offset = 0h) [reset = 66803100h]

The Revision Register contains the major and minor revisions for the module.

Return to [Summary Table](#)

**Table 4-680. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 9000h       |

**Figure 4-216. RAT\_PID Name Register**

|        |    |       |    |      |       |    |    |
|--------|----|-------|----|------|-------|----|----|
| 31     | 30 | 29    | 28 | 27   | 26    | 25 | 24 |
| SCHEME |    | BU    |    | FUNC |       |    |    |
| R      |    | R     |    | R    |       |    |    |
| 1h     |    | 2h    |    | 680h |       |    |    |
| 23     | 22 | 21    | 20 | 19   | 18    | 17 | 16 |
| FUNC   |    |       |    |      |       |    |    |
| R      |    |       |    |      |       |    |    |
| 680h   |    |       |    |      |       |    |    |
| 15     | 14 | 13    | 12 | 11   | 10    | 9  | 8  |
| RTL    |    |       |    |      | MAJOR |    |    |
| R      |    |       |    |      | R     |    |    |
| 6h     |    |       |    |      | 1h    |    |    |
| 7      | 6  | 5     | 4  | 3    | 2     | 1  | 0  |
| CUSTOM |    | MINOR |    |      |       |    |    |
| R      |    | R     |    |      |       |    |    |
| 0h     |    | 0h    |    |      |       |    |    |

**Table 4-682. RAT\_PID Register Field Descriptions**

| Bit   | Field  | Type | Reset | Description                                   |
|-------|--------|------|-------|-----------------------------------------------|
| 31:30 | SCHEME | R    | 1h    | PID register scheme                           |
| 29:28 | BU     | R    | 2h    | Business Unit: 10 = Processors                |
| 27:16 | FUNC   | R    | 680h  | Module ID                                     |
| 15:11 | RTL    | R    | 6h    | RTL revision. Will vary depending on release. |
| 10:8  | MAJOR  | R    | 1h    | Major revision                                |
| 7:6   | CUSTOM | R    | 0h    | Custom                                        |
| 5:0   | MINOR  | R    | 0h    | Minor revision                                |

#### 4.2.2.23 RAT\_CONFIG Register

##### 1 RAT\_CONFIG Register (Offset = 4h) [reset = 240106h]

The Config Register contains the configuration values for the module.

Return to [Summary Table](#)

**Table 4-683. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 9004h       |

**Figure 4-217. RAT\_CONFIG Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ADDR_WIDTH |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 24h        |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ADDRS      |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 1h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| REGIONS    |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 6h         |    |    |    |    |    |    |    |

**Table 4-685. RAT\_CONFIG Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description            |
|-------|------------|------|-------|------------------------|
| 31:24 | RESERVED   | NONE | 0h    | Reserved               |
| 23:16 | ADDR_WIDTH | R    | 24h   | Number of address bits |
| 15:8  | ADDRS      | R    | 1h    | Number of addresses    |
| 7:0   | REGIONS    | R    | 6h    | Number of regions      |

#### 4.2.2.24 RAT\_DESTINATION\_ID Register

##### 1 RAT\_DESTINATION\_ID Register (Offset = 804h) [reset = 0h]

The Destination ID Register defines the destination ID value for error messages.

Return to [Summary Table](#)

**Table 4-686. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 9804h       |

**Figure 4-218. RAT\_DESTINATION\_ID Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DEST_ID  |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-688. RAT\_DESTINATION\_ID Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description         |
|------|----------|------|-------|---------------------|
| 31:8 | RESERVED | NONE | 0h    | Reserved            |
| 7:0  | DEST_ID  | R/W  | 0h    | The destination ID. |



#### 4.2.2.25 RAT\_EXCEPTION\_LOGGING\_CONTROL Register

##### 1 RAT\_EXCEPTION\_LOGGING\_CONTROL Register (Offset = 820h) [reset = 0h]

The Exception Logging Control Register controls the exception logging.

Return to [Summary Table](#)

**Table 4-689. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 9820h       |

**Figure 4-219. RAT\_EXCEPTION\_LOGGING\_CONTROL Name Register**

|          |    |    |    |    |    |              |           |
|----------|----|----|----|----|----|--------------|-----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25           | 24        |
| RESERVED |    |    |    |    |    |              |           |
| NONE     |    |    |    |    |    |              |           |
| 0h       |    |    |    |    |    |              |           |
| 23       | 22 | 21 | 20 | 19 | 18 | 17           | 16        |
| RESERVED |    |    |    |    |    |              |           |
| NONE     |    |    |    |    |    |              |           |
| 0h       |    |    |    |    |    |              |           |
| 15       | 14 | 13 | 12 | 11 | 10 | 9            | 8         |
| RESERVED |    |    |    |    |    |              |           |
| NONE     |    |    |    |    |    |              |           |
| 0h       |    |    |    |    |    |              |           |
| 7        | 6  | 5  | 4  | 3  | 2  | 1            | 0         |
| RESERVED |    |    |    |    |    | DISABLE_INTR | DISABLE_F |
| NONE     |    |    |    |    |    | R/W          | R/W       |
| 0h       |    |    |    |    |    | 0h           | 0h        |

**Table 4-691. RAT\_EXCEPTION\_LOGGING\_CONTROL Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                          |
|------|--------------|------|-------|--------------------------------------|
| 31:2 | RESERVED     | NONE | 0h    | Reserved                             |
| 1    | DISABLE_INTR | R/W  | 0h    | Disables logging interrupt when set. |
| 0    | DISABLE_F    | R/W  | 0h    | Disables logging when set.           |

#### 4.2.2.26 RAT\_EXCEPTION\_LOGGING\_HEADER0 Register

##### 1 RAT\_EXCEPTION\_LOGGING\_HEADER0 Register (Offset = 824h) [reset = 0h]

The Exception Logging Header 0 Register contains the first word of the header.

Return to [Summary Table](#)

**Table 4-692. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 9824h       |

**Figure 4-220. RAT\_EXCEPTION\_LOGGING\_HEADER0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TYPE_F  |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SRC_ID  |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SRC_ID  |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DEST_ID |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-694. RAT\_EXCEPTION\_LOGGING\_HEADER0 Register Field Descriptions**

| Bit   | Field   | Type | Reset | Description     |
|-------|---------|------|-------|-----------------|
| 31:24 | TYPE_F  | R    | 0h    | Type. 4 = RAT.  |
| 23:8  | SRC_ID  | R    | 0h    | Source ID.      |
| 7:0   | DEST_ID | R    | 0h    | Destination ID. |

#### 4.2.2.27 RAT\_EXCEPTION\_LOGGING\_HEADER1 Register

##### 1 RAT\_EXCEPTION\_LOGGING\_HEADER1 Register (Offset = 828h) [reset = 0h]

The Exception Logging Header 1 Register contains the second word of the header.

Return to [Summary Table](#)

**Table 4-695. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 9828h       |

**Figure 4-221. RAT\_EXCEPTION\_LOGGING\_HEADER1 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| GROUP    |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CODE     |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-697. RAT\_EXCEPTION\_LOGGING\_HEADER1 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                        |
|-------|----------|------|-------|------------------------------------|
| 31:24 | GROUP    | R    | 0h    | Group.                             |
| 23:16 | CODE     | R    | 0h    | Code. 1 = Boundary crossing error. |
| 15:0  | RESERVED | NONE | 0h    | Reserved                           |

#### 4.2.2.28 RAT\_EXCEPTION\_LOGGING\_DATA0 Register

##### 1 RAT\_EXCEPTION\_LOGGING\_DATA0 Register (Offset = 82Ch) [reset = 0h]

The Exception Logging Data 0 Register contains the first word of the data.

Return to [Summary Table](#)

**Table 4-698. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 982Ch       |

**Figure 4-222. RAT\_EXCEPTION\_LOGGING\_DATA0 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ADDR_L |    |    |    |    |    |    |    |
| R      |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ADDR_L |    |    |    |    |    |    |    |
| R      |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ADDR_L |    |    |    |    |    |    |    |
| R      |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ADDR_L |    |    |    |    |    |    |    |
| R      |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 4-700. RAT\_EXCEPTION\_LOGGING\_DATA0 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description            |
|------|--------|------|-------|------------------------|
| 31:0 | ADDR_L | R    | 0h    | Address lower 32 bits. |

#### 4.2.2.29 RAT\_EXCEPTION\_LOGGING\_DATA1 Register

##### 1 RAT\_EXCEPTION\_LOGGING\_DATA1 Register (Offset = 830h) [reset = 0h]

The Exception Logging Data 1 Register contains the second word of the data.

Return to [Summary Table](#)

**Table 4-701. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 9830h       |

**Figure 4-223. RAT\_EXCEPTION\_LOGGING\_DATA1 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ADDR_H   |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ADDR_H   |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-703. RAT\_EXCEPTION\_LOGGING\_DATA1 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description            |
|-------|----------|------|-------|------------------------|
| 31:16 | RESERVED | NONE | 0h    | Reserved               |
| 15:0  | ADDR_H   | R    | 0h    | Address upper 12 bits. |

#### 4.2.2.30 RAT\_EXCEPTION\_LOGGING\_DATA2 Register

##### 1 RAT\_EXCEPTION\_LOGGING\_DATA2 Register (Offset = 834h) [reset = 0h]

The Exception Logging Data 2 Register contains the third word of the data.

Return to [Summary Table](#)

**Table 4-704. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 9834h       |

**Figure 4-224. RAT\_EXCEPTION\_LOGGING\_DATA2 Name Register**

|          |    |       |      |         |           |      |        |
|----------|----|-------|------|---------|-----------|------|--------|
| 31       | 30 | 29    | 28   | 27      | 26        | 25   | 24     |
| RESERVED |    |       |      | ROUTEID |           |      |        |
| NONE     |    |       |      | R       |           |      |        |
| 0h       |    |       |      | 0h      |           |      |        |
| 23       | 22 | 21    | 20   | 19      | 18        | 17   | 16     |
| ROUTEID  |    |       |      |         |           |      |        |
| R        |    |       |      |         |           |      |        |
| 0h       |    |       |      |         |           |      |        |
| 15       | 14 | 13    | 12   | 11      | 10        | 9    | 8      |
| RESERVED |    | WRITE | READ | DEBUG   | CACHEABLE | PRIV | SECURE |
| NONE     |    | R     | R    | R       | R         | R    | R      |
| 0h       |    | 0h    | 0h   | 0h      | 0h        | 0h   | 0h     |
| 7        | 6  | 5     | 4    | 3       | 2         | 1    | 0      |
| PRIV_ID  |    |       |      |         |           |      |        |
| R        |    |       |      |         |           |      |        |
| 0h       |    |       |      |         |           |      |        |

**Table 4-706. RAT\_EXCEPTION\_LOGGING\_DATA2 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description |
|-------|-----------|------|-------|-------------|
| 31:28 | RESERVED  | NONE | 0h    | Reserved    |
| 27:16 | ROUTEID   | R    | 0h    | Route ID.   |
| 15:14 | RESERVED  | NONE | 0h    | Reserved    |
| 13    | WRITE     | R    | 0h    | Write.      |
| 12    | READ      | R    | 0h    | Read.       |
| 11    | DEBUG     | R    | 0h    | Debug.      |
| 10    | CACHEABLE | R    | 0h    | Cacheable.  |
| 9     | PRIV      | R    | 0h    | Priv.       |
| 8     | SECURE    | R    | 0h    | Secure.     |
| 7:0   | PRIV_ID   | R    | 0h    | Priv ID.    |

#### 4.2.2.31 RAT\_EXCEPTION\_LOGGING\_DATA3 Register

##### 1 RAT\_EXCEPTION\_LOGGING\_DATA3 Register (Offset = 838h) [reset = 0h]

The Exception Logging Data 3 Register contains the fourth word of the data. Reading this register will clear the error pending bit.

Return to [Summary Table](#)

**Table 4-707. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 9838h       |

**Figure 4-225. RAT\_EXCEPTION\_LOGGING\_DATA3 Name Register**

|          |    |    |    |    |    |         |    |
|----------|----|----|----|----|----|---------|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25      | 24 |
| RESERVED |    |    |    |    |    |         |    |
| NONE     |    |    |    |    |    |         |    |
| 0h       |    |    |    |    |    |         |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17      | 16 |
| RESERVED |    |    |    |    |    |         |    |
| NONE     |    |    |    |    |    |         |    |
| 0h       |    |    |    |    |    |         |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9       | 8  |
| RESERVED |    |    |    |    |    | BYTECNT |    |
| NONE     |    |    |    |    |    | R       |    |
| 0h       |    |    |    |    |    | 0h      |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1       | 0  |
| BYTECNT  |    |    |    |    |    |         |    |
| R        |    |    |    |    |    |         |    |
| 0h       |    |    |    |    |    |         |    |

**Table 4-709. RAT\_EXCEPTION\_LOGGING\_DATA3 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:10 | RESERVED | NONE | 0h    | Reserved    |
| 9:0   | BYTECNT  | R    | 0h    | Byte count. |

#### 4.2.2.32 RAT\_EXCEPTION\_PEND\_SET Register

##### 1 RAT\_EXCEPTION\_PEND\_SET Register (Offset = 840h) [reset = 0h]

The Exception Logging Interrupt Pending Set Register allows to set the pend signal.

Return to [Summary Table](#)

**Table 4-710. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 9840h       |

**Figure 4-226. RAT\_EXCEPTION\_PEND\_SET Name Register**

|          |    |    |    |    |    |    |          |
|----------|----|----|----|----|----|----|----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24       |
| RESERVED |    |    |    |    |    |    |          |
| NONE     |    |    |    |    |    |    |          |
| 0h       |    |    |    |    |    |    |          |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16       |
| RESERVED |    |    |    |    |    |    |          |
| NONE     |    |    |    |    |    |    |          |
| 0h       |    |    |    |    |    |    |          |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8        |
| RESERVED |    |    |    |    |    |    |          |
| NONE     |    |    |    |    |    |    |          |
| 0h       |    |    |    |    |    |    |          |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0        |
| RESERVED |    |    |    |    |    |    | PEND_SET |
| NONE     |    |    |    |    |    |    | R/W1TS   |
| 0h       |    |    |    |    |    |    | 0h       |

**Table 4-712. RAT\_EXCEPTION\_PEND\_SET Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description                                 |
|------|----------|--------|-------|---------------------------------------------|
| 31:1 | RESERVED | NONE   | 0h    | Reserved                                    |
| 0    | PEND_SET | R/W1TS | 0h    | Write a 1 to set the exception pend signal. |



#### 4.2.2.33 RAT\_EXCEPTION\_PEND\_CLEAR Register

##### 1 RAT\_EXCEPTION\_PEND\_CLEAR Register (Offset = 844h) [reset = 0h]

The Exception Logging Interrupt Pending Clear Register allows to clear the pend signal.

Return to [Summary Table](#)

**Table 4-713. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 9844h       |

**Figure 4-227. RAT\_EXCEPTION\_PEND\_CLEAR Name Register**

|          |    |    |    |    |    |    |          |
|----------|----|----|----|----|----|----|----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24       |
| RESERVED |    |    |    |    |    |    |          |
| NONE     |    |    |    |    |    |    |          |
| 0h       |    |    |    |    |    |    |          |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16       |
| RESERVED |    |    |    |    |    |    |          |
| NONE     |    |    |    |    |    |    |          |
| 0h       |    |    |    |    |    |    |          |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8        |
| RESERVED |    |    |    |    |    |    |          |
| NONE     |    |    |    |    |    |    |          |
| 0h       |    |    |    |    |    |    |          |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0        |
| RESERVED |    |    |    |    |    |    | PEND_CLR |
| NONE     |    |    |    |    |    |    | R/W1TC   |
| 0h       |    |    |    |    |    |    | 0h       |

**Table 4-715. RAT\_EXCEPTION\_PEND\_CLEAR Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description                                   |
|------|----------|--------|-------|-----------------------------------------------|
| 31:1 | RESERVED | NONE   | 0h    | Reserved                                      |
| 0    | PEND_CLR | R/W1TC | 0h    | Write a 1 to clear the exception pend signal. |

#### 4.2.2.34 RAT\_EXCEPTION\_ENABLE\_SET Register

##### 1 RAT\_EXCEPTION\_ENABLE\_SET Register (Offset = 848h) [reset = 0h]

The Exception Logging Interrupt Enable Set Register allows to set the interrupt enable signal.

Return to [Summary Table](#)

**Table 4-716. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 9848h       |

**Figure 4-228. RAT\_EXCEPTION\_ENABLE\_SET Name Register**

|          |    |    |    |    |    |    |            |
|----------|----|----|----|----|----|----|------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24         |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16         |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8          |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0          |
| RESERVED |    |    |    |    |    |    | ENABLE_SET |
| NONE     |    |    |    |    |    |    | R/W1TS     |
| 0h       |    |    |    |    |    |    | 0h         |

**Table 4-718. RAT\_EXCEPTION\_ENABLE\_SET Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                             |
|------|------------|--------|-------|---------------------------------------------------------|
| 31:1 | RESERVED   | NONE   | 0h    | Reserved                                                |
| 0    | ENABLE_SET | R/W1TS | 0h    | Write a 1 to set the exception interrupt enable signal. |

#### 4.2.2.35 RAT\_EXCEPTION\_ENABLE\_CLEAR Register

##### 1 RAT\_EXCEPTION\_ENABLE\_CLEAR Register (Offset = 84Ch) [reset = 0h]

The Exception Logging Interrupt Enable Clear Register allows to clear the interrupt enable signal.

Return to [Summary Table](#)

**Table 4-719. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 984Ch       |

**Figure 4-229. RAT\_EXCEPTION\_ENABLE\_CLEAR Name Register**

|          |    |    |    |    |    |    |            |
|----------|----|----|----|----|----|----|------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24         |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16         |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8          |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0          |
| RESERVED |    |    |    |    |    |    | ENABLE_CLR |
| NONE     |    |    |    |    |    |    | R/W1TC     |
| 0h       |    |    |    |    |    |    | 0h         |

**Table 4-721. RAT\_EXCEPTION\_ENABLE\_CLEAR Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                                               |
|------|------------|--------|-------|-----------------------------------------------------------|
| 31:1 | RESERVED   | NONE   | 0h    | Reserved                                                  |
| 0    | ENABLE_CLR | R/W1TC | 0h    | Write a 1 to clear the exception interrupt enable signal. |

#### 4.2.2.36 RAT\_EOI\_REG Register

##### 1 RAT\_EOI\_REG Register (Offset = 850h) [reset = 0h]

EOI Register.

Return to [Summary Table](#)

**Table 4-722. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4800 9850h       |

**Figure 4-230. RAT\_EOI\_REG Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| EOI_WR   |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| EOI_WR   |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-724. RAT\_EOI\_REG Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description  |
|-------|----------|------|-------|--------------|
| 31:16 | RESERVED | NONE | 0h    | Reserved     |
| 15:0  | EOI_WR   | R/W  | 0h    | EOI Register |

#### 4.2.2.37 RAT\_REGION\_CTRL\_J Register

##### 1 RAT\_REGION\_CTRL\_J Register (Offset = 20h) [reset = 0h]

The Control for Region a

Return to [Summary Table](#)

Offset = Base + (j \* 10h); where j = 0 to 5d

**Table 4-725. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ICSSM0        | 4800 9020h + formula |

**Figure 4-231. RAT\_REGION\_CTRL\_J Name Register**

|          |          |      |    |    |    |    |    |
|----------|----------|------|----|----|----|----|----|
| 31       | 30       | 29   | 28 | 27 | 26 | 25 | 24 |
| EN       | RESERVED |      |    |    |    |    |    |
| R/W      | NONE     |      |    |    |    |    |    |
| 0h       | 0h       |      |    |    |    |    |    |
| 23       | 22       | 21   | 20 | 19 | 18 | 17 | 16 |
| RESERVED |          |      |    |    |    |    |    |
| NONE     |          |      |    |    |    |    |    |
| 0h       |          |      |    |    |    |    |    |
| 15       | 14       | 13   | 12 | 11 | 10 | 9  | 8  |
| RESERVED |          |      |    |    |    |    |    |
| NONE     |          |      |    |    |    |    |    |
| 0h       |          |      |    |    |    |    |    |
| 7        | 6        | 5    | 4  | 3  | 2  | 1  | 0  |
| RESERVED |          | SIZE |    |    |    |    |    |
| NONE     |          | R/W  |    |    |    |    |    |
| 0h       |          | 0h   |    |    |    |    |    |

**Table 4-727. RAT\_REGION\_CTRL\_J Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                  |
|------|----------|------|-------|----------------------------------------------------------------------------------------------|
| 31   | EN       | R/W  | 0h    | Enable for the Region                                                                        |
| 30:6 | RESERVED | NONE | 0h    | Reserved                                                                                     |
| 5:0  | SIZE     | R/W  | 0h    | Size of the Region in Address Bits. 0 = 1 byte, 1 = 2B, 2 = 4B, 3 = 8B, etc. up to 32 = 4GB. |

#### 4.2.2.38 RAT\_REGION\_BASE\_J Register

##### 1 RAT\_REGION\_BASE\_J Register (Offset = 24h) [reset = 0h]

The Base Address for Region a. This is the source address for matching to a region.

Return to [Summary Table](#)

Offset = Base + (j \* 10h); where j = 0 to 5d

**Table 4-728. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ICSSM0        | 4800 9024h + formula |

**Figure 4-232. RAT\_REGION\_BASE\_J Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BASE |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BASE |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| BASE |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| BASE |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 4-730. RAT\_REGION\_BASE\_J Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                             |
|------|-------|------|-------|-------------------------------------------------------------------------|
| 31:0 | BASE  | R/W  | 0h    | Base Address for the Region. It must be aligned to the programmed size. |

#### 4.2.2.39 RAT\_REGION\_TRANS\_L\_J Register

##### 1 RAT\_REGION\_TRANS\_L\_J Register (Offset = 28h) [reset = 0h]

The Translated Lower Address Bits for Region a

Return to [Summary Table](#)

Offset = Base + (j \* 10h); where j = 0 to 5d

**Table 4-731. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ICSSM0        | 4800 9028h + formula |

**Figure 4-233. RAT\_REGION\_TRANS\_L\_J Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| LOWER |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LOWER |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| LOWER |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LOWER |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-733. RAT\_REGION\_TRANS\_L\_J Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                              |
|------|-------|------|-------|------------------------------------------------------------------------------------------|
| 31:0 | LOWER | R/W  | 0h    | Translated Lower Address Bits for the Region. It must be aligned to the programmed size. |

#### 4.2.2.40 RAT\_REGION\_TRANS\_U\_J Register

##### 1 RAT\_REGION\_TRANS\_U\_J Register (Offset = 2Ch) [reset = 0h]

The Translated Upper Address Bits for Region a

Return to [Summary Table](#)

Offset = Base + (j \* 10h); where j = 0 to 5d

**Table 4-734. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ICSSM0        | 4800 902Ch + formula |

**Figure 4-234. RAT\_REGION\_TRANS\_U\_J Name Register**

|          |    |    |    |       |    |    |    |
|----------|----|----|----|-------|----|----|----|
| 31       | 30 | 29 | 28 | 27    | 26 | 25 | 24 |
| RESERVED |    |    |    |       |    |    |    |
| NONE     |    |    |    |       |    |    |    |
| 0h       |    |    |    |       |    |    |    |
| 23       | 22 | 21 | 20 | 19    | 18 | 17 | 16 |
| RESERVED |    |    |    |       |    |    |    |
| NONE     |    |    |    |       |    |    |    |
| 0h       |    |    |    |       |    |    |    |
| 15       | 14 | 13 | 12 | 11    | 10 | 9  | 8  |
| RESERVED |    |    |    |       |    |    |    |
| NONE     |    |    |    |       |    |    |    |
| 0h       |    |    |    |       |    |    |    |
| 7        | 6  | 5  | 4  | 3     | 2  | 1  | 0  |
| RESERVED |    |    |    | UPPER |    |    |    |
| NONE     |    |    |    | R/W   |    |    |    |
| 0h       |    |    |    | 0h    |    |    |    |

**Table 4-736. RAT\_REGION\_TRANS\_U\_J Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                  |
|------|----------|------|-------|----------------------------------------------|
| 31:4 | RESERVED | NONE | 0h    | Reserved                                     |
| 3:0  | UPPER    | R/W  | 0h    | Translated Upper Address Bits for the Region |



#### 4.2.2.41 ICSSM\_RAM\_SLV\_RAM\_RAM\_REG\_j Register

##### 1 ICSSM\_RAM\_SLV\_RAM\_RAM\_REG\_j Register (Offset = 0h + formula) [reset = 0h]

The RAM memory words provide memory mapped random access data storage.

Return to [Summary Table](#)

Offset = (j \* 4h); where j = 0 to 8191d

**Table 4-737. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ICSSM0        | 4801 0000h + formula |

**Figure 4-235. ICSSM\_RAM\_SLV\_RAM\_RAM\_REG\_j Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BYTE3 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BYTE2 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| BYTE1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| BYTE0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-739. ICSSM\_RAM\_SLV\_RAM\_RAM\_REG\_j Register Field Descriptions**

| Bit   | Field | Type | Reset | Description         |
|-------|-------|------|-------|---------------------|
| 31:24 | BYTE3 | R/W  | 0h    | This is the MS byte |
| 23:16 | BYTE2 | R/W  | 0h    | This is the UM byte |
| 15:8  | BYTE1 | R/W  | 0h    | This is the LM byte |
| 7:0   | BYTE0 | R/W  | 0h    | This is the LS byte |

#### 4.2.2.42 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_REVISION\_REG Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_REVISION\_REG Register (Offset = 0h) [reset = 4E82A900h]

Revision Register

Return to [Summary Table](#)

**Table 4-740. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0000h       |

**Figure 4-236. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_REVISION\_REG Name Register**

|            |    |           |    |            |           |    |    |
|------------|----|-----------|----|------------|-----------|----|----|
| 31         | 30 | 29        | 28 | 27         | 26        | 25 | 24 |
| REV_SCHEME |    | RESERVED  |    | REV_MODULE |           |    |    |
| R          |    | NONE      |    | R          |           |    |    |
| 1h         |    | 0h        |    | E82h       |           |    |    |
| 23         | 22 | 21        | 20 | 19         | 18        | 17 | 16 |
| REV_MODULE |    |           |    |            |           |    |    |
| R          |    |           |    |            |           |    |    |
| E82h       |    |           |    |            |           |    |    |
| 15         | 14 | 13        | 12 | 11         | 10        | 9  | 8  |
| REV_RTL    |    |           |    |            | REV_MAJOR |    |    |
| R          |    |           |    |            | R         |    |    |
| 15h        |    |           |    |            | 1h        |    |    |
| 7          | 6  | 5         | 4  | 3          | 2         | 1  | 0  |
| REV_CUSTOM |    | REV_MINOR |    |            |           |    |    |
| R          |    | R         |    |            |           |    |    |
| 0h         |    | 0h        |    |            |           |    |    |

**Table 4-742. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_REVISION\_REG Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description     |
|-------|------------|------|-------|-----------------|
| 31:30 | REV_SCHEME | R    | 1h    | Scheme          |
| 29:28 | RESERVED   | NONE | 0h    | Reserved        |
| 27:16 | REV_MODULE | R    | E82h  | Module ID       |
| 15:11 | REV_RTL    | R    | 15h   | RTL revisions   |
| 10:8  | REV_MAJOR  | R    | 1h    | Major revision  |
| 7:6   | REV_CUSTOM | R    | 0h    | Custom revision |
| 5:0   | REV_MINOR  | R    | 0h    | Minor revision  |

#### 4.2.2.43 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CONTROL\_REG Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CONTROL\_REG Register (Offset = 4h) [reset = 0h]

Control Register

Return to [Summary Table](#)

**Table 4-743. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0004h       |

**Figure 4-237. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CONTROL\_REG Name Register**

|          |    |    |                    |           |    |             |          |
|----------|----|----|--------------------|-----------|----|-------------|----------|
| 31       | 30 | 29 | 28                 | 27        | 26 | 25          | 24       |
| RESERVED |    |    |                    |           |    |             |          |
| NONE     |    |    |                    |           |    |             |          |
| 0h       |    |    |                    |           |    |             |          |
| 23       | 22 | 21 | 20                 | 19        | 18 | 17          | 16       |
| RESERVED |    |    |                    |           |    |             |          |
| NONE     |    |    |                    |           |    |             |          |
| 0h       |    |    |                    |           |    |             |          |
| 15       | 14 | 13 | 12                 | 11        | 10 | 9           | 8        |
| RESERVED |    |    |                    |           |    |             |          |
| NONE     |    |    |                    |           |    |             |          |
| 0h       |    |    |                    |           |    |             |          |
| 7        | 6  | 5  | 4                  | 3         | 2  | 1           | 0        |
| RESERVED |    |    | PRIORITY_HOLD_MODE | NEST_MODE |    | WAKEUP_MODE | RESERVED |
| NONE     |    |    | R/W                | R/W       |    | R/W         | NONE     |
| 0h       |    |    | 0h                 | 0h        |    | 0h          | 0h       |

**Table 4-745. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CONTROL\_REG Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description           |
|------|--------------------|------|-------|-----------------------|
| 31:5 | RESERVED           | NONE | 0h    | Reserved              |
| 4    | PRIORITY_HOLD_MODE | R/W  | 0h    | Priority Holding Mode |
| 3:2  | NEST_MODE          | R/W  | 0h    | Nesting Mode          |
| 1    | WAKEUP_MODE        | R/W  | 0h    | Wakeup mode enable    |
| 0    | RESERVED           | NONE | 0h    | Reserved              |

#### 4.2.2.44 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_GLOBAL\_ENABLE\_HINT\_REG Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_GLOBAL\_ENABLE\_HINT\_REG Register (Offset = 10h) [reset = 0h]

Global Host Int Enable Register

Return to [Summary Table](#)

**Table 4-746. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0010h       |

**Figure 4-238. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_GLOBAL\_ENABLE\_HINT\_REG Name Register**

|          |    |    |    |    |    |    |                 |
|----------|----|----|----|----|----|----|-----------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24              |
| RESERVED |    |    |    |    |    |    |                 |
| NONE     |    |    |    |    |    |    |                 |
| 0h       |    |    |    |    |    |    |                 |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16              |
| RESERVED |    |    |    |    |    |    |                 |
| NONE     |    |    |    |    |    |    |                 |
| 0h       |    |    |    |    |    |    |                 |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8               |
| RESERVED |    |    |    |    |    |    |                 |
| NONE     |    |    |    |    |    |    |                 |
| 0h       |    |    |    |    |    |    |                 |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0               |
| RESERVED |    |    |    |    |    |    | ENABLE_HINT_ANY |
| NONE     |    |    |    |    |    |    | R/W             |
| 0h       |    |    |    |    |    |    | 0h              |

**Table 4-748. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_GLOBAL\_ENABLE\_HINT\_REG Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                     |
|------|-----------------|------|-------|---------------------------------|
| 31:1 | RESERVED        | NONE | 0h    | Reserved                        |
| 0    | ENABLE_HINT_ANY | R/W  | 0h    | Global Enable for all Host Ints |

#### 4.2.2.45 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_GLB\_NEST\_LEVEL\_REG Register

#### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_GLB\_NEST\_LEVEL\_REG Register (Offset = 1Ch) [reset = 100h]

Global Nesting Level Register

Return to [Summary Table](#)

**Table 4-749. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 001Ch       |

**Figure 4-239. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_GLB\_NEST\_LEVEL\_REG Name Register**

|                   |          |    |    |    |    |    |                |
|-------------------|----------|----|----|----|----|----|----------------|
| 31                | 30       | 29 | 28 | 27 | 26 | 25 | 24             |
| GLB_NEST_AUTO_OVR | RESERVED |    |    |    |    |    |                |
| W                 | NONE     |    |    |    |    |    |                |
| X                 | 0h       |    |    |    |    |    |                |
| 23                | 22       | 21 | 20 | 19 | 18 | 17 | 16             |
| RESERVED          |          |    |    |    |    |    |                |
| NONE              |          |    |    |    |    |    |                |
| 0h                |          |    |    |    |    |    |                |
| 15                | 14       | 13 | 12 | 11 | 10 | 9  | 8              |
| RESERVED          |          |    |    |    |    |    | GLB_NEST_LEVEL |
| NONE              |          |    |    |    |    |    | R/W            |
| 0h                |          |    |    |    |    |    | 100h           |
| 7                 | 6        | 5  | 4  | 3  | 2  | 1  | 0              |
| GLB_NEST_LEVEL    |          |    |    |    |    |    |                |
| R/W               |          |    |    |    |    |    |                |
| 100h              |          |    |    |    |    |    |                |

**Table 4-751. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_GLB\_NEST\_LEVEL\_REG Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                             |
|------|-------------------|------|-------|-----------------------------------------|
| 31   | GLB_NEST_AUTO_OVR | W    | X     | Global Nesting Level Override Automatic |
| 30:9 | RESERVED          | NONE | 0h    | Reserved                                |
| 8:0  | GLB_NEST_LEVEL    | R/W  | 100h  | Global Nesting Level                    |

#### 4.2.2.46 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_STATUS\_SET\_INDEX\_REG Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_STATUS\_SET\_INDEX\_REG Register (Offset = 20h) [reset = 0h]

Status Set Index Register

Return to [Summary Table](#)

**Table 4-752. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0020h       |

**Figure 4-240. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_STATUS\_SET\_INDEX\_REG Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | STATUS_SET_INDEX |    |
| NONE             |    |    |    |    |    | W                |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| STATUS_SET_INDEX |    |    |    |    |    |                  |    |
| W                |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 4-754. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_STATUS\_SET\_INDEX\_REG Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                              |
|-------|------------------|------|-------|----------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                 |
| 9:0   | STATUS_SET_INDEX | W    | 0h    | Status Set Index Register (write index to set status of) |

#### 4.2.2.47 ICSSM\_PR1\_ICSS\_INTc\_INTc\_SLV\_STATUS\_CLR\_INDEX\_REG Register

##### 1 ICSSM\_PR1\_ICSS\_INTc\_INTc\_SLV\_STATUS\_CLR\_INDEX\_REG Register (Offset = 24h) [reset = 0h]

Status Clear Index Register

Return to [Summary Table](#)

**Table 4-755. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0024h       |

**Figure 4-241. ICSSM\_PR1\_ICSS\_INTc\_INTc\_SLV\_STATUS\_CLR\_INDEX\_REG Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | STATUS_CLR_INDEX |    |
| NONE             |    |    |    |    |    | W                |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| STATUS_CLR_INDEX |    |    |    |    |    |                  |    |
| W                |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 4-757. ICSSM\_PR1\_ICSS\_INTc\_INTc\_SLV\_STATUS\_CLR\_INDEX\_REG Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                  |
|-------|------------------|------|-------|--------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                     |
| 9:0   | STATUS_CLR_INDEX | W    | 0h    | Status Clear Index Register (write index to clear status of) |

#### 4.2.2.48 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENABLE\_SET\_INDEX\_REG Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENABLE\_SET\_INDEX\_REG Register (Offset = 28h) [reset = 0h]

Enable Set Index Register

Return to [Summary Table](#)

**Table 4-758. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0028h       |

**Figure 4-242. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENABLE\_SET\_INDEX\_REG Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | ENABLE_SET_INDEX |    |
| NONE             |    |    |    |    |    | W1TS             |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| ENABLE_SET_INDEX |    |    |    |    |    |                  |    |
| W1TS             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 4-760. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENABLE\_SET\_INDEX\_REG Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                              |
|-------|------------------|------|-------|----------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                 |
| 9:0   | ENABLE_SET_INDEX | W1TS | 0h    | Enable Set Index Register (write index to set enable of) |



#### 4.2.2.49 ICSSM\_PR1\_ICSS\_INTX\_INTX\_SLV\_ENABLE\_CLR\_INDEX\_REG Register

##### 1 ICSSM\_PR1\_ICSS\_INTX\_INTX\_SLV\_ENABLE\_CLR\_INDEX\_REG Register (Offset = 2Ch) [reset = 0h]

Enable Clear Index Register

Return to [Summary Table](#)

**Table 4-761. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 002Ch       |

**Figure 4-243. ICSSM\_PR1\_ICSS\_INTX\_INTX\_SLV\_ENABLE\_CLR\_INDEX\_REG Name Register**

|                  |    |    |    |    |    |                  |    |
|------------------|----|----|----|----|----|------------------|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25               | 24 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17               | 16 |
| RESERVED         |    |    |    |    |    |                  |    |
| NONE             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9                | 8  |
| RESERVED         |    |    |    |    |    | ENABLE_CLR_INDEX |    |
| NONE             |    |    |    |    |    | W1TC             |    |
| 0h               |    |    |    |    |    | 0h               |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1                | 0  |
| ENABLE_CLR_INDEX |    |    |    |    |    |                  |    |
| W1TC             |    |    |    |    |    |                  |    |
| 0h               |    |    |    |    |    |                  |    |

**Table 4-763. ICSSM\_PR1\_ICSS\_INTX\_INTX\_SLV\_ENABLE\_CLR\_INDEX\_REG Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                  |
|-------|------------------|------|-------|--------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                     |
| 9:0   | ENABLE_CLR_INDEX | W1TC | 0h    | Enable Clear Index Register (write index to clear enable of) |

#### 4.2.2.50 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_HINT\_ENABLE\_SET\_INDEX\_REG Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_HINT\_ENABLE\_SET\_INDEX\_REG Register (Offset = 34h) [reset = 0h]

Host Int Enable Set Index Register

Return to [Summary Table](#)
**Table 4-764. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0034h       |

**Figure 4-244. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_HINT\_ENABLE\_SET\_INDEX\_REG Name Register**

|                       |    |    |    |    |    |                       |    |
|-----------------------|----|----|----|----|----|-----------------------|----|
| 31                    | 30 | 29 | 28 | 27 | 26 | 25                    | 24 |
| RESERVED              |    |    |    |    |    |                       |    |
| NONE                  |    |    |    |    |    |                       |    |
| 0h                    |    |    |    |    |    |                       |    |
| 23                    | 22 | 21 | 20 | 19 | 18 | 17                    | 16 |
| RESERVED              |    |    |    |    |    |                       |    |
| NONE                  |    |    |    |    |    |                       |    |
| 0h                    |    |    |    |    |    |                       |    |
| 15                    | 14 | 13 | 12 | 11 | 10 | 9                     | 8  |
| RESERVED              |    |    |    |    |    | HINT_ENABLE_SET_INDEX |    |
| NONE                  |    |    |    |    |    | W1TS                  |    |
| 0h                    |    |    |    |    |    | 0h                    |    |
| 7                     | 6  | 5  | 4  | 3  | 2  | 1                     | 0  |
| HINT_ENABLE_SET_INDEX |    |    |    |    |    |                       |    |
| W1TS                  |    |    |    |    |    |                       |    |
| 0h                    |    |    |    |    |    |                       |    |

**Table 4-766. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_HINT\_ENABLE\_SET\_INDEX\_REG Register Field Descriptions**

| Bit   | Field                 | Type | Reset | Description                    |
|-------|-----------------------|------|-------|--------------------------------|
| 31:10 | RESERVED              | NONE | 0h    | Reserved                       |
| 9:0   | HINT_ENABLE_SET_INDEX | W1TS | 0h    | Enable set for Host Interrupts |

#### 4.2.2.51 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_HINT\_ENABLE\_CLR\_INDEX\_REG Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_HINT\_ENABLE\_CLR\_INDEX\_REG Register (Offset = 38h) [reset = 0h]

Host Int Enable Clear Index Register

Return to [Summary Table](#)

**Table 4-767. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0038h       |

**Figure 4-245. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_HINT\_ENABLE\_CLR\_INDEX\_REG Name Register**

|                       |    |    |    |    |    |                       |    |
|-----------------------|----|----|----|----|----|-----------------------|----|
| 31                    | 30 | 29 | 28 | 27 | 26 | 25                    | 24 |
| RESERVED              |    |    |    |    |    |                       |    |
| NONE                  |    |    |    |    |    |                       |    |
| 0h                    |    |    |    |    |    |                       |    |
| 23                    | 22 | 21 | 20 | 19 | 18 | 17                    | 16 |
| RESERVED              |    |    |    |    |    |                       |    |
| NONE                  |    |    |    |    |    |                       |    |
| 0h                    |    |    |    |    |    |                       |    |
| 15                    | 14 | 13 | 12 | 11 | 10 | 9                     | 8  |
| RESERVED              |    |    |    |    |    | HINT_ENABLE_CLR_INDEX |    |
| NONE                  |    |    |    |    |    | W1TC                  |    |
| 0h                    |    |    |    |    |    | 0h                    |    |
| 7                     | 6  | 5  | 4  | 3  | 2  | 1                     | 0  |
| HINT_ENABLE_CLR_INDEX |    |    |    |    |    |                       |    |
| W1TC                  |    |    |    |    |    |                       |    |
| 0h                    |    |    |    |    |    |                       |    |

**Table 4-769. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_HINT\_ENABLE\_CLR\_INDEX\_REG Register Field Descriptions**

| Bit   | Field                 | Type | Reset | Description                      |
|-------|-----------------------|------|-------|----------------------------------|
| 31:10 | RESERVED              | NONE | 0h    | Reserved                         |
| 9:0   | HINT_ENABLE_CLR_INDEX | W1TC | 0h    | Enable clear for Host Interrupts |

#### 4.2.2.52 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_GLB\_PRI\_INTR\_REG Register

#### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_GLB\_PRI\_INTR\_REG Register (Offset = 80h) [reset = 80000000h]

Global Prioritized Interrupt Register

Return to [Summary Table](#)

**Table 4-770. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0080h       |

**Figure 4-246. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_GLB\_PRI\_INTR\_REG Name Register**

|              |          |    |    |    |    |              |    |
|--------------|----------|----|----|----|----|--------------|----|
| 31           | 30       | 29 | 28 | 27 | 26 | 25           | 24 |
| GLB_NONE     | RESERVED |    |    |    |    |              |    |
| R            | NONE     |    |    |    |    |              |    |
| 1h           | 0h       |    |    |    |    |              |    |
| 23           | 22       | 21 | 20 | 19 | 18 | 17           | 16 |
| RESERVED     |          |    |    |    |    |              |    |
| NONE         |          |    |    |    |    |              |    |
| 0h           |          |    |    |    |    |              |    |
| 15           | 14       | 13 | 12 | 11 | 10 | 9            | 8  |
| RESERVED     |          |    |    |    |    | GLB_PRI_INTR |    |
| NONE         |          |    |    |    |    | R            |    |
| 0h           |          |    |    |    |    | 0h           |    |
| 7            | 6        | 5  | 4  | 3  | 2  | 1            | 0  |
| GLB_PRI_INTR |          |    |    |    |    |              |    |
| R            |          |    |    |    |    |              |    |
| 0h           |          |    |    |    |    |              |    |

**Table 4-772. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_GLB\_PRI\_INTR\_REG Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description               |
|-------|--------------|------|-------|---------------------------|
| 31    | GLB_NONE     | R    | 1h    | No interrupt pending flag |
| 30:10 | RESERVED     | NONE | 0h    | Reserved                  |
| 9:0   | GLB_PRI_INTR | R    | 0h    | Prioritized Interrupt     |

#### 4.2.2.53 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_RAW\_STATUS\_REG0 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_RAW\_STATUS\_REG0 Register (Offset = 200h) [reset = 0h]

Raw Status Register 0

Return to [Summary Table](#)

**Table 4-773. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0200h       |

**Figure 4-247. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_RAW\_STATUS\_REG0 Name Register**

| 31            | 30            | 29            | 28            | 27            | 26            | 25            | 24            |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| RAW_STATUS_31 | RAW_STATUS_30 | RAW_STATUS_29 | RAW_STATUS_28 | RAW_STATUS_27 | RAW_STATUS_26 | RAW_STATUS_25 | RAW_STATUS_24 |
| W1TS          | W1TS          | W1TS          | W1TS          | W1TS          | W1TS          | W1TS          | W1TS          |
| 0h            | 0h            | 0h            | 0h            | 0h            | 0h            | 0h            | 0h            |
| 23            | 22            | 21            | 20            | 19            | 18            | 17            | 16            |
| RAW_STATUS_23 | RAW_STATUS_22 | RAW_STATUS_21 | RAW_STATUS_20 | RAW_STATUS_19 | RAW_STATUS_18 | RAW_STATUS_17 | RAW_STATUS_16 |
| W1TS          | W1TS          | W1TS          | W1TS          | W1TS          | W1TS          | W1TS          | W1TS          |
| 0h            | 0h            | 0h            | 0h            | 0h            | 0h            | 0h            | 0h            |
| 15            | 14            | 13            | 12            | 11            | 10            | 9             | 8             |
| RAW_STATUS_15 | RAW_STATUS_14 | RAW_STATUS_13 | RAW_STATUS_12 | RAW_STATUS_11 | RAW_STATUS_10 | RAW_STATUS_9  | RAW_STATUS_8  |
| W1TS          | W1TS          | W1TS          | W1TS          | W1TS          | W1TS          | W1TS          | W1TS          |
| 0h            | 0h            | 0h            | 0h            | 0h            | 0h            | 0h            | 0h            |
| 7             | 6             | 5             | 4             | 3             | 2             | 1             | 0             |
| RAW_STATUS_7  | RAW_STATUS_6  | RAW_STATUS_5  | RAW_STATUS_4  | RAW_STATUS_3  | RAW_STATUS_2  | RAW_STATUS_1  | RAW_STATUS_0  |
| W1TS          | W1TS          | W1TS          | W1TS          | W1TS          | W1TS          | W1TS          | W1TS          |
| 0h            | 0h            | 0h            | 0h            | 0h            | 0h            | 0h            | 0h            |

**Table 4-775. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_RAW\_STATUS\_REG0 Register Field Descriptions**

| Bit | Field         | Type | Reset | Description                                 |
|-----|---------------|------|-------|---------------------------------------------|
| 31  | RAW_STATUS_31 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[31] |
| 30  | RAW_STATUS_30 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[30] |
| 29  | RAW_STATUS_29 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[29] |
| 28  | RAW_STATUS_28 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[28] |
| 27  | RAW_STATUS_27 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[27] |
| 26  | RAW_STATUS_26 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[26] |
| 25  | RAW_STATUS_25 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[25] |
| 24  | RAW_STATUS_24 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[24] |
| 23  | RAW_STATUS_23 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[23] |
| 22  | RAW_STATUS_22 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[22] |
| 21  | RAW_STATUS_21 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[21] |
| 20  | RAW_STATUS_20 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[20] |
| 19  | RAW_STATUS_19 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[19] |
| 18  | RAW_STATUS_18 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[18] |
| 17  | RAW_STATUS_17 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[17] |

**Table 4-775. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_RAW\_STATUS\_REG0 Register Field Descriptions  
(continued)**

| Bit | Field         | Type | Reset | Description                                 |
|-----|---------------|------|-------|---------------------------------------------|
| 16  | RAW_STATUS_16 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[16] |
| 15  | RAW_STATUS_15 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[15] |
| 14  | RAW_STATUS_14 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[14] |
| 13  | RAW_STATUS_13 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[13] |
| 12  | RAW_STATUS_12 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[12] |
| 11  | RAW_STATUS_11 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[11] |
| 10  | RAW_STATUS_10 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[10] |
| 9   | RAW_STATUS_9  | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[9]  |
| 8   | RAW_STATUS_8  | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[8]  |
| 7   | RAW_STATUS_7  | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[7]  |
| 6   | RAW_STATUS_6  | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[6]  |
| 5   | RAW_STATUS_5  | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[5]  |
| 4   | RAW_STATUS_4  | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[4]  |
| 3   | RAW_STATUS_3  | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[3]  |
| 2   | RAW_STATUS_2  | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[2]  |
| 1   | RAW_STATUS_1  | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[1]  |
| 0   | RAW_STATUS_0  | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[0]  |

#### 4.2.2.54 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_RAW\_STATUS\_REG1 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_RAW\_STATUS\_REG1 Register (Offset = 204h) [reset = 0h]

Raw Status Register 1

Return to [Summary Table](#)

**Table 4-776. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0204h       |

**Figure 4-248. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_RAW\_STATUS\_REG1 Name Register**

| 31            | 30            | 29            | 28            | 27            | 26            | 25            | 24            |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| RAW_STATUS_63 | RAW_STATUS_62 | RAW_STATUS_61 | RAW_STATUS_60 | RAW_STATUS_59 | RAW_STATUS_58 | RAW_STATUS_57 | RAW_STATUS_56 |
| W1TS          | W1TS          | W1TS          | W1TS          | W1TS          | W1TS          | W1TS          | W1TS          |
| 0h            | 0h            | 0h            | 0h            | 0h            | 0h            | 0h            | 0h            |
| 23            | 22            | 21            | 20            | 19            | 18            | 17            | 16            |
| RAW_STATUS_55 | RAW_STATUS_54 | RAW_STATUS_53 | RAW_STATUS_52 | RAW_STATUS_51 | RAW_STATUS_50 | RAW_STATUS_49 | RAW_STATUS_48 |
| W1TS          | W1TS          | W1TS          | W1TS          | W1TS          | W1TS          | W1TS          | W1TS          |
| 0h            | 0h            | 0h            | 0h            | 0h            | 0h            | 0h            | 0h            |
| 15            | 14            | 13            | 12            | 11            | 10            | 9             | 8             |
| RAW_STATUS_47 | RAW_STATUS_46 | RAW_STATUS_45 | RAW_STATUS_44 | RAW_STATUS_43 | RAW_STATUS_42 | RAW_STATUS_41 | RAW_STATUS_40 |
| W1TS          | W1TS          | W1TS          | W1TS          | W1TS          | W1TS          | W1TS          | W1TS          |
| 0h            | 0h            | 0h            | 0h            | 0h            | 0h            | 0h            | 0h            |
| 7             | 6             | 5             | 4             | 3             | 2             | 1             | 0             |
| RAW_STATUS_39 | RAW_STATUS_38 | RAW_STATUS_37 | RAW_STATUS_36 | RAW_STATUS_35 | RAW_STATUS_34 | RAW_STATUS_33 | RAW_STATUS_32 |
| W1TS          | W1TS          | W1TS          | W1TS          | W1TS          | W1TS          | W1TS          | W1TS          |
| 0h            | 0h            | 0h            | 0h            | 0h            | 0h            | 0h            | 0h            |

**Table 4-778. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_RAW\_STATUS\_REG1 Register Field Descriptions**

| Bit | Field         | Type | Reset | Description                                 |
|-----|---------------|------|-------|---------------------------------------------|
| 31  | RAW_STATUS_63 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[63] |
| 30  | RAW_STATUS_62 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[62] |
| 29  | RAW_STATUS_61 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[61] |
| 28  | RAW_STATUS_60 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[60] |
| 27  | RAW_STATUS_59 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[59] |
| 26  | RAW_STATUS_58 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[58] |
| 25  | RAW_STATUS_57 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[57] |
| 24  | RAW_STATUS_56 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[56] |
| 23  | RAW_STATUS_55 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[55] |
| 22  | RAW_STATUS_54 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[54] |
| 21  | RAW_STATUS_53 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[53] |
| 20  | RAW_STATUS_52 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[52] |
| 19  | RAW_STATUS_51 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[51] |
| 18  | RAW_STATUS_50 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[50] |
| 17  | RAW_STATUS_49 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[49] |

**Table 4-778. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_RAW\_STATUS\_REG1 Register Field Descriptions  
(continued)**

| Bit | Field         | Type | Reset | Description                                 |
|-----|---------------|------|-------|---------------------------------------------|
| 16  | RAW_STATUS_48 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[48] |
| 15  | RAW_STATUS_47 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[47] |
| 14  | RAW_STATUS_46 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[46] |
| 13  | RAW_STATUS_45 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[45] |
| 12  | RAW_STATUS_44 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[44] |
| 11  | RAW_STATUS_43 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[43] |
| 10  | RAW_STATUS_42 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[42] |
| 9   | RAW_STATUS_41 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[41] |
| 8   | RAW_STATUS_40 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[40] |
| 7   | RAW_STATUS_39 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[39] |
| 6   | RAW_STATUS_38 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[38] |
| 5   | RAW_STATUS_37 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[37] |
| 4   | RAW_STATUS_36 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[36] |
| 3   | RAW_STATUS_35 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[35] |
| 2   | RAW_STATUS_34 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[34] |
| 1   | RAW_STATUS_33 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[33] |
| 0   | RAW_STATUS_32 | W1TS | 0h    | Raw Status (write 1 to set) for intr_in[32] |



#### 4.2.2.55 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENA\_STATUS\_REG0 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENA\_STATUS\_REG0 Register (Offset = 280h) [reset = 0h]

Enabled Status Register 0

Return to [Summary Table](#)

**Table 4-779. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0280h       |

**Figure 4-249. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENA\_STATUS\_REG0 Name Register**

| 31                | 30                | 29                | 28                | 27                | 26                | 25                | 24                |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| ENA_STATUS_<br>31 | ENA_STATUS_<br>30 | ENA_STATUS_<br>29 | ENA_STATUS_<br>28 | ENA_STATUS_<br>27 | ENA_STATUS_<br>26 | ENA_STATUS_<br>25 | ENA_STATUS_<br>24 |
| W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              |
| 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                |
| 23                | 22                | 21                | 20                | 19                | 18                | 17                | 16                |
| ENA_STATUS_<br>23 | ENA_STATUS_<br>22 | ENA_STATUS_<br>21 | ENA_STATUS_<br>20 | ENA_STATUS_<br>19 | ENA_STATUS_<br>18 | ENA_STATUS_<br>17 | ENA_STATUS_<br>16 |
| W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              |
| 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                |
| 15                | 14                | 13                | 12                | 11                | 10                | 9                 | 8                 |
| ENA_STATUS_<br>15 | ENA_STATUS_<br>14 | ENA_STATUS_<br>13 | ENA_STATUS_<br>12 | ENA_STATUS_<br>11 | ENA_STATUS_<br>10 | ENA_STATUS_<br>9  | ENA_STATUS_<br>8  |
| W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              |
| 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                |
| 7                 | 6                 | 5                 | 4                 | 3                 | 2                 | 1                 | 0                 |
| ENA_STATUS_<br>7  | ENA_STATUS_<br>6  | ENA_STATUS_<br>5  | ENA_STATUS_<br>4  | ENA_STATUS_<br>3  | ENA_STATUS_<br>2  | ENA_STATUS_<br>1  | ENA_STATUS_<br>0  |
| W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              |
| 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                |

**Table 4-781. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENA\_STATUS\_REG0 Register Field Descriptions**

| Bit | Field         | Type | Reset | Description                    |
|-----|---------------|------|-------|--------------------------------|
| 31  | ENA_STATUS_31 | W1TC | 0h    | Enabled Status for intr_in[31] |
| 30  | ENA_STATUS_30 | W1TC | 0h    | Enabled Status for intr_in[30] |
| 29  | ENA_STATUS_29 | W1TC | 0h    | Enabled Status for intr_in[29] |
| 28  | ENA_STATUS_28 | W1TC | 0h    | Enabled Status for intr_in[28] |
| 27  | ENA_STATUS_27 | W1TC | 0h    | Enabled Status for intr_in[27] |
| 26  | ENA_STATUS_26 | W1TC | 0h    | Enabled Status for intr_in[26] |
| 25  | ENA_STATUS_25 | W1TC | 0h    | Enabled Status for intr_in[25] |
| 24  | ENA_STATUS_24 | W1TC | 0h    | Enabled Status for intr_in[24] |
| 23  | ENA_STATUS_23 | W1TC | 0h    | Enabled Status for intr_in[23] |
| 22  | ENA_STATUS_22 | W1TC | 0h    | Enabled Status for intr_in[22] |
| 21  | ENA_STATUS_21 | W1TC | 0h    | Enabled Status for intr_in[21] |
| 20  | ENA_STATUS_20 | W1TC | 0h    | Enabled Status for intr_in[20] |
| 19  | ENA_STATUS_19 | W1TC | 0h    | Enabled Status for intr_in[19] |
| 18  | ENA_STATUS_18 | W1TC | 0h    | Enabled Status for intr_in[18] |
| 17  | ENA_STATUS_17 | W1TC | 0h    | Enabled Status for intr_in[17] |

**Table 4-781. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENA\_STATUS\_REG0 Register Field Descriptions  
(continued)**

| Bit | Field         | Type | Reset | Description                    |
|-----|---------------|------|-------|--------------------------------|
| 16  | ENA_STATUS_16 | W1TC | 0h    | Enabled Status for intr_in[16] |
| 15  | ENA_STATUS_15 | W1TC | 0h    | Enabled Status for intr_in[15] |
| 14  | ENA_STATUS_14 | W1TC | 0h    | Enabled Status for intr_in[14] |
| 13  | ENA_STATUS_13 | W1TC | 0h    | Enabled Status for intr_in[13] |
| 12  | ENA_STATUS_12 | W1TC | 0h    | Enabled Status for intr_in[12] |
| 11  | ENA_STATUS_11 | W1TC | 0h    | Enabled Status for intr_in[11] |
| 10  | ENA_STATUS_10 | W1TC | 0h    | Enabled Status for intr_in[10] |
| 9   | ENA_STATUS_9  | W1TC | 0h    | Enabled Status for intr_in[9]  |
| 8   | ENA_STATUS_8  | W1TC | 0h    | Enabled Status for intr_in[8]  |
| 7   | ENA_STATUS_7  | W1TC | 0h    | Enabled Status for intr_in[7]  |
| 6   | ENA_STATUS_6  | W1TC | 0h    | Enabled Status for intr_in[6]  |
| 5   | ENA_STATUS_5  | W1TC | 0h    | Enabled Status for intr_in[5]  |
| 4   | ENA_STATUS_4  | W1TC | 0h    | Enabled Status for intr_in[4]  |
| 3   | ENA_STATUS_3  | W1TC | 0h    | Enabled Status for intr_in[3]  |
| 2   | ENA_STATUS_2  | W1TC | 0h    | Enabled Status for intr_in[2]  |
| 1   | ENA_STATUS_1  | W1TC | 0h    | Enabled Status for intr_in[1]  |
| 0   | ENA_STATUS_0  | W1TC | 0h    | Enabled Status for intr_in[0]  |

#### 4.2.2.56 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENA\_STATUS\_REG1 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENA\_STATUS\_REG1 Register (Offset = 284h) [reset = 0h]

Enabled Status Register 1

Return to [Summary Table](#)

**Table 4-782. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0284h       |

**Figure 4-250. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENA\_STATUS\_REG1 Name Register**

| 31            | 30            | 29            | 28            | 27            | 26            | 25            | 24            |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| ENA_STATUS_63 | ENA_STATUS_62 | ENA_STATUS_61 | ENA_STATUS_60 | ENA_STATUS_59 | ENA_STATUS_58 | ENA_STATUS_57 | ENA_STATUS_56 |
| W1TC          | W1TC          | W1TC          | W1TC          | W1TC          | W1TC          | W1TC          | W1TC          |
| 0h            | 0h            | 0h            | 0h            | 0h            | 0h            | 0h            | 0h            |
| 23            | 22            | 21            | 20            | 19            | 18            | 17            | 16            |
| ENA_STATUS_55 | ENA_STATUS_54 | ENA_STATUS_53 | ENA_STATUS_52 | ENA_STATUS_51 | ENA_STATUS_50 | ENA_STATUS_49 | ENA_STATUS_48 |
| W1TC          | W1TC          | W1TC          | W1TC          | W1TC          | W1TC          | W1TC          | W1TC          |
| 0h            | 0h            | 0h            | 0h            | 0h            | 0h            | 0h            | 0h            |
| 15            | 14            | 13            | 12            | 11            | 10            | 9             | 8             |
| ENA_STATUS_47 | ENA_STATUS_46 | ENA_STATUS_45 | ENA_STATUS_44 | ENA_STATUS_43 | ENA_STATUS_42 | ENA_STATUS_41 | ENA_STATUS_40 |
| W1TC          | W1TC          | W1TC          | W1TC          | W1TC          | W1TC          | W1TC          | W1TC          |
| 0h            | 0h            | 0h            | 0h            | 0h            | 0h            | 0h            | 0h            |
| 7             | 6             | 5             | 4             | 3             | 2             | 1             | 0             |
| ENA_STATUS_39 | ENA_STATUS_38 | ENA_STATUS_37 | ENA_STATUS_36 | ENA_STATUS_35 | ENA_STATUS_34 | ENA_STATUS_33 | ENA_STATUS_32 |
| W1TC          | W1TC          | W1TC          | W1TC          | W1TC          | W1TC          | W1TC          | W1TC          |
| 0h            | 0h            | 0h            | 0h            | 0h            | 0h            | 0h            | 0h            |

**Table 4-784. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENA\_STATUS\_REG1 Register Field Descriptions**

| Bit | Field         | Type | Reset | Description                    |
|-----|---------------|------|-------|--------------------------------|
| 31  | ENA_STATUS_63 | W1TC | 0h    | Enabled Status for intr_in[63] |
| 30  | ENA_STATUS_62 | W1TC | 0h    | Enabled Status for intr_in[62] |
| 29  | ENA_STATUS_61 | W1TC | 0h    | Enabled Status for intr_in[61] |
| 28  | ENA_STATUS_60 | W1TC | 0h    | Enabled Status for intr_in[60] |
| 27  | ENA_STATUS_59 | W1TC | 0h    | Enabled Status for intr_in[59] |
| 26  | ENA_STATUS_58 | W1TC | 0h    | Enabled Status for intr_in[58] |
| 25  | ENA_STATUS_57 | W1TC | 0h    | Enabled Status for intr_in[57] |
| 24  | ENA_STATUS_56 | W1TC | 0h    | Enabled Status for intr_in[56] |
| 23  | ENA_STATUS_55 | W1TC | 0h    | Enabled Status for intr_in[55] |
| 22  | ENA_STATUS_54 | W1TC | 0h    | Enabled Status for intr_in[54] |
| 21  | ENA_STATUS_53 | W1TC | 0h    | Enabled Status for intr_in[53] |
| 20  | ENA_STATUS_52 | W1TC | 0h    | Enabled Status for intr_in[52] |
| 19  | ENA_STATUS_51 | W1TC | 0h    | Enabled Status for intr_in[51] |
| 18  | ENA_STATUS_50 | W1TC | 0h    | Enabled Status for intr_in[50] |
| 17  | ENA_STATUS_49 | W1TC | 0h    | Enabled Status for intr_in[49] |

**Table 4-784. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENA\_STATUS\_REG1 Register Field Descriptions  
(continued)**

| Bit | Field         | Type | Reset | Description                    |
|-----|---------------|------|-------|--------------------------------|
| 16  | ENA_STATUS_48 | W1TC | 0h    | Enabled Status for intr_in[48] |
| 15  | ENA_STATUS_47 | W1TC | 0h    | Enabled Status for intr_in[47] |
| 14  | ENA_STATUS_46 | W1TC | 0h    | Enabled Status for intr_in[46] |
| 13  | ENA_STATUS_45 | W1TC | 0h    | Enabled Status for intr_in[45] |
| 12  | ENA_STATUS_44 | W1TC | 0h    | Enabled Status for intr_in[44] |
| 11  | ENA_STATUS_43 | W1TC | 0h    | Enabled Status for intr_in[43] |
| 10  | ENA_STATUS_42 | W1TC | 0h    | Enabled Status for intr_in[42] |
| 9   | ENA_STATUS_41 | W1TC | 0h    | Enabled Status for intr_in[41] |
| 8   | ENA_STATUS_40 | W1TC | 0h    | Enabled Status for intr_in[40] |
| 7   | ENA_STATUS_39 | W1TC | 0h    | Enabled Status for intr_in[39] |
| 6   | ENA_STATUS_38 | W1TC | 0h    | Enabled Status for intr_in[38] |
| 5   | ENA_STATUS_37 | W1TC | 0h    | Enabled Status for intr_in[37] |
| 4   | ENA_STATUS_36 | W1TC | 0h    | Enabled Status for intr_in[36] |
| 3   | ENA_STATUS_35 | W1TC | 0h    | Enabled Status for intr_in[35] |
| 2   | ENA_STATUS_34 | W1TC | 0h    | Enabled Status for intr_in[34] |
| 1   | ENA_STATUS_33 | W1TC | 0h    | Enabled Status for intr_in[33] |
| 0   | ENA_STATUS_32 | W1TC | 0h    | Enabled Status for intr_in[32] |

#### 4.2.2.57 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENABLE\_REG0 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENABLE\_REG0 Register (Offset = 300h) [reset = 0h]

Enable Register 0

Return to [Summary Table](#)

**Table 4-785. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0300h       |

**Figure 4-251. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENABLE\_REG0 Name Register**

| 31        | 30        | 29        | 28        | 27        | 26        | 25        | 24        |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| ENABLE_31 | ENABLE_30 | ENABLE_29 | ENABLE_28 | ENABLE_27 | ENABLE_26 | ENABLE_25 | ENABLE_24 |
| W1TS      | W1TS      | W1TS      | W1TS      | W1TS      | W1TS      | W1TS      | W1TS      |
| 0h        | 0h        | 0h        | 0h        | 0h        | 0h        | 0h        | 0h        |
| 23        | 22        | 21        | 20        | 19        | 18        | 17        | 16        |
| ENABLE_23 | ENABLE_22 | ENABLE_21 | ENABLE_20 | ENABLE_19 | ENABLE_18 | ENABLE_17 | ENABLE_16 |
| W1TS      | W1TS      | W1TS      | W1TS      | W1TS      | W1TS      | W1TS      | W1TS      |
| 0h        | 0h        | 0h        | 0h        | 0h        | 0h        | 0h        | 0h        |
| 15        | 14        | 13        | 12        | 11        | 10        | 9         | 8         |
| ENABLE_15 | ENABLE_14 | ENABLE_13 | ENABLE_12 | ENABLE_11 | ENABLE_10 | ENABLE_9  | ENABLE_8  |
| W1TS      | W1TS      | W1TS      | W1TS      | W1TS      | W1TS      | W1TS      | W1TS      |
| 0h        | 0h        | 0h        | 0h        | 0h        | 0h        | 0h        | 0h        |
| 7         | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
| ENABLE_7  | ENABLE_6  | ENABLE_5  | ENABLE_4  | ENABLE_3  | ENABLE_2  | ENABLE_1  | ENABLE_0  |
| W1TS      | W1TS      | W1TS      | W1TS      | W1TS      | W1TS      | W1TS      | W1TS      |
| 0h        | 0h        | 0h        | 0h        | 0h        | 0h        | 0h        | 0h        |

**Table 4-787. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENABLE\_REG0 Register Field Descriptions**

| Bit | Field     | Type | Reset | Description                  |
|-----|-----------|------|-------|------------------------------|
| 31  | ENABLE_31 | W1TS | 0h    | Enable (set) for intr_in[31] |
| 30  | ENABLE_30 | W1TS | 0h    | Enable (set) for intr_in[30] |
| 29  | ENABLE_29 | W1TS | 0h    | Enable (set) for intr_in[29] |
| 28  | ENABLE_28 | W1TS | 0h    | Enable (set) for intr_in[28] |
| 27  | ENABLE_27 | W1TS | 0h    | Enable (set) for intr_in[27] |
| 26  | ENABLE_26 | W1TS | 0h    | Enable (set) for intr_in[26] |
| 25  | ENABLE_25 | W1TS | 0h    | Enable (set) for intr_in[25] |
| 24  | ENABLE_24 | W1TS | 0h    | Enable (set) for intr_in[24] |
| 23  | ENABLE_23 | W1TS | 0h    | Enable (set) for intr_in[23] |
| 22  | ENABLE_22 | W1TS | 0h    | Enable (set) for intr_in[22] |
| 21  | ENABLE_21 | W1TS | 0h    | Enable (set) for intr_in[21] |
| 20  | ENABLE_20 | W1TS | 0h    | Enable (set) for intr_in[20] |
| 19  | ENABLE_19 | W1TS | 0h    | Enable (set) for intr_in[19] |
| 18  | ENABLE_18 | W1TS | 0h    | Enable (set) for intr_in[18] |
| 17  | ENABLE_17 | W1TS | 0h    | Enable (set) for intr_in[17] |
| 16  | ENABLE_16 | W1TS | 0h    | Enable (set) for intr_in[16] |
| 15  | ENABLE_15 | W1TS | 0h    | Enable (set) for intr_in[15] |
| 14  | ENABLE_14 | W1TS | 0h    | Enable (set) for intr_in[14] |

**Table 4-787. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENABLE\_REG0 Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description                  |
|-----|-----------|------|-------|------------------------------|
| 13  | ENABLE_13 | W1TS | 0h    | Enable (set) for intr_in[13] |
| 12  | ENABLE_12 | W1TS | 0h    | Enable (set) for intr_in[12] |
| 11  | ENABLE_11 | W1TS | 0h    | Enable (set) for intr_in[11] |
| 10  | ENABLE_10 | W1TS | 0h    | Enable (set) for intr_in[10] |
| 9   | ENABLE_9  | W1TS | 0h    | Enable (set) for intr_in[9]  |
| 8   | ENABLE_8  | W1TS | 0h    | Enable (set) for intr_in[8]  |
| 7   | ENABLE_7  | W1TS | 0h    | Enable (set) for intr_in[7]  |
| 6   | ENABLE_6  | W1TS | 0h    | Enable (set) for intr_in[6]  |
| 5   | ENABLE_5  | W1TS | 0h    | Enable (set) for intr_in[5]  |
| 4   | ENABLE_4  | W1TS | 0h    | Enable (set) for intr_in[4]  |
| 3   | ENABLE_3  | W1TS | 0h    | Enable (set) for intr_in[3]  |
| 2   | ENABLE_2  | W1TS | 0h    | Enable (set) for intr_in[2]  |
| 1   | ENABLE_1  | W1TS | 0h    | Enable (set) for intr_in[1]  |
| 0   | ENABLE_0  | W1TS | 0h    | Enable (set) for intr_in[0]  |

#### 4.2.2.58 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENABLE\_REG1 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENABLE\_REG1 Register (Offset = 304h) [reset = 0h]

Enable Register 1

Return to [Summary Table](#)

**Table 4-788. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0304h       |

**Figure 4-252. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENABLE\_REG1 Name Register**

| 31        | 30        | 29        | 28        | 27        | 26        | 25        | 24        |
|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| ENABLE_63 | ENABLE_62 | ENABLE_61 | ENABLE_60 | ENABLE_59 | ENABLE_58 | ENABLE_57 | ENABLE_56 |
| W1TS      | W1TS      | W1TS      | W1TS      | W1TS      | W1TS      | W1TS      | W1TS      |
| 0h        | 0h        | 0h        | 0h        | 0h        | 0h        | 0h        | 0h        |
| 23        | 22        | 21        | 20        | 19        | 18        | 17        | 16        |
| ENABLE_55 | ENABLE_54 | ENABLE_53 | ENABLE_52 | ENABLE_51 | ENABLE_50 | ENABLE_49 | ENABLE_48 |
| W1TS      | W1TS      | W1TS      | W1TS      | W1TS      | W1TS      | W1TS      | W1TS      |
| 0h        | 0h        | 0h        | 0h        | 0h        | 0h        | 0h        | 0h        |
| 15        | 14        | 13        | 12        | 11        | 10        | 9         | 8         |
| ENABLE_47 | ENABLE_46 | ENABLE_45 | ENABLE_44 | ENABLE_43 | ENABLE_42 | ENABLE_41 | ENABLE_40 |
| W1TS      | W1TS      | W1TS      | W1TS      | W1TS      | W1TS      | W1TS      | W1TS      |
| 0h        | 0h        | 0h        | 0h        | 0h        | 0h        | 0h        | 0h        |
| 7         | 6         | 5         | 4         | 3         | 2         | 1         | 0         |
| ENABLE_39 | ENABLE_38 | ENABLE_37 | ENABLE_36 | ENABLE_35 | ENABLE_34 | ENABLE_33 | ENABLE_32 |
| W1TS      | W1TS      | W1TS      | W1TS      | W1TS      | W1TS      | W1TS      | W1TS      |
| 0h        | 0h        | 0h        | 0h        | 0h        | 0h        | 0h        | 0h        |

**Table 4-790. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENABLE\_REG1 Register Field Descriptions**

| Bit | Field     | Type | Reset | Description                  |
|-----|-----------|------|-------|------------------------------|
| 31  | ENABLE_63 | W1TS | 0h    | Enable (set) for intr_in[63] |
| 30  | ENABLE_62 | W1TS | 0h    | Enable (set) for intr_in[62] |
| 29  | ENABLE_61 | W1TS | 0h    | Enable (set) for intr_in[61] |
| 28  | ENABLE_60 | W1TS | 0h    | Enable (set) for intr_in[60] |
| 27  | ENABLE_59 | W1TS | 0h    | Enable (set) for intr_in[59] |
| 26  | ENABLE_58 | W1TS | 0h    | Enable (set) for intr_in[58] |
| 25  | ENABLE_57 | W1TS | 0h    | Enable (set) for intr_in[57] |
| 24  | ENABLE_56 | W1TS | 0h    | Enable (set) for intr_in[56] |
| 23  | ENABLE_55 | W1TS | 0h    | Enable (set) for intr_in[55] |
| 22  | ENABLE_54 | W1TS | 0h    | Enable (set) for intr_in[54] |
| 21  | ENABLE_53 | W1TS | 0h    | Enable (set) for intr_in[53] |
| 20  | ENABLE_52 | W1TS | 0h    | Enable (set) for intr_in[52] |
| 19  | ENABLE_51 | W1TS | 0h    | Enable (set) for intr_in[51] |
| 18  | ENABLE_50 | W1TS | 0h    | Enable (set) for intr_in[50] |
| 17  | ENABLE_49 | W1TS | 0h    | Enable (set) for intr_in[49] |
| 16  | ENABLE_48 | W1TS | 0h    | Enable (set) for intr_in[48] |
| 15  | ENABLE_47 | W1TS | 0h    | Enable (set) for intr_in[47] |
| 14  | ENABLE_46 | W1TS | 0h    | Enable (set) for intr_in[46] |

**Table 4-790. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENABLE\_REG1 Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description                  |
|-----|-----------|------|-------|------------------------------|
| 13  | ENABLE_45 | W1TS | 0h    | Enable (set) for intr_in[45] |
| 12  | ENABLE_44 | W1TS | 0h    | Enable (set) for intr_in[44] |
| 11  | ENABLE_43 | W1TS | 0h    | Enable (set) for intr_in[43] |
| 10  | ENABLE_42 | W1TS | 0h    | Enable (set) for intr_in[42] |
| 9   | ENABLE_41 | W1TS | 0h    | Enable (set) for intr_in[41] |
| 8   | ENABLE_40 | W1TS | 0h    | Enable (set) for intr_in[40] |
| 7   | ENABLE_39 | W1TS | 0h    | Enable (set) for intr_in[39] |
| 6   | ENABLE_38 | W1TS | 0h    | Enable (set) for intr_in[38] |
| 5   | ENABLE_37 | W1TS | 0h    | Enable (set) for intr_in[37] |
| 4   | ENABLE_36 | W1TS | 0h    | Enable (set) for intr_in[36] |
| 3   | ENABLE_35 | W1TS | 0h    | Enable (set) for intr_in[35] |
| 2   | ENABLE_34 | W1TS | 0h    | Enable (set) for intr_in[34] |
| 1   | ENABLE_33 | W1TS | 0h    | Enable (set) for intr_in[33] |
| 0   | ENABLE_32 | W1TS | 0h    | Enable (set) for intr_in[32] |



#### 4.2.2.59 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENABLE\_CLR\_REG0 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENABLE\_CLR\_REG0 Register (Offset = 380h) [reset = 0h]

Enable Clear Register 0

Return to [Summary Table](#)

**Table 4-791. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0380h       |

**Figure 4-253. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENABLE\_CLR\_REG0 Name Register**

| 31                | 30                | 29                | 28                | 27                | 26                | 25                | 24                |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| ENABLE_31_C<br>LR | ENABLE_30_C<br>LR | ENABLE_29_C<br>LR | ENABLE_28_C<br>LR | ENABLE_27_C<br>LR | ENABLE_26_C<br>LR | ENABLE_25_C<br>LR | ENABLE_24_C<br>LR |
| W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              |
| 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                |
| 23                | 22                | 21                | 20                | 19                | 18                | 17                | 16                |
| ENABLE_23_C<br>LR | ENABLE_22_C<br>LR | ENABLE_21_C<br>LR | ENABLE_20_C<br>LR | ENABLE_19_C<br>LR | ENABLE_18_C<br>LR | ENABLE_17_C<br>LR | ENABLE_16_C<br>LR |
| W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              |
| 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                |
| 15                | 14                | 13                | 12                | 11                | 10                | 9                 | 8                 |
| ENABLE_15_C<br>LR | ENABLE_14_C<br>LR | ENABLE_13_C<br>LR | ENABLE_12_C<br>LR | ENABLE_11_C<br>LR | ENABLE_10_C<br>LR | ENABLE_9_C<br>LR  | ENABLE_8_C<br>LR  |
| W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              |
| 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                |
| 7                 | 6                 | 5                 | 4                 | 3                 | 2                 | 1                 | 0                 |
| ENABLE_7_C<br>LR  | ENABLE_6_C<br>LR  | ENABLE_5_C<br>LR  | ENABLE_4_C<br>LR  | ENABLE_3_C<br>LR  | ENABLE_2_C<br>LR  | ENABLE_1_C<br>LR  | ENABLE_0_C<br>LR  |
| W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              |
| 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                |

**Table 4-793. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENABLE\_CLR\_REG0 Register Field Descriptions**

| Bit | Field         | Type | Reset | Description                  |
|-----|---------------|------|-------|------------------------------|
| 31  | ENABLE_31_CLR | W1TC | 0h    | Enable clear for intr_in[31] |
| 30  | ENABLE_30_CLR | W1TC | 0h    | Enable clear for intr_in[30] |
| 29  | ENABLE_29_CLR | W1TC | 0h    | Enable clear for intr_in[29] |
| 28  | ENABLE_28_CLR | W1TC | 0h    | Enable clear for intr_in[28] |
| 27  | ENABLE_27_CLR | W1TC | 0h    | Enable clear for intr_in[27] |
| 26  | ENABLE_26_CLR | W1TC | 0h    | Enable clear for intr_in[26] |
| 25  | ENABLE_25_CLR | W1TC | 0h    | Enable clear for intr_in[25] |
| 24  | ENABLE_24_CLR | W1TC | 0h    | Enable clear for intr_in[24] |
| 23  | ENABLE_23_CLR | W1TC | 0h    | Enable clear for intr_in[23] |
| 22  | ENABLE_22_CLR | W1TC | 0h    | Enable clear for intr_in[22] |
| 21  | ENABLE_21_CLR | W1TC | 0h    | Enable clear for intr_in[21] |
| 20  | ENABLE_20_CLR | W1TC | 0h    | Enable clear for intr_in[20] |
| 19  | ENABLE_19_CLR | W1TC | 0h    | Enable clear for intr_in[19] |
| 18  | ENABLE_18_CLR | W1TC | 0h    | Enable clear for intr_in[18] |
| 17  | ENABLE_17_CLR | W1TC | 0h    | Enable clear for intr_in[17] |

**Table 4-793. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENABLE\_CLR\_REG0 Register Field Descriptions  
(continued)**

| Bit | Field         | Type | Reset | Description                  |
|-----|---------------|------|-------|------------------------------|
| 16  | ENABLE_16_CLR | W1TC | 0h    | Enable clear for intr_in[16] |
| 15  | ENABLE_15_CLR | W1TC | 0h    | Enable clear for intr_in[15] |
| 14  | ENABLE_14_CLR | W1TC | 0h    | Enable clear for intr_in[14] |
| 13  | ENABLE_13_CLR | W1TC | 0h    | Enable clear for intr_in[13] |
| 12  | ENABLE_12_CLR | W1TC | 0h    | Enable clear for intr_in[12] |
| 11  | ENABLE_11_CLR | W1TC | 0h    | Enable clear for intr_in[11] |
| 10  | ENABLE_10_CLR | W1TC | 0h    | Enable clear for intr_in[10] |
| 9   | ENABLE_9_CLR  | W1TC | 0h    | Enable clear for intr_in[9]  |
| 8   | ENABLE_8_CLR  | W1TC | 0h    | Enable clear for intr_in[8]  |
| 7   | ENABLE_7_CLR  | W1TC | 0h    | Enable clear for intr_in[7]  |
| 6   | ENABLE_6_CLR  | W1TC | 0h    | Enable clear for intr_in[6]  |
| 5   | ENABLE_5_CLR  | W1TC | 0h    | Enable clear for intr_in[5]  |
| 4   | ENABLE_4_CLR  | W1TC | 0h    | Enable clear for intr_in[4]  |
| 3   | ENABLE_3_CLR  | W1TC | 0h    | Enable clear for intr_in[3]  |
| 2   | ENABLE_2_CLR  | W1TC | 0h    | Enable clear for intr_in[2]  |
| 1   | ENABLE_1_CLR  | W1TC | 0h    | Enable clear for intr_in[1]  |
| 0   | ENABLE_0_CLR  | W1TC | 0h    | Enable clear for intr_in[0]  |

#### 4.2.2.60 ICSSM\_PR1\_ICSS\_INTIC\_INTIC\_SLV\_ENABLE\_CLR\_REG1 Register

##### 1 ICSSM\_PR1\_ICSS\_INTIC\_INTIC\_SLV\_ENABLE\_CLR\_REG1 Register (Offset = 384h) [reset = 0h]

Enable Clear Register 1

Return to [Summary Table](#)

**Table 4-794. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0384h       |

**Figure 4-254. ICSSM\_PR1\_ICSS\_INTIC\_INTIC\_SLV\_ENABLE\_CLR\_REG1 Name Register**

| 31                | 30                | 29                | 28                | 27                | 26                | 25                | 24                |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| ENABLE_63_C<br>LR | ENABLE_62_C<br>LR | ENABLE_61_C<br>LR | ENABLE_60_C<br>LR | ENABLE_59_C<br>LR | ENABLE_58_C<br>LR | ENABLE_57_C<br>LR | ENABLE_56_C<br>LR |
| W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              |
| 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                |
| 23                | 22                | 21                | 20                | 19                | 18                | 17                | 16                |
| ENABLE_55_C<br>LR | ENABLE_54_C<br>LR | ENABLE_53_C<br>LR | ENABLE_52_C<br>LR | ENABLE_51_C<br>LR | ENABLE_50_C<br>LR | ENABLE_49_C<br>LR | ENABLE_48_C<br>LR |
| W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              |
| 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                |
| 15                | 14                | 13                | 12                | 11                | 10                | 9                 | 8                 |
| ENABLE_47_C<br>LR | ENABLE_46_C<br>LR | ENABLE_45_C<br>LR | ENABLE_44_C<br>LR | ENABLE_43_C<br>LR | ENABLE_42_C<br>LR | ENABLE_41_C<br>LR | ENABLE_40_C<br>LR |
| W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              |
| 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                |
| 7                 | 6                 | 5                 | 4                 | 3                 | 2                 | 1                 | 0                 |
| ENABLE_39_C<br>LR | ENABLE_38_C<br>LR | ENABLE_37_C<br>LR | ENABLE_36_C<br>LR | ENABLE_35_C<br>LR | ENABLE_34_C<br>LR | ENABLE_33_C<br>LR | ENABLE_32_C<br>LR |
| W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              | W1TC              |
| 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                |

**Table 4-796. ICSSM\_PR1\_ICSS\_INTIC\_INTIC\_SLV\_ENABLE\_CLR\_REG1 Register Field Descriptions**

| Bit | Field         | Type | Reset | Description                  |
|-----|---------------|------|-------|------------------------------|
| 31  | ENABLE_63_CLR | W1TC | 0h    | Enable clear for intr_in[63] |
| 30  | ENABLE_62_CLR | W1TC | 0h    | Enable clear for intr_in[62] |
| 29  | ENABLE_61_CLR | W1TC | 0h    | Enable clear for intr_in[61] |
| 28  | ENABLE_60_CLR | W1TC | 0h    | Enable clear for intr_in[60] |
| 27  | ENABLE_59_CLR | W1TC | 0h    | Enable clear for intr_in[59] |
| 26  | ENABLE_58_CLR | W1TC | 0h    | Enable clear for intr_in[58] |
| 25  | ENABLE_57_CLR | W1TC | 0h    | Enable clear for intr_in[57] |
| 24  | ENABLE_56_CLR | W1TC | 0h    | Enable clear for intr_in[56] |
| 23  | ENABLE_55_CLR | W1TC | 0h    | Enable clear for intr_in[55] |
| 22  | ENABLE_54_CLR | W1TC | 0h    | Enable clear for intr_in[54] |
| 21  | ENABLE_53_CLR | W1TC | 0h    | Enable clear for intr_in[53] |
| 20  | ENABLE_52_CLR | W1TC | 0h    | Enable clear for intr_in[52] |
| 19  | ENABLE_51_CLR | W1TC | 0h    | Enable clear for intr_in[51] |
| 18  | ENABLE_50_CLR | W1TC | 0h    | Enable clear for intr_in[50] |
| 17  | ENABLE_49_CLR | W1TC | 0h    | Enable clear for intr_in[49] |

**Table 4-796. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENABLE\_CLR\_REG1 Register Field Descriptions  
(continued)**

| Bit | Field         | Type | Reset | Description                  |
|-----|---------------|------|-------|------------------------------|
| 16  | ENABLE_48_CLR | W1TC | 0h    | Enable clear for intr_in[48] |
| 15  | ENABLE_47_CLR | W1TC | 0h    | Enable clear for intr_in[47] |
| 14  | ENABLE_46_CLR | W1TC | 0h    | Enable clear for intr_in[46] |
| 13  | ENABLE_45_CLR | W1TC | 0h    | Enable clear for intr_in[45] |
| 12  | ENABLE_44_CLR | W1TC | 0h    | Enable clear for intr_in[44] |
| 11  | ENABLE_43_CLR | W1TC | 0h    | Enable clear for intr_in[43] |
| 10  | ENABLE_42_CLR | W1TC | 0h    | Enable clear for intr_in[42] |
| 9   | ENABLE_41_CLR | W1TC | 0h    | Enable clear for intr_in[41] |
| 8   | ENABLE_40_CLR | W1TC | 0h    | Enable clear for intr_in[40] |
| 7   | ENABLE_39_CLR | W1TC | 0h    | Enable clear for intr_in[39] |
| 6   | ENABLE_38_CLR | W1TC | 0h    | Enable clear for intr_in[38] |
| 5   | ENABLE_37_CLR | W1TC | 0h    | Enable clear for intr_in[37] |
| 4   | ENABLE_36_CLR | W1TC | 0h    | Enable clear for intr_in[36] |
| 3   | ENABLE_35_CLR | W1TC | 0h    | Enable clear for intr_in[35] |
| 2   | ENABLE_34_CLR | W1TC | 0h    | Enable clear for intr_in[34] |
| 1   | ENABLE_33_CLR | W1TC | 0h    | Enable clear for intr_in[33] |
| 0   | ENABLE_32_CLR | W1TC | 0h    | Enable clear for intr_in[32] |

#### 4.2.2.61 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG0 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG0 Register (Offset = 400h) [reset = 0h]

Interrupt Channel Map Register for 0 to 0+3

Return to [Summary Table](#)

**Table 4-797. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0400h       |

**Figure 4-255. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG0 Name Register**

| 31       | 30 | 29 | 28 | 27       | 26 | 25 | 24 |
|----------|----|----|----|----------|----|----|----|
| RESERVED |    |    |    | CH_MAP_3 |    |    |    |
| NONE     |    |    |    | R/W      |    |    |    |
| 0h       |    |    |    | 0h       |    |    |    |
| 23       | 22 | 21 | 20 | 19       | 18 | 17 | 16 |
| RESERVED |    |    |    | CH_MAP_2 |    |    |    |
| NONE     |    |    |    | R/W      |    |    |    |
| 0h       |    |    |    | 0h       |    |    |    |
| 15       | 14 | 13 | 12 | 11       | 10 | 9  | 8  |
| RESERVED |    |    |    | CH_MAP_1 |    |    |    |
| NONE     |    |    |    | R/W      |    |    |    |
| 0h       |    |    |    | 0h       |    |    |    |
| 7        | 6  | 5  | 4  | 3        | 2  | 1  | 0  |
| RESERVED |    |    |    | CH_MAP_0 |    |    |    |
| NONE     |    |    |    | W        |    |    |    |
| 0h       |    |    |    | 0h       |    |    |    |

**Table 4-799. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG0 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                          |
|-------|----------|------|-------|--------------------------------------|
| 31:28 | RESERVED | NONE | 0h    | Reserved                             |
| 27:24 | CH_MAP_3 | R/W  | 0h    | Interrupt Channel Map for intr_in[3] |
| 23:20 | RESERVED | NONE | 0h    | Reserved                             |
| 19:16 | CH_MAP_2 | R/W  | 0h    | Interrupt Channel Map for intr_in[2] |
| 15:12 | RESERVED | NONE | 0h    | Reserved                             |
| 11:8  | CH_MAP_1 | R/W  | 0h    | Interrupt Channel Map for intr_in[1] |
| 7:4   | RESERVED | NONE | 0h    | Reserved                             |
| 3:0   | CH_MAP_0 | W    | 0h    | Interrupt Channel Map for intr_in[0] |

#### 4.2.2.62 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG1 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG1 Register (Offset = 404h) [reset = 0h]

Interrupt Channel Map Register for 4 to 4+3

Return to [Summary Table](#)

**Table 4-800. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0404h       |

**Figure 4-256. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG1 Name Register**

| 31       | 30 | 29 | 28 | 27       | 26 | 25 | 24 |
|----------|----|----|----|----------|----|----|----|
| RESERVED |    |    |    | CH_MAP_7 |    |    |    |
| NONE     |    |    |    | R/W      |    |    |    |
| 0h       |    |    |    | 0h       |    |    |    |
| 23       | 22 | 21 | 20 | 19       | 18 | 17 | 16 |
| RESERVED |    |    |    | CH_MAP_6 |    |    |    |
| NONE     |    |    |    | R/W      |    |    |    |
| 0h       |    |    |    | 0h       |    |    |    |
| 15       | 14 | 13 | 12 | 11       | 10 | 9  | 8  |
| RESERVED |    |    |    | CH_MAP_5 |    |    |    |
| NONE     |    |    |    | R/W      |    |    |    |
| 0h       |    |    |    | 0h       |    |    |    |
| 7        | 6  | 5  | 4  | 3        | 2  | 1  | 0  |
| RESERVED |    |    |    | CH_MAP_4 |    |    |    |
| NONE     |    |    |    | R/W      |    |    |    |
| 0h       |    |    |    | 0h       |    |    |    |

**Table 4-802. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG1 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                          |
|-------|----------|------|-------|--------------------------------------|
| 31:28 | RESERVED | NONE | 0h    | Reserved                             |
| 27:24 | CH_MAP_7 | R/W  | 0h    | Interrupt Channel Map for intr_in[7] |
| 23:20 | RESERVED | NONE | 0h    | Reserved                             |
| 19:16 | CH_MAP_6 | R/W  | 0h    | Interrupt Channel Map for intr_in[6] |
| 15:12 | RESERVED | NONE | 0h    | Reserved                             |
| 11:8  | CH_MAP_5 | R/W  | 0h    | Interrupt Channel Map for intr_in[5] |
| 7:4   | RESERVED | NONE | 0h    | Reserved                             |
| 3:0   | CH_MAP_4 | R/W  | 0h    | Interrupt Channel Map for intr_in[4] |

#### 4.2.2.63 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG2 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG2 Register (Offset = 408h) [reset = 0h]

Interrupt Channel Map Register for 8 to 8+3

Return to [Summary Table](#)

**Table 4-803. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0408h       |

**Figure 4-257. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG2 Name Register**

| 31       | 30 | 29 | 28 | 27        | 26 | 25 | 24 |
|----------|----|----|----|-----------|----|----|----|
| RESERVED |    |    |    | CH_MAP_11 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 23       | 22 | 21 | 20 | 19        | 18 | 17 | 16 |
| RESERVED |    |    |    | CH_MAP_10 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 15       | 14 | 13 | 12 | 11        | 10 | 9  | 8  |
| RESERVED |    |    |    | CH_MAP_9  |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 7        | 6  | 5  | 4  | 3         | 2  | 1  | 0  |
| RESERVED |    |    |    | CH_MAP_8  |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |

**Table 4-805. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG2 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                           |
|-------|-----------|------|-------|---------------------------------------|
| 31:28 | RESERVED  | NONE | 0h    | Reserved                              |
| 27:24 | CH_MAP_11 | R/W  | 0h    | Interrupt Channel Map for intr_in[11] |
| 23:20 | RESERVED  | NONE | 0h    | Reserved                              |
| 19:16 | CH_MAP_10 | R/W  | 0h    | Interrupt Channel Map for intr_in[10] |
| 15:12 | RESERVED  | NONE | 0h    | Reserved                              |
| 11:8  | CH_MAP_9  | R/W  | 0h    | Interrupt Channel Map for intr_in[9]  |
| 7:4   | RESERVED  | NONE | 0h    | Reserved                              |
| 3:0   | CH_MAP_8  | R/W  | 0h    | Interrupt Channel Map for intr_in[8]  |

#### 4.2.2.64 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG3 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG3 Register (Offset = 40Ch) [reset = 0h]

Interrupt Channel Map Register for 12 to 12+3

Return to [Summary Table](#)

**Table 4-806. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 040Ch       |

**Figure 4-258. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG3 Name Register**

| 31       | 30 | 29 | 28 | 27        | 26 | 25 | 24 |
|----------|----|----|----|-----------|----|----|----|
| RESERVED |    |    |    | CH_MAP_15 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 23       | 22 | 21 | 20 | 19        | 18 | 17 | 16 |
| RESERVED |    |    |    | CH_MAP_14 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 15       | 14 | 13 | 12 | 11        | 10 | 9  | 8  |
| RESERVED |    |    |    | CH_MAP_13 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 7        | 6  | 5  | 4  | 3         | 2  | 1  | 0  |
| RESERVED |    |    |    | CH_MAP_12 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |

**Table 4-808. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG3 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                           |
|-------|-----------|------|-------|---------------------------------------|
| 31:28 | RESERVED  | NONE | 0h    | Reserved                              |
| 27:24 | CH_MAP_15 | R/W  | 0h    | Interrupt Channel Map for intr_in[15] |
| 23:20 | RESERVED  | NONE | 0h    | Reserved                              |
| 19:16 | CH_MAP_14 | R/W  | 0h    | Interrupt Channel Map for intr_in[14] |
| 15:12 | RESERVED  | NONE | 0h    | Reserved                              |
| 11:8  | CH_MAP_13 | R/W  | 0h    | Interrupt Channel Map for intr_in[13] |
| 7:4   | RESERVED  | NONE | 0h    | Reserved                              |
| 3:0   | CH_MAP_12 | R/W  | 0h    | Interrupt Channel Map for intr_in[12] |



#### 4.2.2.65 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG4 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG4 Register (Offset = 410h) [reset = 0h]

Interrupt Channel Map Register for 16 to 16+3

Return to [Summary Table](#)

**Table 4-809. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0410h       |

**Figure 4-259. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG4 Name Register**

| 31       | 30 | 29 | 28 | 27        | 26 | 25 | 24 |
|----------|----|----|----|-----------|----|----|----|
| RESERVED |    |    |    | CH_MAP_19 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 23       | 22 | 21 | 20 | 19        | 18 | 17 | 16 |
| RESERVED |    |    |    | CH_MAP_18 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 15       | 14 | 13 | 12 | 11        | 10 | 9  | 8  |
| RESERVED |    |    |    | CH_MAP_17 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 7        | 6  | 5  | 4  | 3         | 2  | 1  | 0  |
| RESERVED |    |    |    | CH_MAP_16 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |

**Table 4-811. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG4 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                           |
|-------|-----------|------|-------|---------------------------------------|
| 31:28 | RESERVED  | NONE | 0h    | Reserved                              |
| 27:24 | CH_MAP_19 | R/W  | 0h    | Interrupt Channel Map for intr_in[19] |
| 23:20 | RESERVED  | NONE | 0h    | Reserved                              |
| 19:16 | CH_MAP_18 | R/W  | 0h    | Interrupt Channel Map for intr_in[18] |
| 15:12 | RESERVED  | NONE | 0h    | Reserved                              |
| 11:8  | CH_MAP_17 | R/W  | 0h    | Interrupt Channel Map for intr_in[17] |
| 7:4   | RESERVED  | NONE | 0h    | Reserved                              |
| 3:0   | CH_MAP_16 | R/W  | 0h    | Interrupt Channel Map for intr_in[16] |

#### 4.2.2.66 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG5 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG5 Register (Offset = 414h) [reset = 0h]

Interrupt Channel Map Register for 20 to 20+3

Return to [Summary Table](#)

**Table 4-812. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0414h       |

**Figure 4-260. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG5 Name Register**

| 31       | 30 | 29 | 28 | 27        | 26 | 25 | 24 |
|----------|----|----|----|-----------|----|----|----|
| RESERVED |    |    |    | CH_MAP_23 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 23       | 22 | 21 | 20 | 19        | 18 | 17 | 16 |
| RESERVED |    |    |    | CH_MAP_22 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 15       | 14 | 13 | 12 | 11        | 10 | 9  | 8  |
| RESERVED |    |    |    | CH_MAP_21 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 7        | 6  | 5  | 4  | 3         | 2  | 1  | 0  |
| RESERVED |    |    |    | CH_MAP_20 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |

**Table 4-814. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG5 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                           |
|-------|-----------|------|-------|---------------------------------------|
| 31:28 | RESERVED  | NONE | 0h    | Reserved                              |
| 27:24 | CH_MAP_23 | R/W  | 0h    | Interrupt Channel Map for intr_in[23] |
| 23:20 | RESERVED  | NONE | 0h    | Reserved                              |
| 19:16 | CH_MAP_22 | R/W  | 0h    | Interrupt Channel Map for intr_in[22] |
| 15:12 | RESERVED  | NONE | 0h    | Reserved                              |
| 11:8  | CH_MAP_21 | R/W  | 0h    | Interrupt Channel Map for intr_in[21] |
| 7:4   | RESERVED  | NONE | 0h    | Reserved                              |
| 3:0   | CH_MAP_20 | R/W  | 0h    | Interrupt Channel Map for intr_in[20] |

#### 4.2.2.67 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG6 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG6 Register (Offset = 418h) [reset = 0h]

Interrupt Channel Map Register for 24 to 24+3

Return to [Summary Table](#)

**Table 4-815. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0418h       |

**Figure 4-261. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG6 Name Register**

| 31       | 30 | 29 | 28 | 27        | 26 | 25 | 24 |
|----------|----|----|----|-----------|----|----|----|
| RESERVED |    |    |    | CH_MAP_27 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 23       | 22 | 21 | 20 | 19        | 18 | 17 | 16 |
| RESERVED |    |    |    | CH_MAP_26 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 15       | 14 | 13 | 12 | 11        | 10 | 9  | 8  |
| RESERVED |    |    |    | CH_MAP_25 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 7        | 6  | 5  | 4  | 3         | 2  | 1  | 0  |
| RESERVED |    |    |    | CH_MAP_24 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |

**Table 4-817. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG6 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                           |
|-------|-----------|------|-------|---------------------------------------|
| 31:28 | RESERVED  | NONE | 0h    | Reserved                              |
| 27:24 | CH_MAP_27 | R/W  | 0h    | Interrupt Channel Map for intr_in[27] |
| 23:20 | RESERVED  | NONE | 0h    | Reserved                              |
| 19:16 | CH_MAP_26 | R/W  | 0h    | Interrupt Channel Map for intr_in[26] |
| 15:12 | RESERVED  | NONE | 0h    | Reserved                              |
| 11:8  | CH_MAP_25 | R/W  | 0h    | Interrupt Channel Map for intr_in[25] |
| 7:4   | RESERVED  | NONE | 0h    | Reserved                              |
| 3:0   | CH_MAP_24 | R/W  | 0h    | Interrupt Channel Map for intr_in[24] |

#### 4.2.2.68 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG7 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG7 Register (Offset = 41Ch) [reset = 0h]

Interrupt Channel Map Register for 28 to 28+3

Return to [Summary Table](#)

**Table 4-818. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 041Ch       |

**Figure 4-262. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG7 Name Register**

| 31       | 30 | 29 | 28 | 27        | 26 | 25 | 24 |
|----------|----|----|----|-----------|----|----|----|
| RESERVED |    |    |    | CH_MAP_31 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 23       | 22 | 21 | 20 | 19        | 18 | 17 | 16 |
| RESERVED |    |    |    | CH_MAP_30 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 15       | 14 | 13 | 12 | 11        | 10 | 9  | 8  |
| RESERVED |    |    |    | CH_MAP_29 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 7        | 6  | 5  | 4  | 3         | 2  | 1  | 0  |
| RESERVED |    |    |    | CH_MAP_28 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |

**Table 4-820. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG7 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                           |
|-------|-----------|------|-------|---------------------------------------|
| 31:28 | RESERVED  | NONE | 0h    | Reserved                              |
| 27:24 | CH_MAP_31 | R/W  | 0h    | Interrupt Channel Map for intr_in[31] |
| 23:20 | RESERVED  | NONE | 0h    | Reserved                              |
| 19:16 | CH_MAP_30 | R/W  | 0h    | Interrupt Channel Map for intr_in[30] |
| 15:12 | RESERVED  | NONE | 0h    | Reserved                              |
| 11:8  | CH_MAP_29 | R/W  | 0h    | Interrupt Channel Map for intr_in[29] |
| 7:4   | RESERVED  | NONE | 0h    | Reserved                              |
| 3:0   | CH_MAP_28 | R/W  | 0h    | Interrupt Channel Map for intr_in[28] |

#### 4.2.2.69 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG8 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG8 Register (Offset = 420h) [reset = 0h]

Interrupt Channel Map Register for 32 to 32+3

Return to [Summary Table](#)

**Table 4-821. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0420h       |

**Figure 4-263. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG8 Name Register**

| 31       | 30 | 29 | 28 | 27        | 26 | 25 | 24 |
|----------|----|----|----|-----------|----|----|----|
| RESERVED |    |    |    | CH_MAP_35 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 23       | 22 | 21 | 20 | 19        | 18 | 17 | 16 |
| RESERVED |    |    |    | CH_MAP_34 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 15       | 14 | 13 | 12 | 11        | 10 | 9  | 8  |
| RESERVED |    |    |    | CH_MAP_33 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 7        | 6  | 5  | 4  | 3         | 2  | 1  | 0  |
| RESERVED |    |    |    | CH_MAP_32 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |

**Table 4-823. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG8 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                           |
|-------|-----------|------|-------|---------------------------------------|
| 31:28 | RESERVED  | NONE | 0h    | Reserved                              |
| 27:24 | CH_MAP_35 | R/W  | 0h    | Interrupt Channel Map for intr_in[35] |
| 23:20 | RESERVED  | NONE | 0h    | Reserved                              |
| 19:16 | CH_MAP_34 | R/W  | 0h    | Interrupt Channel Map for intr_in[34] |
| 15:12 | RESERVED  | NONE | 0h    | Reserved                              |
| 11:8  | CH_MAP_33 | R/W  | 0h    | Interrupt Channel Map for intr_in[33] |
| 7:4   | RESERVED  | NONE | 0h    | Reserved                              |
| 3:0   | CH_MAP_32 | R/W  | 0h    | Interrupt Channel Map for intr_in[32] |

#### 4.2.2.70 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG9 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG9 Register (Offset = 424h) [reset = 0h]

Interrupt Channel Map Register for 36 to 36+3

Return to [Summary Table](#)

**Table 4-824. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0424h       |

**Figure 4-264. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG9 Name Register**

| 31       | 30 | 29 | 28 | 27        | 26 | 25 | 24 |
|----------|----|----|----|-----------|----|----|----|
| RESERVED |    |    |    | CH_MAP_39 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 23       | 22 | 21 | 20 | 19        | 18 | 17 | 16 |
| RESERVED |    |    |    | CH_MAP_38 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 15       | 14 | 13 | 12 | 11        | 10 | 9  | 8  |
| RESERVED |    |    |    | CH_MAP_37 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 7        | 6  | 5  | 4  | 3         | 2  | 1  | 0  |
| RESERVED |    |    |    | CH_MAP_36 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |

**Table 4-826. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG9 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                           |
|-------|-----------|------|-------|---------------------------------------|
| 31:28 | RESERVED  | NONE | 0h    | Reserved                              |
| 27:24 | CH_MAP_39 | R/W  | 0h    | Interrupt Channel Map for intr_in[39] |
| 23:20 | RESERVED  | NONE | 0h    | Reserved                              |
| 19:16 | CH_MAP_38 | R/W  | 0h    | Interrupt Channel Map for intr_in[38] |
| 15:12 | RESERVED  | NONE | 0h    | Reserved                              |
| 11:8  | CH_MAP_37 | R/W  | 0h    | Interrupt Channel Map for intr_in[37] |
| 7:4   | RESERVED  | NONE | 0h    | Reserved                              |
| 3:0   | CH_MAP_36 | R/W  | 0h    | Interrupt Channel Map for intr_in[36] |

#### 4.2.2.71 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG10 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG10 Register (Offset = 428h) [reset = 0h]

Interrupt Channel Map Register for 40 to 40+3

Return to [Summary Table](#)

**Table 4-827. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0428h       |

**Figure 4-265. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG10 Name Register**

|          |    |    |    |           |    |    |    |
|----------|----|----|----|-----------|----|----|----|
| 31       | 30 | 29 | 28 | 27        | 26 | 25 | 24 |
| RESERVED |    |    |    | CH_MAP_43 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 23       | 22 | 21 | 20 | 19        | 18 | 17 | 16 |
| RESERVED |    |    |    | CH_MAP_42 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 15       | 14 | 13 | 12 | 11        | 10 | 9  | 8  |
| RESERVED |    |    |    | CH_MAP_41 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 7        | 6  | 5  | 4  | 3         | 2  | 1  | 0  |
| RESERVED |    |    |    | CH_MAP_40 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |

**Table 4-829. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG10 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                           |
|-------|-----------|------|-------|---------------------------------------|
| 31:28 | RESERVED  | NONE | 0h    | Reserved                              |
| 27:24 | CH_MAP_43 | R/W  | 0h    | Interrupt Channel Map for intr_in[43] |
| 23:20 | RESERVED  | NONE | 0h    | Reserved                              |
| 19:16 | CH_MAP_42 | R/W  | 0h    | Interrupt Channel Map for intr_in[42] |
| 15:12 | RESERVED  | NONE | 0h    | Reserved                              |
| 11:8  | CH_MAP_41 | R/W  | 0h    | Interrupt Channel Map for intr_in[41] |
| 7:4   | RESERVED  | NONE | 0h    | Reserved                              |
| 3:0   | CH_MAP_40 | R/W  | 0h    | Interrupt Channel Map for intr_in[40] |

#### 4.2.2.72 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG11 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG11 Register (Offset = 42Ch) [reset = 0h]

Interrupt Channel Map Register for 44 to 44+3

Return to [Summary Table](#)

**Table 4-830. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 042Ch       |

**Figure 4-266. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG11 Name Register**

| 31       | 30 | 29 | 28 | 27        | 26 | 25 | 24 |
|----------|----|----|----|-----------|----|----|----|
| RESERVED |    |    |    | CH_MAP_47 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 23       | 22 | 21 | 20 | 19        | 18 | 17 | 16 |
| RESERVED |    |    |    | CH_MAP_46 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 15       | 14 | 13 | 12 | 11        | 10 | 9  | 8  |
| RESERVED |    |    |    | CH_MAP_45 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 7        | 6  | 5  | 4  | 3         | 2  | 1  | 0  |
| RESERVED |    |    |    | CH_MAP_44 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |

**Table 4-832. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG11 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                           |
|-------|-----------|------|-------|---------------------------------------|
| 31:28 | RESERVED  | NONE | 0h    | Reserved                              |
| 27:24 | CH_MAP_47 | R/W  | 0h    | Interrupt Channel Map for intr_in[47] |
| 23:20 | RESERVED  | NONE | 0h    | Reserved                              |
| 19:16 | CH_MAP_46 | R/W  | 0h    | Interrupt Channel Map for intr_in[46] |
| 15:12 | RESERVED  | NONE | 0h    | Reserved                              |
| 11:8  | CH_MAP_45 | R/W  | 0h    | Interrupt Channel Map for intr_in[45] |
| 7:4   | RESERVED  | NONE | 0h    | Reserved                              |
| 3:0   | CH_MAP_44 | R/W  | 0h    | Interrupt Channel Map for intr_in[44] |



#### 4.2.2.73 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG12 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG12 Register (Offset = 430h) [reset = 0h]

Interrupt Channel Map Register for 48 to 48+3

Return to [Summary Table](#)

**Table 4-833. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0430h       |

**Figure 4-267. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG12 Name Register**

| 31       | 30 | 29 | 28 | 27        | 26 | 25 | 24 |
|----------|----|----|----|-----------|----|----|----|
| RESERVED |    |    |    | CH_MAP_51 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 23       | 22 | 21 | 20 | 19        | 18 | 17 | 16 |
| RESERVED |    |    |    | CH_MAP_50 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 15       | 14 | 13 | 12 | 11        | 10 | 9  | 8  |
| RESERVED |    |    |    | CH_MAP_49 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 7        | 6  | 5  | 4  | 3         | 2  | 1  | 0  |
| RESERVED |    |    |    | CH_MAP_48 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |

**Table 4-835. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG12 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                           |
|-------|-----------|------|-------|---------------------------------------|
| 31:28 | RESERVED  | NONE | 0h    | Reserved                              |
| 27:24 | CH_MAP_51 | R/W  | 0h    | Interrupt Channel Map for intr_in[51] |
| 23:20 | RESERVED  | NONE | 0h    | Reserved                              |
| 19:16 | CH_MAP_50 | R/W  | 0h    | Interrupt Channel Map for intr_in[50] |
| 15:12 | RESERVED  | NONE | 0h    | Reserved                              |
| 11:8  | CH_MAP_49 | R/W  | 0h    | Interrupt Channel Map for intr_in[49] |
| 7:4   | RESERVED  | NONE | 0h    | Reserved                              |
| 3:0   | CH_MAP_48 | R/W  | 0h    | Interrupt Channel Map for intr_in[48] |

#### 4.2.2.74 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG13 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG13 Register (Offset = 434h) [reset = 0h]

Interrupt Channel Map Register for 52 to 52+3

Return to [Summary Table](#)

**Table 4-836. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0434h       |

**Figure 4-268. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG13 Name Register**

| 31       | 30 | 29 | 28 | 27        | 26 | 25 | 24 |
|----------|----|----|----|-----------|----|----|----|
| RESERVED |    |    |    | CH_MAP_55 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 23       | 22 | 21 | 20 | 19        | 18 | 17 | 16 |
| RESERVED |    |    |    | CH_MAP_54 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 15       | 14 | 13 | 12 | 11        | 10 | 9  | 8  |
| RESERVED |    |    |    | CH_MAP_53 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 7        | 6  | 5  | 4  | 3         | 2  | 1  | 0  |
| RESERVED |    |    |    | CH_MAP_52 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |

**Table 4-838. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG13 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                           |
|-------|-----------|------|-------|---------------------------------------|
| 31:28 | RESERVED  | NONE | 0h    | Reserved                              |
| 27:24 | CH_MAP_55 | R/W  | 0h    | Interrupt Channel Map for intr_in[55] |
| 23:20 | RESERVED  | NONE | 0h    | Reserved                              |
| 19:16 | CH_MAP_54 | R/W  | 0h    | Interrupt Channel Map for intr_in[54] |
| 15:12 | RESERVED  | NONE | 0h    | Reserved                              |
| 11:8  | CH_MAP_53 | R/W  | 0h    | Interrupt Channel Map for intr_in[53] |
| 7:4   | RESERVED  | NONE | 0h    | Reserved                              |
| 3:0   | CH_MAP_52 | R/W  | 0h    | Interrupt Channel Map for intr_in[52] |

#### 4.2.2.75 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG14 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG14 Register (Offset = 438h) [reset = 0h]

Interrupt Channel Map Register for 56 to 56+3

Return to [Summary Table](#)

**Table 4-839. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0438h       |

**Figure 4-269. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG14 Name Register**

| 31       | 30 | 29 | 28 | 27        | 26 | 25 | 24 |
|----------|----|----|----|-----------|----|----|----|
| RESERVED |    |    |    | CH_MAP_59 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 23       | 22 | 21 | 20 | 19        | 18 | 17 | 16 |
| RESERVED |    |    |    | CH_MAP_58 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 15       | 14 | 13 | 12 | 11        | 10 | 9  | 8  |
| RESERVED |    |    |    | CH_MAP_57 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 7        | 6  | 5  | 4  | 3         | 2  | 1  | 0  |
| RESERVED |    |    |    | CH_MAP_56 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |

**Table 4-841. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG14 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                           |
|-------|-----------|------|-------|---------------------------------------|
| 31:28 | RESERVED  | NONE | 0h    | Reserved                              |
| 27:24 | CH_MAP_59 | R/W  | 0h    | Interrupt Channel Map for intr_in[59] |
| 23:20 | RESERVED  | NONE | 0h    | Reserved                              |
| 19:16 | CH_MAP_58 | R/W  | 0h    | Interrupt Channel Map for intr_in[58] |
| 15:12 | RESERVED  | NONE | 0h    | Reserved                              |
| 11:8  | CH_MAP_57 | R/W  | 0h    | Interrupt Channel Map for intr_in[57] |
| 7:4   | RESERVED  | NONE | 0h    | Reserved                              |
| 3:0   | CH_MAP_56 | R/W  | 0h    | Interrupt Channel Map for intr_in[56] |

#### 4.2.2.76 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG15 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG15 Register (Offset = 43Ch) [reset = 0h]

Interrupt Channel Map Register for 60 to 60+3

Return to [Summary Table](#)

**Table 4-842. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 043Ch       |

**Figure 4-270. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG15 Name Register**

| 31       | 30 | 29 | 28 | 27        | 26 | 25 | 24 |
|----------|----|----|----|-----------|----|----|----|
| RESERVED |    |    |    | CH_MAP_63 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 23       | 22 | 21 | 20 | 19        | 18 | 17 | 16 |
| RESERVED |    |    |    | CH_MAP_62 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 15       | 14 | 13 | 12 | 11        | 10 | 9  | 8  |
| RESERVED |    |    |    | CH_MAP_61 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |
| 7        | 6  | 5  | 4  | 3         | 2  | 1  | 0  |
| RESERVED |    |    |    | CH_MAP_60 |    |    |    |
| NONE     |    |    |    | R/W       |    |    |    |
| 0h       |    |    |    | 0h        |    |    |    |

**Table 4-844. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_CH\_MAP\_REG15 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                           |
|-------|-----------|------|-------|---------------------------------------|
| 31:28 | RESERVED  | NONE | 0h    | Reserved                              |
| 27:24 | CH_MAP_63 | R/W  | 0h    | Interrupt Channel Map for intr_in[63] |
| 23:20 | RESERVED  | NONE | 0h    | Reserved                              |
| 19:16 | CH_MAP_62 | R/W  | 0h    | Interrupt Channel Map for intr_in[62] |
| 15:12 | RESERVED  | NONE | 0h    | Reserved                              |
| 11:8  | CH_MAP_61 | R/W  | 0h    | Interrupt Channel Map for intr_in[61] |
| 7:4   | RESERVED  | NONE | 0h    | Reserved                              |
| 3:0   | CH_MAP_60 | R/W  | 0h    | Interrupt Channel Map for intr_in[60] |

#### 4.2.2.77 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_HINT\_MAP\_REG0 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_HINT\_MAP\_REG0 Register (Offset = 800h) [reset = 0h]

Host Interrupt Map Register for 0 to 0+3

Return to [Summary Table](#)

**Table 4-845. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0800h       |

**Figure 4-271. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_HINT\_MAP\_REG0 Name Register**

| 31       | 30 | 29 | 28 | 27         | 26 | 25 | 24 |
|----------|----|----|----|------------|----|----|----|
| RESERVED |    |    |    | HINT_MAP_3 |    |    |    |
| NONE     |    |    |    | R/W        |    |    |    |
| 0h       |    |    |    | 0h         |    |    |    |
| 23       | 22 | 21 | 20 | 19         | 18 | 17 | 16 |
| RESERVED |    |    |    | HINT_MAP_2 |    |    |    |
| NONE     |    |    |    | R/W        |    |    |    |
| 0h       |    |    |    | 0h         |    |    |    |
| 15       | 14 | 13 | 12 | 11         | 10 | 9  | 8  |
| RESERVED |    |    |    | HINT_MAP_1 |    |    |    |
| NONE     |    |    |    | R/W        |    |    |    |
| 0h       |    |    |    | 0h         |    |    |    |
| 7        | 6  | 5  | 4  | 3          | 2  | 1  | 0  |
| RESERVED |    |    |    | HINT_MAP_0 |    |    |    |
| NONE     |    |    |    | R/W        |    |    |    |
| 0h       |    |    |    | 0h         |    |    |    |

**Table 4-847. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_HINT\_MAP\_REG0 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                      |
|-------|------------|------|-------|----------------------------------|
| 31:28 | RESERVED   | NONE | 0h    | Reserved                         |
| 27:24 | HINT_MAP_3 | R/W  | 0h    | Host Interrupt Map for Channel 3 |
| 23:20 | RESERVED   | NONE | 0h    | Reserved                         |
| 19:16 | HINT_MAP_2 | R/W  | 0h    | Host Interrupt Map for Channel 2 |
| 15:12 | RESERVED   | NONE | 0h    | Reserved                         |
| 11:8  | HINT_MAP_1 | R/W  | 0h    | Host Interrupt Map for Channel 1 |
| 7:4   | RESERVED   | NONE | 0h    | Reserved                         |
| 3:0   | HINT_MAP_0 | R/W  | 0h    | Host Interrupt Map for Channel 0 |

#### 4.2.2.78 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_HINT\_MAP\_REG1 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_HINT\_MAP\_REG1 Register (Offset = 804h) [reset = 0h]

Host Interrupt Map Register for 4 to 4+3

Return to [Summary Table](#)

**Table 4-848. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0804h       |

**Figure 4-272. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_HINT\_MAP\_REG1 Name Register**

| 31       | 30 | 29 | 28 | 27         | 26 | 25 | 24 |
|----------|----|----|----|------------|----|----|----|
| RESERVED |    |    |    | HINT_MAP_7 |    |    |    |
| NONE     |    |    |    | R/W        |    |    |    |
| 0h       |    |    |    | 0h         |    |    |    |
| 23       | 22 | 21 | 20 | 19         | 18 | 17 | 16 |
| RESERVED |    |    |    | HINT_MAP_6 |    |    |    |
| NONE     |    |    |    | R/W        |    |    |    |
| 0h       |    |    |    | 0h         |    |    |    |
| 15       | 14 | 13 | 12 | 11         | 10 | 9  | 8  |
| RESERVED |    |    |    | HINT_MAP_5 |    |    |    |
| NONE     |    |    |    | R/W        |    |    |    |
| 0h       |    |    |    | 0h         |    |    |    |
| 7        | 6  | 5  | 4  | 3          | 2  | 1  | 0  |
| RESERVED |    |    |    | HINT_MAP_4 |    |    |    |
| NONE     |    |    |    | R/W        |    |    |    |
| 0h       |    |    |    | 0h         |    |    |    |

**Table 4-850. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_HINT\_MAP\_REG1 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                      |
|-------|------------|------|-------|----------------------------------|
| 31:28 | RESERVED   | NONE | 0h    | Reserved                         |
| 27:24 | HINT_MAP_7 | R/W  | 0h    | Host Interrupt Map for Channel 7 |
| 23:20 | RESERVED   | NONE | 0h    | Reserved                         |
| 19:16 | HINT_MAP_6 | R/W  | 0h    | Host Interrupt Map for Channel 6 |
| 15:12 | RESERVED   | NONE | 0h    | Reserved                         |
| 11:8  | HINT_MAP_5 | R/W  | 0h    | Host Interrupt Map for Channel 5 |
| 7:4   | RESERVED   | NONE | 0h    | Reserved                         |
| 3:0   | HINT_MAP_4 | R/W  | 0h    | Host Interrupt Map for Channel 4 |

#### 4.2.2.79 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_HINT\_MAP\_REG2 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_HINT\_MAP\_REG2 Register (Offset = 808h) [reset = 0h]

Host Interrupt Map Register for 8 to 8+3

Return to [Summary Table](#)

**Table 4-851. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0808h       |

**Figure 4-273. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_HINT\_MAP\_REG2 Name Register**

|          |    |    |    |            |    |    |    |
|----------|----|----|----|------------|----|----|----|
| 31       | 30 | 29 | 28 | 27         | 26 | 25 | 24 |
| RESERVED |    |    |    |            |    |    |    |
| NONE     |    |    |    |            |    |    |    |
| 0h       |    |    |    |            |    |    |    |
| 23       | 22 | 21 | 20 | 19         | 18 | 17 | 16 |
| RESERVED |    |    |    |            |    |    |    |
| NONE     |    |    |    |            |    |    |    |
| 0h       |    |    |    |            |    |    |    |
| 15       | 14 | 13 | 12 | 11         | 10 | 9  | 8  |
| RESERVED |    |    |    | HINT_MAP_9 |    |    |    |
| NONE     |    |    |    | R/W        |    |    |    |
| 0h       |    |    |    | 0h         |    |    |    |
| 7        | 6  | 5  | 4  | 3          | 2  | 1  | 0  |
| RESERVED |    |    |    | HINT_MAP_8 |    |    |    |
| NONE     |    |    |    | R/W        |    |    |    |
| 0h       |    |    |    | 0h         |    |    |    |

**Table 4-853. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_HINT\_MAP\_REG2 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                      |
|-------|------------|------|-------|----------------------------------|
| 31:12 | RESERVED   | NONE | 0h    | Reserved                         |
| 11:8  | HINT_MAP_9 | R/W  | 0h    | Host Interrupt Map for Channel 9 |
| 7:4   | RESERVED   | NONE | 0h    | Reserved                         |
| 3:0   | HINT_MAP_8 | R/W  | 0h    | Host Interrupt Map for Channel 8 |

#### 4.2.2.80 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG0 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG0 Register (Offset = 900h) [reset = 80000000h]

Host Int 0 Prioritized Interrupt Register

Return to [Summary Table](#)

**Table 4-854. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0900h       |

**Figure 4-274. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG0 Name Register**

|             |          |    |    |    |    |            |    |
|-------------|----------|----|----|----|----|------------|----|
| 31          | 30       | 29 | 28 | 27 | 26 | 25         | 24 |
| NONE_HINT_0 | RESERVED |    |    |    |    |            |    |
| R           | NONE     |    |    |    |    |            |    |
| 1h          | 0h       |    |    |    |    |            |    |
| 23          | 22       | 21 | 20 | 19 | 18 | 17         | 16 |
| RESERVED    |          |    |    |    |    |            |    |
| NONE        |          |    |    |    |    |            |    |
| 0h          |          |    |    |    |    |            |    |
| 15          | 14       | 13 | 12 | 11 | 10 | 9          | 8  |
| RESERVED    |          |    |    |    |    | PRI_HINT_0 |    |
| NONE        |          |    |    |    |    | R          |    |
| 0h          |          |    |    |    |    | 0h         |    |
| 7           | 6        | 5  | 4  | 3  | 2  | 1          | 0  |
| PRI_HINT_0  |          |    |    |    |    |            |    |
| R           |          |    |    |    |    |            |    |
| 0h          |          |    |    |    |    |            |    |

**Table 4-856. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG0 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                      |
|-------|-------------|------|-------|----------------------------------|
| 31    | NONE_HINT_0 | R    | 1h    | No interrupt pending flag        |
| 30:10 | RESERVED    | NONE | 0h    | Reserved                         |
| 9:0   | PRI_HINT_0  | R    | 0h    | Host Int 0 Prioritized Interrupt |



#### 4.2.2.81 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG1 Register

#### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG1 Register (Offset = 904h) [reset = 80000000h]

Host Int 1 Prioritized Interrupt Register

Return to [Summary Table](#)

**Table 4-857. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0904h       |

**Figure 4-275. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG1 Name Register**

|             |          |    |    |    |    |            |    |
|-------------|----------|----|----|----|----|------------|----|
| 31          | 30       | 29 | 28 | 27 | 26 | 25         | 24 |
| NONE_HINT_1 | RESERVED |    |    |    |    |            |    |
| R           | NONE     |    |    |    |    |            |    |
| 1h          | 0h       |    |    |    |    |            |    |
| 23          | 22       | 21 | 20 | 19 | 18 | 17         | 16 |
| RESERVED    |          |    |    |    |    |            |    |
| NONE        |          |    |    |    |    |            |    |
| 0h          |          |    |    |    |    |            |    |
| 15          | 14       | 13 | 12 | 11 | 10 | 9          | 8  |
| RESERVED    |          |    |    |    |    | PRI_HINT_1 |    |
| NONE        |          |    |    |    |    | R          |    |
| 0h          |          |    |    |    |    | 0h         |    |
| 7           | 6        | 5  | 4  | 3  | 2  | 1          | 0  |
| PRI_HINT_1  |          |    |    |    |    |            |    |
| R           |          |    |    |    |    |            |    |
| 0h          |          |    |    |    |    |            |    |

**Table 4-859. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG1 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                      |
|-------|-------------|------|-------|----------------------------------|
| 31    | NONE_HINT_1 | R    | 1h    | No interrupt pending flag        |
| 30:10 | RESERVED    | NONE | 0h    | Reserved                         |
| 9:0   | PRI_HINT_1  | R    | 0h    | Host Int 1 Prioritized Interrupt |

#### 4.2.2.82 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG2 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG2 Register (Offset = 908h) [reset = 80000000h]

Host Int 2 Prioritized Interrupt Register

Return to [Summary Table](#)

**Table 4-860. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0908h       |

**Figure 4-276. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG2 Name Register**

|             |          |    |    |    |    |            |    |
|-------------|----------|----|----|----|----|------------|----|
| 31          | 30       | 29 | 28 | 27 | 26 | 25         | 24 |
| NONE_HINT_2 | RESERVED |    |    |    |    |            |    |
| R           | NONE     |    |    |    |    |            |    |
| 1h          | 0h       |    |    |    |    |            |    |
| 23          | 22       | 21 | 20 | 19 | 18 | 17         | 16 |
| RESERVED    |          |    |    |    |    |            |    |
| NONE        |          |    |    |    |    |            |    |
| 0h          |          |    |    |    |    |            |    |
| 15          | 14       | 13 | 12 | 11 | 10 | 9          | 8  |
| RESERVED    |          |    |    |    |    | PRI_HINT_2 |    |
| NONE        |          |    |    |    |    | R          |    |
| 0h          |          |    |    |    |    | 0h         |    |
| 7           | 6        | 5  | 4  | 3  | 2  | 1          | 0  |
| PRI_HINT_2  |          |    |    |    |    |            |    |
| R           |          |    |    |    |    |            |    |
| 0h          |          |    |    |    |    |            |    |

**Table 4-862. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG2 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                      |
|-------|-------------|------|-------|----------------------------------|
| 31    | NONE_HINT_2 | R    | 1h    | No interrupt pending flag        |
| 30:10 | RESERVED    | NONE | 0h    | Reserved                         |
| 9:0   | PRI_HINT_2  | R    | 0h    | Host Int 2 Prioritized Interrupt |

#### 4.2.2.83 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG3 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG3 Register (Offset = 90Ch) [reset = 80000000h]

Host Int 3 Prioritized Interrupt Register

Return to [Summary Table](#)

**Table 4-863. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 090Ch       |

**Figure 4-277. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG3 Name Register**

|             |          |    |    |    |    |            |    |
|-------------|----------|----|----|----|----|------------|----|
| 31          | 30       | 29 | 28 | 27 | 26 | 25         | 24 |
| NONE_HINT_3 | RESERVED |    |    |    |    |            |    |
| R           | NONE     |    |    |    |    |            |    |
| 1h          | 0h       |    |    |    |    |            |    |
| 23          | 22       | 21 | 20 | 19 | 18 | 17         | 16 |
| RESERVED    |          |    |    |    |    |            |    |
| NONE        |          |    |    |    |    |            |    |
| 0h          |          |    |    |    |    |            |    |
| 15          | 14       | 13 | 12 | 11 | 10 | 9          | 8  |
| RESERVED    |          |    |    |    |    | PRI_HINT_3 |    |
| NONE        |          |    |    |    |    | R          |    |
| 0h          |          |    |    |    |    | 0h         |    |
| 7           | 6        | 5  | 4  | 3  | 2  | 1          | 0  |
| PRI_HINT_3  |          |    |    |    |    |            |    |
| R           |          |    |    |    |    |            |    |
| 0h          |          |    |    |    |    |            |    |

**Table 4-865. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG3 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                      |
|-------|-------------|------|-------|----------------------------------|
| 31    | NONE_HINT_3 | R    | 1h    | No interrupt pending flag        |
| 30:10 | RESERVED    | NONE | 0h    | Reserved                         |
| 9:0   | PRI_HINT_3  | R    | 0h    | Host Int 3 Prioritized Interrupt |

#### 4.2.2.84 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG4 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG4 Register (Offset = 910h) [reset = 80000000h]

Host Int 4 Prioritized Interrupt Register

Return to [Summary Table](#)

**Table 4-866. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0910h       |

**Figure 4-278. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG4 Name Register**

|             |          |    |    |    |    |            |    |
|-------------|----------|----|----|----|----|------------|----|
| 31          | 30       | 29 | 28 | 27 | 26 | 25         | 24 |
| NONE_HINT_4 | RESERVED |    |    |    |    |            |    |
| R           | NONE     |    |    |    |    |            |    |
| 1h          | 0h       |    |    |    |    |            |    |
| 23          | 22       | 21 | 20 | 19 | 18 | 17         | 16 |
| RESERVED    |          |    |    |    |    |            |    |
| NONE        |          |    |    |    |    |            |    |
| 0h          |          |    |    |    |    |            |    |
| 15          | 14       | 13 | 12 | 11 | 10 | 9          | 8  |
| RESERVED    |          |    |    |    |    | PRI_HINT_4 |    |
| NONE        |          |    |    |    |    | R          |    |
| 0h          |          |    |    |    |    | 0h         |    |
| 7           | 6        | 5  | 4  | 3  | 2  | 1          | 0  |
| PRI_HINT_4  |          |    |    |    |    |            |    |
| R           |          |    |    |    |    |            |    |
| 0h          |          |    |    |    |    |            |    |

**Table 4-868. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG4 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                      |
|-------|-------------|------|-------|----------------------------------|
| 31    | NONE_HINT_4 | R    | 1h    | No interrupt pending flag        |
| 30:10 | RESERVED    | NONE | 0h    | Reserved                         |
| 9:0   | PRI_HINT_4  | R    | 0h    | Host Int 4 Prioritized Interrupt |

#### 4.2.2.85 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG5 Register

#### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG5 Register (Offset = 914h) [reset = 80000000h]

Host Int 5 Prioritized Interrupt Register

Return to [Summary Table](#)

**Table 4-869. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0914h       |

**Figure 4-279. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG5 Name Register**

|             |          |    |    |    |    |            |    |
|-------------|----------|----|----|----|----|------------|----|
| 31          | 30       | 29 | 28 | 27 | 26 | 25         | 24 |
| NONE_HINT_5 | RESERVED |    |    |    |    |            |    |
| R           | NONE     |    |    |    |    |            |    |
| 1h          | 0h       |    |    |    |    |            |    |
| 23          | 22       | 21 | 20 | 19 | 18 | 17         | 16 |
| RESERVED    |          |    |    |    |    |            |    |
| NONE        |          |    |    |    |    |            |    |
| 0h          |          |    |    |    |    |            |    |
| 15          | 14       | 13 | 12 | 11 | 10 | 9          | 8  |
| RESERVED    |          |    |    |    |    | PRI_HINT_5 |    |
| NONE        |          |    |    |    |    | R          |    |
| 0h          |          |    |    |    |    | 0h         |    |
| 7           | 6        | 5  | 4  | 3  | 2  | 1          | 0  |
| PRI_HINT_5  |          |    |    |    |    |            |    |
| R           |          |    |    |    |    |            |    |
| 0h          |          |    |    |    |    |            |    |

**Table 4-871. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG5 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                      |
|-------|-------------|------|-------|----------------------------------|
| 31    | NONE_HINT_5 | R    | 1h    | No interrupt pending flag        |
| 30:10 | RESERVED    | NONE | 0h    | Reserved                         |
| 9:0   | PRI_HINT_5  | R    | 0h    | Host Int 5 Prioritized Interrupt |

#### 4.2.2.86 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG6 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG6 Register (Offset = 918h) [reset = 80000000h]

Host Int 6 Prioritized Interrupt Register

Return to [Summary Table](#)

**Table 4-872. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0918h       |

**Figure 4-280. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG6 Name Register**

|             |          |    |    |    |    |            |    |
|-------------|----------|----|----|----|----|------------|----|
| 31          | 30       | 29 | 28 | 27 | 26 | 25         | 24 |
| NONE_HINT_6 | RESERVED |    |    |    |    |            |    |
| R           | NONE     |    |    |    |    |            |    |
| 1h          | 0h       |    |    |    |    |            |    |
| 23          | 22       | 21 | 20 | 19 | 18 | 17         | 16 |
| RESERVED    |          |    |    |    |    |            |    |
| NONE        |          |    |    |    |    |            |    |
| 0h          |          |    |    |    |    |            |    |
| 15          | 14       | 13 | 12 | 11 | 10 | 9          | 8  |
| RESERVED    |          |    |    |    |    | PRI_HINT_6 |    |
| NONE        |          |    |    |    |    | R          |    |
| 0h          |          |    |    |    |    | 0h         |    |
| 7           | 6        | 5  | 4  | 3  | 2  | 1          | 0  |
| PRI_HINT_6  |          |    |    |    |    |            |    |
| R           |          |    |    |    |    |            |    |
| 0h          |          |    |    |    |    |            |    |

**Table 4-874. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG6 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                      |
|-------|-------------|------|-------|----------------------------------|
| 31    | NONE_HINT_6 | R    | 1h    | No interrupt pending flag        |
| 30:10 | RESERVED    | NONE | 0h    | Reserved                         |
| 9:0   | PRI_HINT_6  | R    | 0h    | Host Int 6 Prioritized Interrupt |

#### 4.2.2.87 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG7 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG7 Register (Offset = 91Ch) [reset = 80000000h]

Host Int 7 Prioritized Interrupt Register

Return to [Summary Table](#)

**Table 4-875. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 091Ch       |

**Figure 4-281. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG7 Name Register**

|             |          |    |    |    |    |            |    |
|-------------|----------|----|----|----|----|------------|----|
| 31          | 30       | 29 | 28 | 27 | 26 | 25         | 24 |
| NONE_HINT_7 | RESERVED |    |    |    |    |            |    |
| R           | NONE     |    |    |    |    |            |    |
| 1h          | 0h       |    |    |    |    |            |    |
| 23          | 22       | 21 | 20 | 19 | 18 | 17         | 16 |
| RESERVED    |          |    |    |    |    |            |    |
| NONE        |          |    |    |    |    |            |    |
| 0h          |          |    |    |    |    |            |    |
| 15          | 14       | 13 | 12 | 11 | 10 | 9          | 8  |
| RESERVED    |          |    |    |    |    | PRI_HINT_7 |    |
| NONE        |          |    |    |    |    | R          |    |
| 0h          |          |    |    |    |    | 0h         |    |
| 7           | 6        | 5  | 4  | 3  | 2  | 1          | 0  |
| PRI_HINT_7  |          |    |    |    |    |            |    |
| R           |          |    |    |    |    |            |    |
| 0h          |          |    |    |    |    |            |    |

**Table 4-877. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG7 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                      |
|-------|-------------|------|-------|----------------------------------|
| 31    | NONE_HINT_7 | R    | 1h    | No interrupt pending flag        |
| 30:10 | RESERVED    | NONE | 0h    | Reserved                         |
| 9:0   | PRI_HINT_7  | R    | 0h    | Host Int 7 Prioritized Interrupt |

#### 4.2.2.88 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG8 Register

#### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG8 Register (Offset = 920h) [reset = 80000000h]

Host Int 8 Prioritized Interrupt Register

Return to [Summary Table](#)

**Table 4-878. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0920h       |

**Figure 4-282. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG8 Name Register**

|             |          |    |    |    |    |            |    |
|-------------|----------|----|----|----|----|------------|----|
| 31          | 30       | 29 | 28 | 27 | 26 | 25         | 24 |
| NONE_HINT_8 | RESERVED |    |    |    |    |            |    |
| R           | NONE     |    |    |    |    |            |    |
| 1h          | 0h       |    |    |    |    |            |    |
| 23          | 22       | 21 | 20 | 19 | 18 | 17         | 16 |
| RESERVED    |          |    |    |    |    |            |    |
| NONE        |          |    |    |    |    |            |    |
| 0h          |          |    |    |    |    |            |    |
| 15          | 14       | 13 | 12 | 11 | 10 | 9          | 8  |
| RESERVED    |          |    |    |    |    | PRI_HINT_8 |    |
| NONE        |          |    |    |    |    | R          |    |
| 0h          |          |    |    |    |    | 0h         |    |
| 7           | 6        | 5  | 4  | 3  | 2  | 1          | 0  |
| PRI_HINT_8  |          |    |    |    |    |            |    |
| R           |          |    |    |    |    |            |    |
| 0h          |          |    |    |    |    |            |    |

**Table 4-880. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG8 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                      |
|-------|-------------|------|-------|----------------------------------|
| 31    | NONE_HINT_8 | R    | 1h    | No interrupt pending flag        |
| 30:10 | RESERVED    | NONE | 0h    | Reserved                         |
| 9:0   | PRI_HINT_8  | R    | 0h    | Host Int 8 Prioritized Interrupt |



#### 4.2.2.89 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG9 Register

#### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG9 Register (Offset = 924h) [reset = 80000000h]

Host Int 9 Prioritized Interrupt Register

Return to [Summary Table](#)

**Table 4-881. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0924h       |

**Figure 4-283. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG9 Name Register**

|             |          |    |    |    |    |            |    |
|-------------|----------|----|----|----|----|------------|----|
| 31          | 30       | 29 | 28 | 27 | 26 | 25         | 24 |
| NONE_HINT_9 | RESERVED |    |    |    |    |            |    |
| R           | NONE     |    |    |    |    |            |    |
| 1h          | 0h       |    |    |    |    |            |    |
| 23          | 22       | 21 | 20 | 19 | 18 | 17         | 16 |
| RESERVED    |          |    |    |    |    |            |    |
| NONE        |          |    |    |    |    |            |    |
| 0h          |          |    |    |    |    |            |    |
| 15          | 14       | 13 | 12 | 11 | 10 | 9          | 8  |
| RESERVED    |          |    |    |    |    | PRI_HINT_9 |    |
| NONE        |          |    |    |    |    | R          |    |
| 0h          |          |    |    |    |    | 0h         |    |
| 7           | 6        | 5  | 4  | 3  | 2  | 1          | 0  |
| PRI_HINT_9  |          |    |    |    |    |            |    |
| R           |          |    |    |    |    |            |    |
| 0h          |          |    |    |    |    |            |    |

**Table 4-883. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_PRI\_HINT\_REG9 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                      |
|-------|-------------|------|-------|----------------------------------|
| 31    | NONE_HINT_9 | R    | 1h    | No interrupt pending flag        |
| 30:10 | RESERVED    | NONE | 0h    | Reserved                         |
| 9:0   | PRI_HINT_9  | R    | 0h    | Host Int 9 Prioritized Interrupt |

#### 4.2.2.90 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_POLARITY\_REG0 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_POLARITY\_REG0 Register (Offset = D00h) [reset = FFFFFFFFh]

Polarity Register 0

Return to [Summary Table](#)

**Table 4-884. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0D00h       |

**Figure 4-284. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_POLARITY\_REG0 Name Register**

| 31          | 30          | 29          | 28          | 27          | 26          | 25          | 24          |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| POLARITY_31 | POLARITY_30 | POLARITY_29 | POLARITY_28 | POLARITY_27 | POLARITY_26 | POLARITY_25 | POLARITY_24 |
| R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         |
| 1h          | 1h          | 1h          | 1h          | 1h          | 1h          | 1h          | 1h          |
| 23          | 22          | 21          | 20          | 19          | 18          | 17          | 16          |
| POLARITY_23 | POLARITY_22 | POLARITY_21 | POLARITY_20 | POLARITY_19 | POLARITY_18 | POLARITY_17 | POLARITY_16 |
| R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         |
| 1h          | 1h          | 1h          | 1h          | 1h          | 1h          | 1h          | 1h          |
| 15          | 14          | 13          | 12          | 11          | 10          | 9           | 8           |
| POLARITY_15 | POLARITY_14 | POLARITY_13 | POLARITY_12 | POLARITY_11 | POLARITY_10 | POLARITY_9  | POLARITY_8  |
| R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         |
| 1h          | 1h          | 1h          | 1h          | 1h          | 1h          | 1h          | 1h          |
| 7           | 6           | 5           | 4           | 3           | 2           | 1           | 0           |
| POLARITY_7  | POLARITY_6  | POLARITY_5  | POLARITY_4  | POLARITY_3  | POLARITY_2  | POLARITY_1  | POLARITY_0  |
| R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         |
| 1h          | 1h          | 1h          | 1h          | 1h          | 1h          | 1h          | 1h          |

**Table 4-886. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_POLARITY\_REG0 Register Field Descriptions**

| Bit | Field       | Type | Reset | Description                    |
|-----|-------------|------|-------|--------------------------------|
| 31  | POLARITY_31 | R/W  | 1h    | Polarity for intr_in[31] 0=low |
| 30  | POLARITY_30 | R/W  | 1h    | Polarity for intr_in[30] 0=low |
| 29  | POLARITY_29 | R/W  | 1h    | Polarity for intr_in[29] 0=low |
| 28  | POLARITY_28 | R/W  | 1h    | Polarity for intr_in[28] 0=low |
| 27  | POLARITY_27 | R/W  | 1h    | Polarity for intr_in[27] 0=low |
| 26  | POLARITY_26 | R/W  | 1h    | Polarity for intr_in[26] 0=low |
| 25  | POLARITY_25 | R/W  | 1h    | Polarity for intr_in[25] 0=low |
| 24  | POLARITY_24 | R/W  | 1h    | Polarity for intr_in[24] 0=low |
| 23  | POLARITY_23 | R/W  | 1h    | Polarity for intr_in[23] 0=low |
| 22  | POLARITY_22 | R/W  | 1h    | Polarity for intr_in[22] 0=low |
| 21  | POLARITY_21 | R/W  | 1h    | Polarity for intr_in[21] 0=low |
| 20  | POLARITY_20 | R/W  | 1h    | Polarity for intr_in[20] 0=low |
| 19  | POLARITY_19 | R/W  | 1h    | Polarity for intr_in[19] 0=low |
| 18  | POLARITY_18 | R/W  | 1h    | Polarity for intr_in[18] 0=low |
| 17  | POLARITY_17 | R/W  | 1h    | Polarity for intr_in[17] 0=low |
| 16  | POLARITY_16 | R/W  | 1h    | Polarity for intr_in[16] 0=low |
| 15  | POLARITY_15 | R/W  | 1h    | Polarity for intr_in[15] 0=low |
| 14  | POLARITY_14 | R/W  | 1h    | Polarity for intr_in[14] 0=low |

**Table 4-886. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_POLARITY\_REG0 Register Field Descriptions  
(continued)**

| Bit | Field       | Type | Reset | Description                    |
|-----|-------------|------|-------|--------------------------------|
| 13  | POLARITY_13 | R/W  | 1h    | Polarity for intr_in[13] 0=low |
| 12  | POLARITY_12 | R/W  | 1h    | Polarity for intr_in[12] 0=low |
| 11  | POLARITY_11 | R/W  | 1h    | Polarity for intr_in[11] 0=low |
| 10  | POLARITY_10 | R/W  | 1h    | Polarity for intr_in[10] 0=low |
| 9   | POLARITY_9  | R/W  | 1h    | Polarity for intr_in[9] 0=low  |
| 8   | POLARITY_8  | R/W  | 1h    | Polarity for intr_in[8] 0=low  |
| 7   | POLARITY_7  | R/W  | 1h    | Polarity for intr_in[7] 0=low  |
| 6   | POLARITY_6  | R/W  | 1h    | Polarity for intr_in[6] 0=low  |
| 5   | POLARITY_5  | R/W  | 1h    | Polarity for intr_in[5] 0=low  |
| 4   | POLARITY_4  | R/W  | 1h    | Polarity for intr_in[4] 0=low  |
| 3   | POLARITY_3  | R/W  | 1h    | Polarity for intr_in[3] 0=low  |
| 2   | POLARITY_2  | R/W  | 1h    | Polarity for intr_in[2] 0=low  |
| 1   | POLARITY_1  | R/W  | 1h    | Polarity for intr_in[1] 0=low  |
| 0   | POLARITY_0  | R/W  | 1h    | Polarity for intr_in[0] 0=low  |

#### 4.2.2.91 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_POLARITY\_REG1 Register

#### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_POLARITY\_REG1 Register (Offset = D04h) [reset = FFFFFFFFh]

Polarity Register 1

Return to [Summary Table](#)

**Table 4-887. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0D04h       |

**Figure 4-285. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_POLARITY\_REG1 Name Register**

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 31          | 30          | 29          | 28          | 27          | 26          | 25          | 24          |
| POLARITY_63 | POLARITY_62 | POLARITY_61 | POLARITY_60 | POLARITY_59 | POLARITY_58 | POLARITY_57 | POLARITY_56 |
| R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         |
| 1h          | 1h          | 1h          | 1h          | 1h          | 1h          | 1h          | 1h          |
| 23          | 22          | 21          | 20          | 19          | 18          | 17          | 16          |
| POLARITY_55 | POLARITY_54 | POLARITY_53 | POLARITY_52 | POLARITY_51 | POLARITY_50 | POLARITY_49 | POLARITY_48 |
| R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         |
| 1h          | 1h          | 1h          | 1h          | 1h          | 1h          | 1h          | 1h          |
| 15          | 14          | 13          | 12          | 11          | 10          | 9           | 8           |
| POLARITY_47 | POLARITY_46 | POLARITY_45 | POLARITY_44 | POLARITY_43 | POLARITY_42 | POLARITY_41 | POLARITY_40 |
| R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         |
| 1h          | 1h          | 1h          | 1h          | 1h          | 1h          | 1h          | 1h          |
| 7           | 6           | 5           | 4           | 3           | 2           | 1           | 0           |
| POLARITY_39 | POLARITY_38 | POLARITY_37 | POLARITY_36 | POLARITY_35 | POLARITY_34 | POLARITY_33 | POLARITY_32 |
| R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         | R/W         |
| 1h          | 1h          | 1h          | 1h          | 1h          | 1h          | 1h          | 1h          |

**Table 4-889. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_POLARITY\_REG1 Register Field Descriptions**

| Bit | Field       | Type | Reset | Description                    |
|-----|-------------|------|-------|--------------------------------|
| 31  | POLARITY_63 | R/W  | 1h    | Polarity for intr_in[63] 0=low |
| 30  | POLARITY_62 | R/W  | 1h    | Polarity for intr_in[62] 0=low |
| 29  | POLARITY_61 | R/W  | 1h    | Polarity for intr_in[61] 0=low |
| 28  | POLARITY_60 | R/W  | 1h    | Polarity for intr_in[60] 0=low |
| 27  | POLARITY_59 | R/W  | 1h    | Polarity for intr_in[59] 0=low |
| 26  | POLARITY_58 | R/W  | 1h    | Polarity for intr_in[58] 0=low |
| 25  | POLARITY_57 | R/W  | 1h    | Polarity for intr_in[57] 0=low |
| 24  | POLARITY_56 | R/W  | 1h    | Polarity for intr_in[56] 0=low |
| 23  | POLARITY_55 | R/W  | 1h    | Polarity for intr_in[55] 0=low |
| 22  | POLARITY_54 | R/W  | 1h    | Polarity for intr_in[54] 0=low |
| 21  | POLARITY_53 | R/W  | 1h    | Polarity for intr_in[53] 0=low |
| 20  | POLARITY_52 | R/W  | 1h    | Polarity for intr_in[52] 0=low |
| 19  | POLARITY_51 | R/W  | 1h    | Polarity for intr_in[51] 0=low |
| 18  | POLARITY_50 | R/W  | 1h    | Polarity for intr_in[50] 0=low |
| 17  | POLARITY_49 | R/W  | 1h    | Polarity for intr_in[49] 0=low |
| 16  | POLARITY_48 | R/W  | 1h    | Polarity for intr_in[48] 0=low |
| 15  | POLARITY_47 | R/W  | 1h    | Polarity for intr_in[47] 0=low |
| 14  | POLARITY_46 | R/W  | 1h    | Polarity for intr_in[46] 0=low |

**Table 4-889. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_POLARITY\_REG1 Register Field Descriptions  
(continued)**

| Bit | Field       | Type | Reset | Description                    |
|-----|-------------|------|-------|--------------------------------|
| 13  | POLARITY_45 | R/W  | 1h    | Polarity for intr_in[45] 0=low |
| 12  | POLARITY_44 | R/W  | 1h    | Polarity for intr_in[44] 0=low |
| 11  | POLARITY_43 | R/W  | 1h    | Polarity for intr_in[43] 0=low |
| 10  | POLARITY_42 | R/W  | 1h    | Polarity for intr_in[42] 0=low |
| 9   | POLARITY_41 | R/W  | 1h    | Polarity for intr_in[41] 0=low |
| 8   | POLARITY_40 | R/W  | 1h    | Polarity for intr_in[40] 0=low |
| 7   | POLARITY_39 | R/W  | 1h    | Polarity for intr_in[39] 0=low |
| 6   | POLARITY_38 | R/W  | 1h    | Polarity for intr_in[38] 0=low |
| 5   | POLARITY_37 | R/W  | 1h    | Polarity for intr_in[37] 0=low |
| 4   | POLARITY_36 | R/W  | 1h    | Polarity for intr_in[36] 0=low |
| 3   | POLARITY_35 | R/W  | 1h    | Polarity for intr_in[35] 0=low |
| 2   | POLARITY_34 | R/W  | 1h    | Polarity for intr_in[34] 0=low |
| 1   | POLARITY_33 | R/W  | 1h    | Polarity for intr_in[33] 0=low |
| 0   | POLARITY_32 | R/W  | 1h    | Polarity for intr_in[32] 0=low |

#### 4.2.2.92 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_TYPE\_REG0 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_TYPE\_REG0 Register (Offset = D80h) [reset = 0h]

Type Register 0

Return to [Summary Table](#)
**Table 4-890. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0D80h       |

**Figure 4-286. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_TYPE\_REG0 Name Register**

| 31      | 30      | 29      | 28      | 27      | 26      | 25      | 24      |
|---------|---------|---------|---------|---------|---------|---------|---------|
| TYPE_31 | TYPE_30 | TYPE_29 | TYPE_28 | TYPE_27 | TYPE_26 | TYPE_25 | TYPE_24 |
| R/W     | R/W     | R/W     | R/W     | R/W     | R/W     | R/W     | R/W     |
| 0h      | 0h      | 0h      | 0h      | 0h      | 0h      | 0h      | 0h      |
| 23      | 22      | 21      | 20      | 19      | 18      | 17      | 16      |
| TYPE_23 | TYPE_22 | TYPE_21 | TYPE_20 | TYPE_19 | TYPE_18 | TYPE_17 | TYPE_16 |
| R/W     | R/W     | R/W     | R/W     | R/W     | R/W     | R/W     | R/W     |
| 0h      | 0h      | 0h      | 0h      | 0h      | 0h      | 0h      | 0h      |
| 15      | 14      | 13      | 12      | 11      | 10      | 9       | 8       |
| TYPE_15 | TYPE_14 | TYPE_13 | TYPE_12 | TYPE_11 | TYPE_10 | TYPE_9  | TYPE_8  |
| R/W     | R/W     | R/W     | R/W     | R/W     | R/W     | R/W     | R/W     |
| 0h      | 0h      | 0h      | 0h      | 0h      | 0h      | 0h      | 0h      |
| 7       | 6       | 5       | 4       | 3       | 2       | 1       | 0       |
| TYPE_7  | TYPE_6  | TYPE_5  | TYPE_4  | TYPE_3  | TYPE_2  | TYPE_1  | TYPE_0  |
| R/W     | R/W     | R/W     | R/W     | R/W     | R/W     | R/W     | R/W     |
| 0h      | 0h      | 0h      | 0h      | 0h      | 0h      | 0h      | 0h      |

**Table 4-892. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_TYPE\_REG0 Register Field Descriptions**

| Bit | Field   | Type | Reset | Description                  |
|-----|---------|------|-------|------------------------------|
| 31  | TYPE_31 | R/W  | 0h    | Type for intr_in[31] 0=level |
| 30  | TYPE_30 | R/W  | 0h    | Type for intr_in[30] 0=level |
| 29  | TYPE_29 | R/W  | 0h    | Type for intr_in[29] 0=level |
| 28  | TYPE_28 | R/W  | 0h    | Type for intr_in[28] 0=level |
| 27  | TYPE_27 | R/W  | 0h    | Type for intr_in[27] 0=level |
| 26  | TYPE_26 | R/W  | 0h    | Type for intr_in[26] 0=level |
| 25  | TYPE_25 | R/W  | 0h    | Type for intr_in[25] 0=level |
| 24  | TYPE_24 | R/W  | 0h    | Type for intr_in[24] 0=level |
| 23  | TYPE_23 | R/W  | 0h    | Type for intr_in[23] 0=level |
| 22  | TYPE_22 | R/W  | 0h    | Type for intr_in[22] 0=level |
| 21  | TYPE_21 | R/W  | 0h    | Type for intr_in[21] 0=level |
| 20  | TYPE_20 | R/W  | 0h    | Type for intr_in[20] 0=level |
| 19  | TYPE_19 | R/W  | 0h    | Type for intr_in[19] 0=level |
| 18  | TYPE_18 | R/W  | 0h    | Type for intr_in[18] 0=level |
| 17  | TYPE_17 | R/W  | 0h    | Type for intr_in[17] 0=level |
| 16  | TYPE_16 | R/W  | 0h    | Type for intr_in[16] 0=level |
| 15  | TYPE_15 | R/W  | 0h    | Type for intr_in[15] 0=level |
| 14  | TYPE_14 | R/W  | 0h    | Type for intr_in[14] 0=level |

**Table 4-892. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_TYPE\_REG0 Register Field Descriptions (continued)**

| Bit | Field   | Type | Reset | Description                  |
|-----|---------|------|-------|------------------------------|
| 13  | TYPE_13 | R/W  | 0h    | Type for intr_in[13] 0=level |
| 12  | TYPE_12 | R/W  | 0h    | Type for intr_in[12] 0=level |
| 11  | TYPE_11 | R/W  | 0h    | Type for intr_in[11] 0=level |
| 10  | TYPE_10 | R/W  | 0h    | Type for intr_in[10] 0=level |
| 9   | TYPE_9  | R/W  | 0h    | Type for intr_in[9] 0=level  |
| 8   | TYPE_8  | R/W  | 0h    | Type for intr_in[8] 0=level  |
| 7   | TYPE_7  | R/W  | 0h    | Type for intr_in[7] 0=level  |
| 6   | TYPE_6  | R/W  | 0h    | Type for intr_in[6] 0=level  |
| 5   | TYPE_5  | R/W  | 0h    | Type for intr_in[5] 0=level  |
| 4   | TYPE_4  | R/W  | 0h    | Type for intr_in[4] 0=level  |
| 3   | TYPE_3  | R/W  | 0h    | Type for intr_in[3] 0=level  |
| 2   | TYPE_2  | R/W  | 0h    | Type for intr_in[2] 0=level  |
| 1   | TYPE_1  | R/W  | 0h    | Type for intr_in[1] 0=level  |
| 0   | TYPE_0  | R/W  | 0h    | Type for intr_in[0] 0=level  |

#### 4.2.2.93 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_TYPE\_REG1 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_TYPE\_REG1 Register (Offset = D84h) [reset = 0h]

Type Register 1

Return to [Summary Table](#)
**Table 4-893. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 0D84h       |

**Figure 4-287. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_TYPE\_REG1 Name Register**

| 31      | 30      | 29      | 28      | 27      | 26      | 25      | 24      |
|---------|---------|---------|---------|---------|---------|---------|---------|
| TYPE_63 | TYPE_62 | TYPE_61 | TYPE_60 | TYPE_59 | TYPE_58 | TYPE_57 | TYPE_56 |
| R/W     | R/W     | R/W     | R/W     | R/W     | R/W     | R/W     | R/W     |
| 0h      | 0h      | 0h      | 0h      | 0h      | 0h      | 0h      | 0h      |
| 23      | 22      | 21      | 20      | 19      | 18      | 17      | 16      |
| TYPE_55 | TYPE_54 | TYPE_53 | TYPE_52 | TYPE_51 | TYPE_50 | TYPE_49 | TYPE_48 |
| R/W     | R/W     | R/W     | R/W     | R/W     | R/W     | R/W     | R/W     |
| 0h      | 0h      | 0h      | 0h      | 0h      | 0h      | 0h      | 0h      |
| 15      | 14      | 13      | 12      | 11      | 10      | 9       | 8       |
| TYPE_47 | TYPE_46 | TYPE_45 | TYPE_44 | TYPE_43 | TYPE_42 | TYPE_41 | TYPE_40 |
| R/W     | R/W     | R/W     | R/W     | R/W     | R/W     | R/W     | R/W     |
| 0h      | 0h      | 0h      | 0h      | 0h      | 0h      | 0h      | 0h      |
| 7       | 6       | 5       | 4       | 3       | 2       | 1       | 0       |
| TYPE_39 | TYPE_38 | TYPE_37 | TYPE_36 | TYPE_35 | TYPE_34 | TYPE_33 | TYPE_32 |
| R/W     | R/W     | R/W     | R/W     | R/W     | R/W     | R/W     | R/W     |
| 0h      | 0h      | 0h      | 0h      | 0h      | 0h      | 0h      | 0h      |

**Table 4-895. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_TYPE\_REG1 Register Field Descriptions**

| Bit | Field   | Type | Reset | Description                  |
|-----|---------|------|-------|------------------------------|
| 31  | TYPE_63 | R/W  | 0h    | Type for intr_in[63] 0=level |
| 30  | TYPE_62 | R/W  | 0h    | Type for intr_in[62] 0=level |
| 29  | TYPE_61 | R/W  | 0h    | Type for intr_in[61] 0=level |
| 28  | TYPE_60 | R/W  | 0h    | Type for intr_in[60] 0=level |
| 27  | TYPE_59 | R/W  | 0h    | Type for intr_in[59] 0=level |
| 26  | TYPE_58 | R/W  | 0h    | Type for intr_in[58] 0=level |
| 25  | TYPE_57 | R/W  | 0h    | Type for intr_in[57] 0=level |
| 24  | TYPE_56 | R/W  | 0h    | Type for intr_in[56] 0=level |
| 23  | TYPE_55 | R/W  | 0h    | Type for intr_in[55] 0=level |
| 22  | TYPE_54 | R/W  | 0h    | Type for intr_in[54] 0=level |
| 21  | TYPE_53 | R/W  | 0h    | Type for intr_in[53] 0=level |
| 20  | TYPE_52 | R/W  | 0h    | Type for intr_in[52] 0=level |
| 19  | TYPE_51 | R/W  | 0h    | Type for intr_in[51] 0=level |
| 18  | TYPE_50 | R/W  | 0h    | Type for intr_in[50] 0=level |
| 17  | TYPE_49 | R/W  | 0h    | Type for intr_in[49] 0=level |
| 16  | TYPE_48 | R/W  | 0h    | Type for intr_in[48] 0=level |
| 15  | TYPE_47 | R/W  | 0h    | Type for intr_in[47] 0=level |
| 14  | TYPE_46 | R/W  | 0h    | Type for intr_in[46] 0=level |



**Table 4-895. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_TYPE\_REG1 Register Field Descriptions (continued)**

| Bit | Field   | Type | Reset | Description                  |
|-----|---------|------|-------|------------------------------|
| 13  | TYPE_45 | R/W  | 0h    | Type for intr_in[45] 0=level |
| 12  | TYPE_44 | R/W  | 0h    | Type for intr_in[44] 0=level |
| 11  | TYPE_43 | R/W  | 0h    | Type for intr_in[43] 0=level |
| 10  | TYPE_42 | R/W  | 0h    | Type for intr_in[42] 0=level |
| 9   | TYPE_41 | R/W  | 0h    | Type for intr_in[41] 0=level |
| 8   | TYPE_40 | R/W  | 0h    | Type for intr_in[40] 0=level |
| 7   | TYPE_39 | R/W  | 0h    | Type for intr_in[39] 0=level |
| 6   | TYPE_38 | R/W  | 0h    | Type for intr_in[38] 0=level |
| 5   | TYPE_37 | R/W  | 0h    | Type for intr_in[37] 0=level |
| 4   | TYPE_36 | R/W  | 0h    | Type for intr_in[36] 0=level |
| 3   | TYPE_35 | R/W  | 0h    | Type for intr_in[35] 0=level |
| 2   | TYPE_34 | R/W  | 0h    | Type for intr_in[34] 0=level |
| 1   | TYPE_33 | R/W  | 0h    | Type for intr_in[33] 0=level |
| 0   | TYPE_32 | R/W  | 0h    | Type for intr_in[32] 0=level |

#### 4.2.2.94 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_NEST\_LEVEL\_REG0 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_NEST\_LEVEL\_REG0 Register (Offset = 1100h) [reset = 100h]

Host Int 0 Nesting Level Register

Return to [Summary Table](#)

**Table 4-896. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 1100h       |

**Figure 4-288. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_NEST\_LEVEL\_REG0 Name Register**

|               |          |    |    |    |    |    |             |
|---------------|----------|----|----|----|----|----|-------------|
| 31            | 30       | 29 | 28 | 27 | 26 | 25 | 24          |
| NEST_AUTO_OVR | RESERVED |    |    |    |    |    |             |
| W             | NONE     |    |    |    |    |    |             |
| X             | 0h       |    |    |    |    |    |             |
| 23            | 22       | 21 | 20 | 19 | 18 | 17 | 16          |
| RESERVED      |          |    |    |    |    |    |             |
| NONE          |          |    |    |    |    |    |             |
| 0h            |          |    |    |    |    |    |             |
| 15            | 14       | 13 | 12 | 11 | 10 | 9  | 8           |
| RESERVED      |          |    |    |    |    |    | NEST_HINT_0 |
| NONE          |          |    |    |    |    |    | R/W         |
| 0h            |          |    |    |    |    |    | 100h        |
| 7             | 6        | 5  | 4  | 3  | 2  | 1  | 0           |
| NEST_HINT_0   |          |    |    |    |    |    |             |
| R/W           |          |    |    |    |    |    |             |
| 100h          |          |    |    |    |    |    |             |

**Table 4-898. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_NEST\_LEVEL\_REG0 Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                      |
|------|---------------|------|-------|----------------------------------|
| 31   | NEST_AUTO_OVR | W    | X     | Nesting Level Override Automatic |
| 30:9 | RESERVED      | NONE | 0h    | Reserved                         |
| 8:0  | NEST_HINT_0   | R/W  | 100h  | Host Int 0 Nesting Level         |

#### 4.2.2.95 ICSSM\_PR1\_ICSS\_INTc\_INTc\_SLV\_NEST\_LEVEL\_REG1 Register

##### 1 ICSSM\_PR1\_ICSS\_INTc\_INTc\_SLV\_NEST\_LEVEL\_REG1 Register (Offset = 1104h) [reset = 100h]

Host Int 1 Nesting Level Register

Return to [Summary Table](#)

**Table 4-899. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 1104h       |

**Figure 4-289. ICSSM\_PR1\_ICSS\_INTc\_INTc\_SLV\_NEST\_LEVEL\_REG1 Name Register**

|               |          |    |    |    |    |    |             |
|---------------|----------|----|----|----|----|----|-------------|
| 31            | 30       | 29 | 28 | 27 | 26 | 25 | 24          |
| NEST_AUTO_OVR | RESERVED |    |    |    |    |    |             |
| W             | NONE     |    |    |    |    |    |             |
| X             | 0h       |    |    |    |    |    |             |
| 23            | 22       | 21 | 20 | 19 | 18 | 17 | 16          |
| RESERVED      |          |    |    |    |    |    |             |
| NONE          |          |    |    |    |    |    |             |
| 0h            |          |    |    |    |    |    |             |
| 15            | 14       | 13 | 12 | 11 | 10 | 9  | 8           |
| RESERVED      |          |    |    |    |    |    | NEST_HINT_1 |
| NONE          |          |    |    |    |    |    | R/W         |
| 0h            |          |    |    |    |    |    | 100h        |
| 7             | 6        | 5  | 4  | 3  | 2  | 1  | 0           |
| NEST_HINT_1   |          |    |    |    |    |    |             |
| R/W           |          |    |    |    |    |    |             |
| 100h          |          |    |    |    |    |    |             |

**Table 4-901. ICSSM\_PR1\_ICSS\_INTc\_INTc\_SLV\_NEST\_LEVEL\_REG1 Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                      |
|------|---------------|------|-------|----------------------------------|
| 31   | NEST_AUTO_OVR | W    | X     | Nesting Level Override Automatic |
| 30:9 | RESERVED      | NONE | 0h    | Reserved                         |
| 8:0  | NEST_HINT_1   | R/W  | 100h  | Host Int 1 Nesting Level         |

#### 4.2.2.96 ICSSM\_PR1\_ICSS\_INTc\_INTc\_SLV\_NEST\_LEVEL\_REG2 Register

##### 1 ICSSM\_PR1\_ICSS\_INTc\_INTc\_SLV\_NEST\_LEVEL\_REG2 Register (Offset = 1108h) [reset = 100h]

Host Int 2 Nesting Level Register

Return to [Summary Table](#)

**Table 4-902. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 1108h       |

**Figure 4-290. ICSSM\_PR1\_ICSS\_INTc\_INTc\_SLV\_NEST\_LEVEL\_REG2 Name Register**

|               |          |    |    |    |    |    |             |
|---------------|----------|----|----|----|----|----|-------------|
| 31            | 30       | 29 | 28 | 27 | 26 | 25 | 24          |
| NEST_AUTO_OVR | RESERVED |    |    |    |    |    |             |
| W             | NONE     |    |    |    |    |    |             |
| X             | 0h       |    |    |    |    |    |             |
| 23            | 22       | 21 | 20 | 19 | 18 | 17 | 16          |
| RESERVED      |          |    |    |    |    |    |             |
| NONE          |          |    |    |    |    |    |             |
| 0h            |          |    |    |    |    |    |             |
| 15            | 14       | 13 | 12 | 11 | 10 | 9  | 8           |
| RESERVED      |          |    |    |    |    |    | NEST_HINT_2 |
| NONE          |          |    |    |    |    |    | R/W         |
| 0h            |          |    |    |    |    |    | 100h        |
| 7             | 6        | 5  | 4  | 3  | 2  | 1  | 0           |
| NEST_HINT_2   |          |    |    |    |    |    |             |
| R/W           |          |    |    |    |    |    |             |
| 100h          |          |    |    |    |    |    |             |

**Table 4-904. ICSSM\_PR1\_ICSS\_INTc\_INTc\_SLV\_NEST\_LEVEL\_REG2 Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                      |
|------|---------------|------|-------|----------------------------------|
| 31   | NEST_AUTO_OVR | W    | X     | Nesting Level Override Automatic |
| 30:9 | RESERVED      | NONE | 0h    | Reserved                         |
| 8:0  | NEST_HINT_2   | R/W  | 100h  | Host Int 2 Nesting Level         |

#### 4.2.2.97 ICSSM\_PR1\_ICSS\_INT3\_INT3\_SLV\_NEST\_LEVEL\_REG3 Register

##### 1 ICSSM\_PR1\_ICSS\_INT3\_INT3\_SLV\_NEST\_LEVEL\_REG3 Register (Offset = 110Ch) [reset = 100h]

Host Int 3 Nesting Level Register

Return to [Summary Table](#)

**Table 4-905. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 110Ch       |

**Figure 4-291. ICSSM\_PR1\_ICSS\_INT3\_INT3\_SLV\_NEST\_LEVEL\_REG3 Name Register**

|               |          |    |    |    |    |    |             |
|---------------|----------|----|----|----|----|----|-------------|
| 31            | 30       | 29 | 28 | 27 | 26 | 25 | 24          |
| NEST_AUTO_OVR | RESERVED |    |    |    |    |    |             |
| W             | NONE     |    |    |    |    |    |             |
| X             | 0h       |    |    |    |    |    |             |
| 23            | 22       | 21 | 20 | 19 | 18 | 17 | 16          |
| RESERVED      |          |    |    |    |    |    |             |
| NONE          |          |    |    |    |    |    |             |
| 0h            |          |    |    |    |    |    |             |
| 15            | 14       | 13 | 12 | 11 | 10 | 9  | 8           |
| RESERVED      |          |    |    |    |    |    | NEST_HINT_3 |
| NONE          |          |    |    |    |    |    | R/W         |
| 0h            |          |    |    |    |    |    | 100h        |
| 7             | 6        | 5  | 4  | 3  | 2  | 1  | 0           |
| NEST_HINT_3   |          |    |    |    |    |    |             |
| R/W           |          |    |    |    |    |    |             |
| 100h          |          |    |    |    |    |    |             |

**Table 4-907. ICSSM\_PR1\_ICSS\_INT3\_INT3\_SLV\_NEST\_LEVEL\_REG3 Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                      |
|------|---------------|------|-------|----------------------------------|
| 31   | NEST_AUTO_OVR | W    | X     | Nesting Level Override Automatic |
| 30:9 | RESERVED      | NONE | 0h    | Reserved                         |
| 8:0  | NEST_HINT_3   | R/W  | 100h  | Host Int 3 Nesting Level         |

#### 4.2.2.98 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_NEST\_LEVEL\_REG4 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_NEST\_LEVEL\_REG4 Register (Offset = 1110h) [reset = 100h]

Host Int 4 Nesting Level Register

Return to [Summary Table](#)

**Table 4-908. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 1110h       |

**Figure 4-292. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_NEST\_LEVEL\_REG4 Name Register**

|               |          |    |    |    |    |    |             |
|---------------|----------|----|----|----|----|----|-------------|
| 31            | 30       | 29 | 28 | 27 | 26 | 25 | 24          |
| NEST_AUTO_OVR | RESERVED |    |    |    |    |    |             |
| W             | NONE     |    |    |    |    |    |             |
| X             | 0h       |    |    |    |    |    |             |
| 23            | 22       | 21 | 20 | 19 | 18 | 17 | 16          |
| RESERVED      |          |    |    |    |    |    |             |
| NONE          |          |    |    |    |    |    |             |
| 0h            |          |    |    |    |    |    |             |
| 15            | 14       | 13 | 12 | 11 | 10 | 9  | 8           |
| RESERVED      |          |    |    |    |    |    | NEST_HINT_4 |
| NONE          |          |    |    |    |    |    | R/W         |
| 0h            |          |    |    |    |    |    | 100h        |
| 7             | 6        | 5  | 4  | 3  | 2  | 1  | 0           |
| NEST_HINT_4   |          |    |    |    |    |    |             |
| R/W           |          |    |    |    |    |    |             |
| 100h          |          |    |    |    |    |    |             |

**Table 4-910. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_NEST\_LEVEL\_REG4 Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                      |
|------|---------------|------|-------|----------------------------------|
| 31   | NEST_AUTO_OVR | W    | X     | Nesting Level Override Automatic |
| 30:9 | RESERVED      | NONE | 0h    | Reserved                         |
| 8:0  | NEST_HINT_4   | R/W  | 100h  | Host Int 4 Nesting Level         |

#### 4.2.2.99 ICSSM\_PR1\_ICSS\_INTc\_INTc\_SLV\_NEST\_LEVEL\_REG5 Register

##### 1 ICSSM\_PR1\_ICSS\_INTc\_INTc\_SLV\_NEST\_LEVEL\_REG5 Register (Offset = 1114h) [reset = 100h]

Host Int 5 Nesting Level Register

Return to [Summary Table](#)

**Table 4-911. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 1114h       |

**Figure 4-293. ICSSM\_PR1\_ICSS\_INTc\_INTc\_SLV\_NEST\_LEVEL\_REG5 Name Register**

|               |          |    |    |    |    |    |             |
|---------------|----------|----|----|----|----|----|-------------|
| 31            | 30       | 29 | 28 | 27 | 26 | 25 | 24          |
| NEST_AUTO_OVR | RESERVED |    |    |    |    |    |             |
| W             | NONE     |    |    |    |    |    |             |
| X             | 0h       |    |    |    |    |    |             |
| 23            | 22       | 21 | 20 | 19 | 18 | 17 | 16          |
| RESERVED      |          |    |    |    |    |    |             |
| NONE          |          |    |    |    |    |    |             |
| 0h            |          |    |    |    |    |    |             |
| 15            | 14       | 13 | 12 | 11 | 10 | 9  | 8           |
| RESERVED      |          |    |    |    |    |    | NEST_HINT_5 |
| NONE          |          |    |    |    |    |    | R/W         |
| 0h            |          |    |    |    |    |    | 100h        |
| 7             | 6        | 5  | 4  | 3  | 2  | 1  | 0           |
| NEST_HINT_5   |          |    |    |    |    |    |             |
| R/W           |          |    |    |    |    |    |             |
| 100h          |          |    |    |    |    |    |             |

**Table 4-913. ICSSM\_PR1\_ICSS\_INTc\_INTc\_SLV\_NEST\_LEVEL\_REG5 Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                      |
|------|---------------|------|-------|----------------------------------|
| 31   | NEST_AUTO_OVR | W    | X     | Nesting Level Override Automatic |
| 30:9 | RESERVED      | NONE | 0h    | Reserved                         |
| 8:0  | NEST_HINT_5   | R/W  | 100h  | Host Int 5 Nesting Level         |

#### 4.2.2.100 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_NEST\_LEVEL\_REG6 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_NEST\_LEVEL\_REG6 Register (Offset = 1118h) [reset = 100h]

Host Int 6 Nesting Level Register

Return to [Summary Table](#)

**Table 4-914. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 1118h       |

**Figure 4-294. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_NEST\_LEVEL\_REG6 Name Register**

|               |          |    |    |    |    |    |             |
|---------------|----------|----|----|----|----|----|-------------|
| 31            | 30       | 29 | 28 | 27 | 26 | 25 | 24          |
| NEST_AUTO_OVR | RESERVED |    |    |    |    |    |             |
| W             | NONE     |    |    |    |    |    |             |
| X             | 0h       |    |    |    |    |    |             |
| 23            | 22       | 21 | 20 | 19 | 18 | 17 | 16          |
| RESERVED      |          |    |    |    |    |    |             |
| NONE          |          |    |    |    |    |    |             |
| 0h            |          |    |    |    |    |    |             |
| 15            | 14       | 13 | 12 | 11 | 10 | 9  | 8           |
| RESERVED      |          |    |    |    |    |    | NEST_HINT_6 |
| NONE          |          |    |    |    |    |    | R/W         |
| 0h            |          |    |    |    |    |    | 100h        |
| 7             | 6        | 5  | 4  | 3  | 2  | 1  | 0           |
| NEST_HINT_6   |          |    |    |    |    |    |             |
| R/W           |          |    |    |    |    |    |             |
| 100h          |          |    |    |    |    |    |             |

**Table 4-916. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_NEST\_LEVEL\_REG6 Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                      |
|------|---------------|------|-------|----------------------------------|
| 31   | NEST_AUTO_OVR | W    | X     | Nesting Level Override Automatic |
| 30:9 | RESERVED      | NONE | 0h    | Reserved                         |
| 8:0  | NEST_HINT_6   | R/W  | 100h  | Host Int 6 Nesting Level         |



#### 4.2.2.101 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_NEST\_LEVEL\_REG7 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_NEST\_LEVEL\_REG7 Register (Offset = 111Ch) [reset = 100h]

Host Int 7 Nesting Level Register

Return to [Summary Table](#)

**Table 4-917. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 111Ch       |

**Figure 4-295. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_NEST\_LEVEL\_REG7 Name Register**

|               |          |    |    |    |    |    |             |
|---------------|----------|----|----|----|----|----|-------------|
| 31            | 30       | 29 | 28 | 27 | 26 | 25 | 24          |
| NEST_AUTO_OVR | RESERVED |    |    |    |    |    |             |
| W             | NONE     |    |    |    |    |    |             |
| X             | 0h       |    |    |    |    |    |             |
| 23            | 22       | 21 | 20 | 19 | 18 | 17 | 16          |
| RESERVED      |          |    |    |    |    |    |             |
| NONE          |          |    |    |    |    |    |             |
| 0h            |          |    |    |    |    |    |             |
| 15            | 14       | 13 | 12 | 11 | 10 | 9  | 8           |
| RESERVED      |          |    |    |    |    |    | NEST_HINT_7 |
| NONE          |          |    |    |    |    |    | R/W         |
| 0h            |          |    |    |    |    |    | 100h        |
| 7             | 6        | 5  | 4  | 3  | 2  | 1  | 0           |
| NEST_HINT_7   |          |    |    |    |    |    |             |
| R/W           |          |    |    |    |    |    |             |
| 100h          |          |    |    |    |    |    |             |

**Table 4-919. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_NEST\_LEVEL\_REG7 Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                      |
|------|---------------|------|-------|----------------------------------|
| 31   | NEST_AUTO_OVR | W    | X     | Nesting Level Override Automatic |
| 30:9 | RESERVED      | NONE | 0h    | Reserved                         |
| 8:0  | NEST_HINT_7   | R/W  | 100h  | Host Int 7 Nesting Level         |

#### 4.2.2.102 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_NEST\_LEVEL\_REG8 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_NEST\_LEVEL\_REG8 Register (Offset = 1120h) [reset = 100h]

Host Int 8 Nesting Level Register

Return to [Summary Table](#)

**Table 4-920. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 1120h       |

**Figure 4-296. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_NEST\_LEVEL\_REG8 Name Register**

|               |          |    |    |    |    |    |             |
|---------------|----------|----|----|----|----|----|-------------|
| 31            | 30       | 29 | 28 | 27 | 26 | 25 | 24          |
| NEST_AUTO_OVR | RESERVED |    |    |    |    |    |             |
| W             | NONE     |    |    |    |    |    |             |
| X             | 0h       |    |    |    |    |    |             |
| 23            | 22       | 21 | 20 | 19 | 18 | 17 | 16          |
| RESERVED      |          |    |    |    |    |    |             |
| NONE          |          |    |    |    |    |    |             |
| 0h            |          |    |    |    |    |    |             |
| 15            | 14       | 13 | 12 | 11 | 10 | 9  | 8           |
| RESERVED      |          |    |    |    |    |    | NEST_HINT_8 |
| NONE          |          |    |    |    |    |    | R/W         |
| 0h            |          |    |    |    |    |    | 100h        |
| 7             | 6        | 5  | 4  | 3  | 2  | 1  | 0           |
| NEST_HINT_8   |          |    |    |    |    |    |             |
| R/W           |          |    |    |    |    |    |             |
| 100h          |          |    |    |    |    |    |             |

**Table 4-922. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_NEST\_LEVEL\_REG8 Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                      |
|------|---------------|------|-------|----------------------------------|
| 31   | NEST_AUTO_OVR | W    | X     | Nesting Level Override Automatic |
| 30:9 | RESERVED      | NONE | 0h    | Reserved                         |
| 8:0  | NEST_HINT_8   | R/W  | 100h  | Host Int 8 Nesting Level         |

#### 4.2.2.103 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_NEST\_LEVEL\_REG9 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_NEST\_LEVEL\_REG9 Register (Offset = 1124h) [reset = 100h]

Host Int 9 Nesting Level Register

Return to [Summary Table](#)

**Table 4-923. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 1124h       |

**Figure 4-297. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_NEST\_LEVEL\_REG9 Name Register**

|               |          |    |    |    |    |    |             |
|---------------|----------|----|----|----|----|----|-------------|
| 31            | 30       | 29 | 28 | 27 | 26 | 25 | 24          |
| NEST_AUTO_OVR | RESERVED |    |    |    |    |    |             |
| W             | NONE     |    |    |    |    |    |             |
| X             | 0h       |    |    |    |    |    |             |
| 23            | 22       | 21 | 20 | 19 | 18 | 17 | 16          |
| RESERVED      |          |    |    |    |    |    |             |
| NONE          |          |    |    |    |    |    |             |
| 0h            |          |    |    |    |    |    |             |
| 15            | 14       | 13 | 12 | 11 | 10 | 9  | 8           |
| RESERVED      |          |    |    |    |    |    | NEST_HINT_9 |
| NONE          |          |    |    |    |    |    | R/W         |
| 0h            |          |    |    |    |    |    | 100h        |
| 7             | 6        | 5  | 4  | 3  | 2  | 1  | 0           |
| NEST_HINT_9   |          |    |    |    |    |    |             |
| R/W           |          |    |    |    |    |    |             |
| 100h          |          |    |    |    |    |    |             |

**Table 4-925. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_NEST\_LEVEL\_REG9 Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                      |
|------|---------------|------|-------|----------------------------------|
| 31   | NEST_AUTO_OVR | W    | X     | Nesting Level Override Automatic |
| 30:9 | RESERVED      | NONE | 0h    | Reserved                         |
| 8:0  | NEST_HINT_9   | R/W  | 100h  | Host Int 9 Nesting Level         |

#### 4.2.2.104 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENABLE\_HINT\_REG0 Register

##### 1 ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENABLE\_HINT\_REG0 Register (Offset = 1500h) [reset = 0h]

Host Int Enable Register 0

Return to [Summary Table](#)
**Table 4-926. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 1500h       |

**Figure 4-298. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENABLE\_HINT\_REG0 Name Register**

|               |               |               |               |               |               |               |               |
|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| 31            | 30            | 29            | 28            | 27            | 26            | 25            | 24            |
| RESERVED      |               |               |               |               |               |               |               |
| NONE          |               |               |               |               |               |               |               |
| 0h            |               |               |               |               |               |               |               |
| 23            | 22            | 21            | 20            | 19            | 18            | 17            | 16            |
| RESERVED      |               |               |               |               |               |               |               |
| NONE          |               |               |               |               |               |               |               |
| 0h            |               |               |               |               |               |               |               |
| 15            | 14            | 13            | 12            | 11            | 10            | 9             | 8             |
| RESERVED      |               |               |               |               |               | ENABLE_HINT_9 | ENABLE_HINT_8 |
| NONE          |               |               |               |               |               | R/W           | R/W           |
| 0h            |               |               |               |               |               | 0h            | 0h            |
| 7             | 6             | 5             | 4             | 3             | 2             | 1             | 0             |
| ENABLE_HINT_7 | ENABLE_HINT_6 | ENABLE_HINT_5 | ENABLE_HINT_4 | ENABLE_HINT_3 | ENABLE_HINT_2 | ENABLE_HINT_1 | ENABLE_HINT_0 |
| R/W           | R/W           | R/W           | R/W           | R/W           | R/W           | R/W           | R/W           |
| 0h            | 0h            | 0h            | 0h            | 0h            | 0h            | 0h            | 0h            |

**Table 4-928. ICSSM\_PR1\_ICSS\_INTC\_INTC\_SLV\_ENABLE\_HINT\_REG0 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description           |
|-------|---------------|------|-------|-----------------------|
| 31:10 | RESERVED      | NONE | 0h    | Reserved              |
| 9     | ENABLE_HINT_9 | R/W  | 0h    | Enable for Host Int 9 |
| 8     | ENABLE_HINT_8 | R/W  | 0h    | Enable for Host Int 8 |
| 7     | ENABLE_HINT_7 | R/W  | 0h    | Enable for Host Int 7 |
| 6     | ENABLE_HINT_6 | R/W  | 0h    | Enable for Host Int 6 |
| 5     | ENABLE_HINT_5 | R/W  | 0h    | Enable for Host Int 5 |
| 4     | ENABLE_HINT_4 | R/W  | 0h    | Enable for Host Int 4 |
| 3     | ENABLE_HINT_3 | R/W  | 0h    | Enable for Host Int 3 |
| 2     | ENABLE_HINT_2 | R/W  | 0h    | Enable for Host Int 2 |
| 1     | ENABLE_HINT_1 | R/W  | 0h    | Enable for Host Int 1 |
| 0     | ENABLE_HINT_0 | R/W  | 0h    | Enable for Host Int 0 |

#### 4.2.2.105 ICSSM\_PR1\_PROTECT\_SLV\_UNLOCK\_KEY Register

##### 1 ICSSM\_PR1\_PROTECT\_SLV\_UNLOCK\_KEY Register (Offset = 0h) [reset = 0h]

LOCK KEY

Return to [Summary Table](#)

**Table 4-929. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 4C00h       |

**Figure 4-299. ICSSM\_PR1\_PROTECT\_SLV\_UNLOCK\_KEY Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UNLOCK_KEY |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UNLOCK_KEY |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| UNLOCK_KEY |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| UNLOCK_KEY |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 4-931. ICSSM\_PR1\_PROTECT\_SLV\_UNLOCK\_KEY Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                |
|------|------------|------|-------|--------------------------------------------------------------------------------------------|
| 31:0 | UNLOCK_KEY | R/W  | 0h    | UnLock Key Pattern 0x83E7_0B13 to UnLock 0x0000_0000 to Lock<br>Must unlock to update MMRs |

#### 4.2.2.106 ICSSM\_PR1\_PROTECT\_SLV\_CFG Register

##### 1 ICSSM\_PR1\_PROTECT\_SLV\_CFG Register (Offset = 4h) [reset = 0h]

Config.

Return to [Summary Table](#)

**Table 4-932. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 4C04h       |

**Figure 4-300. ICSSM\_PR1\_PROTECT\_SLV\_CFG Name Register**

|          |                    |                    |                |                |                |            |            |
|----------|--------------------|--------------------|----------------|----------------|----------------|------------|------------|
| 31       | 30                 | 29                 | 28             | 27             | 26             | 25         | 24         |
| RESERVED |                    |                    |                |                |                |            |            |
| NONE     |                    |                    |                |                |                |            |            |
| 0h       |                    |                    |                |                |                |            |            |
| 23       | 22                 | 21                 | 20             | 19             | 18             | 17         | 16         |
| RESERVED |                    |                    |                |                |                |            |            |
| NONE     |                    |                    |                |                |                |            |            |
| 0h       |                    |                    |                |                |                |            |            |
| 15       | 14                 | 13                 | 12             | 11             | 10             | 9          | 8          |
| RESERVED |                    |                    |                |                |                |            |            |
| NONE     |                    |                    |                |                |                |            |            |
| 0h       |                    |                    |                |                |                |            |            |
| 7        | 6                  | 5                  | 4              | 3              | 2              | 1          | 0          |
| RESERVED | PRU1_DMEM1_LOCK_EN | PRU0_DMEM0_LOCK_EN | ICSS_CFG_WP_EN | RTU1_PRU_WP_EN | RTU0_PRU_WP_EN | PRU1_WP_EN | PRU0_WP_EN |
| NONE     | R/W                | R/W                | R/W            | R/W            | R/W            | R/W        | R/W        |
| 0h       | 0h                 | 0h                 | 0h             | 0h             | 0h             | 0h         | 0h         |

**Table 4-934. ICSSM\_PR1\_PROTECT\_SLV\_CFG Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                            |
|------|--------------------|------|-------|----------------------------------------------------------------------------------------|
| 31:7 | RESERVED           | NONE | 0h    | Reserved                                                                               |
| 6    | PRU1_DMEM1_LOCK_EN | R/W  | 0h    | Write Protect DMEM1<br>0:disable<br>1:enable When enabled only PRU1 can write to DMEM1 |
| 5    | PRU0_DMEM0_LOCK_EN | R/W  | 0h    | Write Protect DMEM0<br>0:disable<br>1:enable When enabled only PRU0 can write to DMEM0 |
| 4    | ICSS_CFG_WP_EN     | R/W  | 0h    | Write Protect ICSS_CFG<br>0:disable<br>1:enable                                        |
| 3    | RTU1_PRU_WP_EN     | R/W  | 0h    | Write Protect RTU1_PRU access Debug IMEM<br>0:disable<br>1:enable                      |
| 2    | RTU0_PRU_WP_EN     | R/W  | 0h    | Write Protect RTU0_PRU access Debug IMEM<br>0:disable<br>1:enable                      |
| 1    | PRU1_WP_EN         | R/W  | 0h    | Write Protect PRU1 access Debug IMEM<br>0:disable<br>1:enable                          |

**Table 4-934. ICSSM\_PR1\_PROTECT\_SLV\_CFG Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                   |
|-----|------------|------|-------|---------------------------------------------------------------|
| 0   | PRU0_WP_EN | R/W  | 0h    | Write Protect PRU0 access Debug IMEM<br>0:disable<br>1:enable |

#### 4.2.2.107 ICSSM\_PR1\_CFG\_SLV\_PID\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PID\_REG Register (Offset = 0h) [reset = 6B080203h]

PID Register

Return to [Summary Table](#)

**Table 4-935. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6000h       |

**Figure 4-301. ICSSM\_PR1\_CFG\_SLV\_PID\_REG Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ICSS_IDVER |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 6B080203h  |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ICSS_IDVER |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 6B080203h  |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICSS_IDVER |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 6B080203h  |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICSS_IDVER |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 6B080203h  |    |    |    |    |    |    |    |

**Table 4-937. ICSSM\_PR1\_CFG\_SLV\_PID\_REG Register Field Descriptions**

| Bit  | Field      | Type | Reset     | Description     |
|------|------------|------|-----------|-----------------|
| 31:0 | ICSS_IDVER | R    | 6B080203h | Module ID field |



#### 4.2.2.108 ICSSM\_PR1\_CFG\_SLV\_HWDIS\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_HWDIS\_REG Register (Offset = 4h) [reset = 0h]

HW DIS Register

Return to [Summary Table](#)

**Table 4-938. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6004h       |

**Figure 4-302. ICSSM\_PR1\_CFG\_SLV\_HWDIS\_REG Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| HWDIS    |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| X        |    |    |    |    |    |    |    |

**Table 4-940. ICSSM\_PR1\_CFG\_SLV\_HWDIS\_REG Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description            |
|------|----------|------|-------|------------------------|
| 31:8 | RESERVED | NONE | 0h    | Reserved               |
| 7:0  | HWDIS    | R    | X     | HW Disable Observation |

#### 4.2.2.109 ICSSM\_PR1\_CFG\_SLV\_GPCFG0\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_GPCFG0\_REG Register (Offset = 8h) [reset = 0h]

gpcfg0 Register

Return to [Summary Table](#)
**Table 4-941. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6008h       |

**Figure 4-303. ICSSM\_PR1\_CFG\_SLV\_GPCFG0\_REG Name Register**

| 31            | 30            | 29                  | 28            | 27            | 26                | 25               | 24            |
|---------------|---------------|---------------------|---------------|---------------|-------------------|------------------|---------------|
| RESERVED      |               | PR1_PRU0_GP_MUX_SEL |               |               |                   | PRU0_GPO_SH1_SEL | PRU0_GPO_DIV1 |
| NONE          |               | R/W                 |               |               |                   | R                | R/W           |
| 0h            |               | 0h                  |               |               |                   | 0h               | 0h            |
| 23            | 22            | 21                  | 20            | 19            | 18                | 17               | 16            |
| PRU0_GPO_DIV1 |               |                     |               | PRU0_GPO_DIV0 |                   |                  |               |
| R/W           |               |                     |               | R/W           |                   |                  |               |
| 0h            |               |                     |               | 0h            |                   |                  |               |
| 15            | 14            | 13                  | 12            | 11            | 10                | 9                | 8             |
| PRU0_GPO_DIV0 | PRU0_GPO_MODE | PRU0_GPI_SB         | PRU0_GPI_DIV1 |               |                   |                  |               |
| R/W           | R/W           | R/W1TC              | R/W           |               |                   |                  |               |
| 0h            | 0h            | 0h                  | 0h            |               |                   |                  |               |
| 7             | 6             | 5                   | 4             | 3             | 2                 | 1                | 0             |
| PRU0_GPI_DIV0 |               |                     |               |               | PRU0_GPI_CLK_MODE | PRU0_GPI_MODE    |               |
| R/W           |               |                     |               |               | R/W               | R/W              |               |
| 0h            |               |                     |               |               | 0h                | 0h               |               |

**Table 4-943. ICSSM\_PR1\_CFG\_SLV\_GPCFG0\_REG Register Field Descriptions**

| Bit   | Field               | Type   | Reset | Description |
|-------|---------------------|--------|-------|-------------|
| 31:30 | RESERVED            | NONE   | 0h    | Reserved    |
| 29:26 | PR1_PRU0_GP_MUX_SEL | R/W    | 0h    |             |
| 25    | PRU0_GPO_SH1_SEL    | R      | 0h    |             |
| 24:20 | PRU0_GPO_DIV1       | R/W    | 0h    |             |
| 19:15 | PRU0_GPO_DIV0       | R/W    | 0h    |             |
| 14    | PRU0_GPO_MODE       | R/W    | 0h    |             |
| 13    | PRU0_GPI_SB         | R/W1TC | 0h    |             |
| 12:8  | PRU0_GPI_DIV1       | R/W    | 0h    |             |
| 7:3   | PRU0_GPI_DIV0       | R/W    | 0h    |             |
| 2     | PRU0_GPI_CLK_MODE   | R/W    | 0h    |             |
| 1:0   | PRU0_GPI_MODE       | R/W    | 0h    |             |

#### 4.2.2.110 ICSSM\_PR1\_CFG\_SLV\_GPCFG1\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_GPCFG1\_REG Register (Offset = Ch) [reset = 0h]

gpcfg1 Register

Return to [Summary Table](#)
**Table 4-944. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 600Ch       |

**Figure 4-304. ICSSM\_PR1\_CFG\_SLV\_GPCFG1\_REG Name Register**

| 31            | 30            | 29                  | 28            | 27            | 26                | 25               | 24            |
|---------------|---------------|---------------------|---------------|---------------|-------------------|------------------|---------------|
| RESERVED      |               | PR1_PRU1_GP_MUX_SEL |               |               |                   | PRU1_GPO_SH1_SEL | PRU1_GPO_DIV1 |
| NONE          |               | R/W                 |               |               |                   | R                | R/W           |
| 0h            |               | 0h                  |               |               |                   | 0h               | 0h            |
| 23            | 22            | 21                  | 20            | 19            | 18                | 17               | 16            |
| PRU1_GPO_DIV1 |               |                     |               | PRU1_GPO_DIV0 |                   |                  |               |
| R/W           |               |                     |               | R/W           |                   |                  |               |
| 0h            |               |                     |               | 0h            |                   |                  |               |
| 15            | 14            | 13                  | 12            | 11            | 10                | 9                | 8             |
| PRU1_GPO_DIV0 | PRU1_GPO_MODE | PRU1_GPI_SB         | PRU1_GPI_DIV1 |               |                   |                  |               |
| R/W           | R/W           | R/W1TC              | R/W           |               |                   |                  |               |
| 0h            | 0h            | 0h                  | 0h            |               |                   |                  |               |
| 7             | 6             | 5                   | 4             | 3             | 2                 | 1                | 0             |
| PRU1_GPI_DIV0 |               |                     |               |               | PRU1_GPI_CLK_MODE | PRU1_GPI_MODE    |               |
| R/W           |               |                     |               |               | R/W               | R/W              |               |
| 0h            |               |                     |               |               | 0h                | 0h               |               |

**Table 4-946. ICSSM\_PR1\_CFG\_SLV\_GPCFG1\_REG Register Field Descriptions**

| Bit   | Field               | Type   | Reset | Description |
|-------|---------------------|--------|-------|-------------|
| 31:30 | RESERVED            | NONE   | 0h    | Reserved    |
| 29:26 | PR1_PRU1_GP_MUX_SEL | R/W    | 0h    |             |
| 25    | PRU1_GPO_SH1_SEL    | R      | 0h    |             |
| 24:20 | PRU1_GPO_DIV1       | R/W    | 0h    |             |
| 19:15 | PRU1_GPO_DIV0       | R/W    | 0h    |             |
| 14    | PRU1_GPO_MODE       | R/W    | 0h    |             |
| 13    | PRU1_GPI_SB         | R/W1TC | 0h    |             |
| 12:8  | PRU1_GPI_DIV1       | R/W    | 0h    |             |
| 7:3   | PRU1_GPI_DIV0       | R/W    | 0h    |             |
| 2     | PRU1_GPI_CLK_MODE   | R/W    | 0h    |             |
| 1:0   | PRU1_GPI_MODE       | R/W    | 0h    |             |

#### 4.2.2.111 ICSSM\_PR1\_CFG\_SLV\_CGR\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_CGR\_REG Register (Offset = 10h) [reset = A0324900h]

cgr Register

Return to [Summary Table](#)
**Table 4-947. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6010h       |

**Figure 4-305. ICSSM\_PR1\_CFG\_SLV\_CGR\_REG Name Register**

| 31                    | 30                    | 29                              | 28                       | 27                              | 26                              | 25                    | 24                   |
|-----------------------|-----------------------|---------------------------------|--------------------------|---------------------------------|---------------------------------|-----------------------|----------------------|
| ICSS_STOP_A<br>CK     | ICSS_STOP_R<br>EQ     | ICSS_PWR_ID<br>LE               | RESERVED                 |                                 |                                 |                       |                      |
| R/W                   | R                     | R/W                             | NONE                     |                                 |                                 |                       |                      |
| 1h                    | 0h                    | 1h                              | 0h                       |                                 |                                 |                       |                      |
| 23                    | 22                    | 21                              | 20                       | 19                              | 18                              | 17                    | 16                   |
| RESERVED              |                       | BOTTOM_HAL<br>F_CLK_GATE_<br>EN | TOP_HALF_CL<br>K_GATE_EN | AUTO_SLICE1<br>_CLK_GATE_<br>EN | AUTO_SLICE0<br>_CLK_GATE_<br>EN | IEP_CLK_EN            | IEP_CLK_STO<br>P_ACK |
| NONE                  |                       | R/W                             | R/W                      | R/W                             | R/W                             | R/W                   | R                    |
| 0h                    |                       | 1h                              | 1h                       | 0h                              | 0h                              | 1h                    | 0h                   |
| 15                    | 14                    | 13                              | 12                       | 11                              | 10                              | 9                     | 8                    |
| IEP_CLK_STO<br>P_REQ  | ECAP_CLK_EN           | ECAP_CLK_ST<br>OP_ACK           | ECAP_CLK_ST<br>OP_REQ    | UART_CLK_EN                     | UART_CLK_ST<br>OP_ACK           | UART_CLK_ST<br>OP_REQ | INTC_CLK_EN          |
| R/W                   | R/W                   | R                               | R/W                      | R/W                             | R                               | R/W                   | R/W                  |
| 0h                    | 1h                    | 0h                              | 0h                       | 1h                              | 0h                              | 0h                    | 1h                   |
| 7                     | 6                     | 5                               | 4                        | 3                               | 2                               | 1                     | 0                    |
| INTC_CLK_ST<br>OP_ACK | INTC_CLK_ST<br>OP_REQ | RESERVED                        |                          |                                 |                                 |                       |                      |
| R                     | R/W                   | NONE                            |                          |                                 |                                 |                       |                      |
| 0h                    | 0h                    | 0h                              |                          |                                 |                                 |                       |                      |

**Table 4-949. ICSSM\_PR1\_CFG\_SLV\_CGR\_REG Register Field Descriptions**

| Bit   | Field                       | Type | Reset | Description |
|-------|-----------------------------|------|-------|-------------|
| 31    | ICSS_STOP_ACK               | R/W  | 1h    |             |
| 30    | ICSS_STOP_REQ               | R    | 0h    |             |
| 29    | ICSS_PWR_IDLE               | R/W  | 1h    |             |
| 28:22 | RESERVED                    | NONE | 0h    | Reserved    |
| 21    | BOTTOM_HALF_CLK_GA<br>TE_EN | R/W  | 1h    |             |
| 20    | TOP_HALF_CLK_GATE_<br>EN    | R/W  | 1h    |             |
| 19    | AUTO_SLICE1_CLK_GAT<br>E_EN | R/W  | 0h    |             |
| 18    | AUTO_SLICE0_CLK_GAT<br>E_EN | R/W  | 0h    |             |
| 17    | IEP_CLK_EN                  | R/W  | 1h    |             |
| 16    | IEP_CLK_STOP_ACK            | R    | 0h    |             |
| 15    | IEP_CLK_STOP_REQ            | R/W  | 0h    |             |
| 14    | ECAP_CLK_EN                 | R/W  | 1h    |             |

**Table 4-949. ICSSM\_PR1\_CFG\_SLV\_CGR\_REG Register Field Descriptions (continued)**

| Bit | Field             | Type | Reset | Description |
|-----|-------------------|------|-------|-------------|
| 13  | ECAP_CLK_STOP_ACK | R    | 0h    |             |
| 12  | ECAP_CLK_STOP_REQ | R/W  | 0h    |             |
| 11  | UART_CLK_EN       | R/W  | 1h    |             |
| 10  | UART_CLK_STOP_ACK | R    | 0h    |             |
| 9   | UART_CLK_STOP_REQ | R/W  | 0h    |             |
| 8   | INTC_CLK_EN       | R/W  | 1h    |             |
| 7   | INTC_CLK_STOP_ACK | R    | 0h    |             |
| 6   | INTC_CLK_STOP_REQ | R/W  | 0h    |             |
| 5:0 | RESERVED          | NONE | 0h    | Reserved    |

#### 4.2.2.112 ICSSM\_PR1\_CFG\_SLV\_GPECFG0\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_GPECFG0\_REG Register (Offset = 14h) [reset = 23h]

gpecfg0 Register

Return to [Summary Table](#)
**Table 4-950. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6014h       |

**Figure 4-306. ICSSM\_PR1\_CFG\_SLV\_GPECFG0\_REG Name Register**

|                    |                          |                                 |                         |          |    |                                 |                                 |
|--------------------|--------------------------|---------------------------------|-------------------------|----------|----|---------------------------------|---------------------------------|
| 31                 | 30                       | 29                              | 28                      | 27       | 26 | 25                              | 24                              |
| RESERVED           |                          |                                 |                         |          |    |                                 |                                 |
| NONE               |                          |                                 |                         |          |    |                                 |                                 |
| 0h                 |                          |                                 |                         |          |    |                                 |                                 |
| 23                 | 22                       | 21                              | 20                      | 19       | 18 | 17                              | 16                              |
| RESERVED           |                          |                                 |                         |          |    | PRU0_GPO_S<br>HIFT_CLK_DO<br>NE | PRU0_GPO_S<br>HIFT_CLK_HIG<br>H |
| NONE               |                          |                                 |                         |          |    | R/W1C                           | R/W                             |
| 0h                 |                          |                                 |                         |          |    | 0h                              | 0h                              |
| 15                 | 14                       | 13                              | 12                      | 11       | 10 | 9                               | 8                               |
| PRU0_GPO_SHIFT_CNT |                          |                                 |                         |          |    |                                 |                                 |
| R/W                |                          |                                 |                         |          |    |                                 |                                 |
| 0h                 |                          |                                 |                         |          |    |                                 |                                 |
| 7                  | 6                        | 5                               | 4                       | 3        | 2  | 1                               | 0                               |
| RESERVED           | PRU0_GPO_S<br>HIFT_GP_EN | PRU0_GPO_S<br>HIFT_CLK_FR<br>EE | PRU0_GPO_S<br>HIFT_SWAP | RESERVED |    | PRU0_GPI_SHI<br>FT_EN           | PRU0_GPI_SB<br>_P               |
| NONE               | R/W                      | R/W                             | R/W                     | NONE     |    | R/W                             | R/W                             |
| 0h                 | 0h                       | 1h                              | 0h                      | 0h       |    | 1h                              | 1h                              |

**Table 4-952. ICSSM\_PR1\_CFG\_SLV\_GPECFG0\_REG Register Field Descriptions**

| Bit   | Field                   | Type  | Reset | Description |
|-------|-------------------------|-------|-------|-------------|
| 31:18 | RESERVED                | NONE  | 0h    | Reserved    |
| 17    | PRU0_GPO_SHIFT_CLK_DONE | R/W1C | 0h    |             |
| 16    | PRU0_GPO_SHIFT_CLK_HIGH | R/W   | 0h    |             |
| 15:8  | PRU0_GPO_SHIFT_CNT      | R/W   | 0h    |             |
| 7     | RESERVED                | NONE  | 0h    | Reserved    |
| 6     | PRU0_GPO_SHIFT_GP_EN    | R/W   | 0h    |             |
| 5     | PRU0_GPO_SHIFT_CLK_FREE | R/W   | 1h    |             |
| 4     | PRU0_GPO_SHIFT_SWAP     | R/W   | 0h    |             |
| 3:2   | RESERVED                | NONE  | 0h    | Reserved    |
| 1     | PRU0_GPI_SHIFT_EN       | R/W   | 1h    |             |
| 0     | PRU0_GPI_SB_P           | R/W   | 1h    |             |

#### 4.2.2.113 ICSSM\_PR1\_CFG\_SLV\_GPECFG1\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_GPECFG1\_REG Register (Offset = 18h) [reset = 23h]

gpecfg1 Register

Return to [Summary Table](#)
**Table 4-953. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6018h       |

**Figure 4-307. ICSSM\_PR1\_CFG\_SLV\_GPECFG1\_REG Name Register**

|                    |                              |                                 |                         |          |    |                                 |                                 |
|--------------------|------------------------------|---------------------------------|-------------------------|----------|----|---------------------------------|---------------------------------|
| 31                 | 30                           | 29                              | 28                      | 27       | 26 | 25                              | 24                              |
| RESERVED           |                              |                                 |                         |          |    |                                 |                                 |
| NONE               |                              |                                 |                         |          |    |                                 |                                 |
| 0h                 |                              |                                 |                         |          |    |                                 |                                 |
| 23                 | 22                           | 21                              | 20                      | 19       | 18 | 17                              | 16                              |
| RESERVED           |                              |                                 |                         |          |    | PRU1_GPO_S<br>HIFT_CLK_D<br>ONE | PRU1_GPO_S<br>HIFT_CLK_H<br>IGH |
| NONE               |                              |                                 |                         |          |    | R/W1C                           | R/W                             |
| 0h                 |                              |                                 |                         |          |    | 0h                              | 0h                              |
| 15                 | 14                           | 13                              | 12                      | 11       | 10 | 9                               | 8                               |
| PRU1_GPO_SHIFT_CNT |                              |                                 |                         |          |    |                                 |                                 |
| R/W                |                              |                                 |                         |          |    |                                 |                                 |
| 0h                 |                              |                                 |                         |          |    |                                 |                                 |
| 7                  | 6                            | 5                               | 4                       | 3        | 2  | 1                               | 0                               |
| RESERVED           | PRU1_GPO_S<br>HIFT_GP_E<br>N | PRU1_GPO_S<br>HIFT_CLK_F<br>REE | PRU1_GPO_S<br>HIFT_SWAP | RESERVED |    | PRU1_GPI_SH<br>IFT_EN           | PRU1_GPI_SB<br>_P               |
| NONE               | R/W                          | R/W                             | R/W                     | NONE     |    | R/W                             | R/W                             |
| 0h                 | 0h                           | 1h                              | 0h                      | 0h       |    | 1h                              | 1h                              |

**Table 4-955. ICSSM\_PR1\_CFG\_SLV\_GPECFG1\_REG Register Field Descriptions**

| Bit   | Field                   | Type  | Reset | Description |
|-------|-------------------------|-------|-------|-------------|
| 31:18 | RESERVED                | NONE  | 0h    | Reserved    |
| 17    | PRU1_GPO_SHIFT_CLK_DONE | R/W1C | 0h    |             |
| 16    | PRU1_GPO_SHIFT_CLK_HIGH | R/W   | 0h    |             |
| 15:8  | PRU1_GPO_SHIFT_CNT      | R/W   | 0h    |             |
| 7     | RESERVED                | NONE  | 0h    | Reserved    |
| 6     | PRU1_GPO_SHIFT_GP_EN    | R/W   | 0h    |             |
| 5     | PRU1_GPO_SHIFT_CLK_FREE | R/W   | 1h    |             |
| 4     | PRU1_GPO_SHIFT_SWAP     | R/W   | 0h    |             |
| 3:2   | RESERVED                | NONE  | 0h    | Reserved    |
| 1     | PRU1_GPI_SHIFT_EN       | R/W   | 1h    |             |
| 0     | PRU1_GPI_SB_P           | R/W   | 1h    |             |

#### 4.2.2.114 ICSSM\_PR1\_CFG\_SLV\_RESET\_ISO\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_RESET\_ISO\_REG Register (Offset = 1Ch) [reset = 0h]

Reset ISO Register

Return to [Summary Table](#)

**Table 4-956. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 601Ch       |

**Figure 4-308. ICSSM\_PR1\_CFG\_SLV\_RESET\_ISO\_REG Name Register**

|          |    |    |    |    |                    |                   |                   |
|----------|----|----|----|----|--------------------|-------------------|-------------------|
| 31       | 30 | 29 | 28 | 27 | 26                 | 25                | 24                |
| RESERVED |    |    |    |    |                    |                   |                   |
| NONE     |    |    |    |    |                    |                   |                   |
| 0h       |    |    |    |    |                    |                   |                   |
| 23       | 22 | 21 | 20 | 19 | 18                 | 17                | 16                |
| RESERVED |    |    |    |    |                    |                   |                   |
| NONE     |    |    |    |    |                    |                   |                   |
| 0h       |    |    |    |    |                    |                   |                   |
| 15       | 14 | 13 | 12 | 11 | 10                 | 9                 | 8                 |
| RESERVED |    |    |    |    |                    |                   |                   |
| NONE     |    |    |    |    |                    |                   |                   |
| 0h       |    |    |    |    |                    |                   |                   |
| 7        | 6  | 5  | 4  | 3  | 2                  | 1                 | 0                 |
| RESERVED |    |    |    |    | RESET_ISO_E<br>DGE | RESET_ISO_A<br>CK | RESET_ISO_R<br>EQ |
| NONE     |    |    |    |    | W                  | W                 | R/W1C             |
| 0h       |    |    |    |    | 0h                 | 0h                | 0h                |

**Table 4-958. ICSSM\_PR1\_CFG\_SLV\_RESET\_ISO\_REG Register Field Descriptions**

| Bit  | Field          | Type  | Reset | Description |
|------|----------------|-------|-------|-------------|
| 31:3 | RESERVED       | NONE  | 0h    | Reserved    |
| 2    | RESET_ISO_EDGE | W     | 0h    |             |
| 1    | RESET_ISO_ACK  | W     | 0h    |             |
| 0    | RESET_ISO_REQ  | R/W1C | 0h    |             |



#### 4.2.2.115 ICSSM\_PR1\_CFG\_SLV\_MII\_RT\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_MII\_RT\_REG Register (Offset = 2Ch) [reset = 1h]

mii\_rt Register

Return to [Summary Table](#)
**Table 4-959. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 602Ch       |

**Figure 4-309. ICSSM\_PR1\_CFG\_SLV\_MII\_RT\_REG Name Register**

|          |    |    |    |    |    |    |                 |
|----------|----|----|----|----|----|----|-----------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24              |
| RESERVED |    |    |    |    |    |    |                 |
| NONE     |    |    |    |    |    |    |                 |
| 0h       |    |    |    |    |    |    |                 |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16              |
| RESERVED |    |    |    |    |    |    |                 |
| NONE     |    |    |    |    |    |    |                 |
| 0h       |    |    |    |    |    |    |                 |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8               |
| RESERVED |    |    |    |    |    |    |                 |
| NONE     |    |    |    |    |    |    |                 |
| 0h       |    |    |    |    |    |    |                 |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0               |
| RESERVED |    |    |    |    |    |    | MII_RT_EVENT_EN |
| NONE     |    |    |    |    |    |    | R/W             |
| 0h       |    |    |    |    |    |    | 1h              |

**Table 4-961. ICSSM\_PR1\_CFG\_SLV\_MII\_RT\_REG Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description |
|------|-----------------|------|-------|-------------|
| 31:1 | RESERVED        | NONE | 0h    | Reserved    |
| 0    | MII_RT_EVENT_EN | R/W  | 1h    |             |

#### 4.2.2.116 ICSSM\_PR1\_CFG\_SLV\_IEPCLK\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_IEPCLK\_REG Register (Offset = 30h) [reset = 0h]

iepclk Register

Return to [Summary Table](#)
**Table 4-962. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6030h       |

**Figure 4-310. ICSSM\_PR1\_CFG\_SLV\_IEPCLK\_REG Name Register**

|          |    |    |    |    |    |             |                |
|----------|----|----|----|----|----|-------------|----------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25          | 24             |
| RESERVED |    |    |    |    |    |             |                |
| NONE     |    |    |    |    |    |             |                |
| 0h       |    |    |    |    |    |             |                |
| 23       | 22 | 21 | 20 | 19 | 18 | 17          | 16             |
| RESERVED |    |    |    |    |    |             |                |
| NONE     |    |    |    |    |    |             |                |
| 0h       |    |    |    |    |    |             |                |
| 15       | 14 | 13 | 12 | 11 | 10 | 9           | 8              |
| RESERVED |    |    |    |    |    |             |                |
| NONE     |    |    |    |    |    |             |                |
| 0h       |    |    |    |    |    |             |                |
| 7        | 6  | 5  | 4  | 3  | 2  | 1           | 0              |
| RESERVED |    |    |    |    |    | IEP1_SLV_EN | IEP_OCP_CLK_EN |
| NONE     |    |    |    |    |    | R/W         | R/W            |
| 0h       |    |    |    |    |    | 0h          | 0h             |

**Table 4-964. ICSSM\_PR1\_CFG\_SLV\_IEPCLK\_REG Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description |
|------|----------------|------|-------|-------------|
| 31:2 | RESERVED       | NONE | 0h    | Reserved    |
| 1    | IEP1_SLV_EN    | R/W  | 0h    |             |
| 0    | IEP_OCP_CLK_EN | R/W  | 0h    |             |

#### 4.2.2.117 ICSSM\_PR1\_CFG\_SLV\_SPP\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_SPP\_REG Register (Offset = 34h) [reset = 0h]

ppl Register

Return to [Summary Table](#)
**Table 4-965. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6034h       |

**Figure 4-311. ICSSM\_PR1\_CFG\_SLV\_SPP\_REG Name Register**

|          |    |    |    |                  |                   |              |                |
|----------|----|----|----|------------------|-------------------|--------------|----------------|
| 31       | 30 | 29 | 28 | 27               | 26                | 25           | 24             |
| RESERVED |    |    |    |                  |                   |              |                |
| NONE     |    |    |    |                  |                   |              |                |
| 0h       |    |    |    |                  |                   |              |                |
| 23       | 22 | 21 | 20 | 19               | 18                | 17           | 16             |
| RESERVED |    |    |    |                  |                   |              |                |
| NONE     |    |    |    |                  |                   |              |                |
| 0h       |    |    |    |                  |                   |              |                |
| 15       | 14 | 13 | 12 | 11               | 10                | 9            | 8              |
| RESERVED |    |    |    |                  |                   |              |                |
| NONE     |    |    |    |                  |                   |              |                |
| 0h       |    |    |    |                  |                   |              |                |
| 7        | 6  | 5  | 4  | 3                | 2                 | 1            | 0              |
| RESERVED |    |    |    | RTU_XFR_SHIFT_EN | XFR_BYTE_SHIFT_EN | XFR_SHIFT_EN | PRU1_PAD_HP_EN |
| NONE     |    |    |    | R/W              | R/W               | R/W          | R/W            |
| 0h       |    |    |    | 0h               | 0h                | 0h           | 0h             |

**Table 4-967. ICSSM\_PR1\_CFG\_SLV\_SPP\_REG Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description |
|------|-------------------|------|-------|-------------|
| 31:4 | RESERVED          | NONE | 0h    | Reserved    |
| 3    | RTU_XFR_SHIFT_EN  | R/W  | 0h    |             |
| 2    | XFR_BYTE_SHIFT_EN | R/W  | 0h    |             |
| 1    | XFR_SHIFT_EN      | R/W  | 0h    |             |
| 0    | PRU1_PAD_HP_EN    | R/W  | 0h    |             |

#### 4.2.2.118 ICSSM\_PR1\_CFG\_SLV\_SPIN\_CFG\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_SPIN\_CFG\_REG Register (Offset = 38h) [reset = 0h]

Spin Lock CFG Register

Return to [Summary Table](#)
**Table 4-968. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6038h       |

**Figure 4-312. ICSSM\_PR1\_CFG\_SLV\_SPIN\_CFG\_REG Name Register**

|          |    |    |    |    |    |    |                      |
|----------|----|----|----|----|----|----|----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                   |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                   |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                    |
| RESERVED |    |    |    |    |    |    |                      |
| NONE     |    |    |    |    |    |    |                      |
| 0h       |    |    |    |    |    |    |                      |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                    |
| RESERVED |    |    |    |    |    |    | SPIN_CLOCK_TX_PRU_EN |
| NONE     |    |    |    |    |    |    | R/W                  |
| 0h       |    |    |    |    |    |    | 0h                   |

**Table 4-970. ICSSM\_PR1\_CFG\_SLV\_SPIN\_CFG\_REG Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description |
|------|----------------------|------|-------|-------------|
| 31:1 | RESERVED             | NONE | 0h    | Reserved    |
| 0    | SPIN_CLOCK_TX_PRU_EN | R/W  | 0h    |             |

#### 4.2.2.119 ICSSM\_PR1\_CFG\_SLV\_CORE\_SYNC\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_CORE\_SYNC\_REG Register (Offset = 3Ch) [reset = 0h]

Core Sync Register

Return to [Summary Table](#)

**Table 4-971. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 603Ch       |

**Figure 4-313. ICSSM\_PR1\_CFG\_SLV\_CORE\_SYNC\_REG Name Register**

|          |    |    |    |    |    |    |                    |
|----------|----|----|----|----|----|----|--------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                 |
| RESERVED |    |    |    |    |    |    |                    |
| NONE     |    |    |    |    |    |    |                    |
| 0h       |    |    |    |    |    |    |                    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
| RESERVED |    |    |    |    |    |    |                    |
| NONE     |    |    |    |    |    |    |                    |
| 0h       |    |    |    |    |    |    |                    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                  |
| RESERVED |    |    |    |    |    |    |                    |
| NONE     |    |    |    |    |    |    |                    |
| 0h       |    |    |    |    |    |    |                    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| RESERVED |    |    |    |    |    |    | CORE_VBUSB_SYNC_EN |
| NONE     |    |    |    |    |    |    | R/W                |
| 0h       |    |    |    |    |    |    | 0h                 |

**Table 4-973. ICSSM\_PR1\_CFG\_SLV\_CORE\_SYNC\_REG Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description |
|------|--------------------|------|-------|-------------|
| 31:1 | RESERVED           | NONE | 0h    | Reserved    |
| 0    | CORE_VBUSB_SYNC_EN | R/W  | 0h    |             |

#### 4.2.2.120 ICSSM\_PR1\_CFG\_SLV\_SA\_MX\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_SA\_MX\_REG Register (Offset = 40h) [reset = 0h]

sa\_mx Register

Return to [Summary Table](#)
**Table 4-974. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6040h       |

**Figure 4-314. ICSSM\_PR1\_CFG\_SLV\_SA\_MX\_REG Name Register**

|            |    |    |    |               |    |               |            |
|------------|----|----|----|---------------|----|---------------|------------|
| 31         | 30 | 29 | 28 | 27            | 26 | 25            | 24         |
| RESERVED   |    |    |    |               |    |               |            |
| NONE       |    |    |    |               |    |               |            |
| 0h         |    |    |    |               |    |               |            |
| 23         | 22 | 21 | 20 | 19            | 18 | 17            | 16         |
| RESERVED   |    |    |    |               |    |               | PWM_EFC_EN |
| NONE       |    |    |    |               |    |               | R/W        |
| 0h         |    |    |    |               |    |               | 0h         |
| 15         | 14 | 13 | 12 | 11            | 10 | 9             | 8          |
| RESERVED   |    |    |    | PWM3_REMAP_EN |    | PWM0_REMAP_EN |            |
| NONE       |    |    |    | R/W           |    | R/W           |            |
| 0h         |    |    |    | 0h            |    | 0h            |            |
| 7          | 6  | 5  | 4  | 3             | 2  | 1             | 0          |
| SA_MUX_SEL |    |    |    |               |    |               |            |
| R/W        |    |    |    |               |    |               |            |
| 0h         |    |    |    |               |    |               |            |

**Table 4-976. ICSSM\_PR1\_CFG\_SLV\_SA\_MX\_REG Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description |
|-------|---------------|------|-------|-------------|
| 31:17 | RESERVED      | NONE | 0h    | Reserved    |
| 16    | PWM_EFC_EN    | R/W  | 0h    |             |
| 15:12 | RESERVED      | NONE | 0h    | Reserved    |
| 11:10 | PWM3_REMAP_EN | R/W  | 0h    |             |
| 9:8   | PWM0_REMAP_EN | R/W  | 0h    |             |
| 7:0   | SA_MUX_SEL    | R/W  | 0h    |             |

#### 4.2.2.121 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_DIV\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_DIV\_REG Register (Offset = 44h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-977. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6044h       |

**Figure 4-315. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_DIV\_REG Name Register**

| 31                         | 30             | 29 | 28 | 27 | 26                             | 25                 | 24                               |
|----------------------------|----------------|----|----|----|--------------------------------|--------------------|----------------------------------|
| PRU0_SD_MAN_REC_CLK_PERIOD |                |    |    |    |                                |                    |                                  |
| R                          |                |    |    |    |                                |                    |                                  |
| 0h                         |                |    |    |    |                                |                    |                                  |
| 23                         | 22             | 21 | 20 | 19 | 18                             | 17                 | 16                               |
| RESERVED                   |                |    |    |    |                                |                    | PRU0_SD_MA<br>N_CLK_CAL_D<br>ONE |
| NONE                       |                |    |    |    |                                |                    | R                                |
| 0h                         |                |    |    |    |                                |                    | 0h                               |
| 15                         | 14             | 13 | 12 | 11 | 10                             | 9                  | 8                                |
| PRU0_SD_MA<br>N_STATUS     | PRU0_SD_CH_SEL |    |    |    | PRU0_SD_MA<br>N_NV_DATA_E<br>N | PRU0_SD_MA<br>N_EN | PRU0_SD_SHA<br>RE_EN             |
| R                          | R/W            |    |    |    | R/W                            | R/W                | R/W                              |
| 0h                         | 0h             |    |    |    | 0h                             | 0h                 | 0h                               |
| 7                          | 6              | 5  | 4  | 3  | 2                              | 1                  | 0                                |
| RESERVED                   |                |    |    |    |                                |                    |                                  |
| NONE                       |                |    |    |    |                                |                    |                                  |
| 0h                         |                |    |    |    |                                |                    |                                  |

**Table 4-979. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_DIV\_REG Register Field Descriptions**

| Bit   | Field                      | Type | Reset | Description |
|-------|----------------------------|------|-------|-------------|
| 31:24 | PRU0_SD_MAN_REC_CLK_PERIOD | R    | 0h    |             |
| 23:17 | RESERVED                   | NONE | 0h    | Reserved    |
| 16    | PRU0_SD_MAN_CLK_CAL_DONE   | R    | 0h    |             |
| 15    | PRU0_SD_MAN_STATUS         | R    | 0h    |             |
| 14:11 | PRU0_SD_CH_SEL             | R/W  | 0h    |             |
| 10    | PRU0_SD_MAN_NV_DATA_EN     | R/W  | 0h    |             |
| 9     | PRU0_SD_MAN_EN             | R/W  | 0h    |             |
| 8     | PRU0_SD_SHARE_EN           | R/W  | 0h    |             |
| 7:0   | RESERVED                   | NONE | 0h    | Reserved    |

#### 4.2.2.122 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG0 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG0 Register (Offset = 48h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-980. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6048h       |

**Figure 4-316. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG0 Name Register**

|                          |                    |                          |    |          |                  |                    |    |
|--------------------------|--------------------|--------------------------|----|----------|------------------|--------------------|----|
| 31                       | 30                 | 29                       | 28 | 27       | 26               | 25                 | 24 |
| RESERVED                 |                    |                          |    |          |                  |                    |    |
| NONE                     |                    |                          |    |          |                  |                    |    |
| 0h                       |                    |                          |    |          |                  |                    |    |
| 23                       | 22                 | 21                       | 20 | 19       | 18               | 17                 | 16 |
| RESERVED                 | PRU0_FD_ZERO_MAX_0 | PRU0_FD_ZERO_MAX_LIMIT_0 |    |          |                  | PRU0_FD_ZERO_MIN_0 |    |
| NONE                     | R/W1C              | R/W                      |    |          |                  | R/W1C              |    |
| 0h                       | 0h                 | 0h                       |    |          |                  | 0h                 |    |
| 15                       | 14                 | 13                       | 12 | 11       | 10               | 9                  | 8  |
| PRU0_FD_ZERO_MIN_LIMIT_0 |                    |                          |    |          | RESERVED         |                    |    |
| R/W                      |                    |                          |    |          | NONE             |                    |    |
| 0h                       |                    |                          |    |          | 0h               |                    |    |
| 7                        | 6                  | 5                        | 4  | 3        | 2                | 1                  | 0  |
| RESERVED                 |                    | PRU0_SD_ACC_SEL0         |    | RESERVED | PRU0_SD_CLK_INV0 | PRU0_SD_CLK_SEL0   |    |
| NONE                     |                    | R/W                      |    | NONE     | R/W              | R/W                |    |
| 0h                       |                    | 0h                       |    | 0h       | 0h               | 0h                 |    |

**Table 4-982. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG0 Register Field Descriptions**

| Bit   | Field                    | Type  | Reset | Description |
|-------|--------------------------|-------|-------|-------------|
| 31:23 | RESERVED                 | NONE  | 0h    | Reserved    |
| 22    | PRU0_FD_ZERO_MAX_0       | R/W1C | 0h    |             |
| 21:17 | PRU0_FD_ZERO_MAX_LIMIT_0 | R/W   | 0h    |             |
| 16    | PRU0_FD_ZERO_MIN_0       | R/W1C | 0h    |             |
| 15:11 | PRU0_FD_ZERO_MIN_LIMIT_0 | R/W   | 0h    |             |
| 10:6  | RESERVED                 | NONE  | 0h    | Reserved    |
| 5:4   | PRU0_SD_ACC_SEL0         | R/W   | 0h    |             |
| 3     | RESERVED                 | NONE  | 0h    | Reserved    |
| 2     | PRU0_SD_CLK_INV0         | R/W   | 0h    |             |
| 1:0   | PRU0_SD_CLK_SEL0         | R/W   | 0h    |             |



#### 4.2.2.123 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG0 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG0 Register (Offset = 4Ch) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-983. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 604Ch       |

**Figure 4-317. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG0 Name Register**

|                         |                       |                         |    |    |                       |                       |    |
|-------------------------|-----------------------|-------------------------|----|----|-----------------------|-----------------------|----|
| 31                      | 30                    | 29                      | 28 | 27 | 26                    | 25                    | 24 |
| RESERVED                |                       |                         |    |    |                       |                       |    |
| NONE                    |                       |                         |    |    |                       |                       |    |
| 0h                      |                       |                         |    |    |                       |                       |    |
| 23                      | 22                    | 21                      | 20 | 19 | 18                    | 17                    | 16 |
| PRU0_FD_EN_0            | PRU0_FD_ON<br>E_MAX_0 | PRU0_FD_ONE_MAX_LIMIT_0 |    |    |                       | PRU0_FD_ON<br>E_MIN_0 |    |
| R/W                     | R/W1C                 | R/W                     |    |    |                       | R/W1C                 |    |
| 0h                      | 0h                    | 0h                      |    |    |                       | 0h                    |    |
| 15                      | 14                    | 13                      | 12 | 11 | 10                    | 9                     | 8  |
| PRU0_FD_ONE_MIN_LIMIT_0 |                       |                         |    |    | PRU0_FD_WINDOW_SIZE_0 |                       |    |
| R/W                     |                       |                         |    |    | R/W                   |                       |    |
| 0h                      |                       |                         |    |    | 0h                    |                       |    |
| 7                       | 6                     | 5                       | 4  | 3  | 2                     | 1                     | 0  |
| PRU0_SD_SAMPLE_SIZE0    |                       |                         |    |    |                       |                       |    |
| R/W                     |                       |                         |    |    |                       |                       |    |
| 0h                      |                       |                         |    |    |                       |                       |    |

**Table 4-985. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG0 Register Field Descriptions**

| Bit   | Field                       | Type  | Reset | Description |
|-------|-----------------------------|-------|-------|-------------|
| 31:24 | RESERVED                    | NONE  | 0h    | Reserved    |
| 23    | PRU0_FD_EN_0                | R/W   | 0h    |             |
| 22    | PRU0_FD_ONE_MAX_0           | R/W1C | 0h    |             |
| 21:17 | PRU0_FD_ONE_MAX_LI<br>MIT_0 | R/W   | 0h    |             |
| 16    | PRU0_FD_ONE_MIN_0           | R/W1C | 0h    |             |
| 15:11 | PRU0_FD_ONE_MIN_LIM<br>IT_0 | R/W   | 0h    |             |
| 10:8  | PRU0_FD_WINDOW_SIZ<br>E_0   | R/W   | 0h    |             |
| 7:0   | PRU0_SD_SAMPLE_SIZ<br>E0    | R/W   | 0h    |             |

#### 4.2.2.124 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG1 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG1 Register (Offset = 50h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-986. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6050h       |

**Figure 4-318. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG1 Name Register**

|                          |                        |                          |    |          |                      |                        |    |
|--------------------------|------------------------|--------------------------|----|----------|----------------------|------------------------|----|
| 31                       | 30                     | 29                       | 28 | 27       | 26                   | 25                     | 24 |
| RESERVED                 |                        |                          |    |          |                      |                        |    |
| NONE                     |                        |                          |    |          |                      |                        |    |
| 0h                       |                        |                          |    |          |                      |                        |    |
| 23                       | 22                     | 21                       | 20 | 19       | 18                   | 17                     | 16 |
| RESERVED                 | PRU0_FD_ZER<br>O_MAX_1 | PRU0_FD_ZERO_MAX_LIMIT_1 |    |          |                      | PRU0_FD_ZER<br>O_MIN_1 |    |
| NONE                     | R/W1C                  | R/W                      |    |          |                      | R/W1C                  |    |
| 0h                       | 0h                     | 0h                       |    |          |                      | 0h                     |    |
| 15                       | 14                     | 13                       | 12 | 11       | 10                   | 9                      | 8  |
| PRU0_FD_ZERO_MIN_LIMIT_1 |                        |                          |    |          | RESERVED             |                        |    |
| R/W                      |                        |                          |    |          | NONE                 |                        |    |
| 0h                       |                        |                          |    |          | 0h                   |                        |    |
| 7                        | 6                      | 5                        | 4  | 3        | 2                    | 1                      | 0  |
| RESERVED                 |                        | PRU0_SD_ACC_SEL1         |    | RESERVED | PRU0_SD_CLK<br>_INV1 | PRU0_SD_CLK_SEL1       |    |
| NONE                     |                        | R/W                      |    | NONE     | R/W                  | R/W                    |    |
| 0h                       |                        | 0h                       |    | 0h       | 0h                   | 0h                     |    |

**Table 4-988. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG1 Register Field Descriptions**

| Bit   | Field                        | Type  | Reset | Description |
|-------|------------------------------|-------|-------|-------------|
| 31:23 | RESERVED                     | NONE  | 0h    | Reserved    |
| 22    | PRU0_FD_ZERO_MAX_1           | R/W1C | 0h    |             |
| 21:17 | PRU0_FD_ZERO_MAX_L<br>IMIT_1 | R/W   | 0h    |             |
| 16    | PRU0_FD_ZERO_MIN_1           | R/W1C | 0h    |             |
| 15:11 | PRU0_FD_ZERO_MIN_LI<br>MIT_1 | R/W   | 0h    |             |
| 10:6  | RESERVED                     | NONE  | 0h    | Reserved    |
| 5:4   | PRU0_SD_ACC_SEL1             | R/W   | 0h    |             |
| 3     | RESERVED                     | NONE  | 0h    | Reserved    |
| 2     | PRU0_SD_CLK_INV1             | R/W   | 0h    |             |
| 1:0   | PRU0_SD_CLK_SEL1             | R/W   | 0h    |             |

#### 4.2.2.125 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG1 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG1 Register (Offset = 54h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-989. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6054h       |

**Figure 4-319. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG1 Name Register**

|                         |                    |                         |    |                       |    |                    |    |
|-------------------------|--------------------|-------------------------|----|-----------------------|----|--------------------|----|
| 31                      | 30                 | 29                      | 28 | 27                    | 26 | 25                 | 24 |
| RESERVED                |                    |                         |    |                       |    |                    |    |
| NONE                    |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |
| 23                      | 22                 | 21                      | 20 | 19                    | 18 | 17                 | 16 |
| PRU0_FD_EN_1            | PRU0_FD_ON E_MAX_1 | PRU0_FD_ONE_MAX_LIMIT_1 |    |                       |    | PRU0_FD_ON E_MIN_1 |    |
| R/W                     | R/W1C              | R/W                     |    |                       |    | R/W1C              |    |
| 0h                      | 0h                 | 0h                      |    |                       |    | 0h                 |    |
| 15                      | 14                 | 13                      | 12 | 11                    | 10 | 9                  | 8  |
| PRU0_FD_ONE_MIN_LIMIT_1 |                    |                         |    | PRU0_FD_WINDOW_SIZE_1 |    |                    |    |
| R/W                     |                    |                         |    | R/W                   |    |                    |    |
| 0h                      |                    |                         |    | 0h                    |    |                    |    |
| 7                       | 6                  | 5                       | 4  | 3                     | 2  | 1                  | 0  |
| PRU0_SD_SAMPLE_SIZE1    |                    |                         |    |                       |    |                    |    |
| R/W                     |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |

**Table 4-991. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG1 Register Field Descriptions**

| Bit   | Field                    | Type  | Reset | Description |
|-------|--------------------------|-------|-------|-------------|
| 31:24 | RESERVED                 | NONE  | 0h    | Reserved    |
| 23    | PRU0_FD_EN_1             | R/W   | 0h    |             |
| 22    | PRU0_FD_ONE_MAX_1        | R/W1C | 0h    |             |
| 21:17 | PRU0_FD_ONE_MAX_LI MIT_1 | R/W   | 0h    |             |
| 16    | PRU0_FD_ONE_MIN_1        | R/W1C | 0h    |             |
| 15:11 | PRU0_FD_ONE_MIN_LIM IT_1 | R/W   | 0h    |             |
| 10:8  | PRU0_FD_WINDOW_SIZ E_1   | R/W   | 0h    |             |
| 7:0   | PRU0_SD_SAMPLE_SIZ E1    | R/W   | 0h    |             |

#### 4.2.2.126 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG2 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG2 Register (Offset = 58h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-992. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6058h       |

**Figure 4-320. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG2 Name Register**

|                          |                    |                          |    |          |                  |                    |    |
|--------------------------|--------------------|--------------------------|----|----------|------------------|--------------------|----|
| 31                       | 30                 | 29                       | 28 | 27       | 26               | 25                 | 24 |
| RESERVED                 |                    |                          |    |          |                  |                    |    |
| NONE                     |                    |                          |    |          |                  |                    |    |
| 0h                       |                    |                          |    |          |                  |                    |    |
| 23                       | 22                 | 21                       | 20 | 19       | 18               | 17                 | 16 |
| RESERVED                 | PRU0_FD_ZERO_MAX_2 | PRU0_FD_ZERO_MAX_LIMIT_2 |    |          |                  | PRU0_FD_ZERO_MIN_2 |    |
| NONE                     | R/W1C              | R/W                      |    |          |                  | R/W1C              |    |
| 0h                       | 0h                 | 0h                       |    |          |                  | 0h                 |    |
| 15                       | 14                 | 13                       | 12 | 11       | 10               | 9                  | 8  |
| PRU0_FD_ZERO_MIN_LIMIT_2 |                    |                          |    |          | RESERVED         |                    |    |
| R/W                      |                    |                          |    |          | NONE             |                    |    |
| 0h                       |                    |                          |    |          | 0h               |                    |    |
| 7                        | 6                  | 5                        | 4  | 3        | 2                | 1                  | 0  |
| RESERVED                 |                    | PRU0_SD_ACC_SEL2         |    | RESERVED | PRU0_SD_CLK_INV2 | PRU0_SD_CLK_SEL2   |    |
| NONE                     |                    | R/W                      |    | NONE     | R/W              | R/W                |    |
| 0h                       |                    | 0h                       |    | 0h       | 0h               | 0h                 |    |

**Table 4-994. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG2 Register Field Descriptions**

| Bit   | Field                    | Type  | Reset | Description |
|-------|--------------------------|-------|-------|-------------|
| 31:23 | RESERVED                 | NONE  | 0h    | Reserved    |
| 22    | PRU0_FD_ZERO_MAX_2       | R/W1C | 0h    |             |
| 21:17 | PRU0_FD_ZERO_MAX_LIMIT_2 | R/W   | 0h    |             |
| 16    | PRU0_FD_ZERO_MIN_2       | R/W1C | 0h    |             |
| 15:11 | PRU0_FD_ZERO_MIN_LIMIT_2 | R/W   | 0h    |             |
| 10:6  | RESERVED                 | NONE  | 0h    | Reserved    |
| 5:4   | PRU0_SD_ACC_SEL2         | R/W   | 0h    |             |
| 3     | RESERVED                 | NONE  | 0h    | Reserved    |
| 2     | PRU0_SD_CLK_INV2         | R/W   | 0h    |             |
| 1:0   | PRU0_SD_CLK_SEL2         | R/W   | 0h    |             |

#### 4.2.2.127 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG2 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG2 Register (Offset = 5Ch) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-995. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 605Ch       |

**Figure 4-321. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG2 Name Register**

|                         |                    |                         |    |                       |    |                    |    |
|-------------------------|--------------------|-------------------------|----|-----------------------|----|--------------------|----|
| 31                      | 30                 | 29                      | 28 | 27                    | 26 | 25                 | 24 |
| RESERVED                |                    |                         |    |                       |    |                    |    |
| NONE                    |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |
| 23                      | 22                 | 21                      | 20 | 19                    | 18 | 17                 | 16 |
| PRU0_FD_EN_2            | PRU0_FD_ON_E_MAX_2 | PRU0_FD_ONE_MAX_LIMIT_2 |    |                       |    | PRU0_FD_ON_E_MIN_2 |    |
| R/W                     | R/W1C              | R/W                     |    |                       |    | R/W1C              |    |
| 0h                      | 0h                 | 0h                      |    |                       |    | 0h                 |    |
| 15                      | 14                 | 13                      | 12 | 11                    | 10 | 9                  | 8  |
| PRU0_FD_ONE_MIN_LIMIT_2 |                    |                         |    | PRU0_FD_WINDOW_SIZE_2 |    |                    |    |
| R/W                     |                    |                         |    | R/W                   |    |                    |    |
| 0h                      |                    |                         |    | 0h                    |    |                    |    |
| 7                       | 6                  | 5                       | 4  | 3                     | 2  | 1                  | 0  |
| PRU0_SD_SAMPLE_SIZE2    |                    |                         |    |                       |    |                    |    |
| R/W                     |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |

**Table 4-997. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG2 Register Field Descriptions**

| Bit   | Field                   | Type  | Reset | Description |
|-------|-------------------------|-------|-------|-------------|
| 31:24 | RESERVED                | NONE  | 0h    | Reserved    |
| 23    | PRU0_FD_EN_2            | R/W   | 0h    |             |
| 22    | PRU0_FD_ONE_MAX_2       | R/W1C | 0h    |             |
| 21:17 | PRU0_FD_ONE_MAX_LIMIT_2 | R/W   | 0h    |             |
| 16    | PRU0_FD_ONE_MIN_2       | R/W1C | 0h    |             |
| 15:11 | PRU0_FD_ONE_MIN_LIMIT_2 | R/W   | 0h    |             |
| 10:8  | PRU0_FD_WINDOW_SIZE_2   | R/W   | 0h    |             |
| 7:0   | PRU0_SD_SAMPLE_SIZE2    | R/W   | 0h    |             |

#### 4.2.2.128 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG3 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG3 Register (Offset = 60h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-998. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6060h       |

**Figure 4-322. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG3 Name Register**

|                          |                        |                          |    |          |                      |                        |    |
|--------------------------|------------------------|--------------------------|----|----------|----------------------|------------------------|----|
| 31                       | 30                     | 29                       | 28 | 27       | 26                   | 25                     | 24 |
| RESERVED                 |                        |                          |    |          |                      |                        |    |
| NONE                     |                        |                          |    |          |                      |                        |    |
| 0h                       |                        |                          |    |          |                      |                        |    |
| 23                       | 22                     | 21                       | 20 | 19       | 18                   | 17                     | 16 |
| RESERVED                 | PRU0_FD_ZER<br>O_MAX_3 | PRU0_FD_ZERO_MAX_LIMIT_3 |    |          |                      | PRU0_FD_ZER<br>O_MIN_3 |    |
| NONE                     | R/W1C                  | R/W                      |    |          |                      | R/W1C                  |    |
| 0h                       | 0h                     | 0h                       |    |          |                      | 0h                     |    |
| 15                       | 14                     | 13                       | 12 | 11       | 10                   | 9                      | 8  |
| PRU0_FD_ZERO_MIN_LIMIT_3 |                        |                          |    |          | RESERVED             |                        |    |
| R/W                      |                        |                          |    |          | NONE                 |                        |    |
| 0h                       |                        |                          |    |          | 0h                   |                        |    |
| 7                        | 6                      | 5                        | 4  | 3        | 2                    | 1                      | 0  |
| RESERVED                 |                        | PRU0_SD_ACC_SEL3         |    | RESERVED | PRU0_SD_CLK<br>_INV3 | PRU0_SD_CLK_SEL3       |    |
| NONE                     |                        | R/W                      |    | NONE     | R/W                  | R/W                    |    |
| 0h                       |                        | 0h                       |    | 0h       | 0h                   | 0h                     |    |

**Table 4-1000. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG3 Register Field Descriptions**

| Bit   | Field                        | Type  | Reset | Description |
|-------|------------------------------|-------|-------|-------------|
| 31:23 | RESERVED                     | NONE  | 0h    | Reserved    |
| 22    | PRU0_FD_ZERO_MAX_3           | R/W1C | 0h    |             |
| 21:17 | PRU0_FD_ZERO_MAX_L<br>IMIT_3 | R/W   | 0h    |             |
| 16    | PRU0_FD_ZERO_MIN_3           | R/W1C | 0h    |             |
| 15:11 | PRU0_FD_ZERO_MIN_LI<br>MIT_3 | R/W   | 0h    |             |
| 10:6  | RESERVED                     | NONE  | 0h    | Reserved    |
| 5:4   | PRU0_SD_ACC_SEL3             | R/W   | 0h    |             |
| 3     | RESERVED                     | NONE  | 0h    | Reserved    |
| 2     | PRU0_SD_CLK_INV3             | R/W   | 0h    |             |
| 1:0   | PRU0_SD_CLK_SEL3             | R/W   | 0h    |             |

#### 4.2.2.129 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG3 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG3 Register (Offset = 64h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1001. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6064h       |

**Figure 4-323. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG3 Name Register**

|                         |                    |                         |    |                       |    |                    |    |
|-------------------------|--------------------|-------------------------|----|-----------------------|----|--------------------|----|
| 31                      | 30                 | 29                      | 28 | 27                    | 26 | 25                 | 24 |
| RESERVED                |                    |                         |    |                       |    |                    |    |
| NONE                    |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |
| 23                      | 22                 | 21                      | 20 | 19                    | 18 | 17                 | 16 |
| PRU0_FD_EN_3            | PRU0_FD_ON_E_MAX_3 | PRU0_FD_ONE_MAX_LIMIT_3 |    |                       |    | PRU0_FD_ON_E_MIN_3 |    |
| R/W                     | R/W1C              | R/W                     |    |                       |    | R/W1C              |    |
| 0h                      | 0h                 | 0h                      |    |                       |    | 0h                 |    |
| 15                      | 14                 | 13                      | 12 | 11                    | 10 | 9                  | 8  |
| PRU0_FD_ONE_MIN_LIMIT_3 |                    |                         |    | PRU0_FD_WINDOW_SIZE_3 |    |                    |    |
| R/W                     |                    |                         |    | R/W                   |    |                    |    |
| 0h                      |                    |                         |    | 0h                    |    |                    |    |
| 7                       | 6                  | 5                       | 4  | 3                     | 2  | 1                  | 0  |
| PRU0_SD_SAMPLE_SIZE3    |                    |                         |    |                       |    |                    |    |
| R/W                     |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |

**Table 4-1003. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG3 Register Field Descriptions**

| Bit   | Field                   | Type  | Reset | Description |
|-------|-------------------------|-------|-------|-------------|
| 31:24 | RESERVED                | NONE  | 0h    | Reserved    |
| 23    | PRU0_FD_EN_3            | R/W   | 0h    |             |
| 22    | PRU0_FD_ONE_MAX_3       | R/W1C | 0h    |             |
| 21:17 | PRU0_FD_ONE_MAX_LIMIT_3 | R/W   | 0h    |             |
| 16    | PRU0_FD_ONE_MIN_3       | R/W1C | 0h    |             |
| 15:11 | PRU0_FD_ONE_MIN_LIMIT_3 | R/W   | 0h    |             |
| 10:8  | PRU0_FD_WINDOW_SIZE_3   | R/W   | 0h    |             |
| 7:0   | PRU0_SD_SAMPLE_SIZE3    | R/W   | 0h    |             |

#### 4.2.2.130 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG4 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG4 Register (Offset = 68h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1004. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6068h       |

**Figure 4-324. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG4 Name Register**

|                          |                    |                          |    |          |                  |                    |    |
|--------------------------|--------------------|--------------------------|----|----------|------------------|--------------------|----|
| 31                       | 30                 | 29                       | 28 | 27       | 26               | 25                 | 24 |
| RESERVED                 |                    |                          |    |          |                  |                    |    |
| NONE                     |                    |                          |    |          |                  |                    |    |
| 0h                       |                    |                          |    |          |                  |                    |    |
| 23                       | 22                 | 21                       | 20 | 19       | 18               | 17                 | 16 |
| RESERVED                 | PRU0_FD_ZERO_MAX_4 | PRU0_FD_ZERO_MAX_LIMIT_4 |    |          |                  | PRU0_FD_ZERO_MIN_4 |    |
| NONE                     | R/W1C              | R/W                      |    |          |                  | R/W1C              |    |
| 0h                       | 0h                 | 0h                       |    |          |                  | 0h                 |    |
| 15                       | 14                 | 13                       | 12 | 11       | 10               | 9                  | 8  |
| PRU0_FD_ZERO_MIN_LIMIT_4 |                    |                          |    |          | RESERVED         |                    |    |
| R/W                      |                    |                          |    |          | NONE             |                    |    |
| 0h                       |                    |                          |    |          | 0h               |                    |    |
| 7                        | 6                  | 5                        | 4  | 3        | 2                | 1                  | 0  |
| RESERVED                 |                    | PRU0_SD_ACC_SEL4         |    | RESERVED | PRU0_SD_CLK_INV4 | PRU0_SD_CLK_SEL4   |    |
| NONE                     |                    | R/W                      |    | NONE     | R/W              | R/W                |    |
| 0h                       |                    | 0h                       |    | 0h       | 0h               | 0h                 |    |

**Table 4-1006. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG4 Register Field Descriptions**

| Bit   | Field                    | Type  | Reset | Description |
|-------|--------------------------|-------|-------|-------------|
| 31:23 | RESERVED                 | NONE  | 0h    | Reserved    |
| 22    | PRU0_FD_ZERO_MAX_4       | R/W1C | 0h    |             |
| 21:17 | PRU0_FD_ZERO_MAX_LIMIT_4 | R/W   | 0h    |             |
| 16    | PRU0_FD_ZERO_MIN_4       | R/W1C | 0h    |             |
| 15:11 | PRU0_FD_ZERO_MIN_LIMIT_4 | R/W   | 0h    |             |
| 10:6  | RESERVED                 | NONE  | 0h    | Reserved    |
| 5:4   | PRU0_SD_ACC_SEL4         | R/W   | 0h    |             |
| 3     | RESERVED                 | NONE  | 0h    | Reserved    |
| 2     | PRU0_SD_CLK_INV4         | R/W   | 0h    |             |
| 1:0   | PRU0_SD_CLK_SEL4         | R/W   | 0h    |             |



#### 4.2.2.131 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG4 Register

#### 1 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG4 Register (Offset = 6Ch) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1007. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 606Ch       |

**Figure 4-325. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG4 Name Register**

|                         |                       |                         |    |                       |    |                       |    |
|-------------------------|-----------------------|-------------------------|----|-----------------------|----|-----------------------|----|
| 31                      | 30                    | 29                      | 28 | 27                    | 26 | 25                    | 24 |
| RESERVED                |                       |                         |    |                       |    |                       |    |
| NONE                    |                       |                         |    |                       |    |                       |    |
| 0h                      |                       |                         |    |                       |    |                       |    |
| 23                      | 22                    | 21                      | 20 | 19                    | 18 | 17                    | 16 |
| PRU0_FD_EN_4            | PRU0_FD_ON<br>E_MAX_4 | PRU0_FD_ONE_MAX_LIMIT_4 |    |                       |    | PRU0_FD_ON<br>E_MIN_4 |    |
| R/W                     | R/W1C                 | R/W                     |    |                       |    | R/W1C                 |    |
| 0h                      | 0h                    | 0h                      |    |                       |    | 0h                    |    |
| 15                      | 14                    | 13                      | 12 | 11                    | 10 | 9                     | 8  |
| PRU0_FD_ONE_MIN_LIMIT_4 |                       |                         |    | PRU0_FD_WINDOW_SIZE_4 |    |                       |    |
| R/W                     |                       |                         |    | R/W                   |    |                       |    |
| 0h                      |                       |                         |    | 0h                    |    |                       |    |
| 7                       | 6                     | 5                       | 4  | 3                     | 2  | 1                     | 0  |
| PRU0_SD_SAMPLE_SIZE4    |                       |                         |    |                       |    |                       |    |
| R/W                     |                       |                         |    |                       |    |                       |    |
| 0h                      |                       |                         |    |                       |    |                       |    |

**Table 4-1009. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG4 Register Field Descriptions**

| Bit   | Field                       | Type  | Reset | Description |
|-------|-----------------------------|-------|-------|-------------|
| 31:24 | RESERVED                    | NONE  | 0h    | Reserved    |
| 23    | PRU0_FD_EN_4                | R/W   | 0h    |             |
| 22    | PRU0_FD_ONE_MAX_4           | R/W1C | 0h    |             |
| 21:17 | PRU0_FD_ONE_MAX_LI<br>MIT_4 | R/W   | 0h    |             |
| 16    | PRU0_FD_ONE_MIN_4           | R/W1C | 0h    |             |
| 15:11 | PRU0_FD_ONE_MIN_LIM<br>IT_4 | R/W   | 0h    |             |
| 10:8  | PRU0_FD_WINDOW_SIZ<br>E_4   | R/W   | 0h    |             |
| 7:0   | PRU0_SD_SAMPLE_SIZ<br>E4    | R/W   | 0h    |             |

#### 4.2.2.132 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG5 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG5 Register (Offset = 70h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1010. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6070h       |

**Figure 4-326. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG5 Name Register**

|                          |                    |                          |    |          |                  |                    |    |
|--------------------------|--------------------|--------------------------|----|----------|------------------|--------------------|----|
| 31                       | 30                 | 29                       | 28 | 27       | 26               | 25                 | 24 |
| RESERVED                 |                    |                          |    |          |                  |                    |    |
| NONE                     |                    |                          |    |          |                  |                    |    |
| 0h                       |                    |                          |    |          |                  |                    |    |
| 23                       | 22                 | 21                       | 20 | 19       | 18               | 17                 | 16 |
| RESERVED                 | PRU0_FD_ZERO_MAX_5 | PRU0_FD_ZERO_MAX_LIMIT_5 |    |          |                  | PRU0_FD_ZERO_MIN_5 |    |
| NONE                     | R/W1C              | R/W                      |    |          |                  | R/W1C              |    |
| 0h                       | 0h                 | 0h                       |    |          |                  | 0h                 |    |
| 15                       | 14                 | 13                       | 12 | 11       | 10               | 9                  | 8  |
| PRU0_FD_ZERO_MIN_LIMIT_5 |                    |                          |    |          | RESERVED         |                    |    |
| R/W                      |                    |                          |    |          | NONE             |                    |    |
| 0h                       |                    |                          |    |          | 0h               |                    |    |
| 7                        | 6                  | 5                        | 4  | 3        | 2                | 1                  | 0  |
| RESERVED                 |                    | PRU0_SD_ACC_SEL5         |    | RESERVED | PRU0_SD_CLK_INV5 | PRU0_SD_CLK_SEL5   |    |
| NONE                     |                    | R/W                      |    | NONE     | R/W              | R/W                |    |
| 0h                       |                    | 0h                       |    | 0h       | 0h               | 0h                 |    |

**Table 4-1012. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG5 Register Field Descriptions**

| Bit   | Field                    | Type  | Reset | Description |
|-------|--------------------------|-------|-------|-------------|
| 31:23 | RESERVED                 | NONE  | 0h    | Reserved    |
| 22    | PRU0_FD_ZERO_MAX_5       | R/W1C | 0h    |             |
| 21:17 | PRU0_FD_ZERO_MAX_LIMIT_5 | R/W   | 0h    |             |
| 16    | PRU0_FD_ZERO_MIN_5       | R/W1C | 0h    |             |
| 15:11 | PRU0_FD_ZERO_MIN_LIMIT_5 | R/W   | 0h    |             |
| 10:6  | RESERVED                 | NONE  | 0h    | Reserved    |
| 5:4   | PRU0_SD_ACC_SEL5         | R/W   | 0h    |             |
| 3     | RESERVED                 | NONE  | 0h    | Reserved    |
| 2     | PRU0_SD_CLK_INV5         | R/W   | 0h    |             |
| 1:0   | PRU0_SD_CLK_SEL5         | R/W   | 0h    |             |

#### 4.2.2.133 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG5 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG5 Register (Offset = 74h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1013. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6074h       |

**Figure 4-327. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG5 Name Register**

|                         |                    |                         |    |                       |    |                    |    |
|-------------------------|--------------------|-------------------------|----|-----------------------|----|--------------------|----|
| 31                      | 30                 | 29                      | 28 | 27                    | 26 | 25                 | 24 |
| RESERVED                |                    |                         |    |                       |    |                    |    |
| NONE                    |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |
| 23                      | 22                 | 21                      | 20 | 19                    | 18 | 17                 | 16 |
| PRU0_FD_EN_5            | PRU0_FD_ON_E_MAX_5 | PRU0_FD_ONE_MAX_LIMIT_5 |    |                       |    | PRU0_FD_ON_E_MIN_5 |    |
| R/W                     | R/W1C              | R/W                     |    |                       |    | R/W1C              |    |
| 0h                      | 0h                 | 0h                      |    |                       |    | 0h                 |    |
| 15                      | 14                 | 13                      | 12 | 11                    | 10 | 9                  | 8  |
| PRU0_FD_ONE_MIN_LIMIT_5 |                    |                         |    | PRU0_FD_WINDOW_SIZE_5 |    |                    |    |
| R/W                     |                    |                         |    | R/W                   |    |                    |    |
| 0h                      |                    |                         |    | 0h                    |    |                    |    |
| 7                       | 6                  | 5                       | 4  | 3                     | 2  | 1                  | 0  |
| PRU0_SD_SAMPLE_SIZE5    |                    |                         |    |                       |    |                    |    |
| R/W                     |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |

**Table 4-1015. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG5 Register Field Descriptions**

| Bit   | Field                   | Type  | Reset | Description |
|-------|-------------------------|-------|-------|-------------|
| 31:24 | RESERVED                | NONE  | 0h    | Reserved    |
| 23    | PRU0_FD_EN_5            | R/W   | 0h    |             |
| 22    | PRU0_FD_ONE_MAX_5       | R/W1C | 0h    |             |
| 21:17 | PRU0_FD_ONE_MAX_LIMIT_5 | R/W   | 0h    |             |
| 16    | PRU0_FD_ONE_MIN_5       | R/W1C | 0h    |             |
| 15:11 | PRU0_FD_ONE_MIN_LIMIT_5 | R/W   | 0h    |             |
| 10:8  | PRU0_FD_WINDOW_SIZE_5   | R/W   | 0h    |             |
| 7:0   | PRU0_SD_SAMPLE_SIZE5    | R/W   | 0h    |             |

#### 4.2.2.134 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG6 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG6 Register (Offset = 78h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1016. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6078h       |

**Figure 4-328. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG6 Name Register**

|                          |                    |                          |    |          |                  |                    |    |
|--------------------------|--------------------|--------------------------|----|----------|------------------|--------------------|----|
| 31                       | 30                 | 29                       | 28 | 27       | 26               | 25                 | 24 |
| RESERVED                 |                    |                          |    |          |                  |                    |    |
| NONE                     |                    |                          |    |          |                  |                    |    |
| 0h                       |                    |                          |    |          |                  |                    |    |
| 23                       | 22                 | 21                       | 20 | 19       | 18               | 17                 | 16 |
| RESERVED                 | PRU0_FD_ZERO_MAX_6 | PRU0_FD_ZERO_MAX_LIMIT_6 |    |          |                  | PRU0_FD_ZERO_MIN_6 |    |
| NONE                     | R/W1C              | R/W                      |    |          |                  | R/W1C              |    |
| 0h                       | 0h                 | 0h                       |    |          |                  | 0h                 |    |
| 15                       | 14                 | 13                       | 12 | 11       | 10               | 9                  | 8  |
| PRU0_FD_ZERO_MIN_LIMIT_6 |                    |                          |    |          | RESERVED         |                    |    |
| R/W                      |                    |                          |    |          | NONE             |                    |    |
| 0h                       |                    |                          |    |          | 0h               |                    |    |
| 7                        | 6                  | 5                        | 4  | 3        | 2                | 1                  | 0  |
| RESERVED                 |                    | PRU0_SD_ACC_SEL6         |    | RESERVED | PRU0_SD_CLK_INV6 | PRU0_SD_CLK_SEL6   |    |
| NONE                     |                    | R/W                      |    | NONE     | R/W              | R/W                |    |
| 0h                       |                    | 0h                       |    | 0h       | 0h               | 0h                 |    |

**Table 4-1018. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG6 Register Field Descriptions**

| Bit   | Field                    | Type  | Reset | Description |
|-------|--------------------------|-------|-------|-------------|
| 31:23 | RESERVED                 | NONE  | 0h    | Reserved    |
| 22    | PRU0_FD_ZERO_MAX_6       | R/W1C | 0h    |             |
| 21:17 | PRU0_FD_ZERO_MAX_LIMIT_6 | R/W   | 0h    |             |
| 16    | PRU0_FD_ZERO_MIN_6       | R/W1C | 0h    |             |
| 15:11 | PRU0_FD_ZERO_MIN_LIMIT_6 | R/W   | 0h    |             |
| 10:6  | RESERVED                 | NONE  | 0h    | Reserved    |
| 5:4   | PRU0_SD_ACC_SEL6         | R/W   | 0h    |             |
| 3     | RESERVED                 | NONE  | 0h    | Reserved    |
| 2     | PRU0_SD_CLK_INV6         | R/W   | 0h    |             |
| 1:0   | PRU0_SD_CLK_SEL6         | R/W   | 0h    |             |

#### 4.2.2.135 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG6 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG6 Register (Offset = 7Ch) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1019. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 607Ch       |

**Figure 4-329. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG6 Name Register**

|                         |                    |                         |    |                       |    |                    |    |
|-------------------------|--------------------|-------------------------|----|-----------------------|----|--------------------|----|
| 31                      | 30                 | 29                      | 28 | 27                    | 26 | 25                 | 24 |
| RESERVED                |                    |                         |    |                       |    |                    |    |
| NONE                    |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |
| 23                      | 22                 | 21                      | 20 | 19                    | 18 | 17                 | 16 |
| PRU0_FD_EN_6            | PRU0_FD_ON_E_MAX_6 | PRU0_FD_ONE_MAX_LIMIT_6 |    |                       |    | PRU0_FD_ON_E_MIN_6 |    |
| R/W                     | R/W1C              | R/W                     |    |                       |    | R/W1C              |    |
| 0h                      | 0h                 | 0h                      |    |                       |    | 0h                 |    |
| 15                      | 14                 | 13                      | 12 | 11                    | 10 | 9                  | 8  |
| PRU0_FD_ONE_MIN_LIMIT_6 |                    |                         |    | PRU0_FD_WINDOW_SIZE_6 |    |                    |    |
| R/W                     |                    |                         |    | R/W                   |    |                    |    |
| 0h                      |                    |                         |    | 0h                    |    |                    |    |
| 7                       | 6                  | 5                       | 4  | 3                     | 2  | 1                  | 0  |
| PRU0_SD_SAMPLE_SIZE6    |                    |                         |    |                       |    |                    |    |
| R/W                     |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |

**Table 4-1021. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG6 Register Field Descriptions**

| Bit   | Field                   | Type  | Reset | Description |
|-------|-------------------------|-------|-------|-------------|
| 31:24 | RESERVED                | NONE  | 0h    | Reserved    |
| 23    | PRU0_FD_EN_6            | R/W   | 0h    |             |
| 22    | PRU0_FD_ONE_MAX_6       | R/W1C | 0h    |             |
| 21:17 | PRU0_FD_ONE_MAX_LIMIT_6 | R/W   | 0h    |             |
| 16    | PRU0_FD_ONE_MIN_6       | R/W1C | 0h    |             |
| 15:11 | PRU0_FD_ONE_MIN_LIMIT_6 | R/W   | 0h    |             |
| 10:8  | PRU0_FD_WINDOW_SIZE_6   | R/W   | 0h    |             |
| 7:0   | PRU0_SD_SAMPLE_SIZE6    | R/W   | 0h    |             |

#### 4.2.2.136 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG7 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG7 Register (Offset = 80h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1022. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6080h       |

**Figure 4-330. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG7 Name Register**

|                          |                    |                          |    |          |                  |                    |    |
|--------------------------|--------------------|--------------------------|----|----------|------------------|--------------------|----|
| 31                       | 30                 | 29                       | 28 | 27       | 26               | 25                 | 24 |
| RESERVED                 |                    |                          |    |          |                  |                    |    |
| NONE                     |                    |                          |    |          |                  |                    |    |
| 0h                       |                    |                          |    |          |                  |                    |    |
| 23                       | 22                 | 21                       | 20 | 19       | 18               | 17                 | 16 |
| RESERVED                 | PRU0_FD_ZERO_MAX_7 | PRU0_FD_ZERO_MAX_LIMIT_7 |    |          |                  | PRU0_FD_ZERO_MIN_7 |    |
| NONE                     | R/W1C              | R/W                      |    |          |                  | R/W1C              |    |
| 0h                       | 0h                 | 0h                       |    |          |                  | 0h                 |    |
| 15                       | 14                 | 13                       | 12 | 11       | 10               | 9                  | 8  |
| PRU0_FD_ZERO_MIN_LIMIT_7 |                    |                          |    |          | RESERVED         |                    |    |
| R/W                      |                    |                          |    |          | NONE             |                    |    |
| 0h                       |                    |                          |    |          | 0h               |                    |    |
| 7                        | 6                  | 5                        | 4  | 3        | 2                | 1                  | 0  |
| RESERVED                 |                    | PRU0_SD_ACC_SEL7         |    | RESERVED | PRU0_SD_CLK_INV7 | PRU0_SD_CLK_SEL7   |    |
| NONE                     |                    | R/W                      |    | NONE     | R/W              | R/W                |    |
| 0h                       |                    | 0h                       |    | 0h       | 0h               | 0h                 |    |

**Table 4-1024. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG7 Register Field Descriptions**

| Bit   | Field                    | Type  | Reset | Description |
|-------|--------------------------|-------|-------|-------------|
| 31:23 | RESERVED                 | NONE  | 0h    | Reserved    |
| 22    | PRU0_FD_ZERO_MAX_7       | R/W1C | 0h    |             |
| 21:17 | PRU0_FD_ZERO_MAX_LIMIT_7 | R/W   | 0h    |             |
| 16    | PRU0_FD_ZERO_MIN_7       | R/W1C | 0h    |             |
| 15:11 | PRU0_FD_ZERO_MIN_LIMIT_7 | R/W   | 0h    |             |
| 10:6  | RESERVED                 | NONE  | 0h    | Reserved    |
| 5:4   | PRU0_SD_ACC_SEL7         | R/W   | 0h    |             |
| 3     | RESERVED                 | NONE  | 0h    | Reserved    |
| 2     | PRU0_SD_CLK_INV7         | R/W   | 0h    |             |
| 1:0   | PRU0_SD_CLK_SEL7         | R/W   | 0h    |             |

#### 4.2.2.137 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG7 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG7 Register (Offset = 84h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1025. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6084h       |

**Figure 4-331. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG7 Name Register**

|                         |                       |                         |    |    |                       |    |                       |
|-------------------------|-----------------------|-------------------------|----|----|-----------------------|----|-----------------------|
| 31                      | 30                    | 29                      | 28 | 27 | 26                    | 25 | 24                    |
| RESERVED                |                       |                         |    |    |                       |    |                       |
| NONE                    |                       |                         |    |    |                       |    |                       |
| 0h                      |                       |                         |    |    |                       |    |                       |
| 23                      | 22                    | 21                      | 20 | 19 | 18                    | 17 | 16                    |
| PRU0_FD_EN_7            | PRU0_FD_ON<br>E_MAX_7 | PRU0_FD_ONE_MAX_LIMIT_7 |    |    |                       |    | PRU0_FD_ON<br>E_MIN_7 |
| R/W                     | R/W1C                 | R/W                     |    |    |                       |    | R/W1C                 |
| 0h                      | 0h                    | 0h                      |    |    |                       |    | 0h                    |
| 15                      | 14                    | 13                      | 12 | 11 | 10                    | 9  | 8                     |
| PRU0_FD_ONE_MIN_LIMIT_7 |                       |                         |    |    | PRU0_FD_WINDOW_SIZE_7 |    |                       |
| R/W                     |                       |                         |    |    | R/W                   |    |                       |
| 0h                      |                       |                         |    |    | 0h                    |    |                       |
| 7                       | 6                     | 5                       | 4  | 3  | 2                     | 1  | 0                     |
| PRU0_SD_SAMPLE_SIZE7    |                       |                         |    |    |                       |    |                       |
| R/W                     |                       |                         |    |    |                       |    |                       |
| 0h                      |                       |                         |    |    |                       |    |                       |

**Table 4-1027. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG7 Register Field Descriptions**

| Bit   | Field                       | Type  | Reset | Description |
|-------|-----------------------------|-------|-------|-------------|
| 31:24 | RESERVED                    | NONE  | 0h    | Reserved    |
| 23    | PRU0_FD_EN_7                | R/W   | 0h    |             |
| 22    | PRU0_FD_ONE_MAX_7           | R/W1C | 0h    |             |
| 21:17 | PRU0_FD_ONE_MAX_LI<br>MIT_7 | R/W   | 0h    |             |
| 16    | PRU0_FD_ONE_MIN_7           | R/W1C | 0h    |             |
| 15:11 | PRU0_FD_ONE_MIN_LIM<br>IT_7 | R/W   | 0h    |             |
| 10:8  | PRU0_FD_WINDOW_SIZ<br>E_7   | R/W   | 0h    |             |
| 7:0   | PRU0_SD_SAMPLE_SIZ<br>E7    | R/W   | 0h    |             |

#### 4.2.2.138 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG8 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG8 Register (Offset = 88h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1028. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6088h       |

**Figure 4-332. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG8 Name Register**

|                          |                    |                          |    |          |                  |                    |    |
|--------------------------|--------------------|--------------------------|----|----------|------------------|--------------------|----|
| 31                       | 30                 | 29                       | 28 | 27       | 26               | 25                 | 24 |
| RESERVED                 |                    |                          |    |          |                  |                    |    |
| NONE                     |                    |                          |    |          |                  |                    |    |
| 0h                       |                    |                          |    |          |                  |                    |    |
| 23                       | 22                 | 21                       | 20 | 19       | 18               | 17                 | 16 |
| RESERVED                 | PRU0_FD_ZERO_MAX_8 | PRU0_FD_ZERO_MAX_LIMIT_8 |    |          |                  | PRU0_FD_ZERO_MIN_8 |    |
| NONE                     | R/W1C              | R/W                      |    |          |                  | R/W1C              |    |
| 0h                       | 0h                 | 0h                       |    |          |                  | 0h                 |    |
| 15                       | 14                 | 13                       | 12 | 11       | 10               | 9                  | 8  |
| PRU0_FD_ZERO_MIN_LIMIT_8 |                    |                          |    |          | RESERVED         |                    |    |
| R/W                      |                    |                          |    |          | NONE             |                    |    |
| 0h                       |                    |                          |    |          | 0h               |                    |    |
| 7                        | 6                  | 5                        | 4  | 3        | 2                | 1                  | 0  |
| RESERVED                 |                    | PRU0_SD_ACC_SEL8         |    | RESERVED | PRU0_SD_CLK_INV8 | PRU0_SD_CLK_SEL8   |    |
| NONE                     |                    | R/W                      |    | NONE     | R/W              | R/W                |    |
| 0h                       |                    | 0h                       |    | 0h       | 0h               | 0h                 |    |

**Table 4-1030. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_CLK\_SEL\_REG8 Register Field Descriptions**

| Bit   | Field                    | Type  | Reset | Description |
|-------|--------------------------|-------|-------|-------------|
| 31:23 | RESERVED                 | NONE  | 0h    | Reserved    |
| 22    | PRU0_FD_ZERO_MAX_8       | R/W1C | 0h    |             |
| 21:17 | PRU0_FD_ZERO_MAX_LIMIT_8 | R/W   | 0h    |             |
| 16    | PRU0_FD_ZERO_MIN_8       | R/W1C | 0h    |             |
| 15:11 | PRU0_FD_ZERO_MIN_LIMIT_8 | R/W   | 0h    |             |
| 10:6  | RESERVED                 | NONE  | 0h    | Reserved    |
| 5:4   | PRU0_SD_ACC_SEL8         | R/W   | 0h    |             |
| 3     | RESERVED                 | NONE  | 0h    | Reserved    |
| 2     | PRU0_SD_CLK_INV8         | R/W   | 0h    |             |
| 1:0   | PRU0_SD_CLK_SEL8         | R/W   | 0h    |             |



#### 4.2.2.139 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG8 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG8 Register (Offset = 8Ch) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1031. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 608Ch       |

**Figure 4-333. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG8 Name Register**

|                         |                    |                         |    |                       |    |                    |    |
|-------------------------|--------------------|-------------------------|----|-----------------------|----|--------------------|----|
| 31                      | 30                 | 29                      | 28 | 27                    | 26 | 25                 | 24 |
| RESERVED                |                    |                         |    |                       |    |                    |    |
| NONE                    |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |
| 23                      | 22                 | 21                      | 20 | 19                    | 18 | 17                 | 16 |
| PRU0_FD_EN_8            | PRU0_FD_ON_E_MAX_8 | PRU0_FD_ONE_MAX_LIMIT_8 |    |                       |    | PRU0_FD_ON_E_MIN_8 |    |
| R/W                     | R/W1C              | R/W                     |    |                       |    | R/W1C              |    |
| 0h                      | 0h                 | 0h                      |    |                       |    | 0h                 |    |
| 15                      | 14                 | 13                      | 12 | 11                    | 10 | 9                  | 8  |
| PRU0_FD_ONE_MIN_LIMIT_8 |                    |                         |    | PRU0_FD_WINDOW_SIZE_8 |    |                    |    |
| R/W                     |                    |                         |    | R/W                   |    |                    |    |
| 0h                      |                    |                         |    | 0h                    |    |                    |    |
| 7                       | 6                  | 5                       | 4  | 3                     | 2  | 1                  | 0  |
| PRU0_SD_SAMPLE_SIZE8    |                    |                         |    |                       |    |                    |    |
| R/W                     |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |

**Table 4-1033. ICSSM\_PR1\_CFG\_SLV\_PRU0\_SD\_SAMPLE\_SIZE\_REG8 Register Field Descriptions**

| Bit   | Field                   | Type  | Reset | Description |
|-------|-------------------------|-------|-------|-------------|
| 31:24 | RESERVED                | NONE  | 0h    | Reserved    |
| 23    | PRU0_FD_EN_8            | R/W   | 0h    |             |
| 22    | PRU0_FD_ONE_MAX_8       | R/W1C | 0h    |             |
| 21:17 | PRU0_FD_ONE_MAX_LIMIT_8 | R/W   | 0h    |             |
| 16    | PRU0_FD_ONE_MIN_8       | R/W1C | 0h    |             |
| 15:11 | PRU0_FD_ONE_MIN_LIMIT_8 | R/W   | 0h    |             |
| 10:8  | PRU0_FD_WINDOW_SIZE_8   | R/W   | 0h    |             |
| 7:0   | PRU0_SD_SAMPLE_SIZE8    | R/W   | 0h    |             |

#### 4.2.2.140 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_DIV\_REG Register

#### 1 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_DIV\_REG Register (Offset = 90h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1034. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6090h       |

**Figure 4-334. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_DIV\_REG Name Register**

|                            |                |    |    |    |                                |                    |                                  |
|----------------------------|----------------|----|----|----|--------------------------------|--------------------|----------------------------------|
| 31                         | 30             | 29 | 28 | 27 | 26                             | 25                 | 24                               |
| PRU1_SD_MAN_REC_CLK_PERIOD |                |    |    |    |                                |                    |                                  |
| R                          |                |    |    |    |                                |                    |                                  |
| 0h                         |                |    |    |    |                                |                    |                                  |
| 23                         | 22             | 21 | 20 | 19 | 18                             | 17                 | 16                               |
| RESERVED                   |                |    |    |    |                                |                    | PRU1_SD_MA<br>N_CLK_CAL_D<br>ONE |
| NONE                       |                |    |    |    |                                |                    | R                                |
| 0h                         |                |    |    |    |                                |                    | 0h                               |
| 15                         | 14             | 13 | 12 | 11 | 10                             | 9                  | 8                                |
| PRU1_SD_MA<br>N_STATUS     | PRU1_SD_CH_SEL |    |    |    | PRU1_SD_MA<br>N_NV_DATA_E<br>N | PRU1_SD_MA<br>N_EN | PRU1_SD_SHA<br>RE_EN             |
| R                          | R/W            |    |    |    | R/W                            | R/W                | R/W                              |
| 0h                         | 0h             |    |    |    | 0h                             | 0h                 | 0h                               |
| 7                          | 6              | 5  | 4  | 3  | 2                              | 1                  | 0                                |
| RESERVED                   |                |    |    |    |                                |                    |                                  |
| NONE                       |                |    |    |    |                                |                    |                                  |
| 0h                         |                |    |    |    |                                |                    |                                  |

**Table 4-1036. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_DIV\_REG Register Field Descriptions**

| Bit   | Field                      | Type | Reset | Description |
|-------|----------------------------|------|-------|-------------|
| 31:24 | PRU1_SD_MAN_REC_CLK_PERIOD | R    | 0h    |             |
| 23:17 | RESERVED                   | NONE | 0h    | Reserved    |
| 16    | PRU1_SD_MAN_CLK_CAL_DONE   | R    | 0h    |             |
| 15    | PRU1_SD_MAN_STATUS         | R    | 0h    |             |
| 14:11 | PRU1_SD_CH_SEL             | R/W  | 0h    |             |
| 10    | PRU1_SD_MAN_NV_DATA_EN     | R/W  | 0h    |             |
| 9     | PRU1_SD_MAN_EN             | R/W  | 0h    |             |
| 8     | PRU1_SD_SHARE_EN           | R/W  | 0h    |             |
| 7:0   | RESERVED                   | NONE | 0h    | Reserved    |

#### 4.2.2.141 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG0 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG0 Register (Offset = 94h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1037. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6094h       |

**Figure 4-335. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG0 Name Register**

|                          |                        |                          |    |          |                      |                        |    |
|--------------------------|------------------------|--------------------------|----|----------|----------------------|------------------------|----|
| 31                       | 30                     | 29                       | 28 | 27       | 26                   | 25                     | 24 |
| RESERVED                 |                        |                          |    |          |                      |                        |    |
| NONE                     |                        |                          |    |          |                      |                        |    |
| 0h                       |                        |                          |    |          |                      |                        |    |
| 23                       | 22                     | 21                       | 20 | 19       | 18                   | 17                     | 16 |
| RESERVED                 | PRU1_FD_ZER<br>O_MAX_0 | PRU1_FD_ZERO_MAX_LIMIT_0 |    |          |                      | PRU1_FD_ZER<br>O_MIN_0 |    |
| NONE                     | R/W1C                  | R/W                      |    |          |                      | R/W1C                  |    |
| 0h                       | 0h                     | 0h                       |    |          |                      | 0h                     |    |
| 15                       | 14                     | 13                       | 12 | 11       | 10                   | 9                      | 8  |
| PRU1_FD_ZERO_MIN_LIMIT_0 |                        |                          |    |          | RESERVED             |                        |    |
| R/W                      |                        |                          |    |          | NONE                 |                        |    |
| 0h                       |                        |                          |    |          | 0h                   |                        |    |
| 7                        | 6                      | 5                        | 4  | 3        | 2                    | 1                      | 0  |
| RESERVED                 |                        | PRU1_SD_ACC_SEL0         |    | RESERVED | PRU1_SD_CLK<br>_INV0 | PRU1_SD_CLK_SEL0       |    |
| NONE                     |                        | R/W                      |    | NONE     | R/W                  | R/W                    |    |
| 0h                       |                        | 0h                       |    | 0h       | 0h                   | 0h                     |    |

**Table 4-1039. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG0 Register Field Descriptions**

| Bit   | Field                        | Type  | Reset | Description |
|-------|------------------------------|-------|-------|-------------|
| 31:23 | RESERVED                     | NONE  | 0h    | Reserved    |
| 22    | PRU1_FD_ZERO_MAX_0           | R/W1C | 0h    |             |
| 21:17 | PRU1_FD_ZERO_MAX_L<br>IMIT_0 | R/W   | 0h    |             |
| 16    | PRU1_FD_ZERO_MIN_0           | R/W1C | 0h    |             |
| 15:11 | PRU1_FD_ZERO_MIN_LI<br>MIT_0 | R/W   | 0h    |             |
| 10:6  | RESERVED                     | NONE  | 0h    | Reserved    |
| 5:4   | PRU1_SD_ACC_SEL0             | R/W   | 0h    |             |
| 3     | RESERVED                     | NONE  | 0h    | Reserved    |
| 2     | PRU1_SD_CLK_INV0             | R/W   | 0h    |             |
| 1:0   | PRU1_SD_CLK_SEL0             | R/W   | 0h    |             |

#### 4.2.2.142 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG0 Register

#### 1 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG0 Register (Offset = 98h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1040. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6098h       |

**Figure 4-336. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG0 Name Register**

|                         |                    |                         |    |                       |    |                    |    |
|-------------------------|--------------------|-------------------------|----|-----------------------|----|--------------------|----|
| 31                      | 30                 | 29                      | 28 | 27                    | 26 | 25                 | 24 |
| RESERVED                |                    |                         |    |                       |    |                    |    |
| NONE                    |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |
| 23                      | 22                 | 21                      | 20 | 19                    | 18 | 17                 | 16 |
| PRU1_FD_EN_0            | PRU1_FD_ON_E_MAX_0 | PRU1_FD_ONE_MAX_LIMIT_0 |    |                       |    | PRU1_FD_ON_E_MIN_0 |    |
| R/W                     | R/W1C              | R/W                     |    |                       |    | R/W1C              |    |
| 0h                      | 0h                 | 0h                      |    |                       |    | 0h                 |    |
| 15                      | 14                 | 13                      | 12 | 11                    | 10 | 9                  | 8  |
| PRU1_FD_ONE_MIN_LIMIT_0 |                    |                         |    | PRU1_FD_WINDOW_SIZE_0 |    |                    |    |
| R/W                     |                    |                         |    | R/W                   |    |                    |    |
| 0h                      |                    |                         |    | 0h                    |    |                    |    |
| 7                       | 6                  | 5                       | 4  | 3                     | 2  | 1                  | 0  |
| PRU1_SD_SAMPLE_SIZE0    |                    |                         |    |                       |    |                    |    |
| R/W                     |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |

**Table 4-1042. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG0 Register Field Descriptions**

| Bit   | Field                   | Type  | Reset | Description |
|-------|-------------------------|-------|-------|-------------|
| 31:24 | RESERVED                | NONE  | 0h    | Reserved    |
| 23    | PRU1_FD_EN_0            | R/W   | 0h    |             |
| 22    | PRU1_FD_ONE_MAX_0       | R/W1C | 0h    |             |
| 21:17 | PRU1_FD_ONE_MAX_LIMIT_0 | R/W   | 0h    |             |
| 16    | PRU1_FD_ONE_MIN_0       | R/W1C | 0h    |             |
| 15:11 | PRU1_FD_ONE_MIN_LIMIT_0 | R/W   | 0h    |             |
| 10:8  | PRU1_FD_WINDOW_SIZE_0   | R/W   | 0h    |             |
| 7:0   | PRU1_SD_SAMPLE_SIZE0    | R/W   | 0h    |             |

#### 4.2.2.143 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG1 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG1 Register (Offset = 9Ch) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1043. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 609Ch       |

**Figure 4-337. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG1 Name Register**

|                          |                    |                          |    |          |                  |                    |    |
|--------------------------|--------------------|--------------------------|----|----------|------------------|--------------------|----|
| 31                       | 30                 | 29                       | 28 | 27       | 26               | 25                 | 24 |
| RESERVED                 |                    |                          |    |          |                  |                    |    |
| NONE                     |                    |                          |    |          |                  |                    |    |
| 0h                       |                    |                          |    |          |                  |                    |    |
| 23                       | 22                 | 21                       | 20 | 19       | 18               | 17                 | 16 |
| RESERVED                 | PRU1_FD_ZERO_MAX_1 | PRU1_FD_ZERO_MAX_LIMIT_1 |    |          |                  | PRU1_FD_ZERO_MIN_1 |    |
| NONE                     | R/W1C              | R/W                      |    |          |                  | R/W1C              |    |
| 0h                       | 0h                 | 0h                       |    |          |                  | 0h                 |    |
| 15                       | 14                 | 13                       | 12 | 11       | 10               | 9                  | 8  |
| PRU1_FD_ZERO_MIN_LIMIT_1 |                    |                          |    |          | RESERVED         |                    |    |
| R/W                      |                    |                          |    |          | NONE             |                    |    |
| 0h                       |                    |                          |    |          | 0h               |                    |    |
| 7                        | 6                  | 5                        | 4  | 3        | 2                | 1                  | 0  |
| RESERVED                 |                    | PRU1_SD_ACC_SEL1         |    | RESERVED | PRU1_SD_CLK_INV1 | PRU1_SD_CLK_SEL1   |    |
| NONE                     |                    | R/W                      |    | NONE     | R/W              | R/W                |    |
| 0h                       |                    | 0h                       |    | 0h       | 0h               | 0h                 |    |

**Table 4-1045. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG1 Register Field Descriptions**

| Bit   | Field                    | Type  | Reset | Description |
|-------|--------------------------|-------|-------|-------------|
| 31:23 | RESERVED                 | NONE  | 0h    | Reserved    |
| 22    | PRU1_FD_ZERO_MAX_1       | R/W1C | 0h    |             |
| 21:17 | PRU1_FD_ZERO_MAX_LIMIT_1 | R/W   | 0h    |             |
| 16    | PRU1_FD_ZERO_MIN_1       | R/W1C | 0h    |             |
| 15:11 | PRU1_FD_ZERO_MIN_LIMIT_1 | R/W   | 0h    |             |
| 10:6  | RESERVED                 | NONE  | 0h    | Reserved    |
| 5:4   | PRU1_SD_ACC_SEL1         | R/W   | 0h    |             |
| 3     | RESERVED                 | NONE  | 0h    | Reserved    |
| 2     | PRU1_SD_CLK_INV1         | R/W   | 0h    |             |
| 1:0   | PRU1_SD_CLK_SEL1         | R/W   | 0h    |             |

#### 4.2.2.144 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG1 Register

#### 1 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG1 Register (Offset = A0h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1046. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 60A0h       |

**Figure 4-338. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG1 Name Register**

|                         |                    |                         |    |                       |    |                    |    |
|-------------------------|--------------------|-------------------------|----|-----------------------|----|--------------------|----|
| 31                      | 30                 | 29                      | 28 | 27                    | 26 | 25                 | 24 |
| RESERVED                |                    |                         |    |                       |    |                    |    |
| NONE                    |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |
| 23                      | 22                 | 21                      | 20 | 19                    | 18 | 17                 | 16 |
| PRU1_FD_EN_1            | PRU1_FD_ON_E_MAX_1 | PRU1_FD_ONE_MAX_LIMIT_1 |    |                       |    | PRU1_FD_ON_E_MIN_1 |    |
| R/W                     | R/W1C              | R/W                     |    |                       |    | R/W1C              |    |
| 0h                      | 0h                 | 0h                      |    |                       |    | 0h                 |    |
| 15                      | 14                 | 13                      | 12 | 11                    | 10 | 9                  | 8  |
| PRU1_FD_ONE_MIN_LIMIT_1 |                    |                         |    | PRU1_FD_WINDOW_SIZE_1 |    |                    |    |
| R/W                     |                    |                         |    | R/W                   |    |                    |    |
| 0h                      |                    |                         |    | 0h                    |    |                    |    |
| 7                       | 6                  | 5                       | 4  | 3                     | 2  | 1                  | 0  |
| PRU1_SD_SAMPLE_SIZE1    |                    |                         |    |                       |    |                    |    |
| R/W                     |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |

**Table 4-1048. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG1 Register Field Descriptions**

| Bit   | Field                   | Type  | Reset | Description |
|-------|-------------------------|-------|-------|-------------|
| 31:24 | RESERVED                | NONE  | 0h    | Reserved    |
| 23    | PRU1_FD_EN_1            | R/W   | 0h    |             |
| 22    | PRU1_FD_ON_E_MAX_1      | R/W1C | 0h    |             |
| 21:17 | PRU1_FD_ONE_MAX_LIMIT_1 | R/W   | 0h    |             |
| 16    | PRU1_FD_ON_E_MIN_1      | R/W1C | 0h    |             |
| 15:11 | PRU1_FD_ONE_MIN_LIMIT_1 | R/W   | 0h    |             |
| 10:8  | PRU1_FD_WINDOW_SIZE_1   | R/W   | 0h    |             |
| 7:0   | PRU1_SD_SAMPLE_SIZE1    | R/W   | 0h    |             |

#### 4.2.2.145 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG2 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG2 Register (Offset = A4h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1049. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 60A4h       |

**Figure 4-339. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG2 Name Register**

|                          |                    |                          |    |          |                  |                    |    |
|--------------------------|--------------------|--------------------------|----|----------|------------------|--------------------|----|
| 31                       | 30                 | 29                       | 28 | 27       | 26               | 25                 | 24 |
| RESERVED                 |                    |                          |    |          |                  |                    |    |
| NONE                     |                    |                          |    |          |                  |                    |    |
| 0h                       |                    |                          |    |          |                  |                    |    |
| 23                       | 22                 | 21                       | 20 | 19       | 18               | 17                 | 16 |
| RESERVED                 | PRU1_FD_ZERO_MAX_2 | PRU1_FD_ZERO_MAX_LIMIT_2 |    |          |                  | PRU1_FD_ZERO_MIN_2 |    |
| NONE                     | R/W1C              | R/W                      |    |          |                  | R/W1C              |    |
| 0h                       | 0h                 | 0h                       |    |          |                  | 0h                 |    |
| 15                       | 14                 | 13                       | 12 | 11       | 10               | 9                  | 8  |
| PRU1_FD_ZERO_MIN_LIMIT_2 |                    |                          |    |          | RESERVED         |                    |    |
| R/W                      |                    |                          |    |          | NONE             |                    |    |
| 0h                       |                    |                          |    |          | 0h               |                    |    |
| 7                        | 6                  | 5                        | 4  | 3        | 2                | 1                  | 0  |
| RESERVED                 |                    | PRU1_SD_ACC_SEL2         |    | RESERVED | PRU1_SD_CLK_INV2 | PRU1_SD_CLK_SEL2   |    |
| NONE                     |                    | R/W                      |    | NONE     | R/W              | R/W                |    |
| 0h                       |                    | 0h                       |    | 0h       | 0h               | 0h                 |    |

**Table 4-1051. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG2 Register Field Descriptions**

| Bit   | Field                    | Type  | Reset | Description |
|-------|--------------------------|-------|-------|-------------|
| 31:23 | RESERVED                 | NONE  | 0h    | Reserved    |
| 22    | PRU1_FD_ZERO_MAX_2       | R/W1C | 0h    |             |
| 21:17 | PRU1_FD_ZERO_MAX_LIMIT_2 | R/W   | 0h    |             |
| 16    | PRU1_FD_ZERO_MIN_2       | R/W1C | 0h    |             |
| 15:11 | PRU1_FD_ZERO_MIN_LIMIT_2 | R/W   | 0h    |             |
| 10:6  | RESERVED                 | NONE  | 0h    | Reserved    |
| 5:4   | PRU1_SD_ACC_SEL2         | R/W   | 0h    |             |
| 3     | RESERVED                 | NONE  | 0h    | Reserved    |
| 2     | PRU1_SD_CLK_INV2         | R/W   | 0h    |             |
| 1:0   | PRU1_SD_CLK_SEL2         | R/W   | 0h    |             |

#### 4.2.2.146 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG2 Register

#### 1 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG2 Register (Offset = A8h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1052. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 60A8h       |

**Figure 4-340. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG2 Name Register**

|                         |                    |                         |    |                       |    |                    |    |
|-------------------------|--------------------|-------------------------|----|-----------------------|----|--------------------|----|
| 31                      | 30                 | 29                      | 28 | 27                    | 26 | 25                 | 24 |
| RESERVED                |                    |                         |    |                       |    |                    |    |
| NONE                    |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |
| 23                      | 22                 | 21                      | 20 | 19                    | 18 | 17                 | 16 |
| PRU1_FD_EN_2            | PRU1_FD_ON_E_MAX_2 | PRU1_FD_ONE_MAX_LIMIT_2 |    |                       |    | PRU1_FD_ON_E_MIN_2 |    |
| R/W                     | R/W1C              | R/W                     |    |                       |    | R/W1C              |    |
| 0h                      | 0h                 | 0h                      |    |                       |    | 0h                 |    |
| 15                      | 14                 | 13                      | 12 | 11                    | 10 | 9                  | 8  |
| PRU1_FD_ONE_MIN_LIMIT_2 |                    |                         |    | PRU1_FD_WINDOW_SIZE_2 |    |                    |    |
| R/W                     |                    |                         |    | R/W                   |    |                    |    |
| 0h                      |                    |                         |    | 0h                    |    |                    |    |
| 7                       | 6                  | 5                       | 4  | 3                     | 2  | 1                  | 0  |
| PRU1_SD_SAMPLE_SIZE2    |                    |                         |    |                       |    |                    |    |
| R/W                     |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |

**Table 4-1054. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG2 Register Field Descriptions**

| Bit   | Field                   | Type  | Reset | Description |
|-------|-------------------------|-------|-------|-------------|
| 31:24 | RESERVED                | NONE  | 0h    | Reserved    |
| 23    | PRU1_FD_EN_2            | R/W   | 0h    |             |
| 22    | PRU1_FD_ONE_MAX_2       | R/W1C | 0h    |             |
| 21:17 | PRU1_FD_ONE_MAX_LIMIT_2 | R/W   | 0h    |             |
| 16    | PRU1_FD_ONE_MIN_2       | R/W1C | 0h    |             |
| 15:11 | PRU1_FD_ONE_MIN_LIMIT_2 | R/W   | 0h    |             |
| 10:8  | PRU1_FD_WINDOW_SIZE_2   | R/W   | 0h    |             |
| 7:0   | PRU1_SD_SAMPLE_SIZE2    | R/W   | 0h    |             |



#### 4.2.2.147 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG3 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG3 Register (Offset = ACh) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1055. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 60ACh       |

**Figure 4-341. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG3 Name Register**

|                          |                    |                          |    |          |                  |                    |    |
|--------------------------|--------------------|--------------------------|----|----------|------------------|--------------------|----|
| 31                       | 30                 | 29                       | 28 | 27       | 26               | 25                 | 24 |
| RESERVED                 |                    |                          |    |          |                  |                    |    |
| NONE                     |                    |                          |    |          |                  |                    |    |
| 0h                       |                    |                          |    |          |                  |                    |    |
| 23                       | 22                 | 21                       | 20 | 19       | 18               | 17                 | 16 |
| RESERVED                 | PRU1_FD_ZERO_MAX_3 | PRU1_FD_ZERO_MAX_LIMIT_3 |    |          |                  | PRU1_FD_ZERO_MIN_3 |    |
| NONE                     | R/W1C              | R/W                      |    |          |                  | R/W1C              |    |
| 0h                       | 0h                 | 0h                       |    |          |                  | 0h                 |    |
| 15                       | 14                 | 13                       | 12 | 11       | 10               | 9                  | 8  |
| PRU1_FD_ZERO_MIN_LIMIT_3 |                    |                          |    |          | RESERVED         |                    |    |
| R/W                      |                    |                          |    |          | NONE             |                    |    |
| 0h                       |                    |                          |    |          | 0h               |                    |    |
| 7                        | 6                  | 5                        | 4  | 3        | 2                | 1                  | 0  |
| RESERVED                 |                    | PRU1_SD_ACC_SEL3         |    | RESERVED | PRU1_SD_CLK_INV3 | PRU1_SD_CLK_SEL3   |    |
| NONE                     |                    | R/W                      |    | NONE     | R/W              | R/W                |    |
| 0h                       |                    | 0h                       |    | 0h       | 0h               | 0h                 |    |

**Table 4-1057. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG3 Register Field Descriptions**

| Bit   | Field                    | Type  | Reset | Description |
|-------|--------------------------|-------|-------|-------------|
| 31:23 | RESERVED                 | NONE  | 0h    | Reserved    |
| 22    | PRU1_FD_ZERO_MAX_3       | R/W1C | 0h    |             |
| 21:17 | PRU1_FD_ZERO_MAX_LIMIT_3 | R/W   | 0h    |             |
| 16    | PRU1_FD_ZERO_MIN_3       | R/W1C | 0h    |             |
| 15:11 | PRU1_FD_ZERO_MIN_LIMIT_3 | R/W   | 0h    |             |
| 10:6  | RESERVED                 | NONE  | 0h    | Reserved    |
| 5:4   | PRU1_SD_ACC_SEL3         | R/W   | 0h    |             |
| 3     | RESERVED                 | NONE  | 0h    | Reserved    |
| 2     | PRU1_SD_CLK_INV3         | R/W   | 0h    |             |
| 1:0   | PRU1_SD_CLK_SEL3         | R/W   | 0h    |             |

#### 4.2.2.148 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG3 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG3 Register (Offset = B0h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1058. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 60B0h       |

**Figure 4-342. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG3 Name Register**

|                         |                    |                         |    |                       |    |                    |    |
|-------------------------|--------------------|-------------------------|----|-----------------------|----|--------------------|----|
| 31                      | 30                 | 29                      | 28 | 27                    | 26 | 25                 | 24 |
| RESERVED                |                    |                         |    |                       |    |                    |    |
| NONE                    |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |
| 23                      | 22                 | 21                      | 20 | 19                    | 18 | 17                 | 16 |
| PRU1_FD_EN_3            | PRU1_FD_ON_E_MAX_3 | PRU1_FD_ONE_MAX_LIMIT_3 |    |                       |    | PRU1_FD_ON_E_MIN_3 |    |
| R/W                     | R/W1C              | R/W                     |    |                       |    | R/W1C              |    |
| 0h                      | 0h                 | 0h                      |    |                       |    | 0h                 |    |
| 15                      | 14                 | 13                      | 12 | 11                    | 10 | 9                  | 8  |
| PRU1_FD_ONE_MIN_LIMIT_3 |                    |                         |    | PRU1_FD_WINDOW_SIZE_3 |    |                    |    |
| R/W                     |                    |                         |    | R/W                   |    |                    |    |
| 0h                      |                    |                         |    | 0h                    |    |                    |    |
| 7                       | 6                  | 5                       | 4  | 3                     | 2  | 1                  | 0  |
| PRU1_SD_SAMPLE_SIZE3    |                    |                         |    |                       |    |                    |    |
| R/W                     |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |

**Table 4-1060. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG3 Register Field Descriptions**

| Bit   | Field                   | Type  | Reset | Description |
|-------|-------------------------|-------|-------|-------------|
| 31:24 | RESERVED                | NONE  | 0h    | Reserved    |
| 23    | PRU1_FD_EN_3            | R/W   | 0h    |             |
| 22    | PRU1_FD_ONE_MAX_3       | R/W1C | 0h    |             |
| 21:17 | PRU1_FD_ONE_MAX_LIMIT_3 | R/W   | 0h    |             |
| 16    | PRU1_FD_ONE_MIN_3       | R/W1C | 0h    |             |
| 15:11 | PRU1_FD_ONE_MIN_LIMIT_3 | R/W   | 0h    |             |
| 10:8  | PRU1_FD_WINDOW_SIZE_3   | R/W   | 0h    |             |
| 7:0   | PRU1_SD_SAMPLE_SIZE3    | R/W   | 0h    |             |

#### 4.2.2.149 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG4 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG4 Register (Offset = B4h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1061. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 60B4h       |

**Figure 4-343. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG4 Name Register**

|                          |                    |                          |    |          |                  |                    |    |
|--------------------------|--------------------|--------------------------|----|----------|------------------|--------------------|----|
| 31                       | 30                 | 29                       | 28 | 27       | 26               | 25                 | 24 |
| RESERVED                 |                    |                          |    |          |                  |                    |    |
| NONE                     |                    |                          |    |          |                  |                    |    |
| 0h                       |                    |                          |    |          |                  |                    |    |
| 23                       | 22                 | 21                       | 20 | 19       | 18               | 17                 | 16 |
| RESERVED                 | PRU1_FD_ZERO_MAX_4 | PRU1_FD_ZERO_MAX_LIMIT_4 |    |          |                  | PRU1_FD_ZERO_MIN_4 |    |
| NONE                     | R/W1C              | R/W                      |    |          |                  | R/W1C              |    |
| 0h                       | 0h                 | 0h                       |    |          |                  | 0h                 |    |
| 15                       | 14                 | 13                       | 12 | 11       | 10               | 9                  | 8  |
| PRU1_FD_ZERO_MIN_LIMIT_4 |                    |                          |    |          | RESERVED         |                    |    |
| R/W                      |                    |                          |    |          | NONE             |                    |    |
| 0h                       |                    |                          |    |          | 0h               |                    |    |
| 7                        | 6                  | 5                        | 4  | 3        | 2                | 1                  | 0  |
| RESERVED                 |                    | PRU1_SD_ACC_SEL4         |    | RESERVED | PRU1_SD_CLK_INV4 | PRU1_SD_CLK_SEL4   |    |
| NONE                     |                    | R/W                      |    | NONE     | R/W              | R/W                |    |
| 0h                       |                    | 0h                       |    | 0h       | 0h               | 0h                 |    |

**Table 4-1063. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG4 Register Field Descriptions**

| Bit   | Field                    | Type  | Reset | Description |
|-------|--------------------------|-------|-------|-------------|
| 31:23 | RESERVED                 | NONE  | 0h    | Reserved    |
| 22    | PRU1_FD_ZERO_MAX_4       | R/W1C | 0h    |             |
| 21:17 | PRU1_FD_ZERO_MAX_LIMIT_4 | R/W   | 0h    |             |
| 16    | PRU1_FD_ZERO_MIN_4       | R/W1C | 0h    |             |
| 15:11 | PRU1_FD_ZERO_MIN_LIMIT_4 | R/W   | 0h    |             |
| 10:6  | RESERVED                 | NONE  | 0h    | Reserved    |
| 5:4   | PRU1_SD_ACC_SEL4         | R/W   | 0h    |             |
| 3     | RESERVED                 | NONE  | 0h    | Reserved    |
| 2     | PRU1_SD_CLK_INV4         | R/W   | 0h    |             |
| 1:0   | PRU1_SD_CLK_SEL4         | R/W   | 0h    |             |

#### 4.2.2.150 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG4 Register

#### 1 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG4 Register (Offset = B8h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1064. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 60B8h       |

**Figure 4-344. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG4 Name Register**

|                         |                    |                         |    |                       |    |                    |    |
|-------------------------|--------------------|-------------------------|----|-----------------------|----|--------------------|----|
| 31                      | 30                 | 29                      | 28 | 27                    | 26 | 25                 | 24 |
| RESERVED                |                    |                         |    |                       |    |                    |    |
| NONE                    |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |
| 23                      | 22                 | 21                      | 20 | 19                    | 18 | 17                 | 16 |
| PRU1_FD_EN_4            | PRU1_FD_ON_E_MAX_4 | PRU1_FD_ONE_MAX_LIMIT_4 |    |                       |    | PRU1_FD_ON_E_MIN_4 |    |
| R/W                     | R/W1C              | R/W                     |    |                       |    | R/W1C              |    |
| 0h                      | 0h                 | 0h                      |    |                       |    | 0h                 |    |
| 15                      | 14                 | 13                      | 12 | 11                    | 10 | 9                  | 8  |
| PRU1_FD_ONE_MIN_LIMIT_4 |                    |                         |    | PRU1_FD_WINDOW_SIZE_4 |    |                    |    |
| R/W                     |                    |                         |    | R/W                   |    |                    |    |
| 0h                      |                    |                         |    | 0h                    |    |                    |    |
| 7                       | 6                  | 5                       | 4  | 3                     | 2  | 1                  | 0  |
| PRU1_SD_SAMPLE_SIZE4    |                    |                         |    |                       |    |                    |    |
| R/W                     |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |

**Table 4-1066. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG4 Register Field Descriptions**

| Bit   | Field                   | Type  | Reset | Description |
|-------|-------------------------|-------|-------|-------------|
| 31:24 | RESERVED                | NONE  | 0h    | Reserved    |
| 23    | PRU1_FD_EN_4            | R/W   | 0h    |             |
| 22    | PRU1_FD_ONE_MAX_4       | R/W1C | 0h    |             |
| 21:17 | PRU1_FD_ONE_MAX_LIMIT_4 | R/W   | 0h    |             |
| 16    | PRU1_FD_ONE_MIN_4       | R/W1C | 0h    |             |
| 15:11 | PRU1_FD_ONE_MIN_LIMIT_4 | R/W   | 0h    |             |
| 10:8  | PRU1_FD_WINDOW_SIZE_4   | R/W   | 0h    |             |
| 7:0   | PRU1_SD_SAMPLE_SIZE4    | R/W   | 0h    |             |

#### 4.2.2.151 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG5 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG5 Register (Offset = BCh) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1067. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 60BCh       |

**Figure 4-345. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG5 Name Register**

|                          |                        |                          |    |          |                      |                        |    |
|--------------------------|------------------------|--------------------------|----|----------|----------------------|------------------------|----|
| 31                       | 30                     | 29                       | 28 | 27       | 26                   | 25                     | 24 |
| RESERVED                 |                        |                          |    |          |                      |                        |    |
| NONE                     |                        |                          |    |          |                      |                        |    |
| 0h                       |                        |                          |    |          |                      |                        |    |
| 23                       | 22                     | 21                       | 20 | 19       | 18                   | 17                     | 16 |
| RESERVED                 | PRU1_FD_ZER<br>O_MAX_5 | PRU1_FD_ZERO_MAX_LIMIT_5 |    |          |                      | PRU1_FD_ZER<br>O_MIN_5 |    |
| NONE                     | R/W1C                  | R/W                      |    |          |                      | R/W1C                  |    |
| 0h                       | 0h                     | 0h                       |    |          |                      | 0h                     |    |
| 15                       | 14                     | 13                       | 12 | 11       | 10                   | 9                      | 8  |
| PRU1_FD_ZERO_MIN_LIMIT_5 |                        |                          |    |          | RESERVED             |                        |    |
| R/W                      |                        |                          |    |          | NONE                 |                        |    |
| 0h                       |                        |                          |    |          | 0h                   |                        |    |
| 7                        | 6                      | 5                        | 4  | 3        | 2                    | 1                      | 0  |
| RESERVED                 |                        | PRU1_SD_ACC_SEL5         |    | RESERVED | PRU1_SD_CLK<br>_INV5 | PRU1_SD_CLK_SEL5       |    |
| NONE                     |                        | R/W                      |    | NONE     | R/W                  | R/W                    |    |
| 0h                       |                        | 0h                       |    | 0h       | 0h                   | 0h                     |    |

**Table 4-1069. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG5 Register Field Descriptions**

| Bit   | Field                        | Type  | Reset | Description |
|-------|------------------------------|-------|-------|-------------|
| 31:23 | RESERVED                     | NONE  | 0h    | Reserved    |
| 22    | PRU1_FD_ZERO_MAX_5           | R/W1C | 0h    |             |
| 21:17 | PRU1_FD_ZERO_MAX_L<br>IMIT_5 | R/W   | 0h    |             |
| 16    | PRU1_FD_ZERO_MIN_5           | R/W1C | 0h    |             |
| 15:11 | PRU1_FD_ZERO_MIN_LI<br>MIT_5 | R/W   | 0h    |             |
| 10:6  | RESERVED                     | NONE  | 0h    | Reserved    |
| 5:4   | PRU1_SD_ACC_SEL5             | R/W   | 0h    |             |
| 3     | RESERVED                     | NONE  | 0h    | Reserved    |
| 2     | PRU1_SD_CLK_INV5             | R/W   | 0h    |             |
| 1:0   | PRU1_SD_CLK_SEL5             | R/W   | 0h    |             |

#### 4.2.2.152 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG5 Register

#### 1 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG5 Register (Offset = C0h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1070. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 60C0h       |

**Figure 4-346. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG5 Name Register**

|                         |                    |                         |    |                       |    |                    |    |
|-------------------------|--------------------|-------------------------|----|-----------------------|----|--------------------|----|
| 31                      | 30                 | 29                      | 28 | 27                    | 26 | 25                 | 24 |
| RESERVED                |                    |                         |    |                       |    |                    |    |
| NONE                    |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |
| 23                      | 22                 | 21                      | 20 | 19                    | 18 | 17                 | 16 |
| PRU1_FD_EN_5            | PRU1_FD_ON_E_MAX_5 | PRU1_FD_ONE_MAX_LIMIT_5 |    |                       |    | PRU1_FD_ON_E_MIN_5 |    |
| R/W                     | R/W1C              | R/W                     |    |                       |    | R/W1C              |    |
| 0h                      | 0h                 | 0h                      |    |                       |    | 0h                 |    |
| 15                      | 14                 | 13                      | 12 | 11                    | 10 | 9                  | 8  |
| PRU1_FD_ONE_MIN_LIMIT_5 |                    |                         |    | PRU1_FD_WINDOW_SIZE_5 |    |                    |    |
| R/W                     |                    |                         |    | R/W                   |    |                    |    |
| 0h                      |                    |                         |    | 0h                    |    |                    |    |
| 7                       | 6                  | 5                       | 4  | 3                     | 2  | 1                  | 0  |
| PRU1_SD_SAMPLE_SIZE5    |                    |                         |    |                       |    |                    |    |
| R/W                     |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |

**Table 4-1072. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG5 Register Field Descriptions**

| Bit   | Field                   | Type  | Reset | Description |
|-------|-------------------------|-------|-------|-------------|
| 31:24 | RESERVED                | NONE  | 0h    | Reserved    |
| 23    | PRU1_FD_EN_5            | R/W   | 0h    |             |
| 22    | PRU1_FD_ONE_MAX_5       | R/W1C | 0h    |             |
| 21:17 | PRU1_FD_ONE_MAX_LIMIT_5 | R/W   | 0h    |             |
| 16    | PRU1_FD_ONE_MIN_5       | R/W1C | 0h    |             |
| 15:11 | PRU1_FD_ONE_MIN_LIMIT_5 | R/W   | 0h    |             |
| 10:8  | PRU1_FD_WINDOW_SIZE_5   | R/W   | 0h    |             |
| 7:0   | PRU1_SD_SAMPLE_SIZE5    | R/W   | 0h    |             |

#### 4.2.2.153 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG6 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG6 Register (Offset = C4h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1073. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 60C4h       |

**Figure 4-347. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG6 Name Register**

|                          |                    |                          |    |          |                  |                    |    |
|--------------------------|--------------------|--------------------------|----|----------|------------------|--------------------|----|
| 31                       | 30                 | 29                       | 28 | 27       | 26               | 25                 | 24 |
| RESERVED                 |                    |                          |    |          |                  |                    |    |
| NONE                     |                    |                          |    |          |                  |                    |    |
| 0h                       |                    |                          |    |          |                  |                    |    |
| 23                       | 22                 | 21                       | 20 | 19       | 18               | 17                 | 16 |
| RESERVED                 | PRU1_FD_ZERO_MAX_6 | PRU1_FD_ZERO_MAX_LIMIT_6 |    |          |                  | PRU1_FD_ZERO_MIN_6 |    |
| NONE                     | R/W1C              | R/W                      |    |          |                  | R/W1C              |    |
| 0h                       | 0h                 | 0h                       |    |          |                  | 0h                 |    |
| 15                       | 14                 | 13                       | 12 | 11       | 10               | 9                  | 8  |
| PRU1_FD_ZERO_MIN_LIMIT_6 |                    |                          |    |          | RESERVED         |                    |    |
| R/W                      |                    |                          |    |          | NONE             |                    |    |
| 0h                       |                    |                          |    |          | 0h               |                    |    |
| 7                        | 6                  | 5                        | 4  | 3        | 2                | 1                  | 0  |
| RESERVED                 |                    | PRU1_SD_ACC_SEL6         |    | RESERVED | PRU1_SD_CLK_INV6 | PRU1_SD_CLK_SEL6   |    |
| NONE                     |                    | R/W                      |    | NONE     | R/W              | R/W                |    |
| 0h                       |                    | 0h                       |    | 0h       | 0h               | 0h                 |    |

**Table 4-1075. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG6 Register Field Descriptions**

| Bit   | Field                    | Type  | Reset | Description |
|-------|--------------------------|-------|-------|-------------|
| 31:23 | RESERVED                 | NONE  | 0h    | Reserved    |
| 22    | PRU1_FD_ZERO_MAX_6       | R/W1C | 0h    |             |
| 21:17 | PRU1_FD_ZERO_MAX_LIMIT_6 | R/W   | 0h    |             |
| 16    | PRU1_FD_ZERO_MIN_6       | R/W1C | 0h    |             |
| 15:11 | PRU1_FD_ZERO_MIN_LIMIT_6 | R/W   | 0h    |             |
| 10:6  | RESERVED                 | NONE  | 0h    | Reserved    |
| 5:4   | PRU1_SD_ACC_SEL6         | R/W   | 0h    |             |
| 3     | RESERVED                 | NONE  | 0h    | Reserved    |
| 2     | PRU1_SD_CLK_INV6         | R/W   | 0h    |             |
| 1:0   | PRU1_SD_CLK_SEL6         | R/W   | 0h    |             |

#### 4.2.2.154 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG6 Register

#### 1 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG6 Register (Offset = C8h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1076. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 60C8h       |

**Figure 4-348. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG6 Name Register**

|                         |                    |                         |    |    |                       |    |                    |
|-------------------------|--------------------|-------------------------|----|----|-----------------------|----|--------------------|
| 31                      | 30                 | 29                      | 28 | 27 | 26                    | 25 | 24                 |
| RESERVED                |                    |                         |    |    |                       |    |                    |
| NONE                    |                    |                         |    |    |                       |    |                    |
| 0h                      |                    |                         |    |    |                       |    |                    |
| 23                      | 22                 | 21                      | 20 | 19 | 18                    | 17 | 16                 |
| PRU1_FD_EN_6            | PRU1_FD_ON_E_MAX_6 | PRU1_FD_ONE_MAX_LIMIT_6 |    |    |                       |    | PRU1_FD_ON_E_MIN_6 |
| R/W                     | R/W1C              | R/W                     |    |    |                       |    | R/W1C              |
| 0h                      | 0h                 | 0h                      |    |    |                       |    | 0h                 |
| 15                      | 14                 | 13                      | 12 | 11 | 10                    | 9  | 8                  |
| PRU1_FD_ONE_MIN_LIMIT_6 |                    |                         |    |    | PRU1_FD_WINDOW_SIZE_6 |    |                    |
| R/W                     |                    |                         |    |    | R/W                   |    |                    |
| 0h                      |                    |                         |    |    | 0h                    |    |                    |
| 7                       | 6                  | 5                       | 4  | 3  | 2                     | 1  | 0                  |
| PRU1_SD_SAMPLE_SIZE6    |                    |                         |    |    |                       |    |                    |
| R/W                     |                    |                         |    |    |                       |    |                    |
| 0h                      |                    |                         |    |    |                       |    |                    |

**Table 4-1078. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG6 Register Field Descriptions**

| Bit   | Field                   | Type  | Reset | Description |
|-------|-------------------------|-------|-------|-------------|
| 31:24 | RESERVED                | NONE  | 0h    | Reserved    |
| 23    | PRU1_FD_EN_6            | R/W   | 0h    |             |
| 22    | PRU1_FD_ONE_MAX_6       | R/W1C | 0h    |             |
| 21:17 | PRU1_FD_ONE_MAX_LIMIT_6 | R/W   | 0h    |             |
| 16    | PRU1_FD_ONE_MIN_6       | R/W1C | 0h    |             |
| 15:11 | PRU1_FD_ONE_MIN_LIMIT_6 | R/W   | 0h    |             |
| 10:8  | PRU1_FD_WINDOW_SIZE_6   | R/W   | 0h    |             |
| 7:0   | PRU1_SD_SAMPLE_SIZE6    | R/W   | 0h    |             |



#### 4.2.2.155 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG7 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG7 Register (Offset = CCh) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1079. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 60CCh       |

**Figure 4-349. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG7 Name Register**

|                          |                    |                          |    |          |                  |                  |                    |
|--------------------------|--------------------|--------------------------|----|----------|------------------|------------------|--------------------|
| 31                       | 30                 | 29                       | 28 | 27       | 26               | 25               | 24                 |
| RESERVED                 |                    |                          |    |          |                  |                  |                    |
| NONE                     |                    |                          |    |          |                  |                  |                    |
| 0h                       |                    |                          |    |          |                  |                  |                    |
| 23                       | 22                 | 21                       | 20 | 19       | 18               | 17               | 16                 |
| RESERVED                 | PRU1_FD_ZERO_MAX_7 | PRU1_FD_ZERO_MAX_LIMIT_7 |    |          |                  |                  | PRU1_FD_ZERO_MIN_7 |
| NONE                     | R/W1C              | R/W                      |    |          |                  |                  | R/W1C              |
| 0h                       | 0h                 | 0h                       |    |          |                  |                  | 0h                 |
| 15                       | 14                 | 13                       | 12 | 11       | 10               | 9                | 8                  |
| PRU1_FD_ZERO_MIN_LIMIT_7 |                    |                          |    |          | RESERVED         |                  |                    |
| R/W                      |                    |                          |    |          | NONE             |                  |                    |
| 0h                       |                    |                          |    |          | 0h               |                  |                    |
| 7                        | 6                  | 5                        | 4  | 3        | 2                | 1                | 0                  |
| RESERVED                 |                    | PRU1_SD_ACC_SEL7         |    | RESERVED | PRU1_SD_CLK_INV7 | PRU1_SD_CLK_SEL7 |                    |
| NONE                     |                    | R/W                      |    | NONE     | R/W              | R/W              |                    |
| 0h                       |                    | 0h                       |    | 0h       | 0h               | 0h               |                    |

**Table 4-1081. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG7 Register Field Descriptions**

| Bit   | Field                    | Type  | Reset | Description |
|-------|--------------------------|-------|-------|-------------|
| 31:23 | RESERVED                 | NONE  | 0h    | Reserved    |
| 22    | PRU1_FD_ZERO_MAX_7       | R/W1C | 0h    |             |
| 21:17 | PRU1_FD_ZERO_MAX_LIMIT_7 | R/W   | 0h    |             |
| 16    | PRU1_FD_ZERO_MIN_7       | R/W1C | 0h    |             |
| 15:11 | PRU1_FD_ZERO_MIN_LIMIT_7 | R/W   | 0h    |             |
| 10:6  | RESERVED                 | NONE  | 0h    | Reserved    |
| 5:4   | PRU1_SD_ACC_SEL7         | R/W   | 0h    |             |
| 3     | RESERVED                 | NONE  | 0h    | Reserved    |
| 2     | PRU1_SD_CLK_INV7         | R/W   | 0h    |             |
| 1:0   | PRU1_SD_CLK_SEL7         | R/W   | 0h    |             |

#### 4.2.2.156 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG7 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG7 Register (Offset = D0h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1082. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 60D0h       |

**Figure 4-350. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG7 Name Register**

|                         |                    |                         |    |                       |    |                    |    |
|-------------------------|--------------------|-------------------------|----|-----------------------|----|--------------------|----|
| 31                      | 30                 | 29                      | 28 | 27                    | 26 | 25                 | 24 |
| RESERVED                |                    |                         |    |                       |    |                    |    |
| NONE                    |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |
| 23                      | 22                 | 21                      | 20 | 19                    | 18 | 17                 | 16 |
| PRU1_FD_EN_7            | PRU1_FD_ON_E_MAX_7 | PRU1_FD_ONE_MAX_LIMIT_7 |    |                       |    | PRU1_FD_ON_E_MIN_7 |    |
| R/W                     | R/W1C              | R/W                     |    |                       |    | R/W1C              |    |
| 0h                      | 0h                 | 0h                      |    |                       |    | 0h                 |    |
| 15                      | 14                 | 13                      | 12 | 11                    | 10 | 9                  | 8  |
| PRU1_FD_ONE_MIN_LIMIT_7 |                    |                         |    | PRU1_FD_WINDOW_SIZE_7 |    |                    |    |
| R/W                     |                    |                         |    | R/W                   |    |                    |    |
| 0h                      |                    |                         |    | 0h                    |    |                    |    |
| 7                       | 6                  | 5                       | 4  | 3                     | 2  | 1                  | 0  |
| PRU1_SD_SAMPLE_SIZE7    |                    |                         |    |                       |    |                    |    |
| R/W                     |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |

**Table 4-1084. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG7 Register Field Descriptions**

| Bit   | Field                   | Type  | Reset | Description |
|-------|-------------------------|-------|-------|-------------|
| 31:24 | RESERVED                | NONE  | 0h    | Reserved    |
| 23    | PRU1_FD_EN_7            | R/W   | 0h    |             |
| 22    | PRU1_FD_ONE_MAX_7       | R/W1C | 0h    |             |
| 21:17 | PRU1_FD_ONE_MAX_LIMIT_7 | R/W   | 0h    |             |
| 16    | PRU1_FD_ONE_MIN_7       | R/W1C | 0h    |             |
| 15:11 | PRU1_FD_ONE_MIN_LIMIT_7 | R/W   | 0h    |             |
| 10:8  | PRU1_FD_WINDOW_SIZE_7   | R/W   | 0h    |             |
| 7:0   | PRU1_SD_SAMPLE_SIZE7    | R/W   | 0h    |             |

#### 4.2.2.157 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG8 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG8 Register (Offset = D4h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1085. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 60D4h       |

**Figure 4-351. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG8 Name Register**

|                          |                    |                          |    |          |                  |                    |    |
|--------------------------|--------------------|--------------------------|----|----------|------------------|--------------------|----|
| 31                       | 30                 | 29                       | 28 | 27       | 26               | 25                 | 24 |
| RESERVED                 |                    |                          |    |          |                  |                    |    |
| NONE                     |                    |                          |    |          |                  |                    |    |
| 0h                       |                    |                          |    |          |                  |                    |    |
| 23                       | 22                 | 21                       | 20 | 19       | 18               | 17                 | 16 |
| RESERVED                 | PRU1_FD_ZERO_MAX_8 | PRU1_FD_ZERO_MAX_LIMIT_8 |    |          |                  | PRU1_FD_ZERO_MIN_8 |    |
| NONE                     | R/W1C              | R/W                      |    |          |                  | R/W1C              |    |
| 0h                       | 0h                 | 0h                       |    |          |                  | 0h                 |    |
| 15                       | 14                 | 13                       | 12 | 11       | 10               | 9                  | 8  |
| PRU1_FD_ZERO_MIN_LIMIT_8 |                    |                          |    |          | RESERVED         |                    |    |
| R/W                      |                    |                          |    |          | NONE             |                    |    |
| 0h                       |                    |                          |    |          | 0h               |                    |    |
| 7                        | 6                  | 5                        | 4  | 3        | 2                | 1                  | 0  |
| RESERVED                 |                    | PRU1_SD_ACC_SEL8         |    | RESERVED | PRU1_SD_CLK_INV8 | PRU1_SD_CLK_SEL8   |    |
| NONE                     |                    | R/W                      |    | NONE     | R/W              | R/W                |    |
| 0h                       |                    | 0h                       |    | 0h       | 0h               | 0h                 |    |

**Table 4-1087. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_CLK\_SEL\_REG8 Register Field Descriptions**

| Bit   | Field                    | Type  | Reset | Description |
|-------|--------------------------|-------|-------|-------------|
| 31:23 | RESERVED                 | NONE  | 0h    | Reserved    |
| 22    | PRU1_FD_ZERO_MAX_8       | R/W1C | 0h    |             |
| 21:17 | PRU1_FD_ZERO_MAX_LIMIT_8 | R/W   | 0h    |             |
| 16    | PRU1_FD_ZERO_MIN_8       | R/W1C | 0h    |             |
| 15:11 | PRU1_FD_ZERO_MIN_LIMIT_8 | R/W   | 0h    |             |
| 10:6  | RESERVED                 | NONE  | 0h    | Reserved    |
| 5:4   | PRU1_SD_ACC_SEL8         | R/W   | 0h    |             |
| 3     | RESERVED                 | NONE  | 0h    | Reserved    |
| 2     | PRU1_SD_CLK_INV8         | R/W   | 0h    |             |
| 1:0   | PRU1_SD_CLK_SEL8         | R/W   | 0h    |             |

#### 4.2.2.158 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG8 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG8 Register (Offset = D8h) [reset = 0h]

SD Register

Return to [Summary Table](#)
**Table 4-1088. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 60D8h       |

**Figure 4-352. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG8 Name Register**

|                         |                    |                         |    |                       |    |                    |    |
|-------------------------|--------------------|-------------------------|----|-----------------------|----|--------------------|----|
| 31                      | 30                 | 29                      | 28 | 27                    | 26 | 25                 | 24 |
| RESERVED                |                    |                         |    |                       |    |                    |    |
| NONE                    |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |
| 23                      | 22                 | 21                      | 20 | 19                    | 18 | 17                 | 16 |
| PRU1_FD_EN_8            | PRU1_FD_ON_E_MAX_8 | PRU1_FD_ONE_MAX_LIMIT_8 |    |                       |    | PRU1_FD_ON_E_MIN_8 |    |
| R/W                     | R/W1C              | R/W                     |    |                       |    | R/W1C              |    |
| 0h                      | 0h                 | 0h                      |    |                       |    | 0h                 |    |
| 15                      | 14                 | 13                      | 12 | 11                    | 10 | 9                  | 8  |
| PRU1_FD_ONE_MIN_LIMIT_8 |                    |                         |    | PRU1_FD_WINDOW_SIZE_8 |    |                    |    |
| R/W                     |                    |                         |    | R/W                   |    |                    |    |
| 0h                      |                    |                         |    | 0h                    |    |                    |    |
| 7                       | 6                  | 5                       | 4  | 3                     | 2  | 1                  | 0  |
| PRU1_SD_SAMPLE_SIZE8    |                    |                         |    |                       |    |                    |    |
| R/W                     |                    |                         |    |                       |    |                    |    |
| 0h                      |                    |                         |    |                       |    |                    |    |

**Table 4-1090. ICSSM\_PR1\_CFG\_SLV\_PRU1\_SD\_SAMPLE\_SIZE\_REG8 Register Field Descriptions**

| Bit   | Field                   | Type  | Reset | Description |
|-------|-------------------------|-------|-------|-------------|
| 31:24 | RESERVED                | NONE  | 0h    | Reserved    |
| 23    | PRU1_FD_EN_8            | R/W   | 0h    |             |
| 22    | PRU1_FD_ONE_MAX_8       | R/W1C | 0h    |             |
| 21:17 | PRU1_FD_ONE_MAX_LIMIT_8 | R/W   | 0h    |             |
| 16    | PRU1_FD_ONE_MIN_8       | R/W1C | 0h    |             |
| 15:11 | PRU1_FD_ONE_MIN_LIMIT_8 | R/W   | 0h    |             |
| 10:8  | PRU1_FD_WINDOW_SIZE_8   | R/W   | 0h    |             |
| 7:0   | PRU1_SD_SAMPLE_SIZE8    | R/W   | 0h    |             |

#### 4.2.2.159 ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_RX\_CFG\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_RX\_CFG\_REG Register (Offset = E0h) [reset = Fh]

ED Register

Return to [Summary Table](#)
**Table 4-1091. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 60E0h       |

**Figure 4-353. ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_RX\_CFG\_REG Name Register**

|                            |          |    |                    |                   |                        |    |    |
|----------------------------|----------|----|--------------------|-------------------|------------------------|----|----|
| 31                         | 30       | 29 | 28                 | 27                | 26                     | 25 | 24 |
| PRU0_ED_RX_DIV_FACTOR      |          |    |                    |                   |                        |    |    |
| R/W                        |          |    |                    |                   |                        |    |    |
| 0h                         |          |    |                    |                   |                        |    |    |
| 23                         | 22       | 21 | 20                 | 19                | 18                     | 17 | 16 |
| PRU0_ED_RX_DIV_FACTOR      |          |    |                    |                   |                        |    |    |
| R/W                        |          |    |                    |                   |                        |    |    |
| 0h                         |          |    |                    |                   |                        |    |    |
| 15                         | 14       | 13 | 12                 | 11                | 10                     | 9  | 8  |
| PRU0_ED_RX_DIV_FACTOR_FRAC | RESERVED |    |                    |                   |                        |    |    |
| R/W                        | NONE     |    |                    |                   |                        |    |    |
| 0h                         | 0h       |    |                    |                   |                        |    |    |
| 7                          | 6        | 5  | 4                  | 3                 | 2                      | 1  | 0  |
| RESERVED                   |          |    | PRU0_ED_RX_CLK_SEL | PRU0_ED_RX_SB_POL | PRU0_ED_RX_SAMPLE_SIZE |    |    |
| NONE                       |          |    | R/W                | R/W               | R/W                    |    |    |
| 0h                         |          |    | 0h                 | 1h                | 7h                     |    |    |

**Table 4-1093. ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_RX\_CFG\_REG Register Field Descriptions**

| Bit   | Field                      | Type | Reset | Description |
|-------|----------------------------|------|-------|-------------|
| 31:16 | PRU0_ED_RX_DIV_FACTOR      | R/W  | 0h    |             |
| 15    | PRU0_ED_RX_DIV_FACTOR_FRAC | R/W  | 0h    |             |
| 14:5  | RESERVED                   | NONE | 0h    | Reserved    |
| 4     | PRU0_ED_RX_CLK_SEL         | R/W  | 0h    |             |
| 3     | PRU0_ED_RX_SB_POL          | R/W  | 1h    |             |
| 2:0   | PRU0_ED_RX_SAMPLE_SIZE     | R/W  | 7h    |             |

#### 4.2.2.160 ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_TX\_CFG\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_TX\_CFG\_REG Register (Offset = E4h) [reset = 700h]

Register

Return to [Summary Table](#)
**Table 4-1094. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 60E4h       |

**Figure 4-354. ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_TX\_CFG\_REG Name Register**

|                            |                |                |                    |                     |                      |                      |                      |
|----------------------------|----------------|----------------|--------------------|---------------------|----------------------|----------------------|----------------------|
| 31                         | 30             | 29             | 28                 | 27                  | 26                   | 25                   | 24                   |
| PRU0_ED_TX_DIV_FACTOR      |                |                |                    |                     |                      |                      |                      |
| R/W                        |                |                |                    |                     |                      |                      |                      |
| 0h                         |                |                |                    |                     |                      |                      |                      |
| 23                         | 22             | 21             | 20                 | 19                  | 18                   | 17                   | 16                   |
| PRU0_ED_TX_DIV_FACTOR      |                |                |                    |                     |                      |                      |                      |
| R/W                        |                |                |                    |                     |                      |                      |                      |
| 0h                         |                |                |                    |                     |                      |                      |                      |
| 15                         | 14             | 13             | 12                 | 11                  | 10                   | 9                    | 8                    |
| PRU0_ED_TX_DIV_FACTOR_FRAC | RESERVED       |                |                    | PRU0_ENDAT_SHARE_EN | PRU0_ENDAT2_CLK_SYNC | PRU0_ENDAT1_CLK_SYNC | PRU0_ENDAT0_CLK_SYNC |
| R/W                        | NONE           |                |                    | R/W                 | R                    | R                    | R                    |
| 0h                         | 0h             |                |                    | 0h                  | 1h                   | 1h                   | 1h                   |
| 7                          | 6              | 5              | 4                  | 3                   | 2                    | 1                    | 0                    |
| PRU0_ED_BUSY_2             | PRU0_ED_BUSY_1 | PRU0_ED_BUSY_0 | PRU0_ED_TX_CLK_SEL | RESERVED            |                      |                      |                      |
| R                          | R              | R              | R/W                | NONE                |                      |                      |                      |
| 0h                         | 0h             | 0h             | 0h                 | 0h                  |                      |                      |                      |

**Table 4-1096. ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_TX\_CFG\_REG Register Field Descriptions**

| Bit   | Field                      | Type | Reset | Description |
|-------|----------------------------|------|-------|-------------|
| 31:16 | PRU0_ED_TX_DIV_FACTOR      | R/W  | 0h    |             |
| 15    | PRU0_ED_TX_DIV_FACTOR_FRAC | R/W  | 0h    |             |
| 14:12 | RESERVED                   | NONE | 0h    | Reserved    |
| 11    | PRU0_ENDAT_SHARE_EN        | R/W  | 0h    |             |
| 10    | PRU0_ENDAT2_CLK_SYNC       | R    | 1h    |             |
| 9     | PRU0_ENDAT1_CLK_SYNC       | R    | 1h    |             |
| 8     | PRU0_ENDAT0_CLK_SYNC       | R    | 1h    |             |
| 7     | PRU0_ED_BUSY_2             | R    | 0h    |             |
| 6     | PRU0_ED_BUSY_1             | R    | 0h    |             |
| 5     | PRU0_ED_BUSY_0             | R    | 0h    |             |
| 4     | PRU0_ED_TX_CLK_SEL         | R/W  | 0h    |             |

**Table 4-1096. ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_TX\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 3:0 | RESERVED | NONE | 0h    | Reserved    |

#### 4.2.2.161 ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_CH0\_CFG0\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_CH0\_CFG0\_REG Register (Offset = E8h) [reset = 0h]

ED Register

Return to [Summary Table](#)
**Table 4-1097. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 60E8h       |

**Figure 4-355. ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_CH0\_CFG0\_REG Name Register**

| 31                         | 30                  | 29                      | 28                | 27                     | 26               | 25 | 24 |
|----------------------------|---------------------|-------------------------|-------------------|------------------------|------------------|----|----|
| PRU0_ED_TX_FIFO_SWAP_BITS0 | PRU0_ED_SW_CLK_OUT0 | PRU0_ED_CLK_OUT_OVR_EN0 | PRU0_ED_RX_SNOOP0 | PRU0_ED_RX_FRAME_SIZE0 |                  |    |    |
| R/W                        | R/W                 | R/W                     | R                 | R/W                    |                  |    |    |
| 0h                         | 0h                  | 0h                      | 0h                | 0h                     |                  |    |    |
| 23                         | 22                  | 21                      | 20                | 19                     | 18               | 17 | 16 |
| PRU0_ED_RX_FRAME_SIZE0     |                     |                         |                   |                        |                  |    |    |
| R/W                        |                     |                         |                   |                        |                  |    |    |
| 0h                         |                     |                         |                   |                        |                  |    |    |
| 15                         | 14                  | 13                      | 12                | 11                     | 10               | 9  | 8  |
| PRU0_ED_TX_FRAME_SIZE0     |                     |                         |                   |                        | PRU0_ED_TX_WDLY0 |    |    |
| R/W                        |                     |                         |                   |                        | R/W              |    |    |
| 0h                         |                     |                         |                   |                        | 0h               |    |    |
| 7                          | 6                   | 5                       | 4                 | 3                      | 2                | 1  | 0  |
| PRU0_ED_TX_WDLY0           |                     |                         |                   |                        |                  |    |    |
| R/W                        |                     |                         |                   |                        |                  |    |    |
| 0h                         |                     |                         |                   |                        |                  |    |    |

**Table 4-1099. ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_CH0\_CFG0\_REG Register Field Descriptions**

| Bit   | Field                      | Type | Reset | Description |
|-------|----------------------------|------|-------|-------------|
| 31    | PRU0_ED_TX_FIFO_SWAP_BITS0 | R/W  | 0h    |             |
| 30    | PRU0_ED_SW_CLK_OUT0        | R/W  | 0h    |             |
| 29    | PRU0_ED_CLK_OUT_OVR_EN0    | R/W  | 0h    |             |
| 28    | PRU0_ED_RX_SNOOP0          | R    | 0h    |             |
| 27:16 | PRU0_ED_RX_FRAME_SIZE0     | R/W  | 0h    |             |
| 15:11 | PRU0_ED_TX_FRAME_SIZE0     | R/W  | 0h    |             |
| 10:0  | PRU0_ED_TX_WDLY0           | R/W  | 0h    |             |



#### 4.2.2.162 ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_CH0\_CFG1\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_CH0\_CFG1\_REG Register (Offset = ECh) [reset = 0h]

ED Register

Return to [Summary Table](#)
**Table 4-1100. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 60ECh       |

**Figure 4-356. ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_CH0\_CFG1\_REG Name Register**

|                            |    |    |    |    |    |    |    |
|----------------------------|----|----|----|----|----|----|----|
| 31                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PRU0_ED_RX_EN_COUNTER0     |    |    |    |    |    |    |    |
| R/W                        |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |
| 23                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PRU0_ED_RX_EN_COUNTER0     |    |    |    |    |    |    |    |
| R/W                        |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |
| 15                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PRU0_ED_TST_DELAY_COUNTER0 |    |    |    |    |    |    |    |
| R/W                        |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |
| 7                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PRU0_ED_TST_DELAY_COUNTER0 |    |    |    |    |    |    |    |
| R/W                        |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |

**Table 4-1102. ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_CH0\_CFG1\_REG Register Field Descriptions**

| Bit   | Field                      | Type | Reset | Description |
|-------|----------------------------|------|-------|-------------|
| 31:16 | PRU0_ED_RX_EN_COUNTER0     | R/W  | 0h    |             |
| 15:0  | PRU0_ED_TST_DELAY_COUNTER0 | R/W  | 0h    |             |

#### 4.2.2.163 ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_CH1\_CFG0\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_CH1\_CFG0\_REG Register (Offset = F0h) [reset = 0h]

ED Register

Return to [Summary Table](#)
**Table 4-1103. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 60F0h       |

**Figure 4-357. ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_CH1\_CFG0\_REG Name Register**

| 31                         | 30                  | 29                      | 28                | 27                     | 26               | 25 | 24 |
|----------------------------|---------------------|-------------------------|-------------------|------------------------|------------------|----|----|
| PRU0_ED_TX_FIFO_SWAP_BITS1 | PRU0_ED_SW_CLK_OUT1 | PRU0_ED_CLK_OUT_OVR_EN1 | PRU0_ED_RX_SNOOP1 | PRU0_ED_RX_FRAME_SIZE1 |                  |    |    |
| R/W                        | R/W                 | R/W                     | R                 | R/W                    |                  |    |    |
| 0h                         | 0h                  | 0h                      | 0h                | 0h                     |                  |    |    |
| 23                         | 22                  | 21                      | 20                | 19                     | 18               | 17 | 16 |
| PRU0_ED_RX_FRAME_SIZE1     |                     |                         |                   |                        |                  |    |    |
| R/W                        |                     |                         |                   |                        |                  |    |    |
| 0h                         |                     |                         |                   |                        |                  |    |    |
| 15                         | 14                  | 13                      | 12                | 11                     | 10               | 9  | 8  |
| PRU0_ED_TX_FRAME_SIZE1     |                     |                         |                   |                        | PRU0_ED_TX_WDLY1 |    |    |
| R/W                        |                     |                         |                   |                        | R/W              |    |    |
| 0h                         |                     |                         |                   |                        | 0h               |    |    |
| 7                          | 6                   | 5                       | 4                 | 3                      | 2                | 1  | 0  |
| PRU0_ED_TX_WDLY1           |                     |                         |                   |                        |                  |    |    |
| R/W                        |                     |                         |                   |                        |                  |    |    |
| 0h                         |                     |                         |                   |                        |                  |    |    |

**Table 4-1105. ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_CH1\_CFG0\_REG Register Field Descriptions**

| Bit   | Field                      | Type | Reset | Description |
|-------|----------------------------|------|-------|-------------|
| 31    | PRU0_ED_TX_FIFO_SWAP_BITS1 | R/W  | 0h    |             |
| 30    | PRU0_ED_SW_CLK_OUT1        | R/W  | 0h    |             |
| 29    | PRU0_ED_CLK_OUT_OVR_EN1    | R/W  | 0h    |             |
| 28    | PRU0_ED_RX_SNOOP1          | R    | 0h    |             |
| 27:16 | PRU0_ED_RX_FRAME_SIZE1     | R/W  | 0h    |             |
| 15:11 | PRU0_ED_TX_FRAME_SIZE1     | R/W  | 0h    |             |
| 10:0  | PRU0_ED_TX_WDLY1           | R/W  | 0h    |             |

#### 4.2.2.164 ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_CH1\_CFG1\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_CH1\_CFG1\_REG Register (Offset = F4h) [reset = 0h]

ED Register

Return to [Summary Table](#)
**Table 4-1106. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 60F4h       |

**Figure 4-358. ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_CH1\_CFG1\_REG Name Register**

|                            |    |    |    |    |    |    |    |
|----------------------------|----|----|----|----|----|----|----|
| 31                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PRU0_ED_RX_EN_COUNTER1     |    |    |    |    |    |    |    |
| R/W                        |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |
| 23                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PRU0_ED_RX_EN_COUNTER1     |    |    |    |    |    |    |    |
| R/W                        |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |
| 15                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PRU0_ED_TST_DELAY_COUNTER1 |    |    |    |    |    |    |    |
| R/W                        |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |
| 7                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PRU0_ED_TST_DELAY_COUNTER1 |    |    |    |    |    |    |    |
| R/W                        |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |

**Table 4-1108. ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_CH1\_CFG1\_REG Register Field Descriptions**

| Bit   | Field                      | Type | Reset | Description |
|-------|----------------------------|------|-------|-------------|
| 31:16 | PRU0_ED_RX_EN_COUNTER1     | R/W  | 0h    |             |
| 15:0  | PRU0_ED_TST_DELAY_COUNTER1 | R/W  | 0h    |             |

#### 4.2.2.165 ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_CH2\_CFG0\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_CH2\_CFG0\_REG Register (Offset = F8h) [reset = 0h]

ED Register

Return to [Summary Table](#)
**Table 4-1109. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 60F8h       |

**Figure 4-359. ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_CH2\_CFG0\_REG Name Register**

| 31                         | 30                  | 29                      | 28                | 27                     | 26               | 25 | 24 |
|----------------------------|---------------------|-------------------------|-------------------|------------------------|------------------|----|----|
| PRU0_ED_TX_FIFO_SWAP_BITS2 | PRU0_ED_SW_CLK_OUT2 | PRU0_ED_CLK_OUT_OVR_EN2 | PRU0_ED_RX_SNOOP2 | PRU0_ED_RX_FRAME_SIZE2 |                  |    |    |
| R/W                        | R/W                 | R/W                     | R                 | R/W                    |                  |    |    |
| 0h                         | 0h                  | 0h                      | 0h                | 0h                     |                  |    |    |
| 23                         | 22                  | 21                      | 20                | 19                     | 18               | 17 | 16 |
| PRU0_ED_RX_FRAME_SIZE2     |                     |                         |                   |                        |                  |    |    |
| R/W                        |                     |                         |                   |                        |                  |    |    |
| 0h                         |                     |                         |                   |                        |                  |    |    |
| 15                         | 14                  | 13                      | 12                | 11                     | 10               | 9  | 8  |
| PRU0_ED_TX_FRAME_SIZE2     |                     |                         |                   |                        | PRU0_ED_TX_WDLY2 |    |    |
| R/W                        |                     |                         |                   |                        | R/W              |    |    |
| 0h                         |                     |                         |                   |                        | 0h               |    |    |
| 7                          | 6                   | 5                       | 4                 | 3                      | 2                | 1  | 0  |
| PRU0_ED_TX_WDLY2           |                     |                         |                   |                        |                  |    |    |
| R/W                        |                     |                         |                   |                        |                  |    |    |
| 0h                         |                     |                         |                   |                        |                  |    |    |

**Table 4-1111. ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_CH2\_CFG0\_REG Register Field Descriptions**

| Bit   | Field                      | Type | Reset | Description |
|-------|----------------------------|------|-------|-------------|
| 31    | PRU0_ED_TX_FIFO_SWAP_BITS2 | R/W  | 0h    |             |
| 30    | PRU0_ED_SW_CLK_OUT2        | R/W  | 0h    |             |
| 29    | PRU0_ED_CLK_OUT_OVR_EN2    | R/W  | 0h    |             |
| 28    | PRU0_ED_RX_SNOOP2          | R    | 0h    |             |
| 27:16 | PRU0_ED_RX_FRAME_SIZE2     | R/W  | 0h    |             |
| 15:11 | PRU0_ED_TX_FRAME_SIZE2     | R/W  | 0h    |             |
| 10:0  | PRU0_ED_TX_WDLY2           | R/W  | 0h    |             |

#### 4.2.2.166 ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_CH2\_CFG1\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_CH2\_CFG1\_REG Register (Offset = FCh) [reset = 0h]

ED Register

Return to [Summary Table](#)

**Table 4-1112. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 60FCh       |

**Figure 4-360. ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_CH2\_CFG1\_REG Name Register**

|                            |    |    |    |    |    |    |    |
|----------------------------|----|----|----|----|----|----|----|
| 31                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PRU0_ED_RX_EN_COUNTER2     |    |    |    |    |    |    |    |
| R/W                        |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |
| 23                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PRU0_ED_RX_EN_COUNTER2     |    |    |    |    |    |    |    |
| R/W                        |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |
| 15                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PRU0_ED_TST_DELAY_COUNTER2 |    |    |    |    |    |    |    |
| R/W                        |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |
| 7                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PRU0_ED_TST_DELAY_COUNTER2 |    |    |    |    |    |    |    |
| R/W                        |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |

**Table 4-1114. ICSSM\_PR1\_CFG\_SLV\_PRU0\_ED\_CH2\_CFG1\_REG Register Field Descriptions**

| Bit   | Field                      | Type | Reset | Description |
|-------|----------------------------|------|-------|-------------|
| 31:16 | PRU0_ED_RX_EN_COUNTER2     | R/W  | 0h    |             |
| 15:0  | PRU0_ED_TST_DELAY_COUNTER2 | R/W  | 0h    |             |

#### 4.2.2.167 ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_RX\_CFG\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_RX\_CFG\_REG Register (Offset = 100h) [reset = Fh]

ED Register

Return to [Summary Table](#)
**Table 4-1115. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6100h       |

**Figure 4-361. ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_RX\_CFG\_REG Name Register**

|                            |          |    |                    |                   |                        |    |    |
|----------------------------|----------|----|--------------------|-------------------|------------------------|----|----|
| 31                         | 30       | 29 | 28                 | 27                | 26                     | 25 | 24 |
| PRU1_ED_RX_DIV_FACTOR      |          |    |                    |                   |                        |    |    |
| R/W                        |          |    |                    |                   |                        |    |    |
| 0h                         |          |    |                    |                   |                        |    |    |
| 23                         | 22       | 21 | 20                 | 19                | 18                     | 17 | 16 |
| PRU1_ED_RX_DIV_FACTOR      |          |    |                    |                   |                        |    |    |
| R/W                        |          |    |                    |                   |                        |    |    |
| 0h                         |          |    |                    |                   |                        |    |    |
| 15                         | 14       | 13 | 12                 | 11                | 10                     | 9  | 8  |
| PRU1_ED_RX_DIV_FACTOR_FRAC | RESERVED |    |                    |                   |                        |    |    |
| R/W                        | NONE     |    |                    |                   |                        |    |    |
| 0h                         | 0h       |    |                    |                   |                        |    |    |
| 7                          | 6        | 5  | 4                  | 3                 | 2                      | 1  | 0  |
| RESERVED                   |          |    | PRU1_ED_RX_CLK_SEL | PRU1_ED_RX_SB_POL | PRU1_ED_RX_SAMPLE_SIZE |    |    |
| NONE                       |          |    | R/W                | R/W               | R/W                    |    |    |
| 0h                         |          |    | 0h                 | 1h                | 7h                     |    |    |

**Table 4-1117. ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_RX\_CFG\_REG Register Field Descriptions**

| Bit   | Field                      | Type | Reset | Description |
|-------|----------------------------|------|-------|-------------|
| 31:16 | PRU1_ED_RX_DIV_FACTOR      | R/W  | 0h    |             |
| 15    | PRU1_ED_RX_DIV_FACTOR_FRAC | R/W  | 0h    |             |
| 14:5  | RESERVED                   | NONE | 0h    | Reserved    |
| 4     | PRU1_ED_RX_CLK_SEL         | R/W  | 0h    |             |
| 3     | PRU1_ED_RX_SB_POL          | R/W  | 1h    |             |
| 2:0   | PRU1_ED_RX_SAMPLE_SIZE     | R/W  | 7h    |             |

#### 4.2.2.168 ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_TX\_CFG\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_TX\_CFG\_REG Register (Offset = 104h) [reset = 700h]

ED Register

Return to [Summary Table](#)
**Table 4-1118. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6104h       |

**Figure 4-362. ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_TX\_CFG\_REG Name Register**

|                            |                 |                 |                    |                     |                      |                      |                      |
|----------------------------|-----------------|-----------------|--------------------|---------------------|----------------------|----------------------|----------------------|
| 31                         | 30              | 29              | 28                 | 27                  | 26                   | 25                   | 24                   |
| PRU1_ED_TX_DIV_FACTOR      |                 |                 |                    |                     |                      |                      |                      |
| R/W                        |                 |                 |                    |                     |                      |                      |                      |
| 0h                         |                 |                 |                    |                     |                      |                      |                      |
| 23                         | 22              | 21              | 20                 | 19                  | 18                   | 17                   | 16                   |
| PRU1_ED_TX_DIV_FACTOR      |                 |                 |                    |                     |                      |                      |                      |
| R/W                        |                 |                 |                    |                     |                      |                      |                      |
| 0h                         |                 |                 |                    |                     |                      |                      |                      |
| 15                         | 14              | 13              | 12                 | 11                  | 10                   | 9                    | 8                    |
| PRU1_ED_TX_DIV_FACTOR_FRAC | RESERVED        |                 |                    | PRU1_ENDAT_SHARE_EN | PRU1_ENDAT2_CLK_SYNC | PRU1_ENDAT1_CLK_SYNC | PRU1_ENDAT0_CLK_SYNC |
| R/W                        | NONE            |                 |                    | R/W                 | R                    | R                    | R                    |
| 0h                         | 0h              |                 |                    | 0h                  | 1h                   | 1h                   | 1h                   |
| 7                          | 6               | 5               | 4                  | 3                   | 2                    | 1                    | 0                    |
| PRU1_ED_BUS_Y_2            | PRU1_ED_BUS_Y_1 | PRU1_ED_BUS_Y_0 | PRU1_ED_TX_CLK_SEL | RESERVED            |                      |                      |                      |
| R                          | R               | R               | R/W                | NONE                |                      |                      |                      |
| 0h                         | 0h              | 0h              | 0h                 | 0h                  |                      |                      |                      |

**Table 4-1120. ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_TX\_CFG\_REG Register Field Descriptions**

| Bit   | Field                      | Type | Reset | Description |
|-------|----------------------------|------|-------|-------------|
| 31:16 | PRU1_ED_TX_DIV_FACTOR      | R/W  | 0h    |             |
| 15    | PRU1_ED_TX_DIV_FACTOR_FRAC | R/W  | 0h    |             |
| 14:12 | RESERVED                   | NONE | 0h    | Reserved    |
| 11    | PRU1_ENDAT_SHARE_EN        | R/W  | 0h    |             |
| 10    | PRU1_ENDAT2_CLK_SYNC       | R    | 1h    |             |
| 9     | PRU1_ENDAT1_CLK_SYNC       | R    | 1h    |             |
| 8     | PRU1_ENDAT0_CLK_SYNC       | R    | 1h    |             |
| 7     | PRU1_ED_BUSY_2             | R    | 0h    |             |
| 6     | PRU1_ED_BUSY_1             | R    | 0h    |             |
| 5     | PRU1_ED_BUSY_0             | R    | 0h    |             |
| 4     | PRU1_ED_TX_CLK_SEL         | R/W  | 0h    |             |

**Table 4-1120. ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_TX\_CFG\_REG Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 3:0 | RESERVED | NONE | 0h    | Reserved    |



#### 4.2.2.169 ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_CH0\_CFG0\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_CH0\_CFG0\_REG Register (Offset = 108h) [reset = 0h]

ED Register

Return to [Summary Table](#)
**Table 4-1121. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6108h       |

**Figure 4-363. ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_CH0\_CFG0\_REG Name Register**

| 31                         | 30                  | 29                      | 28                | 27                     | 26               | 25 | 24 |
|----------------------------|---------------------|-------------------------|-------------------|------------------------|------------------|----|----|
| PRU1_ED_TX_FIFO_SWAP_BITS0 | PRU1_ED_SW_CLK_OUT0 | PRU1_ED_CLK_OUT_OVR_EN0 | PRU1_ED_RX_SNOOP0 | PRU1_ED_RX_FRAME_SIZE0 |                  |    |    |
| R/W                        | R/W                 | R/W                     | R                 | R/W                    |                  |    |    |
| 0h                         | 0h                  | 0h                      | 0h                | 0h                     |                  |    |    |
| 23                         | 22                  | 21                      | 20                | 19                     | 18               | 17 | 16 |
| PRU1_ED_RX_FRAME_SIZE0     |                     |                         |                   |                        |                  |    |    |
| R/W                        |                     |                         |                   |                        |                  |    |    |
| 0h                         |                     |                         |                   |                        |                  |    |    |
| 15                         | 14                  | 13                      | 12                | 11                     | 10               | 9  | 8  |
| PRU1_ED_TX_FRAME_SIZE0     |                     |                         |                   |                        | PRU1_ED_TX_WDLY0 |    |    |
| R/W                        |                     |                         |                   |                        | R/W              |    |    |
| 0h                         |                     |                         |                   |                        | 0h               |    |    |
| 7                          | 6                   | 5                       | 4                 | 3                      | 2                | 1  | 0  |
| PRU1_ED_TX_WDLY0           |                     |                         |                   |                        |                  |    |    |
| R/W                        |                     |                         |                   |                        |                  |    |    |
| 0h                         |                     |                         |                   |                        |                  |    |    |

**Table 4-1123. ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_CH0\_CFG0\_REG Register Field Descriptions**

| Bit   | Field                      | Type | Reset | Description |
|-------|----------------------------|------|-------|-------------|
| 31    | PRU1_ED_TX_FIFO_SWAP_BITS0 | R/W  | 0h    |             |
| 30    | PRU1_ED_SW_CLK_OUT0        | R/W  | 0h    |             |
| 29    | PRU1_ED_CLK_OUT_OVR_EN0    | R/W  | 0h    |             |
| 28    | PRU1_ED_RX_SNOOP0          | R    | 0h    |             |
| 27:16 | PRU1_ED_RX_FRAME_SIZE0     | R/W  | 0h    |             |
| 15:11 | PRU1_ED_TX_FRAME_SIZE0     | R/W  | 0h    |             |
| 10:0  | PRU1_ED_TX_WDLY0           | R/W  | 0h    |             |

#### 4.2.2.170 ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_CH0\_CFG1\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_CH0\_CFG1\_REG Register (Offset = 10Ch) [reset = 0h]

ED Register

Return to [Summary Table](#)
**Table 4-1124. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 610Ch       |

**Figure 4-364. ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_CH0\_CFG1\_REG Name Register**

|                            |    |    |    |    |    |    |    |
|----------------------------|----|----|----|----|----|----|----|
| 31                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PRU1_ED_RX_EN_COUNTER0     |    |    |    |    |    |    |    |
| R/W                        |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |
| 23                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PRU1_ED_RX_EN_COUNTER0     |    |    |    |    |    |    |    |
| R/W                        |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |
| 15                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PRU1_ED_TST_DELAY_COUNTER0 |    |    |    |    |    |    |    |
| R/W                        |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |
| 7                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PRU1_ED_TST_DELAY_COUNTER0 |    |    |    |    |    |    |    |
| R/W                        |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |

**Table 4-1126. ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_CH0\_CFG1\_REG Register Field Descriptions**

| Bit   | Field                      | Type | Reset | Description |
|-------|----------------------------|------|-------|-------------|
| 31:16 | PRU1_ED_RX_EN_COUNTER0     | R/W  | 0h    |             |
| 15:0  | PRU1_ED_TST_DELAY_COUNTER0 | R/W  | 0h    |             |

#### 4.2.2.171 ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_CH1\_CFG0\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_CH1\_CFG0\_REG Register (Offset = 110h) [reset = 0h]

ED Register

Return to [Summary Table](#)
**Table 4-1127. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6110h       |

**Figure 4-365. ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_CH1\_CFG0\_REG Name Register**

| 31                         | 30                  | 29                      | 28                | 27                     | 26               | 25 | 24 |
|----------------------------|---------------------|-------------------------|-------------------|------------------------|------------------|----|----|
| PRU1_ED_TX_FIFO_SWAP_BITS1 | PRU1_ED_SW_CLK_OUT1 | PRU1_ED_CLK_OUT_OVR_EN1 | PRU1_ED_RX_SNOOP1 | PRU1_ED_RX_FRAME_SIZE1 |                  |    |    |
| R/W                        | R/W                 | R/W                     | R                 | R/W                    |                  |    |    |
| 0h                         | 0h                  | 0h                      | 0h                | 0h                     |                  |    |    |
| 23                         | 22                  | 21                      | 20                | 19                     | 18               | 17 | 16 |
| PRU1_ED_RX_FRAME_SIZE1     |                     |                         |                   |                        |                  |    |    |
| R/W                        |                     |                         |                   |                        |                  |    |    |
| 0h                         |                     |                         |                   |                        |                  |    |    |
| 15                         | 14                  | 13                      | 12                | 11                     | 10               | 9  | 8  |
| PRU1_ED_TX_FRAME_SIZE1     |                     |                         |                   |                        | PRU1_ED_TX_WDLY1 |    |    |
| R/W                        |                     |                         |                   |                        | R/W              |    |    |
| 0h                         |                     |                         |                   |                        | 0h               |    |    |
| 7                          | 6                   | 5                       | 4                 | 3                      | 2                | 1  | 0  |
| PRU1_ED_TX_WDLY1           |                     |                         |                   |                        |                  |    |    |
| R/W                        |                     |                         |                   |                        |                  |    |    |
| 0h                         |                     |                         |                   |                        |                  |    |    |

**Table 4-1129. ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_CH1\_CFG0\_REG Register Field Descriptions**

| Bit   | Field                      | Type | Reset | Description |
|-------|----------------------------|------|-------|-------------|
| 31    | PRU1_ED_TX_FIFO_SWAP_BITS1 | R/W  | 0h    |             |
| 30    | PRU1_ED_SW_CLK_OUT1        | R/W  | 0h    |             |
| 29    | PRU1_ED_CLK_OUT_OVR_EN1    | R/W  | 0h    |             |
| 28    | PRU1_ED_RX_SNOOP1          | R    | 0h    |             |
| 27:16 | PRU1_ED_RX_FRAME_SIZE1     | R/W  | 0h    |             |
| 15:11 | PRU1_ED_TX_FRAME_SIZE1     | R/W  | 0h    |             |
| 10:0  | PRU1_ED_TX_WDLY1           | R/W  | 0h    |             |

#### 4.2.2.172 ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_CH1\_CFG1\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_CH1\_CFG1\_REG Register (Offset = 114h) [reset = 0h]

ED Register

Return to [Summary Table](#)
**Table 4-1130. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6114h       |

**Figure 4-366. ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_CH1\_CFG1\_REG Name Register**

|                            |    |    |    |    |    |    |    |
|----------------------------|----|----|----|----|----|----|----|
| 31                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PRU1_ED_RX_EN_COUNTER1     |    |    |    |    |    |    |    |
| R/W                        |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |
| 23                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PRU1_ED_RX_EN_COUNTER1     |    |    |    |    |    |    |    |
| R/W                        |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |
| 15                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PRU1_ED_TST_DELAY_COUNTER1 |    |    |    |    |    |    |    |
| R/W                        |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |
| 7                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PRU1_ED_TST_DELAY_COUNTER1 |    |    |    |    |    |    |    |
| R/W                        |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |

**Table 4-1132. ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_CH1\_CFG1\_REG Register Field Descriptions**

| Bit   | Field                      | Type | Reset | Description |
|-------|----------------------------|------|-------|-------------|
| 31:16 | PRU1_ED_RX_EN_COUNTER1     | R/W  | 0h    |             |
| 15:0  | PRU1_ED_TST_DELAY_COUNTER1 | R/W  | 0h    |             |

#### 4.2.2.173 ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_CH2\_CFG0\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_CH2\_CFG0\_REG Register (Offset = 118h) [reset = 0h]

ED Register

Return to [Summary Table](#)
**Table 4-1133. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6118h       |

**Figure 4-367. ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_CH2\_CFG0\_REG Name Register**

| 31                         | 30                  | 29                      | 28                | 27                     | 26               | 25 | 24 |
|----------------------------|---------------------|-------------------------|-------------------|------------------------|------------------|----|----|
| PRU1_ED_TX_FIFO_SWAP_BITS2 | PRU1_ED_SW_CLK_OUT2 | PRU1_ED_CLK_OUT_OVR_EN2 | PRU1_ED_RX_SNOOP2 | PRU1_ED_RX_FRAME_SIZE2 |                  |    |    |
| R/W                        | R/W                 | R/W                     | R                 | R/W                    |                  |    |    |
| 0h                         | 0h                  | 0h                      | 0h                | 0h                     |                  |    |    |
| 23                         | 22                  | 21                      | 20                | 19                     | 18               | 17 | 16 |
| PRU1_ED_RX_FRAME_SIZE2     |                     |                         |                   |                        |                  |    |    |
| R/W                        |                     |                         |                   |                        |                  |    |    |
| 0h                         |                     |                         |                   |                        |                  |    |    |
| 15                         | 14                  | 13                      | 12                | 11                     | 10               | 9  | 8  |
| PRU1_ED_TX_FRAME_SIZE2     |                     |                         |                   |                        | PRU1_ED_TX_WDLY2 |    |    |
| R/W                        |                     |                         |                   |                        | R/W              |    |    |
| 0h                         |                     |                         |                   |                        | 0h               |    |    |
| 7                          | 6                   | 5                       | 4                 | 3                      | 2                | 1  | 0  |
| PRU1_ED_TX_WDLY2           |                     |                         |                   |                        |                  |    |    |
| R/W                        |                     |                         |                   |                        |                  |    |    |
| 0h                         |                     |                         |                   |                        |                  |    |    |

**Table 4-1135. ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_CH2\_CFG0\_REG Register Field Descriptions**

| Bit   | Field                      | Type | Reset | Description |
|-------|----------------------------|------|-------|-------------|
| 31    | PRU1_ED_TX_FIFO_SWAP_BITS2 | R/W  | 0h    |             |
| 30    | PRU1_ED_SW_CLK_OUT2        | R/W  | 0h    |             |
| 29    | PRU1_ED_CLK_OUT_OVR_EN2    | R/W  | 0h    |             |
| 28    | PRU1_ED_RX_SNOOP2          | R    | 0h    |             |
| 27:16 | PRU1_ED_RX_FRAME_SIZE2     | R/W  | 0h    |             |
| 15:11 | PRU1_ED_TX_FRAME_SIZE2     | R/W  | 0h    |             |
| 10:0  | PRU1_ED_TX_WDLY2           | R/W  | 0h    |             |

#### 4.2.2.174 ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_CH2\_CFG1\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_CH2\_CFG1\_REG Register (Offset = 11Ch) [reset = 0h]

ED Register

Return to [Summary Table](#)
**Table 4-1136. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 611Ch       |

**Figure 4-368. ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_CH2\_CFG1\_REG Name Register**

|                            |    |    |    |    |    |    |    |
|----------------------------|----|----|----|----|----|----|----|
| 31                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PRU1_ED_RX_EN_COUNTER2     |    |    |    |    |    |    |    |
| R/W                        |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |
| 23                         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PRU1_ED_RX_EN_COUNTER2     |    |    |    |    |    |    |    |
| R/W                        |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |
| 15                         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PRU1_ED_TST_DELAY_COUNTER2 |    |    |    |    |    |    |    |
| R/W                        |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |
| 7                          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PRU1_ED_TST_DELAY_COUNTER2 |    |    |    |    |    |    |    |
| R/W                        |    |    |    |    |    |    |    |
| 0h                         |    |    |    |    |    |    |    |

**Table 4-1138. ICSSM\_PR1\_CFG\_SLV\_PRU1\_ED\_CH2\_CFG1\_REG Register Field Descriptions**

| Bit   | Field                      | Type | Reset | Description |
|-------|----------------------------|------|-------|-------------|
| 31:16 | PRU1_ED_RX_EN_COUNTER2     | R/W  | 0h    |             |
| 15:0  | PRU1_ED_TST_DELAY_COUNTER2 | R/W  | 0h    |             |

#### 4.2.2.175 ICSSM\_PR1\_CFG\_SLV\_RTU0\_POKE\_EN0\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_RTU0\_POKE\_EN0\_REG Register (Offset = 124h) [reset = 0h]

RTU PRU Poke Enable

Return to [Summary Table](#)

**Table 4-1139. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6124h       |

**Figure 4-369. ICSSM\_PR1\_CFG\_SLV\_RTU0\_POKE\_EN0\_REG Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1141. ICSSM\_PR1\_CFG\_SLV\_RTU0\_POKE\_EN0\_REG Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |

#### 4.2.2.176 ICSSM\_PR1\_CFG\_SLV\_RTU1\_POKE\_EN0\_REG Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_RTU1\_POKE\_EN0\_REG Register (Offset = 12Ch) [reset = 0h]

RTU PRU Poke Enable

Return to [Summary Table](#)

**Table 4-1142. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 612Ch       |

**Figure 4-370. ICSSM\_PR1\_CFG\_SLV\_RTU1\_POKE\_EN0\_REG Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1144. ICSSM\_PR1\_CFG\_SLV\_RTU1\_POKE\_EN0\_REG Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |



#### 4.2.2.177 ICSSM\_PR1\_CFG\_SLV\_PWM0 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PWM0 Register (Offset = 130h) [reset = 0h]

PWM0 Safety Config

Return to [Summary Table](#)

**Table 4-1145. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6130h       |

**Figure 4-371. ICSSM\_PR1\_CFG\_SLV\_PWM0 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1147. ICSSM\_PR1\_CFG\_SLV\_PWM0 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |

#### 4.2.2.178 ICSSM\_PR1\_CFG\_SLV\_PWM1 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PWM1 Register (Offset = 134h) [reset = 0h]

PWM1 Safety Config

Return to [Summary Table](#)

**Table 4-1148. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6134h       |

**Figure 4-372. ICSSM\_PR1\_CFG\_SLV\_PWM1 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1150. ICSSM\_PR1\_CFG\_SLV\_PWM1 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |

#### 4.2.2.179 ICSSM\_PR1\_CFG\_SLV\_PWM2 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PWM2 Register (Offset = 138h) [reset = 0h]

PWM2 Safety Config

Return to [Summary Table](#)

**Table 4-1151. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6138h       |

**Figure 4-373. ICSSM\_PR1\_CFG\_SLV\_PWM2 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1153. ICSSM\_PR1\_CFG\_SLV\_PWM2 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |

#### 4.2.2.180 ICSSM\_PR1\_CFG\_SLV\_PWM3 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PWM3 Register (Offset = 13Ch) [reset = 0h]

PWM3 Safety Config

Return to [Summary Table](#)

**Table 4-1154. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 613Ch       |

**Figure 4-374. ICSSM\_PR1\_CFG\_SLV\_PWM3 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1156. ICSSM\_PR1\_CFG\_SLV\_PWM3 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |

#### 4.2.2.181 ICSSM\_PR1\_CFG\_SLV\_PWM0\_0 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PWM0\_0 Register (Offset = 140h) [reset = 0h]

PWM0 State Config0

Return to [Summary Table](#)

**Table 4-1157. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6140h       |

**Figure 4-375. ICSSM\_PR1\_CFG\_SLV\_PWM0\_0 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1159. ICSSM\_PR1\_CFG\_SLV\_PWM0\_0 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |

#### 4.2.2.182 ICSSM\_PR1\_CFG\_SLV\_PWM0\_1 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PWM0\_1 Register (Offset = 144h) [reset = 0h]

PWM0 State Config1

Return to [Summary Table](#)

**Table 4-1160. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6144h       |

**Figure 4-376. ICSSM\_PR1\_CFG\_SLV\_PWM0\_1 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1162. ICSSM\_PR1\_CFG\_SLV\_PWM0\_1 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |

#### 4.2.2.183 ICSSM\_PR1\_CFG\_SLV\_PWM0\_2 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PWM0\_2 Register (Offset = 148h) [reset = 0h]

PWM0 State Config2

Return to [Summary Table](#)

**Table 4-1163. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6148h       |

**Figure 4-377. ICSSM\_PR1\_CFG\_SLV\_PWM0\_2 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1165. ICSSM\_PR1\_CFG\_SLV\_PWM0\_2 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |

#### 4.2.2.184 ICSSM\_PR1\_CFG\_SLV\_PWM1\_0 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PWM1\_0 Register (Offset = 14Ch) [reset = 0h]

PWM1 State Config0

Return to [Summary Table](#)

**Table 4-1166. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 614Ch       |

**Figure 4-378. ICSSM\_PR1\_CFG\_SLV\_PWM1\_0 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1168. ICSSM\_PR1\_CFG\_SLV\_PWM1\_0 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |



#### 4.2.2.185 ICSSM\_PR1\_CFG\_SLV\_PWM1\_1 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PWM1\_1 Register (Offset = 150h) [reset = 0h]

PWM1 State Config1

Return to [Summary Table](#)

**Table 4-1169. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6150h       |

**Figure 4-379. ICSSM\_PR1\_CFG\_SLV\_PWM1\_1 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1171. ICSSM\_PR1\_CFG\_SLV\_PWM1\_1 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |

#### 4.2.2.186 ICSSM\_PR1\_CFG\_SLV\_PWM1\_2 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PWM1\_2 Register (Offset = 154h) [reset = 0h]

PWM1 State Config2

Return to [Summary Table](#)

**Table 4-1172. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6154h       |

**Figure 4-380. ICSSM\_PR1\_CFG\_SLV\_PWM1\_2 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1174. ICSSM\_PR1\_CFG\_SLV\_PWM1\_2 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |

#### 4.2.2.187 ICSSM\_PR1\_CFG\_SLV\_PWM2\_0 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PWM2\_0 Register (Offset = 158h) [reset = 0h]

PWM2 State Config0

Return to [Summary Table](#)

**Table 4-1175. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6158h       |

**Figure 4-381. ICSSM\_PR1\_CFG\_SLV\_PWM2\_0 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1177. ICSSM\_PR1\_CFG\_SLV\_PWM2\_0 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |

#### 4.2.2.188 ICSSM\_PR1\_CFG\_SLV\_PWM2\_1 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PWM2\_1 Register (Offset = 15Ch) [reset = 0h]

PWM2 State Config1

Return to [Summary Table](#)

**Table 4-1178. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 615Ch       |

**Figure 4-382. ICSSM\_PR1\_CFG\_SLV\_PWM2\_1 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1180. ICSSM\_PR1\_CFG\_SLV\_PWM2\_1 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |

#### 4.2.2.189 ICSSM\_PR1\_CFG\_SLV\_PWM2\_2 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PWM2\_2 Register (Offset = 160h) [reset = 0h]

PWM2 State Config2

Return to [Summary Table](#)

**Table 4-1181. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6160h       |

**Figure 4-383. ICSSM\_PR1\_CFG\_SLV\_PWM2\_2 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1183. ICSSM\_PR1\_CFG\_SLV\_PWM2\_2 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |

#### 4.2.2.190 ICSSM\_PR1\_CFG\_SLV\_PWM3\_0 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PWM3\_0 Register (Offset = 164h) [reset = 0h]

PWM3 State Config0

Return to [Summary Table](#)

**Table 4-1184. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6164h       |

**Figure 4-384. ICSSM\_PR1\_CFG\_SLV\_PWM3\_0 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1186. ICSSM\_PR1\_CFG\_SLV\_PWM3\_0 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |

#### 4.2.2.191 ICSSM\_PR1\_CFG\_SLV\_PWM3\_1 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PWM3\_1 Register (Offset = 168h) [reset = 0h]

PWM3 State Config1

Return to [Summary Table](#)

**Table 4-1187. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6168h       |

**Figure 4-385. ICSSM\_PR1\_CFG\_SLV\_PWM3\_1 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1189. ICSSM\_PR1\_CFG\_SLV\_PWM3\_1 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |

#### 4.2.2.192 ICSSM\_PR1\_CFG\_SLV\_PWM3\_2 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PWM3\_2 Register (Offset = 16Ch) [reset = 0h]

PWM3 State Config2

Return to [Summary Table](#)

**Table 4-1190. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 616Ch       |

**Figure 4-386. ICSSM\_PR1\_CFG\_SLV\_PWM3\_2 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1192. ICSSM\_PR1\_CFG\_SLV\_PWM3\_2 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |



#### 4.2.2.193 ICSSM\_PR1\_CFG\_SLV\_SPIN\_LOCK0 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_SPIN\_LOCK0 Register (Offset = 170h) [reset = 0h]

Spin Lock

Return to [Summary Table](#)

**Table 4-1193. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6170h       |

**Figure 4-387. ICSSM\_PR1\_CFG\_SLV\_SPIN\_LOCK0 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1195. ICSSM\_PR1\_CFG\_SLV\_SPIN\_LOCK0 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |

#### 4.2.2.194 ICSSM\_PR1\_CFG\_SLV\_SPIN\_LOCK1 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_SPIN\_LOCK1 Register (Offset = 174h) [reset = 0h]

Spin Lock

Return to [Summary Table](#)

**Table 4-1196. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6174h       |

**Figure 4-388. ICSSM\_PR1\_CFG\_SLV\_SPIN\_LOCK1 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1198. ICSSM\_PR1\_CFG\_SLV\_SPIN\_LOCK1 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |

#### 4.2.2.195 ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_CFG0 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_CFG0 Register (Offset = 178h) [reset = 0h]

PA STATS PDSP0 Vector

Return to [Summary Table](#)

**Table 4-1199. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6178h       |

**Figure 4-389. ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_CFG0 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1201. ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_CFG0 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |

#### 4.2.2.196 ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_STAT0 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_STAT0 Register (Offset = 17Ch) [reset = 0h]

PA STATS PDSP0 Status

Return to [Summary Table](#)

**Table 4-1202. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 617Ch       |

**Figure 4-390. ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_STAT0 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1204. ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_STAT0 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |

#### 4.2.2.197 ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_CFG1 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_CFG1 Register (Offset = 180h) [reset = 0h]

PA STATS PDSP1 Vector

Return to [Summary Table](#)

**Table 4-1205. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6180h       |

**Figure 4-391. ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_CFG1 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1207. ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_CFG1 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |

#### 4.2.2.198 ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_STAT1 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_STAT1 Register (Offset = 184h) [reset = 0h]

PA STATS PDSP1 Status

Return to [Summary Table](#)

**Table 4-1208. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6184h       |

**Figure 4-392. ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_STAT1 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1210. ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_STAT1 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |

#### 4.2.2.199 ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_CFG2 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_CFG2 Register (Offset = 188h) [reset = 0h]

PA STATS PDSP2 Vector

Return to [Summary Table](#)

**Table 4-1211. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6188h       |

**Figure 4-393. ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_CFG2 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1213. ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_CFG2 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |

#### 4.2.2.200 ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_STAT2 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_STAT2 Register (Offset = 18Ch) [reset = 0h]

PA STATS PDSP2 Status

Return to [Summary Table](#)

**Table 4-1214. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 618Ch       |

**Figure 4-394. ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_STAT2 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1216. ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_STAT2 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |



#### 4.2.2.201 ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_CFG3 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_CFG3 Register (Offset = 190h) [reset = 0h]

PA STATS PDSP3 Vector

Return to [Summary Table](#)

**Table 4-1217. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6190h       |

**Figure 4-395. ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_CFG3 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1219. ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_CFG3 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |

#### 4.2.2.202 ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_STAT3 Register

##### 1 ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_STAT3 Register (Offset = 194h) [reset = 0h]

PA STATS PDSP3 Status

Return to [Summary Table](#)

**Table 4-1220. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 6194h       |

**Figure 4-396. ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_STAT3 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1222. ICSSM\_PR1\_CFG\_SLV\_PA\_STAT\_PDSP\_STAT3 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |

#### 4.2.2.203 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_RBR Register

##### 1 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_RBR Register (Offset = 0h) [reset = 0h]

Receiver Buffer Register (read only)

The UART receiver section consists of a receiver shift register (RSR) and a receiver buffer register (RBR). When the UART is in the FIFO mode, RBR is a 16-byte FIFO. Timing is supplied by the 16x receiver clock or 13x receiver clock by programming OSM\_SEL bit field of MDR register. Receiver section control is a function of the line control register (LCR).

RSR receives serial data from the UARTn\_RXD pin. Then RSR concatenates the data and moves it into RBR (or the receiver FIFO). In the non-FIFO mode, when a character is placed in RBR and the receiver data-ready interrupt is enabled (DR = 1 in IER), an interrupt is generated. This interrupt is cleared when the character is read from RBR. In the FIFO mode, the interrupt is generated when the FIFO is filled to the trigger level selected in the FIFO control register (FCR), and it is cleared when the FIFO contents drop below the trigger level.

Return to [Summary Table](#)

**Table 4-1223. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 8000h       |

**Figure 4-397. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_RBR Name Register**

|          |    |    |    |    |    |          |    |
|----------|----|----|----|----|----|----------|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25       | 24 |
| RESERVED |    |    |    |    |    |          |    |
| NONE     |    |    |    |    |    |          |    |
| 0h       |    |    |    |    |    |          |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17       | 16 |
| RESERVED |    |    |    |    |    | RESERVED |    |
| NONE     |    |    |    |    |    | W        |    |
| 0h       |    |    |    |    |    | 0h       |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9        | 8  |
| RESERVED |    |    |    |    |    |          |    |
| W        |    |    |    |    |    |          |    |
| 0h       |    |    |    |    |    |          |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1        | 0  |
| DATA     |    |    |    |    |    |          |    |
| R        |    |    |    |    |    |          |    |
| 0h       |    |    |    |    |    |          |    |

**Table 4-1225. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_RBR Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description   |
|-------|----------|------|-------|---------------|
| 31:18 | RESERVED | NONE | 0h    | Reserved      |
| 17:8  | RESERVED | W    | 0h    | Reserved      |
| 7:0   | DATA     | R    | 0h    | Received Data |

#### 4.2.2.204 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_IER Register

##### 1 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_IER Register (Offset = 4h) [reset = 0h]

The interrupt enable register (IER) is used to individually enable or disable each type of interrupt request that can be generated by the UART. Each interrupt request that is enabled in IER is forwarded to the CPU.

Return to [Summary Table](#)

**Table 4-1226. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 8004h       |

**Figure 4-398. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_IER Name Register**

|          |    |    |    |       |      |       |      |
|----------|----|----|----|-------|------|-------|------|
| 31       | 30 | 29 | 28 | 27    | 26   | 25    | 24   |
| RESERVED |    |    |    |       |      |       |      |
| NONE     |    |    |    |       |      |       |      |
| 0h       |    |    |    |       |      |       |      |
| 23       | 22 | 21 | 20 | 19    | 18   | 17    | 16   |
| RESERVED |    |    |    |       |      |       |      |
| NONE     |    |    |    |       |      |       |      |
| 0h       |    |    |    |       |      |       |      |
| 15       | 14 | 13 | 12 | 11    | 10   | 9     | 8    |
| RESERVED |    |    |    |       |      |       |      |
| NONE     |    |    |    |       |      |       |      |
| 0h       |    |    |    |       |      |       |      |
| 7        | 6  | 5  | 4  | 3     | 2    | 1     | 0    |
| RESERVED |    |    |    | EDSSI | ELSI | ETBEI | ERBI |
| NONE     |    |    |    | R/W   | R/W  | R/W   | R/W  |
| 0h       |    |    |    | 0h    | 0h   | 0h    | 0h   |

**Table 4-1228. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_IER Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                 |
|------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                    |
| 3    | EDSSI    | R/W  | 0h    | Enable for Modem Status Interrupt                                                                                                                                                                                                           |
| 2    | ELSI     | R/W  | 0h    | Enable for Receiver Line Status Interrupt<br>1h Received line status is enabled<br>0h Receiver line status interrupt is disabled.                                                                                                           |
| 1    | ETBEI    | R/W  | 0h    | Enable for Transmitter Holding Register Empty Interrupt<br>1h Transmitter holding register empty interrupt is enabled.<br>0h Transmitter holding register empty interrupt is disabled.                                                      |
| 0    | ERBI     | R/W  | 0h    | Enable for Receiver Data Available Interrupt<br>1h Receiver data available interrupt and character timeout indication interrupt is enabled.<br>0h Receiver data available interrupt and character timeout indication interrupt is disabled. |

#### 4.2.2.205 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_IIR Register

##### 1 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_IIR Register (Offset = 8h) [reset = 1h]

The interrupt identification register (IIR) is a read-only register at the same address as the FIFO control register (FCR), which is a write-only register. When an interrupt is generated and enabled in the interrupt enable register (IER), IIR indicates that an interrupt is pending in the IPEND bit and encodes the type of interrupt in the INTID bits. Reading IIR clears any THR empty (THRE) interrupts that are pending.

Return to [Summary Table](#)

**Table 4-1229. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 8008h       |

**Figure 4-399. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_IIR Name Register**

|          |          |          |          |          |          |          |          |
|----------|----------|----------|----------|----------|----------|----------|----------|
| 31       | 30       | 29       | 28       | 27       | 26       | 25       | 24       |
| RESERVED |          |          |          |          |          |          |          |
| NONE     |          |          |          |          |          |          |          |
| 0h       |          |          |          |          |          |          |          |
| 23       | 22       | 21       | 20       | 19       | 18       | 17       | 16       |
| RESERVED |          |          |          |          |          |          |          |
| NONE     |          |          |          |          |          |          |          |
| 0h       |          |          |          |          |          |          |          |
| 15       | 14       | 13       | 12       | 11       | 10       | 9        | 8        |
| RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED |
| W        | NONE     | W        | W        | W        | W        | W        | W        |
| 0h       | 0h       | 0h       | 0h       | 0h       | 0h       | 0h       | 0h       |
| 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
| FIFOEN   | RESERVED | INTID    |          |          |          | IPEND    |          |
| R        | NONE     | R        |          |          |          | R        |          |
| 0h       | 0h       | 0h       |          |          |          | 1h       |          |

**Table 4-1231. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_IIR Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                             |
|-------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED | NONE | 0h    | Reserved                                                                                                                                |
| 15:14 | RESERVED | W    | 0h    | Reserved                                                                                                                                |
| 13:12 | RESERVED | NONE | 0h    | Reserved                                                                                                                                |
| 11    | RESERVED | W    | 0h    | Reserved                                                                                                                                |
| 10    | RESERVED | W    | 0h    | Reserved                                                                                                                                |
| 9     | RESERVED | W    | 0h    | Reserved                                                                                                                                |
| 8     | RESERVED | W    | 0h    | Reserved                                                                                                                                |
| 7:6   | FIFOEN   | R    | 0h    | FIFOs enabled<br>3h FIFOs are enabled. FIFOEN bit in the FIFO control register (FCR) is set to 1.<br>1h-2h Reserved<br>0h Non-FIFO mode |
| 5:4   | RESERVED | NONE | 0h    | Reserved                                                                                                                                |

**Table 4-1231. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_IIR Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                          |
|-----|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:1 | INTID | R    | 0h    | <p>Interrupt Type</p> <p>7h Reserved</p> <p>6h Character timeout indication (priority 2)</p> <p>4h-5h Reserved</p> <p>3h Receiver line status (priority 1, highest)</p> <p>2h Receiver data available (priority 2)</p> <p>1h Transmitter holding register empty (priority 3)</p> <p>0h Reserved</p>                                  |
| 0   | IPEND | R    | 1h    | <p>Interrupt pending.</p> <p>When any UART interrupt is generated and is enabled in IER, IPEND is forced to 0. IPEND remains 0 until all pending interrupts are cleared or until a hardware reset occurs. If no interrupts are enabled, IPEND is never forced to 0.</p> <p>1h No interrupts pending</p> <p>0h Interrupts pending</p> |

#### 4.2.2.206 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_LCR Register

##### 1 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_LCR Register (Offset = Ch) [reset = 0h]

###### Line Control Register (LCR)

The system programmer controls the format of the asynchronous data communication exchange by using LCR. In addition, the programmer can retrieve, inspect, and modify the content of LCR; this eliminates the need for separate storage of the line characteristics in system memory.

Return to [Summary Table](#)

**Table 4-1232. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 800Ch       |

**Figure 4-400. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_LCR Name Register**

|          |     |     |     |     |     |      |     |
|----------|-----|-----|-----|-----|-----|------|-----|
| 31       | 30  | 29  | 28  | 27  | 26  | 25   | 24  |
| RESERVED |     |     |     |     |     |      |     |
| NONE     |     |     |     |     |     |      |     |
| 0h       |     |     |     |     |     |      |     |
| 23       | 22  | 21  | 20  | 19  | 18  | 17   | 16  |
| RESERVED |     |     |     |     |     |      |     |
| NONE     |     |     |     |     |     |      |     |
| 0h       |     |     |     |     |     |      |     |
| 15       | 14  | 13  | 12  | 11  | 10  | 9    | 8   |
| RESERVED |     |     |     |     |     |      |     |
| NONE     |     |     |     |     |     |      |     |
| 0h       |     |     |     |     |     |      |     |
| 7        | 6   | 5   | 4   | 3   | 2   | 1    | 0   |
| DLAB     | BC  | SP  | EPS | PEN | STB | WLS1 | WLS |
| R/W      | R/W | R/W | R/W | R/W | R/W | R/W  | R/W |
| 0h       | 0h  | 0h  | 0h  | 0h  | 0h  | 0h   | 0h  |

**Table 4-1234. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_LCR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 7    | DLAB     | R/W  | 0h    | <p>Divisor latch access bit. The divisor latch registers (DLL and DLH) can be accessed at dedicated addresses or at addresses shared by RBR, THR, and IER. Using the shared addresses requires toggling DLAB to change which registers are selected. If you use the dedicated addresses, you can keep DLAB = 0.</p> <p>1 Allows access to the divisor latches of the baud generator during a read or write operation (DLL and DLH). At the address shared by RBR, THR, and DLL, the CPU can read from and write to DLL. At the address shared by IER and DLH, the CPU can read from and write to DLH.</p> <p>0 Allows access to the receiver buffer register (RBR), the transmitter holding register (THR), and the interrupt enable register (IER) selected. At the address shared by RBR, THR, and DLL, the CPU can read from RBR and write to THR. At the address shared by IER and DLH, the CPU can read from and write to IER.</p> |

**Table 4-1234. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_LCR Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6   | BC    | R/W  | 0h    | Break Control<br>1 Break condition is transmitted to the receiving UART. A break condition is a condition where the UARTn_TXD signal is forced to the spacing (cleared) state. Break condition is disabled<br>0                                                                                                                                                                                                                                      |
| 5   | SP    | R/W  | 0h    | Stick parity. The SP bit works in conjunction with the EPS and PEN bits.<br>1 Stick parity is enabled -when odd parity is selected (EPS = 0), the PARITY bit is transmitted and checked as set. -when even parity is selected (EPS = 1), the PARITY bit is transmitted and checked as cleared. Stick parity is disabled<br>0                                                                                                                         |
| 4   | EPS   | R/W  | 0h    | Even parity select. Selects the parity when parity is enabled (PEN = 1). The EPS bit works in conjunction with the SP and PEN bits.<br>1 Even parity is selected (an even number of logic 1s is transmitted or checked in the data and PARITY bits).<br>0 Odd parity is selected (an odd number of logic 1s is transmitted or checked in the data and PARITY bits).                                                                                  |
| 3   | PEN   | R/W  | 0h    | Parity enable. The PEN bit works in conjunction with the SP and EPS bits.<br>1 Parity bit is generated in transmitted data and is checked in received data between the last data word bit and the first STOP bit. No PARITY bit is transmitted or checked.<br>0                                                                                                                                                                                      |
| 2   | STB   | R/W  | 0h    | Number of STOP bits generated. STB specifies 1, 1.5, or 2 STOP bits in each transmitted character. When STB = 1, the WLS bit determines the number of STOP bits. The receiver clocks only the first STOP bit, regardless of the number of STOP bits selected.<br>1 WLS bit determines the number of STOP bits:<br>-when WLS = 0, 1.5 STOP bits are generated.<br>-when WLS = 1h, 2h, or 3h, 2 STOP bits are generated.<br>0 1 STOP bit is generated. |
| 1   | WLS1  | R/W  | 0h    | Word Length Select Bit 1                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 0   | WLS   | R/W  | 0h    | Word length select.<br>Number of bits in each transmitted or received serial character.<br>When STB = 1, the WLS bit determines the number of STOP bits.<br>3 8 bits<br>2 7 bits<br>1 6 bits<br>0 5 bits                                                                                                                                                                                                                                             |



#### 4.2.2.207 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_MCR Register

##### 1 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_MCR Register (Offset = 10h) [reset = 0h]

Modem Control Register (MCR)

The modem control register provides the ability to enable/disable the autoflow functions, and enable/disable the loopback function for diagnostic purposes.

Return to [Summary Table](#)

**Table 4-1235. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 8010h       |

**Figure 4-401. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_MCR Name Register**

|          |     |      |      |      |     |          |    |
|----------|-----|------|------|------|-----|----------|----|
| 31       | 30  | 29   | 28   | 27   | 26  | 25       | 24 |
| RESERVED |     |      |      |      |     |          |    |
| NONE     |     |      |      |      |     |          |    |
| 0h       |     |      |      |      |     |          |    |
| 23       | 22  | 21   | 20   | 19   | 18  | 17       | 16 |
| RESERVED |     |      |      |      |     |          |    |
| NONE     |     |      |      |      |     |          |    |
| 0h       |     |      |      |      |     |          |    |
| 15       | 14  | 13   | 12   | 11   | 10  | 9        | 8  |
| RESERVED |     |      |      |      |     |          |    |
| NONE     |     |      |      |      |     |          |    |
| 0h       |     |      |      |      |     |          |    |
| 7        | 6   | 5    | 4    | 3    | 2   | 1        | 0  |
| RESERVED | AFE | LOOP | OUT2 | OUT1 | RTS | RESERVED |    |
| NONE     | R/W | R/W  | R/W  | R/W  | R/W | R/W      |    |
| 0h       | 0h  | 0h   | 0h   | 0h   | 0h  | 0h       |    |

**Table 4-1237. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_MCR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|------|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:6 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 5    | AFE      | R/W  | 0h    | Autoflow control enable.<br>Autoflow control allows the UARTn_RTS and UARTn_CTS signals to provide handshaking between UARTs during data transfer. When AFE = 1, the RTS bit determines the autoflow control enabled. Note that all UARTs do not support this feature, see your device-specific data manual for supported features. If this feature is not available, this bit is reserved and should be cleared to 0.<br><br>1      Autoflow control is enabled: -when RTS = 0, UARTnCTS is only enabled -when RTS = 1, UARTn_RTS and UARTn_CTS are enabled<br>0      Autoflow control is disabled. |
| 4    | LOOP     | R/W  | 0h    | Loop back mode enable. LOOP is used for the diagnostic testing using the loop back feature.<br><br>1      Loop back mode is enabled. when LOOP is set, the following occur: -The UARTn_TXD signal is set high. -The UARTn_RXD pin is disconnected -The output of the transmitter shift register (TSR) is lopped back in to the receiver shift register (RSR) input.<br>0      Loop back mode is disabled.                                                                                                                                                                                            |
| 3    | OUT2     | R/W  | 0h    | Out2 Bit                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

**Table 4-1237. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_MCR Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                  |
|-----|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | OUT1     | R/W  | 0h    | Out1 Bit                                                                                                                                                                                                                                                                                                                                                                                                     |
| 1   | RTS      | R/W  | 0h    | <p>RTS control. When AFE = 1, the RTS bit determines the autoflow control enabled. Note that all UARTs do not support this feature, see your device-specific data manual for supported features. If this feature is not available, this bit is reserved and should be cleared to 0.</p> <p>1        UARTn_RTS and UARTn_CTS are enabled.<br/> 0        UARTn_RTS is disabled, UARTn_CTS is only enabled.</p> |
| 0   | RESERVED | R/W  | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                     |

#### 4.2.2.208 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_LSR Register

##### 1 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_LSR Register (Offset = 14h) [reset = 60h]

Line Status Register (LSR)

LSR provides information to the CPU concerning the status of data transfers. LSR is intended for read operations only; do not write to this register. Bits 1 through 4 record the error conditions that produce a receiver line status interrupt.

Return to [Summary Table](#)

**Table 4-1238. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 8014h       |

**Figure 4-402. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_LSR Name Register**

|          |      |      |    |    |    |    |    |
|----------|------|------|----|----|----|----|----|
| 31       | 30   | 29   | 28 | 27 | 26 | 25 | 24 |
| RESERVED |      |      |    |    |    |    |    |
| NONE     |      |      |    |    |    |    |    |
| 0h       |      |      |    |    |    |    |    |
| 23       | 22   | 21   | 20 | 19 | 18 | 17 | 16 |
| RESERVED |      |      |    |    |    |    |    |
| NONE     |      |      |    |    |    |    |    |
| 0h       |      |      |    |    |    |    |    |
| 15       | 14   | 13   | 12 | 11 | 10 | 9  | 8  |
| RESERVED |      |      |    |    |    |    |    |
| NONE     |      |      |    |    |    |    |    |
| 0h       |      |      |    |    |    |    |    |
| 7        | 6    | 5    | 4  | 3  | 2  | 1  | 0  |
| RXFIFOE  | TEMT | THRE | BI | FE | PE | OE | DR |
| R        | R    | R    | R  | R  | R  | R  | R  |
| 0h       | 1h   | 1h   | 0h | 0h | 0h | 0h | 0h |

**Table 4-1240. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_LSR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|------|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 7    | RXFIFOE  | R    | 0h    | Receiver FIFO error.<br>In non-FIFO mode:<br>0 = There has been no error, or RXFIFOE was cleared because the CPU read the erroneous character from the receiver buffer register (RBR).<br>1 = There is a parity error, framing error, or break indicator in the receiver buffer register (RBR).<br>In FIFO mode:<br>0 = There has been no error, or RXFIFOE was cleared because the CPU read the erroneous character from the receiver FIFO and there are no more errors in the receiver FIFO.<br>1 = At least one parity error, framing error, or break indicator in the receiver FIFO. |

**Table 4-1240. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_LSR Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-----|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6   | TEMT  | R    | 1h    | Transmitter empty (TEMT) indicator.<br>In non-FIFO mode:<br>0 = Either the transmitter holding register (THR) or the transmitter shift register (TSR) contains a data character.<br>1 = Both the transmitter holding register (THR) and the transmitter shift register (TSR) are empty.<br>In FIFO mode:<br>0 = Either the transmitter FIFO or the transmitter shift register (TSR) contains a data character.<br>1 = Both the transmitter FIFO and the transmitter shift register (TSR) are empty.                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 5   | THRE  | R    | 1h    | Transmitter holding register empty (THRE) indicator.<br>If the THRE bit is set and the corresponding interrupt enable bit is set (ETBEI = 1 in IER), an interrupt request is generated.<br>In non-FIFO mode:<br>0 = Transmitter holding register (THR) is not empty. THR has been loaded by the CPU.<br>1 = Transmitter holding register (THR) is empty (ready to accept a new character). The content of THR has been transferred to the transmitter shift register (TSR).<br>In FIFO mode:<br>0 = Transmitter FIFO is not empty. At least one character has been written to the transmitter FIFO. You can write to the transmitter FIFO if it is not full.<br>1 = Transmitter FIFO is empty. The last character in the FIFO has been transferred to the transmitter shift register (TSR).                                                                                                                                                                                 |
| 4   | BI    | R    | 0h    | Break indicator.<br>The BI bit is set whenever the receive data input (UARTn_RXD) was held low for longer than a full-word transmission time. A full-word transmission time is defined as the total time to transmit the START, data, PARITY, and STOP bits. If the BI bit is set and the corresponding interrupt enable bit is set (ELSI = 1 in IER), an interrupt request is generated.<br>In non-FIFO mode:<br>0 = No break has been detected, or the BI bit was cleared because the CPU read the erroneous character from the receiver buffer register (RBR).<br>1 = A break has been detected with the character in the receiver buffer register (RBR).<br>In FIFO mode:<br>0 = No break has been detected, or the BI bit was cleared because the CPU read the erroneous character from the receiver FIFO and the next character to be read from the FIFO has no break indicator.<br>1 = A break has been detected with the character at the top of the receiver FIFO. |

**Table 4-1240. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_LSR Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-----|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3   | FE    | R    | 0h    | <p>Framing error (FE) indicator.</p> <p>A framing error occurs when the received character does not have a valid STOP bit. In response to a framing error, the UART sets the FE bit and waits until the signal on the RX pin goes high. Once the RX signal goes high, the receiver is ready to detect a new START bit and receive new data. If the FE bit is set and the corresponding interrupt enable bit is set (ELSI = 1 in IER), an interrupt request is generated.</p> <p>In non-FIFO mode:</p> <p>0 = No framing error has been detected, or the FE bit was cleared because the CPU read the erroneous data from the receiver buffer register (RBR).</p> <p>1 = A framing error has been detected with the character in the receiver buffer register (RBR).</p> <p>In FIFO mode:</p> <p>0 = No framing error has been detected, or the FE bit was cleared because the CPU read the erroneous data from the receiver FIFO and the next character to be read from the FIFO has no framing error.</p> <p>1 = A framing error has been detected with the character at the top of the receiver FIFO.</p>                                                                                            |
| 2   | PE    | R    | 0h    | <p>Parity error (PE) indicator. A parity error occurs when the parity of the received character does not match the parity selected with the EPS bit in the line control register (LCR). If the PE bit is set and the corresponding interrupt enable bit is set (ELSI = 1 in IER), an interrupt request is generated.</p> <p>In non-FIFO mode:</p> <p>0 = No parity error has been detected, or the PE bit was cleared because the CPU read the erroneous data from the receiver buffer register (RBR).</p> <p>1 = A parity error has been detected with the character in the receiver buffer register (RBR).</p> <p>In FIFO mode:</p> <p>0 = No parity error has been detected, or the PE bit was cleared because the CPU read the erroneous data from the receiver FIFO and the next character to be read from the FIFO has no parity error.</p> <p>1 = A parity error has been detected with the character at the top of the receiver FIFO.</p>                                                                                                                                                                                                                                                     |
| 1   | OE    | R    | 0h    | <p>Overrun error (OE) indicator. An overrun error in the non-FIFO mode is different from an overrun error in the FIFO mode. If the OE bit is set and the corresponding interrupt enable bit is set (ELSI = 1 in IER), an interrupt request is generated.</p> <p>In non-FIFO mode:</p> <p>0 = No overrun error has been detected, or the OE bit was cleared because the CPU read the content of the line status register (LSR).</p> <p>1 = Overrun error has been detected. Before the character in the receiver buffer register (RBR) could be read, it was overwritten by the next character arriving in RBR.</p> <p>In FIFO mode:</p> <p>0 = No overrun error has been detected, or the OE bit was cleared because the CPU read the content of the line status register (LSR).</p> <p>1 = Overrun error has been detected. If data continues to fill the FIFO beyond the trigger level, an overrun error occurs only after the FIFO is full and the next character has been completely received in the shift register. An overrun error is indicated to the CPU as soon as it happens. The new character overwrites the character in the shift register, but it is not transferred to the FIFO.</p> |

**Table 4-1240. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_LSR Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | DR    | R    | 0h    | <p>Data-ready (DR) indicator for the receiver. If the DR bit is set and the corresponding interrupt enable bit is set (ERBI = 1 in IER), an interrupt request is generated.</p> <p>In non-FIFO mode:</p> <p>0 = Data is not ready, or the DR bit was cleared because the character was read from the receiver buffer register (RBR).</p> <p>1 = Data is ready. A complete incoming character has been received and transferred into the receiver buffer register (RBR).</p> <p>In FIFO mode:</p> <p>0 = Data is not ready, or the DR bit was cleared because all of the characters in the receiver FIFO have been read.</p> <p>1 = Data is ready. There is at least one unread character in the receiver FIFO. If the FIFO is empty, the DR bit is set as soon as a complete incoming character has been received and transferred into the FIFO. The DR bit remains set until the FIFO is empty again.</p> |

#### 4.2.2.209 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_MSR Register

##### 1 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_MSR Register (Offset = 18h) [reset = 0h]

Modem Status Register (MSR)

MSR provides information to the CPU concerning the status of modem control signals. MSR is intended for read operations only; do not write to this register.

Return to [Summary Table](#)

**Table 4-1241. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 8018h       |

**Figure 4-403. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_MSR Name Register**

|          |    |     |     |     |      |      |      |
|----------|----|-----|-----|-----|------|------|------|
| 31       | 30 | 29  | 28  | 27  | 26   | 25   | 24   |
| RESERVED |    |     |     |     |      |      |      |
| NONE     |    |     |     |     |      |      |      |
| 0h       |    |     |     |     |      |      |      |
| 23       | 22 | 21  | 20  | 19  | 18   | 17   | 16   |
| RESERVED |    |     |     |     |      |      |      |
| NONE     |    |     |     |     |      |      |      |
| 0h       |    |     |     |     |      |      |      |
| 15       | 14 | 13  | 12  | 11  | 10   | 9    | 8    |
| RESERVED |    |     |     |     |      |      |      |
| NONE     |    |     |     |     |      |      |      |
| 0h       |    |     |     |     |      |      |      |
| 7        | 6  | 5   | 4   | 3   | 2    | 1    | 0    |
| CD       | RI | DSR | CTS | DCD | TERI | DDSR | DCTS |
| R        | R  | R   | R   | R   | R    | R    | R    |
| 0h       | 0h | 0h  | 0h  | 0h  | 0h   | 0h   | 0h   |

**Table 4-1243. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_MSR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                   |
|------|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                      |
| 7    | CD       | R    | 0h    | Complement of the Carrier Detect input. When the UART is in the diagnostic test mode (loopback mode MCR[4] = 1), this bit is equal to the MCR bit 3 (OUT2).                                                                   |
| 6    | RI       | R    | 0h    | Complement of the Ring Indicator input. When the UART is in the diagnostic test mode (loopback mode MCR[4] = 1), this bit is equal to the MCR bit 2 (OUT1).                                                                   |
| 5    | DSR      | R    | 0h    | Complement of the Data Set Ready input. When the UART is in the diagnostic test mode (loopback mode MCR[4] = 1), this bit is equal to the MCR bit 0 (DTR).                                                                    |
| 4    | CTS      | R    | 0h    | Complement of the Clear To Send input. When the UART is in the diagnostic test mode (loopback mode MCR[4] = 1), this bit is equal to the MCR bit 1 (RTS).                                                                     |
| 3    | DCD      | R    | 0h    | Change in DCD indicator bit. DCD indicates that the DCD input has changed state since the last time it was read by the CPU. When DCD is set and the modem status interrupt is enabled, a modem status interrupt is generated. |
| 2    | TERI     | R    | 0h    | Trailing edge of RI (TERI) indicator bit. TERI indicates that the RI input has changed from a low to a high. When TERI is set and the modem status interrupt is enabled, a modem status interrupt is generated.               |

**Table 4-1243. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_MSR Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                    |
|-----|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | DDSR  | R    | 0h    | Change in DSR indicator bit. DDSR indicates that the DSR input has changed state since the last time it was read by the CPU. When DDSR is set and the modem status interrupt is enabled, a modem status interrupt is generated.                                                                                                |
| 0   | DCTS  | R    | 0h    | Change in CTS indicator bit. DCTS indicates that the CTS input has changed state since the last time it was read by the CPU. When DCTS is set (autoflow control is not enabled and the modem status interrupt is enabled), a modem status interrupt is generated. When autoflow control is enabled, no interrupt is generated. |



#### 4.2.2.210 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_SCR Register

##### 1 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_SCR Register (Offset = 1Ch) [reset = 0h]

Scratch Pad Register (SCR)

SCR is intended for programmer's use as a scratch pad. It temporarily holds the programmer's data without affecting UART operation.

Return to [Summary Table](#)

**Table 4-1244. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 801Ch       |

**Figure 4-404. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_SCR Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DATA     |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1246. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_SCR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                         |
|------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                            |
| 7:0  | DATA     | R/W  | 0h    | Scratch Register Bits<br>These bits are intended for the programmer's use as a scratch pad in the sense that it temporarily holds the programmer's data without affecting any other UART operation. |

#### 4.2.2.211 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_DLL Register

##### 1 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_DLL Register (Offset = 20h) [reset = 0h]

Divisor LSB Latch.

Return to [Summary Table](#)

**Table 4-1247. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 8020h       |

**Figure 4-405. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_DLL Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DLL      |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1249. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_DLL Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                            |
|------|----------|------|-------|------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED | NONE | 0h    | Reserved                                                                                                               |
| 7:0  | DLL      | R/W  | 0h    | The 8 least-significant bits (LSBs) of the 16-bit divisor for generation of the baud clock in the baud rate generator. |

#### 4.2.2.212 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_DLH Register

##### 1 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_DLH Register (Offset = 24h) [reset = 0h]

Divisor MSB Latch.

Return to [Summary Table](#)

**Table 4-1250. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 8024h       |

**Figure 4-406. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_DLH Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DLH      |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1252. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_DLH Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                           |
|------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED | NONE | 0h    | Reserved                                                                                                              |
| 7:0  | DLH      | R/W  | 0h    | The 8 most-significant bits (MSBs) of the 16-bit divisor for generation of the baud clock in the baud rate generator. |

#### 4.2.2.213 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_REVID1 Register

##### 1 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_REVID1 Register (Offset = 28h) [reset = 44141102h]

Revision Identification Register 1

Return to [Summary Table](#)

**Table 4-1253. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 8028h       |

**Figure 4-407. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_REVID1 Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| REVID1    |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 11020002h |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| REVID1    |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 11020002h |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| REVID1    |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 11020002h |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| REVID1    |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 11020002h |    |    |    |    |    |    |    |

**Table 4-1255. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_REVID1 Register Field Descriptions**

| Bit  | Field  | Type | Reset     | Description                      |
|------|--------|------|-----------|----------------------------------|
| 31:0 | REVID1 | R    | 11020002h | Peripheral Identification Number |

#### 4.2.2.214 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_PWREMU\_MGMT Register

##### 1 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_PWREMU\_MGMT Register (Offset = 30h) [reset = 2h]

UART PowerManagement and Emulation Register.

Return to [Summary Table](#)

**Table 4-1256. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 8030h       |

**Figure 4-408. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_PWREMU\_MGMT Name Register**

|          |       |       |          |    |    |          |      |
|----------|-------|-------|----------|----|----|----------|------|
| 31       | 30    | 29    | 28       | 27 | 26 | 25       | 24   |
| RESERVED |       |       |          |    |    |          |      |
| NONE     |       |       |          |    |    |          |      |
| 0h       |       |       |          |    |    |          |      |
| 23       | 22    | 21    | 20       | 19 | 18 | 17       | 16   |
| RESERVED |       |       |          |    |    |          |      |
| NONE     |       |       |          |    |    |          |      |
| 0h       |       |       |          |    |    |          |      |
| 15       | 14    | 13    | 12       | 11 | 10 | 9        | 8    |
| RESERVED | UTRST | URRST | RESERVED |    |    |          |      |
| R/W      | R/W   | R/W   | NONE     |    |    |          |      |
| 0h       | 0h    | 0h    | 0h       |    |    |          |      |
| 7        | 6     | 5     | 4        | 3  | 2  | 1        | 0    |
| RESERVED |       |       |          |    |    | RESERVED | FREE |
| NONE     |       |       |          |    |    | R        | R/W  |
| 0h       |       |       |          |    |    | 1h       | 0h   |

**Table 4-1258. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_PWREMU\_MGMT Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 15    | RESERVED | R/W  | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 14    | UTRST    | R/W  | 0h    | UART transmitter reset. Resets and enables the transmitter.<br>1 Transmitter is enabled.<br>0 Transmitter is disabled and in reset state.                                                                                                                                                                                                                                                                                                                                        |
| 13    | URRST    | R/W  | 0h    | UART receiver reset. Resets and enables the receiver.<br>1 Receiver is enabled.<br>0 Receiver is disabled and in reset state.                                                                                                                                                                                                                                                                                                                                                    |
| 12:2  | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 1     | RESERVED | R    | 1h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 0     | FREE     | R/W  | 0h    | Free-running enable mode bit. This bit determines the emulation mode functionality of the UART. When halted, the UART can handle register read/write requests, but does not generate any transmission/reception, interrupts or events.<br>1 Free-running mode is enabled; UART continues to run normally.<br>0 If a transmission is not in progress, the UART halts immediately. If a transmission is in progress, the UART halts after completion of the one-word transmission. |

#### 4.2.2.215 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_MDR Register

##### 1 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_MDR Register (Offset = 34h) [reset = 0h]

UART Mode Definition Register.

Return to [Summary Table](#)

**Table 4-1259. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 8034h       |

**Figure 4-409. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_MDR Name Register**

|          |    |    |    |    |    |    |         |
|----------|----|----|----|----|----|----|---------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24      |
| RESERVED |    |    |    |    |    |    |         |
| NONE     |    |    |    |    |    |    |         |
| 0h       |    |    |    |    |    |    |         |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16      |
| RESERVED |    |    |    |    |    |    |         |
| NONE     |    |    |    |    |    |    |         |
| 0h       |    |    |    |    |    |    |         |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8       |
| RESERVED |    |    |    |    |    |    |         |
| NONE     |    |    |    |    |    |    |         |
| 0h       |    |    |    |    |    |    |         |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0       |
| RESERVED |    |    |    |    |    |    | OSM_SEL |
| NONE     |    |    |    |    |    |    | R/W     |
| 0h       |    |    |    |    |    |    | 0h      |

**Table 4-1261. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_MDR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                             |
|------|----------|------|-------|-------------------------------------------------------------------------|
| 31:1 | RESERVED | NONE | 0h    | Reserved                                                                |
| 0    | OSM_SEL  | R/W  | 0h    | Over-Sampling Mode Select<br>1 13x over-sampling<br>0 16x over-sampling |

#### 4.2.2.216 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_THR Register

##### 1 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_THR Register (Offset = 0h) [reset = 0h]

The transmitter holding register (THR) (write only)

The UART transmitter section consists of a transmitter hold register (THR) and a transmitter shift register (TSR). When the UART is in the FIFO mode, THR is a 16-byte FIFO. Transmitter section control is a function of the line control register (LCR).

THR receives data from the internal data bus and when TSR is idle, the UART moves the data from THR to TSR. The UART serializes the data in TSR and transmits the data on the TX pin. In the non-FIFO mode, if THR is empty and the THR empty (THRE) interrupt is enabled (ETBEI = 1 in IER), an interrupt is generated. This interrupt is cleared when a character is loaded into THR or the interrupt identification register (IIR) is read. In the FIFO mode, the interrupt is generated when the transmitter FIFO is empty, and it is cleared when at least one byte is loaded into the FIFO or IIR is read.

Return to [Summary Table](#)

**Table 4-1262. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 8000h       |

**Figure 4-410. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_THR Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DATA     |    |    |    |    |    |    |    |
| W        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1264. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_THR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description      |
|------|----------|------|-------|------------------|
| 31:8 | RESERVED | NONE | 0h    | Reserved         |
| 7:0  | DATA     | W    | 0h    | Data to transmit |

#### 4.2.2.217 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_FCR Register

##### 1 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_FCR Register (Offset = 8h) [reset = 0h]

FIFO Control Register (write only)

The FIFO control register (FCR) is a write-only register at the same address as the interrupt identification register (IIR), which is a read-only register.

Return to [Summary Table](#)

**Table 4-1265. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 8008h       |

**Figure 4-411. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_FCR Name Register**

|          |          |    |    |          |       |       |        |
|----------|----------|----|----|----------|-------|-------|--------|
| 31       | 30       | 29 | 28 | 27       | 26    | 25    | 24     |
| RESERVED |          |    |    |          |       |       |        |
| NONE     |          |    |    |          |       |       |        |
| 0h       |          |    |    |          |       |       |        |
| 23       | 22       | 21 | 20 | 19       | 18    | 17    | 16     |
| RESERVED |          |    |    |          |       |       |        |
| NONE     |          |    |    |          |       |       |        |
| 0h       |          |    |    |          |       |       |        |
| 15       | 14       | 13 | 12 | 11       | 10    | 9     | 8      |
| RESERVED |          |    |    |          |       |       |        |
| NONE     |          |    |    |          |       |       |        |
| 0h       |          |    |    |          |       |       |        |
| 7        | 6        | 5  | 4  | 3        | 2     | 1     | 0      |
| RXFITL   | RESERVED |    |    | DMAMODE1 | TXCLR | RXCLR | FIFOEN |
| W        | NONE     |    |    | W        | W     | W     | W      |
| 0h       | 0h       |    |    | 1h       | 0h    | 0h    | 0h     |

**Table 4-1267. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_FCR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                          |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                             |
| 7:6  | RXFITL   | W    | 0h    | Receiver FIFO trigger level.<br>RXFITL sets the trigger level for the receiver FIFO.<br>When the trigger level is reached, a receiver data-ready interrupt is generated (if the interrupt request is enabled).<br>Once the FIFO drops below the trigger level, the interrupt is cleared.<br><br>3h     14 bytes<br>2h     8 bytes<br>1h     4 bytes<br>0h     1 byte |
| 5:4  | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                             |
| 3    | DMAMODE1 | W    | 1h    | DMA MODE1 enable if FIFOs are enabled.<br>Always write 1 to DMAMODE1.<br>After a hardware reset, change DMAMODE1 from 0 to 1.<br>DMAMODE1 = 1 is a requirement for proper communication between the UART and the EDMA controller.<br><br>1h     DMA MODE 1 is enabled<br>0h     DMA MODE 1 is disabled                                                               |



**Table 4-1267. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_FCR Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                       |
|-----|--------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | TXCLR  | W    | 0h    | Transmitter FIFO clear. Write a 1 to TXCLR to clear the bit.<br><br>1h Clears transmitter FIFO and resets the transmitter FIFO counter. The shift register is not cleared.<br>0h No effect                                                                                                                                                                        |
| 1   | RXCLR  | W    | 0h    | Receiver FIFO clear. Write a 1 to RXCLR to clear the bit.<br><br>1h Clears receiver FIFO and resets the receiver FIFO counter. The shift register is not cleared.<br>0h No effect                                                                                                                                                                                 |
| 0   | FIFOEN | W    | 0h    | Transmitter and receiver FIFOs mode enable. FIFOEN must be set before other FCR bits are written to or the FCR bits are not programmed. Clearing this bit clears the FIFO counters.<br><br>1h FIFO mode. The transmitter and receiver FIFOs are enabled.<br>0h Non-FIFO mode. The transmitter and receiver FIFOs are disabled, and the FIFO pointers are cleared. |

#### 4.2.2.218 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_REVID2 Register

##### 1 ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_REVID2 Register (Offset = 2Ch) [reset = 0h]

Revision Identification Register 2

Return to [Summary Table](#)

**Table 4-1268. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 802Ch       |

**Figure 4-412. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_REVID2 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| REVID2   |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1270. ICSSM\_PR1\_ICSS\_UART\_UART\_SLV\_REVID2 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                      |
|------|----------|------|-------|----------------------------------|
| 31:8 | RESERVED | NONE | 0h    | Reserved                         |
| 7:0  | REVID2   | R    | 0h    | Peripheral Identification Number |

#### 4.2.2.219 ICSSM\_PR1\_IEP0\_SLV\_GLOBAL\_CFG\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_GLOBAL\_CFG\_REG Register (Offset = 0h) [reset = 550h]

Global Cfg

Return to [Summary Table](#)

**Table 4-1271. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E000h       |

**Figure 4-413. ICSSM\_PR1\_IEP0\_SLV\_GLOBAL\_CFG\_REG Name Register**

|             |    |    |    |          |    |            |    |
|-------------|----|----|----|----------|----|------------|----|
| 31          | 30 | 29 | 28 | 27       | 26 | 25         | 24 |
| RESERVED    |    |    |    |          |    |            |    |
| NONE        |    |    |    |          |    |            |    |
| 0h          |    |    |    |          |    |            |    |
| 23          | 22 | 21 | 20 | 19       | 18 | 17         | 16 |
| RESERVED    |    |    |    | CMP_INC  |    |            |    |
| NONE        |    |    |    | R/W      |    |            |    |
| 0h          |    |    |    | 5h       |    |            |    |
| 15          | 14 | 13 | 12 | 11       | 10 | 9          | 8  |
| CMP_INC     |    |    |    |          |    |            |    |
| R/W         |    |    |    |          |    |            |    |
| 5h          |    |    |    |          |    |            |    |
| 7           | 6  | 5  | 4  | 3        | 2  | 1          | 0  |
| DEFAULT_INC |    |    |    | RESERVED |    | CNT_ENABLE |    |
| R/W         |    |    |    | NONE     |    | R/W        |    |
| 5h          |    |    |    | 0h       |    | 0h         |    |

**Table 4-1273. ICSSM\_PR1\_IEP0\_SLV\_GLOBAL\_CFG\_REG Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description |
|-------|-------------|------|-------|-------------|
| 31:20 | RESERVED    | NONE | 0h    | Reserved    |
| 19:8  | CMP_INC     | R/W  | 5h    |             |
| 7:4   | DEFAULT_INC | R/W  | 5h    |             |
| 3:1   | RESERVED    | NONE | 0h    | Reserved    |
| 0     | CNT_ENABLE  | R/W  | 0h    |             |

#### 4.2.2.220 ICSSM\_PR1\_IEP0\_SLV\_GLOBAL\_STATUS\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_GLOBAL\_STATUS\_REG Register (Offset = 4h) [reset = 0h]

Status

Return to [Summary Table](#)

**Table 4-1274. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E004h       |

**Figure 4-414. ICSSM\_PR1\_IEP0\_SLV\_GLOBAL\_STATUS\_REG Name Register**

|          |    |    |    |    |    |    |         |
|----------|----|----|----|----|----|----|---------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24      |
| RESERVED |    |    |    |    |    |    |         |
| NONE     |    |    |    |    |    |    |         |
| 0h       |    |    |    |    |    |    |         |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16      |
| RESERVED |    |    |    |    |    |    |         |
| NONE     |    |    |    |    |    |    |         |
| 0h       |    |    |    |    |    |    |         |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8       |
| RESERVED |    |    |    |    |    |    |         |
| NONE     |    |    |    |    |    |    |         |
| 0h       |    |    |    |    |    |    |         |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0       |
| RESERVED |    |    |    |    |    |    | CNT_OVF |
| NONE     |    |    |    |    |    |    | R/W1TC  |
| 0h       |    |    |    |    |    |    | 0h      |

**Table 4-1276. ICSSM\_PR1\_IEP0\_SLV\_GLOBAL\_STATUS\_REG Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description |
|------|----------|--------|-------|-------------|
| 31:1 | RESERVED | NONE   | 0h    | Reserved    |
| 0    | CNT_OVF  | R/W1TC | 0h    |             |

#### 4.2.2.221 ICSSM\_PR1\_IEP0\_SLV\_COMPEN\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_COMPEN\_REG Register (Offset = 8h) [reset = 0h]

Compensation

Return to [Summary Table](#)

**Table 4-1277. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E008h       |

**Figure 4-415. ICSSM\_PR1\_IEP0\_SLV\_COMPEN\_REG Name Register**

|            |            |    |    |    |    |    |    |
|------------|------------|----|----|----|----|----|----|
| 31         | 30         | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED   |            |    |    |    |    |    |    |
| NONE       |            |    |    |    |    |    |    |
| 0h         |            |    |    |    |    |    |    |
| 23         | 22         | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED   | COMPEN_CNT |    |    |    |    |    |    |
| NONE       | R/W        |    |    |    |    |    |    |
| 0h         | 0h         |    |    |    |    |    |    |
| 15         | 14         | 13 | 12 | 11 | 10 | 9  | 8  |
| COMPEN_CNT |            |    |    |    |    |    |    |
| R/W        |            |    |    |    |    |    |    |
| 0h         |            |    |    |    |    |    |    |
| 7          | 6          | 5  | 4  | 3  | 2  | 1  | 0  |
| COMPEN_CNT |            |    |    |    |    |    |    |
| R/W        |            |    |    |    |    |    |    |
| 0h         |            |    |    |    |    |    |    |

**Table 4-1279. ICSSM\_PR1\_IEP0\_SLV\_COMPEN\_REG Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description |
|-------|------------|------|-------|-------------|
| 31:23 | RESERVED   | NONE | 0h    | Reserved    |
| 22:0  | COMPEN_CNT | R/W  | 0h    |             |

#### 4.2.2.222 ICSSM\_PR1\_IEP0\_SLV\_SLOW\_COMPEN\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_SLOW\_COMPEN\_REG Register (Offset = Ch) [reset = 0h]

Slow Compensation

Return to [Summary Table](#)

**Table 4-1280. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E00Ch       |

**Figure 4-416. ICSSM\_PR1\_IEP0\_SLV\_SLOW\_COMPEN\_REG Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SLOW_COMPEN_CNT |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SLOW_COMPEN_CNT |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SLOW_COMPEN_CNT |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SLOW_COMPEN_CNT |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 4-1282. ICSSM\_PR1\_IEP0\_SLV\_SLOW\_COMPEN\_REG Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description |
|------|-----------------|------|-------|-------------|
| 31:0 | SLOW_COMPEN_CNT | R/W  | 0h    |             |

#### 4.2.2.223 ICSSM\_PR1\_IEP0\_SLV\_COUNT\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_COUNT\_REG0 Register (Offset = 10h) [reset = 0h]

Low Counter

Return to [Summary Table](#)

**Table 4-1283. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E010h       |

**Figure 4-417. ICSSM\_PR1\_IEP0\_SLV\_COUNT\_REG0 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT_LO |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT_LO |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT_LO |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT_LO |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1285. ICSSM\_PR1\_IEP0\_SLV\_COUNT\_REG0 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | COUNT_LO | R/W  | 0h    |             |

#### 4.2.2.224 ICSSM\_PR1\_IEP0\_SLV\_COUNT\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_COUNT\_REG1 Register (Offset = 14h) [reset = 0h]

High Counter

Return to [Summary Table](#)

**Table 4-1286. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E014h       |

**Figure 4-418. ICSSM\_PR1\_IEP0\_SLV\_COUNT\_REG1 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT_HI |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT_HI |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT_HI |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT_HI |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1288. ICSSM\_PR1\_IEP0\_SLV\_COUNT\_REG1 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | COUNT_HI | R/W  | 0h    |             |



#### 4.2.2.225 ICSSM\_PR1\_IEP0\_SLV\_CAP\_CFG\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAP\_CFG\_REG Register (Offset = 18h) [reset = 1FC00h]

Capture Cfg

Return to [Summary Table](#)

**Table 4-1289. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E018h       |

**Figure 4-419. ICSSM\_PR1\_IEP0\_SLV\_CAP\_CFG\_REG Name Register**

|              |    |    |    |              |    |    |    |
|--------------|----|----|----|--------------|----|----|----|
| 31           | 30 | 29 | 28 | 27           | 26 | 25 | 24 |
| RESERVED     |    |    |    |              |    |    |    |
| NONE         |    |    |    |              |    |    |    |
| 0h           |    |    |    |              |    |    |    |
| 23           | 22 | 21 | 20 | 19           | 18 | 17 | 16 |
| EXT_CAP_EN   |    |    |    | CAP_ASYNC_EN |    |    |    |
| R/W          |    |    |    | R/W          |    |    |    |
| 0h           |    |    |    | 7Fh          |    |    |    |
| 15           | 14 | 13 | 12 | 11           | 10 | 9  | 8  |
| CAP_ASYNC_EN |    |    |    | CAP_EN       |    |    |    |
| R/W          |    |    |    | R/W          |    |    |    |
| 7Fh          |    |    |    | 0h           |    |    |    |
| 7            | 6  | 5  | 4  | 3            | 2  | 1  | 0  |
| CAP_EN       |    |    |    |              |    |    |    |
| R/W          |    |    |    |              |    |    |    |
| 0h           |    |    |    |              |    |    |    |

**Table 4-1291. ICSSM\_PR1\_IEP0\_SLV\_CAP\_CFG\_REG Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description |
|-------|--------------|------|-------|-------------|
| 31:24 | RESERVED     | NONE | 0h    | Reserved    |
| 23:18 | EXT_CAP_EN   | R/W  | 0h    |             |
| 17:10 | CAP_ASYNC_EN | R/W  | 7Fh   |             |
| 9:0   | CAP_EN       | R/W  | 0h    |             |

#### 4.2.2.226 ICSSM\_PR1\_IEP0\_SLV\_CAP\_STATUS\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAP\_STATUS\_REG Register (Offset = 1Ch) [reset = 0h]

Capture Status Cfg

Return to [Summary Table](#)

**Table 4-1292. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E01Ch       |

**Figure 4-420. ICSSM\_PR1\_IEP0\_SLV\_CAP\_STATUS\_REG Name Register**

|           |    |    |    |    |           |    |    |
|-----------|----|----|----|----|-----------|----|----|
| 31        | 30 | 29 | 28 | 27 | 26        | 25 | 24 |
| RESERVED  |    |    |    |    |           |    |    |
| NONE      |    |    |    |    |           |    |    |
| 0h        |    |    |    |    |           |    |    |
| 23        | 22 | 21 | 20 | 19 | 18        | 17 | 16 |
| CAP_RAW   |    |    |    |    |           |    |    |
| R         |    |    |    |    |           |    |    |
| 0h        |    |    |    |    |           |    |    |
| 15        | 14 | 13 | 12 | 11 | 10        | 9  | 8  |
| RESERVED  |    |    |    |    | CAP_VALID |    |    |
| NONE      |    |    |    |    | R         |    |    |
| 0h        |    |    |    |    | 0h        |    |    |
| 7         | 6  | 5  | 4  | 3  | 2         | 1  | 0  |
| CAP_VALID |    |    |    |    |           |    |    |
| R         |    |    |    |    |           |    |    |
| 0h        |    |    |    |    |           |    |    |

**Table 4-1294. ICSSM\_PR1\_IEP0\_SLV\_CAP\_STATUS\_REG Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description |
|-------|-----------|------|-------|-------------|
| 31:24 | RESERVED  | NONE | 0h    | Reserved    |
| 23:16 | CAP_RAW   | R    | 0h    |             |
| 15:11 | RESERVED  | NONE | 0h    | Reserved    |
| 10:0  | CAP_VALID | R    | 0h    |             |

#### 4.2.2.227 ICSSM\_PR1\_IEP0\_SLV\_CAPR0\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR0\_REG0 Register (Offset = 20h) [reset = 0h]

Capture Rise00

Return to [Summary Table](#)

**Table 4-1295. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E020h       |

**Figure 4-421. ICSSM\_PR1\_IEP0\_SLV\_CAPR0\_REG0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR0_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR0_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR0_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR0_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1297. ICSSM\_PR1\_IEP0\_SLV\_CAPR0\_REG0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR0_0 | R    | 0h    |             |

#### 4.2.2.228 ICSSM\_PR1\_IEP0\_SLV\_CAPR0\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR0\_REG1 Register (Offset = 24h) [reset = 0h]

Capture Rise10

Return to [Summary Table](#)

**Table 4-1298. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E024h       |

**Figure 4-422. ICSSM\_PR1\_IEP0\_SLV\_CAPR0\_REG1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR0_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR0_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR0_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR0_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1300. ICSSM\_PR1\_IEP0\_SLV\_CAPR0\_REG1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR0_1 | R    | 0h    |             |

#### 4.2.2.229 ICSSM\_PR1\_IEP0\_SLV\_CAPR1\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR1\_REG0 Register (Offset = 28h) [reset = 0h]

Capture Rise01

Return to [Summary Table](#)

**Table 4-1301. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E028h       |

**Figure 4-423. ICSSM\_PR1\_IEP0\_SLV\_CAPR1\_REG0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR1_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR1_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR1_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR1_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1303. ICSSM\_PR1\_IEP0\_SLV\_CAPR1\_REG0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR1_0 | R    | 0h    |             |

#### 4.2.2.230 ICSSM\_PR1\_IEP0\_SLV\_CAPR1\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR1\_REG1 Register (Offset = 2Ch) [reset = 0h]

Capture Rise11

Return to [Summary Table](#)

**Table 4-1304. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E02Ch       |

**Figure 4-424. ICSSM\_PR1\_IEP0\_SLV\_CAPR1\_REG1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR1_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR1_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR1_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR1_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1306. ICSSM\_PR1\_IEP0\_SLV\_CAPR1\_REG1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR1_1 | R    | 0h    |             |

#### 4.2.2.231 ICSSM\_PR1\_IEP0\_SLV\_CAPR2\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR2\_REG0 Register (Offset = 30h) [reset = 0h]

Capture Rise02

Return to [Summary Table](#)

**Table 4-1307. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E030h       |

**Figure 4-425. ICSSM\_PR1\_IEP0\_SLV\_CAPR2\_REG0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR2_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR2_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR2_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR2_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1309. ICSSM\_PR1\_IEP0\_SLV\_CAPR2\_REG0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR2_0 | R    | 0h    |             |

#### 4.2.2.232 ICSSM\_PR1\_IEP0\_SLV\_CAPR2\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR2\_REG1 Register (Offset = 34h) [reset = 0h]

Capture Rise12

Return to [Summary Table](#)

**Table 4-1310. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E034h       |

**Figure 4-426. ICSSM\_PR1\_IEP0\_SLV\_CAPR2\_REG1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR2_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR2_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR2_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR2_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1312. ICSSM\_PR1\_IEP0\_SLV\_CAPR2\_REG1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR2_1 | R    | 0h    |             |



#### 4.2.2.233 ICSSM\_PR1\_IEP0\_SLV\_CAPR3\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR3\_REG0 Register (Offset = 38h) [reset = 0h]

Capture Rise03

Return to [Summary Table](#)

**Table 4-1313. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E038h       |

**Figure 4-427. ICSSM\_PR1\_IEP0\_SLV\_CAPR3\_REG0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR3_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR3_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR3_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR3_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1315. ICSSM\_PR1\_IEP0\_SLV\_CAPR3\_REG0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR3_0 | R    | 0h    |             |

#### 4.2.2.234 ICSSM\_PR1\_IEP0\_SLV\_CAPR3\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR3\_REG1 Register (Offset = 3Ch) [reset = 0h]

Capture Rise13

Return to [Summary Table](#)

**Table 4-1316. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E03Ch       |

**Figure 4-428. ICSSM\_PR1\_IEP0\_SLV\_CAPR3\_REG1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR3_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR3_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR3_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR3_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1318. ICSSM\_PR1\_IEP0\_SLV\_CAPR3\_REG1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR3_1 | R    | 0h    |             |

#### 4.2.2.235 ICSSM\_PR1\_IEP0\_SLV\_CAPR4\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR4\_REG0 Register (Offset = 40h) [reset = 0h]

Capture Rise04

Return to [Summary Table](#)

**Table 4-1319. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E040h       |

**Figure 4-429. ICSSM\_PR1\_IEP0\_SLV\_CAPR4\_REG0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR4_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR4_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR4_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR4_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1321. ICSSM\_PR1\_IEP0\_SLV\_CAPR4\_REG0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR4_0 | R    | 0h    |             |

#### 4.2.2.236 ICSSM\_PR1\_IEP0\_SLV\_CAPR4\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR4\_REG1 Register (Offset = 44h) [reset = 0h]

Capture Rise14

Return to [Summary Table](#)

**Table 4-1322. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E044h       |

**Figure 4-430. ICSSM\_PR1\_IEP0\_SLV\_CAPR4\_REG1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR4_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR4_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR4_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR4_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1324. ICSSM\_PR1\_IEP0\_SLV\_CAPR4\_REG1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR4_1 | R    | 0h    |             |

#### 4.2.2.237 ICSSM\_PR1\_IEP0\_SLV\_CAPR5\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR5\_REG0 Register (Offset = 48h) [reset = 0h]

Capture Rise05

Return to [Summary Table](#)

**Table 4-1325. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E048h       |

**Figure 4-431. ICSSM\_PR1\_IEP0\_SLV\_CAPR5\_REG0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR5_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR5_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR5_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR5_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1327. ICSSM\_PR1\_IEP0\_SLV\_CAPR5\_REG0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR5_0 | R    | 0h    |             |

#### 4.2.2.238 ICSSM\_PR1\_IEP0\_SLV\_CAPR5\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR5\_REG1 Register (Offset = 4Ch) [reset = 0h]

Capture Rise15

Return to [Summary Table](#)

**Table 4-1328. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E04Ch       |

**Figure 4-432. ICSSM\_PR1\_IEP0\_SLV\_CAPR5\_REG1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR5_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR5_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR5_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR5_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1330. ICSSM\_PR1\_IEP0\_SLV\_CAPR5\_REG1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR5_1 | R    | 0h    |             |

#### 4.2.2.239 ICSSM\_PR1\_IEP0\_SLV\_CAPR6\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR6\_REG0 Register (Offset = 50h) [reset = 0h]

Capture Rise06

Return to [Summary Table](#)

**Table 4-1331. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E050h       |

**Figure 4-433. ICSSM\_PR1\_IEP0\_SLV\_CAPR6\_REG0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR6_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR6_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR6_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR6_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1333. ICSSM\_PR1\_IEP0\_SLV\_CAPR6\_REG0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR6_0 | R    | 0h    |             |

#### 4.2.2.240 ICSSM\_PR1\_IEP0\_SLV\_CAPR6\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR6\_REG1 Register (Offset = 54h) [reset = 0h]

Capture Rise16

Return to [Summary Table](#)

**Table 4-1334. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E054h       |

**Figure 4-434. ICSSM\_PR1\_IEP0\_SLV\_CAPR6\_REG1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR6_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR6_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR6_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR6_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1336. ICSSM\_PR1\_IEP0\_SLV\_CAPR6\_REG1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR6_1 | R    | 0h    |             |



#### 4.2.2.241 ICSSM\_PR1\_IEP0\_SLV\_CAPF6\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPF6\_REG0 Register (Offset = 58h) [reset = 0h]

Capture Fall06

Return to [Summary Table](#)

**Table 4-1337. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E058h       |

**Figure 4-435. ICSSM\_PR1\_IEP0\_SLV\_CAPF6\_REG0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPF6_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPF6_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPF6_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPF6_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1339. ICSSM\_PR1\_IEP0\_SLV\_CAPF6\_REG0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPF6_0 | R    | 0h    |             |

#### 4.2.2.242 ICSSM\_PR1\_IEP0\_SLV\_CAPF6\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPF6\_REG1 Register (Offset = 5Ch) [reset = 0h]

Capture Fall16

Return to [Summary Table](#)

**Table 4-1340. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E05Ch       |

**Figure 4-436. ICSSM\_PR1\_IEP0\_SLV\_CAPF6\_REG1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPF6_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPF6_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPF6_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPF6_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1342. ICSSM\_PR1\_IEP0\_SLV\_CAPF6\_REG1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPF6_1 | R    | 0h    |             |

#### 4.2.2.243 ICSSM\_PR1\_IEP0\_SLV\_CAPR7\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR7\_REG0 Register (Offset = 60h) [reset = 0h]

Capture Rise07

Return to [Summary Table](#)

**Table 4-1343. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E060h       |

**Figure 4-437. ICSSM\_PR1\_IEP0\_SLV\_CAPR7\_REG0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR7_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR7_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR7_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR7_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1345. ICSSM\_PR1\_IEP0\_SLV\_CAPR7\_REG0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR7_0 | R    | 0h    |             |

#### 4.2.2.244 ICSSM\_PR1\_IEP0\_SLV\_CAPR7\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR7\_REG1 Register (Offset = 64h) [reset = 0h]

Capture Rise17

Return to [Summary Table](#)

**Table 4-1346. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E064h       |

**Figure 4-438. ICSSM\_PR1\_IEP0\_SLV\_CAPR7\_REG1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR7_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR7_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR7_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR7_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1348. ICSSM\_PR1\_IEP0\_SLV\_CAPR7\_REG1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR7_1 | R    | 0h    |             |

#### 4.2.2.245 ICSSM\_PR1\_IEP0\_SLV\_CAPF7\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPF7\_REG0 Register (Offset = 68h) [reset = 0h]

Capture Fall07

Return to [Summary Table](#)

**Table 4-1349. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E068h       |

**Figure 4-439. ICSSM\_PR1\_IEP0\_SLV\_CAPF7\_REG0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPF7_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPF7_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPF7_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPF7_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1351. ICSSM\_PR1\_IEP0\_SLV\_CAPF7\_REG0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPF7_0 | R    | 0h    |             |

#### 4.2.2.246 ICSSM\_PR1\_IEP0\_SLV\_CAPF7\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPF7\_REG1 Register (Offset = 6Ch) [reset = 0h]

Capture Fall17

Return to [Summary Table](#)

**Table 4-1352. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E06Ch       |

**Figure 4-440. ICSSM\_PR1\_IEP0\_SLV\_CAPF7\_REG1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPF7_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPF7_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPF7_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPF7_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1354. ICSSM\_PR1\_IEP0\_SLV\_CAPF7\_REG1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPF7_1 | R    | 0h    |             |

#### 4.2.2.247 ICSSM\_PR1\_IEP0\_SLV\_CMP\_CFG\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP\_CFG\_REG Register (Offset = 70h) [reset = 0h]

Capture Cfg

Return to [Summary Table](#)

**Table 4-1355. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E070h       |

**Figure 4-441. ICSSM\_PR1\_IEP0\_SLV\_CMP\_CFG\_REG Name Register**

|          |    |    |    |    |    |                 |        |
|----------|----|----|----|----|----|-----------------|--------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25              | 24     |
| RESERVED |    |    |    |    |    |                 |        |
| NONE     |    |    |    |    |    |                 |        |
| 0h       |    |    |    |    |    |                 |        |
| 23       | 22 | 21 | 20 | 19 | 18 | 17              | 16     |
| RESERVED |    |    |    |    |    | SHADOW_EN       | CMP_EN |
| NONE     |    |    |    |    |    | R/W             | R/W    |
| 0h       |    |    |    |    |    | 0h              | 0h     |
| 15       | 14 | 13 | 12 | 11 | 10 | 9               | 8      |
| CMP_EN   |    |    |    |    |    |                 |        |
| R/W      |    |    |    |    |    |                 |        |
| 0h       |    |    |    |    |    |                 |        |
| 7        | 6  | 5  | 4  | 3  | 2  | 1               | 0      |
| CMP_EN   |    |    |    |    |    | CMP0_RST_CNT_EN |        |
| R/W      |    |    |    |    |    | R/W             |        |
| 0h       |    |    |    |    |    | 0h              |        |

**Table 4-1357. ICSSM\_PR1\_IEP0\_SLV\_CMP\_CFG\_REG Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description |
|-------|-----------------|------|-------|-------------|
| 31:18 | RESERVED        | NONE | 0h    | Reserved    |
| 17    | SHADOW_EN       | R/W  | 0h    |             |
| 16:1  | CMP_EN          | R/W  | 0h    |             |
| 0     | CMP0_RST_CNT_EN | R/W  | 0h    |             |

#### 4.2.2.248 ICSSM\_PR1\_IEP0\_SLV\_CMP\_STATUS\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP\_STATUS\_REG Register (Offset = 74h) [reset = 0h]

Capture Status

Return to [Summary Table](#)

**Table 4-1358. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E074h       |

**Figure 4-442. ICSSM\_PR1\_IEP0\_SLV\_CMP\_STATUS\_REG Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP_STATUS |    |    |    |    |    |    |    |
| R/W1TC     |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP_STATUS |    |    |    |    |    |    |    |
| R/W1TC     |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 4-1360. ICSSM\_PR1\_IEP0\_SLV\_CMP\_STATUS\_REG Register Field Descriptions**

| Bit   | Field      | Type   | Reset | Description |
|-------|------------|--------|-------|-------------|
| 31:16 | RESERVED   | NONE   | 0h    | Reserved    |
| 15:0  | CMP_STATUS | R/W1TC | 0h    |             |



#### 4.2.2.249 ICSSM\_PR1\_IEP0\_SLV\_CMP0\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP0\_REG0 Register (Offset = 78h) [reset = 0h]

Compare00

Return to [Summary Table](#)

**Table 4-1361. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E078h       |

**Figure 4-443. ICSSM\_PR1\_IEP0\_SLV\_CMP0\_REG0 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP0_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP0_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP0_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP0_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 4-1363. ICSSM\_PR1\_IEP0\_SLV\_CMP0\_REG0 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description |
|------|--------|------|-------|-------------|
| 31:0 | CMP0_0 | R/W  | 0h    |             |

#### 4.2.2.250 ICSSM\_PR1\_IEP0\_SLV\_CMP0\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP0\_REG1 Register (Offset = 7Ch) [reset = 0h]

Compare10

Return to [Summary Table](#)

**Table 4-1364. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E07Ch       |

**Figure 4-444. ICSSM\_PR1\_IEP0\_SLV\_CMP0\_REG1 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP0_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP0_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP0_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP0_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 4-1366. ICSSM\_PR1\_IEP0\_SLV\_CMP0\_REG1 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description |
|------|--------|------|-------|-------------|
| 31:0 | CMP0_1 | R/W  | 0h    |             |

#### 4.2.2.251 ICSSM\_PR1\_IEP0\_SLV\_CMP1\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP1\_REG0 Register (Offset = 80h) [reset = 0h]

Compare01

Return to [Summary Table](#)

**Table 4-1367. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E080h       |

**Figure 4-445. ICSSM\_PR1\_IEP0\_SLV\_CMP1\_REG0 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP1_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP1_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP1_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP1_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 4-1369. ICSSM\_PR1\_IEP0\_SLV\_CMP1\_REG0 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description |
|------|--------|------|-------|-------------|
| 31:0 | CMP1_0 | R/W  | 0h    |             |

#### 4.2.2.252 ICSSM\_PR1\_IEP0\_SLV\_CMP1\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP1\_REG1 Register (Offset = 84h) [reset = 0h]

Compare11

Return to [Summary Table](#)

**Table 4-1370. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E084h       |

**Figure 4-446. ICSSM\_PR1\_IEP0\_SLV\_CMP1\_REG1 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP1_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP1_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP1_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP1_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 4-1372. ICSSM\_PR1\_IEP0\_SLV\_CMP1\_REG1 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description |
|------|--------|------|-------|-------------|
| 31:0 | CMP1_1 | R/W  | 0h    |             |

#### 4.2.2.253 ICSSM\_PR1\_IEP0\_SLV\_CMP2\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP2\_REG0 Register (Offset = 88h) [reset = 0h]

Compare02

Return to [Summary Table](#)

**Table 4-1373. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E088h       |

**Figure 4-447. ICSSM\_PR1\_IEP0\_SLV\_CMP2\_REG0 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP2_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP2_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP2_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP2_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 4-1375. ICSSM\_PR1\_IEP0\_SLV\_CMP2\_REG0 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description |
|------|--------|------|-------|-------------|
| 31:0 | CMP2_0 | R/W  | 0h    |             |

#### 4.2.2.254 ICSSM\_PR1\_IEP0\_SLV\_CMP2\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP2\_REG1 Register (Offset = 8Ch) [reset = 0h]

Compare12

Return to [Summary Table](#)

**Table 4-1376. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E08Ch       |

**Figure 4-448. ICSSM\_PR1\_IEP0\_SLV\_CMP2\_REG1 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP2_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP2_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP2_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP2_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 4-1378. ICSSM\_PR1\_IEP0\_SLV\_CMP2\_REG1 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description |
|------|--------|------|-------|-------------|
| 31:0 | CMP2_1 | R/W  | 0h    |             |

#### 4.2.2.255 ICSSM\_PR1\_IEP0\_SLV\_CMP3\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP3\_REG0 Register (Offset = 90h) [reset = 0h]

Compare03

Return to [Summary Table](#)

**Table 4-1379. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E090h       |

**Figure 4-449. ICSSM\_PR1\_IEP0\_SLV\_CMP3\_REG0 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP3_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP3_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP3_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP3_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 4-1381. ICSSM\_PR1\_IEP0\_SLV\_CMP3\_REG0 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description |
|------|--------|------|-------|-------------|
| 31:0 | CMP3_0 | R/W  | 0h    |             |

#### 4.2.2.256 ICSSM\_PR1\_IEP0\_SLV\_CMP3\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP3\_REG1 Register (Offset = 94h) [reset = 0h]

Compare13

Return to [Summary Table](#)

**Table 4-1382. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E094h       |

**Figure 4-450. ICSSM\_PR1\_IEP0\_SLV\_CMP3\_REG1 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP3_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP3_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP3_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP3_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 4-1384. ICSSM\_PR1\_IEP0\_SLV\_CMP3\_REG1 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description |
|------|--------|------|-------|-------------|
| 31:0 | CMP3_1 | R/W  | 0h    |             |



#### 4.2.2.257 ICSSM\_PR1\_IEP0\_SLV\_CMP4\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP4\_REG0 Register (Offset = 98h) [reset = 0h]

Compare04

Return to [Summary Table](#)

**Table 4-1385. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E098h       |

**Figure 4-451. ICSSM\_PR1\_IEP0\_SLV\_CMP4\_REG0 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP4_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP4_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP4_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP4_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 4-1387. ICSSM\_PR1\_IEP0\_SLV\_CMP4\_REG0 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description |
|------|--------|------|-------|-------------|
| 31:0 | CMP4_0 | R/W  | 0h    |             |

#### 4.2.2.258 ICSSM\_PR1\_IEP0\_SLV\_CMP4\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP4\_REG1 Register (Offset = 9Ch) [reset = 0h]

Compare14

Return to [Summary Table](#)

**Table 4-1388. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E09Ch       |

**Figure 4-452. ICSSM\_PR1\_IEP0\_SLV\_CMP4\_REG1 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP4_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP4_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP4_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP4_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 4-1390. ICSSM\_PR1\_IEP0\_SLV\_CMP4\_REG1 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description |
|------|--------|------|-------|-------------|
| 31:0 | CMP4_1 | R/W  | 0h    |             |

#### 4.2.2.259 ICSSM\_PR1\_IEP0\_SLV\_CMP5\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP5\_REG0 Register (Offset = A0h) [reset = 0h]

Compare05

Return to [Summary Table](#)

**Table 4-1391. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E0A0h       |

**Figure 4-453. ICSSM\_PR1\_IEP0\_SLV\_CMP5\_REG0 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP5_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP5_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP5_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP5_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 4-1393. ICSSM\_PR1\_IEP0\_SLV\_CMP5\_REG0 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description |
|------|--------|------|-------|-------------|
| 31:0 | CMP5_0 | R/W  | 0h    |             |

#### 4.2.2.260 ICSSM\_PR1\_IEP0\_SLV\_CMP5\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP5\_REG1 Register (Offset = A4h) [reset = 0h]

Compare15

Return to [Summary Table](#)

**Table 4-1394. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E0A4h       |

**Figure 4-454. ICSSM\_PR1\_IEP0\_SLV\_CMP5\_REG1 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP5_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP5_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP5_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP5_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 4-1396. ICSSM\_PR1\_IEP0\_SLV\_CMP5\_REG1 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description |
|------|--------|------|-------|-------------|
| 31:0 | CMP5_1 | R/W  | 0h    |             |

#### 4.2.2.261 ICSSM\_PR1\_IEP0\_SLV\_CMP6\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP6\_REG0 Register (Offset = A8h) [reset = 0h]

Compare06

Return to [Summary Table](#)

**Table 4-1397. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E0A8h       |

**Figure 4-455. ICSSM\_PR1\_IEP0\_SLV\_CMP6\_REG0 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP6_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP6_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP6_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP6_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 4-1399. ICSSM\_PR1\_IEP0\_SLV\_CMP6\_REG0 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description |
|------|--------|------|-------|-------------|
| 31:0 | CMP6_0 | R/W  | 0h    |             |

#### 4.2.2.262 ICSSM\_PR1\_IEP0\_SLV\_CMP6\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP6\_REG1 Register (Offset = ACh) [reset = 0h]

Compare16

Return to [Summary Table](#)

**Table 4-1400. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E0ACh       |

**Figure 4-456. ICSSM\_PR1\_IEP0\_SLV\_CMP6\_REG1 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP6_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP6_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP6_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP6_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 4-1402. ICSSM\_PR1\_IEP0\_SLV\_CMP6\_REG1 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description |
|------|--------|------|-------|-------------|
| 31:0 | CMP6_1 | R/W  | 0h    |             |

#### 4.2.2.263 ICSSM\_PR1\_IEP0\_SLV\_CMP7\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP7\_REG0 Register (Offset = B0h) [reset = 0h]

Compare07

Return to [Summary Table](#)

**Table 4-1403. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E0B0h       |

**Figure 4-457. ICSSM\_PR1\_IEP0\_SLV\_CMP7\_REG0 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP7_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP7_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP7_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP7_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 4-1405. ICSSM\_PR1\_IEP0\_SLV\_CMP7\_REG0 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description |
|------|--------|------|-------|-------------|
| 31:0 | CMP7_0 | R/W  | 0h    |             |

#### 4.2.2.264 ICSSM\_PR1\_IEP0\_SLV\_CMP7\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP7\_REG1 Register (Offset = B4h) [reset = 0h]

Compare17

Return to [Summary Table](#)

**Table 4-1406. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E0B4h       |

**Figure 4-458. ICSSM\_PR1\_IEP0\_SLV\_CMP7\_REG1 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP7_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP7_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP7_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP7_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 4-1408. ICSSM\_PR1\_IEP0\_SLV\_CMP7\_REG1 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description |
|------|--------|------|-------|-------------|
| 31:0 | CMP7_1 | R/W  | 0h    |             |



#### 4.2.2.265 ICSSM\_PR1\_IEP0\_SLV\_RXIPG0\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_RXIPG0\_REG Register (Offset = B8h) [reset = FFFF0000h]

RXIPG0

Return to [Summary Table](#)
**Table 4-1409. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E0B8h       |

**Figure 4-459. ICSSM\_PR1\_IEP0\_SLV\_RXIPG0\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RX_MIN_IPG0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| FFFFh       |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RX_MIN_IPG0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| FFFFh       |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RX_IPG0     |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RX_IPG0     |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 4-1411. ICSSM\_PR1\_IEP0\_SLV\_RXIPG0\_REG Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description |
|-------|-------------|------|-------|-------------|
| 31:16 | RX_MIN_IPG0 | R/W  | FFFFh |             |
| 15:0  | RX_IPG0     | R    | 0h    |             |

#### 4.2.2.266 ICSSM\_PR1\_IEP0\_SLV\_RXIPG1\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_RXIPG1\_REG Register (Offset = BCh) [reset = FFFF0000h]

RXIPG1

Return to [Summary Table](#)
**Table 4-1412. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E0BCh       |

**Figure 4-460. ICSSM\_PR1\_IEP0\_SLV\_RXIPG1\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RX_MIN_IPG1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| FFFFh       |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RX_MIN_IPG1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| FFFFh       |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RX_IPG1     |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RX_IPG1     |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 4-1414. ICSSM\_PR1\_IEP0\_SLV\_RXIPG1\_REG Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description |
|-------|-------------|------|-------|-------------|
| 31:16 | RX_MIN_IPG1 | R/W  | FFFFh |             |
| 15:0  | RX_IPG1     | R    | 0h    |             |

#### 4.2.2.267 ICSSM\_PR1\_IEP0\_SLV\_CMP8\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP8\_REG0 Register (Offset = C0h) [reset = 0h]

Compare08

Return to [Summary Table](#)

**Table 4-1415. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E0C0h       |

**Figure 4-461. ICSSM\_PR1\_IEP0\_SLV\_CMP8\_REG0 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP8_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP8_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP8_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP8_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 4-1417. ICSSM\_PR1\_IEP0\_SLV\_CMP8\_REG0 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description |
|------|--------|------|-------|-------------|
| 31:0 | CMP8_0 | R/W  | 0h    |             |

#### 4.2.2.268 ICSSM\_PR1\_IEP0\_SLV\_CMP8\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP8\_REG1 Register (Offset = C4h) [reset = 0h]

Compare18

Return to [Summary Table](#)

**Table 4-1418. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E0C4h       |

**Figure 4-462. ICSSM\_PR1\_IEP0\_SLV\_CMP8\_REG1 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP8_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP8_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP8_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP8_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 4-1420. ICSSM\_PR1\_IEP0\_SLV\_CMP8\_REG1 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description |
|------|--------|------|-------|-------------|
| 31:0 | CMP8_1 | R/W  | 0h    |             |

#### 4.2.2.269 ICSSM\_PR1\_IEP0\_SLV\_CMP9\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP9\_REG0 Register (Offset = C8h) [reset = 0h]

Compare09

Return to [Summary Table](#)

**Table 4-1421. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E0C8h       |

**Figure 4-463. ICSSM\_PR1\_IEP0\_SLV\_CMP9\_REG0 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP9_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP9_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP9_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP9_0 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 4-1423. ICSSM\_PR1\_IEP0\_SLV\_CMP9\_REG0 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description |
|------|--------|------|-------|-------------|
| 31:0 | CMP9_0 | R/W  | 0h    |             |

#### 4.2.2.270 ICSSM\_PR1\_IEP0\_SLV\_CMP9\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP9\_REG1 Register (Offset = CCh) [reset = 0h]

Compare19

Return to [Summary Table](#)

**Table 4-1424. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E0CCh       |

**Figure 4-464. ICSSM\_PR1\_IEP0\_SLV\_CMP9\_REG1 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP9_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP9_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP9_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP9_1 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 4-1426. ICSSM\_PR1\_IEP0\_SLV\_CMP9\_REG1 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description |
|------|--------|------|-------|-------------|
| 31:0 | CMP9_1 | R/W  | 0h    |             |

#### 4.2.2.271 ICSSM\_PR1\_IEP0\_SLV\_CMP10\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP10\_REG0 Register (Offset = D0h) [reset = 0h]

Compare010

Return to [Summary Table](#)

**Table 4-1427. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E0D0h       |

**Figure 4-465. ICSSM\_PR1\_IEP0\_SLV\_CMP10\_REG0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP10_0 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP10_0 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP10_0 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP10_0 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1429. ICSSM\_PR1\_IEP0\_SLV\_CMP10\_REG0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CMP10_0 | R/W  | 0h    |             |

#### 4.2.2.272 ICSSM\_PR1\_IEP0\_SLV\_CMP10\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP10\_REG1 Register (Offset = D4h) [reset = 0h]

Compare110

Return to [Summary Table](#)

**Table 4-1430. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E0D4h       |

**Figure 4-466. ICSSM\_PR1\_IEP0\_SLV\_CMP10\_REG1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP10_1 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP10_1 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP10_1 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP10_1 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1432. ICSSM\_PR1\_IEP0\_SLV\_CMP10\_REG1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CMP10_1 | R/W  | 0h    |             |



#### 4.2.2.273 ICSSM\_PR1\_IEP0\_SLV\_CMP11\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP11\_REG0 Register (Offset = D8h) [reset = 0h]

Compare011

Return to [Summary Table](#)

**Table 4-1433. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E0D8h       |

**Figure 4-467. ICSSM\_PR1\_IEP0\_SLV\_CMP11\_REG0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP11_0 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP11_0 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP11_0 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP11_0 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1435. ICSSM\_PR1\_IEP0\_SLV\_CMP11\_REG0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CMP11_0 | R/W  | 0h    |             |

#### 4.2.2.274 ICSSM\_PR1\_IEP0\_SLV\_CMP11\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP11\_REG1 Register (Offset = DCh) [reset = 0h]

Compare111

Return to [Summary Table](#)

**Table 4-1436. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E0DCh       |

**Figure 4-468. ICSSM\_PR1\_IEP0\_SLV\_CMP11\_REG1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP11_1 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP11_1 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP11_1 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP11_1 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1438. ICSSM\_PR1\_IEP0\_SLV\_CMP11\_REG1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CMP11_1 | R/W  | 0h    |             |

#### 4.2.2.275 ICSSM\_PR1\_IEP0\_SLV\_CMP12\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP12\_REG0 Register (Offset = E0h) [reset = 0h]

Compare012

Return to [Summary Table](#)

**Table 4-1439. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E0E0h       |

**Figure 4-469. ICSSM\_PR1\_IEP0\_SLV\_CMP12\_REG0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP12_0 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP12_0 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP12_0 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP12_0 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1441. ICSSM\_PR1\_IEP0\_SLV\_CMP12\_REG0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CMP12_0 | R/W  | 0h    |             |

#### 4.2.2.276 ICSSM\_PR1\_IEP0\_SLV\_CMP12\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP12\_REG1 Register (Offset = E4h) [reset = 0h]

Compare112

Return to [Summary Table](#)

**Table 4-1442. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E0E4h       |

**Figure 4-470. ICSSM\_PR1\_IEP0\_SLV\_CMP12\_REG1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP12_1 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP12_1 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP12_1 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP12_1 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1444. ICSSM\_PR1\_IEP0\_SLV\_CMP12\_REG1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CMP12_1 | R/W  | 0h    |             |

#### 4.2.2.277 ICSSM\_PR1\_IEP0\_SLV\_CMP13\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP13\_REG0 Register (Offset = E8h) [reset = 0h]

Compare013

Return to [Summary Table](#)

**Table 4-1445. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E0E8h       |

**Figure 4-471. ICSSM\_PR1\_IEP0\_SLV\_CMP13\_REG0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP13_0 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP13_0 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP13_0 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP13_0 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1447. ICSSM\_PR1\_IEP0\_SLV\_CMP13\_REG0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CMP13_0 | R/W  | 0h    |             |

#### 4.2.2.278 ICSSM\_PR1\_IEP0\_SLV\_CMP13\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP13\_REG1 Register (Offset = ECh) [reset = 0h]

Compare113

Return to [Summary Table](#)

**Table 4-1448. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E0ECh       |

**Figure 4-472. ICSSM\_PR1\_IEP0\_SLV\_CMP13\_REG1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP13_1 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP13_1 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP13_1 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP13_1 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1450. ICSSM\_PR1\_IEP0\_SLV\_CMP13\_REG1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CMP13_1 | R/W  | 0h    |             |

#### 4.2.2.279 ICSSM\_PR1\_IEP0\_SLV\_CMP14\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP14\_REG0 Register (Offset = F0h) [reset = 0h]

Compare014

Return to [Summary Table](#)

**Table 4-1451. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E0F0h       |

**Figure 4-473. ICSSM\_PR1\_IEP0\_SLV\_CMP14\_REG0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP14_0 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP14_0 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP14_0 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP14_0 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1453. ICSSM\_PR1\_IEP0\_SLV\_CMP14\_REG0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CMP14_0 | R/W  | 0h    |             |

#### 4.2.2.280 ICSSM\_PR1\_IEP0\_SLV\_CMP14\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP14\_REG1 Register (Offset = F4h) [reset = 0h]

Compare114

Return to [Summary Table](#)

**Table 4-1454. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E0F4h       |

**Figure 4-474. ICSSM\_PR1\_IEP0\_SLV\_CMP14\_REG1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP14_1 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP14_1 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP14_1 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP14_1 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1456. ICSSM\_PR1\_IEP0\_SLV\_CMP14\_REG1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CMP14_1 | R/W  | 0h    |             |



#### 4.2.2.281 ICSSM\_PR1\_IEP0\_SLV\_CMP15\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP15\_REG0 Register (Offset = F8h) [reset = 0h]

Compare015

Return to [Summary Table](#)

**Table 4-1457. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E0F8h       |

**Figure 4-475. ICSSM\_PR1\_IEP0\_SLV\_CMP15\_REG0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP15_0 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP15_0 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP15_0 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP15_0 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1459. ICSSM\_PR1\_IEP0\_SLV\_CMP15\_REG0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CMP15_0 | R/W  | 0h    |             |

#### 4.2.2.282 ICSSM\_PR1\_IEP0\_SLV\_CMP15\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CMP15\_REG1 Register (Offset = FCh) [reset = 0h]

Compare115

Return to [Summary Table](#)

**Table 4-1460. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E0FCh       |

**Figure 4-476. ICSSM\_PR1\_IEP0\_SLV\_CMP15\_REG1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CMP15_1 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CMP15_1 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CMP15_1 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CMP15_1 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1462. ICSSM\_PR1\_IEP0\_SLV\_CMP15\_REG1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CMP15_1 | R/W  | 0h    |             |

#### 4.2.2.283 ICSSM\_PR1\_IEP0\_SLV\_COUNT\_RESET\_VAL\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_COUNT\_RESET\_VAL\_REG0 Register (Offset = 100h) [reset = 0h]

Low Counter Reset Value

Return to [Summary Table](#)

**Table 4-1463. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E100h       |

**Figure 4-477. ICSSM\_PR1\_IEP0\_SLV\_COUNT\_RESET\_VAL\_REG0 Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESET_VAL_0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESET_VAL_0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESET_VAL_0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESET_VAL_0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 4-1465. ICSSM\_PR1\_IEP0\_SLV\_COUNT\_RESET\_VAL\_REG0 Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description |
|------|-------------|------|-------|-------------|
| 31:0 | RESET_VAL_0 | R/W  | 0h    |             |

#### 4.2.2.284 ICSSM\_PR1\_IEP0\_SLV\_COUNT\_RESET\_VAL\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_COUNT\_RESET\_VAL\_REG1 Register (Offset = 104h) [reset = 0h]

Low Counter Reset Value

Return to [Summary Table](#)

**Table 4-1466. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E104h       |

**Figure 4-478. ICSSM\_PR1\_IEP0\_SLV\_COUNT\_RESET\_VAL\_REG1 Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESET_VAL_1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESET_VAL_1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESET_VAL_1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESET_VAL_1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 4-1468. ICSSM\_PR1\_IEP0\_SLV\_COUNT\_RESET\_VAL\_REG1 Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description |
|------|-------------|------|-------|-------------|
| 31:0 | RESET_VAL_1 | R/W  | 0h    |             |

#### 4.2.2.285 ICSSM\_PR1\_IEP0\_SLV\_PWM\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_PWM\_REG Register (Offset = 108h) [reset = 0h]

PWM

Return to [Summary Table](#)

**Table 4-1469. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E108h       |

**Figure 4-479. ICSSM\_PR1\_IEP0\_SLV\_PWM\_REG Name Register**

|          |    |    |    |          |                 |          |                 |
|----------|----|----|----|----------|-----------------|----------|-----------------|
| 31       | 30 | 29 | 28 | 27       | 26              | 25       | 24              |
| RESERVED |    |    |    |          |                 |          |                 |
| NONE     |    |    |    |          |                 |          |                 |
| 0h       |    |    |    |          |                 |          |                 |
| 23       | 22 | 21 | 20 | 19       | 18              | 17       | 16              |
| RESERVED |    |    |    |          |                 |          |                 |
| NONE     |    |    |    |          |                 |          |                 |
| 0h       |    |    |    |          |                 |          |                 |
| 15       | 14 | 13 | 12 | 11       | 10              | 9        | 8               |
| RESERVED |    |    |    |          |                 |          |                 |
| NONE     |    |    |    |          |                 |          |                 |
| 0h       |    |    |    |          |                 |          |                 |
| 7        | 6  | 5  | 4  | 3        | 2               | 1        | 0               |
| RESERVED |    |    |    | PWM3_HIT | PWM3_RST_CNT_EN | PWM0_HIT | PWM0_RST_CNT_EN |
| NONE     |    |    |    | R/W1TC   | R/W             | R/W1TC   | R/W             |
| 0h       |    |    |    | 0h       | 0h              | 0h       | 0h              |

**Table 4-1471. ICSSM\_PR1\_IEP0\_SLV\_PWM\_REG Register Field Descriptions**

| Bit  | Field           | Type   | Reset | Description |
|------|-----------------|--------|-------|-------------|
| 31:4 | RESERVED        | NONE   | 0h    | Reserved    |
| 3    | PWM3_HIT        | R/W1TC | 0h    |             |
| 2    | PWM3_RST_CNT_EN | R/W    | 0h    |             |
| 1    | PWM0_HIT        | R/W1TC | 0h    |             |
| 0    | PWM0_RST_CNT_EN | R/W    | 0h    |             |

#### 4.2.2.286 ICSSM\_PR1\_IEP0\_SLV\_CAPR0\_BI\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR0\_BI\_REG0 Register (Offset = 10Ch) [reset = 0h]

Capture Big Indian Rise00

Return to [Summary Table](#)

**Table 4-1472. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E10Ch       |

**Figure 4-480. ICSSM\_PR1\_IEP0\_SLV\_CAPR0\_BI\_REG0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR0_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR0_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR0_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR0_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1474. ICSSM\_PR1\_IEP0\_SLV\_CAPR0\_BI\_REG0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR0_0 | R    | 0h    |             |

#### 4.2.2.287 ICSSM\_PR1\_IEP0\_SLV\_CAPR0\_BI\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR0\_BI\_REG1 Register (Offset = 110h) [reset = 0h]

Capture Big Indian Rise10

Return to [Summary Table](#)

**Table 4-1475. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E110h       |

**Figure 4-481. ICSSM\_PR1\_IEP0\_SLV\_CAPR0\_BI\_REG1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR0_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR0_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR0_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR0_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1477. ICSSM\_PR1\_IEP0\_SLV\_CAPR0\_BI\_REG1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR0_1 | R    | 0h    |             |

#### 4.2.2.288 ICSSM\_PR1\_IEP0\_SLV\_CAPR1\_BI\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR1\_BI\_REG0 Register (Offset = 114h) [reset = 0h]

Capture Big Indian Rise01

Return to [Summary Table](#)

**Table 4-1478. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E114h       |

**Figure 4-482. ICSSM\_PR1\_IEP0\_SLV\_CAPR1\_BI\_REG0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR1_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR1_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR1_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR1_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1480. ICSSM\_PR1\_IEP0\_SLV\_CAPR1\_BI\_REG0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR1_0 | R    | 0h    |             |



#### 4.2.2.289 ICSSM\_PR1\_IEP0\_SLV\_CAPR1\_BI\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR1\_BI\_REG1 Register (Offset = 118h) [reset = 0h]

Capture Big Indian Rise11

Return to [Summary Table](#)

**Table 4-1481. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E118h       |

**Figure 4-483. ICSSM\_PR1\_IEP0\_SLV\_CAPR1\_BI\_REG1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR1_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR1_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR1_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR1_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1483. ICSSM\_PR1\_IEP0\_SLV\_CAPR1\_BI\_REG1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR1_1 | R    | 0h    |             |

#### 4.2.2.290 ICSSM\_PR1\_IEP0\_SLV\_CAPR2\_BI\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR2\_BI\_REG0 Register (Offset = 11Ch) [reset = 0h]

Capture Big Indian Rise02

Return to [Summary Table](#)

**Table 4-1484. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E11Ch       |

**Figure 4-484. ICSSM\_PR1\_IEP0\_SLV\_CAPR2\_BI\_REG0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR2_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR2_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR2_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR2_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1486. ICSSM\_PR1\_IEP0\_SLV\_CAPR2\_BI\_REG0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR2_0 | R    | 0h    |             |

#### 4.2.2.291 ICSSM\_PR1\_IEP0\_SLV\_CAPR2\_BI\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR2\_BI\_REG1 Register (Offset = 120h) [reset = 0h]

Capture Big Indian Rise12

Return to [Summary Table](#)

**Table 4-1487. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E120h       |

**Figure 4-485. ICSSM\_PR1\_IEP0\_SLV\_CAPR2\_BI\_REG1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR2_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR2_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR2_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR2_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1489. ICSSM\_PR1\_IEP0\_SLV\_CAPR2\_BI\_REG1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR2_1 | R    | 0h    |             |

#### 4.2.2.292 ICSSM\_PR1\_IEP0\_SLV\_CAPR3\_BI\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR3\_BI\_REG0 Register (Offset = 124h) [reset = 0h]

Capture Big Indian Rise03

Return to [Summary Table](#)

**Table 4-1490. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E124h       |

**Figure 4-486. ICSSM\_PR1\_IEP0\_SLV\_CAPR3\_BI\_REG0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR3_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR3_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR3_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR3_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1492. ICSSM\_PR1\_IEP0\_SLV\_CAPR3\_BI\_REG0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR3_0 | R    | 0h    |             |

#### 4.2.2.293 ICSSM\_PR1\_IEP0\_SLV\_CAPR3\_BI\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR3\_BI\_REG1 Register (Offset = 128h) [reset = 0h]

Capture Big Indian Rise13

Return to [Summary Table](#)

**Table 4-1493. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E128h       |

**Figure 4-487. ICSSM\_PR1\_IEP0\_SLV\_CAPR3\_BI\_REG1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR3_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR3_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR3_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR3_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1495. ICSSM\_PR1\_IEP0\_SLV\_CAPR3\_BI\_REG1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR3_1 | R    | 0h    |             |

#### 4.2.2.294 ICSSM\_PR1\_IEP0\_SLV\_CAPR4\_BI\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR4\_BI\_REG0 Register (Offset = 12Ch) [reset = 0h]

Capture Big Indian Rise04

Return to [Summary Table](#)

**Table 4-1496. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E12Ch       |

**Figure 4-488. ICSSM\_PR1\_IEP0\_SLV\_CAPR4\_BI\_REG0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR4_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR4_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR4_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR4_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1498. ICSSM\_PR1\_IEP0\_SLV\_CAPR4\_BI\_REG0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR4_0 | R    | 0h    |             |

#### 4.2.2.295 ICSSM\_PR1\_IEP0\_SLV\_CAPR4\_BI\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR4\_BI\_REG1 Register (Offset = 130h) [reset = 0h]

Capture Big Indian Rise14

Return to [Summary Table](#)

**Table 4-1499. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E130h       |

**Figure 4-489. ICSSM\_PR1\_IEP0\_SLV\_CAPR4\_BI\_REG1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR4_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR4_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR4_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR4_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1501. ICSSM\_PR1\_IEP0\_SLV\_CAPR4\_BI\_REG1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR4_1 | R    | 0h    |             |

#### 4.2.2.296 ICSSM\_PR1\_IEP0\_SLV\_CAPR5\_BI\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR5\_BI\_REG0 Register (Offset = 134h) [reset = 0h]

Capture Big Indian Rise05

Return to [Summary Table](#)

**Table 4-1502. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E134h       |

**Figure 4-490. ICSSM\_PR1\_IEP0\_SLV\_CAPR5\_BI\_REG0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR5_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR5_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR5_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR5_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1504. ICSSM\_PR1\_IEP0\_SLV\_CAPR5\_BI\_REG0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR5_0 | R    | 0h    |             |



#### 4.2.2.297 ICSSM\_PR1\_IEP0\_SLV\_CAPR5\_BI\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR5\_BI\_REG1 Register (Offset = 138h) [reset = 0h]

Capture Big Indian Rise15

Return to [Summary Table](#)

**Table 4-1505. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E138h       |

**Figure 4-491. ICSSM\_PR1\_IEP0\_SLV\_CAPR5\_BI\_REG1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR5_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR5_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR5_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR5_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1507. ICSSM\_PR1\_IEP0\_SLV\_CAPR5\_BI\_REG1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR5_1 | R    | 0h    |             |

#### 4.2.2.298 ICSSM\_PR1\_IEP0\_SLV\_CAPR6\_BI\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR6\_BI\_REG0 Register (Offset = 13Ch) [reset = 0h]

Capture Big Indian Rise06

Return to [Summary Table](#)

**Table 4-1508. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E13Ch       |

**Figure 4-492. ICSSM\_PR1\_IEP0\_SLV\_CAPR6\_BI\_REG0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR6_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR6_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR6_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR6_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1510. ICSSM\_PR1\_IEP0\_SLV\_CAPR6\_BI\_REG0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR6_0 | R    | 0h    |             |

#### 4.2.2.299 ICSSM\_PR1\_IEP0\_SLV\_CAPR6\_BI\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR6\_BI\_REG1 Register (Offset = 140h) [reset = 0h]

Capture Big Indian Rise16

Return to [Summary Table](#)

**Table 4-1511. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E140h       |

**Figure 4-493. ICSSM\_PR1\_IEP0\_SLV\_CAPR6\_BI\_REG1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR6_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR6_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR6_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR6_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1513. ICSSM\_PR1\_IEP0\_SLV\_CAPR6\_BI\_REG1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR6_1 | R    | 0h    |             |

#### 4.2.2.300 ICSSM\_PR1\_IEP0\_SLV\_CAPF6\_BI\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPF6\_BI\_REG0 Register (Offset = 144h) [reset = 0h]

Capture Big Indian Fall06

Return to [Summary Table](#)

**Table 4-1514. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E144h       |

**Figure 4-494. ICSSM\_PR1\_IEP0\_SLV\_CAPF6\_BI\_REG0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPF6_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPF6_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPF6_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPF6_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1516. ICSSM\_PR1\_IEP0\_SLV\_CAPF6\_BI\_REG0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPF6_0 | R    | 0h    |             |

#### 4.2.2.301 ICSSM\_PR1\_IEP0\_SLV\_CAPF6\_BI\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPF6\_BI\_REG1 Register (Offset = 148h) [reset = 0h]

Capture Big Indian Fall16

Return to [Summary Table](#)

**Table 4-1517. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E148h       |

**Figure 4-495. ICSSM\_PR1\_IEP0\_SLV\_CAPF6\_BI\_REG1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPF6_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPF6_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPF6_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPF6_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1519. ICSSM\_PR1\_IEP0\_SLV\_CAPF6\_BI\_REG1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPF6_1 | R    | 0h    |             |

#### 4.2.2.302 ICSSM\_PR1\_IEP0\_SLV\_CAPR7\_BI\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR7\_BI\_REG0 Register (Offset = 14Ch) [reset = 0h]

Capture Big Indian Rise07

Return to [Summary Table](#)

**Table 4-1520. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E14Ch       |

**Figure 4-496. ICSSM\_PR1\_IEP0\_SLV\_CAPR7\_BI\_REG0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR7_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR7_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR7_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR7_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1522. ICSSM\_PR1\_IEP0\_SLV\_CAPR7\_BI\_REG0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR7_0 | R    | 0h    |             |

#### 4.2.2.303 ICSSM\_PR1\_IEP0\_SLV\_CAPR7\_BI\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPR7\_BI\_REG1 Register (Offset = 150h) [reset = 0h]

Capture Big Indian Rise17

Return to [Summary Table](#)

**Table 4-1523. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E150h       |

**Figure 4-497. ICSSM\_PR1\_IEP0\_SLV\_CAPR7\_BI\_REG1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPR7_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPR7_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPR7_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPR7_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1525. ICSSM\_PR1\_IEP0\_SLV\_CAPR7\_BI\_REG1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPR7_1 | R    | 0h    |             |

#### 4.2.2.304 ICSSM\_PR1\_IEP0\_SLV\_CAPF7\_BI\_REG0 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPF7\_BI\_REG0 Register (Offset = 154h) [reset = 0h]

Capture Big Indian Fall07

Return to [Summary Table](#)

**Table 4-1526. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E154h       |

**Figure 4-498. ICSSM\_PR1\_IEP0\_SLV\_CAPF7\_BI\_REG0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPF7_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPF7_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPF7_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPF7_0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1528. ICSSM\_PR1\_IEP0\_SLV\_CAPF7\_BI\_REG0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPF7_0 | R    | 0h    |             |



#### 4.2.2.305 ICSSM\_PR1\_IEP0\_SLV\_CAPF7\_BI\_REG1 Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_CAPF7\_BI\_REG1 Register (Offset = 158h) [reset = 0h]

Capture Big Indian Fall17

Return to [Summary Table](#)

**Table 4-1529. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E158h       |

**Figure 4-499. ICSSM\_PR1\_IEP0\_SLV\_CAPF7\_BI\_REG1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAPF7_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAPF7_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAPF7_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAPF7_1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1531. ICSSM\_PR1\_IEP0\_SLV\_CAPF7\_BI\_REG1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | CAPF7_1 | R    | 0h    |             |

#### 4.2.2.306 ICSSM\_PR1\_IEP0\_SLV\_SYNC\_CTRL\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_SYNC\_CTRL\_REG Register (Offset = 180h) [reset = 0h]

Sync Ctrl

Return to [Summary Table](#)

**Table 4-1532. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E180h       |

**Figure 4-500. ICSSM\_PR1\_IEP0\_SLV\_SYNC\_CTRL\_REG Name Register**

|                 |              |                 |              |          |                 |                 |              |
|-----------------|--------------|-----------------|--------------|----------|-----------------|-----------------|--------------|
| 31              | 30           | 29              | 28           | 27       | 26              | 25              | 24           |
| RESERVED        |              |                 |              |          |                 |                 |              |
| NONE            |              |                 |              |          |                 |                 |              |
| 0h              |              |                 |              |          |                 |                 |              |
| 23              | 22           | 21              | 20           | 19       | 18              | 17              | 16           |
| RESERVED        |              |                 |              |          |                 |                 |              |
| NONE            |              |                 |              |          |                 |                 |              |
| 0h              |              |                 |              |          |                 |                 |              |
| 15              | 14           | 13              | 12           | 11       | 10              | 9               | 8            |
| RESERVED        |              |                 |              |          | SYNC1_OUT_NV_EN | SYNC0_OUT_NV_EN | SYNC1_IND_EN |
| NONE            |              |                 |              |          | R/W             | R/W             | R/W          |
| 0h              |              |                 |              |          | 0h              | 0h              | 0h           |
| 7               | 6            | 5               | 4            | 3        | 2               | 1               | 0            |
| SYNC1_CYCLIC_EN | SYNC1_ACK_EN | SYNC0_CYCLIC_EN | SYNC0_ACK_EN | RESERVED | SYNC1_EN        | SYNC0_EN        | SYNC_EN      |
| R/W             | R/W          | R/W             | R/W          | NONE     | R/W             | R/W             | R/W          |
| 0h              | 0h           | 0h              | 0h           | 0h       | 0h              | 0h              | 0h           |

**Table 4-1534. ICSSM\_PR1\_IEP0\_SLV\_SYNC\_CTRL\_REG Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description |
|-------|-----------------|------|-------|-------------|
| 31:11 | RESERVED        | NONE | 0h    | Reserved    |
| 10    | SYNC1_OUT_NV_EN | R/W  | 0h    |             |
| 9     | SYNC0_OUT_NV_EN | R/W  | 0h    |             |
| 8     | SYNC1_IND_EN    | R/W  | 0h    |             |
| 7     | SYNC1_CYCLIC_EN | R/W  | 0h    |             |
| 6     | SYNC1_ACK_EN    | R/W  | 0h    |             |
| 5     | SYNC0_CYCLIC_EN | R/W  | 0h    |             |
| 4     | SYNC0_ACK_EN    | R/W  | 0h    |             |
| 3     | RESERVED        | NONE | 0h    | Reserved    |
| 2     | SYNC1_EN        | R/W  | 0h    |             |
| 1     | SYNC0_EN        | R/W  | 0h    |             |
| 0     | SYNC_EN         | R/W  | 0h    |             |

#### 4.2.2.307 ICSSM\_PR1\_IEP0\_SLV\_SYNC\_FIRST\_STAT\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_SYNC\_FIRST\_STAT\_REG Register (Offset = 184h) [reset = 0h]

Sync Ctrl

Return to [Summary Table](#)

**Table 4-1535. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E184h       |

**Figure 4-501. ICSSM\_PR1\_IEP0\_SLV\_SYNC\_FIRST\_STAT\_REG Name Register**

|          |    |    |    |    |    |             |             |
|----------|----|----|----|----|----|-------------|-------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25          | 24          |
| RESERVED |    |    |    |    |    |             |             |
| NONE     |    |    |    |    |    |             |             |
| 0h       |    |    |    |    |    |             |             |
| 23       | 22 | 21 | 20 | 19 | 18 | 17          | 16          |
| RESERVED |    |    |    |    |    |             |             |
| NONE     |    |    |    |    |    |             |             |
| 0h       |    |    |    |    |    |             |             |
| 15       | 14 | 13 | 12 | 11 | 10 | 9           | 8           |
| RESERVED |    |    |    |    |    |             |             |
| NONE     |    |    |    |    |    |             |             |
| 0h       |    |    |    |    |    |             |             |
| 7        | 6  | 5  | 4  | 3  | 2  | 1           | 0           |
| RESERVED |    |    |    |    |    | FIRST_SYNC1 | FIRST_SYNC0 |
| NONE     |    |    |    |    |    | R           | R           |
| 0h       |    |    |    |    |    | 0h          | 0h          |

**Table 4-1537. ICSSM\_PR1\_IEP0\_SLV\_SYNC\_FIRST\_STAT\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description |
|------|-------------|------|-------|-------------|
| 31:2 | RESERVED    | NONE | 0h    | Reserved    |
| 1    | FIRST_SYNC1 | R    | 0h    |             |
| 0    | FIRST_SYNC0 | R    | 0h    |             |

#### 4.2.2.308 ICSSM\_PR1\_IEP0\_SLV\_SYNC0\_STAT\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_SYNC0\_STAT\_REG Register (Offset = 188h) [reset = 0h]

Sync Ctrl

Return to [Summary Table](#)

**Table 4-1538. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E188h       |

**Figure 4-502. ICSSM\_PR1\_IEP0\_SLV\_SYNC0\_STAT\_REG Name Register**

|          |    |    |    |    |    |    |            |
|----------|----|----|----|----|----|----|------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24         |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16         |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8          |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0          |
| RESERVED |    |    |    |    |    |    | SYNC0_PEND |
| NONE     |    |    |    |    |    |    | R          |
| 0h       |    |    |    |    |    |    | 0h         |

**Table 4-1540. ICSSM\_PR1\_IEP0\_SLV\_SYNC0\_STAT\_REG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description |
|------|------------|------|-------|-------------|
| 31:1 | RESERVED   | NONE | 0h    | Reserved    |
| 0    | SYNC0_PEND | R    | 0h    |             |

#### 4.2.2.309 ICSSM\_PR1\_IEP0\_SLV\_SYNC1\_STAT\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_SYNC1\_STAT\_REG Register (Offset = 18Ch) [reset = 0h]

Sync Ctrl

Return to [Summary Table](#)

**Table 4-1541. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E18Ch       |

**Figure 4-503. ICSSM\_PR1\_IEP0\_SLV\_SYNC1\_STAT\_REG Name Register**

|          |    |    |    |    |    |    |            |
|----------|----|----|----|----|----|----|------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24         |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16         |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8          |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0          |
| RESERVED |    |    |    |    |    |    | SYNC1_PEND |
| NONE     |    |    |    |    |    |    | R          |
| 0h       |    |    |    |    |    |    | 0h         |

**Table 4-1543. ICSSM\_PR1\_IEP0\_SLV\_SYNC1\_STAT\_REG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description |
|------|------------|------|-------|-------------|
| 31:1 | RESERVED   | NONE | 0h    | Reserved    |
| 0    | SYNC1_PEND | R    | 0h    |             |

#### 4.2.2.310 ICSSM\_PR1\_IEP0\_SLV\_SYNC\_PWIDTH\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_SYNC\_PWIDTH\_REG Register (Offset = 190h) [reset = 0h]

Sync Ctrl

Return to [Summary Table](#)

**Table 4-1544. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E190h       |

**Figure 4-504. ICSSM\_PR1\_IEP0\_SLV\_SYNC\_PWIDTH\_REG Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SYNC_HPW |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SYNC_HPW |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SYNC_HPW |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SYNC_HPW |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1546. ICSSM\_PR1\_IEP0\_SLV\_SYNC\_PWIDTH\_REG Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | SYNC_HPW | R/W  | 0h    |             |

#### 4.2.2.311 ICSSM\_PR1\_IEP0\_SLV\_SYNC0\_PERIOD\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_SYNC0\_PERIOD\_REG Register (Offset = 194h) [reset = 1h]

Sync Ctrl

Return to [Summary Table](#)

**Table 4-1547. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E194h       |

**Figure 4-505. ICSSM\_PR1\_IEP0\_SLV\_SYNC0\_PERIOD\_REG Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SYNC0_PERIOD |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 1h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SYNC0_PERIOD |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 1h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SYNC0_PERIOD |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 1h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SYNC0_PERIOD |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 1h           |    |    |    |    |    |    |    |

**Table 4-1549. ICSSM\_PR1\_IEP0\_SLV\_SYNC0\_PERIOD\_REG Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description |
|------|--------------|------|-------|-------------|
| 31:0 | SYNC0_PERIOD | R/W  | 1h    |             |

#### 4.2.2.312 ICSSM\_PR1\_IEP0\_SLV\_SYNC1\_DELAY\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_SYNC1\_DELAY\_REG Register (Offset = 198h) [reset = 0h]

Sync Ctrl

Return to [Summary Table](#)

**Table 4-1550. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E198h       |

**Figure 4-506. ICSSM\_PR1\_IEP0\_SLV\_SYNC1\_DELAY\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SYNC1_DELAY |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SYNC1_DELAY |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SYNC1_DELAY |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SYNC1_DELAY |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 4-1552. ICSSM\_PR1\_IEP0\_SLV\_SYNC1\_DELAY\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description |
|------|-------------|------|-------|-------------|
| 31:0 | SYNC1_DELAY | R/W  | 0h    |             |



#### 4.2.2.313 ICSSM\_PR1\_IEP0\_SLV\_SYNC\_START\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_SYNC\_START\_REG Register (Offset = 19Ch) [reset = 0h]

Sync Ctrl

Return to [Summary Table](#)

**Table 4-1553. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E19Ch       |

**Figure 4-507. ICSSM\_PR1\_IEP0\_SLV\_SYNC\_START\_REG Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SYNC_START |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SYNC_START |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SYNC_START |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SYNC_START |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 4-1555. ICSSM\_PR1\_IEP0\_SLV\_SYNC\_START\_REG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description |
|------|------------|------|-------|-------------|
| 31:0 | SYNC_START | R/W  | 0h    |             |

#### 4.2.2.314 ICSSM\_PR1\_IEP0\_SLV\_WD\_PREDIV\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_WD\_PREDIV\_REG Register (Offset = 200h) [reset = 4E20h]

WD

Return to [Summary Table](#)
**Table 4-1556. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E200h       |

**Figure 4-508. ICSSM\_PR1\_IEP0\_SLV\_WD\_PREDIV\_REG Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PRE_DIV  |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 4E20h    |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PRE_DIV  |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 4E20h    |    |    |    |    |    |    |    |

**Table 4-1558. ICSSM\_PR1\_IEP0\_SLV\_WD\_PREDIV\_REG Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description |
|-------|----------|------|-------|-------------|
| 31:16 | RESERVED | NONE | 0h    | Reserved    |
| 15:0  | PRE_DIV  | R/W  | 4E20h |             |

#### 4.2.2.315 ICSSM\_PR1\_IEP0\_SLV\_PDI\_WD\_TIM\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_PDI\_WD\_TIM\_REG Register (Offset = 204h) [reset = 3E8h]

WD

Return to [Summary Table](#)
**Table 4-1559. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E204h       |

**Figure 4-509. ICSSM\_PR1\_IEP0\_SLV\_PDI\_WD\_TIM\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PDI_WD_TIME |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 3E8h        |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PDI_WD_TIME |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 3E8h        |    |    |    |    |    |    |    |

**Table 4-1561. ICSSM\_PR1\_IEP0\_SLV\_PDI\_WD\_TIM\_REG Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description |
|-------|-------------|------|-------|-------------|
| 31:16 | RESERVED    | NONE | 0h    | Reserved    |
| 15:0  | PDI_WD_TIME | R/W  | 3E8h  |             |

#### 4.2.2.316 ICSSM\_PR1\_IEP0\_SLV\_PD\_WD\_TIM\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_PD\_WD\_TIM\_REG Register (Offset = 208h) [reset = 3E8h]

WD

Return to [Summary Table](#)

**Table 4-1562. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E208h       |

**Figure 4-510. ICSSM\_PR1\_IEP0\_SLV\_PD\_WD\_TIM\_REG Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PD_WD_TIME |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 3E8h       |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PD_WD_TIME |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 3E8h       |    |    |    |    |    |    |    |

**Table 4-1564. ICSSM\_PR1\_IEP0\_SLV\_PD\_WD\_TIM\_REG Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description |
|-------|------------|------|-------|-------------|
| 31:16 | RESERVED   | NONE | 0h    | Reserved    |
| 15:0  | PD_WD_TIME | R/W  | 3E8h  |             |

#### 4.2.2.317 ICSSM\_PR1\_IEP0\_SLV\_WD\_STATUS\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_WD\_STATUS\_REG Register (Offset = 20Ch) [reset = 10001h]

WD

Return to [Summary Table](#)
**Table 4-1565. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E20Ch       |

**Figure 4-511. ICSSM\_PR1\_IEP0\_SLV\_WD\_STATUS\_REG Name Register**

|          |    |    |    |    |    |    |             |
|----------|----|----|----|----|----|----|-------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24          |
| RESERVED |    |    |    |    |    |    |             |
| NONE     |    |    |    |    |    |    |             |
| 0h       |    |    |    |    |    |    |             |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16          |
| RESERVED |    |    |    |    |    |    | PDI_WD_STAT |
| NONE     |    |    |    |    |    |    | R           |
| 0h       |    |    |    |    |    |    | 1h          |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8           |
| RESERVED |    |    |    |    |    |    |             |
| NONE     |    |    |    |    |    |    |             |
| 0h       |    |    |    |    |    |    |             |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0           |
| RESERVED |    |    |    |    |    |    | PD_WD_STAT  |
| NONE     |    |    |    |    |    |    | R           |
| 0h       |    |    |    |    |    |    | 1h          |

**Table 4-1567. ICSSM\_PR1\_IEP0\_SLV\_WD\_STATUS\_REG Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description |
|-------|-------------|------|-------|-------------|
| 31:17 | RESERVED    | NONE | 0h    | Reserved    |
| 16    | PDI_WD_STAT | R    | 1h    |             |
| 15:1  | RESERVED    | NONE | 0h    | Reserved    |
| 0     | PD_WD_STAT  | R    | 1h    |             |

#### 4.2.2.318 ICSSM\_PR1\_IEP0\_SLV\_WD\_EXP\_CNT\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_WD\_EXP\_CNT\_REG Register (Offset = 210h) [reset = 0h]

WD

Return to [Summary Table](#)

**Table 4-1568. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E210h       |

**Figure 4-512. ICSSM\_PR1\_IEP0\_SLV\_WD\_EXP\_CNT\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PD_EXP_CNT  |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PDI_EXP_CNT |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 4-1570. ICSSM\_PR1\_IEP0\_SLV\_WD\_EXP\_CNT\_REG Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description |
|-------|-------------|------|-------|-------------|
| 31:16 | RESERVED    | NONE | 0h    | Reserved    |
| 15:8  | PD_EXP_CNT  | R/W  | 0h    |             |
| 7:0   | PDI_EXP_CNT | R/W  | 0h    |             |

#### 4.2.2.319 ICSSM\_PR1\_IEP0\_SLV\_WD\_CTRL\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_WD\_CTRL\_REG Register (Offset = 214h) [reset = 0h]

WD

Return to [Summary Table](#)

**Table 4-1571. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E214h       |

**Figure 4-513. ICSSM\_PR1\_IEP0\_SLV\_WD\_CTRL\_REG Name Register**

|          |    |    |    |    |    |    |           |
|----------|----|----|----|----|----|----|-----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24        |
| RESERVED |    |    |    |    |    |    |           |
| NONE     |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16        |
| RESERVED |    |    |    |    |    |    | PDI_WD_EN |
| NONE     |    |    |    |    |    |    | R/W       |
| 0h       |    |    |    |    |    |    | 0h        |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8         |
| RESERVED |    |    |    |    |    |    |           |
| NONE     |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0         |
| RESERVED |    |    |    |    |    |    | PD_WD_EN  |
| NONE     |    |    |    |    |    |    | R/W       |
| 0h       |    |    |    |    |    |    | 0h        |

**Table 4-1573. ICSSM\_PR1\_IEP0\_SLV\_WD\_CTRL\_REG Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description |
|-------|-----------|------|-------|-------------|
| 31:17 | RESERVED  | NONE | 0h    | Reserved    |
| 16    | PDI_WD_EN | R/W  | 0h    |             |
| 15:1  | RESERVED  | NONE | 0h    | Reserved    |
| 0     | PD_WD_EN  | R/W  | 0h    |             |

#### 4.2.2.320 ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_CTRL\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_CTRL\_REG Register (Offset = 300h) [reset = 4h]

DIGIO

Return to [Summary Table](#)
**Table 4-1574. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E300h       |

**Figure 4-514. ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_CTRL\_REG Name Register**

|          |    |         |    |         |           |               |              |
|----------|----|---------|----|---------|-----------|---------------|--------------|
| 31       | 30 | 29      | 28 | 27      | 26        | 25            | 24           |
| RESERVED |    |         |    |         |           |               |              |
| NONE     |    |         |    |         |           |               |              |
| 0h       |    |         |    |         |           |               |              |
| 23       | 22 | 21      | 20 | 19      | 18        | 17            | 16           |
| RESERVED |    |         |    |         |           |               |              |
| NONE     |    |         |    |         |           |               |              |
| 0h       |    |         |    |         |           |               |              |
| 15       | 14 | 13      | 12 | 11      | 10        | 9             | 8            |
| RESERVED |    |         |    |         |           |               |              |
| NONE     |    |         |    |         |           |               |              |
| 0h       |    |         |    |         |           |               |              |
| 7        | 6  | 5       | 4  | 3       | 2         | 1             | 0            |
| OUT_MODE |    | IN_MODE |    | WD_MODE | BIDI_MODE | OUTVALID_MODE | OUTVALID_POL |
| R/W      |    | R/W     |    | R/W     | R         | R/W           | R            |
| 0h       |    | 0h      |    | 0h      | 1h        | 0h            | 0h           |

**Table 4-1576. ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_CTRL\_REG Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description |
|------|---------------|------|-------|-------------|
| 31:8 | RESERVED      | NONE | 0h    | Reserved    |
| 7:6  | OUT_MODE      | R/W  | 0h    |             |
| 5:4  | IN_MODE       | R/W  | 0h    |             |
| 3    | WD_MODE       | R/W  | 0h    |             |
| 2    | BIDI_MODE     | R    | 1h    |             |
| 1    | OUTVALID_MODE | R/W  | 0h    |             |
| 0    | OUTVALID_POL  | R    | 0h    |             |



#### 4.2.2.321 ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_STATUS\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_STATUS\_REG Register (Offset = 304h) [reset = 0h]

DIGIO

Return to [Summary Table](#)

**Table 4-1577. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E304h       |

**Figure 4-515. ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_STATUS\_REG Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DIGIO_STAT |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DIGIO_STAT |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DIGIO_STAT |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DIGIO_STAT |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 4-1579. ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_STATUS\_REG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description |
|------|------------|------|-------|-------------|
| 31:0 | DIGIO_STAT | R    | 0h    |             |

#### 4.2.2.322 ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_DATA\_IN\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_DATA\_IN\_REG Register (Offset = 308h) [reset = 0h]

DIGIO

Return to [Summary Table](#)

**Table 4-1580. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E308h       |

**Figure 4-516. ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_DATA\_IN\_REG Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DATA_IN |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DATA_IN |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DATA_IN |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DATA_IN |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1582. ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_DATA\_IN\_REG Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description |
|------|---------|------|-------|-------------|
| 31:0 | DATA_IN | R    | 0h    |             |

#### 4.2.2.323 ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_DATA\_IN\_RAW\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_DATA\_IN\_RAW\_REG Register (Offset = 30Ch) [reset = 0h]

DIGIO

Return to [Summary Table](#)

**Table 4-1583. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E30Ch       |

**Figure 4-517. ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_DATA\_IN\_RAW\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DATA_IN_RAW |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DATA_IN_RAW |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DATA_IN_RAW |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DATA_IN_RAW |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 4-1585. ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_DATA\_IN\_RAW\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description |
|------|-------------|------|-------|-------------|
| 31:0 | DATA_IN_RAW | R    | 0h    |             |

#### 4.2.2.324 ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_DATA\_OUT\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_DATA\_OUT\_REG Register (Offset = 310h) [reset = 0h]

DIGIO

Return to [Summary Table](#)

**Table 4-1586. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E310h       |

**Figure 4-518. ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_DATA\_OUT\_REG Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DATA_OUT |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DATA_OUT |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DATA_OUT |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DATA_OUT |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1588. ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_DATA\_OUT\_REG Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | DATA_OUT | R/W  | 0h    |             |

#### 4.2.2.325 ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_DATA\_OUT\_EN\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_DATA\_OUT\_EN\_REG Register (Offset = 314h) [reset = 0h]

DIGIO

Return to [Summary Table](#)

**Table 4-1589. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E314h       |

**Figure 4-519. ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_DATA\_OUT\_EN\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DATA_OUT_EN |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DATA_OUT_EN |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DATA_OUT_EN |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DATA_OUT_EN |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 4-1591. ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_DATA\_OUT\_EN\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description |
|------|-------------|------|-------|-------------|
| 31:0 | DATA_OUT_EN | R/W  | 0h    |             |

#### 4.2.2.326 ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_EXP\_REG Register

##### 1 ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_EXP\_REG Register (Offset = 318h) [reset = 20h]

DIGIO

Return to [Summary Table](#)
**Table 4-1592. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4802 E318h       |

**Figure 4-520. ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_EXP\_REG Name Register**

|              |    |         |         |          |             |                 |                |
|--------------|----|---------|---------|----------|-------------|-----------------|----------------|
| 31           | 30 | 29      | 28      | 27       | 26          | 25              | 24             |
| RESERVED     |    |         |         |          |             |                 |                |
| NONE         |    |         |         |          |             |                 |                |
| 0h           |    |         |         |          |             |                 |                |
| 23           | 22 | 21      | 20      | 19       | 18          | 17              | 16             |
| RESERVED     |    |         |         |          |             |                 |                |
| NONE         |    |         |         |          |             |                 |                |
| 0h           |    |         |         |          |             |                 |                |
| 15           | 14 | 13      | 12      | 11       | 10          | 9               | 8              |
| RESERVED     |    | EOF_SEL | SOF_SEL | SOF_DLY  |             |                 |                |
| NONE         |    | R/W     | R/W     | R/W      |             |                 |                |
| 0h           |    | 0h      | 0h      | 0h       |             |                 |                |
| 7            | 6  | 5       | 4       | 3        | 2           | 1               | 0              |
| OUTVALID_DLY |    |         |         | RESERVED | SW_OUTVALID | OUTVALID_OVR_EN | SW_DATA_OUT_UP |
| R/W          |    |         |         | NONE     | R/W         | R/W             | R/W            |
| 2h           |    |         |         | 0h       | 0h          | 0h              | 0h             |

**Table 4-1594. ICSSM\_PR1\_IEP0\_SLV\_DIGIO\_EXP\_REG Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description |
|-------|-----------------|------|-------|-------------|
| 31:14 | RESERVED        | NONE | 0h    | Reserved    |
| 13    | EOF_SEL         | R/W  | 0h    |             |
| 12    | SOF_SEL         | R/W  | 0h    |             |
| 11:8  | SOF_DLY         | R/W  | 0h    |             |
| 7:4   | OUTVALID_DLY    | R/W  | 2h    |             |
| 3     | RESERVED        | NONE | 0h    | Reserved    |
| 2     | SW_OUTVALID     | R/W  | 0h    |             |
| 1     | OUTVALID_OVR_EN | R/W  | 0h    |             |
| 0     | SW_DATA_OUT_UP  | R/W  | 0h    |             |

#### 4.2.2.327 ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_TSCNT Register

##### 1 ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_TSCNT Register (Offset = 0h) [reset = 0h]

TIME STAMP COUNTER REGISTER.

Return to [Summary Table](#)

**Table 4-1595. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 0000h       |

**Figure 4-521. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_TSCNT Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TSCNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TSCNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TSCNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TSCNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-1597. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_TSCNT Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                            |
|------|-------|------|-------|------------------------------------------------------------------------|
| 31:0 | TSCNT | R/W  | 0h    | Active 32-bit counter register which is used as the Capture time-base. |

#### 4.2.2.328 ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_CNTPHS Register

##### 1 ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_CNTPHS Register (Offset = 4h) [reset = 0h]

COUNTER PHASE CONTROL REGISTER.

Return to [Summary Table](#)

**Table 4-1598. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 0004h       |

**Figure 4-522. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_CNTPHS Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CNTPHS |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CNTPHS |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CNTPHS |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CNTPHS |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 4-1600. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_CNTPHS Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                    |
|------|--------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CNTPHS | R/W  | 0h    | Counter phase value register that can be programmed for phase Lag/Lead.<br>This register shadows the TSCNT register and is loaded into the TSCNT register upon either a SYNCI event or software force via a control bit.<br>Used to achieve phase control sync with respect to other ECAP and EPWM time-bases. |



#### 4.2.2.329 ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_CAP1 Register

##### 1 ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_CAP1 Register (Offset = 8h) [reset = 0h]

CAPTURE-1 REGISTER.

Return to [Summary Table](#)

**Table 4-1601. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 0008h       |

**Figure 4-523. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_CAP1 Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAP1 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAP1 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAP1 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAP1 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 4-1603. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_CAP1 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                   |
|------|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CAP1  | R/W  | 0h    | This register can be loaded (written) by:<br>1. Time-Stamp (counter value) during a capture event.<br>2. Software - may be useful for test purposes/initialization.<br>3. APRD shadow register (CAP3) when used in APWM mode. |

#### 4.2.2.330 ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_CAP2 Register

##### 1 ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_CAP2 Register (Offset = Ch) [reset = 0h]

CAPTURE-2 REGISTER.

Return to [Summary Table](#)

**Table 4-1604. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 000Ch       |

**Figure 4-524. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_CAP2 Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAP2 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAP2 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAP2 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAP2 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 4-1606. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_CAP2 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                    |
|------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CAP2  | R/W  | 0h    | This register can be loaded (written) by:<br>1. Time-Stamp (counter value) during a capture event.<br>2. Software - may be useful for test purposes.<br>3. ACMP shadow register (CAP4) when used in APWM mode. |

#### 4.2.2.331 ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_CAP3 Register

##### 1 ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_CAP3 Register (Offset = 10h) [reset = 0h]

CAPTURE-3 REGISTER.

Return to [Summary Table](#)

**Table 4-1607. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 0010h       |

**Figure 4-525. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_CAP3 Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAP3 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAP3 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAP3 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAP3 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 4-1609. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_CAP3 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                               |
|------|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CAP3  | R/W  | 0h    | In CMP mode this is a time-stamp capture register.<br>In APMW mode this is the period shadow (APER) register.<br>User updates the PWM period value via this register.<br>In this mode the CAP3 (APRD) register shadows the CAP1 register. |

#### 4.2.2.332 ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_CAP4 Register

##### 1 ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_CAP4 Register (Offset = 14h) [reset = 0h]

CAPTURE-4 REGISTER.

Return to [Summary Table](#)

**Table 4-1610. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 0014h       |

**Figure 4-526. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_CAP4 Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAP4 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAP4 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAP4 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAP4 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 4-1612. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_CAP4 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                 |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CAP4  | R/W  | 0h    | In CMP mode this is a time-stamp capture register.<br>In APMW mode this is the compare shadow (ACMP) register.<br>User updates the PWM Compare value via this register.<br>In this mode the CAP4 (ACMP) register shadows the CAP2 register. |

#### 4.2.2.333 ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_ECCTL2\_ECCTL1 Register

#### 1 ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_ECCTL2\_ECCTL1 Register (Offset = 28h) [reset = 60000h]

##### ECAP CONTROL REGISTER 1

Return to [Summary Table](#)

**Table 4-1613. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 0028h       |

**Figure 4-527. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_ECCTL2\_ECCTL1 Name Register**

| 31        | 30      | 29       | 28       | 27              | 26        | 25       | 24              |
|-----------|---------|----------|----------|-----------------|-----------|----------|-----------------|
| FILTER    |         |          |          |                 | APWMPOL   | CAP_APWM | SWSYNC          |
| R         |         |          |          |                 | R/W       | R/W      | R/W             |
| 0h        |         |          |          |                 | 0h        | 0h       | 0h              |
| 23        | 22      | 21       | 20       | 19              | 18        | 17       | 16              |
| SYNCO_SEL |         | SYNCl_EN | TSCNTSTP | REARM_RESE<br>T | STOPVALUE |          | CONT_ONESH<br>T |
| R/W       |         | R/W      | R/W      | R/W             | R/W       |          | R/W             |
| 0h        |         | 0h       | 0h       | 0h              | 3h        |          | 0h              |
| 15        | 14      | 13       | 12       | 11              | 10        | 9        | 8               |
| FREE      | SOFT    | EVTFLTPS |          |                 |           |          | CAPLDEN         |
| R/W       | R/W     | R/W      |          |                 |           |          | R/W             |
| 0h        | 0h      | 0h       |          |                 |           |          | 0h              |
| 7         | 6       | 5        | 4        | 3               | 2         | 1        | 0               |
| CTRRST4   | CAP4POL | CTRRST3  | CAP3POL  | CTRRST2         | CAP2POL   | CTRRST1  | CAP1POL         |
| R/W       | R/W     | R/W      | R/W      | R/W             | R/W       | R/W      | R/W             |
| 0h        | 0h      | 0h       | 0h       | 0h              | 0h        | 0h       | 0h              |

**Table 4-1615. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_ECCTL2\_ECCTL1 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:27 | FILTER   | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 26    | APWMPOL  | R/W  | 0h    | APWM Output Polarity Select:<br>Note: This is applicable only in APWM operating mode.<br>0 Output is Active High (Compare value defines High time)<br>1 Output is Active Low (Compare value defines Low time)                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 25    | CAP_APWM | R/W  | 0h    | CAP/APWM Operating Mode Select:<br>0 ECAP module operates in Capture mode. This mode forces the following configuration:1. Inhibits the TSCNT register resets via PRD event.2. Inhibits the Shadow loads on the CAP1 and CAP2 registers.3. Permits user to enable the CAP1 to CAP4 register load.4. CAPx/APWMx pin operates as a Capture input.<br>1 ECAP module operates in APWM mode. This mode forces the following configuration:1. Resets the TSCNT register on PRD event (period boundary)2. Permits Shadow loading on the CAP1 and CAP2 registers.3. Disables loading of Time-stamps into the CAP1 - CAP4 registers4. CAPx/APWMx pin operates as a APWM output. |

**Table 4-1615. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_ECCTL2\_ECCTL1 Register Field Descriptions  
(continued)**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|-------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24    | SWSYNC      | R/W  | 0h    | Software Forced Counter (TSCNT) Synchronizing:<br>Note: This provides a convenient software method to synchronize some or all ECAP timebases in APWM mode. The Syncing can also be done via the PRD_EQ Event.<br><br>0      writing a zero has no effect. Reading will always return a zero.<br>1      Writing a one will force a TSCNT shadow load of current ECAP module and any ECAP modules down-stream providing the SYNCO_SEL bits are 0h. After writing a 1, this bit returns to a 0.                                                                                                                                                             |
| 23:22 | SYNCO_SEL   | R/W  | 0h    | SyncOut Select:<br>Note: Selection PRD is meaningful only in APWM mode, however can still be chosen in CAP mode if user believes it to be useful.<br><br>0      Select SyncIn event to be the SyncOut signal (pass through)<br>1      Select PRD event to be the SyncOut signal<br>2      Disable SyncOut Signal<br>3      Disable SyncOut Signal                                                                                                                                                                                                                                                                                                        |
| 21    | SYNCI_EN    | R/W  | 0h    | Counter (TSCNT) SyncIn select mode:<br><br>0      Disable SyncIn option<br>1      Enable Counter (TSCNT) to be loaded from the CNTPHS register upon either a SYNCI signal or a software force event.                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 20    | TSCNTSTP    | R/W  | 0h    | Counter Stop (freeze) Control:<br><br>0      Counter Stopped<br>1      Counter Free Running                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 19    | REARM_RESET | R/W  | 0h    | One-Shot Re-arming Control Wait for stop trigger:<br><br>0      Has no effect. Reading always returns a 0h<br>1      Arms the One-Shot sequence:1. Resets the Mod4 counter to zero.2. Un-freezes the Mod4 counter.3. Enables Capture Register Loads.                                                                                                                                                                                                                                                                                                                                                                                                     |
| 18:17 | STOPVALUE   | R/W  | 3h    | Stop Value for One-Shot Mode:<br>This is the number (between 1 and 4) of captures allowed to occur before the CAP1 through CAP4 registers are frozen (capture sequence is stopped).<br>Notes:<br>[1] STOPVALUE is compared to Mod4 counter, when equal, two actions occur:<br>1. Mod4 Counter is stopped (frozen)<br>2. Capture register loads are inhibited<br>[2] In one shot mode, further interrupt events are blocked until we re-arm, once the number of events captured has been reached.<br><br>0      Stop after Capture Event 1<br>1      Stop after Capture Event 2<br>2      Stop after Capture Event 3<br>3      Stop after Capture Event 4 |
| 16    | CONT_ONESHT | R/W  | 0h    | Continuous or One-shot Mode Control (applicable only in Capture mode):<br><br>0      Operate in Continuous mode<br>1      Operate in One-Shot mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 15    | FREE        | R/W  | 0h    | Emulation Control<br><br>0      TSCNT Counter stops immediately on emulation suspend<br>1      TSCNT Counter runs until = 0h<br>3      TSCNT Counter is unaffected by emulation suspend (Run Free)                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

**Table 4-1615. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_ECCTL2\_ECCTL1 Register Field Descriptions  
(continued)**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                   |
|------|-----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14   | SOFT      | R/W  | 0h    | Emulation Control<br>0 TSCNT Counter stops immediately on emulation suspend<br>1 TSCNT Counter runs until = 0h<br>3 TSCNT Counter is unaffected by emulation suspend (Run Free)                                               |
| 13:9 | EVTFLTPTS | R/W  | 0h    | Event Filter Prescale Select:<br>00h Divide by 1 (no prescale, by-pass the prescaler)<br>01h Divide by 2<br>02h Divide by 4<br>03h Divide by 6<br>04h Divide by 8<br>05h Divide by 10<br>1Eh Divide by 60<br>1Fh Divide by 62 |
| 8    | CAPLDEN   | R/W  | 0h    | Enable Loading of the CAP1 to CAP4 registers on a capture event:<br>0 Disable CAP1 to CAP4 register loads at capture event time.<br>1 Enable CAP1 to CAP4 register loads at capture event time.                               |
| 7    | CTRRST4   | R/W  | 0h    | Counter Reset on Capture Event 4:<br>0 Do Not reset Counter on Capture Event 4 (absolute time stamp)<br>1 Reset counter after Event 4 time-stamp has been captured (used in Difference mode operation)                        |
| 6    | CAP4POL   | R/W  | 0h    | Capture Event 4 Polarity Select:<br>0 Capture event 4 triggered on a Rising Edge (RE)<br>1 Capture event 4 triggered on a Falling Edge (FE)                                                                                   |
| 5    | CTRRST3   | R/W  | 0h    | Counter Reset on Capture Event 3:<br>0 Do not reset counter on Capture Event 3 (absolute time stamp)<br>1 Reset counter after Event 3 time-stamp has been captured (used in difference mode operation)                        |
| 4    | CAP3POL   | R/W  | 0h    | Capture Event 3 Polarity Select:<br>0 Capture event 3 triggered on a Rising Edge (RE)<br>1 Capture event 3 triggered on a Falling Edge (FE)                                                                                   |
| 3    | CTRRST2   | R/W  | 0h    | Counter Reset on Capture Event 2:<br>0 Do not reset counter on Capture Event 2 (absolute time stamp)<br>1 Reset Counter after Event 2 time-stamp has been captured (used in difference mode operation)                        |
| 2    | CAP2POL   | R/W  | 0h    | Capture Event 2 Polarity Select:<br>0 Capture event 2 triggered on a Rising Edge (RE)<br>1 Capture event 2 triggered on a Falling Edge (FE)                                                                                   |

**Table 4-1615. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_ECCTL2\_ECCTL1 Register Field Descriptions  
(continued)**

| Bit | Field   | Type | Reset | Description                                                                                                                                                                                            |
|-----|---------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | CTRRST1 | R/W  | 0h    | Counter Reset on Capture Event 1:<br>0 Do not reset counter on Capture Event 1 (absolute time stamp)<br>1 Reset counter after Event 1 time-stamp has been captured (used in difference mode operation) |
| 0   | CAP1POL | R/W  | 0h    | Capture Event 1 Polarity Select:<br>0 Capture event 1 triggered on a Rising Edge (RE)<br>1 Capture event 1 triggered on a Falling Edge (FE)                                                            |



#### 4.2.2.334 ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_ECFLG\_ECEINT Register

##### 1 ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_ECFLG\_ECEINT Register (Offset = 2Ch) [reset = 0h]

ECAP INTERRUPT ENABLE REGISTER.

Return to [Summary Table](#)

**Table 4-1616. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 002Ch       |

**Figure 4-528. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_ECFLG\_ECEINT Name Register**

|            |            |             |           |           |           |           |          |
|------------|------------|-------------|-----------|-----------|-----------|-----------|----------|
| 31         | 30         | 29          | 28        | 27        | 26        | 25        | 24       |
| FLAG_RESV0 |            |             |           |           |           |           |          |
| R          |            |             |           |           |           |           |          |
| 0h         |            |             |           |           |           |           |          |
| 23         | 22         | 21          | 20        | 19        | 18        | 17        | 16       |
| FLAG_CMPEQ | FLAG_PRDEQ | FLAG_CNTOVF | FLAG_CEV4 | FLAG_CEV3 | FLAG_CEV2 | FLAG_CEV1 | FLAG_INT |
| R          | R          | R           | R         | R         | R         | R         | R        |
| 0h         | 0h         | 0h          | 0h        | 0h        | 0h        | 0h        | 0h       |
| 15         | 14         | 13          | 12        | 11        | 10        | 9         | 8        |
| EN_RESV1   |            |             |           |           |           |           |          |
| R          |            |             |           |           |           |           |          |
| 0h         |            |             |           |           |           |           |          |
| 7          | 6          | 5           | 4         | 3         | 2         | 1         | 0        |
| EN_CMPEQ   | EN_PRDEQ   | EN_CNTOVF   | EN_CEV4   | EN_CEV3   | EN_CEV2   | EN_CEV1   | EN_RESV0 |
| R/W        | R/W        | R/W         | R/W       | R/W       | R/W       | R/W       | R        |
| 0h         | 0h         | 0h          | 0h        | 0h        | 0h        | 0h        | 0h       |

**Table 4-1618. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_ECFLG\_ECEINT Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                 |
|-------|-------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | FLAG_RESV0  | R    | 0h    |                                                                                                                                                                                                             |
| 23    | FLAG_CMPEQ  | R    | 0h    | Compare Equal Status Flag:<br>Note: This flag is only active in APWM mode.<br>0 Indicates no event occurred<br>1 Indicates the counter (TSCNT) reached the Compare register value (ACMP)                    |
| 22    | FLAG_PRDEQ  | R    | 0h    | Period Equal Status Flag:<br>Note: This flag is only active in APWM mode.<br>0 Indicates no event occurred<br>1 Indicates the Counter (TSCNT) reached the Period register value (APER) and was reset.       |
| 21    | FLAG_CNTOVF | R    | 0h    | Counter Overflow Status Flag:<br>Note: This flag is active in CAP and APWM mode.<br>0 Indicates no event occurred.<br>1 Indicates the Counter (TSCNT) has made the transition from FFFF FFFFh to 0000 0000h |
| 20    | FLAG_CEV4   | R    | 0h    | Capture Event 4 Status Flag:<br>Note: This flag is only active in CAP mode.<br>0 Indicates no event occurred.<br>1 Indicates the fourth event occurred at ECAPx pin.                                        |

**Table 4-1618. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_ECFLG\_ECEINT Register Field Descriptions  
(continued)**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                          |
|------|-------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19   | FLAG_C EVT3 | R    | 0h    | Capture Event 3 Status Flag:<br>Note: This flag is only active in CAP mode.<br>0 Indicates no event occurred.<br>1 Indicates the third event occurred at ECAPx pin.  |
| 18   | FLAG_C EVT2 | R    | 0h    | Capture Event 2 Status Flag:<br>Note: This flag is only active in CAP mode.<br>0 Indicates no event occurred.<br>1 Indicates the second event occurred at ECAPx pin. |
| 17   | FLAG_C EVT1 | R    | 0h    | Capture Event 1 Status Flag:<br>Note: This flag is only active in CAP mode.<br>0 Indicates no event occurred.<br>1 Indicates the first event occurred at ECAPx pin.  |
| 16   | FLAG_INT    | R    | 0h    | Global Interrupt Status Flag:<br>0 Indicates no interrupt generated.<br>1 Indicates that an interrupt was generated from one of the following events.                |
| 15:8 | EN__RESV1   | R    | 0h    |                                                                                                                                                                      |
| 7    | EN_CMPEQ    | R/W  | 0h    | Compare Equal Interrupt Enable:<br>0 Disabled Compare Equal as an Interrupt source<br>1 Enable Compare Equal as an Interrupt source                                  |
| 6    | EN_PRDEQ    | R/W  | 0h    | Period Equal Interrupt Enable:<br>0 Disabled Period Equal as an Interrupt source<br>1 Enable Period Equal as an Interrupt source                                     |
| 5    | EN_CNTOVF   | R/W  | 0h    | Counter Overflow Interrupt Enable:<br>0 Disabled Counter Overflow as an Interrupt source<br>1 Enable Counter Overflow as an Interrupt source                         |
| 4    | EN_C EVT4   | R/W  | 0h    | Capture Event 4 Interrupt Enable:<br>0 Disabled Capture Event 4 as an Interrupt source:<br>1 Enable Capture Event 4 as an Interrupt source                           |
| 3    | EN_C EVT3   | R/W  | 0h    | Capture Event 3 Interrupt Enable:<br>0 Disabled Capture Event 3 as an Interrupt source:<br>1 Enable Capture Event 3 as an Interrupt source                           |
| 2    | EN_C EVT2   | R/W  | 0h    | Capture Event 2 Interrupt Enable:<br>0 Disabled Capture Event 2 as an Interrupt source:<br>1 Enable Capture Event 2 as an Interrupt source                           |
| 1    | EN_C EVT1   | R/W  | 0h    | Capture Event 1 Interrupt Enable:<br>0 Disabled Capture Event 1 as an Interrupt source:<br>1 Enable Capture Event 1 as an Interrupt source                           |

**Table 4-1618. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_ECFLG\_ECEINT Register Field Descriptions  
(continued)**

| Bit | Field    | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 0   | EN_RESV0 | R    | 0h    |             |

#### 4.2.2.335 ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_ECCLR Register

##### 1 ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_ECCLR Register (Offset = 30h) [reset = 0h]

ECAP INTERRUPT CLEAR REGISTER.

Return to [Summary Table](#)

**Table 4-1619. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 0030h       |

**Figure 4-529. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_ECCLR Name Register**

|          |       |        |       |       |       |       |     |
|----------|-------|--------|-------|-------|-------|-------|-----|
| 31       | 30    | 29     | 28    | 27    | 26    | 25    | 24  |
| RESERVED |       |        |       |       |       |       |     |
| NONE     |       |        |       |       |       |       |     |
| 0h       |       |        |       |       |       |       |     |
| 23       | 22    | 21     | 20    | 19    | 18    | 17    | 16  |
| RESERVED |       |        |       |       |       |       |     |
| NONE     |       |        |       |       |       |       |     |
| 0h       |       |        |       |       |       |       |     |
| 15       | 14    | 13     | 12    | 11    | 10    | 9     | 8   |
| _RESV0   |       |        |       |       |       |       |     |
| R        |       |        |       |       |       |       |     |
| 0h       |       |        |       |       |       |       |     |
| 7        | 6     | 5      | 4     | 3     | 2     | 1     | 0   |
| CMPEQ    | PRDEQ | CNTOVF | CEVT4 | CEVT3 | CEVT2 | CEVT1 | INT |
| R/W      | R/W   | R/W    | R/W   | R/W   | R/W   | R/W   | R/W |
| 0h       | 0h    | 0h     | 0h    | 0h    | 0h    | 0h    | 0h  |

**Table 4-1621. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_ECCLR Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                  |
|-------|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED | NONE | 0h    | Reserved                                                                                                                     |
| 15:8  | _RESV0   | R    | 0h    |                                                                                                                              |
| 7     | CMPEQ    | R/W  | 0h    | Compare Equal Status Flag:<br>0 No effect. Always reads back a 0.<br>1 Writing a 1h will clear the CMPEQ flag condition.     |
| 6     | PRDEQ    | R/W  | 0h    | Period Equal Status Flag:<br>0 No effect. Always reads back a 0.<br>1 Writing a 1h will clear the PRDEQ flag condition.      |
| 5     | CNTOVF   | R/W  | 0h    | Counter Overflow Status Flag:<br>0 No effect. Always reads back a 0.<br>1 Writing a 1h will clear the CNTOVF flag condition. |
| 4     | CEVT4    | R/W  | 0h    | Capture Event 4 Status Flag:<br>0 No effect. Always reads back a 0.<br>1 Writing a 1h will clear the CEVT4 flag condition.   |

**Table 4-1621. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_ECCLR Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                          |
|-----|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3   | CEVT3 | R/W  | 0h    | Capture Event 3 Status Flag:<br>0 No effect. Always reads back a 0.<br>1 Writing a 1h will clear the CEVT3 flag condition.                                                                           |
| 2   | CEVT2 | R/W  | 0h    | Capture Event 2 Status Flag:<br>0 No effect. Always reads back a 0.<br>1 Writing a 1h will clear the CEVT2 flag condition.                                                                           |
| 1   | CEVT1 | R/W  | 0h    | Capture Event 1 Status Flag:<br>0 No effect. Always reads back a 0.<br>1 Writing a 1h will clear the CEVT1 flag condition.                                                                           |
| 0   | INT   | R/W  | 0h    | Global Interrupt Clear Flag:<br>0 No effect. Always reads back a 0.<br>1 Writing a 1h will clear the INT flag and enable further interrupts to be generated if any of the event flags are set to 1h. |

#### 4.2.2.336 ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_ECFRC Register

##### 1 ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_ECFRC Register (Offset = 34h) [reset = 0h]

ECAP INTERRUPT FORCING REGISTER.

Return to [Summary Table](#)

**Table 4-1622. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 0034h       |

**Figure 4-530. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_ECFRC Name Register**

|          |       |        |       |       |       |       |        |
|----------|-------|--------|-------|-------|-------|-------|--------|
| 31       | 30    | 29     | 28    | 27    | 26    | 25    | 24     |
| RESERVED |       |        |       |       |       |       |        |
| NONE     |       |        |       |       |       |       |        |
| 0h       |       |        |       |       |       |       |        |
| 23       | 22    | 21     | 20    | 19    | 18    | 17    | 16     |
| RESERVED |       |        |       |       |       |       |        |
| NONE     |       |        |       |       |       |       |        |
| 0h       |       |        |       |       |       |       |        |
| 15       | 14    | 13     | 12    | 11    | 10    | 9     | 8      |
| _RESV1   |       |        |       |       |       |       |        |
| R        |       |        |       |       |       |       |        |
| 0h       |       |        |       |       |       |       |        |
| 7        | 6     | 5      | 4     | 3     | 2     | 1     | 0      |
| CMPEQ    | PRDEQ | CNTOVF | CEVT4 | CEVT3 | CEVT2 | CEVT1 | _RESV0 |
| R/W      | R/W   | R/W    | R/W   | R/W   | R/W   | R/W   | R      |
| 0h       | 0h    | 0h     | 0h    | 0h    | 0h    | 0h    | 0h     |

**Table 4-1624. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_ECFRC Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                |
|-------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED | NONE | 0h    | Reserved                                                                                                                   |
| 15:8  | _RESV1   | R    | 0h    |                                                                                                                            |
| 7     | CMPEQ    | R/W  | 0h    | Force Compare Equal:<br>0 No effect. Always reads back a 0h<br>1 Writing a 1h to this bit will set the CMPEQ flag bit.     |
| 6     | PRDEQ    | R/W  | 0h    | Force Period Equal:<br>0 No effect. Always reads back a 0.<br>1 Writing a 1h to this bit will set the PRDEQ flag bit.      |
| 5     | CNTOVF   | R/W  | 0h    | Force Counter Overflow:<br>0 No effect. Always reads back a 0.<br>1 Writing a 1h to this bit will set the CNTOVF flag bit. |
| 4     | CEVT4    | R/W  | 0h    | Force Capture Event 4:<br>0 No effect. Always reads back a 0.<br>1 Writing a 1h to this bit will set the CEVT4 flag bit.   |

**Table 4-1624. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_ECFRC Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                              |
|-----|--------|------|-------|--------------------------------------------------------------------------------------------------------------------------|
| 3   | CEVT3  | R/W  | 0h    | Force Capture Event 3:<br>0 No effect. Always reads back a 0.<br>1 Writing a 1h to this bit will set the CEVT3 flag bit. |
| 2   | CEVT2  | R/W  | 0h    | Force Capture Event 2:<br>0 No effect. Always reads back a 0.<br>1 Writing a 1h to this bit will set the CEVT2 flag bit. |
| 1   | CEVT1  | R/W  | 0h    | Force Capture Event 1:<br>0 No effect. Always reads back a 0.<br>1 Writing a 1h to this bit will set the CEVT1 flag bit. |
| 0   | _RESV0 | R    | 0h    |                                                                                                                          |

#### 4.2.2.337 ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_REVID1 Register

#### 1 ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_REVID1 Register (Offset = 5Ch) [reset = 44D22100h]

Revision Identification Register 1

Return to [Summary Table](#)

**Table 4-1625. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 005Ch       |

**Figure 4-531. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_REVID1 Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| REVID     |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 44D22100h |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| REVID     |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 44D22100h |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| REVID     |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 44D22100h |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| REVID     |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 44D22100h |    |    |    |    |    |    |    |

**Table 4-1627. ICSSM\_PR1\_ICSS\_ECAP0\_ECAP\_SLV\_REVID1 Register Field Descriptions**

| Bit  | Field | Type | Reset     | Description |
|------|-------|------|-----------|-------------|
| 31:0 | REVID | R    | 44D22100h |             |



#### 4.2.2.338 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RXCFG0 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RXCFG0 Register (Offset = 0h) [reset = 0h]

MIIRXCFG0Register.

Return to [Summary Table](#)

**Table 4-1628. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2000h       |

**Figure 4-532. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RXCFG0 Name Register**

|             |                  |               |           |             |                  |                       |             |
|-------------|------------------|---------------|-----------|-------------|------------------|-----------------------|-------------|
| 31          | 30               | 29            | 28        | 27          | 26               | 25                    | 24          |
| RESERVED    |                  |               |           |             |                  |                       |             |
| NONE        |                  |               |           |             |                  |                       |             |
| 0h          |                  |               |           |             |                  |                       |             |
| 23          | 22               | 21            | 20        | 19          | 18               | 17                    | 16          |
| RESERVED    |                  |               |           |             |                  |                       |             |
| NONE        |                  |               |           |             |                  |                       |             |
| 0h          |                  |               |           |             |                  |                       |             |
| 15          | 14               | 13            | 12        | 11          | 10               | 9                     | 8           |
| RESERVED    |                  |               |           |             |                  | RX_EOF_SCLR_DIS0      | RX_ERR_RAW0 |
| NONE        |                  |               |           |             |                  | R/W                   | R/W         |
| 0h          |                  |               |           |             |                  | 0h                    | 0h          |
| 7           | 6                | 5             | 4         | 3           | 2                | 1                     | 0           |
| RX_SFD_RAW0 | RX_AUTO_FWD_PRE0 | RX_BYTE_SWAP0 | RX_L2_EN0 | RX_MUX_SEL0 | RX_CUT_PREAMBLE0 | RX_DATA_RDY_MODE_DIS0 | RX_ENABLE0  |
| R/W         | R/W              | R/W           | R/W       | R/W         | R/W              | R/W                   | R/W         |
| 0h          | 0h               | 0h            | 0h        | 0h          | 0h               | 0h                    | 0h          |

**Table 4-1630. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RXCFG0 Register Field Descriptions**

| Bit   | Field                 | Type | Reset | Description |
|-------|-----------------------|------|-------|-------------|
| 31:10 | RESERVED              | NONE | 0h    | Reserved    |
| 9     | RX_EOF_SCLR_DIS0      | R/W  | 0h    |             |
| 8     | RX_ERR_RAW0           | R/W  | 0h    |             |
| 7     | RX_SFD_RAW0           | R/W  | 0h    |             |
| 6     | RX_AUTO_FWD_PRE0      | R/W  | 0h    |             |
| 5     | RX_BYTE_SWAP0         | R/W  | 0h    |             |
| 4     | RX_L2_EN0             | R/W  | 0h    |             |
| 3     | RX_MUX_SEL0           | R/W  | 0h    |             |
| 2     | RX_CUT_PREAMBLE0      | R/W  | 0h    |             |
| 1     | RX_DATA_RDY_MODE_DIS0 | R/W  | 0h    |             |
| 0     | RX_ENABLE0            | R/W  | 0h    |             |

#### 4.2.2.339 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RXCFG1 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RXCFG1 Register (Offset = 4h) [reset = 8h]

MIIRXCFG1Register.

Return to [Summary Table](#)

**Table 4-1631. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2004h       |

**Figure 4-533. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RXCFG1 Name Register**

|             |                  |               |           |             |                  |                       |             |
|-------------|------------------|---------------|-----------|-------------|------------------|-----------------------|-------------|
| 31          | 30               | 29            | 28        | 27          | 26               | 25                    | 24          |
| RESERVED    |                  |               |           |             |                  |                       |             |
| NONE        |                  |               |           |             |                  |                       |             |
| 0h          |                  |               |           |             |                  |                       |             |
| 23          | 22               | 21            | 20        | 19          | 18               | 17                    | 16          |
| RESERVED    |                  |               |           |             |                  |                       |             |
| NONE        |                  |               |           |             |                  |                       |             |
| 0h          |                  |               |           |             |                  |                       |             |
| 15          | 14               | 13            | 12        | 11          | 10               | 9                     | 8           |
| RESERVED    |                  |               |           |             |                  | RX_EOF_SCLR_DIS1      | RX_ERR_RAW1 |
| NONE        |                  |               |           |             |                  | R/W                   | R/W         |
| 0h          |                  |               |           |             |                  | 0h                    | 0h          |
| 7           | 6                | 5             | 4         | 3           | 2                | 1                     | 0           |
| RX_SFD_RAW1 | RX_AUTO_FWD_PRE1 | RX_BYTE_SWAP1 | RX_L2_EN1 | RX_MUX_SEL1 | RX_CUT_PREAMBLE1 | RX_DATA_RDY_MODE_DIS1 | RX_ENABLE1  |
| R/W         | R/W              | R/W           | R/W       | R/W         | R/W              | R/W                   | R/W         |
| 0h          | 0h               | 0h            | 0h        | 1h          | 0h               | 0h                    | 0h          |

**Table 4-1633. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RXCFG1 Register Field Descriptions**

| Bit   | Field                 | Type | Reset | Description |
|-------|-----------------------|------|-------|-------------|
| 31:10 | RESERVED              | NONE | 0h    | Reserved    |
| 9     | RX_EOF_SCLR_DIS1      | R/W  | 0h    |             |
| 8     | RX_ERR_RAW1           | R/W  | 0h    |             |
| 7     | RX_SFD_RAW1           | R/W  | 0h    |             |
| 6     | RX_AUTO_FWD_PRE1      | R/W  | 0h    |             |
| 5     | RX_BYTE_SWAP1         | R/W  | 0h    |             |
| 4     | RX_L2_EN1             | R/W  | 0h    |             |
| 3     | RX_MUX_SEL1           | R/W  | 1h    |             |
| 2     | RX_CUT_PREAMBLE1      | R/W  | 0h    |             |
| 1     | RX_DATA_RDY_MODE_DIS1 | R/W  | 0h    |             |
| 0     | RX_ENABLE1            | R/W  | 0h    |             |

#### 4.2.2.340 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TXCFG0 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TXCFG0 Register (Offset = 10h) [reset = 400100h]

MIITXCFG0Register.

Return to [Summary Table](#)

**Table 4-1634. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2010h       |

**Figure 4-534. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TXCFG0 Name Register**

| 31              | 30            | 29 | 28                  | 27             | 26                   | 25                    | 24          |
|-----------------|---------------|----|---------------------|----------------|----------------------|-----------------------|-------------|
| RESERVED        | TX_CLK_DELAY0 |    |                     | RESERVED       | TX_START_DELAY0      |                       |             |
| NONE            | R/W           |    |                     | NONE           | R/W                  |                       |             |
| 0h              | 0h            |    |                     | 0h             | 40h                  |                       |             |
| 23              | 22            | 21 | 20                  | 19             | 18                   | 17                    | 16          |
| TX_START_DELAY0 |               |    |                     |                |                      |                       |             |
| R/W             |               |    |                     |                |                      |                       |             |
| 40h             |               |    |                     |                |                      |                       |             |
| 15              | 14            | 13 | 12                  | 11             | 10                   | 9                     | 8           |
| RESERVED        |               |    | TX_IPG_WIRE_CLK_EN0 | TX_32_MODE_EN0 | PRE_TX_AUTO_ESC_ERR0 | PRE_TX_AUTO_SEQUENCE0 | TX_MUX_SEL0 |
| NONE            |               |    | R/W                 | R/W            | R/W                  | R/W                   | R/W         |
| 0h              |               |    | 0h                  | 0h             | 0h                   | 0h                    | 1h          |
| 7               | 6             | 5  | 4                   | 3              | 2                    | 1                     | 0           |
| RESERVED        |               |    |                     | TX_BYTE_SWAP0  | TX_EN_MODE0          | TX_AUTO_PREAMBLE0     | TX_ENABLE0  |
| NONE            |               |    |                     | R/W            | R/W                  | R/W                   | R/W         |
| 0h              |               |    |                     | 0h             | 0h                   | 0h                    | 0h          |

**Table 4-1636. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TXCFG0 Register Field Descriptions**

| Bit   | Field                 | Type | Reset | Description |
|-------|-----------------------|------|-------|-------------|
| 31    | RESERVED              | NONE | 0h    | Reserved    |
| 30:28 | TX_CLK_DELAY0         | R/W  | 0h    |             |
| 27:26 | RESERVED              | NONE | 0h    | Reserved    |
| 25:16 | TX_START_DELAY0       | R/W  | 40h   |             |
| 15:13 | RESERVED              | NONE | 0h    | Reserved    |
| 12    | TX_IPG_WIRE_CLK_EN0   | R/W  | 0h    |             |
| 11    | TX_32_MODE_EN0        | R/W  | 0h    |             |
| 10    | PRE_TX_AUTO_ESC_ERR0  | R/W  | 0h    |             |
| 9     | PRE_TX_AUTO_SEQUENCE0 | R/W  | 0h    |             |
| 8     | TX_MUX_SEL0           | R/W  | 1h    |             |
| 7:4   | RESERVED              | NONE | 0h    | Reserved    |
| 3     | TX_BYTE_SWAP0         | R/W  | 0h    |             |
| 2     | TX_EN_MODE0           | R/W  | 0h    |             |
| 1     | TX_AUTO_PREAMBLE0     | R/W  | 0h    |             |
| 0     | TX_ENABLE0            | R/W  | 0h    |             |

#### 4.2.2.341 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TXCFG1 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TXCFG1 Register (Offset = 14h) [reset = 400000h]

MIITXCFG1Register.

Return to [Summary Table](#)

**Table 4-1637. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2014h       |

**Figure 4-535. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TXCFG1 Name Register**

| 31              | 30            | 29 | 28                  | 27             | 26                   | 25                    | 24          |
|-----------------|---------------|----|---------------------|----------------|----------------------|-----------------------|-------------|
| RESERVED        | TX_CLK_DELAY1 |    |                     | RESERVED       | TX_START_DELAY1      |                       |             |
| NONE            | R/W           |    |                     | NONE           | R/W                  |                       |             |
| 0h              | 0h            |    |                     | 0h             | 40h                  |                       |             |
| 23              | 22            | 21 | 20                  | 19             | 18                   | 17                    | 16          |
| TX_START_DELAY1 |               |    |                     |                |                      |                       |             |
| R/W             |               |    |                     |                |                      |                       |             |
| 40h             |               |    |                     |                |                      |                       |             |
| 15              | 14            | 13 | 12                  | 11             | 10                   | 9                     | 8           |
| RESERVED        |               |    | TX_IPG_WIRE_CLK_EN1 | TX_32_MODE_EN1 | PRE_TX_AUTO_ESC_ERR1 | PRE_TX_AUTO_SEQUENCE1 | TX_MUX_SEL1 |
| NONE            |               |    | R/W                 | R/W            | R/W                  | R/W                   | R/W         |
| 0h              |               |    | 0h                  | 0h             | 0h                   | 0h                    | 0h          |
| 7               | 6             | 5  | 4                   | 3              | 2                    | 1                     | 0           |
| RESERVED        |               |    |                     | TX_BYTE_SWAP1  | TX_EN_MODE1          | TX_AUTO_PREAMBLE1     | TX_ENABLE1  |
| NONE            |               |    |                     | R/W            | R/W                  | R/W                   | R/W         |
| 0h              |               |    |                     | 0h             | 0h                   | 0h                    | 0h          |

**Table 4-1639. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TXCFG1 Register Field Descriptions**

| Bit   | Field                 | Type | Reset | Description |
|-------|-----------------------|------|-------|-------------|
| 31    | RESERVED              | NONE | 0h    | Reserved    |
| 30:28 | TX_CLK_DELAY1         | R/W  | 0h    |             |
| 27:26 | RESERVED              | NONE | 0h    | Reserved    |
| 25:16 | TX_START_DELAY1       | R/W  | 40h   |             |
| 15:13 | RESERVED              | NONE | 0h    | Reserved    |
| 12    | TX_IPG_WIRE_CLK_EN1   | R/W  | 0h    |             |
| 11    | TX_32_MODE_EN1        | R/W  | 0h    |             |
| 10    | PRE_TX_AUTO_ESC_ERR1  | R/W  | 0h    |             |
| 9     | PRE_TX_AUTO_SEQUENCE1 | R/W  | 0h    |             |
| 8     | TX_MUX_SEL1           | R/W  | 0h    |             |
| 7:4   | RESERVED              | NONE | 0h    | Reserved    |
| 3     | TX_BYTE_SWAP1         | R/W  | 0h    |             |
| 2     | TX_EN_MODE1           | R/W  | 0h    |             |
| 1     | TX_AUTO_PREAMBLE1     | R/W  | 0h    |             |
| 0     | TX_ENABLE1            | R/W  | 0h    |             |

#### 4.2.2.342 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TX\_CRC0 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TX\_CRC0 Register (Offset = 20h) [reset = 0h]

MIITXCRC0Register.

Return to [Summary Table](#)

**Table 4-1640. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2020h       |

**Figure 4-536. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TX\_CRC0 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TX_CRC0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TX_CRC0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TX_CRC0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TX_CRC0 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1642. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TX\_CRC0 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                  |
|------|---------|------|-------|------------------------------|
| 31:0 | TX_CRC0 | R    | 0h    | Transmit CRC for last packet |

#### 4.2.2.343 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TX\_CRC1 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TX\_CRC1 Register (Offset = 24h) [reset = 0h]

MIITXCRC1Register.

Return to [Summary Table](#)

**Table 4-1643. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2024h       |

**Figure 4-537. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TX\_CRC1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TX_CRC1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TX_CRC1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TX_CRC1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TX_CRC1 |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-1645. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TX\_CRC1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                  |
|------|---------|------|-------|------------------------------|
| 31:0 | TX_CRC1 | R    | 0h    | Transmit CRC for last packet |

#### 4.2.2.344 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TX\_IPG0 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TX\_IPG0 Register (Offset = 30h) [reset = 28h]

MIITXIPG0Register.

Return to [Summary Table](#)

**Table 4-1646. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2030h       |

**Figure 4-538. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TX\_IPG0 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TX_IPG0  |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 28h      |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TX_IPG0  |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 28h      |    |    |    |    |    |    |    |

**Table 4-1648. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TX\_IPG0 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description  |
|-------|----------|------|-------|--------------|
| 31:16 | RESERVED | NONE | 0h    | Reserved     |
| 15:0  | TX_IPG0  | R/W  | 28h   | Transmit IPG |

#### 4.2.2.345 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TX\_IPG1 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TX\_IPG1 Register (Offset = 34h) [reset = 28h]

MIITXIPG1Register.

Return to [Summary Table](#)

**Table 4-1649. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2034h       |

**Figure 4-539. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TX\_IPG1 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TX_IPG1  |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 28h      |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TX_IPG1  |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 28h      |    |    |    |    |    |    |    |

**Table 4-1651. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TX\_IPG1 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description  |
|-------|----------|------|-------|--------------|
| 31:16 | RESERVED | NONE | 0h    | Reserved     |
| 15:0  | TX_IPG1  | R/W  | 28h   | Transmit IPG |



#### 4.2.2.346 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_PRS0 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_PRS0 Register (Offset = 38h) [reset = 0h]

MIIPortStatus0Register.

Return to [Summary Table](#)

**Table 4-1652. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2038h       |

**Figure 4-540. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_PRS0 Name Register**

|          |    |    |    |    |    |                |                |
|----------|----|----|----|----|----|----------------|----------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25             | 24             |
| RESERVED |    |    |    |    |    |                |                |
| NONE     |    |    |    |    |    |                |                |
| 0h       |    |    |    |    |    |                |                |
| 23       | 22 | 21 | 20 | 19 | 18 | 17             | 16             |
| RESERVED |    |    |    |    |    |                |                |
| NONE     |    |    |    |    |    |                |                |
| 0h       |    |    |    |    |    |                |                |
| 15       | 14 | 13 | 12 | 11 | 10 | 9              | 8              |
| RESERVED |    |    |    |    |    |                |                |
| NONE     |    |    |    |    |    |                |                |
| 0h       |    |    |    |    |    |                |                |
| 7        | 6  | 5  | 4  | 3  | 2  | 1              | 0              |
| RESERVED |    |    |    |    |    | SYNC_PORT0_CRS | SYNC_PORT0_COL |
| NONE     |    |    |    |    |    | R              | R              |
| 0h       |    |    |    |    |    | 0h             | 0h             |

**Table 4-1654. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_PRS0 Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description    |
|------|----------------|------|-------|----------------|
| 31:2 | RESERVED       | NONE | 0h    | Reserved       |
| 1    | SYNC_PORT0_CRS | R    | 0h    | Sync_port0_crs |
| 0    | SYNC_PORT0_COL | R    | 0h    | Sync_port0_col |

#### 4.2.2.347 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_PRS1 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_PRS1 Register (Offset = 3Ch) [reset = 0h]

MIIPortStatus1Register.

Return to [Summary Table](#)

**Table 4-1655. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 203Ch       |

**Figure 4-541. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_PRS1 Name Register**

|          |    |    |    |    |    |                 |                 |
|----------|----|----|----|----|----|-----------------|-----------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25              | 24              |
| RESERVED |    |    |    |    |    |                 |                 |
| NONE     |    |    |    |    |    |                 |                 |
| 0h       |    |    |    |    |    |                 |                 |
| 23       | 22 | 21 | 20 | 19 | 18 | 17              | 16              |
| RESERVED |    |    |    |    |    |                 |                 |
| NONE     |    |    |    |    |    |                 |                 |
| 0h       |    |    |    |    |    |                 |                 |
| 15       | 14 | 13 | 12 | 11 | 10 | 9               | 8               |
| RESERVED |    |    |    |    |    |                 |                 |
| NONE     |    |    |    |    |    |                 |                 |
| 0h       |    |    |    |    |    |                 |                 |
| 7        | 6  | 5  | 4  | 3  | 2  | 1               | 0               |
| RESERVED |    |    |    |    |    | SYNC_PORT1_ CRS | SYNC_PORT1_ COL |
| NONE     |    |    |    |    |    | R               | R               |
| 0h       |    |    |    |    |    | 0h              | 0h              |

**Table 4-1657. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_PRS1 Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description    |
|------|----------------|------|-------|----------------|
| 31:2 | RESERVED       | NONE | 0h    | Reserved       |
| 1    | SYNC_PORT1_CRS | R    | 0h    | Sync_port1_crs |
| 0    | SYNC_PORT1_COL | R    | 0h    | Sync_port1_col |

#### 4.2.2.348 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_FRMS0 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_FRMS0 Register (Offset = 40h) [reset = 5F1003Fh]

MIIRXFRMS0Register.

Return to [Summary Table](#)

**Table 4-1658. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2040h       |

**Figure 4-542. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_FRMS0 Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RX_MAX_FRM0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 5F1h        |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RX_MAX_FRM0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 5F1h        |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RX_MIN_FRM0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 3Fh         |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RX_MIN_FRM0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 3Fh         |    |    |    |    |    |    |    |

**Table 4-1660. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_FRMS0 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description |
|-------|-------------|------|-------|-------------|
| 31:16 | RX_MAX_FRM0 | R/W  | 5F1h  | Rx_max_frm0 |
| 15:0  | RX_MIN_FRM0 | R/W  | 3Fh   | Rx_min_frm0 |

#### 4.2.2.349 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_FRMS1 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_FRMS1 Register (Offset = 44h) [reset = 5F1003Fh]

MIIRXFRMS1Register.

Return to [Summary Table](#)

**Table 4-1661. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2044h       |

**Figure 4-543. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_FRMS1 Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RX_MAX_FRM1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 5F1h        |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RX_MAX_FRM1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 5F1h        |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RX_MIN_FRM1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 3Fh         |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RX_MIN_FRM1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 3Fh         |    |    |    |    |    |    |    |

**Table 4-1663. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_FRMS1 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description |
|-------|-------------|------|-------|-------------|
| 31:16 | RX_MAX_FRM1 | R/W  | 5F1h  | Rx_max_frm1 |
| 15:0  | RX_MIN_FRM1 | R/W  | 3Fh   | Rx_min_frm1 |

#### 4.2.2.350 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_PCNT0 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_PCNT0 Register (Offset = 48h) [reset = E1h]

MIIRXPCNT0Register.

Return to [Summary Table](#)

**Table 4-1664. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2048h       |

**Figure 4-544. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_PCNT0 Name Register**

|              |    |    |    |              |    |    |              |
|--------------|----|----|----|--------------|----|----|--------------|
| 31           | 30 | 29 | 28 | 27           | 26 | 25 | 24           |
| RESERVED     |    |    |    |              |    |    |              |
| NONE         |    |    |    |              |    |    |              |
| 0h           |    |    |    |              |    |    |              |
| 23           | 22 | 21 | 20 | 19           | 18 | 17 | 16           |
| RESERVED     |    |    |    |              |    |    |              |
| NONE         |    |    |    |              |    |    |              |
| 0h           |    |    |    |              |    |    |              |
| 15           | 14 | 13 | 12 | 11           | 10 | 9  | 8            |
| RESERVED     |    |    |    |              |    |    | RX_MAX_PCNT0 |
| NONE         |    |    |    |              |    |    | R/W          |
| 0h           |    |    |    |              |    |    | Eh           |
| 7            | 6  | 5  | 4  | 3            | 2  | 1  | 0            |
| RX_MAX_PCNT0 |    |    |    | RX_MIN_PCNT0 |    |    |              |
| R/W          |    |    |    | R/W          |    |    |              |
| Eh           |    |    |    | 1h           |    |    |              |

**Table 4-1666. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_PCNT0 Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description  |
|------|--------------|------|-------|--------------|
| 31:9 | RESERVED     | NONE | 0h    | Reserved     |
| 8:4  | RX_MAX_PCNT0 | R/W  | Eh    | Rx_max_pcnt0 |
| 3:0  | RX_MIN_PCNT0 | R/W  | 1h    | Rx_min_pcnt0 |

#### 4.2.2.351 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_PCNT1 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_PCNT1 Register (Offset = 4Ch) [reset = E1h]

MIIRXPCNT1Register.

Return to [Summary Table](#)
**Table 4-1667. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 204Ch       |

**Figure 4-545. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_PCNT1 Name Register**

|              |    |    |    |              |    |    |              |
|--------------|----|----|----|--------------|----|----|--------------|
| 31           | 30 | 29 | 28 | 27           | 26 | 25 | 24           |
| RESERVED     |    |    |    |              |    |    |              |
| NONE         |    |    |    |              |    |    |              |
| 0h           |    |    |    |              |    |    |              |
| 23           | 22 | 21 | 20 | 19           | 18 | 17 | 16           |
| RESERVED     |    |    |    |              |    |    |              |
| NONE         |    |    |    |              |    |    |              |
| 0h           |    |    |    |              |    |    |              |
| 15           | 14 | 13 | 12 | 11           | 10 | 9  | 8            |
| RESERVED     |    |    |    |              |    |    | RX_MAX_PCNT1 |
| NONE         |    |    |    |              |    |    | R/W          |
| 0h           |    |    |    |              |    |    | Eh           |
| 7            | 6  | 5  | 4  | 3            | 2  | 1  | 0            |
| RX_MAX_PCNT1 |    |    |    | RX_MIN_PCNT1 |    |    |              |
| R/W          |    |    |    | R/W          |    |    |              |
| Eh           |    |    |    | 1h           |    |    |              |

**Table 4-1669. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_PCNT1 Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description  |
|------|--------------|------|-------|--------------|
| 31:9 | RESERVED     | NONE | 0h    | Reserved     |
| 8:4  | RX_MAX_PCNT1 | R/W  | Eh    | Rx_max_pcnt1 |
| 3:0  | RX_MIN_PCNT1 | R/W  | 1h    | Rx_min_pcnt1 |

#### 4.2.2.352 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_ERR0 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_ERR0 Register (Offset = 50h) [reset = 0h]

MIIRXERR0Register.

Return to [Summary Table](#)

**Table 4-1670. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2050h       |

**Figure 4-546. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_ERR0 Name Register**

|          |    |    |    |                 |                 |                  |                  |
|----------|----|----|----|-----------------|-----------------|------------------|------------------|
| 31       | 30 | 29 | 28 | 27              | 26              | 25               | 24               |
| RESERVED |    |    |    |                 |                 |                  |                  |
| NONE     |    |    |    |                 |                 |                  |                  |
| 0h       |    |    |    |                 |                 |                  |                  |
| 23       | 22 | 21 | 20 | 19              | 18              | 17               | 16               |
| RESERVED |    |    |    |                 |                 |                  |                  |
| NONE     |    |    |    |                 |                 |                  |                  |
| 0h       |    |    |    |                 |                 |                  |                  |
| 15       | 14 | 13 | 12 | 11              | 10              | 9                | 8                |
| RESERVED |    |    |    |                 |                 |                  |                  |
| NONE     |    |    |    |                 |                 |                  |                  |
| 0h       |    |    |    |                 |                 |                  |                  |
| 7        | 6  | 5  | 4  | 3               | 2               | 1                | 0                |
| RESERVED |    |    |    | RX_MAX_FRM_ERR0 | RX_MIN_FRM_ERR0 | RX_MAX_PCNT_ERR0 | RX_MIN_PCNT_ERR0 |
| NONE     |    |    |    | R/W1C           | R/W1C           | R/W1C            | R/W1C            |
| 0h       |    |    |    | 0h              | 0h              | 0h               | 0h               |

**Table 4-1672. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_ERR0 Register Field Descriptions**

| Bit  | Field            | Type  | Reset | Description      |
|------|------------------|-------|-------|------------------|
| 31:4 | RESERVED         | NONE  | 0h    | Reserved         |
| 3    | RX_MAX_FRM_ERR0  | R/W1C | 0h    | Rx_max_frm_err0  |
| 2    | RX_MIN_FRM_ERR0  | R/W1C | 0h    | Rx_min_frm_err0  |
| 1    | RX_MAX_PCNT_ERR0 | R/W1C | 0h    | Rx_max_pcnt_err0 |
| 0    | RX_MIN_PCNT_ERR0 | R/W1C | 0h    | Rx_min_pcnt_err0 |

#### 4.2.2.353 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_ERR1 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_ERR1 Register (Offset = 54h) [reset = 0h]

MIIRXERR1 Register.

Return to [Summary Table](#)

**Table 4-1673. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2054h       |

**Figure 4-547. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_ERR1 Name Register**

|          |    |    |    |                 |                 |                  |                  |
|----------|----|----|----|-----------------|-----------------|------------------|------------------|
| 31       | 30 | 29 | 28 | 27              | 26              | 25               | 24               |
| RESERVED |    |    |    |                 |                 |                  |                  |
| NONE     |    |    |    |                 |                 |                  |                  |
| 0h       |    |    |    |                 |                 |                  |                  |
| 23       | 22 | 21 | 20 | 19              | 18              | 17               | 16               |
| RESERVED |    |    |    |                 |                 |                  |                  |
| NONE     |    |    |    |                 |                 |                  |                  |
| 0h       |    |    |    |                 |                 |                  |                  |
| 15       | 14 | 13 | 12 | 11              | 10              | 9                | 8                |
| RESERVED |    |    |    |                 |                 |                  |                  |
| NONE     |    |    |    |                 |                 |                  |                  |
| 0h       |    |    |    |                 |                 |                  |                  |
| 7        | 6  | 5  | 4  | 3               | 2               | 1                | 0                |
| RESERVED |    |    |    | RX_MAX_FRM_ERR1 | RX_MIN_FRM_ERR1 | RX_MAX_PCNT_ERR1 | RX_MIN_PCNT_ERR1 |
| NONE     |    |    |    | R/W1C           | R/W1C           | R/W1C            | R/W1C            |
| 0h       |    |    |    | 0h              | 0h              | 0h               | 0h               |

**Table 4-1675. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_ERR1 Register Field Descriptions**

| Bit  | Field            | Type  | Reset | Description      |
|------|------------------|-------|-------|------------------|
| 31:4 | RESERVED         | NONE  | 0h    | Reserved         |
| 3    | RX_MAX_FRM_ERR1  | R/W1C | 0h    | Rx_max_frm_err1  |
| 2    | RX_MIN_FRM_ERR1  | R/W1C | 0h    | Rx_min_frm_err1  |
| 1    | RX_MAX_PCNT_ERR1 | R/W1C | 0h    | Rx_max_pcnt_err1 |
| 0    | RX_MIN_PCNT_ERR1 | R/W1C | 0h    | Rx_min_pcnt_err1 |



#### 4.2.2.354 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_FIFO\_LEVEL0 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_FIFO\_LEVEL0 Register (Offset = 60h) [reset = 0h]

MIIRXFIFOLEVEL0Register.

Return to [Summary Table](#)

**Table 4-1676. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2060h       |

**Figure 4-548. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_FIFO\_LEVEL0 Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RX_FIFO_LEVEL0 |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 4-1678. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_FIFO\_LEVEL0 Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description    |
|------|----------------|------|-------|----------------|
| 31:8 | RESERVED       | NONE | 0h    | Reserved       |
| 7:0  | RX_FIFO_LEVEL0 | R    | 0h    | Rx_fifo_level0 |

#### 4.2.2.355 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_FIFO\_LEVEL1 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_FIFO\_LEVEL1 Register (Offset = 64h) [reset = 0h]

MIIRXFIFOLEVEL1Register.

Return to [Summary Table](#)

**Table 4-1679. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2064h       |

**Figure 4-549. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_FIFO\_LEVEL1 Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RX_FIFO_LEVEL1 |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 4-1681. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_RX\_FIFO\_LEVEL1 Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description    |
|------|----------------|------|-------|----------------|
| 31:8 | RESERVED       | NONE | 0h    | Reserved       |
| 7:0  | RX_FIFO_LEVEL1 | R    | 0h    | Rx_fifo_level1 |

#### 4.2.2.356 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TX\_FIFO\_LEVEL0 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TX\_FIFO\_LEVEL0 Register (Offset = 68h) [reset = 0h]

MIIRXFIFOLEVEL0Register.

Return to [Summary Table](#)

**Table 4-1682. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2068h       |

**Figure 4-550. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TX\_FIFO\_LEVEL0 Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TX_FIFO_LEVEL0 |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 4-1684. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TX\_FIFO\_LEVEL0 Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description    |
|------|----------------|------|-------|----------------|
| 31:8 | RESERVED       | NONE | 0h    | Reserved       |
| 7:0  | TX_FIFO_LEVEL0 | R    | 0h    | tx_fifo_level0 |

#### 4.2.2.357 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TX\_FIFO\_LEVEL1 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TX\_FIFO\_LEVEL1 Register (Offset = 6Ch) [reset = 0h]

MIIRXFIFOLEVEL1Register.

Return to [Summary Table](#)

**Table 4-1685. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 206Ch       |

**Figure 4-551. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TX\_FIFO\_LEVEL1 Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TX_FIFO_LEVEL1 |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 4-1687. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_CFG\_TX\_FIFO\_LEVEL1 Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description    |
|------|----------------|------|-------|----------------|
| 31:8 | RESERVED       | NONE | 0h    | Reserved       |
| 7:0  | TX_FIFO_LEVEL1 | R    | 0h    | tx_fifo_level1 |

#### 4.2.2.358 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_MDIO\_VERSION\_REG Register

##### 1 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_MDIO\_VERSION\_REG Register (Offset = 0h) [reset = 70107h]

version\_reg.

Return to [Summary Table](#)

**Table 4-1688. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2400h       |

**Figure 4-552. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_MDIO\_VERSION\_REG Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MODID    |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 7h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MODID    |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 7h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| REVMAJ   |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 1h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| REVMINOR |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 7h       |    |    |    |    |    |    |    |

**Table 4-1690. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_MDIO\_VERSION\_REG Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description          |
|-------|----------|------|-------|----------------------|
| 31:16 | MODID    | R    | 7h    | Module ID            |
| 15:8  | REVMAJ   | R    | 1h    | Major revision value |
| 7:0   | REVMINOR | R    | 7h    | Minor revision value |

#### 4.2.2.359 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_CONTROL\_REG Register

##### 1 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_CONTROL\_REG Register (Offset = 4h) [reset = 810000FFh]

control\_reg.

Return to [Summary Table](#)

**Table 4-1691. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2404h       |

**Figure 4-553. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_CONTROL\_REG Name Register**

|          |        |          |                      |        |                     |                 |          |
|----------|--------|----------|----------------------|--------|---------------------|-----------------|----------|
| 31       | 30     | 29       | 28                   | 27     | 26                  | 25              | 24       |
| IDLE     | ENABLE | RESERVED | HIGHEST_USER_CHANNEL |        |                     |                 |          |
| R        | R/W    | NONE     | R                    |        |                     |                 |          |
| 1h       | 0h     | 0h       | 1h                   |        |                     |                 |          |
| 23       | 22     | 21       | 20                   | 19     | 18                  | 17              | 16       |
| RESERVED |        |          | PREAMBLE             | FAULT  | FAULT_DETECT_ENABLE | INT_TEST_ENABLE | RESERVED |
| NONE     |        |          | R/W                  | R/W1TC | R/W                 | R/W             | NONE     |
| 0h       |        |          | 0h                   | 0h     | 0h                  | 0h              | 0h       |
| 15       | 14     | 13       | 12                   | 11     | 10                  | 9               | 8        |
| CLKDIV   |        |          |                      |        |                     |                 |          |
| R/W      |        |          |                      |        |                     |                 |          |
| FFh      |        |          |                      |        |                     |                 |          |
| 7        | 6      | 5        | 4                    | 3      | 2                   | 1               | 0        |
| CLKDIV   |        |          |                      |        |                     |                 |          |
| R/W      |        |          |                      |        |                     |                 |          |
| FFh      |        |          |                      |        |                     |                 |          |

**Table 4-1693. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_CONTROL\_REG Register Field Descriptions**

| Bit   | Field                | Type   | Reset | Description             |
|-------|----------------------|--------|-------|-------------------------|
| 31    | IDLE                 | R      | 1h    | MDIO state machine idle |
| 30    | ENABLE               | R/W    | 0h    | Enable control          |
| 29    | RESERVED             | NONE   | 0h    | Reserved                |
| 28:24 | HIGHEST_USER_CHANNEL | R      | 1h    | Highest user channel    |
| 23:21 | RESERVED             | NONE   | 0h    | Reserved                |
| 20    | PREAMBLE             | R/W    | 0h    | Preamble disable        |
| 19    | FAULT                | R/W1TC | 0h    | Fault indicator         |
| 18    | FAULT_DETECT_ENABLE  | R/W    | 0h    | Fault detect enable     |
| 17    | INT_TEST_ENABLE      | R/W    | 0h    | Interrupt test enable   |
| 16    | RESERVED             | NONE   | 0h    | Reserved                |
| 15:0  | CLKDIV               | R/W    | FFh   | Clock divider           |

#### 4.2.2.360 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_ALIVE\_REG Register

##### 1 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_ALIVE\_REG Register (Offset = 8h) [reset = 0h]

Alive\_reg.

Return to [Summary Table](#)

**Table 4-1694. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2408h       |

**Figure 4-554. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_ALIVE\_REG Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ALIVE  |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ALIVE  |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ALIVE  |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ALIVE  |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 4-1696. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_ALIVE\_REG Register Field Descriptions**

| Bit  | Field | Type   | Reset | Description |
|------|-------|--------|-------|-------------|
| 31:0 | ALIVE | R/W1TC | 0h    | MDIO alive  |

#### 4.2.2.361 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_LINK\_REG Register

##### 1 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_LINK\_REG Register (Offset = Ch) [reset = 0h]

Link\_reg.

Return to [Summary Table](#)

**Table 4-1697. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 240Ch       |

**Figure 4-555. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_LINK\_REG Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| LINK |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LINK |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| LINK |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LINK |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 4-1699. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_LINK\_REG Register Field Descriptions**

| Bit  | Field | Type | Reset | Description     |
|------|-------|------|-------|-----------------|
| 31:0 | LINK  | R    | 0h    | MDIO link state |



#### 4.2.2.362 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_LINK\_INT\_RAW\_REG Register

##### 1 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_LINK\_INT\_RAW\_REG Register (Offset = 10h) [reset = 0h]

Link\_int\_raw\_reg.

Return to [Summary Table](#)

**Table 4-1700. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2410h       |

**Figure 4-556. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_LINK\_INT\_RAW\_REG Name Register**

|          |    |    |    |    |    |            |    |
|----------|----|----|----|----|----|------------|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25         | 24 |
| RESERVED |    |    |    |    |    |            |    |
| NONE     |    |    |    |    |    |            |    |
| 0h       |    |    |    |    |    |            |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17         | 16 |
| RESERVED |    |    |    |    |    |            |    |
| NONE     |    |    |    |    |    |            |    |
| 0h       |    |    |    |    |    |            |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9          | 8  |
| RESERVED |    |    |    |    |    |            |    |
| NONE     |    |    |    |    |    |            |    |
| 0h       |    |    |    |    |    |            |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1          | 0  |
| RESERVED |    |    |    |    |    | LINKINTRAW |    |
| NONE     |    |    |    |    |    | R/W1TC     |    |
| 0h       |    |    |    |    |    | 0h         |    |

**Table 4-1702. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_LINK\_INT\_RAW\_REG Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description                      |
|------|------------|--------|-------|----------------------------------|
| 31:2 | RESERVED   | NONE   | 0h    | Reserved                         |
| 1:0  | LINKINTRAW | R/W1TC | 0h    | MDIO link change event raw value |

#### 4.2.2.363 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_LINK\_INT\_MASKED\_REG Register

##### 1 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_LINK\_INT\_MASKED\_REG Register (Offset = 14h) [reset = 0h]

Link\_int\_masked\_reg.

Return to [Summary Table](#)

**Table 4-1703. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2414h       |

**Figure 4-557. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_LINK\_INT\_MASKED\_REG Name Register**

|          |    |    |    |    |    |               |    |
|----------|----|----|----|----|----|---------------|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25            | 24 |
| RESERVED |    |    |    |    |    |               |    |
| NONE     |    |    |    |    |    |               |    |
| 0h       |    |    |    |    |    |               |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17            | 16 |
| RESERVED |    |    |    |    |    |               |    |
| NONE     |    |    |    |    |    |               |    |
| 0h       |    |    |    |    |    |               |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9             | 8  |
| RESERVED |    |    |    |    |    |               |    |
| NONE     |    |    |    |    |    |               |    |
| 0h       |    |    |    |    |    |               |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1             | 0  |
| RESERVED |    |    |    |    |    | LINKINTMASKED |    |
| NONE     |    |    |    |    |    | R/W1TC        |    |
| 0h       |    |    |    |    |    | 0h            |    |

**Table 4-1705. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_LINK\_INT\_MASKED\_REG Register Field Descriptions**

| Bit  | Field         | Type   | Reset | Description                             |
|------|---------------|--------|-------|-----------------------------------------|
| 31:2 | RESERVED      | NONE   | 0h    | Reserved                                |
| 1:0  | LINKINTMASKED | R/W1TC | 0h    | MDIO link change interrupt masked value |

#### 4.2.2.364 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_LINK\_INT\_MASK\_SET\_REG Register

##### 1 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_LINK\_INT\_MASK\_SET\_REG Register (Offset = 18h) [reset = 0h]

Link\_int\_mask\_set\_reg.

Return to [Summary Table](#)

**Table 4-1706. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2418h       |

**Figure 4-558. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_LINK\_INT\_MASK\_SET\_REG Name Register**

|          |    |    |    |    |    |    |                    |
|----------|----|----|----|----|----|----|--------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                 |
| RESERVED |    |    |    |    |    |    |                    |
| NONE     |    |    |    |    |    |    |                    |
| 0h       |    |    |    |    |    |    |                    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
| RESERVED |    |    |    |    |    |    |                    |
| NONE     |    |    |    |    |    |    |                    |
| 0h       |    |    |    |    |    |    |                    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                  |
| RESERVED |    |    |    |    |    |    |                    |
| NONE     |    |    |    |    |    |    |                    |
| 0h       |    |    |    |    |    |    |                    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| RESERVED |    |    |    |    |    |    | LINKINTMASK<br>SET |
| NONE     |    |    |    |    |    |    | R/W1TS             |
| 0h       |    |    |    |    |    |    | 0h                 |

**Table 4-1708. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_LINK\_INT\_MASK\_SET\_REG Register Field Descriptions**

| Bit  | Field          | Type   | Reset | Description                  |
|------|----------------|--------|-------|------------------------------|
| 31:1 | RESERVED       | NONE   | 0h    | Reserved                     |
| 0    | LINKINTMASKSET | R/W1TS | 0h    | MDIO link interrupt mask set |

#### 4.2.2.365 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_LINK\_INT\_MASK\_CLEAR\_REG Register

##### 1 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_LINK\_INT\_MASK\_CLEAR\_REG Register (Offset = 1Ch) [reset = 0h]

Link\_int\_mask\_clear\_reg.

Return to [Summary Table](#)

**Table 4-1709. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 241Ch       |

**Figure 4-559. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_LINK\_INT\_MASK\_CLEAR\_REG Name Register**

|          |    |    |    |    |    |    |                    |
|----------|----|----|----|----|----|----|--------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                 |
| RESERVED |    |    |    |    |    |    |                    |
| NONE     |    |    |    |    |    |    |                    |
| 0h       |    |    |    |    |    |    |                    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
| RESERVED |    |    |    |    |    |    |                    |
| NONE     |    |    |    |    |    |    |                    |
| 0h       |    |    |    |    |    |    |                    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                  |
| RESERVED |    |    |    |    |    |    |                    |
| NONE     |    |    |    |    |    |    |                    |
| 0h       |    |    |    |    |    |    |                    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| RESERVED |    |    |    |    |    |    | LINKINTMASK<br>CLR |
| NONE     |    |    |    |    |    |    | R/W1TC             |
| 0h       |    |    |    |    |    |    | 0h                 |

**Table 4-1711. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_LINK\_INT\_MASK\_CLEAR\_REG Register Field Descriptions**

| Bit  | Field          | Type   | Reset | Description                    |
|------|----------------|--------|-------|--------------------------------|
| 31:1 | RESERVED       | NONE   | 0h    | Reserved                       |
| 0    | LINKINTMASKCLR | R/W1TC | 0h    | MDIO link interrupt mask clear |

#### 4.2.2.366 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_INT\_RAW\_REG Register

##### 1 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_INT\_RAW\_REG Register (Offset = 20h) [reset = 0h]

user\_int\_raw\_reg.

Return to [Summary Table](#)

**Table 4-1712. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2420h       |

**Figure 4-560. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_INT\_RAW\_REG Name Register**

|          |    |    |    |    |    |            |    |
|----------|----|----|----|----|----|------------|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25         | 24 |
| RESERVED |    |    |    |    |    |            |    |
| NONE     |    |    |    |    |    |            |    |
| 0h       |    |    |    |    |    |            |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17         | 16 |
| RESERVED |    |    |    |    |    |            |    |
| NONE     |    |    |    |    |    |            |    |
| 0h       |    |    |    |    |    |            |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9          | 8  |
| RESERVED |    |    |    |    |    |            |    |
| NONE     |    |    |    |    |    |            |    |
| 0h       |    |    |    |    |    |            |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1          | 0  |
| RESERVED |    |    |    |    |    | USERINTRAW |    |
| NONE     |    |    |    |    |    | R/W1TC     |    |
| 0h       |    |    |    |    |    | 0h         |    |

**Table 4-1714. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_INT\_RAW\_REG Register Field Descriptions**

| Bit  | Field      | Type   | Reset | Description        |
|------|------------|--------|-------|--------------------|
| 31:2 | RESERVED   | NONE   | 0h    | Reserved           |
| 1:0  | USERINTRAW | R/W1TC | 0h    | User interrupt raw |

#### 4.2.2.367 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_INT\_MASKED\_REG Register

##### 1 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_INT\_MASKED\_REG Register (Offset = 24h) [reset = 0h]

user\_int\_masked\_reg.

Return to [Summary Table](#)

**Table 4-1715. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2424h       |

**Figure 4-561. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_INT\_MASKED\_REG Name Register**

|          |    |    |    |    |    |               |    |
|----------|----|----|----|----|----|---------------|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25            | 24 |
| RESERVED |    |    |    |    |    |               |    |
| NONE     |    |    |    |    |    |               |    |
| 0h       |    |    |    |    |    |               |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17            | 16 |
| RESERVED |    |    |    |    |    |               |    |
| NONE     |    |    |    |    |    |               |    |
| 0h       |    |    |    |    |    |               |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9             | 8  |
| RESERVED |    |    |    |    |    |               |    |
| NONE     |    |    |    |    |    |               |    |
| 0h       |    |    |    |    |    |               |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1             | 0  |
| RESERVED |    |    |    |    |    | USERINTMASKED |    |
| NONE     |    |    |    |    |    | R/W1TC        |    |
| 0h       |    |    |    |    |    | 0h            |    |

**Table 4-1717. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_INT\_MASKED\_REG Register Field Descriptions**

| Bit  | Field         | Type   | Reset | Description           |
|------|---------------|--------|-------|-----------------------|
| 31:2 | RESERVED      | NONE   | 0h    | Reserved              |
| 1:0  | USERINTMASKED | R/W1TC | 0h    | User interrupt masked |

#### 4.2.2.368 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_INT\_MASK\_SET\_REG Register

##### 1 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_INT\_MASK\_SET\_REG Register (Offset = 28h) [reset = 0h]

user\_int\_mask\_set\_reg.

Return to [Summary Table](#)

**Table 4-1718. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2428h       |

**Figure 4-562. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_INT\_MASK\_SET\_REG Name Register**

|          |    |    |    |    |    |                |    |
|----------|----|----|----|----|----|----------------|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25             | 24 |
| RESERVED |    |    |    |    |    |                |    |
| NONE     |    |    |    |    |    |                |    |
| 0h       |    |    |    |    |    |                |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17             | 16 |
| RESERVED |    |    |    |    |    |                |    |
| NONE     |    |    |    |    |    |                |    |
| 0h       |    |    |    |    |    |                |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9              | 8  |
| RESERVED |    |    |    |    |    |                |    |
| NONE     |    |    |    |    |    |                |    |
| 0h       |    |    |    |    |    |                |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1              | 0  |
| RESERVED |    |    |    |    |    | USERINTMASKSET |    |
| NONE     |    |    |    |    |    | R/W1TS         |    |
| 0h       |    |    |    |    |    | 0h             |    |

**Table 4-1720. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_INT\_MASK\_SET\_REG Register Field Descriptions**

| Bit  | Field          | Type   | Reset | Description                  |
|------|----------------|--------|-------|------------------------------|
| 31:2 | RESERVED       | NONE   | 0h    | Reserved                     |
| 1:0  | USERINTMASKSET | R/W1TS | 0h    | MDIO user interrupt mask set |

#### 4.2.2.369 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_INT\_MASK\_CLEAR\_REG Register

##### 1 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_INT\_MASK\_CLEAR\_REG Register (Offset = 2Ch) [reset = 0h]

user\_int\_mask\_clear\_reg.

Return to [Summary Table](#)

**Table 4-1721. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 242Ch       |

**Figure 4-563. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_INT\_MASK\_CLEAR\_REG Name Register**

|          |    |    |    |    |    |                |    |
|----------|----|----|----|----|----|----------------|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25             | 24 |
| RESERVED |    |    |    |    |    |                |    |
| NONE     |    |    |    |    |    |                |    |
| 0h       |    |    |    |    |    |                |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17             | 16 |
| RESERVED |    |    |    |    |    |                |    |
| NONE     |    |    |    |    |    |                |    |
| 0h       |    |    |    |    |    |                |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9              | 8  |
| RESERVED |    |    |    |    |    |                |    |
| NONE     |    |    |    |    |    |                |    |
| 0h       |    |    |    |    |    |                |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1              | 0  |
| RESERVED |    |    |    |    |    | USERINTMASKCLR |    |
| NONE     |    |    |    |    |    | R/W1TC         |    |
| 0h       |    |    |    |    |    | 0h             |    |

**Table 4-1723. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_INT\_MASK\_CLEAR\_REG Register Field Descriptions**

| Bit  | Field          | Type   | Reset | Description                    |
|------|----------------|--------|-------|--------------------------------|
| 31:2 | RESERVED       | NONE   | 0h    | Reserved                       |
| 1:0  | USERINTMASKCLR | R/W1TC | 0h    | MDIO user interrupt mask clear |



#### 4.2.2.370 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_MANUAL\_IF\_REG Register

##### 1 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_MANUAL\_IF\_REG Register (Offset = 30h) [reset = 0h]

manual\_if\_reg.

Return to [Summary Table](#)

**Table 4-1724. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2430h       |

**Figure 4-564. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_MANUAL\_IF\_REG Name Register**

|          |    |    |    |    |              |         |          |
|----------|----|----|----|----|--------------|---------|----------|
| 31       | 30 | 29 | 28 | 27 | 26           | 25      | 24       |
| RESERVED |    |    |    |    |              |         |          |
| NONE     |    |    |    |    |              |         |          |
| 0h       |    |    |    |    |              |         |          |
| 23       | 22 | 21 | 20 | 19 | 18           | 17      | 16       |
| RESERVED |    |    |    |    |              |         |          |
| NONE     |    |    |    |    |              |         |          |
| 0h       |    |    |    |    |              |         |          |
| 15       | 14 | 13 | 12 | 11 | 10           | 9       | 8        |
| RESERVED |    |    |    |    |              |         |          |
| NONE     |    |    |    |    |              |         |          |
| 0h       |    |    |    |    |              |         |          |
| 7        | 6  | 5  | 4  | 3  | 2            | 1       | 0        |
| RESERVED |    |    |    |    | MDIO_MDCLK_O | MDIO_OE | MDIO_PIN |
| NONE     |    |    |    |    | R/W          | R/W     | R/W      |
| 0h       |    |    |    |    | 0h           | 0h      | 0h       |

**Table 4-1726. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_MANUAL\_IF\_REG Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description        |
|------|--------------|------|-------|--------------------|
| 31:3 | RESERVED     | NONE | 0h    | Reserved           |
| 2    | MDIO_MDCLK_O | R/W  | 0h    | MDIO Clock Output  |
| 1    | MDIO_OE      | R/W  | 0h    | MDIO Output Enable |
| 0    | MDIO_PIN     | R/W  | 0h    | MDIO Pin           |

#### 4.2.2.371 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_POLL\_REG Register

##### 1 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_POLL\_REG Register (Offset = 34h) [reset = 0h]

poll\_reg.

Return to [Summary Table](#)

**Table 4-1727. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2434h       |

**Figure 4-565. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_POLL\_REG Name Register**

|            |                     |          |    |    |    |    |    |
|------------|---------------------|----------|----|----|----|----|----|
| 31         | 30                  | 29       | 28 | 27 | 26 | 25 | 24 |
| MANUALMODE | STATECHANG<br>EMODE | RESERVED |    |    |    |    |    |
| R/W        | R/W                 | NONE     |    |    |    |    |    |
| 0h         | 0h                  | 0h       |    |    |    |    |    |
| 23         | 22                  | 21       | 20 | 19 | 18 | 17 | 16 |
| RESERVED   |                     |          |    |    |    |    |    |
| NONE       |                     |          |    |    |    |    |    |
| 0h         |                     |          |    |    |    |    |    |
| 15         | 14                  | 13       | 12 | 11 | 10 | 9  | 8  |
| RESERVED   |                     |          |    |    |    |    |    |
| NONE       |                     |          |    |    |    |    |    |
| 0h         |                     |          |    |    |    |    |    |
| 7          | 6                   | 5        | 4  | 3  | 2  | 1  | 0  |
| IPG        |                     |          |    |    |    |    |    |
| R/W        |                     |          |    |    |    |    |    |
| 0h         |                     |          |    |    |    |    |    |

**Table 4-1729. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_POLL\_REG Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description            |
|------|-----------------|------|-------|------------------------|
| 31   | MANUALMODE      | R/W  | 0h    | MDIO Manual Mode       |
| 30   | STATECHANGEMODE | R/W  | 0h    | MDIO State Change Mode |
| 29:8 | RESERVED        | NONE | 0h    | Reserved               |
| 7:0  | IPG             | R/W  | 0h    | MDIO IPG               |

#### 4.2.2.372 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_POLL\_EN\_REG Register

##### 1 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_POLL\_EN\_REG Register (Offset = 38h) [reset = FFFFFFFFh]

poll\_en\_reg.

Return to [Summary Table](#)

**Table 4-1730. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2438h       |

**Figure 4-566. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_POLL\_EN\_REG Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| POLL_EN   |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| FFFFFFFFh |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| POLL_EN   |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| FFFFFFFFh |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| POLL_EN   |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| FFFFFFFFh |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| POLL_EN   |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| FFFFFFFFh |    |    |    |    |    |    |    |

**Table 4-1732. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_POLL\_EN\_REG Register Field Descriptions**

| Bit  | Field   | Type | Reset     | Description      |
|------|---------|------|-----------|------------------|
| 31:0 | POLL_EN | R/W  | FFFFFFFFh | MDIO Poll Enable |

#### 4.2.2.373 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_CLAUS45\_REG Register

##### 1 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_CLAUS45\_REG Register (Offset = 3Ch) [reset = 0h]

clause 45\_reg

Return to [Summary Table](#)

**Table 4-1733. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 243Ch       |

**Figure 4-567. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_CLAUS45\_REG Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CLAUSE45 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CLAUSE45 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CLAUSE45 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CLAUSE45 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1735. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_CLAUS45\_REG Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description    |
|------|----------|------|-------|----------------|
| 31:0 | CLAUSE45 | R/W  | 0h    | MDIO Clause 45 |

#### 4.2.2.374 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_ADDR0\_REG Register

##### 1 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_ADDR0\_REG Register (Offset = 40h) [reset = 0h]

MDIO USER Address 0

Return to [Summary Table](#)

**Table 4-1736. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2440h       |

**Figure 4-568. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_ADDR0\_REG Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| USER_ADDR0 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| USER_ADDR0 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 4-1738. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_ADDR0\_REG Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description         |
|-------|------------|------|-------|---------------------|
| 31:16 | RESERVED   | NONE | 0h    | Reserved            |
| 15:0  | USER_ADDR0 | R/W  | 0h    | MDIO USER Address 0 |

#### 4.2.2.375 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_ADDR1\_REG Register

##### 1 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_ADDR1\_REG Register (Offset = 44h) [reset = 0h]

MDIO USER Address 1

Return to [Summary Table](#)

**Table 4-1739. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 2444h       |

**Figure 4-569. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_ADDR1\_REG Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| USER_ADDR1 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| USER_ADDR1 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 4-1741. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_ADDR1\_REG Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description         |
|-------|------------|------|-------|---------------------|
| 31:16 | RESERVED   | NONE | 0h    | Reserved            |
| 15:0  | USER_ADDR1 | R/W  | 0h    | MDIO USER Address 1 |

#### 4.2.2.376 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_GROUP\_USER\_ACCESS\_REG\_J Register

**1 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_GROUP\_USER\_ACCESS\_REG\_J Register (Offset = 80h) [reset = 0h]**

user\_access\_reg

Return to [Summary Table](#)

Offset = Base + (j \* 8h); where j = 0 to 1d

**Table 4-1742. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ICSSM0        | 4803 2480h + formula |

**Figure 4-570. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_GROUP\_USER\_ACCESS\_REG\_J Name Register**

| 31     | 30    | 29  | 28       | 27 | 26 | 25     | 24 |
|--------|-------|-----|----------|----|----|--------|----|
| GO     | WRITE | ACK | RESERVED |    |    | REGADR |    |
| R/W1TS | R/W   | R/W | NONE     |    |    | R/W    |    |
| 0h     | 0h    | 0h  | 0h       |    |    | 0h     |    |
| 23     | 22    | 21  | 20       | 19 | 18 | 17     | 16 |
| REGADR |       |     | PHYADR   |    |    |        |    |
| R/W    |       |     | R/W      |    |    |        |    |
| 0h     |       |     | 0h       |    |    |        |    |
| 15     | 14    | 13  | 12       | 11 | 10 | 9      | 8  |
| DATA   |       |     |          |    |    |        |    |
| R/W    |       |     |          |    |    |        |    |
| 0h     |       |     |          |    |    |        |    |
| 7      | 6     | 5   | 4        | 3  | 2  | 1      | 0  |
| DATA   |       |     |          |    |    |        |    |
| R/W    |       |     |          |    |    |        |    |
| 0h     |       |     |          |    |    |        |    |

**Table 4-1744. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_GROUP\_USER\_ACCESS\_REG\_J Register Field Descriptions**

| Bit   | Field    | Type   | Reset | Description      |
|-------|----------|--------|-------|------------------|
| 31    | GO       | R/W1TS | 0h    | Go               |
| 30    | WRITE    | R/W    | 0h    | Write            |
| 29    | ACK      | R/W    | 0h    | Acknowledge      |
| 28:26 | RESERVED | NONE   | 0h    | Reserved         |
| 25:21 | REGADR   | R/W    | 0h    | Register address |
| 20:16 | PHYADR   | R/W    | 0h    | PHY address      |
| 15:0  | DATA     | R/W    | 0h    | User data        |

#### 4.2.2.377 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_GROUP\_USER\_PHY\_SEL\_REG\_J Register

**1 ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_GROUP\_USER\_PHY\_SEL\_REG\_J Register (Offset = 84h) [reset = 0h]**

user\_phy\_sel\_reg

Return to [Summary Table](#)

Offset = Base + (j \* 8h); where j = 0 to 1d

**Table 4-1745. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ICSSM0        | 4803 2484h + formula |

**Figure 4-571. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_GROUP\_USER\_PHY\_SEL\_REG\_J Name Register**

|          |                |          |            |    |    |    |    |
|----------|----------------|----------|------------|----|----|----|----|
| 31       | 30             | 29       | 28         | 27 | 26 | 25 | 24 |
| RESERVED |                |          |            |    |    |    |    |
| NONE     |                |          |            |    |    |    |    |
| 0h       |                |          |            |    |    |    |    |
| 23       | 22             | 21       | 20         | 19 | 18 | 17 | 16 |
| RESERVED |                |          |            |    |    |    |    |
| NONE     |                |          |            |    |    |    |    |
| 0h       |                |          |            |    |    |    |    |
| 15       | 14             | 13       | 12         | 11 | 10 | 9  | 8  |
| RESERVED |                |          |            |    |    |    |    |
| NONE     |                |          |            |    |    |    |    |
| 0h       |                |          |            |    |    |    |    |
| 7        | 6              | 5        | 4          | 3  | 2  | 1  | 0  |
| LINKSEL  | LINKINT_ENABLE | RESERVED | PHYADR_MON |    |    |    |    |
| R/W      | R/W            | NONE     | R/W        |    |    |    |    |
| 0h       | 0h             | 0h       | 0h         |    |    |    |    |

**Table 4-1747. ICSSM\_PR1\_MDIO\_V1P7\_MDIO\_USER\_GROUP\_USER\_PHY\_SEL\_REG\_J Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                |
|------|----------------|------|-------|--------------------------------------------|
| 31:8 | RESERVED       | NONE | 0h    | Reserved                                   |
| 7    | LINKSEL        | R/W  | 0h    | Link status determination select           |
| 6    | LINKINT_ENABLE | R/W  | 0h    | Link change interrupt enable               |
| 5    | RESERVED       | NONE | 0h    | Reserved                                   |
| 4:0  | PHYADR_MON     | R/W  | 0h    | PHY address whose link status is monitored |



#### 4.2.2.378 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_ICSS\_G\_CFG Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_ICSS\_G\_CFG Register (Offset = 0h) [reset = 1h]

ICSS\_G Ethernet Cfg.

Return to [Summary Table](#)

**Table 4-1748. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3000h       |

**Figure 4-572. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_ICSS\_G\_CFG Name Register**

|          |           |    |           |    |                      |          |          |
|----------|-----------|----|-----------|----|----------------------|----------|----------|
| 31       | 30        | 29 | 28        | 27 | 26                   | 25       | 24       |
| RESERVED |           |    |           |    |                      |          |          |
| NONE     |           |    |           |    |                      |          |          |
| 0h       |           |    |           |    |                      |          |          |
| 23       | 22        | 21 | 20        | 19 | 18                   | 17       | 16       |
| RESERVED |           |    |           |    |                      |          |          |
| NONE     |           |    |           |    |                      |          |          |
| 0h       |           |    |           |    |                      |          |          |
| 15       | 14        | 13 | 12        | 11 | 10                   | 9        | 8        |
| RESERVED |           |    |           |    | RX_SFD_TX_S<br>OF_EN | RESERVED |          |
| NONE     |           |    |           |    | R/W                  | NONE     |          |
| 0h       |           |    |           |    | 0h                   | 0h       |          |
| 7        | 6         | 5  | 4         | 3  | 2                    | 1        | 0        |
| RESERVED | MII1_MODE |    | MII0_MODE |    | RX_L2_G_EN           | TX_L2_EN | TX_L1_EN |
| NONE     | R/W       |    | R/W       |    | R/W                  | R/W      | R/W      |
| 0h       | 0h        |    | 0h        |    | 0h                   | 0h       | 1h       |

**Table 4-1750. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_ICSS\_G\_CFG Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                               |
|-------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------|
| 31:11 | RESERVED         | NONE | 0h    | Reserved                                                                                                  |
| 10    | RX_SFD_TX_SOF_EN | R/W  | 0h    | Enable the remapping of tx_sof to rx_sfd if auto fwd is enable                                            |
| 9:7   | RESERVED         | NONE | 0h    | Reserved                                                                                                  |
| 6:5   | MII1_MODE        | R/W  | 0h    | MII1 MODE<br>0:MII<br>1:RGMII<br>2:SGMII                                                                  |
| 4:3   | MII0_MODE        | R/W  | 0h    | MII0 MODE<br>0:MII<br>1:RGMII<br>2:SGMII                                                                  |
| 2     | RX_L2_G_EN       | R/W  | 0h    | Enable the RX L2 G features of filter frags of size TBD and backpressure RX L2<br>0:Disabled<br>1:Enabled |
| 1     | TX_L2_EN         | R/W  | 0h    | Enable the TX L2 Fifo<br>0:Disabled<br>1:Enabled                                                          |

**Table 4-1750. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_ICSS\_G\_CFG Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                                      |
|-----|----------|------|-------|--------------------------------------------------|
| 0   | TX_L1_EN | R/W  | 1h    | Enable the TX L1 Fifo<br>0:Disabled<br>1:Enabled |

#### 4.2.2.379 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_PREEMPT\_CFG Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_PREEMPT\_CFG Register (Offset = 4h) [reset = 1907D500h]**

Preemption\_Cfg

Return to [Summary Table](#)

**Table 4-1751. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3004h       |

**Figure 4-573. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_PREEMPT\_CFG Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SMD_R    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 19h      |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SMD_V    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 7h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| EXP_SMD  |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| D5h      |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1753. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_PREEMPT\_CFG Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                    |
|-------|----------|------|-------|------------------------------------------------|
| 31:24 | SMD_R    | R/W  | 19h   | Response frame TAG                             |
| 23:16 | SMD_V    | R/W  | 7h    | Verification frame TAG                         |
| 15:8  | EXP_SMD  | R/W  | D5h   | None preemptable frame start, or express frame |
| 7:0   | RESERVED | NONE | 0h    | Reserved                                       |

#### 4.2.2.380 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_SMDT1S\_CFG Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_SMDT1S\_CFG Register (Offset = 8h) [reset = B37F4CE6h]**

SMDType1SPreemptableFrameStartCfg

Return to [Summary Table](#)

**Table 4-1754. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3008h       |

**Figure 4-574. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_SMDT1S\_CFG Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SMDT1S_3 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| B3h      |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SMDT1S_2 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 7Fh      |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SMDT1S_1 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 4Ch      |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SMDT1S_0 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| E6h      |    |    |    |    |    |    |    |

**Table 4-1756. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_SMDT1S\_CFG Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description     |
|-------|----------|------|-------|-----------------|
| 31:24 | SMDT1S_3 | R/W  | B3h   | SMDT1S3 pattern |
| 23:16 | SMDT1S_2 | R/W  | 7Fh   | SMDT1S2 pattern |
| 15:8  | SMDT1S_1 | R/W  | 4Ch   | SMDT1S1 pattern |
| 7:0   | SMDT1S_0 | R/W  | E6h   | SMDT1S0 pattern |

#### 4.2.2.381 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_SMDT1C\_CFG Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_SMDT1C\_CFG Register (Offset = Ch) [reset = 2A9E5261h]**

SMDType1CNoneInitialFragCfg

Return to [Summary Table](#)

**Table 4-1757. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 300Ch       |

**Figure 4-575. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_SMDT1C\_CFG Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SMDT1C_3 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 2Ah      |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SMDT1C_2 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 9Eh      |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SMDT1C_1 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 52h      |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SMDT1C_0 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 61h      |    |    |    |    |    |    |    |

**Table 4-1759. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_SMDT1C\_CFG Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description     |
|-------|----------|------|-------|-----------------|
| 31:24 | SMDT1C_3 | R/W  | 2Ah   | SMDT1C3 pattern |
| 23:16 | SMDT1C_2 | R/W  | 9Eh   | SMDT1C2 pattern |
| 15:8  | SMDT1C_1 | R/W  | 52h   | SMDT1C1 pattern |
| 7:0   | SMDT1C_0 | R/W  | 61h   | SMDT1C0 pattern |

#### 4.2.2.382 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_POOL\_PTR\_CFG Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_POOL\_PTR\_CFG Register (Offset = 10h) [reset = 800h]**

PoolPtrCfg

Return to [Summary Table](#)

**Table 4-1760. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3010h       |

**Figure 4-576. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_POOL\_PTR\_CFG Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED     |    |    |    |    |    |    |    |
| NONE         |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED     |    |    |    |    |    |    |    |
| NONE         |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MAX_PKT_SIZE |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 800h         |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MAX_PKT_SIZE |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 800h         |    |    |    |    |    |    |    |

**Table 4-1762. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_POOL\_PTR\_CFG Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                          |
|-------|--------------|------|-------|------------------------------------------------------|
| 31:16 | RESERVED     | NONE | 0h    | Reserved                                             |
| 15:0  | MAX_PKT_SIZE | R/W  | 800h  | Max Pkt Size, used in pool ptr logic for wrap around |

#### 4.2.2.383 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_TX\_EARLY\_EOF Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_TX\_EARLY\_EOF Register (Offset = 14h) [reset = 0h]**

TX Early EOF Enable Reserved

Return to [Summary Table](#)

**Table 4-1763. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3014h       |

**Figure 4-577. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_TX\_EARLY\_EOF Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-1765. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_TX\_EARLY\_EOF Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |

#### 4.2.2.384 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_FRAG\_CNT\_CFG Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_FRAG\_CNT\_CFG Register (Offset = 18h) [reset = B37F4CE6h]**

FragCntCfg

Return to [Summary Table](#)

**Table 4-1766. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3018h       |

**Figure 4-578. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_FRAG\_CNT\_CFG Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FRAG_CNT_3 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| B3h        |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FRAG_CNT_2 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 7Fh        |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FRAG_CNT_1 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 4Ch        |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FRAG_CNT_0 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| E6h        |    |    |    |    |    |    |    |

**Table 4-1768. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_FRAG\_CNT\_CFG Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description       |
|-------|------------|------|-------|-------------------|
| 31:24 | FRAG_CNT_3 | R/W  | B3h   | FRAG Cnt3 pattern |
| 23:16 | FRAG_CNT_2 | R/W  | 7Fh   | FRAG Cnt2 pattern |
| 15:8  | FRAG_CNT_1 | R/W  | 4Ch   | FRAG Cnt1 pattern |
| 7:0   | FRAG_CNT_0 | R/W  | E6h   | FRAG Cnt0 pattern |



#### 4.2.2.385 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE0 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE0 Register (Offset = D00h) [reset = 0h]

Queue0

Return to [Summary Table](#)

**Table 4-1769. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D00h       |

**Figure 4-579. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE0 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED     |    |    |    |    |    |    |    |
| NONE         |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED     |    |    |    |    |    |    |    |
| NONE         |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 4-1771. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE0 Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description |
|-------|--------------|------|-------|-------------|
| 31:16 | RESERVED     | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR0 | R/W  | 0h    | Queue 0     |

#### 4.2.2.386 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE1 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE1 Register (Offset = D04h) [reset = 0h]

Queue1

Return to [Summary Table](#)

**Table 4-1772. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D04h       |

**Figure 4-580. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE1 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED     |    |    |    |    |    |    |    |
| NONE         |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED     |    |    |    |    |    |    |    |
| NONE         |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR1 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR1 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 4-1774. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE1 Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description |
|-------|--------------|------|-------|-------------|
| 31:16 | RESERVED     | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR1 | R/W  | 0h    | Queue 1     |

#### 4.2.2.387 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE2 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE2 Register (Offset = D08h) [reset = 0h]

Queue2

Return to [Summary Table](#)

**Table 4-1775. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D08h       |

**Figure 4-581. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE2 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED     |    |    |    |    |    |    |    |
| NONE         |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED     |    |    |    |    |    |    |    |
| NONE         |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR2 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR2 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 4-1777. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE2 Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description |
|-------|--------------|------|-------|-------------|
| 31:16 | RESERVED     | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR2 | R/W  | 0h    | Queue 2     |

#### 4.2.2.388 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE3 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE3 Register (Offset = D0Ch) [reset = 0h]

Queue3

Return to [Summary Table](#)

**Table 4-1778. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D0Ch       |

**Figure 4-582. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE3 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED     |    |    |    |    |    |    |    |
| NONE         |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED     |    |    |    |    |    |    |    |
| NONE         |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR3 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR3 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 4-1780. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE3 Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description |
|-------|--------------|------|-------|-------------|
| 31:16 | RESERVED     | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR3 | R/W  | 0h    | Queue 3     |

#### 4.2.2.389 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE4 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE4 Register (Offset = D10h) [reset = 0h]

Queue4

Return to [Summary Table](#)

**Table 4-1781. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D10h       |

**Figure 4-583. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE4 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED     |    |    |    |    |    |    |    |
| NONE         |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED     |    |    |    |    |    |    |    |
| NONE         |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR4 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR4 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 4-1783. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE4 Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description |
|-------|--------------|------|-------|-------------|
| 31:16 | RESERVED     | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR4 | R/W  | 0h    | Queue 4     |

#### 4.2.2.390 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE5 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE5 Register (Offset = D14h) [reset = 0h]

Queue5

Return to [Summary Table](#)

**Table 4-1784. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D14h       |

**Figure 4-584. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE5 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED     |    |    |    |    |    |    |    |
| NONE         |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED     |    |    |    |    |    |    |    |
| NONE         |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR5 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR5 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 4-1786. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE5 Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description |
|-------|--------------|------|-------|-------------|
| 31:16 | RESERVED     | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR5 | R/W  | 0h    | Queue 5     |

#### 4.2.2.391 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE6 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE6 Register (Offset = D18h) [reset = 0h]

Queue6

Return to [Summary Table](#)

**Table 4-1787. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D18h       |

**Figure 4-585. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE6 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED     |    |    |    |    |    |    |    |
| NONE         |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED     |    |    |    |    |    |    |    |
| NONE         |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR6 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR6 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 4-1789. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE6 Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description |
|-------|--------------|------|-------|-------------|
| 31:16 | RESERVED     | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR6 | R/W  | 0h    | Queue 6     |

#### 4.2.2.392 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE7 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE7 Register (Offset = D1Ch) [reset = 0h]

Queue7

Return to [Summary Table](#)

**Table 4-1790. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D1Ch       |

**Figure 4-586. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE7 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED     |    |    |    |    |    |    |    |
| NONE         |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED     |    |    |    |    |    |    |    |
| NONE         |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR7 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR7 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 4-1792. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE7 Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description |
|-------|--------------|------|-------|-------------|
| 31:16 | RESERVED     | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR7 | R/W  | 0h    | Queue 7     |



#### 4.2.2.393 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE8 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE8 Register (Offset = D20h) [reset = 0h]

Queue8

Return to [Summary Table](#)

**Table 4-1793. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D20h       |

**Figure 4-587. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE8 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED     |    |    |    |    |    |    |    |
| NONE         |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED     |    |    |    |    |    |    |    |
| NONE         |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR8 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR8 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 4-1795. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE8 Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description |
|-------|--------------|------|-------|-------------|
| 31:16 | RESERVED     | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR8 | R/W  | 0h    | Queue 8     |

#### 4.2.2.394 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE9 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE9 Register (Offset = D24h) [reset = 0h]

Queue9

Return to [Summary Table](#)

**Table 4-1796. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D24h       |

**Figure 4-588. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE9 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED     |    |    |    |    |    |    |    |
| NONE         |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED     |    |    |    |    |    |    |    |
| NONE         |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR9 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR9 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 4-1798. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE9 Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description |
|-------|--------------|------|-------|-------------|
| 31:16 | RESERVED     | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR9 | R/W  | 0h    | Queue 9     |

#### 4.2.2.395 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE10 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE10 Register (Offset = D28h) [reset = 0h]

Queue10

Return to [Summary Table](#)

**Table 4-1799. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D28h       |

**Figure 4-589. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE10 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR10 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR10 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 4-1801. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE10 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description |
|-------|---------------|------|-------|-------------|
| 31:16 | RESERVED      | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR10 | R/W  | 0h    | Queue 10    |

#### 4.2.2.396 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE11 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE11 Register (Offset = D2Ch) [reset = 0h]

Queue11

Return to [Summary Table](#)

**Table 4-1802. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D2Ch       |

**Figure 4-590. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE11 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR11 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR11 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 4-1804. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE11 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description |
|-------|---------------|------|-------|-------------|
| 31:16 | RESERVED      | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR11 | R/W  | 0h    | Queue 11    |

#### 4.2.2.397 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE12 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE12 Register (Offset = D30h) [reset = 0h]

Queue12

Return to [Summary Table](#)

**Table 4-1805. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D30h       |

**Figure 4-591. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE12 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR12 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR12 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 4-1807. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE12 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description |
|-------|---------------|------|-------|-------------|
| 31:16 | RESERVED      | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR12 | R/W  | 0h    | Queue 12    |

#### 4.2.2.398 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE13 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE13 Register (Offset = D34h) [reset = 0h]

Queue13

Return to [Summary Table](#)

**Table 4-1808. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D34h       |

**Figure 4-592. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE13 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR13 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR13 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 4-1810. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE13 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description |
|-------|---------------|------|-------|-------------|
| 31:16 | RESERVED      | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR13 | R/W  | 0h    | Queue 13    |

#### 4.2.2.399 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE14 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE14 Register (Offset = D38h) [reset = 0h]

Queue14

Return to [Summary Table](#)

**Table 4-1811. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D38h       |

**Figure 4-593. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE14 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR14 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR14 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 4-1813. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE14 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description |
|-------|---------------|------|-------|-------------|
| 31:16 | RESERVED      | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR14 | R/W  | 0h    | Queue 14    |

#### 4.2.2.400 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE15 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE15 Register (Offset = D3Ch) [reset = 0h]

Queue15

Return to [Summary Table](#)

**Table 4-1814. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D3Ch       |

**Figure 4-594. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE15 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR15 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR15 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 4-1816. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE15 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description |
|-------|---------------|------|-------|-------------|
| 31:16 | RESERVED      | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR15 | R/W  | 0h    | Queue 15    |



#### 4.2.2.401 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE16 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE16 Register (Offset = D40h) [reset = 0h]

Queue16

Return to [Summary Table](#)

**Table 4-1817. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D40h       |

**Figure 4-595. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE16 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR16 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR16 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 4-1819. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE16 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description |
|-------|---------------|------|-------|-------------|
| 31:16 | RESERVED      | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR16 | R/W  | 0h    | Queue 16    |

#### 4.2.2.402 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE17 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE17 Register (Offset = D44h) [reset = 0h]

Queue17

Return to [Summary Table](#)

**Table 4-1820. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D44h       |

**Figure 4-596. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE17 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR17 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR17 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 4-1822. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE17 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description |
|-------|---------------|------|-------|-------------|
| 31:16 | RESERVED      | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR17 | R/W  | 0h    | Queue 17    |

#### 4.2.2.403 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE18 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE18 Register (Offset = D48h) [reset = 0h]

Queue18

Return to [Summary Table](#)

**Table 4-1823. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D48h       |

**Figure 4-597. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE18 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR18 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR18 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 4-1825. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE18 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description |
|-------|---------------|------|-------|-------------|
| 31:16 | RESERVED      | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR18 | R/W  | 0h    | Queue 18    |

#### 4.2.2.404 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE19 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE19 Register (Offset = D4Ch) [reset = 0h]

Queue19

Return to [Summary Table](#)

**Table 4-1826. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D4Ch       |

**Figure 4-598. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE19 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR19 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR19 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 4-1828. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE19 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description |
|-------|---------------|------|-------|-------------|
| 31:16 | RESERVED      | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR19 | R/W  | 0h    | Queue 19    |

#### 4.2.2.405 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE20 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE20 Register (Offset = D50h) [reset = 0h]

Queue20

Return to [Summary Table](#)

**Table 4-1829. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D50h       |

**Figure 4-599. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE20 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR20 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR20 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 4-1831. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE20 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description |
|-------|---------------|------|-------|-------------|
| 31:16 | RESERVED      | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR20 | R/W  | 0h    | Queue 20    |

#### 4.2.2.406 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE21 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE21 Register (Offset = D54h) [reset = 0h]

Queue21

Return to [Summary Table](#)

**Table 4-1832. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D54h       |

**Figure 4-600. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE21 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR21 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR21 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 4-1834. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE21 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description |
|-------|---------------|------|-------|-------------|
| 31:16 | RESERVED      | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR21 | R/W  | 0h    | Queue 21    |

#### 4.2.2.407 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE22 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE22 Register (Offset = D58h) [reset = 0h]

Queue22

Return to [Summary Table](#)

**Table 4-1835. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D58h       |

**Figure 4-601. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE22 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR22 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR22 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 4-1837. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE22 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description |
|-------|---------------|------|-------|-------------|
| 31:16 | RESERVED      | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR22 | R/W  | 0h    | Queue 22    |

#### 4.2.2.408 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE23 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE23 Register (Offset = D5Ch) [reset = 0h]

Queue23

Return to [Summary Table](#)

**Table 4-1838. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D5Ch       |

**Figure 4-602. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE23 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR23 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR23 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 4-1840. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE23 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description |
|-------|---------------|------|-------|-------------|
| 31:16 | RESERVED      | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR23 | R/W  | 0h    | Queue 23    |



#### 4.2.2.409 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE24 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE24 Register (Offset = D60h) [reset = 0h]

Queue24

Return to [Summary Table](#)

**Table 4-1841. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D60h       |

**Figure 4-603. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE24 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR24 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR24 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 4-1843. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE24 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description |
|-------|---------------|------|-------|-------------|
| 31:16 | RESERVED      | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR24 | R/W  | 0h    | Queue 24    |

#### 4.2.2.410 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE25 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE25 Register (Offset = D64h) [reset = 0h]

Queue25

Return to [Summary Table](#)

**Table 4-1844. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D64h       |

**Figure 4-604. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE25 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR25 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR25 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 4-1846. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE25 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description |
|-------|---------------|------|-------|-------------|
| 31:16 | RESERVED      | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR25 | R/W  | 0h    | Queue 25    |

#### 4.2.2.411 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE26 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE26 Register (Offset = D68h) [reset = 0h]

Queue26

Return to [Summary Table](#)

**Table 4-1847. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D68h       |

**Figure 4-605. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE26 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR26 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR26 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 4-1849. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE26 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description |
|-------|---------------|------|-------|-------------|
| 31:16 | RESERVED      | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR26 | R/W  | 0h    | Queue 26    |

#### 4.2.2.412 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE27 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE27 Register (Offset = D6Ch) [reset = 0h]

Queue27

Return to [Summary Table](#)

**Table 4-1850. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D6Ch       |

**Figure 4-606. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE27 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR27 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR27 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 4-1852. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE27 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description |
|-------|---------------|------|-------|-------------|
| 31:16 | RESERVED      | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR27 | R/W  | 0h    | Queue 27    |

#### 4.2.2.413 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE28 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE28 Register (Offset = D70h) [reset = 0h]

Queue28

Return to [Summary Table](#)

**Table 4-1853. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D70h       |

**Figure 4-607. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE28 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR28 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR28 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 4-1855. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE28 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description |
|-------|---------------|------|-------|-------------|
| 31:16 | RESERVED      | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR28 | R/W  | 0h    | Queue 28    |

#### 4.2.2.414 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE29 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE29 Register (Offset = D74h) [reset = 0h]

Queue29

Return to [Summary Table](#)

**Table 4-1856. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D74h       |

**Figure 4-608. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE29 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR29 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR29 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 4-1858. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE29 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description |
|-------|---------------|------|-------|-------------|
| 31:16 | RESERVED      | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR29 | R/W  | 0h    | Queue 29    |

#### 4.2.2.415 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE30 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE30 Register (Offset = D78h) [reset = 0h]

Queue30

Return to [Summary Table](#)

**Table 4-1859. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D78h       |

**Figure 4-609. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE30 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR30 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR30 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 4-1861. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE30 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description |
|-------|---------------|------|-------|-------------|
| 31:16 | RESERVED      | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR30 | R/W  | 0h    | Queue 30    |

#### 4.2.2.416 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE31 Register

##### 1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE31 Register (Offset = D7Ch) [reset = 0h]

Queue31

Return to [Summary Table](#)

**Table 4-1862. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3D7Ch       |

**Figure 4-610. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE31 Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PTR31 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PTR31 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 4-1864. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE31 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description |
|-------|---------------|------|-------|-------------|
| 31:16 | RESERVED      | NONE | 0h    | Reserved    |
| 15:0  | QUEUE_H_PTR31 | R/W  | 0h    | Queue 31    |



#### 4.2.2.417 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK0 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK0 Register (Offset = E00h) [reset = 0h]**

QueuePeek0

Return to [Summary Table](#)

**Table 4-1865. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E00h       |

**Figure 4-611. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK0 Name Register**

|                   |    |    |    |    |    |    |    |
|-------------------|----|----|----|----|----|----|----|
| 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PEEK_PTR0 |    |    |    |    |    |    |    |
| R                 |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PEEK_PTR0 |    |    |    |    |    |    |    |
| R                 |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |

**Table 4-1867. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK0 Register Field Descriptions**

| Bit   | Field             | Type | Reset | Description         |
|-------|-------------------|------|-------|---------------------|
| 31:16 | RESERVED          | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_H_PEEK_PTR0 | R    | 0h    | Queue 0 Peek portal |

#### 4.2.2.418 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK1 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK1 Register (Offset = E04h) [reset = 0h]**

QueuePeek1

Return to [Summary Table](#)

**Table 4-1868. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E04h       |

**Figure 4-612. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK1 Name Register**

|                   |    |    |    |    |    |    |    |
|-------------------|----|----|----|----|----|----|----|
| 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PEEK_PTR1 |    |    |    |    |    |    |    |
| R                 |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PEEK_PTR1 |    |    |    |    |    |    |    |
| R                 |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |

**Table 4-1870. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK1 Register Field Descriptions**

| Bit   | Field             | Type | Reset | Description         |
|-------|-------------------|------|-------|---------------------|
| 31:16 | RESERVED          | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_H_PEEK_PTR1 | R    | 0h    | Queue 1 Peek portal |

#### 4.2.2.419 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK2 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK2 Register (Offset = E08h) [reset = 0h]**

QueuePeek2

Return to [Summary Table](#)

**Table 4-1871. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E08h       |

**Figure 4-613. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK2 Name Register**

|                   |    |    |    |    |    |    |    |
|-------------------|----|----|----|----|----|----|----|
| 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PEEK_PTR2 |    |    |    |    |    |    |    |
| R                 |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PEEK_PTR2 |    |    |    |    |    |    |    |
| R                 |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |

**Table 4-1873. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK2 Register Field Descriptions**

| Bit   | Field             | Type | Reset | Description         |
|-------|-------------------|------|-------|---------------------|
| 31:16 | RESERVED          | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_H_PEEK_PTR2 | R    | 0h    | Queue 2 Peek portal |

#### 4.2.2.420 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK3 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK3 Register (Offset = E0Ch) [reset = 0h]**

QueuePeek3

Return to [Summary Table](#)

**Table 4-1874. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E0Ch       |

**Figure 4-614. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK3 Name Register**

|                   |    |    |    |    |    |    |    |
|-------------------|----|----|----|----|----|----|----|
| 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PEEK_PTR3 |    |    |    |    |    |    |    |
| R                 |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PEEK_PTR3 |    |    |    |    |    |    |    |
| R                 |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |

**Table 4-1876. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK3 Register Field Descriptions**

| Bit   | Field             | Type | Reset | Description         |
|-------|-------------------|------|-------|---------------------|
| 31:16 | RESERVED          | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_H_PEEK_PTR3 | R    | 0h    | Queue 3 Peek portal |

#### 4.2.2.421 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK4 Register

1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK4 Register (Offset = E10h) [reset = 0h]

QueuePeek4

Return to [Summary Table](#)

**Table 4-1877. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E10h       |

**Figure 4-615. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK4 Name Register**

|                   |    |    |    |    |    |    |    |
|-------------------|----|----|----|----|----|----|----|
| 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PEEK_PTR4 |    |    |    |    |    |    |    |
| R                 |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PEEK_PTR4 |    |    |    |    |    |    |    |
| R                 |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |

**Table 4-1879. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK4 Register Field Descriptions**

| Bit   | Field             | Type | Reset | Description         |
|-------|-------------------|------|-------|---------------------|
| 31:16 | RESERVED          | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_H_PEEK_PTR4 | R    | 0h    | Queue 4 Peek portal |

#### 4.2.2.422 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK5 Register

1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK5 Register (Offset = E14h) [reset = 0h]

QueuePeek5

Return to [Summary Table](#)

**Table 4-1880. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E14h       |

**Figure 4-616. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK5 Name Register**

|                   |    |    |    |    |    |    |    |
|-------------------|----|----|----|----|----|----|----|
| 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PEEK_PTR5 |    |    |    |    |    |    |    |
| R                 |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PEEK_PTR5 |    |    |    |    |    |    |    |
| R                 |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |

**Table 4-1882. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK5 Register Field Descriptions**

| Bit   | Field             | Type | Reset | Description         |
|-------|-------------------|------|-------|---------------------|
| 31:16 | RESERVED          | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_H_PEEK_PTR5 | R    | 0h    | Queue 5 Peek portal |

#### 4.2.2.423 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK6 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK6 Register (Offset = E18h) [reset = 0h]**

QueuePeek6

Return to [Summary Table](#)

**Table 4-1883. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E18h       |

**Figure 4-617. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK6 Name Register**

|                   |    |    |    |    |    |    |    |
|-------------------|----|----|----|----|----|----|----|
| 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PEEK_PTR6 |    |    |    |    |    |    |    |
| R                 |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PEEK_PTR6 |    |    |    |    |    |    |    |
| R                 |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |

**Table 4-1885. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK6 Register Field Descriptions**

| Bit   | Field             | Type | Reset | Description         |
|-------|-------------------|------|-------|---------------------|
| 31:16 | RESERVED          | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_H_PEEK_PTR6 | R    | 0h    | Queue 6 Peek portal |

#### 4.2.2.424 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK7 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK7 Register (Offset = E1Ch) [reset = 0h]**

QueuePeek7

Return to [Summary Table](#)

**Table 4-1886. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E1Ch       |

**Figure 4-618. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK7 Name Register**

|                   |    |    |    |    |    |    |    |
|-------------------|----|----|----|----|----|----|----|
| 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PEEK_PTR7 |    |    |    |    |    |    |    |
| R                 |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PEEK_PTR7 |    |    |    |    |    |    |    |
| R                 |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |

**Table 4-1888. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK7 Register Field Descriptions**

| Bit   | Field             | Type | Reset | Description         |
|-------|-------------------|------|-------|---------------------|
| 31:16 | RESERVED          | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_H_PEEK_PTR7 | R    | 0h    | Queue 7 Peek portal |



#### 4.2.2.425 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK8 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK8 Register (Offset = E20h) [reset = 0h]**

QueuePeek8

Return to [Summary Table](#)

**Table 4-1889. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E20h       |

**Figure 4-619. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK8 Name Register**

|                   |    |    |    |    |    |    |    |
|-------------------|----|----|----|----|----|----|----|
| 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PEEK_PTR8 |    |    |    |    |    |    |    |
| R                 |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PEEK_PTR8 |    |    |    |    |    |    |    |
| R                 |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |

**Table 4-1891. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK8 Register Field Descriptions**

| Bit   | Field             | Type | Reset | Description         |
|-------|-------------------|------|-------|---------------------|
| 31:16 | RESERVED          | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_H_PEEK_PTR8 | R    | 0h    | Queue 8 Peek portal |

#### 4.2.2.426 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK9 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK9 Register (Offset = E24h) [reset = 0h]**

QueuePeek9

Return to [Summary Table](#)

**Table 4-1892. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E24h       |

**Figure 4-620. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK9 Name Register**

|                   |    |    |    |    |    |    |    |
|-------------------|----|----|----|----|----|----|----|
| 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PEEK_PTR9 |    |    |    |    |    |    |    |
| R                 |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PEEK_PTR9 |    |    |    |    |    |    |    |
| R                 |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |

**Table 4-1894. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK9 Register Field Descriptions**

| Bit   | Field             | Type | Reset | Description         |
|-------|-------------------|------|-------|---------------------|
| 31:16 | RESERVED          | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_H_PEEK_PTR9 | R    | 0h    | Queue 9 Peek portal |

#### 4.2.2.427 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK10 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK10 Register (Offset = E28h) [reset = 0h]**

QueuePeek10

Return to [Summary Table](#)

**Table 4-1895. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E28h       |

**Figure 4-621. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK10 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PEEK_PTR10 |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PEEK_PTR10 |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 4-1897. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK10 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description          |
|-------|--------------------|------|-------|----------------------|
| 31:16 | RESERVED           | NONE | 0h    | Reserved             |
| 15:0  | QUEUE_H_PEEK_PTR10 | R    | 0h    | Queue 10 Peek portal |

#### 4.2.2.428 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK11 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK11 Register (Offset = E2Ch) [reset = 0h]**

QueuePeek11

Return to [Summary Table](#)

**Table 4-1898. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E2Ch       |

**Figure 4-622. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK11 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PEEK_PTR11 |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PEEK_PTR11 |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 4-1900. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK11 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description          |
|-------|--------------------|------|-------|----------------------|
| 31:16 | RESERVED           | NONE | 0h    | Reserved             |
| 15:0  | QUEUE_H_PEEK_PTR11 | R    | 0h    | Queue 11 Peek portal |

#### 4.2.2.429 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK12 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK12 Register (Offset = E30h) [reset = 0h]**

QueuePeek12

Return to [Summary Table](#)

**Table 4-1901. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E30h       |

**Figure 4-623. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK12 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PEEK_PTR12 |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PEEK_PTR12 |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 4-1903. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK12 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description          |
|-------|--------------------|------|-------|----------------------|
| 31:16 | RESERVED           | NONE | 0h    | Reserved             |
| 15:0  | QUEUE_H_PEEK_PTR12 | R    | 0h    | Queue 12 Peek portal |

#### 4.2.2.430 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK13 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK13 Register (Offset = E34h) [reset = 0h]**

QueuePeek13

Return to [Summary Table](#)

**Table 4-1904. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E34h       |

**Figure 4-624. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK13 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PEEK_PTR13 |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PEEK_PTR13 |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 4-1906. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK13 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description          |
|-------|--------------------|------|-------|----------------------|
| 31:16 | RESERVED           | NONE | 0h    | Reserved             |
| 15:0  | QUEUE_H_PEEK_PTR13 | R    | 0h    | Queue 13 Peek portal |

#### 4.2.2.431 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK14 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK14 Register (Offset = E38h) [reset = 0h]**

QueuePeek14

Return to [Summary Table](#)

**Table 4-1907. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E38h       |

**Figure 4-625. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK14 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PEEK_PTR14 |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PEEK_PTR14 |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 4-1909. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK14 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description          |
|-------|--------------------|------|-------|----------------------|
| 31:16 | RESERVED           | NONE | 0h    | Reserved             |
| 15:0  | QUEUE_H_PEEK_PTR14 | R    | 0h    | Queue 14 Peek portal |

#### 4.2.2.432 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK15 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK15 Register (Offset = E3Ch) [reset = 0h]**

QueuePeek15

Return to [Summary Table](#)

**Table 4-1910. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E3Ch       |

**Figure 4-626. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK15 Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_H_PEEK_PTR15 |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_H_PEEK_PTR15 |    |    |    |    |    |    |    |
| R                  |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 4-1912. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_PEEK15 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description          |
|-------|--------------------|------|-------|----------------------|
| 31:16 | RESERVED           | NONE | 0h    | Reserved             |
| 15:0  | QUEUE_H_PEEK_PTR15 | R    | 0h    | Queue 15 Peek portal |



#### 4.2.2.433 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT0 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT0 Register (Offset = E40h) [reset = 0h]**

QueueCnt0

Return to [Summary Table](#)

**Table 4-1913. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E40h       |

**Figure 4-627. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT0 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_0 |    |    |    |    |    |    |    |
| R                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_0 |    |    |    |    |    |    |    |
| R                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 4-1915. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT0 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description        |
|-------|---------------------|------|-------|--------------------|
| 31:16 | RESERVED            | NONE | 0h    | Reserved           |
| 15:0  | QUEUE_CNT_ENTRIES_0 | R    | 0h    | Queue Entry Count0 |

#### 4.2.2.434 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT1 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT1 Register (Offset = E44h) [reset = 0h]**

QueueCnt1

Return to [Summary Table](#)

**Table 4-1916. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E44h       |

**Figure 4-628. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT1 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_1 |    |    |    |    |    |    |    |
| R                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_1 |    |    |    |    |    |    |    |
| R                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 4-1918. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT1 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description        |
|-------|---------------------|------|-------|--------------------|
| 31:16 | RESERVED            | NONE | 0h    | Reserved           |
| 15:0  | QUEUE_CNT_ENTRIES_1 | R    | 0h    | Queue Entry Count1 |

#### 4.2.2.435 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT2 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT2 Register (Offset = E48h) [reset = 0h]**

QueueCnt2

Return to [Summary Table](#)

**Table 4-1919. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E48h       |

**Figure 4-629. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT2 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_2 |    |    |    |    |    |    |    |
| R                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_2 |    |    |    |    |    |    |    |
| R                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 4-1921. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT2 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description        |
|-------|---------------------|------|-------|--------------------|
| 31:16 | RESERVED            | NONE | 0h    | Reserved           |
| 15:0  | QUEUE_CNT_ENTRIES_2 | R    | 0h    | Queue Entry Count2 |

#### 4.2.2.436 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT3 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT3 Register (Offset = E4Ch) [reset = 0h]**

QueueCnt3

Return to [Summary Table](#)

**Table 4-1922. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E4Ch       |

**Figure 4-630. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT3 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_3 |    |    |    |    |    |    |    |
| R                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_3 |    |    |    |    |    |    |    |
| R                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 4-1924. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT3 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description        |
|-------|---------------------|------|-------|--------------------|
| 31:16 | RESERVED            | NONE | 0h    | Reserved           |
| 15:0  | QUEUE_CNT_ENTRIES_3 | R    | 0h    | Queue Entry Count3 |

#### 4.2.2.437 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT4 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT4 Register (Offset = E50h) [reset = 0h]**

QueueCnt4

Return to [Summary Table](#)

**Table 4-1925. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E50h       |

**Figure 4-631. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT4 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_4 |    |    |    |    |    |    |    |
| R                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_4 |    |    |    |    |    |    |    |
| R                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 4-1927. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT4 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description        |
|-------|---------------------|------|-------|--------------------|
| 31:16 | RESERVED            | NONE | 0h    | Reserved           |
| 15:0  | QUEUE_CNT_ENTRIES_4 | R    | 0h    | Queue Entry Count4 |

#### 4.2.2.438 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT5 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT5 Register (Offset = E54h) [reset = 0h]**

QueueCnt5

Return to [Summary Table](#)

**Table 4-1928. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E54h       |

**Figure 4-632. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT5 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_5 |    |    |    |    |    |    |    |
| R                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_5 |    |    |    |    |    |    |    |
| R                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 4-1930. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT5 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description        |
|-------|---------------------|------|-------|--------------------|
| 31:16 | RESERVED            | NONE | 0h    | Reserved           |
| 15:0  | QUEUE_CNT_ENTRIES_5 | R    | 0h    | Queue Entry Count5 |

#### 4.2.2.439 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT6 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT6 Register (Offset = E58h) [reset = 0h]**

QueueCnt6

Return to [Summary Table](#)

**Table 4-1931. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E58h       |

**Figure 4-633. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT6 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_6 |    |    |    |    |    |    |    |
| R                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_6 |    |    |    |    |    |    |    |
| R                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 4-1933. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT6 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description        |
|-------|---------------------|------|-------|--------------------|
| 31:16 | RESERVED            | NONE | 0h    | Reserved           |
| 15:0  | QUEUE_CNT_ENTRIES_6 | R    | 0h    | Queue Entry Count6 |

#### 4.2.2.440 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT7 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT7 Register (Offset = E5Ch) [reset = 0h]**

QueueCnt7

Return to [Summary Table](#)

**Table 4-1934. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E5Ch       |

**Figure 4-634. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT7 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_7 |    |    |    |    |    |    |    |
| R                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_7 |    |    |    |    |    |    |    |
| R                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 4-1936. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT7 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description        |
|-------|---------------------|------|-------|--------------------|
| 31:16 | RESERVED            | NONE | 0h    | Reserved           |
| 15:0  | QUEUE_CNT_ENTRIES_7 | R    | 0h    | Queue Entry Count7 |



#### 4.2.2.441 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT8 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT8 Register (Offset = E60h) [reset = 0h]**

QueueCnt8

Return to [Summary Table](#)

**Table 4-1937. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E60h       |

**Figure 4-635. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT8 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_8 |    |    |    |    |    |    |    |
| R                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_8 |    |    |    |    |    |    |    |
| R                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 4-1939. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT8 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description        |
|-------|---------------------|------|-------|--------------------|
| 31:16 | RESERVED            | NONE | 0h    | Reserved           |
| 15:0  | QUEUE_CNT_ENTRIES_8 | R    | 0h    | Queue Entry Count8 |

#### 4.2.2.442 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT9 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT9 Register (Offset = E64h) [reset = 0h]**

QueueCnt9

Return to [Summary Table](#)

**Table 4-1940. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E64h       |

**Figure 4-636. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT9 Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED            |    |    |    |    |    |    |    |
| NONE                |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_9 |    |    |    |    |    |    |    |
| R                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_9 |    |    |    |    |    |    |    |
| R                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 4-1942. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT9 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description        |
|-------|---------------------|------|-------|--------------------|
| 31:16 | RESERVED            | NONE | 0h    | Reserved           |
| 15:0  | QUEUE_CNT_ENTRIES_9 | R    | 0h    | Queue Entry Count9 |

#### 4.2.2.443 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT10 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT10 Register (Offset = E68h) [reset = 0h]**

QueueCnt10

Return to [Summary Table](#)

**Table 4-1943. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E68h       |

**Figure 4-637. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT10 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_10 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_10 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 4-1945. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT10 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description         |
|-------|----------------------|------|-------|---------------------|
| 31:16 | RESERVED             | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_CNT_ENTRIES_10 | R    | 0h    | Queue Entry Count10 |

#### 4.2.2.444 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT11 Register

1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT11 Register (Offset = E6Ch) [reset = 0h]

QueueCnt11

Return to [Summary Table](#)

**Table 4-1946. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E6Ch       |

**Figure 4-638. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT11 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_11 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_11 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 4-1948. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT11 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description         |
|-------|----------------------|------|-------|---------------------|
| 31:16 | RESERVED             | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_CNT_ENTRIES_11 | R    | 0h    | Queue Entry Count11 |

#### 4.2.2.445 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT12 Register

1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT12 Register (Offset = E70h) [reset = 0h]

QueueCnt12

Return to [Summary Table](#)

**Table 4-1949. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E70h       |

**Figure 4-639. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT12 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_12 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_12 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 4-1951. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT12 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description         |
|-------|----------------------|------|-------|---------------------|
| 31:16 | RESERVED             | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_CNT_ENTRIES_12 | R    | 0h    | Queue Entry Count12 |

#### 4.2.2.446 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT13 Register

1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT13 Register (Offset = E74h) [reset = 0h]

QueueCnt13

Return to [Summary Table](#)

**Table 4-1952. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E74h       |

**Figure 4-640. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT13 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_13 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_13 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 4-1954. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT13 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description         |
|-------|----------------------|------|-------|---------------------|
| 31:16 | RESERVED             | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_CNT_ENTRIES_13 | R    | 0h    | Queue Entry Count13 |

#### 4.2.2.447 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT14 Register

1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT14 Register (Offset = E78h) [reset = 0h]

QueueCnt14

Return to [Summary Table](#)

**Table 4-1955. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E78h       |

**Figure 4-641. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT14 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_14 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_14 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 4-1957. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT14 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description         |
|-------|----------------------|------|-------|---------------------|
| 31:16 | RESERVED             | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_CNT_ENTRIES_14 | R    | 0h    | Queue Entry Count14 |

#### 4.2.2.448 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT15 Register

1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT15 Register (Offset = E7Ch) [reset = 0h]

QueueCnt15

Return to [Summary Table](#)

**Table 4-1958. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E7Ch       |

**Figure 4-642. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT15 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_15 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_15 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 4-1960. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT15 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description         |
|-------|----------------------|------|-------|---------------------|
| 31:16 | RESERVED             | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_CNT_ENTRIES_15 | R    | 0h    | Queue Entry Count15 |



#### 4.2.2.449 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT16 Register

1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT16 Register (Offset = E80h) [reset = 0h]

QueueCnt16

Return to [Summary Table](#)

**Table 4-1961. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E80h       |

**Figure 4-643. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT16 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_16 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_16 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 4-1963. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT16 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description         |
|-------|----------------------|------|-------|---------------------|
| 31:16 | RESERVED             | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_CNT_ENTRIES_16 | R    | 0h    | Queue Entry Count16 |

#### 4.2.2.450 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT17 Register

1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT17 Register (Offset = E84h) [reset = 0h]

QueueCnt17

Return to [Summary Table](#)

**Table 4-1964. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E84h       |

**Figure 4-644. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT17 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_17 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_17 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 4-1966. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT17 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description         |
|-------|----------------------|------|-------|---------------------|
| 31:16 | RESERVED             | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_CNT_ENTRIES_17 | R    | 0h    | Queue Entry Count17 |

#### 4.2.2.451 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT18 Register

1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT18 Register (Offset = E88h) [reset = 0h]

QueueCnt18

Return to [Summary Table](#)

**Table 4-1967. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E88h       |

**Figure 4-645. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT18 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_18 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_18 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 4-1969. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT18 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description         |
|-------|----------------------|------|-------|---------------------|
| 31:16 | RESERVED             | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_CNT_ENTRIES_18 | R    | 0h    | Queue Entry Count18 |

#### 4.2.2.452 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT19 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT19 Register (Offset = E8Ch) [reset = 0h]**

QueueCnt19

Return to [Summary Table](#)

**Table 4-1970. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E8Ch       |

**Figure 4-646. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT19 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_19 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_19 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 4-1972. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT19 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description         |
|-------|----------------------|------|-------|---------------------|
| 31:16 | RESERVED             | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_CNT_ENTRIES_19 | R    | 0h    | Queue Entry Count19 |

#### 4.2.2.453 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT20 Register

1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT20 Register (Offset = E90h) [reset = 0h]

QueueCnt20

Return to [Summary Table](#)

**Table 4-1973. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E90h       |

**Figure 4-647. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT20 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_20 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_20 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 4-1975. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT20 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description         |
|-------|----------------------|------|-------|---------------------|
| 31:16 | RESERVED             | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_CNT_ENTRIES_20 | R    | 0h    | Queue Entry Count20 |

#### 4.2.2.454 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT21 Register

1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT21 Register (Offset = E94h) [reset = 0h]

QueueCnt21

Return to [Summary Table](#)

**Table 4-1976. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E94h       |

**Figure 4-648. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT21 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_21 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_21 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 4-1978. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT21 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description         |
|-------|----------------------|------|-------|---------------------|
| 31:16 | RESERVED             | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_CNT_ENTRIES_21 | R    | 0h    | Queue Entry Count21 |

#### 4.2.2.455 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT22 Register

1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT22 Register (Offset = E98h) [reset = 0h]

QueueCnt22

Return to [Summary Table](#)

**Table 4-1979. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E98h       |

**Figure 4-649. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT22 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_22 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_22 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 4-1981. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT22 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description         |
|-------|----------------------|------|-------|---------------------|
| 31:16 | RESERVED             | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_CNT_ENTRIES_22 | R    | 0h    | Queue Entry Count22 |

#### 4.2.2.456 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT23 Register

1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT23 Register (Offset = E9Ch) [reset = 0h]

QueueCnt23

Return to [Summary Table](#)

**Table 4-1982. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3E9Ch       |

**Figure 4-650. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT23 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_23 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_23 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 4-1984. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT23 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description         |
|-------|----------------------|------|-------|---------------------|
| 31:16 | RESERVED             | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_CNT_ENTRIES_23 | R    | 0h    | Queue Entry Count23 |



#### 4.2.2.457 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT24 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT24 Register (Offset = EA0h) [reset = 0h]**

QueueCnt24

Return to [Summary Table](#)

**Table 4-1985. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3EA0h       |

**Figure 4-651. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT24 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_24 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_24 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 4-1987. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT24 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description         |
|-------|----------------------|------|-------|---------------------|
| 31:16 | RESERVED             | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_CNT_ENTRIES_24 | R    | 0h    | Queue Entry Count24 |

#### 4.2.2.458 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT25 Register

1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT25 Register (Offset = EA4h) [reset = 0h]

QueueCnt25

Return to [Summary Table](#)

**Table 4-1988. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3EA4h       |

**Figure 4-652. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT25 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_25 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_25 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 4-1990. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT25 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description         |
|-------|----------------------|------|-------|---------------------|
| 31:16 | RESERVED             | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_CNT_ENTRIES_25 | R    | 0h    | Queue Entry Count25 |

#### 4.2.2.459 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT26 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT26 Register (Offset = EA8h) [reset = 0h]**

QueueCnt26

Return to [Summary Table](#)

**Table 4-1991. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3EA8h       |

**Figure 4-653. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT26 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_26 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_26 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 4-1993. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT26 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description         |
|-------|----------------------|------|-------|---------------------|
| 31:16 | RESERVED             | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_CNT_ENTRIES_26 | R    | 0h    | Queue Entry Count26 |

#### 4.2.2.460 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT27 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT27 Register (Offset = EAC<sub>h</sub>) [reset = 0<sub>h</sub>]**

QueueCnt27

Return to [Summary Table](#)

**Table 4-1994. Instance Table**

| Instance Name | Physical Address       |
|---------------|------------------------|
| ICSSM0        | 4803 3EAC <sub>h</sub> |

**Figure 4-654. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT27 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0 <sub>h</sub>       |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0 <sub>h</sub>       |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_27 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0 <sub>h</sub>       |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_27 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0 <sub>h</sub>       |    |    |    |    |    |    |    |

**Table 4-1996. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT27 Register Field Descriptions**

| Bit   | Field                | Type | Reset          | Description         |
|-------|----------------------|------|----------------|---------------------|
| 31:16 | RESERVED             | NONE | 0 <sub>h</sub> | Reserved            |
| 15:0  | QUEUE_CNT_ENTRIES_27 | R    | 0 <sub>h</sub> | Queue Entry Count27 |

#### 4.2.2.461 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT28 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT28 Register (Offset = EB0h) [reset = 0h]**

QueueCnt28

Return to [Summary Table](#)

**Table 4-1997. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3EB0h       |

**Figure 4-655. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT28 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_28 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_28 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 4-1999. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT28 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description         |
|-------|----------------------|------|-------|---------------------|
| 31:16 | RESERVED             | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_CNT_ENTRIES_28 | R    | 0h    | Queue Entry Count28 |

#### 4.2.2.462 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT29 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT29 Register (Offset = EB4h) [reset = 0h]**

QueueCnt29

Return to [Summary Table](#)

**Table 4-2000. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3EB4h       |

**Figure 4-656. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT29 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_29 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_29 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 4-2002. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT29 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description         |
|-------|----------------------|------|-------|---------------------|
| 31:16 | RESERVED             | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_CNT_ENTRIES_29 | R    | 0h    | Queue Entry Count29 |

#### 4.2.2.463 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT30 Register

1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT30 Register (Offset = EB8h) [reset = 0h]

QueueCnt30

Return to [Summary Table](#)

**Table 4-2003. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3EB8h       |

**Figure 4-657. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT30 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_30 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_30 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 4-2005. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT30 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description         |
|-------|----------------------|------|-------|---------------------|
| 31:16 | RESERVED             | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_CNT_ENTRIES_30 | R    | 0h    | Queue Entry Count30 |

#### 4.2.2.464 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT31 Register

**1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT31 Register (Offset = EBCh) [reset = 0h]**

QueueCnt31

Return to [Summary Table](#)

**Table 4-2006. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3EBCh       |

**Figure 4-658. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT31 Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED             |    |    |    |    |    |    |    |
| NONE                 |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| QUEUE_CNT_ENTRIES_31 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| QUEUE_CNT_ENTRIES_31 |    |    |    |    |    |    |    |
| R                    |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 4-2008. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_CNT31 Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description         |
|-------|----------------------|------|-------|---------------------|
| 31:16 | RESERVED             | NONE | 0h    | Reserved            |
| 15:0  | QUEUE_CNT_ENTRIES_31 | R    | 0h    | Queue Entry Count31 |



#### 4.2.2.465 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_RESET Register

1 ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_RESET Register (Offset = F40h) [reset = 0h]

QueueReset32

Return to [Summary Table](#)

**Table 4-2009. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4803 3F40h       |

**Figure 4-659. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_RESET Name Register**

|          |    |                |    |    |    |    |    |
|----------|----|----------------|----|----|----|----|----|
| 31       | 30 | 29             | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |                |    |    |    |    |    |
| NONE     |    |                |    |    |    |    |    |
| 0h       |    |                |    |    |    |    |    |
| 23       | 22 | 21             | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |                |    |    |    |    |    |
| NONE     |    |                |    |    |    |    |    |
| 0h       |    |                |    |    |    |    |    |
| 15       | 14 | 13             | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |                |    |    |    |    |    |
| NONE     |    |                |    |    |    |    |    |
| 0h       |    |                |    |    |    |    |    |
| 7        | 6  | 5              | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    | RESET_QUEUE_ID |    |    |    |    |    |
| NONE     |    | R/W            |    |    |    |    |    |
| 0h       |    | 0h             |    |    |    |    |    |

**Table 4-2011. ICSSM\_PR1\_MII\_RT\_PR1\_MII\_RT\_G\_CFG\_REGS\_G\_QUEUE\_RESET Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description    |
|------|----------------|------|-------|----------------|
| 31:6 | RESERVED       | NONE | 0h    | Reserved       |
| 5:0  | RESET_QUEUE_ID | R/W  | 0h    | Reset Queue ID |

#### 4.2.2.466 ECC\_AGGR\_REV Register

##### 1 ECC\_AGGR\_REV Register (Offset = 0h) [reset = 66A0EA00h]

Revision parameters.

Return to [Summary Table](#)

**Table 4-2012. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4810 0000h       |

**Figure 4-660. ECC\_AGGR\_REV Name Register**

|           |    |        |    |           |        |    |    |
|-----------|----|--------|----|-----------|--------|----|----|
| 31        | 30 | 29     | 28 | 27        | 26     | 25 | 24 |
| SCHEME    |    | BU     |    | MODULE_ID |        |    |    |
| R         |    | R      |    | R         |        |    |    |
| 1h        |    | 2h     |    | 6A0h      |        |    |    |
| 23        | 22 | 21     | 20 | 19        | 18     | 17 | 16 |
| MODULE_ID |    |        |    |           |        |    |    |
| R         |    |        |    |           |        |    |    |
| 6A0h      |    |        |    |           |        |    |    |
| 15        | 14 | 13     | 12 | 11        | 10     | 9  | 8  |
| REVRTL    |    |        |    |           | REVMAJ |    |    |
| R         |    |        |    |           | R      |    |    |
| 1Dh       |    |        |    |           | 2h     |    |    |
| 7         | 6  | 5      | 4  | 3         | 2      | 1  | 0  |
| CUSTOM    |    | REVMIN |    |           |        |    |    |
| R         |    | R      |    |           |        |    |    |
| 0h        |    | 0h     |    |           |        |    |    |

**Table 4-2014. ECC\_AGGR\_REV Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description    |
|-------|-----------|------|-------|----------------|
| 31:30 | SCHEME    | R    | 1h    | Scheme         |
| 29:28 | BU        | R    | 2h    | bu             |
| 27:16 | MODULE_ID | R    | 6A0h  | Module ID      |
| 15:11 | REVRTL    | R    | 1Dh   | RTL version    |
| 10:8  | REVMAJ    | R    | 2h    | Major version  |
| 7:6   | CUSTOM    | R    | 0h    | Custom version |
| 5:0   | REVMIN    | R    | 0h    | Minor version  |

#### 4.2.2.467 ECC\_AGGR\_VECTOR Register

##### 1 ECC\_AGGR\_VECTOR Register (Offset = 8h) [reset = 0h]

ECC Vector Register.

Return to [Summary Table](#)

**Table 4-2015. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4810 0008h       |

**Figure 4-661. ECC\_AGGR\_VECTOR Name Register**

|                  |          |    |    |    |            |    |                   |
|------------------|----------|----|----|----|------------|----|-------------------|
| 31               | 30       | 29 | 28 | 27 | 26         | 25 | 24                |
| RESERVED         |          |    |    |    |            |    | RD_SVBUS_D<br>ONE |
| NONE             |          |    |    |    |            |    | R/W1TC            |
| 0h               |          |    |    |    |            |    | 0h                |
| 23               | 22       | 21 | 20 | 19 | 18         | 17 | 16                |
| RD_SVBUS_ADDRESS |          |    |    |    |            |    |                   |
| R/W              |          |    |    |    |            |    |                   |
| 0h               |          |    |    |    |            |    |                   |
| 15               | 14       | 13 | 12 | 11 | 10         | 9  | 8                 |
| RD_SVBUS         | RESERVED |    |    |    | ECC_VECTOR |    |                   |
| R/W1TS           | NONE     |    |    |    | R/W        |    |                   |
| 0h               | 0h       |    |    |    | 0h         |    |                   |
| 7                | 6        | 5  | 4  | 3  | 2          | 1  | 0                 |
| ECC_VECTOR       |          |    |    |    |            |    |                   |
| R/W              |          |    |    |    |            |    |                   |
| 0h               |          |    |    |    |            |    |                   |

**Table 4-2017. ECC\_AGGR\_VECTOR Register Field Descriptions**

| Bit   | Field            | Type   | Reset | Description                                                                                    |
|-------|------------------|--------|-------|------------------------------------------------------------------------------------------------|
| 31:25 | RESERVED         | NONE   | 0h    | Reserved                                                                                       |
| 24    | RD_SVBUS_DONE    | R/W1TC | 0h    | Status to indicate if read on serial VBUS is complete, write of any value will clear this bit. |
| 23:16 | RD_SVBUS_ADDRESS | R/W    | 0h    | Read address                                                                                   |
| 15    | RD_SVBUS         | R/W1TS | 0h    | Write 1 to trigger a read on the serial VBUS                                                   |
| 14:11 | RESERVED         | NONE   | 0h    | Reserved                                                                                       |
| 10:0  | ECC_VECTOR       | R/W    | 0h    | Value written to select the corresponding ECC RAM for control or status                        |

#### 4.2.2.468 ECC\_AGGR\_STAT Register

##### 1 ECC\_AGGR\_STAT Register (Offset = Ch) [reset = 5h]

Misc Status.

Return to [Summary Table](#)

**Table 4-2018. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4810 000Ch       |

**Figure 4-662. ECC\_AGGR\_STAT Name Register**

|          |    |    |    |    |          |    |    |
|----------|----|----|----|----|----------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26       | 25 | 24 |
| RESERVED |    |    |    |    |          |    |    |
| NONE     |    |    |    |    |          |    |    |
| 0h       |    |    |    |    |          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18       | 17 | 16 |
| RESERVED |    |    |    |    |          |    |    |
| NONE     |    |    |    |    |          |    |    |
| 0h       |    |    |    |    |          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10       | 9  | 8  |
| RESERVED |    |    |    |    | NUM_RAMs |    |    |
| NONE     |    |    |    |    | R        |    |    |
| 0h       |    |    |    |    | 5h       |    |    |
| 7        | 6  | 5  | 4  | 3  | 2        | 1  | 0  |
| NUM_RAMs |    |    |    |    |          |    |    |
| R        |    |    |    |    |          |    |    |
| 5h       |    |    |    |    |          |    |    |

**Table 4-2020. ECC\_AGGR\_STAT Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                 |
|-------|----------|------|-------|-------------------------------------------------------------|
| 31:11 | RESERVED | NONE | 0h    | Reserved                                                    |
| 10:0  | NUM_RAMs | R    | 5h    | Indicates the number of RAMs serviced by the ECC aggregator |

#### 4.2.2.469 ECC\_AGGR\_RESERVED\_SVBUS\_J Register

##### 1 ECC\_AGGR\_RESERVED\_SVBUS\_J Register (Offset = 10h) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Return to [Summary Table](#)

Offset = Base + (j \* 4h); where j = 0 to 7d

**Table 4-2021. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ICSSM0        | 4810 0010h + formula |

**Figure 4-663. ECC\_AGGR\_RESERVED\_SVBUS\_J Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 4-2023. ECC\_AGGR\_RESERVED\_SVBUS\_J Register Field Descriptions**

| Bit  | Field | Type | Reset | Description               |
|------|-------|------|-------|---------------------------|
| 31:0 | DATA  | R/W  | 0h    | Serial VBUS register data |

#### 4.2.2.470 ECC\_AGGR\_SEC\_EOI\_REG Register

##### 1 ECC\_AGGR\_SEC\_EOI\_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register.

Return to [Summary Table](#)

**Table 4-2024. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4810 003Ch       |

**Figure 4-664. ECC\_AGGR\_SEC\_EOI\_REG Name Register**

|          |    |    |    |    |    |    |        |
|----------|----|----|----|----|----|----|--------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24     |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16     |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8      |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0      |
| RESERVED |    |    |    |    |    |    | EOI_WR |
| NONE     |    |    |    |    |    |    | R/W1TS |
| 0h       |    |    |    |    |    |    | 0h     |

**Table 4-2026. ECC\_AGGR\_SEC\_EOI\_REG Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description  |
|------|----------|--------|-------|--------------|
| 31:1 | RESERVED | NONE   | 0h    | Reserved     |
| 0    | EOI_WR   | R/W1TS | 0h    | EOI Register |

#### 4.2.2.471 ECC\_AGGR\_SEC\_STATUS\_REG0 Register

##### 1 ECC\_AGGR\_SEC\_STATUS\_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

Return to [Summary Table](#)

**Table 4-2027. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4810 0040h       |

**Figure 4-665. ECC\_AGGR\_SEC\_STATUS\_REG0 Name Register**

|          |    |    |              |                     |                     |                |                |
|----------|----|----|--------------|---------------------|---------------------|----------------|----------------|
| 31       | 30 | 29 | 28           | 27                  | 26                  | 25             | 24             |
| RESERVED |    |    |              |                     |                     |                |                |
| NONE     |    |    |              |                     |                     |                |                |
| 0h       |    |    |              |                     |                     |                |                |
| 23       | 22 | 21 | 20           | 19                  | 18                  | 17             | 16             |
| RESERVED |    |    |              |                     |                     |                |                |
| NONE     |    |    |              |                     |                     |                |                |
| 0h       |    |    |              |                     |                     |                |                |
| 15       | 14 | 13 | 12           | 11                  | 10                  | 9              | 8              |
| RESERVED |    |    |              |                     |                     |                |                |
| NONE     |    |    |              |                     |                     |                |                |
| 0h       |    |    |              |                     |                     |                |                |
| 7        | 6  | 5  | 4            | 3                   | 2                   | 1              | 0              |
| RESERVED |    |    | PR1_RAM_PEND | PR1_PDSP1_IRAM_PEND | PR1_PDSP0_IRAM_PEND | PR1_DRAM1_PEND | PR1_DRAM0_PEND |
| NONE     |    |    | R/W1TS       | R/W1TS              | R/W1TS              | R/W1TS         | R/W1TS         |
| 0h       |    |    | 0h           | 0h                  | 0h                  | 0h             | 0h             |

**Table 4-2029. ECC\_AGGR\_SEC\_STATUS\_REG0 Register Field Descriptions**

| Bit  | Field               | Type   | Reset | Description                                         |
|------|---------------------|--------|-------|-----------------------------------------------------|
| 31:5 | RESERVED            | NONE   | 0h    | Reserved                                            |
| 4    | PR1_RAM_PEND        | R/W1TS | 0h    | Interrupt Pending Status for pr1_ram_pending        |
| 3    | PR1_PDSP1_IRAM_PEND | R/W1TS | 0h    | Interrupt Pending Status for pr1_pdsp1_iram_pending |
| 2    | PR1_PDSP0_IRAM_PEND | R/W1TS | 0h    | Interrupt Pending Status for pr1_pdsp0_iram_pending |
| 1    | PR1_DRAM1_PEND      | R/W1TS | 0h    | Interrupt Pending Status for pr1_dram1_pending      |
| 0    | PR1_DRAM0_PEND      | R/W1TS | 0h    | Interrupt Pending Status for pr1_dram0_pending      |

#### 4.2.2.472 ECC\_AGGR\_SEC\_ENABLE\_SET\_REG0 Register

##### 1 ECC\_AGGR\_SEC\_ENABLE\_SET\_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

Return to [Summary Table](#)

**Table 4-2030. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4810 0080h       |

**Figure 4-666. ECC\_AGGR\_SEC\_ENABLE\_SET\_REG0 Name Register**

|          |    |    |                        |                                   |                                   |                          |                          |
|----------|----|----|------------------------|-----------------------------------|-----------------------------------|--------------------------|--------------------------|
| 31       | 30 | 29 | 28                     | 27                                | 26                                | 25                       | 24                       |
| RESERVED |    |    |                        |                                   |                                   |                          |                          |
| NONE     |    |    |                        |                                   |                                   |                          |                          |
| 0h       |    |    |                        |                                   |                                   |                          |                          |
| 23       | 22 | 21 | 20                     | 19                                | 18                                | 17                       | 16                       |
| RESERVED |    |    |                        |                                   |                                   |                          |                          |
| NONE     |    |    |                        |                                   |                                   |                          |                          |
| 0h       |    |    |                        |                                   |                                   |                          |                          |
| 15       | 14 | 13 | 12                     | 11                                | 10                                | 9                        | 8                        |
| RESERVED |    |    |                        |                                   |                                   |                          |                          |
| NONE     |    |    |                        |                                   |                                   |                          |                          |
| 0h       |    |    |                        |                                   |                                   |                          |                          |
| 7        | 6  | 5  | 4                      | 3                                 | 2                                 | 1                        | 0                        |
| RESERVED |    |    | PR1_RAM_EN<br>ABLE_SET | PR1_PDSP1_I<br>RAM_ENABLE<br>_SET | PR1_PDSP0_I<br>RAM_ENABLE<br>_SET | PR1_DRAM1_E<br>NABLE_SET | PR1_DRAM0_E<br>NABLE_SET |
| NONE     |    |    | R/W1TS                 | R/W1TS                            | R/W1TS                            | R/W1TS                   | R/W1TS                   |
| 0h       |    |    | 0h                     | 0h                                | 0h                                | 0h                       | 0h                       |

**Table 4-2032. ECC\_AGGR\_SEC\_ENABLE\_SET\_REG0 Register Field Descriptions**

| Bit  | Field                         | Type   | Reset | Description                                           |
|------|-------------------------------|--------|-------|-------------------------------------------------------|
| 31:5 | RESERVED                      | NONE   | 0h    | Reserved                                              |
| 4    | PR1_RAM_ENABLE_SET            | R/W1TS | 0h    | Interrupt Enable Set Register for pr1_ram_pend        |
| 3    | PR1_PDSP1_IRAM_ENA<br>BLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for pr1_pdsp1_iram_pend |
| 2    | PR1_PDSP0_IRAM_ENA<br>BLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for pr1_pdsp0_iram_pend |
| 1    | PR1_DRAM1_ENABLE_S<br>ET      | R/W1TS | 0h    | Interrupt Enable Set Register for pr1_dram1_pend      |
| 0    | PR1_DRAM0_ENABLE_S<br>ET      | R/W1TS | 0h    | Interrupt Enable Set Register for pr1_dram0_pend      |



#### 4.2.2.473 ECC\_AGGR\_SEC\_ENABLE\_CLR\_REG0 Register

##### 1 ECC\_AGGR\_SEC\_ENABLE\_CLR\_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to [Summary Table](#)

**Table 4-2033. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4810 00C0h       |

**Figure 4-667. ECC\_AGGR\_SEC\_ENABLE\_CLR\_REG0 Name Register**

|          |    |    |                        |                                   |                                   |                          |                          |
|----------|----|----|------------------------|-----------------------------------|-----------------------------------|--------------------------|--------------------------|
| 31       | 30 | 29 | 28                     | 27                                | 26                                | 25                       | 24                       |
| RESERVED |    |    |                        |                                   |                                   |                          |                          |
| NONE     |    |    |                        |                                   |                                   |                          |                          |
| 0h       |    |    |                        |                                   |                                   |                          |                          |
| 23       | 22 | 21 | 20                     | 19                                | 18                                | 17                       | 16                       |
| RESERVED |    |    |                        |                                   |                                   |                          |                          |
| NONE     |    |    |                        |                                   |                                   |                          |                          |
| 0h       |    |    |                        |                                   |                                   |                          |                          |
| 15       | 14 | 13 | 12                     | 11                                | 10                                | 9                        | 8                        |
| RESERVED |    |    |                        |                                   |                                   |                          |                          |
| NONE     |    |    |                        |                                   |                                   |                          |                          |
| 0h       |    |    |                        |                                   |                                   |                          |                          |
| 7        | 6  | 5  | 4                      | 3                                 | 2                                 | 1                        | 0                        |
| RESERVED |    |    | PR1_RAM_EN<br>ABLE_CLR | PR1_PDSP1_I<br>RAM_ENABLE<br>_CLR | PR1_PDSP0_I<br>RAM_ENABLE<br>_CLR | PR1_DRAM1_E<br>NABLE_CLR | PR1_DRAM0_E<br>NABLE_CLR |
| NONE     |    |    | R/W1TC                 | R/W1TC                            | R/W1TC                            | R/W1TC                   | R/W1TC                   |
| 0h       |    |    | 0h                     | 0h                                | 0h                                | 0h                       | 0h                       |

**Table 4-2035. ECC\_AGGR\_SEC\_ENABLE\_CLR\_REG0 Register Field Descriptions**

| Bit  | Field                         | Type   | Reset | Description                                             |
|------|-------------------------------|--------|-------|---------------------------------------------------------|
| 31:5 | RESERVED                      | NONE   | 0h    | Reserved                                                |
| 4    | PR1_RAM_ENABLE_CLR            | R/W1TC | 0h    | Interrupt Enable Clear Register for pr1_ram_pend        |
| 3    | PR1_PDSP1_IRAM_ENA<br>BLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for pr1_pdsp1_iram_pend |
| 2    | PR1_PDSP0_IRAM_ENA<br>BLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for pr1_pdsp0_iram_pend |
| 1    | PR1_DRAM1_ENABLE_C<br>LR      | R/W1TC | 0h    | Interrupt Enable Clear Register for pr1_dram1_pend      |
| 0    | PR1_DRAM0_ENABLE_C<br>LR      | R/W1TC | 0h    | Interrupt Enable Clear Register for pr1_dram0_pend      |

#### 4.2.2.474 ECC\_AGGR\_DED\_EOI\_REG Register

##### 1 ECC\_AGGR\_DED\_EOI\_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register.

Return to [Summary Table](#)

**Table 4-2036. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4810 013Ch       |

**Figure 4-668. ECC\_AGGR\_DED\_EOI\_REG Name Register**

|          |    |    |    |    |    |    |        |
|----------|----|----|----|----|----|----|--------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24     |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16     |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8      |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0      |
| RESERVED |    |    |    |    |    |    | EOI_WR |
| NONE     |    |    |    |    |    |    | R/W1TS |
| 0h       |    |    |    |    |    |    | 0h     |

**Table 4-2038. ECC\_AGGR\_DED\_EOI\_REG Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description  |
|------|----------|--------|-------|--------------|
| 31:1 | RESERVED | NONE   | 0h    | Reserved     |
| 0    | EOI_WR   | R/W1TS | 0h    | EOI Register |

#### 4.2.2.475 ECC\_AGGR\_DED\_STATUS\_REG0 Register

##### 1 ECC\_AGGR\_DED\_STATUS\_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

Return to [Summary Table](#)

**Table 4-2039. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4810 0140h       |

**Figure 4-669. ECC\_AGGR\_DED\_STATUS\_REG0 Name Register**

|          |    |    |              |                     |                     |                |                |
|----------|----|----|--------------|---------------------|---------------------|----------------|----------------|
| 31       | 30 | 29 | 28           | 27                  | 26                  | 25             | 24             |
| RESERVED |    |    |              |                     |                     |                |                |
| NONE     |    |    |              |                     |                     |                |                |
| 0h       |    |    |              |                     |                     |                |                |
| 23       | 22 | 21 | 20           | 19                  | 18                  | 17             | 16             |
| RESERVED |    |    |              |                     |                     |                |                |
| NONE     |    |    |              |                     |                     |                |                |
| 0h       |    |    |              |                     |                     |                |                |
| 15       | 14 | 13 | 12           | 11                  | 10                  | 9              | 8              |
| RESERVED |    |    |              |                     |                     |                |                |
| NONE     |    |    |              |                     |                     |                |                |
| 0h       |    |    |              |                     |                     |                |                |
| 7        | 6  | 5  | 4            | 3                   | 2                   | 1              | 0              |
| RESERVED |    |    | PR1_RAM_PEND | PR1_PDSP1_IRAM_PEND | PR1_PDSP0_IRAM_PEND | PR1_DRAM1_PEND | PR1_DRAM0_PEND |
| NONE     |    |    | R/W1TS       | R/W1TS              | R/W1TS              | R/W1TS         | R/W1TS         |
| 0h       |    |    | 0h           | 0h                  | 0h                  | 0h             | 0h             |

**Table 4-2041. ECC\_AGGR\_DED\_STATUS\_REG0 Register Field Descriptions**

| Bit  | Field               | Type   | Reset | Description                                         |
|------|---------------------|--------|-------|-----------------------------------------------------|
| 31:5 | RESERVED            | NONE   | 0h    | Reserved                                            |
| 4    | PR1_RAM_PEND        | R/W1TS | 0h    | Interrupt Pending Status for pr1_ram_pending        |
| 3    | PR1_PDSP1_IRAM_PEND | R/W1TS | 0h    | Interrupt Pending Status for pr1_pdsp1_iram_pending |
| 2    | PR1_PDSP0_IRAM_PEND | R/W1TS | 0h    | Interrupt Pending Status for pr1_pdsp0_iram_pending |
| 1    | PR1_DRAM1_PEND      | R/W1TS | 0h    | Interrupt Pending Status for pr1_dram1_pending      |
| 0    | PR1_DRAM0_PEND      | R/W1TS | 0h    | Interrupt Pending Status for pr1_dram0_pending      |

#### 4.2.2.476 ECC\_AGGR\_DED\_ENABLE\_SET\_REG0 Register

##### 1 ECC\_AGGR\_DED\_ENABLE\_SET\_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

Return to [Summary Table](#)

**Table 4-2042. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4810 0180h       |

**Figure 4-670. ECC\_AGGR\_DED\_ENABLE\_SET\_REG0 Name Register**

|          |    |    |                        |                                   |                                   |                          |                          |
|----------|----|----|------------------------|-----------------------------------|-----------------------------------|--------------------------|--------------------------|
| 31       | 30 | 29 | 28                     | 27                                | 26                                | 25                       | 24                       |
| RESERVED |    |    |                        |                                   |                                   |                          |                          |
| NONE     |    |    |                        |                                   |                                   |                          |                          |
| 0h       |    |    |                        |                                   |                                   |                          |                          |
| 23       | 22 | 21 | 20                     | 19                                | 18                                | 17                       | 16                       |
| RESERVED |    |    |                        |                                   |                                   |                          |                          |
| NONE     |    |    |                        |                                   |                                   |                          |                          |
| 0h       |    |    |                        |                                   |                                   |                          |                          |
| 15       | 14 | 13 | 12                     | 11                                | 10                                | 9                        | 8                        |
| RESERVED |    |    |                        |                                   |                                   |                          |                          |
| NONE     |    |    |                        |                                   |                                   |                          |                          |
| 0h       |    |    |                        |                                   |                                   |                          |                          |
| 7        | 6  | 5  | 4                      | 3                                 | 2                                 | 1                        | 0                        |
| RESERVED |    |    | PR1_RAM_EN<br>ABLE_SET | PR1_PDSP1_I<br>RAM_ENABLE<br>_SET | PR1_PDSP0_I<br>RAM_ENABLE<br>_SET | PR1_DRAM1_E<br>NABLE_SET | PR1_DRAM0_E<br>NABLE_SET |
| NONE     |    |    | R/W1TS                 | R/W1TS                            | R/W1TS                            | R/W1TS                   | R/W1TS                   |
| 0h       |    |    | 0h                     | 0h                                | 0h                                | 0h                       | 0h                       |

**Table 4-2044. ECC\_AGGR\_DED\_ENABLE\_SET\_REG0 Register Field Descriptions**

| Bit  | Field                         | Type   | Reset | Description                                           |
|------|-------------------------------|--------|-------|-------------------------------------------------------|
| 31:5 | RESERVED                      | NONE   | 0h    | Reserved                                              |
| 4    | PR1_RAM_ENABLE_SET            | R/W1TS | 0h    | Interrupt Enable Set Register for pr1_ram_pend        |
| 3    | PR1_PDSP1_IRAM_ENA<br>BLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for pr1_pdsp1_iram_pend |
| 2    | PR1_PDSP0_IRAM_ENA<br>BLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for pr1_pdsp0_iram_pend |
| 1    | PR1_DRAM1_ENABLE_S<br>ET      | R/W1TS | 0h    | Interrupt Enable Set Register for pr1_dram1_pend      |
| 0    | PR1_DRAM0_ENABLE_S<br>ET      | R/W1TS | 0h    | Interrupt Enable Set Register for pr1_dram0_pend      |

#### 4.2.2.477 ECC\_AGGR\_DED\_ENABLE\_CLR\_REG0 Register

##### 1 ECC\_AGGR\_DED\_ENABLE\_CLR\_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to [Summary Table](#)

**Table 4-2045. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4810 01C0h       |

**Figure 4-671. ECC\_AGGR\_DED\_ENABLE\_CLR\_REG0 Name Register**

|          |    |    |                        |                                   |                                   |                          |                          |
|----------|----|----|------------------------|-----------------------------------|-----------------------------------|--------------------------|--------------------------|
| 31       | 30 | 29 | 28                     | 27                                | 26                                | 25                       | 24                       |
| RESERVED |    |    |                        |                                   |                                   |                          |                          |
| NONE     |    |    |                        |                                   |                                   |                          |                          |
| 0h       |    |    |                        |                                   |                                   |                          |                          |
| 23       | 22 | 21 | 20                     | 19                                | 18                                | 17                       | 16                       |
| RESERVED |    |    |                        |                                   |                                   |                          |                          |
| NONE     |    |    |                        |                                   |                                   |                          |                          |
| 0h       |    |    |                        |                                   |                                   |                          |                          |
| 15       | 14 | 13 | 12                     | 11                                | 10                                | 9                        | 8                        |
| RESERVED |    |    |                        |                                   |                                   |                          |                          |
| NONE     |    |    |                        |                                   |                                   |                          |                          |
| 0h       |    |    |                        |                                   |                                   |                          |                          |
| 7        | 6  | 5  | 4                      | 3                                 | 2                                 | 1                        | 0                        |
| RESERVED |    |    | PR1_RAM_EN<br>ABLE_CLR | PR1_PDSP1_I<br>RAM_ENABLE<br>_CLR | PR1_PDSP0_I<br>RAM_ENABLE<br>_CLR | PR1_DRAM1_E<br>NABLE_CLR | PR1_DRAM0_E<br>NABLE_CLR |
| NONE     |    |    | R/W1TC                 | R/W1TC                            | R/W1TC                            | R/W1TC                   | R/W1TC                   |
| 0h       |    |    | 0h                     | 0h                                | 0h                                | 0h                       | 0h                       |

**Table 4-2047. ECC\_AGGR\_DED\_ENABLE\_CLR\_REG0 Register Field Descriptions**

| Bit  | Field                         | Type   | Reset | Description                                             |
|------|-------------------------------|--------|-------|---------------------------------------------------------|
| 31:5 | RESERVED                      | NONE   | 0h    | Reserved                                                |
| 4    | PR1_RAM_ENABLE_CLR            | R/W1TC | 0h    | Interrupt Enable Clear Register for pr1_ram_pend        |
| 3    | PR1_PDSP1_IRAM_ENA<br>BLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for pr1_pdsp1_iram_pend |
| 2    | PR1_PDSP0_IRAM_ENA<br>BLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for pr1_pdsp0_iram_pend |
| 1    | PR1_DRAM1_ENABLE_C<br>LR      | R/W1TC | 0h    | Interrupt Enable Clear Register for pr1_dram1_pend      |
| 0    | PR1_DRAM0_ENABLE_C<br>LR      | R/W1TC | 0h    | Interrupt Enable Clear Register for pr1_dram0_pend      |

#### 4.2.2.478 ECC\_AGGR\_AGGR\_ENABLE\_SET Register

##### 1 ECC\_AGGR\_AGGR\_ENABLE\_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register.

Return to [Summary Table](#)

**Table 4-2048. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4810 0200h       |

**Figure 4-672. ECC\_AGGR\_AGGR\_ENABLE\_SET Name Register**

|          |    |    |    |    |    |         |        |
|----------|----|----|----|----|----|---------|--------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25      | 24     |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 23       | 22 | 21 | 20 | 19 | 18 | 17      | 16     |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 15       | 14 | 13 | 12 | 11 | 10 | 9       | 8      |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 7        | 6  | 5  | 4  | 3  | 2  | 1       | 0      |
| RESERVED |    |    |    |    |    | TIMEOUT | PARITY |
| NONE     |    |    |    |    |    | R/W1TS  | R/W1TS |
| 0h       |    |    |    |    |    | 0h      | 0h     |

**Table 4-2050. ECC\_AGGR\_AGGR\_ENABLE\_SET Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description                                   |
|------|----------|--------|-------|-----------------------------------------------|
| 31:2 | RESERVED | NONE   | 0h    | Reserved                                      |
| 1    | TIMEOUT  | R/W1TS | 0h    | Interrupt enable set for svbus timeout errors |
| 0    | PARITY   | R/W1TS | 0h    | Interrupt enable set for parity errors        |

#### 4.2.2.479 ECC\_AGGR\_AGGR\_ENABLE\_CLR Register

##### 1 ECC\_AGGR\_AGGR\_ENABLE\_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register.

Return to [Summary Table](#)

**Table 4-2051. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4810 0204h       |

**Figure 4-673. ECC\_AGGR\_AGGR\_ENABLE\_CLR Name Register**

|          |    |    |    |    |    |         |        |
|----------|----|----|----|----|----|---------|--------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25      | 24     |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 23       | 22 | 21 | 20 | 19 | 18 | 17      | 16     |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 15       | 14 | 13 | 12 | 11 | 10 | 9       | 8      |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 7        | 6  | 5  | 4  | 3  | 2  | 1       | 0      |
| RESERVED |    |    |    |    |    | TIMEOUT | PARITY |
| NONE     |    |    |    |    |    | R/W1TC  | R/W1TC |
| 0h       |    |    |    |    |    | 0h      | 0h     |

**Table 4-2053. ECC\_AGGR\_AGGR\_ENABLE\_CLR Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description                                     |
|------|----------|--------|-------|-------------------------------------------------|
| 31:2 | RESERVED | NONE   | 0h    | Reserved                                        |
| 1    | TIMEOUT  | R/W1TC | 0h    | Interrupt enable clear for svbus timeout errors |
| 0    | PARITY   | R/W1TC | 0h    | Interrupt enable clear for parity errors        |

#### 4.2.2.480 ECC\_AGGR\_AGGR\_STATUS\_SET Register

##### 1 ECC\_AGGR\_AGGR\_STATUS\_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register.

Return to [Summary Table](#)

**Table 4-2054. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4810 0208h       |

**Figure 4-674. ECC\_AGGR\_AGGR\_STATUS\_SET Name Register**

|          |    |    |    |         |    |        |    |
|----------|----|----|----|---------|----|--------|----|
| 31       | 30 | 29 | 28 | 27      | 26 | 25     | 24 |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 23       | 22 | 21 | 20 | 19      | 18 | 17     | 16 |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 15       | 14 | 13 | 12 | 11      | 10 | 9      | 8  |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 7        | 6  | 5  | 4  | 3       | 2  | 1      | 0  |
| RESERVED |    |    |    | TIMEOUT |    | PARITY |    |
| NONE     |    |    |    | R/WI    |    | R/WI   |    |
| 0h       |    |    |    | 0h      |    | 0h     |    |

**Table 4-2056. ECC\_AGGR\_AGGR\_STATUS\_SET Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                   |
|------|----------|------|-------|-----------------------------------------------|
| 31:4 | RESERVED | NONE | 0h    | Reserved                                      |
| 3:2  | TIMEOUT  | R/WI | 0h    | Interrupt status set for svbus timeout errors |
| 1:0  | PARITY   | R/WI | 0h    | Interrupt status set for parity errors        |



#### 4.2.2.481 ECC\_AGGR\_AGGR\_STATUS\_CLR Register

##### 1 ECC\_AGGR\_AGGR\_STATUS\_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register.

Return to [Summary Table](#)

**Table 4-2057. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ICSSM0        | 4810 020Ch       |

**Figure 4-675. ECC\_AGGR\_AGGR\_STATUS\_CLR Name Register**

|          |    |    |    |         |    |        |    |
|----------|----|----|----|---------|----|--------|----|
| 31       | 30 | 29 | 28 | 27      | 26 | 25     | 24 |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 23       | 22 | 21 | 20 | 19      | 18 | 17     | 16 |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 15       | 14 | 13 | 12 | 11      | 10 | 9      | 8  |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 7        | 6  | 5  | 4  | 3       | 2  | 1      | 0  |
| RESERVED |    |    |    | TIMEOUT |    | PARITY |    |
| NONE     |    |    |    | R/WD    |    | R/WD   |    |
| 0h       |    |    |    | 0h      |    | 0h     |    |

**Table 4-2059. ECC\_AGGR\_AGGR\_STATUS\_CLR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                     |
|------|----------|------|-------|-------------------------------------------------|
| 31:4 | RESERVED | NONE | 0h    | Reserved                                        |
| 3:2  | TIMEOUT  | R/WD | 0h    | Interrupt status clear for svbus timeout errors |
| 1:0  | PARITY   | R/WD | 0h    | Interrupt status clear for parity errors        |

## 4.3 ICSSM\_XBAR\_INTR

### ICSSM\_XBAR\_INTR

#### 4.3.1 ICSSM\_XBAR\_INTR Summaries

#### ICSSM\_XBAR\_INTR Summaries

**Table 4-2060. ICSSM\_XBAR\_INTR Registers, Base Address=52E0 3000h, Length=512**

| Offset | Length | Register Name                             | ICSSM_XBAR_INTR Physical Address |
|--------|--------|-------------------------------------------|----------------------------------|
| 0h     | 32     | <a href="#">ICSSM_XBAR_INTR_PID</a>       | 52E0 3000h                       |
| 4h     | 32     | <a href="#">ICSSM_XBAR_INTR_MUXCNTL_J</a> | 52E0 3004h + formula             |

#### 4.3.2 ICSSM\_XBAR\_INTR Registers

#### ICSSM\_XBAR\_INTR Registers

#### 4.3.2.1 ICSSM\_XBAR\_INTR\_PID Register

##### 1 ICSSM\_XBAR\_INTR\_PID Register (Offset = 0h) [reset = 66948100h]

Identification register.

Return to [Summary Table](#)

**Table 4-2061. Instance Table**

| Instance Name   | Physical Address |
|-----------------|------------------|
| ICSSM_XBAR_INTR | 52E0 3000h       |

**Figure 4-676. ICSSM\_XBAR\_INTR\_PID Name Register**

|          |    |        |    |          |        |    |    |
|----------|----|--------|----|----------|--------|----|----|
| 31       | 30 | 29     | 28 | 27       | 26     | 25 | 24 |
| SCHEME   |    | BU     |    | FUNCTION |        |    |    |
| R        |    | R      |    | R        |        |    |    |
| 1h       |    | 2h     |    | 694h     |        |    |    |
| 23       | 22 | 21     | 20 | 19       | 18     | 17 | 16 |
| FUNCTION |    |        |    |          |        |    |    |
| R        |    |        |    |          |        |    |    |
| 694h     |    |        |    |          |        |    |    |
| 15       | 14 | 13     | 12 | 11       | 10     | 9  | 8  |
| RTLVER   |    |        |    |          | MAJREV |    |    |
| R        |    |        |    |          | R      |    |    |
| 10h      |    |        |    |          | 1h     |    |    |
| 7        | 6  | 5      | 4  | 3        | 2      | 1  | 0  |
| CUSTOM   |    | MINREV |    |          |        |    |    |
| R        |    | R      |    |          |        |    |    |
| 0h       |    | 0h     |    |          |        |    |    |

**Table 4-2063. ICSSM\_XBAR\_INTR\_PID Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description   |
|-------|----------|------|-------|---------------|
| 31:30 | SCHEME   | R    | 1h    | Scheme        |
| 29:28 | BU       | R    | 2h    | bu            |
| 27:16 | FUNCTION | R    | 694h  | function      |
| 15:11 | RTLVER   | R    | 10h   | Rtl version   |
| 10:8  | MAJREV   | R    | 1h    | major version |
| 7:6   | CUSTOM   | R    | 0h    | custom id     |
| 5:0   | MINREV   | R    | 0h    | minor version |

#### 4.3.2.2 ICSSM\_XBAR\_INTR\_MUXCNTL\_j Register

##### 1 ICSSM\_XBAR\_INTR\_MUXCNTL\_j Register (Offset = 4h + formula) [reset = 0h]

Interrupt mux control register.

Return to [Summary Table](#)

Offset = (j \* 4h); where j = 0 to 15d

**Table 4-2064. Instance Table**

| Instance Name   | Physical Address     |
|-----------------|----------------------|
| ICSSM_XBAR_INTR | 52E0 3004h + formula |

**Figure 4-677. ICSSM\_XBAR\_INTR\_MUXCNTL\_j Name Register**

|          |    |          |    |    |    |    |            |
|----------|----|----------|----|----|----|----|------------|
| 31       | 30 | 29       | 28 | 27 | 26 | 25 | 24         |
| RESERVED |    |          |    |    |    |    |            |
| NONE     |    |          |    |    |    |    |            |
| 0h       |    |          |    |    |    |    |            |
| 23       | 22 | 21       | 20 | 19 | 18 | 17 | 16         |
| RESERVED |    |          |    |    |    |    | INT_ENABLE |
| NONE     |    |          |    |    |    |    | R/W        |
| 0h       |    |          |    |    |    |    | 0h         |
| 15       | 14 | 13       | 12 | 11 | 10 | 9  | 8          |
| RESERVED |    |          |    |    |    |    |            |
| NONE     |    |          |    |    |    |    |            |
| 0h       |    |          |    |    |    |    |            |
| 7        | 6  | 5        | 4  | 3  | 2  | 1  | 0          |
| RESERVED |    | MUX_CNTL |    |    |    |    |            |
| NONE     |    | R/W      |    |    |    |    |            |
| 0h       |    | 0h       |    |    |    |    |            |

**Table 4-2066. ICSSM\_XBAR\_INTR\_MUXCNTL\_j Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                           |
|-------|------------|------|-------|-------------------------------------------------------|
| 31:17 | RESERVED   | NONE | 0h    | Reserved                                              |
| 16    | INT_ENABLE | R/W  | 0h    | Interrupt j Output Enable.<br>0 Disabled<br>1 Enabled |
| 15:6  | RESERVED   | NONE | 0h    | Reserved                                              |
| 5:0   | MUX_CNTL   | R/W  | 0h    | Mux Control for Interrupt j.                          |

## 4.4 EDMA

### EDMA

#### 4.4.1 EDMA Summaries

#### EDMA Summaries

**Table 4-2067. TPCC Registers, Base Address=52A0 0000h, Length=32768**

| Offset | Length | Register Name                 | EDMA0 Physical Address |
|--------|--------|-------------------------------|------------------------|
| 0h     | 32     | <a href="#">TPCC_PID</a>      | 52A0 0000h             |
| 4h     | 32     | <a href="#">TPCC_CCCFG</a>    | 52A0 0004h             |
| 100h   | 32     | <a href="#">TPCC_DCHMAPN</a>  | 52A0 0100h             |
| 200h   | 32     | <a href="#">TPCC_QCHMAPN</a>  | 52A0 0200h             |
| 240h   | 32     | <a href="#">TPCC_DMAQNUMN</a> | 52A0 0240h             |
| 260h   | 32     | <a href="#">TPCC_QDMAQNUM</a> | 52A0 0260h             |
| 280h   | 32     | <a href="#">TPCC_QUETCMAP</a> | 52A0 0280h             |
| 284h   | 32     | <a href="#">TPCC_QUEPRI</a>   | 52A0 0284h             |
| 300h   | 32     | <a href="#">TPCC_EMR</a>      | 52A0 0300h             |
| 304h   | 32     | <a href="#">TPCC_EMRH</a>     | 52A0 0304h             |
| 308h   | 32     | <a href="#">TPCC_EMCR</a>     | 52A0 0308h             |
| 30Ch   | 32     | <a href="#">TPCC_EMCRH</a>    | 52A0 030Ch             |
| 310h   | 32     | <a href="#">TPCC_QEMR</a>     | 52A0 0310h             |
| 314h   | 32     | <a href="#">TPCC_QEMCR</a>    | 52A0 0314h             |
| 318h   | 32     | <a href="#">TPCC_CCERR</a>    | 52A0 0318h             |
| 31Ch   | 32     | <a href="#">TPCC_CCERRCLR</a> | 52A0 031Ch             |
| 320h   | 32     | <a href="#">TPCC_EEVAL</a>    | 52A0 0320h             |
| 340h   | 32     | <a href="#">TPCC_DRAEM</a>    | 52A0 0340h             |
| 344h   | 32     | <a href="#">TPCC_DRAEHM</a>   | 52A0 0344h             |
| 380h   | 32     | <a href="#">TPCC_QRAEN</a>    | 52A0 0380h             |
| 400h   | 32     | <a href="#">TPCC_QNE0</a>     | 52A0 0400h             |
| 404h   | 32     | <a href="#">TPCC_QNE1</a>     | 52A0 0404h             |
| 408h   | 32     | <a href="#">TPCC_QNE2</a>     | 52A0 0408h             |
| 40Ch   | 32     | <a href="#">TPCC_QNE3</a>     | 52A0 040Ch             |
| 410h   | 32     | <a href="#">TPCC_QNE4</a>     | 52A0 0410h             |
| 414h   | 32     | <a href="#">TPCC_QNE5</a>     | 52A0 0414h             |
| 418h   | 32     | <a href="#">TPCC_QNE6</a>     | 52A0 0418h             |
| 41Ch   | 32     | <a href="#">TPCC_QNE7</a>     | 52A0 041Ch             |
| 420h   | 32     | <a href="#">TPCC_QNE8</a>     | 52A0 0420h             |
| 424h   | 32     | <a href="#">TPCC_QNE9</a>     | 52A0 0424h             |
| 428h   | 32     | <a href="#">TPCC_QNE10</a>    | 52A0 0428h             |
| 42Ch   | 32     | <a href="#">TPCC_QNE11</a>    | 52A0 042Ch             |
| 430h   | 32     | <a href="#">TPCC_QNE12</a>    | 52A0 0430h             |
| 434h   | 32     | <a href="#">TPCC_QNE13</a>    | 52A0 0434h             |
| 438h   | 32     | <a href="#">TPCC_QNE14</a>    | 52A0 0438h             |
| 43Ch   | 32     | <a href="#">TPCC_QNE15</a>    | 52A0 043Ch             |
| 600h   | 32     | <a href="#">TPCC_QSTATN</a>   | 52A0 0600h             |
| 620h   | 32     | <a href="#">TPCC_QWMTHRA</a>  | 52A0 0620h             |

**Table 4-2067. TPCC Registers, Base Address=52A0 0000h, Length=32768 (continued)**

| Offset | Length | Register Name                | EDMA0 Physical Address |
|--------|--------|------------------------------|------------------------|
| 640h   | 32     | <a href="#">TPCC_CCSTAT</a>  | 52A0 0640h             |
| 700h   | 32     | <a href="#">TPCC_AETCTL</a>  | 52A0 0700h             |
| 704h   | 32     | <a href="#">TPCC_AETSTAT</a> | 52A0 0704h             |
| 708h   | 32     | <a href="#">TPCC_AETCMD</a>  | 52A0 0708h             |
| 1000h  | 32     | <a href="#">TPCC_ER</a>      | 52A0 1000h             |
| 1004h  | 32     | <a href="#">TPCC_ERH</a>     | 52A0 1004h             |
| 1008h  | 32     | <a href="#">TPCC_ECR</a>     | 52A0 1008h             |
| 100Ch  | 32     | <a href="#">TPCC_ECRH</a>    | 52A0 100Ch             |
| 1010h  | 32     | <a href="#">TPCC_ESR</a>     | 52A0 1010h             |
| 1014h  | 32     | <a href="#">TPCC_ESRH</a>    | 52A0 1014h             |
| 1018h  | 32     | <a href="#">TPCC_CER</a>     | 52A0 1018h             |
| 101Ch  | 32     | <a href="#">TPCC_CERH</a>    | 52A0 101Ch             |
| 1020h  | 32     | <a href="#">TPCC_EER</a>     | 52A0 1020h             |
| 1024h  | 32     | <a href="#">TPCC_EERH</a>    | 52A0 1024h             |
| 1028h  | 32     | <a href="#">TPCC_EECR</a>    | 52A0 1028h             |
| 102Ch  | 32     | <a href="#">TPCC_EECRH</a>   | 52A0 102Ch             |
| 1030h  | 32     | <a href="#">TPCC_EESR</a>    | 52A0 1030h             |
| 1034h  | 32     | <a href="#">TPCC_EESRH</a>   | 52A0 1034h             |
| 1038h  | 32     | <a href="#">TPCC_SER</a>     | 52A0 1038h             |
| 103Ch  | 32     | <a href="#">TPCC_SERH</a>    | 52A0 103Ch             |
| 1040h  | 32     | <a href="#">TPCC_SECR</a>    | 52A0 1040h             |
| 1044h  | 32     | <a href="#">TPCC_SECRH</a>   | 52A0 1044h             |
| 1050h  | 32     | <a href="#">TPCC_IER</a>     | 52A0 1050h             |
| 1054h  | 32     | <a href="#">TPCC_IERH</a>    | 52A0 1054h             |
| 1058h  | 32     | <a href="#">TPCC_IECR</a>    | 52A0 1058h             |
| 105Ch  | 32     | <a href="#">TPCC_IECRH</a>   | 52A0 105Ch             |
| 1060h  | 32     | <a href="#">TPCC_IESR</a>    | 52A0 1060h             |
| 1064h  | 32     | <a href="#">TPCC_IESRH</a>   | 52A0 1064h             |
| 1068h  | 32     | <a href="#">TPCC_IPR</a>     | 52A0 1068h             |
| 106Ch  | 32     | <a href="#">TPCC_IPRH</a>    | 52A0 106Ch             |
| 1070h  | 32     | <a href="#">TPCC_ICR</a>     | 52A0 1070h             |
| 1074h  | 32     | <a href="#">TPCC_ICRH</a>    | 52A0 1074h             |
| 1078h  | 32     | <a href="#">TPCC_IEVAL</a>   | 52A0 1078h             |
| 1080h  | 32     | <a href="#">TPCC_QER</a>     | 52A0 1080h             |
| 1084h  | 32     | <a href="#">TPCC_QEER</a>    | 52A0 1084h             |
| 1088h  | 32     | <a href="#">TPCC_QEECR</a>   | 52A0 1088h             |
| 108Ch  | 32     | <a href="#">TPCC_QEESR</a>   | 52A0 108Ch             |
| 1090h  | 32     | <a href="#">TPCC_QSER</a>    | 52A0 1090h             |
| 1094h  | 32     | <a href="#">TPCC_QSECR</a>   | 52A0 1094h             |
| 2000h  | 32     | <a href="#">TPCC_ER_RN</a>   | 52A0 2000h             |
| 2004h  | 32     | <a href="#">TPCC_ERH_RN</a>  | 52A0 2004h             |
| 2008h  | 32     | <a href="#">TPCC_ECR_RN</a>  | 52A0 2008h             |
| 200Ch  | 32     | <a href="#">TPCC_ECRH_RN</a> | 52A0 200Ch             |
| 2010h  | 32     | <a href="#">TPCC_ESR_RN</a>  | 52A0 2010h             |
| 2014h  | 32     | <a href="#">TPCC_ESRH_RN</a> | 52A0 2014h             |

**Table 4-2067. TPCC Registers, Base Address=52A0 0000h, Length=32768 (continued)**

| Offset | Length | Register Name                 | EDMA0 Physical Address |
|--------|--------|-------------------------------|------------------------|
| 2018h  | 32     | <a href="#">TPCC_CER_RN</a>   | 52A0 2018h             |
| 201Ch  | 32     | <a href="#">TPCC_CERH_RN</a>  | 52A0 201Ch             |
| 2020h  | 32     | <a href="#">TPCC_EER_RN</a>   | 52A0 2020h             |
| 2024h  | 32     | <a href="#">TPCC_EERH_RN</a>  | 52A0 2024h             |
| 2028h  | 32     | <a href="#">TPCC_EECR_RN</a>  | 52A0 2028h             |
| 202Ch  | 32     | <a href="#">TPCC_EECRH_RN</a> | 52A0 202Ch             |
| 2030h  | 32     | <a href="#">TPCC_EESR_RN</a>  | 52A0 2030h             |
| 2034h  | 32     | <a href="#">TPCC_EESRH_RN</a> | 52A0 2034h             |
| 2038h  | 32     | <a href="#">TPCC_SER_RN</a>   | 52A0 2038h             |
| 203Ch  | 32     | <a href="#">TPCC_SERH_RN</a>  | 52A0 203Ch             |
| 2040h  | 32     | <a href="#">TPCC_SECR_RN</a>  | 52A0 2040h             |
| 2044h  | 32     | <a href="#">TPCC_SECRH_RN</a> | 52A0 2044h             |
| 2050h  | 32     | <a href="#">TPCC_IER_RN</a>   | 52A0 2050h             |
| 2054h  | 32     | <a href="#">TPCC_IERH_RN</a>  | 52A0 2054h             |
| 2058h  | 32     | <a href="#">TPCC_IECR_RN</a>  | 52A0 2058h             |
| 205Ch  | 32     | <a href="#">TPCC_IECRH_RN</a> | 52A0 205Ch             |
| 2060h  | 32     | <a href="#">TPCC_IESR_RN</a>  | 52A0 2060h             |
| 2064h  | 32     | <a href="#">TPCC_IESRH_RN</a> | 52A0 2064h             |
| 2068h  | 32     | <a href="#">TPCC_IPR_RN</a>   | 52A0 2068h             |
| 206Ch  | 32     | <a href="#">TPCC_IPRH_RN</a>  | 52A0 206Ch             |
| 2070h  | 32     | <a href="#">TPCC_ICR_RN</a>   | 52A0 2070h             |
| 2074h  | 32     | <a href="#">TPCC_ICRH_RN</a>  | 52A0 2074h             |
| 2078h  | 32     | <a href="#">TPCC_IEVAL_RN</a> | 52A0 2078h             |
| 2080h  | 32     | <a href="#">TPCC_QER_RN</a>   | 52A0 2080h             |
| 2084h  | 32     | <a href="#">TPCC_QEER_RN</a>  | 52A0 2084h             |
| 2088h  | 32     | <a href="#">TPCC_QEECR_RN</a> | 52A0 2088h             |
| 208Ch  | 32     | <a href="#">TPCC_QEESR_RN</a> | 52A0 208Ch             |
| 2090h  | 32     | <a href="#">TPCC_QSER_RN</a>  | 52A0 2090h             |
| 2094h  | 32     | <a href="#">TPCC_QSECR_RN</a> | 52A0 2094h             |
| 4000h  | 32     | <a href="#">TPCC_OPT</a>      | 52A0 4000h             |
| 4004h  | 32     | <a href="#">TPCC_SRC</a>      | 52A0 4004h             |
| 4008h  | 32     | <a href="#">TPCC_ABCNT</a>    | 52A0 4008h             |
| 400Ch  | 32     | <a href="#">TPCC_DST</a>      | 52A0 400Ch             |
| 4010h  | 32     | <a href="#">TPCC_BIDX</a>     | 52A0 4010h             |
| 4014h  | 32     | <a href="#">TPCC_LNK</a>      | 52A0 4014h             |
| 4018h  | 32     | <a href="#">TPCC_CIDX</a>     | 52A0 4018h             |
| 401Ch  | 32     | <a href="#">TPCC_CCNT</a>     | 52A0 401Ch             |

**Table 4-2068. TPTC Registers, Base Address=52A6 0000h, Length=4096**

| Offset | Length | Register Name                | EDMA0 Physical Address | EDMA1 Physical Address |
|--------|--------|------------------------------|------------------------|------------------------|
| 0h     | 32     | <a href="#">TPTC_PID</a>     | 52A6 0000h             | 52A4 0000h             |
| 4h     | 32     | <a href="#">TPTC_TCCFG</a>   | 52A6 0004h             | 52A4 0004h             |
| 100h   | 32     | <a href="#">TPTC_TCSTAT</a>  | 52A6 0100h             | 52A4 0100h             |
| 104h   | 32     | <a href="#">TPTC_INTSTAT</a> | 52A6 0104h             | 52A4 0104h             |

**Table 4-2068. TPTC Registers, Base Address=52A6 0000h, Length=4096 (continued)**

| Offset | Length | Register Name                  | EDMA0 Physical Address | EDMA1 Physical Address |
|--------|--------|--------------------------------|------------------------|------------------------|
| 108h   | 32     | <a href="#">TPTC_INTEN</a>     | 52A6 0108h             | 52A4 0108h             |
| 10Ch   | 32     | <a href="#">TPTC_INTCLR</a>    | 52A6 010Ch             | 52A4 010Ch             |
| 110h   | 32     | <a href="#">TPTC_INTCMD</a>    | 52A6 0110h             | 52A4 0110h             |
| 120h   | 32     | <a href="#">TPTC_ERRSTAT</a>   | 52A6 0120h             | 52A4 0120h             |
| 124h   | 32     | <a href="#">TPTC_ERREN</a>     | 52A6 0124h             | 52A4 0124h             |
| 128h   | 32     | <a href="#">TPTC_ERRCLR</a>    | 52A6 0128h             | 52A4 0128h             |
| 12Ch   | 32     | <a href="#">TPTC_ERRDET</a>    | 52A6 012Ch             | 52A4 012Ch             |
| 130h   | 32     | <a href="#">TPTC_ERRCMD</a>    | 52A6 0130h             | 52A4 0130h             |
| 140h   | 32     | <a href="#">TPTC_RDRATE</a>    | 52A6 0140h             | 52A4 0140h             |
| 200h   | 32     | <a href="#">TPTC_POPT</a>      | 52A6 0200h             | 52A4 0200h             |
| 204h   | 32     | <a href="#">TPTC_PSRC</a>      | 52A6 0204h             | 52A4 0204h             |
| 208h   | 32     | <a href="#">TPTC_PCNT</a>      | 52A6 0208h             | 52A4 0208h             |
| 20Ch   | 32     | <a href="#">TPTC_PDST</a>      | 52A6 020Ch             | 52A4 020Ch             |
| 210h   | 32     | <a href="#">TPTC_PBDX</a>      | 52A6 0210h             | 52A4 0210h             |
| 214h   | 32     | <a href="#">TPTC_PMPRXY</a>    | 52A6 0214h             | 52A4 0214h             |
| 240h   | 32     | <a href="#">TPTC_SAOPT</a>     | 52A6 0240h             | 52A4 0240h             |
| 244h   | 32     | <a href="#">TPTC_SASRC</a>     | 52A6 0244h             | 52A4 0244h             |
| 248h   | 32     | <a href="#">TPTC_SACNT</a>     | 52A6 0248h             | 52A4 0248h             |
| 24Ch   | 32     | <a href="#">TPTC_SADST</a>     | 52A6 024Ch             | 52A4 024Ch             |
| 250h   | 32     | <a href="#">TPTC_SABDX</a>     | 52A6 0250h             | 52A4 0250h             |
| 254h   | 32     | <a href="#">TPTC_SAMPRXY</a>   | 52A6 0254h             | 52A4 0254h             |
| 258h   | 32     | <a href="#">TPTC_SACNTRLD</a>  | 52A6 0258h             | 52A4 0258h             |
| 25Ch   | 32     | <a href="#">TPTC_SASRCBREF</a> | 52A6 025Ch             | 52A4 025Ch             |
| 260h   | 32     | <a href="#">TPTC_SADSTBREF</a> | 52A6 0260h             | 52A4 0260h             |
| 264h   | 32     | <a href="#">TPTC_SABCNT</a>    | 52A6 0264h             | 52A4 0264h             |
| 280h   | 32     | <a href="#">TPTC_DFCNTRLD</a>  | 52A6 0280h             | 52A4 0280h             |
| 284h   | 32     | <a href="#">TPTC_DFSRCBREF</a> | 52A6 0284h             | 52A4 0284h             |
| 300h   | 32     | <a href="#">TPTC_DFOPT0</a>    | 52A6 0300h             | 52A4 0300h             |
| 304h   | 32     | <a href="#">TPTC_DFSRC0</a>    | 52A6 0304h             | 52A4 0304h             |
| 308h   | 32     | <a href="#">TPTC_DFACNT0</a>   | 52A6 0308h             | 52A4 0308h             |
| 30Ch   | 32     | <a href="#">TPTC_DFDST0</a>    | 52A6 030Ch             | 52A4 030Ch             |
| 310h   | 32     | <a href="#">TPTC_DFBIDX0</a>   | 52A6 0310h             | 52A4 0310h             |
| 314h   | 32     | <a href="#">TPTC_DFMPPRXY0</a> | 52A6 0314h             | 52A4 0314h             |
| 318h   | 32     | <a href="#">TPTC_DFBCNT0</a>   | 52A6 0318h             | 52A4 0318h             |
| 340h   | 32     | <a href="#">TPTC_DFOPT1</a>    | 52A6 0340h             | 52A4 0340h             |
| 344h   | 32     | <a href="#">TPTC_DFSRC1</a>    | 52A6 0344h             | 52A4 0344h             |
| 348h   | 32     | <a href="#">TPTC_DFACNT1</a>   | 52A6 0348h             | 52A4 0348h             |
| 34Ch   | 32     | <a href="#">TPTC_DFDST1</a>    | 52A6 034Ch             | 52A4 034Ch             |
| 350h   | 32     | <a href="#">TPTC_DFBIDX1</a>   | 52A6 0350h             | 52A4 0350h             |
| 354h   | 32     | <a href="#">TPTC_DFMPPRXY1</a> | 52A6 0354h             | 52A4 0354h             |
| 358h   | 32     | <a href="#">TPTC_DFBCNT1</a>   | 52A6 0358h             | 52A4 0358h             |

#### 4.4.2 EDMA Registers

##### EDMA Registers



#### 4.4.2.1 TPCC\_PID Register

##### 1 TPCC\_PID Register (Offset = 0h) [reset = 4001AB00h]

Peripheral ID Register

Return to [Summary Table](#)

**Table 4-2069. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0000h       |

**Figure 4-678. TPCC\_PID Name Register**

|        |    |       |    |      |       |    |    |
|--------|----|-------|----|------|-------|----|----|
| 31     | 30 | 29    | 28 | 27   | 26    | 25 | 24 |
| SCHEME |    | RES1  |    | FUNC |       |    |    |
| R      |    | R     |    | R    |       |    |    |
| 1h     |    | 0h    |    | 1h   |       |    |    |
| 23     | 22 | 21    | 20 | 19   | 18    | 17 | 16 |
| FUNC   |    |       |    |      |       |    |    |
| R      |    |       |    |      |       |    |    |
| 1h     |    |       |    |      |       |    |    |
| 15     | 14 | 13    | 12 | 11   | 10    | 9  | 8  |
| RTL    |    |       |    |      | MAJOR |    |    |
| R      |    |       |    |      | R     |    |    |
| 15h    |    |       |    |      | 3h    |    |    |
| 7      | 6  | 5     | 4  | 3    | 2     | 1  | 0  |
| CUSTOM |    | MINOR |    |      |       |    |    |
| R      |    | R     |    |      |       |    |    |
| 0h     |    | 0h    |    |      |       |    |    |

**Table 4-2071. TPCC\_PID Register Field Descriptions**

| Bit   | Field  | Type | Reset | Description                                                                                                                                               |
|-------|--------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | SCHEME | R    | 1h    | PID Scheme: Used to distinguish between old ID scheme and current. Spare bit to encode future schemes EDMA uses 'new scheme' indicated with value of 0x1. |
| 29:28 | RES1   | R    | 0h    | RESERVE FIELD                                                                                                                                             |
| 27:16 | FUNC   | R    | 1h    | Function indicates a software compatible module family.                                                                                                   |
| 15:11 | RTL    | R    | 15h   | RTL Version                                                                                                                                               |
| 10:8  | MAJOR  | R    | 3h    | Major Revision                                                                                                                                            |
| 7:6   | CUSTOM | R    | 0h    | Custom revision field: Not used on this version of EDMA.                                                                                                  |
| 5:0   | MINOR  | R    | 0h    | Minor Revision                                                                                                                                            |

#### 4.4.2.2 TPCC\_CCCFG Register

##### 1 TPCC\_CCCFG Register (Offset = 4h) [reset = 3314445h]

CC Configuration Register

Return to [Summary Table](#)

**Table 4-2072. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0004h       |

**Figure 4-679. TPCC\_CCCFG Name Register**

| 31   | 30         | 29      | 28 | 27   | 26       | 25      | 24         |
|------|------------|---------|----|------|----------|---------|------------|
| RES2 |            |         |    |      |          | MPEXIST | CHMAPEXIST |
| R    |            |         |    |      |          | R       | R          |
| 0h   |            |         |    |      |          | 1h      | 1h         |
| 23   | 22         | 21      | 20 | 19   | 18       | 17      | 16         |
| RES3 |            | NUMREGN |    | RES4 | NUMTC    |         |            |
| R    |            | R       |    | R    | R        |         |            |
| 0h   |            | 3h      |    | 0h   | 1h       |         |            |
| 15   | 14         | 13      | 12 | 11   | 10       | 9       | 8          |
| RES5 | NUMPAENTRY |         |    | RES6 | NUMINTCH |         |            |
| R    | R          |         |    | R    | R        |         |            |
| 0h   | 4h         |         |    | 0h   | 4h       |         |            |
| 7    | 6          | 5       | 4  | 3    | 2        | 1       | 0          |
| RES7 | NUMQDMACH  |         |    | RES8 | NUMDMACH |         |            |
| R    | R          |         |    | R    | R        |         |            |
| 0h   | 4h         |         |    | 0h   | 5h       |         |            |

**Table 4-2074. TPCC\_CCCFG Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                           |
|-------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------|
| 31:26 | RES2       | R    | 0h    | RESERVE FIELD                                                                                                         |
| 25    | MPEXIST    | R    | 1h    | Memory Protection Existence MPEXIST =<br>0 : No memory protection. MPEXIST =<br>1 : Memory Protection logic included. |
| 24    | CHMAPEXIST | R    | 1h    | Channel Mapping Existence CHMAPEXIST =<br>0 : No Channel mapping. CHMAPEXIST =<br>1 : Channel mapping logic included. |
| 23:22 | RES3       | R    | 0h    | RESERVE FIELD                                                                                                         |
| 21:20 | NUMREGN    | R    | 3h    | Number of MP and Shadow regions                                                                                       |
| 19    | RES4       | R    | 0h    | RESERVE FIELD                                                                                                         |
| 18:16 | NUMTC      | R    | 1h    | Number of Queues/Number of TCs                                                                                        |
| 15    | RES5       | R    | 0h    | RESERVE FIELD                                                                                                         |
| 14:12 | NUMPAENTRY | R    | 4h    | Number of PaRAM entries                                                                                               |
| 11    | RES6       | R    | 0h    | RESERVE FIELD                                                                                                         |
| 10:8  | NUMINTCH   | R    | 4h    | Number of Interrupt Channels                                                                                          |
| 7     | RES7       | R    | 0h    | RESERVE FIELD                                                                                                         |
| 6:4   | NUMQDMACH  | R    | 4h    | Number of QDMA Channels                                                                                               |
| 3     | RES8       | R    | 0h    | RESERVE FIELD                                                                                                         |
| 2:0   | NUMDMACH   | R    | 5h    | Number of DMA Channels                                                                                                |

#### 4.4.2.3 TPCC\_DCHMAPN Register

##### 1 TPCC\_DCHMAPN Register (Offset = 100h) [reset = 0h]

DMA Channel N mapping to PaRAM.

Return to [Summary Table](#)

**Table 4-2075. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0100h       |

**Figure 4-680. TPCC\_DCHMAPN Name Register**

|         |    |         |        |    |    |    |    |
|---------|----|---------|--------|----|----|----|----|
| 31      | 30 | 29      | 28     | 27 | 26 | 25 | 24 |
| RES10   |    |         |        |    |    |    |    |
| R       |    |         |        |    |    |    |    |
| 0h      |    |         |        |    |    |    |    |
| 23      | 22 | 21      | 20     | 19 | 18 | 17 | 16 |
| RES10   |    |         |        |    |    |    |    |
| R       |    |         |        |    |    |    |    |
| 0h      |    |         |        |    |    |    |    |
| 15      | 14 | 13      | 12     | 11 | 10 | 9  | 8  |
| RES10   |    | PAENTRY |        |    |    |    |    |
| R       |    | R/W     |        |    |    |    |    |
| 0h      |    | 0h      |        |    |    |    |    |
| 7       | 6  | 5       | 4      | 3  | 2  | 1  | 0  |
| PAENTRY |    |         | RES100 |    |    |    |    |
| R/W     |    |         | R      |    |    |    |    |
| 0h      |    |         | 0h     |    |    |    |    |

**Table 4-2077. TPCC\_DCHMAPN Register Field Descriptions**

| Bit   | Field   | Type | Reset | Description                                                |
|-------|---------|------|-------|------------------------------------------------------------|
| 31:14 | RES10   | R    | 0h    | RESERVE FIELD                                              |
| 13:5  | PAENTRY | R/W  | 0h    | PAENTRY points to the PaRAM Entry number for DMA Channel N |
| 4:0   | RES100  | R    | 0h    | RESERVE FIELD                                              |

#### 4.4.2.4 TPCC\_QCHMAPN Register

##### 1 TPCC\_QCHMAPN Register (Offset = 200h) [reset = 0h]

QDMA Channel N Mapping Register

Return to [Summary Table](#)

**Table 4-2078. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0200h       |

**Figure 4-681. TPCC\_QCHMAPN Name Register**

|         |    |         |        |    |    |          |    |
|---------|----|---------|--------|----|----|----------|----|
| 31      | 30 | 29      | 28     | 27 | 26 | 25       | 24 |
| RES10   |    |         |        |    |    |          |    |
| R       |    |         |        |    |    |          |    |
| 0h      |    |         |        |    |    |          |    |
| 23      | 22 | 21      | 20     | 19 | 18 | 17       | 16 |
| RES10   |    |         |        |    |    |          |    |
| R       |    |         |        |    |    |          |    |
| 0h      |    |         |        |    |    |          |    |
| 15      | 14 | 13      | 12     | 11 | 10 | 9        | 8  |
| RES10   |    | PAENTRY |        |    |    |          |    |
| R       |    | R/W     |        |    |    |          |    |
| 0h      |    | 0h      |        |    |    |          |    |
| 7       | 6  | 5       | 4      | 3  | 2  | 1        | 0  |
| PAENTRY |    |         | TRWORD |    |    | RESERVED |    |
| R/W     |    |         | R/W    |    |    | NONE     |    |
| 0h      |    |         | 0h     |    |    | 0h       |    |

**Table 4-2080. TPCC\_QCHMAPN Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                             |
|-------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:14 | RES10    | R    | 0h    | RESERVE FIELD                                                                                                                                           |
| 13:5  | PAENTRY  | R/W  | 0h    | PaRAM Entry number for QDMA Channel N.                                                                                                                  |
| 4:2   | TRWORD   | R/W  | 0h    | TRWORD points to the specific trigger word of the PaRAM Entry defined by PAENTRY. A write to the trigger word results in a QDMA Event being recognized. |
| 1:0   | RESERVED | NONE | 0h    | Reserved                                                                                                                                                |

#### 4.4.2.5 TPCC\_DMAQNUMN Register

##### 1 TPCC\_DMAQNUMN Register (Offset = 240h) [reset = 0h]

DMA Queue Number Register n Contains the Event queue number to be used for the corresponding DMA Channel.

Return to [Summary Table](#)

**Table 4-2081. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0240h       |

**Figure 4-682. TPCC\_DMAQNUMN Name Register**

| 31    | 30 | 29  | 28 | 27    | 26 | 25  | 24 |
|-------|----|-----|----|-------|----|-----|----|
| RES11 |    | E7  |    | RES12 |    | E6  |    |
| R     |    | R/W |    | R     |    | R/W |    |
| 0h    |    | 0h  |    | 0h    |    | 0h  |    |
| 23    | 22 | 21  | 20 | 19    | 18 | 17  | 16 |
| RES13 |    | E5  |    | RES14 |    | E4  |    |
| R     |    | R/W |    | R     |    | R/W |    |
| 0h    |    | 0h  |    | 0h    |    | 0h  |    |
| 15    | 14 | 13  | 12 | 11    | 10 | 9   | 8  |
| RES15 |    | E3  |    | RES16 |    | E2  |    |
| R     |    | R/W |    | R     |    | R/W |    |
| 0h    |    | 0h  |    | 0h    |    | 0h  |    |
| 7     | 6  | 5   | 4  | 3     | 2  | 1   | 0  |
| RES17 |    | E1  |    | RES18 |    | E0  |    |
| R     |    | R/W |    | R     |    | R/W |    |
| 0h    |    | 0h  |    | 0h    |    | 0h  |    |

**Table 4-2083. TPCC\_DMAQNUMN Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                   |
|-------|-------|------|-------|-------------------------------|
| 31    | RES11 | R    | 0h    | RESERVE FIELD                 |
| 30:28 | E7    | R/W  | 0h    | DMA Queue Number for event #7 |
| 27    | RES12 | R    | 0h    | RESERVE FIELD                 |
| 26:24 | E6    | R/W  | 0h    | DMA Queue Number for event #6 |
| 23    | RES13 | R    | 0h    | RESERVE FIELD                 |
| 22:20 | E5    | R/W  | 0h    | DMA Queue Number for event #5 |
| 19    | RES14 | R    | 0h    | RESERVE FIELD                 |
| 18:16 | E4    | R/W  | 0h    | DMA Queue Number for event #4 |
| 15    | RES15 | R    | 0h    | RESERVE FIELD                 |
| 14:12 | E3    | R/W  | 0h    | DMA Queue Number for event #3 |
| 11    | RES16 | R    | 0h    | RESERVE FIELD                 |
| 10:8  | E2    | R/W  | 0h    | DMA Queue Number for event #2 |
| 7     | RES17 | R    | 0h    | RESERVE FIELD                 |
| 6:4   | E1    | R/W  | 0h    | DMA Queue Number for event #1 |
| 3     | RES18 | R    | 0h    | RESERVE FIELD                 |
| 2:0   | E0    | R/W  | 0h    | DMA Queue Number for event #0 |

#### 4.4.2.6 TPCC\_QDMAQNUM Register

##### 1 TPCC\_QDMAQNUM Register (Offset = 260h) [reset = 0h]

QDMA Queue Number Register Contains the Event queue number to be used for the corresponding QDMA Channel.

Return to [Summary Table](#)

**Table 4-2084. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0260h       |

**Figure 4-683. TPCC\_QDMAQNUM Name Register**

| 31    | 30 | 29  | 28 | 27    | 26 | 25  | 24 |
|-------|----|-----|----|-------|----|-----|----|
| RES19 |    | E7  |    | RES20 |    | E6  |    |
| R     |    | R/W |    | R     |    | R/W |    |
| 0h    |    | 0h  |    | 0h    |    | 0h  |    |
| 23    | 22 | 21  | 20 | 19    | 18 | 17  | 16 |
| RES21 |    | E5  |    | RES22 |    | E4  |    |
| R     |    | R/W |    | R     |    | R/W |    |
| 0h    |    | 0h  |    | 0h    |    | 0h  |    |
| 15    | 14 | 13  | 12 | 11    | 10 | 9   | 8  |
| RES23 |    | E3  |    | RES24 |    | E2  |    |
| R     |    | R/W |    | R     |    | R/W |    |
| 0h    |    | 0h  |    | 0h    |    | 0h  |    |
| 7     | 6  | 5   | 4  | 3     | 2  | 1   | 0  |
| RES25 |    | E1  |    | RES26 |    | E0  |    |
| R     |    | R/W |    | R     |    | R/W |    |
| 0h    |    | 0h  |    | 0h    |    | 0h  |    |

**Table 4-2086. TPCC\_QDMAQNUM Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                    |
|-------|-------|------|-------|--------------------------------|
| 31    | RES19 | R    | 0h    | RESERVE FIELD                  |
| 30:28 | E7    | R/W  | 0h    | QDMA Queue Number for event #7 |
| 27    | RES20 | R    | 0h    | RESERVE FIELD                  |
| 26:24 | E6    | R/W  | 0h    | QDMA Queue Number for event #6 |
| 23    | RES21 | R    | 0h    | RESERVE FIELD                  |
| 22:20 | E5    | R/W  | 0h    | QDMA Queue Number for event #5 |
| 19    | RES22 | R    | 0h    | RESERVE FIELD                  |
| 18:16 | E4    | R/W  | 0h    | QDMA Queue Number for event #4 |
| 15    | RES23 | R    | 0h    | RESERVE FIELD                  |
| 14:12 | E3    | R/W  | 0h    | QDMA Queue Number for event #3 |
| 11    | RES24 | R    | 0h    | RESERVE FIELD                  |
| 10:8  | E2    | R/W  | 0h    | QDMA Queue Number for event #2 |
| 7     | RES25 | R    | 0h    | RESERVE FIELD                  |
| 6:4   | E1    | R/W  | 0h    | QDMA Queue Number for event #1 |
| 3     | RES26 | R    | 0h    | RESERVE FIELD                  |
| 2:0   | E0    | R/W  | 0h    | QDMA Queue Number for event #0 |

#### 4.4.2.7 TPCC\_QUETCMAP Register

##### 1 TPCC\_QUETCMAP Register (Offset = 280h) [reset = 10h]

Queue to TC Mapping

Return to [Summary Table](#)

**Table 4-2087. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0280h       |

**Figure 4-684. TPCC\_QUETCMAP Name Register**

|       |         |    |    |       |         |    |    |
|-------|---------|----|----|-------|---------|----|----|
| 31    | 30      | 29 | 28 | 27    | 26      | 25 | 24 |
| RES27 |         |    |    |       |         |    |    |
| R     |         |    |    |       |         |    |    |
| 0h    |         |    |    |       |         |    |    |
| 23    | 22      | 21 | 20 | 19    | 18      | 17 | 16 |
| RES27 |         |    |    |       |         |    |    |
| R     |         |    |    |       |         |    |    |
| 0h    |         |    |    |       |         |    |    |
| 15    | 14      | 13 | 12 | 11    | 10      | 9  | 8  |
| RES27 |         |    |    |       |         |    |    |
| R     |         |    |    |       |         |    |    |
| 0h    |         |    |    |       |         |    |    |
| 7     | 6       | 5  | 4  | 3     | 2       | 1  | 0  |
| RES27 | TCNUMQ1 |    |    | RES28 | TCNUMQ0 |    |    |
| R     | R/W     |    |    | R     | R/W     |    |    |
| 0h    | 1h      |    |    | 0h    | 0h      |    |    |

**Table 4-2089. TPCC\_QUETCMAP Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                         |
|------|---------|------|-------|-------------------------------------------------------------------------------------|
| 31:7 | RES27   | R    | 0h    | RESERVE FIELD                                                                       |
| 6:4  | TCNUMQ1 | R/W  | 1h    | TC Number for Queue N: Defines the TC number that Event Queue N TRs are written to. |
| 3    | RES28   | R    | 0h    | RESERVE FIELD                                                                       |
| 2:0  | TCNUMQ0 | R/W  | 0h    | TC Number for Queue N: Defines the TC number that Event Queue N TRs are written to. |

#### 4.4.2.8 TPCC\_QUEPRI Register

##### 1 TPCC\_QUEPRI Register (Offset = 284h) [reset = 0h]

Queue Priority

Return to [Summary Table](#)

**Table 4-2090. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0284h       |

**Figure 4-685. TPCC\_QUEPRI Name Register**

|       |       |    |    |       |       |    |    |
|-------|-------|----|----|-------|-------|----|----|
| 31    | 30    | 29 | 28 | 27    | 26    | 25 | 24 |
| RES29 |       |    |    |       |       |    |    |
| R     |       |    |    |       |       |    |    |
| 0h    |       |    |    |       |       |    |    |
| 23    | 22    | 21 | 20 | 19    | 18    | 17 | 16 |
| RES29 |       |    |    |       |       |    |    |
| R     |       |    |    |       |       |    |    |
| 0h    |       |    |    |       |       |    |    |
| 15    | 14    | 13 | 12 | 11    | 10    | 9  | 8  |
| RES29 |       |    |    |       |       |    |    |
| R     |       |    |    |       |       |    |    |
| 0h    |       |    |    |       |       |    |    |
| 7     | 6     | 5  | 4  | 3     | 2     | 1  | 0  |
| RES29 | PRIQ1 |    |    | RES30 | PRIQ0 |    |    |
| R     | R/W   |    |    | R     | R/W   |    |    |
| 0h    | 0h    |    |    | 0h    | 0h    |    |    |

**Table 4-2092. TPCC\_QUEPRI Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                      |
|------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RES29 | R    | 0h    | RESERVE FIELD                                                                                                                                                    |
| 6:4  | PRIQ1 | R/W  | 0h    | Priority Level for Queue 1 Dictates the priority level used for the OPTIONS field programming for Qn TRs. Sets the priority used for TC read and write commands. |
| 3    | RES30 | R    | 0h    | RESERVE FIELD                                                                                                                                                    |
| 2:0  | PRIQ0 | R/W  | 0h    | Priority Level for Queue 0 Dictates the priority level used for the OPTIONS field programming for Qn TRs. Sets the priority used for TC read and write commands. |



#### 4.4.2.9 TPCC\_EMR Register

##### 1 TPCC\_EMR Register (Offset = 300h) [reset = 0h]

Event Missed Register: The Event Missed register is set if 2 events are received without the first event being cleared or if a Null TR is serviced. Chained events (CER) Set Events (ESR) and normal events (ER) are treated individually. If any bit in the EMR register is set (and all errors (including QEMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.

Return to [Summary Table](#)

**Table 4-2093. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0300h       |

**Figure 4-686. TPCC\_EMR Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E31 | E30 | E29 | E28 | E27 | E26 | E25 | E24 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E23 | E22 | E21 | E20 | E19 | E18 | E17 | E16 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E15 | E14 | E13 | E12 | E11 | E10 | E9  | E8  |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E7  | E6  | E5  | E4  | E3  | E2  | E1  | E0  |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2095. TPCC\_EMR Register Field Descriptions**

| Bit | Field | Type | Reset | Description      |
|-----|-------|------|-------|------------------|
| 31  | E31   | R    | 0h    | Event Missed #31 |
| 30  | E30   | R    | 0h    | Event Missed #30 |
| 29  | E29   | R    | 0h    | Event Missed #29 |
| 28  | E28   | R    | 0h    | Event Missed #28 |
| 27  | E27   | R    | 0h    | Event Missed #27 |
| 26  | E26   | R    | 0h    | Event Missed #26 |
| 25  | E25   | R    | 0h    | Event Missed #25 |
| 24  | E24   | R    | 0h    | Event Missed #24 |
| 23  | E23   | R    | 0h    | Event Missed #23 |
| 22  | E22   | R    | 0h    | Event Missed #22 |
| 21  | E21   | R    | 0h    | Event Missed #21 |
| 20  | E20   | R    | 0h    | Event Missed #20 |
| 19  | E19   | R    | 0h    | Event Missed #19 |
| 18  | E18   | R    | 0h    | Event Missed #18 |
| 17  | E17   | R    | 0h    | Event Missed #17 |

**Table 4-2095. TPCC\_EMR Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description      |
|-----|-------|------|-------|------------------|
| 16  | E16   | R    | 0h    | Event Missed #16 |
| 15  | E15   | R    | 0h    | Event Missed #15 |
| 14  | E14   | R    | 0h    | Event Missed #14 |
| 13  | E13   | R    | 0h    | Event Missed #13 |
| 12  | E12   | R    | 0h    | Event Missed #12 |
| 11  | E11   | R    | 0h    | Event Missed #11 |
| 10  | E10   | R    | 0h    | Event Missed #10 |
| 9   | E9    | R    | 0h    | Event Missed #9  |
| 8   | E8    | R    | 0h    | Event Missed #8  |
| 7   | E7    | R    | 0h    | Event Missed #7  |
| 6   | E6    | R    | 0h    | Event Missed #6  |
| 5   | E5    | R    | 0h    | Event Missed #5  |
| 4   | E4    | R    | 0h    | Event Missed #4  |
| 3   | E3    | R    | 0h    | Event Missed #3  |
| 2   | E2    | R    | 0h    | Event Missed #2  |
| 1   | E1    | R    | 0h    | Event Missed #1  |
| 0   | E0    | R    | 0h    | Event Missed #0  |

#### 4.4.2.10 TPCC\_EMRH Register

##### 1 TPCC\_EMRH Register (Offset = 304h) [reset = 0h]

Event Missed Register (High Part): The Event Missed register is set if 2 events are received without the first event being cleared or if a Null TR is serviced. Chained events (CER) Set Events (ESR) and normal events (ER) are treated individually. If any bit in the EMR register is set (and all errors (including QEMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.

Return to [Summary Table](#)

**Table 4-2096. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0304h       |

**Figure 4-687. TPCC\_EMRH Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E63 | E62 | E61 | E60 | E59 | E58 | E57 | E56 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E55 | E54 | E53 | E52 | E51 | E50 | E49 | E48 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E47 | E46 | E45 | E44 | E43 | E42 | E41 | E40 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E39 | E38 | E37 | E36 | E35 | E34 | E33 | E32 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2098. TPCC\_EMRH Register Field Descriptions**

| Bit | Field | Type | Reset | Description      |
|-----|-------|------|-------|------------------|
| 31  | E63   | R    | 0h    | Event Missed #63 |
| 30  | E62   | R    | 0h    | Event Missed #62 |
| 29  | E61   | R    | 0h    | Event Missed #61 |
| 28  | E60   | R    | 0h    | Event Missed #60 |
| 27  | E59   | R    | 0h    | Event Missed #59 |
| 26  | E58   | R    | 0h    | Event Missed #58 |
| 25  | E57   | R    | 0h    | Event Missed #57 |
| 24  | E56   | R    | 0h    | Event Missed #56 |
| 23  | E55   | R    | 0h    | Event Missed #55 |
| 22  | E54   | R    | 0h    | Event Missed #54 |
| 21  | E53   | R    | 0h    | Event Missed #53 |
| 20  | E52   | R    | 0h    | Event Missed #52 |
| 19  | E51   | R    | 0h    | Event Missed #51 |
| 18  | E50   | R    | 0h    | Event Missed #50 |
| 17  | E49   | R    | 0h    | Event Missed #49 |

**Table 4-2098. TPCC\_EMRH Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description      |
|-----|-------|------|-------|------------------|
| 16  | E48   | R    | 0h    | Event Missed #48 |
| 15  | E47   | R    | 0h    | Event Missed #47 |
| 14  | E46   | R    | 0h    | Event Missed #46 |
| 13  | E45   | R    | 0h    | Event Missed #45 |
| 12  | E44   | R    | 0h    | Event Missed #44 |
| 11  | E43   | R    | 0h    | Event Missed #43 |
| 10  | E42   | R    | 0h    | Event Missed #42 |
| 9   | E41   | R    | 0h    | Event Missed #41 |
| 8   | E40   | R    | 0h    | Event Missed #40 |
| 7   | E39   | R    | 0h    | Event Missed #39 |
| 6   | E38   | R    | 0h    | Event Missed #38 |
| 5   | E37   | R    | 0h    | Event Missed #37 |
| 4   | E36   | R    | 0h    | Event Missed #36 |
| 3   | E35   | R    | 0h    | Event Missed #35 |
| 2   | E34   | R    | 0h    | Event Missed #34 |
| 1   | E33   | R    | 0h    | Event Missed #33 |
| 0   | E32   | R    | 0h    | Event Missed #32 |

#### 4.4.2.11 TPCC\_EMCR Register

##### 1 TPCC\_EMCR Register (Offset = 308h) [reset = 0h]

Event Missed Clear Register: CPU write of '1' to the EMCR.En bit causes the EMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.

Return to [Summary Table](#)

**Table 4-2099. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0308h       |

**Figure 4-688. TPCC\_EMCR Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E31 | E30 | E29 | E28 | E27 | E26 | E25 | E24 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E23 | E22 | E21 | E20 | E19 | E18 | E17 | E16 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E15 | E14 | E13 | E12 | E11 | E10 | E9  | E8  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E7  | E6  | E5  | E4  | E3  | E2  | E1  | E0  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2101. TPCC\_EMCR Register Field Descriptions**

| Bit | Field | Type | Reset | Description            |
|-----|-------|------|-------|------------------------|
| 31  | E31   | W    | 0h    | Event Missed Clear #31 |
| 30  | E30   | W    | 0h    | Event Missed Clear #30 |
| 29  | E29   | W    | 0h    | Event Missed Clear #29 |
| 28  | E28   | W    | 0h    | Event Missed Clear #28 |
| 27  | E27   | W    | 0h    | Event Missed Clear #27 |
| 26  | E26   | W    | 0h    | Event Missed Clear #26 |
| 25  | E25   | W    | 0h    | Event Missed Clear #25 |
| 24  | E24   | W    | 0h    | Event Missed Clear #24 |
| 23  | E23   | W    | 0h    | Event Missed Clear #23 |
| 22  | E22   | W    | 0h    | Event Missed Clear #22 |
| 21  | E21   | W    | 0h    | Event Missed Clear #21 |
| 20  | E20   | W    | 0h    | Event Missed Clear #20 |
| 19  | E19   | W    | 0h    | Event Missed Clear #19 |
| 18  | E18   | W    | 0h    | Event Missed Clear #18 |
| 17  | E17   | W    | 0h    | Event Missed Clear #17 |
| 16  | E16   | W    | 0h    | Event Missed Clear #16 |
| 15  | E15   | W    | 0h    | Event Missed Clear #15 |

**Table 4-2101. TPCC\_EMCR Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description            |
|-----|-------|------|-------|------------------------|
| 14  | E14   | W    | 0h    | Event Missed Clear #14 |
| 13  | E13   | W    | 0h    | Event Missed Clear #13 |
| 12  | E12   | W    | 0h    | Event Missed Clear #12 |
| 11  | E11   | W    | 0h    | Event Missed Clear #11 |
| 10  | E10   | W    | 0h    | Event Missed Clear #10 |
| 9   | E9    | W    | 0h    | Event Missed Clear #9  |
| 8   | E8    | W    | 0h    | Event Missed Clear #8  |
| 7   | E7    | W    | 0h    | Event Missed Clear #7  |
| 6   | E6    | W    | 0h    | Event Missed Clear #6  |
| 5   | E5    | W    | 0h    | Event Missed Clear #5  |
| 4   | E4    | W    | 0h    | Event Missed Clear #4  |
| 3   | E3    | W    | 0h    | Event Missed Clear #3  |
| 2   | E2    | W    | 0h    | Event Missed Clear #2  |
| 1   | E1    | W    | 0h    | Event Missed Clear #1  |
| 0   | E0    | W    | 0h    | Event Missed Clear #0  |

#### 4.4.2.12 TPCC\_EMCRH Register

##### 1 TPCC\_EMCRH Register (Offset = 30Ch) [reset = 0h]

Event Missed Clear Register (High Part): CPU write of '1' to the EMCR.En bit causes the EMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.

Return to [Summary Table](#)

**Table 4-2102. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 030Ch       |

**Figure 4-689. TPCC\_EMCRH Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E63 | E62 | E61 | E60 | E59 | E58 | E57 | E56 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E55 | E54 | E53 | E52 | E51 | E50 | E49 | E48 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E47 | E46 | E45 | E44 | E43 | E42 | E41 | E40 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E39 | E38 | E37 | E36 | E35 | E34 | E33 | E32 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2104. TPCC\_EMCRH Register Field Descriptions**

| Bit | Field | Type | Reset | Description            |
|-----|-------|------|-------|------------------------|
| 31  | E63   | W    | 0h    | Event Missed Clear #63 |
| 30  | E62   | W    | 0h    | Event Missed Clear #62 |
| 29  | E61   | W    | 0h    | Event Missed Clear #61 |
| 28  | E60   | W    | 0h    | Event Missed Clear #60 |
| 27  | E59   | W    | 0h    | Event Missed Clear #59 |
| 26  | E58   | W    | 0h    | Event Missed Clear #58 |
| 25  | E57   | W    | 0h    | Event Missed Clear #57 |
| 24  | E56   | W    | 0h    | Event Missed Clear #56 |
| 23  | E55   | W    | 0h    | Event Missed Clear #55 |
| 22  | E54   | W    | 0h    | Event Missed Clear #54 |
| 21  | E53   | W    | 0h    | Event Missed Clear #53 |
| 20  | E52   | W    | 0h    | Event Missed Clear #52 |
| 19  | E51   | W    | 0h    | Event Missed Clear #51 |
| 18  | E50   | W    | 0h    | Event Missed Clear #50 |
| 17  | E49   | W    | 0h    | Event Missed Clear #49 |
| 16  | E48   | W    | 0h    | Event Missed Clear #48 |

**Table 4-2104. TPCC\_EMCRH Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description            |
|-----|-------|------|-------|------------------------|
| 15  | E47   | W    | 0h    | Event Missed Clear #47 |
| 14  | E46   | W    | 0h    | Event Missed Clear #46 |
| 13  | E45   | W    | 0h    | Event Missed Clear #45 |
| 12  | E44   | W    | 0h    | Event Missed Clear #44 |
| 11  | E43   | W    | 0h    | Event Missed Clear #43 |
| 10  | E42   | W    | 0h    | Event Missed Clear #42 |
| 9   | E41   | W    | 0h    | Event Missed Clear #41 |
| 8   | E40   | W    | 0h    | Event Missed Clear #40 |
| 7   | E39   | W    | 0h    | Event Missed Clear #39 |
| 6   | E38   | W    | 0h    | Event Missed Clear #38 |
| 5   | E37   | W    | 0h    | Event Missed Clear #37 |
| 4   | E36   | W    | 0h    | Event Missed Clear #36 |
| 3   | E35   | W    | 0h    | Event Missed Clear #35 |
| 2   | E34   | W    | 0h    | Event Missed Clear #34 |
| 1   | E33   | W    | 0h    | Event Missed Clear #33 |
| 0   | E32   | W    | 0h    | Event Missed Clear #32 |



#### 4.4.2.13 TPCC\_QEMR Register

##### 1 TPCC\_QEMR Register (Offset = 310h) [reset = 0h]

QDMA Event Missed Register: The QDMA Event Missed register is set if 2 QDMA events are detected without the first event being cleared or if a Null TR is serviced.. If any bit in the QEMR register is set (and all errors (including EMR/CCERR) were previously clear) then an error will be signaled with TPCC error interrupt.

Return to [Summary Table](#)

**Table 4-2105. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0310h       |

**Figure 4-690. TPCC\_QEMR Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RES31 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RES31 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RES31 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| E7    | E6 | E5 | E4 | E3 | E2 | E1 | E0 |
| R     | R  | R  | R  | R  | R  | R  | R  |
| 0h    | 0h | 0h | 0h | 0h | 0h | 0h | 0h |

**Table 4-2107. TPCC\_QEMR Register Field Descriptions**

| Bit  | Field | Type | Reset | Description     |
|------|-------|------|-------|-----------------|
| 31:8 | RES31 | R    | 0h    | RESERVE FIELD   |
| 7    | E7    | R    | 0h    | Event Missed #7 |
| 6    | E6    | R    | 0h    | Event Missed #6 |
| 5    | E5    | R    | 0h    | Event Missed #5 |
| 4    | E4    | R    | 0h    | Event Missed #4 |
| 3    | E3    | R    | 0h    | Event Missed #3 |
| 2    | E2    | R    | 0h    | Event Missed #2 |
| 1    | E1    | R    | 0h    | Event Missed #1 |
| 0    | E0    | R    | 0h    | Event Missed #0 |

#### 4.4.2.14 TPCC\_QEMCR Register

##### 1 TPCC\_QEMCR Register (Offset = 314h) [reset = 0h]

QDMA Event Missed Clear Register: CPU write of '1' to the QEMCR.En bit causes the QEMR.En bit to be cleared. CPU write of '0' has no effect.. All error bits must be cleared before additional error interrupts will be asserted by CC.

Return to [Summary Table](#)

**Table 4-2108. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0314h       |

**Figure 4-691. TPCC\_QEMCR Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RES32 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RES32 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RES32 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| E7    | E6 | E5 | E4 | E3 | E2 | E1 | E0 |
| W     | W  | W  | W  | W  | W  | W  | W  |
| 0h    | 0h | 0h | 0h | 0h | 0h | 0h | 0h |

**Table 4-2110. TPCC\_QEMCR Register Field Descriptions**

| Bit  | Field | Type | Reset | Description           |
|------|-------|------|-------|-----------------------|
| 31:8 | RES32 | R    | 0h    | RESERVE FIELD         |
| 7    | E7    | W    | 0h    | Event Missed Clear #7 |
| 6    | E6    | W    | 0h    | Event Missed Clear #6 |
| 5    | E5    | W    | 0h    | Event Missed Clear #5 |
| 4    | E4    | W    | 0h    | Event Missed Clear #4 |
| 3    | E3    | W    | 0h    | Event Missed Clear #3 |
| 2    | E2    | W    | 0h    | Event Missed Clear #2 |
| 1    | E1    | W    | 0h    | Event Missed Clear #1 |
| 0    | E0    | W    | 0h    | Event Missed Clear #0 |

#### 4.4.2.15 TPCC\_CCERR Register

##### 1 TPCC\_CCERR Register (Offset = 318h) [reset = 0h]

CC Error Register

Return to [Summary Table](#)

**Table 4-2111. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0318h       |

**Figure 4-692. TPCC\_CCERR Name Register**

|          |          |          |          |          |          |          |          |
|----------|----------|----------|----------|----------|----------|----------|----------|
| 31       | 30       | 29       | 28       | 27       | 26       | 25       | 24       |
| RES33    |          |          |          |          |          |          |          |
| R        |          |          |          |          |          |          |          |
| 0h       |          |          |          |          |          |          |          |
| 23       | 22       | 21       | 20       | 19       | 18       | 17       | 16       |
| RES33    |          |          |          |          |          | TCERR    |          |
| R        |          |          |          |          |          | R        |          |
| 0h       |          |          |          |          |          | 0h       |          |
| 15       | 14       | 13       | 12       | 11       | 10       | 9        | 8        |
| RES34    |          |          |          |          |          |          |          |
| R        |          |          |          |          |          |          |          |
| 0h       |          |          |          |          |          |          |          |
| 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
| QTHRXCD7 | QTHRXCD6 | QTHRXCD5 | QTHRXCD4 | QTHRXCD3 | QTHRXCD2 | QTHRXCD1 | QTHRXCD0 |
| R        | R        | R        | R        | R        | R        | R        | R        |
| 0h       | 0h       | 0h       | 0h       | 0h       | 0h       | 0h       | 0h       |

**Table 4-2113. TPCC\_CCERR Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | RES33    | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                                                                                                                                                                                   |
| 16    | TCERR    | R    | 0h    | Transfer Completion Code Error: TCCERR =<br>0 : Total number of allowed TCCs outstanding has not been reached.<br>TCCERR = 1 : Total number of allowed TCCs has been reached.<br>TCCERR can be cleared by Writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set [and all errors were previously clear] then an error will be signaled with TPCC error interrupt.     |
| 15:8  | RES34    | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                                                                                                                                                                                   |
| 7     | QTHRXCD7 | R    | 0h    | Queue Threshold Error for Q7: QTHRXCD7 =<br>0 : Watermark/threshold has not been exceeded. QTHRXCD7 =<br>1 : Watermark/threshold has been exceeded. CCERR.QTHRXCD7 can be cleared by Writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set [and all errors [including EMR/QEMR] were previously clear] then an error will be signaled with the TPCC error interrupt. |
| 6     | QTHRXCD6 | R    | 0h    | Queue Threshold Error for Q6: QTHRXCD6 =<br>0 : Watermark/threshold has not been exceeded. QTHRXCD6 =<br>1 : Watermark/threshold has been exceeded. CCERR.QTHRXCD6 can be cleared by Writing a '1' to corresponding bit in CCERRCLR register. If any bit in the CCERR register is set [and all errors [including EMR/QEMR] were previously clear] then an error will be signaled with the TPCC error interrupt. |

**Table 4-2113. TPCC\_CCERR Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-----|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | QTHRXCD5 | R    | 0h    | Queue Threshold Error for Q5: QTHRXCD5 =<br>0 : Watermark/threshold has not been exceeded. QTHRXCD5 =<br>1 : Watermark/threshold has been exceeded. CCERR.QTHRXCD5<br>can be cleared by Writing a '1' to corresponding bit in CCERRCLR<br>register. If any bit in the CCERR register is set [and all errors<br>[including EMR/QEMR] were previously clear] then an error will be<br>signaled with the TPCC error interrupt. |
| 4   | QTHRXCD4 | R    | 0h    | Queue Threshold Error for Q4: QTHRXCD4 =<br>0 : Watermark/threshold has not been exceeded. QTHRXCD4 =<br>1 : Watermark/threshold has been exceeded. CCERR.QTHRXCD4<br>can be cleared by Writing a '1' to corresponding bit in CCERRCLR<br>register. If any bit in the CCERR register is set [and all errors<br>[including EMR/QEMR] were previously clear] then an error will be<br>signaled with the TPCC error interrupt. |
| 3   | QTHRXCD3 | R    | 0h    | Queue Threshold Error for Q3: QTHRXCD3 =<br>0 : Watermark/threshold has not been exceeded. QTHRXCD3 =<br>1 : Watermark/threshold has been exceeded. CCERR.QTHRXCD3<br>can be cleared by Writing a '1' to corresponding bit in CCERRCLR<br>register. If any bit in the CCERR register is set [and all errors<br>[including EMR/QEMR] were previously clear] then an error will be<br>signaled with the TPCC error interrupt. |
| 2   | QTHRXCD2 | R    | 0h    | Queue Threshold Error for Q2: QTHRXCD2 =<br>0 : Watermark/threshold has not been exceeded. QTHRXCD2 =<br>1 : Watermark/threshold has been exceeded. CCERR.QTHRXCD2<br>can be cleared by Writing a '1' to corresponding bit in CCERRCLR<br>register. If any bit in the CCERR register is set [and all errors<br>[including EMR/QEMR] were previously clear] then an error will be<br>signaled with the TPCC error interrupt. |
| 1   | QTHRXCD1 | R    | 0h    | Queue Threshold Error for Q1: QTHRXCD1 =<br>0 : Watermark/threshold has not been exceeded. QTHRXCD1 =<br>1 : Watermark/threshold has been exceeded. CCERR.QTHRXCD1<br>can be cleared by Writing a '1' to corresponding bit in CCERRCLR<br>register. If any bit in the CCERR register is set [and all errors<br>[including EMR/QEMR] were previously clear] then an error will be<br>signaled with the TPCC error interrupt. |
| 0   | QTHRXCD0 | R    | 0h    | Queue Threshold Error for Q0: QTHRXCD0 =<br>0 : Watermark/threshold has not been exceeded. QTHRXCD0 =<br>1 : Watermark/threshold has been exceeded. CCERR.QTHRXCD0<br>can be cleared by Writing a '1' to corresponding bit in CCERRCLR<br>register. If any bit in the CCERR register is set [and all errors<br>[including EMR/QEMR] were previously clear] then an error will be<br>signaled with the TPCC error interrupt. |

#### 4.4.2.16 TPCC\_CCERRCLR Register

##### 1 TPCC\_CCERRCLR Register (Offset = 31Ch) [reset = 0h]

CC Error Clear Register

Return to [Summary Table](#)

**Table 4-2114. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 031Ch       |

**Figure 4-693. TPCC\_CCERRCLR Name Register**

|          |          |          |          |          |          |          |          |
|----------|----------|----------|----------|----------|----------|----------|----------|
| 31       | 30       | 29       | 28       | 27       | 26       | 25       | 24       |
| RES35    |          |          |          |          |          |          |          |
| R        |          |          |          |          |          |          |          |
| 0h       |          |          |          |          |          |          |          |
| 23       | 22       | 21       | 20       | 19       | 18       | 17       | 16       |
| RES35    |          |          |          |          |          | TCERR    |          |
| R        |          |          |          |          |          | W        |          |
| 0h       |          |          |          |          |          | 0h       |          |
| 15       | 14       | 13       | 12       | 11       | 10       | 9        | 8        |
| RES36    |          |          |          |          |          |          |          |
| R        |          |          |          |          |          |          |          |
| 0h       |          |          |          |          |          |          |          |
| 7        | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
| QTHRXCD7 | QTHRXCD6 | QTHRXCD5 | QTHRXCD4 | QTHRXCD3 | QTHRXCD2 | QTHRXCD1 | QTHRXCD0 |
| W        | W        | W        | W        | W        | W        | W        | W        |
| 0h       | 0h       | 0h       | 0h       | 0h       | 0h       | 0h       | 0h       |

**Table 4-2116. TPCC\_CCERRCLR Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                            |
|-------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | RES35    | R    | 0h    | RESERVE FIELD                                                                                                                          |
| 16    | TCERR    | W    | 0h    | Clear Error for CCERR.TCERR: Write of '1' clears the value of CCERR bit N. Writes of '0' have no affect.                               |
| 15:8  | RES36    | R    | 0h    | RESERVE FIELD                                                                                                                          |
| 7     | QTHRXCD7 | W    | 0h    | Clear error for CCERR.QTHRXCD7: Write of '1' clears the values of QSTAT7.WM QSTAT7.THRXCD CCERR.QTHRXCD7 Writes of '0' have no affect. |
| 6     | QTHRXCD6 | W    | 0h    | Clear error for CCERR.QTHRXCD6: Write of '1' clears the values of QSTAT6.WM QSTAT6.THRXCD CCERR.QTHRXCD6 Writes of '0' have no affect. |
| 5     | QTHRXCD5 | W    | 0h    | Clear error for CCERR.QTHRXCD5: Write of '1' clears the values of QSTAT5.WM QSTAT5.THRXCD CCERR.QTHRXCD5 Writes of '0' have no affect. |
| 4     | QTHRXCD4 | W    | 0h    | Clear error for CCERR.QTHRXCD4: Write of '1' clears the values of QSTAT4.WM QSTAT4.THRXCD CCERR.QTHRXCD4 Writes of '0' have no affect. |
| 3     | QTHRXCD3 | W    | 0h    | Clear error for CCERR.QTHRXCD3: Write of '1' clears the values of QSTAT3.WM QSTAT3.THRXCD CCERR.QTHRXCD3 Writes of '0' have no affect. |
| 2     | QTHRXCD2 | W    | 0h    | Clear error for CCERR.QTHRXCD2: Write of '1' clears the values of QSTAT2.WM QSTAT2.THRXCD CCERR.QTHRXCD2 Writes of '0' have no affect. |

**Table 4-2116. TPCC\_CCERRCLR Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                                                                                                                            |
|-----|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------|
| 1   | QTHRXCD1 | W    | 0h    | Clear error for CCERR.QTHRXCD1: Write of '1' clears the values of QSTAT1.WM QSTAT1.THRXCD CCERR.QTHRXCD1 Writes of '0' have no affect. |
| 0   | QTHRXCD0 | W    | 0h    | Clear error for CCERR.QTHRXCD0: Write of '1' clears the values of QSTAT0.WM QSTAT0.THRXCD CCERR.QTHRXCD0 Writes of '0' have no affect. |

#### 4.4.2.17 TPCC\_EEVAL Register

##### 1 TPCC\_EEVAL Register (Offset = 320h) [reset = 0h]

Error Eval Register

Return to [Summary Table](#)

**Table 4-2117. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0320h       |

**Figure 4-694. TPCC\_EEVAL Name Register**

|       |    |    |    |    |    |     |      |
|-------|----|----|----|----|----|-----|------|
| 31    | 30 | 29 | 28 | 27 | 26 | 25  | 24   |
| RES37 |    |    |    |    |    |     |      |
| R     |    |    |    |    |    |     |      |
| 0h    |    |    |    |    |    |     |      |
| 23    | 22 | 21 | 20 | 19 | 18 | 17  | 16   |
| RES37 |    |    |    |    |    |     |      |
| R     |    |    |    |    |    |     |      |
| 0h    |    |    |    |    |    |     |      |
| 15    | 14 | 13 | 12 | 11 | 10 | 9   | 8    |
| RES37 |    |    |    |    |    |     |      |
| R     |    |    |    |    |    |     |      |
| 0h    |    |    |    |    |    |     |      |
| 7     | 6  | 5  | 4  | 3  | 2  | 1   | 0    |
| RES37 |    |    |    |    |    | SET | EVAL |
| R     |    |    |    |    |    | W   | W    |
| 0h    |    |    |    |    |    | 0h  | 0h   |

**Table 4-2119. TPCC\_EEVAL Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                          |
|------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RES37 | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                        |
| 1    | SET   | W    | 0h    | Error Interrupt Set: CPU write of '1' to the SET bit causes the TPCC error interrupt to be pulsed regardless of state of EMR/EMRH QEMR or CCERR. CPU write of '0' has no effect.                                     |
| 0    | EVAL  | W    | 0h    | Error Interrupt Evaluate: CPU write of '1' to the EVAL bit causes the TPCC error interrupt to be pulsed if any errors have not been cleared in the EMR/EMRH QEMR or CCERR registers. CPU write of '0' has no effect. |

#### 4.4.2.18 TPCC\_DRAEM Register

##### 1 TPCC\_DRAEM Register (Offset = 340h) [reset = 0h]

DMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt.

Return to [Summary Table](#)

**Table 4-2120. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0340h       |

**Figure 4-695. TPCC\_DRAEM Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E31 | E30 | E29 | E28 | E27 | E26 | E25 | E24 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E23 | E22 | E21 | E20 | E19 | E18 | E17 | E16 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E15 | E14 | E13 | E12 | E11 | E10 | E9  | E8  |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E7  | E6  | E5  | E4  | E3  | E2  | E1  | E0  |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2122. TPCC\_DRAEM Register Field Descriptions**

| Bit | Field | Type | Reset | Description                                   |
|-----|-------|------|-------|-----------------------------------------------|
| 31  | E31   | R/W  | 0h    | DMA Region Access enable for Region M bit #31 |
| 30  | E30   | R/W  | 0h    | DMA Region Access enable for Region M bit #30 |
| 29  | E29   | R/W  | 0h    | DMA Region Access enable for Region M bit #29 |
| 28  | E28   | R/W  | 0h    | DMA Region Access enable for Region M bit #28 |
| 27  | E27   | R/W  | 0h    | DMA Region Access enable for Region M bit #27 |
| 26  | E26   | R/W  | 0h    | DMA Region Access enable for Region M bit #26 |
| 25  | E25   | R/W  | 0h    | DMA Region Access enable for Region M bit #25 |
| 24  | E24   | R/W  | 0h    | DMA Region Access enable for Region M bit #24 |
| 23  | E23   | R/W  | 0h    | DMA Region Access enable for Region M bit #23 |
| 22  | E22   | R/W  | 0h    | DMA Region Access enable for Region M bit #22 |
| 21  | E21   | R/W  | 0h    | DMA Region Access enable for Region M bit #21 |
| 20  | E20   | R/W  | 0h    | DMA Region Access enable for Region M bit #20 |
| 19  | E19   | R/W  | 0h    | DMA Region Access enable for Region M bit #19 |
| 18  | E18   | R/W  | 0h    | DMA Region Access enable for Region M bit #18 |



**Table 4-2122. TPCC\_DRAEM Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                   |
|-----|-------|------|-------|-----------------------------------------------|
| 17  | E17   | R/W  | 0h    | DMA Region Access enable for Region M bit #17 |
| 16  | E16   | R/W  | 0h    | DMA Region Access enable for Region M bit #16 |
| 15  | E15   | R/W  | 0h    | DMA Region Access enable for Region M bit #15 |
| 14  | E14   | R/W  | 0h    | DMA Region Access enable for Region M bit #14 |
| 13  | E13   | R/W  | 0h    | DMA Region Access enable for Region M bit #13 |
| 12  | E12   | R/W  | 0h    | DMA Region Access enable for Region M bit #12 |
| 11  | E11   | R/W  | 0h    | DMA Region Access enable for Region M bit #11 |
| 10  | E10   | R/W  | 0h    | DMA Region Access enable for Region M bit #10 |
| 9   | E9    | R/W  | 0h    | DMA Region Access enable for Region M bit #9  |
| 8   | E8    | R/W  | 0h    | DMA Region Access enable for Region M bit #8  |
| 7   | E7    | R/W  | 0h    | DMA Region Access enable for Region M bit #7  |
| 6   | E6    | R/W  | 0h    | DMA Region Access enable for Region M bit #6  |
| 5   | E5    | R/W  | 0h    | DMA Region Access enable for Region M bit #5  |
| 4   | E4    | R/W  | 0h    | DMA Region Access enable for Region M bit #4  |
| 3   | E3    | R/W  | 0h    | DMA Region Access enable for Region M bit #3  |
| 2   | E2    | R/W  | 0h    | DMA Region Access enable for Region M bit #2  |
| 1   | E1    | R/W  | 0h    | DMA Region Access enable for Region M bit #1  |
| 0   | E0    | R/W  | 0h    | DMA Region Access enable for Region M bit #0  |

#### 4.4.2.19 TPCC\_DRAEHM Register

##### 1 TPCC\_DRAEHM Register (Offset = 344h) [reset = 0h]

DMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt. En = 0 : Accesses via Region M address space to Bit N in any DMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any DMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region M interrupt.

Return to [Summary Table](#)

**Table 4-2123. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0344h       |

**Figure 4-696. TPCC\_DRAEHM Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E63 | E62 | E61 | E60 | E59 | E58 | E57 | E56 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E55 | E54 | E53 | E52 | E51 | E50 | E49 | E48 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E47 | E46 | E45 | E44 | E43 | E42 | E41 | E40 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E39 | E38 | E37 | E36 | E35 | E34 | E33 | E32 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2125. TPCC\_DRAEHM Register Field Descriptions**

| Bit | Field | Type | Reset | Description                                   |
|-----|-------|------|-------|-----------------------------------------------|
| 31  | E63   | R/W  | 0h    | DMA Region Access enable for Region M bit #63 |
| 30  | E62   | R/W  | 0h    | DMA Region Access enable for Region M bit #62 |
| 29  | E61   | R/W  | 0h    | DMA Region Access enable for Region M bit #61 |
| 28  | E60   | R/W  | 0h    | DMA Region Access enable for Region M bit #60 |
| 27  | E59   | R/W  | 0h    | DMA Region Access enable for Region M bit #59 |
| 26  | E58   | R/W  | 0h    | DMA Region Access enable for Region M bit #58 |
| 25  | E57   | R/W  | 0h    | DMA Region Access enable for Region M bit #57 |
| 24  | E56   | R/W  | 0h    | DMA Region Access enable for Region M bit #56 |
| 23  | E55   | R/W  | 0h    | DMA Region Access enable for Region M bit #55 |

**Table 4-2125. TPCC\_DRAEHM Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                   |
|-----|-------|------|-------|-----------------------------------------------|
| 22  | E54   | R/W  | 0h    | DMA Region Access enable for Region M bit #54 |
| 21  | E53   | R/W  | 0h    | DMA Region Access enable for Region M bit #53 |
| 20  | E52   | R/W  | 0h    | DMA Region Access enable for Region M bit #52 |
| 19  | E51   | R/W  | 0h    | DMA Region Access enable for Region M bit #51 |
| 18  | E50   | R/W  | 0h    | DMA Region Access enable for Region M bit #50 |
| 17  | E49   | R/W  | 0h    | DMA Region Access enable for Region M bit #49 |
| 16  | E48   | R/W  | 0h    | DMA Region Access enable for Region M bit #48 |
| 15  | E47   | R/W  | 0h    | DMA Region Access enable for Region M bit #47 |
| 14  | E46   | R/W  | 0h    | DMA Region Access enable for Region M bit #46 |
| 13  | E45   | R/W  | 0h    | DMA Region Access enable for Region M bit #45 |
| 12  | E44   | R/W  | 0h    | DMA Region Access enable for Region M bit #44 |
| 11  | E43   | R/W  | 0h    | DMA Region Access enable for Region M bit #43 |
| 10  | E42   | R/W  | 0h    | DMA Region Access enable for Region M bit #42 |
| 9   | E41   | R/W  | 0h    | DMA Region Access enable for Region M bit #41 |
| 8   | E40   | R/W  | 0h    | DMA Region Access enable for Region M bit #40 |
| 7   | E39   | R/W  | 0h    | DMA Region Access enable for Region M bit #39 |
| 6   | E38   | R/W  | 0h    | DMA Region Access enable for Region M bit #38 |
| 5   | E37   | R/W  | 0h    | DMA Region Access enable for Region M bit #37 |
| 4   | E36   | R/W  | 0h    | DMA Region Access enable for Region M bit #36 |
| 3   | E35   | R/W  | 0h    | DMA Region Access enable for Region M bit #35 |
| 2   | E34   | R/W  | 0h    | DMA Region Access enable for Region M bit #34 |
| 1   | E33   | R/W  | 0h    | DMA Region Access enable for Region M bit #33 |
| 0   | E32   | R/W  | 0h    | DMA Region Access enable for Region M bit #32 |

#### 4.4.2.20 TPCC\_QRAEN Register

##### 1 TPCC\_QRAEN Register (Offset = 380h) [reset = 0h]

QDMA Region Access enable for bit N in Region M: En = 0 : Accesses via Region M address space to Bit N in any QDMA Channel Register are not allowed. Reads will return 'b0 on Bit N and writes will not modify the state of bit N. Enabled interrupt bits for bit N do not contribute to the generation of the TPCC region M interrupt. En = 1 : Accesses via Region M address space to Bit N in any QDMA Channel Register are allowed. Reads will return the value from Bit N and writes will modify the state of bit N. Enabled interrupt bits for bit N do contribute to the generation of the TPCC region n interrupt.

Return to [Summary Table](#)

**Table 4-2126. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0380h       |

**Figure 4-697. TPCC\_QRAEN Name Register**

|       |     |     |     |     |     |     |     |
|-------|-----|-----|-----|-----|-----|-----|-----|
| 31    | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
| RES38 |     |     |     |     |     |     |     |
| R     |     |     |     |     |     |     |     |
| 0h    |     |     |     |     |     |     |     |
| 23    | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| RES38 |     |     |     |     |     |     |     |
| R     |     |     |     |     |     |     |     |
| 0h    |     |     |     |     |     |     |     |
| 15    | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| RES38 |     |     |     |     |     |     |     |
| R     |     |     |     |     |     |     |     |
| 0h    |     |     |     |     |     |     |     |
| 7     | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E7    | E6  | E5  | E4  | E3  | E2  | E1  | E0  |
| R/W   | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| 0h    | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2128. TPCC\_QRAEN Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                   |
|------|-------|------|-------|-----------------------------------------------|
| 31:8 | RES38 | R    | 0h    | RESERVE FIELD                                 |
| 7    | E7    | R/W  | 0h    | QDMA Region Access enable for Region M bit #7 |
| 6    | E6    | R/W  | 0h    | QDMA Region Access enable for Region M bit #6 |
| 5    | E5    | R/W  | 0h    | QDMA Region Access enable for Region M bit #5 |
| 4    | E4    | R/W  | 0h    | QDMA Region Access enable for Region M bit #4 |
| 3    | E3    | R/W  | 0h    | QDMA Region Access enable for Region M bit #3 |
| 2    | E2    | R/W  | 0h    | QDMA Region Access enable for Region M bit #2 |
| 1    | E1    | R/W  | 0h    | QDMA Region Access enable for Region M bit #1 |
| 0    | E0    | R/W  | 0h    | QDMA Region Access enable for Region M bit #0 |

#### 4.4.2.21 TPCC\_QNE0 Register

##### 1 TPCC\_QNE0 Register (Offset = 400h) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 0

Return to [Summary Table](#)

**Table 4-2129. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0400h       |

**Figure 4-698. TPCC\_QNE0 Name Register**

|       |    |    |    |      |    |    |    |
|-------|----|----|----|------|----|----|----|
| 31    | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
| RES39 |    |    |    |      |    |    |    |
| R     |    |    |    |      |    |    |    |
| 0h    |    |    |    |      |    |    |    |
| 23    | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| RES39 |    |    |    |      |    |    |    |
| R     |    |    |    |      |    |    |    |
| 0h    |    |    |    |      |    |    |    |
| 15    | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| RES39 |    |    |    |      |    |    |    |
| R     |    |    |    |      |    |    |    |
| 0h    |    |    |    |      |    |    |    |
| 7     | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| ETYPE |    |    |    | ENUM |    |    |    |
| R     |    |    |    | R    |    |    |    |
| 0h    |    |    |    | 0h   |    |    |    |

**Table 4-2131. TPCC\_QNE0 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                         |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RES39 | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                                       |
| 7:6  | ETYPE | R    | 0h    | Event Type: Specifies the specific Event Type for the given entry in the Event Queue.                                                                                                                                                                               |
| 5:0  | ENUM  | R    | 0h    | Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. |

#### 4.4.2.22 TPCC\_QNE1 Register

##### 1 TPCC\_QNE1 Register (Offset = 404h) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 1

Return to [Summary Table](#)

**Table 4-2132. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0404h       |

**Figure 4-699. TPCC\_QNE1 Name Register**

|       |    |    |    |      |    |    |    |
|-------|----|----|----|------|----|----|----|
| 31    | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
| RES40 |    |    |    |      |    |    |    |
| R     |    |    |    |      |    |    |    |
| 0h    |    |    |    |      |    |    |    |
| 23    | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| RES40 |    |    |    |      |    |    |    |
| R     |    |    |    |      |    |    |    |
| 0h    |    |    |    |      |    |    |    |
| 15    | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| RES40 |    |    |    |      |    |    |    |
| R     |    |    |    |      |    |    |    |
| 0h    |    |    |    |      |    |    |    |
| 7     | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| ETYPE |    |    |    | ENUM |    |    |    |
| R     |    |    |    | R    |    |    |    |
| 0h    |    |    |    | 0h   |    |    |    |

**Table 4-2134. TPCC\_QNE1 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                         |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RES40 | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                                       |
| 7:6  | ETYPE | R    | 0h    | Event Type: Specifies the specific Event Type for the given entry in the Event Queue.                                                                                                                                                                               |
| 5:0  | ENUM  | R    | 0h    | Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. |

#### 4.4.2.23 TPCC\_QNE2 Register

##### 1 TPCC\_QNE2 Register (Offset = 408h) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 2

Return to [Summary Table](#)

**Table 4-2135. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0408h       |

**Figure 4-700. TPCC\_QNE2 Name Register**

|       |    |      |    |    |    |    |    |
|-------|----|------|----|----|----|----|----|
| 31    | 30 | 29   | 28 | 27 | 26 | 25 | 24 |
| RES41 |    |      |    |    |    |    |    |
| R     |    |      |    |    |    |    |    |
| 0h    |    |      |    |    |    |    |    |
| 23    | 22 | 21   | 20 | 19 | 18 | 17 | 16 |
| RES41 |    |      |    |    |    |    |    |
| R     |    |      |    |    |    |    |    |
| 0h    |    |      |    |    |    |    |    |
| 15    | 14 | 13   | 12 | 11 | 10 | 9  | 8  |
| RES41 |    |      |    |    |    |    |    |
| R     |    |      |    |    |    |    |    |
| 0h    |    |      |    |    |    |    |    |
| 7     | 6  | 5    | 4  | 3  | 2  | 1  | 0  |
| ETYPE |    | ENUM |    |    |    |    |    |
| R     |    | R    |    |    |    |    |    |
| 0h    |    | 0h   |    |    |    |    |    |

**Table 4-2137. TPCC\_QNE2 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                         |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RES41 | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                                       |
| 7:6  | ETYPE | R    | 0h    | Event Type: Specifies the specific Event Type for the given entry in the Event Queue.                                                                                                                                                                               |
| 5:0  | ENUM  | R    | 0h    | Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. |

#### 4.4.2.24 TPCC\_QNE3 Register

##### 1 TPCC\_QNE3 Register (Offset = 40Ch) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 3

Return to [Summary Table](#)

**Table 4-2138. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 040Ch       |

**Figure 4-701. TPCC\_QNE3 Name Register**

|       |    |      |    |    |    |    |    |
|-------|----|------|----|----|----|----|----|
| 31    | 30 | 29   | 28 | 27 | 26 | 25 | 24 |
| RES42 |    |      |    |    |    |    |    |
| R     |    |      |    |    |    |    |    |
| 0h    |    |      |    |    |    |    |    |
| 23    | 22 | 21   | 20 | 19 | 18 | 17 | 16 |
| RES42 |    |      |    |    |    |    |    |
| R     |    |      |    |    |    |    |    |
| 0h    |    |      |    |    |    |    |    |
| 15    | 14 | 13   | 12 | 11 | 10 | 9  | 8  |
| RES42 |    |      |    |    |    |    |    |
| R     |    |      |    |    |    |    |    |
| 0h    |    |      |    |    |    |    |    |
| 7     | 6  | 5    | 4  | 3  | 2  | 1  | 0  |
| ETYPE |    | ENUM |    |    |    |    |    |
| R     |    | R    |    |    |    |    |    |
| 0h    |    | 0h   |    |    |    |    |    |

**Table 4-2140. TPCC\_QNE3 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                         |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RES42 | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                                       |
| 7:6  | ETYPE | R    | 0h    | Event Type: Specifies the specific Event Type for the given entry in the Event Queue.                                                                                                                                                                               |
| 5:0  | ENUM  | R    | 0h    | Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. |



#### 4.4.2.25 TPCC\_QNE4 Register

##### 1 TPCC\_QNE4 Register (Offset = 410h) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 4

Return to [Summary Table](#)

**Table 4-2141. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0410h       |

**Figure 4-702. TPCC\_QNE4 Name Register**

|       |    |      |    |    |    |    |    |
|-------|----|------|----|----|----|----|----|
| 31    | 30 | 29   | 28 | 27 | 26 | 25 | 24 |
| RES43 |    |      |    |    |    |    |    |
| R     |    |      |    |    |    |    |    |
| 0h    |    |      |    |    |    |    |    |
| 23    | 22 | 21   | 20 | 19 | 18 | 17 | 16 |
| RES43 |    |      |    |    |    |    |    |
| R     |    |      |    |    |    |    |    |
| 0h    |    |      |    |    |    |    |    |
| 15    | 14 | 13   | 12 | 11 | 10 | 9  | 8  |
| RES43 |    |      |    |    |    |    |    |
| R     |    |      |    |    |    |    |    |
| 0h    |    |      |    |    |    |    |    |
| 7     | 6  | 5    | 4  | 3  | 2  | 1  | 0  |
| ETYPE |    | ENUM |    |    |    |    |    |
| R     |    | R    |    |    |    |    |    |
| 0h    |    | 0h   |    |    |    |    |    |

**Table 4-2143. TPCC\_QNE4 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                         |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RES43 | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                                       |
| 7:6  | ETYPE | R    | 0h    | Event Type: Specifies the specific Event Type for the given entry in the Event Queue.                                                                                                                                                                               |
| 5:0  | ENUM  | R    | 0h    | Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. |

#### 4.4.2.26 TPCC\_QNE5 Register

##### 1 TPCC\_QNE5 Register (Offset = 414h) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 5

Return to [Summary Table](#)

**Table 4-2144. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0414h       |

**Figure 4-703. TPCC\_QNE5 Name Register**

|       |    |      |    |    |    |    |    |
|-------|----|------|----|----|----|----|----|
| 31    | 30 | 29   | 28 | 27 | 26 | 25 | 24 |
| RES44 |    |      |    |    |    |    |    |
| R     |    |      |    |    |    |    |    |
| 0h    |    |      |    |    |    |    |    |
| 23    | 22 | 21   | 20 | 19 | 18 | 17 | 16 |
| RES44 |    |      |    |    |    |    |    |
| R     |    |      |    |    |    |    |    |
| 0h    |    |      |    |    |    |    |    |
| 15    | 14 | 13   | 12 | 11 | 10 | 9  | 8  |
| RES44 |    |      |    |    |    |    |    |
| R     |    |      |    |    |    |    |    |
| 0h    |    |      |    |    |    |    |    |
| 7     | 6  | 5    | 4  | 3  | 2  | 1  | 0  |
| ETYPE |    | ENUM |    |    |    |    |    |
| R     |    | R    |    |    |    |    |    |
| 0h    |    | 0h   |    |    |    |    |    |

**Table 4-2146. TPCC\_QNE5 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                         |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RES44 | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                                       |
| 7:6  | ETYPE | R    | 0h    | Event Type: Specifies the specific Event Type for the given entry in the Event Queue.                                                                                                                                                                               |
| 5:0  | ENUM  | R    | 0h    | Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. |

#### 4.4.2.27 TPCC\_QNE6 Register

##### 1 TPCC\_QNE6 Register (Offset = 418h) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 6

Return to [Summary Table](#)

**Table 4-2147. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0418h       |

**Figure 4-704. TPCC\_QNE6 Name Register**

|       |    |      |    |    |    |    |    |
|-------|----|------|----|----|----|----|----|
| 31    | 30 | 29   | 28 | 27 | 26 | 25 | 24 |
| RES45 |    |      |    |    |    |    |    |
| R     |    |      |    |    |    |    |    |
| 0h    |    |      |    |    |    |    |    |
| 23    | 22 | 21   | 20 | 19 | 18 | 17 | 16 |
| RES45 |    |      |    |    |    |    |    |
| R     |    |      |    |    |    |    |    |
| 0h    |    |      |    |    |    |    |    |
| 15    | 14 | 13   | 12 | 11 | 10 | 9  | 8  |
| RES45 |    |      |    |    |    |    |    |
| R     |    |      |    |    |    |    |    |
| 0h    |    |      |    |    |    |    |    |
| 7     | 6  | 5    | 4  | 3  | 2  | 1  | 0  |
| ETYPE |    | ENUM |    |    |    |    |    |
| R     |    | R    |    |    |    |    |    |
| 0h    |    | 0h   |    |    |    |    |    |

**Table 4-2149. TPCC\_QNE6 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                         |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RES45 | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                                       |
| 7:6  | ETYPE | R    | 0h    | Event Type: Specifies the specific Event Type for the given entry in the Event Queue.                                                                                                                                                                               |
| 5:0  | ENUM  | R    | 0h    | Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. |

#### 4.4.2.28 TPCC\_QNE7 Register

##### 1 TPCC\_QNE7 Register (Offset = 41Ch) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 7

Return to [Summary Table](#)

**Table 4-2150. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 041Ch       |

**Figure 4-705. TPCC\_QNE7 Name Register**

|       |    |    |    |      |    |    |    |
|-------|----|----|----|------|----|----|----|
| 31    | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
| RES46 |    |    |    |      |    |    |    |
| R     |    |    |    |      |    |    |    |
| 0h    |    |    |    |      |    |    |    |
| 23    | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| RES46 |    |    |    |      |    |    |    |
| R     |    |    |    |      |    |    |    |
| 0h    |    |    |    |      |    |    |    |
| 15    | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| RES46 |    |    |    |      |    |    |    |
| R     |    |    |    |      |    |    |    |
| 0h    |    |    |    |      |    |    |    |
| 7     | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| ETYPE |    |    |    | ENUM |    |    |    |
| R     |    |    |    | R    |    |    |    |
| 0h    |    |    |    | 0h   |    |    |    |

**Table 4-2152. TPCC\_QNE7 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                         |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RES46 | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                                       |
| 7:6  | ETYPE | R    | 0h    | Event Type: Specifies the specific Event Type for the given entry in the Event Queue.                                                                                                                                                                               |
| 5:0  | ENUM  | R    | 0h    | Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. |

#### 4.4.2.29 TPCC\_QNE8 Register

##### 1 TPCC\_QNE8 Register (Offset = 420h) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 8

Return to [Summary Table](#)

**Table 4-2153. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0420h       |

**Figure 4-706. TPCC\_QNE8 Name Register**

|       |    |      |    |    |    |    |    |
|-------|----|------|----|----|----|----|----|
| 31    | 30 | 29   | 28 | 27 | 26 | 25 | 24 |
| RES47 |    |      |    |    |    |    |    |
| R     |    |      |    |    |    |    |    |
| 0h    |    |      |    |    |    |    |    |
| 23    | 22 | 21   | 20 | 19 | 18 | 17 | 16 |
| RES47 |    |      |    |    |    |    |    |
| R     |    |      |    |    |    |    |    |
| 0h    |    |      |    |    |    |    |    |
| 15    | 14 | 13   | 12 | 11 | 10 | 9  | 8  |
| RES47 |    |      |    |    |    |    |    |
| R     |    |      |    |    |    |    |    |
| 0h    |    |      |    |    |    |    |    |
| 7     | 6  | 5    | 4  | 3  | 2  | 1  | 0  |
| ETYPE |    | ENUM |    |    |    |    |    |
| R     |    | R    |    |    |    |    |    |
| 0h    |    | 0h   |    |    |    |    |    |

**Table 4-2155. TPCC\_QNE8 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                         |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RES47 | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                                       |
| 7:6  | ETYPE | R    | 0h    | Event Type: Specifies the specific Event Type for the given entry in the Event Queue.                                                                                                                                                                               |
| 5:0  | ENUM  | R    | 0h    | Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. |

#### 4.4.2.30 TPCC\_QNE9 Register

##### 1 TPCC\_QNE9 Register (Offset = 424h) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 9

Return to [Summary Table](#)

**Table 4-2156. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0424h       |

**Figure 4-707. TPCC\_QNE9 Name Register**

|       |    |    |    |      |    |    |    |
|-------|----|----|----|------|----|----|----|
| 31    | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
| RES48 |    |    |    |      |    |    |    |
| R     |    |    |    |      |    |    |    |
| 0h    |    |    |    |      |    |    |    |
| 23    | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| RES48 |    |    |    |      |    |    |    |
| R     |    |    |    |      |    |    |    |
| 0h    |    |    |    |      |    |    |    |
| 15    | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| RES48 |    |    |    |      |    |    |    |
| R     |    |    |    |      |    |    |    |
| 0h    |    |    |    |      |    |    |    |
| 7     | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| ETYPE |    |    |    | ENUM |    |    |    |
| R     |    |    |    | R    |    |    |    |
| 0h    |    |    |    | 0h   |    |    |    |

**Table 4-2158. TPCC\_QNE9 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                         |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RES48 | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                                       |
| 7:6  | ETYPE | R    | 0h    | Event Type: Specifies the specific Event Type for the given entry in the Event Queue.                                                                                                                                                                               |
| 5:0  | ENUM  | R    | 0h    | Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. |

#### 4.4.2.31 TPCC\_QNE10 Register

##### 1 TPCC\_QNE10 Register (Offset = 428h) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 0

Return to [Summary Table](#)

**Table 4-2159. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0428h       |

**Figure 4-708. TPCC\_QNE10 Name Register**

|       |    |    |    |      |    |    |    |
|-------|----|----|----|------|----|----|----|
| 31    | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
| RES49 |    |    |    |      |    |    |    |
| R     |    |    |    |      |    |    |    |
| 0h    |    |    |    |      |    |    |    |
| 23    | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| RES49 |    |    |    |      |    |    |    |
| R     |    |    |    |      |    |    |    |
| 0h    |    |    |    |      |    |    |    |
| 15    | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| RES49 |    |    |    |      |    |    |    |
| R     |    |    |    |      |    |    |    |
| 0h    |    |    |    |      |    |    |    |
| 7     | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| ETYPE |    |    |    | ENUM |    |    |    |
| R     |    |    |    | R    |    |    |    |
| 0h    |    |    |    | 0h   |    |    |    |

**Table 4-2161. TPCC\_QNE10 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                         |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RES49 | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                                       |
| 7:6  | ETYPE | R    | 0h    | Event Type: Specifies the specific Event Type for the given entry in the Event Queue.                                                                                                                                                                               |
| 5:0  | ENUM  | R    | 0h    | Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. |

#### 4.4.2.32 TPCC\_QNE11 Register

##### 1 TPCC\_QNE11 Register (Offset = 42Ch) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 11

Return to [Summary Table](#)

**Table 4-2162. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 042Ch       |

**Figure 4-709. TPCC\_QNE11 Name Register**

|       |    |    |    |      |    |    |    |
|-------|----|----|----|------|----|----|----|
| 31    | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
| RES50 |    |    |    |      |    |    |    |
| R     |    |    |    |      |    |    |    |
| 0h    |    |    |    |      |    |    |    |
| 23    | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| RES50 |    |    |    |      |    |    |    |
| R     |    |    |    |      |    |    |    |
| 0h    |    |    |    |      |    |    |    |
| 15    | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| RES50 |    |    |    |      |    |    |    |
| R     |    |    |    |      |    |    |    |
| 0h    |    |    |    |      |    |    |    |
| 7     | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| ETYPE |    |    |    | ENUM |    |    |    |
| R     |    |    |    | R    |    |    |    |
| 0h    |    |    |    | 0h   |    |    |    |

**Table 4-2164. TPCC\_QNE11 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                         |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RES50 | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                                       |
| 7:6  | ETYPE | R    | 0h    | Event Type: Specifies the specific Event Type for the given entry in the Event Queue.                                                                                                                                                                               |
| 5:0  | ENUM  | R    | 0h    | Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. |



#### 4.4.2.33 TPCC\_QNE12 Register

##### 1 TPCC\_QNE12 Register (Offset = 430h) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 12

Return to [Summary Table](#)

**Table 4-2165. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0430h       |

**Figure 4-710. TPCC\_QNE12 Name Register**

|       |    |      |    |    |    |    |    |
|-------|----|------|----|----|----|----|----|
| 31    | 30 | 29   | 28 | 27 | 26 | 25 | 24 |
| RES51 |    |      |    |    |    |    |    |
| R     |    |      |    |    |    |    |    |
| 0h    |    |      |    |    |    |    |    |
| 23    | 22 | 21   | 20 | 19 | 18 | 17 | 16 |
| RES51 |    |      |    |    |    |    |    |
| R     |    |      |    |    |    |    |    |
| 0h    |    |      |    |    |    |    |    |
| 15    | 14 | 13   | 12 | 11 | 10 | 9  | 8  |
| RES51 |    |      |    |    |    |    |    |
| R     |    |      |    |    |    |    |    |
| 0h    |    |      |    |    |    |    |    |
| 7     | 6  | 5    | 4  | 3  | 2  | 1  | 0  |
| ETYPE |    | ENUM |    |    |    |    |    |
| R     |    | R    |    |    |    |    |    |
| 0h    |    | 0h   |    |    |    |    |    |

**Table 4-2167. TPCC\_QNE12 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                         |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RES51 | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                                       |
| 7:6  | ETYPE | R    | 0h    | Event Type: Specifies the specific Event Type for the given entry in the Event Queue.                                                                                                                                                                               |
| 5:0  | ENUM  | R    | 0h    | Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. |

#### 4.4.2.34 TPCC\_QNE13 Register

##### 1 TPCC\_QNE13 Register (Offset = 434h) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 13

Return to [Summary Table](#)

**Table 4-2168. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0434h       |

**Figure 4-711. TPCC\_QNE13 Name Register**

|       |    |      |    |    |    |    |    |
|-------|----|------|----|----|----|----|----|
| 31    | 30 | 29   | 28 | 27 | 26 | 25 | 24 |
| RES52 |    |      |    |    |    |    |    |
| R     |    |      |    |    |    |    |    |
| 0h    |    |      |    |    |    |    |    |
| 23    | 22 | 21   | 20 | 19 | 18 | 17 | 16 |
| RES52 |    |      |    |    |    |    |    |
| R     |    |      |    |    |    |    |    |
| 0h    |    |      |    |    |    |    |    |
| 15    | 14 | 13   | 12 | 11 | 10 | 9  | 8  |
| RES52 |    |      |    |    |    |    |    |
| R     |    |      |    |    |    |    |    |
| 0h    |    |      |    |    |    |    |    |
| 7     | 6  | 5    | 4  | 3  | 2  | 1  | 0  |
| ETYPE |    | ENUM |    |    |    |    |    |
| R     |    | R    |    |    |    |    |    |
| 0h    |    | 0h   |    |    |    |    |    |

**Table 4-2170. TPCC\_QNE13 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                         |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RES52 | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                                       |
| 7:6  | ETYPE | R    | 0h    | Event Type: Specifies the specific Event Type for the given entry in the Event Queue.                                                                                                                                                                               |
| 5:0  | ENUM  | R    | 0h    | Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. |

#### 4.4.2.35 TPCC\_QNE14 Register

##### 1 TPCC\_QNE14 Register (Offset = 438h) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 14

Return to [Summary Table](#)

**Table 4-2171. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0438h       |

**Figure 4-712. TPCC\_QNE14 Name Register**

|       |    |    |    |      |    |    |    |
|-------|----|----|----|------|----|----|----|
| 31    | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
| RES53 |    |    |    |      |    |    |    |
| R     |    |    |    |      |    |    |    |
| 0h    |    |    |    |      |    |    |    |
| 23    | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| RES53 |    |    |    |      |    |    |    |
| R     |    |    |    |      |    |    |    |
| 0h    |    |    |    |      |    |    |    |
| 15    | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| RES53 |    |    |    |      |    |    |    |
| R     |    |    |    |      |    |    |    |
| 0h    |    |    |    |      |    |    |    |
| 7     | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| ETYPE |    |    |    | ENUM |    |    |    |
| R     |    |    |    | R    |    |    |    |
| 0h    |    |    |    | 0h   |    |    |    |

**Table 4-2173. TPCC\_QNE14 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                         |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RES53 | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                                       |
| 7:6  | ETYPE | R    | 0h    | Event Type: Specifies the specific Event Type for the given entry in the Event Queue.                                                                                                                                                                               |
| 5:0  | ENUM  | R    | 0h    | Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. |

#### 4.4.2.36 TPCC\_QNE15 Register

##### 1 TPCC\_QNE15 Register (Offset = 43Ch) [reset = 0h]

Event Queue Entry Diagram for Queue n - Entry 15

Return to [Summary Table](#)

**Table 4-2174. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 043Ch       |

**Figure 4-713. TPCC\_QNE15 Name Register**

|       |    |      |    |    |    |    |    |
|-------|----|------|----|----|----|----|----|
| 31    | 30 | 29   | 28 | 27 | 26 | 25 | 24 |
| RES54 |    |      |    |    |    |    |    |
| R     |    |      |    |    |    |    |    |
| 0h    |    |      |    |    |    |    |    |
| 23    | 22 | 21   | 20 | 19 | 18 | 17 | 16 |
| RES54 |    |      |    |    |    |    |    |
| R     |    |      |    |    |    |    |    |
| 0h    |    |      |    |    |    |    |    |
| 15    | 14 | 13   | 12 | 11 | 10 | 9  | 8  |
| RES54 |    |      |    |    |    |    |    |
| R     |    |      |    |    |    |    |    |
| 0h    |    |      |    |    |    |    |    |
| 7     | 6  | 5    | 4  | 3  | 2  | 1  | 0  |
| ETYPE |    | ENUM |    |    |    |    |    |
| R     |    | R    |    |    |    |    |    |
| 0h    |    | 0h   |    |    |    |    |    |

**Table 4-2176. TPCC\_QNE15 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                         |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RES54 | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                                       |
| 7:6  | ETYPE | R    | 0h    | Event Type: Specifies the specific Event Type for the given entry in the Event Queue.                                                                                                                                                                               |
| 5:0  | ENUM  | R    | 0h    | Event Number: Specifies the specific Event Number for the given entry in the Event Queue. For DMA Channel events [ER/ESR/CER] ENUM will range between 0 and NUM_DMACH [up to 63]. For QDMA Channel events [QER] ENUM will range between 0 and NUM_QDMACH [up to 7]. |

#### 4.4.2.37 TPCC\_QSTATN Register

##### 1 TPCC\_QSTATN Register (Offset = 600h) [reset = 0h]

QSTATn Register Set

Return to [Summary Table](#)
**Table 4-2177. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0600h       |

**Figure 4-714. TPCC\_QSTATN Name Register**

| 31    | 30 | 29 | 28 | 27      | 26 | 25 | 24     |
|-------|----|----|----|---------|----|----|--------|
| RES55 |    |    |    |         |    |    | THRXCD |
| R     |    |    |    |         |    |    | R      |
| 0h    |    |    |    |         |    |    | 0h     |
| 23    | 22 | 21 | 20 | 19      | 18 | 17 | 16     |
| RES56 |    |    |    | WM      |    |    |        |
| R     |    |    |    | R       |    |    |        |
| 0h    |    |    |    | 0h      |    |    |        |
| 15    | 14 | 13 | 12 | 11      | 10 | 9  | 8      |
| RES57 |    |    |    | NUMVAL  |    |    |        |
| R     |    |    |    | R       |    |    |        |
| 0h    |    |    |    | 0h      |    |    |        |
| 7     | 6  | 5  | 4  | 3       | 2  | 1  | 0      |
| RES58 |    |    |    | STRTPTR |    |    |        |
| R     |    |    |    | R       |    |    |        |
| 0h    |    |    |    | 0h      |    |    |        |

**Table 4-2179. TPCC\_QSTATN Register Field Descriptions**

| Bit   | Field   | Type | Reset | Description                                                                                                                                                                                                                                                |
|-------|---------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:25 | RES55   | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                              |
| 24    | THRXCD  | R    | 0h    | Threshold Exceeded: THRXCD =<br>0 : Threshold specified by QWMTHR[A B].Qn has not been exceeded. THRXCD =<br>1 : Threshold specified by QWMTHR[A B].Qn has been exceeded. QSTATn.THXXCD is cleared via CCERR.WMCLRn bit.                                   |
| 23:21 | RES56   | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                              |
| 20:16 | WM      | R    | 0h    | Watermark for Maximum Queue Usage: Watermark tracks the most entries that have been in QueueN since reset or since the last time that the watermark [WM] was cleared. QSTATn.WM is cleared via CCERR.WMCLRn bit. Legal values = 0x0 [empty] to 0x10 [full] |
| 15:13 | RES57   | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                              |
| 12:8  | NUMVAL  | R    | 0h    | Number of Valid Entries in QueueN: Represents the total number of entries residing in the Queue Manager FIFO at a given instant. Always enabled. Legal values = 0x0 [empty] to 0x10 [full]                                                                 |
| 7:4   | RES58   | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                              |
| 3:0   | STRTPTR | R    | 0h    | Start Pointer: Represents the offset to the head entry of QueueN in units of entries. Always enabled. Legal values = 0x0 [0th entry] to 0xF [15th entry]                                                                                                   |

#### 4.4.2.38 TPCC\_QWMTHRA Register

##### 1 TPCC\_QWMTHRA Register (Offset = 620h) [reset = 1010h]

Queue Threshold A for Q[3:0]: CCERR.QTHRXCDn and QSTATn.THRXCD error bit is set when the number of Events in QueueN at an instant in time (visible via QSTATn.NUMVAL) equals or exceeds the value specified by QWMTHRA.Qn. Legal values = 0x0 (ever used?) to 0x10 (ever full?) A value of 0x11 disables threshold errors.

Return to [Summary Table](#)

**Table 4-2180. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0620h       |

**Figure 4-715. TPCC\_QWMTHRA Name Register**

|       |    |    |    |     |    |    |    |
|-------|----|----|----|-----|----|----|----|
| 31    | 30 | 29 | 28 | 27  | 26 | 25 | 24 |
| RES59 |    |    |    |     |    |    |    |
| R     |    |    |    |     |    |    |    |
| 0h    |    |    |    |     |    |    |    |
| 23    | 22 | 21 | 20 | 19  | 18 | 17 | 16 |
| RES59 |    |    |    |     |    |    |    |
| R     |    |    |    |     |    |    |    |
| 0h    |    |    |    |     |    |    |    |
| 15    | 14 | 13 | 12 | 11  | 10 | 9  | 8  |
| RES59 |    |    |    | Q1  |    |    |    |
| R     |    |    |    | R/W |    |    |    |
| 0h    |    |    |    | 10h |    |    |    |
| 7     | 6  | 5  | 4  | 3   | 2  | 1  | 0  |
| RES60 |    |    |    | Q0  |    |    |    |
| R     |    |    |    | R/W |    |    |    |
| 0h    |    |    |    | 10h |    |    |    |

**Table 4-2182. TPCC\_QWMTHRA Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                  |
|-------|-------|------|-------|------------------------------|
| 31:13 | RES59 | R    | 0h    | RESERVE FIELD                |
| 12:8  | Q1    | R/W  | 10h   | Queue Threshold for Q1 value |
| 7:5   | RES60 | R    | 0h    | RESERVE FIELD                |
| 4:0   | Q0    | R/W  | 10h   | Queue Threshold for Q0 value |

#### 4.4.2.39 TPCC\_CCSTAT Register

##### 1 TPCC\_CCSTAT Register (Offset = 640h) [reset = 0h]

CC Status Register

Return to [Summary Table](#)

**Table 4-2183. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0640h       |

**Figure 4-716. TPCC\_CCSTAT Name Register**

|          |          |          |          |          |          |           |          |
|----------|----------|----------|----------|----------|----------|-----------|----------|
| 31       | 30       | 29       | 28       | 27       | 26       | 25        | 24       |
| RES61    |          |          |          |          |          |           |          |
| R        |          |          |          |          |          |           |          |
| 0h       |          |          |          |          |          |           |          |
| 23       | 22       | 21       | 20       | 19       | 18       | 17        | 16       |
| QUEACTV7 | QUEACTV6 | QUEACTV5 | QUEACTV4 | QUEACTV3 | QUEACTV2 | QUEACTV1  | QUEACTV0 |
| R        | R        | R        | R        | R        | R        | R         | R        |
| 0h       | 0h       | 0h       | 0h       | 0h       | 0h       | 0h        | 0h       |
| 15       | 14       | 13       | 12       | 11       | 10       | 9         | 8        |
| RES62    |          | COMPACTV |          |          |          |           |          |
| R        |          | R        |          |          |          |           |          |
| 0h       |          | 0h       |          |          |          |           |          |
| 7        | 6        | 5        | 4        | 3        | 2        | 1         | 0        |
| RES63    |          |          | ACTV     | RES64    | TRACTV   | QEV TACTV | EVTACTV  |
| R        |          |          | R        | R        | R        | R         | R        |
| 0h       |          |          | 0h       | 0h       | 0h       | 0h        | 0h       |

**Table 4-2185. TPCC\_CCSTAT Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                   |
|-------|----------|------|-------|---------------------------------------------------------------------------------------------------------------|
| 31:24 | RES61    | R    | 0h    | RESERVE FIELD                                                                                                 |
| 23    | QUEACTV7 | R    | 0h    | Queue 7 Active QUEACTV7 =<br>0 : No Evts are queued in Q7. QUEACTV7 =<br>1 : At least one TR is queued in Q7. |
| 22    | QUEACTV6 | R    | 0h    | Queue 6 Active QUEACTV6 =<br>0 : No Evts are queued in Q6. QUEACTV6 =<br>1 : At least one TR is queued in Q6. |
| 21    | QUEACTV5 | R    | 0h    | Queue 5 Active QUEACTV5 =<br>0 : No Evts are queued in Q5. QUEACTV5 =<br>1 : At least one TR is queued in Q5. |
| 20    | QUEACTV4 | R    | 0h    | Queue 4 Active QUEACTV4 =<br>0 : No Evts are queued in Q4. QUEACTV4 =<br>1 : At least one TR is queued in Q4. |
| 19    | QUEACTV3 | R    | 0h    | Queue 3 Active QUEACTV3 =<br>0 : No Evts are queued in Q3. QUEACTV3 =<br>1 : At least one TR is queued in Q3. |
| 18    | QUEACTV2 | R    | 0h    | Queue 2 Active QUEACTV2 =<br>0 : No Evts are queued in Q2. QUEACTV2 =<br>1 : At least one TR is queued in Q2. |
| 17    | QUEACTV1 | R    | 0h    | Queue 1 Active QUEACTV1 =<br>0 : No Evts are queued in Q1. QUEACTV1 =<br>1 : At least one TR is queued in Q1. |

**Table 4-2185. TPCC\_CCSTAT Register Field Descriptions (continued)**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 16    | QUEACTV0 | R    | 0h    | Queue 0 Active QUEACTV0 =<br>0 : No Evts are queued in Q0. QUEACTV0 =<br>1 : At least one TR is queued in Q0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 15:14 | RES62    | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 13:8  | COMPACTV | R    | 0h    | Completion Request Active: Counter that tracks the total number of completion requests submitted to the TC. The counter increments when a TR is submitted with TCINTEN or TCCHEN set to '1'. The counter decrements for every valid completion code received from any of the external TCs. The CC will not service new TRs if COMPACTV count is already at the limit. COMPACTV =<br>0 : No completion requests outstanding. COMPACTV =<br>1:Total of '1' completion request outstanding. ... COMPACTV =<br>63 : Total of 63 completion requests are outstanding. No additional TRs will be submitted until count is less than 63. |
| 7:5   | RES63    | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 4     | ACTV     | R    | 0h    | Channel Controller Active: Channel Controller Active is a logical-OR of each of the ACTV signals. The ACTV bit must remain high through the life of a TR. ACTV =<br>0 : Channel is idle. ACTV =<br>1 : Channel is busy.                                                                                                                                                                                                                                                                                                                                                                                                           |
| 3     | RES64    | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 2     | TRACTV   | R    | 0h    | Transfer Request Active: TRACTV =<br>0 : Transfer Request processing/submission logic is inactive. TRACTV =<br>1 : Transfer Request processing/submission logic is active.                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 1     | QEVACTV  | R    | 0h    | QDMA Event Active: QEVACTV =<br>0 : No enabled QDMA Events are active within the CC. QEVACTV =<br>1 : At least one enabled DMA Event [ER & EER ESR CER] is active within the CC.                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 0     | EVTACTV  | R    | 0h    | DMA Event Active: EVTACTV =<br>0 : No enabled DMA Events are active within the CC. EVTACTV =<br>1 : At least one enabled DMA Event [ER & EER ESR CER] is active within the CC.                                                                                                                                                                                                                                                                                                                                                                                                                                                    |



#### 4.4.2.40 TPCC\_AETCTL Register

##### 1 TPCC\_AETCTL Register (Offset = 700h) [reset = 0h]

Advanced Event Trigger Control

Return to [Summary Table](#)

**Table 4-2186. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0700h       |

**Figure 4-717. TPCC\_AETCTL Name Register**

|       |       |         |    |    |    |    |    |
|-------|-------|---------|----|----|----|----|----|
| 31    | 30    | 29      | 28 | 27 | 26 | 25 | 24 |
| EN    | RES65 |         |    |    |    |    |    |
| R/W   | R     |         |    |    |    |    |    |
| 0h    | 0h    |         |    |    |    |    |    |
| 23    | 22    | 21      | 20 | 19 | 18 | 17 | 16 |
| RES65 |       |         |    |    |    |    |    |
| R     |       |         |    |    |    |    |    |
| 0h    |       |         |    |    |    |    |    |
| 15    | 14    | 13      | 12 | 11 | 10 | 9  | 8  |
| RES65 |       | ENDINT  |    |    |    |    |    |
| R     |       | R/W     |    |    |    |    |    |
| 0h    |       | 0h      |    |    |    |    |    |
| 7     | 6     | 5       | 4  | 3  | 2  | 1  | 0  |
| RES66 | TYPE  | STRTEVT |    |    |    |    |    |
| R     | R/W   | R/W     |    |    |    |    |    |
| 0h    | 0h    | 0h      |    |    |    |    |    |

**Table 4-2188. TPCC\_AETCTL Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                             |
|-------|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | EN       | R/W  | 0h    | AET Enable: EN =<br>0 : AET event generation is disabled. EN =<br>1 : AET event generation is enabled.                                                                  |
| 30:14 | RES65    | R    | 0h    | RESERVE FIELD                                                                                                                                                           |
| 13:8  | ENDINT   | R/W  | 0h    | AET End Interrupt: Dictates the completion interrupt number that will force the tpcc_aet signal to be deasserted [low]                                                  |
| 7     | RES66    | R    | 0h    | RESERVE FIELD                                                                                                                                                           |
| 6     | TYPE     | R/W  | 0h    | AET Event Type: TYPE =<br>0 : Event specified by STARTEVT applies to DMA Events [set by ER ESR or CER] TYPE =<br>1 : Event specified by STARTEVT applies to QDMA Events |
| 5:0   | STARTEVT | R/W  | 0h    | AET Start Event: Dictates the Event Number that will force the tpcc_aet signal to be asserted [high]                                                                    |

#### 4.4.2.41 TPCC\_AETSTAT Register

##### 1 TPCC\_AETSTAT Register (Offset = 704h) [reset = 0h]

Advanced Event Trigger Stat

Return to [Summary Table](#)

**Table 4-2189. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0704h       |

**Figure 4-718. TPCC\_AETSTAT Name Register**

|       |    |    |    |    |    |    |      |
|-------|----|----|----|----|----|----|------|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24   |
| RES67 |    |    |    |    |    |    |      |
| R     |    |    |    |    |    |    |      |
| 0h    |    |    |    |    |    |    |      |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16   |
| RES67 |    |    |    |    |    |    |      |
| R     |    |    |    |    |    |    |      |
| 0h    |    |    |    |    |    |    |      |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8    |
| RES67 |    |    |    |    |    |    |      |
| R     |    |    |    |    |    |    |      |
| 0h    |    |    |    |    |    |    |      |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0    |
| RES67 |    |    |    |    |    |    | STAT |
| R     |    |    |    |    |    |    | R    |
| 0h    |    |    |    |    |    |    | 0h   |

**Table 4-2191. TPCC\_AETSTAT Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                          |
|------|-------|------|-------|------------------------------------------------------------------------------------------------------|
| 31:1 | RES67 | R    | 0h    | RESERVE FIELD                                                                                        |
| 0    | STAT  | R    | 0h    | AET Status: AETSTAT =<br>0 : tpcc_aet is currently low. AETSTAT =<br>1 : tpcc_aet is currently high. |

#### 4.4.2.42 TPCC\_AETCMD Register

##### 1 TPCC\_AETCMD Register (Offset = 708h) [reset = 0h]

AET Command

Return to [Summary Table](#)
**Table 4-2192. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 0708h       |

**Figure 4-719. TPCC\_AETCMD Name Register**

|       |    |    |    |    |    |    |     |
|-------|----|----|----|----|----|----|-----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24  |
| RES68 |    |    |    |    |    |    |     |
| R     |    |    |    |    |    |    |     |
| 0h    |    |    |    |    |    |    |     |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16  |
| RES68 |    |    |    |    |    |    |     |
| R     |    |    |    |    |    |    |     |
| 0h    |    |    |    |    |    |    |     |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8   |
| RES68 |    |    |    |    |    |    |     |
| R     |    |    |    |    |    |    |     |
| 0h    |    |    |    |    |    |    |     |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0   |
| RES68 |    |    |    |    |    |    | CLR |
| R     |    |    |    |    |    |    | W   |
| 0h    |    |    |    |    |    |    | 0h  |

**Table 4-2194. TPCC\_AETCMD Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                    |
|------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RES68 | R    | 0h    | RESERVE FIELD                                                                                                                                                  |
| 0    | CLR   | W    | 0h    | AET Clear command: CPU write of '1' to the CLR bit causes the tpcc_aet output signal and AETSTAT.STAT register to be cleared. CPU write of '0' has no effect.. |

#### 4.4.2.43 TPCC\_ER Register

##### 1 TPCC\_ER Register (Offset = 1000h) [reset = 0h]

Event Register: If ER.En bit is set and the EER.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ER.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EER.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ER.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EER register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECR pseudo-register.

Return to [Summary Table](#)

**Table 4-2195. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1000h       |

**Figure 4-720. TPCC\_ER Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E31 | E30 | E29 | E28 | E27 | E26 | E25 | E24 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E23 | E22 | E21 | E20 | E19 | E18 | E17 | E16 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E15 | E14 | E13 | E12 | E11 | E10 | E9  | E8  |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E7  | E6  | E5  | E4  | E3  | E2  | E1  | E0  |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2197. TPCC\_ER Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E31   | R    | 0h    | Event #31   |
| 30  | E30   | R    | 0h    | Event #30   |
| 29  | E29   | R    | 0h    | Event #29   |
| 28  | E28   | R    | 0h    | Event #28   |
| 27  | E27   | R    | 0h    | Event #27   |
| 26  | E26   | R    | 0h    | Event #26   |
| 25  | E25   | R    | 0h    | Event #25   |
| 24  | E24   | R    | 0h    | Event #24   |
| 23  | E23   | R    | 0h    | Event #23   |
| 22  | E22   | R    | 0h    | Event #22   |
| 21  | E21   | R    | 0h    | Event #21   |
| 20  | E20   | R    | 0h    | Event #20   |
| 19  | E19   | R    | 0h    | Event #19   |

**Table 4-2197. TPCC\_ER Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 18  | E18   | R    | 0h    | Event #18   |
| 17  | E17   | R    | 0h    | Event #17   |
| 16  | E16   | R    | 0h    | Event #16   |
| 15  | E15   | R    | 0h    | Event #15   |
| 14  | E14   | R    | 0h    | Event #14   |
| 13  | E13   | R    | 0h    | Event #13   |
| 12  | E12   | R    | 0h    | Event #12   |
| 11  | E11   | R    | 0h    | Event #11   |
| 10  | E10   | R    | 0h    | Event #10   |
| 9   | E9    | R    | 0h    | Event #9    |
| 8   | E8    | R    | 0h    | Event #8    |
| 7   | E7    | R    | 0h    | Event #7    |
| 6   | E6    | R    | 0h    | Event #6    |
| 5   | E5    | R    | 0h    | Event #5    |
| 4   | E4    | R    | 0h    | Event #4    |
| 3   | E3    | R    | 0h    | Event #3    |
| 2   | E2    | R    | 0h    | Event #2    |
| 1   | E1    | R    | 0h    | Event #1    |
| 0   | E0    | R    | 0h    | Event #0    |

#### 4.4.2.44 TPCC\_ERH Register

##### 1 TPCC\_ERH Register (Offset = 1004h) [reset = 0h]

Event Register (High Part): If ERH.En bit is set and the EERH.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ERH.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EERH.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ERH.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EERH register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECRH pseudo-register.

Return to [Summary Table](#)

**Table 4-2198. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1004h       |

**Figure 4-721. TPCC\_ERH Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E63 | E62 | E61 | E60 | E59 | E58 | E57 | E56 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E55 | E54 | E53 | E52 | E51 | E50 | E49 | E48 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E47 | E46 | E45 | E44 | E43 | E42 | E41 | E40 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E39 | E38 | E37 | E36 | E35 | E34 | E33 | E32 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2200. TPCC\_ERH Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E63   | R    | 0h    | Event #63   |
| 30  | E62   | R    | 0h    | Event #62   |
| 29  | E61   | R    | 0h    | Event #61   |
| 28  | E60   | R    | 0h    | Event #60   |
| 27  | E59   | R    | 0h    | Event #59   |
| 26  | E58   | R    | 0h    | Event #58   |
| 25  | E57   | R    | 0h    | Event #57   |
| 24  | E56   | R    | 0h    | Event #56   |
| 23  | E55   | R    | 0h    | Event #55   |
| 22  | E54   | R    | 0h    | Event #54   |
| 21  | E53   | R    | 0h    | Event #53   |
| 20  | E52   | R    | 0h    | Event #52   |
| 19  | E51   | R    | 0h    | Event #51   |

**Table 4-2200. TPCC\_ERH Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 18  | E50   | R    | 0h    | Event #50   |
| 17  | E49   | R    | 0h    | Event #49   |
| 16  | E48   | R    | 0h    | Event #48   |
| 15  | E47   | R    | 0h    | Event #47   |
| 14  | E46   | R    | 0h    | Event #46   |
| 13  | E45   | R    | 0h    | Event #45   |
| 12  | E44   | R    | 0h    | Event #44   |
| 11  | E43   | R    | 0h    | Event #43   |
| 10  | E42   | R    | 0h    | Event #42   |
| 9   | E41   | R    | 0h    | Event #41   |
| 8   | E40   | R    | 0h    | Event #40   |
| 7   | E39   | R    | 0h    | Event #39   |
| 6   | E38   | R    | 0h    | Event #38   |
| 5   | E37   | R    | 0h    | Event #37   |
| 4   | E36   | R    | 0h    | Event #36   |
| 3   | E35   | R    | 0h    | Event #35   |
| 2   | E34   | R    | 0h    | Event #34   |
| 1   | E33   | R    | 0h    | Event #33   |
| 0   | E32   | R    | 0h    | Event #32   |

#### 4.4.2.45 TPCC\_ECR Register

##### 1 TPCC\_ECR Register (Offset = 1008h) [reset = 0h]

Event Clear Register: CPU write of '1' to the ECR.En bit causes the ER.En bit to be cleared. CPU write of '0' has no effect.

Return to [Summary Table](#)

**Table 4-2201. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1008h       |

**Figure 4-722. TPCC\_ECR Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E31 | E30 | E29 | E28 | E27 | E26 | E25 | E24 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E23 | E22 | E21 | E20 | E19 | E18 | E17 | E16 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E15 | E14 | E13 | E12 | E11 | E10 | E9  | E8  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E7  | E6  | E5  | E4  | E3  | E2  | E1  | E0  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2203. TPCC\_ECR Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E31   | W    | 0h    | Event #31   |
| 30  | E30   | W    | 0h    | Event #30   |
| 29  | E29   | W    | 0h    | Event #29   |
| 28  | E28   | W    | 0h    | Event #28   |
| 27  | E27   | W    | 0h    | Event #27   |
| 26  | E26   | W    | 0h    | Event #26   |
| 25  | E25   | W    | 0h    | Event #25   |
| 24  | E24   | W    | 0h    | Event #24   |
| 23  | E23   | W    | 0h    | Event #23   |
| 22  | E22   | W    | 0h    | Event #22   |
| 21  | E21   | W    | 0h    | Event #21   |
| 20  | E20   | W    | 0h    | Event #20   |
| 19  | E19   | W    | 0h    | Event #19   |
| 18  | E18   | W    | 0h    | Event #18   |
| 17  | E17   | W    | 0h    | Event #17   |
| 16  | E16   | W    | 0h    | Event #16   |
| 15  | E15   | W    | 0h    | Event #15   |



**Table 4-2203. TPCC\_ECR Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 14  | E14   | W    | 0h    | Event #14   |
| 13  | E13   | W    | 0h    | Event #13   |
| 12  | E12   | W    | 0h    | Event #12   |
| 11  | E11   | W    | 0h    | Event #11   |
| 10  | E10   | W    | 0h    | Event #10   |
| 9   | E9    | W    | 0h    | Event #9    |
| 8   | E8    | W    | 0h    | Event #8    |
| 7   | E7    | W    | 0h    | Event #7    |
| 6   | E6    | W    | 0h    | Event #6    |
| 5   | E5    | W    | 0h    | Event #5    |
| 4   | E4    | W    | 0h    | Event #4    |
| 3   | E3    | W    | 0h    | Event #3    |
| 2   | E2    | W    | 0h    | Event #2    |
| 1   | E1    | W    | 0h    | Event #1    |
| 0   | E0    | W    | 0h    | Event #0    |

#### 4.4.2.46 TPCC\_ECRH Register

##### 1 TPCC\_ECRH Register (Offset = 100Ch) [reset = 0h]

Event Clear Register (High Part): CPU write of '1' to the ECRH.En bit causes the ERH.En bit to be cleared. CPU write of '0' has no effect.

Return to [Summary Table](#)

**Table 4-2204. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 100Ch       |

**Figure 4-723. TPCC\_ECRH Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E63 | E62 | E61 | E60 | E59 | E58 | E57 | E56 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E55 | E54 | E53 | E52 | E51 | E50 | E49 | E48 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E47 | E46 | E45 | E44 | E43 | E42 | E41 | E40 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E39 | E38 | E37 | E36 | E35 | E34 | E33 | E32 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2206. TPCC\_ECRH Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E63   | W    | 0h    | Event #63   |
| 30  | E62   | W    | 0h    | Event #62   |
| 29  | E61   | W    | 0h    | Event #61   |
| 28  | E60   | W    | 0h    | Event #60   |
| 27  | E59   | W    | 0h    | Event #59   |
| 26  | E58   | W    | 0h    | Event #58   |
| 25  | E57   | W    | 0h    | Event #57   |
| 24  | E56   | W    | 0h    | Event #56   |
| 23  | E55   | W    | 0h    | Event #55   |
| 22  | E54   | W    | 0h    | Event #54   |
| 21  | E53   | W    | 0h    | Event #53   |
| 20  | E52   | W    | 0h    | Event #52   |
| 19  | E51   | W    | 0h    | Event #51   |
| 18  | E50   | W    | 0h    | Event #50   |
| 17  | E49   | W    | 0h    | Event #49   |
| 16  | E48   | W    | 0h    | Event #48   |
| 15  | E47   | W    | 0h    | Event #47   |

**Table 4-2206. TPCC\_ECRH Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 14  | E46   | W    | 0h    | Event #46   |
| 13  | E45   | W    | 0h    | Event #45   |
| 12  | E44   | W    | 0h    | Event #44   |
| 11  | E43   | W    | 0h    | Event #43   |
| 10  | E42   | W    | 0h    | Event #42   |
| 9   | E41   | W    | 0h    | Event #41   |
| 8   | E40   | W    | 0h    | Event #40   |
| 7   | E39   | W    | 0h    | Event #39   |
| 6   | E38   | W    | 0h    | Event #38   |
| 5   | E37   | W    | 0h    | Event #37   |
| 4   | E36   | W    | 0h    | Event #36   |
| 3   | E35   | W    | 0h    | Event #35   |
| 2   | E34   | W    | 0h    | Event #34   |
| 1   | E33   | W    | 0h    | Event #33   |
| 0   | E32   | W    | 0h    | Event #32   |

#### 4.4.2.47 TPCC\_ESR Register

##### 1 TPCC\_ESR Register (Offset = 1010h) [reset = 0h]

Event Set Register: CPU write of '1' to the ESR.En bit causes the ER.En bit to be set. CPU write of '0' has no effect.

Return to [Summary Table](#)

**Table 4-2207. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1010h       |

**Figure 4-724. TPCC\_ESR Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E31 | E30 | E29 | E28 | E27 | E26 | E25 | E24 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E23 | E22 | E21 | E20 | E19 | E18 | E17 | E16 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E15 | E14 | E13 | E12 | E11 | E10 | E9  | E8  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E7  | E6  | E5  | E4  | E3  | E2  | E1  | E0  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2209. TPCC\_ESR Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E31   | W    | 0h    | Event #31   |
| 30  | E30   | W    | 0h    | Event #30   |
| 29  | E29   | W    | 0h    | Event #29   |
| 28  | E28   | W    | 0h    | Event #28   |
| 27  | E27   | W    | 0h    | Event #27   |
| 26  | E26   | W    | 0h    | Event #26   |
| 25  | E25   | W    | 0h    | Event #25   |
| 24  | E24   | W    | 0h    | Event #24   |
| 23  | E23   | W    | 0h    | Event #23   |
| 22  | E22   | W    | 0h    | Event #22   |
| 21  | E21   | W    | 0h    | Event #21   |
| 20  | E20   | W    | 0h    | Event #20   |
| 19  | E19   | W    | 0h    | Event #19   |
| 18  | E18   | W    | 0h    | Event #18   |
| 17  | E17   | W    | 0h    | Event #17   |
| 16  | E16   | W    | 0h    | Event #16   |
| 15  | E15   | W    | 0h    | Event #15   |

**Table 4-2209. TPCC\_ESR Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 14  | E14   | W    | 0h    | Event #14   |
| 13  | E13   | W    | 0h    | Event #13   |
| 12  | E12   | W    | 0h    | Event #12   |
| 11  | E11   | W    | 0h    | Event #11   |
| 10  | E10   | W    | 0h    | Event #10   |
| 9   | E9    | W    | 0h    | Event #9    |
| 8   | E8    | W    | 0h    | Event #8    |
| 7   | E7    | W    | 0h    | Event #7    |
| 6   | E6    | W    | 0h    | Event #6    |
| 5   | E5    | W    | 0h    | Event #5    |
| 4   | E4    | W    | 0h    | Event #4    |
| 3   | E3    | W    | 0h    | Event #3    |
| 2   | E2    | W    | 0h    | Event #2    |
| 1   | E1    | W    | 0h    | Event #1    |
| 0   | E0    | W    | 0h    | Event #0    |

#### 4.4.2.48 TPCC\_ESRH Register

##### 1 TPCC\_ESRH Register (Offset = 1014h) [reset = 0h]

Event Set Register (High Part) CPU write of '1' to the ESRH.En bit causes the ERH.En bit to be set. CPU write of '0' has no effect.

Return to [Summary Table](#)

**Table 4-2210. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1014h       |

**Figure 4-725. TPCC\_ESRH Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E63 | E62 | E61 | E60 | E59 | E58 | E57 | E56 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E55 | E54 | E53 | E52 | E51 | E50 | E49 | E48 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E47 | E46 | E45 | E44 | E43 | E42 | E41 | E40 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E39 | E38 | E37 | E36 | E35 | E34 | E33 | E32 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2212. TPCC\_ESRH Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E63   | W    | 0h    | Event #63   |
| 30  | E62   | W    | 0h    | Event #62   |
| 29  | E61   | W    | 0h    | Event #61   |
| 28  | E60   | W    | 0h    | Event #60   |
| 27  | E59   | W    | 0h    | Event #59   |
| 26  | E58   | W    | 0h    | Event #58   |
| 25  | E57   | W    | 0h    | Event #57   |
| 24  | E56   | W    | 0h    | Event #56   |
| 23  | E55   | W    | 0h    | Event #55   |
| 22  | E54   | W    | 0h    | Event #54   |
| 21  | E53   | W    | 0h    | Event #53   |
| 20  | E52   | W    | 0h    | Event #52   |
| 19  | E51   | W    | 0h    | Event #51   |
| 18  | E50   | W    | 0h    | Event #50   |
| 17  | E49   | W    | 0h    | Event #49   |
| 16  | E48   | W    | 0h    | Event #48   |
| 15  | E47   | W    | 0h    | Event #47   |

**Table 4-2212. TPCC\_ESRH Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 14  | E46   | W    | 0h    | Event #46   |
| 13  | E45   | W    | 0h    | Event #45   |
| 12  | E44   | W    | 0h    | Event #44   |
| 11  | E43   | W    | 0h    | Event #43   |
| 10  | E42   | W    | 0h    | Event #42   |
| 9   | E41   | W    | 0h    | Event #41   |
| 8   | E40   | W    | 0h    | Event #40   |
| 7   | E39   | W    | 0h    | Event #39   |
| 6   | E38   | W    | 0h    | Event #38   |
| 5   | E37   | W    | 0h    | Event #37   |
| 4   | E36   | W    | 0h    | Event #36   |
| 3   | E35   | W    | 0h    | Event #35   |
| 2   | E34   | W    | 0h    | Event #34   |
| 1   | E33   | W    | 0h    | Event #33   |
| 0   | E32   | W    | 0h    | Event #32   |

#### 4.4.2.49 TPCC\_CER Register

##### 1 TPCC\_CER Register (Offset = 1018h) [reset = 0h]

Chained Event Register: If CER.En bit is set (regardless of state of EER.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CER.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CER.En bit is cleared when the corresponding event is prioritized and serviced. If the CER.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CER.En cannot be set or cleared via software.

Return to [Summary Table](#)

**Table 4-2213. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1018h       |

**Figure 4-726. TPCC\_CER Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E31 | E30 | E29 | E28 | E27 | E26 | E25 | E24 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E23 | E22 | E21 | E20 | E19 | E18 | E17 | E16 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E15 | E14 | E13 | E12 | E11 | E10 | E9  | E8  |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E7  | E6  | E5  | E4  | E3  | E2  | E1  | E0  |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2215. TPCC\_CER Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E31   | R    | 0h    | Event #31   |
| 30  | E30   | R    | 0h    | Event #30   |
| 29  | E29   | R    | 0h    | Event #29   |
| 28  | E28   | R    | 0h    | Event #28   |
| 27  | E27   | R    | 0h    | Event #27   |
| 26  | E26   | R    | 0h    | Event #26   |
| 25  | E25   | R    | 0h    | Event #25   |
| 24  | E24   | R    | 0h    | Event #24   |
| 23  | E23   | R    | 0h    | Event #23   |
| 22  | E22   | R    | 0h    | Event #22   |
| 21  | E21   | R    | 0h    | Event #21   |
| 20  | E20   | R    | 0h    | Event #20   |
| 19  | E19   | R    | 0h    | Event #19   |
| 18  | E18   | R    | 0h    | Event #18   |



**Table 4-2215. TPCC\_CER Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 17  | E17   | R    | 0h    | Event #17   |
| 16  | E16   | R    | 0h    | Event #16   |
| 15  | E15   | R    | 0h    | Event #15   |
| 14  | E14   | R    | 0h    | Event #14   |
| 13  | E13   | R    | 0h    | Event #13   |
| 12  | E12   | R    | 0h    | Event #12   |
| 11  | E11   | R    | 0h    | Event #11   |
| 10  | E10   | R    | 0h    | Event #10   |
| 9   | E9    | R    | 0h    | Event #9    |
| 8   | E8    | R    | 0h    | Event #8    |
| 7   | E7    | R    | 0h    | Event #7    |
| 6   | E6    | R    | 0h    | Event #6    |
| 5   | E5    | R    | 0h    | Event #5    |
| 4   | E4    | R    | 0h    | Event #4    |
| 3   | E3    | R    | 0h    | Event #3    |
| 2   | E2    | R    | 0h    | Event #2    |
| 1   | E1    | R    | 0h    | Event #1    |
| 0   | E0    | R    | 0h    | Event #0    |

#### 4.4.2.50 TPCC\_CERH Register

##### 1 TPCC\_CERH Register (Offset = 101Ch) [reset = 0h]

Chained Event Register (High Part): If CERH.En bit is set (regardless of state of EERH.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CERH.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CERH.En bit is cleared when the corresponding event is prioritized and serviced. If the CERH.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CERH.En cannot be set or cleared via software.

Return to [Summary Table](#)

**Table 4-2216. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 101Ch       |

**Figure 4-727. TPCC\_CERH Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E63 | E62 | E61 | E60 | E59 | E58 | E57 | E56 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E55 | E54 | E53 | E52 | E51 | E50 | E49 | E48 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E47 | E46 | E45 | E44 | E43 | E42 | E41 | E40 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E39 | E38 | E37 | E36 | E35 | E34 | E33 | E32 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2218. TPCC\_CERH Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E63   | R    | 0h    | Event #63   |
| 30  | E62   | R    | 0h    | Event #62   |
| 29  | E61   | R    | 0h    | Event #61   |
| 28  | E60   | R    | 0h    | Event #60   |
| 27  | E59   | R    | 0h    | Event #59   |
| 26  | E58   | R    | 0h    | Event #58   |
| 25  | E57   | R    | 0h    | Event #57   |
| 24  | E56   | R    | 0h    | Event #56   |
| 23  | E55   | R    | 0h    | Event #55   |
| 22  | E54   | R    | 0h    | Event #54   |
| 21  | E53   | R    | 0h    | Event #53   |
| 20  | E52   | R    | 0h    | Event #52   |
| 19  | E51   | R    | 0h    | Event #51   |

**Table 4-2218. TPCC\_CERH Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 18  | E50   | R    | 0h    | Event #50   |
| 17  | E49   | R    | 0h    | Event #49   |
| 16  | E48   | R    | 0h    | Event #48   |
| 15  | E47   | R    | 0h    | Event #47   |
| 14  | E46   | R    | 0h    | Event #46   |
| 13  | E45   | R    | 0h    | Event #45   |
| 12  | E44   | R    | 0h    | Event #44   |
| 11  | E43   | R    | 0h    | Event #43   |
| 10  | E42   | R    | 0h    | Event #42   |
| 9   | E41   | R    | 0h    | Event #41   |
| 8   | E40   | R    | 0h    | Event #40   |
| 7   | E39   | R    | 0h    | Event #39   |
| 6   | E38   | R    | 0h    | Event #38   |
| 5   | E37   | R    | 0h    | Event #37   |
| 4   | E36   | R    | 0h    | Event #36   |
| 3   | E35   | R    | 0h    | Event #35   |
| 2   | E34   | R    | 0h    | Event #34   |
| 1   | E33   | R    | 0h    | Event #33   |
| 0   | E32   | R    | 0h    | Event #32   |

#### 4.4.2.51 TPCC\_EER Register

##### 1 TPCC\_EER Register (Offset = 1020h) [reset = 0h]

Event Enable Register: Enables DMA transfers for ER.En pending events. ER.En is set based on externally asserted events (via tpcc\_eventN\_pi). This register has no effect on Chained Event Register (CER) or Event Set Register (ESR). Note that if a bit is set in ER.En while EER.En is disabled no action is taken. If EER.En is enabled at a later point (and ER.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EER.En is not directly writeable. Events can be enabled via writes to EESR and can be disabled via writes to EECR register. EER.En = 0: ER.En is not enabled to trigger DMA transfers. EER.En = 1: ER.En is enabled to trigger DMA transfers.

Return to [Summary Table](#)

**Table 4-2219. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1020h       |

**Figure 4-728. TPCC\_EER Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E31 | E30 | E29 | E28 | E27 | E26 | E25 | E24 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E23 | E22 | E21 | E20 | E19 | E18 | E17 | E16 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E15 | E14 | E13 | E12 | E11 | E10 | E9  | E8  |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E7  | E6  | E5  | E4  | E3  | E2  | E1  | E0  |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2221. TPCC\_EER Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E31   | R    | 0h    | Event #31   |
| 30  | E30   | R    | 0h    | Event #30   |
| 29  | E29   | R    | 0h    | Event #29   |
| 28  | E28   | R    | 0h    | Event #28   |
| 27  | E27   | R    | 0h    | Event #27   |
| 26  | E26   | R    | 0h    | Event #26   |
| 25  | E25   | R    | 0h    | Event #25   |
| 24  | E24   | R    | 0h    | Event #24   |
| 23  | E23   | R    | 0h    | Event #23   |
| 22  | E22   | R    | 0h    | Event #22   |
| 21  | E21   | R    | 0h    | Event #21   |
| 20  | E20   | R    | 0h    | Event #20   |
| 19  | E19   | R    | 0h    | Event #19   |

**Table 4-2221. TPCC\_EER Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 18  | E18   | R    | 0h    | Event #18   |
| 17  | E17   | R    | 0h    | Event #17   |
| 16  | E16   | R    | 0h    | Event #16   |
| 15  | E15   | R    | 0h    | Event #15   |
| 14  | E14   | R    | 0h    | Event #14   |
| 13  | E13   | R    | 0h    | Event #13   |
| 12  | E12   | R    | 0h    | Event #12   |
| 11  | E11   | R    | 0h    | Event #11   |
| 10  | E10   | R    | 0h    | Event #10   |
| 9   | E9    | R    | 0h    | Event #9    |
| 8   | E8    | R    | 0h    | Event #8    |
| 7   | E7    | R    | 0h    | Event #7    |
| 6   | E6    | R    | 0h    | Event #6    |
| 5   | E5    | R    | 0h    | Event #5    |
| 4   | E4    | R    | 0h    | Event #4    |
| 3   | E3    | R    | 0h    | Event #3    |
| 2   | E2    | R    | 0h    | Event #2    |
| 1   | E1    | R    | 0h    | Event #1    |
| 0   | E0    | R    | 0h    | Event #0    |

#### 4.4.2.52 TPCC\_EERH Register

##### 1 TPCC\_EERH Register (Offset = 1024h) [reset = 0h]

Event Enable Register (High Part): Enables DMA transfers for ERH.En pending events. ERH.En is set based on externally asserted events (via tpcc\_eventN\_pi). This register has no effect on Chained Event Register (CERH) or Event Set Register (ESRH). Note that if a bit is set in ERH.En while EERH.En is disabled no action is taken. If EERH.En is enabled at a later point (and ERH.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EERH.En is not directly writeable. Events can be enabled via writes to EESRH and can be disabled via writes to EECRH register. EERH.En = 0: ER.En is not enabled to trigger DMA transfers. EERH.En = 1: ER.En is enabled to trigger DMA transfers.

Return to [Summary Table](#)

**Table 4-2222. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1024h       |

**Figure 4-729. TPCC\_EERH Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E63 | E62 | E61 | E60 | E59 | E58 | E57 | E56 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E55 | E54 | E53 | E52 | E51 | E50 | E49 | E48 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E47 | E46 | E45 | E44 | E43 | E42 | E41 | E40 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E39 | E38 | E37 | E36 | E35 | E34 | E33 | E32 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2224. TPCC\_EERH Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E63   | R    | 0h    | Event #63   |
| 30  | E62   | R    | 0h    | Event #62   |
| 29  | E61   | R    | 0h    | Event #61   |
| 28  | E60   | R    | 0h    | Event #60   |
| 27  | E59   | R    | 0h    | Event #59   |
| 26  | E58   | R    | 0h    | Event #58   |
| 25  | E57   | R    | 0h    | Event #57   |
| 24  | E56   | R    | 0h    | Event #56   |
| 23  | E55   | R    | 0h    | Event #55   |
| 22  | E54   | R    | 0h    | Event #54   |
| 21  | E53   | R    | 0h    | Event #53   |
| 20  | E52   | R    | 0h    | Event #52   |
| 19  | E51   | R    | 0h    | Event #51   |

**Table 4-2224. TPCC\_EERH Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 18  | E50   | R    | 0h    | Event #50   |
| 17  | E49   | R    | 0h    | Event #49   |
| 16  | E48   | R    | 0h    | Event #48   |
| 15  | E47   | R    | 0h    | Event #47   |
| 14  | E46   | R    | 0h    | Event #46   |
| 13  | E45   | R    | 0h    | Event #45   |
| 12  | E44   | R    | 0h    | Event #44   |
| 11  | E43   | R    | 0h    | Event #43   |
| 10  | E42   | R    | 0h    | Event #42   |
| 9   | E41   | R    | 0h    | Event #41   |
| 8   | E40   | R    | 0h    | Event #40   |
| 7   | E39   | R    | 0h    | Event #39   |
| 6   | E38   | R    | 0h    | Event #38   |
| 5   | E37   | R    | 0h    | Event #37   |
| 4   | E36   | R    | 0h    | Event #36   |
| 3   | E35   | R    | 0h    | Event #35   |
| 2   | E34   | R    | 0h    | Event #34   |
| 1   | E33   | R    | 0h    | Event #33   |
| 0   | E32   | R    | 0h    | Event #32   |

#### 4.4.2.53 TPCC\_EECR Register

##### 1 TPCC\_EECR Register (Offset = 1028h) [reset = 0h]

Event Enable Clear Register: CPU write of '1' to the EECR.En bit causes the EER.En bit to be cleared. CPU write of '0' has no effect..

Return to [Summary Table](#)

**Table 4-2225. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1028h       |

**Figure 4-730. TPCC\_EECR Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E31 | E30 | E29 | E28 | E27 | E26 | E25 | E24 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E23 | E22 | E21 | E20 | E19 | E18 | E17 | E16 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E15 | E14 | E13 | E12 | E11 | E10 | E9  | E8  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E7  | E6  | E5  | E4  | E3  | E2  | E1  | E0  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2227. TPCC\_EECR Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E31   | W    | 0h    | Event #31   |
| 30  | E30   | W    | 0h    | Event #30   |
| 29  | E29   | W    | 0h    | Event #29   |
| 28  | E28   | W    | 0h    | Event #28   |
| 27  | E27   | W    | 0h    | Event #27   |
| 26  | E26   | W    | 0h    | Event #26   |
| 25  | E25   | W    | 0h    | Event #25   |
| 24  | E24   | W    | 0h    | Event #24   |
| 23  | E23   | W    | 0h    | Event #23   |
| 22  | E22   | W    | 0h    | Event #22   |
| 21  | E21   | W    | 0h    | Event #21   |
| 20  | E20   | W    | 0h    | Event #20   |
| 19  | E19   | W    | 0h    | Event #19   |
| 18  | E18   | W    | 0h    | Event #18   |
| 17  | E17   | W    | 0h    | Event #17   |
| 16  | E16   | W    | 0h    | Event #16   |
| 15  | E15   | W    | 0h    | Event #15   |



**Table 4-2227. TPCC\_EECR Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 14  | E14   | W    | 0h    | Event #14   |
| 13  | E13   | W    | 0h    | Event #13   |
| 12  | E12   | W    | 0h    | Event #12   |
| 11  | E11   | W    | 0h    | Event #11   |
| 10  | E10   | W    | 0h    | Event #10   |
| 9   | E9    | W    | 0h    | Event #9    |
| 8   | E8    | W    | 0h    | Event #8    |
| 7   | E7    | W    | 0h    | Event #7    |
| 6   | E6    | W    | 0h    | Event #6    |
| 5   | E5    | W    | 0h    | Event #5    |
| 4   | E4    | W    | 0h    | Event #4    |
| 3   | E3    | W    | 0h    | Event #3    |
| 2   | E2    | W    | 0h    | Event #2    |
| 1   | E1    | W    | 0h    | Event #1    |
| 0   | E0    | W    | 0h    | Event #0    |

#### 4.4.2.54 TPCC\_EECRH Register

##### 1 TPCC\_EECRH Register (Offset = 102Ch) [reset = 0h]

Event Enable Clear Register (High Part): CPU write of '1' to the EECRH.En bit causes the EERH.En bit to be cleared. CPU write of '0' has no effect..

Return to [Summary Table](#)

**Table 4-2228. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 102Ch       |

**Figure 4-731. TPCC\_EECRH Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E63 | E62 | E61 | E60 | E59 | E58 | E57 | E56 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E55 | E54 | E53 | E52 | E51 | E50 | E49 | E48 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E47 | E46 | E45 | E44 | E43 | E42 | E41 | E40 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E39 | E38 | E37 | E36 | E35 | E34 | E33 | E32 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2230. TPCC\_EECRH Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E63   | W    | 0h    | Event #63   |
| 30  | E62   | W    | 0h    | Event #62   |
| 29  | E61   | W    | 0h    | Event #61   |
| 28  | E60   | W    | 0h    | Event #60   |
| 27  | E59   | W    | 0h    | Event #59   |
| 26  | E58   | W    | 0h    | Event #58   |
| 25  | E57   | W    | 0h    | Event #57   |
| 24  | E56   | W    | 0h    | Event #56   |
| 23  | E55   | W    | 0h    | Event #55   |
| 22  | E54   | W    | 0h    | Event #54   |
| 21  | E53   | W    | 0h    | Event #53   |
| 20  | E52   | W    | 0h    | Event #52   |
| 19  | E51   | W    | 0h    | Event #51   |
| 18  | E50   | W    | 0h    | Event #50   |
| 17  | E49   | W    | 0h    | Event #49   |
| 16  | E48   | W    | 0h    | Event #48   |
| 15  | E47   | W    | 0h    | Event #47   |

**Table 4-2230. TPCC\_EECRH Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 14  | E46   | W    | 0h    | Event #46   |
| 13  | E45   | W    | 0h    | Event #45   |
| 12  | E44   | W    | 0h    | Event #44   |
| 11  | E43   | W    | 0h    | Event #43   |
| 10  | E42   | W    | 0h    | Event #42   |
| 9   | E41   | W    | 0h    | Event #41   |
| 8   | E40   | W    | 0h    | Event #40   |
| 7   | E39   | W    | 0h    | Event #39   |
| 6   | E38   | W    | 0h    | Event #38   |
| 5   | E37   | W    | 0h    | Event #37   |
| 4   | E36   | W    | 0h    | Event #36   |
| 3   | E35   | W    | 0h    | Event #35   |
| 2   | E34   | W    | 0h    | Event #34   |
| 1   | E33   | W    | 0h    | Event #33   |
| 0   | E32   | W    | 0h    | Event #32   |

#### 4.4.2.55 TPCC\_EESR Register

##### 1 TPCC\_EESR Register (Offset = 1030h) [reset = 0h]

Event Enable Set Register: CPU write of '1' to the EESR.En bit causes the EER.En bit to be set. CPU write of '0' has no effect..

Return to [Summary Table](#)

**Table 4-2231. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1030h       |

**Figure 4-732. TPCC\_EESR Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E31 | E30 | E29 | E28 | E27 | E26 | E25 | E24 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E23 | E22 | E21 | E20 | E19 | E18 | E17 | E16 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E15 | E14 | E13 | E12 | E11 | E10 | E9  | E8  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E7  | E6  | E5  | E4  | E3  | E2  | E1  | E0  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2233. TPCC\_EESR Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E31   | W    | 0h    | Event #31   |
| 30  | E30   | W    | 0h    | Event #30   |
| 29  | E29   | W    | 0h    | Event #29   |
| 28  | E28   | W    | 0h    | Event #28   |
| 27  | E27   | W    | 0h    | Event #27   |
| 26  | E26   | W    | 0h    | Event #26   |
| 25  | E25   | W    | 0h    | Event #25   |
| 24  | E24   | W    | 0h    | Event #24   |
| 23  | E23   | W    | 0h    | Event #23   |
| 22  | E22   | W    | 0h    | Event #22   |
| 21  | E21   | W    | 0h    | Event #21   |
| 20  | E20   | W    | 0h    | Event #20   |
| 19  | E19   | W    | 0h    | Event #19   |
| 18  | E18   | W    | 0h    | Event #18   |
| 17  | E17   | W    | 0h    | Event #17   |
| 16  | E16   | W    | 0h    | Event #16   |
| 15  | E15   | W    | 0h    | Event #15   |

**Table 4-2233. TPCC\_EESR Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 14  | E14   | W    | 0h    | Event #14   |
| 13  | E13   | W    | 0h    | Event #13   |
| 12  | E12   | W    | 0h    | Event #12   |
| 11  | E11   | W    | 0h    | Event #11   |
| 10  | E10   | W    | 0h    | Event #10   |
| 9   | E9    | W    | 0h    | Event #9    |
| 8   | E8    | W    | 0h    | Event #8    |
| 7   | E7    | W    | 0h    | Event #7    |
| 6   | E6    | W    | 0h    | Event #6    |
| 5   | E5    | W    | 0h    | Event #5    |
| 4   | E4    | W    | 0h    | Event #4    |
| 3   | E3    | W    | 0h    | Event #3    |
| 2   | E2    | W    | 0h    | Event #2    |
| 1   | E1    | W    | 0h    | Event #1    |
| 0   | E0    | W    | 0h    | Event #0    |

#### 4.4.2.56 TPCC\_EESRH Register

##### 1 TPCC\_EESRH Register (Offset = 1034h) [reset = 0h]

Event Enable Set Register (High Part): CPU write of '1' to the EESRH.En bit causes the EERH.En bit to be set. CPU write of '0' has no effect..

Return to [Summary Table](#)

**Table 4-2234. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1034h       |

**Figure 4-733. TPCC\_EESRH Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E63 | E62 | E61 | E60 | E59 | E58 | E57 | E56 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E55 | E54 | E53 | E52 | E51 | E50 | E49 | E48 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E47 | E46 | E45 | E44 | E43 | E42 | E41 | E40 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E39 | E38 | E37 | E36 | E35 | E34 | E33 | E32 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2236. TPCC\_EESRH Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E63   | W    | 0h    | Event #63   |
| 30  | E62   | W    | 0h    | Event #62   |
| 29  | E61   | W    | 0h    | Event #61   |
| 28  | E60   | W    | 0h    | Event #60   |
| 27  | E59   | W    | 0h    | Event #59   |
| 26  | E58   | W    | 0h    | Event #58   |
| 25  | E57   | W    | 0h    | Event #57   |
| 24  | E56   | W    | 0h    | Event #56   |
| 23  | E55   | W    | 0h    | Event #55   |
| 22  | E54   | W    | 0h    | Event #54   |
| 21  | E53   | W    | 0h    | Event #53   |
| 20  | E52   | W    | 0h    | Event #52   |
| 19  | E51   | W    | 0h    | Event #51   |
| 18  | E50   | W    | 0h    | Event #50   |
| 17  | E49   | W    | 0h    | Event #49   |
| 16  | E48   | W    | 0h    | Event #48   |
| 15  | E47   | W    | 0h    | Event #47   |

**Table 4-2236. TPCC\_EESRH Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 14  | E46   | W    | 0h    | Event #46   |
| 13  | E45   | W    | 0h    | Event #45   |
| 12  | E44   | W    | 0h    | Event #44   |
| 11  | E43   | W    | 0h    | Event #43   |
| 10  | E42   | W    | 0h    | Event #42   |
| 9   | E41   | W    | 0h    | Event #41   |
| 8   | E40   | W    | 0h    | Event #40   |
| 7   | E39   | W    | 0h    | Event #39   |
| 6   | E38   | W    | 0h    | Event #38   |
| 5   | E37   | W    | 0h    | Event #37   |
| 4   | E36   | W    | 0h    | Event #36   |
| 3   | E35   | W    | 0h    | Event #35   |
| 2   | E34   | W    | 0h    | Event #34   |
| 1   | E33   | W    | 0h    | Event #33   |
| 0   | E32   | W    | 0h    | Event #32   |

#### 4.4.2.57 TPCC\_SER Register

##### 1 TPCC\_SER Register (Offset = 1038h) [reset = 0h]

Secondary Event Register: The secondary event register is used along with the Event Register (ER) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Return to [Summary Table](#)

**Table 4-2237. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1038h       |

**Figure 4-734. TPCC\_SER Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E31 | E30 | E29 | E28 | E27 | E26 | E25 | E24 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E23 | E22 | E21 | E20 | E19 | E18 | E17 | E16 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E15 | E14 | E13 | E12 | E11 | E10 | E9  | E8  |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E7  | E6  | E5  | E4  | E3  | E2  | E1  | E0  |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2239. TPCC\_SER Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E31   | R    | 0h    | Event #31   |
| 30  | E30   | R    | 0h    | Event #30   |
| 29  | E29   | R    | 0h    | Event #29   |
| 28  | E28   | R    | 0h    | Event #28   |
| 27  | E27   | R    | 0h    | Event #27   |
| 26  | E26   | R    | 0h    | Event #26   |
| 25  | E25   | R    | 0h    | Event #25   |
| 24  | E24   | R    | 0h    | Event #24   |
| 23  | E23   | R    | 0h    | Event #23   |
| 22  | E22   | R    | 0h    | Event #22   |
| 21  | E21   | R    | 0h    | Event #21   |
| 20  | E20   | R    | 0h    | Event #20   |
| 19  | E19   | R    | 0h    | Event #19   |
| 18  | E18   | R    | 0h    | Event #18   |
| 17  | E17   | R    | 0h    | Event #17   |
| 16  | E16   | R    | 0h    | Event #16   |



**Table 4-2239. TPCC\_SER Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 15  | E15   | R    | 0h    | Event #15   |
| 14  | E14   | R    | 0h    | Event #14   |
| 13  | E13   | R    | 0h    | Event #13   |
| 12  | E12   | R    | 0h    | Event #12   |
| 11  | E11   | R    | 0h    | Event #11   |
| 10  | E10   | R    | 0h    | Event #10   |
| 9   | E9    | R    | 0h    | Event #9    |
| 8   | E8    | R    | 0h    | Event #8    |
| 7   | E7    | R    | 0h    | Event #7    |
| 6   | E6    | R    | 0h    | Event #6    |
| 5   | E5    | R    | 0h    | Event #5    |
| 4   | E4    | R    | 0h    | Event #4    |
| 3   | E3    | R    | 0h    | Event #3    |
| 2   | E2    | R    | 0h    | Event #2    |
| 1   | E1    | R    | 0h    | Event #1    |
| 0   | E0    | R    | 0h    | Event #0    |

#### 4.4.2.58 TPCC\_SERH Register

##### 1 TPCC\_SERH Register (Offset = 103Ch) [reset = 0h]

Secondary Event Register (High Part): The secondary event register is used along with the Event Register (ERH) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Return to [Summary Table](#)

**Table 4-2240. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 103Ch       |

**Figure 4-735. TPCC\_SERH Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E63 | E62 | E61 | E60 | E59 | E58 | E57 | E56 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E55 | E54 | E53 | E52 | E51 | E50 | E49 | E48 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E47 | E46 | E45 | E44 | E43 | E42 | E41 | E40 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E39 | E38 | E37 | E36 | E35 | E34 | E33 | E32 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2242. TPCC\_SERH Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E63   | R    | 0h    | Event #63   |
| 30  | E62   | R    | 0h    | Event #62   |
| 29  | E61   | R    | 0h    | Event #61   |
| 28  | E60   | R    | 0h    | Event #60   |
| 27  | E59   | R    | 0h    | Event #59   |
| 26  | E58   | R    | 0h    | Event #58   |
| 25  | E57   | R    | 0h    | Event #57   |
| 24  | E56   | R    | 0h    | Event #56   |
| 23  | E55   | R    | 0h    | Event #55   |
| 22  | E54   | R    | 0h    | Event #54   |
| 21  | E53   | R    | 0h    | Event #53   |
| 20  | E52   | R    | 0h    | Event #52   |
| 19  | E51   | R    | 0h    | Event #51   |
| 18  | E50   | R    | 0h    | Event #50   |
| 17  | E49   | R    | 0h    | Event #49   |
| 16  | E48   | R    | 0h    | Event #48   |

**Table 4-2242. TPCC\_SERH Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 15  | E47   | R    | 0h    | Event #47   |
| 14  | E46   | R    | 0h    | Event #46   |
| 13  | E45   | R    | 0h    | Event #45   |
| 12  | E44   | R    | 0h    | Event #44   |
| 11  | E43   | R    | 0h    | Event #43   |
| 10  | E42   | R    | 0h    | Event #42   |
| 9   | E41   | R    | 0h    | Event #41   |
| 8   | E40   | R    | 0h    | Event #40   |
| 7   | E39   | R    | 0h    | Event #39   |
| 6   | E38   | R    | 0h    | Event #38   |
| 5   | E37   | R    | 0h    | Event #37   |
| 4   | E36   | R    | 0h    | Event #36   |
| 3   | E35   | R    | 0h    | Event #35   |
| 2   | E34   | R    | 0h    | Event #34   |
| 1   | E33   | R    | 0h    | Event #33   |
| 0   | E32   | R    | 0h    | Event #32   |

#### 4.4.2.59 TPCC\_SECR Register

##### 1 TPCC\_SECR Register (Offset = 1040h) [reset = 0h]

Secondary Event Clear Register: The secondary event clear register is used to clear the status of the SER registers. CPU write of '1' to the SECR.En bit clears the SER register. CPU write of '0' has no effect.

Return to [Summary Table](#)

**Table 4-2243. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1040h       |

**Figure 4-736. TPCC\_SECR Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E31 | E30 | E29 | E28 | E27 | E26 | E25 | E24 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E23 | E22 | E21 | E20 | E19 | E18 | E17 | E16 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E15 | E14 | E13 | E12 | E11 | E10 | E9  | E8  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E7  | E6  | E5  | E4  | E3  | E2  | E1  | E0  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2245. TPCC\_SECR Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E31   | W    | 0h    | Event #31   |
| 30  | E30   | W    | 0h    | Event #30   |
| 29  | E29   | W    | 0h    | Event #29   |
| 28  | E28   | W    | 0h    | Event #28   |
| 27  | E27   | W    | 0h    | Event #27   |
| 26  | E26   | W    | 0h    | Event #26   |
| 25  | E25   | W    | 0h    | Event #25   |
| 24  | E24   | W    | 0h    | Event #24   |
| 23  | E23   | W    | 0h    | Event #23   |
| 22  | E22   | W    | 0h    | Event #22   |
| 21  | E21   | W    | 0h    | Event #21   |
| 20  | E20   | W    | 0h    | Event #20   |
| 19  | E19   | W    | 0h    | Event #19   |
| 18  | E18   | W    | 0h    | Event #18   |
| 17  | E17   | W    | 0h    | Event #17   |
| 16  | E16   | W    | 0h    | Event #16   |
| 15  | E15   | W    | 0h    | Event #15   |

**Table 4-2245. TPCC\_SECR Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 14  | E14   | W    | 0h    | Event #14   |
| 13  | E13   | W    | 0h    | Event #13   |
| 12  | E12   | W    | 0h    | Event #12   |
| 11  | E11   | W    | 0h    | Event #11   |
| 10  | E10   | W    | 0h    | Event #10   |
| 9   | E9    | W    | 0h    | Event #9    |
| 8   | E8    | W    | 0h    | Event #8    |
| 7   | E7    | W    | 0h    | Event #7    |
| 6   | E6    | W    | 0h    | Event #6    |
| 5   | E5    | W    | 0h    | Event #5    |
| 4   | E4    | W    | 0h    | Event #4    |
| 3   | E3    | W    | 0h    | Event #3    |
| 2   | E2    | W    | 0h    | Event #2    |
| 1   | E1    | W    | 0h    | Event #1    |
| 0   | E0    | W    | 0h    | Event #0    |

#### 4.4.2.60 TPCC\_SECRH Register

##### 1 TPCC\_SECRH Register (Offset = 1044h) [reset = 0h]

Secondary Event Clear Register (High Part): The secondary event clear register is used to clear the status of the SERH registers. CPU write of '1' to the SECRH.En bit clears the SERH register. CPU write of '0' has no effect.

Return to [Summary Table](#)

**Table 4-2246. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1044h       |

**Figure 4-737. TPCC\_SECRH Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E63 | E62 | E61 | E60 | E59 | E58 | E57 | E56 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E55 | E54 | E53 | E52 | E51 | E50 | E49 | E48 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E47 | E46 | E45 | E44 | E43 | E42 | E41 | E40 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E39 | E38 | E37 | E36 | E35 | E34 | E33 | E32 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2248. TPCC\_SECRH Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E63   | W    | 0h    | Event #63   |
| 30  | E62   | W    | 0h    | Event #62   |
| 29  | E61   | W    | 0h    | Event #61   |
| 28  | E60   | W    | 0h    | Event #60   |
| 27  | E59   | W    | 0h    | Event #59   |
| 26  | E58   | W    | 0h    | Event #58   |
| 25  | E57   | W    | 0h    | Event #57   |
| 24  | E56   | W    | 0h    | Event #56   |
| 23  | E55   | W    | 0h    | Event #55   |
| 22  | E54   | W    | 0h    | Event #54   |
| 21  | E53   | W    | 0h    | Event #53   |
| 20  | E52   | W    | 0h    | Event #52   |
| 19  | E51   | W    | 0h    | Event #51   |
| 18  | E50   | W    | 0h    | Event #50   |
| 17  | E49   | W    | 0h    | Event #49   |
| 16  | E48   | W    | 0h    | Event #48   |
| 15  | E47   | W    | 0h    | Event #47   |

**Table 4-2248. TPCC\_SECRH Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 14  | E46   | W    | 0h    | Event #46   |
| 13  | E45   | W    | 0h    | Event #45   |
| 12  | E44   | W    | 0h    | Event #44   |
| 11  | E43   | W    | 0h    | Event #43   |
| 10  | E42   | W    | 0h    | Event #42   |
| 9   | E41   | W    | 0h    | Event #41   |
| 8   | E40   | W    | 0h    | Event #40   |
| 7   | E39   | W    | 0h    | Event #39   |
| 6   | E38   | W    | 0h    | Event #38   |
| 5   | E37   | W    | 0h    | Event #37   |
| 4   | E36   | W    | 0h    | Event #36   |
| 3   | E35   | W    | 0h    | Event #35   |
| 2   | E34   | W    | 0h    | Event #34   |
| 1   | E33   | W    | 0h    | Event #33   |
| 0   | E32   | W    | 0h    | Event #32   |

#### 4.4.2.61 TPCC\_IER Register

##### 1 TPCC\_IER Register (Offset = 1050h) [reset = 0h]

Int Enable Register: IER.In is not directly writeable. Interrupts can be enabled via writes to IESR and can be disabled via writes to IECR register. IER.In = 0: IPR.In is NOT enabled for interrupts. IER.In = 1: IPR.In IS enabled for interrupts.

Return to [Summary Table](#)

**Table 4-2249. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1050h       |

**Figure 4-738. TPCC\_IER Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| I31 | I30 | I29 | I28 | I27 | I26 | I25 | I24 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| I23 | I22 | I21 | I20 | I19 | I18 | I17 | I16 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| I15 | I14 | I13 | I12 | I11 | I10 | I9  | I8  |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| I7  | I6  | I5  | I4  | I3  | I2  | I1  | I0  |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2251. TPCC\_IER Register Field Descriptions**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 31  | I31   | R    | 0h    | Interrupt associated with TCC #31 |
| 30  | I30   | R    | 0h    | Interrupt associated with TCC #30 |
| 29  | I29   | R    | 0h    | Interrupt associated with TCC #29 |
| 28  | I28   | R    | 0h    | Interrupt associated with TCC #28 |
| 27  | I27   | R    | 0h    | Interrupt associated with TCC #27 |
| 26  | I26   | R    | 0h    | Interrupt associated with TCC #26 |
| 25  | I25   | R    | 0h    | Interrupt associated with TCC #25 |
| 24  | I24   | R    | 0h    | Interrupt associated with TCC #24 |
| 23  | I23   | R    | 0h    | Interrupt associated with TCC #23 |
| 22  | I22   | R    | 0h    | Interrupt associated with TCC #22 |
| 21  | I21   | R    | 0h    | Interrupt associated with TCC #21 |
| 20  | I20   | R    | 0h    | Interrupt associated with TCC #20 |
| 19  | I19   | R    | 0h    | Interrupt associated with TCC #19 |
| 18  | I18   | R    | 0h    | Interrupt associated with TCC #18 |
| 17  | I17   | R    | 0h    | Interrupt associated with TCC #17 |
| 16  | I16   | R    | 0h    | Interrupt associated with TCC #16 |



**Table 4-2251. TPCC\_IER Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 15  | I15   | R    | 0h    | Interrupt associated with TCC #15 |
| 14  | I14   | R    | 0h    | Interrupt associated with TCC #14 |
| 13  | I13   | R    | 0h    | Interrupt associated with TCC #13 |
| 12  | I12   | R    | 0h    | Interrupt associated with TCC #12 |
| 11  | I11   | R    | 0h    | Interrupt associated with TCC #11 |
| 10  | I10   | R    | 0h    | Interrupt associated with TCC #10 |
| 9   | I9    | R    | 0h    | Interrupt associated with TCC #9  |
| 8   | I8    | R    | 0h    | Interrupt associated with TCC #8  |
| 7   | I7    | R    | 0h    | Interrupt associated with TCC #7  |
| 6   | I6    | R    | 0h    | Interrupt associated with TCC #6  |
| 5   | I5    | R    | 0h    | Interrupt associated with TCC #5  |
| 4   | I4    | R    | 0h    | Interrupt associated with TCC #4  |
| 3   | I3    | R    | 0h    | Interrupt associated with TCC #3  |
| 2   | I2    | R    | 0h    | Interrupt associated with TCC #2  |
| 1   | I1    | R    | 0h    | Interrupt associated with TCC #1  |
| 0   | I0    | R    | 0h    | Interrupt associated with TCC #0  |

#### 4.4.2.62 TPCC\_IERH Register

##### 1 TPCC\_IERH Register (Offset = 1054h) [reset = 0h]

Int Enable Register (High Part): IERH.In is not directly writeable. Interrupts can be enabled via writes to IESRH and can be disabled via writes to IECRH register. IERH.In = 0: IPRH.In is NOT enabled for interrupts. IERH.In = 1: IPRH.In IS enabled for interrupts.

Return to [Summary Table](#)

**Table 4-2252. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1054h       |

**Figure 4-739. TPCC\_IERH Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| I63 | I62 | I61 | I60 | I59 | I58 | I57 | I56 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| I55 | I54 | I53 | I52 | I51 | I50 | I49 | I48 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| I47 | I46 | I45 | I44 | I43 | I42 | I41 | I40 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| I39 | I38 | I37 | I36 | I35 | I34 | I33 | I32 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2254. TPCC\_IERH Register Field Descriptions**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 31  | I63   | R    | 0h    | Interrupt associated with TCC #63 |
| 30  | I62   | R    | 0h    | Interrupt associated with TCC #62 |
| 29  | I61   | R    | 0h    | Interrupt associated with TCC #61 |
| 28  | I60   | R    | 0h    | Interrupt associated with TCC #60 |
| 27  | I59   | R    | 0h    | Interrupt associated with TCC #59 |
| 26  | I58   | R    | 0h    | Interrupt associated with TCC #58 |
| 25  | I57   | R    | 0h    | Interrupt associated with TCC #57 |
| 24  | I56   | R    | 0h    | Interrupt associated with TCC #56 |
| 23  | I55   | R    | 0h    | Interrupt associated with TCC #55 |
| 22  | I54   | R    | 0h    | Interrupt associated with TCC #54 |
| 21  | I53   | R    | 0h    | Interrupt associated with TCC #53 |
| 20  | I52   | R    | 0h    | Interrupt associated with TCC #52 |
| 19  | I51   | R    | 0h    | Interrupt associated with TCC #51 |
| 18  | I50   | R    | 0h    | Interrupt associated with TCC #50 |
| 17  | I49   | R    | 0h    | Interrupt associated with TCC #49 |
| 16  | I48   | R    | 0h    | Interrupt associated with TCC #48 |

**Table 4-2254. TPCC\_IERH Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 15  | I47   | R    | 0h    | Interrupt associated with TCC #47 |
| 14  | I46   | R    | 0h    | Interrupt associated with TCC #46 |
| 13  | I45   | R    | 0h    | Interrupt associated with TCC #45 |
| 12  | I44   | R    | 0h    | Interrupt associated with TCC #44 |
| 11  | I43   | R    | 0h    | Interrupt associated with TCC #43 |
| 10  | I42   | R    | 0h    | Interrupt associated with TCC #42 |
| 9   | I41   | R    | 0h    | Interrupt associated with TCC #41 |
| 8   | I40   | R    | 0h    | Interrupt associated with TCC #40 |
| 7   | I39   | R    | 0h    | Interrupt associated with TCC #39 |
| 6   | I38   | R    | 0h    | Interrupt associated with TCC #38 |
| 5   | I37   | R    | 0h    | Interrupt associated with TCC #37 |
| 4   | I36   | R    | 0h    | Interrupt associated with TCC #36 |
| 3   | I35   | R    | 0h    | Interrupt associated with TCC #35 |
| 2   | I34   | R    | 0h    | Interrupt associated with TCC #34 |
| 1   | I33   | R    | 0h    | Interrupt associated with TCC #33 |
| 0   | I32   | R    | 0h    | Interrupt associated with TCC #32 |

#### 4.4.2.63 TPCC\_IECR Register

##### 1 TPCC\_IECR Register (Offset = 1058h) [reset = 0h]

Int Enable Clear Register: CPU write of '1' to the IECR.In bit causes the IER.In bit to be cleared. CPU write of '0' has no effect..

Return to [Summary Table](#)

**Table 4-2255. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1058h       |

**Figure 4-740. TPCC\_IECR Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| I31 | I30 | I29 | I28 | I27 | I26 | I25 | I24 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| I23 | I22 | I21 | I20 | I19 | I18 | I17 | I16 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| I15 | I14 | I13 | I12 | I11 | I10 | I9  | I8  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| I7  | I6  | I5  | I4  | I3  | I2  | I1  | I0  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2257. TPCC\_IECR Register Field Descriptions**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 31  | I31   | W    | 0h    | Interrupt associated with TCC #31 |
| 30  | I30   | W    | 0h    | Interrupt associated with TCC #30 |
| 29  | I29   | W    | 0h    | Interrupt associated with TCC #29 |
| 28  | I28   | W    | 0h    | Interrupt associated with TCC #28 |
| 27  | I27   | W    | 0h    | Interrupt associated with TCC #27 |
| 26  | I26   | W    | 0h    | Interrupt associated with TCC #26 |
| 25  | I25   | W    | 0h    | Interrupt associated with TCC #25 |
| 24  | I24   | W    | 0h    | Interrupt associated with TCC #24 |
| 23  | I23   | W    | 0h    | Interrupt associated with TCC #23 |
| 22  | I22   | W    | 0h    | Interrupt associated with TCC #22 |
| 21  | I21   | W    | 0h    | Interrupt associated with TCC #21 |
| 20  | I20   | W    | 0h    | Interrupt associated with TCC #20 |
| 19  | I19   | W    | 0h    | Interrupt associated with TCC #19 |
| 18  | I18   | W    | 0h    | Interrupt associated with TCC #18 |
| 17  | I17   | W    | 0h    | Interrupt associated with TCC #17 |
| 16  | I16   | W    | 0h    | Interrupt associated with TCC #16 |
| 15  | I15   | W    | 0h    | Interrupt associated with TCC #15 |

**Table 4-2257. TPCC\_IECR Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 14  | I14   | W    | 0h    | Interrupt associated with TCC #14 |
| 13  | I13   | W    | 0h    | Interrupt associated with TCC #13 |
| 12  | I12   | W    | 0h    | Interrupt associated with TCC #12 |
| 11  | I11   | W    | 0h    | Interrupt associated with TCC #11 |
| 10  | I10   | W    | 0h    | Interrupt associated with TCC #10 |
| 9   | I9    | W    | 0h    | Interrupt associated with TCC #9  |
| 8   | I8    | W    | 0h    | Interrupt associated with TCC #8  |
| 7   | I7    | W    | 0h    | Interrupt associated with TCC #7  |
| 6   | I6    | W    | 0h    | Interrupt associated with TCC #6  |
| 5   | I5    | W    | 0h    | Interrupt associated with TCC #5  |
| 4   | I4    | W    | 0h    | Interrupt associated with TCC #4  |
| 3   | I3    | W    | 0h    | Interrupt associated with TCC #3  |
| 2   | I2    | W    | 0h    | Interrupt associated with TCC #2  |
| 1   | I1    | W    | 0h    | Interrupt associated with TCC #1  |
| 0   | I0    | W    | 0h    | Interrupt associated with TCC #0  |

#### 4.4.2.64 TPCC\_IECRH Register

##### 1 TPCC\_IECRH Register (Offset = 105Ch) [reset = 0h]

Int Enable Clear Register (High Part): CPU write of '1' to the IECRH.In bit causes the IERH.In bit to be cleared. CPU write of '0' has no effect..

Return to [Summary Table](#)

**Table 4-2258. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 105Ch       |

**Figure 4-741. TPCC\_IECRH Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| I63 | I62 | I61 | I60 | I59 | I58 | I57 | I56 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| I55 | I54 | I53 | I52 | I51 | I50 | I49 | I48 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| I47 | I46 | I45 | I44 | I43 | I42 | I41 | I40 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| I39 | I38 | I37 | I36 | I35 | I34 | I33 | I32 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2260. TPCC\_IECRH Register Field Descriptions**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 31  | I63   | W    | 0h    | Interrupt associated with TCC #63 |
| 30  | I62   | W    | 0h    | Interrupt associated with TCC #62 |
| 29  | I61   | W    | 0h    | Interrupt associated with TCC #61 |
| 28  | I60   | W    | 0h    | Interrupt associated with TCC #60 |
| 27  | I59   | W    | 0h    | Interrupt associated with TCC #59 |
| 26  | I58   | W    | 0h    | Interrupt associated with TCC #58 |
| 25  | I57   | W    | 0h    | Interrupt associated with TCC #57 |
| 24  | I56   | W    | 0h    | Interrupt associated with TCC #56 |
| 23  | I55   | W    | 0h    | Interrupt associated with TCC #55 |
| 22  | I54   | W    | 0h    | Interrupt associated with TCC #54 |
| 21  | I53   | W    | 0h    | Interrupt associated with TCC #53 |
| 20  | I52   | W    | 0h    | Interrupt associated with TCC #52 |
| 19  | I51   | W    | 0h    | Interrupt associated with TCC #51 |
| 18  | I50   | W    | 0h    | Interrupt associated with TCC #50 |
| 17  | I49   | W    | 0h    | Interrupt associated with TCC #49 |
| 16  | I48   | W    | 0h    | Interrupt associated with TCC #48 |
| 15  | I47   | W    | 0h    | Interrupt associated with TCC #47 |

**Table 4-2260. TPCC\_IECRH Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 14  | I46   | W    | 0h    | Interrupt associated with TCC #46 |
| 13  | I45   | W    | 0h    | Interrupt associated with TCC #45 |
| 12  | I44   | W    | 0h    | Interrupt associated with TCC #44 |
| 11  | I43   | W    | 0h    | Interrupt associated with TCC #43 |
| 10  | I42   | W    | 0h    | Interrupt associated with TCC #42 |
| 9   | I41   | W    | 0h    | Interrupt associated with TCC #41 |
| 8   | I40   | W    | 0h    | Interrupt associated with TCC #40 |
| 7   | I39   | W    | 0h    | Interrupt associated with TCC #39 |
| 6   | I38   | W    | 0h    | Interrupt associated with TCC #38 |
| 5   | I37   | W    | 0h    | Interrupt associated with TCC #37 |
| 4   | I36   | W    | 0h    | Interrupt associated with TCC #36 |
| 3   | I35   | W    | 0h    | Interrupt associated with TCC #35 |
| 2   | I34   | W    | 0h    | Interrupt associated with TCC #34 |
| 1   | I33   | W    | 0h    | Interrupt associated with TCC #33 |
| 0   | I32   | W    | 0h    | Interrupt associated with TCC #32 |

#### 4.4.2.65 TPCC\_IESR Register

##### 1 TPCC\_IESR Register (Offset = 1060h) [reset = 0h]

Int Enable Set Register: CPU write of '1' to the IESR.In bit causes the IESR.In bit to be set. CPU write of '0' has no effect..

Return to [Summary Table](#)

**Table 4-2261. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1060h       |

**Figure 4-742. TPCC\_IESR Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| I31 | I30 | I29 | I28 | I27 | I26 | I25 | I24 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| I23 | I22 | I21 | I20 | I19 | I18 | I17 | I16 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| I15 | I14 | I13 | I12 | I11 | I10 | I9  | I8  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| I7  | I6  | I5  | I4  | I3  | I2  | I1  | I0  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2263. TPCC\_IESR Register Field Descriptions**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 31  | I31   | W    | 0h    | Interrupt associated with TCC #31 |
| 30  | I30   | W    | 0h    | Interrupt associated with TCC #30 |
| 29  | I29   | W    | 0h    | Interrupt associated with TCC #29 |
| 28  | I28   | W    | 0h    | Interrupt associated with TCC #28 |
| 27  | I27   | W    | 0h    | Interrupt associated with TCC #27 |
| 26  | I26   | W    | 0h    | Interrupt associated with TCC #26 |
| 25  | I25   | W    | 0h    | Interrupt associated with TCC #25 |
| 24  | I24   | W    | 0h    | Interrupt associated with TCC #24 |
| 23  | I23   | W    | 0h    | Interrupt associated with TCC #23 |
| 22  | I22   | W    | 0h    | Interrupt associated with TCC #22 |
| 21  | I21   | W    | 0h    | Interrupt associated with TCC #21 |
| 20  | I20   | W    | 0h    | Interrupt associated with TCC #20 |
| 19  | I19   | W    | 0h    | Interrupt associated with TCC #19 |
| 18  | I18   | W    | 0h    | Interrupt associated with TCC #18 |
| 17  | I17   | W    | 0h    | Interrupt associated with TCC #17 |
| 16  | I16   | W    | 0h    | Interrupt associated with TCC #16 |
| 15  | I15   | W    | 0h    | Interrupt associated with TCC #15 |



**Table 4-2263. TPCC\_IESR Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 14  | I14   | W    | 0h    | Interrupt associated with TCC #14 |
| 13  | I13   | W    | 0h    | Interrupt associated with TCC #13 |
| 12  | I12   | W    | 0h    | Interrupt associated with TCC #12 |
| 11  | I11   | W    | 0h    | Interrupt associated with TCC #11 |
| 10  | I10   | W    | 0h    | Interrupt associated with TCC #10 |
| 9   | I9    | W    | 0h    | Interrupt associated with TCC #9  |
| 8   | I8    | W    | 0h    | Interrupt associated with TCC #8  |
| 7   | I7    | W    | 0h    | Interrupt associated with TCC #7  |
| 6   | I6    | W    | 0h    | Interrupt associated with TCC #6  |
| 5   | I5    | W    | 0h    | Interrupt associated with TCC #5  |
| 4   | I4    | W    | 0h    | Interrupt associated with TCC #4  |
| 3   | I3    | W    | 0h    | Interrupt associated with TCC #3  |
| 2   | I2    | W    | 0h    | Interrupt associated with TCC #2  |
| 1   | I1    | W    | 0h    | Interrupt associated with TCC #1  |
| 0   | I0    | W    | 0h    | Interrupt associated with TCC #0  |

#### 4.4.2.66 TPCC\_IESRH Register

##### 1 TPCC\_IESRH Register (Offset = 1064h) [reset = 0h]

Int Enable Set Register (High Part): CPU write of '1' to the IESRH.In bit causes the IESRH.In bit to be set. CPU write of '0' has no effect..

Return to [Summary Table](#)

**Table 4-2264. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1064h       |

**Figure 4-743. TPCC\_IESRH Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| I63 | I62 | I61 | I60 | I59 | I58 | I57 | I56 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| I55 | I54 | I53 | I52 | I51 | I50 | I49 | I48 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| I47 | I46 | I45 | I44 | I43 | I42 | I41 | I40 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| I39 | I38 | I37 | I36 | I35 | I34 | I33 | I32 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2266. TPCC\_IESRH Register Field Descriptions**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 31  | I63   | W    | 0h    | Interrupt associated with TCC #63 |
| 30  | I62   | W    | 0h    | Interrupt associated with TCC #62 |
| 29  | I61   | W    | 0h    | Interrupt associated with TCC #61 |
| 28  | I60   | W    | 0h    | Interrupt associated with TCC #60 |
| 27  | I59   | W    | 0h    | Interrupt associated with TCC #59 |
| 26  | I58   | W    | 0h    | Interrupt associated with TCC #58 |
| 25  | I57   | W    | 0h    | Interrupt associated with TCC #57 |
| 24  | I56   | W    | 0h    | Interrupt associated with TCC #56 |
| 23  | I55   | W    | 0h    | Interrupt associated with TCC #55 |
| 22  | I54   | W    | 0h    | Interrupt associated with TCC #54 |
| 21  | I53   | W    | 0h    | Interrupt associated with TCC #53 |
| 20  | I52   | W    | 0h    | Interrupt associated with TCC #52 |
| 19  | I51   | W    | 0h    | Interrupt associated with TCC #51 |
| 18  | I50   | W    | 0h    | Interrupt associated with TCC #50 |
| 17  | I49   | W    | 0h    | Interrupt associated with TCC #49 |
| 16  | I48   | W    | 0h    | Interrupt associated with TCC #48 |
| 15  | I47   | W    | 0h    | Interrupt associated with TCC #47 |

**Table 4-2266. TPCC\_IESRH Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 14  | I46   | W    | 0h    | Interrupt associated with TCC #46 |
| 13  | I45   | W    | 0h    | Interrupt associated with TCC #45 |
| 12  | I44   | W    | 0h    | Interrupt associated with TCC #44 |
| 11  | I43   | W    | 0h    | Interrupt associated with TCC #43 |
| 10  | I42   | W    | 0h    | Interrupt associated with TCC #42 |
| 9   | I41   | W    | 0h    | Interrupt associated with TCC #41 |
| 8   | I40   | W    | 0h    | Interrupt associated with TCC #40 |
| 7   | I39   | W    | 0h    | Interrupt associated with TCC #39 |
| 6   | I38   | W    | 0h    | Interrupt associated with TCC #38 |
| 5   | I37   | W    | 0h    | Interrupt associated with TCC #37 |
| 4   | I36   | W    | 0h    | Interrupt associated with TCC #36 |
| 3   | I35   | W    | 0h    | Interrupt associated with TCC #35 |
| 2   | I34   | W    | 0h    | Interrupt associated with TCC #34 |
| 1   | I33   | W    | 0h    | Interrupt associated with TCC #33 |
| 0   | I32   | W    | 0h    | Interrupt associated with TCC #32 |

#### 4.4.2.67 TPCC\_IPR Register

##### 1 TPCC\_IPR Register (Offset = 1068h) [reset = 0h]

Interrupt Pending Register: IPR.In bit is set when a interrupt completion code with TCC of N is detected. IPR.In bit is cleared via software by writing a '1' to ICR.In bit.

Return to [Summary Table](#)

**Table 4-2267. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1068h       |

**Figure 4-744. TPCC\_IPR Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| I31 | I30 | I29 | I28 | I27 | I26 | I25 | I24 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| I23 | I22 | I21 | I20 | I19 | I18 | I17 | I16 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| I15 | I14 | I13 | I12 | I11 | I10 | I9  | I8  |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| I7  | I6  | I5  | I4  | I3  | I2  | I1  | I0  |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2269. TPCC\_IPR Register Field Descriptions**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 31  | I31   | R    | 0h    | Interrupt associated with TCC #31 |
| 30  | I30   | R    | 0h    | Interrupt associated with TCC #30 |
| 29  | I29   | R    | 0h    | Interrupt associated with TCC #29 |
| 28  | I28   | R    | 0h    | Interrupt associated with TCC #28 |
| 27  | I27   | R    | 0h    | Interrupt associated with TCC #27 |
| 26  | I26   | R    | 0h    | Interrupt associated with TCC #26 |
| 25  | I25   | R    | 0h    | Interrupt associated with TCC #25 |
| 24  | I24   | R    | 0h    | Interrupt associated with TCC #24 |
| 23  | I23   | R    | 0h    | Interrupt associated with TCC #23 |
| 22  | I22   | R    | 0h    | Interrupt associated with TCC #22 |
| 21  | I21   | R    | 0h    | Interrupt associated with TCC #21 |
| 20  | I20   | R    | 0h    | Interrupt associated with TCC #20 |
| 19  | I19   | R    | 0h    | Interrupt associated with TCC #19 |
| 18  | I18   | R    | 0h    | Interrupt associated with TCC #18 |
| 17  | I17   | R    | 0h    | Interrupt associated with TCC #17 |
| 16  | I16   | R    | 0h    | Interrupt associated with TCC #16 |
| 15  | I15   | R    | 0h    | Interrupt associated with TCC #15 |

**Table 4-2269. TPCC\_IPR Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 14  | I14   | R    | 0h    | Interrupt associated with TCC #14 |
| 13  | I13   | R    | 0h    | Interrupt associated with TCC #13 |
| 12  | I12   | R    | 0h    | Interrupt associated with TCC #12 |
| 11  | I11   | R    | 0h    | Interrupt associated with TCC #11 |
| 10  | I10   | R    | 0h    | Interrupt associated with TCC #10 |
| 9   | I9    | R    | 0h    | Interrupt associated with TCC #9  |
| 8   | I8    | R    | 0h    | Interrupt associated with TCC #8  |
| 7   | I7    | R    | 0h    | Interrupt associated with TCC #7  |
| 6   | I6    | R    | 0h    | Interrupt associated with TCC #6  |
| 5   | I5    | R    | 0h    | Interrupt associated with TCC #5  |
| 4   | I4    | R    | 0h    | Interrupt associated with TCC #4  |
| 3   | I3    | R    | 0h    | Interrupt associated with TCC #3  |
| 2   | I2    | R    | 0h    | Interrupt associated with TCC #2  |
| 1   | I1    | R    | 0h    | Interrupt associated with TCC #1  |
| 0   | I0    | R    | 0h    | Interrupt associated with TCC #0  |

#### 4.4.2.68 TPCC\_IPRH Register

##### 1 TPCC\_IPRH Register (Offset = 106Ch) [reset = 0h]

Interrupt Pending Register (High Part): IPRH.In bit is set when a interrupt completion code with TCC of N is detected. IPRH.In bit is cleared via software by writing a '1' to ICRH.In bit.

Return to [Summary Table](#)

**Table 4-2270. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 106Ch       |

**Figure 4-745. TPCC\_IPRH Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| I63 | I62 | I61 | I60 | I59 | I58 | I57 | I56 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| I55 | I54 | I53 | I52 | I51 | I50 | I49 | I48 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| I47 | I46 | I45 | I44 | I43 | I42 | I41 | I40 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| I39 | I38 | I37 | I36 | I35 | I34 | I33 | I32 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2272. TPCC\_IPRH Register Field Descriptions**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 31  | I63   | R    | 0h    | Interrupt associated with TCC #63 |
| 30  | I62   | R    | 0h    | Interrupt associated with TCC #62 |
| 29  | I61   | R    | 0h    | Interrupt associated with TCC #61 |
| 28  | I60   | R    | 0h    | Interrupt associated with TCC #60 |
| 27  | I59   | R    | 0h    | Interrupt associated with TCC #59 |
| 26  | I58   | R    | 0h    | Interrupt associated with TCC #58 |
| 25  | I57   | R    | 0h    | Interrupt associated with TCC #57 |
| 24  | I56   | R    | 0h    | Interrupt associated with TCC #56 |
| 23  | I55   | R    | 0h    | Interrupt associated with TCC #55 |
| 22  | I54   | R    | 0h    | Interrupt associated with TCC #54 |
| 21  | I53   | R    | 0h    | Interrupt associated with TCC #53 |
| 20  | I52   | R    | 0h    | Interrupt associated with TCC #52 |
| 19  | I51   | R    | 0h    | Interrupt associated with TCC #51 |
| 18  | I50   | R    | 0h    | Interrupt associated with TCC #50 |
| 17  | I49   | R    | 0h    | Interrupt associated with TCC #49 |
| 16  | I48   | R    | 0h    | Interrupt associated with TCC #48 |
| 15  | I47   | R    | 0h    | Interrupt associated with TCC #47 |

**Table 4-2272. TPCC\_IPRH Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 14  | I46   | R    | 0h    | Interrupt associated with TCC #46 |
| 13  | I45   | R    | 0h    | Interrupt associated with TCC #45 |
| 12  | I44   | R    | 0h    | Interrupt associated with TCC #44 |
| 11  | I43   | R    | 0h    | Interrupt associated with TCC #43 |
| 10  | I42   | R    | 0h    | Interrupt associated with TCC #42 |
| 9   | I41   | R    | 0h    | Interrupt associated with TCC #41 |
| 8   | I40   | R    | 0h    | Interrupt associated with TCC #40 |
| 7   | I39   | R    | 0h    | Interrupt associated with TCC #39 |
| 6   | I38   | R    | 0h    | Interrupt associated with TCC #38 |
| 5   | I37   | R    | 0h    | Interrupt associated with TCC #37 |
| 4   | I36   | R    | 0h    | Interrupt associated with TCC #36 |
| 3   | I35   | R    | 0h    | Interrupt associated with TCC #35 |
| 2   | I34   | R    | 0h    | Interrupt associated with TCC #34 |
| 1   | I33   | R    | 0h    | Interrupt associated with TCC #33 |
| 0   | I32   | R    | 0h    | Interrupt associated with TCC #32 |

#### 4.4.2.69 TPCC\_ICR Register

##### 1 TPCC\_ICR Register (Offset = 1070h) [reset = 0h]

Interrupt Clear Register: CPU write of '1' to the ICR.In bit causes the IPR.In bit to be cleared. CPU write of '0' has no effect. All IPR.In bits must be cleared before additional interrupts will be asserted by CC.

Return to [Summary Table](#)

**Table 4-2273. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1070h       |

**Figure 4-746. TPCC\_ICR Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| I31 | I30 | I29 | I28 | I27 | I26 | I25 | I24 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| I23 | I22 | I21 | I20 | I19 | I18 | I17 | I16 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| I15 | I14 | I13 | I12 | I11 | I10 | I9  | I8  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| I7  | I6  | I5  | I4  | I3  | I2  | I1  | I0  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2275. TPCC\_ICR Register Field Descriptions**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 31  | I31   | W    | 0h    | Interrupt associated with TCC #31 |
| 30  | I30   | W    | 0h    | Interrupt associated with TCC #30 |
| 29  | I29   | W    | 0h    | Interrupt associated with TCC #29 |
| 28  | I28   | W    | 0h    | Interrupt associated with TCC #28 |
| 27  | I27   | W    | 0h    | Interrupt associated with TCC #27 |
| 26  | I26   | W    | 0h    | Interrupt associated with TCC #26 |
| 25  | I25   | W    | 0h    | Interrupt associated with TCC #25 |
| 24  | I24   | W    | 0h    | Interrupt associated with TCC #24 |
| 23  | I23   | W    | 0h    | Interrupt associated with TCC #23 |
| 22  | I22   | W    | 0h    | Interrupt associated with TCC #22 |
| 21  | I21   | W    | 0h    | Interrupt associated with TCC #21 |
| 20  | I20   | W    | 0h    | Interrupt associated with TCC #20 |
| 19  | I19   | W    | 0h    | Interrupt associated with TCC #19 |
| 18  | I18   | W    | 0h    | Interrupt associated with TCC #18 |
| 17  | I17   | W    | 0h    | Interrupt associated with TCC #17 |
| 16  | I16   | W    | 0h    | Interrupt associated with TCC #16 |
| 15  | I15   | W    | 0h    | Interrupt associated with TCC #15 |



**Table 4-2275. TPCC\_ICR Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 14  | I14   | W    | 0h    | Interrupt associated with TCC #14 |
| 13  | I13   | W    | 0h    | Interrupt associated with TCC #13 |
| 12  | I12   | W    | 0h    | Interrupt associated with TCC #12 |
| 11  | I11   | W    | 0h    | Interrupt associated with TCC #11 |
| 10  | I10   | W    | 0h    | Interrupt associated with TCC #10 |
| 9   | I9    | W    | 0h    | Interrupt associated with TCC #9  |
| 8   | I8    | W    | 0h    | Interrupt associated with TCC #8  |
| 7   | I7    | W    | 0h    | Interrupt associated with TCC #7  |
| 6   | I6    | W    | 0h    | Interrupt associated with TCC #6  |
| 5   | I5    | W    | 0h    | Interrupt associated with TCC #5  |
| 4   | I4    | W    | 0h    | Interrupt associated with TCC #4  |
| 3   | I3    | W    | 0h    | Interrupt associated with TCC #3  |
| 2   | I2    | W    | 0h    | Interrupt associated with TCC #2  |
| 1   | I1    | W    | 0h    | Interrupt associated with TCC #1  |
| 0   | I0    | W    | 0h    | Interrupt associated with TCC #0  |

#### 4.4.2.70 TPCC\_ICRH Register

##### 1 TPCC\_ICRH Register (Offset = 1074h) [reset = 0h]

Interrupt Clear Register (High Part): CPU write of '1' to the ICRH.In bit causes the IPRH.In bit to be cleared. CPU write of '0' has no effect. All IPRH.In bits must be cleared before additional interrupts will be asserted by CC.

Return to [Summary Table](#)

**Table 4-2276. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1074h       |

**Figure 4-747. TPCC\_ICRH Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| I63 | I62 | I61 | I60 | I59 | I58 | I57 | I56 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| I55 | I54 | I53 | I52 | I51 | I50 | I49 | I48 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| I47 | I46 | I45 | I44 | I43 | I42 | I41 | I40 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| I39 | I38 | I37 | I36 | I35 | I34 | I33 | I32 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2278. TPCC\_ICRH Register Field Descriptions**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 31  | I63   | W    | 0h    | Interrupt associated with TCC #63 |
| 30  | I62   | W    | 0h    | Interrupt associated with TCC #62 |
| 29  | I61   | W    | 0h    | Interrupt associated with TCC #61 |
| 28  | I60   | W    | 0h    | Interrupt associated with TCC #60 |
| 27  | I59   | W    | 0h    | Interrupt associated with TCC #59 |
| 26  | I58   | W    | 0h    | Interrupt associated with TCC #58 |
| 25  | I57   | W    | 0h    | Interrupt associated with TCC #57 |
| 24  | I56   | W    | 0h    | Interrupt associated with TCC #56 |
| 23  | I55   | W    | 0h    | Interrupt associated with TCC #55 |
| 22  | I54   | W    | 0h    | Interrupt associated with TCC #54 |
| 21  | I53   | W    | 0h    | Interrupt associated with TCC #53 |
| 20  | I52   | W    | 0h    | Interrupt associated with TCC #52 |
| 19  | I51   | W    | 0h    | Interrupt associated with TCC #51 |
| 18  | I50   | W    | 0h    | Interrupt associated with TCC #50 |
| 17  | I49   | W    | 0h    | Interrupt associated with TCC #49 |
| 16  | I48   | W    | 0h    | Interrupt associated with TCC #48 |
| 15  | I47   | W    | 0h    | Interrupt associated with TCC #47 |

**Table 4-2278. TPCC\_ICRH Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 14  | I46   | W    | 0h    | Interrupt associated with TCC #46 |
| 13  | I45   | W    | 0h    | Interrupt associated with TCC #45 |
| 12  | I44   | W    | 0h    | Interrupt associated with TCC #44 |
| 11  | I43   | W    | 0h    | Interrupt associated with TCC #43 |
| 10  | I42   | W    | 0h    | Interrupt associated with TCC #42 |
| 9   | I41   | W    | 0h    | Interrupt associated with TCC #41 |
| 8   | I40   | W    | 0h    | Interrupt associated with TCC #40 |
| 7   | I39   | W    | 0h    | Interrupt associated with TCC #39 |
| 6   | I38   | W    | 0h    | Interrupt associated with TCC #38 |
| 5   | I37   | W    | 0h    | Interrupt associated with TCC #37 |
| 4   | I36   | W    | 0h    | Interrupt associated with TCC #36 |
| 3   | I35   | W    | 0h    | Interrupt associated with TCC #35 |
| 2   | I34   | W    | 0h    | Interrupt associated with TCC #34 |
| 1   | I33   | W    | 0h    | Interrupt associated with TCC #33 |
| 0   | I32   | W    | 0h    | Interrupt associated with TCC #32 |

#### 4.4.2.71 TPCC\_IEVAL Register

##### 1 TPCC\_IEVAL Register (Offset = 1078h) [reset = 0h]

Interrupt Eval Register

Return to [Summary Table](#)

**Table 4-2279. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1078h       |

**Figure 4-748. TPCC\_IEVAL Name Register**

|       |    |    |    |    |    |     |      |
|-------|----|----|----|----|----|-----|------|
| 31    | 30 | 29 | 28 | 27 | 26 | 25  | 24   |
| RES69 |    |    |    |    |    |     |      |
| R     |    |    |    |    |    |     |      |
| 0h    |    |    |    |    |    |     |      |
| 23    | 22 | 21 | 20 | 19 | 18 | 17  | 16   |
| RES69 |    |    |    |    |    |     |      |
| R     |    |    |    |    |    |     |      |
| 0h    |    |    |    |    |    |     |      |
| 15    | 14 | 13 | 12 | 11 | 10 | 9   | 8    |
| RES69 |    |    |    |    |    |     |      |
| R     |    |    |    |    |    |     |      |
| 0h    |    |    |    |    |    |     |      |
| 7     | 6  | 5  | 4  | 3  | 2  | 1   | 0    |
| RES69 |    |    |    |    |    | SET | EVAL |
| R     |    |    |    |    |    | W   | W    |
| 0h    |    |    |    |    |    | 0h  | 0h   |

**Table 4-2281. TPCC\_IEVAL Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                       |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RES69 | R    | 0h    | RESERVE FIELD                                                                                                                                                                                     |
| 1    | SET   | W    | 0h    | Interrupt Set: CPU write of '1' to the SETn bit causes the tpcc_intN output signal to be pulsed egardless of state of interrupts enable [IERn] and status [IPRn]. CPU write of '0' has no effect. |
| 0    | EVAL  | W    | 0h    | Interrupt Evaluate: CPU write of '1' to the EVALn bit causes the tpcc_intN output signal to be pulsed if any enabled interrupts [IERn] are still pending [IPRn]. CPU write of '0' has no effect.. |

#### 4.4.2.72 TPCC\_QER Register

##### 1 TPCC\_QER Register (Offset = 1080h) [reset = 0h]

QDMA Event Register: If QER.En bit is set then the corresponding QDMA channel is prioritized vs. other qdma events for submission to the TC. QER.En bit is set when a vbus write byte matches the address defined in the QCHMAPn register. QER.En bit is cleared when the corresponding event is prioritized and serviced. QER.En is also cleared when user writes a '1' to the QSECR.En bit. If the QER.En bit is already set and a new QDMA event is detected due to user write to QDMA trigger location and QEER register is set then the corresponding bit in the QDMA Event Missed Register is set.

Return to [Summary Table](#)

**Table 4-2282. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1080h       |

**Figure 4-749. TPCC\_QER Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RES70 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RES70 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RES70 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| E7    | E6 | E5 | E4 | E3 | E2 | E1 | E0 |
| R     | R  | R  | R  | R  | R  | R  | R  |
| 0h    | 0h | 0h | 0h | 0h | 0h | 0h | 0h |

**Table 4-2284. TPCC\_QER Register Field Descriptions**

| Bit  | Field | Type | Reset | Description   |
|------|-------|------|-------|---------------|
| 31:8 | RES70 | R    | 0h    | RESERVE FIELD |
| 7    | E7    | R    | 0h    | Event #7      |
| 6    | E6    | R    | 0h    | Event #6      |
| 5    | E5    | R    | 0h    | Event #5      |
| 4    | E4    | R    | 0h    | Event #4      |
| 3    | E3    | R    | 0h    | Event #3      |
| 2    | E2    | R    | 0h    | Event #2      |
| 1    | E1    | R    | 0h    | Event #1      |
| 0    | E0    | R    | 0h    | Event #0      |

#### 4.4.2.73 TPCC\_QEER Register

##### 1 TPCC\_QEER Register (Offset = 1084h) [reset = 0h]

QDMA Event Enable Register: Enabled/disabled QDMA address comparator for QDMA Channel N. QEER.En is not directly writeable. QDMA channels can be enabled via writes to QEESR and can be disabled via writes to QEECR register. QEER.En = 1 The corresponding QDMA channel comparator is enabled and Events will be recognized and latched in QER.En. QEER.En = 0 The corresponding QDMA channel comparator is disabled. Events will not be recognized/latched in QER.En.

Return to [Summary Table](#)

**Table 4-2285. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1084h       |

**Figure 4-750. TPCC\_QEER Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RES71 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RES71 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RES71 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| E7    | E6 | E5 | E4 | E3 | E2 | E1 | E0 |
| R     | R  | R  | R  | R  | R  | R  | R  |
| 0h    | 0h | 0h | 0h | 0h | 0h | 0h | 0h |

**Table 4-2287. TPCC\_QEER Register Field Descriptions**

| Bit  | Field | Type | Reset | Description   |
|------|-------|------|-------|---------------|
| 31:8 | RES71 | R    | 0h    | RESERVE FIELD |
| 7    | E7    | R    | 0h    | Event #7      |
| 6    | E6    | R    | 0h    | Event #6      |
| 5    | E5    | R    | 0h    | Event #5      |
| 4    | E4    | R    | 0h    | Event #4      |
| 3    | E3    | R    | 0h    | Event #3      |
| 2    | E2    | R    | 0h    | Event #2      |
| 1    | E1    | R    | 0h    | Event #1      |
| 0    | E0    | R    | 0h    | Event #0      |

#### 4.4.2.74 TPCC\_QEECR Register

##### 1 TPCC\_QEECR Register (Offset = 1088h) [reset = 0h]

QDMA Event Enable Clear Register: CPU write of '1' to the QEECR.En bit causes the QEER.En bit to be cleared. CPU write of '0' has no effect..

Return to [Summary Table](#)

**Table 4-2288. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1088h       |

**Figure 4-751. TPCC\_QEECR Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RES72 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RES72 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RES72 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| E7    | E6 | E5 | E4 | E3 | E2 | E1 | E0 |
| W     | W  | W  | W  | W  | W  | W  | W  |
| 0h    | 0h | 0h | 0h | 0h | 0h | 0h | 0h |

**Table 4-2290. TPCC\_QEECR Register Field Descriptions**

| Bit  | Field | Type | Reset | Description   |
|------|-------|------|-------|---------------|
| 31:8 | RES72 | R    | 0h    | RESERVE FIELD |
| 7    | E7    | W    | 0h    | Event #7      |
| 6    | E6    | W    | 0h    | Event #6      |
| 5    | E5    | W    | 0h    | Event #5      |
| 4    | E4    | W    | 0h    | Event #4      |
| 3    | E3    | W    | 0h    | Event #3      |
| 2    | E2    | W    | 0h    | Event #2      |
| 1    | E1    | W    | 0h    | Event #1      |
| 0    | E0    | W    | 0h    | Event #0      |

#### 4.4.2.75 TPCC\_QEESR Register

##### 1 TPCC\_QEESR Register (Offset = 108Ch) [reset = 0h]

QDMA Event Enable Set Register: CPU write of '1' to the QEESR.En bit causes the QEESR.En bit to be set. CPU write of '0' has no effect..

Return to [Summary Table](#)

**Table 4-2291. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 108Ch       |

**Figure 4-752. TPCC\_QEESR Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RES73 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RES73 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RES73 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| E7    | E6 | E5 | E4 | E3 | E2 | E1 | E0 |
| W     | W  | W  | W  | W  | W  | W  | W  |
| 0h    | 0h | 0h | 0h | 0h | 0h | 0h | 0h |

**Table 4-2293. TPCC\_QEESR Register Field Descriptions**

| Bit  | Field | Type | Reset | Description   |
|------|-------|------|-------|---------------|
| 31:8 | RES73 | R    | 0h    | RESERVE FIELD |
| 7    | E7    | W    | 0h    | Event #7      |
| 6    | E6    | W    | 0h    | Event #6      |
| 5    | E5    | W    | 0h    | Event #5      |
| 4    | E4    | W    | 0h    | Event #4      |
| 3    | E3    | W    | 0h    | Event #3      |
| 2    | E2    | W    | 0h    | Event #2      |
| 1    | E1    | W    | 0h    | Event #1      |
| 0    | E0    | W    | 0h    | Event #0      |



#### 4.4.2.76 TPCC\_QSER Register

##### 1 TPCC\_QSER Register (Offset = 1090h) [reset = 0h]

QDMA Secondary Event Register: The QDMA secondary event register is used along with the QDMA Event Register (QER) to provide information on the state of a QDMA Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Return to [Summary Table](#)

**Table 4-2294. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1090h       |

**Figure 4-753. TPCC\_QSER Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RES74 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RES74 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RES74 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| E7    | E6 | E5 | E4 | E3 | E2 | E1 | E0 |
| R     | R  | R  | R  | R  | R  | R  | R  |
| 0h    | 0h | 0h | 0h | 0h | 0h | 0h | 0h |

**Table 4-2296. TPCC\_QSER Register Field Descriptions**

| Bit  | Field | Type | Reset | Description   |
|------|-------|------|-------|---------------|
| 31:8 | RES74 | R    | 0h    | RESERVE FIELD |
| 7    | E7    | R    | 0h    | Event #7      |
| 6    | E6    | R    | 0h    | Event #6      |
| 5    | E5    | R    | 0h    | Event #5      |
| 4    | E4    | R    | 0h    | Event #4      |
| 3    | E3    | R    | 0h    | Event #3      |
| 2    | E2    | R    | 0h    | Event #2      |
| 1    | E1    | R    | 0h    | Event #1      |
| 0    | E0    | R    | 0h    | Event #0      |

#### 4.4.2.77 TPCC\_QSECR Register

##### 1 TPCC\_QSECR Register (Offset = 1094h) [reset = 0h]

QDMA Secondary Event Clear Register: The secondary event clear register is used to clear the status of the QSER and QER register (note that this is slightly different than the SER operation which does not clear the ER.En register). CPU write of '1' to the QSECR.En bit clears the QSER.En and QER.En register fields. CPU write of '0' has no effect..

Return to [Summary Table](#)

**Table 4-2297. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 1094h       |

**Figure 4-754. TPCC\_QSECR Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RES75 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RES75 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RES75 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| E7    | E6 | E5 | E4 | E3 | E2 | E1 | E0 |
| W     | W  | W  | W  | W  | W  | W  | W  |
| 0h    | 0h | 0h | 0h | 0h | 0h | 0h | 0h |

**Table 4-2299. TPCC\_QSECR Register Field Descriptions**

| Bit  | Field | Type | Reset | Description   |
|------|-------|------|-------|---------------|
| 31:8 | RES75 | R    | 0h    | RESERVE FIELD |
| 7    | E7    | W    | 0h    | Event #7      |
| 6    | E6    | W    | 0h    | Event #6      |
| 5    | E5    | W    | 0h    | Event #5      |
| 4    | E4    | W    | 0h    | Event #4      |
| 3    | E3    | W    | 0h    | Event #3      |
| 2    | E2    | W    | 0h    | Event #2      |
| 1    | E1    | W    | 0h    | Event #1      |
| 0    | E0    | W    | 0h    | Event #0      |

#### 4.4.2.78 TPCC\_ER\_RN Register

##### 1 TPCC\_ER\_RN Register (Offset = 2000h) [reset = 0h]

Event Register: If ER.En bit is set and the EER.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ER.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EER.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ER.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EER register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECR pseudo-register.

Return to [Summary Table](#)

**Table 4-2300. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2000h       |

**Figure 4-755. TPCC\_ER\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E31 | E30 | E29 | E28 | E27 | E26 | E25 | E24 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E23 | E22 | E21 | E20 | E19 | E18 | E17 | E16 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E15 | E14 | E13 | E12 | E11 | E10 | E9  | E8  |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E7  | E6  | E5  | E4  | E3  | E2  | E1  | E0  |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2302. TPCC\_ER\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E31   | R    | 0h    | Event #31   |
| 30  | E30   | R    | 0h    | Event #30   |
| 29  | E29   | R    | 0h    | Event #29   |
| 28  | E28   | R    | 0h    | Event #28   |
| 27  | E27   | R    | 0h    | Event #27   |
| 26  | E26   | R    | 0h    | Event #26   |
| 25  | E25   | R    | 0h    | Event #25   |
| 24  | E24   | R    | 0h    | Event #24   |
| 23  | E23   | R    | 0h    | Event #23   |
| 22  | E22   | R    | 0h    | Event #22   |
| 21  | E21   | R    | 0h    | Event #21   |
| 20  | E20   | R    | 0h    | Event #20   |
| 19  | E19   | R    | 0h    | Event #19   |

**Table 4-2302. TPCC\_ER\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 18  | E18   | R    | 0h    | Event #18   |
| 17  | E17   | R    | 0h    | Event #17   |
| 16  | E16   | R    | 0h    | Event #16   |
| 15  | E15   | R    | 0h    | Event #15   |
| 14  | E14   | R    | 0h    | Event #14   |
| 13  | E13   | R    | 0h    | Event #13   |
| 12  | E12   | R    | 0h    | Event #12   |
| 11  | E11   | R    | 0h    | Event #11   |
| 10  | E10   | R    | 0h    | Event #10   |
| 9   | E9    | R    | 0h    | Event #9    |
| 8   | E8    | R    | 0h    | Event #8    |
| 7   | E7    | R    | 0h    | Event #7    |
| 6   | E6    | R    | 0h    | Event #6    |
| 5   | E5    | R    | 0h    | Event #5    |
| 4   | E4    | R    | 0h    | Event #4    |
| 3   | E3    | R    | 0h    | Event #3    |
| 2   | E2    | R    | 0h    | Event #2    |
| 1   | E1    | R    | 0h    | Event #1    |
| 0   | E0    | R    | 0h    | Event #0    |

#### 4.4.2.79 TPCC\_ERH\_RN Register

##### 1 TPCC\_ERH\_RN Register (Offset = 2004h) [reset = 0h]

Event Register (High Part): If ERH.En bit is set and the EERH.En bit is also set then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. ERH.En bit is set when the input event #n transitions from inactive (low) to active (high) regardless of the state of EERH.En bit. ER.En bit is cleared when the corresponding event is prioritized and serviced. If the ERH.En bit is already set and a new inactive to active transition is detected on the input event #n input AND the corresponding bit in the EERH register is set then the corresponding bit in the Event Missed Register is set. Event N can be cleared via sw by writing a '1' to the ECRH pseudo-register.

Return to [Summary Table](#)

**Table 4-2303. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2004h       |

**Figure 4-756. TPCC\_ERH\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E63 | E62 | E61 | E60 | E59 | E58 | E57 | E56 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E55 | E54 | E53 | E52 | E51 | E50 | E49 | E48 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E47 | E46 | E45 | E44 | E43 | E42 | E41 | E40 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E39 | E38 | E37 | E36 | E35 | E34 | E33 | E32 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2305. TPCC\_ERH\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E63   | R    | 0h    | Event #63   |
| 30  | E62   | R    | 0h    | Event #62   |
| 29  | E61   | R    | 0h    | Event #61   |
| 28  | E60   | R    | 0h    | Event #60   |
| 27  | E59   | R    | 0h    | Event #59   |
| 26  | E58   | R    | 0h    | Event #58   |
| 25  | E57   | R    | 0h    | Event #57   |
| 24  | E56   | R    | 0h    | Event #56   |
| 23  | E55   | R    | 0h    | Event #55   |
| 22  | E54   | R    | 0h    | Event #54   |
| 21  | E53   | R    | 0h    | Event #53   |
| 20  | E52   | R    | 0h    | Event #52   |
| 19  | E51   | R    | 0h    | Event #51   |

**Table 4-2305. TPCC\_ERH\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 18  | E50   | R    | 0h    | Event #50   |
| 17  | E49   | R    | 0h    | Event #49   |
| 16  | E48   | R    | 0h    | Event #48   |
| 15  | E47   | R    | 0h    | Event #47   |
| 14  | E46   | R    | 0h    | Event #46   |
| 13  | E45   | R    | 0h    | Event #45   |
| 12  | E44   | R    | 0h    | Event #44   |
| 11  | E43   | R    | 0h    | Event #43   |
| 10  | E42   | R    | 0h    | Event #42   |
| 9   | E41   | R    | 0h    | Event #41   |
| 8   | E40   | R    | 0h    | Event #40   |
| 7   | E39   | R    | 0h    | Event #39   |
| 6   | E38   | R    | 0h    | Event #38   |
| 5   | E37   | R    | 0h    | Event #37   |
| 4   | E36   | R    | 0h    | Event #36   |
| 3   | E35   | R    | 0h    | Event #35   |
| 2   | E34   | R    | 0h    | Event #34   |
| 1   | E33   | R    | 0h    | Event #33   |
| 0   | E32   | R    | 0h    | Event #32   |

#### 4.4.2.80 TPCC\_ECR\_RN Register

##### 1 TPCC\_ECR\_RN Register (Offset = 2008h) [reset = 0h]

Event Clear Register: CPU write of '1' to the ECR.En bit causes the ER.En bit to be cleared. CPU write of '0' has no effect.

Return to [Summary Table](#)

**Table 4-2306. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2008h       |

**Figure 4-757. TPCC\_ECR\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E31 | E30 | E29 | E28 | E27 | E26 | E25 | E24 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E23 | E22 | E21 | E20 | E19 | E18 | E17 | E16 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E15 | E14 | E13 | E12 | E11 | E10 | E9  | E8  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E7  | E6  | E5  | E4  | E3  | E2  | E1  | E0  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2308. TPCC\_ECR\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E31   | W    | 0h    | Event #31   |
| 30  | E30   | W    | 0h    | Event #30   |
| 29  | E29   | W    | 0h    | Event #29   |
| 28  | E28   | W    | 0h    | Event #28   |
| 27  | E27   | W    | 0h    | Event #27   |
| 26  | E26   | W    | 0h    | Event #26   |
| 25  | E25   | W    | 0h    | Event #25   |
| 24  | E24   | W    | 0h    | Event #24   |
| 23  | E23   | W    | 0h    | Event #23   |
| 22  | E22   | W    | 0h    | Event #22   |
| 21  | E21   | W    | 0h    | Event #21   |
| 20  | E20   | W    | 0h    | Event #20   |
| 19  | E19   | W    | 0h    | Event #19   |
| 18  | E18   | W    | 0h    | Event #18   |
| 17  | E17   | W    | 0h    | Event #17   |
| 16  | E16   | W    | 0h    | Event #16   |
| 15  | E15   | W    | 0h    | Event #15   |

**Table 4-2308. TPCC\_ECR\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 14  | E14   | W    | 0h    | Event #14   |
| 13  | E13   | W    | 0h    | Event #13   |
| 12  | E12   | W    | 0h    | Event #12   |
| 11  | E11   | W    | 0h    | Event #11   |
| 10  | E10   | W    | 0h    | Event #10   |
| 9   | E9    | W    | 0h    | Event #9    |
| 8   | E8    | W    | 0h    | Event #8    |
| 7   | E7    | W    | 0h    | Event #7    |
| 6   | E6    | W    | 0h    | Event #6    |
| 5   | E5    | W    | 0h    | Event #5    |
| 4   | E4    | W    | 0h    | Event #4    |
| 3   | E3    | W    | 0h    | Event #3    |
| 2   | E2    | W    | 0h    | Event #2    |
| 1   | E1    | W    | 0h    | Event #1    |
| 0   | E0    | W    | 0h    | Event #0    |



#### 4.4.2.81 TPCC\_ECRH\_RN Register

##### 1 TPCC\_ECRH\_RN Register (Offset = 200Ch) [reset = 0h]

Event Clear Register (High Part): CPU write of '1' to the ECRH.En bit causes the ERH.En bit to be cleared. CPU write of '0' has no effect.

Return to [Summary Table](#)

**Table 4-2309. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 200Ch       |

**Figure 4-758. TPCC\_ECRH\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E63 | E62 | E61 | E60 | E59 | E58 | E57 | E56 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E55 | E54 | E53 | E52 | E51 | E50 | E49 | E48 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E47 | E46 | E45 | E44 | E43 | E42 | E41 | E40 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E39 | E38 | E37 | E36 | E35 | E34 | E33 | E32 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2311. TPCC\_ECRH\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E63   | W    | 0h    | Event #63   |
| 30  | E62   | W    | 0h    | Event #62   |
| 29  | E61   | W    | 0h    | Event #61   |
| 28  | E60   | W    | 0h    | Event #60   |
| 27  | E59   | W    | 0h    | Event #59   |
| 26  | E58   | W    | 0h    | Event #58   |
| 25  | E57   | W    | 0h    | Event #57   |
| 24  | E56   | W    | 0h    | Event #56   |
| 23  | E55   | W    | 0h    | Event #55   |
| 22  | E54   | W    | 0h    | Event #54   |
| 21  | E53   | W    | 0h    | Event #53   |
| 20  | E52   | W    | 0h    | Event #52   |
| 19  | E51   | W    | 0h    | Event #51   |
| 18  | E50   | W    | 0h    | Event #50   |
| 17  | E49   | W    | 0h    | Event #49   |
| 16  | E48   | W    | 0h    | Event #48   |
| 15  | E47   | W    | 0h    | Event #47   |

**Table 4-2311. TPCC\_ECRH\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 14  | E46   | W    | 0h    | Event #46   |
| 13  | E45   | W    | 0h    | Event #45   |
| 12  | E44   | W    | 0h    | Event #44   |
| 11  | E43   | W    | 0h    | Event #43   |
| 10  | E42   | W    | 0h    | Event #42   |
| 9   | E41   | W    | 0h    | Event #41   |
| 8   | E40   | W    | 0h    | Event #40   |
| 7   | E39   | W    | 0h    | Event #39   |
| 6   | E38   | W    | 0h    | Event #38   |
| 5   | E37   | W    | 0h    | Event #37   |
| 4   | E36   | W    | 0h    | Event #36   |
| 3   | E35   | W    | 0h    | Event #35   |
| 2   | E34   | W    | 0h    | Event #34   |
| 1   | E33   | W    | 0h    | Event #33   |
| 0   | E32   | W    | 0h    | Event #32   |

#### 4.4.2.82 TPCC\_ESR\_RN Register

##### 1 TPCC\_ESR\_RN Register (Offset = 2010h) [reset = 0h]

Event Set Register: CPU write of '1' to the ESR.En bit causes the ER.En bit to be set. CPU write of '0' has no effect.

Return to [Summary Table](#)

**Table 4-2312. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2010h       |

**Figure 4-759. TPCC\_ESR\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E31 | E30 | E29 | E28 | E27 | E26 | E25 | E24 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E23 | E22 | E21 | E20 | E19 | E18 | E17 | E16 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E15 | E14 | E13 | E12 | E11 | E10 | E9  | E8  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E7  | E6  | E5  | E4  | E3  | E2  | E1  | E0  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2314. TPCC\_ESR\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E31   | W    | 0h    | Event #31   |
| 30  | E30   | W    | 0h    | Event #30   |
| 29  | E29   | W    | 0h    | Event #29   |
| 28  | E28   | W    | 0h    | Event #28   |
| 27  | E27   | W    | 0h    | Event #27   |
| 26  | E26   | W    | 0h    | Event #26   |
| 25  | E25   | W    | 0h    | Event #25   |
| 24  | E24   | W    | 0h    | Event #24   |
| 23  | E23   | W    | 0h    | Event #23   |
| 22  | E22   | W    | 0h    | Event #22   |
| 21  | E21   | W    | 0h    | Event #21   |
| 20  | E20   | W    | 0h    | Event #20   |
| 19  | E19   | W    | 0h    | Event #19   |
| 18  | E18   | W    | 0h    | Event #18   |
| 17  | E17   | W    | 0h    | Event #17   |
| 16  | E16   | W    | 0h    | Event #16   |
| 15  | E15   | W    | 0h    | Event #15   |

**Table 4-2314. TPCC\_ESR\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 14  | E14   | W    | 0h    | Event #14   |
| 13  | E13   | W    | 0h    | Event #13   |
| 12  | E12   | W    | 0h    | Event #12   |
| 11  | E11   | W    | 0h    | Event #11   |
| 10  | E10   | W    | 0h    | Event #10   |
| 9   | E9    | W    | 0h    | Event #9    |
| 8   | E8    | W    | 0h    | Event #8    |
| 7   | E7    | W    | 0h    | Event #7    |
| 6   | E6    | W    | 0h    | Event #6    |
| 5   | E5    | W    | 0h    | Event #5    |
| 4   | E4    | W    | 0h    | Event #4    |
| 3   | E3    | W    | 0h    | Event #3    |
| 2   | E2    | W    | 0h    | Event #2    |
| 1   | E1    | W    | 0h    | Event #1    |
| 0   | E0    | W    | 0h    | Event #0    |

#### 4.4.2.83 TPCC\_ESRH\_RN Register

##### 1 TPCC\_ESRH\_RN Register (Offset = 2014h) [reset = 0h]

Event Set Register (High Part) CPU write of '1' to the ESRH.En bit causes the ERH.En bit to be set. CPU write of '0' has no effect.

Return to [Summary Table](#)

**Table 4-2315. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2014h       |

**Figure 4-760. TPCC\_ESRH\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E63 | E62 | E61 | E60 | E59 | E58 | E57 | E56 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E55 | E54 | E53 | E52 | E51 | E50 | E49 | E48 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E47 | E46 | E45 | E44 | E43 | E42 | E41 | E40 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E39 | E38 | E37 | E36 | E35 | E34 | E33 | E32 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2317. TPCC\_ESRH\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E63   | W    | 0h    | Event #63   |
| 30  | E62   | W    | 0h    | Event #62   |
| 29  | E61   | W    | 0h    | Event #61   |
| 28  | E60   | W    | 0h    | Event #60   |
| 27  | E59   | W    | 0h    | Event #59   |
| 26  | E58   | W    | 0h    | Event #58   |
| 25  | E57   | W    | 0h    | Event #57   |
| 24  | E56   | W    | 0h    | Event #56   |
| 23  | E55   | W    | 0h    | Event #55   |
| 22  | E54   | W    | 0h    | Event #54   |
| 21  | E53   | W    | 0h    | Event #53   |
| 20  | E52   | W    | 0h    | Event #52   |
| 19  | E51   | W    | 0h    | Event #51   |
| 18  | E50   | W    | 0h    | Event #50   |
| 17  | E49   | W    | 0h    | Event #49   |
| 16  | E48   | W    | 0h    | Event #48   |
| 15  | E47   | W    | 0h    | Event #47   |

**Table 4-2317. TPCC\_ESRH\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 14  | E46   | W    | 0h    | Event #46   |
| 13  | E45   | W    | 0h    | Event #45   |
| 12  | E44   | W    | 0h    | Event #44   |
| 11  | E43   | W    | 0h    | Event #43   |
| 10  | E42   | W    | 0h    | Event #42   |
| 9   | E41   | W    | 0h    | Event #41   |
| 8   | E40   | W    | 0h    | Event #40   |
| 7   | E39   | W    | 0h    | Event #39   |
| 6   | E38   | W    | 0h    | Event #38   |
| 5   | E37   | W    | 0h    | Event #37   |
| 4   | E36   | W    | 0h    | Event #36   |
| 3   | E35   | W    | 0h    | Event #35   |
| 2   | E34   | W    | 0h    | Event #34   |
| 1   | E33   | W    | 0h    | Event #33   |
| 0   | E32   | W    | 0h    | Event #32   |

#### 4.4.2.84 TPCC\_CER\_RN Register

##### 1 TPCC\_CER\_RN Register (Offset = 2018h) [reset = 0h]

Chained Event Register: If CER.En bit is set (regardless of state of EER.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CER.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CER.En bit is cleared when the corresponding event is prioritized and serviced. If the CER.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CER.En cannot be set or cleared via software.

Return to [Summary Table](#)

**Table 4-2318. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2018h       |

**Figure 4-761. TPCC\_CER\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E31 | E30 | E29 | E28 | E27 | E26 | E25 | E24 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E23 | E22 | E21 | E20 | E19 | E18 | E17 | E16 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E15 | E14 | E13 | E12 | E11 | E10 | E9  | E8  |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E7  | E6  | E5  | E4  | E3  | E2  | E1  | E0  |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2320. TPCC\_CER\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E31   | R    | 0h    | Event #31   |
| 30  | E30   | R    | 0h    | Event #30   |
| 29  | E29   | R    | 0h    | Event #29   |
| 28  | E28   | R    | 0h    | Event #28   |
| 27  | E27   | R    | 0h    | Event #27   |
| 26  | E26   | R    | 0h    | Event #26   |
| 25  | E25   | R    | 0h    | Event #25   |
| 24  | E24   | R    | 0h    | Event #24   |
| 23  | E23   | R    | 0h    | Event #23   |
| 22  | E22   | R    | 0h    | Event #22   |
| 21  | E21   | R    | 0h    | Event #21   |
| 20  | E20   | R    | 0h    | Event #20   |
| 19  | E19   | R    | 0h    | Event #19   |
| 18  | E18   | R    | 0h    | Event #18   |

**Table 4-2320. TPCC\_CER\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 17  | E17   | R    | 0h    | Event #17   |
| 16  | E16   | R    | 0h    | Event #16   |
| 15  | E15   | R    | 0h    | Event #15   |
| 14  | E14   | R    | 0h    | Event #14   |
| 13  | E13   | R    | 0h    | Event #13   |
| 12  | E12   | R    | 0h    | Event #12   |
| 11  | E11   | R    | 0h    | Event #11   |
| 10  | E10   | R    | 0h    | Event #10   |
| 9   | E9    | R    | 0h    | Event #9    |
| 8   | E8    | R    | 0h    | Event #8    |
| 7   | E7    | R    | 0h    | Event #7    |
| 6   | E6    | R    | 0h    | Event #6    |
| 5   | E5    | R    | 0h    | Event #5    |
| 4   | E4    | R    | 0h    | Event #4    |
| 3   | E3    | R    | 0h    | Event #3    |
| 2   | E2    | R    | 0h    | Event #2    |
| 1   | E1    | R    | 0h    | Event #1    |
| 0   | E0    | R    | 0h    | Event #0    |



#### 4.4.2.85 TPCC\_CERH\_RN Register

##### 1 TPCC\_CERH\_RN Register (Offset = 201Ch) [reset = 0h]

Chained Event Register (High Part): If CERH.En bit is set (regardless of state of EERH.En) then the corresponding DMA channel is prioritized vs. other pending DMA events for submission to the TC. CERH.En bit is set when a chaining completion code is returned from one of the 3PTCs via the completion interface or is generated internally via Early Completion path. CERH.En bit is cleared when the corresponding event is prioritized and serviced. If the CERH.En bit is already set and the corresponding chaining completion code is returned from the TC then the corresponding bit in the Event Missed Register is set. CERH.En cannot be set or cleared via software.

Return to [Summary Table](#)

**Table 4-2321. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 201Ch       |

**Figure 4-762. TPCC\_CERH\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E63 | E62 | E61 | E60 | E59 | E58 | E57 | E56 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E55 | E54 | E53 | E52 | E51 | E50 | E49 | E48 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E47 | E46 | E45 | E44 | E43 | E42 | E41 | E40 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E39 | E38 | E37 | E36 | E35 | E34 | E33 | E32 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2323. TPCC\_CERH\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E63   | R    | 0h    | Event #63   |
| 30  | E62   | R    | 0h    | Event #62   |
| 29  | E61   | R    | 0h    | Event #61   |
| 28  | E60   | R    | 0h    | Event #60   |
| 27  | E59   | R    | 0h    | Event #59   |
| 26  | E58   | R    | 0h    | Event #58   |
| 25  | E57   | R    | 0h    | Event #57   |
| 24  | E56   | R    | 0h    | Event #56   |
| 23  | E55   | R    | 0h    | Event #55   |
| 22  | E54   | R    | 0h    | Event #54   |
| 21  | E53   | R    | 0h    | Event #53   |
| 20  | E52   | R    | 0h    | Event #52   |
| 19  | E51   | R    | 0h    | Event #51   |

**Table 4-2323. TPCC\_CERH\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 18  | E50   | R    | 0h    | Event #50   |
| 17  | E49   | R    | 0h    | Event #49   |
| 16  | E48   | R    | 0h    | Event #48   |
| 15  | E47   | R    | 0h    | Event #47   |
| 14  | E46   | R    | 0h    | Event #46   |
| 13  | E45   | R    | 0h    | Event #45   |
| 12  | E44   | R    | 0h    | Event #44   |
| 11  | E43   | R    | 0h    | Event #43   |
| 10  | E42   | R    | 0h    | Event #42   |
| 9   | E41   | R    | 0h    | Event #41   |
| 8   | E40   | R    | 0h    | Event #40   |
| 7   | E39   | R    | 0h    | Event #39   |
| 6   | E38   | R    | 0h    | Event #38   |
| 5   | E37   | R    | 0h    | Event #37   |
| 4   | E36   | R    | 0h    | Event #36   |
| 3   | E35   | R    | 0h    | Event #35   |
| 2   | E34   | R    | 0h    | Event #34   |
| 1   | E33   | R    | 0h    | Event #33   |
| 0   | E32   | R    | 0h    | Event #32   |

#### 4.4.2.86 TPCC\_EER\_RN Register

##### 1 TPCC\_EER\_RN Register (Offset = 2020h) [reset = 0h]

Event Enable Register: Enables DMA transfers for ER.En pending events. ER.En is set based on externally asserted events (via tpcc\_eventN\_pi). This register has no effect on Chained Event Register (CER) or Event Set Register (ESR). Note that if a bit is set in ER.En while EER.En is disabled no action is taken. If EER.En is enabled at a later point (and ER.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EER.En is not directly writeable. Events can be enabled via writes to EESR and can be disabled via writes to EECR register. EER.En = 0: ER.En is not enabled to trigger DMA transfers. EER.En = 1: ER.En is enabled to trigger DMA transfers.

Return to [Summary Table](#)

**Table 4-2324. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2020h       |

**Figure 4-763. TPCC\_EER\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E31 | E30 | E29 | E28 | E27 | E26 | E25 | E24 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E23 | E22 | E21 | E20 | E19 | E18 | E17 | E16 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E15 | E14 | E13 | E12 | E11 | E10 | E9  | E8  |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E7  | E6  | E5  | E4  | E3  | E2  | E1  | E0  |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2326. TPCC\_EER\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E31   | R    | 0h    | Event #31   |
| 30  | E30   | R    | 0h    | Event #30   |
| 29  | E29   | R    | 0h    | Event #29   |
| 28  | E28   | R    | 0h    | Event #28   |
| 27  | E27   | R    | 0h    | Event #27   |
| 26  | E26   | R    | 0h    | Event #26   |
| 25  | E25   | R    | 0h    | Event #25   |
| 24  | E24   | R    | 0h    | Event #24   |
| 23  | E23   | R    | 0h    | Event #23   |
| 22  | E22   | R    | 0h    | Event #22   |
| 21  | E21   | R    | 0h    | Event #21   |
| 20  | E20   | R    | 0h    | Event #20   |
| 19  | E19   | R    | 0h    | Event #19   |

**Table 4-2326. TPCC\_EER\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 18  | E18   | R    | 0h    | Event #18   |
| 17  | E17   | R    | 0h    | Event #17   |
| 16  | E16   | R    | 0h    | Event #16   |
| 15  | E15   | R    | 0h    | Event #15   |
| 14  | E14   | R    | 0h    | Event #14   |
| 13  | E13   | R    | 0h    | Event #13   |
| 12  | E12   | R    | 0h    | Event #12   |
| 11  | E11   | R    | 0h    | Event #11   |
| 10  | E10   | R    | 0h    | Event #10   |
| 9   | E9    | R    | 0h    | Event #9    |
| 8   | E8    | R    | 0h    | Event #8    |
| 7   | E7    | R    | 0h    | Event #7    |
| 6   | E6    | R    | 0h    | Event #6    |
| 5   | E5    | R    | 0h    | Event #5    |
| 4   | E4    | R    | 0h    | Event #4    |
| 3   | E3    | R    | 0h    | Event #3    |
| 2   | E2    | R    | 0h    | Event #2    |
| 1   | E1    | R    | 0h    | Event #1    |
| 0   | E0    | R    | 0h    | Event #0    |

#### 4.4.2.87 TPCC\_EERH\_RN Register

##### 1 TPCC\_EERH\_RN Register (Offset = 2024h) [reset = 0h]

Event Enable Register (High Part): Enables DMA transfers for ERH.En pending events. ERH.En is set based on externally asserted events (via tpcc\_eventN\_pi). This register has no effect on Chained Event Register (CERH) or Event Set Register (ESRH). Note that if a bit is set in ERH.En while EERH.En is disabled no action is taken. If EERH.En is enabled at a later point (and ERH.En has not been cleared via SW) then the event will be recognized as a valid 'TR Sync' EERH.En is not directly writeable. Events can be enabled via writes to EESRH and can be disabled via writes to EECRH register. EERH.En = 0: ER.En is not enabled to trigger DMA transfers. EERH.En = 1: ER.En is enabled to trigger DMA transfers.

Return to [Summary Table](#)

**Table 4-2327. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2024h       |

**Figure 4-764. TPCC\_EERH\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E63 | E62 | E61 | E60 | E59 | E58 | E57 | E56 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E55 | E54 | E53 | E52 | E51 | E50 | E49 | E48 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E47 | E46 | E45 | E44 | E43 | E42 | E41 | E40 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E39 | E38 | E37 | E36 | E35 | E34 | E33 | E32 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2329. TPCC\_EERH\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E63   | R    | 0h    | Event #63   |
| 30  | E62   | R    | 0h    | Event #62   |
| 29  | E61   | R    | 0h    | Event #61   |
| 28  | E60   | R    | 0h    | Event #60   |
| 27  | E59   | R    | 0h    | Event #59   |
| 26  | E58   | R    | 0h    | Event #58   |
| 25  | E57   | R    | 0h    | Event #57   |
| 24  | E56   | R    | 0h    | Event #56   |
| 23  | E55   | R    | 0h    | Event #55   |
| 22  | E54   | R    | 0h    | Event #54   |
| 21  | E53   | R    | 0h    | Event #53   |
| 20  | E52   | R    | 0h    | Event #52   |
| 19  | E51   | R    | 0h    | Event #51   |

**Table 4-2329. TPCC\_EERH\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 18  | E50   | R    | 0h    | Event #50   |
| 17  | E49   | R    | 0h    | Event #49   |
| 16  | E48   | R    | 0h    | Event #48   |
| 15  | E47   | R    | 0h    | Event #47   |
| 14  | E46   | R    | 0h    | Event #46   |
| 13  | E45   | R    | 0h    | Event #45   |
| 12  | E44   | R    | 0h    | Event #44   |
| 11  | E43   | R    | 0h    | Event #43   |
| 10  | E42   | R    | 0h    | Event #42   |
| 9   | E41   | R    | 0h    | Event #41   |
| 8   | E40   | R    | 0h    | Event #40   |
| 7   | E39   | R    | 0h    | Event #39   |
| 6   | E38   | R    | 0h    | Event #38   |
| 5   | E37   | R    | 0h    | Event #37   |
| 4   | E36   | R    | 0h    | Event #36   |
| 3   | E35   | R    | 0h    | Event #35   |
| 2   | E34   | R    | 0h    | Event #34   |
| 1   | E33   | R    | 0h    | Event #33   |
| 0   | E32   | R    | 0h    | Event #32   |

#### 4.4.2.88 TPCC\_EECR\_RN Register

##### 1 TPCC\_EECR\_RN Register (Offset = 2028h) [reset = 0h]

Event Enable Clear Register: CPU write of '1' to the EECR.En bit causes the EER.En bit to be cleared. CPU write of '0' has no effect..

Return to [Summary Table](#)

**Table 4-2330. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2028h       |

**Figure 4-765. TPCC\_EECR\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E31 | E30 | E29 | E28 | E27 | E26 | E25 | E24 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E23 | E22 | E21 | E20 | E19 | E18 | E17 | E16 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E15 | E14 | E13 | E12 | E11 | E10 | E9  | E8  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E7  | E6  | E5  | E4  | E3  | E2  | E1  | E0  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2332. TPCC\_EECR\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E31   | W    | 0h    | Event #31   |
| 30  | E30   | W    | 0h    | Event #30   |
| 29  | E29   | W    | 0h    | Event #29   |
| 28  | E28   | W    | 0h    | Event #28   |
| 27  | E27   | W    | 0h    | Event #27   |
| 26  | E26   | W    | 0h    | Event #26   |
| 25  | E25   | W    | 0h    | Event #25   |
| 24  | E24   | W    | 0h    | Event #24   |
| 23  | E23   | W    | 0h    | Event #23   |
| 22  | E22   | W    | 0h    | Event #22   |
| 21  | E21   | W    | 0h    | Event #21   |
| 20  | E20   | W    | 0h    | Event #20   |
| 19  | E19   | W    | 0h    | Event #19   |
| 18  | E18   | W    | 0h    | Event #18   |
| 17  | E17   | W    | 0h    | Event #17   |
| 16  | E16   | W    | 0h    | Event #16   |
| 15  | E15   | W    | 0h    | Event #15   |

**Table 4-2332. TPCC\_EECR\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 14  | E14   | W    | 0h    | Event #14   |
| 13  | E13   | W    | 0h    | Event #13   |
| 12  | E12   | W    | 0h    | Event #12   |
| 11  | E11   | W    | 0h    | Event #11   |
| 10  | E10   | W    | 0h    | Event #10   |
| 9   | E9    | W    | 0h    | Event #9    |
| 8   | E8    | W    | 0h    | Event #8    |
| 7   | E7    | W    | 0h    | Event #7    |
| 6   | E6    | W    | 0h    | Event #6    |
| 5   | E5    | W    | 0h    | Event #5    |
| 4   | E4    | W    | 0h    | Event #4    |
| 3   | E3    | W    | 0h    | Event #3    |
| 2   | E2    | W    | 0h    | Event #2    |
| 1   | E1    | W    | 0h    | Event #1    |
| 0   | E0    | W    | 0h    | Event #0    |



#### 4.4.2.89 TPCC\_EECRH\_RN Register

##### 1 TPCC\_EECRH\_RN Register (Offset = 202Ch) [reset = 0h]

Event Enable Clear Register (High Part): CPU write of '1' to the EECRH.En bit causes the EECRH.En bit to be cleared. CPU write of '0' has no effect..

Return to [Summary Table](#)

**Table 4-2333. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 202Ch       |

**Figure 4-766. TPCC\_EECRH\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E63 | E62 | E61 | E60 | E59 | E58 | E57 | E56 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E55 | E54 | E53 | E52 | E51 | E50 | E49 | E48 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E47 | E46 | E45 | E44 | E43 | E42 | E41 | E40 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E39 | E38 | E37 | E36 | E35 | E34 | E33 | E32 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2335. TPCC\_EECRH\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E63   | W    | 0h    | Event #63   |
| 30  | E62   | W    | 0h    | Event #62   |
| 29  | E61   | W    | 0h    | Event #61   |
| 28  | E60   | W    | 0h    | Event #60   |
| 27  | E59   | W    | 0h    | Event #59   |
| 26  | E58   | W    | 0h    | Event #58   |
| 25  | E57   | W    | 0h    | Event #57   |
| 24  | E56   | W    | 0h    | Event #56   |
| 23  | E55   | W    | 0h    | Event #55   |
| 22  | E54   | W    | 0h    | Event #54   |
| 21  | E53   | W    | 0h    | Event #53   |
| 20  | E52   | W    | 0h    | Event #52   |
| 19  | E51   | W    | 0h    | Event #51   |
| 18  | E50   | W    | 0h    | Event #50   |
| 17  | E49   | W    | 0h    | Event #49   |
| 16  | E48   | W    | 0h    | Event #48   |
| 15  | E47   | W    | 0h    | Event #47   |

**Table 4-2335. TPCC\_EECRH\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 14  | E46   | W    | 0h    | Event #46   |
| 13  | E45   | W    | 0h    | Event #45   |
| 12  | E44   | W    | 0h    | Event #44   |
| 11  | E43   | W    | 0h    | Event #43   |
| 10  | E42   | W    | 0h    | Event #42   |
| 9   | E41   | W    | 0h    | Event #41   |
| 8   | E40   | W    | 0h    | Event #40   |
| 7   | E39   | W    | 0h    | Event #39   |
| 6   | E38   | W    | 0h    | Event #38   |
| 5   | E37   | W    | 0h    | Event #37   |
| 4   | E36   | W    | 0h    | Event #36   |
| 3   | E35   | W    | 0h    | Event #35   |
| 2   | E34   | W    | 0h    | Event #34   |
| 1   | E33   | W    | 0h    | Event #33   |
| 0   | E32   | W    | 0h    | Event #32   |

#### 4.4.2.90 TPCC\_EESR\_RN Register

##### 1 TPCC\_EESR\_RN Register (Offset = 2030h) [reset = 0h]

Event Enable Set Register: CPU write of '1' to the EESR.En bit causes the EER.En bit to be set. CPU write of '0' has no effect..

Return to [Summary Table](#)

**Table 4-2336. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2030h       |

**Figure 4-767. TPCC\_EESR\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E31 | E30 | E29 | E28 | E27 | E26 | E25 | E24 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E23 | E22 | E21 | E20 | E19 | E18 | E17 | E16 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E15 | E14 | E13 | E12 | E11 | E10 | E9  | E8  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E7  | E6  | E5  | E4  | E3  | E2  | E1  | E0  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2338. TPCC\_EESR\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E31   | W    | 0h    | Event #31   |
| 30  | E30   | W    | 0h    | Event #30   |
| 29  | E29   | W    | 0h    | Event #29   |
| 28  | E28   | W    | 0h    | Event #28   |
| 27  | E27   | W    | 0h    | Event #27   |
| 26  | E26   | W    | 0h    | Event #26   |
| 25  | E25   | W    | 0h    | Event #25   |
| 24  | E24   | W    | 0h    | Event #24   |
| 23  | E23   | W    | 0h    | Event #23   |
| 22  | E22   | W    | 0h    | Event #22   |
| 21  | E21   | W    | 0h    | Event #21   |
| 20  | E20   | W    | 0h    | Event #20   |
| 19  | E19   | W    | 0h    | Event #19   |
| 18  | E18   | W    | 0h    | Event #18   |
| 17  | E17   | W    | 0h    | Event #17   |
| 16  | E16   | W    | 0h    | Event #16   |
| 15  | E15   | W    | 0h    | Event #15   |

**Table 4-2338. TPCC\_EESR\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 14  | E14   | W    | 0h    | Event #14   |
| 13  | E13   | W    | 0h    | Event #13   |
| 12  | E12   | W    | 0h    | Event #12   |
| 11  | E11   | W    | 0h    | Event #11   |
| 10  | E10   | W    | 0h    | Event #10   |
| 9   | E9    | W    | 0h    | Event #9    |
| 8   | E8    | W    | 0h    | Event #8    |
| 7   | E7    | W    | 0h    | Event #7    |
| 6   | E6    | W    | 0h    | Event #6    |
| 5   | E5    | W    | 0h    | Event #5    |
| 4   | E4    | W    | 0h    | Event #4    |
| 3   | E3    | W    | 0h    | Event #3    |
| 2   | E2    | W    | 0h    | Event #2    |
| 1   | E1    | W    | 0h    | Event #1    |
| 0   | E0    | W    | 0h    | Event #0    |

#### 4.4.2.91 TPCC\_EESRH\_RN Register

##### 1 TPCC\_EESRH\_RN Register (Offset = 2034h) [reset = 0h]

Event Enable Set Register (High Part): CPU write of '1' to the EESRH.En bit causes the EERH.En bit to be set. CPU write of '0' has no effect..

Return to [Summary Table](#)

**Table 4-2339. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2034h       |

**Figure 4-768. TPCC\_EESRH\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E63 | E62 | E61 | E60 | E59 | E58 | E57 | E56 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E55 | E54 | E53 | E52 | E51 | E50 | E49 | E48 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E47 | E46 | E45 | E44 | E43 | E42 | E41 | E40 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E39 | E38 | E37 | E36 | E35 | E34 | E33 | E32 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2341. TPCC\_EESRH\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E63   | W    | 0h    | Event #63   |
| 30  | E62   | W    | 0h    | Event #62   |
| 29  | E61   | W    | 0h    | Event #61   |
| 28  | E60   | W    | 0h    | Event #60   |
| 27  | E59   | W    | 0h    | Event #59   |
| 26  | E58   | W    | 0h    | Event #58   |
| 25  | E57   | W    | 0h    | Event #57   |
| 24  | E56   | W    | 0h    | Event #56   |
| 23  | E55   | W    | 0h    | Event #55   |
| 22  | E54   | W    | 0h    | Event #54   |
| 21  | E53   | W    | 0h    | Event #53   |
| 20  | E52   | W    | 0h    | Event #52   |
| 19  | E51   | W    | 0h    | Event #51   |
| 18  | E50   | W    | 0h    | Event #50   |
| 17  | E49   | W    | 0h    | Event #49   |
| 16  | E48   | W    | 0h    | Event #48   |
| 15  | E47   | W    | 0h    | Event #47   |

**Table 4-2341. TPCC\_EESRH\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 14  | E46   | W    | 0h    | Event #46   |
| 13  | E45   | W    | 0h    | Event #45   |
| 12  | E44   | W    | 0h    | Event #44   |
| 11  | E43   | W    | 0h    | Event #43   |
| 10  | E42   | W    | 0h    | Event #42   |
| 9   | E41   | W    | 0h    | Event #41   |
| 8   | E40   | W    | 0h    | Event #40   |
| 7   | E39   | W    | 0h    | Event #39   |
| 6   | E38   | W    | 0h    | Event #38   |
| 5   | E37   | W    | 0h    | Event #37   |
| 4   | E36   | W    | 0h    | Event #36   |
| 3   | E35   | W    | 0h    | Event #35   |
| 2   | E34   | W    | 0h    | Event #34   |
| 1   | E33   | W    | 0h    | Event #33   |
| 0   | E32   | W    | 0h    | Event #32   |

#### 4.4.2.92 TPCC\_SER\_RN Register

##### 1 TPCC\_SER\_RN Register (Offset = 2038h) [reset = 0h]

Secondary Event Register: The secondary event register is used along with the Event Register (ER) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Return to [Summary Table](#)

**Table 4-2342. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2038h       |

**Figure 4-769. TPCC\_SER\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E31 | E30 | E29 | E28 | E27 | E26 | E25 | E24 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E23 | E22 | E21 | E20 | E19 | E18 | E17 | E16 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E15 | E14 | E13 | E12 | E11 | E10 | E9  | E8  |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E7  | E6  | E5  | E4  | E3  | E2  | E1  | E0  |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2344. TPCC\_SER\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E31   | R    | 0h    | Event #31   |
| 30  | E30   | R    | 0h    | Event #30   |
| 29  | E29   | R    | 0h    | Event #29   |
| 28  | E28   | R    | 0h    | Event #28   |
| 27  | E27   | R    | 0h    | Event #27   |
| 26  | E26   | R    | 0h    | Event #26   |
| 25  | E25   | R    | 0h    | Event #25   |
| 24  | E24   | R    | 0h    | Event #24   |
| 23  | E23   | R    | 0h    | Event #23   |
| 22  | E22   | R    | 0h    | Event #22   |
| 21  | E21   | R    | 0h    | Event #21   |
| 20  | E20   | R    | 0h    | Event #20   |
| 19  | E19   | R    | 0h    | Event #19   |
| 18  | E18   | R    | 0h    | Event #18   |
| 17  | E17   | R    | 0h    | Event #17   |
| 16  | E16   | R    | 0h    | Event #16   |

**Table 4-2344. TPCC\_SER\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 15  | E15   | R    | 0h    | Event #15   |
| 14  | E14   | R    | 0h    | Event #14   |
| 13  | E13   | R    | 0h    | Event #13   |
| 12  | E12   | R    | 0h    | Event #12   |
| 11  | E11   | R    | 0h    | Event #11   |
| 10  | E10   | R    | 0h    | Event #10   |
| 9   | E9    | R    | 0h    | Event #9    |
| 8   | E8    | R    | 0h    | Event #8    |
| 7   | E7    | R    | 0h    | Event #7    |
| 6   | E6    | R    | 0h    | Event #6    |
| 5   | E5    | R    | 0h    | Event #5    |
| 4   | E4    | R    | 0h    | Event #4    |
| 3   | E3    | R    | 0h    | Event #3    |
| 2   | E2    | R    | 0h    | Event #2    |
| 1   | E1    | R    | 0h    | Event #1    |
| 0   | E0    | R    | 0h    | Event #0    |



#### 4.4.2.93 TPCC\_SERH\_RN Register

##### 1 TPCC\_SERH\_RN Register (Offset = 203Ch) [reset = 0h]

Secondary Event Register (High Part): The secondary event register is used along with the Event Register (ERH) to provide information on the state of an Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Return to [Summary Table](#)

**Table 4-2345. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 203Ch       |

**Figure 4-770. TPCC\_SERH\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E63 | E62 | E61 | E60 | E59 | E58 | E57 | E56 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E55 | E54 | E53 | E52 | E51 | E50 | E49 | E48 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E47 | E46 | E45 | E44 | E43 | E42 | E41 | E40 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E39 | E38 | E37 | E36 | E35 | E34 | E33 | E32 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2347. TPCC\_SERH\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E63   | R    | 0h    | Event #63   |
| 30  | E62   | R    | 0h    | Event #62   |
| 29  | E61   | R    | 0h    | Event #61   |
| 28  | E60   | R    | 0h    | Event #60   |
| 27  | E59   | R    | 0h    | Event #59   |
| 26  | E58   | R    | 0h    | Event #58   |
| 25  | E57   | R    | 0h    | Event #57   |
| 24  | E56   | R    | 0h    | Event #56   |
| 23  | E55   | R    | 0h    | Event #55   |
| 22  | E54   | R    | 0h    | Event #54   |
| 21  | E53   | R    | 0h    | Event #53   |
| 20  | E52   | R    | 0h    | Event #52   |
| 19  | E51   | R    | 0h    | Event #51   |
| 18  | E50   | R    | 0h    | Event #50   |
| 17  | E49   | R    | 0h    | Event #49   |
| 16  | E48   | R    | 0h    | Event #48   |

**Table 4-2347. TPCC\_SERH\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 15  | E47   | R    | 0h    | Event #47   |
| 14  | E46   | R    | 0h    | Event #46   |
| 13  | E45   | R    | 0h    | Event #45   |
| 12  | E44   | R    | 0h    | Event #44   |
| 11  | E43   | R    | 0h    | Event #43   |
| 10  | E42   | R    | 0h    | Event #42   |
| 9   | E41   | R    | 0h    | Event #41   |
| 8   | E40   | R    | 0h    | Event #40   |
| 7   | E39   | R    | 0h    | Event #39   |
| 6   | E38   | R    | 0h    | Event #38   |
| 5   | E37   | R    | 0h    | Event #37   |
| 4   | E36   | R    | 0h    | Event #36   |
| 3   | E35   | R    | 0h    | Event #35   |
| 2   | E34   | R    | 0h    | Event #34   |
| 1   | E33   | R    | 0h    | Event #33   |
| 0   | E32   | R    | 0h    | Event #32   |

#### 4.4.2.94 TPCC\_SECR\_RN Register

##### 1 TPCC\_SECR\_RN Register (Offset = 2040h) [reset = 0h]

Secondary Event Clear Register: The secondary event clear register is used to clear the status of the SER registers. CPU write of '1' to the SECR.En bit clears the SER register. CPU write of '0' has no effect.

Return to [Summary Table](#)

**Table 4-2348. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2040h       |

**Figure 4-771. TPCC\_SECR\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E31 | E30 | E29 | E28 | E27 | E26 | E25 | E24 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E23 | E22 | E21 | E20 | E19 | E18 | E17 | E16 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E15 | E14 | E13 | E12 | E11 | E10 | E9  | E8  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E7  | E6  | E5  | E4  | E3  | E2  | E1  | E0  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2350. TPCC\_SECR\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E31   | W    | 0h    | Event #31   |
| 30  | E30   | W    | 0h    | Event #30   |
| 29  | E29   | W    | 0h    | Event #29   |
| 28  | E28   | W    | 0h    | Event #28   |
| 27  | E27   | W    | 0h    | Event #27   |
| 26  | E26   | W    | 0h    | Event #26   |
| 25  | E25   | W    | 0h    | Event #25   |
| 24  | E24   | W    | 0h    | Event #24   |
| 23  | E23   | W    | 0h    | Event #23   |
| 22  | E22   | W    | 0h    | Event #22   |
| 21  | E21   | W    | 0h    | Event #21   |
| 20  | E20   | W    | 0h    | Event #20   |
| 19  | E19   | W    | 0h    | Event #19   |
| 18  | E18   | W    | 0h    | Event #18   |
| 17  | E17   | W    | 0h    | Event #17   |
| 16  | E16   | W    | 0h    | Event #16   |
| 15  | E15   | W    | 0h    | Event #15   |

**Table 4-2350. TPCC\_SECR\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 14  | E14   | W    | 0h    | Event #14   |
| 13  | E13   | W    | 0h    | Event #13   |
| 12  | E12   | W    | 0h    | Event #12   |
| 11  | E11   | W    | 0h    | Event #11   |
| 10  | E10   | W    | 0h    | Event #10   |
| 9   | E9    | W    | 0h    | Event #9    |
| 8   | E8    | W    | 0h    | Event #8    |
| 7   | E7    | W    | 0h    | Event #7    |
| 6   | E6    | W    | 0h    | Event #6    |
| 5   | E5    | W    | 0h    | Event #5    |
| 4   | E4    | W    | 0h    | Event #4    |
| 3   | E3    | W    | 0h    | Event #3    |
| 2   | E2    | W    | 0h    | Event #2    |
| 1   | E1    | W    | 0h    | Event #1    |
| 0   | E0    | W    | 0h    | Event #0    |

#### 4.4.2.95 TPCC\_SECRH\_RN Register

##### 1 TPCC\_SECRH\_RN Register (Offset = 2044h) [reset = 0h]

Secondary Event Clear Register (High Part): The secondary event clear register is used to clear the status of the SERH registers. CPU write of '1' to the SECRH.En bit clears the SERH register. CPU write of '0' has no effect.

Return to [Summary Table](#)

**Table 4-2351. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2044h       |

**Figure 4-772. TPCC\_SECRH\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| E63 | E62 | E61 | E60 | E59 | E58 | E57 | E56 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| E55 | E54 | E53 | E52 | E51 | E50 | E49 | E48 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| E47 | E46 | E45 | E44 | E43 | E42 | E41 | E40 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| E39 | E38 | E37 | E36 | E35 | E34 | E33 | E32 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2353. TPCC\_SECRH\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 31  | E63   | W    | 0h    | Event #63   |
| 30  | E62   | W    | 0h    | Event #62   |
| 29  | E61   | W    | 0h    | Event #61   |
| 28  | E60   | W    | 0h    | Event #60   |
| 27  | E59   | W    | 0h    | Event #59   |
| 26  | E58   | W    | 0h    | Event #58   |
| 25  | E57   | W    | 0h    | Event #57   |
| 24  | E56   | W    | 0h    | Event #56   |
| 23  | E55   | W    | 0h    | Event #55   |
| 22  | E54   | W    | 0h    | Event #54   |
| 21  | E53   | W    | 0h    | Event #53   |
| 20  | E52   | W    | 0h    | Event #52   |
| 19  | E51   | W    | 0h    | Event #51   |
| 18  | E50   | W    | 0h    | Event #50   |
| 17  | E49   | W    | 0h    | Event #49   |
| 16  | E48   | W    | 0h    | Event #48   |
| 15  | E47   | W    | 0h    | Event #47   |

**Table 4-2353. TPCC\_SECRH\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 14  | E46   | W    | 0h    | Event #46   |
| 13  | E45   | W    | 0h    | Event #45   |
| 12  | E44   | W    | 0h    | Event #44   |
| 11  | E43   | W    | 0h    | Event #43   |
| 10  | E42   | W    | 0h    | Event #42   |
| 9   | E41   | W    | 0h    | Event #41   |
| 8   | E40   | W    | 0h    | Event #40   |
| 7   | E39   | W    | 0h    | Event #39   |
| 6   | E38   | W    | 0h    | Event #38   |
| 5   | E37   | W    | 0h    | Event #37   |
| 4   | E36   | W    | 0h    | Event #36   |
| 3   | E35   | W    | 0h    | Event #35   |
| 2   | E34   | W    | 0h    | Event #34   |
| 1   | E33   | W    | 0h    | Event #33   |
| 0   | E32   | W    | 0h    | Event #32   |

#### 4.4.2.96 TPCC\_IER\_RN Register

##### 1 TPCC\_IER\_RN Register (Offset = 2050h) [reset = 0h]

Int Enable Register: IER.In is not directly writeable. Interrupts can be enabled via writes to IESR and can be disabled via writes to IECR register. IER.In = 0: IPR.In is NOT enabled for interrupts. IER.In = 1: IPR.In IS enabled for interrupts.

Return to [Summary Table](#)

**Table 4-2354. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2050h       |

**Figure 4-773. TPCC\_IER\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| I31 | I30 | I29 | I28 | I27 | I26 | I25 | I24 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| I23 | I22 | I21 | I20 | I19 | I18 | I17 | I16 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| I15 | I14 | I13 | I12 | I11 | I10 | I9  | I8  |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| I7  | I6  | I5  | I4  | I3  | I2  | I1  | I0  |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2356. TPCC\_IER\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 31  | I31   | R    | 0h    | Interrupt associated with TCC #31 |
| 30  | I30   | R    | 0h    | Interrupt associated with TCC #30 |
| 29  | I29   | R    | 0h    | Interrupt associated with TCC #29 |
| 28  | I28   | R    | 0h    | Interrupt associated with TCC #28 |
| 27  | I27   | R    | 0h    | Interrupt associated with TCC #27 |
| 26  | I26   | R    | 0h    | Interrupt associated with TCC #26 |
| 25  | I25   | R    | 0h    | Interrupt associated with TCC #25 |
| 24  | I24   | R    | 0h    | Interrupt associated with TCC #24 |
| 23  | I23   | R    | 0h    | Interrupt associated with TCC #23 |
| 22  | I22   | R    | 0h    | Interrupt associated with TCC #22 |
| 21  | I21   | R    | 0h    | Interrupt associated with TCC #21 |
| 20  | I20   | R    | 0h    | Interrupt associated with TCC #20 |
| 19  | I19   | R    | 0h    | Interrupt associated with TCC #19 |
| 18  | I18   | R    | 0h    | Interrupt associated with TCC #18 |
| 17  | I17   | R    | 0h    | Interrupt associated with TCC #17 |
| 16  | I16   | R    | 0h    | Interrupt associated with TCC #16 |

**Table 4-2356. TPCC\_IER\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 15  | I15   | R    | 0h    | Interrupt associated with TCC #15 |
| 14  | I14   | R    | 0h    | Interrupt associated with TCC #14 |
| 13  | I13   | R    | 0h    | Interrupt associated with TCC #13 |
| 12  | I12   | R    | 0h    | Interrupt associated with TCC #12 |
| 11  | I11   | R    | 0h    | Interrupt associated with TCC #11 |
| 10  | I10   | R    | 0h    | Interrupt associated with TCC #10 |
| 9   | I9    | R    | 0h    | Interrupt associated with TCC #9  |
| 8   | I8    | R    | 0h    | Interrupt associated with TCC #8  |
| 7   | I7    | R    | 0h    | Interrupt associated with TCC #7  |
| 6   | I6    | R    | 0h    | Interrupt associated with TCC #6  |
| 5   | I5    | R    | 0h    | Interrupt associated with TCC #5  |
| 4   | I4    | R    | 0h    | Interrupt associated with TCC #4  |
| 3   | I3    | R    | 0h    | Interrupt associated with TCC #3  |
| 2   | I2    | R    | 0h    | Interrupt associated with TCC #2  |
| 1   | I1    | R    | 0h    | Interrupt associated with TCC #1  |
| 0   | I0    | R    | 0h    | Interrupt associated with TCC #0  |



#### 4.4.2.97 TPCC\_IERH\_RN Register

##### 1 TPCC\_IERH\_RN Register (Offset = 2054h) [reset = 0h]

Int Enable Register (High Part): IERH.In is not directly writeable. Interrupts can be enabled via writes to IESRH and can be disabled via writes to IECRH register. IERH.In = 0: IPRH.In is NOT enabled for interrupts. IERH.In = 1: IPRH.In IS enabled for interrupts.

Return to [Summary Table](#)

**Table 4-2357. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2054h       |

**Figure 4-774. TPCC\_IERH\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| I63 | I62 | I61 | I60 | I59 | I58 | I57 | I56 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| I55 | I54 | I53 | I52 | I51 | I50 | I49 | I48 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| I47 | I46 | I45 | I44 | I43 | I42 | I41 | I40 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| I39 | I38 | I37 | I36 | I35 | I34 | I33 | I32 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2359. TPCC\_IERH\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 31  | I63   | R    | 0h    | Interrupt associated with TCC #63 |
| 30  | I62   | R    | 0h    | Interrupt associated with TCC #62 |
| 29  | I61   | R    | 0h    | Interrupt associated with TCC #61 |
| 28  | I60   | R    | 0h    | Interrupt associated with TCC #60 |
| 27  | I59   | R    | 0h    | Interrupt associated with TCC #59 |
| 26  | I58   | R    | 0h    | Interrupt associated with TCC #58 |
| 25  | I57   | R    | 0h    | Interrupt associated with TCC #57 |
| 24  | I56   | R    | 0h    | Interrupt associated with TCC #56 |
| 23  | I55   | R    | 0h    | Interrupt associated with TCC #55 |
| 22  | I54   | R    | 0h    | Interrupt associated with TCC #54 |
| 21  | I53   | R    | 0h    | Interrupt associated with TCC #53 |
| 20  | I52   | R    | 0h    | Interrupt associated with TCC #52 |
| 19  | I51   | R    | 0h    | Interrupt associated with TCC #51 |
| 18  | I50   | R    | 0h    | Interrupt associated with TCC #50 |
| 17  | I49   | R    | 0h    | Interrupt associated with TCC #49 |
| 16  | I48   | R    | 0h    | Interrupt associated with TCC #48 |

**Table 4-2359. TPCC\_IERH\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 15  | I47   | R    | 0h    | Interrupt associated with TCC #47 |
| 14  | I46   | R    | 0h    | Interrupt associated with TCC #46 |
| 13  | I45   | R    | 0h    | Interrupt associated with TCC #45 |
| 12  | I44   | R    | 0h    | Interrupt associated with TCC #44 |
| 11  | I43   | R    | 0h    | Interrupt associated with TCC #43 |
| 10  | I42   | R    | 0h    | Interrupt associated with TCC #42 |
| 9   | I41   | R    | 0h    | Interrupt associated with TCC #41 |
| 8   | I40   | R    | 0h    | Interrupt associated with TCC #40 |
| 7   | I39   | R    | 0h    | Interrupt associated with TCC #39 |
| 6   | I38   | R    | 0h    | Interrupt associated with TCC #38 |
| 5   | I37   | R    | 0h    | Interrupt associated with TCC #37 |
| 4   | I36   | R    | 0h    | Interrupt associated with TCC #36 |
| 3   | I35   | R    | 0h    | Interrupt associated with TCC #35 |
| 2   | I34   | R    | 0h    | Interrupt associated with TCC #34 |
| 1   | I33   | R    | 0h    | Interrupt associated with TCC #33 |
| 0   | I32   | R    | 0h    | Interrupt associated with TCC #32 |

#### 4.4.2.98 TPCC\_IECR\_RN Register

##### 1 TPCC\_IECR\_RN Register (Offset = 2058h) [reset = 0h]

Int Enable Clear Register: CPU write of '1' to the IECR.In bit causes the IER.In bit to be cleared. CPU write of '0' has no effect..

Return to [Summary Table](#)

**Table 4-2360. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2058h       |

**Figure 4-775. TPCC\_IECR\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| I31 | I30 | I29 | I28 | I27 | I26 | I25 | I24 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| I23 | I22 | I21 | I20 | I19 | I18 | I17 | I16 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| I15 | I14 | I13 | I12 | I11 | I10 | I9  | I8  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| I7  | I6  | I5  | I4  | I3  | I2  | I1  | I0  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2362. TPCC\_IECR\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 31  | I31   | W    | 0h    | Interrupt associated with TCC #31 |
| 30  | I30   | W    | 0h    | Interrupt associated with TCC #30 |
| 29  | I29   | W    | 0h    | Interrupt associated with TCC #29 |
| 28  | I28   | W    | 0h    | Interrupt associated with TCC #28 |
| 27  | I27   | W    | 0h    | Interrupt associated with TCC #27 |
| 26  | I26   | W    | 0h    | Interrupt associated with TCC #26 |
| 25  | I25   | W    | 0h    | Interrupt associated with TCC #25 |
| 24  | I24   | W    | 0h    | Interrupt associated with TCC #24 |
| 23  | I23   | W    | 0h    | Interrupt associated with TCC #23 |
| 22  | I22   | W    | 0h    | Interrupt associated with TCC #22 |
| 21  | I21   | W    | 0h    | Interrupt associated with TCC #21 |
| 20  | I20   | W    | 0h    | Interrupt associated with TCC #20 |
| 19  | I19   | W    | 0h    | Interrupt associated with TCC #19 |
| 18  | I18   | W    | 0h    | Interrupt associated with TCC #18 |
| 17  | I17   | W    | 0h    | Interrupt associated with TCC #17 |
| 16  | I16   | W    | 0h    | Interrupt associated with TCC #16 |
| 15  | I15   | W    | 0h    | Interrupt associated with TCC #15 |

**Table 4-2362. TPCC\_IECR\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 14  | I14   | W    | 0h    | Interrupt associated with TCC #14 |
| 13  | I13   | W    | 0h    | Interrupt associated with TCC #13 |
| 12  | I12   | W    | 0h    | Interrupt associated with TCC #12 |
| 11  | I11   | W    | 0h    | Interrupt associated with TCC #11 |
| 10  | I10   | W    | 0h    | Interrupt associated with TCC #10 |
| 9   | I9    | W    | 0h    | Interrupt associated with TCC #9  |
| 8   | I8    | W    | 0h    | Interrupt associated with TCC #8  |
| 7   | I7    | W    | 0h    | Interrupt associated with TCC #7  |
| 6   | I6    | W    | 0h    | Interrupt associated with TCC #6  |
| 5   | I5    | W    | 0h    | Interrupt associated with TCC #5  |
| 4   | I4    | W    | 0h    | Interrupt associated with TCC #4  |
| 3   | I3    | W    | 0h    | Interrupt associated with TCC #3  |
| 2   | I2    | W    | 0h    | Interrupt associated with TCC #2  |
| 1   | I1    | W    | 0h    | Interrupt associated with TCC #1  |
| 0   | I0    | W    | 0h    | Interrupt associated with TCC #0  |

#### 4.4.2.99 TPCC\_IERH\_RN Register

##### 1 TPCC\_IERH\_RN Register (Offset = 205Ch) [reset = 0h]

Int Enable Clear Register (High Part): CPU write of '1' to the IERH.In bit causes the IERH.In bit to be cleared. CPU write of '0' has no effect..

Return to [Summary Table](#)

**Table 4-2363. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 205Ch       |

**Figure 4-776. TPCC\_IERH\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| I63 | I62 | I61 | I60 | I59 | I58 | I57 | I56 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| I55 | I54 | I53 | I52 | I51 | I50 | I49 | I48 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| I47 | I46 | I45 | I44 | I43 | I42 | I41 | I40 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| I39 | I38 | I37 | I36 | I35 | I34 | I33 | I32 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2365. TPCC\_IERH\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 31  | I63   | W    | 0h    | Interrupt associated with TCC #63 |
| 30  | I62   | W    | 0h    | Interrupt associated with TCC #62 |
| 29  | I61   | W    | 0h    | Interrupt associated with TCC #61 |
| 28  | I60   | W    | 0h    | Interrupt associated with TCC #60 |
| 27  | I59   | W    | 0h    | Interrupt associated with TCC #59 |
| 26  | I58   | W    | 0h    | Interrupt associated with TCC #58 |
| 25  | I57   | W    | 0h    | Interrupt associated with TCC #57 |
| 24  | I56   | W    | 0h    | Interrupt associated with TCC #56 |
| 23  | I55   | W    | 0h    | Interrupt associated with TCC #55 |
| 22  | I54   | W    | 0h    | Interrupt associated with TCC #54 |
| 21  | I53   | W    | 0h    | Interrupt associated with TCC #53 |
| 20  | I52   | W    | 0h    | Interrupt associated with TCC #52 |
| 19  | I51   | W    | 0h    | Interrupt associated with TCC #51 |
| 18  | I50   | W    | 0h    | Interrupt associated with TCC #50 |
| 17  | I49   | W    | 0h    | Interrupt associated with TCC #49 |
| 16  | I48   | W    | 0h    | Interrupt associated with TCC #48 |
| 15  | I47   | W    | 0h    | Interrupt associated with TCC #47 |

**Table 4-2365. TPCC\_IECRH\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 14  | I46   | W    | 0h    | Interrupt associated with TCC #46 |
| 13  | I45   | W    | 0h    | Interrupt associated with TCC #45 |
| 12  | I44   | W    | 0h    | Interrupt associated with TCC #44 |
| 11  | I43   | W    | 0h    | Interrupt associated with TCC #43 |
| 10  | I42   | W    | 0h    | Interrupt associated with TCC #42 |
| 9   | I41   | W    | 0h    | Interrupt associated with TCC #41 |
| 8   | I40   | W    | 0h    | Interrupt associated with TCC #40 |
| 7   | I39   | W    | 0h    | Interrupt associated with TCC #39 |
| 6   | I38   | W    | 0h    | Interrupt associated with TCC #38 |
| 5   | I37   | W    | 0h    | Interrupt associated with TCC #37 |
| 4   | I36   | W    | 0h    | Interrupt associated with TCC #36 |
| 3   | I35   | W    | 0h    | Interrupt associated with TCC #35 |
| 2   | I34   | W    | 0h    | Interrupt associated with TCC #34 |
| 1   | I33   | W    | 0h    | Interrupt associated with TCC #33 |
| 0   | I32   | W    | 0h    | Interrupt associated with TCC #32 |

#### 4.4.2.100 TPCC\_IESR\_RN Register

##### 1 TPCC\_IESR\_RN Register (Offset = 2060h) [reset = 0h]

Int Enable Set Register: CPU write of '1' to the IESR.In bit causes the IESR.In bit to be set. CPU write of '0' has no effect..

Return to [Summary Table](#)

**Table 4-2366. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2060h       |

**Figure 4-777. TPCC\_IESR\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| I31 | I30 | I29 | I28 | I27 | I26 | I25 | I24 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| I23 | I22 | I21 | I20 | I19 | I18 | I17 | I16 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| I15 | I14 | I13 | I12 | I11 | I10 | I9  | I8  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| I7  | I6  | I5  | I4  | I3  | I2  | I1  | I0  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2368. TPCC\_IESR\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 31  | I31   | W    | 0h    | Interrupt associated with TCC #31 |
| 30  | I30   | W    | 0h    | Interrupt associated with TCC #30 |
| 29  | I29   | W    | 0h    | Interrupt associated with TCC #29 |
| 28  | I28   | W    | 0h    | Interrupt associated with TCC #28 |
| 27  | I27   | W    | 0h    | Interrupt associated with TCC #27 |
| 26  | I26   | W    | 0h    | Interrupt associated with TCC #26 |
| 25  | I25   | W    | 0h    | Interrupt associated with TCC #25 |
| 24  | I24   | W    | 0h    | Interrupt associated with TCC #24 |
| 23  | I23   | W    | 0h    | Interrupt associated with TCC #23 |
| 22  | I22   | W    | 0h    | Interrupt associated with TCC #22 |
| 21  | I21   | W    | 0h    | Interrupt associated with TCC #21 |
| 20  | I20   | W    | 0h    | Interrupt associated with TCC #20 |
| 19  | I19   | W    | 0h    | Interrupt associated with TCC #19 |
| 18  | I18   | W    | 0h    | Interrupt associated with TCC #18 |
| 17  | I17   | W    | 0h    | Interrupt associated with TCC #17 |
| 16  | I16   | W    | 0h    | Interrupt associated with TCC #16 |
| 15  | I15   | W    | 0h    | Interrupt associated with TCC #15 |

**Table 4-2368. TPCC\_IESR\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 14  | I14   | W    | 0h    | Interrupt associated with TCC #14 |
| 13  | I13   | W    | 0h    | Interrupt associated with TCC #13 |
| 12  | I12   | W    | 0h    | Interrupt associated with TCC #12 |
| 11  | I11   | W    | 0h    | Interrupt associated with TCC #11 |
| 10  | I10   | W    | 0h    | Interrupt associated with TCC #10 |
| 9   | I9    | W    | 0h    | Interrupt associated with TCC #9  |
| 8   | I8    | W    | 0h    | Interrupt associated with TCC #8  |
| 7   | I7    | W    | 0h    | Interrupt associated with TCC #7  |
| 6   | I6    | W    | 0h    | Interrupt associated with TCC #6  |
| 5   | I5    | W    | 0h    | Interrupt associated with TCC #5  |
| 4   | I4    | W    | 0h    | Interrupt associated with TCC #4  |
| 3   | I3    | W    | 0h    | Interrupt associated with TCC #3  |
| 2   | I2    | W    | 0h    | Interrupt associated with TCC #2  |
| 1   | I1    | W    | 0h    | Interrupt associated with TCC #1  |
| 0   | I0    | W    | 0h    | Interrupt associated with TCC #0  |



#### 4.4.2.101 TPCC\_IESRH\_RN Register

##### 1 TPCC\_IESRH\_RN Register (Offset = 2064h) [reset = 0h]

Int Enable Set Register (High Part): CPU write of '1' to the IESRH.In bit causes the IESRH.In bit to be set. CPU write of '0' has no effect..

Return to [Summary Table](#)

**Table 4-2369. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2064h       |

**Figure 4-778. TPCC\_IESRH\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| I63 | I62 | I61 | I60 | I59 | I58 | I57 | I56 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| I55 | I54 | I53 | I52 | I51 | I50 | I49 | I48 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| I47 | I46 | I45 | I44 | I43 | I42 | I41 | I40 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| I39 | I38 | I37 | I36 | I35 | I34 | I33 | I32 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2371. TPCC\_IESRH\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 31  | I63   | W    | 0h    | Interrupt associated with TCC #63 |
| 30  | I62   | W    | 0h    | Interrupt associated with TCC #62 |
| 29  | I61   | W    | 0h    | Interrupt associated with TCC #61 |
| 28  | I60   | W    | 0h    | Interrupt associated with TCC #60 |
| 27  | I59   | W    | 0h    | Interrupt associated with TCC #59 |
| 26  | I58   | W    | 0h    | Interrupt associated with TCC #58 |
| 25  | I57   | W    | 0h    | Interrupt associated with TCC #57 |
| 24  | I56   | W    | 0h    | Interrupt associated with TCC #56 |
| 23  | I55   | W    | 0h    | Interrupt associated with TCC #55 |
| 22  | I54   | W    | 0h    | Interrupt associated with TCC #54 |
| 21  | I53   | W    | 0h    | Interrupt associated with TCC #53 |
| 20  | I52   | W    | 0h    | Interrupt associated with TCC #52 |
| 19  | I51   | W    | 0h    | Interrupt associated with TCC #51 |
| 18  | I50   | W    | 0h    | Interrupt associated with TCC #50 |
| 17  | I49   | W    | 0h    | Interrupt associated with TCC #49 |
| 16  | I48   | W    | 0h    | Interrupt associated with TCC #48 |
| 15  | I47   | W    | 0h    | Interrupt associated with TCC #47 |

**Table 4-2371. TPCC\_IESRH\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 14  | I46   | W    | 0h    | Interrupt associated with TCC #46 |
| 13  | I45   | W    | 0h    | Interrupt associated with TCC #45 |
| 12  | I44   | W    | 0h    | Interrupt associated with TCC #44 |
| 11  | I43   | W    | 0h    | Interrupt associated with TCC #43 |
| 10  | I42   | W    | 0h    | Interrupt associated with TCC #42 |
| 9   | I41   | W    | 0h    | Interrupt associated with TCC #41 |
| 8   | I40   | W    | 0h    | Interrupt associated with TCC #40 |
| 7   | I39   | W    | 0h    | Interrupt associated with TCC #39 |
| 6   | I38   | W    | 0h    | Interrupt associated with TCC #38 |
| 5   | I37   | W    | 0h    | Interrupt associated with TCC #37 |
| 4   | I36   | W    | 0h    | Interrupt associated with TCC #36 |
| 3   | I35   | W    | 0h    | Interrupt associated with TCC #35 |
| 2   | I34   | W    | 0h    | Interrupt associated with TCC #34 |
| 1   | I33   | W    | 0h    | Interrupt associated with TCC #33 |
| 0   | I32   | W    | 0h    | Interrupt associated with TCC #32 |

#### 4.4.2.102 TPCC\_IPR\_RN Register

##### 1 TPCC\_IPR\_RN Register (Offset = 2068h) [reset = 0h]

Interrupt Pending Register: IPR.In bit is set when a interrupt completion code with TCC of N is detected. IPR.In bit is cleared via software by writing a '1' to ICR.In bit.

Return to [Summary Table](#)

**Table 4-2372. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2068h       |

**Figure 4-779. TPCC\_IPR\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| I31 | I30 | I29 | I28 | I27 | I26 | I25 | I24 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| I23 | I22 | I21 | I20 | I19 | I18 | I17 | I16 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| I15 | I14 | I13 | I12 | I11 | I10 | I9  | I8  |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| I7  | I6  | I5  | I4  | I3  | I2  | I1  | I0  |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2374. TPCC\_IPR\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 31  | I31   | R    | 0h    | Interrupt associated with TCC #31 |
| 30  | I30   | R    | 0h    | Interrupt associated with TCC #30 |
| 29  | I29   | R    | 0h    | Interrupt associated with TCC #29 |
| 28  | I28   | R    | 0h    | Interrupt associated with TCC #28 |
| 27  | I27   | R    | 0h    | Interrupt associated with TCC #27 |
| 26  | I26   | R    | 0h    | Interrupt associated with TCC #26 |
| 25  | I25   | R    | 0h    | Interrupt associated with TCC #25 |
| 24  | I24   | R    | 0h    | Interrupt associated with TCC #24 |
| 23  | I23   | R    | 0h    | Interrupt associated with TCC #23 |
| 22  | I22   | R    | 0h    | Interrupt associated with TCC #22 |
| 21  | I21   | R    | 0h    | Interrupt associated with TCC #21 |
| 20  | I20   | R    | 0h    | Interrupt associated with TCC #20 |
| 19  | I19   | R    | 0h    | Interrupt associated with TCC #19 |
| 18  | I18   | R    | 0h    | Interrupt associated with TCC #18 |
| 17  | I17   | R    | 0h    | Interrupt associated with TCC #17 |
| 16  | I16   | R    | 0h    | Interrupt associated with TCC #16 |
| 15  | I15   | R    | 0h    | Interrupt associated with TCC #15 |

**Table 4-2374. TPCC\_IPR\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 14  | I14   | R    | 0h    | Interrupt associated with TCC #14 |
| 13  | I13   | R    | 0h    | Interrupt associated with TCC #13 |
| 12  | I12   | R    | 0h    | Interrupt associated with TCC #12 |
| 11  | I11   | R    | 0h    | Interrupt associated with TCC #11 |
| 10  | I10   | R    | 0h    | Interrupt associated with TCC #10 |
| 9   | I9    | R    | 0h    | Interrupt associated with TCC #9  |
| 8   | I8    | R    | 0h    | Interrupt associated with TCC #8  |
| 7   | I7    | R    | 0h    | Interrupt associated with TCC #7  |
| 6   | I6    | R    | 0h    | Interrupt associated with TCC #6  |
| 5   | I5    | R    | 0h    | Interrupt associated with TCC #5  |
| 4   | I4    | R    | 0h    | Interrupt associated with TCC #4  |
| 3   | I3    | R    | 0h    | Interrupt associated with TCC #3  |
| 2   | I2    | R    | 0h    | Interrupt associated with TCC #2  |
| 1   | I1    | R    | 0h    | Interrupt associated with TCC #1  |
| 0   | I0    | R    | 0h    | Interrupt associated with TCC #0  |

#### 4.4.2.103 TPCC\_IPRH\_RN Register

##### 1 TPCC\_IPRH\_RN Register (Offset = 206Ch) [reset = 0h]

Interrupt Pending Register (High Part): IPRH.In bit is set when a interrupt completion code with TCC of N is detected. IPRH.In bit is cleared via software by writing a '1' to ICRH.In bit.

Return to [Summary Table](#)

**Table 4-2375. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 206Ch       |

**Figure 4-780. TPCC\_IPRH\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| I63 | I62 | I61 | I60 | I59 | I58 | I57 | I56 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| I55 | I54 | I53 | I52 | I51 | I50 | I49 | I48 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| I47 | I46 | I45 | I44 | I43 | I42 | I41 | I40 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| I39 | I38 | I37 | I36 | I35 | I34 | I33 | I32 |
| R   | R   | R   | R   | R   | R   | R   | R   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2377. TPCC\_IPRH\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 31  | I63   | R    | 0h    | Interrupt associated with TCC #63 |
| 30  | I62   | R    | 0h    | Interrupt associated with TCC #62 |
| 29  | I61   | R    | 0h    | Interrupt associated with TCC #61 |
| 28  | I60   | R    | 0h    | Interrupt associated with TCC #60 |
| 27  | I59   | R    | 0h    | Interrupt associated with TCC #59 |
| 26  | I58   | R    | 0h    | Interrupt associated with TCC #58 |
| 25  | I57   | R    | 0h    | Interrupt associated with TCC #57 |
| 24  | I56   | R    | 0h    | Interrupt associated with TCC #56 |
| 23  | I55   | R    | 0h    | Interrupt associated with TCC #55 |
| 22  | I54   | R    | 0h    | Interrupt associated with TCC #54 |
| 21  | I53   | R    | 0h    | Interrupt associated with TCC #53 |
| 20  | I52   | R    | 0h    | Interrupt associated with TCC #52 |
| 19  | I51   | R    | 0h    | Interrupt associated with TCC #51 |
| 18  | I50   | R    | 0h    | Interrupt associated with TCC #50 |
| 17  | I49   | R    | 0h    | Interrupt associated with TCC #49 |
| 16  | I48   | R    | 0h    | Interrupt associated with TCC #48 |
| 15  | I47   | R    | 0h    | Interrupt associated with TCC #47 |

**Table 4-2377. TPCC\_IPRH\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 14  | I46   | R    | 0h    | Interrupt associated with TCC #46 |
| 13  | I45   | R    | 0h    | Interrupt associated with TCC #45 |
| 12  | I44   | R    | 0h    | Interrupt associated with TCC #44 |
| 11  | I43   | R    | 0h    | Interrupt associated with TCC #43 |
| 10  | I42   | R    | 0h    | Interrupt associated with TCC #42 |
| 9   | I41   | R    | 0h    | Interrupt associated with TCC #41 |
| 8   | I40   | R    | 0h    | Interrupt associated with TCC #40 |
| 7   | I39   | R    | 0h    | Interrupt associated with TCC #39 |
| 6   | I38   | R    | 0h    | Interrupt associated with TCC #38 |
| 5   | I37   | R    | 0h    | Interrupt associated with TCC #37 |
| 4   | I36   | R    | 0h    | Interrupt associated with TCC #36 |
| 3   | I35   | R    | 0h    | Interrupt associated with TCC #35 |
| 2   | I34   | R    | 0h    | Interrupt associated with TCC #34 |
| 1   | I33   | R    | 0h    | Interrupt associated with TCC #33 |
| 0   | I32   | R    | 0h    | Interrupt associated with TCC #32 |

#### 4.4.2.104 TPCC\_ICR\_RN Register

##### 1 TPCC\_ICR\_RN Register (Offset = 2070h) [reset = 0h]

Interrupt Clear Register: CPU write of '1' to the ICR.In bit causes the IPR.In bit to be cleared. CPU write of '0' has no effect. All IPR.In bits must be cleared before additional interrupts will be asserted by CC.

Return to [Summary Table](#)

**Table 4-2378. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2070h       |

**Figure 4-781. TPCC\_ICR\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| I31 | I30 | I29 | I28 | I27 | I26 | I25 | I24 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| I23 | I22 | I21 | I20 | I19 | I18 | I17 | I16 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| I15 | I14 | I13 | I12 | I11 | I10 | I9  | I8  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| I7  | I6  | I5  | I4  | I3  | I2  | I1  | I0  |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2380. TPCC\_ICR\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 31  | I31   | W    | 0h    | Interrupt associated with TCC #31 |
| 30  | I30   | W    | 0h    | Interrupt associated with TCC #30 |
| 29  | I29   | W    | 0h    | Interrupt associated with TCC #29 |
| 28  | I28   | W    | 0h    | Interrupt associated with TCC #28 |
| 27  | I27   | W    | 0h    | Interrupt associated with TCC #27 |
| 26  | I26   | W    | 0h    | Interrupt associated with TCC #26 |
| 25  | I25   | W    | 0h    | Interrupt associated with TCC #25 |
| 24  | I24   | W    | 0h    | Interrupt associated with TCC #24 |
| 23  | I23   | W    | 0h    | Interrupt associated with TCC #23 |
| 22  | I22   | W    | 0h    | Interrupt associated with TCC #22 |
| 21  | I21   | W    | 0h    | Interrupt associated with TCC #21 |
| 20  | I20   | W    | 0h    | Interrupt associated with TCC #20 |
| 19  | I19   | W    | 0h    | Interrupt associated with TCC #19 |
| 18  | I18   | W    | 0h    | Interrupt associated with TCC #18 |
| 17  | I17   | W    | 0h    | Interrupt associated with TCC #17 |
| 16  | I16   | W    | 0h    | Interrupt associated with TCC #16 |
| 15  | I15   | W    | 0h    | Interrupt associated with TCC #15 |

**Table 4-2380. TPCC\_ICR\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 14  | I14   | W    | 0h    | Interrupt associated with TCC #14 |
| 13  | I13   | W    | 0h    | Interrupt associated with TCC #13 |
| 12  | I12   | W    | 0h    | Interrupt associated with TCC #12 |
| 11  | I11   | W    | 0h    | Interrupt associated with TCC #11 |
| 10  | I10   | W    | 0h    | Interrupt associated with TCC #10 |
| 9   | I9    | W    | 0h    | Interrupt associated with TCC #9  |
| 8   | I8    | W    | 0h    | Interrupt associated with TCC #8  |
| 7   | I7    | W    | 0h    | Interrupt associated with TCC #7  |
| 6   | I6    | W    | 0h    | Interrupt associated with TCC #6  |
| 5   | I5    | W    | 0h    | Interrupt associated with TCC #5  |
| 4   | I4    | W    | 0h    | Interrupt associated with TCC #4  |
| 3   | I3    | W    | 0h    | Interrupt associated with TCC #3  |
| 2   | I2    | W    | 0h    | Interrupt associated with TCC #2  |
| 1   | I1    | W    | 0h    | Interrupt associated with TCC #1  |
| 0   | I0    | W    | 0h    | Interrupt associated with TCC #0  |



#### 4.4.2.105 TPCC\_ICRH\_RN Register

##### 1 TPCC\_ICRH\_RN Register (Offset = 2074h) [reset = 0h]

Interrupt Clear Register (High Part): CPU write of '1' to the ICRH.In bit causes the IPRH.In bit to be cleared. CPU write of '0' has no effect. All IPRH.In bits must be cleared before additional interrupts will be asserted by CC.

Return to [Summary Table](#)

**Table 4-2381. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2074h       |

**Figure 4-782. TPCC\_ICRH\_RN Name Register**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  |
|-----|-----|-----|-----|-----|-----|-----|-----|
| I63 | I62 | I61 | I60 | I59 | I58 | I57 | I56 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  |
| I55 | I54 | I53 | I52 | I51 | I50 | I49 | I48 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   |
| I47 | I46 | I45 | I44 | I43 | I42 | I41 | I40 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |
| 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
| I39 | I38 | I37 | I36 | I35 | I34 | I33 | I32 |
| W   | W   | W   | W   | W   | W   | W   | W   |
| 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  | 0h  |

**Table 4-2383. TPCC\_ICRH\_RN Register Field Descriptions**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 31  | I63   | W    | 0h    | Interrupt associated with TCC #63 |
| 30  | I62   | W    | 0h    | Interrupt associated with TCC #62 |
| 29  | I61   | W    | 0h    | Interrupt associated with TCC #61 |
| 28  | I60   | W    | 0h    | Interrupt associated with TCC #60 |
| 27  | I59   | W    | 0h    | Interrupt associated with TCC #59 |
| 26  | I58   | W    | 0h    | Interrupt associated with TCC #58 |
| 25  | I57   | W    | 0h    | Interrupt associated with TCC #57 |
| 24  | I56   | W    | 0h    | Interrupt associated with TCC #56 |
| 23  | I55   | W    | 0h    | Interrupt associated with TCC #55 |
| 22  | I54   | W    | 0h    | Interrupt associated with TCC #54 |
| 21  | I53   | W    | 0h    | Interrupt associated with TCC #53 |
| 20  | I52   | W    | 0h    | Interrupt associated with TCC #52 |
| 19  | I51   | W    | 0h    | Interrupt associated with TCC #51 |
| 18  | I50   | W    | 0h    | Interrupt associated with TCC #50 |
| 17  | I49   | W    | 0h    | Interrupt associated with TCC #49 |
| 16  | I48   | W    | 0h    | Interrupt associated with TCC #48 |
| 15  | I47   | W    | 0h    | Interrupt associated with TCC #47 |

**Table 4-2383. TPCC\_ICRH\_RN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                       |
|-----|-------|------|-------|-----------------------------------|
| 14  | I46   | W    | 0h    | Interrupt associated with TCC #46 |
| 13  | I45   | W    | 0h    | Interrupt associated with TCC #45 |
| 12  | I44   | W    | 0h    | Interrupt associated with TCC #44 |
| 11  | I43   | W    | 0h    | Interrupt associated with TCC #43 |
| 10  | I42   | W    | 0h    | Interrupt associated with TCC #42 |
| 9   | I41   | W    | 0h    | Interrupt associated with TCC #41 |
| 8   | I40   | W    | 0h    | Interrupt associated with TCC #40 |
| 7   | I39   | W    | 0h    | Interrupt associated with TCC #39 |
| 6   | I38   | W    | 0h    | Interrupt associated with TCC #38 |
| 5   | I37   | W    | 0h    | Interrupt associated with TCC #37 |
| 4   | I36   | W    | 0h    | Interrupt associated with TCC #36 |
| 3   | I35   | W    | 0h    | Interrupt associated with TCC #35 |
| 2   | I34   | W    | 0h    | Interrupt associated with TCC #34 |
| 1   | I33   | W    | 0h    | Interrupt associated with TCC #33 |
| 0   | I32   | W    | 0h    | Interrupt associated with TCC #32 |

#### 4.4.2.106 TPCC\_IEVAL\_RN Register

##### 1 TPCC\_IEVAL\_RN Register (Offset = 2078h) [reset = 0h]

Interrupt Eval Register

Return to [Summary Table](#)

**Table 4-2384. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2078h       |

**Figure 4-783. TPCC\_IEVAL\_RN Name Register**

|       |    |    |    |    |    |     |      |
|-------|----|----|----|----|----|-----|------|
| 31    | 30 | 29 | 28 | 27 | 26 | 25  | 24   |
| RES76 |    |    |    |    |    |     |      |
| R     |    |    |    |    |    |     |      |
| 0h    |    |    |    |    |    |     |      |
| 23    | 22 | 21 | 20 | 19 | 18 | 17  | 16   |
| RES76 |    |    |    |    |    |     |      |
| R     |    |    |    |    |    |     |      |
| 0h    |    |    |    |    |    |     |      |
| 15    | 14 | 13 | 12 | 11 | 10 | 9   | 8    |
| RES76 |    |    |    |    |    |     |      |
| R     |    |    |    |    |    |     |      |
| 0h    |    |    |    |    |    |     |      |
| 7     | 6  | 5  | 4  | 3  | 2  | 1   | 0    |
| RES76 |    |    |    |    |    | SET | EVAL |
| R     |    |    |    |    |    | W   | W    |
| 0h    |    |    |    |    |    | 0h  | 0h   |

**Table 4-2386. TPCC\_IEVAL\_RN Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                       |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RES76 | R    | 0h    | RESERVE FIELD                                                                                                                                                                                     |
| 1    | SET   | W    | 0h    | Interrupt Set: CPU write of '1' to the SETn bit causes the tpcc_intN output signal to be pulsed egardless of state of interrupts enable [IERn] and status [IPRn]. CPU write of '0' has no effect. |
| 0    | EVAL  | W    | 0h    | Interrupt Evaluate: CPU write of '1' to the EVALn bit causes the tpcc_intN output signal to be pulsed if any enabled interrupts [IERn] are still pending [IPRn]. CPU write of '0' has no effect.. |

#### 4.4.2.107 TPCC\_QER\_RN Register

##### 1 TPCC\_QER\_RN Register (Offset = 2080h) [reset = 0h]

QDMA Event Register: If QER.En bit is set then the corresponding QDMA channel is prioritized vs. other qdma events for submission to the TC. QER.En bit is set when a vbus write byte matches the address defined in the QCHMAPn register. QER.En bit is cleared when the corresponding event is prioritized and serviced. QER.En is also cleared when user writes a '1' to the QSECR.En bit. If the QER.En bit is already set and a new QDMA event is detected due to user write to QDMA trigger location and QEER register is set then the corresponding bit in the QDMA Event Missed Register is set.

Return to [Summary Table](#)

**Table 4-2387. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2080h       |

**Figure 4-784. TPCC\_QER\_RN Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RES77 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RES77 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RES77 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| E7    | E6 | E5 | E4 | E3 | E2 | E1 | E0 |
| R     | R  | R  | R  | R  | R  | R  | R  |
| 0h    | 0h | 0h | 0h | 0h | 0h | 0h | 0h |

**Table 4-2389. TPCC\_QER\_RN Register Field Descriptions**

| Bit  | Field | Type | Reset | Description   |
|------|-------|------|-------|---------------|
| 31:8 | RES77 | R    | 0h    | RESERVE FIELD |
| 7    | E7    | R    | 0h    | Event #7      |
| 6    | E6    | R    | 0h    | Event #6      |
| 5    | E5    | R    | 0h    | Event #5      |
| 4    | E4    | R    | 0h    | Event #4      |
| 3    | E3    | R    | 0h    | Event #3      |
| 2    | E2    | R    | 0h    | Event #2      |
| 1    | E1    | R    | 0h    | Event #1      |
| 0    | E0    | R    | 0h    | Event #0      |

#### 4.4.2.108 TPCC\_QEER\_RN Register

##### 1 TPCC\_QEER\_RN Register (Offset = 2084h) [reset = 0h]

QDMA Event Enable Register: Enabled/disabled QDMA address comparator for QDMA Channel N. QEER.En is not directly writeable. QDMA channels can be enabled via writes to QEESR and can be disabled via writes to QEECR register. QEER.En = 1 The corresponding QDMA channel comparator is enabled and Events will be recognized and latched in QER.En. QEER.En = 0 The corresponding QDMA channel comparator is disabled. Events will not be recognized/latched in QER.En.

Return to [Summary Table](#)

**Table 4-2390. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2084h       |

**Figure 4-785. TPCC\_QEER\_RN Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RES78 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RES78 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RES78 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| E7    | E6 | E5 | E4 | E3 | E2 | E1 | E0 |
| R     | R  | R  | R  | R  | R  | R  | R  |
| 0h    | 0h | 0h | 0h | 0h | 0h | 0h | 0h |

**Table 4-2392. TPCC\_QEER\_RN Register Field Descriptions**

| Bit  | Field | Type | Reset | Description   |
|------|-------|------|-------|---------------|
| 31:8 | RES78 | R    | 0h    | RESERVE FIELD |
| 7    | E7    | R    | 0h    | Event #7      |
| 6    | E6    | R    | 0h    | Event #6      |
| 5    | E5    | R    | 0h    | Event #5      |
| 4    | E4    | R    | 0h    | Event #4      |
| 3    | E3    | R    | 0h    | Event #3      |
| 2    | E2    | R    | 0h    | Event #2      |
| 1    | E1    | R    | 0h    | Event #1      |
| 0    | E0    | R    | 0h    | Event #0      |

#### 4.4.2.109 TPCC\_QEECR\_RN Register

##### 1 TPCC\_QEECR\_RN Register (Offset = 2088h) [reset = 0h]

QDMA Event Enable Clear Register: CPU write of '1' to the QEECR.En bit causes the QEER.En bit to be cleared. CPU write of '0' has no effect..

Return to [Summary Table](#)

**Table 4-2393. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2088h       |

**Figure 4-786. TPCC\_QEECR\_RN Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RES79 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RES79 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RES79 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| E7    | E6 | E5 | E4 | E3 | E2 | E1 | E0 |
| W     | W  | W  | W  | W  | W  | W  | W  |
| 0h    | 0h | 0h | 0h | 0h | 0h | 0h | 0h |

**Table 4-2395. TPCC\_QEECR\_RN Register Field Descriptions**

| Bit  | Field | Type | Reset | Description   |
|------|-------|------|-------|---------------|
| 31:8 | RES79 | R    | 0h    | RESERVE FIELD |
| 7    | E7    | W    | 0h    | Event #7      |
| 6    | E6    | W    | 0h    | Event #6      |
| 5    | E5    | W    | 0h    | Event #5      |
| 4    | E4    | W    | 0h    | Event #4      |
| 3    | E3    | W    | 0h    | Event #3      |
| 2    | E2    | W    | 0h    | Event #2      |
| 1    | E1    | W    | 0h    | Event #1      |
| 0    | E0    | W    | 0h    | Event #0      |

#### 4.4.2.110 TPCC\_QEESR\_RN Register

##### 1 TPCC\_QEESR\_RN Register (Offset = 208Ch) [reset = 0h]

QDMA Event Enable Set Register: CPU write of '1' to the QEESR.En bit causes the QEESR.En bit to be set. CPU write of '0' has no effect..

Return to [Summary Table](#)

**Table 4-2396. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 208Ch       |

**Figure 4-787. TPCC\_QEESR\_RN Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RES80 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RES80 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RES80 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| E7    | E6 | E5 | E4 | E3 | E2 | E1 | E0 |
| W     | W  | W  | W  | W  | W  | W  | W  |
| 0h    | 0h | 0h | 0h | 0h | 0h | 0h | 0h |

**Table 4-2398. TPCC\_QEESR\_RN Register Field Descriptions**

| Bit  | Field | Type | Reset | Description   |
|------|-------|------|-------|---------------|
| 31:8 | RES80 | R    | 0h    | RESERVE FIELD |
| 7    | E7    | W    | 0h    | Event #7      |
| 6    | E6    | W    | 0h    | Event #6      |
| 5    | E5    | W    | 0h    | Event #5      |
| 4    | E4    | W    | 0h    | Event #4      |
| 3    | E3    | W    | 0h    | Event #3      |
| 2    | E2    | W    | 0h    | Event #2      |
| 1    | E1    | W    | 0h    | Event #1      |
| 0    | E0    | W    | 0h    | Event #0      |

#### 4.4.2.111 TPCC\_QSER\_RN Register

##### 1 TPCC\_QSER\_RN Register (Offset = 2090h) [reset = 0h]

QDMA Secondary Event Register: The QDMA secondary event register is used along with the QDMA Event Register (QER) to provide information on the state of a QDMA Event. En = 0 : Event is not currently in the Event Queue. En = 1 : Event is currently stored in Event Queue. Event arbiter will not prioritize additional events.

Return to [Summary Table](#)

**Table 4-2399. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2090h       |

**Figure 4-788. TPCC\_QSER\_RN Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RES81 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RES81 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RES81 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| E7    | E6 | E5 | E4 | E3 | E2 | E1 | E0 |
| R     | R  | R  | R  | R  | R  | R  | R  |
| 0h    | 0h | 0h | 0h | 0h | 0h | 0h | 0h |

**Table 4-2401. TPCC\_QSER\_RN Register Field Descriptions**

| Bit  | Field | Type | Reset | Description   |
|------|-------|------|-------|---------------|
| 31:8 | RES81 | R    | 0h    | RESERVE FIELD |
| 7    | E7    | R    | 0h    | Event #7      |
| 6    | E6    | R    | 0h    | Event #6      |
| 5    | E5    | R    | 0h    | Event #5      |
| 4    | E4    | R    | 0h    | Event #4      |
| 3    | E3    | R    | 0h    | Event #3      |
| 2    | E2    | R    | 0h    | Event #2      |
| 1    | E1    | R    | 0h    | Event #1      |
| 0    | E0    | R    | 0h    | Event #0      |



#### 4.4.2.112 TPCC\_QSECR\_RN Register

##### 1 TPCC\_QSECR\_RN Register (Offset = 2094h) [reset = 0h]

QDMA Secondary Event Clear Register: The secondary event clear register is used to clear the status of the QSER and QER register (note that this is slightly different than the SER operation which does not clear the ER.En register). CPU write of '1' to the QSECR.En bit clears the QSER.En and QER.En register fields. CPU write of '0' has no effect..

Return to [Summary Table](#)

**Table 4-2402. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 2094h       |

**Figure 4-789. TPCC\_QSECR\_RN Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RES82 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RES82 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RES82 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| E7    | E6 | E5 | E4 | E3 | E2 | E1 | E0 |
| W     | W  | W  | W  | W  | W  | W  | W  |
| 0h    | 0h | 0h | 0h | 0h | 0h | 0h | 0h |

**Table 4-2404. TPCC\_QSECR\_RN Register Field Descriptions**

| Bit  | Field | Type | Reset | Description   |
|------|-------|------|-------|---------------|
| 31:8 | RES82 | R    | 0h    | RESERVE FIELD |
| 7    | E7    | W    | 0h    | Event #7      |
| 6    | E6    | W    | 0h    | Event #6      |
| 5    | E5    | W    | 0h    | Event #5      |
| 4    | E4    | W    | 0h    | Event #4      |
| 3    | E3    | W    | 0h    | Event #3      |
| 2    | E2    | W    | 0h    | Event #2      |
| 1    | E1    | W    | 0h    | Event #1      |
| 0    | E0    | W    | 0h    | Event #0      |

#### 4.4.2.113 TPCC\_OPT Register

##### 1 TPCC\_OPT Register (Offset = 4000h) [reset = 0h]

Options Parameter

Return to [Summary Table](#)
**Table 4-2405. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 4000h       |

**Figure 4-790. TPCC\_OPT Name Register**

| 31      | 30     | 29       | 28      | 27      | 26      | 25  | 24  |
|---------|--------|----------|---------|---------|---------|-----|-----|
| PRIV    | RES83  |          |         | PRIVID  |         |     |     |
| R       | R      |          |         | R       |         |     |     |
| 0h      | 0h     |          |         | 0h      |         |     |     |
| 23      | 22     | 21       | 20      | 19      | 18      | 17  | 16  |
| ITCCHEN | TCCHEN | ITCINTEN | TCINTEN | WIMODE  | RES84   | TCC |     |
| R/W     | R/W    | R/W      | R/W     | R/W     | R       | R/W |     |
| 0h      | 0h     | 0h       | 0h      | 0h      | 0h      | 0h  |     |
| 15      | 14     | 13       | 12      | 11      | 10      | 9   | 8   |
| TCC     |        |          |         | TCCMODE | FWID    |     |     |
| R/W     |        |          |         | R/W     | R/W     |     |     |
| 0h      |        |          |         | 0h      | 0h      |     |     |
| 7       | 6      | 5        | 4       | 3       | 2       | 1   | 0   |
| RES85   |        |          |         | STATIC  | SYNCDIM | DAM | SAM |
| R       |        |          |         | R/W     | R/W     | R/W | R/W |
| 0h      |        |          |         | 0h      | 0h      | 0h  | 0h  |

**Table 4-2407. TPCC\_OPT Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                    |
|-------|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | PRIV     | R    | 0h    | Privilege level: privilege level [supervisor vs. user] for the host/cpu/dma that programmed this PaRAM Entry. Value is set with the vbus priv value when any part of the PaRAM Entry is written. Not writeable via vbus wdata bus. Is readable via VBus rdata bus. PRIV =<br>0 : User level privilege PRIV =<br>1 : Supervisor level privilege |
| 30:28 | RES83    | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                                                                                                                  |
| 27:24 | PRIVID   | R    | 0h    | Privilege ID: Privilege ID for the external host/cpu/dma that programmed this PaRAM Entry. This value is set with the vbus privid value when any part of the PaRAM Entry is written. Not writeable via vbus wdata bus. Is readable via VBus rdata bus.                                                                                         |
| 23    | ITCCHEN  | R/W  | 0h    | Intermediate transfer completion chaining enable:<br>0: Intermediate transfer complete chaining is disabled.<br>1: Intermediate transfer complete chaining is enabled.                                                                                                                                                                         |
| 22    | TCCHEN   | R/W  | 0h    | Transfer complete chaining enable:<br>0: Transfer complete chaining is disabled.<br>1: Transfer complete chaining is enabled.                                                                                                                                                                                                                  |
| 21    | ITCINTEN | R/W  | 0h    | Intermediate transfer completion interrupt enable:<br>0: Intermediate transfer complete interrupt is disabled.<br>1: Intermediate transfer complete interrupt is enabled [corresponding IER[TCC] bit must be set to 1 to generate interrupt]                                                                                                   |

**Table 4-2407. TPCC\_OPT Register Field Descriptions (continued)**

| Bit   | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|---------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 20    | TCINTEN | R/W  | 0h    | Transfer complete interrupt enable:<br>0:Transfer complete interrupt is disabled.<br>1:Transfer complete interrupt is enabled [corresponding IER[TCC] bit must be set to 1 to generate interrupt]                                                                                                                                                                                                                                                  |
| 19    | WIMODE  | R/W  | 0h    | Backward compatibility mode:<br>0:Normal operation<br>1 : WI Backwards Compatibility mode forces BCNT to be adjusted by '1' upon TR submission [0 means 1 1 means 2 ... ] and forces ACNT to be treated as a word-count [left shifted by 2 by hardware to create byte cnt for TR submission]                                                                                                                                                       |
| 18    | RES84   | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 17:12 | TCC     | R/W  | 0h    | Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER [bit CER[TCC]] for chaining or in IER [bit IER[TCC]] for interrupts.                                                                                                                                                                                                                                                                                                 |
| 11    | TCCMODE | R/W  | 0h    | Transfer complete code mode: Indicates the point at which a transfer is considered completed. Applies to both chaining and interrupt.<br>0:Normal Completion A transfer is considered completed after the transfer parameters are returned to the CC from the TC [which was returned from the peripheral].<br>1:Early Completion A transfer is considered completed after the CC submits a TR to the TC. CC generates completion code internally . |
| 10:8  | FWID    | R/W  | 0h    | FIFO width: Applies if either SAM or DAM is set to FIFO mode. Pass-thru to TC.                                                                                                                                                                                                                                                                                                                                                                     |
| 7:4   | RES85   | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 3     | STATIC  | R/W  | 0h    | Static Entry:<br>0:Entry is updated as normal<br>1:Entry is static Count and Address updates are not updated after TRP is submitted. Linking is not performed.                                                                                                                                                                                                                                                                                     |
| 2     | SYNCDIM | R/W  | 0h    | Transfer Synchronization Dimension:<br>0:A-Sync Each event triggers the transfer of ACNT elements.<br>1:AB-Sync Each event triggers the transfer of BCNT arrays of ACNT elements                                                                                                                                                                                                                                                                   |
| 1     | DAM     | R/W  | 0h    | Destination Address Mode: Destination Address Mode within an array. Pass-thru to TC.<br>0:INCR Dst addressing within an array increments. Dst is not a FIFO.<br>1:FIFO Dst addressing within an array wraps around upon reaching FIFO width.                                                                                                                                                                                                       |
| 0     | SAM     | R/W  | 0h    | Source Address Mode: Source Address Mode within an array. Pass-thru to TC.<br>0:INCR Src addressing within an array increments. Source is not a FIFO.<br>1:FIFO Src addressing within an array wraps around upon reaching FIFO width.                                                                                                                                                                                                              |

#### 4.4.2.114 TPCC\_SRC Register

##### 1 TPCC\_SRC Register (Offset = 4004h) [reset = 0h]

Source Address

Return to [Summary Table](#)

**Table 4-2408. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 4004h       |

**Figure 4-791. TPCC\_SRC Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SRC |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SRC |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SRC |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SRC |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 4-2410. TPCC\_SRC Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                               |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | SRC   | R/W  | 0h    | Source Address: The 32-bit source address parameters specify the starting byte address of the source . If SAM is set to FIFO mode then the user should program the Source address to be aligned to the value specified by the OPT.FWID field. No errors are recognized here but TC will assert error if this is not true. |

#### 4.4.2.115 TPCC\_ABCNT Register

##### 1 TPCC\_ABCNT Register (Offset = 4008h) [reset = 0h]

A and B byte count

Return to [Summary Table](#)

**Table 4-2411. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 4008h       |

**Figure 4-792. TPCC\_ABCNT Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BCNT |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BCNT |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ACNT |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ACNT |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 4-2413. TPCC\_ABCNT Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | BCNT  | R/W  | 0h    | BCNT : Count for 2nd Dimension: BCNT is a 16-bit unsigned value that specifies the number of arrays of length ACNT. For normal operation valid values for BCNT can be anywhere between 1 and 65535. Therefore the maximum number of arrays in a frame is 65535 [64K-1 arrays]. BCNT=1 means 1 array in the frame and BCNT=0 means 0 arrays in the frame. In normal mode a BCNT of '0' is considered as either a Null or Dummy transfer. A Dummy or Null transfer will generate a Completion code depending on the settings of the completion bit fields of the OPT field. If the OPT.WIMODE bit is set then the programmed BCNT value will be incremented by '1' before submission to TC. I.e. 0 means 1 1 means 2 2 means 3 ... |

**Table 4-2413. TPCC\_ABCNT Register Field Descriptions (continued)**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | ACNT  | R/W  | 0h    | ACNT : number of bytes in 1st dimension: ACNT represents the number of bytes within the first dimension of a transfer. ACNT is a 16-bit unsigned value with valid values between 0 and 65535. Therefore the maximum number of bytes in an array is 65535 bytes [64K-1 bytes]. ACNT must be greater than or equal to '1' for a TR to be submitted to TC. An ACNT of '0' is considered as either a null or dummy transfer. A Dummy or Null transfer will generate a Completion code depending on the settings of the completion bit fields of the OPT field. If the OPT.WIMODE bit is set then the ACNT field represents a word count. The CC must internally multiply by 4 to translate the word count to a byte count prior to submission to the TC. The 2 MSBs of the 16-bit ACNT are reserved and should always be written as 'b00 by the user. If user writes a value other than 0 it will still be treated as 0 since the multiply-by-4 operation [to translate between a word count and a byte count] will drop the 2 msbits. For dummy and null transfer definition the ACNT definition will disregard the 2 msbits. I.e. a programmed ACNT value of 0x8000 in WI-mode will be treated as 0 byte transfer resulting in null or dummy operation dependent on the state of BCNT and CCNT. |

#### 4.4.2.116 TPCC\_DST Register

##### 1 TPCC\_DST Register (Offset = 400Ch) [reset = 0h]

Destination Address

Return to [Summary Table](#)

**Table 4-2414. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 400Ch       |

**Figure 4-793. TPCC\_DST Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DST |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DST |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DST |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DST |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 4-2416. TPCC\_DST Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | DST   | R/W  | 0h    | Destination Address: The 32-bit destination address parameters specify the starting byte address of the destination. If DAM is set to FIFO mode then the user should program the Destination address to be aligned to the value specified by the OPT.FWID field. No errors are recognized here but TC will assert error if this is not true. |

#### 4.4.2.117 TPCC\_BIDX Register

##### 1 TPCC\_BIDX Register (Offset = 4010h) [reset = 0h]

Register description is not available

Return to [Summary Table](#)

**Table 4-2417. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 4010h       |

**Figure 4-794. TPCC\_BIDX Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DBIDX |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DBIDX |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SBIDX |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SBIDX |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-2419. TPCC\_BIDX Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | DBIDX | R/W  | 0h    | Destination 2nd Dimension Index: DBIDX is a 16-bit signed value [2's complement] used for destination address modification in between each array in the 2nd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the destination array to the beginning of the next destination array within the current frame. It applies to both A-Sync and AB-Sync transfers. |
| 15:0  | SBIDX | R/W  | 0h    | Source 2nd Dimension Index: SBIDX is a 16-bit signed value [2's complement] used for source address modification in between each array in the 2nd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the source array to the beginning of the next source array. It applies to both A-sync and AB-sync transfers.                                              |



#### 4.4.2.118 TPCC\_LNK Register

##### 1 TPCC\_LNK Register (Offset = 4014h) [reset = 0h]

Link and Reload parameters

Return to [Summary Table](#)

**Table 4-2420. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 4014h       |

**Figure 4-795. TPCC\_LNK Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BCNTRLD |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BCNTRLD |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| LINK    |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LINK    |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 4-2422. TPCC\_LNK Register Field Descriptions**

| Bit   | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|---------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | BCNTRLD | R/W  | 0h    | BCNT Reload: BCNTRLD is a 16-bit unsigned value used to reload the BCNT field once the last array in the 2nd dimension is transferred. This field is only used for A-Sync'ed transfers. In this case the CC decrements the BCNT value by one on each TR submission. When BCNT [conceptually] reaches zero then the CC decrements CCNT and uses the BCNTRLD value to reinitialize the BCNT value. For AB-synchronized transfers the CC submits the BCNT in the TR and therefore the TC is responsible to keep track of BCNT not thus BCNTRLD is a don't care field. |

**Table 4-2422. TPCC\_LNK Register Field Descriptions (continued)**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | LINK  | R/W  | 0h    | <p>Link Address: The CC provides a mechanism to reload the current PaRAM Entry upon its natural termination [i.e. after count fields are decremented to '0'] with a new PaRAM Entry. This is called 'linking'. The 16-bit parameter LINK specifies the byte address offset in the PaRAM from which the CC loads/reloads the next PaRAM entry in the link. The CC should disregard the value in the upper 2 bits of the LINK field as well as the lower 5-bits of the LINK field. The upper two bits are ignored such that the user can program either the 'literal' byte address of the LINK parameter or the 'PaRAM base-relative' address of the link field. Therefore if the user uses the literal address with a range from 0x4000 to 0x7FFF it will be treated as a PaRAM-base-relative value of 0x0000 to 0x3FFF. The lower-5 bits are ignored and treated as 'b00000' thereby guaranteeing that all Link pointers point to a 32-byte aligned PaRAM entry. In the latter case [5-lsbs] behavior is undefined for the user [i.e. don't have to test it]. In the former case [2 msbs] user should be able to take advantage of this feature [i.e. do have to test it]. If a Link Update is requested to a PaRAM address that is beyond the actual range of implemented PaRAM then the Link will be treated as a Null Link and all 0s plus 0xFFFF will be written to the current entry location. A LINK value of 0xFFFF is referred to as a NULL link which should cause the CC to write 0x0 to all entries of the current PaRAM Entry except for the LINK field which is set to 0xFFFF. The Priv/Privid/Secure state is overwritten to 0x0 when linking. MSBs and LSBS should not be masked when comparing against the 0xFFFF value. I.e. a value of 0x3FFE is a non-NULL PaRAM link field.</p> |

#### 4.4.2.119 TPCC\_CIDX Register

##### 1 TPCC\_CIDX Register (Offset = 4018h) [reset = 0h]

Register description is not available

Return to [Summary Table](#)

**Table 4-2423. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 4018h       |

**Figure 4-796. TPCC\_CIDX Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DCIDX |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DCIDX |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SCIDX |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SCIDX |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-2425. TPCC\_CIDX Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | DCIDX | R/W  | 0h    | Destination Frame Index: DCIDX is a 16-bit signed value [2's complement] used for destination address modification for the 3rd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the current array [pointed to by DST address] to the beginning of the first destination array in the next frame. It applies to both A-sync and AB-sync transfers. Note that when DCIDX is applied the current array in an A-sync transfer is the last array in the frame while the current array in a ABsync transfer is the first array in the frame. |
| 15:0  | SCIDX | R/W  | 0h    | Source Frame Index: SCIDX is a 16-bit signed value [2's complement] used for source address modification for the 3rd dimension. It is a signed value between -32768 and 32767. It provides a byte address offset from the beginning of the current array [pointed to by SRC address] to the beginning of the first source array in the next frame. It applies to both A-sync and AB-sync transfers. Note that when SCIDX is applied the current array in an A-sync transfer is the last array in the frame while the current array in a AB-sync transfer is the first array in the frame.               |

#### 4.4.2.120 TPCC\_CCNT Register

##### 1 TPCC\_CCNT Register (Offset = 401Ch) [reset = 0h]

C byte count

Return to [Summary Table](#)

**Table 4-2426. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A0 401Ch       |

**Figure 4-797. TPCC\_CCNT Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RES86 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RES86 |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CCNT  |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CCNT  |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-2428. TPCC\_CCNT Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RES86 | R    | 0h    | RESERVE FIELD                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 15:0  | CCNT  | R/W  | 0h    | CCNT : Count for 3rd Dimension: CCNT is a 16-bit unsigned value that specifies the number of frames in a block. Valid values for CCNT can be anywhere between 1 and 65535. Therefore the maximum number of frames in a block is 65535 [64K-1 frames]. CCNT of '1' means '1' frame in the block and CCNT of '0' means '0' frames in the block. A CCNT value of '0' is considered as either a null or dummy transfer. A Dummy or Null transfer will generate a Completion code depending on the settings of the completion bit fields of the OPT field. WIMODE has no effect on CCNT operation. |

#### 4.4.2.121 TPTC\_PID Register

##### 1 TPTC\_PID Register (Offset = 0h) [reset = 4000B01h]

Peripheral ID Register.

Return to [Summary Table](#)

**Table 4-2429. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0000h       |
| EDMA1         | 52A4 0000h       |

**Figure 4-798. TPTC\_PID Name Register**

|        |    |          |    |       |    |    |    |
|--------|----|----------|----|-------|----|----|----|
| 31     | 30 | 29       | 28 | 27    | 26 | 25 | 24 |
| SCHEME |    | RESERVED |    | FUNC  |    |    |    |
| R      |    | NONE     |    | R     |    |    |    |
| 1h     |    | 0h       |    | 0h    |    |    |    |
| 23     | 22 | 21       | 20 | 19    | 18 | 17 | 16 |
| FUNC   |    |          |    |       |    |    |    |
| R      |    |          |    |       |    |    |    |
| 0h     |    |          |    |       |    |    |    |
| 15     | 14 | 13       | 12 | 11    | 10 | 9  | 8  |
| RTL    |    |          |    | MAJOR |    |    |    |
| R      |    |          |    | R     |    |    |    |
| 1h     |    |          |    | 3h    |    |    |    |
| 7      | 6  | 5        | 4  | 3     | 2  | 1  | 0  |
| CUSTOM |    | MINOR    |    |       |    |    |    |
| R      |    | R        |    |       |    |    |    |
| 0h     |    | 1h       |    |       |    |    |    |

**Table 4-2431. TPTC\_PID Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                               |
|-------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | SCHEME   | R    | 1h    | PID Scheme: Used to distinguish between old ID scheme and current. Spare bit to encode future schemes EDMA uses 'new scheme' indicated with value of 0x1. |
| 29:28 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                  |
| 27:16 | FUNC     | R    | 0h    | Function indicates a software compatible module family.                                                                                                   |
| 15:11 | RTL      | R    | 1h    | RTL Version                                                                                                                                               |
| 10:8  | MAJOR    | R    | 3h    | Major Revision                                                                                                                                            |
| 7:6   | CUSTOM   | R    | 0h    | Custom revision field: Not used on this version of EDMA.                                                                                                  |
| 5:0   | MINOR    | R    | 1h    | Minor Revision                                                                                                                                            |

#### 4.4.2.122 TPTC\_TCCFG Register

##### 1 TPTC\_TCCFG Register (Offset = 4h) [reset = 224h]

TC Configuration Register.

Return to [Summary Table](#)

**Table 4-2432. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0004h       |
| EDMA1         | 52A4 0004h       |

**Figure 4-799. TPTC\_TCCFG Name Register**

|          |    |          |    |          |    |           |    |
|----------|----|----------|----|----------|----|-----------|----|
| 31       | 30 | 29       | 28 | 27       | 26 | 25        | 24 |
| RESERVED |    |          |    |          |    |           |    |
| NONE     |    |          |    |          |    |           |    |
| 0h       |    |          |    |          |    |           |    |
| 23       | 22 | 21       | 20 | 19       | 18 | 17        | 16 |
| RESERVED |    |          |    |          |    |           |    |
| NONE     |    |          |    |          |    |           |    |
| 0h       |    |          |    |          |    |           |    |
| 15       | 14 | 13       | 12 | 11       | 10 | 9         | 8  |
| RESERVED |    |          |    |          |    | DREGDEPTH |    |
| NONE     |    |          |    |          |    | R         |    |
| 0h       |    |          |    |          |    | 2h        |    |
| 7        | 6  | 5        | 4  | 3        | 2  | 1         | 0  |
| RESERVED |    | BUSWIDTH |    | RESERVED |    | FIFOSIZE  |    |
| NONE     |    | R        |    | NONE     |    | R         |    |
| 0h       |    | 2h       |    | 0h       |    | 4h        |    |

**Table 4-2434. TPTC\_TCCFG Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                              |
|-------|-----------|------|-------|------------------------------------------|
| 31:10 | RESERVED  | NONE | 0h    | Reserved                                 |
| 9:8   | DREGDEPTH | R    | 2h    | Dst Register FIFO Depth Parameterization |
| 7:6   | RESERVED  | NONE | 0h    | Reserved                                 |
| 5:4   | BUSWIDTH  | R    | 2h    | Bus Width Parameterization               |
| 3     | RESERVED  | NONE | 0h    | Reserved                                 |
| 2:0   | FIFOSIZE  | R    | 4h    | Fifo Size Parameterization               |

#### 4.4.2.123 TPTC\_TCSTAT Register

##### 1 TPTC\_TCSTAT Register (Offset = 100h) [reset = 100h]

TC Status Register.

Return to [Summary Table](#)

**Table 4-2435. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0100h       |
| EDMA1         | 52A4 0100h       |

**Figure 4-800. TPTC\_TCSTAT Name Register**

|          |         |           |    |          |        |         |          |
|----------|---------|-----------|----|----------|--------|---------|----------|
| 31       | 30      | 29        | 28 | 27       | 26     | 25      | 24       |
| RESERVED |         |           |    |          |        |         |          |
| NONE     |         |           |    |          |        |         |          |
| 0h       |         |           |    |          |        |         |          |
| 23       | 22      | 21        | 20 | 19       | 18     | 17      | 16       |
| RESERVED |         |           |    |          |        |         |          |
| NONE     |         |           |    |          |        |         |          |
| 0h       |         |           |    |          |        |         |          |
| 15       | 14      | 13        | 12 | 11       | 10     | 9       | 8        |
| RESERVED |         | DFSTRTPTR |    | RESERVED |        | ACTV    |          |
| NONE     |         | R         |    | NONE     |        | R       |          |
| 0h       |         | 0h        |    | 0h       |        | 1h      |          |
| 7        | 6       | 5         | 4  | 3        | 2      | 1       | 0        |
| RESERVED | DSTACTV |           |    | RESERVED | WSACTV | SRCACTV | PROGBUSY |
| NONE     | R       |           |    | NONE     | R      | R       | R        |
| 0h       | 0h      |           |    | 0h       | 0h     | 0h      | 0h       |

**Table 4-2437. TPTC\_TCSTAT Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                    |
|-------|-----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:14 | RESERVED  | NONE | 0h    | Reserved                                                                                                                                                                                                       |
| 13:12 | DFSTRTPTR | R    | 0h    | Dst FIFO Start Pointer<br>Represents the offset to the head entry of Dst Register FIFO in units of entries. Legal values = 0x0 to 0x3                                                                          |
| 11:9  | RESERVED  | NONE | 0h    | Reserved                                                                                                                                                                                                       |
| 8     | ACTV      | R    | 1h    | Channel Active<br>Channel Active is a logical-OR of each of the BUSY/ACTV signals. The ACTV bit must remain high through the life of a TR.<br>ACTV =<br>0 : Channel is idle.<br>ACTV =<br>1 : Channel is busy. |
| 7     | RESERVED  | NONE | 0h    | Reserved                                                                                                                                                                                                       |
| 6:4   | DSTACTV   | R    | 0h    | Destination Active State<br>Specifies the number of TRs that are resident in the Dst Register FIFO at a given instant.<br>Legal values are constrained by the DSTREGDEPTH parameter.                           |
| 3     | RESERVED  | NONE | 0h    | Reserved                                                                                                                                                                                                       |

**Table 4-2437. TPTC\_TCSTAT Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                            |
|-----|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | WSACTV   | R    | 0h    | Write Status Active<br>WSACTV =<br>0 : Write status is not pending. Write status has been received for all previously issued write commands.<br>WSACTV =<br>1 : Write Status is pending. Write status has not been received for all previously issued write commands.                                                                                  |
| 1   | SRACTV   | R    | 0h    | Source Active State<br>SRACTV =<br>0 : Source Active set is idle. Any TR written to Prog Set will immediately transition to Source Active set as long as the Dst FIFO Set is not full [DSTFULL == 1].<br>SRACTV =<br>1 : Source Active set is busy either performing read transfers or waiting to perform read transfers for current Transfer Request. |
| 0   | PROGBUSY | R    | 0h    | Program Register Set Busy<br>PROGBUSY =<br>0 : Prog set idle and is available for programming.<br>PROGBUSY =<br>1 : Prog set busy. User should poll for PROGBUSY equal to '0' prior to re-programming the Program Register set.                                                                                                                        |



#### 4.4.2.124 TPTC\_INTSTAT Register

##### 1 TPTC\_INTSTAT Register (Offset = 104h) [reset = 0h]

Interrupt Status Register.

Return to [Summary Table](#)

**Table 4-2438. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0104h       |
| EDMA1         | 52A4 0104h       |

**Figure 4-801. TPTC\_INTSTAT Name Register**

|          |    |    |    |    |    |        |           |
|----------|----|----|----|----|----|--------|-----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25     | 24        |
| RESERVED |    |    |    |    |    |        |           |
| NONE     |    |    |    |    |    |        |           |
| 0h       |    |    |    |    |    |        |           |
| 23       | 22 | 21 | 20 | 19 | 18 | 17     | 16        |
| RESERVED |    |    |    |    |    |        |           |
| NONE     |    |    |    |    |    |        |           |
| 0h       |    |    |    |    |    |        |           |
| 15       | 14 | 13 | 12 | 11 | 10 | 9      | 8         |
| RESERVED |    |    |    |    |    |        |           |
| NONE     |    |    |    |    |    |        |           |
| 0h       |    |    |    |    |    |        |           |
| 7        | 6  | 5  | 4  | 3  | 2  | 1      | 0         |
| RESERVED |    |    |    |    |    | TRDONE | PROGEMPTY |
| NONE     |    |    |    |    |    | R      | R         |
| 0h       |    |    |    |    |    | 0h     | 0h        |

**Table 4-2440. TPTC\_INTSTAT Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                       |
|------|-----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED  | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                          |
| 1    | TRDONE    | R    | 0h    | TR Done Event Status:<br>TRDONE =<br>0 : Condition not detected.<br>TRDONE =<br>1 : Set when TC has completed a Transfer Request. TRDONE should be set when the write status is returned for the final write of a TR. Cleared when user writes '1' to INTCLR.TRDONE register bit. |
| 0    | PROGEMPTY | R    | 0h    | Program Set Empty Event Status:<br>PROGEMPTY =<br>0 : Condition not detected.<br>PROGEMPTY =<br>1 : Set when Program Register set transitions to empty state. Cleared when user writes '1' to INTCLR.PROGEMPTY register bit.                                                      |

#### 4.4.2.125 TPTC\_INTEN Register

##### 1 TPTC\_INTEN Register (Offset = 108h) [reset = 0h]

Interrupt Enable Register.

Return to [Summary Table](#)

**Table 4-2441. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0108h       |
| EDMA1         | 52A4 0108h       |

**Figure 4-802. TPTC\_INTEN Name Register**

|          |    |    |    |    |    |        |           |
|----------|----|----|----|----|----|--------|-----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25     | 24        |
| RESERVED |    |    |    |    |    |        |           |
| NONE     |    |    |    |    |    |        |           |
| 0h       |    |    |    |    |    |        |           |
| 23       | 22 | 21 | 20 | 19 | 18 | 17     | 16        |
| RESERVED |    |    |    |    |    |        |           |
| NONE     |    |    |    |    |    |        |           |
| 0h       |    |    |    |    |    |        |           |
| 15       | 14 | 13 | 12 | 11 | 10 | 9      | 8         |
| RESERVED |    |    |    |    |    |        |           |
| NONE     |    |    |    |    |    |        |           |
| 0h       |    |    |    |    |    |        |           |
| 7        | 6  | 5  | 4  | 3  | 2  | 1      | 0         |
| RESERVED |    |    |    |    |    | TRDONE | PROGEMPTY |
| NONE     |    |    |    |    |    | R/W    | R/W       |
| 0h       |    |    |    |    |    | 0h     | 0h        |

**Table 4-2443. TPTC\_INTEN Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                             |
|------|-----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED  | NONE | 0h    | Reserved                                                                                                                                                                                |
| 1    | TRDONE    | R/W  | 0h    | TR Done Event Enable:<br>INTEN.TRDONE =<br>0 : TRDONE Event is disabled.<br>INTEN.TRDONE =<br>1 : TRDONE Event is enabled and contributes to interrupt generation                       |
| 0    | PROGEMPTY | R/W  | 0h    | Program Set Empty Event Enable:<br>INTEN.PROGEMPTY =<br>0 : PROGEMPTY Event is disabled.<br>INTEN.PROGEMPTY =<br>1 : PROGEMPTY Event is enabled and contributes to interrupt generation |

#### 4.4.2.126 TPTC\_INTCLR Register

##### 1 TPTC\_INTCLR Register (Offset = 10Ch) [reset = 0h]

Interrupt Clear Register.

Return to [Summary Table](#)

**Table 4-2444. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 010Ch       |
| EDMA1         | 52A4 010Ch       |

**Figure 4-803. TPTC\_INTCLR Name Register**

|          |    |    |    |    |    |        |           |
|----------|----|----|----|----|----|--------|-----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25     | 24        |
| RESERVED |    |    |    |    |    |        |           |
| NONE     |    |    |    |    |    |        |           |
| 0h       |    |    |    |    |    |        |           |
| 23       | 22 | 21 | 20 | 19 | 18 | 17     | 16        |
| RESERVED |    |    |    |    |    |        |           |
| NONE     |    |    |    |    |    |        |           |
| 0h       |    |    |    |    |    |        |           |
| 15       | 14 | 13 | 12 | 11 | 10 | 9      | 8         |
| RESERVED |    |    |    |    |    |        |           |
| NONE     |    |    |    |    |    |        |           |
| 0h       |    |    |    |    |    |        |           |
| 7        | 6  | 5  | 4  | 3  | 2  | 1      | 0         |
| RESERVED |    |    |    |    |    | TRDONE | PROGEMPTY |
| NONE     |    |    |    |    |    | W      | W         |
| 0h       |    |    |    |    |    | 0h     | 0h        |

**Table 4-2446. TPTC\_INTCLR Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                      |
|------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED  | NONE | 0h    | Reserved                                                                                                                                                         |
| 1    | TRDONE    | W    | 0h    | TR Done Event Clear:<br>INTCLR.TRDONE =<br>0 : Writes of '0' have no effect.<br>INTCLR.TRDONE =<br>1 : Write of '1' clears INTSTAT.TRDONE bit                    |
| 0    | PROGEMPTY | W    | 0h    | Program Set Empty Event Clear:<br>INTCLR.PROGEMPTY =<br>0 : Writes of '0' have no effect.<br>INTCLR.PROGEMPTY =<br>1 : Write of '1' clears INTSTAT.PROGEMPTY bit |

#### 4.4.2.127 TPTC\_INTCMD Register

##### 1 TPTC\_INTCMD Register (Offset = 110h) [reset = 0h]

Interrupt Command Register.

Return to [Summary Table](#)

**Table 4-2447. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0110h       |
| EDMA1         | 52A4 0110h       |

**Figure 4-804. TPTC\_INTCMD Name Register**

|          |    |    |    |    |    |     |      |
|----------|----|----|----|----|----|-----|------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25  | 24   |
| RESERVED |    |    |    |    |    |     |      |
| NONE     |    |    |    |    |    |     |      |
| 0h       |    |    |    |    |    |     |      |
| 23       | 22 | 21 | 20 | 19 | 18 | 17  | 16   |
| RESERVED |    |    |    |    |    |     |      |
| NONE     |    |    |    |    |    |     |      |
| 0h       |    |    |    |    |    |     |      |
| 15       | 14 | 13 | 12 | 11 | 10 | 9   | 8    |
| RESERVED |    |    |    |    |    |     |      |
| NONE     |    |    |    |    |    |     |      |
| 0h       |    |    |    |    |    |     |      |
| 7        | 6  | 5  | 4  | 3  | 2  | 1   | 0    |
| RESERVED |    |    |    |    |    | SET | EVAL |
| NONE     |    |    |    |    |    | W   | W    |
| 0h       |    |    |    |    |    | 0h  | 0h   |

**Table 4-2449. TPTC\_INTCMD Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                             |
|------|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                |
| 1    | SET      | W    | 0h    | Set TPTC interrupt:<br>Write of '1' to SET causes TPTC interrupt to be pulsed unconditionally.<br>Writes of '0' have no affect.                                         |
| 0    | EVAL     | W    | 0h    | Evaluate state of TPTC interrupt<br>Write of '1' to EVAL causes TPTC interrupt to be pulsed if any of the INTSTAT bits are set to '1'.<br>Writes of '0' have no affect. |

#### 4.4.2.128 TPTC\_ERRSTAT Register

##### 1 TPTC\_ERRSTAT Register (Offset = 120h) [reset = 0h]

Error Status Register.

Return to [Summary Table](#)

**Table 4-2450. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0120h       |
| EDMA1         | 52A4 0120h       |

**Figure 4-805. TPTC\_ERRSTAT Name Register**

|          |    |    |    |         |       |          |        |
|----------|----|----|----|---------|-------|----------|--------|
| 31       | 30 | 29 | 28 | 27      | 26    | 25       | 24     |
| RESERVED |    |    |    |         |       |          |        |
| NONE     |    |    |    |         |       |          |        |
| 0h       |    |    |    |         |       |          |        |
| 23       | 22 | 21 | 20 | 19      | 18    | 17       | 16     |
| RESERVED |    |    |    |         |       |          |        |
| NONE     |    |    |    |         |       |          |        |
| 0h       |    |    |    |         |       |          |        |
| 15       | 14 | 13 | 12 | 11      | 10    | 9        | 8      |
| RESERVED |    |    |    |         |       |          |        |
| NONE     |    |    |    |         |       |          |        |
| 0h       |    |    |    |         |       |          |        |
| 7        | 6  | 5  | 4  | 3       | 2     | 1        | 0      |
| RESERVED |    |    |    | MMRAERR | TRERR | RESERVED | BUSERR |
| NONE     |    |    |    | R       | R     | NONE     | R      |
| 0h       |    |    |    | 0h      | 0h    | 0h       | 0h     |

**Table 4-2452. TPTC\_ERRSTAT Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                               |
|------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                  |
| 3    | MMRAERR  | R    | 0h    | MMR Address Error:<br>MMRAERR =<br>0 : Condition not detected.<br>MMRAERR =<br>1 : User attempted to read or write to invalid address configuration memory map. [Is only be set for non-emulation accesses]. No additional error information is recorded. |
| 2    | TRERR    | R    | 0h    | TR Error:<br>TR detected that violates FIFO Mode transfer [SAM or DAM is '1'] alignment rules or has ACNT or BCNT == 0. No additional error information is recorded.                                                                                      |
| 1    | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                  |
| 0    | BUSERR   | R    | 0h    | Bus Error Event:<br>BUSERR =<br>0:Condition not detected.<br>BUSERR =<br>1:TC has detected an error code on the write response bus or read response bus. Error information is stored in Error Details Register [ERRDET].                                  |

#### 4.4.2.129 TPTC\_ERREN Register

##### 1 TPTC\_ERREN Register (Offset = 124h) [reset = 0h]

Error Enable Register.

Return to [Summary Table](#)

**Table 4-2453. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0124h       |
| EDMA1         | 52A4 0124h       |

**Figure 4-806. TPTC\_ERREN Name Register**

|          |    |    |    |         |       |          |        |
|----------|----|----|----|---------|-------|----------|--------|
| 31       | 30 | 29 | 28 | 27      | 26    | 25       | 24     |
| RESERVED |    |    |    |         |       |          |        |
| NONE     |    |    |    |         |       |          |        |
| 0h       |    |    |    |         |       |          |        |
| 23       | 22 | 21 | 20 | 19      | 18    | 17       | 16     |
| RESERVED |    |    |    |         |       |          |        |
| NONE     |    |    |    |         |       |          |        |
| 0h       |    |    |    |         |       |          |        |
| 15       | 14 | 13 | 12 | 11      | 10    | 9        | 8      |
| RESERVED |    |    |    |         |       |          |        |
| NONE     |    |    |    |         |       |          |        |
| 0h       |    |    |    |         |       |          |        |
| 7        | 6  | 5  | 4  | 3       | 2     | 1        | 0      |
| RESERVED |    |    |    | MMRAERR | TRERR | RESERVED | BUSERR |
| NONE     |    |    |    | R/W     | R/W   | NONE     | R/W    |
| 0h       |    |    |    | 0h      | 0h    | 0h       | 0h     |

**Table 4-2455. TPTC\_ERREN Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                              |
|------|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                 |
| 3    | MMRAERR  | R/W  | 0h    | Interrupt enable for ERRSTAT.MMRAERR:<br>ERREN.MMRAERR =<br>0 : BUSERR is disabled.<br>ERREN.MMRAERR =<br>1 : MMRAERR is enabled and contributes to the TPTC error interrupt generation. |
| 2    | TRERR    | R/W  | 0h    | Interrupt enable for ERRSTAT.TRERR:<br>ERREN.TRERR =<br>0 : BUSERR is disabled.<br>ERREN.TRERR =<br>1 : TRERR is enabled and contributes to the TPTC error interrupt generation.         |
| 1    | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                 |
| 0    | BUSERR   | R/W  | 0h    | Interrupt enable for ERRSTAT.BUSERR:<br>ERREN.BUSERR =<br>0 : BUSERR is disabled.<br>ERREN.BUSERR =<br>1 : BUSERR is enabled and contributes to the TPTC error interrupt generation.     |

#### 4.4.2.130 TPTC\_ERRCLR Register

##### 1 TPTC\_ERRCLR Register (Offset = 128h) [reset = 0h]

Error Clear Register.

Return to [Summary Table](#)

**Table 4-2456. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0128h       |
| EDMA1         | 52A4 0128h       |

**Figure 4-807. TPTC\_ERRCLR Name Register**

|          |    |    |    |         |       |          |        |
|----------|----|----|----|---------|-------|----------|--------|
| 31       | 30 | 29 | 28 | 27      | 26    | 25       | 24     |
| RESERVED |    |    |    |         |       |          |        |
| NONE     |    |    |    |         |       |          |        |
| 0h       |    |    |    |         |       |          |        |
| 23       | 22 | 21 | 20 | 19      | 18    | 17       | 16     |
| RESERVED |    |    |    |         |       |          |        |
| NONE     |    |    |    |         |       |          |        |
| 0h       |    |    |    |         |       |          |        |
| 15       | 14 | 13 | 12 | 11      | 10    | 9        | 8      |
| RESERVED |    |    |    |         |       |          |        |
| NONE     |    |    |    |         |       |          |        |
| 0h       |    |    |    |         |       |          |        |
| 7        | 6  | 5  | 4  | 3       | 2     | 1        | 0      |
| RESERVED |    |    |    | MMRAERR | TRERR | RESERVED | BUSERR |
| NONE     |    |    |    | W       | W     | NONE     | W      |
| 0h       |    |    |    | 0h      | 0h    | 0h       | 0h     |

**Table 4-2458. TPTC\_ERRCLR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                          |
|------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                             |
| 3    | MMRAERR  | W    | 0h    | Interrupt clear for ERRSTAT.MMRAERR:<br>ERRCLR.MMRAERR =<br>0 : Writes of '0' have no effect.<br>ERRCLR.MMRAERR =<br>1 : Write of '1' clears ERRSTAT.MMRAERR bit. Write of '1' to ERRCLR.MMRAERR does not clear the ERRDET register. |
| 2    | TRERR    | W    | 0h    | Interrupt clear for ERRSTAT.TRERR:<br>ERRCLR.TRERR =<br>0 : Writes of '0' have no effect.<br>ERRCLR.TRERR =<br>1 : Write of '1' clears ERRSTAT.TRERR bit. Write of '1' to ERRCLR.TRERR does not clear the ERRDET register.           |
| 1    | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                             |
| 0    | BUSERR   | W    | 0h    | Interrupt clear for ERRSTAT.BUSERR:<br>ERRCLR.BUSERR =<br>0 : Writes of '0' have no effect.<br>ERRCLR.BUSERR =<br>1 : Write of '1' clears ERRSTAT.BUSERR bit. Write of '1' to ERRCLR.BUSERR clears the ERRDET register.              |

#### 4.4.2.131 TPTC\_ERRDET Register

##### 1 TPTC\_ERRDET Register (Offset = 12Ch) [reset = 0h]

Error Details Register.

Return to [Summary Table](#)

**Table 4-2459. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 012Ch       |
| EDMA1         | 52A4 012Ch       |

**Figure 4-808. TPTC\_ERRDET Name Register**

|          |    |     |    |      |    |        |         |
|----------|----|-----|----|------|----|--------|---------|
| 31       | 30 | 29  | 28 | 27   | 26 | 25     | 24      |
| RESERVED |    |     |    |      |    |        |         |
| NONE     |    |     |    |      |    |        |         |
| 0h       |    |     |    |      |    |        |         |
| 23       | 22 | 21  | 20 | 19   | 18 | 17     | 16      |
| RESERVED |    |     |    |      |    | TCCHEN | TCINTEN |
| NONE     |    |     |    |      |    | R      | R       |
| 0h       |    |     |    |      |    | 0h     | 0h      |
| 15       | 14 | 13  | 12 | 11   | 10 | 9      | 8       |
| RESERVED |    | TCC |    |      |    |        |         |
| NONE     |    | R   |    |      |    |        |         |
| 0h       |    | 0h  |    |      |    |        |         |
| 7        | 6  | 5   | 4  | 3    | 2  | 1      | 0       |
| RESERVED |    |     |    | STAT |    |        |         |
| NONE     |    |     |    | R    |    |        |         |
| 0h       |    |     |    | 0h   |    |        |         |

**Table 4-2461. TPTC\_ERRDET Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                        |
| 17    | TCCHEN   | R    | 0h    | Contains the OPT.TCCHEN value programmed by the user for the Read or Write transaction that resulted in an error.                                                                                                                                                                                                                                                                                               |
| 16    | TCINTEN  | R    | 0h    | Contains the OPT.TCINTEN value programmed by the user for the Read or Write transaction that resulted in an error.                                                                                                                                                                                                                                                                                              |
| 15:14 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                        |
| 13:8  | TCC      | R    | 0h    | Transfer Complete Code: Contains the OPT.TCC value programmed by the user for the Read or Write transaction that resulted in an error.                                                                                                                                                                                                                                                                          |
| 7:4   | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                        |
| 3:0   | STAT     | R    | 0h    | Transaction Status:<br>Stores the non-zero status/error code that was detected on the read status or write status bus.<br>MS-bit effectively serves as the read vs. write error code.<br>If read status and write status are returned on the same cycle then the TC chooses non-zero version. If both are non-zero then write status is treated as higher priority.<br>Encoding of errors matches the CBA spec. |



#### 4.4.2.132 TPTC\_ERRCMD Register

##### 1 TPTC\_ERRCMD Register (Offset = 130h) [reset = 0h]

Error Command Register.

Return to [Summary Table](#)

**Table 4-2462. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0130h       |
| EDMA1         | 52A4 0130h       |

**Figure 4-809. TPTC\_ERRCMD Name Register**

|          |    |    |    |    |    |     |      |
|----------|----|----|----|----|----|-----|------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25  | 24   |
| RESERVED |    |    |    |    |    |     |      |
| NONE     |    |    |    |    |    |     |      |
| 0h       |    |    |    |    |    |     |      |
| 23       | 22 | 21 | 20 | 19 | 18 | 17  | 16   |
| RESERVED |    |    |    |    |    |     |      |
| NONE     |    |    |    |    |    |     |      |
| 0h       |    |    |    |    |    |     |      |
| 15       | 14 | 13 | 12 | 11 | 10 | 9   | 8    |
| RESERVED |    |    |    |    |    |     |      |
| NONE     |    |    |    |    |    |     |      |
| 0h       |    |    |    |    |    |     |      |
| 7        | 6  | 5  | 4  | 3  | 2  | 1   | 0    |
| RESERVED |    |    |    |    |    | SET | EVAL |
| NONE     |    |    |    |    |    | W   | W    |
| 0h       |    |    |    |    |    | 0h  | 0h   |

**Table 4-2464. TPTC\_ERRCMD Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                         |
|------|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                            |
| 1    | SET      | W    | 0h    | Set TPTC error interrupt:<br>Write of '1' to SET causes TPTC error interrupt to be pulsed unconditionally.<br>Writes of '0' have no affect.                                         |
| 0    | EVAL     | W    | 0h    | Evaluate state of TPTC error interrupt<br>Write of '1' to EVAL causes TPTC error interrupt to be pulsed if any of the ERRSTAT bits are set to '1'.<br>Writes of '0' have no affect. |

#### 4.4.2.133 TPTC\_RDRATE Register

##### 1 TPTC\_RDRATE Register (Offset = 140h) [reset = 0h]

Read Rate Register.

Return to [Summary Table](#)

**Table 4-2465. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0140h       |
| EDMA1         | 52A4 0140h       |

**Figure 4-810. TPTC\_RDRATE Name Register**

|          |    |    |    |    |        |    |    |
|----------|----|----|----|----|--------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26     | 25 | 24 |
| RESERVED |    |    |    |    |        |    |    |
| NONE     |    |    |    |    |        |    |    |
| 0h       |    |    |    |    |        |    |    |
| 23       | 22 | 21 | 20 | 19 | 18     | 17 | 16 |
| RESERVED |    |    |    |    |        |    |    |
| NONE     |    |    |    |    |        |    |    |
| 0h       |    |    |    |    |        |    |    |
| 15       | 14 | 13 | 12 | 11 | 10     | 9  | 8  |
| RESERVED |    |    |    |    |        |    |    |
| NONE     |    |    |    |    |        |    |    |
| 0h       |    |    |    |    |        |    |    |
| 7        | 6  | 5  | 4  | 3  | 2      | 1  | 0  |
| RESERVED |    |    |    |    | RDRATE |    |    |
| NONE     |    |    |    |    | R/W    |    |    |
| 0h       |    |    |    |    | 0h     |    |    |

**Table 4-2467. TPTC\_RDRATE Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                           |
|------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED | NONE | 0h    | Reserved                                                                                                                              |
| 2:0  | RDRATE   | R/W  | 0h    | Read Rate Control: Controls the number of cycles between read commands. This is a global setting that applies to all TRs for this TC. |

#### 4.4.2.134 TPTC\_POPT Register

##### 1 TPTC\_POPT Register (Offset = 200h) [reset = 0h]

Prog Set Options.

Return to [Summary Table](#)

**Table 4-2468. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0200h       |
| EDMA1         | 52A4 0200h       |

**Figure 4-811. TPTC\_POPT Name Register**

|          |        |          |         |          |      |     |     |
|----------|--------|----------|---------|----------|------|-----|-----|
| 31       | 30     | 29       | 28      | 27       | 26   | 25  | 24  |
| RESERVED |        | DBG_ID   |         | RESERVED |      |     |     |
| NONE     |        | R/W      |         | NONE     |      |     |     |
| 0h       |        | 0h       |         | 0h       |      |     |     |
| 23       | 22     | 21       | 20      | 19       | 18   | 17  | 16  |
| RESERVED | TCCHEN | RESERVED | TCINTEN | RESERVED |      | TCC |     |
| NONE     | R/W    | NONE     | R/W     | NONE     |      | R/W |     |
| 0h       | 0h     | 0h       | 0h      | 0h       |      | 0h  |     |
| 15       | 14     | 13       | 12      | 11       | 10   | 9   | 8   |
| TCC      |        |          |         | RESERVED | FWID |     |     |
| R/W      |        |          |         | NONE     | R/W  |     |     |
| 0h       |        |          |         | 0h       | 0h   |     |     |
| 7        | 6      | 5        | 4       | 3        | 2    | 1   | 0   |
| RESERVED | PRI    |          |         | RESERVED |      | DAM | SAM |
| NONE     | R/W    |          |         | NONE     |      | R/W | R/W |
| 0h       | 0h     |          |         | 0h       |      | 0h  | 0h  |

**Table 4-2470. TPTC\_POPT Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                              |
|-------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                 |
| 29:28 | DBG_ID   | R/W  | 0h    | Debug ID<br>Value driven on the read [tptc_r_dbg_channel_id] and write [tptc_w_dbg_channel_id] command bus.<br>Used at system level for trace/profiling of user selected transfers in systems that include this feature. |
| 27:23 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                 |
| 22    | TCCHEN   | R/W  | 0h    | Transfer complete chaining enable:<br>0:Transfer complete chaining is disabled.<br>1:Transfer complete chaining is enabled.                                                                                              |
| 21    | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                 |
| 20    | TCINTEN  | R/W  | 0h    | Transfer complete interrupt enable:<br>0:Transfer complete interrupt is disabled.<br>1:Transfer complete interrupt is enabled.                                                                                           |
| 19:18 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                 |
| 17:12 | TCC      | R/W  | 0h    | Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.                                                                                                                 |
| 11    | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                 |
| 10:8  | FWID     | R/W  | 0h    | FIFO width control: Applies if either SAM or DAM is set to FIFO mode.                                                                                                                                                    |

**Table 4-2470. TPTC\_POPT Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                    |
|-----|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                       |
| 6:4 | PRI      | R/W  | 0h    | Transfer Priority:<br>0:Priority 0 - Highest priority<br>1:Priority 1 ...<br>7:Priority 7 - Lowest priority                                                                    |
| 3:2 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                       |
| 1   | DAM      | R/W  | 0h    | Destination Address Mode within an array:<br>0:INCR Dst addressing within an array increments.<br>1:FIFO Dst addressing within an array wraps around upon reaching FIFO width. |
| 0   | SAM      | R/W  | 0h    | Source Address Mode within an array:<br>0:INCR Src addressing within an array increments.<br>1:FIFO Src addressing within an array wraps around upon reaching FIFO width.      |

#### 4.4.2.135 TPTC\_PSRC Register

##### 1 TPTC\_PSRC Register (Offset = 204h) [reset = 0h]

Prog Set Src Address.

Return to [Summary Table](#)

**Table 4-2471. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0204h       |
| EDMA1         | 52A4 0204h       |

**Figure 4-812. TPTC\_PSRC Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SADDR |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SADDR |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SADDR |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SADDR |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-2473. TPTC\_PSRC Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                             |
|------|-------|------|-------|-----------------------------------------|
| 31:0 | SADDR | R/W  | 0h    | Source address for Program Register Set |

#### 4.4.2.136 TPTC\_PCNT Register

##### 1 TPTC\_PCNT Register (Offset = 208h) [reset = 0h]

Prog Set Count.

Return to [Summary Table](#)

**Table 4-2474. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0208h       |
| EDMA1         | 52A4 0208h       |

**Figure 4-813. TPTC\_PCNT Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BCNT |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BCNT |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ACNT |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ACNT |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 4-2476. TPTC\_PCNT Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                               |
|-------|-------|------|-------|-------------------------------------------------------------------------------------------|
| 31:16 | BCNT  | R/W  | 0h    | B-Dimension count. Number of arrays to be transferred where each array is ACNT in length. |
| 15:0  | ACNT  | R/W  | 0h    | A-Dimension count. Number of bytes to be transferred in first dimension.                  |

#### 4.4.2.137 TPTC\_PDST Register

##### 1 TPTC\_PDST Register (Offset = 20Ch) [reset = 0h]

Prog Set Dst Address.

Return to [Summary Table](#)

**Table 4-2477. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 020Ch       |
| EDMA1         | 52A4 020Ch       |

**Figure 4-814. TPTC\_PDST Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DADDR |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DADDR |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DADDR |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DADDR |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-2479. TPTC\_PDST Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                  |
|------|-------|------|-------|----------------------------------------------|
| 31:0 | DADDR | R/W  | 0h    | Destination address for Program Register Set |

#### 4.4.2.138 TPTC\_PBDIX Register

##### 1 TPTC\_PBDIX Register (Offset = 210h) [reset = 0h]

Prog Set B-Dim Idx.

Return to [Summary Table](#)

**Table 4-2480. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0210h       |
| EDMA1         | 52A4 0210h       |

**Figure 4-815. TPTC\_PBDIX Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DBIDX |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DBIDX |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SBIDX |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SBIDX |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-2482. TPTC\_PBDIX Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                            |
|-------|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | DBIDX | R/W  | 0h    | Dest B-Idx for Program Register Set:<br>B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements]. DBIDX is always used regardless of whether DAM is Increment or FIFO mode. |
| 15:0  | SBIDX | R/W  | 0h    | Source B-Idx for Program Register Set:<br>B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements]. SBIDX is always used regardless of whether SAM is Increment or FIFO mode.         |



#### 4.4.2.139 TPTC\_PMPPRXY Register

##### 1 TPTC\_PMPPRXY Register (Offset = 214h) [reset = 0h]

Prog Set Mem Protect Proxy.

Return to [Summary Table](#)

**Table 4-2483. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0214h       |
| EDMA1         | 52A4 0214h       |

**Figure 4-816. TPTC\_PMPPRXY Name Register**

|          |    |    |    |        |    |        |      |
|----------|----|----|----|--------|----|--------|------|
| 31       | 30 | 29 | 28 | 27     | 26 | 25     | 24   |
| RESERVED |    |    |    |        |    |        |      |
| NONE     |    |    |    |        |    |        |      |
| 0h       |    |    |    |        |    |        |      |
| 23       | 22 | 21 | 20 | 19     | 18 | 17     | 16   |
| RESERVED |    |    |    |        |    |        |      |
| NONE     |    |    |    |        |    |        |      |
| 0h       |    |    |    |        |    |        |      |
| 15       | 14 | 13 | 12 | 11     | 10 | 9      | 8    |
| RESERVED |    |    |    |        |    | SECURE | PRIV |
| NONE     |    |    |    |        |    | R      | R    |
| 0h       |    |    |    |        |    | 0h     | 0h   |
| 7        | 6  | 5  | 4  | 3      | 2  | 1      | 0    |
| RESERVED |    |    |    | PRIVID |    |        |      |
| NONE     |    |    |    | R      |    |        |      |
| 0h       |    |    |    | 0h     |    |        |      |

**Table 4-2485. TPTC\_PMPPRXY Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 9     | SECURE   | R    | 0h    | Secure Level: Deprecated, always read as 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 8     | PRIV     | R    | 0h    | Privilege Level:<br>PRIV =<br>0 : User level privilege<br>PRIV =<br>1 : Supervisor level privilege<br>PMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register].<br>The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values. The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction. |
| 7:4   | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

**Table 4-2485. TPTC\_PMPPRXY Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-----|--------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0 | PRIVID | R    | 0h    | <p>Privilege ID:<br/>PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register].</p> <p>The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values. The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.</p> |

#### 4.4.2.140 TPTC\_SAOPT Register

##### 1 TPTC\_SAOPT Register (Offset = 240h) [reset = 0h]

Src Actv Set Options.

Return to [Summary Table](#)

**Table 4-2486. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0240h       |
| EDMA1         | 52A4 0240h       |

**Figure 4-817. TPTC\_SAOPT Name Register**

|          |        |          |         |          |      |     |     |
|----------|--------|----------|---------|----------|------|-----|-----|
| 31       | 30     | 29       | 28      | 27       | 26   | 25  | 24  |
| RESERVED |        | DBG_ID   |         | RESERVED |      |     |     |
| NONE     |        | R        |         | NONE     |      |     |     |
| 0h       |        | 0h       |         | 0h       |      |     |     |
| 23       | 22     | 21       | 20      | 19       | 18   | 17  | 16  |
| RESERVED | TCCHEN | RESERVED | TCINTEN | RESERVED |      | TCC |     |
| NONE     | R      | NONE     | R       | NONE     |      | R   |     |
| 0h       | 0h     | 0h       | 0h      | 0h       |      | 0h  |     |
| 15       | 14     | 13       | 12      | 11       | 10   | 9   | 8   |
| TCC      |        |          |         | RESERVED | FWID |     |     |
| R        |        |          |         | NONE     | R    |     |     |
| 0h       |        |          |         | 0h       | 0h   |     |     |
| 7        | 6      | 5        | 4       | 3        | 2    | 1   | 0   |
| RESERVED | PRI    |          |         | RESERVED |      | DAM | SAM |
| NONE     | R      |          |         | NONE     |      | R   | R   |
| 0h       | 0h     |          |         | 0h       |      | 0h  | 0h  |

**Table 4-2488. TPTC\_SAOPT Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                              |
|-------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                 |
| 29:28 | DBG_ID   | R    | 0h    | Debug ID<br>Value driven on the read [tptc_r_dbg_channel_id] and write [tptc_w_dbg_channel_id] command bus.<br>Used at system level for trace/profiling of user selected transfers in systems that include this feature. |
| 27:23 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                 |
| 22    | TCCHEN   | R    | 0h    | Transfer complete chaining enable:<br>0:Transfer complete chaining is disabled.<br>1:Transfer complete chaining is enabled.                                                                                              |
| 21    | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                 |
| 20    | TCINTEN  | R    | 0h    | Transfer complete interrupt enable:<br>0:Transfer complete interrupt is disabled.<br>1:Transfer complete interrupt is enabled.                                                                                           |
| 19:18 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                 |
| 17:12 | TCC      | R    | 0h    | Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.                                                                                                                 |
| 11    | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                 |
| 10:8  | FWID     | R    | 0h    | FIFO width control: Applies if either SAM or DAM is set to FIFO mode.                                                                                                                                                    |

**Table 4-2488. TPTC\_SAOPT Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                    |
|-----|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                       |
| 6:4 | PRI      | R    | 0h    | Transfer Priority:<br>0:Priority 0 - Highest priority<br>1:Priority 1 ...<br>7:Priority 7 - Lowest priority                                                                    |
| 3:2 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                       |
| 1   | DAM      | R    | 0h    | Destination Address Mode within an array:<br>0:INCR Dst addressing within an array increments.<br>1:FIFO Dst addressing within an array wraps around upon reaching FIFO width. |
| 0   | SAM      | R    | 0h    | Source Address Mode within an array:<br>0:INCR Src addressing within an array increments.<br>1:FIFO Src addressing within an array wraps around upon reaching FIFO width.      |

#### 4.4.2.141 TPTC\_SASRC Register

##### 1 TPTC\_SASRC Register (Offset = 244h) [reset = 0h]

Src Actv Set Src Address.

Return to [Summary Table](#)

**Table 4-2489. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0244h       |
| EDMA1         | 52A4 0244h       |

**Figure 4-818. TPTC\_SASRC Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SADDR |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SADDR |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SADDR |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SADDR |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-2491. TPTC\_SASRC Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                   |
|------|-------|------|-------|-----------------------------------------------|
| 31:0 | SADDR | R    | 0h    | Source address for Source Active Register Set |

#### 4.4.2.142 TPTC\_SACNT Register

##### 1 TPTC\_SACNT Register (Offset = 248h) [reset = 0h]

Src Actv Set A-Count.

Return to [Summary Table](#)

**Table 4-2492. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0248h       |
| EDMA1         | 52A4 0248h       |

**Figure 4-819. TPTC\_SACNT Name Register**

|          |      |    |    |    |    |    |    |
|----------|------|----|----|----|----|----|----|
| 31       | 30   | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |      |    |    |    |    |    |    |
| NONE     |      |    |    |    |    |    |    |
| 0h       |      |    |    |    |    |    |    |
| 23       | 22   | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | ACNT |    |    |    |    |    |    |
| NONE     | R    |    |    |    |    |    |    |
| 0h       | 0h   |    |    |    |    |    |    |
| 15       | 14   | 13 | 12 | 11 | 10 | 9  | 8  |
| ACNT     |      |    |    |    |    |    |    |
| R        |      |    |    |    |    |    |    |
| 0h       |      |    |    |    |    |    |    |
| 7        | 6    | 5  | 4  | 3  | 2  | 1  | 0  |
| ACNT     |      |    |    |    |    |    |    |
| R        |      |    |    |    |    |    |    |
| 0h       |      |    |    |    |    |    |    |

**Table 4-2494. TPTC\_SACNT Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                              |
|-------|----------|------|-------|--------------------------------------------------------------------------|
| 31:23 | RESERVED | NONE | 0h    | Reserved                                                                 |
| 22:0  | ACNT     | R    | 0h    | A-Dimension count. Number of bytes to be transferred in first dimension. |

#### 4.4.2.143 TPTC\_SADST Register

##### 1 TPTC\_SADST Register (Offset = 24Ch) [reset = 0h]

Src Actv Set Dst Address.

Return to [Summary Table](#)

**Table 4-2495. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 024Ch       |
| EDMA1         | 52A4 024Ch       |

**Figure 4-820. TPTC\_SADST Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DADDR |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DADDR |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DADDR |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DADDR |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-2497. TPTC\_SADST Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                        |
|------|-------|------|-------|----------------------------------------------------|
| 31:0 | DADDR | R    | 0h    | Destination address for Source Active Register Set |

#### 4.4.2.144 TPTC\_SABIDX Register

##### 1 TPTC\_SABIDX Register (Offset = 250h) [reset = 0h]

Src Actv Set B-Dim Idx.

Return to [Summary Table](#)

**Table 4-2498. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0250h       |
| EDMA1         | 52A4 0250h       |

**Figure 4-821. TPTC\_SABIDX Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DBIDX |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DBIDX |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SBIDX |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SBIDX |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-2500. TPTC\_SABIDX Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                  |
|-------|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | DBIDX | R    | 0h    | Dest B-Idx for Source Active Register Set:<br>B-Idx offset between Destination arrays: Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements]. DBIDX is always used regardless of whether DAM is Increment or FIFO mode. |
| 15:0  | SBIDX | R    | 0h    | Source B-Idx for Source Active Register Set:<br>B-Idx offset between Source arrays: Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements]. SBIDX is always used regardless of whether SAM is Increment or FIFO mode.         |



#### 4.4.2.145 TPTC\_SAMPPRXY Register

##### 1 TPTC\_SAMPPRXY Register (Offset = 254h) [reset = 0h]

Src Actv Set Mem Protect Proxy.

Return to [Summary Table](#)

**Table 4-2501. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0254h       |
| EDMA1         | 52A4 0254h       |

**Figure 4-822. TPTC\_SAMPPRXY Name Register**

|          |    |    |    |        |    |        |      |
|----------|----|----|----|--------|----|--------|------|
| 31       | 30 | 29 | 28 | 27     | 26 | 25     | 24   |
| RESERVED |    |    |    |        |    |        |      |
| NONE     |    |    |    |        |    |        |      |
| 0h       |    |    |    |        |    |        |      |
| 23       | 22 | 21 | 20 | 19     | 18 | 17     | 16   |
| RESERVED |    |    |    |        |    |        |      |
| NONE     |    |    |    |        |    |        |      |
| 0h       |    |    |    |        |    |        |      |
| 15       | 14 | 13 | 12 | 11     | 10 | 9      | 8    |
| RESERVED |    |    |    |        |    | SECURE | PRIV |
| NONE     |    |    |    |        |    | R      | R    |
| 0h       |    |    |    |        |    | 0h     | 0h   |
| 7        | 6  | 5  | 4  | 3      | 2  | 1      | 0    |
| RESERVED |    |    |    | PRIVID |    |        |      |
| NONE     |    |    |    | R      |    |        |      |
| 0h       |    |    |    | 0h     |    |        |      |

**Table 4-2503. TPTC\_SAMPPRXY Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 9     | SECURE   | R    | 0h    | Secure Level: Deprecated, always read as 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 8     | PRIV     | R    | 0h    | Privilege Level:<br>PRIV =<br>0 : User level privilege<br>PRIV =<br>1 : Supervisor level privilege<br>PMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register].<br>The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values. The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction. |
| 7:4   | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

**Table 4-2503. TPTC\_SAMPPRXY Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-----|--------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0 | PRIVID | R    | 0h    | <p>Privilege ID:<br/>PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register].</p> <p>The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values. The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.</p> |

#### 4.4.2.146 TPTC\_SACNTRLD Register

##### 1 TPTC\_SACNTRLD Register (Offset = 258h) [reset = 0h]

Src Actv Set Cnt Reload.

Return to [Summary Table](#)

**Table 4-2504. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0258h       |
| EDMA1         | 52A4 0258h       |

**Figure 4-823. TPTC\_SACNTRLD Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ACNTRLD  |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ACNTRLD  |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-2506. TPTC\_SACNTRLD Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                   |
|-------|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                      |
| 15:0  | ACNTRLD  | R    | 0h    | A-Cnt Reload value for Source Active Register set. Value copied from PCNT.ACNT: Represents the originally programmed value of ACNT.<br>The Reload value is used to reinitialize ACNT after each array is serviced [i.e. ACNT decrements to 0]. by the Src offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT bytes] |

#### 4.4.2.147 TPTC\_SASRCBREF Register

##### 1 TPTC\_SASRCBREF Register (Offset = 25Ch) [reset = 0h]

Src Actv Set Src Addr B-Reference.

Return to [Summary Table](#)

**Table 4-2507. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 025Ch       |
| EDMA1         | 52A4 025Ch       |

**Figure 4-824. TPTC\_SASRCBREF Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SADDRBREF |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SADDRBREF |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SADDRBREF |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SADDRBREF |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 4-2509. TPTC\_SASRCBREF Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                                  |
|------|-----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | SADDRBREF | R    | 0h    | Source address reference for Source Active Register Set:<br>Represents the starting address for the array currently being read.<br>The next array's starting address is calculated as the 'reference address' plus the 'source b-idx' value. |

#### 4.4.2.148 TPTC\_SADSTBREF Register

##### 1 TPTC\_SADSTBREF Register (Offset = 260h) [reset = 0h]

Src Actv Set Dst Addr B-Reference.

Return to [Summary Table](#)

**Table 4-2510. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0260h       |
| EDMA1         | 52A4 0260h       |

**Figure 4-825. TPTC\_SADSTBREF Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DADDRBREF |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DADDRBREF |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DADDRBREF |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DADDRBREF |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 4-2512. TPTC\_SADSTBREF Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                            |
|------|-----------|------|-------|----------------------------------------------------------------------------------------|
| 31:0 | DADDRBREF | R    | 0h    | Dst address reference is not applicable for Src Active Register Set. Reads return 0x0. |

#### 4.4.2.149 TPTC\_SABCNT Register

##### 1 TPTC\_SABCNT Register (Offset = 264h) [reset = 0h]

Src Actv Set B-Count.

Return to [Summary Table](#)

**Table 4-2513. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0264h       |
| EDMA1         | 52A4 0264h       |

**Figure 4-826. TPTC\_SABCNT Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| BCNT     |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| BCNT     |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-2515. TPTC\_SABCNT Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                  |
|-------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | BCNT     | R    | 0h    | B-Dimension count:<br>Number of arrays to be transferred where each array is ACNT in length.<br>Count Remaining for Src Active Register Set. Represents the amount of data remaining to be read. Initial value is copied from PCNT. TC decrements ACNT and BCNT as necessary after each read command is issued. Final value should be 0 when TR is complete. |

#### 4.4.2.150 TPTC\_DFCNTRLD Register

##### 1 TPTC\_DFCNTRLD Register (Offset = 280h) [reset = 0h]

Dst FIFO Set Cnt Reload.

Return to [Summary Table](#)

**Table 4-2516. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0280h       |
| EDMA1         | 52A4 0280h       |

**Figure 4-827. TPTC\_DFCNTRLD Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ACNTRLD  |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ACNTRLD  |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-2518. TPTC\_DFCNTRLD Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                      |
|-------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                         |
| 15:0  | ACNTRLD  | R    | 0h    | A-Cnt Reload value for Destination FIFO Register set. Value copied from PCNT.ACNT: Represents the originally programmed value of ACNT.<br>The Reload value is used to reinitialize ACNT after each array is serviced [i.e. ACNT decrements to 0]. by the Src offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT bytes] |

#### 4.4.2.151 TPTC\_DFSCBREF Register

##### 1 TPTC\_DFSCBREF Register (Offset = 284h) [reset = 0h]

Dst FIFO Set Src Addr B-Reference.

Return to [Summary Table](#)

**Table 4-2519. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0284h       |
| EDMA1         | 52A4 0284h       |

**Figure 4-828. TPTC\_DFSCBREF Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SADDRBREF |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SADDRBREF |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SADDRBREF |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SADDRBREF |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 4-2521. TPTC\_DFSCBREF Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                               |
|------|-----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | SADDRBREF | R    | 0h    | Source address reference for Destination FIFO Register Set: Represents the starting address for the array currently being read. The next array's starting address is calculated as the 'reference address' plus the 'source b-idx' value. |



#### 4.4.2.152 TPTC\_DFOPT0 Register

##### 1 TPTC\_DFOPT0 Register (Offset = 300h) [reset = 0h]

Dst FIFO Set Options.

Return to [Summary Table](#)

**Table 4-2522. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0300h       |
| EDMA1         | 52A4 0300h       |

**Figure 4-829. TPTC\_DFOPT0 Name Register**

|          |        |          |         |          |      |     |     |
|----------|--------|----------|---------|----------|------|-----|-----|
| 31       | 30     | 29       | 28      | 27       | 26   | 25  | 24  |
| RESERVED |        | DBG_ID   |         | RESERVED |      |     |     |
| NONE     |        | R        |         | NONE     |      |     |     |
| 0h       |        | 0h       |         | 0h       |      |     |     |
| 23       | 22     | 21       | 20      | 19       | 18   | 17  | 16  |
| RESERVED | TCCHEN | RESERVED | TCINTEN | RESERVED |      | TCC |     |
| NONE     | R      | NONE     | R       | NONE     |      | R   |     |
| 0h       | 0h     | 0h       | 0h      | 0h       |      | 0h  |     |
| 15       | 14     | 13       | 12      | 11       | 10   | 9   | 8   |
| TCC      |        |          |         | RESERVED | FWID |     |     |
| R        |        |          |         | NONE     | R    |     |     |
| 0h       |        |          |         | 0h       | 0h   |     |     |
| 7        | 6      | 5        | 4       | 3        | 2    | 1   | 0   |
| RESERVED | PRI    |          |         | RESERVED |      | DAM | SAM |
| NONE     | R      |          |         | NONE     |      | R   | R   |
| 0h       | 0h     |          |         | 0h       |      | 0h  | 0h  |

**Table 4-2524. TPTC\_DFOPT0 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                            |
|-------|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                               |
| 29:28 | DBG_ID   | R    | 0h    | Debug ID<br>Value driven on the read [tpc_r_dbg_channel_id] and write [tpc_w_dbg_channel_id] command bus.<br>Used at system level for trace/profiling of user selected transfers in systems that include this feature. |
| 27:23 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                               |
| 22    | TCCHEN   | R    | 0h    | Transfer complete chaining enable:<br>0:Transfer complete chaining is disabled.<br>1:Transfer complete chaining is enabled.                                                                                            |
| 21    | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                               |
| 20    | TCINTEN  | R    | 0h    | Transfer complete interrupt enable:<br>0:Transfer complete interrupt is disabled.<br>1:Transfer complete interrupt is enabled.                                                                                         |
| 19:18 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                               |
| 17:12 | TCC      | R    | 0h    | Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.                                                                                                               |
| 11    | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                               |
| 10:8  | FWID     | R    | 0h    | FIFO width control: Applies if either SAM or DAM is set to FIFO mode.                                                                                                                                                  |

**Table 4-2524. TPTC\_DFOPT0 Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                    |
|-----|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                       |
| 6:4 | PRI      | R    | 0h    | Transfer Priority:<br>0:Priority 0 - Highest priority<br>1:Priority 1 ...<br>7:Priority 7 - Lowest priority                                                                    |
| 3:2 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                       |
| 1   | DAM      | R    | 0h    | Destination Address Mode within an array:<br>0:INCR Dst addressing within an array increments.<br>1:FIFO Dst addressing within an array wraps around upon reaching FIFO width. |
| 0   | SAM      | R    | 0h    | Source Address Mode within an array:<br>0:INCR Src addressing within an array increments.<br>1:FIFO Src addressing within an array wraps around upon reaching FIFO width.      |

#### 4.4.2.153 TPTC\_DF SRC0 Register

##### 1 TPTC\_DF SRC0 Register (Offset = 304h) [reset = 0h]

Dst FIFO Set Src Address.

Return to [Summary Table](#)

**Table 4-2525. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0304h       |
| EDMA1         | 52A4 0304h       |

**Figure 4-830. TPTC\_DF SRC0 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SADDR |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SADDR |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SADDR |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SADDR |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-2527. TPTC\_DF SRC0 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                   |
|------|-------|------|-------|-------------------------------------------------------------------------------|
| 31:0 | SADDR | R    | 0h    | Source address is not applicable for Dst FIFO Register Set: Reads return 0x0. |

#### 4.4.2.154 TPTC\_DFACNT0 Register

##### 1 TPTC\_DFACNT0 Register (Offset = 308h) [reset = 0h]

Dst FIFO Set A-Count.

Return to [Summary Table](#)

**Table 4-2528. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0308h       |
| EDMA1         | 52A4 0308h       |

**Figure 4-831. TPTC\_DFACNT0 Name Register**

|          |      |    |    |    |    |    |    |
|----------|------|----|----|----|----|----|----|
| 31       | 30   | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |      |    |    |    |    |    |    |
| NONE     |      |    |    |    |    |    |    |
| 0h       |      |    |    |    |    |    |    |
| 23       | 22   | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | ACNT |    |    |    |    |    |    |
| NONE     | R    |    |    |    |    |    |    |
| 0h       | 0h   |    |    |    |    |    |    |
| 15       | 14   | 13 | 12 | 11 | 10 | 9  | 8  |
| ACNT     |      |    |    |    |    |    |    |
| R        |      |    |    |    |    |    |    |
| 0h       |      |    |    |    |    |    |    |
| 7        | 6    | 5  | 4  | 3  | 2  | 1  | 0  |
| ACNT     |      |    |    |    |    |    |    |
| R        |      |    |    |    |    |    |    |
| 0h       |      |    |    |    |    |    |    |

**Table 4-2530. TPTC\_DFACNT0 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                              |
|-------|----------|------|-------|--------------------------------------------------------------------------|
| 31:23 | RESERVED | NONE | 0h    | Reserved                                                                 |
| 22:0  | ACNT     | R    | 0h    | A-Dimension count. Number of bytes to be transferred in first dimension. |

#### 4.4.2.155 TPTC\_DFDST0 Register

##### 1 TPTC\_DFDST0 Register (Offset = 30Ch) [reset = 0h]

Dst FIFO Set Dst Address.

Return to [Summary Table](#)

**Table 4-2531. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 030Ch       |
| EDMA1         | 52A4 030Ch       |

**Figure 4-832. TPTC\_DFDST0 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DADDR |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DADDR |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DADDR |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DADDR |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-2533. TPTC\_DFDST0 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                 |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | DADDR | R    | 0h    | Destination address for Dst FIFO Register Set:<br>Initial value is copied from PDST.DADDR.<br>TC updates value according to destination addressing mode [OPT.SAM] and/or dest index value [BIDX.DBIDX] after each write command is issued.<br>When a TR is complete the final value should be the address of the last write command issued. |

#### 4.4.2.156 TPTC\_DFBIDX0 Register

##### 1 TPTC\_DFBIDX0 Register (Offset = 310h) [reset = 0h]

Dst FIFO Set B-Dim Idx.

Return to [Summary Table](#)

**Table 4-2534. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0310h       |
| EDMA1         | 52A4 0310h       |

**Figure 4-833. TPTC\_DFBIDX0 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DBIDX |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DBIDX |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SBIDX |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SBIDX |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-2536. TPTC\_DFBIDX0 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                             |
|-------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | DBIDX | R    | 0h    | Dest B-Idx for Dest FIFO Register Set.<br>Value copied from PBIDX: B-Idx offset between Destination arrays:<br>Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements].<br>DBIDX is always used regardless of whether DAM is Increment or FIFO mode. |
| 15:0  | SBIDX | R    | 0h    | Src B-Idx for Dest FIFO Register Set.<br>Value copied from PBIDX: B-Idx offset between Source arrays:<br>Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements].<br>SBIDX is always used regardless of whether SAM is Increment or FIFO mode.            |

#### 4.4.2.157 TPTC\_DFMPPRXY0 Register

##### 1 TPTC\_DFMPPRXY0 Register (Offset = 314h) [reset = 0h]

Dst FIFO Set Mem Protect Proxy.

Return to [Summary Table](#)

**Table 4-2537. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0314h       |
| EDMA1         | 52A4 0314h       |

**Figure 4-834. TPTC\_DFMPPRXY0 Name Register**

|          |    |    |    |        |    |        |      |
|----------|----|----|----|--------|----|--------|------|
| 31       | 30 | 29 | 28 | 27     | 26 | 25     | 24   |
| RESERVED |    |    |    |        |    |        |      |
| NONE     |    |    |    |        |    |        |      |
| 0h       |    |    |    |        |    |        |      |
| 23       | 22 | 21 | 20 | 19     | 18 | 17     | 16   |
| RESERVED |    |    |    |        |    |        |      |
| NONE     |    |    |    |        |    |        |      |
| 0h       |    |    |    |        |    |        |      |
| 15       | 14 | 13 | 12 | 11     | 10 | 9      | 8    |
| RESERVED |    |    |    |        |    | SECURE | PRIV |
| NONE     |    |    |    |        |    | R      | R    |
| 0h       |    |    |    |        |    | 0h     | 0h   |
| 7        | 6  | 5  | 4  | 3      | 2  | 1      | 0    |
| RESERVED |    |    |    | PRIVID |    |        |      |
| NONE     |    |    |    | R      |    |        |      |
| 0h       |    |    |    | 0h     |    |        |      |

**Table 4-2539. TPTC\_DFMPPRXY0 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 9     | SECURE   | R    | 0h    | Secure Level: Deprecated, always read as 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 8     | PRIV     | R    | 0h    | Privilege Level:<br>PRIV =<br>0 : User level privilege<br>PRIV =<br>1 : Supervisor level privilege<br>PMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register].<br>The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values. The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction. |
| 7:4   | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

**Table 4-2539. TPTC\_DFMPPRXY0 Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-----|--------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0 | PRIVID | R    | 0h    | <p>Privilege ID:<br/>PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register].</p> <p>The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values. The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.</p> |



#### 4.4.2.158 TPTC\_DFBCNT0 Register

##### 1 TPTC\_DFBCNT0 Register (Offset = 318h) [reset = 0h]

Dst FIFO Set B-Count.

Return to [Summary Table](#)

**Table 4-2540. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0318h       |
| EDMA1         | 52A4 0318h       |

**Figure 4-835. TPTC\_DFBCNT0 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| BCNT     |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| BCNT     |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-2542. TPTC\_DFBCNT0 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                      |
|-------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                         |
| 15:0  | BCNT     | R    | 0h    | B-Count Remaining for Dst Register Set:<br>Number of arrays to be transferred where each array is ACNT in length.<br>Represents the amount of data remaining to be written.<br>Initial value is copied from PCNT.<br>TC decrements ACNT and BCNT as necessary after each write dataphase is issued. Final value should be 0 when TR is complete. |

#### 4.4.2.159 TPTC\_DFOPT1 Register

##### 1 TPTC\_DFOPT1 Register (Offset = 340h) [reset = 0h]

Dst FIFO Set Options.

Return to [Summary Table](#)

**Table 4-2543. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0340h       |
| EDMA1         | 52A4 0340h       |

**Figure 4-836. TPTC\_DFOPT1 Name Register**

|          |        |          |         |          |      |     |     |
|----------|--------|----------|---------|----------|------|-----|-----|
| 31       | 30     | 29       | 28      | 27       | 26   | 25  | 24  |
| RESERVED |        | DBG_ID   |         | RESERVED |      |     |     |
| NONE     |        | R        |         | NONE     |      |     |     |
| 0h       |        | 0h       |         | 0h       |      |     |     |
| 23       | 22     | 21       | 20      | 19       | 18   | 17  | 16  |
| RESERVED | TCCHEN | RESERVED | TCINTEN | RESERVED |      | TCC |     |
| NONE     | R      | NONE     | R       | NONE     |      | R   |     |
| 0h       | 0h     | 0h       | 0h      | 0h       |      | 0h  |     |
| 15       | 14     | 13       | 12      | 11       | 10   | 9   | 8   |
| TCC      |        |          |         | RESERVED | FWID |     |     |
| R        |        |          |         | NONE     | R    |     |     |
| 0h       |        |          |         | 0h       | 0h   |     |     |
| 7        | 6      | 5        | 4       | 3        | 2    | 1   | 0   |
| RESERVED | PRI    |          |         | RESERVED |      | DAM | SAM |
| NONE     | R      |          |         | NONE     |      | R   | R   |
| 0h       | 0h     |          |         | 0h       |      | 0h  | 0h  |

**Table 4-2545. TPTC\_DFOPT1 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                              |
|-------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                 |
| 29:28 | DBG_ID   | R    | 0h    | Debug ID<br>Value driven on the read [tptc_r_dbg_channel_id] and write [tptc_w_dbg_channel_id] command bus.<br>Used at system level for trace/profiling of user selected transfers in systems that include this feature. |
| 27:23 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                 |
| 22    | TCCHEN   | R    | 0h    | Transfer complete chaining enable:<br>0:Transfer complete chaining is disabled.<br>1:Transfer complete chaining is enabled.                                                                                              |
| 21    | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                 |
| 20    | TCINTEN  | R    | 0h    | Transfer complete interrupt enable:<br>0:Transfer complete interrupt is disabled.<br>1:Transfer complete interrupt is enabled.                                                                                           |
| 19:18 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                 |
| 17:12 | TCC      | R    | 0h    | Transfer Complete Code: The 6-bit code is used to set the relevant bit in CER or IPR of the TPCC module.                                                                                                                 |
| 11    | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                 |
| 10:8  | FWID     | R    | 0h    | FIFO width control: Applies if either SAM or DAM is set to FIFO mode.                                                                                                                                                    |

**Table 4-2545. TPTC\_DFOPT1 Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                    |
|-----|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                       |
| 6:4 | PRI      | R    | 0h    | Transfer Priority:<br>0:Priority 0 - Highest priority<br>1:Priority 1 ...<br>7:Priority 7 - Lowest priority                                                                    |
| 3:2 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                       |
| 1   | DAM      | R    | 0h    | Destination Address Mode within an array:<br>0:INCR Dst addressing within an array increments.<br>1:FIFO Dst addressing within an array wraps around upon reaching FIFO width. |
| 0   | SAM      | R    | 0h    | Source Address Mode within an array:<br>0:INCR Src addressing within an array increments.<br>1:FIFO Src addressing within an array wraps around upon reaching FIFO width.      |

#### 4.4.2.160 TPTC\_DF SRC1 Register

##### 1 TPTC\_DF SRC1 Register (Offset = 344h) [reset = 0h]

Dst FIFO Set Src Address.

Return to [Summary Table](#)

**Table 4-2546. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0344h       |
| EDMA1         | 52A4 0344h       |

**Figure 4-837. TPTC\_DF SRC1 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SADDR |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SADDR |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SADDR |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SADDR |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-2548. TPTC\_DF SRC1 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                   |
|------|-------|------|-------|-------------------------------------------------------------------------------|
| 31:0 | SADDR | R    | 0h    | Source address is not applicable for Dst FIFO Register Set: Reads return 0x0. |

#### 4.4.2.161 TPTC\_DFACNT1 Register

##### 1 TPTC\_DFACNT1 Register (Offset = 348h) [reset = 0h]

Dst FIFO Set A-Count.

Return to [Summary Table](#)

**Table 4-2549. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0348h       |
| EDMA1         | 52A4 0348h       |

**Figure 4-838. TPTC\_DFACNT1 Name Register**

|          |      |    |    |    |    |    |    |
|----------|------|----|----|----|----|----|----|
| 31       | 30   | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |      |    |    |    |    |    |    |
| NONE     |      |    |    |    |    |    |    |
| 0h       |      |    |    |    |    |    |    |
| 23       | 22   | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED | ACNT |    |    |    |    |    |    |
| NONE     | R    |    |    |    |    |    |    |
| 0h       | 0h   |    |    |    |    |    |    |
| 15       | 14   | 13 | 12 | 11 | 10 | 9  | 8  |
| ACNT     |      |    |    |    |    |    |    |
| R        |      |    |    |    |    |    |    |
| 0h       |      |    |    |    |    |    |    |
| 7        | 6    | 5  | 4  | 3  | 2  | 1  | 0  |
| ACNT     |      |    |    |    |    |    |    |
| R        |      |    |    |    |    |    |    |
| 0h       |      |    |    |    |    |    |    |

**Table 4-2551. TPTC\_DFACNT1 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                              |
|-------|----------|------|-------|--------------------------------------------------------------------------|
| 31:23 | RESERVED | NONE | 0h    | Reserved                                                                 |
| 22:0  | ACNT     | R    | 0h    | A-Dimension count. Number of bytes to be transferred in first dimension. |

#### 4.4.2.162 TPTC\_DFDST1 Register

##### 1 TPTC\_DFDST1 Register (Offset = 34Ch) [reset = 0h]

Dst FIFO Set Dst Address.

Return to [Summary Table](#)

**Table 4-2552. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 034Ch       |
| EDMA1         | 52A4 034Ch       |

**Figure 4-839. TPTC\_DFDST1 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DADDR |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DADDR |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DADDR |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DADDR |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-2554. TPTC\_DFDST1 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                 |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | DADDR | R    | 0h    | Destination address for Dst FIFO Register Set:<br>Initial value is copied from PDST.DADDR.<br>TC updates value according to destination addressing mode [OPT.SAM] and/or dest index value [BIDX.DBIDX] after each write command is issued.<br>When a TR is complete the final value should be the address of the last write command issued. |

#### 4.4.2.163 TPTC\_DFBIDX1 Register

##### 1 TPTC\_DFBIDX1 Register (Offset = 350h) [reset = 0h]

Dst FIFO Set B-Dim Idx.

Return to [Summary Table](#)

**Table 4-2555. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0350h       |
| EDMA1         | 52A4 0350h       |

**Figure 4-840. TPTC\_DFBIDX1 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DBIDX |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DBIDX |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SBIDX |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SBIDX |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 4-2557. TPTC\_DFBIDX1 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                             |
|-------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | DBIDX | R    | 0h    | Dest B-Idx for Dest FIFO Register Set.<br>Value copied from PBIDX: B-Idx offset between Destination arrays:<br>Represents the offset in bytes between the starting address of each destination array [recall that there are BCNT arrays of ACNT elements].<br>DBIDX is always used regardless of whether DAM is Increment or FIFO mode. |
| 15:0  | SBIDX | R    | 0h    | Src B-Idx for Dest FIFO Register Set.<br>Value copied from PBIDX: B-Idx offset between Source arrays:<br>Represents the offset in bytes between the starting address of each source array [recall that there are BCNT arrays of ACNT elements].<br>SBIDX is always used regardless of whether SAM is Increment or FIFO mode.            |

#### 4.4.2.164 TPTC\_DFMPPRXY1 Register

##### 1 TPTC\_DFMPPRXY1 Register (Offset = 354h) [reset = 0h]

Dst FIFO Set Mem Protect Proxy.

Return to [Summary Table](#)

**Table 4-2558. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0354h       |
| EDMA1         | 52A4 0354h       |

**Figure 4-841. TPTC\_DFMPPRXY1 Name Register**

|          |    |    |    |        |    |        |      |
|----------|----|----|----|--------|----|--------|------|
| 31       | 30 | 29 | 28 | 27     | 26 | 25     | 24   |
| RESERVED |    |    |    |        |    |        |      |
| NONE     |    |    |    |        |    |        |      |
| 0h       |    |    |    |        |    |        |      |
| 23       | 22 | 21 | 20 | 19     | 18 | 17     | 16   |
| RESERVED |    |    |    |        |    |        |      |
| NONE     |    |    |    |        |    |        |      |
| 0h       |    |    |    |        |    |        |      |
| 15       | 14 | 13 | 12 | 11     | 10 | 9      | 8    |
| RESERVED |    |    |    |        |    | SECURE | PRIV |
| NONE     |    |    |    |        |    | R      | R    |
| 0h       |    |    |    |        |    | 0h     | 0h   |
| 7        | 6  | 5  | 4  | 3      | 2  | 1      | 0    |
| RESERVED |    |    |    | PRIVID |    |        |      |
| NONE     |    |    |    | R      |    |        |      |
| 0h       |    |    |    | 0h     |    |        |      |

**Table 4-2560. TPTC\_DFMPPRXY1 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 9     | SECURE   | R    | 0h    | Secure Level: Deprecated, always read as 0.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 8     | PRIV     | R    | 0h    | Privilege Level:<br>PRIV =<br>0 : User level privilege<br>PRIV =<br>1 : Supervisor level privilege<br>PMPPRXY.PRIV is always updated with the value from the configuration bus privilege field on any/every write to Program Set BIDX Register [trigger register].<br>The PRIV value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values. The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the PRIV of the external host that sets up the DMA transaction. |
| 7:4   | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |



**Table 4-2560. TPTC\_DFMPPRXY1 Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-----|--------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0 | PRIVID | R    | 0h    | <p>Privilege ID:<br/>PMPPRXY.PRIVID is always updated with the value from configuration bus privilege ID field on any/every write to Program Set BIDX Register [trigger register].</p> <p>The PRIVID value for the SA Set and DF Set are copied from the value in the Program set along with the remainder of the parameter values. The privilege ID is issued on the VBusM read and write command bus such that the target endpoints can perform memory protection checks based on the privid of the external host that sets up the DMA transaction.</p> |

#### 4.4.2.165 TPTC\_DFBCNT1 Register

##### 1 TPTC\_DFBCNT1 Register (Offset = 358h) [reset = 0h]

Dst FIFO Set B-Count.

Return to [Summary Table](#)

**Table 4-2561. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EDMA0         | 52A6 0358h       |
| EDMA1         | 52A4 0358h       |

**Figure 4-842. TPTC\_DFBCNT1 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| BCNT     |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| BCNT     |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 4-2563. TPTC\_DFBCNT1 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                      |
|-------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                         |
| 15:0  | BCNT     | R    | 0h    | B-Count Remaining for Dst Register Set:<br>Number of arrays to be transferred where each array is ACNT in length.<br>Represents the amount of data remaining to be written.<br>Initial value is copied from PCNT.<br>TC decrements ACNT and BCNT as necessary after each write dataphase is issued. Final value should be 0 when TR is complete. |

## 4.5 EDMA\_TRIGXBAR\_INTR

### EDMA\_TRIGXBAR\_INTR

#### 4.5.1 EDMA\_TRIGXBAR\_INTR Summaries

#### EDMA\_TRIGXBAR\_INTR Summaries

**Table 4-2564. EDMA\_TRIGXBAR\_INTR Registers, Base Address=52E0 1000h, Length=2048**

| Offset | Length | Register Name                                | EDMA_TRIGXBAR_INTR Physical Address |
|--------|--------|----------------------------------------------|-------------------------------------|
| 0h     | 32     | <a href="#">EDMA_TRIGXBAR_INTR_PID</a>       | 52E0 1000h                          |
| 4h     | 32     | <a href="#">EDMA_TRIGXBAR_INTR_MUXCNTL_J</a> | 52E0 1004h + formula                |

#### 4.5.2 EDMA\_TRIGXBAR\_INTR Registers

#### EDMA\_TRIGXBAR\_INTR Registers

#### 4.5.2.1 EDMA\_TRIGXBAR\_INTR\_PID Register

##### 1 EDMA\_TRIGXBAR\_INTR\_PID Register (Offset = 0h) [reset = 66948100h]

Identification register.

Return to [Summary Table](#)

**Table 4-2565. Instance Table**

| Instance Name      | Physical Address |
|--------------------|------------------|
| EDMA_TRIGXBAR_INTR | 52E0 1000h       |

**Figure 4-843. EDMA\_TRIGXBAR\_INTR\_PID Name Register**

|          |    |        |    |          |        |    |    |
|----------|----|--------|----|----------|--------|----|----|
| 31       | 30 | 29     | 28 | 27       | 26     | 25 | 24 |
| SCHEME   |    | BU     |    | FUNCTION |        |    |    |
| R        |    | R      |    | R        |        |    |    |
| 1h       |    | 2h     |    | 694h     |        |    |    |
| 23       | 22 | 21     | 20 | 19       | 18     | 17 | 16 |
| FUNCTION |    |        |    |          |        |    |    |
| R        |    |        |    |          |        |    |    |
| 694h     |    |        |    |          |        |    |    |
| 15       | 14 | 13     | 12 | 11       | 10     | 9  | 8  |
| RTLVER   |    |        |    |          | MAJREV |    |    |
| R        |    |        |    |          | R      |    |    |
| 10h      |    |        |    |          | 1h     |    |    |
| 7        | 6  | 5      | 4  | 3        | 2      | 1  | 0  |
| CUSTOM   |    | MINREV |    |          |        |    |    |
| R        |    | R      |    |          |        |    |    |
| 0h       |    | 0h     |    |          |        |    |    |

**Table 4-2567. EDMA\_TRIGXBAR\_INTR\_PID Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description   |
|-------|----------|------|-------|---------------|
| 31:30 | SCHEME   | R    | 1h    | Scheme        |
| 29:28 | BU       | R    | 2h    | bu            |
| 27:16 | FUNCTION | R    | 694h  | function      |
| 15:11 | RTLVER   | R    | 10h   | Rtl version   |
| 10:8  | MAJREV   | R    | 1h    | major version |
| 7:6   | CUSTOM   | R    | 0h    | custom id     |
| 5:0   | MINREV   | R    | 0h    | minor version |

#### 4.5.2.2 EDMA\_TRIGXBAR\_INTR\_MUXCNTL\_j Register

##### 1 EDMA\_TRIGXBAR\_INTR\_MUXCNTL\_j Register (Offset = 4h + formula) [reset = 0h]

Interrupt mux control register.

Return to [Summary Table](#)

Offset = (j \* 4h); where j = 0 to 63d

**Table 4-2568. Instance Table**

| Instance Name      | Physical Address     |
|--------------------|----------------------|
| EDMA_TRIGXBAR_INTR | 52E0 1004h + formula |

**Figure 4-844. EDMA\_TRIGXBAR\_INTR\_MUXCNTL\_j Name Register**

|          |    |    |    |    |    |    |            |
|----------|----|----|----|----|----|----|------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24         |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16         |
| RESERVED |    |    |    |    |    |    | INT_ENABLE |
| NONE     |    |    |    |    |    |    | R/W        |
| 0h       |    |    |    |    |    |    | 0h         |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8          |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0          |
| MUX_CNTL |    |    |    |    |    |    |            |
| R/W      |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |

**Table 4-2570. EDMA\_TRIGXBAR\_INTR\_MUXCNTL\_j Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                           |
|-------|------------|------|-------|-------------------------------------------------------|
| 31:17 | RESERVED   | NONE | 0h    | Reserved                                              |
| 16    | INT_ENABLE | R/W  | 0h    | Interrupt j Output Enable.<br>0 Disabled<br>1 Enabled |
| 15:8  | RESERVED   | NONE | 0h    | Reserved                                              |
| 7:0   | MUX_CNTL   | R/W  | 0h    | Mux Control for Interrupt j.                          |

## Chapter 5

# System-on-chip (SoC) Registers

---



The System-on-chip (SoC) module registers are described in the following sections.

---

### Note

All images except for VIM images use hexadecimal. VIM uses decimal due to legacy documentation.

---

## 5.1 CPSW

### CPSW

#### 5.1.1 CPSW Summaries

#### CPSW Summaries

**Table 5-1. CPSW Registers, Base Address=5280 0000h, Length=2097152**

| Offset | Length | Register Name                                                  | CPSW0 Physical Address |
|--------|--------|----------------------------------------------------------------|------------------------|
| 0h     | 32     | <a href="#">CPSW_IDVER_REG</a>                                 | 5280 0000h             |
| 4h     | 32     | <a href="#">CPSW_SS_SYNCE_COUNT_REG</a>                        | 5280 0004h             |
| 8h     | 32     | <a href="#">CPSW_SS_SYNCE_MUX_REG</a>                          | 5280 0008h             |
| Ch     | 32     | <a href="#">CPSW_SS_CONTROL_REG</a>                            | 5280 000Ch             |
| 18h    | 32     | <a href="#">CPSW_SS_INT_CONTROL_REG</a>                        | 5280 0018h             |
| 1Ch    | 32     | <a href="#">CPSW_SS_STATUS_REG</a>                             | 5280 001Ch             |
| 20h    | 32     | <a href="#">CPSW_SUBSYSTEM_CONFIG_REG</a>                      | 5280 0020h             |
| 30h    | 32     | <a href="#">CPSW_RGMII1_STATUS_REG</a>                         | 5280 0030h             |
| 34h    | 32     | <a href="#">CPSW_RGMII2_STATUS_REG</a>                         | 5280 0034h             |
| F00h   | 32     | <a href="#">CPSW_MDIO_VERSION_REG</a>                          | 5280 0F00h             |
| F04h   | 32     | <a href="#">CPSW_MDIO_CONTROL_REG</a>                          | 5280 0F04h             |
| F08h   | 32     | <a href="#">CPSW_MDIO_ALIVE_REG</a>                            | 5280 0F08h             |
| F0Ch   | 32     | <a href="#">CPSW_MDIO_LINK_REG</a>                             | 5280 0F0Ch             |
| F10h   | 32     | <a href="#">CPSW_MDIO_LINK_INT_RAW_REG</a>                     | 5280 0F10h             |
| F14h   | 32     | <a href="#">CPSW_MDIO_LINK_INT_MASKED_REG</a>                  | 5280 0F14h             |
| F18h   | 32     | <a href="#">CPSW_MDIO_LINK_INT_MASK_SET_REG</a>                | 5280 0F18h             |
| F1Ch   | 32     | <a href="#">CPSW_MDIO_LINK_INT_MASK_CLEAR_REG</a>              | 5280 0F1Ch             |
| F20h   | 32     | <a href="#">CPSW_MDIO_USER_INT_RAW_REG</a>                     | 5280 0F20h             |
| F24h   | 32     | <a href="#">CPSW_MDIO_USER_INT_MASKED_REG</a>                  | 5280 0F24h             |
| F28h   | 32     | <a href="#">CPSW_MDIO_USER_INT_MASK_SET_REG</a>                | 5280 0F28h             |
| F2Ch   | 32     | <a href="#">CPSW_MDIO_USER_INT_MASK_CLEAR_REG</a>              | 5280 0F2Ch             |
| F30h   | 32     | <a href="#">CPSW_MDIO_MANUAL_IF_REG</a>                        | 5280 0F30h             |
| F34h   | 32     | <a href="#">CPSW_MDIO_POLL_REG</a>                             | 5280 0F34h             |
| F38h   | 32     | <a href="#">CPSW_MDIO_POLL_EN_REG</a>                          | 5280 0F38h             |
| F3Ch   | 32     | <a href="#">CPSW_MDIO_CLAUS45_REG</a>                          | 5280 0F3Ch             |
| F40h   | 32     | <a href="#">CPSW_MDIO_USER_ADDR0_REG</a>                       | 5280 0F40h             |
| F44h   | 32     | <a href="#">CPSW_MDIO_USER_ADDR1_REG</a>                       | 5280 0F44h             |
| F80h   | 32     | <a href="#">CPSW_MDIO_USER_GROUP_USER_ACCESS_REG_K</a>         | 5280 0F80h + formula   |
| F84h   | 32     | <a href="#">CPSW_MDIO_USER_GROUP_USER_PHY_SEL_REG_K</a>        | 5280 0F84h + formula   |
| 1800h  | 32     | <a href="#">CPSW_REGS_INT_SS_C0_TH_THRESH_PULSE_EN_REG</a>     | 5280 1800h             |
| 1804h  | 32     | <a href="#">CPSW_REGS_INT_SS_C0_TH_PULSE_EN_REG</a>            | 5280 1804h             |
| 1808h  | 32     | <a href="#">CPSW_REGS_INT_SS_C0_FH_PULSE_EN_REG</a>            | 5280 1808h             |
| 180Ch  | 32     | <a href="#">CPSW_REGS_INT_SS_C0_MISC_EN_REG</a>                | 5280 180Ch             |
| 1810h  | 32     | <a href="#">CPSW_REGS_INT_SS_C0_TH_THRESH_PULSE_STATUS_REG</a> | 5280 1810h             |
| 1814h  | 32     | <a href="#">CPSW_REGS_INT_SS_C0_TH_PULSE_STATUS_REG</a>        | 5280 1814h             |
| 1818h  | 32     | <a href="#">CPSW_REGS_INT_SS_C0_FH_PULSE_STATUS_REG</a>        | 5280 1818h             |

**Table 5-1. CPSW Registers, Base Address=5280 0000h, Length=2097152 (continued)**

| Offset | Length | Register Name                                  | CPSW0 Physical Address |
|--------|--------|------------------------------------------------|------------------------|
| 181Ch  | 32     | CPSW_REGS_INT_SS_C0_MISC_STATUS_REG            | 5280 181Ch             |
| 1820h  | 32     | CPSW_REGS_INT_SS_C0_TH_IMAX_REG                | 5280 1820h             |
| 1824h  | 32     | CPSW_REGS_INT_SS_C0_FH_IMAX_REG                | 5280 1824h             |
| 1840h  | 32     | CPSW_REGS_INT_SS_C1_TH_THRESH_PULSE_EN_REG     | 5280 1840h             |
| 1844h  | 32     | CPSW_REGS_INT_SS_C1_TH_PULSE_EN_REG            | 5280 1844h             |
| 1848h  | 32     | CPSW_REGS_INT_SS_C1_FH_PULSE_EN_REG            | 5280 1848h             |
| 184Ch  | 32     | CPSW_REGS_INT_SS_C1_MISC_EN_REG                | 5280 184Ch             |
| 1850h  | 32     | CPSW_REGS_INT_SS_C1_TH_THRESH_PULSE_STATUS_REG | 5280 1850h             |
| 1854h  | 32     | CPSW_REGS_INT_SS_C1_TH_PULSE_STATUS_REG        | 5280 1854h             |
| 1858h  | 32     | CPSW_REGS_INT_SS_C1_FH_PULSE_STATUS_REG        | 5280 1858h             |
| 185Ch  | 32     | CPSW_REGS_INT_SS_C1_MISC_STATUS_REG            | 5280 185Ch             |
| 1860h  | 32     | CPSW_REGS_INT_SS_C1_TH_IMAX_REG                | 5280 1860h             |
| 1864h  | 32     | CPSW_REGS_INT_SS_C1_FH_IMAX_REG                | 5280 1864h             |
| 1880h  | 32     | CPSW_REGS_INT_SS_C2_TH_THRESH_PULSE_EN_REG     | 5280 1880h             |
| 1884h  | 32     | CPSW_REGS_INT_SS_C2_TH_PULSE_EN_REG            | 5280 1884h             |
| 1888h  | 32     | CPSW_REGS_INT_SS_C2_FH_PULSE_EN_REG            | 5280 1888h             |
| 188Ch  | 32     | CPSW_REGS_INT_SS_C2_MISC_EN_REG                | 5280 188Ch             |
| 1890h  | 32     | CPSW_REGS_INT_SS_C2_TH_THRESH_PULSE_STATUS_REG | 5280 1890h             |
| 1894h  | 32     | CPSW_REGS_INT_SS_C2_TH_PULSE_STATUS_REG        | 5280 1894h             |
| 1898h  | 32     | CPSW_REGS_INT_SS_C2_FH_PULSE_STATUS_REG        | 5280 1898h             |
| 189Ch  | 32     | CPSW_REGS_INT_SS_C2_MISC_STATUS_REG            | 5280 189Ch             |
| 18A0h  | 32     | CPSW_REGS_INT_SS_C2_TH_IMAX_REG                | 5280 18A0h             |
| 18A4h  | 32     | CPSW_REGS_INT_SS_C2_FH_IMAX_REG                | 5280 18A4h             |
| 18C0h  | 32     | CPSW_REGS_INT_SS_C3_TH_THRESH_PULSE_EN_REG     | 5280 18C0h             |
| 18C4h  | 32     | CPSW_REGS_INT_SS_C3_TH_PULSE_EN_REG            | 5280 18C4h             |
| 18C8h  | 32     | CPSW_REGS_INT_SS_C3_FH_PULSE_EN_REG            | 5280 18C8h             |
| 18CCh  | 32     | CPSW_REGS_INT_SS_C3_MISC_EN_REG                | 5280 18CCh             |
| 18D0h  | 32     | CPSW_REGS_INT_SS_C3_TH_THRESH_PULSE_STATUS_REG | 5280 18D0h             |
| 18D4h  | 32     | CPSW_REGS_INT_SS_C3_TH_PULSE_STATUS_REG        | 5280 18D4h             |
| 18D8h  | 32     | CPSW_REGS_INT_SS_C3_FH_PULSE_STATUS_REG        | 5280 18D8h             |
| 18DCh  | 32     | CPSW_REGS_INT_SS_C3_MISC_STATUS_REG            | 5280 18DCh             |
| 18E0h  | 32     | CPSW_REGS_INT_SS_C3_TH_IMAX_REG                | 5280 18E0h             |
| 18E4h  | 32     | CPSW_REGS_INT_SS_C3_FH_IMAX_REG                | 5280 18E4h             |
| 20000h | 32     | CPSW_NC_VER_REG                                | 5282 0000h             |
| 20004h | 32     | CPSW_NC_CONTROL_REG                            | 5282 0004h             |
| 2000Ch | 32     | CPSW_NC_STATUS_REG                             | 5282 000Ch             |
| 20010h | 32     | CPSW_NC_EM_CONTROL_REG                         | 5282 0010h             |
| 20014h | 32     | CPSW_NC_STAT_PORT_EN_REG                       | 5282 0014h             |
| 20018h | 32     | CPSW_NC_PTYPE_REG                              | 5282 0018h             |
| 2001Ch | 32     | CPSW_NC_SOFT_IDLE_REG                          | 5282 001Ch             |
| 20020h | 32     | CPSW_NC_THRU_RATE_REG                          | 5282 0020h             |



**Table 5-1. CPSW Registers, Base Address=5280 0000h, Length=2097152 (continued)**

| Offset | Length | Register Name                                             | CPSW0 Physical Address |
|--------|--------|-----------------------------------------------------------|------------------------|
| 20024h | 32     | <a href="#">CPSW_NC_GAP_THRESH_REG</a>                    | 5282 0024h             |
| 2002Ch | 32     | <a href="#">CPSW_NC_EEE_PRESCALE_REG</a>                  | 5282 002Ch             |
| 20030h | 32     | <a href="#">CPSW_NC_TX_G_OFLOW_THRESH_SET_REG</a>         | 5282 0030h             |
| 20034h | 32     | <a href="#">CPSW_NC_TX_G_OFLOW_THRESH_CLR_REG</a>         | 5282 0034h             |
| 20038h | 32     | <a href="#">CPSW_NC_TX_G_BUF_THRESH_SET_L_REG</a>         | 5282 0038h             |
| 2003Ch | 32     | <a href="#">CPSW_NC_TX_G_BUF_THRESH_SET_H_REG</a>         | 5282 003Ch             |
| 20040h | 32     | <a href="#">CPSW_NC_TX_G_BUF_THRESH_CLR_L_REG</a>         | 5282 0040h             |
| 20044h | 32     | <a href="#">CPSW_NC_TX_G_BUF_THRESH_CLR_H_REG</a>         | 5282 0044h             |
| 20050h | 32     | <a href="#">CPSW_NC_VLAN_LTYPE_REG</a>                    | 5282 0050h             |
| 20054h | 32     | <a href="#">CPSW_NC_EST_TS_DOMAIN_REG</a>                 | 5282 0054h             |
| 20100h | 32     | <a href="#">CPSW_NC_TX_PRI0_MAXLEN_REG</a>                | 5282 0100h             |
| 20104h | 32     | <a href="#">CPSW_NC_TX_PRI1_MAXLEN_REG</a>                | 5282 0104h             |
| 20108h | 32     | <a href="#">CPSW_NC_TX_PRI2_MAXLEN_REG</a>                | 5282 0108h             |
| 2010Ch | 32     | <a href="#">CPSW_NC_TX_PRI3_MAXLEN_REG</a>                | 5282 010Ch             |
| 20110h | 32     | <a href="#">CPSW_NC_TX_PRI4_MAXLEN_REG</a>                | 5282 0110h             |
| 20114h | 32     | <a href="#">CPSW_NC_TX_PRI5_MAXLEN_REG</a>                | 5282 0114h             |
| 20118h | 32     | <a href="#">CPSW_NC_TX_PRI6_MAXLEN_REG</a>                | 5282 0118h             |
| 2011Ch | 32     | <a href="#">CPSW_NC_TX_PRI7_MAXLEN_REG</a>                | 5282 011Ch             |
| 21004h | 32     | <a href="#">CPSW_NC_CPPI_P0_CONTROL_REG</a>               | 5282 1004h             |
| 21010h | 32     | <a href="#">CPSW_NC_CPPI_P0_BLK_CNT_REG</a>               | 5282 1010h             |
| 21014h | 32     | <a href="#">CPSW_NC_CPPI_P0_PORT_VLAN_REG</a>             | 5282 1014h             |
| 21018h | 32     | <a href="#">CPSW_NC_CPPI_P0_TH_PRI_MAP_REG</a>            | 5282 1018h             |
| 2101Ch | 32     | <a href="#">CPSW_NC_CPPI_P0_PRI_CTL_REG</a>               | 5282 101Ch             |
| 21020h | 32     | <a href="#">CPSW_NC_CPPI_P0_FH_PRI_MAP_REG</a>            | 5282 1020h             |
| 21024h | 32     | <a href="#">CPSW_NC_CPPI_P0_FH_MAXLEN_REG</a>             | 5282 1024h             |
| 21028h | 32     | <a href="#">CPSW_NC_CPPI_P0_TH_BLK_PRI_REG</a>            | 5282 1028h             |
| 21030h | 32     | <a href="#">CPSW_NC_CPPI_P0_IDLE2LPI_REG</a>              | 5282 1030h             |
| 21034h | 32     | <a href="#">CPSW_NC_CPPI_P0_LPI2WAKE_REG</a>              | 5282 1034h             |
| 21038h | 32     | <a href="#">CPSW_NC_CPPI_P0_EEE_STATUS_REG</a>            | 5282 1038h             |
| 21050h | 32     | <a href="#">CPSW_NC_CPPI_P0_FIFO_STATUS_REG</a>           | 5282 1050h             |
| 21120h | 32     | <a href="#">CPSW_NC_CPPI_FH_DSCP_MAP_REG</a>              | 5282 1120h             |
| 21140h | 32     | <a href="#">CPSW_NC_CPPI_P0_PRI_CIR_REG</a>               | 5282 1140h             |
| 21160h | 32     | <a href="#">CPSW_NC_CPPI_P0_PRI_EIR_REG</a>               | 5282 1160h             |
| 21180h | 32     | <a href="#">CPSW_NC_CPPI_P0_TH_D_THRESH_SET_L_REG</a>     | 5282 1180h             |
| 21184h | 32     | <a href="#">CPSW_NC_CPPI_P0_TH_D_THRESH_SET_H_REG</a>     | 5282 1184h             |
| 21188h | 32     | <a href="#">CPSW_NC_CPPI_P0_TH_D_THRESH_CLR_L_REG</a>     | 5282 1188h             |
| 2118Ch | 32     | <a href="#">CPSW_NC_CPPI_P0_TH_D_THRESH_CLR_H_REG</a>     | 5282 118Ch             |
| 21190h | 32     | <a href="#">CPSW_NC_CPPI_P0_TH_G_BUF_THRESH_SET_L_REG</a> | 5282 1190h             |
| 21194h | 32     | <a href="#">CPSW_NC_CPPI_P0_TH_G_BUF_THRESH_SET_H_REG</a> | 5282 1194h             |
| 21198h | 32     | <a href="#">CPSW_NC_CPPI_P0_TH_G_BUF_THRESH_CLR_L_REG</a> | 5282 1198h             |
| 2119Ch | 32     | <a href="#">CPSW_NC_CPPI_P0_TH_G_BUF_THRESH_CLR_H_REG</a> | 5282 119Ch             |
| 21300h | 32     | <a href="#">CPSW_NC_CPPI_P0_SRC_ID_A_REG</a>              | 5282 1300h             |
| 21304h | 32     | <a href="#">CPSW_NC_CPPI_P0_SRC_ID_B_REG</a>              | 5282 1304h             |
| 21320h | 32     | <a href="#">CPSW_NC_CPPI_P0_HOST_BLK_PRI_REG</a>          | 5282 1320h             |

**Table 5-1. CPSW Registers, Base Address=5280 0000h, Length=2097152 (continued)**

| Offset | Length | Register Name                                                  | CPSW0 Physical Address |
|--------|--------|----------------------------------------------------------------|------------------------|
| 22004h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_CONTROL_REG_K</a>               | 5282 2004h + formula   |
| 22008h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_MAX_BLKs_REG_K</a>              | 5282 2008h + formula   |
| 22010h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_BLK_CNT_REG_K</a>               | 5282 2010h + formula   |
| 22014h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_PORT_VLAN_REG_K</a>             | 5282 2014h + formula   |
| 22018h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_TX_PRI_MAP_REG_K</a>            | 5282 2018h + formula   |
| 2201Ch | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_PRI_CTL_REG_K</a>               | 5282 201Ch + formula   |
| 22020h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_RX_PRI_MAP_REG_K</a>            | 5282 2020h + formula   |
| 22024h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_RX_MAXLEN_REG_K</a>             | 5282 2024h + formula   |
| 22028h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_TX_BLKs_PRI_REG_K</a>           | 5282 2028h + formula   |
| 22030h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_IDLE2LPI_REG_K</a>              | 5282 2030h + formula   |
| 22034h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_LPI2WAKE_REG_K</a>              | 5282 2034h + formula   |
| 22038h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_EEE_STATUS_REG_K</a>            | 5282 2038h + formula   |
| 22050h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_FIFO_STATUS_REG_K</a>           | 5282 2050h + formula   |
| 22060h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_EST_CONTROL_REG_K</a>           | 5282 2060h + formula   |
| 22120h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_FH_DSCP_MAP_REG_K</a>           | 5282 2120h + formula   |
| 22140h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_PRI_CIR_REG_K</a>               | 5282 2140h + formula   |
| 22160h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_PRI_EIR_REG_K</a>               | 5282 2160h + formula   |
| 22180h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_TX_D_THRESH_SET_L_REG_K</a>     | 5282 2180h + formula   |
| 22184h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_TX_D_THRESH_SET_H_REG_K</a>     | 5282 2184h + formula   |
| 22188h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_TX_D_THRESH_CLR_L_REG_K</a>     | 5282 2188h + formula   |
| 2218Ch | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_TX_D_THRESH_CLR_H_REG_K</a>     | 5282 218Ch + formula   |
| 22190h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_TX_G_BUF_THRESH_SET_L_REG_K</a> | 5282 2190h + formula   |
| 22194h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_TX_G_BUF_THRESH_SET_H_REG_K</a> | 5282 2194h + formula   |
| 22198h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_TX_G_BUF_THRESH_CLR_L_REG_K</a> | 5282 2198h + formula   |
| 2219Ch | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_TX_G_BUF_THRESH_CLR_H_REG_K</a> | 5282 219Ch + formula   |
| 22300h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_TX_D_OFLOW_ADDVAL_L_REG_K</a>   | 5282 2300h + formula   |
| 22304h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_TX_D_OFLOW_ADDVAL_H_REG_K</a>   | 5282 2304h + formula   |
| 22308h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_SA_L_REG_K</a>                  | 5282 2308h + formula   |
| 2230Ch | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_SA_H_REG_K</a>                  | 5282 230Ch + formula   |
| 22310h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_TS_CTL_REG_K</a>                | 5282 2310h + formula   |
| 22314h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_TS_SEQ_LTYPE_REG_K</a>          | 5282 2314h + formula   |
| 22318h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_TS_VLAN_LTYPE_REG_K</a>         | 5282 2318h + formula   |
| 2231Ch | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_TS_CTL_LTYPE2_REG_K</a>         | 5282 231Ch + formula   |
| 22320h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_TS_CTL2_REG_K</a>               | 5282 2320h + formula   |
| 22330h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_MAC_CONTROL_REG_K</a>           | 5282 2330h + formula   |
| 22334h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_MAC_STATUS_REG_K</a>            | 5282 2334h + formula   |
| 22338h | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_MAC_SOFT_RESET_REG_K</a>        | 5282 2338h + formula   |
| 2233Ch | 32     | <a href="#">CPSW_NC_ETH_MAC_PN_MAC_BOFFTEST_REG_K</a>          | 5282 233Ch + formula   |

**Table 5-1. CPSW Registers, Base Address=5280 0000h, Length=2097152 (continued)**

| Offset | Length | Register Name                                  | CPSW0 Physical Address |
|--------|--------|------------------------------------------------|------------------------|
| 22340h | 32     | CPSW_NC_ETH_MAC_PN_MAC_RX_PAUSETIMER_REG_K     | 5282 2340h + formula   |
| 22350h | 32     | CPSW_NC_ETH_MAC_PN_MAC_RXN_PAUSETIMER_REG_K    | 5282 2350h + formula   |
| 22370h | 32     | CPSW_NC_ETH_MAC_PN_MAC_TX_PAUSETIMER_REG_K     | 5282 2370h + formula   |
| 22380h | 32     | CPSW_NC_ETH_MAC_PN_MAC_TX0_PAUSETIMER_REG_K    | 5282 2380h + formula   |
| 223A0h | 32     | CPSW_NC_ETH_MAC_PN_MAC_EMCONTROL_REG_K         | 5282 23A0h + formula   |
| 223A4h | 32     | CPSW_NC_ETH_MAC_PN_MAC_TX_GAP_REG_K            | 5282 23A4h + formula   |
| 223A8h | 32     | CPSW_NC_ETH_MAC_PN_MAC_PORT_CONFIG_K           | 5282 23A8h + formula   |
| 223ACh | 32     | CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_POINTER_REG_K | 5282 23ACh + formula   |
| 223B0h | 32     | CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_A_REG_K       | 5282 23B0h + formula   |
| 223B4h | 32     | CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_B_REG_K       | 5282 23B4h + formula   |
| 223B8h | 32     | CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_C_REG_K       | 5282 23B8h + formula   |
| 223BCh | 32     | CPSW_NC_ETH_MAC_PN_INTERVLAN_OPX_D_REG_K       | 5282 23BCh + formula   |
| 32000h | 32     | CPSW_NC_EST_FETCH_LOC                          | 5283 2000h             |
| 34000h | 32     | CPSW_NC_CPDMA_REGS_FH_IDVER_REG                | 5283 4000h             |
| 34004h | 32     | CPSW_NC_CPDMA_REGS_FH_CONTROL_REG              | 5283 4004h             |
| 34008h | 32     | CPSW_NC_CPDMA_REGS_FH_TEARDOWN_REG             | 5283 4008h             |
| 3400Ch | 32     | CPSW_NC_CPDMA_REGS_FH_CONTROL2_REG             | 5283 400Ch             |
| 34010h | 32     | CPSW_NC_CPDMA_REGS_TH_IDVER_REG                | 5283 4010h             |
| 34014h | 32     | CPSW_NC_CPDMA_REGS_TH_CONTROL_REG              | 5283 4014h             |
| 34018h | 32     | CPSW_NC_CPDMA_REGS_TH_TEARDOWN_REG             | 5283 4018h             |
| 3401Ch | 32     | CPSW_NC_CPDMA_REGS_SOFT_RESET_REG              | 5283 401Ch             |
| 34020h | 32     | CPSW_NC_CPDMA_REGS_CONTROL_REG                 | 5283 4020h             |
| 34024h | 32     | CPSW_NC_CPDMA_REGS_STATUS_REG                  | 5283 4024h             |
| 34028h | 32     | CPSW_NC_CPDMA_REGS_TH_BUFFER_OFFSET_REG        | 5283 4028h             |
| 3402Ch | 32     | CPSW_NC_CPDMA_REGS_EMULATION_CONTROL_REG       | 5283 402Ch             |
| 34080h | 32     | CPSW_NC_CPDMA_INT_FH_INTSTAT_RAW_REG           | 5283 4080h             |
| 34084h | 32     | CPSW_NC_CPDMA_INT_FH_INTSTAT_MASKED_REG        | 5283 4084h             |
| 34088h | 32     | CPSW_NC_CPDMA_INT_FH_INTMASK_SET_REG           | 5283 4088h             |
| 3408Ch | 32     | CPSW_NC_CPDMA_INT_FH_INTMASK_CLEAR_REG         | 5283 408Ch             |
| 34090h | 32     | CPSW_NC_CPDMA_INT_IN_VECTOR_REG                | 5283 4090h             |
| 34094h | 32     | CPSW_NC_CPDMA_INT_EOI_VECTOR_REG               | 5283 4094h             |
| 340A0h | 32     | CPSW_NC_CPDMA_INT_TH_INTSTAT_RAW_REG           | 5283 40A0h             |
| 340A4h | 32     | CPSW_NC_CPDMA_INT_TH_INTSTAT_MASKED_REG        | 5283 40A4h             |
| 340A8h | 32     | CPSW_NC_CPDMA_INT_TH_INTMASK_SET_REG           | 5283 40A8h             |
| 340ACh | 32     | CPSW_NC_CPDMA_INT_TH_INTMASK_CLEAR_REG         | 5283 40ACh             |
| 340B0h | 32     | CPSW_NC_CPDMA_INT_INTSTAT_RAW_REG              | 5283 40B0h             |
| 340B4h | 32     | CPSW_NC_CPDMA_INT_INTSTAT_MASKED_REG           | 5283 40B4h             |
| 340B8h | 32     | CPSW_NC_CPDMA_INT_INTMASK_SET_REG              | 5283 40B8h             |
| 340BCh | 32     | CPSW_NC_CPDMA_INT_INTMASK_CLEAR_REG            | 5283 40BCh             |
| 340C0h | 32     | CPSW_NC_CPDMA_INT_TH0_PENDTHRESH_REG           | 5283 40C0h             |
| 340C4h | 32     | CPSW_NC_CPDMA_INT_TH1_PENDTHRESH_REG           | 5283 40C4h             |

**Table 5-1. CPSW Registers, Base Address=5280 0000h, Length=2097152 (continued)**

| Offset | Length | Register Name                                        | CPSW0 Physical Address |
|--------|--------|------------------------------------------------------|------------------------|
| 340C8h | 32     | <a href="#">CPSW_NC_CPDMA_INT_TH2_PENDTHRESH_REG</a> | 5283 40C8h             |
| 340CCh | 32     | <a href="#">CPSW_NC_CPDMA_INT_TH3_PENDTHRESH_REG</a> | 5283 40CCh             |
| 340D0h | 32     | <a href="#">CPSW_NC_CPDMA_INT_TH4_PENDTHRESH_REG</a> | 5283 40D0h             |
| 340D4h | 32     | <a href="#">CPSW_NC_CPDMA_INT_TH5_PENDTHRESH_REG</a> | 5283 40D4h             |
| 340D8h | 32     | <a href="#">CPSW_NC_CPDMA_INT_TH6_PENDTHRESH_REG</a> | 5283 40D8h             |
| 340DCh | 32     | <a href="#">CPSW_NC_CPDMA_INT_TH7_PENDTHRESH_REG</a> | 5283 40DCh             |
| 340E0h | 32     | <a href="#">CPSW_NC_CPDMA_INT_TH0_FREEBUFFER_REG</a> | 5283 40E0h             |
| 340E4h | 32     | <a href="#">CPSW_NC_CPDMA_INT_TH1_FREEBUFFER_REG</a> | 5283 40E4h             |
| 340E8h | 32     | <a href="#">CPSW_NC_CPDMA_INT_TH2_FREEBUFFER_REG</a> | 5283 40E8h             |
| 340ECh | 32     | <a href="#">CPSW_NC_CPDMA_INT_TH3_FREEBUFFER_REG</a> | 5283 40ECh             |
| 340F0h | 32     | <a href="#">CPSW_NC_CPDMA_INT_TH4_FREEBUFFER_REG</a> | 5283 40F0h             |
| 340F4h | 32     | <a href="#">CPSW_NC_CPDMA_INT_TH5_FREEBUFFER_REG</a> | 5283 40F4h             |
| 340F8h | 32     | <a href="#">CPSW_NC_CPDMA_INT_TH6_FREEBUFFER_REG</a> | 5283 40F8h             |
| 340FCh | 32     | <a href="#">CPSW_NC_CPDMA_INT_TH7_FREEBUFFER_REG</a> | 5283 40FCh             |
| 34200h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_FH0_HDP_REG</a>       | 5283 4200h             |
| 34204h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_FH1_HDP_REG</a>       | 5283 4204h             |
| 34208h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_FH2_HDP_REG</a>       | 5283 4208h             |
| 3420Ch | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_FH3_HDP_REG</a>       | 5283 420Ch             |
| 34210h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_FH4_HDP_REG</a>       | 5283 4210h             |
| 34214h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_FH5_HDP_REG</a>       | 5283 4214h             |
| 34218h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_FH6_HDP_REG</a>       | 5283 4218h             |
| 3421Ch | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_FH7_HDP_REG</a>       | 5283 421Ch             |
| 34220h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TH0_HDP_REG</a>       | 5283 4220h             |
| 34224h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TH1_HDP_REG</a>       | 5283 4224h             |
| 34228h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TH2_HDP_REG</a>       | 5283 4228h             |
| 3422Ch | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TH3_HDP_REG</a>       | 5283 422Ch             |
| 34230h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TH4_HDP_REG</a>       | 5283 4230h             |
| 34234h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TH5_HDP_REG</a>       | 5283 4234h             |
| 34238h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TH6_HDP_REG</a>       | 5283 4238h             |
| 3423Ch | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TH7_HDP_REG</a>       | 5283 423Ch             |
| 34240h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_FH0_CP_REG</a>        | 5283 4240h             |
| 34244h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_FH1_CP_REG</a>        | 5283 4244h             |
| 34248h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_FH2_CP_REG</a>        | 5283 4248h             |
| 3424Ch | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_FH3_CP_REG</a>        | 5283 424Ch             |
| 34250h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_FH4_CP_REG</a>        | 5283 4250h             |
| 34254h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_FH5_CP_REG</a>        | 5283 4254h             |
| 34258h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_FH6_CP_REG</a>        | 5283 4258h             |
| 3425Ch | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_FH7_CP_REG</a>        | 5283 425Ch             |
| 34260h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TH0_CP_REG</a>        | 5283 4260h             |
| 34264h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TH1_CP_REG</a>        | 5283 4264h             |
| 34268h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TH2_CP_REG</a>        | 5283 4268h             |
| 3426Ch | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TH3_CP_REG</a>        | 5283 426Ch             |
| 34270h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TH4_CP_REG</a>        | 5283 4270h             |
| 34274h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TH5_CP_REG</a>        | 5283 4274h             |
| 34278h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TH6_CP_REG</a>        | 5283 4278h             |

**Table 5-1. CPSW Registers, Base Address=5280 0000h, Length=2097152 (continued)**

| Offset | Length | Register Name                                       | CPSW0 Physical Address |
|--------|--------|-----------------------------------------------------|------------------------|
| 3427Ch | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TH7_CP_REG</a>       | 5283 427Ch             |
| 34300h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_FH0_HDP_REG</a> | 5283 4300h             |
| 34304h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_FH1_HDP_REG</a> | 5283 4304h             |
| 34308h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_FH2_HDP_REG</a> | 5283 4308h             |
| 3430Ch | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_FH3_HDP_REG</a> | 5283 430Ch             |
| 34310h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_FH4_HDP_REG</a> | 5283 4310h             |
| 34314h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_FH5_HDP_REG</a> | 5283 4314h             |
| 34318h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_FH6_HDP_REG</a> | 5283 4318h             |
| 3431Ch | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_FH7_HDP_REG</a> | 5283 431Ch             |
| 34320h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_TH0_HDP_REG</a> | 5283 4320h             |
| 34324h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_TH1_HDP_REG</a> | 5283 4324h             |
| 34328h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_TH2_HDP_REG</a> | 5283 4328h             |
| 3432Ch | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_TH3_HDP_REG</a> | 5283 432Ch             |
| 34330h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_TH4_HDP_REG</a> | 5283 4330h             |
| 34334h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_TH5_HDP_REG</a> | 5283 4334h             |
| 34338h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_TH6_HDP_REG</a> | 5283 4338h             |
| 3433Ch | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_TH7_HDP_REG</a> | 5283 433Ch             |
| 34340h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_FH0_CP_REG</a>  | 5283 4340h             |
| 34344h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_FH1_CP_REG</a>  | 5283 4344h             |
| 34348h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_FH2_CP_REG</a>  | 5283 4348h             |
| 3434Ch | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_FH3_CP_REG</a>  | 5283 434Ch             |
| 34350h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_FH4_CP_REG</a>  | 5283 4350h             |
| 34354h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_FH5_CP_REG</a>  | 5283 4354h             |
| 34358h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_FH6_CP_REG</a>  | 5283 4358h             |
| 3435Ch | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_FH7_CP_REG</a>  | 5283 435Ch             |
| 34360h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_TH0_CP_REG</a>  | 5283 4360h             |
| 34364h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_TH1_CP_REG</a>  | 5283 4364h             |
| 34368h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_TH2_CP_REG</a>  | 5283 4368h             |
| 3436Ch | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_TH3_CP_REG</a>  | 5283 436Ch             |
| 34370h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_TH4_CP_REG</a>  | 5283 4370h             |
| 34374h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_TH5_CP_REG</a>  | 5283 4374h             |
| 34378h | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_TH6_CP_REG</a>  | 5283 4378h             |
| 3437Ch | 32     | <a href="#">CPSW_NC_CPDMA_SRAM_TEST_TH7_CP_REG</a>  | 5283 437Ch             |
| 3A000h | 32     | <a href="#">CPSW_NC_STAT_RXGOODFRAMES_K</a>         | 5283 A000h + formula   |
| 3A004h | 32     | <a href="#">CPSW_NC_STAT_RXBROADCASTFRAMES_K</a>    | 5283 A004h + formula   |
| 3A008h | 32     | <a href="#">CPSW_NC_STAT_RXMULTICASTFRAMES_K</a>    | 5283 A008h + formula   |
| 3A00Ch | 32     | <a href="#">CPSW_NC_STAT_RXPAUSEFRAMES_K</a>        | 5283 A00Ch + formula   |
| 3A010h | 32     | <a href="#">CPSW_NC_STAT_RXCRCERRORS_K</a>          | 5283 A010h + formula   |
| 3A014h | 32     | <a href="#">CPSW_NC_STAT_RXALIGNCODEERRORS_K</a>    | 5283 A014h + formula   |
| 3A018h | 32     | <a href="#">CPSW_NC_STAT_RXOVERSIZEDFRAMES_K</a>    | 5283 A018h + formula   |
| 3A01Ch | 32     | <a href="#">CPSW_NC_STAT_RXJABBERFRAMES_K</a>       | 5283 A01Ch + formula   |
| 3A020h | 32     | <a href="#">CPSW_NC_STAT_RXUNDERSIZEDFRAMES_K</a>   | 5283 A020h + formula   |
| 3A024h | 32     | <a href="#">CPSW_NC_STAT_RXFRAGMENTS_K</a>          | 5283 A024h + formula   |
| 3A028h | 32     | <a href="#">CPSW_NC_STAT_ALE_DROP_K</a>             | 5283 A028h + formula   |
| 3A02Ch | 32     | <a href="#">CPSW_NC_STAT_ALE_OVERRUN_DROP_K</a>     | 5283 A02Ch + formula   |

**Table 5-1. CPSW Registers, Base Address=5280 0000h, Length=2097152 (continued)**

| Offset | Length | Register Name                                          | CPSW0 Physical Address |
|--------|--------|--------------------------------------------------------|------------------------|
| 3A030h | 32     | <a href="#">CPSW_NC_STAT_RXOCTETS_K</a>                | 5283 A030h + formula   |
| 3A034h | 32     | <a href="#">CPSW_NC_STAT_TXGOODFRAMES_K</a>            | 5283 A034h + formula   |
| 3A038h | 32     | <a href="#">CPSW_NC_STAT_TXBROADCASTFRAMES_K</a>       | 5283 A038h + formula   |
| 3A03Ch | 32     | <a href="#">CPSW_NC_STAT_TXMULTICASTFRAMES_K</a>       | 5283 A03Ch + formula   |
| 3A040h | 32     | <a href="#">CPSW_NC_STAT_TXPAUSEFRAMES_K</a>           | 5283 A040h + formula   |
| 3A044h | 32     | <a href="#">CPSW_NC_STAT_TXDEFERREDFRAMES_K</a>        | 5283 A044h + formula   |
| 3A048h | 32     | <a href="#">CPSW_NC_STAT_TXCOLLISIONFRAMES_K</a>       | 5283 A048h + formula   |
| 3A04Ch | 32     | <a href="#">CPSW_NC_STAT_TXSINGLECOLLFRAMES_K</a>      | 5283 A04Ch + formula   |
| 3A050h | 32     | <a href="#">CPSW_NC_STAT_TXMULTCOLLFRAMES_K</a>        | 5283 A050h + formula   |
| 3A054h | 32     | <a href="#">CPSW_NC_STAT_TXEXCESSIVECOLLISIONS_K</a>   | 5283 A054h + formula   |
| 3A058h | 32     | <a href="#">CPSW_NC_STAT_TXLATECOLLISIONS_K</a>        | 5283 A058h + formula   |
| 3A05Ch | 32     | <a href="#">CPSW_NC_STAT_RXIPGERROR_K</a>              | 5283 A05Ch + formula   |
| 3A060h | 32     | <a href="#">CPSW_NC_STAT_TXCARRIERSENSEERRORS_K</a>    | 5283 A060h + formula   |
| 3A064h | 32     | <a href="#">CPSW_NC_STAT_TXOCTETS_K</a>                | 5283 A064h + formula   |
| 3A068h | 32     | <a href="#">CPSW_NC_STAT_OCTETFRAMES64_K</a>           | 5283 A068h + formula   |
| 3A06Ch | 32     | <a href="#">CPSW_NC_STAT_OCTETFRAMES65T127_K</a>       | 5283 A06Ch + formula   |
| 3A070h | 32     | <a href="#">CPSW_NC_STAT_OCTETFRAMES128T255_K</a>      | 5283 A070h + formula   |
| 3A074h | 32     | <a href="#">CPSW_NC_STAT_OCTETFRAMES256T511_K</a>      | 5283 A074h + formula   |
| 3A078h | 32     | <a href="#">CPSW_NC_STAT_OCTETFRAMES512T1023_K</a>     | 5283 A078h + formula   |
| 3A07Ch | 32     | <a href="#">CPSW_NC_STAT_OCTETFRAMES1024TUP_K</a>      | 5283 A07Ch + formula   |
| 3A080h | 32     | <a href="#">CPSW_NC_STAT_NETOCTETS_K</a>               | 5283 A080h + formula   |
| 3A084h | 32     | <a href="#">CPSW_NC_STAT_RX_BOTTOM_OF_FIFO_DROP_K</a>  | 5283 A084h + formula   |
| 3A088h | 32     | <a href="#">CPSW_NC_STAT_PORTMASK_DROP_K</a>           | 5283 A088h + formula   |
| 3A08Ch | 32     | <a href="#">CPSW_NC_STAT_RX_TOP_OF_FIFO_DROP_K</a>     | 5283 A08Ch + formula   |
| 3A090h | 32     | <a href="#">CPSW_NC_STAT_ALE_RATE_LIMIT_DROP_K</a>     | 5283 A090h + formula   |
| 3A094h | 32     | <a href="#">CPSW_NC_STAT_ALE_VID_INGRESS_DROP_K</a>    | 5283 A094h + formula   |
| 3A098h | 32     | <a href="#">CPSW_NC_STAT_ALE_DA_EQ_SA_DROP_K</a>       | 5283 A098h + formula   |
| 3A09Ch | 32     | <a href="#">CPSW_NC_STAT_ALE_BLOCK_DROP_K</a>          | 5283 A09Ch + formula   |
| 3A0A0h | 32     | <a href="#">CPSW_NC_STAT_ALE_SECURE_DROP_K</a>         | 5283 A0A0h + formula   |
| 3A0A4h | 32     | <a href="#">CPSW_NC_STAT_ALE_AUTH_DROP_K</a>           | 5283 A0A4h + formula   |
| 3A0A8h | 32     | <a href="#">CPSW_NC_STAT_ALE_UNKN_UNI_K</a>            | 5283 A0A8h + formula   |
| 3A0ACh | 32     | <a href="#">CPSW_NC_STAT_ALE_UNKN_UNI_BCNT_K</a>       | 5283 A0ACh + formula   |
| 3A0B0h | 32     | <a href="#">CPSW_NC_STAT_ALE_UNKN_MLT_K</a>            | 5283 A0B0h + formula   |
| 3A0B4h | 32     | <a href="#">CPSW_NC_STAT_ALE_UNKN_MLT_BCNT_K</a>       | 5283 A0B4h + formula   |
| 3A0B8h | 32     | <a href="#">CPSW_NC_STAT_ALE_UNKN_BRD_K</a>            | 5283 A0B8h + formula   |
| 3A0BCh | 32     | <a href="#">CPSW_NC_STAT_ALE_UNKN_BRD_BCNT_K</a>       | 5283 A0BCh + formula   |
| 3A0C0h | 32     | <a href="#">CPSW_NC_STAT_ALE_POL_MATCH_K</a>           | 5283 A0C0h + formula   |
| 3A0C4h | 32     | <a href="#">CPSW_NC_STAT_ALE_POL_MATCH_RED_K</a>       | 5283 A0C4h + formula   |
| 3A0C8h | 32     | <a href="#">CPSW_NC_STAT_ALE_POL_MATCH_YELLOW_K</a>    | 5283 A0C8h + formula   |
| 3A0CCh | 32     | <a href="#">CPSW_NC_STAT_ALE_MULT_SA_DROP_K</a>        | 5283 A0CCh + formula   |
| 3A0D0h | 32     | <a href="#">CPSW_NC_STAT_ALE_DUAL_VLAN_DROP_K</a>      | 5283 A0D0h + formula   |
| 3A0D4h | 32     | <a href="#">CPSW_NC_STAT_ALE_LEN_ERROR_DROP_K</a>      | 5283 A0D4h + formula   |
| 3A0D8h | 32     | <a href="#">CPSW_NC_STAT_ALE_IP_NEXT_HDR_DROP_K</a>    | 5283 A0D8h + formula   |
| 3A0DCh | 32     | <a href="#">CPSW_NC_STAT_ALE_IPV4_FRAG_DROP_K</a>      | 5283 A0DCh + formula   |
| 3A17Ch | 32     | <a href="#">CPSW_NC_STAT_TX_MEMORY_PROTECT_ERROR_K</a> | 5283 A17Ch + formula   |



**Table 5-1. CPSW Registers, Base Address=5280 0000h, Length=2097152 (continued)**

| Offset | Length | Register Name                                               | CPSW0 Physical Address |
|--------|--------|-------------------------------------------------------------|------------------------|
| 3A180h | 32     | <a href="#">CPSW_NC_STAT_ENET_PN_TX_PRI_REG_K</a>           | 5283 A180h + formula   |
| 3A1A0h | 32     | <a href="#">CPSW_NC_STAT_ENET_PN_TX_PRI_BCNT_REG_K</a>      | 5283 A1A0h + formula   |
| 3A1C0h | 32     | <a href="#">CPSW_NC_STAT_ENET_PN_TX_PRI_DROP_REG_K</a>      | 5283 A1C0h + formula   |
| 3A1E0h | 32     | <a href="#">CPSW_NC_STAT_ENET_PN_TX_PRI_DROP_BCNT_REG_K</a> | 5283 A1E0h + formula   |
| 3D000h | 32     | <a href="#">CPSW_NC_CPTS_IDVER_REG</a>                      | 5283 D000h             |
| 3D004h | 32     | <a href="#">CPSW_NC_CPTS_CONTROL_REG</a>                    | 5283 D004h             |
| 3D008h | 32     | <a href="#">CPSW_NC_CPTS_RFTCLK_SEL_REG</a>                 | 5283 D008h             |
| 3D00Ch | 32     | <a href="#">CPSW_NC_CPTS_TS_PUSH_REG</a>                    | 5283 D00Ch             |
| 3D010h | 32     | <a href="#">CPSW_NC_CPTS_TS_LOAD_VAL_REG</a>                | 5283 D010h             |
| 3D014h | 32     | <a href="#">CPSW_NC_CPTS_TS_LOAD_EN_REG</a>                 | 5283 D014h             |
| 3D018h | 32     | <a href="#">CPSW_NC_CPTS_TS_COMP_VAL_REG</a>                | 5283 D018h             |
| 3D01Ch | 32     | <a href="#">CPSW_NC_CPTS_TS_COMP_LEN_REG</a>                | 5283 D01Ch             |
| 3D020h | 32     | <a href="#">CPSW_NC_CPTS_INTSTAT_RAW_REG</a>                | 5283 D020h             |
| 3D024h | 32     | <a href="#">CPSW_NC_CPTS_INTSTAT_MASKED_REG</a>             | 5283 D024h             |
| 3D028h | 32     | <a href="#">CPSW_NC_CPTS_INT_ENABLE_REG</a>                 | 5283 D028h             |
| 3D02Ch | 32     | <a href="#">CPSW_NC_CPTS_TS_COMP_NUDGE_REG</a>              | 5283 D02Ch             |
| 3D030h | 32     | <a href="#">CPSW_NC_CPTS_EVENT_POP_REG</a>                  | 5283 D030h             |
| 3D034h | 32     | <a href="#">CPSW_NC_CPTS_EVENT_0_REG</a>                    | 5283 D034h             |
| 3D038h | 32     | <a href="#">CPSW_NC_CPTS_EVENT_1_REG</a>                    | 5283 D038h             |
| 3D03Ch | 32     | <a href="#">CPSW_NC_CPTS_EVENT_2_REG</a>                    | 5283 D03Ch             |
| 3D040h | 32     | <a href="#">CPSW_NC_CPTS_EVENT_3_REG</a>                    | 5283 D040h             |
| 3D044h | 32     | <a href="#">CPSW_NC_CPTS_TS_LOAD_HIGH_VAL_REG</a>           | 5283 D044h             |
| 3D048h | 32     | <a href="#">CPSW_NC_CPTS_TS_COMP_HIGH_VAL_REG</a>           | 5283 D048h             |
| 3D04Ch | 32     | <a href="#">CPSW_NC_CPTS_TS_ADD_VAL_REG</a>                 | 5283 D04Ch             |
| 3D050h | 32     | <a href="#">CPSW_NC_CPTS_TS_PPM_LOW_VAL_REG</a>             | 5283 D050h             |
| 3D054h | 32     | <a href="#">CPSW_NC_CPTS_TS_PPM_HIGH_VAL_REG</a>            | 5283 D054h             |
| 3D058h | 32     | <a href="#">CPSW_NC_CPTS_TS_NUDGE_VAL_REG</a>               | 5283 D058h             |
| 3D0D0h | 32     | <a href="#">CPSW_NC_CPTS_TS_CONFIG</a>                      | 5283 D0D0h             |
| 3D0E0h | 32     | <a href="#">CPSW_NC_CPTS_TS_GENF_COMP_LOW_REG_L</a>         | 5283 D0E0h + formula   |
| 3D0E4h | 32     | <a href="#">CPSW_NC_CPTS_TS_GENF_COMP_HIGH_REG_L</a>        | 5283 D0E4h + formula   |
| 3D0E8h | 32     | <a href="#">CPSW_NC_CPTS_TS_GENF_CONTROL_REG_L</a>          | 5283 D0E8h + formula   |
| 3D0ECh | 32     | <a href="#">CPSW_NC_CPTS_TS_GENF_LENGTH_REG_L</a>           | 5283 D0ECh + formula   |
| 3D0F0h | 32     | <a href="#">CPSW_NC_CPTS_TS_GENF_PPM_LOW_REG_L</a>          | 5283 D0F0h + formula   |
| 3D0F4h | 32     | <a href="#">CPSW_NC_CPTS_TS_GENF_PPM_HIGH_REG_L</a>         | 5283 D0F4h + formula   |
| 3D0F8h | 32     | <a href="#">CPSW_NC_CPTS_TS_GENF_NUDGE_REG_L</a>            | 5283 D0F8h + formula   |
| 3D200h | 32     | <a href="#">CPSW_NC_CPTS_TS_ESTF_COMP_LOW_REG_L</a>         | 5283 D200h + formula   |
| 3D204h | 32     | <a href="#">CPSW_NC_CPTS_TS_ESTF_COMP_HIGH_REG_L</a>        | 5283 D204h + formula   |
| 3D208h | 32     | <a href="#">CPSW_NC_CPTS_TS_ESTF_CONTROL_REG_L</a>          | 5283 D208h + formula   |
| 3D20Ch | 32     | <a href="#">CPSW_NC_CPTS_TS_ESTF_LENGTH_REG_L</a>           | 5283 D20Ch + formula   |
| 3D210h | 32     | <a href="#">CPSW_NC_CPTS_TS_ESTF_PPM_LOW_REG_L</a>          | 5283 D210h + formula   |
| 3D214h | 32     | <a href="#">CPSW_NC_CPTS_TS_ESTF_PPM_HIGH_REG_L</a>         | 5283 D214h + formula   |
| 3D218h | 32     | <a href="#">CPSW_NC_CPTS_TS_ESTF_NUDGE_REG_L</a>            | 5283 D218h + formula   |
| 3E000h | 32     | <a href="#">CPSW_NC_ALE_MOD_VER</a>                         | 5283 E000h             |
| 3E004h | 32     | <a href="#">CPSW_NC_ALE_STATUS</a>                          | 5283 E004h             |

**Table 5-1. CPSW Registers, Base Address=5280 0000h, Length=2097152 (continued)**

| Offset | Length | Register Name                                   | CPSW0 Physical Address |
|--------|--------|-------------------------------------------------|------------------------|
| 3E008h | 32     | <a href="#">CPSW_NC_ALE_CONTROL</a>             | 5283 E008h             |
| 3E00Ch | 32     | <a href="#">CPSW_NC_ALE_CTRL2</a>               | 5283 E00Ch             |
| 3E010h | 32     | <a href="#">CPSW_NC_ALE_PRESCALE</a>            | 5283 E010h             |
| 3E014h | 32     | <a href="#">CPSW_NC_ALE_AGING_CTRL</a>          | 5283 E014h             |
| 3E01Ch | 32     | <a href="#">CPSW_NC_ALE_NXT_HDR</a>             | 5283 E01Ch             |
| 3E020h | 32     | <a href="#">CPSW_NC_ALE_TBLCTL</a>              | 5283 E020h             |
| 3E034h | 32     | <a href="#">CPSW_NC_ALE_TBLW2</a>               | 5283 E034h             |
| 3E038h | 32     | <a href="#">CPSW_NC_ALE_TBLW1</a>               | 5283 E038h             |
| 3E03Ch | 32     | <a href="#">CPSW_NC_ALE_TBLW0</a>               | 5283 E03Ch             |
| 3E040h | 32     | <a href="#">CPSW_NC_ALE_I0_PORTCTL0</a>         | 5283 E040h             |
| 3E090h | 32     | <a href="#">CPSW_NC_ALE_UVLAN_MEMBER</a>        | 5283 E090h             |
| 3E094h | 32     | <a href="#">CPSW_NC_ALE_UVLAN_URCAST</a>        | 5283 E094h             |
| 3E098h | 32     | <a href="#">CPSW_NC_ALE_UVLAN_RMCAST</a>        | 5283 E098h             |
| 3E09Ch | 32     | <a href="#">CPSW_NC_ALE_UVLAN_UNTAG</a>         | 5283 E09Ch             |
| 3E0B4h | 32     | <a href="#">CPSW_NC_ALE_FAST_LUT</a>            | 5283 E0B4h             |
| 3E0B8h | 32     | <a href="#">CPSW_NC_ALE_STAT_DIAG</a>           | 5283 E0B8h             |
| 3E0BCh | 32     | <a href="#">CPSW_NC_ALE_OAM_LB_CTRL</a>         | 5283 E0BCh             |
| 3E0FCh | 32     | <a href="#">CPSW_NC_ALE_EGRESSOP</a>            | 5283 E0FCh             |
| 3E100h | 32     | <a href="#">CPSW_NC_ALE_POLICECFG0</a>          | 5283 E100h             |
| 3E104h | 32     | <a href="#">CPSW_NC_ALE_POLICECFG1</a>          | 5283 E104h             |
| 3E108h | 32     | <a href="#">CPSW_NC_ALE_POLICECFG2</a>          | 5283 E108h             |
| 3E10Ch | 32     | <a href="#">CPSW_NC_ALE_POLICECFG3</a>          | 5283 E10Ch             |
| 3E110h | 32     | <a href="#">CPSW_NC_ALE_POLICECFG4</a>          | 5283 E110h             |
| 3E118h | 32     | <a href="#">CPSW_NC_ALE_POLICECFG6</a>          | 5283 E118h             |
| 3E11Ch | 32     | <a href="#">CPSW_NC_ALE_POLICECFG7</a>          | 5283 E11Ch             |
| 3E120h | 32     | <a href="#">CPSW_NC_ALE_POLICETBLCTL</a>        | 5283 E120h             |
| 3E124h | 32     | <a href="#">CPSW_NC_ALE_POLICECONTROL</a>       | 5283 E124h             |
| 3E128h | 32     | <a href="#">CPSW_NC_ALE_POLICETESTCTL</a>       | 5283 E128h             |
| 3E12Ch | 32     | <a href="#">CPSW_NC_ALE_POLICEHSTAT</a>         | 5283 E12Ch             |
| 3E134h | 32     | <a href="#">CPSW_NC_ALE_THREADMAPDEF</a>        | 5283 E134h             |
| 3E138h | 32     | <a href="#">CPSW_NC_ALE_THREADMAPCTL</a>        | 5283 E138h             |
| 3E13Ch | 32     | <a href="#">CPSW_NC_ALE_THREADMAPVAL</a>        | 5283 E13Ch             |
| 3F000h | 32     | <a href="#">CPSW_NC_ECC_REV</a>                 | 5283 F000h             |
| 3F008h | 32     | <a href="#">CPSW_NC_ECC_VECTOR</a>              | 5283 F008h             |
| 3F00Ch | 32     | <a href="#">CPSW_NC_ECC_STAT</a>                | 5283 F00Ch             |
| 3F010h | 32     | <a href="#">CPSW_NC_ECC_RESERVED_SVBUS</a>      | 5283 F010h             |
| 3F03Ch | 32     | <a href="#">CPSW_NC_ECC_SEC_EOI_REG</a>         | 5283 F03Ch             |
| 3F040h | 32     | <a href="#">CPSW_NC_ECC_SEC_STATUS_REG0</a>     | 5283 F040h             |
| 3F080h | 32     | <a href="#">CPSW_NC_ECC_SEC_ENABLE_SET_REG0</a> | 5283 F080h             |
| 3F0C0h | 32     | <a href="#">CPSW_NC_ECC_SEC_ENABLE_CLR_REG0</a> | 5283 F0C0h             |
| 3F13Ch | 32     | <a href="#">CPSW_NC_ECC_DED_EOI_REG</a>         | 5283 F13Ch             |
| 3F140h | 32     | <a href="#">CPSW_NC_ECC_DED_STATUS_REG0</a>     | 5283 F140h             |
| 3F180h | 32     | <a href="#">CPSW_NC_ECC_DED_ENABLE_SET_REG0</a> | 5283 F180h             |
| 3F1C0h | 32     | <a href="#">CPSW_NC_ECC_DED_ENABLE_CLR_REG0</a> | 5283 F1C0h             |
| 3F200h | 32     | <a href="#">CPSW_NC_ECC_AGGR_ENABLE_SET</a>     | 5283 F200h             |



**Table 5-1. CPSW Registers, Base Address=5280 0000h, Length=2097152 (continued)**

| Offset | Length | Register Name                               | CPSW0 Physical Address |
|--------|--------|---------------------------------------------|------------------------|
| 3F204h | 32     | <a href="#">CPSW_NC_ECC_AGGR_ENABLE_CLR</a> | 5283 F204h             |
| 3F208h | 32     | <a href="#">CPSW_NC_ECC_AGGR_STATUS_SET</a> | 5283 F208h             |
| 3F20Ch | 32     | <a href="#">CPSW_NC_ECC_AGGR_STATUS_CLR</a> | 5283 F20Ch             |

### 5.1.2 CPSW Registers

#### CPSW Registers

### 5.1.2.1 CPSW\_IDVER\_REG Register

#### 1 CPSW\_IDVER\_REG Register (Offset = 0h) [reset = 6BA03103h]

ID Version Register.

Return to [Summary Table](#)

**Table 5-2. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 0000h       |

**Figure 5-1. CPSW\_IDVER\_REG Name Register**

|           |    |    |    |           |    |    |    |
|-----------|----|----|----|-----------|----|----|----|
| 31        | 30 | 29 | 28 | 27        | 26 | 25 | 24 |
| IDENT     |    |    |    |           |    |    |    |
| R         |    |    |    |           |    |    |    |
| 6BA0h     |    |    |    |           |    |    |    |
| 23        | 22 | 21 | 20 | 19        | 18 | 17 | 16 |
| IDENT     |    |    |    |           |    |    |    |
| R         |    |    |    |           |    |    |    |
| 6BA0h     |    |    |    |           |    |    |    |
| 15        | 14 | 13 | 12 | 11        | 10 | 9  | 8  |
| RTL_VER   |    |    |    | MAJOR_VER |    |    |    |
| R         |    |    |    | R         |    |    |    |
| 3h        |    |    |    | 1h        |    |    |    |
| 7         | 6  | 5  | 4  | 3         | 2  | 1  | 0  |
| MINOR_VER |    |    |    |           |    |    |    |
| R         |    |    |    |           |    |    |    |
| 3h        |    |    |    |           |    |    |    |

**Table 5-4. CPSW\_IDVER\_REG Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description          |
|-------|-----------|------|-------|----------------------|
| 31:16 | IDENT     | R    | 6BA0h | Identification value |
| 15:11 | RTL_VER   | R    | 3h    | RTL version value    |
| 10:8  | MAJOR_VER | R    | 1h    | Major version value  |
| 7:0   | MINOR_VER | R    | 3h    | Minor version value  |

### 5.1.2.2 CPSW\_SS\_SYNCE\_COUNT\_REG Register

#### 1 CPSW\_SS\_SYNCE\_COUNT\_REG Register (Offset = 4h) [reset = 0h]

SS SYNCE Count Register.

Return to [Summary Table](#)

**Table 5-5. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 0004h       |

**Figure 5-2. CPSW\_SS\_SYNCE\_COUNT\_REG Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SYNCE_CNT |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SYNCE_CNT |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SYNCE_CNT |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SYNCE_CNT |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 5-7. CPSW\_SS\_SYNCE\_COUNT\_REG Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                       |
|------|-----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | SYNCE_CNT | R/W  | 0h    | SyncE Count Value - This value determines the toggle rate of the TS_SYNCE output. When this value is zero the TS_SYNCE output is disabled (low). When this value is non-zero, the TS_SYNCE output toggles each time the synce count value is reached. If this value is to be changed to another non-zero value then it should be written with a zero value before Writing the new non-zero value. |

### 5.1.2.3 CPSW\_SS\_SYNCE\_MUX\_REG Register

#### 1 CPSW\_SS\_SYNCE\_MUX\_REG Register (Offset = 8h) [reset = 0h]

SS Synce Mux Register.

Return to [Summary Table](#)

**Table 5-8. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 0008h       |

**Figure 5-3. CPSW\_SS\_SYNCE\_MUX\_REG Name Register**

|          |    |           |    |                |    |    |    |
|----------|----|-----------|----|----------------|----|----|----|
| 31       | 30 | 29        | 28 | 27             | 26 | 25 | 24 |
| RESERVED |    |           |    |                |    |    |    |
| NONE     |    |           |    |                |    |    |    |
| 0h       |    |           |    |                |    |    |    |
| 23       | 22 | 21        | 20 | 19             | 18 | 17 | 16 |
| RESERVED |    |           |    |                |    |    |    |
| NONE     |    |           |    |                |    |    |    |
| 0h       |    |           |    |                |    |    |    |
| 15       | 14 | 13        | 12 | 11             | 10 | 9  | 8  |
| RESERVED |    |           |    |                |    |    |    |
| NONE     |    |           |    |                |    |    |    |
| 0h       |    |           |    |                |    |    |    |
| 7        | 6  | 5         | 4  | 3              | 2  | 1  | 0  |
| RESERVED |    | SYNCE_SEL |    | SYNCE_PORT_SEL |    |    |    |
| NONE     |    | R/W       |    | R/W            |    |    |    |
| 0h       |    | 0h        |    | 0h             |    |    |    |

**Table 5-10. CPSW\_SS\_SYNCE\_MUX\_REG Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                        |
|------|----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:6 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                           |
| 5:4  | SYNCE_SEL      | R/W  | 0h    | Sync E Interface Select.<br>00 - GMII <sub>n</sub> _MRCLK <sub>I</sub> input clock from selected GMII port<br>01 - RMII_MHZ_50_CLK (same for all ports if RMII included)<br>10 - RGMII <sub>n</sub> _RXC <sub>I</sub> input clock from selected port (If RGMII included)<br>11 - SERDES <sub>n</sub> _RXCLK from selected port (If SGMII included) |
| 3:0  | SYNCE_PORT_SEL | R/W  | 0h    | Sync E Port Select - This field selects the port that will be used for the synchronous Ethernet receive clock. The port interface is selected with synce_sel.<br>0 - Port 1<br>1 - Port 2<br>...<br>7 - Port 8<br>8-15 - Reserved                                                                                                                  |

### 5.1.2.4 CPSW\_SS\_CONTROL\_REG Register

#### 1 CPSW\_SS\_CONTROL\_REG Register (Offset = Ch) [reset = 0h]

SS Control Register.

Return to [Summary Table](#)

**Table 5-11. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 000Ch       |

**Figure 5-4. CPSW\_SS\_CONTROL\_REG Name Register**

|          |    |    |    |    |    |                  |        |
|----------|----|----|----|----|----|------------------|--------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25               | 24     |
| RESERVED |    |    |    |    |    |                  |        |
| NONE     |    |    |    |    |    |                  |        |
| 0h       |    |    |    |    |    |                  |        |
| 23       | 22 | 21 | 20 | 19 | 18 | 17               | 16     |
| RESERVED |    |    |    |    |    |                  |        |
| NONE     |    |    |    |    |    |                  |        |
| 0h       |    |    |    |    |    |                  |        |
| 15       | 14 | 13 | 12 | 11 | 10 | 9                | 8      |
| RESERVED |    |    |    |    |    |                  |        |
| NONE     |    |    |    |    |    |                  |        |
| 0h       |    |    |    |    |    |                  |        |
| 7        | 6  | 5  | 4  | 3  | 2  | 1                | 0      |
| RESERVED |    |    |    |    |    | EEE_PHY_ONL<br>Y | EEE_EN |
| NONE     |    |    |    |    |    | R/W              | R/W    |
| 0h       |    |    |    |    |    | 0h               | 0h     |

**Table 5-13. CPSW\_SS\_CONTROL\_REG Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                                                                                                                                   |
|------|--------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED     | NONE | 0h    | Reserved                                                                                                                                                                                                      |
| 1    | EEE_PHY_ONLY | R/W  | 0h    | Energy Efficient Enable Phy Only Mode.<br>0 - The low power indicate state (LPI) includes gating off the CPPI_GCLK to the CPSW.<br>1 - The low power indicate state (LPI) does not gate the clock to the CPSW |
| 0    | EEE_EN       | R/W  | 0h    | Energy Efficient Ethernet Enable.<br>0 - EEE is disabled<br>1 - EEE is enabled                                                                                                                                |

### 5.1.2.5 CPSW\_SS\_INT\_CONTROL\_REG Register

#### 1 CPSW\_SS\_INT\_CONTROL\_REG Register (Offset = 18h) [reset = 0h]

SS Interrupt Control Register.

Return to [Summary Table](#)

**Table 5-14. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 0018h       |

**Figure 5-5. CPSW\_SS\_INT\_CONTROL\_REG Name Register**

|              |                |             |    |              |    |    |    |
|--------------|----------------|-------------|----|--------------|----|----|----|
| 31           | 30             | 29          | 28 | 27           | 26 | 25 | 24 |
| INT_TEST     | INT_SEL_VEC_EN | RESERVED    |    |              |    |    |    |
| R/W          | R/W            | NONE        |    |              |    |    |    |
| 0h           | 0h             | 0h          |    |              |    |    |    |
| 23           | 22             | 21          | 20 | 19           | 18 | 17 | 16 |
| RESERVED     |                | INT_PACE_EN |    |              |    |    |    |
| NONE         |                | R/W         |    |              |    |    |    |
| 0h           |                | 0h          |    |              |    |    |    |
| 15           | 14             | 13          | 12 | 11           | 10 | 9  | 8  |
| RESERVED     |                |             |    | INT_PRESCALE |    |    |    |
| NONE         |                |             |    | R/W          |    |    |    |
| 0h           |                |             |    | 0h           |    |    |    |
| 7            | 6              | 5           | 4  | 3            | 2  | 1  | 0  |
| INT_PRESCALE |                |             |    |              |    |    |    |
| R/W          |                |             |    |              |    |    |    |
| 0h           |                |             |    |              |    |    |    |

**Table 5-16. CPSW\_SS\_INT\_CONTROL\_REG Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | INT_TEST       | R/W  | 0h    | Interrupt Test - Test bit to the interrupt pacing blocks                                                                                                                                                                                                                                                                                                                                                                                             |
| 30    | INT_SEL_VEC_EN | R/W  | 0h    | Interrupt Select Vector Enable.<br>0 - in_vector is an 8-bit mask for tx_pend, rx_pend, and rx_thresh_pend.<br>1 - in_vector is the 3-bit encoded value of the highest interrupt channel set for tx_pend, rx_pend, and rx_thresh_pend.                                                                                                                                                                                                               |
| 29:22 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 21:16 | INT_PACE_EN    | R/W  | 0h    | Interrupt Pacing Enable Bus.<br>int_pace_en[0] - Enables C0_Rx_Pulse Pacing (0 is pacing bypass)<br>int_pace_en[1] - Enables C0_Tx_Pulse Pacing (0 is pacing bypass)<br>int_pace_en[2] - Enables C1_Rx_Pulse Pacing (0 is pacing bypass)<br>int_pace_en[3] - Enables C1_Tx_Pulse Pacing (0 is pacing bypass)<br>int_pace_en[4] - Enables C2_Rx_Pulse Pacing (0 is pacing bypass)<br>int_pace_en[5] - Enables C2_Tx_Pulse Pacing (0 is pacing bypass) |
| 15:12 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 11:0  | INT_PRESCALE   | R/W  | 0h    | Interrupt Counter Prescaler - The number of VBUSP_CLK periods in 4us.                                                                                                                                                                                                                                                                                                                                                                                |

### 5.1.2.6 CPSW\_SS\_STATUS\_REG Register

#### 1 CPSW\_SS\_STATUS\_REG Register (Offset = 1Ch) [reset = 0h]

SS Status Register.

Return to [Summary Table](#)

**Table 5-17. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 001Ch       |

**Figure 5-6. CPSW\_SS\_STATUS\_REG Name Register**

|          |    |    |    |    |    |    |                 |
|----------|----|----|----|----|----|----|-----------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24              |
| RESERVED |    |    |    |    |    |    |                 |
| NONE     |    |    |    |    |    |    |                 |
| 0h       |    |    |    |    |    |    |                 |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16              |
| RESERVED |    |    |    |    |    |    |                 |
| NONE     |    |    |    |    |    |    |                 |
| 0h       |    |    |    |    |    |    |                 |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8               |
| RESERVED |    |    |    |    |    |    |                 |
| NONE     |    |    |    |    |    |    |                 |
| 0h       |    |    |    |    |    |    |                 |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0               |
| RESERVED |    |    |    |    |    |    | EEE_CLKSTOP_ACK |
| NONE     |    |    |    |    |    |    | R               |
| 0h       |    |    |    |    |    |    | 0h              |

**Table 5-19. CPSW\_SS\_STATUS\_REG Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                               |
|------|-----------------|------|-------|-----------------------------------------------------------|
| 31:1 | RESERVED        | NONE | 0h    | Reserved                                                  |
| 0    | EEE_CLKSTOP_ACK | R    | 0h    | Energy Efficient Ethernet clockstop acknowledge from CPSW |

### 5.1.2.7 CPSW\_SUBSYSTEM\_CONFIG\_REG Register

#### 1 CPSW\_SUBSYSTEM\_CONFIG\_REG Register (Offset = 20h) [reset = 30203h]

Subsystem Configuration Register.

Return to [Summary Table](#)

**Table 5-20. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 0020h       |

**Figure 5-7. CPSW\_SUBSYSTEM\_CONFIG\_REG Name Register**

|           |    |    |    |          |       |       |      |
|-----------|----|----|----|----------|-------|-------|------|
| 31        | 30 | 29 | 28 | 27       | 26    | 25    | 24   |
| RESERVED  |    |    |    | XGMII    |       |       |      |
| NONE      |    |    |    | R        |       |       |      |
| 0h        |    |    |    | 0h       |       |       |      |
| 23        | 22 | 21 | 20 | 19       | 18    | 17    | 16   |
| XGMII     |    |    |    | QSGMII   | SGMII | RGMII | RMII |
| R         |    |    |    | R        | R     | R     | R    |
| 0h        |    |    |    | 0h       | 0h    | 1h    | 1h   |
| 15        | 14 | 13 | 12 | 11       | 10    | 9     | 8    |
| RESERVED  |    |    |    | NUM_GENF |       |       |      |
| NONE      |    |    |    | R        |       |       |      |
| 0h        |    |    |    | 2h       |       |       |      |
| 7         | 6  | 5  | 4  | 3        | 2     | 1     | 0    |
| NUM_PORTS |    |    |    |          |       |       |      |
| R         |    |    |    |          |       |       |      |
| 3h        |    |    |    |          |       |       |      |

**Table 5-22. CPSW\_SUBSYSTEM\_CONFIG\_REG Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                         |
|-------|-----------|------|-------|-----------------------------------------------------|
| 31:28 | RESERVED  | NONE | 0h    | Reserved                                            |
| 27:20 | XGMII     | R    | 0h    | The Number of XGMII Ports included in the CPSW      |
| 19    | QSGMII    | R    | 0h    | QSGMII is included in the CPSW                      |
| 18    | SGMII     | R    | 0h    | SGMII is included in the CPSW                       |
| 17    | RGMII     | R    | 1h    | RGMII is included in the CPSW                       |
| 16    | RMII      | R    | 1h    | RMII is included in the CPSW                        |
| 15:13 | RESERVED  | NONE | 0h    | Reserved                                            |
| 12:8  | NUM_GENF  | R    | 2h    | The number of CPTS GENF outputs                     |
| 7:0   | NUM_PORTS | R    | 3h    | The total number of ports including the host port 0 |



### 5.1.2.8 CPSW\_RGMII1\_STATUS\_REG Register

#### 1 CPSW\_RGMII1\_STATUS\_REG Register (Offset = 30h) [reset = 0h]

RGMII1 Status Register.

Return to [Summary Table](#)

**Table 5-23. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 0030h       |

**Figure 5-8. CPSW\_RGMII1\_STATUS\_REG Name Register**

|          |    |    |    |            |       |    |      |
|----------|----|----|----|------------|-------|----|------|
| 31       | 30 | 29 | 28 | 27         | 26    | 25 | 24   |
| RESERVED |    |    |    |            |       |    |      |
| NONE     |    |    |    |            |       |    |      |
| 0h       |    |    |    |            |       |    |      |
| 23       | 22 | 21 | 20 | 19         | 18    | 17 | 16   |
| RESERVED |    |    |    |            |       |    |      |
| NONE     |    |    |    |            |       |    |      |
| 0h       |    |    |    |            |       |    |      |
| 15       | 14 | 13 | 12 | 11         | 10    | 9  | 8    |
| RESERVED |    |    |    |            |       |    |      |
| NONE     |    |    |    |            |       |    |      |
| 0h       |    |    |    |            |       |    |      |
| 7        | 6  | 5  | 4  | 3          | 2     | 1  | 0    |
| RESERVED |    |    |    | FULLDUPLEX | SPEED |    | LINK |
| NONE     |    |    |    | R          | R     |    | R    |
| 0h       |    |    |    | 0h         | 0h    |    | 0h   |

**Table 5-25. CPSW\_RGMII1\_STATUS\_REG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                   |
|------|------------|------|-------|-------------------------------------------------------------------------------|
| 31:4 | RESERVED   | NONE | 0h    | Reserved                                                                      |
| 3    | FULLDUPLEX | R    | 0h    | Rgmii1 Full-duplex<br>0 - Half-duplex<br>1 - Full-duplex                      |
| 2:1  | SPEED      | R    | 0h    | Rgmii1 Speed<br>00 - 10Mbps<br>01 - 100Mbps<br>10 - 1000Mbps<br>11 - reserved |
| 0    | LINK       | R    | 0h    | Rgmii1 Link Indicator<br>0 - Link is down<br>1 - Link is up                   |

### 5.1.2.9 CPSW\_RGMII2\_STATUS\_REG Register

#### 1 CPSW\_RGMII2\_STATUS\_REG Register (Offset = 34h) [reset = 0h]

RGMII2 Status Register.

Return to [Summary Table](#)

**Table 5-26. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 0034h       |

**Figure 5-9. CPSW\_RGMII2\_STATUS\_REG Name Register**

|          |    |    |    |            |       |    |      |
|----------|----|----|----|------------|-------|----|------|
| 31       | 30 | 29 | 28 | 27         | 26    | 25 | 24   |
| RESERVED |    |    |    |            |       |    |      |
| NONE     |    |    |    |            |       |    |      |
| 0h       |    |    |    |            |       |    |      |
| 23       | 22 | 21 | 20 | 19         | 18    | 17 | 16   |
| RESERVED |    |    |    |            |       |    |      |
| NONE     |    |    |    |            |       |    |      |
| 0h       |    |    |    |            |       |    |      |
| 15       | 14 | 13 | 12 | 11         | 10    | 9  | 8    |
| RESERVED |    |    |    |            |       |    |      |
| NONE     |    |    |    |            |       |    |      |
| 0h       |    |    |    |            |       |    |      |
| 7        | 6  | 5  | 4  | 3          | 2     | 1  | 0    |
| RESERVED |    |    |    | FULLDUPLEX | SPEED |    | LINK |
| NONE     |    |    |    | R          | R     |    | R    |
| 0h       |    |    |    | 0h         | 0h    |    | 0h   |

**Table 5-28. CPSW\_RGMII2\_STATUS\_REG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                   |
|------|------------|------|-------|-------------------------------------------------------------------------------|
| 31:4 | RESERVED   | NONE | 0h    | Reserved                                                                      |
| 3    | FULLDUPLEX | R    | 0h    | Rgmii2 Full-duplex<br>0 - Half-duplex<br>1 - Full-duplex                      |
| 2:1  | SPEED      | R    | 0h    | Rgmii2 Speed<br>00 - 10Mbps<br>01 - 100Mbps<br>10 - 1000Mbps<br>11 - reserved |
| 0    | LINK       | R    | 0h    | Rgmii2 Link Indicator<br>0 - Link is down<br>1 - Link is up                   |

### 5.1.2.10 CPSW\_MDIO\_VERSION\_REG Register

#### 1 CPSW\_MDIO\_VERSION\_REG Register (Offset = F00h) [reset = 71107h]

MDIO Version Register

Return to [Summary Table](#)
**Table 5-29. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 0F00h       |

**Figure 5-10. CPSW\_MDIO\_VERSION\_REG Name Register**

|           |    |        |    |           |        |    |    |
|-----------|----|--------|----|-----------|--------|----|----|
| 31        | 30 | 29     | 28 | 27        | 26     | 25 | 24 |
| SCHEME    |    | BU     |    | MODULE_ID |        |    |    |
| R         |    | R      |    | R         |        |    |    |
| 0h        |    | 0h     |    | 7h        |        |    |    |
| 23        | 22 | 21     | 20 | 19        | 18     | 17 | 16 |
| MODULE_ID |    |        |    |           |        |    |    |
| R         |    |        |    |           |        |    |    |
| 7h        |    |        |    |           |        |    |    |
| 15        | 14 | 13     | 12 | 11        | 10     | 9  | 8  |
| REVRTL    |    |        |    |           | REVMAJ |    |    |
| R         |    |        |    |           | R      |    |    |
| 2h        |    |        |    |           | 1h     |    |    |
| 7         | 6  | 5      | 4  | 3         | 2      | 1  | 0  |
| CUSTOM    |    | REVMIN |    |           |        |    |    |
| R         |    | R      |    |           |        |    |    |
| 0h        |    | 7h     |    |           |        |    |    |

**Table 5-31. CPSW\_MDIO\_VERSION\_REG Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description    |
|-------|-----------|------|-------|----------------|
| 31:30 | SCHEME    | R    | 0h    | Scheme         |
| 29:28 | BU        | R    | 0h    | bu             |
| 27:16 | MODULE_ID | R    | 7h    | Module ID      |
| 15:11 | REVRTL    | R    | 2h    | RTL version    |
| 10:8  | REVMAJ    | R    | 1h    | Major version  |
| 7:6   | CUSTOM    | R    | 0h    | Custom version |
| 5:0   | REVMIN    | R    | 7h    | Minor version  |

### 5.1.2.11 CPSW\_MDIO\_CONTROL\_REG Register

#### 1 CPSW\_MDIO\_CONTROL\_REG Register (Offset = F04h) [reset = 81000FFh]

MDIO Control Register

Return to [Summary Table](#)
**Table 5-32. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 0F04h       |

**Figure 5-11. CPSW\_MDIO\_CONTROL\_REG Name Register**

| 31       | 30     | 29       | 28                   | 27    | 26                  | 25              | 24       |
|----------|--------|----------|----------------------|-------|---------------------|-----------------|----------|
| IDLE     | ENABLE | RESERVED | HIGHEST_USER_CHANNEL |       |                     |                 |          |
| R        | R/W    | NONE     | R                    |       |                     |                 |          |
| 1h       | 0h     | 0h       | 1h                   |       |                     |                 |          |
| 23       | 22     | 21       | 20                   | 19    | 18                  | 17              | 16       |
| RESERVED |        |          | PREAMBLE             | FAULT | FAULT_DETECT_ENABLE | INT_TEST_ENABLE | RESERVED |
| NONE     |        |          | R/W                  | R/W   | R/W                 | R/W             | NONE     |
| 0h       |        |          | 0h                   | 0h    | 0h                  | 0h              | 0h       |
| 15       | 14     | 13       | 12                   | 11    | 10                  | 9               | 8        |
| CLKDIV   |        |          |                      |       |                     |                 |          |
| R/W      |        |          |                      |       |                     |                 |          |
| FFh      |        |          |                      |       |                     |                 |          |
| 7        | 6      | 5        | 4                    | 3     | 2                   | 1               | 0        |
| CLKDIV   |        |          |                      |       |                     |                 |          |
| R/W      |        |          |                      |       |                     |                 |          |
| FFh      |        |          |                      |       |                     |                 |          |

**Table 5-34. CPSW\_MDIO\_CONTROL\_REG Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description                                                                                                                                                                                                                                                                                                                            |
|-------|----------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | IDLE                 | R    | 1h    | MDIO state machine IDLE. Set to 1 by the hardware when the state machine is in the idle state.                                                                                                                                                                                                                                         |
| 30    | ENABLE               | R/W  | 0h    | Enable control. Writing a 1 to this bit enables the MDIO state machine, writing a 0 disables it. If the MDIO state machine is active at the time it is disabled, it will complete the current operation before halting and setting the idle bit. If using byte access, the enable bit has to be the last bit written in this register. |
| 29    | RESERVED             | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                               |
| 28:24 | HIGHEST_USER_CHANNEL | R    | 1h    | Highest user channel. This field specifies the highest user access channel that is available in the module and is currently set to 1. This implies that MDIOUserAccess1 is the highest available user access channel.                                                                                                                  |
| 23:21 | RESERVED             | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                               |
| 20    | PREAMBLE             | R/W  | 0h    | Preamble disable. Writing a 1 to this bit disables this device from sending MDIO frame preambles in clause 22 mode of operation. This bit has no effect in clause 45 mode of operation.                                                                                                                                                |
| 19    | FAULT                | R/W  | 0h    | Fault indicator. This bit is set to 1 if the MDIO pins fail to read back what the device is driving onto them. This indicates a physical layer fault and the module state machine is reset. Writing a 1 to it clears this bit.                                                                                                         |
| 18    | FAULT_DETECT_ENABLE  | R/W  | 0h    | Fault detect enable. This bit has to be set to 1 to enable the physical layer fault detection.                                                                                                                                                                                                                                         |

**Table 5-34. CPSW\_MDIO\_CONTROL\_REG Register Field Descriptions (continued)**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                           |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 17   | INT_TEST_ENABLE | R/W  | 0h    | Interrupt test enable. This bit can be set to 1 to enable the host to set the userint and linkint bits for test purposes.                                                             |
| 16   | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                              |
| 15:0 | CLKDIV          | R/W  | FFh   | Clock Divider. This field specifies the division ratio between CLK and the frequency of MDCLK. MDCLK is disabled when clkdiv is set to 0. MDCLK frequency = clk frequency/(clkdiv+1). |

### 5.1.2.12 CPSW\_MDIO\_ALIVE\_REG Register

#### 1 CPSW\_MDIO\_ALIVE\_REG Register (Offset = F08h) [reset = 0h]

MDIO Alive Register

Return to [Summary Table](#)
**Table 5-35. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 0F08h       |

**Figure 5-12. CPSW\_MDIO\_ALIVE\_REG Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ALIVE |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ALIVE |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ALIVE |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ALIVE |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-37. CPSW\_MDIO\_ALIVE\_REG Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ALIVE | R/W  | 0h    | MDIO Alive. Each of the 32 bits of this register is set if the most recent access to the PHY with address corresponding to the register bit number was acknowledged by the PHY, the bit is reset if the PHY fails to acknowledge the access. Both the user and polling accesses to a PHY will cause the corresponding alive bit to be updated. The alive bits are intended to be used to give an indication of the presence or not of the PHY with the corresponding address. Writing a 1 to any bit will clear it, writing a 0 has no effect. |

### 5.1.2.13 CPSW\_MDIO\_LINK\_REG Register

#### 1 CPSW\_MDIO\_LINK\_REG Register (Offset = F0Ch) [reset = 0h]

MDIO Link Register

Return to [Summary Table](#)
**Table 5-38. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 0F0Ch       |

**Figure 5-13. CPSW\_MDIO\_LINK\_REG Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| LINK |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LINK |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| LINK |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LINK |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-40. CPSW\_MDIO\_LINK\_REG Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | LINK  | R    | 0h    | MDIO Link state. This register is updated after a read of the Generic Status Register of a PHY. The corresponding bit is set if the PHY with the corresponding address has link and the PHY acknowledges the read transaction. The bit is cleared to zero if the PHY indicates it does not have link or fails to acknowledge the read transaction. Writes to the register have no effect. In addition, in Normal Mode Operation, the status of the two PHYs specified in the MDIOUserPhySel registers can be determined using the MLINK input pins. This is determined by the linksel bit in the MDIOUserPhySel register. In State Change Mode the MLINK input pins are unused. |

#### 5.1.2.14 CPSW\_MDIO\_LINK\_INT\_RAW\_REG Register

#### 1 CPSW\_MDIO\_LINK\_INT\_RAW\_REG Register (Offset = F10h) [reset = 0h]

MDIO Link Interrupt Raw Register

Return to [Summary Table](#)

**Table 5-41. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 0F10h       |

**Figure 5-14. CPSW\_MDIO\_LINK\_INT\_RAW\_REG Name Register**

|          |    |    |    |    |    |            |    |
|----------|----|----|----|----|----|------------|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25         | 24 |
| RESERVED |    |    |    |    |    |            |    |
| NONE     |    |    |    |    |    |            |    |
| 0h       |    |    |    |    |    |            |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17         | 16 |
| RESERVED |    |    |    |    |    |            |    |
| NONE     |    |    |    |    |    |            |    |
| 0h       |    |    |    |    |    |            |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9          | 8  |
| RESERVED |    |    |    |    |    |            |    |
| NONE     |    |    |    |    |    |            |    |
| 0h       |    |    |    |    |    |            |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1          | 0  |
| RESERVED |    |    |    |    |    | LINKINTRAW |    |
| NONE     |    |    |    |    |    | R/W        |    |
| 0h       |    |    |    |    |    | 0h         |    |

**Table 5-43. CPSW\_MDIO\_LINK\_INT\_RAW\_REG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 1:0  | LINKINTRAW | R/W  | 0h    | MDIO link change event raw value. Normal mode operation: When asserted, a bit indicates that there was an MDIO link change event (i.e. change in the MDIOLink register) corresponding to the PHY address in the MDIOUserPhySel register. linkintraw[0] and linkintraw[1] correspond to MDIOUserPhySel0 and MDIOUserPhySel1, respectively. Writing a 1 will clear the event and writing 0 has no effect. If the int_test bit in the MDIOControl register is set, the host may set linkintraw bits to a 1 which may be used for test purposes.<br>MDIO link change event raw value. State Change Mode operation: The linkintraw[0] bit will be asserted when any bit (for any PHY) in the MDIOAlive or MDIOLink registers changes due to MDIO operations. The linkintraw[1] bit is unused in State Change Mode. State Change Mode allows any state change in any PHY to issue an interrupt. If the int_test bit in the MDIOControl register is set, the host may set the linkintraw[0] bit high which may be used for test purposes. |



### 5.1.2.15 CPSW\_MDIO\_LINK\_INT\_MASKED\_REG Register

#### 1 CPSW\_MDIO\_LINK\_INT\_MASKED\_REG Register (Offset = F14h) [reset = 0h]

MDIO Link Interrupt Masked Register

Return to [Summary Table](#)
**Table 5-44. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 0F14h       |

**Figure 5-15. CPSW\_MDIO\_LINK\_INT\_MASKED\_REG Name Register**

|          |    |    |    |    |    |               |    |
|----------|----|----|----|----|----|---------------|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25            | 24 |
| RESERVED |    |    |    |    |    |               |    |
| NONE     |    |    |    |    |    |               |    |
| 0h       |    |    |    |    |    |               |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17            | 16 |
| RESERVED |    |    |    |    |    |               |    |
| NONE     |    |    |    |    |    |               |    |
| 0h       |    |    |    |    |    |               |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9             | 8  |
| RESERVED |    |    |    |    |    |               |    |
| NONE     |    |    |    |    |    |               |    |
| 0h       |    |    |    |    |    |               |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1             | 0  |
| RESERVED |    |    |    |    |    | LINKINTMASKED |    |
| NONE     |    |    |    |    |    | R/W           |    |
| 0h       |    |    |    |    |    | 0h            |    |

**Table 5-46. CPSW\_MDIO\_LINK\_INT\_MASKED\_REG Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|------|---------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED      | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 1:0  | LINKINTMASKED | R/W  | 0h    | MDIO link change interrupt masked value. Normal mode operation:<br>When asserted, a bit indicates that there was an MDIO link change event (i.e. change in the MDIOLink register) corresponding to the PHY address in the MDIOUserPhySel register and the corresponding linkint_enable bit was set. linkintmasked[0] and linkintmasked[1] correspond to MDIOUserPhySel0 and MDIOUserPhySel1, respectively. Writing a 1 will clear the interrupt and writing 0 has no effect. These masked interrupt bits are the MDIO_LINKINT[1:0] pin values.<br>MDIO link change interrupt masked value. State Change Mode operation:<br>The linkintmasked[0] bit will be asserted when linkintraw[0] is asserted and when the linkintmaskset bit is set to 1. Writing a 1 will clear linkintmasked[0] (and the MDIO_LINKINT[0] output) and writing 0 has no effect. The linkintmasked[1] bit is not used in State Change Mode (MDIO_LINKINT[1] is therefore also unused in State Change Mode). |

### 5.1.2.16 CPSW\_MDIO\_LINK\_INT\_MASK\_SET\_REG Register

#### 1 CPSW\_MDIO\_LINK\_INT\_MASK\_SET\_REG Register (Offset = F18h) [reset = 0h]

MDIO Link Interrupt Mask Set Register

Return to [Summary Table](#)

**Table 5-47. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 0F18h       |

**Figure 5-16. CPSW\_MDIO\_LINK\_INT\_MASK\_SET\_REG Name Register**

|          |    |    |    |    |    |    |                    |
|----------|----|----|----|----|----|----|--------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24                 |
| RESERVED |    |    |    |    |    |    |                    |
| NONE     |    |    |    |    |    |    |                    |
| 0h       |    |    |    |    |    |    |                    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
| RESERVED |    |    |    |    |    |    |                    |
| NONE     |    |    |    |    |    |    |                    |
| 0h       |    |    |    |    |    |    |                    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8                  |
| RESERVED |    |    |    |    |    |    |                    |
| NONE     |    |    |    |    |    |    |                    |
| 0h       |    |    |    |    |    |    |                    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| RESERVED |    |    |    |    |    |    | LINKINTMASK<br>SET |
| NONE     |    |    |    |    |    |    | R/W                |
| 0h       |    |    |    |    |    |    | 0h                 |

**Table 5-49. CPSW\_MDIO\_LINK\_INT\_MASK\_SET\_REG Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|------|----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 0    | LINKINTMASKSET | R/W  | 0h    | MDIO link interrupt mask set. Normal Mode Operation:<br>This register is not used in normal mode. In normal mode the MDIO_LINKINT[1:0] interrupts are enabled with the linkint_enable bit in the associated MDIOUserPhySel0/1 register.<br>MDIO link interrupt mask set. State Change Mode Operation:<br>Writing this bit to 1 will enable the MDIO link status change interrupt (MDIO_LINKINT[0]) to be asserted when linkintraw[0] is asserted. |

### 5.1.2.17 CPSW\_MDIO\_LINK\_INT\_MASK\_CLEAR\_REG Register

#### 1 CPSW\_MDIO\_LINK\_INT\_MASK\_CLEAR\_REG Register (Offset = F1Ch) [reset = 0h]

MDIO Link Interrupt Mask Clear Register

Return to [Summary Table](#)

**Table 5-50. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 0F1Ch       |

**Figure 5-17. CPSW\_MDIO\_LINK\_INT\_MASK\_CLEAR\_REG Name Register**

|          |    |    |    |    |    |    |                 |
|----------|----|----|----|----|----|----|-----------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24              |
| RESERVED |    |    |    |    |    |    |                 |
| NONE     |    |    |    |    |    |    |                 |
| 0h       |    |    |    |    |    |    |                 |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16              |
| RESERVED |    |    |    |    |    |    |                 |
| NONE     |    |    |    |    |    |    |                 |
| 0h       |    |    |    |    |    |    |                 |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8               |
| RESERVED |    |    |    |    |    |    |                 |
| NONE     |    |    |    |    |    |    |                 |
| 0h       |    |    |    |    |    |    |                 |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0               |
| RESERVED |    |    |    |    |    |    | LINKINTMASK CLR |
| NONE     |    |    |    |    |    |    | R/W             |
| 0h       |    |    |    |    |    |    | 0h              |

**Table 5-52. CPSW\_MDIO\_LINK\_INT\_MASK\_CLEAR\_REG Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|------|----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 0    | LINKINTMASKCLR | R/W  | 0h    | MDIO link interrupt mask clear. Normal Mode Operation:<br>This register is not used in normal mode. In normal mode the MDIO_LINKINT[1:0] interrupts are enabled with the linkint_enable bit in the associated MDIOUserPhySel0/1 register.<br>MDIO link interrupt mask clear. State Change Mode Operation:<br>Writing this bit to 1 will disable the MDIO link status change interrupt (MDIO_LINKINT[0]) regardless of the linkintraw[0] bit value. |

### 5.1.2.18 CPSW\_MDIO\_USER\_INT\_RAW\_REG Register

#### 1 CPSW\_MDIO\_USER\_INT\_RAW\_REG Register (Offset = F20h) [reset = 0h]

MDIO User Interrupt Raw Register

Return to [Summary Table](#)

**Table 5-53. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 0F20h       |

**Figure 5-18. CPSW\_MDIO\_USER\_INT\_RAW\_REG Name Register**

|          |    |    |    |    |    |            |    |
|----------|----|----|----|----|----|------------|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25         | 24 |
| RESERVED |    |    |    |    |    |            |    |
| NONE     |    |    |    |    |    |            |    |
| 0h       |    |    |    |    |    |            |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17         | 16 |
| RESERVED |    |    |    |    |    |            |    |
| NONE     |    |    |    |    |    |            |    |
| 0h       |    |    |    |    |    |            |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9          | 8  |
| RESERVED |    |    |    |    |    |            |    |
| NONE     |    |    |    |    |    |            |    |
| 0h       |    |    |    |    |    |            |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1          | 0  |
| RESERVED |    |    |    |    |    | USERINTRAW |    |
| NONE     |    |    |    |    |    | R/W        |    |
| 0h       |    |    |    |    |    | 0h         |    |

**Table 5-55. CPSW\_MDIO\_USER\_INT\_RAW\_REG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 1:0  | USERINTRAW | R/W  | 0h    | Raw value of MDIO user command complete event for MDIOUserAccess1 through MDIOUserAccess0, respectively. When asserted, a bit indicates that the previously scheduled PHY read or write command using that particular MDIOUserAccess register has completed. Writing a 1 will clear the event and writing 0 has no effect. If the int_test bit in the MDIOControl register is set, the host may set the userintraw bits to a 1. This mode may be used for test purposes. |

### 5.1.2.19 CPSW\_MDIO\_USER\_INT\_MASKED\_REG Register

#### 1 CPSW\_MDIO\_USER\_INT\_MASKED\_REG Register (Offset = F24h) [reset = 0h]

MDIO User Interrupt Masked Register

Return to [Summary Table](#)

**Table 5-56. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 0F24h       |

**Figure 5-19. CPSW\_MDIO\_USER\_INT\_MASKED\_REG Name Register**

|          |    |    |    |    |    |               |    |
|----------|----|----|----|----|----|---------------|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25            | 24 |
| RESERVED |    |    |    |    |    |               |    |
| NONE     |    |    |    |    |    |               |    |
| 0h       |    |    |    |    |    |               |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17            | 16 |
| RESERVED |    |    |    |    |    |               |    |
| NONE     |    |    |    |    |    |               |    |
| 0h       |    |    |    |    |    |               |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9             | 8  |
| RESERVED |    |    |    |    |    |               |    |
| NONE     |    |    |    |    |    |               |    |
| 0h       |    |    |    |    |    |               |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1             | 0  |
| RESERVED |    |    |    |    |    | USERINTMASKED |    |
| NONE     |    |    |    |    |    | R/W           |    |
| 0h       |    |    |    |    |    | 0h            |    |

**Table 5-58. CPSW\_MDIO\_USER\_INT\_MASKED\_REG Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED      | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 1:0  | USERINTMASKED | R/W  | 0h    | Masked value of MDIO user command complete interrupt for MDIOUserAccess1 through MDIOUserAccess0, respectively. When asserted, a bit indicates that the previously scheduled PHY read or write command using that particular MDIOUserAccess register has completed and the corresponding userintmaskset bit is set to 1. Writing a 1 will clear the interrupt and writing 0 has no effect. If the int_test bit in the MDIOControl register is set, the host may set the userintmasked bits to a 1. This mode may be used for test purposes. |

### 5.1.2.20 CPSW\_MDIO\_USER\_INT\_MASK\_SET\_REG Register

#### 1 CPSW\_MDIO\_USER\_INT\_MASK\_SET\_REG Register (Offset = F28h) [reset = 0h]

MDIO User Interrupt Mask Set Register

Return to [Summary Table](#)

**Table 5-59. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 0F28h       |

**Figure 5-20. CPSW\_MDIO\_USER\_INT\_MASK\_SET\_REG Name Register**

|          |    |    |    |    |    |                |    |
|----------|----|----|----|----|----|----------------|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25             | 24 |
| RESERVED |    |    |    |    |    |                |    |
| NONE     |    |    |    |    |    |                |    |
| 0h       |    |    |    |    |    |                |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17             | 16 |
| RESERVED |    |    |    |    |    |                |    |
| NONE     |    |    |    |    |    |                |    |
| 0h       |    |    |    |    |    |                |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9              | 8  |
| RESERVED |    |    |    |    |    |                |    |
| NONE     |    |    |    |    |    |                |    |
| 0h       |    |    |    |    |    |                |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1              | 0  |
| RESERVED |    |    |    |    |    | USERINTMASKSET |    |
| NONE     |    |    |    |    |    | R/W            |    |
| 0h       |    |    |    |    |    | 0h             |    |

**Table 5-61. CPSW\_MDIO\_USER\_INT\_MASK\_SET\_REG Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                              |
|------|----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                 |
| 1:0  | USERINTMASKSET | R/W  | 0h    | MDIO user interrupt mask set for userintmasked[1:0], respectively. Writing a bit to 1 will enable MDIO user command complete interrupts for that particular MDIOUserAccess register. MDIO user interrupt for a particular MDIOUserAccess register is disabled if the corresponding bit is 0. Writing a 0 to this register has no effect. |

### 5.1.2.21 CPSW\_MDIO\_USER\_INT\_MASK\_CLEAR\_REG Register

#### 1 CPSW\_MDIO\_USER\_INT\_MASK\_CLEAR\_REG Register (Offset = F2Ch) [reset = 0h]

MDIO User Interrupt Mask Clear Register

Return to [Summary Table](#)

**Table 5-62. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 0F2Ch       |

**Figure 5-21. CPSW\_MDIO\_USER\_INT\_MASK\_CLEAR\_REG Name Register**

|          |    |    |    |    |    |                |    |
|----------|----|----|----|----|----|----------------|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25             | 24 |
| RESERVED |    |    |    |    |    |                |    |
| NONE     |    |    |    |    |    |                |    |
| 0h       |    |    |    |    |    |                |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17             | 16 |
| RESERVED |    |    |    |    |    |                |    |
| NONE     |    |    |    |    |    |                |    |
| 0h       |    |    |    |    |    |                |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9              | 8  |
| RESERVED |    |    |    |    |    |                |    |
| NONE     |    |    |    |    |    |                |    |
| 0h       |    |    |    |    |    |                |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1              | 0  |
| RESERVED |    |    |    |    |    | USERINTMASKCLR |    |
| NONE     |    |    |    |    |    | R/W            |    |
| 0h       |    |    |    |    |    | 0h             |    |

**Table 5-64. CPSW\_MDIO\_USER\_INT\_MASK\_CLEAR\_REG Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                                                                                                                                                                             |
|------|----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                |
| 1:0  | USERINTMASKCLR | R/W  | 0h    | MDIO user command complete interrupt mask clear for userintmasked[1:0], respectively. Writing a bit to 1 will disable further user command complete interrupts for that particular MDIOUserAccess register. Writing a 0 to this register has no effect. |

### 5.1.2.22 CPSW\_MDIO\_MANUAL\_IF\_REG Register

#### 1 CPSW\_MDIO\_MANUAL\_IF\_REG Register (Offset = F30h) [reset = 0h]

MDIO Manual Interface Register

Return to [Summary Table](#)

**Table 5-65. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 0F30h       |

**Figure 5-22. CPSW\_MDIO\_MANUAL\_IF\_REG Name Register**

|          |    |    |    |    |              |         |          |
|----------|----|----|----|----|--------------|---------|----------|
| 31       | 30 | 29 | 28 | 27 | 26           | 25      | 24       |
| RESERVED |    |    |    |    |              |         |          |
| NONE     |    |    |    |    |              |         |          |
| 0h       |    |    |    |    |              |         |          |
| 23       | 22 | 21 | 20 | 19 | 18           | 17      | 16       |
| RESERVED |    |    |    |    |              |         |          |
| NONE     |    |    |    |    |              |         |          |
| 0h       |    |    |    |    |              |         |          |
| 15       | 14 | 13 | 12 | 11 | 10           | 9       | 8        |
| RESERVED |    |    |    |    |              |         |          |
| NONE     |    |    |    |    |              |         |          |
| 0h       |    |    |    |    |              |         |          |
| 7        | 6  | 5  | 4  | 3  | 2            | 1       | 0        |
| RESERVED |    |    |    |    | MDIO_MDCLK_O | MDIO_OE | MDIO_PIN |
| NONE     |    |    |    |    | R/W          | R/W     | R/W      |
| 0h       |    |    |    |    | 0h           | 0h      | 0h       |

**Table 5-67. CPSW\_MDIO\_MANUAL\_IF\_REG Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------|--------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED     | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 2    | MDIO_MDCLK_O | R/W  | 0h    | MDIO Clock Output - This value is the MDCLK_O output value when the manualmode bit is set in the MDIO_POLL_IPG register.                                                                                                                                                                                                                                                                                                                                       |
| 1    | MDIO_OE      | R/W  | 0h    | MDIO Output Enable - This value is inverted and output on the MDIO_OE_N output when the manualmode bit is set in the MDIO_POLL_IPG register.                                                                                                                                                                                                                                                                                                                   |
| 0    | MDIO_PIN     | R/W  | 0h    | MDIO_Pin Value - This is the external MDIO data pin value when the manualmode bit is set in the MDIO_POLL_IPG register. That is, this value is driven on the MDIO_O (the MDIO serial data output) when MDIO_OE is asserted. The read value for this bit comes from MDIO_I (the MDIO serial data input). If MDIO_OE is asserted and MDIO_PIN is written with a 1 then MDIO_PIN should read a 1 if there are no external devices pulling the MDIO data line low. |



### 5.1.2.23 CPSW\_MDIO\_POLL\_REG Register

#### 1 CPSW\_MDIO\_POLL\_REG Register (Offset = F34h) [reset = 0h]

MDIO Poll Register

Return to [Summary Table](#)
**Table 5-68. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 0F34h       |

**Figure 5-23. CPSW\_MDIO\_POLL\_REG Name Register**

|            |                     |          |    |    |    |    |    |
|------------|---------------------|----------|----|----|----|----|----|
| 31         | 30                  | 29       | 28 | 27 | 26 | 25 | 24 |
| MANUALMODE | STATECHANG<br>EMODE | RESERVED |    |    |    |    |    |
| R/W        | R/W                 | NONE     |    |    |    |    |    |
| 0h         | 0h                  | 0h       |    |    |    |    |    |
| 23         | 22                  | 21       | 20 | 19 | 18 | 17 | 16 |
| RESERVED   |                     |          |    |    |    |    |    |
| NONE       |                     |          |    |    |    |    |    |
| 0h         |                     |          |    |    |    |    |    |
| 15         | 14                  | 13       | 12 | 11 | 10 | 9  | 8  |
| RESERVED   |                     |          |    |    |    |    |    |
| NONE       |                     |          |    |    |    |    |    |
| 0h         |                     |          |    |    |    |    |    |
| 7          | 6                   | 5        | 4  | 3  | 2  | 1  | 0  |
| IPG        |                     |          |    |    |    |    |    |
| R/W        |                     |          |    |    |    |    |    |
| 0h         |                     |          |    |    |    |    |    |

**Table 5-70. CPSW\_MDIO\_POLL\_REG Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                 |
|------|-----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31   | MANUALMODE      | R/W  | 0h    | Polling Inter Packet Gap Value - This value is the number of MDCLK_O clocks between each poll when polling is enabled.                                                      |
| 30   | STATECHANGEMODE | R/W  | 0h    | State Change Mode - When set, the MDIO is operating in State Change Mode. When clear, the MDIO is operating in normal mode. State change mode effects interrupt operations. |
| 29:8 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                    |
| 7:0  | IPG             | R/W  | 0h    | Manual Mode - When set, the MDIO pins are directly controlled by software through the bits in the MDIOManual_IF register                                                    |

### 5.1.2.24 CPSW\_MDIO\_POLL\_EN\_REG Register

#### 1 CPSW\_MDIO\_POLL\_EN\_REG Register (Offset = F38h) [reset = FFFFFFFFh]

MDIO Poll Enable Register

Return to [Summary Table](#)
**Table 5-71. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 0F38h       |

**Figure 5-24. CPSW\_MDIO\_POLL\_EN\_REG Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| POLL_EN  |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| FFFFFFFh |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| POLL_EN  |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| FFFFFFFh |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| POLL_EN  |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| FFFFFFFh |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| POLL_EN  |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| FFFFFFFh |    |    |    |    |    |    |    |

**Table 5-73. CPSW\_MDIO\_POLL\_EN\_REG Register Field Descriptions**

| Bit  | Field   | Type | Reset    | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|------|---------|------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | POLL_EN | R/W  | FFFFFFFh | Poll Enable - When set, the bit indicates that the associated PHY will be included in polling operations. When clear, the associated PHY will not be polled. Each bit in this field is associated with a PHY. Bit zero is associated with PHY 0 and so on. Due to a limitation in the hardware, bit 31 must always be set, regardless of the value of the preamble disable bit in the MDIO_CONTROL register. However, there does not have to be a PHY at address 31. |

### 5.1.2.25 CPSW\_MDIO\_CLAUS45\_REG Register

#### 1 CPSW\_MDIO\_CLAUS45\_REG Register (Offset = F3Ch) [reset = 0h]

MDIO Clause45 Register

Return to [Summary Table](#)
**Table 5-74. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 0F3Ch       |

**Figure 5-25. CPSW\_MDIO\_CLAUS45\_REG Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CLAUSE45 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CLAUSE45 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CLAUSE45 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CLAUSE45 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-76. CPSW\_MDIO\_CLAUS45\_REG Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                        |
|------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CLAUSE45 | R/W  | 0h    | MDIO clause 45 mode. When a clause45 bit is cleared, the PHY associated with the clause45 bit is operating in the clause 22 mode. When set, the PHY associated with the clause45 bit is operating in the clause 45 mode. Bit 0 is associated with PHY 0 and so on. |

### 5.1.2.26 CPSW\_MDIO\_USER\_ADDR0\_REG Register

#### 1 CPSW\_MDIO\_USER\_ADDR0\_REG Register (Offset = F40h) [reset = 0h]

MDIO Address 0 Register

Return to [Summary Table](#)
**Table 5-77. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 0F40h       |

**Figure 5-26. CPSW\_MDIO\_USER\_ADDR0\_REG Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| USER_ADDR0 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| USER_ADDR0 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-79. CPSW\_MDIO\_USER\_ADDR0\_REG Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                        |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                           |
| 15:0  | USER_ADDR0 | R/W  | 0h    | User Address 0 - In clause 45 mode, this field value is the address transferred in the address transfer initiated before each MDIOUserAccess0 access. This is not used for PHYs operating in clause22 mode as there is no address transfer preceeding each MDIOUserAccess0 access. |

### 5.1.2.27 CPSW\_MDIO\_USER\_ADDR1\_REG Register

#### 1 CPSW\_MDIO\_USER\_ADDR1\_REG Register (Offset = F44h) [reset = 0h]

MDIO Address 1 Register

Return to [Summary Table](#)
**Table 5-80. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 0F44h       |

**Figure 5-27. CPSW\_MDIO\_USER\_ADDR1\_REG Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| USER_ADDR1 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| USER_ADDR1 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-82. CPSW\_MDIO\_USER\_ADDR1\_REG Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                        |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                           |
| 15:0  | USER_ADDR1 | R/W  | 0h    | User Address 1 - In clause 45 mode, this field value is the address transferred in the address transfer initiated before each MDIOUserAccess1 access. This is not used for PHYs operating in clause22 mode as there is no address transfer preceeding each MDIOUserAccess1 access. |

### 5.1.2.28 CPSW\_MDIO\_USER\_GROUP\_USER\_ACCESS\_REG\_K Register

#### 1 CPSW\_MDIO\_USER\_GROUP\_USER\_ACCESS\_REG\_K Register (Offset = F80h) [reset = 0h]

MDIO User Access Register

Return to [Summary Table](#)

Offset = Base + (k \* 8h); where k = 0 to 1d

**Table 5-83. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5280 0F80h + formula |

**Figure 5-28. CPSW\_MDIO\_USER\_GROUP\_USER\_ACCESS\_REG\_K Name Register**

| 31     | 30    | 29  | 28       | 27 | 26 | 25     | 24 |
|--------|-------|-----|----------|----|----|--------|----|
| GO     | WRITE | ACK | RESERVED |    |    | REGADR |    |
| R/W    | R/W   | R/W | NONE     |    |    | R/W    |    |
| 0h     | 0h    | 0h  | 0h       |    |    | 0h     |    |
| 23     | 22    | 21  | 20       | 19 | 18 | 17     | 16 |
| REGADR |       |     | PHYADR   |    |    |        |    |
| R/W    |       |     | R/W      |    |    |        |    |
| 0h     |       |     | 0h       |    |    |        |    |
| 15     | 14    | 13  | 12       | 11 | 10 | 9      | 8  |
| DATA   |       |     |          |    |    |        |    |
| R/W    |       |     |          |    |    |        |    |
| 0h     |       |     |          |    |    |        |    |
| 7      | 6     | 5   | 4        | 3  | 2  | 1      | 0  |
| DATA   |       |     |          |    |    |        |    |
| R/W    |       |     |          |    |    |        |    |
| 0h     |       |     |          |    |    |        |    |

**Table 5-85. CPSW\_MDIO\_USER\_GROUP\_USER\_ACCESS\_REG\_K Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | GO       | R/W  | 0h    | Go. Writing a 1 to this bit causes the MDIO state machine to perform an MDIO access when it is convenient for it to do so, this is not an instantaneous process. Writing a 0 to this bit has no effect. This bit is write able only if the MDIO state machine is enabled. This bit will self clear when the requested access has been completed. Any writes to the MDIOUserAccess0 register are blocked when the go bit is 1. If byte access is being used, the go bit should be written last. |
| 30    | WRITE    | R/W  | 0h    | Write enable. Setting this bit to a 1 causes the MDIO transaction to be a register write, otherwise it is a register read.                                                                                                                                                                                                                                                                                                                                                                     |
| 29    | ACK      | R/W  | 0h    | Acknowledge. This bit is set if the PHY acknowledged the read transaction.                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 28:26 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 25:21 | REGADR   | R/W  | 0h    | Register address. This field specifies the PHY register to be accessed for this transaction in clause 22 mode or the MMD value in clause 45 mode.                                                                                                                                                                                                                                                                                                                                              |
| 20:16 | PHYADR   | R/W  | 0h    | PHY address. This field specifies the PHY to be accessed for this transaction.                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 15:0  | DATA     | R/W  | 0h    | User data. The data value read from or to be written to the specified PHY register.                                                                                                                                                                                                                                                                                                                                                                                                            |

### 5.1.2.29 CPSW\_MDIO\_USER\_GROUP\_USER\_PHY\_SEL\_REG\_K Register

#### 1 CPSW\_MDIO\_USER\_GROUP\_USER\_PHY\_SEL\_REG\_K Register (Offset = F84h) [reset = 0h]

MDIO User PHY Select Register

Return to [Summary Table](#)

Offset = Base + (k \* 8h); where k = 0 to 1d

**Table 5-86. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5280 0F84h + formula |

**Figure 5-29. CPSW\_MDIO\_USER\_GROUP\_USER\_PHY\_SEL\_REG\_K Name Register**

|          |                |          |            |    |    |    |    |
|----------|----------------|----------|------------|----|----|----|----|
| 31       | 30             | 29       | 28         | 27 | 26 | 25 | 24 |
| RESERVED |                |          |            |    |    |    |    |
| NONE     |                |          |            |    |    |    |    |
| 0h       |                |          |            |    |    |    |    |
| 23       | 22             | 21       | 20         | 19 | 18 | 17 | 16 |
| RESERVED |                |          |            |    |    |    |    |
| NONE     |                |          |            |    |    |    |    |
| 0h       |                |          |            |    |    |    |    |
| 15       | 14             | 13       | 12         | 11 | 10 | 9  | 8  |
| RESERVED |                |          |            |    |    |    |    |
| NONE     |                |          |            |    |    |    |    |
| 0h       |                |          |            |    |    |    |    |
| 7        | 6              | 5        | 4          | 3  | 2  | 1  | 0  |
| LINKSEL  | LINKINT_ENABLE | RESERVED | PHYADR_MON |    |    |    |    |
| R/W      | R/W            | NONE     | R/W        |    |    |    |    |
| 0h       | 0h             | 0h       | 0h         |    |    |    |    |

**Table 5-88. CPSW\_MDIO\_USER\_GROUP\_USER\_PHY\_SEL\_REG\_K Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                                                                                                             |
|------|----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                |
| 7    | LINKSEL        | R/W  | 0h    | Link status determination select. Set to 1 to determine link status using the MLINK pin. Default value is 0 which implies that the link status is determined by the MDIO state machine. |
| 6    | LINKINT_ENABLE | R/W  | 0h    | Link change interrupt enable. Set to 1 to enable link change status interrupts for PHY address specified in phyadr_mon. Link change interrupts are disabled if this bit is set to 0.    |
| 5    | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                |
| 4:0  | PHYADR_MON     | R/W  | 0h    | PHY address whose link status is to be monitored.                                                                                                                                       |

### 5.1.2.30 CPSW\_REGS\_INT\_SS\_C0\_TH\_THRESH\_PULSE\_EN\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C0\_TH\_THRESH\_PULSE\_EN\_REG Register (Offset = 1800h) [reset = 0h]

Core 0 THost Threshold Pulse Interrupt Enable Register

Return to [Summary Table](#)

**Table 5-89. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 1800h       |

**Figure 5-30. CPSW\_REGS\_INT\_SS\_C0\_TH\_THRESH\_PULSE\_EN\_REG Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH_THRESH_PULSE_EN |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 5-91. CPSW\_REGS\_INT\_SS\_C0\_TH\_THRESH\_PULSE\_EN\_REG Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                                                                       |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                          |
| 7:0  | TH_THRESH_PULSE_EN | R/W  | 0h    | Core 0 THost Threshold Enable - Each bit in this register corresponds to the bit in the THost threshold interrupt that is enabled to generate an interrupt on C0_TH_THRESH_PULSE. |



### 5.1.2.31 CPSW\_REGS\_INT\_SS\_C0\_TH\_PULSE\_EN\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C0\_TH\_PULSE\_EN\_REG Register (Offset = 1804h) [reset = 0h]

Core 0 THost Pulse Interrupt Enable Register

Return to [Summary Table](#)

**Table 5-92. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 1804h       |

**Figure 5-31. CPSW\_REGS\_INT\_SS\_C0\_TH\_PULSE\_EN\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH_PULSE_EN |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-94. CPSW\_REGS\_INT\_SS\_C0\_TH\_PULSE\_EN\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                            |
|------|-------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED    | NONE | 0h    | Reserved                                                                                                                                               |
| 7:0  | TH_PULSE_EN | R/W  | 0h    | Core 0 THost Enable - Each bit in this register corresponds to the bit in the THost interrupt that is enabled to generate an interrupt on C0_TH_PULSE. |

### 5.1.2.32 CPSW\_REGS\_INT\_SS\_C0\_FH\_PULSE\_EN\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C0\_FH\_PULSE\_EN\_REG Register (Offset = 1808h) [reset = 0h]

Core 0 FHost Pulse Interrupt Enable Register

Return to [Summary Table](#)

**Table 5-95. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 1808h       |

**Figure 5-32. CPSW\_REGS\_INT\_SS\_C0\_FH\_PULSE\_EN\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FH_PULSE_EN |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-97. CPSW\_REGS\_INT\_SS\_C0\_FH\_PULSE\_EN\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                      |
|------|-------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED    | NONE | 0h    | Reserved                                                                                                                                                         |
| 7:0  | FH_PULSE_EN | R/W  | 0h    | Core 0 FHost Interrupt Enable - Each bit in this register corresponds to the bit in the FHost interrupt that is enabled to generate an interrupt on C0_FH_PULSE. |

### 5.1.2.33 CPSW\_REGS\_INT\_SS\_C0\_MISC\_EN\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C0\_MISC\_EN\_REG Register (Offset = 180Ch) [reset = 0h]

Core 0 Misc Interrupt Enable Register

Return to [Summary Table](#)

**Table 5-98. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 180Ch       |

**Figure 5-33. CPSW\_REGS\_INT\_SS\_C0\_MISC\_EN\_REG Name Register**

|          |             |             |              |              |              |                 |                 |
|----------|-------------|-------------|--------------|--------------|--------------|-----------------|-----------------|
| 31       | 30          | 29          | 28           | 27           | 26           | 25              | 24              |
| RESERVED |             |             |              |              |              |                 |                 |
| NONE     |             |             |              |              |              |                 |                 |
| 0h       |             |             |              |              |              |                 |                 |
| 23       | 22          | 21          | 20           | 19           | 18           | 17              | 16              |
| RESERVED |             |             |              |              |              |                 |                 |
| NONE     |             |             |              |              |              |                 |                 |
| 0h       |             |             |              |              |              |                 |                 |
| 15       | 14          | 13          | 12           | 11           | 10           | 9               | 8               |
| RESERVED |             |             |              |              |              |                 |                 |
| NONE     |             |             |              |              |              |                 |                 |
| 0h       |             |             |              |              |              |                 |                 |
| 7        | 6           | 5           | 4            | 3            | 2            | 1               | 0               |
| RESERVED | DED_PEND_EN | SEC_PEND_EN | EVNT_PEND_EN | STAT_PEND_EN | HOST_PEND_EN | MDIO_LINKINT_EN | MDIO_USERINT_EN |
| NONE     | R/W         | R/W         | R/W          | R/W          | R/W          | R/W             | R/W             |
| 0h       | 0h          | 0h          | 0h           | 0h           | 0h           | 0h              | 0h              |

**Table 5-100. CPSW\_REGS\_INT\_SS\_C0\_MISC\_EN\_REG Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                            |
|------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                               |
| 6    | DED_PEND_EN     | R/W  | 0h    | Core 0 MISC DED Memory Protect Error Interrupt Enable - enabled to generate an interrupt on C0_Misc_PULSE                                              |
| 5    | SEC_PEND_EN     | R/W  | 0h    | Core 0 MISC SEC Memory Protect Error Interrupt Enable - enabled to generate an interrupt on C0_Misc_PULSE                                              |
| 4    | EVNT_PEND_EN    | R/W  | 0h    | Core 0 MISC CPTS Event Interrupt Enable - enabled to generate an interrupt on C0_Misc_PULSE                                                            |
| 3    | STAT_PEND_EN    | R/W  | 0h    | Core 0 MISC Statistics Interrupt Enable - Logical OR of all port statistics bits (bits n downto 0) - enabled to generate an interrupt on C0_Misc_PULSE |
| 2    | HOST_PEND_EN    | R/W  | 0h    | Core 0 MISC Host Interrupt Enable - enabled to generate an interrupt on C0_Misc_PULSE                                                                  |
| 1    | MDIO_LINKINT_EN | R/W  | 0h    | Core 0 MISC MDIO linkint - Logical OR of bits 1 and 0 - enabled to generate an interrupt on C0_Misc_PULSE                                              |
| 0    | MDIO_USERINT_EN | R/W  | 0h    | Core 0 MISC MDIO userint interrupt enable - Logical OR of bits 1 and 0 - enabled to generate an interrupt on C0_Misc_PULSE                             |

### 5.1.2.34 CPSW\_REGS\_INT\_SS\_C0\_TH\_THRESH\_PULSE\_STATUS\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C0\_TH\_THRESH\_PULSE\_STATUS\_REG Register (Offset = 1810h) [reset = 0h]

THost Threshold Pulse Interrupt Status Register

Return to [Summary Table](#)

**Table 5-101. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 1810h       |

**Figure 5-34. CPSW\_REGS\_INT\_SS\_C0\_TH\_THRESH\_PULSE\_STATUS\_REG Name Register**

|                        |    |    |    |    |    |    |    |
|------------------------|----|----|----|----|----|----|----|
| 31                     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED               |    |    |    |    |    |    |    |
| NONE                   |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |
| 23                     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED               |    |    |    |    |    |    |    |
| NONE                   |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |
| 15                     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED               |    |    |    |    |    |    |    |
| NONE                   |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |
| 7                      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH_THRESH_PULSE_STATUS |    |    |    |    |    |    |    |
| R                      |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |

**Table 5-103. CPSW\_REGS\_INT\_SS\_C0\_TH\_THRESH\_PULSE\_STATUS\_REG Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                                                                                                                                                                     |
|------|------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED               | NONE | 0h    | Reserved                                                                                                                                                                                                        |
| 7:0  | TH_THRESH_PULSE_STATUS | R    | 0h    | Core 0 THost Threshold Masked Interrupt Status - Each bit in this read only register corresponds to the bit in the THost threshold interrupt that is enabled and generating an interrupt on C0_TH_THRESH_PULSE. |

### 5.1.2.35 CPSW\_REGS\_INT\_SS\_C0\_TH\_PULSE\_STATUS\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C0\_TH\_PULSE\_STATUS\_REG Register (Offset = 1814h) [reset = 0h]

THost Pulse Interrupt Status Register

Return to [Summary Table](#)

**Table 5-104. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 1814h       |

**Figure 5-35. CPSW\_REGS\_INT\_SS\_C0\_TH\_PULSE\_STATUS\_REG Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH_PULSE_STATUS |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 5-106. CPSW\_REGS\_INT\_SS\_C0\_TH\_PULSE\_STATUS\_REG Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                               |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                  |
| 7:0  | TH_PULSE_STATUS | R    | 0h    | Core 0 THost Pulse Interrupt Status Register - Each bit in this read only register corresponds to the bit in the Rx interrupt that is enabled and generating an interrupt on C0_TH_PULSE. |

### 5.1.2.36 CPSW\_REGS\_INT\_SS\_C0\_FH\_PULSE\_STATUS\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C0\_FH\_PULSE\_STATUS\_REG Register (Offset = 1818h) [reset = 0h]

FHost Pulse Interrupt Status Register

Return to [Summary Table](#)

**Table 5-107. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 1818h       |

**Figure 5-36. CPSW\_REGS\_INT\_SS\_C0\_FH\_PULSE\_STATUS\_REG Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FH_PULSE_STATUS |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 5-109. CPSW\_REGS\_INT\_SS\_C0\_FH\_PULSE\_STATUS\_REG Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                |
|------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                   |
| 7:0  | FH_PULSE_STATUS | R    | 0h    | Core 0 FHost Pulse Interrupt Status Register - Each bit in this read only register corresponds to the bit in the Tx interrupt that is enabled and generating an interrupt on C0_FH_PULSE . |

### 5.1.2.37 CPSW\_REGS\_INT\_SS\_C0\_MISC\_STATUS\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C0\_MISC\_STATUS\_REG Register (Offset = 181Ch) [reset = 0h]

Misc Interrupt Status Register - Set bits in this register indicate that an enabled interrupt is asserted

Return to [Summary Table](#)

**Table 5-110. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 181Ch       |

**Figure 5-37. CPSW\_REGS\_INT\_SS\_C0\_MISC\_STATUS\_REG Name Register**

|          |          |          |           |           |           |              |              |
|----------|----------|----------|-----------|-----------|-----------|--------------|--------------|
| 31       | 30       | 29       | 28        | 27        | 26        | 25           | 24           |
| RESERVED |          |          |           |           |           |              |              |
| NONE     |          |          |           |           |           |              |              |
| 0h       |          |          |           |           |           |              |              |
| 23       | 22       | 21       | 20        | 19        | 18        | 17           | 16           |
| RESERVED |          |          |           |           |           |              |              |
| NONE     |          |          |           |           |           |              |              |
| 0h       |          |          |           |           |           |              |              |
| 15       | 14       | 13       | 12        | 11        | 10        | 9            | 8            |
| RESERVED |          |          |           |           |           |              |              |
| NONE     |          |          |           |           |           |              |              |
| 0h       |          |          |           |           |           |              |              |
| 7        | 6        | 5        | 4         | 3         | 2         | 1            | 0            |
| RESERVED | DED_PEND | SEC_PEND | EVNT_PEND | STAT_PEND | HOST_PEND | MDIO_LINKINT | MDIO_USERINT |
| NONE     | R/W      | R/W      | R/W       | R/W       | R/W       | R/W          | R/W          |
| 0h       | 0h       | 0h       | 0h        | 0h        | 0h        | 0h           | 0h           |

**Table 5-112. CPSW\_REGS\_INT\_SS\_C0\_MISC\_STATUS\_REG Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                      |
|------|--------------|------|-------|------------------------------------------------------------------|
| 31:7 | RESERVED     | NONE | 0h    | Reserved                                                         |
| 6    | DED_PEND     | R/W  | 0h    | Core 0 MISC DED Memory Protect Error Interrupt                   |
| 5    | SEC_PEND     | R/W  | 0h    | Core 0 MISC SEC Memory Protect Error Interrupt                   |
| 4    | EVNT_PEND    | R/W  | 0h    | Core 0 MISC CPTS Event Interrupt                                 |
| 3    | STAT_PEND    | R/W  | 0h    | Core 0 MISC Statistics Interrupt - Logical OR of bits n downto 0 |
| 2    | HOST_PEND    | R/W  | 0h    | Core 0 MISC Host Interrupt Enable                                |
| 1    | MDIO_LINKINT | R/W  | 0h    | Core 0 MISC MDIO linkint - Logical OR of bits 1 and 0            |
| 0    | MDIO_USERINT | R/W  | 0h    | Core 0 MISC MDIO userint interrupt - Logical OR of bits 1 and 0  |

### 5.1.2.38 CPSW\_REGS\_INT\_SS\_C0\_TH\_IMAX\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C0\_TH\_IMAX\_REG Register (Offset = 1820h) [reset = 0h]

Core 0 THost Interrupt Max Register Register

Return to [Summary Table](#)

**Table 5-113. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 1820h       |

**Figure 5-38. CPSW\_REGS\_INT\_SS\_C0\_TH\_IMAX\_REG Name Register**

|          |    |         |    |    |    |    |    |
|----------|----|---------|----|----|----|----|----|
| 31       | 30 | 29      | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |         |    |    |    |    |    |
| NONE     |    |         |    |    |    |    |    |
| 0h       |    |         |    |    |    |    |    |
| 23       | 22 | 21      | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |         |    |    |    |    |    |
| NONE     |    |         |    |    |    |    |    |
| 0h       |    |         |    |    |    |    |    |
| 15       | 14 | 13      | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |         |    |    |    |    |    |
| NONE     |    |         |    |    |    |    |    |
| 0h       |    |         |    |    |    |    |    |
| 7        | 6  | 5       | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    | TH_IMAX |    |    |    |    |    |
| NONE     |    | R/W     |    |    |    |    |    |
| 0h       |    | 0h      |    |    |    |    |    |

**Table 5-115. CPSW\_REGS\_INT\_SS\_C0\_TH\_IMAX\_REG Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                  |
|------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:6 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                     |
| 5:0  | TH_IMAX  | R/W  | 0h    | Core 0 THost Interrupts per millisecond - The maximum number of interrupts per millisecond generated on C0_TH_PULSE if pacing is enabled for this interrupt. |



### 5.1.2.39 CPSW\_REGS\_INT\_SS\_C0\_FH\_IMAX\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C0\_FH\_IMAX\_REG Register (Offset = 1824h) [reset = 0h]

Core 0 FHost Interrupt Max Register Register

Return to [Summary Table](#)

**Table 5-116. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 1824h       |

**Figure 5-39. CPSW\_REGS\_INT\_SS\_C0\_FH\_IMAX\_REG Name Register**

|          |    |    |    |         |    |    |    |
|----------|----|----|----|---------|----|----|----|
| 31       | 30 | 29 | 28 | 27      | 26 | 25 | 24 |
| RESERVED |    |    |    |         |    |    |    |
| NONE     |    |    |    |         |    |    |    |
| 0h       |    |    |    |         |    |    |    |
| 23       | 22 | 21 | 20 | 19      | 18 | 17 | 16 |
| RESERVED |    |    |    |         |    |    |    |
| NONE     |    |    |    |         |    |    |    |
| 0h       |    |    |    |         |    |    |    |
| 15       | 14 | 13 | 12 | 11      | 10 | 9  | 8  |
| RESERVED |    |    |    |         |    |    |    |
| NONE     |    |    |    |         |    |    |    |
| 0h       |    |    |    |         |    |    |    |
| 7        | 6  | 5  | 4  | 3       | 2  | 1  | 0  |
| RESERVED |    |    |    | FH_IMAX |    |    |    |
| NONE     |    |    |    | R/W     |    |    |    |
| 0h       |    |    |    | 0h      |    |    |    |

**Table 5-118. CPSW\_REGS\_INT\_SS\_C0\_FH\_IMAX\_REG Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                  |
|------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:6 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                     |
| 5:0  | FH_IMAX  | R/W  | 0h    | Core 0 FHost Interrupts per millisecond - The maximum number of interrupts per millisecond generated on C0_FH_PULSE if pacing is enabled for this interrupt. |

### 5.1.2.40 CPSW\_REGS\_INT\_SS\_C1\_TH\_THRESH\_PULSE\_EN\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C1\_TH\_THRESH\_PULSE\_EN\_REG Register (Offset = 1840h) [reset = 0h]

Core 1 THost Threshold Pulse Interrupt Enable Register

Return to [Summary Table](#)

**Table 5-119. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 1840h       |

**Figure 5-40. CPSW\_REGS\_INT\_SS\_C1\_TH\_THRESH\_PULSE\_EN\_REG Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH_THRESH_PULSE_EN |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 5-121. CPSW\_REGS\_INT\_SS\_C1\_TH\_THRESH\_PULSE\_EN\_REG Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                                                                       |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                          |
| 7:0  | TH_THRESH_PULSE_EN | R/W  | 0h    | Core 1 THost Threshold Enable - Each bit in this register corresponds to the bit in the THost threshold interrupt that is enabled to generate an interrupt on C1_TH_THRESH_PULSE. |

### 5.1.2.41 CPSW\_REGS\_INT\_SS\_C1\_TH\_PULSE\_EN\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C1\_TH\_PULSE\_EN\_REG Register (Offset = 1844h) [reset = 0h]

Core 1 THost Pulse Interrupt Enable Register

Return to [Summary Table](#)

**Table 5-122. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 1844h       |

**Figure 5-41. CPSW\_REGS\_INT\_SS\_C1\_TH\_PULSE\_EN\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH_PULSE_EN |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-124. CPSW\_REGS\_INT\_SS\_C1\_TH\_PULSE\_EN\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                            |
|------|-------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED    | NONE | 0h    | Reserved                                                                                                                                               |
| 7:0  | TH_PULSE_EN | R/W  | 0h    | Core 1 THost Enable - Each bit in this register corresponds to the bit in the THost interrupt that is enabled to generate an interrupt on C1_TH_PULSE. |

### 5.1.2.42 CPSW\_REGS\_INT\_SS\_C1\_FH\_PULSE\_EN\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C1\_FH\_PULSE\_EN\_REG Register (Offset = 1848h) [reset = 0h]

Core 1 FHost Pulse Interrupt Enable Register

Return to [Summary Table](#)

**Table 5-125. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 1848h       |

**Figure 5-42. CPSW\_REGS\_INT\_SS\_C1\_FH\_PULSE\_EN\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FH_PULSE_EN |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-127. CPSW\_REGS\_INT\_SS\_C1\_FH\_PULSE\_EN\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                      |
|------|-------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED    | NONE | 0h    | Reserved                                                                                                                                                         |
| 7:0  | FH_PULSE_EN | R/W  | 0h    | Core 1 FHost Interrupt Enable - Each bit in this register corresponds to the bit in the FHost interrupt that is enabled to generate an interrupt on C1_FH_PULSE. |

### 5.1.2.43 CPSW\_REGS\_INT\_SS\_C1\_MISC\_EN\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C1\_MISC\_EN\_REG Register (Offset = 184Ch) [reset = 0h]

Core 1 Misc Interrupt Enable Register

Return to [Summary Table](#)

**Table 5-128. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 184Ch       |

**Figure 5-43. CPSW\_REGS\_INT\_SS\_C1\_MISC\_EN\_REG Name Register**

|          |             |             |              |              |              |                 |                 |
|----------|-------------|-------------|--------------|--------------|--------------|-----------------|-----------------|
| 31       | 30          | 29          | 28           | 27           | 26           | 25              | 24              |
| RESERVED |             |             |              |              |              |                 |                 |
| NONE     |             |             |              |              |              |                 |                 |
| 0h       |             |             |              |              |              |                 |                 |
| 23       | 22          | 21          | 20           | 19           | 18           | 17              | 16              |
| RESERVED |             |             |              |              |              |                 |                 |
| NONE     |             |             |              |              |              |                 |                 |
| 0h       |             |             |              |              |              |                 |                 |
| 15       | 14          | 13          | 12           | 11           | 10           | 9               | 8               |
| RESERVED |             |             |              |              |              |                 |                 |
| NONE     |             |             |              |              |              |                 |                 |
| 0h       |             |             |              |              |              |                 |                 |
| 7        | 6           | 5           | 4            | 3            | 2            | 1               | 0               |
| RESERVED | DED_PEND_EN | SEC_PEND_EN | EVNT_PEND_EN | STAT_PEND_EN | HOST_PEND_EN | MDIO_LINKINT_EN | MDIO_USERINT_EN |
| NONE     | R/W         | R/W         | R/W          | R/W          | R/W          | R/W             | R/W             |
| 0h       | 0h          | 0h          | 0h           | 0h           | 0h           | 0h              | 0h              |

**Table 5-130. CPSW\_REGS\_INT\_SS\_C1\_MISC\_EN\_REG Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                            |
|------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                               |
| 6    | DED_PEND_EN     | R/W  | 0h    | Core 1 MISC DED Memory Protect Error Interrupt Enable - enabled to generate an interrupt on C1_Misc_PULSE                                              |
| 5    | SEC_PEND_EN     | R/W  | 0h    | Core 1 MISC SEC Memory Protect Error Interrupt Enable - enabled to generate an interrupt on C1_Misc_PULSE                                              |
| 4    | EVNT_PEND_EN    | R/W  | 0h    | Core 1 MISC CPTS Event Interrupt Enable - enabled to generate an interrupt on C1_Misc_PULSE                                                            |
| 3    | STAT_PEND_EN    | R/W  | 0h    | Core 1 MISC Statistics Interrupt Enable - Logical OR of all port statistics bits (bits n downto 0) - enabled to generate an interrupt on C1_Misc_PULSE |
| 2    | HOST_PEND_EN    | R/W  | 0h    | Core 1 MISC Host Interrupt Enable - enabled to generate an interrupt on C1_Misc_PULSE                                                                  |
| 1    | MDIO_LINKINT_EN | R/W  | 0h    | Core 1 MISC MDIO linkint - Logical OR of bits 1 and 0 - enabled to generate an interrupt on C1_Misc_PULSE                                              |
| 0    | MDIO_USERINT_EN | R/W  | 0h    | Core 1 MISC MDIO userint interrupt enable - Logical OR of bits 1 and 0 - enabled to generate an interrupt on C1_Misc_PULSE                             |

### 5.1.2.44 CPSW\_REGS\_INT\_SS\_C1\_TH\_THRESH\_PULSE\_STATUS\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C1\_TH\_THRESH\_PULSE\_STATUS\_REG Register (Offset = 1850h) [reset = 0h]

THost Threshold Pulse Interrupt Status Register

Return to [Summary Table](#)

**Table 5-131. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 1850h       |

**Figure 5-44. CPSW\_REGS\_INT\_SS\_C1\_TH\_THRESH\_PULSE\_STATUS\_REG Name Register**

|                        |    |    |    |    |    |    |    |
|------------------------|----|----|----|----|----|----|----|
| 31                     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED               |    |    |    |    |    |    |    |
| NONE                   |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |
| 23                     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED               |    |    |    |    |    |    |    |
| NONE                   |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |
| 15                     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED               |    |    |    |    |    |    |    |
| NONE                   |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |
| 7                      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH_THRESH_PULSE_STATUS |    |    |    |    |    |    |    |
| R                      |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |

**Table 5-133. CPSW\_REGS\_INT\_SS\_C1\_TH\_THRESH\_PULSE\_STATUS\_REG Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                                                                                                                                                                     |
|------|------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED               | NONE | 0h    | Reserved                                                                                                                                                                                                        |
| 7:0  | TH_THRESH_PULSE_STATUS | R    | 0h    | Core 1 THost Threshold Masked Interrupt Status - Each bit in this read only register corresponds to the bit in the THost threshold interrupt that is enabled and generating an interrupt on C1_TH_THRESH_PULSE. |

### 5.1.2.45 CPSW\_REGS\_INT\_SS\_C1\_TH\_PULSE\_STATUS\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C1\_TH\_PULSE\_STATUS\_REG Register (Offset = 1854h) [reset = 0h]

THost Pulse Interrupt Status Register

Return to [Summary Table](#)

**Table 5-134. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 1854h       |

**Figure 5-45. CPSW\_REGS\_INT\_SS\_C1\_TH\_PULSE\_STATUS\_REG Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH_PULSE_STATUS |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 5-136. CPSW\_REGS\_INT\_SS\_C1\_TH\_PULSE\_STATUS\_REG Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                               |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                  |
| 7:0  | TH_PULSE_STATUS | R    | 0h    | Core 1 THost Pulse Interrupt Status Register - Each bit in this read only register corresponds to the bit in the Rx interrupt that is enabled and generating an interrupt on C1_TH_PULSE. |

### 5.1.2.46 CPSW\_REGS\_INT\_SS\_C1\_FH\_PULSE\_STATUS\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C1\_FH\_PULSE\_STATUS\_REG Register (Offset = 1858h) [reset = 0h]

FHost Pulse Interrupt Status Register

Return to [Summary Table](#)

**Table 5-137. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 1858h       |

**Figure 5-46. CPSW\_REGS\_INT\_SS\_C1\_FH\_PULSE\_STATUS\_REG Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FH_PULSE_STATUS |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 5-139. CPSW\_REGS\_INT\_SS\_C1\_FH\_PULSE\_STATUS\_REG Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                |
|------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                   |
| 7:0  | FH_PULSE_STATUS | R    | 0h    | Core 1 FHost Pulse Interrupt Status Register - Each bit in this read only register corresponds to the bit in the Tx interrupt that is enabled and generating an interrupt on C1_FH_PULSE . |



### 5.1.2.47 CPSW\_REGS\_INT\_SS\_C1\_MISC\_STATUS\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C1\_MISC\_STATUS\_REG Register (Offset = 185Ch) [reset = 0h]

Misc Interrupt Status Register - Set bits in this register indicate that an enabled interrupt is asserted

Return to [Summary Table](#)

**Table 5-140. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 185Ch       |

**Figure 5-47. CPSW\_REGS\_INT\_SS\_C1\_MISC\_STATUS\_REG Name Register**

|          |          |          |           |           |           |              |              |
|----------|----------|----------|-----------|-----------|-----------|--------------|--------------|
| 31       | 30       | 29       | 28        | 27        | 26        | 25           | 24           |
| RESERVED |          |          |           |           |           |              |              |
| NONE     |          |          |           |           |           |              |              |
| 0h       |          |          |           |           |           |              |              |
| 23       | 22       | 21       | 20        | 19        | 18        | 17           | 16           |
| RESERVED |          |          |           |           |           |              |              |
| NONE     |          |          |           |           |           |              |              |
| 0h       |          |          |           |           |           |              |              |
| 15       | 14       | 13       | 12        | 11        | 10        | 9            | 8            |
| RESERVED |          |          |           |           |           |              |              |
| NONE     |          |          |           |           |           |              |              |
| 0h       |          |          |           |           |           |              |              |
| 7        | 6        | 5        | 4         | 3         | 2         | 1            | 0            |
| RESERVED | DED_PEND | SEC_PEND | EVNT_PEND | STAT_PEND | HOST_PEND | MDIO_LINKINT | MDIO_USERINT |
| NONE     | R/W      | R/W      | R/W       | R/W       | R/W       | R/W          | R/W          |
| 0h       | 0h       | 0h       | 0h        | 0h        | 0h        | 0h           | 0h           |

**Table 5-142. CPSW\_REGS\_INT\_SS\_C1\_MISC\_STATUS\_REG Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                      |
|------|--------------|------|-------|------------------------------------------------------------------|
| 31:7 | RESERVED     | NONE | 0h    | Reserved                                                         |
| 6    | DED_PEND     | R/W  | 0h    | Core 1 MISC DED Memory Protect Error Interrupt                   |
| 5    | SEC_PEND     | R/W  | 0h    | Core 1 MISC SEC Memory Protect Error Interrupt                   |
| 4    | EVNT_PEND    | R/W  | 0h    | Core 1 MISC CPTS Event Interrupt                                 |
| 3    | STAT_PEND    | R/W  | 0h    | Core 1 MISC Statistics Interrupt - Logical OR of bits n downto 0 |
| 2    | HOST_PEND    | R/W  | 0h    | Core 1 MISC Host Interrupt Enable                                |
| 1    | MDIO_LINKINT | R/W  | 0h    | Core 1 MISC MDIO linkint - Logical OR of bits 1 and 0            |
| 0    | MDIO_USERINT | R/W  | 0h    | Core 1 MISC MDIO userint interrupt - Logical OR of bits 1 and 0  |

### 5.1.2.48 CPSW\_REGS\_INT\_SS\_C1\_TH\_IMAX\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C1\_TH\_IMAX\_REG Register (Offset = 1860h) [reset = 0h]

Core 1 THost Interrupt Max Register Register

Return to [Summary Table](#)

**Table 5-143. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 1860h       |

**Figure 5-48. CPSW\_REGS\_INT\_SS\_C1\_TH\_IMAX\_REG Name Register**

|          |    |         |    |    |    |    |    |
|----------|----|---------|----|----|----|----|----|
| 31       | 30 | 29      | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |         |    |    |    |    |    |
| NONE     |    |         |    |    |    |    |    |
| 0h       |    |         |    |    |    |    |    |
| 23       | 22 | 21      | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |         |    |    |    |    |    |
| NONE     |    |         |    |    |    |    |    |
| 0h       |    |         |    |    |    |    |    |
| 15       | 14 | 13      | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |         |    |    |    |    |    |
| NONE     |    |         |    |    |    |    |    |
| 0h       |    |         |    |    |    |    |    |
| 7        | 6  | 5       | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    | TH_IMAX |    |    |    |    |    |
| NONE     |    | R/W     |    |    |    |    |    |
| 0h       |    | 0h      |    |    |    |    |    |

**Table 5-145. CPSW\_REGS\_INT\_SS\_C1\_TH\_IMAX\_REG Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                  |
|------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:6 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                     |
| 5:0  | TH_IMAX  | R/W  | 0h    | Core 1 THost Interrupts per millisecond - The maximum number of interrupts per millisecond generated on C1_TH_PULSE if pacing is enabled for this interrupt. |

### 5.1.2.49 CPSW\_REGS\_INT\_SS\_C1\_FH\_IMAX\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C1\_FH\_IMAX\_REG Register (Offset = 1864h) [reset = 0h]

Core 1 FHost Interrupt Max Register Register

Return to [Summary Table](#)

**Table 5-146. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 1864h       |

**Figure 5-49. CPSW\_REGS\_INT\_SS\_C1\_FH\_IMAX\_REG Name Register**

|          |    |    |    |         |    |    |    |
|----------|----|----|----|---------|----|----|----|
| 31       | 30 | 29 | 28 | 27      | 26 | 25 | 24 |
| RESERVED |    |    |    |         |    |    |    |
| NONE     |    |    |    |         |    |    |    |
| 0h       |    |    |    |         |    |    |    |
| 23       | 22 | 21 | 20 | 19      | 18 | 17 | 16 |
| RESERVED |    |    |    |         |    |    |    |
| NONE     |    |    |    |         |    |    |    |
| 0h       |    |    |    |         |    |    |    |
| 15       | 14 | 13 | 12 | 11      | 10 | 9  | 8  |
| RESERVED |    |    |    |         |    |    |    |
| NONE     |    |    |    |         |    |    |    |
| 0h       |    |    |    |         |    |    |    |
| 7        | 6  | 5  | 4  | 3       | 2  | 1  | 0  |
| RESERVED |    |    |    | FH_IMAX |    |    |    |
| NONE     |    |    |    | R/W     |    |    |    |
| 0h       |    |    |    | 0h      |    |    |    |

**Table 5-148. CPSW\_REGS\_INT\_SS\_C1\_FH\_IMAX\_REG Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                  |
|------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:6 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                     |
| 5:0  | FH_IMAX  | R/W  | 0h    | Core 1 FHost Interrupts per millisecond - The maximum number of interrupts per millisecond generated on C1_FH_PULSE if pacing is enabled for this interrupt. |

### 5.1.2.50 CPSW\_REGS\_INT\_SS\_C2\_TH\_THRESH\_PULSE\_EN\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C2\_TH\_THRESH\_PULSE\_EN\_REG Register (Offset = 1880h) [reset = 0h]

Core 2 THost Threshold Pulse Interrupt Enable Register

Return to [Summary Table](#)

**Table 5-149. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 1880h       |

**Figure 5-50. CPSW\_REGS\_INT\_SS\_C2\_TH\_THRESH\_PULSE\_EN\_REG Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH_THRESH_PULSE_EN |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 5-151. CPSW\_REGS\_INT\_SS\_C2\_TH\_THRESH\_PULSE\_EN\_REG Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                                                                       |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                          |
| 7:0  | TH_THRESH_PULSE_EN | R/W  | 0h    | Core 2 THost Threshold Enable - Each bit in this register corresponds to the bit in the THost threshold interrupt that is enabled to generate an interrupt on C2_TH_THRESH_PULSE. |

### 5.1.2.51 CPSW\_REGS\_INT\_SS\_C2\_TH\_PULSE\_EN\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C2\_TH\_PULSE\_EN\_REG Register (Offset = 1884h) [reset = 0h]

Core 2 THost Pulse Interrupt Enable Register

Return to [Summary Table](#)

**Table 5-152. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 1884h       |

**Figure 5-51. CPSW\_REGS\_INT\_SS\_C2\_TH\_PULSE\_EN\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH_PULSE_EN |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-154. CPSW\_REGS\_INT\_SS\_C2\_TH\_PULSE\_EN\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                            |
|------|-------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED    | NONE | 0h    | Reserved                                                                                                                                               |
| 7:0  | TH_PULSE_EN | R/W  | 0h    | Core 2 THost Enable - Each bit in this register corresponds to the bit in the THost interrupt that is enabled to generate an interrupt on C2_TH_PULSE. |

### 5.1.2.52 CPSW\_REGS\_INT\_SS\_C2\_FH\_PULSE\_EN\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C2\_FH\_PULSE\_EN\_REG Register (Offset = 1888h) [reset = 0h]

Core 2 FHost Pulse Interrupt Enable Register

Return to [Summary Table](#)

**Table 5-155. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 1888h       |

**Figure 5-52. CPSW\_REGS\_INT\_SS\_C2\_FH\_PULSE\_EN\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FH_PULSE_EN |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-157. CPSW\_REGS\_INT\_SS\_C2\_FH\_PULSE\_EN\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                      |
|------|-------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED    | NONE | 0h    | Reserved                                                                                                                                                         |
| 7:0  | FH_PULSE_EN | R/W  | 0h    | Core 2 FHost Interrupt Enable - Each bit in this register corresponds to the bit in the FHost interrupt that is enabled to generate an interrupt on C2_FH_PULSE. |

### 5.1.2.53 CPSW\_REGS\_INT\_SS\_C2\_MISC\_EN\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C2\_MISC\_EN\_REG Register (Offset = 188Ch) [reset = 0h]

Core 2 Misc Interrupt Enable Register

Return to [Summary Table](#)

**Table 5-158. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 188Ch       |

**Figure 5-53. CPSW\_REGS\_INT\_SS\_C2\_MISC\_EN\_REG Name Register**

|          |             |             |              |              |              |                 |                 |
|----------|-------------|-------------|--------------|--------------|--------------|-----------------|-----------------|
| 31       | 30          | 29          | 28           | 27           | 26           | 25              | 24              |
| RESERVED |             |             |              |              |              |                 |                 |
| NONE     |             |             |              |              |              |                 |                 |
| 0h       |             |             |              |              |              |                 |                 |
| 23       | 22          | 21          | 20           | 19           | 18           | 17              | 16              |
| RESERVED |             |             |              |              |              |                 |                 |
| NONE     |             |             |              |              |              |                 |                 |
| 0h       |             |             |              |              |              |                 |                 |
| 15       | 14          | 13          | 12           | 11           | 10           | 9               | 8               |
| RESERVED |             |             |              |              |              |                 |                 |
| NONE     |             |             |              |              |              |                 |                 |
| 0h       |             |             |              |              |              |                 |                 |
| 7        | 6           | 5           | 4            | 3            | 2            | 1               | 0               |
| RESERVED | DED_PEND_EN | SEC_PEND_EN | EVNT_PEND_EN | STAT_PEND_EN | HOST_PEND_EN | MDIO_LINKINT_EN | MDIO_USERINT_EN |
| NONE     | R/W         | R/W         | R/W          | R/W          | R/W          | R/W             | R/W             |
| 0h       | 0h          | 0h          | 0h           | 0h           | 0h           | 0h              | 0h              |

**Table 5-160. CPSW\_REGS\_INT\_SS\_C2\_MISC\_EN\_REG Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                            |
|------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                               |
| 6    | DED_PEND_EN     | R/W  | 0h    | Core 2 MISC DED Memory Protect Error Interrupt Enable - enabled to generate an interrupt on C2_Misc_PULSE                                              |
| 5    | SEC_PEND_EN     | R/W  | 0h    | Core 2 MISC SEC Memory Protect Error Interrupt Enable - enabled to generate an interrupt on C2_Misc_PULSE                                              |
| 4    | EVNT_PEND_EN    | R/W  | 0h    | Core 2 MISC CPTS Event Interrupt Enable - enabled to generate an interrupt on C2_Misc_PULSE                                                            |
| 3    | STAT_PEND_EN    | R/W  | 0h    | Core 2 MISC Statistics Interrupt Enable - Logical OR of all port statistics bits (bits n downto 0) - enabled to generate an interrupt on C2_Misc_PULSE |
| 2    | HOST_PEND_EN    | R/W  | 0h    | Core 2 MISC Host Interrupt Enable - enabled to generate an interrupt on C2_Misc_PULSE                                                                  |
| 1    | MDIO_LINKINT_EN | R/W  | 0h    | Core 2 MISC MDIO linkint - Logical OR of bits 1 and 0 - enabled to generate an interrupt on C2_Misc_PULSE                                              |
| 0    | MDIO_USERINT_EN | R/W  | 0h    | Core 2 MISC MDIO userint interrupt enable - Logical OR of bits 1 and 0 - enabled to generate an interrupt on C2_Misc_PULSE                             |

### 5.1.2.54 CPSW\_REGS\_INT\_SS\_C2\_TH\_THRESH\_PULSE\_STATUS\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C2\_TH\_THRESH\_PULSE\_STATUS\_REG Register (Offset = 1890h) [reset = 0h]

THost Threshold Pulse Interrupt Status Register

Return to [Summary Table](#)

**Table 5-161. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 1890h       |

**Figure 5-54. CPSW\_REGS\_INT\_SS\_C2\_TH\_THRESH\_PULSE\_STATUS\_REG Name Register**

|                        |    |    |    |    |    |    |    |
|------------------------|----|----|----|----|----|----|----|
| 31                     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED               |    |    |    |    |    |    |    |
| NONE                   |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |
| 23                     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED               |    |    |    |    |    |    |    |
| NONE                   |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |
| 15                     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED               |    |    |    |    |    |    |    |
| NONE                   |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |
| 7                      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH_THRESH_PULSE_STATUS |    |    |    |    |    |    |    |
| R                      |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |

**Table 5-163. CPSW\_REGS\_INT\_SS\_C2\_TH\_THRESH\_PULSE\_STATUS\_REG Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                                                                                                                                                                     |
|------|------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED               | NONE | 0h    | Reserved                                                                                                                                                                                                        |
| 7:0  | TH_THRESH_PULSE_STATUS | R    | 0h    | Core 2 THost Threshold Masked Interrupt Status - Each bit in this read only register corresponds to the bit in the THost threshold interrupt that is enabled and generating an interrupt on C2_TH_THRESH_PULSE. |



### 5.1.2.55 CPSW\_REGS\_INT\_SS\_C2\_TH\_PULSE\_STATUS\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C2\_TH\_PULSE\_STATUS\_REG Register (Offset = 1894h) [reset = 0h]

THost Pulse Interrupt Status Register

Return to [Summary Table](#)

**Table 5-164. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 1894h       |

**Figure 5-55. CPSW\_REGS\_INT\_SS\_C2\_TH\_PULSE\_STATUS\_REG Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH_PULSE_STATUS |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 5-166. CPSW\_REGS\_INT\_SS\_C2\_TH\_PULSE\_STATUS\_REG Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                               |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                  |
| 7:0  | TH_PULSE_STATUS | R    | 0h    | Core 2 THost Pulse Interrupt Status Register - Each bit in this read only register corresponds to the bit in the Rx interrupt that is enabled and generating an interrupt on C2_TH_PULSE. |

### 5.1.2.56 CPSW\_REGS\_INT\_SS\_C2\_FH\_PULSE\_STATUS\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C2\_FH\_PULSE\_STATUS\_REG Register (Offset = 1898h) [reset = 0h]

FHost Pulse Interrupt Status Register

Return to [Summary Table](#)

**Table 5-167. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 1898h       |

**Figure 5-56. CPSW\_REGS\_INT\_SS\_C2\_FH\_PULSE\_STATUS\_REG Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FH_PULSE_STATUS |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 5-169. CPSW\_REGS\_INT\_SS\_C2\_FH\_PULSE\_STATUS\_REG Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                |
|------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                   |
| 7:0  | FH_PULSE_STATUS | R    | 0h    | Core 2 FHost Pulse Interrupt Status Register - Each bit in this read only register corresponds to the bit in the Tx interrupt that is enabled and generating an interrupt on C2_FH_PULSE . |

### 5.1.2.57 CPSW\_REGS\_INT\_SS\_C2\_MISC\_STATUS\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C2\_MISC\_STATUS\_REG Register (Offset = 189Ch) [reset = 0h]

Misc Interrupt Status Register - Set bits in this register indicate that an enabled interrupt is asserted

Return to [Summary Table](#)

**Table 5-170. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 189Ch       |

**Figure 5-57. CPSW\_REGS\_INT\_SS\_C2\_MISC\_STATUS\_REG Name Register**

|          |          |          |           |           |           |              |              |
|----------|----------|----------|-----------|-----------|-----------|--------------|--------------|
| 31       | 30       | 29       | 28        | 27        | 26        | 25           | 24           |
| RESERVED |          |          |           |           |           |              |              |
| NONE     |          |          |           |           |           |              |              |
| 0h       |          |          |           |           |           |              |              |
| 23       | 22       | 21       | 20        | 19        | 18        | 17           | 16           |
| RESERVED |          |          |           |           |           |              |              |
| NONE     |          |          |           |           |           |              |              |
| 0h       |          |          |           |           |           |              |              |
| 15       | 14       | 13       | 12        | 11        | 10        | 9            | 8            |
| RESERVED |          |          |           |           |           |              |              |
| NONE     |          |          |           |           |           |              |              |
| 0h       |          |          |           |           |           |              |              |
| 7        | 6        | 5        | 4         | 3         | 2         | 1            | 0            |
| RESERVED | DED_PEND | SEC_PEND | EVNT_PEND | STAT_PEND | HOST_PEND | MDIO_LINKINT | MDIO_USERINT |
| NONE     | R/W      | R/W      | R/W       | R/W       | R/W       | R/W          | R/W          |
| 0h       | 0h       | 0h       | 0h        | 0h        | 0h        | 0h           | 0h           |

**Table 5-172. CPSW\_REGS\_INT\_SS\_C2\_MISC\_STATUS\_REG Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                      |
|------|--------------|------|-------|------------------------------------------------------------------|
| 31:7 | RESERVED     | NONE | 0h    | Reserved                                                         |
| 6    | DED_PEND     | R/W  | 0h    | Core 2 MISC DED Memory Protect Error Interrupt                   |
| 5    | SEC_PEND     | R/W  | 0h    | Core 2 MISC SEC Memory Protect Error Interrupt                   |
| 4    | EVNT_PEND    | R/W  | 0h    | Core 2 MISC CPTS Event Interrupt                                 |
| 3    | STAT_PEND    | R/W  | 0h    | Core 2 MISC Statistics Interrupt - Logical OR of bits n downto 0 |
| 2    | HOST_PEND    | R/W  | 0h    | Core 2 MISC Host Interrupt Enable                                |
| 1    | MDIO_LINKINT | R/W  | 0h    | Core 2 MISC MDIO linkint - Logical OR of bits 1 and 0            |
| 0    | MDIO_USERINT | R/W  | 0h    | Core 2 MISC MDIO userint interrupt - Logical OR of bits 1 and 0  |

### 5.1.2.58 CPSW\_REGS\_INT\_SS\_C2\_TH\_IMAX\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C2\_TH\_IMAX\_REG Register (Offset = 18A0h) [reset = 0h]

Core 2 THost Interrupt Max Register Register

Return to [Summary Table](#)

**Table 5-173. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 18A0h       |

**Figure 5-58. CPSW\_REGS\_INT\_SS\_C2\_TH\_IMAX\_REG Name Register**

|          |    |         |    |    |    |    |    |
|----------|----|---------|----|----|----|----|----|
| 31       | 30 | 29      | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |         |    |    |    |    |    |
| NONE     |    |         |    |    |    |    |    |
| 0h       |    |         |    |    |    |    |    |
| 23       | 22 | 21      | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |         |    |    |    |    |    |
| NONE     |    |         |    |    |    |    |    |
| 0h       |    |         |    |    |    |    |    |
| 15       | 14 | 13      | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |         |    |    |    |    |    |
| NONE     |    |         |    |    |    |    |    |
| 0h       |    |         |    |    |    |    |    |
| 7        | 6  | 5       | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    | TH_IMAX |    |    |    |    |    |
| NONE     |    | R/W     |    |    |    |    |    |
| 0h       |    | 0h      |    |    |    |    |    |

**Table 5-175. CPSW\_REGS\_INT\_SS\_C2\_TH\_IMAX\_REG Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                  |
|------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:6 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                     |
| 5:0  | TH_IMAX  | R/W  | 0h    | Core 2 THost Interrupts per millisecond - The maximum number of interrupts per millisecond generated on C2_TH_PULSE if pacing is enabled for this interrupt. |

### 5.1.2.59 CPSW\_REGS\_INT\_SS\_C2\_FH\_IMAX\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C2\_FH\_IMAX\_REG Register (Offset = 18A4h) [reset = 0h]

Core 2 FHost Interrupt Max Register Register

Return to [Summary Table](#)

**Table 5-176. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 18A4h       |

**Figure 5-59. CPSW\_REGS\_INT\_SS\_C2\_FH\_IMAX\_REG Name Register**

|          |    |    |    |         |    |    |    |
|----------|----|----|----|---------|----|----|----|
| 31       | 30 | 29 | 28 | 27      | 26 | 25 | 24 |
| RESERVED |    |    |    |         |    |    |    |
| NONE     |    |    |    |         |    |    |    |
| 0h       |    |    |    |         |    |    |    |
| 23       | 22 | 21 | 20 | 19      | 18 | 17 | 16 |
| RESERVED |    |    |    |         |    |    |    |
| NONE     |    |    |    |         |    |    |    |
| 0h       |    |    |    |         |    |    |    |
| 15       | 14 | 13 | 12 | 11      | 10 | 9  | 8  |
| RESERVED |    |    |    |         |    |    |    |
| NONE     |    |    |    |         |    |    |    |
| 0h       |    |    |    |         |    |    |    |
| 7        | 6  | 5  | 4  | 3       | 2  | 1  | 0  |
| RESERVED |    |    |    | FH_IMAX |    |    |    |
| NONE     |    |    |    | R/W     |    |    |    |
| 0h       |    |    |    | 0h      |    |    |    |

**Table 5-178. CPSW\_REGS\_INT\_SS\_C2\_FH\_IMAX\_REG Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                  |
|------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:6 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                     |
| 5:0  | FH_IMAX  | R/W  | 0h    | Core 2 FHost Interrupts per millisecond - The maximum number of interrupts per millisecond generated on C2_FH_PULSE if pacing is enabled for this interrupt. |

### 5.1.2.60 CPSW\_REGS\_INT\_SS\_C3\_TH\_THRESH\_PULSE\_EN\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C3\_TH\_THRESH\_PULSE\_EN\_REG Register (Offset = 18C0h) [reset = 0h]

Core 3 THost Threshold Pulse Interrupt Enable Register

Return to [Summary Table](#)

**Table 5-179. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 18C0h       |

**Figure 5-60. CPSW\_REGS\_INT\_SS\_C3\_TH\_THRESH\_PULSE\_EN\_REG Name Register**

|                    |    |    |    |    |    |    |    |
|--------------------|----|----|----|----|----|----|----|
| 31                 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 23                 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 15                 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED           |    |    |    |    |    |    |    |
| NONE               |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |
| 7                  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH_THRESH_PULSE_EN |    |    |    |    |    |    |    |
| R/W                |    |    |    |    |    |    |    |
| 0h                 |    |    |    |    |    |    |    |

**Table 5-181. CPSW\_REGS\_INT\_SS\_C3\_TH\_THRESH\_PULSE\_EN\_REG Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                                                                                                                                                       |
|------|--------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                          |
| 7:0  | TH_THRESH_PULSE_EN | R/W  | 0h    | Core 3 THost Threshold Enable - Each bit in this register corresponds to the bit in the THost threshold interrupt that is enabled to generate an interrupt on C3_TH_THRESH_PULSE. |

### 5.1.2.61 CPSW\_REGS\_INT\_SS\_C3\_TH\_PULSE\_EN\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C3\_TH\_PULSE\_EN\_REG Register (Offset = 18C4h) [reset = 0h]

Core 3 THost Pulse Interrupt Enable Register

Return to [Summary Table](#)

**Table 5-182. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 18C4h       |

**Figure 5-61. CPSW\_REGS\_INT\_SS\_C3\_TH\_PULSE\_EN\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH_PULSE_EN |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-184. CPSW\_REGS\_INT\_SS\_C3\_TH\_PULSE\_EN\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                            |
|------|-------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED    | NONE | 0h    | Reserved                                                                                                                                               |
| 7:0  | TH_PULSE_EN | R/W  | 0h    | Core 3 THost Enable - Each bit in this register corresponds to the bit in the THost interrupt that is enabled to generate an interrupt on C3_TH_PULSE. |

### 5.1.2.62 CPSW\_REGS\_INT\_SS\_C3\_FH\_PULSE\_EN\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C3\_FH\_PULSE\_EN\_REG Register (Offset = 18C8h) [reset = 0h]

Core 3 FHost Pulse Interrupt Enable Register

Return to [Summary Table](#)

**Table 5-185. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 18C8h       |

**Figure 5-62. CPSW\_REGS\_INT\_SS\_C3\_FH\_PULSE\_EN\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FH_PULSE_EN |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-187. CPSW\_REGS\_INT\_SS\_C3\_FH\_PULSE\_EN\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                      |
|------|-------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED    | NONE | 0h    | Reserved                                                                                                                                                         |
| 7:0  | FH_PULSE_EN | R/W  | 0h    | Core 3 FHost Interrupt Enable - Each bit in this register corresponds to the bit in the FHost interrupt that is enabled to generate an interrupt on C3_FH_PULSE. |



### 5.1.2.63 CPSW\_REGS\_INT\_SS\_C3\_MISC\_EN\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C3\_MISC\_EN\_REG Register (Offset = 18CCh) [reset = 0h]

Core 3 Misc Interrupt Enable Register

Return to [Summary Table](#)

**Table 5-188. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 18CCh       |

**Figure 5-63. CPSW\_REGS\_INT\_SS\_C3\_MISC\_EN\_REG Name Register**

|          |             |             |              |              |              |                 |                 |
|----------|-------------|-------------|--------------|--------------|--------------|-----------------|-----------------|
| 31       | 30          | 29          | 28           | 27           | 26           | 25              | 24              |
| RESERVED |             |             |              |              |              |                 |                 |
| NONE     |             |             |              |              |              |                 |                 |
| 0h       |             |             |              |              |              |                 |                 |
| 23       | 22          | 21          | 20           | 19           | 18           | 17              | 16              |
| RESERVED |             |             |              |              |              |                 |                 |
| NONE     |             |             |              |              |              |                 |                 |
| 0h       |             |             |              |              |              |                 |                 |
| 15       | 14          | 13          | 12           | 11           | 10           | 9               | 8               |
| RESERVED |             |             |              |              |              |                 |                 |
| NONE     |             |             |              |              |              |                 |                 |
| 0h       |             |             |              |              |              |                 |                 |
| 7        | 6           | 5           | 4            | 3            | 2            | 1               | 0               |
| RESERVED | DED_PEND_EN | SEC_PEND_EN | EVNT_PEND_EN | STAT_PEND_EN | HOST_PEND_EN | MDIO_LINKINT_EN | MDIO_USERINT_EN |
| NONE     | R/W         | R/W         | R/W          | R/W          | R/W          | R/W             | R/W             |
| 0h       | 0h          | 0h          | 0h           | 0h           | 0h           | 0h              | 0h              |

**Table 5-190. CPSW\_REGS\_INT\_SS\_C3\_MISC\_EN\_REG Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                            |
|------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                               |
| 6    | DED_PEND_EN     | R/W  | 0h    | Core 3 MISC DED Memory Protect Error Interrupt Enable - enabled to generate an interrupt on C3_Misc_PULSE                                              |
| 5    | SEC_PEND_EN     | R/W  | 0h    | Core 3 MISC SEC Memory Protect Error Interrupt Enable - enabled to generate an interrupt on C3_Misc_PULSE                                              |
| 4    | EVNT_PEND_EN    | R/W  | 0h    | Core 3 MISC CPTS Event Interrupt Enable - enabled to generate an interrupt on C3_Misc_PULSE                                                            |
| 3    | STAT_PEND_EN    | R/W  | 0h    | Core 3 MISC Statistics Interrupt Enable - Logical OR of all port statistics bits (bits n downto 0) - enabled to generate an interrupt on C3_Misc_PULSE |
| 2    | HOST_PEND_EN    | R/W  | 0h    | Core 3 MISC Host Interrupt Enable - enabled to generate an interrupt on C3_Misc_PULSE                                                                  |
| 1    | MDIO_LINKINT_EN | R/W  | 0h    | Core 3 MISC MDIO linkint - Logical OR of bits 1 and 0 - enabled to generate an interrupt on C3_Misc_PULSE                                              |
| 0    | MDIO_USERINT_EN | R/W  | 0h    | Core 3 MISC MDIO userint interrupt enable - Logical OR of bits 1 and 0 - enabled to generate an interrupt on C3_Misc_PULSE                             |

### 5.1.2.64 CPSW\_REGS\_INT\_SS\_C3\_TH\_THRESH\_PULSE\_STATUS\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C3\_TH\_THRESH\_PULSE\_STATUS\_REG Register (Offset = 18D0h) [reset = 0h]

THost Threshold Pulse Interrupt Status Register

Return to [Summary Table](#)

**Table 5-191. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 18D0h       |

**Figure 5-64. CPSW\_REGS\_INT\_SS\_C3\_TH\_THRESH\_PULSE\_STATUS\_REG Name Register**

|                        |    |    |    |    |    |    |    |
|------------------------|----|----|----|----|----|----|----|
| 31                     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED               |    |    |    |    |    |    |    |
| NONE                   |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |
| 23                     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED               |    |    |    |    |    |    |    |
| NONE                   |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |
| 15                     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED               |    |    |    |    |    |    |    |
| NONE                   |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |
| 7                      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH_THRESH_PULSE_STATUS |    |    |    |    |    |    |    |
| R                      |    |    |    |    |    |    |    |
| 0h                     |    |    |    |    |    |    |    |

**Table 5-193. CPSW\_REGS\_INT\_SS\_C3\_TH\_THRESH\_PULSE\_STATUS\_REG Register Field Descriptions**

| Bit  | Field                  | Type | Reset | Description                                                                                                                                                                                                     |
|------|------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED               | NONE | 0h    | Reserved                                                                                                                                                                                                        |
| 7:0  | TH_THRESH_PULSE_STATUS | R    | 0h    | Core 3 THost Threshold Masked Interrupt Status - Each bit in this read only register corresponds to the bit in the THost threshold interrupt that is enabled and generating an interrupt on C3_TH_THRESH_PULSE. |

### 5.1.2.65 CPSW\_REGS\_INT\_SS\_C3\_TH\_PULSE\_STATUS\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C3\_TH\_PULSE\_STATUS\_REG Register (Offset = 18D4h) [reset = 0h]

THost Pulse Interrupt Status Register

Return to [Summary Table](#)

**Table 5-194. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 18D4h       |

**Figure 5-65. CPSW\_REGS\_INT\_SS\_C3\_TH\_PULSE\_STATUS\_REG Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH_PULSE_STATUS |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 5-196. CPSW\_REGS\_INT\_SS\_C3\_TH\_PULSE\_STATUS\_REG Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                               |
|------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                  |
| 7:0  | TH_PULSE_STATUS | R    | 0h    | Core 3 THost Pulse Interrupt Status Register - Each bit in this read only register corresponds to the bit in the Rx interrupt that is enabled and generating an interrupt on C3_TH_PULSE. |

### 5.1.2.66 CPSW\_REGS\_INT\_SS\_C3\_FH\_PULSE\_STATUS\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C3\_FH\_PULSE\_STATUS\_REG Register (Offset = 18D8h) [reset = 0h]

FHost Pulse Interrupt Status Register

Return to [Summary Table](#)

**Table 5-197. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 18D8h       |

**Figure 5-66. CPSW\_REGS\_INT\_SS\_C3\_FH\_PULSE\_STATUS\_REG Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FH_PULSE_STATUS |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 5-199. CPSW\_REGS\_INT\_SS\_C3\_FH\_PULSE\_STATUS\_REG Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                |
|------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                   |
| 7:0  | FH_PULSE_STATUS | R    | 0h    | Core 3 FHost Pulse Interrupt Status Register - Each bit in this read only register corresponds to the bit in the Tx interrupt that is enabled and generating an interrupt on C3_FH_PULSE . |

### 5.1.2.67 CPSW\_REGS\_INT\_SS\_C3\_MISC\_STATUS\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C3\_MISC\_STATUS\_REG Register (Offset = 18DCh) [reset = 0h]

Misc Interrupt Status Register - Set bits in this register indicate that an enabled interrupt is asserted

Return to [Summary Table](#)

**Table 5-200. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 18DCh       |

**Figure 5-67. CPSW\_REGS\_INT\_SS\_C3\_MISC\_STATUS\_REG Name Register**

|          |          |          |           |           |           |              |                  |
|----------|----------|----------|-----------|-----------|-----------|--------------|------------------|
| 31       | 30       | 29       | 28        | 27        | 26        | 25           | 24               |
| RESERVED |          |          |           |           |           |              |                  |
| NONE     |          |          |           |           |           |              |                  |
| 0h       |          |          |           |           |           |              |                  |
| 23       | 22       | 21       | 20        | 19        | 18        | 17           | 16               |
| RESERVED |          |          |           |           |           |              |                  |
| NONE     |          |          |           |           |           |              |                  |
| 0h       |          |          |           |           |           |              |                  |
| 15       | 14       | 13       | 12        | 11        | 10        | 9            | 8                |
| RESERVED |          |          |           |           |           |              |                  |
| NONE     |          |          |           |           |           |              |                  |
| 0h       |          |          |           |           |           |              |                  |
| 7        | 6        | 5        | 4         | 3         | 2         | 1            | 0                |
| RESERVED | DED_PEND | SEC_PEND | EVNT_PEND | STAT_PEND | HOST_PEND | MDIO_LINKINT | MDIO_USERIN<br>T |
| NONE     | R/W      | R/W      | R/W       | R/W       | R/W       | R/W          | R/W              |
| 0h       | 0h       | 0h       | 0h        | 0h        | 0h        | 0h           | 0h               |

**Table 5-202. CPSW\_REGS\_INT\_SS\_C3\_MISC\_STATUS\_REG Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                      |
|------|--------------|------|-------|------------------------------------------------------------------|
| 31:7 | RESERVED     | NONE | 0h    | Reserved                                                         |
| 6    | DED_PEND     | R/W  | 0h    | Core 3 MISC DED Memory Protect Error Interrupt                   |
| 5    | SEC_PEND     | R/W  | 0h    | Core 3 MISC SEC Memory Protect Error Interrupt                   |
| 4    | EVNT_PEND    | R/W  | 0h    | Core 3 MISC CPTS Event Interrupt                                 |
| 3    | STAT_PEND    | R/W  | 0h    | Core 3 MISC Statistics Interrupt - Logical OR of bits n downto 0 |
| 2    | HOST_PEND    | R/W  | 0h    | Core 3 MISC Host Interrupt Enable                                |
| 1    | MDIO_LINKINT | R/W  | 0h    | Core 3 MISC MDIO linkint - Logical OR of bits 1 and 0            |
| 0    | MDIO_USERINT | R/W  | 0h    | Core 3 MISC MDIO userint interrupt - Logical OR of bits 1 and 0  |

### 5.1.2.68 CPSW\_REGS\_INT\_SS\_C3\_TH\_IMAX\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C3\_TH\_IMAX\_REG Register (Offset = 18E0h) [reset = 0h]

Core 3 THost Interrupt Max Register Register

Return to [Summary Table](#)

**Table 5-203. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 18E0h       |

**Figure 5-68. CPSW\_REGS\_INT\_SS\_C3\_TH\_IMAX\_REG Name Register**

|          |    |         |    |    |    |    |    |
|----------|----|---------|----|----|----|----|----|
| 31       | 30 | 29      | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |         |    |    |    |    |    |
| NONE     |    |         |    |    |    |    |    |
| 0h       |    |         |    |    |    |    |    |
| 23       | 22 | 21      | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |         |    |    |    |    |    |
| NONE     |    |         |    |    |    |    |    |
| 0h       |    |         |    |    |    |    |    |
| 15       | 14 | 13      | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |         |    |    |    |    |    |
| NONE     |    |         |    |    |    |    |    |
| 0h       |    |         |    |    |    |    |    |
| 7        | 6  | 5       | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    | TH_IMAX |    |    |    |    |    |
| NONE     |    | R/W     |    |    |    |    |    |
| 0h       |    | 0h      |    |    |    |    |    |

**Table 5-205. CPSW\_REGS\_INT\_SS\_C3\_TH\_IMAX\_REG Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                  |
|------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:6 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                     |
| 5:0  | TH_IMAX  | R/W  | 0h    | Core 3 THost Interrupts per millisecond - The maximum number of interrupts per millisecond generated on C3_TH_PULSE if pacing is enabled for this interrupt. |

### 5.1.2.69 CPSW\_REGS\_INT\_SS\_C3\_FH\_IMAX\_REG Register

#### 1 CPSW\_REGS\_INT\_SS\_C3\_FH\_IMAX\_REG Register (Offset = 18E4h) [reset = 0h]

Core 3 FHost Interrupt Max Register Register

Return to [Summary Table](#)

**Table 5-206. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5280 18E4h       |

**Figure 5-69. CPSW\_REGS\_INT\_SS\_C3\_FH\_IMAX\_REG Name Register**

|          |    |    |    |         |    |    |    |
|----------|----|----|----|---------|----|----|----|
| 31       | 30 | 29 | 28 | 27      | 26 | 25 | 24 |
| RESERVED |    |    |    |         |    |    |    |
| NONE     |    |    |    |         |    |    |    |
| 0h       |    |    |    |         |    |    |    |
| 23       | 22 | 21 | 20 | 19      | 18 | 17 | 16 |
| RESERVED |    |    |    |         |    |    |    |
| NONE     |    |    |    |         |    |    |    |
| 0h       |    |    |    |         |    |    |    |
| 15       | 14 | 13 | 12 | 11      | 10 | 9  | 8  |
| RESERVED |    |    |    |         |    |    |    |
| NONE     |    |    |    |         |    |    |    |
| 0h       |    |    |    |         |    |    |    |
| 7        | 6  | 5  | 4  | 3       | 2  | 1  | 0  |
| RESERVED |    |    |    | FH_IMAX |    |    |    |
| NONE     |    |    |    | R/W     |    |    |    |
| 0h       |    |    |    | 0h      |    |    |    |

**Table 5-208. CPSW\_REGS\_INT\_SS\_C3\_FH\_IMAX\_REG Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                  |
|------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:6 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                     |
| 5:0  | FH_IMAX  | R/W  | 0h    | Core 3 FHost Interrupts per millisecond - The maximum number of interrupts per millisecond generated on C3_FH_PULSE if pacing is enabled for this interrupt. |

### 5.1.2.70 CPSW\_NC\_VER\_REG Register

#### 1 CPSW\_NC\_VER\_REG Register (Offset = 20000h) [reset = 6B903103h]

CPSW ID Version

Return to [Summary Table](#)

**Table 5-209. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 0000h       |

**Figure 5-70. CPSW\_NC\_VER\_REG Name Register**

|           |    |    |    |           |    |    |    |
|-----------|----|----|----|-----------|----|----|----|
| 31        | 30 | 29 | 28 | 27        | 26 | 25 | 24 |
| IDENT     |    |    |    |           |    |    |    |
| R         |    |    |    |           |    |    |    |
| 6B90h     |    |    |    |           |    |    |    |
| 23        | 22 | 21 | 20 | 19        | 18 | 17 | 16 |
| IDENT     |    |    |    |           |    |    |    |
| R         |    |    |    |           |    |    |    |
| 6B90h     |    |    |    |           |    |    |    |
| 15        | 14 | 13 | 12 | 11        | 10 | 9  | 8  |
| RTL_VER   |    |    |    | MAJOR_VER |    |    |    |
| R         |    |    |    | R         |    |    |    |
| 6h        |    |    |    | 1h        |    |    |    |
| 7         | 6  | 5  | 4  | 3         | 2  | 1  | 0  |
| MINOR_VER |    |    |    |           |    |    |    |
| R         |    |    |    |           |    |    |    |
| 3h        |    |    |    |           |    |    |    |

**Table 5-211. CPSW\_NC\_VER\_REG Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description          |
|-------|-----------|------|-------|----------------------|
| 31:16 | IDENT     | R    | 6B90h | Identification Value |
| 15:11 | RTL_VER   | R    | 6h    | RTL Version Value    |
| 10:8  | MAJOR_VER | R    | 1h    | Major Version Value  |
| 7:0   | MINOR_VER | R    | 3h    | Minor Version Value  |



### 5.1.2.71 CPSW\_NC\_CONTROL\_REG Register

#### 1 CPSW\_NC\_CONTROL\_REG Register (Offset = 20004h) [reset = 0h]

CPSW Switch Control

Return to [Summary Table](#)

**Table 5-212. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 0004h       |

**Figure 5-71. CPSW\_NC\_CONTROL\_REG Name Register**

|                    |                    |                    |                    |                    |                    |                    |                    |
|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| 31                 | 30                 | 29                 | 28                 | 27                 | 26                 | 25                 | 24                 |
| ECC_CRC_MODE       | RESERVED           |                    |                    |                    |                    |                    |                    |
| R/W                | NONE               |                    |                    |                    |                    |                    |                    |
| 0h                 | 0h                 |                    |                    |                    |                    |                    |                    |
| 23                 | 22                 | 21                 | 20                 | 19                 | 18                 | 17                 | 16                 |
| RESERVED           |                    |                    |                    |                    | EST_ENABLE         | RESERVED           | EEE_ENABLE         |
| NONE               |                    |                    |                    |                    | R/W                | R/W                | R/W                |
| 0h                 |                    |                    |                    |                    | 0h                 | 0h                 | 0h                 |
| 15                 | 14                 | 13                 | 12                 | 11                 | 10                 | 9                  | 8                  |
| P0_FH_PASS_CRC_ERR | P0_FH_PAD          | P0_TH_CRC_REMOVE   | RESERVED           | P8_PASS_PRI_TAGGED | P7_PASS_PRI_TAGGED | P6_PASS_PRI_TAGGED | P5_PASS_PRI_TAGGED |
| R/W                | R/W                | R/W                | NONE               | R/W                | R/W                | R/W                | R/W                |
| 0h                 | 0h                 | 0h                 | 0h                 | 0h                 | 0h                 | 0h                 | 0h                 |
| 7                  | 6                  | 5                  | 4                  | 3                  | 2                  | 1                  | 0                  |
| P4_PASS_PRI_TAGGED | P3_PASS_PRI_TAGGED | P2_PASS_PRI_TAGGED | P1_PASS_PRI_TAGGED | P0_PASS_PRI_TAGGED | P0_ENABLE          | VLAN_AWARE         | S_CN_SWITCH        |
| R/W                | R/W                | R/W                | R/W                | R/W                | R/W                | R/W                | R/W                |
| 0h                 | 0h                 | 0h                 | 0h                 | 0h                 | 0h                 | 0h                 | 0h                 |

**Table 5-214. CPSW\_NC\_CONTROL\_REG Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                              |
|-------|--------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | ECC_CRC_MODE       | R/W  | 0h    | ECC CRC Mode -<br>0 - ECC errors induced through the ECC aggregator flip bits in the packet headers (not in packet data).<br>1 - ECC errors induced through the ECC aggregator flip bits in the packet data (not in the packet headers). |
| 30:19 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                 |
| 18    | EST_ENABLE         | R/W  | 0h    | Enhanced Scheduled Traffic enable (EST) -<br>0 - EST is disabled.<br>1 - EST is enabled                                                                                                                                                  |
| 17    | RESERVED           | R/W  | 0h    | RESERVED                                                                                                                                                                                                                                 |
| 16    | EEE_ENABLE         | R/W  | 0h    | Energy Efficient Ethernet enable -<br>0 - Energy Efficient Ethernet is disabled.<br>1 - Energy Efficient Ethernet is enabled.                                                                                                            |
| 15    | P0_FH_PASS_CRC_ERR | R/W  | 0h    | Port 0 Pass Received CRC errors -<br>0 - Packets received with CRC errors on port 0 are dropped.<br>1 - Packets received with CRC errors on port 0 are transferred to the destination ports.                                             |

**Table 5-214. CPSW\_NC\_CONTROL\_REG Register Field Descriptions (continued)**

| Bit | Field              | Type | Reset | Description                                                                                                                                                                                                                               |
|-----|--------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14  | P0_FH_PAD          | R/W  | 0h    | Port 0 Receive Short Packet Pad -<br>0 - short packets are dropped.<br>1 - short packets are padded to 64-bytes (with pad and added CRC) if the CRC is not passed in. Short packets are dropped if the CRC is passed (in the Info0 word). |
| 13  | P0_TH_CRC_REMOVE   | R/W  | 0h    | Port 0 Transmit CRC remove -<br>0 - Do not remove the CRC on Port 0 THost (egress) packets.<br>1 - Remove the CRC on all Port 0 THost (egress) packets.                                                                                   |
| 12  | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                  |
| 11  | P8_PASS_PRI_TAGGED | R/W  | 0h    | Port 8 Pass Priority Tagged -<br>0 - Priority tagged packets have the zero VID replaced with the input port Enet_P8_PORT_VLAN[11:0] on ingress.<br>1 - Priority tagged packets are processed unchanged.                                   |
| 10  | P7_PASS_PRI_TAGGED | R/W  | 0h    | Port 7 Pass Priority Tagged -<br>0 - Priority tagged packets have the zero VID replaced with the input port Enet_P7_PORT_VLAN[11:0] on ingress.<br>1 - Priority tagged packets are processed unchanged.                                   |
| 9   | P6_PASS_PRI_TAGGED | R/W  | 0h    | Port 6 Pass Priority Tagged -<br>0 - Priority tagged packets have the zero VID replaced with the input port Enet_P6_PORT_VLAN[11:0] on ingress.<br>1 - Priority tagged packets are processed unchanged.                                   |
| 8   | P5_PASS_PRI_TAGGED | R/W  | 0h    | Port 5 Pass Priority Tagged -<br>0 - Priority tagged packets have the zero VID replaced with the input port Enet_P5_PORT_VLAN[11:0] on ingress.<br>1 - Priority tagged packets are processed unchanged.                                   |
| 7   | P4_PASS_PRI_TAGGED | R/W  | 0h    | Port 4 Pass Priority Tagged -<br>0 - Priority tagged packets have the zero VID replaced with the input port Enet_P4_PORT_VLAN[11:0] on ingress.<br>1 - Priority tagged packets are processed unchanged.                                   |
| 6   | P3_PASS_PRI_TAGGED | R/W  | 0h    | Port 3 Pass Priority Tagged -<br>0 - Priority tagged packets have the zero VID replaced with the input port Enet_P3_PORT_VLAN[11:0] on ingress.<br>1 - Priority tagged packets are processed unchanged.                                   |
| 5   | P2_PASS_PRI_TAGGED | R/W  | 0h    | Port 2 Pass Priority Tagged -<br>0 - Priority tagged packets have the zero VID replaced with the input port Enet_P2_PORT_VLAN[11:0] on ingress.<br>1 - Priority tagged packets are processed unchanged.                                   |
| 4   | P1_PASS_PRI_TAGGED | R/W  | 0h    | Port 1 Pass Priority Tagged -<br>0 - Priority tagged packets have the zero VID replaced with the input port Enet_P1_PORT_VLAN[11:0] on ingress.<br>1 - Priority tagged packets are processed unchanged.                                   |
| 3   | P0_PASS_PRI_TAGGED | R/W  | 0h    | Port 0 Pass Priority Tagged -<br>0 - Priority tagged packets have the zero VID replaced with the input port Enet_P0_PORT_VLAN[11:0] on ingress.<br>1 - Priority tagged packets are processed unchanged.                                   |
| 2   | P0_ENABLE          | R/W  | 0h    | Port 0 Enable -<br>0 - Port 0 is disabled<br>1 - Port 0 is enabled                                                                                                                                                                        |
| 1   | VLAN_AWARE         | R/W  | 0h    | VLAN Aware Mode -<br>0 - CPSW_NU is in the VLAN unaware mode.<br>1 - CPSW_NU is in the VLAN aware mode.                                                                                                                                   |
| 0   | S_CN_SWITCH        | R/W  | 0h    | Service or Customer VLAN switch.<br>0 - Customer switch. VLAN processing uses the inner_vlan_ltype.<br>1 - Service switch. VLAN processing uses the outer_vlan_ltype.                                                                     |

### 5.1.2.72 CPSW\_NC\_STATUS\_REG Register

#### 1 CPSW\_NC\_STATUS\_REG Register (Offset = 2000Ch) [reset = 1h]

CPSW Status

Return to [Summary Table](#)

**Table 5-215. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 000Ch       |

**Figure 5-72. CPSW\_NC\_STATUS\_REG Name Register**

|          |    |    |    |    |    |    |           |
|----------|----|----|----|----|----|----|-----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24        |
| RESERVED |    |    |    |    |    |    |           |
| NONE     |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16        |
| RESERVED |    |    |    |    |    |    |           |
| NONE     |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8         |
| RESERVED |    |    |    |    |    |    |           |
| NONE     |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0         |
| RESERVED |    |    |    |    |    |    | CPPI_IDLE |
| NONE     |    |    |    |    |    |    | R         |
| 0h       |    |    |    |    |    |    | 1h        |

**Table 5-217. CPSW\_NC\_STATUS\_REG Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                      |
|------|-----------|------|-------|----------------------------------------------------------------------------------|
| 31:1 | RESERVED  | NONE | 0h    | Reserved                                                                         |
| 0    | CPPI_IDLE | R    | 1h    | CPPI Idle - Indicates when set that the CPPI port transmit and receive are idle. |

### 5.1.2.73 CPSW\_NC\_EM\_CONTROL\_REG Register

#### 1 CPSW\_NC\_EM\_CONTROL\_REG Register (Offset = 20010h) [reset = 0h]

CPSW Emulation Control

Return to [Summary Table](#)

**Table 5-218. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 0010h       |

**Figure 5-73. CPSW\_NC\_EM\_CONTROL\_REG Name Register**

|          |    |    |    |    |    |      |      |
|----------|----|----|----|----|----|------|------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25   | 24   |
| RESERVED |    |    |    |    |    |      |      |
| NONE     |    |    |    |    |    |      |      |
| 0h       |    |    |    |    |    |      |      |
| 23       | 22 | 21 | 20 | 19 | 18 | 17   | 16   |
| RESERVED |    |    |    |    |    |      |      |
| NONE     |    |    |    |    |    |      |      |
| 0h       |    |    |    |    |    |      |      |
| 15       | 14 | 13 | 12 | 11 | 10 | 9    | 8    |
| RESERVED |    |    |    |    |    |      |      |
| NONE     |    |    |    |    |    |      |      |
| 0h       |    |    |    |    |    |      |      |
| 7        | 6  | 5  | 4  | 3  | 2  | 1    | 0    |
| RESERVED |    |    |    |    |    | SOFT | FREE |
| NONE     |    |    |    |    |    | R/W  | R/W  |
| 0h       |    |    |    |    |    | 0h   | 0h   |

**Table 5-220. CPSW\_NC\_EM\_CONTROL\_REG Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description        |
|------|----------|------|-------|--------------------|
| 31:2 | RESERVED | NONE | 0h    | Reserved           |
| 1    | SOFT     | R/W  | 0h    | Emulation Soft Bit |
| 0    | FREE     | R/W  | 0h    | Emulation Free Bit |

### 5.1.2.74 CPSW\_NC\_STAT\_PORT\_EN\_REG Register

#### 1 CPSW\_NC\_STAT\_PORT\_EN\_REG Register (Offset = 20014h) [reset = 0h]

CPSW Statistics Port Enable

Return to [Summary Table](#)

**Table 5-221. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 0014h       |

**Figure 5-74. CPSW\_NC\_STAT\_PORT\_EN\_REG Name Register**

|            |            |            |            |            |            |            |            |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 31         | 30         | 29         | 28         | 27         | 26         | 25         | 24         |
| RESERVED   |            |            |            |            |            |            |            |
| NONE       |            |            |            |            |            |            |            |
| 0h         |            |            |            |            |            |            |            |
| 23         | 22         | 21         | 20         | 19         | 18         | 17         | 16         |
| RESERVED   |            |            |            |            |            |            |            |
| NONE       |            |            |            |            |            |            |            |
| 0h         |            |            |            |            |            |            |            |
| 15         | 14         | 13         | 12         | 11         | 10         | 9          | 8          |
| RESERVED   |            |            |            |            |            |            | P8_STAT_EN |
| NONE       |            |            |            |            |            |            | R/W        |
| 0h         |            |            |            |            |            |            | 0h         |
| 7          | 6          | 5          | 4          | 3          | 2          | 1          | 0          |
| P7_STAT_EN | P6_STAT_EN | P5_STAT_EN | P4_STAT_EN | P3_STAT_EN | P2_STAT_EN | P1_STAT_EN | P0_STAT_EN |
| R/W        | R/W        | R/W        | R/W        | R/W        | R/W        | R/W        | R/W        |
| 0h         | 0h         | 0h         | 0h         | 0h         | 0h         | 0h         | 0h         |

**Table 5-223. CPSW\_NC\_STAT\_PORT\_EN\_REG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                       |
|------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------|
| 31:9 | RESERVED   | NONE | 0h    | Reserved                                                                                                          |
| 8    | P8_STAT_EN | R/W  | 0h    | Port 8 Statistics Enable<br>0 - Statistics are disabled for the port.<br>1 - Statistics are enabled for the port. |
| 7    | P7_STAT_EN | R/W  | 0h    | Port 7 Statistics Enable<br>0 - Statistics are disabled for the port.<br>1 - Statistics are enabled for the port. |
| 6    | P6_STAT_EN | R/W  | 0h    | Port 6 Statistics Enable<br>0 - Statistics are disabled for the port.<br>1 - Statistics are enabled for the port. |
| 5    | P5_STAT_EN | R/W  | 0h    | Port 5 Statistics Enable<br>0 - Statistics are disabled for the port.<br>1 - Statistics are enabled for the port. |
| 4    | P4_STAT_EN | R/W  | 0h    | Port 4 Statistics Enable<br>0 - Statistics are disabled for the port.<br>1 - Statistics are enabled for the port. |
| 3    | P3_STAT_EN | R/W  | 0h    | Port 3 Statistics Enable<br>0 - Statistics are disabled for the port.<br>1 - Statistics are enabled for the port. |
| 2    | P2_STAT_EN | R/W  | 0h    | Port 2 Statistics Enable<br>0 - Statistics are disabled for the port.<br>1 - Statistics are enabled for the port. |

**Table 5-223. CPSW\_NC\_STAT\_PORT\_EN\_REG Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                       |
|-----|------------|------|-------|-------------------------------------------------------------------------------------------------------------------|
| 1   | P1_STAT_EN | R/W  | 0h    | Port 1 Statistics Enable<br>0 - Statistics are disabled for the port.<br>1 - Statistics are enabled for the port. |
| 0   | P0_STAT_EN | R/W  | 0h    | Port 0 Statistics Enable<br>0 - Statistics are disabled for the port.<br>1 - Statistics are enabled for the port. |

### 5.1.2.75 CPSW\_NC\_PTYPE\_REG Register

#### 1 CPSW\_NC\_PTYPE\_REG Register (Offset = 20018h) [reset = 0h]

CPSW Transmit Priority Type

Return to [Summary Table](#)

**Table 5-224. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 0018h       |

**Figure 5-75. CPSW\_NC\_PTYPE\_REG Name Register**

|              |              |              |                |              |              |              |              |
|--------------|--------------|--------------|----------------|--------------|--------------|--------------|--------------|
| 31           | 30           | 29           | 28             | 27           | 26           | 25           | 24           |
| RESERVED     |              |              |                |              |              |              |              |
| NONE         |              |              |                |              |              |              |              |
| 0h           |              |              |                |              |              |              |              |
| 23           | 22           | 21           | 20             | 19           | 18           | 17           | 16           |
| RESERVED     |              |              |                |              |              |              | P8_PTYPE_ESC |
| NONE         |              |              |                |              |              |              | R/W          |
| 0h           |              |              |                |              |              |              | 0h           |
| 15           | 14           | 13           | 12             | 11           | 10           | 9            | 8            |
| P7_PTYPE_ESC | P6_PTYPE_ESC | P5_PTYPE_ESC | P4_PTYPE_ESC   | P3_PTYPE_ESC | P2_PTYPE_ESC | P1_PTYPE_ESC | P0_PTYPE_ESC |
| R/W          | R/W          | R/W          | R/W            | R/W          | R/W          | R/W          | R/W          |
| 0h           | 0h           | 0h           | 0h             | 0h           | 0h           | 0h           | 0h           |
| 7            | 6            | 5            | 4              | 3            | 2            | 1            | 0            |
| RESERVED     |              |              | ESC_PRI_LD_VAL |              |              |              |              |
| NONE         |              |              | R/W            |              |              |              |              |
| 0h           |              |              | 0h             |              |              |              |              |

**Table 5-226. CPSW\_NC\_PTYPE\_REG Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                               |
|-------|--------------|------|-------|-------------------------------------------------------------------------------------------|
| 31:17 | RESERVED     | NONE | 0h    | Reserved                                                                                  |
| 16    | P8_PTYPE_ESC | R/W  | 0h    | Port 8 Priority Type Escalate -<br>0 - Priority Type Fixed.<br>1 - Priority Type Escalate |
| 15    | P7_PTYPE_ESC | R/W  | 0h    | Port 7 Priority Type Escalate -<br>0 - Priority Type Fixed.<br>1 - Priority Type Escalate |
| 14    | P6_PTYPE_ESC | R/W  | 0h    | Port 6 Priority Type Escalate -<br>0 - Priority Type Fixed.<br>1 - Priority Type Escalate |
| 13    | P5_PTYPE_ESC | R/W  | 0h    | Port 5 Priority Type Escalate -<br>0 - Priority Type Fixed.<br>1 - Priority Type Escalate |
| 12    | P4_PTYPE_ESC | R/W  | 0h    | Port 4 Priority Type Escalate -<br>0 - Priority Type Fixed.<br>1 - Priority Type Escalate |
| 11    | P3_PTYPE_ESC | R/W  | 0h    | Port 3 Priority Type Escalate -<br>0 - Priority Type Fixed.<br>1 - Priority Type Escalate |

**Table 5-226. CPSW\_NC\_PTYPE\_REG Register Field Descriptions (continued)**

| Bit | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                 |
|-----|----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | P2_PTYPE_ESC   | R/W  | 0h    | Port 2 Priority Type Escalate -<br>0 - Priority Type Fixed.<br>1 - Priority Type Escalate                                                                                                                                                                                                                                                   |
| 9   | P1_PTYPE_ESC   | R/W  | 0h    | Port 1 Priority Type Escalate -<br>0 - Priority Type Fixed.<br>1 - Priority Type Escalate                                                                                                                                                                                                                                                   |
| 8   | P0_PTYPE_ESC   | R/W  | 0h    | Port 0 Priority Type Escalate -<br>0 - Priority Type Fixed.<br>1 - Priority Type Escalate                                                                                                                                                                                                                                                   |
| 7:5 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                    |
| 4:0 | ESC_PRI_LD_VAL | R/W  | 0h    | Escalate Priority Load Value -<br>When a port is in escalate priority, this is the number of higher priority packets sent before the next lower priority is allowed to send a packet. Escalate priority allows lower priority packets to be sent at a fixed rate relative to the next higher priority. The min value of esc_pri_ld_val = 2. |



### 5.1.2.76 CPSW\_NC\_SOFT\_IDLE\_REG Register

#### 1 CPSW\_NC\_SOFT\_IDLE\_REG Register (Offset = 2001Ch) [reset = 0h]

CPSW Software Idle

Return to [Summary Table](#)

**Table 5-227. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 001Ch       |

**Figure 5-76. CPSW\_NC\_SOFT\_IDLE\_REG Name Register**

|          |    |    |    |    |    |    |           |
|----------|----|----|----|----|----|----|-----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24        |
| RESERVED |    |    |    |    |    |    |           |
| NONE     |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16        |
| RESERVED |    |    |    |    |    |    |           |
| NONE     |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8         |
| RESERVED |    |    |    |    |    |    |           |
| NONE     |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0         |
| RESERVED |    |    |    |    |    |    | SOFT_IDLE |
| NONE     |    |    |    |    |    |    | R/W       |
| 0h       |    |    |    |    |    |    | 0h        |

**Table 5-229. CPSW\_NC\_SOFT\_IDLE\_REG Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                     |
|------|-----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED  | NONE | 0h    | Reserved                                                                                                                                                        |
| 0    | SOFT_IDLE | R/W  | 0h    | Software Idle -<br>0 - Software idle not commanded.<br>1 - Command CPSW software idle. When set, port 0 packet DMA operations stop at the next packet boundary. |

### 5.1.2.77 CPSW\_NC\_THRU\_RATE\_REG Register

#### 1 CPSW\_NC\_THRU\_RATE\_REG Register (Offset = 20020h) [reset = 3001h]

CPSW Thru Rate

Return to [Summary Table](#)

**Table 5-230. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 0020h       |

**Figure 5-77. CPSW\_NC\_THRU\_RATE\_REG Name Register**

|                 |    |    |    |                 |    |    |    |
|-----------------|----|----|----|-----------------|----|----|----|
| 31              | 30 | 29 | 28 | 27              | 26 | 25 | 24 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 23              | 22 | 21 | 20 | 19              | 18 | 17 | 16 |
| RESERVED        |    |    |    |                 |    |    |    |
| NONE            |    |    |    |                 |    |    |    |
| 0h              |    |    |    |                 |    |    |    |
| 15              | 14 | 13 | 12 | 11              | 10 | 9  | 8  |
| SL_RX_THRU_RATE |    |    |    | RESERVED        |    |    |    |
| R/W             |    |    |    | NONE            |    |    |    |
| 3h              |    |    |    | 0h              |    |    |    |
| 7               | 6  | 5  | 4  | 3               | 2  | 1  | 0  |
| RESERVED        |    |    |    | P0_FH_THRU_RATE |    |    |    |
| NONE            |    |    |    | R/W             |    |    |    |
| 0h              |    |    |    | 1h              |    |    |    |

**Table 5-232. CPSW\_NC\_THRU\_RATE\_REG Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                            |
|-------|-----------------|------|-------|--------------------------------------------------------|
| 31:16 | RESERVED        | NONE | 0h    | Reserved                                               |
| 15:12 | SL_RX_THRU_RATE | R/W  | 3h    | This is not a field intended to be changed by software |
| 11:4  | RESERVED        | NONE | 0h    | Reserved                                               |
| 3:0   | P0_FH_THRU_RATE | R/W  | 1h    | This is not a field intended to be changed by software |

### 5.1.2.78 CPSW\_NC\_GAP\_THRESH\_REG Register

#### 1 CPSW\_NC\_GAP\_THRESH\_REG Register (Offset = 20024h) [reset = Bh]

CPSW Transmit FIFO Short Gap Threshold

Return to [Summary Table](#)

**Table 5-233. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 0024h       |

**Figure 5-78. CPSW\_NC\_GAP\_THRESH\_REG Name Register**

|          |    |    |    |            |    |    |    |
|----------|----|----|----|------------|----|----|----|
| 31       | 30 | 29 | 28 | 27         | 26 | 25 | 24 |
| RESERVED |    |    |    |            |    |    |    |
| NONE     |    |    |    |            |    |    |    |
| 0h       |    |    |    |            |    |    |    |
| 23       | 22 | 21 | 20 | 19         | 18 | 17 | 16 |
| RESERVED |    |    |    |            |    |    |    |
| NONE     |    |    |    |            |    |    |    |
| 0h       |    |    |    |            |    |    |    |
| 15       | 14 | 13 | 12 | 11         | 10 | 9  | 8  |
| RESERVED |    |    |    |            |    |    |    |
| NONE     |    |    |    |            |    |    |    |
| 0h       |    |    |    |            |    |    |    |
| 7        | 6  | 5  | 4  | 3          | 2  | 1  | 0  |
| RESERVED |    |    |    | GAP_THRESH |    |    |    |
| NONE     |    |    |    | R/W        |    |    |    |
| 0h       |    |    |    | Bh         |    |    |    |

**Table 5-235. CPSW\_NC\_GAP\_THRESH\_REG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                |
|------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:5 | RESERVED   | NONE | 0h    | Reserved                                                                                                                                                                   |
| 4:0  | GAP_THRESH | R/W  | Bh    | Ethernet Port Short Gap Threshold -<br>This is the Ethernet port associated FIFO transmit block usage value for triggering transmit short gap (when short gap is enabled). |

### 5.1.2.79 CPSW\_NC\_EEE\_PRESCALE\_REG Register

#### 1 CPSW\_NC\_EEE\_PRESCALE\_REG Register (Offset = 2002Ch) [reset = 0h]

CPSW Energy Efficient Ethernet Prescale Value

Return to [Summary Table](#)

**Table 5-236. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 002Ch       |

**Figure 5-79. CPSW\_NC\_EEE\_PRESCALE\_REG Name Register**

|              |    |    |    |              |    |    |    |
|--------------|----|----|----|--------------|----|----|----|
| 31           | 30 | 29 | 28 | 27           | 26 | 25 | 24 |
| RESERVED     |    |    |    |              |    |    |    |
| NONE         |    |    |    |              |    |    |    |
| 0h           |    |    |    |              |    |    |    |
| 23           | 22 | 21 | 20 | 19           | 18 | 17 | 16 |
| RESERVED     |    |    |    |              |    |    |    |
| NONE         |    |    |    |              |    |    |    |
| 0h           |    |    |    |              |    |    |    |
| 15           | 14 | 13 | 12 | 11           | 10 | 9  | 8  |
| RESERVED     |    |    |    | EEE_PRESCALE |    |    |    |
| NONE         |    |    |    | R/W          |    |    |    |
| 0h           |    |    |    | 0h           |    |    |    |
| 7            | 6  | 5  | 4  | 3            | 2  | 1  | 0  |
| EEE_PRESCALE |    |    |    |              |    |    |    |
| R/W          |    |    |    |              |    |    |    |
| 0h           |    |    |    |              |    |    |    |

**Table 5-238. CPSW\_NC\_EEE\_PRESCALE\_REG Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|--------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED     | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 11:0  | EEE_PRESCALE | R/W  | 0h    | Energy Efficient Ethernet Prescale count load value - This value is loaded into the EEE pre-scale counter each time the pre-scale count decrements to zero. The EEE counters are enabled to decrement each time the pre-scale counter reaches zero (and the EEE counters are enabled to count time). If this value is zero then the EEE counters decrement on every clock. If this value is 0x001 then the counters decrement on every other clock (and so on). |

### 5.1.2.80 CPSW\_NC\_TX\_G\_OFLOW\_THRESH\_SET\_REG Register

#### 1 CPSW\_NC\_TX\_G\_OFLOW\_THRESH\_SET\_REG Register (Offset = 20030h) [reset = FFFFFFFFh]

CPSW PFC Tx Global Out Flow Threshold Set

Return to [Summary Table](#)

**Table 5-239. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 0030h       |

**Figure 5-80. CPSW\_NC\_TX\_G\_OFLOW\_THRESH\_SET\_REG Name Register**

| 31 | 30 | 29   | 28 | 27 | 26 | 25   | 24 |
|----|----|------|----|----|----|------|----|
|    |    | PRI7 |    |    |    | PRI6 |    |
|    |    | R/W  |    |    |    | R/W  |    |
|    |    | Fh   |    |    |    | Fh   |    |
| 23 | 22 | 21   | 20 | 19 | 18 | 17   | 16 |
|    |    | PRI5 |    |    |    | PRI4 |    |
|    |    | R/W  |    |    |    | R/W  |    |
|    |    | Fh   |    |    |    | Fh   |    |
| 15 | 14 | 13   | 12 | 11 | 10 | 9    | 8  |
|    |    | PRI3 |    |    |    | PRI2 |    |
|    |    | R/W  |    |    |    | R/W  |    |
|    |    | Fh   |    |    |    | Fh   |    |
| 7  | 6  | 5    | 4  | 3  | 2  | 1    | 0  |
|    |    | PRI1 |    |    |    | PRI0 |    |
|    |    | R/W  |    |    |    | R/W  |    |
|    |    | Fh   |    |    |    | Fh   |    |

**Table 5-241. CPSW\_NC\_TX\_G\_OFLOW\_THRESH\_SET\_REG Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                          |
|-------|-------|------|-------|----------------------------------------------------------------------|
| 31:28 | PRI7  | R/W  | Fh    | Priority Based Flow Control Global Outflow Usage Threshold for Pri 7 |
| 27:24 | PRI6  | R/W  | Fh    | Priority Based Flow Control Global Outflow Usage Threshold for Pri 6 |
| 23:20 | PRI5  | R/W  | Fh    | Priority Based Flow Control Global Outflow Usage Threshold for Pri 5 |
| 19:16 | PRI4  | R/W  | Fh    | Priority Based Flow Control Global Outflow Usage Threshold for Pri 4 |
| 15:12 | PRI3  | R/W  | Fh    | Priority Based Flow Control Global Outflow Usage Threshold for Pri 3 |
| 11:8  | PRI2  | R/W  | Fh    | Priority Based Flow Control Global Outflow Usage Threshold for Pri 2 |
| 7:4   | PRI1  | R/W  | Fh    | Priority Based Flow Control Global Outflow Usage Threshold for Pri 1 |
| 3:0   | PRI0  | R/W  | Fh    | Priority Based Flow Control Global Outflow Usage Threshold for Pri 0 |

### 5.1.2.81 CPSW\_NC\_TX\_G\_OFLOW\_THRESH\_CLR\_REG Register

#### 1 CPSW\_NC\_TX\_G\_OFLOW\_THRESH\_CLR\_REG Register (Offset = 20034h) [reset = 0h]

CPSW PFC Tx Global Out Flow Threshold Clear

Return to [Summary Table](#)

**Table 5-242. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 0034h       |

**Figure 5-81. CPSW\_NC\_TX\_G\_OFLOW\_THRESH\_CLR\_REG Name Register**

| 31 | 30 | 29   | 28 | 27 | 26 | 25   | 24 |
|----|----|------|----|----|----|------|----|
|    |    | PRI7 |    |    |    | PRI6 |    |
|    |    | R/W  |    |    |    | R/W  |    |
|    |    | 0h   |    |    |    | 0h   |    |
| 23 | 22 | 21   | 20 | 19 | 18 | 17   | 16 |
|    |    | PRI5 |    |    |    | PRI4 |    |
|    |    | R/W  |    |    |    | R/W  |    |
|    |    | 0h   |    |    |    | 0h   |    |
| 15 | 14 | 13   | 12 | 11 | 10 | 9    | 8  |
|    |    | PRI3 |    |    |    | PRI2 |    |
|    |    | R/W  |    |    |    | R/W  |    |
|    |    | 0h   |    |    |    | 0h   |    |
| 7  | 6  | 5    | 4  | 3  | 2  | 1    | 0  |
|    |    | PRI1 |    |    |    | PRI0 |    |
|    |    | R/W  |    |    |    | R/W  |    |
|    |    | 0h   |    |    |    | 0h   |    |

**Table 5-244. CPSW\_NC\_TX\_G\_OFLOW\_THRESH\_CLR\_REG Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                          |
|-------|-------|------|-------|----------------------------------------------------------------------|
| 31:28 | PRI7  | R/W  | 0h    | Priority Based Flow Control Global Outflow Usage Threshold for Pri 7 |
| 27:24 | PRI6  | R/W  | 0h    | Priority Based Flow Control Global Outflow Usage Threshold for Pri 6 |
| 23:20 | PRI5  | R/W  | 0h    | Priority Based Flow Control Global Outflow Usage Threshold for Pri 5 |
| 19:16 | PRI4  | R/W  | 0h    | Priority Based Flow Control Global Outflow Usage Threshold for Pri 4 |
| 15:12 | PRI3  | R/W  | 0h    | Priority Based Flow Control Global Outflow Usage Threshold for Pri 3 |
| 11:8  | PRI2  | R/W  | 0h    | Priority Based Flow Control Global Outflow Usage Threshold for Pri 2 |
| 7:4   | PRI1  | R/W  | 0h    | Priority Based Flow Control Global Outflow Usage Threshold for Pri 1 |
| 3:0   | PRI0  | R/W  | 0h    | Priority Based Flow Control Global Outflow Usage Threshold for Pri 0 |

### 5.1.2.82 CPSW\_NC\_TX\_G\_BUF\_THRESH\_SET\_L\_REG Register

#### 1 CPSW\_NC\_TX\_G\_BUF\_THRESH\_SET\_L\_REG Register (Offset = 20038h) [reset = FFFFFFFFh]

CPSW PFC Global Tx Buffer Threshold Set Low

Return to [Summary Table](#)

**Table 5-245. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 0038h       |

**Figure 5-82. CPSW\_NC\_TX\_G\_BUF\_THRESH\_SET\_L\_REG Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PRI3 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| FFh  |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PRI2 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| FFh  |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PRI1 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| FFh  |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PRI0 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| FFh  |    |    |    |    |    |    |    |

**Table 5-247. CPSW\_NC\_TX\_G\_BUF\_THRESH\_SET\_L\_REG Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                              |
|-------|-------|------|-------|--------------------------------------------------------------------------|
| 31:24 | PRI3  | R/W  | FFh   | Priority Based Flow Control Global Buffer Usage Threshold for Priority 3 |
| 23:16 | PRI2  | R/W  | FFh   | Priority Based Flow Control Global Buffer Usage Threshold for Priority 2 |
| 15:8  | PRI1  | R/W  | FFh   | Priority Based Flow Control Global Buffer Usage Threshold for Priority 1 |
| 7:0   | PRI0  | R/W  | FFh   | Priority Based Flow Control Global Buffer Usage Threshold for Priority 0 |

### 5.1.2.83 CPSW\_NC\_TX\_G\_BUF\_THRESH\_SET\_H\_REG Register

#### 1 CPSW\_NC\_TX\_G\_BUF\_THRESH\_SET\_H\_REG Register (Offset = 2003Ch) [reset = FFFFFFFFh]

CPSW PFC Global Tx Buffer Threshold Set High

Return to [Summary Table](#)

**Table 5-248. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 003Ch       |

**Figure 5-83. CPSW\_NC\_TX\_G\_BUF\_THRESH\_SET\_H\_REG Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PRI7 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| FFh  |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PRI6 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| FFh  |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PRI5 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| FFh  |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PRI4 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| FFh  |    |    |    |    |    |    |    |

**Table 5-250. CPSW\_NC\_TX\_G\_BUF\_THRESH\_SET\_H\_REG Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                              |
|-------|-------|------|-------|--------------------------------------------------------------------------|
| 31:24 | PRI7  | R/W  | FFh   | Priority Based Flow Control Global Buffer Usage Threshold for Priority 7 |
| 23:16 | PRI6  | R/W  | FFh   | Priority Based Flow Control Global Buffer Usage Threshold for Priority 6 |
| 15:8  | PRI5  | R/W  | FFh   | Priority Based Flow Control Global Buffer Usage Threshold for Priority 5 |
| 7:0   | PRI4  | R/W  | FFh   | Priority Based Flow Control Global Buffer Usage Threshold for Priority 4 |



### 5.1.2.84 CPSW\_NC\_TX\_G\_BUF\_THRESH\_CLR\_L\_REG Register

#### 1 CPSW\_NC\_TX\_G\_BUF\_THRESH\_CLR\_L\_REG Register (Offset = 20040h) [reset = 0h]

CPSW PFC Global Tx Buffer Threshold Clear Low

Return to [Summary Table](#)

**Table 5-251. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 0040h       |

**Figure 5-84. CPSW\_NC\_TX\_G\_BUF\_THRESH\_CLR\_L\_REG Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PRI3 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PRI2 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PRI1 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PRI0 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-253. CPSW\_NC\_TX\_G\_BUF\_THRESH\_CLR\_L\_REG Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                              |
|-------|-------|------|-------|--------------------------------------------------------------------------|
| 31:24 | PRI3  | R/W  | 0h    | Priority Based Flow Control Global Buffer Usage Threshold for Priority 3 |
| 23:16 | PRI2  | R/W  | 0h    | Priority Based Flow Control Global Buffer Usage Threshold for Priority 2 |
| 15:8  | PRI1  | R/W  | 0h    | Priority Based Flow Control Global Buffer Usage Threshold for Priority 1 |
| 7:0   | PRI0  | R/W  | 0h    | Priority Based Flow Control Global Buffer Usage Threshold for Priority 0 |

### 5.1.2.85 CPSW\_NC\_TX\_G\_BUF\_THRESH\_CLR\_H\_REG Register

#### 1 CPSW\_NC\_TX\_G\_BUF\_THRESH\_CLR\_H\_REG Register (Offset = 20044h) [reset = 0h]

CPSW PFC Global Tx Buffer Threshold Clear High

Return to [Summary Table](#)

**Table 5-254. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 0044h       |

**Figure 5-85. CPSW\_NC\_TX\_G\_BUF\_THRESH\_CLR\_H\_REG Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PRI7 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PRI6 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PRI5 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PRI4 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-256. CPSW\_NC\_TX\_G\_BUF\_THRESH\_CLR\_H\_REG Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                              |
|-------|-------|------|-------|--------------------------------------------------------------------------|
| 31:24 | PRI7  | R/W  | 0h    | Priority Based Flow Control Global Buffer Usage Threshold for Priority 7 |
| 23:16 | PRI6  | R/W  | 0h    | Priority Based Flow Control Global Buffer Usage Threshold for Priority 6 |
| 15:8  | PRI5  | R/W  | 0h    | Priority Based Flow Control Global Buffer Usage Threshold for Priority 5 |
| 7:0   | PRI4  | R/W  | 0h    | Priority Based Flow Control Global Buffer Usage Threshold for Priority 4 |

### 5.1.2.86 CPSW\_NC\_VLAN\_LTYPE\_REG Register

#### 1 CPSW\_NC\_VLAN\_LTYPE\_REG Register (Offset = 20050h) [reset = 88A88100h]

VLAN Length/type

Return to [Summary Table](#)

**Table 5-257. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 0050h       |

**Figure 5-86. CPSW\_NC\_VLAN\_LTYPE\_REG Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| VLAN_LTYPE_OUTER |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 88A8h            |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| VLAN_LTYPE_OUTER |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 88A8h            |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| VLAN_LTYPE_INNER |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 8100h            |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| VLAN_LTYPE_INNER |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 8100h            |    |    |    |    |    |    |    |

**Table 5-259. CPSW\_NC\_VLAN\_LTYPE\_REG Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description      |
|-------|------------------|------|-------|------------------|
| 31:16 | VLAN_LTYPE_OUTER | R/W  | 88A8h | Outer VLAN LType |
| 15:0  | VLAN_LTYPE_INNER | R/W  | 8100h | Inner VLAN LType |

### 5.1.2.87 CPSW\_NC\_EST\_TS\_DOMAIN\_REG Register

#### 1 CPSW\_NC\_EST\_TS\_DOMAIN\_REG Register (Offset = 20054h) [reset = 0h]

Enhanced Scheduled Traffic Host Event Domain

Return to [Summary Table](#)

**Table 5-260. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 0054h       |

**Figure 5-87. CPSW\_NC\_EST\_TS\_DOMAIN\_REG Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| EST_TS_DOMAIN |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 5-262. CPSW\_NC\_EST\_TS\_DOMAIN\_REG Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                                                                                                     |
|------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED      | NONE | 0h    | Reserved                                                                                                                        |
| 7:0  | EST_TS_DOMAIN | R/W  | 0h    | Enhanced Scheduled Traffic domain. This value is used as the domain in the CPTS event to indicate that the event came from EST. |

### 5.1.2.88 CPSW\_NC\_TX\_PRI0\_MAXLEN\_REG Register

#### 1 CPSW\_NC\_TX\_PRI0\_MAXLEN\_REG Register (Offset = 20100h) [reset = 7E8h]

Transmit Priority 0 Maximum Length

Return to [Summary Table](#)

**Table 5-263. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 0100h       |

**Figure 5-88. CPSW\_NC\_TX\_PRI0\_MAXLEN\_REG Name Register**

|                |    |                |    |    |    |    |    |
|----------------|----|----------------|----|----|----|----|----|
| 31             | 30 | 29             | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |                |    |    |    |    |    |
| NONE           |    |                |    |    |    |    |    |
| 0h             |    |                |    |    |    |    |    |
| 23             | 22 | 21             | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |                |    |    |    |    |    |
| NONE           |    |                |    |    |    |    |    |
| 0h             |    |                |    |    |    |    |    |
| 15             | 14 | 13             | 12 | 11 | 10 | 9  | 8  |
| RESERVED       |    | TX_PRI0_MAXLEN |    |    |    |    |    |
| NONE           |    | R/W            |    |    |    |    |    |
| 0h             |    | 7E8h           |    |    |    |    |    |
| 7              | 6  | 5              | 4  | 3  | 2  | 1  | 0  |
| TX_PRI0_MAXLEN |    |                |    |    |    |    |    |
| R/W            |    |                |    |    |    |    |    |
| 7E8h           |    |                |    |    |    |    |    |

**Table 5-265. CPSW\_NC\_TX\_PRI0\_MAXLEN\_REG Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:14 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                        |
| 13:0  | TX_PRI0_MAXLEN | R/W  | 7E8h  | This value determines the maximum packet length that will be transmitted on priority 0 Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal or any other egress processing). Packets on a priority that are larger than this value are dropped. |

### 5.1.2.89 CPSW\_NC\_TX\_PRI1\_MAXLEN\_REG Register

#### 1 CPSW\_NC\_TX\_PRI1\_MAXLEN\_REG Register (Offset = 20104h) [reset = 7E8h]

Transmit Priority 1 Maximum Length

Return to [Summary Table](#)

**Table 5-266. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 0104h       |

**Figure 5-89. CPSW\_NC\_TX\_PRI1\_MAXLEN\_REG Name Register**

|                |    |                |    |    |    |    |    |
|----------------|----|----------------|----|----|----|----|----|
| 31             | 30 | 29             | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |                |    |    |    |    |    |
| NONE           |    |                |    |    |    |    |    |
| 0h             |    |                |    |    |    |    |    |
| 23             | 22 | 21             | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |                |    |    |    |    |    |
| NONE           |    |                |    |    |    |    |    |
| 0h             |    |                |    |    |    |    |    |
| 15             | 14 | 13             | 12 | 11 | 10 | 9  | 8  |
| RESERVED       |    | TX_PRI1_MAXLEN |    |    |    |    |    |
| NONE           |    | R/W            |    |    |    |    |    |
| 0h             |    | 7E8h           |    |    |    |    |    |
| 7              | 6  | 5              | 4  | 3  | 2  | 1  | 0  |
| TX_PRI1_MAXLEN |    |                |    |    |    |    |    |
| R/W            |    |                |    |    |    |    |    |
| 7E8h           |    |                |    |    |    |    |    |

**Table 5-268. CPSW\_NC\_TX\_PRI1\_MAXLEN\_REG Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:14 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                        |
| 13:0  | TX_PRI1_MAXLEN | R/W  | 7E8h  | This value determines the maximum packet length that will be transmitted on priority 1 Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal or any other egress processing). Packets on a priority that are larger than this value are dropped. |

### 5.1.2.90 CPSW\_NC\_TX\_PRI2\_MAXLEN\_REG Register

#### 1 CPSW\_NC\_TX\_PRI2\_MAXLEN\_REG Register (Offset = 20108h) [reset = 7E8h]

Transmit Priority 2 Maximum Length

Return to [Summary Table](#)

**Table 5-269. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 0108h       |

**Figure 5-90. CPSW\_NC\_TX\_PRI2\_MAXLEN\_REG Name Register**

|                |    |                |    |    |    |    |    |
|----------------|----|----------------|----|----|----|----|----|
| 31             | 30 | 29             | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |                |    |    |    |    |    |
| NONE           |    |                |    |    |    |    |    |
| 0h             |    |                |    |    |    |    |    |
| 23             | 22 | 21             | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |                |    |    |    |    |    |
| NONE           |    |                |    |    |    |    |    |
| 0h             |    |                |    |    |    |    |    |
| 15             | 14 | 13             | 12 | 11 | 10 | 9  | 8  |
| RESERVED       |    | TX_PRI2_MAXLEN |    |    |    |    |    |
| NONE           |    | R/W            |    |    |    |    |    |
| 0h             |    | 7E8h           |    |    |    |    |    |
| 7              | 6  | 5              | 4  | 3  | 2  | 1  | 0  |
| TX_PRI2_MAXLEN |    |                |    |    |    |    |    |
| R/W            |    |                |    |    |    |    |    |
| 7E8h           |    |                |    |    |    |    |    |

**Table 5-271. CPSW\_NC\_TX\_PRI2\_MAXLEN\_REG Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:14 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                        |
| 13:0  | TX_PRI2_MAXLEN | R/W  | 7E8h  | This value determines the maximum packet length that will be transmitted on priority 2 Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal or any other egress processing). Packets on a priority that are larger than this value are dropped. |

### 5.1.2.91 CPSW\_NC\_TX\_PRI3\_MAXLEN\_REG Register

#### 1 CPSW\_NC\_TX\_PRI3\_MAXLEN\_REG Register (Offset = 2010Ch) [reset = 7E8h]

Transmit Priority 3 Maximum Length

Return to [Summary Table](#)

**Table 5-272. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 010Ch       |

**Figure 5-91. CPSW\_NC\_TX\_PRI3\_MAXLEN\_REG Name Register**

|                |    |                |    |    |    |    |    |
|----------------|----|----------------|----|----|----|----|----|
| 31             | 30 | 29             | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |                |    |    |    |    |    |
| NONE           |    |                |    |    |    |    |    |
| 0h             |    |                |    |    |    |    |    |
| 23             | 22 | 21             | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |                |    |    |    |    |    |
| NONE           |    |                |    |    |    |    |    |
| 0h             |    |                |    |    |    |    |    |
| 15             | 14 | 13             | 12 | 11 | 10 | 9  | 8  |
| RESERVED       |    | TX_PRI3_MAXLEN |    |    |    |    |    |
| NONE           |    | R/W            |    |    |    |    |    |
| 0h             |    | 7E8h           |    |    |    |    |    |
| 7              | 6  | 5              | 4  | 3  | 2  | 1  | 0  |
| TX_PRI3_MAXLEN |    |                |    |    |    |    |    |
| R/W            |    |                |    |    |    |    |    |
| 7E8h           |    |                |    |    |    |    |    |

**Table 5-274. CPSW\_NC\_TX\_PRI3\_MAXLEN\_REG Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:14 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                        |
| 13:0  | TX_PRI3_MAXLEN | R/W  | 7E8h  | This value determines the maximum packet length that will be transmitted on priority 3 Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal or any other egress processing). Packets on a priority that are larger than this value are dropped. |



### 5.1.2.92 CPSW\_NC\_TX\_PRI4\_MAXLEN\_REG Register

#### 1 CPSW\_NC\_TX\_PRI4\_MAXLEN\_REG Register (Offset = 20110h) [reset = 7E8h]

Transmit Priority 4 Maximum Length

Return to [Summary Table](#)

**Table 5-275. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 0110h       |

**Figure 5-92. CPSW\_NC\_TX\_PRI4\_MAXLEN\_REG Name Register**

|                |    |                |    |    |    |    |    |
|----------------|----|----------------|----|----|----|----|----|
| 31             | 30 | 29             | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |                |    |    |    |    |    |
| NONE           |    |                |    |    |    |    |    |
| 0h             |    |                |    |    |    |    |    |
| 23             | 22 | 21             | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |                |    |    |    |    |    |
| NONE           |    |                |    |    |    |    |    |
| 0h             |    |                |    |    |    |    |    |
| 15             | 14 | 13             | 12 | 11 | 10 | 9  | 8  |
| RESERVED       |    | TX_PRI4_MAXLEN |    |    |    |    |    |
| NONE           |    | R/W            |    |    |    |    |    |
| 0h             |    | 7E8h           |    |    |    |    |    |
| 7              | 6  | 5              | 4  | 3  | 2  | 1  | 0  |
| TX_PRI4_MAXLEN |    |                |    |    |    |    |    |
| R/W            |    |                |    |    |    |    |    |
| 7E8h           |    |                |    |    |    |    |    |

**Table 5-277. CPSW\_NC\_TX\_PRI4\_MAXLEN\_REG Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:14 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                        |
| 13:0  | TX_PRI4_MAXLEN | R/W  | 7E8h  | This value determines the maximum packet length that will be transmitted on priority 4 Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal or any other egress processing). Packets on a priority that are larger than this value are dropped. |

### 5.1.2.93 CPSW\_NC\_TX\_PRI5\_MAXLEN\_REG Register

#### 1 CPSW\_NC\_TX\_PRI5\_MAXLEN\_REG Register (Offset = 20114h) [reset = 7E8h]

Transmit Priority 5 Maximum Length

Return to [Summary Table](#)

**Table 5-278. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 0114h       |

**Figure 5-93. CPSW\_NC\_TX\_PRI5\_MAXLEN\_REG Name Register**

|                |    |                |    |    |    |    |    |
|----------------|----|----------------|----|----|----|----|----|
| 31             | 30 | 29             | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |                |    |    |    |    |    |
| NONE           |    |                |    |    |    |    |    |
| 0h             |    |                |    |    |    |    |    |
| 23             | 22 | 21             | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |                |    |    |    |    |    |
| NONE           |    |                |    |    |    |    |    |
| 0h             |    |                |    |    |    |    |    |
| 15             | 14 | 13             | 12 | 11 | 10 | 9  | 8  |
| RESERVED       |    | TX_PRI5_MAXLEN |    |    |    |    |    |
| NONE           |    | R/W            |    |    |    |    |    |
| 0h             |    | 7E8h           |    |    |    |    |    |
| 7              | 6  | 5              | 4  | 3  | 2  | 1  | 0  |
| TX_PRI5_MAXLEN |    |                |    |    |    |    |    |
| R/W            |    |                |    |    |    |    |    |
| 7E8h           |    |                |    |    |    |    |    |

**Table 5-280. CPSW\_NC\_TX\_PRI5\_MAXLEN\_REG Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:14 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                        |
| 13:0  | TX_PRI5_MAXLEN | R/W  | 7E8h  | This value determines the maximum packet length that will be transmitted on priority 5 Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal or any other egress processing). Packets on a priority that are larger than this value are dropped. |

### 5.1.2.94 CPSW\_NC\_TX\_PRI6\_MAXLEN\_REG Register

#### 1 CPSW\_NC\_TX\_PRI6\_MAXLEN\_REG Register (Offset = 20118h) [reset = 7E8h]

Transmit Priority 6 Maximum Length

Return to [Summary Table](#)

**Table 5-281. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 0118h       |

**Figure 5-94. CPSW\_NC\_TX\_PRI6\_MAXLEN\_REG Name Register**

|                |    |                |    |    |    |    |    |
|----------------|----|----------------|----|----|----|----|----|
| 31             | 30 | 29             | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |                |    |    |    |    |    |
| NONE           |    |                |    |    |    |    |    |
| 0h             |    |                |    |    |    |    |    |
| 23             | 22 | 21             | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |                |    |    |    |    |    |
| NONE           |    |                |    |    |    |    |    |
| 0h             |    |                |    |    |    |    |    |
| 15             | 14 | 13             | 12 | 11 | 10 | 9  | 8  |
| RESERVED       |    | TX_PRI6_MAXLEN |    |    |    |    |    |
| NONE           |    | R/W            |    |    |    |    |    |
| 0h             |    | 7E8h           |    |    |    |    |    |
| 7              | 6  | 5              | 4  | 3  | 2  | 1  | 0  |
| TX_PRI6_MAXLEN |    |                |    |    |    |    |    |
| R/W            |    |                |    |    |    |    |    |
| 7E8h           |    |                |    |    |    |    |    |

**Table 5-283. CPSW\_NC\_TX\_PRI6\_MAXLEN\_REG Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:14 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                        |
| 13:0  | TX_PRI6_MAXLEN | R/W  | 7E8h  | This value determines the maximum packet length that will be transmitted on priority 6 Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal or any other egress processing). Packets on a priority that are larger than this value are dropped. |

### 5.1.2.95 CPSW\_NC\_TX\_PRI7\_MAXLEN\_REG Register

#### 1 CPSW\_NC\_TX\_PRI7\_MAXLEN\_REG Register (Offset = 2011Ch) [reset = 7E8h]

Transmit Priority 7 Maximum Length

Return to [Summary Table](#)

**Table 5-284. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 011Ch       |

**Figure 5-95. CPSW\_NC\_TX\_PRI7\_MAXLEN\_REG Name Register**

|                |    |                |    |    |    |    |    |
|----------------|----|----------------|----|----|----|----|----|
| 31             | 30 | 29             | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |                |    |    |    |    |    |
| NONE           |    |                |    |    |    |    |    |
| 0h             |    |                |    |    |    |    |    |
| 23             | 22 | 21             | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |                |    |    |    |    |    |
| NONE           |    |                |    |    |    |    |    |
| 0h             |    |                |    |    |    |    |    |
| 15             | 14 | 13             | 12 | 11 | 10 | 9  | 8  |
| RESERVED       |    | TX_PRI7_MAXLEN |    |    |    |    |    |
| NONE           |    | R/W            |    |    |    |    |    |
| 0h             |    | 7E8h           |    |    |    |    |    |
| 7              | 6  | 5              | 4  | 3  | 2  | 1  | 0  |
| TX_PRI7_MAXLEN |    |                |    |    |    |    |    |
| R/W            |    |                |    |    |    |    |    |
| 7E8h           |    |                |    |    |    |    |    |

**Table 5-286. CPSW\_NC\_TX\_PRI7\_MAXLEN\_REG Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:14 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                        |
| 13:0  | TX_PRI7_MAXLEN | R/W  | 7E8h  | This value determines the maximum packet length that will be transmitted on priority 7 Ethernet egress for all Ethernet ports. The packet length compared to the maximum length value is the ingress packet length (not the actual egress packet length which is the length before VLAN addition or removal or any other egress processing). Packets on a priority that are larger than this value are dropped. |

### 5.1.2.96 CPSW\_NC\_CPPI\_P0\_CONTROL\_REG Register

#### 1 CPSW\_NC\_CPPI\_P0\_CONTROL\_REG Register (Offset = 21004h) [reset = 0h]

CPPI Port 0 Control

Return to [Summary Table](#)
**Table 5-287. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 1004h       |

**Figure 5-96. CPSW\_NC\_CPPI\_P0\_CONTROL\_REG Name Register**

|                   |                   |          |    |                    |                      |                      |                    |
|-------------------|-------------------|----------|----|--------------------|----------------------|----------------------|--------------------|
| 31                | 30                | 29       | 28 | 27                 | 26                   | 25                   | 24                 |
| RESERVED          |                   |          |    |                    |                      |                      |                    |
| NONE              |                   |          |    |                    |                      |                      |                    |
| 0h                |                   |          |    |                    |                      |                      |                    |
| 23                | 22                | 21       | 20 | 19                 | 18                   | 17                   | 16                 |
| RESERVED          |                   |          |    |                    | FH_REMAP_D<br>SCP_V6 | FH_REMAP_D<br>SCP_V4 | FH_REMAP_VL<br>AN  |
| NONE              |                   |          |    |                    | R/W                  | R/W                  | R/W                |
| 0h                |                   |          |    |                    | 0h                   | 0h                   | 0h                 |
| 15                | 14                | 13       | 12 | 11                 | 10                   | 9                    | 8                  |
| FH_ECC_ERR_<br>EN | TH_ECC_ERR_<br>EN | RESERVED |    |                    |                      |                      |                    |
| R/W               | R/W               | NONE     |    |                    |                      |                      |                    |
| 0h                | 0h                | 0h       |    |                    |                      |                      |                    |
| 7                 | 6                 | 5        | 4  | 3                  | 2                    | 1                    | 0                  |
| RESERVED          |                   |          |    | TH_CHECKSU<br>M_EN | FH_DSCP_IPV<br>6_EN  | FH_DSCP_IPV<br>4_EN  | FH_CHECKSU<br>M_EN |
| NONE              |                   |          |    | R/W                | R/W                  | R/W                  | R/W                |
| 0h                |                   |          |    | 0h                 | 0h                   | 0h                   | 0h                 |

**Table 5-289. CPSW\_NC\_CPPI\_P0\_CONTROL\_REG Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                        |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:19 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                           |
| 18    | FH_REMAP_DSCP_V6 | R/W  | 0h    | Port 0 FHost (ingress) remap priority to DSCP IPV6 priority (see packet priority handling section for details).<br>0 - Hardware switch priority IPV6 DSCP priority remapping is disabled.<br>1 - Hardware switch priority IPV6 DSCP priority remapping is enabled. |
| 17    | FH_REMAP_DSCP_V4 | R/W  | 0h    | Port 0 FHost (ingress) remap priority to DSCP IPV4 priority (see packet priority handling section for details).<br>0 - Hardware switch priority IPV4 DSCP priority remapping is disabled.<br>1 - Hardware switch priority IPV4 DSCP priority remapping is enabled. |
| 16    | FH_REMAP_VLAN    | R/W  | 0h    | Port 0 receive (ingress) remap priority to VLAN. See priority remapping section for details.                                                                                                                                                                       |
| 15    | FH_ECC_ERR_EN    | R/W  | 0h    | Port 0 FHost ECC Error Enable. This bit must be set to enable FHost ECC error operations                                                                                                                                                                           |
| 14    | TH_ECC_ERR_EN    | R/W  | 0h    | Port 0 THost ECC Error Enable. This bit must be set to enable THost ECC error operations.                                                                                                                                                                          |
| 13:4  | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                           |

**Table 5-289. CPSW\_NC\_CPPI\_P0\_CONTROL\_REG Register Field Descriptions (continued)**

| Bit | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                  |
|-----|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3   | TH_CHECKSUM_EN  | R/W  | 0h    | Port 0 THost (egress) Checksum Enable<br>0 - THost checksum is disabled.<br>1 - THost checksum is enabled. IPV4/V6 Packets have checksum information (4-bytes) included at the end of the packet data when the chksum_encap descriptor bit is set in the EOP THost buffer descriptor.                        |
| 2   | FH_DSCP_IPV6_EN | R/W  | 0h    | Port 0 FHost IPv6 DSCP enable<br>0 - Ipv6 DSCP priority mapping is disabled.<br>1 - Ipv6 DSCP priority mapping is enabled.                                                                                                                                                                                   |
| 1   | FH_DSCP_IPV4_EN | R/W  | 0h    | Port 0 FHost IPv4 DSCP enable<br>0 - Ipv4 DSCP priority mapping is disabled.<br>1 - Ipv4 DSCP priority mapping is enabled.                                                                                                                                                                                   |
| 0   | FH_CHECKSUM_EN  | R/W  | 0h    | Port 0 FHost (port 0 ingress) Checksum Enable<br>0 - FHost checksum is disabled.<br>1 - FHost checksum is enabled. Four bytes of checksum information can be included at the start of the packet data to be used for checksum packet processing when chksum_encap is set in the SOP FHost buffer descriptor. |

### 5.1.2.97 CPSW\_NC\_CPPI\_P0\_BLK\_CNT\_REG Register

#### 1 CPSW\_NC\_CPPI\_P0\_BLK\_CNT\_REG Register (Offset = 21010h) [reset = 1h]

CPPI Port 0 FIFO Block Usage Count

Return to [Summary Table](#)

**Table 5-290. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 1010h       |

**Figure 5-97. CPSW\_NC\_CPPI\_P0\_BLK\_CNT\_REG Name Register**

|          |    |            |    |            |    |    |    |
|----------|----|------------|----|------------|----|----|----|
| 31       | 30 | 29         | 28 | 27         | 26 | 25 | 24 |
| RESERVED |    |            |    |            |    |    |    |
| NONE     |    |            |    |            |    |    |    |
| 0h       |    |            |    |            |    |    |    |
| 23       | 22 | 21         | 20 | 19         | 18 | 17 | 16 |
| RESERVED |    |            |    |            |    |    |    |
| NONE     |    |            |    |            |    |    |    |
| 0h       |    |            |    |            |    |    |    |
| 15       | 14 | 13         | 12 | 11         | 10 | 9  | 8  |
| RESERVED |    |            |    | TH_BLK_CNT |    |    |    |
| NONE     |    |            |    | R          |    |    |    |
| 0h       |    |            |    | 0h         |    |    |    |
| 7        | 6  | 5          | 4  | 3          | 2  | 1  | 0  |
| RESERVED |    | FH_BLK_CNT |    |            |    |    |    |
| NONE     |    | R          |    |            |    |    |    |
| 0h       |    | 1h         |    |            |    |    |    |

**Table 5-292. CPSW\_NC\_CPPI\_P0\_BLK\_CNT\_REG Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                          |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:13 | RESERVED   | NONE | 0h    | Reserved                                                                                                                                                                             |
| 12:8  | TH_BLK_CNT | R    | 0h    | Port 0 Transmit Block Count Usage - This value is the number of blocks allocated to the FIFO logical transmit queues.<br>note: for N=2 this field is always zero (no transmit FIFO). |
| 7:6   | RESERVED   | NONE | 0h    | Reserved                                                                                                                                                                             |
| 5:0   | FH_BLK_CNT | R    | 1h    | Port 0 Receive Block Count Usage - This value is the number of blocks allocated in the receive FIFO.                                                                                 |

### 5.1.2.98 CPSW\_NC\_CPPI\_P0\_PORT\_VLAN\_REG Register

#### 1 CPSW\_NC\_CPPI\_P0\_PORT\_VLAN\_REG Register (Offset = 21014h) [reset = 0h]

CPPI Port 0 VLAN

Return to [Summary Table](#)

**Table 5-293. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 1014h       |

**Figure 5-98. CPSW\_NC\_CPPI\_P0\_PORT\_VLAN\_REG Name Register**

|          |    |    |          |          |    |    |    |
|----------|----|----|----------|----------|----|----|----|
| 31       | 30 | 29 | 28       | 27       | 26 | 25 | 24 |
| RESERVED |    |    |          |          |    |    |    |
| NONE     |    |    |          |          |    |    |    |
| 0h       |    |    |          |          |    |    |    |
| 23       | 22 | 21 | 20       | 19       | 18 | 17 | 16 |
| RESERVED |    |    |          |          |    |    |    |
| NONE     |    |    |          |          |    |    |    |
| 0h       |    |    |          |          |    |    |    |
| 15       | 14 | 13 | 12       | 11       | 10 | 9  | 8  |
| PORT_PRI |    |    | PORT_CFI | PORT_VID |    |    |    |
| R/W      |    |    | R/W      | R/W      |    |    |    |
| 0h       |    |    | 0h       | 0h       |    |    |    |
| 7        | 6  | 5  | 4        | 3        | 2  | 1  | 0  |
| PORT_VID |    |    |          |          |    |    |    |
| R/W      |    |    |          |          |    |    |    |
| 0h       |    |    |          |          |    |    |    |

**Table 5-295. CPSW\_NC\_CPPI\_P0\_PORT\_VLAN\_REG Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description        |
|-------|----------|------|-------|--------------------|
| 31:16 | RESERVED | NONE | 0h    | Reserved           |
| 15:13 | PORT_PRI | R/W  | 0h    | Port VLAN Priority |
| 12    | PORT_CFI | R/W  | 0h    | Port CFI bit       |
| 11:0  | PORT_VID | R/W  | 0h    | Port VLAN ID       |



### 5.1.2.99 CPSW\_NC\_CPPI\_P0\_TH\_PRI\_MAP\_REG Register

#### 1 CPSW\_NC\_CPPI\_P0\_TH\_PRI\_MAP\_REG Register (Offset = 21018h) [reset = 76543210h]

CPPI Port 0 Tx Header Pri to Switch Pri Mapping

Return to [Summary Table](#)

**Table 5-296. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 1018h       |

**Figure 5-99. CPSW\_NC\_CPPI\_P0\_TH\_PRI\_MAP\_REG Name Register**

| 31       | 30 | 29   | 28 | 27       | 26 | 25   | 24 |
|----------|----|------|----|----------|----|------|----|
| RESERVED |    | PRI7 |    | RESERVED |    | PRI6 |    |
| NONE     |    | R/W  |    | NONE     |    | R/W  |    |
| 0h       |    | 7h   |    | 0h       |    | 6h   |    |
| 23       | 22 | 21   | 20 | 19       | 18 | 17   | 16 |
| RESERVED |    | PRI5 |    | RESERVED |    | PRI4 |    |
| NONE     |    | R/W  |    | NONE     |    | R/W  |    |
| 0h       |    | 5h   |    | 0h       |    | 4h   |    |
| 15       | 14 | 13   | 12 | 11       | 10 | 9    | 8  |
| RESERVED |    | PRI3 |    | RESERVED |    | PRI2 |    |
| NONE     |    | R/W  |    | NONE     |    | R/W  |    |
| 0h       |    | 3h   |    | 0h       |    | 2h   |    |
| 7        | 6  | 5    | 4  | 3        | 2  | 1    | 0  |
| RESERVED |    | PRI1 |    | RESERVED |    | PRI0 |    |
| NONE     |    | R/W  |    | NONE     |    | R/W  |    |
| 0h       |    | 1h   |    | 0h       |    | 0h   |    |

**Table 5-298. CPSW\_NC\_CPPI\_P0\_TH\_PRI\_MAP\_REG Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                       |
|-------|----------|------|-------|-----------------------------------------------------------------------------------|
| 31    | RESERVED | NONE | 0h    | Reserved                                                                          |
| 30:28 | PRI7     | R/W  | 7h    | Priority 7 - A packet header priority of 0x7 is given this switch queue priority. |
| 27    | RESERVED | NONE | 0h    | Reserved                                                                          |
| 26:24 | PRI6     | R/W  | 6h    | Priority 6 - A packet header priority of 0x7 is given this switch queue priority. |
| 23    | RESERVED | NONE | 0h    | Reserved                                                                          |
| 22:20 | PRI5     | R/W  | 5h    | Priority 5 - A packet header priority of 0x7 is given this switch queue priority. |
| 19    | RESERVED | NONE | 0h    | Reserved                                                                          |
| 18:16 | PRI4     | R/W  | 4h    | Priority 4 - A packet header priority of 0x7 is given this switch queue priority. |
| 15    | RESERVED | NONE | 0h    | Reserved                                                                          |
| 14:12 | PRI3     | R/W  | 3h    | Priority 3 - A packet header priority of 0x7 is given this switch queue priority. |
| 11    | RESERVED | NONE | 0h    | Reserved                                                                          |
| 10:8  | PRI2     | R/W  | 2h    | Priority 2 - A packet header priority of 0x7 is given this switch queue priority. |
| 7     | RESERVED | NONE | 0h    | Reserved                                                                          |

**Table 5-298. CPSW\_NC\_CPPI\_P0\_TH\_PRI\_MAP\_REG Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                                                                       |
|-----|----------|------|-------|-----------------------------------------------------------------------------------|
| 6:4 | PRI1     | R/W  | 1h    | Priority 1 - A packet header priority of 0x7 is given this switch queue priority. |
| 3   | RESERVED | NONE | 0h    | Reserved                                                                          |
| 2:0 | PRI0     | R/W  | 0h    | Priority 0 - A packet header priority of 0x7 is given this switch queue priority. |

### 5.1.2.100 CPSW\_NC\_CPPI\_P0\_PRI\_CTL\_REG Register

#### 1 CPSW\_NC\_CPPI\_P0\_PRI\_CTL\_REG Register (Offset = 2101Ch) [reset = 0h]

CPPI Port 0 Priority Control

Return to [Summary Table](#)

**Table 5-299. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 101Ch       |

**Figure 5-100. CPSW\_NC\_CPPI\_P0\_PRI\_CTL\_REG Name Register**

|             |    |    |    |    |    |    |          |
|-------------|----|----|----|----|----|----|----------|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24       |
| RESERVED    |    |    |    |    |    |    |          |
| NONE        |    |    |    |    |    |    |          |
| 0h          |    |    |    |    |    |    |          |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16       |
| FH_FLOW_PRI |    |    |    |    |    |    |          |
| R/W         |    |    |    |    |    |    |          |
| 0h          |    |    |    |    |    |    |          |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8        |
| RESERVED    |    |    |    |    |    |    | FH_PTYPE |
| NONE        |    |    |    |    |    |    | R/W      |
| 0h          |    |    |    |    |    |    | 0h       |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0        |
| RESERVED    |    |    |    |    |    |    |          |
| NONE        |    |    |    |    |    |    |          |
| 0h          |    |    |    |    |    |    |          |

**Table 5-301. CPSW\_NC\_CPPI\_P0\_PRI\_CTL\_REG Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                |
|-------|-------------|------|-------|------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED    | NONE | 0h    | Reserved                                                                                                   |
| 23:16 | FH_FLOW_PRI | R/W  | 0h    | Receive Priority Based Flow Control Enable (per priority).<br>Note: for N=2 this field should remain zero. |
| 15:9  | RESERVED    | NONE | 0h    | Reserved                                                                                                   |
| 8     | FH_PTYPE    | R/W  | 0h    | Receive Priority Type                                                                                      |
| 7:0   | RESERVED    | NONE | 0h    | Reserved                                                                                                   |

### 5.1.2.101 CPSW\_NC\_CPPI\_P0\_FH\_PRI\_MAP\_REG Register

#### 1 CPSW\_NC\_CPPI\_P0\_FH\_PRI\_MAP\_REG Register (Offset = 21020h) [reset = 76543210h]

CPPI Port 0 RX Pkt Pri to Header Pri Map

Return to [Summary Table](#)

**Table 5-302. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 1020h       |

**Figure 5-101. CPSW\_NC\_CPPI\_P0\_FH\_PRI\_MAP\_REG Name Register**

| 31       | 30 | 29   | 28 | 27       | 26 | 25   | 24 |
|----------|----|------|----|----------|----|------|----|
| RESERVED |    | PRI7 |    | RESERVED |    | PRI6 |    |
| NONE     |    | R/W  |    | NONE     |    | R/W  |    |
| 0h       |    | 7h   |    | 0h       |    | 6h   |    |
| 23       | 22 | 21   | 20 | 19       | 18 | 17   | 16 |
| RESERVED |    | PRI5 |    | RESERVED |    | PRI4 |    |
| NONE     |    | R/W  |    | NONE     |    | R/W  |    |
| 0h       |    | 5h   |    | 0h       |    | 4h   |    |
| 15       | 14 | 13   | 12 | 11       | 10 | 9    | 8  |
| RESERVED |    | PRI3 |    | RESERVED |    | PRI2 |    |
| NONE     |    | R/W  |    | NONE     |    | R/W  |    |
| 0h       |    | 3h   |    | 0h       |    | 2h   |    |
| 7        | 6  | 5    | 4  | 3        | 2  | 1    | 0  |
| RESERVED |    | PRI1 |    | RESERVED |    | PRI0 |    |
| NONE     |    | R/W  |    | NONE     |    | R/W  |    |
| 0h       |    | 1h   |    | 0h       |    | 0h   |    |

**Table 5-304. CPSW\_NC\_CPPI\_P0\_FH\_PRI\_MAP\_REG Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                               |
|-------|----------|------|-------|-------------------------------------------------------------------------------------------|
| 31    | RESERVED | NONE | 0h    | Reserved                                                                                  |
| 30:28 | PRI7     | R/W  | 7h    | Priority 7 - A packet priority of 0x7 is mapped (changed) to this header packet priority. |
| 27    | RESERVED | NONE | 0h    | Reserved                                                                                  |
| 26:24 | PRI6     | R/W  | 6h    | Priority 6 - A packet priority of 0x6 is mapped (changed) to this header packet priority. |
| 23    | RESERVED | NONE | 0h    | Reserved                                                                                  |
| 22:20 | PRI5     | R/W  | 5h    | Priority 5 - A packet priority of 0x5 is mapped (changed) to this header packet priority. |
| 19    | RESERVED | NONE | 0h    | Reserved                                                                                  |
| 18:16 | PRI4     | R/W  | 4h    | Priority 4 - A packet priority of 0x4 is mapped (changed) to this header packet priority. |
| 15    | RESERVED | NONE | 0h    | Reserved                                                                                  |
| 14:12 | PRI3     | R/W  | 3h    | Priority 3 - A packet priority of 0x3 is mapped (changed) to this header packet priority. |
| 11    | RESERVED | NONE | 0h    | Reserved                                                                                  |
| 10:8  | PRI2     | R/W  | 2h    | Priority 2 - A packet priority of 0x2 is mapped (changed) to this header packet priority. |
| 7     | RESERVED | NONE | 0h    | Reserved                                                                                  |

**Table 5-304. CPSW\_NC\_CPPI\_P0\_FH\_PRI\_MAP\_REG Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                                                                               |
|-----|----------|------|-------|-------------------------------------------------------------------------------------------|
| 6:4 | PRI1     | R/W  | 1h    | Priority 1 - A packet priority of 0x1 is mapped (changed) to this header packet priority. |
| 3   | RESERVED | NONE | 0h    | Reserved                                                                                  |
| 2:0 | PRI0     | R/W  | 0h    | Priority 0 - A packet priority of 0x0 is mapped (changed) to this header packet priority. |

### 5.1.2.102 CPSW\_NC\_CPPI\_P0\_FH\_MAXLEN\_REG Register

#### 1 CPSW\_NC\_CPPI\_P0\_FH\_MAXLEN\_REG Register (Offset = 21024h) [reset = 5EEh]

CPPI Port 0 Receive Frame Max Length

Return to [Summary Table](#)

**Table 5-305. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 1024h       |

**Figure 5-102. CPSW\_NC\_CPPI\_P0\_FH\_MAXLEN\_REG Name Register**

|           |    |           |    |    |    |    |    |
|-----------|----|-----------|----|----|----|----|----|
| 31        | 30 | 29        | 28 | 27 | 26 | 25 | 24 |
| RESERVED  |    |           |    |    |    |    |    |
| NONE      |    |           |    |    |    |    |    |
| 0h        |    |           |    |    |    |    |    |
| 23        | 22 | 21        | 20 | 19 | 18 | 17 | 16 |
| RESERVED  |    |           |    |    |    |    |    |
| NONE      |    |           |    |    |    |    |    |
| 0h        |    |           |    |    |    |    |    |
| 15        | 14 | 13        | 12 | 11 | 10 | 9  | 8  |
| RESERVED  |    | FH_MAXLEN |    |    |    |    |    |
| NONE      |    | R/W       |    |    |    |    |    |
| 0h        |    | 5EEh      |    |    |    |    |    |
| 7         | 6  | 5         | 4  | 3  | 2  | 1  | 0  |
| FH_MAXLEN |    |           |    |    |    |    |    |
| R/W       |    |           |    |    |    |    |    |
| 5EEh      |    |           |    |    |    |    |    |

**Table 5-307. CPSW\_NC\_CPPI\_P0\_FH\_MAXLEN\_REG Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:14 | RESERVED  | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 13:0  | FH_MAXLEN | R/W  | 5EEh  | Port 0 Ingress Maximum Frame Length - This field determines the maximum length of a received frame. The reset value is 1518 (dec). Frames with byte counts greater than p0_fh_maxlen are long frames. Long frames with no errors are oversized frames. Long frames with CRC, code, or alignment error are jabber frames. The maximum value is 9604 (including VLAN) when the CPSW is configured with 1 = 4. When 1 = 1 the maximum value is 2024 (including VLAN). |

### 5.1.2.103 CPSW\_NC\_CPPI\_P0\_TH\_BLKs\_PRI\_REG Register

#### 1 CPSW\_NC\_CPPI\_P0\_TH\_BLKs\_PRI\_REG Register (Offset = 21028h) [reset = 1245678h]

CPPI Port 0 Transmit Block Sub Per Priority

Return to [Summary Table](#)

**Table 5-308. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 1028h       |

**Figure 5-103. CPSW\_NC\_CPPI\_P0\_TH\_BLKs\_PRI\_REG Name Register**

| 31 | 30 | 29   | 28 | 27 | 26 | 25   | 24 |
|----|----|------|----|----|----|------|----|
|    |    | PRI7 |    |    |    | PRI6 |    |
|    |    | R/W  |    |    |    | R/W  |    |
|    |    | 0h   |    |    |    | 1h   |    |
| 23 | 22 | 21   | 20 | 19 | 18 | 17   | 16 |
|    |    | PRI5 |    |    |    | PRI4 |    |
|    |    | R/W  |    |    |    | R/W  |    |
|    |    | 2h   |    |    |    | 4h   |    |
| 15 | 14 | 13   | 12 | 11 | 10 | 9    | 8  |
|    |    | PRI3 |    |    |    | PRI2 |    |
|    |    | R/W  |    |    |    | R/W  |    |
|    |    | 5h   |    |    |    | 6h   |    |
| 7  | 6  | 5    | 4  | 3  | 2  | 1    | 0  |
|    |    | PRI1 |    |    |    | PRI0 |    |
|    |    | R/W  |    |    |    | R/W  |    |
|    |    | 7h   |    |    |    | 8h   |    |

**Table 5-310. CPSW\_NC\_CPPI\_P0\_TH\_BLKs\_PRI\_REG Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                     |
|-------|-------|------|-------|---------------------------------|
| 31:28 | PRI7  | R/W  | 0h    | Priority 7 Port Transmit Blocks |
| 27:24 | PRI6  | R/W  | 1h    | Priority 6 Port Transmit Blocks |
| 23:20 | PRI5  | R/W  | 2h    | Priority 5 Port Transmit Blocks |
| 19:16 | PRI4  | R/W  | 4h    | Priority 4 Port Transmit Blocks |
| 15:12 | PRI3  | R/W  | 5h    | Priority 3 Port Transmit Blocks |
| 11:8  | PRI2  | R/W  | 6h    | Priority 2 Port Transmit Blocks |
| 7:4   | PRI1  | R/W  | 7h    | Priority 1 Port Transmit Blocks |
| 3:0   | PRI0  | R/W  | 8h    | Priority 0 Port Transmit Blocks |

### 5.1.2.104 CPSW\_NC\_CPPI\_P0\_IDLE2LPI\_REG Register

#### 1 CPSW\_NC\_CPPI\_P0\_IDLE2LPI\_REG Register (Offset = 21030h) [reset = 0h]

Port 0 EEE Idle to LPI counter

Return to [Summary Table](#)

**Table 5-311. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 1030h       |

**Figure 5-104. CPSW\_NC\_CPPI\_P0\_IDLE2LPI\_REG Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-313. CPSW\_NC\_CPPI\_P0\_IDLE2LPI\_REG Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                       |
|-------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                          |
| 23:0  | COUNT    | R/W  | 0h    | Port 0 EEE Idle to LPI counter load value - After CLKSTOP_REQ is asserted, this value is loaded into the port 0 idle to LPI counter on each clock that the port 0 transmit is not idle. Port 0 enters the transmit LPI state when this counter decrements to zero. This counter decrements each time the EEE prescale counter decrements to zero. |



### 5.1.2.105 CPSW\_NC\_CPPI\_P0\_LPI2WAKE\_REG Register

#### 1 CPSW\_NC\_CPPI\_P0\_LPI2WAKE\_REG Register (Offset = 21034h) [reset = 0h]

Port 0 EEE LPI to wake counter

Return to [Summary Table](#)

**Table 5-314. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 1034h       |

**Figure 5-105. CPSW\_NC\_CPPI\_P0\_LPI2WAKE\_REG Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-316. CPSW\_NC\_CPPI\_P0\_LPI2WAKE\_REG Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 23:0  | COUNT    | R/W  | 0h    | Port 0 EEE LPI to wake counter load value - When the port is in the transmit LPI state and the CLKSTOP_REQ signal is deasserted, this value is loaded into the port 0 LPI to wake counter. Transmit packet operations may begin (resume) when the LPI to wake count decrements to zero (on the pre-scale count). This is the time that the CPDMA transmit must wait before transmit (switch ingress) packet operations begin (resume after wakeup). |

### 5.1.2.106 CPSW\_NC\_CPPI\_P0\_EEE\_STATUS\_REG Register

#### 1 CPSW\_NC\_CPPI\_P0\_EEE\_STATUS\_REG Register (Offset = 21038h) [reset = 60h]

Port 0 EEE status

Return to [Summary Table](#)

**Table 5-317. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 1038h       |

**Figure 5-106. CPSW\_NC\_CPPI\_P0\_EEE\_STATUS\_REG Name Register**

|          |               |               |              |         |        |        |               |
|----------|---------------|---------------|--------------|---------|--------|--------|---------------|
| 31       | 30            | 29            | 28           | 27      | 26     | 25     | 24            |
| RESERVED |               |               |              |         |        |        |               |
| NONE     |               |               |              |         |        |        |               |
| 0h       |               |               |              |         |        |        |               |
| 23       | 22            | 21            | 20           | 19      | 18     | 17     | 16            |
| RESERVED |               |               |              |         |        |        |               |
| NONE     |               |               |              |         |        |        |               |
| 0h       |               |               |              |         |        |        |               |
| 15       | 14            | 13            | 12           | 11      | 10     | 9      | 8             |
| RESERVED |               |               |              |         |        |        |               |
| NONE     |               |               |              |         |        |        |               |
| 0h       |               |               |              |         |        |        |               |
| 7        | 6             | 5             | 4            | 3       | 2      | 1      | 0             |
| RESERVED | TH_FIFO_EMPTY | FH_FIFO_EMPTY | TH_FIFO_HOLD | TH_WAKE | TH_LPI | FH_LPI | WAIT_IDLE2LPI |
| NONE     | R             | R             | R            | R       | R      | R      | R             |
| 0h       | 1h            | 1h            | 0h           | 0h      | 0h     | 0h     | 0h            |

**Table 5-319. CPSW\_NC\_CPPI\_P0\_EEE\_STATUS\_REG Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                                                                   |
|------|---------------|------|-------|-----------------------------------------------------------------------------------------------|
| 31:7 | RESERVED      | NONE | 0h    | Reserved                                                                                      |
| 6    | TH_FIFO_EMPTY | R    | 1h    | CPPI port 0 transmit FIFO (switch egress) is empty - contains no packets                      |
| 5    | FH_FIFO_EMPTY | R    | 1h    | CPPI port 0 receive FIFO (switch ingress) is empty - contains no packets                      |
| 4    | TH_FIFO_HOLD  | R    | 0h    | CPPI port 0 transmit FIFO hold - asserted in the LPI state and during the LPI2WAKE count time |
| 3    | TH_WAKE       | R    | 0h    | CPPI port 0 transmit wakeup - asserted in the transmit LPI2WAKE count time                    |
| 2    | TH_LPI        | R    | 0h    | CPPI port 0 transmit LPI state - asserted when the port 0 transmit is in the LPI state        |
| 1    | FH_LPI        | R    | 0h    | CPPI port 0 receive LPI state - asserted when the port 0 receive is in the LPI state          |
| 0    | WAIT_IDLE2LPI | R    | 0h    | CPPI port 0 wait idle to LPI - asserted when port 0 is counting the IDLE2LPI time             |

### 5.1.2.107 CPSW\_NC\_CPPI\_P0\_FIFO\_STATUS\_REG Register

#### 1 CPSW\_NC\_CPPI\_P0\_FIFO\_STATUS\_REG Register (Offset = 21050h) [reset = 0h]

Port 0 FIFO Status

Return to [Summary Table](#)

**Table 5-320. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 1050h       |

**Figure 5-107. CPSW\_NC\_CPPI\_P0\_FIFO\_STATUS\_REG Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH_PRI_ACTIVE |    |    |    |    |    |    |    |
| R             |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 5-322. CPSW\_NC\_CPPI\_P0\_FIFO\_STATUS\_REG Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                                                                                                                                                                                           |
|------|---------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED      | NONE | 0h    | Reserved                                                                                                                                                                                                              |
| 7:0  | TH_PRI_ACTIVE | R    | 0h    | Port 0 Transmit FIFO Priority Active. Each bit indicates whether the corresponding FIFO priority has one or more queued packets on it or not.<br>note: for N=2 this field is always zero (there is no transmit FIFO). |

### 5.1.2.108 CPSW\_NC\_CPPI\_FH\_DSCP\_MAP\_REG Register

#### 1 CPSW\_NC\_CPPI\_FH\_DSCP\_MAP\_REG Register (Offset = 21120h) [reset = 0h]

CPPI Receive IPV4/IPV6 DSCP Map N

Return to [Summary Table](#)

**Table 5-323. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 1120h       |

**Figure 5-108. CPSW\_NC\_CPPI\_FH\_DSCP\_MAP\_REG Name Register**

| 31       | 30 | 29   | 28 | 27       | 26 | 25   | 24 |
|----------|----|------|----|----------|----|------|----|
| RESERVED |    | PRI7 |    | RESERVED |    | PRI6 |    |
| NONE     |    | R/W  |    | NONE     |    | R/W  |    |
| 0h       |    | 0h   |    | 0h       |    | 0h   |    |
| 23       | 22 | 21   | 20 | 19       | 18 | 17   | 16 |
| RESERVED |    | PRI5 |    | RESERVED |    | PRI4 |    |
| NONE     |    | R/W  |    | NONE     |    | R/W  |    |
| 0h       |    | 0h   |    | 0h       |    | 0h   |    |
| 15       | 14 | 13   | 12 | 11       | 10 | 9    | 8  |
| RESERVED |    | PRI3 |    | RESERVED |    | PRI2 |    |
| NONE     |    | R/W  |    | NONE     |    | R/W  |    |
| 0h       |    | 0h   |    | 0h       |    | 0h   |    |
| 7        | 6  | 5    | 4  | 3        | 2  | 1    | 0  |
| RESERVED |    | PRI1 |    | RESERVED |    | PRI0 |    |
| NONE     |    | R/W  |    | NONE     |    | R/W  |    |
| 0h       |    | 0h   |    | 0h       |    | 0h   |    |

**Table 5-325. CPSW\_NC\_CPPI\_FH\_DSCP\_MAP\_REG Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                     |
|-------|----------|------|-------|-----------------------------------------------------------------|
| 31    | RESERVED | NONE | 0h    | Reserved                                                        |
| 30:28 | PRI7     | R/W  | 0h    | A DSCP IPV4/V6 packet TOS 7 is mapped to this received priority |
| 27    | RESERVED | NONE | 0h    | Reserved                                                        |
| 26:24 | PRI6     | R/W  | 0h    | A DSCP IPV4/V6 packet TOS 6 is mapped to this received priority |
| 23    | RESERVED | NONE | 0h    | Reserved                                                        |
| 22:20 | PRI5     | R/W  | 0h    | A DSCP IPV4/V6 packet TOS 5 is mapped to this received priority |
| 19    | RESERVED | NONE | 0h    | Reserved                                                        |
| 18:16 | PRI4     | R/W  | 0h    | A DSCP IPV4/V6 packet TOS 4 is mapped to this received priority |
| 15    | RESERVED | NONE | 0h    | Reserved                                                        |
| 14:12 | PRI3     | R/W  | 0h    | A DSCP IPV4/V6 packet TOS 3 is mapped to this received priority |
| 11    | RESERVED | NONE | 0h    | Reserved                                                        |
| 10:8  | PRI2     | R/W  | 0h    | A DSCP IPV4/V6 packet TOS 2 is mapped to this received priority |
| 7     | RESERVED | NONE | 0h    | Reserved                                                        |
| 6:4   | PRI1     | R/W  | 0h    | A DSCP IPV4/V6 packet TOS 1 is mapped to this received priority |
| 3     | RESERVED | NONE | 0h    | Reserved                                                        |
| 2:0   | PRI0     | R/W  | 0h    | A DSCP IPV4/V6 packet TOS 0 is mapped to this received priority |

### 5.1.2.109 CPSW\_NC\_CPPI\_P0\_PRI\_CIR\_REG Register

#### 1 CPSW\_NC\_CPPI\_P0\_PRI\_CIR\_REG Register (Offset = 21140h) [reset = 0h]

CPPI Port 0 Rx Priority P Committed Information Rate

Return to [Summary Table](#)

**Table 5-326. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 1140h       |

**Figure 5-109. CPSW\_NC\_CPPI\_P0\_PRI\_CIR\_REG Name Register**

|          |    |    |    |         |    |    |    |
|----------|----|----|----|---------|----|----|----|
| 31       | 30 | 29 | 28 | 27      | 26 | 25 | 24 |
| RESERVED |    |    |    | PRI_CIR |    |    |    |
| NONE     |    |    |    | R/W     |    |    |    |
| 0h       |    |    |    | 0h      |    |    |    |
| 23       | 22 | 21 | 20 | 19      | 18 | 17 | 16 |
| PRI_CIR  |    |    |    |         |    |    |    |
| R/W      |    |    |    |         |    |    |    |
| 0h       |    |    |    |         |    |    |    |
| 15       | 14 | 13 | 12 | 11      | 10 | 9  | 8  |
| PRI_CIR  |    |    |    |         |    |    |    |
| R/W      |    |    |    |         |    |    |    |
| 0h       |    |    |    |         |    |    |    |
| 7        | 6  | 5  | 4  | 3       | 2  | 1  | 0  |
| PRI_CIR  |    |    |    |         |    |    |    |
| R/W      |    |    |    |         |    |    |    |
| 0h       |    |    |    |         |    |    |    |

**Table 5-328. CPSW\_NC\_CPPI\_P0\_PRI\_CIR\_REG Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                           |
|-------|----------|------|-------|---------------------------------------|
| 31:28 | RESERVED | NONE | 0h    | Reserved                              |
| 27:0  | PRI_CIR  | R/W  | 0h    | Priority N Committed Information Rate |

### 5.1.2.110 CPSW\_NC\_CPPI\_P0\_PRI\_EIR\_REG Register

#### 1 CPSW\_NC\_CPPI\_P0\_PRI\_EIR\_REG Register (Offset = 21160h) [reset = 0h]

CPPI Port 0 Rx Priority P Excess Information Rate

Return to [Summary Table](#)

**Table 5-329. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 1160h       |

**Figure 5-110. CPSW\_NC\_CPPI\_P0\_PRI\_EIR\_REG Name Register**

|          |    |    |    |         |    |    |    |
|----------|----|----|----|---------|----|----|----|
| 31       | 30 | 29 | 28 | 27      | 26 | 25 | 24 |
| RESERVED |    |    |    | PRI_EIR |    |    |    |
| NONE     |    |    |    | R/W     |    |    |    |
| 0h       |    |    |    | 0h      |    |    |    |
| 23       | 22 | 21 | 20 | 19      | 18 | 17 | 16 |
| PRI_EIR  |    |    |    |         |    |    |    |
| R/W      |    |    |    |         |    |    |    |
| 0h       |    |    |    |         |    |    |    |
| 15       | 14 | 13 | 12 | 11      | 10 | 9  | 8  |
| PRI_EIR  |    |    |    |         |    |    |    |
| R/W      |    |    |    |         |    |    |    |
| 0h       |    |    |    |         |    |    |    |
| 7        | 6  | 5  | 4  | 3       | 2  | 1  | 0  |
| PRI_EIR  |    |    |    |         |    |    |    |
| R/W      |    |    |    |         |    |    |    |
| 0h       |    |    |    |         |    |    |    |

**Table 5-331. CPSW\_NC\_CPPI\_P0\_PRI\_EIR\_REG Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                        |
|-------|----------|------|-------|------------------------------------|
| 31:28 | RESERVED | NONE | 0h    | Reserved                           |
| 27:0  | PRI_EIR  | R/W  | 0h    | Priority N Excess Information Rate |

### 5.1.2.111 CPSW\_NC\_CPPI\_P0\_TH\_D\_THRESH\_SET\_L\_REG Register

#### 1 CPSW\_NC\_CPPI\_P0\_TH\_D\_THRESH\_SET\_L\_REG Register (Offset = 21180h) [reset = 1F1F1F1Fh]

CPPI Port 0 Tx PFC Destination Threshold Set Low

Return to [Summary Table](#)

**Table 5-332. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 1180h       |

**Figure 5-111. CPSW\_NC\_CPPI\_P0\_TH\_D\_THRESH\_SET\_L\_REG Name Register**

| 31       | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
|----------|----|----|----|------|----|----|----|
| RESERVED |    |    |    | PRI3 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |
| 23       | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| RESERVED |    |    |    | PRI2 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |
| 15       | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| RESERVED |    |    |    | PRI1 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |
| 7        | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| RESERVED |    |    |    | PRI0 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |

**Table 5-334. CPSW\_NC\_CPPI\_P0\_TH\_D\_THRESH\_SET\_L\_REG Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                         |
|-------|----------|------|-------|---------------------------------------------------------------------|
| 31:29 | RESERVED | NONE | 0h    | Reserved                                                            |
| 28:24 | PRI3     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 3 |
| 23:21 | RESERVED | NONE | 0h    | Reserved                                                            |
| 20:16 | PRI2     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 2 |
| 15:13 | RESERVED | NONE | 0h    | Reserved                                                            |
| 12:8  | PRI1     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 1 |
| 7:5   | RESERVED | NONE | 0h    | Reserved                                                            |
| 4:0   | PRI0     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 0 |

### 5.1.2.112 CPSW\_NC\_CPPI\_P0\_TH\_D\_THRESH\_SET\_H\_REG Register

#### 1 CPSW\_NC\_CPPI\_P0\_TH\_D\_THRESH\_SET\_H\_REG Register (Offset = 21184h) [reset = 1F1F1F1Fh]

CPPI Port 0 Tx PFC Destination Threshold Set High

Return to [Summary Table](#)

**Table 5-335. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 1184h       |

**Figure 5-112. CPSW\_NC\_CPPI\_P0\_TH\_D\_THRESH\_SET\_H\_REG Name Register**

| 31       | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
|----------|----|----|----|------|----|----|----|
| RESERVED |    |    |    | PRI7 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |
| 23       | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| RESERVED |    |    |    | PRI6 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |
| 15       | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| RESERVED |    |    |    | PRI5 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |
| 7        | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| RESERVED |    |    |    | PRI4 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |

**Table 5-337. CPSW\_NC\_CPPI\_P0\_TH\_D\_THRESH\_SET\_H\_REG Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                         |
|-------|----------|------|-------|---------------------------------------------------------------------|
| 31:29 | RESERVED | NONE | 0h    | Reserved                                                            |
| 28:24 | PRI7     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 7 |
| 23:21 | RESERVED | NONE | 0h    | Reserved                                                            |
| 20:16 | PRI6     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 6 |
| 15:13 | RESERVED | NONE | 0h    | Reserved                                                            |
| 12:8  | PRI5     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 5 |
| 7:5   | RESERVED | NONE | 0h    | Reserved                                                            |
| 4:0   | PRI4     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 4 |



### 5.1.2.113 CPSW\_NC\_CPPI\_P0\_TH\_D\_THRESH\_CLR\_L\_REG Register

#### 1 CPSW\_NC\_CPPI\_P0\_TH\_D\_THRESH\_CLR\_L\_REG Register (Offset = 21188h) [reset = 0h]

CPPI Port 0 Tx PFC Destination Threshold Clr Low

Return to [Summary Table](#)

**Table 5-338. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 1188h       |

**Figure 5-113. CPSW\_NC\_CPPI\_P0\_TH\_D\_THRESH\_CLR\_L\_REG Name Register**

| 31       | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
|----------|----|----|----|------|----|----|----|
| RESERVED |    |    |    | PRI3 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 23       | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| RESERVED |    |    |    | PRI2 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 15       | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| RESERVED |    |    |    | PRI1 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 7        | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| RESERVED |    |    |    | PRI0 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |

**Table 5-340. CPSW\_NC\_CPPI\_P0\_TH\_D\_THRESH\_CLR\_L\_REG Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                           |
|-------|----------|------|-------|-----------------------------------------------------------------------|
| 31:29 | RESERVED | NONE | 0h    | Reserved                                                              |
| 28:24 | PRI3     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 3 |
| 23:21 | RESERVED | NONE | 0h    | Reserved                                                              |
| 20:16 | PRI2     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 2 |
| 15:13 | RESERVED | NONE | 0h    | Reserved                                                              |
| 12:8  | PRI1     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 1 |
| 7:5   | RESERVED | NONE | 0h    | Reserved                                                              |
| 4:0   | PRI0     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 0 |

### 5.1.2.114 CPSW\_NC\_CPPI\_P0\_TH\_D\_THRESH\_CLR\_H\_REG Register

#### 1 CPSW\_NC\_CPPI\_P0\_TH\_D\_THRESH\_CLR\_H\_REG Register (Offset = 2118Ch) [reset = 0h]

CPPI Port 0 Tx PFC Destination Threshold Clr High

Return to [Summary Table](#)

**Table 5-341. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 118Ch       |

**Figure 5-114. CPSW\_NC\_CPPI\_P0\_TH\_D\_THRESH\_CLR\_H\_REG Name Register**

| 31       | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
|----------|----|----|----|------|----|----|----|
| RESERVED |    |    |    | PRI7 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 23       | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| RESERVED |    |    |    | PRI6 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 15       | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| RESERVED |    |    |    | PRI5 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 7        | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| RESERVED |    |    |    | PRI4 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |

**Table 5-343. CPSW\_NC\_CPPI\_P0\_TH\_D\_THRESH\_CLR\_H\_REG Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                           |
|-------|----------|------|-------|-----------------------------------------------------------------------|
| 31:29 | RESERVED | NONE | 0h    | Reserved                                                              |
| 28:24 | PRI7     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 7 |
| 23:21 | RESERVED | NONE | 0h    | Reserved                                                              |
| 20:16 | PRI6     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 6 |
| 15:13 | RESERVED | NONE | 0h    | Reserved                                                              |
| 12:8  | PRI5     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 5 |
| 7:5   | RESERVED | NONE | 0h    | Reserved                                                              |
| 4:0   | PRI4     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 4 |

### 5.1.2.115 CPSW\_NC\_CPPI\_P0\_TH\_G\_BUF\_THRESH\_SET\_L\_REG Register

#### 1 CPSW\_NC\_CPPI\_P0\_TH\_G\_BUF\_THRESH\_SET\_L\_REG Register (Offset = 21190h) [reset = 1F1F1F1Fh]

CPPI Port 0 Tx PFC Global Buffer Threshold Set Low

Return to [Summary Table](#)

**Table 5-344. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 1190h       |

**Figure 5-115. CPSW\_NC\_CPPI\_P0\_TH\_G\_BUF\_THRESH\_SET\_L\_REG Name Register**

|          |    |    |    |      |    |    |    |
|----------|----|----|----|------|----|----|----|
| 31       | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
| RESERVED |    |    |    | PRI3 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |
| 23       | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| RESERVED |    |    |    | PRI2 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |
| 15       | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| RESERVED |    |    |    | PRI1 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |
| 7        | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| RESERVED |    |    |    | PRI0 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |

**Table 5-346. CPSW\_NC\_CPPI\_P0\_TH\_G\_BUF\_THRESH\_SET\_L\_REG Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                         |
|-------|----------|------|-------|---------------------------------------------------------------------|
| 31:29 | RESERVED | NONE | 0h    | Reserved                                                            |
| 28:24 | PRI3     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 3 |
| 23:21 | RESERVED | NONE | 0h    | Reserved                                                            |
| 20:16 | PRI2     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 2 |
| 15:13 | RESERVED | NONE | 0h    | Reserved                                                            |
| 12:8  | PRI1     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 1 |
| 7:5   | RESERVED | NONE | 0h    | Reserved                                                            |
| 4:0   | PRI0     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 0 |

### 5.1.2.116 CPSW\_NC\_CPPI\_P0\_TH\_G\_BUF\_THRESH\_SET\_H\_REG Register

#### 1 CPSW\_NC\_CPPI\_P0\_TH\_G\_BUF\_THRESH\_SET\_H\_REG Register (Offset = 21194h) [reset = 1F1F1F1Fh]

CPPI Port 0 Tx PFC Global Buffer Threshold Set High

Return to [Summary Table](#)

**Table 5-347. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 1194h       |

**Figure 5-116. CPSW\_NC\_CPPI\_P0\_TH\_G\_BUF\_THRESH\_SET\_H\_REG Name Register**

|          |    |    |    |      |    |    |    |
|----------|----|----|----|------|----|----|----|
| 31       | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
| RESERVED |    |    |    | PRI7 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |
| 23       | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| RESERVED |    |    |    | PRI6 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |
| 15       | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| RESERVED |    |    |    | PRI5 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |
| 7        | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| RESERVED |    |    |    | PRI4 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |

**Table 5-349. CPSW\_NC\_CPPI\_P0\_TH\_G\_BUF\_THRESH\_SET\_H\_REG Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                         |
|-------|----------|------|-------|---------------------------------------------------------------------|
| 31:29 | RESERVED | NONE | 0h    | Reserved                                                            |
| 28:24 | PRI7     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 7 |
| 23:21 | RESERVED | NONE | 0h    | Reserved                                                            |
| 20:16 | PRI6     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 6 |
| 15:13 | RESERVED | NONE | 0h    | Reserved                                                            |
| 12:8  | PRI5     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 5 |
| 7:5   | RESERVED | NONE | 0h    | Reserved                                                            |
| 4:0   | PRI4     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 4 |

### 5.1.2.117 CPSW\_NC\_CPPI\_P0\_TH\_G\_BUF\_THRESH\_CLR\_L\_REG Register

#### 1 CPSW\_NC\_CPPI\_P0\_TH\_G\_BUF\_THRESH\_CLR\_L\_REG Register (Offset = 21198h) [reset = 0h]

CPPI Port 0 Tx PFC Global Buffer Threshold Clr Low

Return to [Summary Table](#)

**Table 5-350. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 1198h       |

**Figure 5-117. CPSW\_NC\_CPPI\_P0\_TH\_G\_BUF\_THRESH\_CLR\_L\_REG Name Register**

| 31       | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
|----------|----|----|----|------|----|----|----|
| RESERVED |    |    |    | PRI3 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 23       | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| RESERVED |    |    |    | PRI2 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 15       | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| RESERVED |    |    |    | PRI1 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 7        | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| RESERVED |    |    |    | PRI0 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |

**Table 5-352. CPSW\_NC\_CPPI\_P0\_TH\_G\_BUF\_THRESH\_CLR\_L\_REG Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                           |
|-------|----------|------|-------|-----------------------------------------------------------------------|
| 31:29 | RESERVED | NONE | 0h    | Reserved                                                              |
| 28:24 | PRI3     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 3 |
| 23:21 | RESERVED | NONE | 0h    | Reserved                                                              |
| 20:16 | PRI2     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 2 |
| 15:13 | RESERVED | NONE | 0h    | Reserved                                                              |
| 12:8  | PRI1     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 1 |
| 7:5   | RESERVED | NONE | 0h    | Reserved                                                              |
| 4:0   | PRI0     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 0 |

### 5.1.2.118 CPSW\_NC\_CPPI\_P0\_TH\_G\_BUF\_THRESH\_CLR\_H\_REG Register

#### 1 CPSW\_NC\_CPPI\_P0\_TH\_G\_BUF\_THRESH\_CLR\_H\_REG Register (Offset = 2119Ch) [reset = 0h]

CPPI Port 0 Tx PFC Global Buffer Threshold Clr High

Return to [Summary Table](#)

**Table 5-353. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 119Ch       |

**Figure 5-118. CPSW\_NC\_CPPI\_P0\_TH\_G\_BUF\_THRESH\_CLR\_H\_REG Name Register**

|          |    |    |    |      |    |    |    |
|----------|----|----|----|------|----|----|----|
| 31       | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
| RESERVED |    |    |    | PRI7 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 23       | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| RESERVED |    |    |    | PRI6 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 15       | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| RESERVED |    |    |    | PRI5 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 7        | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| RESERVED |    |    |    | PRI4 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |

**Table 5-355. CPSW\_NC\_CPPI\_P0\_TH\_G\_BUF\_THRESH\_CLR\_H\_REG Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                           |
|-------|----------|------|-------|-----------------------------------------------------------------------|
| 31:29 | RESERVED | NONE | 0h    | Reserved                                                              |
| 28:24 | PRI7     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 7 |
| 23:21 | RESERVED | NONE | 0h    | Reserved                                                              |
| 20:16 | PRI6     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 6 |
| 15:13 | RESERVED | NONE | 0h    | Reserved                                                              |
| 12:8  | PRI5     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 5 |
| 7:5   | RESERVED | NONE | 0h    | Reserved                                                              |
| 4:0   | PRI4     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 4 |

### 5.1.2.119 CPSW\_NC\_CPPI\_P0\_SRC\_ID\_A\_REG Register

#### 1 CPSW\_NC\_CPPI\_P0\_SRC\_ID\_A\_REG Register (Offset = 21300h) [reset = 4030201h]

CPPI Port 0 CPPI Source ID A

Return to [Summary Table](#)

**Table 5-356. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 1300h       |

**Figure 5-119. CPSW\_NC\_CPPI\_P0\_SRC\_ID\_A\_REG Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PORT4 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 4h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PORT3 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 3h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PORT2 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 2h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PORT1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 1h    |    |    |    |    |    |    |    |

**Table 5-358. CPSW\_NC\_CPPI\_P0\_SRC\_ID\_A\_REG Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                            |
|-------|-------|------|-------|----------------------------------------|
| 31:24 | PORT4 | R/W  | 4h    | Port 4 CPPI Info Word0 Source ID Value |
| 23:16 | PORT3 | R/W  | 3h    | Port 3 CPPI Info Word0 Source ID Value |
| 15:8  | PORT2 | R/W  | 2h    | Port 2 CPPI Info Word0 Source ID Value |
| 7:0   | PORT1 | R/W  | 1h    | Port 1 CPPI Info Word0 Source ID Value |

### 5.1.2.120 CPSW\_NC\_CPPI\_P0\_SRC\_ID\_B\_REG Register

#### 1 CPSW\_NC\_CPPI\_P0\_SRC\_ID\_B\_REG Register (Offset = 21304h) [reset = 8070605h]

CPPI Port 0 CPPI Source ID B

Return to [Summary Table](#)

**Table 5-359. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 1304h       |

**Figure 5-120. CPSW\_NC\_CPPI\_P0\_SRC\_ID\_B\_REG Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PORT8 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 8h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PORT7 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 7h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PORT6 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 6h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PORT5 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 5h    |    |    |    |    |    |    |    |

**Table 5-361. CPSW\_NC\_CPPI\_P0\_SRC\_ID\_B\_REG Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                            |
|-------|-------|------|-------|----------------------------------------|
| 31:24 | PORT8 | R/W  | 8h    | Port 8 CPPI Info Word0 Source ID Value |
| 23:16 | PORT7 | R/W  | 7h    | Port 7 CPPI Info Word0 Source ID Value |
| 15:8  | PORT6 | R/W  | 6h    | Port 6 CPPI Info Word0 Source ID Value |
| 7:0   | PORT5 | R/W  | 5h    | Port 5 CPPI Info Word0 Source ID Value |



### 5.1.2.121 CPSW\_NC\_CPPI\_P0\_HOST\_BLKs\_PRI\_REG Register

#### 1 CPSW\_NC\_CPPI\_P0\_HOST\_BLKs\_PRI\_REG Register (Offset = 21320h) [reset = 0h]

CPPI Port 0 Host Blocks Priority

Return to [Summary Table](#)

**Table 5-362. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5282 1320h       |

**Figure 5-121. CPSW\_NC\_CPPI\_P0\_HOST\_BLKs\_PRI\_REG Name Register**

| 31 | 30 | 29   | 28 | 27 | 26 | 25   | 24 |
|----|----|------|----|----|----|------|----|
|    |    | PRI7 |    |    |    | PRI6 |    |
|    |    | R/W  |    |    |    | R/W  |    |
|    |    | 0h   |    |    |    | 0h   |    |
| 23 | 22 | 21   | 20 | 19 | 18 | 17   | 16 |
|    |    | PRI5 |    |    |    | PRI4 |    |
|    |    | R/W  |    |    |    | R/W  |    |
|    |    | 0h   |    |    |    | 0h   |    |
| 15 | 14 | 13   | 12 | 11 | 10 | 9    | 8  |
|    |    | PRI3 |    |    |    | PRI2 |    |
|    |    | R/W  |    |    |    | R/W  |    |
|    |    | 0h   |    |    |    | 0h   |    |
| 7  | 6  | 5    | 4  | 3  | 2  | 1    | 0  |
|    |    | PRI1 |    |    |    | PRI0 |    |
|    |    | R/W  |    |    |    | R/W  |    |
|    |    | 0h   |    |    |    | 0h   |    |

**Table 5-364. CPSW\_NC\_CPPI\_P0\_HOST\_BLKs\_PRI\_REG Register Field Descriptions**

| Bit   | Field | Type | Reset | Description            |
|-------|-------|------|-------|------------------------|
| 31:28 | PRI7  | R/W  | 0h    | Priority 7 Host Blocks |
| 27:24 | PRI6  | R/W  | 0h    | Priority 6 Host Blocks |
| 23:20 | PRI5  | R/W  | 0h    | Priority 5 Host Blocks |
| 19:16 | PRI4  | R/W  | 0h    | Priority 4 Host Blocks |
| 15:12 | PRI3  | R/W  | 0h    | Priority 3 Host Blocks |
| 11:8  | PRI2  | R/W  | 0h    | Priority 2 Host Blocks |
| 7:4   | PRI1  | R/W  | 0h    | Priority 1 Host Blocks |
| 3:0   | PRI0  | R/W  | 0h    | Priority 0 Host Blocks |

### 5.1.2.122 CPSW\_NC\_ETH\_MAC\_PN\_CONTROL\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_CONTROL\_REG\_K Register (Offset = 22004h) [reset = 0h]

Enet Port N Control

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-365. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2004h + formula |

**Figure 5-122. CPSW\_NC\_ETH\_MAC\_PN\_CONTROL\_REG\_K Name Register**

|               |               |          |                   |          |              |              |          |
|---------------|---------------|----------|-------------------|----------|--------------|--------------|----------|
| 31            | 30            | 29       | 28                | 27       | 26           | 25           | 24       |
| RESERVED      |               |          |                   |          |              |              |          |
| NONE          |               |          |                   |          |              |              |          |
| 0h            |               |          |                   |          |              |              |          |
| 23            | 22            | 21       | 20                | 19       | 18           | 17           | 16       |
| RESERVED      |               |          |                   |          |              | EST_PORT_EN  | RESERVED |
| NONE          |               |          |                   |          |              | R/W          | NONE     |
| 0h            |               |          |                   |          |              | 0h           | 0h       |
| 15            | 14            | 13       | 12                | 11       | 10           | 9            | 8        |
| RX_ECC_ERR_EN | TX_ECC_ERR_EN | RESERVED | TX_LPI_CLKSTOP_EN | RESERVED |              |              |          |
| R/W           | R/W           | NONE     | R/W               | NONE     |              |              |          |
| 0h            | 0h            | 0h       | 0h                | 0h       |              |              |          |
| 7             | 6             | 5        | 4                 | 3        | 2            | 1            | 0        |
| RESERVED      |               |          |                   |          | DSCP_IPV6_EN | DSCP_IPV4_EN | RESERVED |
| NONE          |               |          |                   |          | R/W          | R/W          | NONE     |
| 0h            |               |          |                   |          | 0h           | 0h           | 0h       |

**Table 5-367. CPSW\_NC\_ETH\_MAC\_PN\_CONTROL\_REG\_K Register Field Descriptions**

| Bit   | Field             | Type | Reset | Description                                                                                                                                                                 |
|-------|-------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED          | NONE | 0h    | Reserved                                                                                                                                                                    |
| 17    | EST_PORT_EN       | R/W  | 0h    | EST Port Enable<br>0 - EST is disabled on the port.<br>1 - EST is enabled on the port (Does not take effect until the CPSW level est_en is set).                            |
| 16    | RESERVED          | NONE | 0h    | Reserved                                                                                                                                                                    |
| 15    | RX_ECC_ERR_EN     | R/W  | 0h    | This bit must be set to enable receive ECC error operations on the port.                                                                                                    |
| 14    | TX_ECC_ERR_EN     | R/W  | 0h    | This bit must be set to enable transmit ECC error operations on the port.                                                                                                   |
| 13    | RESERVED          | NONE | 0h    | Reserved                                                                                                                                                                    |
| 12    | TX_LPI_CLKSTOP_EN | R/W  | 0h    | Transmit LPI Clock Stop Enable - When set this bit causes the transmit output clock (GMII_GMTCLK_O) to be stopped when the transmit LPI state is entered if EEE is enabled. |
| 11:3  | RESERVED          | NONE | 0h    | Reserved                                                                                                                                                                    |
| 2     | DSCP_IPV6_EN      | R/W  | 0h    | IPv6 DSCP enable<br>0 - Ipv6 DSCP priority mapping is disabled.<br>1 - Ipv6 DSCP priority mapping is enabled.                                                               |

**Table 5-367. CPSW\_NC\_ETH\_MAC\_PN\_CONTROL\_REG\_K Register Field Descriptions (continued)**

| Bit | Field        | Type | Reset | Description                                                                                                   |
|-----|--------------|------|-------|---------------------------------------------------------------------------------------------------------------|
| 1   | DSCP_IPV4_EN | R/W  | 0h    | IPv4 DSCP enable<br>0 - Ipv4 DSCP priority mapping is disabled.<br>1 - Ipv4 DSCP priority mapping is enabled. |
| 0   | RESERVED     | NONE | 0h    | Reserved                                                                                                      |

### 5.1.2.123 CPSW\_NC\_ETH\_MAC\_PN\_MAX\_BLKs\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_MAX\_BLKs\_REG\_K Register (Offset = 22008h) [reset = 1004h]

Enet Port N FIFO Max Blocks

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-368. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2008h + formula |

**Figure 5-123. CPSW\_NC\_ETH\_MAC\_PN\_MAX\_BLKs\_REG\_K Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED    |    |    |    |    |    |    |    |
| NONE        |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TX_MAX_BLKs |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 10h         |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RX_MAX_BLKs |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 4h          |    |    |    |    |    |    |    |

**Table 5-370. CPSW\_NC\_ETH\_MAC\_PN\_MAX\_BLKs\_REG\_K Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                   |
|-------|-------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED    | NONE | 0h    | Reserved                                                                                                                                                                                                                                      |
| 15:8  | TX_MAX_BLKs | R/W  | 10h   | Transmit Max Blocks - The maximum number of blocks allowed on all transmit FIFO priorities combined. If (fifo_oneram = 1) then blocks should be moved from transmit to receive when flow control is enabled to allow for flow control runoff. |
| 7:0   | RX_MAX_BLKs | R/W  | 4h    | Receive Max Blocks - The maximum number of blocks allowed on the express and preempt receive FIFOs (transmit and receive FIFOs combined when fifo_oneram = 1)                                                                                 |

### 5.1.2.124 CPSW\_NC\_ETH\_MAC\_PN\_BLK\_CNT\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_BLK\_CNT\_REG\_K Register (Offset = 22010h) [reset = 1h]

Enet Port N FIFO Block Usage Count

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-371. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2010h + formula |

**Figure 5-124. CPSW\_NC\_ETH\_MAC\_PN\_BLK\_CNT\_REG\_K Name Register**

|          |    |              |            |    |    |    |    |
|----------|----|--------------|------------|----|----|----|----|
| 31       | 30 | 29           | 28         | 27 | 26 | 25 | 24 |
| RESERVED |    |              |            |    |    |    |    |
| NONE     |    |              |            |    |    |    |    |
| 0h       |    |              |            |    |    |    |    |
| 23       | 22 | 21           | 20         | 19 | 18 | 17 | 16 |
| RESERVED |    | RX_BLK_CNT_P |            |    |    |    |    |
| NONE     |    | R            |            |    |    |    |    |
| 0h       |    | 0h           |            |    |    |    |    |
| 15       | 14 | 13           | 12         | 11 | 10 | 9  | 8  |
| RESERVED |    |              | TX_BLK_CNT |    |    |    |    |
| NONE     |    |              | R          |    |    |    |    |
| 0h       |    |              | 0h         |    |    |    |    |
| 7        | 6  | 5            | 4          | 3  | 2  | 1  | 0  |
| RESERVED |    | RX_BLK_CNT_E |            |    |    |    |    |
| NONE     |    | R            |            |    |    |    |    |
| 0h       |    | 1h           |            |    |    |    |    |

**Table 5-373. CPSW\_NC\_ETH\_MAC\_PN\_BLK\_CNT\_REG\_K Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                                                                                                            |
|-------|--------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:22 | RESERVED     | NONE | 0h    | Reserved                                                                                                                                                                                               |
| 21:16 | RX_BLK_CNT_P | R    | 0h    | Receive Express Block Count Usage - This value is the number of blocks allocated to the port FIFO preempt receive queue. No blocks are allocated until the iet_en in the CPSW_Control register is set. |
| 15:13 | RESERVED     | NONE | 0h    | Reserved                                                                                                                                                                                               |
| 12:8  | TX_BLK_CNT   | R    | 0h    | Transmit Block Count Usage - This value is the number of blocks allocated to the port FIFO logical transmit queues.                                                                                    |
| 7:6   | RESERVED     | NONE | 0h    | Reserved                                                                                                                                                                                               |
| 5:0   | RX_BLK_CNT_E | R    | 1h    | Receive Express Block Count Usage - This value is the number of blocks allocated to the ports FIFO express receive queue.                                                                              |

### 5.1.2.125 CPSW\_NC\_ETH\_MAC\_PN\_PORT\_VLAN\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_PORT\_VLAN\_REG\_K Register (Offset = 22014h) [reset = 0h]

Enet Port N VLAN

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-374. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2014h + formula |

**Figure 5-125. CPSW\_NC\_ETH\_MAC\_PN\_PORT\_VLAN\_REG\_K Name Register**

|          |    |    |          |          |    |    |    |
|----------|----|----|----------|----------|----|----|----|
| 31       | 30 | 29 | 28       | 27       | 26 | 25 | 24 |
| RESERVED |    |    |          |          |    |    |    |
| NONE     |    |    |          |          |    |    |    |
| 0h       |    |    |          |          |    |    |    |
| 23       | 22 | 21 | 20       | 19       | 18 | 17 | 16 |
| RESERVED |    |    |          |          |    |    |    |
| NONE     |    |    |          |          |    |    |    |
| 0h       |    |    |          |          |    |    |    |
| 15       | 14 | 13 | 12       | 11       | 10 | 9  | 8  |
| PORT_PRI |    |    | PORT_CFI | PORT_VID |    |    |    |
| R/W      |    |    | R/W      | R/W      |    |    |    |
| 0h       |    |    | 0h       | 0h       |    |    |    |
| 7        | 6  | 5  | 4        | 3        | 2  | 1  | 0  |
| PORT_VID |    |    |          |          |    |    |    |
| R/W      |    |    |          |          |    |    |    |
| 0h       |    |    |          |          |    |    |    |

**Table 5-376. CPSW\_NC\_ETH\_MAC\_PN\_PORT\_VLAN\_REG\_K Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description        |
|-------|----------|------|-------|--------------------|
| 31:16 | RESERVED | NONE | 0h    | Reserved           |
| 15:13 | PORT_PRI | R/W  | 0h    | Port VLAN Priority |
| 12    | PORT_CFI | R/W  | 0h    | Port CFI bit       |
| 11:0  | PORT_VID | R/W  | 0h    | Port VLAN ID       |

### 5.1.2.126 CPSW\_NC\_ETH\_MAC\_PN\_TX\_PRI\_MAP\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_TX\_PRI\_MAP\_REG\_K Register (Offset = 22018h) [reset = 76543210h]

Enet Port N Tx Header Pri to Switch Pri Mapping

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-377. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2018h + formula |

**Figure 5-126. CPSW\_NC\_ETH\_MAC\_PN\_TX\_PRI\_MAP\_REG\_K Name Register**

| 31       | 30 | 29   | 28 | 27       | 26 | 25   | 24 |
|----------|----|------|----|----------|----|------|----|
| RESERVED |    | PRI7 |    | RESERVED |    | PRI6 |    |
| NONE     |    | R/W  |    | NONE     |    | R/W  |    |
| 0h       |    | 7h   |    | 0h       |    | 6h   |    |
| 23       | 22 | 21   | 20 | 19       | 18 | 17   | 16 |
| RESERVED |    | PRI5 |    | RESERVED |    | PRI4 |    |
| NONE     |    | R/W  |    | NONE     |    | R/W  |    |
| 0h       |    | 5h   |    | 0h       |    | 4h   |    |
| 15       | 14 | 13   | 12 | 11       | 10 | 9    | 8  |
| RESERVED |    | PRI3 |    | RESERVED |    | PRI2 |    |
| NONE     |    | R/W  |    | NONE     |    | R/W  |    |
| 0h       |    | 3h   |    | 0h       |    | 2h   |    |
| 7        | 6  | 5    | 4  | 3        | 2  | 1    | 0  |
| RESERVED |    | PRI1 |    | RESERVED |    | PRI0 |    |
| NONE     |    | R/W  |    | NONE     |    | R/W  |    |
| 0h       |    | 1h   |    | 0h       |    | 0h   |    |

**Table 5-379. CPSW\_NC\_ETH\_MAC\_PN\_TX\_PRI\_MAP\_REG\_K Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                       |
|-------|----------|------|-------|-----------------------------------------------------------------------------------|
| 31    | RESERVED | NONE | 0h    | Reserved                                                                          |
| 30:28 | PRI7     | R/W  | 7h    | Priority 7 - A packet header priority of 0x7 is given this switch queue priority. |
| 27    | RESERVED | NONE | 0h    | Reserved                                                                          |
| 26:24 | PRI6     | R/W  | 6h    | Priority 6 - A packet header priority of 0x6 is given this switch queue priority. |
| 23    | RESERVED | NONE | 0h    | Reserved                                                                          |
| 22:20 | PRI5     | R/W  | 5h    | Priority 5 - A packet header priority of 0x5 is given this switch queue priority. |
| 19    | RESERVED | NONE | 0h    | Reserved                                                                          |
| 18:16 | PRI4     | R/W  | 4h    | Priority 4 - A packet header priority of 0x4 is given this switch queue priority. |
| 15    | RESERVED | NONE | 0h    | Reserved                                                                          |
| 14:12 | PRI3     | R/W  | 3h    | Priority 3 - A packet header priority of 0x3 is given this switch queue priority. |
| 11    | RESERVED | NONE | 0h    | Reserved                                                                          |
| 10:8  | PRI2     | R/W  | 2h    | Priority 2 - A packet header priority of 0x2 is given this switch queue priority. |
| 7     | RESERVED | NONE | 0h    | Reserved                                                                          |

**Table 5-379. CPSW\_NC\_ETH\_MAC\_PN\_TX\_PRI\_MAP\_REG\_K Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                                                                       |
|-----|----------|------|-------|-----------------------------------------------------------------------------------|
| 6:4 | PRI1     | R/W  | 1h    | Priority 1 - A packet header priority of 0x1 is given this switch queue priority. |
| 3   | RESERVED | NONE | 0h    | Reserved                                                                          |
| 2:0 | PRI0     | R/W  | 0h    | Priority 0 - A packet header priority of 0x0 is given this switch queue priority. |



### 5.1.2.127 CPSW\_NC\_ETH\_MAC\_PN\_PRI\_CTL\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_PRI\_CTL\_REG\_K Register (Offset = 2201Ch) [reset = 9000h]

Enet Port N Priority Control

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-380. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 201Ch + formula |

**Figure 5-127. CPSW\_NC\_ETH\_MAC\_PN\_PRI\_CTL\_REG\_K Name Register**

|                  |    |    |    |          |    |    |    |
|------------------|----|----|----|----------|----|----|----|
| 31               | 30 | 29 | 28 | 27       | 26 | 25 | 24 |
| TX_FLOW_PRI      |    |    |    |          |    |    |    |
| R/W              |    |    |    |          |    |    |    |
| 0h               |    |    |    |          |    |    |    |
| 23               | 22 | 21 | 20 | 19       | 18 | 17 | 16 |
| RX_FLOW_PRI      |    |    |    |          |    |    |    |
| R/W              |    |    |    |          |    |    |    |
| 0h               |    |    |    |          |    |    |    |
| 15               | 14 | 13 | 12 | 11       | 10 | 9  | 8  |
| TX_HOST_BLKs_REM |    |    |    | RESERVED |    |    |    |
| R/W              |    |    |    | NONE     |    |    |    |
| 9h               |    |    |    | 0h       |    |    |    |
| 7                | 6  | 5  | 4  | 3        | 2  | 1  | 0  |
| RESERVED         |    |    |    |          |    |    |    |
| NONE             |    |    |    |          |    |    |    |
| 0h               |    |    |    |          |    |    |    |

**Table 5-382. CPSW\_NC\_ETH\_MAC\_PN\_PRI\_CTL\_REG\_K Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                            |
|-------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------|
| 31:24 | TX_FLOW_PRI      | R/W  | 0h    | Transmit Priority Based Flow Control Enable (per priority)                                                             |
| 23:16 | RX_FLOW_PRI      | R/W  | 0h    | Receive Priority Based Flow Control Enable (per priority)                                                              |
| 15:12 | TX_HOST_BLKs_REM | R/W  | 9h    | Transmit FIFO Blocks that must be free before a non rate-limited CPPI Port 0 receive thread can begin sending a packet |
| 11:0  | RESERVED         | NONE | 0h    | Reserved                                                                                                               |

### 5.1.2.128 CPSW\_NC\_ETH\_MAC\_PN\_RX\_PRI\_MAP\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_RX\_PRI\_MAP\_REG\_K Register (Offset = 22020h) [reset = 76543210h]

Enet Port N RX Pkt Pri to Header Pri Map

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-383. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2020h + formula |

**Figure 5-128. CPSW\_NC\_ETH\_MAC\_PN\_RX\_PRI\_MAP\_REG\_K Name Register**

| 31       | 30 | 29   | 28 | 27       | 26 | 25   | 24 |
|----------|----|------|----|----------|----|------|----|
| RESERVED |    | PRI7 |    | RESERVED |    | PRI6 |    |
| NONE     |    | R/W  |    | NONE     |    | R/W  |    |
| 0h       |    | 7h   |    | 0h       |    | 6h   |    |
| 23       | 22 | 21   | 20 | 19       | 18 | 17   | 16 |
| RESERVED |    | PRI5 |    | RESERVED |    | PRI4 |    |
| NONE     |    | R/W  |    | NONE     |    | R/W  |    |
| 0h       |    | 5h   |    | 0h       |    | 4h   |    |
| 15       | 14 | 13   | 12 | 11       | 10 | 9    | 8  |
| RESERVED |    | PRI3 |    | RESERVED |    | PRI2 |    |
| NONE     |    | R/W  |    | NONE     |    | R/W  |    |
| 0h       |    | 3h   |    | 0h       |    | 2h   |    |
| 7        | 6  | 5    | 4  | 3        | 2  | 1    | 0  |
| RESERVED |    | PRI1 |    | RESERVED |    | PRI0 |    |
| NONE     |    | R/W  |    | NONE     |    | R/W  |    |
| 0h       |    | 1h   |    | 0h       |    | 0h   |    |

**Table 5-385. CPSW\_NC\_ETH\_MAC\_PN\_RX\_PRI\_MAP\_REG\_K Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                             |
|-------|----------|------|-------|-----------------------------------------------------------------------------------------|
| 31    | RESERVED | NONE | 0h    | Reserved                                                                                |
| 30:28 | PRI7     | R/W  | 7h    | Priority 7 - A packet priority of 7 is mapped (changed) to this header packet priority. |
| 27    | RESERVED | NONE | 0h    | Reserved                                                                                |
| 26:24 | PRI6     | R/W  | 6h    | Priority 6 - A packet priority of 6 is mapped (changed) to this header packet priority. |
| 23    | RESERVED | NONE | 0h    | Reserved                                                                                |
| 22:20 | PRI5     | R/W  | 5h    | Priority 5 - A packet priority of 5 is mapped (changed) to this header packet priority. |
| 19    | RESERVED | NONE | 0h    | Reserved                                                                                |
| 18:16 | PRI4     | R/W  | 4h    | Priority 4 - A packet priority of 4 is mapped (changed) to this header packet priority. |
| 15    | RESERVED | NONE | 0h    | Reserved                                                                                |
| 14:12 | PRI3     | R/W  | 3h    | Priority 3 - A packet priority of 3 is mapped (changed) to this header packet priority. |
| 11    | RESERVED | NONE | 0h    | Reserved                                                                                |
| 10:8  | PRI2     | R/W  | 2h    | Priority 2 - A packet priority of 2 is mapped (changed) to this header packet priority. |
| 7     | RESERVED | NONE | 0h    | Reserved                                                                                |

**Table 5-385. CPSW\_NC\_ETH\_MAC\_PN\_RX\_PRI\_MAP\_REG\_K Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                                                                             |
|-----|----------|------|-------|-----------------------------------------------------------------------------------------|
| 6:4 | PRI1     | R/W  | 1h    | Priority 1 - A packet priority of 1 is mapped (changed) to this header packet priority. |
| 3   | RESERVED | NONE | 0h    | Reserved                                                                                |
| 2:0 | PRI0     | R/W  | 0h    | Priority 0 - A packet priority of 0 is mapped (changed) to this header packet priority. |

### 5.1.2.129 CPSW\_NC\_ETH\_MAC\_PN\_RX\_MAXLEN\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_RX\_MAXLEN\_REG\_K Register (Offset = 22024h) [reset = 5EEh]

Enet Port N Receive Frame Max Length

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-386. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2024h + formula |

**Figure 5-129. CPSW\_NC\_ETH\_MAC\_PN\_RX\_MAXLEN\_REG\_K Name Register**

|           |    |           |    |    |    |    |    |
|-----------|----|-----------|----|----|----|----|----|
| 31        | 30 | 29        | 28 | 27 | 26 | 25 | 24 |
| RESERVED  |    |           |    |    |    |    |    |
| NONE      |    |           |    |    |    |    |    |
| 0h        |    |           |    |    |    |    |    |
| 23        | 22 | 21        | 20 | 19 | 18 | 17 | 16 |
| RESERVED  |    |           |    |    |    |    |    |
| NONE      |    |           |    |    |    |    |    |
| 0h        |    |           |    |    |    |    |    |
| 15        | 14 | 13        | 12 | 11 | 10 | 9  | 8  |
| RESERVED  |    | RX_MAXLEN |    |    |    |    |    |
| NONE      |    | R/W       |    |    |    |    |    |
| 0h        |    | 5EEh      |    |    |    |    |    |
| 7         | 6  | 5         | 4  | 3  | 2  | 1  | 0  |
| RX_MAXLEN |    |           |    |    |    |    |    |
| R/W       |    |           |    |    |    |    |    |
| 5EEh      |    |           |    |    |    |    |    |

**Table 5-388. CPSW\_NC\_ETH\_MAC\_PN\_RX\_MAXLEN\_REG\_K Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                              |
|-------|-----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:14 | RESERVED  | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                 |
| 13:0  | RX_MAXLEN | R/W  | 5EEh  | RX Maximum Frame Length - This field determines the maximum length of a received frame. The reset value is 1518 (dec). Frames with byte counts greater than pn_rx_maxlen are long frames. Long frames with no errors are oversized frames. Long frames with CRC, code, or alignment error are jabber frames. The maximum value is 2024 (including VLAN). |

### 5.1.2.130 CPSW\_NC\_ETH\_MAC\_PN\_TX\_BLKs\_PRI\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_TX\_BLKs\_PRI\_REG\_K Register (Offset = 22028h) [reset = 1245678h]

Enet Port N Transmit Block Sub Per Priority

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-389. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2028h + formula |

**Figure 5-130. CPSW\_NC\_ETH\_MAC\_PN\_TX\_BLKs\_PRI\_REG\_K Name Register**

|      |    |    |    |      |    |    |    |
|------|----|----|----|------|----|----|----|
| 31   | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
| PRI7 |    |    |    | PRI6 |    |    |    |
| R/W  |    |    |    | R/W  |    |    |    |
| 0h   |    |    |    | 1h   |    |    |    |
| 23   | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| PRI5 |    |    |    | PRI4 |    |    |    |
| R/W  |    |    |    | R/W  |    |    |    |
| 2h   |    |    |    | 4h   |    |    |    |
| 15   | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| PRI3 |    |    |    | PRI2 |    |    |    |
| R/W  |    |    |    | R/W  |    |    |    |
| 5h   |    |    |    | 6h   |    |    |    |
| 7    | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| PRI1 |    |    |    | PRI0 |    |    |    |
| R/W  |    |    |    | R/W  |    |    |    |
| 7h   |    |    |    | 8h   |    |    |    |

**Table 5-391. CPSW\_NC\_ETH\_MAC\_PN\_TX\_BLKs\_PRI\_REG\_K Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                     |
|-------|-------|------|-------|-------------------------------------------------|
| 31:28 | PRI7  | R/W  | 0h    | Transmit Blocks Per Priority 7 (subtract value) |
| 27:24 | PRI6  | R/W  | 1h    | Transmit Blocks Per Priority 6 (subtract value) |
| 23:20 | PRI5  | R/W  | 2h    | Transmit Blocks Per Priority 5 (subtract value) |
| 19:16 | PRI4  | R/W  | 4h    | Transmit Blocks Per Priority 4 (subtract value) |
| 15:12 | PRI3  | R/W  | 5h    | Transmit Blocks Per Priority 3 (subtract value) |
| 11:8  | PRI2  | R/W  | 6h    | Transmit Blocks Per Priority 2 (subtract value) |
| 7:4   | PRI1  | R/W  | 7h    | Transmit Blocks Per Priority 1 (subtract value) |
| 3:0   | PRI0  | R/W  | 8h    | Transmit Blocks Per Priority 0 (subtract value) |

### 5.1.2.131 CPSW\_NC\_ETH\_MAC\_PN\_IDLE2LPI\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_IDLE2LPI\_REG\_K Register (Offset = 22030h) [reset = 0h]

Enet Port N EEE Idle to LPI counter

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-392. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2030h + formula |

**Figure 5-131. CPSW\_NC\_ETH\_MAC\_PN\_IDLE2LPI\_REG\_K Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-394. CPSW\_NC\_ETH\_MAC\_PN\_IDLE2LPI\_REG\_K Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                              |
|-------|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                 |
| 23:0  | COUNT    | R/W  | 0h    | EEE Idle to LPI counter load value - After CLKSTOP_REQ is asserted, this value is loaded into the port idle to LPI counter on each clock that the port transmit is not idle. The port enters the transmit LPI state when this counter decrements to zero. This counter decrements each time the EEE prescale counter decrements to zero. |

### 5.1.2.132 CPSW\_NC\_ETH\_MAC\_PN\_LPI2WAKE\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_LPI2WAKE\_REG\_K Register (Offset = 22034h) [reset = 0h]

Enet Port N EEE LPI to wake counter

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-395. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2034h + formula |

**Figure 5-132. CPSW\_NC\_ETH\_MAC\_PN\_LPI2WAKE\_REG\_K Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-397. CPSW\_NC\_ETH\_MAC\_PN\_LPI2WAKE\_REG\_K Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                               |
| 23:0  | COUNT    | R/W  | 0h    | EEE LPI to wake counter load value - When the port is in the transmit LPI state and the CLKSTOP_REQ signal is deasserted, this value is loaded into the LPI to wake counter. Transmit packet operations may begin (resume) when the LPI to wake count decrements to zero (on the pre-scale count). This is the time that the transmit must wait before transmit packet operations resume after wakeup. |

### 5.1.2.133 CPSW\_NC\_ETH\_MAC\_PN\_EEE\_STATUS\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_EEE\_STATUS\_REG\_K Register (Offset = 22038h) [reset = 62h]

Enet Port N EEE status

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-398. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2038h + formula |

**Figure 5-133. CPSW\_NC\_ETH\_MAC\_PN\_EEE\_STATUS\_REG\_K Name Register**

|          |               |               |              |         |        |        |               |
|----------|---------------|---------------|--------------|---------|--------|--------|---------------|
| 31       | 30            | 29            | 28           | 27      | 26     | 25     | 24            |
| RESERVED |               |               |              |         |        |        |               |
| NONE     |               |               |              |         |        |        |               |
| 0h       |               |               |              |         |        |        |               |
| 23       | 22            | 21            | 20           | 19      | 18     | 17     | 16            |
| RESERVED |               |               |              |         |        |        |               |
| NONE     |               |               |              |         |        |        |               |
| 0h       |               |               |              |         |        |        |               |
| 15       | 14            | 13            | 12           | 11      | 10     | 9      | 8             |
| RESERVED |               |               |              |         |        |        |               |
| NONE     |               |               |              |         |        |        |               |
| 0h       |               |               |              |         |        |        |               |
| 7        | 6             | 5             | 4            | 3       | 2      | 1      | 0             |
| RESERVED | TX_FIFO_EMPTY | RX_FIFO_EMPTY | TX_FIFO_HOLD | TX_WAKE | TX_LPI | RX_LPI | WAIT_IDLE2LPI |
| NONE     | R             | R             | R            | R       | R      | R      | R             |
| 0h       | 1h            | 1h            | 0h           | 0h      | 0h     | 1h     | 0h            |

**Table 5-400. CPSW\_NC\_ETH\_MAC\_PN\_EEE\_STATUS\_REG\_K Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                                                       |
|------|---------------|------|-------|-----------------------------------------------------------------------------------|
| 31:7 | RESERVED      | NONE | 0h    | Reserved                                                                          |
| 6    | TX_FIFO_EMPTY | R    | 1h    | Transmit FIFO (switch egress) is empty - contains no packets                      |
| 5    | RX_FIFO_EMPTY | R    | 1h    | Receive FIFO (switch ingress) is empty - contains no packets                      |
| 4    | TX_FIFO_HOLD  | R    | 0h    | Transmit FIFO hold - asserted in the LPI state and during the LPI2WAKE count time |
| 3    | TX_WAKE       | R    | 0h    | Transmit wakeup - asserted in the transmit LPI2WAKE count time                    |
| 2    | TX_LPI        | R    | 0h    | Transmit LPI state - asserted when the port 0 transmit is in the LPI state        |
| 1    | RX_LPI        | R    | 1h    | Receive LPI state - asserted when the port 0 receive is in the LPI state          |
| 0    | WAIT_IDLE2LPI | R    | 0h    | CPPI port 0 wait idle to LPI - asserted when port 0 is counting the IDLE2LPI time |



### 5.1.2.134 CPSW\_NC\_ETH\_MAC\_PN\_FIFO\_STATUS\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_FIFO\_STATUS\_REG\_K Register (Offset = 22050h) [reset = FF00h]

Enet Port N FIFO STATUS

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-401. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2050h + formula |

**Figure 5-134. CPSW\_NC\_ETH\_MAC\_PN\_FIFO\_STATUS\_REG\_K Name Register**

|                |    |    |    |    |            |             |             |
|----------------|----|----|----|----|------------|-------------|-------------|
| 31             | 30 | 29 | 28 | 27 | 26         | 25          | 24          |
| RESERVED       |    |    |    |    |            |             |             |
| NONE           |    |    |    |    |            |             |             |
| 0h             |    |    |    |    |            |             |             |
| 23             | 22 | 21 | 20 | 19 | 18         | 17          | 16          |
| RESERVED       |    |    |    |    | EST_BUFACT | EST_ADD_ERR | EST_CNT_ERR |
| NONE           |    |    |    |    | R          | R           | R           |
| 0h             |    |    |    |    | 0h         | 0h          | 0h          |
| 15             | 14 | 13 | 12 | 11 | 10         | 9           | 8           |
| TX_E_MAC_ALLOW |    |    |    |    |            |             |             |
| R              |    |    |    |    |            |             |             |
| FFh            |    |    |    |    |            |             |             |
| 7              | 6  | 5  | 4  | 3  | 2          | 1           | 0           |
| TX_PRI_ACTIVE  |    |    |    |    |            |             |             |
| R              |    |    |    |    |            |             |             |
| 0h             |    |    |    |    |            |             |             |

**Table 5-403. CPSW\_NC\_ETH\_MAC\_PN\_FIFO\_STATUS\_REG\_K Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:19 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 18    | EST_BUFACT     | R    | 0h    | EST RAM active buffer - Indicates the active 64-word fetch buffer when pn_est_onebuf is cleared to zero. Indicates the fetch ram address MSB when pn_est_onebuf set to one.                                                                                                                                                                                                                                                  |
| 17    | EST_ADD_ERR    | R    | 0h    | EST Address Error - Indicates that the fetch ram was read again after the previous maximum buffer address read (the previous fetch from the maximum address is reused).                                                                                                                                                                                                                                                      |
| 16    | EST_CNT_ERR    | R    | 0h    | EST Fetch Count Error - Indicates that insufficient clocks were programmed into the fetch count and that another fetch was commanded before the previous fetch finished.                                                                                                                                                                                                                                                     |
| 15:8  | TX_E_MAC_ALLOW | R    | FFh   | Transmit mac allow - Bus that indicates the actual priorities assigned to the express queue (and inversely the priorities assigned to the preempt queue). The pn_mac_preempt[7:0] field in the Enet_Pn_IET_Control register indicates which priorities should be assigned to the express/preempt queues. The switch between queues happens only when the priority is empty and the actual assignment is shown in this field. |
| 7:0   | TX_PRI_ACTIVE  | R    | 0h    | Transmit Priority Active - Bus that indicates which priorities have packets (non-empty) at the time of the register read.                                                                                                                                                                                                                                                                                                    |

### 5.1.2.135 CPSW\_NC\_ETH\_MAC\_PN\_EST\_CONTROL\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_EST\_CONTROL\_REG\_K Register (Offset = 22060h) [reset = 0h]

Enet Port N EST CONTROL

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-404. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2060h + formula |

**Figure 5-135. CPSW\_NC\_ETH\_MAC\_PN\_EST\_CONTROL\_REG\_K Name Register**

|                 |    |    |               |              |           |                 |            |
|-----------------|----|----|---------------|--------------|-----------|-----------------|------------|
| 31              | 30 | 29 | 28            | 27           | 26        | 25              | 24         |
| RESERVED        |    |    |               |              |           | EST_FILL_MARGIN |            |
| NONE            |    |    |               |              |           | R/W             |            |
| 0h              |    |    |               |              |           | 0h              |            |
| 23              | 22 | 21 | 20            | 19           | 18        | 17              | 16         |
| EST_FILL_MARGIN |    |    |               |              |           |                 |            |
| R/W             |    |    |               |              |           |                 |            |
| 0h              |    |    |               |              |           |                 |            |
| 15              | 14 | 13 | 12            | 11           | 10        | 9               | 8          |
| EST_PREMPT_COMP |    |    |               |              |           | EST_FILL_EN     |            |
| R/W             |    |    |               |              |           | R/W             |            |
| 0h              |    |    |               |              |           | 0h              |            |
| 7               | 6  | 5  | 4             | 3            | 2         | 1               | 0          |
| EST_TS_PRI      |    |    | EST_TS_ONEPRI | EST_TS_FIRST | EST_TS_EN | EST_BUFSEL      | EST_ONEBUF |
| R/W             |    |    | R/W           | R/W          | R/W       | R/W             | R/W        |
| 0h              |    |    | 0h            | 0h           | 0h        | 0h              | 0h         |

**Table 5-406. CPSW\_NC\_ETH\_MAC\_PN\_EST\_CONTROL\_REG\_K Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:26 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 25:16 | EST_FILL_MARGIN | R/W  | 0h    | EST Fill Margin - Sets the fill margin (in bytes) required to ensure that the Ethernet wire is clear so that the timed EST express packet can egress at the correct required time. Setting this value too high will put an unnecessary gap on the wire. Setting this value too low will cause the express packet to egress at a time later than intended (pushed out by non express traffic that did not have sufficient time to finish). |
| 15:9  | EST_PREMPT_COMP | R/W  | 0h    | EST Preempt Comparison Value - When the count in a zero allow is less than or equal to this value in bytes (times 8), preempt packets are cleared from the wire. This is the preempt clear margin value.                                                                                                                                                                                                                                  |
| 8     | EST_FILL_EN     | R/W  | 0h    | EST Fill Enable - Enable EST fill mode when set.                                                                                                                                                                                                                                                                                                                                                                                          |
| 7:5   | EST_TS_PRI      | R/W  | 0h    | EST Timestamp Express Priority - Selects the express priority that timestamp(s) will be generated on when pn_est_ts_onepri is set.                                                                                                                                                                                                                                                                                                        |
| 4     | EST_TS_ONEPRI   | R/W  | 0h    | EST Timestamp One Express Priority - When set, timestamps are only enabled on packets on the express priority selected by pn_est_ts_pri. When cleared to zero, express packet selection for timestamps is independent of priority.                                                                                                                                                                                                        |

**Table 5-406. CPSW\_NC\_ETH\_MAC\_PN\_EST\_CONTROL\_REG\_K Register Field Descriptions (continued)**

| Bit | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                               |
|-----|--------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3   | EST_TS_FIRST | R/W  | 0h    | EST Timestamp First Express Packet only - Generate a timestamp only on the first selected express packet in each EST time interval when express timestamps are enabled. (If pn_est_ts_onepri is also set then the timestamp is generated only on the first packet on pn_est_ts_pri).                                                                                      |
| 2   | EST_TS_EN    | R/W  | 0h    | EST Timestamp Enable - Enable express timestamps (when est_en and pn_est_port_en are set).                                                                                                                                                                                                                                                                                |
| 1   | EST_BUFSEL   | R/W  | 0h    | EST Buffer Select - If pn_est_onebuf is cleared, this bit selects the upper (when set) or the lower (when cleared) 64-word fetch buffer. The actual fetch buffer used changes only at the start of the EST time interval and can be read in the Enet_Pn_FIFO_Status register pn_est_bufact bit.                                                                           |
| 0   | EST_ONEBUF   | R/W  | 0h    | EST One Fetch Buffer - When set indicates that all 128 fetch words are used in one buffer. When cleared, indicates that the 128 fetch words are split into two 64-word fetch buffers. The pn_est_bufsel selects the buffer to be used when pn_est_onebuf is cleared to zero. Two buffers allows software to change a buffer while the hardware is using the other buffer. |

### 5.1.2.136 CPSW\_NC\_ETH\_MAC\_PN\_FH\_DSCP\_MAP\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_FH\_DSCP\_MAP\_REG\_K Register (Offset = 22120h) [reset = 0h]

Enet Port N Receive IPV4/IPV6 DSCP Map N

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-407. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2120h + formula |

**Figure 5-136. CPSW\_NC\_ETH\_MAC\_PN\_FH\_DSCP\_MAP\_REG\_K Name Register**

| 31       | 30 | 29   | 28 | 27       | 26 | 25   | 24 |
|----------|----|------|----|----------|----|------|----|
| RESERVED |    | PRI7 |    | RESERVED |    | PRI6 |    |
| NONE     |    | R/W  |    | NONE     |    | R/W  |    |
| 0h       |    | 0h   |    | 0h       |    | 0h   |    |
| 23       | 22 | 21   | 20 | 19       | 18 | 17   | 16 |
| RESERVED |    | PRI5 |    | RESERVED |    | PRI4 |    |
| NONE     |    | R/W  |    | NONE     |    | R/W  |    |
| 0h       |    | 0h   |    | 0h       |    | 0h   |    |
| 15       | 14 | 13   | 12 | 11       | 10 | 9    | 8  |
| RESERVED |    | PRI3 |    | RESERVED |    | PRI2 |    |
| NONE     |    | R/W  |    | NONE     |    | R/W  |    |
| 0h       |    | 0h   |    | 0h       |    | 0h   |    |
| 7        | 6  | 5    | 4  | 3        | 2  | 1    | 0  |
| RESERVED |    | PRI1 |    | RESERVED |    | PRI0 |    |
| NONE     |    | R/W  |    | NONE     |    | R/W  |    |
| 0h       |    | 0h   |    | 0h       |    | 0h   |    |

**Table 5-409. CPSW\_NC\_ETH\_MAC\_PN\_FH\_DSCP\_MAP\_REG\_K Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                     |
|-------|----------|------|-------|-----------------------------------------------------------------|
| 31    | RESERVED | NONE | 0h    | Reserved                                                        |
| 30:28 | PRI7     | R/W  | 0h    | A DSCP IPV4/V6 packet TOS 7 is mapped to this received priority |
| 27    | RESERVED | NONE | 0h    | Reserved                                                        |
| 26:24 | PRI6     | R/W  | 0h    | A DSCP IPV4/V6 packet TOS 6 is mapped to this received priority |
| 23    | RESERVED | NONE | 0h    | Reserved                                                        |
| 22:20 | PRI5     | R/W  | 0h    | A DSCP IPV4/V6 packet TOS 5 is mapped to this received priority |
| 19    | RESERVED | NONE | 0h    | Reserved                                                        |
| 18:16 | PRI4     | R/W  | 0h    | A DSCP IPV4/V6 packet TOS 4 is mapped to this received priority |
| 15    | RESERVED | NONE | 0h    | Reserved                                                        |
| 14:12 | PRI3     | R/W  | 0h    | A DSCP IPV4/V6 packet TOS 3 is mapped to this received priority |
| 11    | RESERVED | NONE | 0h    | Reserved                                                        |
| 10:8  | PRI2     | R/W  | 0h    | A DSCP IPV4/V6 packet TOS 2 is mapped to this received priority |
| 7     | RESERVED | NONE | 0h    | Reserved                                                        |
| 6:4   | PRI1     | R/W  | 0h    | A DSCP IPV4/V6 packet TOS 1 is mapped to this received priority |
| 3     | RESERVED | NONE | 0h    | Reserved                                                        |
| 2:0   | PRI0     | R/W  | 0h    | A DSCP IPV4/V6 packet TOS 0 is mapped to this received priority |

### 5.1.2.137 CPSW\_NC\_ETH\_MAC\_PN\_PRI\_CIR\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_PRI\_CIR\_REG\_K Register (Offset = 22140h) [reset = 0h]

Enet Port N Rx Priority P Committed Information Rate Value

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-410. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2140h + formula |

**Figure 5-137. CPSW\_NC\_ETH\_MAC\_PN\_PRI\_CIR\_REG\_K Name Register**

|          |    |    |    |         |    |    |    |
|----------|----|----|----|---------|----|----|----|
| 31       | 30 | 29 | 28 | 27      | 26 | 25 | 24 |
| RESERVED |    |    |    | PRI_CIR |    |    |    |
| NONE     |    |    |    | R/W     |    |    |    |
| 0h       |    |    |    | 0h      |    |    |    |
| 23       | 22 | 21 | 20 | 19      | 18 | 17 | 16 |
| PRI_CIR  |    |    |    |         |    |    |    |
| R/W      |    |    |    |         |    |    |    |
| 0h       |    |    |    |         |    |    |    |
| 15       | 14 | 13 | 12 | 11      | 10 | 9  | 8  |
| PRI_CIR  |    |    |    |         |    |    |    |
| R/W      |    |    |    |         |    |    |    |
| 0h       |    |    |    |         |    |    |    |
| 7        | 6  | 5  | 4  | 3       | 2  | 1  | 0  |
| PRI_CIR  |    |    |    |         |    |    |    |
| R/W      |    |    |    |         |    |    |    |
| 0h       |    |    |    |         |    |    |    |

**Table 5-412. CPSW\_NC\_ETH\_MAC\_PN\_PRI\_CIR\_REG\_K Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                           |
|-------|----------|------|-------|---------------------------------------|
| 31:28 | RESERVED | NONE | 0h    | Reserved                              |
| 27:0  | PRI_CIR  | R/W  | 0h    | Priority N committed information rate |

### 5.1.2.138 CPSW\_NC\_ETH\_MAC\_PN\_PRI\_EIR\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_PRI\_EIR\_REG\_K Register (Offset = 22160h) [reset = 0h]

Enet Port N Rx Priority P Excess Information Rate Value

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-413. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2160h + formula |

**Figure 5-138. CPSW\_NC\_ETH\_MAC\_PN\_PRI\_EIR\_REG\_K Name Register**

|          |    |    |    |         |    |    |    |
|----------|----|----|----|---------|----|----|----|
| 31       | 30 | 29 | 28 | 27      | 26 | 25 | 24 |
| RESERVED |    |    |    | PRI_EIR |    |    |    |
| NONE     |    |    |    | R/W     |    |    |    |
| 0h       |    |    |    | 0h      |    |    |    |
| 23       | 22 | 21 | 20 | 19      | 18 | 17 | 16 |
| PRI_EIR  |    |    |    |         |    |    |    |
| R/W      |    |    |    |         |    |    |    |
| 0h       |    |    |    |         |    |    |    |
| 15       | 14 | 13 | 12 | 11      | 10 | 9  | 8  |
| PRI_EIR  |    |    |    |         |    |    |    |
| R/W      |    |    |    |         |    |    |    |
| 0h       |    |    |    |         |    |    |    |
| 7        | 6  | 5  | 4  | 3       | 2  | 1  | 0  |
| PRI_EIR  |    |    |    |         |    |    |    |
| R/W      |    |    |    |         |    |    |    |
| 0h       |    |    |    |         |    |    |    |

**Table 5-415. CPSW\_NC\_ETH\_MAC\_PN\_PRI\_EIR\_REG\_K Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                              |
|-------|----------|------|-------|------------------------------------------|
| 31:28 | RESERVED | NONE | 0h    | Reserved                                 |
| 27:0  | PRI_EIR  | R/W  | 0h    | Priority N Excess Information Rate count |

### 5.1.2.139 CPSW\_NC\_ETH\_MAC\_PN\_TX\_D\_THRESH\_SET\_L\_REG\_K Register

**1 CPSW\_NC\_ETH\_MAC\_PN\_TX\_D\_THRESH\_SET\_L\_REG\_K Register (Offset = 22180h) [reset = 1F1F1F1Fh]**

Enet Port N Tx PFC Destination Threshold Set Low

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-416. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2180h + formula |

**Figure 5-139. CPSW\_NC\_ETH\_MAC\_PN\_TX\_D\_THRESH\_SET\_L\_REG\_K Name Register**

| 31       | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
|----------|----|----|----|------|----|----|----|
| RESERVED |    |    |    | PRI3 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |
| 23       | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| RESERVED |    |    |    | PRI2 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |
| 15       | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| RESERVED |    |    |    | PRI1 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |
| 7        | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| RESERVED |    |    |    | PRI0 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |

**Table 5-418. CPSW\_NC\_ETH\_MAC\_PN\_TX\_D\_THRESH\_SET\_L\_REG\_K Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                         |
|-------|----------|------|-------|---------------------------------------------------------------------|
| 31:29 | RESERVED | NONE | 0h    | Reserved                                                            |
| 28:24 | PRI3     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 3 |
| 23:21 | RESERVED | NONE | 0h    | Reserved                                                            |
| 20:16 | PRI2     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 2 |
| 15:13 | RESERVED | NONE | 0h    | Reserved                                                            |
| 12:8  | PRI1     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 1 |
| 7:5   | RESERVED | NONE | 0h    | Reserved                                                            |
| 4:0   | PRI0     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 0 |

### 5.1.2.140 CPSW\_NC\_ETH\_MAC\_PN\_TX\_D\_THRESH\_SET\_H\_REG\_K Register

**1 CPSW\_NC\_ETH\_MAC\_PN\_TX\_D\_THRESH\_SET\_H\_REG\_K Register (Offset = 22184h) [reset = 1F1F1F1Fh]**

Enet Port N Tx PFC Destination Threshold Set High

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-419. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2184h + formula |

**Figure 5-140. CPSW\_NC\_ETH\_MAC\_PN\_TX\_D\_THRESH\_SET\_H\_REG\_K Name Register**

|          |    |    |    |      |    |    |    |
|----------|----|----|----|------|----|----|----|
| 31       | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
| RESERVED |    |    |    | PRI7 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |
| 23       | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| RESERVED |    |    |    | PRI6 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |
| 15       | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| RESERVED |    |    |    | PRI5 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |
| 7        | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| RESERVED |    |    |    | PRI4 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |

**Table 5-421. CPSW\_NC\_ETH\_MAC\_PN\_TX\_D\_THRESH\_SET\_H\_REG\_K Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                         |
|-------|----------|------|-------|---------------------------------------------------------------------|
| 31:29 | RESERVED | NONE | 0h    | Reserved                                                            |
| 28:24 | PRI7     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 7 |
| 23:21 | RESERVED | NONE | 0h    | Reserved                                                            |
| 20:16 | PRI6     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 6 |
| 15:13 | RESERVED | NONE | 0h    | Reserved                                                            |
| 12:8  | PRI5     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 5 |
| 7:5   | RESERVED | NONE | 0h    | Reserved                                                            |
| 4:0   | PRI4     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 4 |



### 5.1.2.141 CPSW\_NC\_ETH\_MAC\_PN\_TX\_D\_THRESH\_CLR\_L\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_TX\_D\_THRESH\_CLR\_L\_REG\_K Register (Offset = 22188h) [reset = 0h]

Enet Port N Tx PFC Destination Threshold Clr Low

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-422. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2188h + formula |

**Figure 5-141. CPSW\_NC\_ETH\_MAC\_PN\_TX\_D\_THRESH\_CLR\_L\_REG\_K Name Register**

|          |    |    |    |      |    |    |    |
|----------|----|----|----|------|----|----|----|
| 31       | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
| RESERVED |    |    |    | PRI3 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 23       | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| RESERVED |    |    |    | PRI2 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 15       | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| RESERVED |    |    |    | PRI1 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 7        | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| RESERVED |    |    |    | PRI0 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |

**Table 5-424. CPSW\_NC\_ETH\_MAC\_PN\_TX\_D\_THRESH\_CLR\_L\_REG\_K Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                           |
|-------|----------|------|-------|-----------------------------------------------------------------------|
| 31:29 | RESERVED | NONE | 0h    | Reserved                                                              |
| 28:24 | PRI3     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 3 |
| 23:21 | RESERVED | NONE | 0h    | Reserved                                                              |
| 20:16 | PRI2     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 2 |
| 15:13 | RESERVED | NONE | 0h    | Reserved                                                              |
| 12:8  | PRI1     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 1 |
| 7:5   | RESERVED | NONE | 0h    | Reserved                                                              |
| 4:0   | PRI0     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 0 |

### 5.1.2.142 CPSW\_NC\_ETH\_MAC\_PN\_TX\_D\_THRESH\_CLR\_H\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_TX\_D\_THRESH\_CLR\_H\_REG\_K Register (Offset = 2218Ch) [reset = 0h]

Enet Port N Tx PFC Destination Threshold Clr High

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-425. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 218Ch + formula |

**Figure 5-142. CPSW\_NC\_ETH\_MAC\_PN\_TX\_D\_THRESH\_CLR\_H\_REG\_K Name Register**

|          |    |    |    |      |    |    |    |
|----------|----|----|----|------|----|----|----|
| 31       | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
| RESERVED |    |    |    | PRI7 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 23       | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| RESERVED |    |    |    | PRI6 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 15       | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| RESERVED |    |    |    | PRI5 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 7        | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| RESERVED |    |    |    | PRI4 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |

**Table 5-427. CPSW\_NC\_ETH\_MAC\_PN\_TX\_D\_THRESH\_CLR\_H\_REG\_K Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                           |
|-------|----------|------|-------|-----------------------------------------------------------------------|
| 31:29 | RESERVED | NONE | 0h    | Reserved                                                              |
| 28:24 | PRI7     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 7 |
| 23:21 | RESERVED | NONE | 0h    | Reserved                                                              |
| 20:16 | PRI6     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 6 |
| 15:13 | RESERVED | NONE | 0h    | Reserved                                                              |
| 12:8  | PRI5     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 5 |
| 7:5   | RESERVED | NONE | 0h    | Reserved                                                              |
| 4:0   | PRI4     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 4 |

### 5.1.2.143 CPSW\_NC\_ETH\_MAC\_PN\_TX\_G\_BUF\_THRESH\_SET\_L\_REG\_K Register

**1 CPSW\_NC\_ETH\_MAC\_PN\_TX\_G\_BUF\_THRESH\_SET\_L\_REG\_K Register (Offset = 22190h) [reset = 1F1F1F1Fh]**

Enet Port N Tx PFC Global Buffer Threshold Set Low

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-428. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2190h + formula |

**Figure 5-143. CPSW\_NC\_ETH\_MAC\_PN\_TX\_G\_BUF\_THRESH\_SET\_L\_REG\_K Name Register**

| 31       | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
|----------|----|----|----|------|----|----|----|
| RESERVED |    |    |    | PRI3 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |
| 23       | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| RESERVED |    |    |    | PRI2 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |
| 15       | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| RESERVED |    |    |    | PRI1 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |
| 7        | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| RESERVED |    |    |    | PRI0 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |

**Table 5-430. CPSW\_NC\_ETH\_MAC\_PN\_TX\_G\_BUF\_THRESH\_SET\_L\_REG\_K Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                         |
|-------|----------|------|-------|---------------------------------------------------------------------|
| 31:29 | RESERVED | NONE | 0h    | Reserved                                                            |
| 28:24 | PRI3     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 3 |
| 23:21 | RESERVED | NONE | 0h    | Reserved                                                            |
| 20:16 | PRI2     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 2 |
| 15:13 | RESERVED | NONE | 0h    | Reserved                                                            |
| 12:8  | PRI1     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 1 |
| 7:5   | RESERVED | NONE | 0h    | Reserved                                                            |
| 4:0   | PRI0     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 0 |

### 5.1.2.144 CPSW\_NC\_ETH\_MAC\_PN\_TX\_G\_BUF\_THRESH\_SET\_H\_REG\_K Register

**1 CPSW\_NC\_ETH\_MAC\_PN\_TX\_G\_BUF\_THRESH\_SET\_H\_REG\_K Register (Offset = 22194h) [reset = 1F1F1F1Fh]**

Enet Port N Tx PFC Global Buffer Threshold Set High

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-431. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2194h + formula |

**Figure 5-144. CPSW\_NC\_ETH\_MAC\_PN\_TX\_G\_BUF\_THRESH\_SET\_H\_REG\_K Name Register**

|          |    |    |    |      |    |    |    |
|----------|----|----|----|------|----|----|----|
| 31       | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
| RESERVED |    |    |    | PRI7 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |
| 23       | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| RESERVED |    |    |    | PRI6 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |
| 15       | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| RESERVED |    |    |    | PRI5 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |
| 7        | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| RESERVED |    |    |    | PRI4 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 1Fh  |    |    |    |

**Table 5-433. CPSW\_NC\_ETH\_MAC\_PN\_TX\_G\_BUF\_THRESH\_SET\_H\_REG\_K Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                         |
|-------|----------|------|-------|---------------------------------------------------------------------|
| 31:29 | RESERVED | NONE | 0h    | Reserved                                                            |
| 28:24 | PRI7     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 7 |
| 23:21 | RESERVED | NONE | 0h    | Reserved                                                            |
| 20:16 | PRI6     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 6 |
| 15:13 | RESERVED | NONE | 0h    | Reserved                                                            |
| 12:8  | PRI5     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 5 |
| 7:5   | RESERVED | NONE | 0h    | Reserved                                                            |
| 4:0   | PRI4     | R/W  | 1Fh   | Port Priority Based Flow Control Threshold Set Value for Priority 4 |

### 5.1.2.145 CPSW\_NC\_ETH\_MAC\_PN\_TX\_G\_BUF\_THRESH\_CLR\_L\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_TX\_G\_BUF\_THRESH\_CLR\_L\_REG\_K Register (Offset = 22198h) [reset = 0h]

Enet Port N Tx PFC Global Buffer Threshold Clr Low

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-434. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2198h + formula |

**Figure 5-145. CPSW\_NC\_ETH\_MAC\_PN\_TX\_G\_BUF\_THRESH\_CLR\_L\_REG\_K Name Register**

| 31       | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
|----------|----|----|----|------|----|----|----|
| RESERVED |    |    |    | PRI3 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 23       | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| RESERVED |    |    |    | PRI2 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 15       | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| RESERVED |    |    |    | PRI1 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 7        | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| RESERVED |    |    |    | PRI0 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |

**Table 5-436. CPSW\_NC\_ETH\_MAC\_PN\_TX\_G\_BUF\_THRESH\_CLR\_L\_REG\_K Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                           |
|-------|----------|------|-------|-----------------------------------------------------------------------|
| 31:29 | RESERVED | NONE | 0h    | Reserved                                                              |
| 28:24 | PRI3     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 3 |
| 23:21 | RESERVED | NONE | 0h    | Reserved                                                              |
| 20:16 | PRI2     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 2 |
| 15:13 | RESERVED | NONE | 0h    | Reserved                                                              |
| 12:8  | PRI1     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 1 |
| 7:5   | RESERVED | NONE | 0h    | Reserved                                                              |
| 4:0   | PRI0     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 0 |

### 5.1.2.146 CPSW\_NC\_ETH\_MAC\_PN\_TX\_G\_BUF\_THRESH\_CLR\_H\_REG\_K Register

**1 CPSW\_NC\_ETH\_MAC\_PN\_TX\_G\_BUF\_THRESH\_CLR\_H\_REG\_K Register (Offset = 2219Ch) [reset = 0h]**

Enet Port N Tx PFC Global Buffer Threshold Clr High

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-437. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 219Ch + formula |

**Figure 5-146. CPSW\_NC\_ETH\_MAC\_PN\_TX\_G\_BUF\_THRESH\_CLR\_H\_REG\_K Name Register**

|          |    |    |    |      |    |    |    |
|----------|----|----|----|------|----|----|----|
| 31       | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
| RESERVED |    |    |    | PRI7 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 23       | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| RESERVED |    |    |    | PRI6 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 15       | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| RESERVED |    |    |    | PRI5 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 7        | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| RESERVED |    |    |    | PRI4 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |

**Table 5-439. CPSW\_NC\_ETH\_MAC\_PN\_TX\_G\_BUF\_THRESH\_CLR\_H\_REG\_K Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                           |
|-------|----------|------|-------|-----------------------------------------------------------------------|
| 31:29 | RESERVED | NONE | 0h    | Reserved                                                              |
| 28:24 | PRI7     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 7 |
| 23:21 | RESERVED | NONE | 0h    | Reserved                                                              |
| 20:16 | PRI6     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 6 |
| 15:13 | RESERVED | NONE | 0h    | Reserved                                                              |
| 12:8  | PRI5     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 5 |
| 7:5   | RESERVED | NONE | 0h    | Reserved                                                              |
| 4:0   | PRI4     | R/W  | 0h    | Port Priority Based Flow Control Threshold Clear Value for Priority 4 |

### 5.1.2.147 CPSW\_NC\_ETH\_MAC\_PN\_TX\_D\_OFLOW\_ADDVAL\_L\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_TX\_D\_OFLOW\_ADDVAL\_L\_REG\_K Register (Offset = 22300h) [reset = 0h]

Enet Port N Tx Destination Out Flow Add Values Low

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-440. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2300h + formula |

**Figure 5-147. CPSW\_NC\_ETH\_MAC\_PN\_TX\_D\_OFLOW\_ADDVAL\_L\_REG\_K Name Register**

|          |    |    |    |      |    |    |    |
|----------|----|----|----|------|----|----|----|
| 31       | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
| RESERVED |    |    |    | PRI3 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 23       | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| RESERVED |    |    |    | PRI2 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 15       | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| RESERVED |    |    |    | PRI1 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 7        | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| RESERVED |    |    |    | PRI0 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |

**Table 5-442. CPSW\_NC\_ETH\_MAC\_PN\_TX\_D\_OFLOW\_ADDVAL\_L\_REG\_K Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                  |
|-------|----------|------|-------|--------------------------------------------------------------|
| 31:29 | RESERVED | NONE | 0h    | Reserved                                                     |
| 28:24 | PRI3     | R/W  | 0h    | Port PFC Destination Based Out Flow Add Value for Priority 3 |
| 23:21 | RESERVED | NONE | 0h    | Reserved                                                     |
| 20:16 | PRI2     | R/W  | 0h    | Port PFC Destination Based Out Flow Add Value for Priority 2 |
| 15:13 | RESERVED | NONE | 0h    | Reserved                                                     |
| 12:8  | PRI1     | R/W  | 0h    | Port PFC Destination Based Out Flow Add Value for Priority 1 |
| 7:5   | RESERVED | NONE | 0h    | Reserved                                                     |
| 4:0   | PRI0     | R/W  | 0h    | Port PFC Destination Based Out Flow Add Value for Priority 0 |

### 5.1.2.148 CPSW\_NC\_ETH\_MAC\_PN\_TX\_D\_OFLOW\_ADDVAL\_H\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_TX\_D\_OFLOW\_ADDVAL\_H\_REG\_K Register (Offset = 22304h) [reset = 0h]

Enet Port N Tx Destination Out Flow Add Values High

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-443. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2304h + formula |

**Figure 5-148. CPSW\_NC\_ETH\_MAC\_PN\_TX\_D\_OFLOW\_ADDVAL\_H\_REG\_K Name Register**

|          |    |    |    |      |    |    |    |
|----------|----|----|----|------|----|----|----|
| 31       | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
| RESERVED |    |    |    | PRI7 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 23       | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| RESERVED |    |    |    | PRI6 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 15       | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| RESERVED |    |    |    | PRI5 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |
| 7        | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| RESERVED |    |    |    | PRI4 |    |    |    |
| NONE     |    |    |    | R/W  |    |    |    |
| 0h       |    |    |    | 0h   |    |    |    |

**Table 5-445. CPSW\_NC\_ETH\_MAC\_PN\_TX\_D\_OFLOW\_ADDVAL\_H\_REG\_K Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                  |
|-------|----------|------|-------|--------------------------------------------------------------|
| 31:29 | RESERVED | NONE | 0h    | Reserved                                                     |
| 28:24 | PRI7     | R/W  | 0h    | Port PFC Destination Based Out Flow Add Value for Priority 7 |
| 23:21 | RESERVED | NONE | 0h    | Reserved                                                     |
| 20:16 | PRI6     | R/W  | 0h    | Port PFC Destination Based Out Flow Add Value for Priority 6 |
| 15:13 | RESERVED | NONE | 0h    | Reserved                                                     |
| 12:8  | PRI5     | R/W  | 0h    | Port PFC Destination Based Out Flow Add Value for Priority 5 |
| 7:5   | RESERVED | NONE | 0h    | Reserved                                                     |
| 4:0   | PRI4     | R/W  | 0h    | Port PFC Destination Based Out Flow Add Value for Priority 4 |



### 5.1.2.149 CPSW\_NC\_ETH\_MAC\_PN\_SA\_L\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_SA\_L\_REG\_K Register (Offset = 22308h) [reset = 0h]

Enet Port N Tx Pause Frame Source Address Low

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-446. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2308h + formula |

**Figure 5-149. CPSW\_NC\_ETH\_MAC\_PN\_SA\_L\_REG\_K Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MACSRCADDR_7_0  |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MACSRCADDR_15_8 |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 5-448. CPSW\_NC\_ETH\_MAC\_PN\_SA\_L\_REG\_K Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description              |
|-------|-----------------|------|-------|--------------------------|
| 31:16 | RESERVED        | NONE | 0h    | Reserved                 |
| 15:8  | MACSRCADDR_7_0  | R/W  | 0h    | Source Address bits 7:0  |
| 7:0   | MACSRCADDR_15_8 | R/W  | 0h    | Source Address bits 15:8 |

### 5.1.2.150 CPSW\_NC\_ETH\_MAC\_PN\_SA\_H\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_SA\_H\_REG\_K Register (Offset = 2230Ch) [reset = 0h]

Enet Port N Tx Pause Frame Source Address High

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-449. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 230Ch + formula |

**Figure 5-150. CPSW\_NC\_ETH\_MAC\_PN\_SA\_H\_REG\_K Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MACSRCADDR_23_16 |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MACSRCADDR_31_24 |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MACSRCADDR_39_32 |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MACSRCADDR_47_40 |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 5-451. CPSW\_NC\_ETH\_MAC\_PN\_SA\_H\_REG\_K Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description               |
|-------|------------------|------|-------|---------------------------|
| 31:24 | MACSRCADDR_23_16 | R/W  | 0h    | Source Address bits 23:16 |
| 23:16 | MACSRCADDR_31_24 | R/W  | 0h    | Source Address bits 31:24 |
| 15:8  | MACSRCADDR_39_32 | R/W  | 0h    | Source Address bits 39:32 |
| 7:0   | MACSRCADDR_47_40 | R/W  | 0h    | Source Address bits 47:40 |

### 5.1.2.151 CPSW\_NC\_ETH\_MAC\_PN\_TS\_CTL\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_TS\_CTL\_REG\_K Register (Offset = 22310h) [reset = 0h]

Enet Port N Time Sync Control

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-452. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2310h + formula |

**Figure 5-151. CPSW\_NC\_ETH\_MAC\_PN\_TS\_CTL\_REG\_K Name Register**

|                  |                      |                      |                  |                  |                      |                      |                  |
|------------------|----------------------|----------------------|------------------|------------------|----------------------|----------------------|------------------|
| 31               | 30                   | 29                   | 28               | 27               | 26                   | 25                   | 24               |
| TS_MSG_TYPE_EN   |                      |                      |                  |                  |                      |                      |                  |
| R/W              |                      |                      |                  |                  |                      |                      |                  |
| 0h               |                      |                      |                  |                  |                      |                      |                  |
| 23               | 22                   | 21                   | 20               | 19               | 18                   | 17                   | 16               |
| TS_MSG_TYPE_EN   |                      |                      |                  |                  |                      |                      |                  |
| R/W              |                      |                      |                  |                  |                      |                      |                  |
| 0h               |                      |                      |                  |                  |                      |                      |                  |
| 15               | 14                   | 13                   | 12               | 11               | 10                   | 9                    | 8                |
| RESERVED         |                      |                      |                  | TS_TX_HOST_TS_EN | TS_TX_ANNEX_E_EN     | TS_RX_ANNEX_E_EN     | TS_LTYPE2_EN     |
| NONE             |                      |                      |                  | R/W              | R/W                  | R/W                  | R/W              |
| 0h               |                      |                      |                  | 0h               | 0h                   | 0h                   | 0h               |
| 7                | 6                    | 5                    | 4                | 3                | 2                    | 1                    | 0                |
| TS_TX_ANNEX_D_EN | TS_TX_VLAN_LTYPE2_EN | TS_TX_VLAN_LTYPE1_EN | TS_TX_ANNEX_F_EN | TS_RX_ANNEX_D_EN | TS_RX_VLAN_LTYPE2_EN | TS_RX_VLAN_LTYPE1_EN | TS_RX_ANNEX_F_EN |
| R/W              | R/W                  | R/W                  | R/W              | R/W              | R/W                  | R/W                  | R/W              |
| 0h               | 0h                   | 0h                   | 0h               | 0h               | 0h                   | 0h                   | 0h               |

**Table 5-454. CPSW\_NC\_ETH\_MAC\_PN\_TS\_CTL\_REG\_K Register Field Descriptions**

| Bit   | Field                | Type | Reset | Description                                                                                                                                                                  |
|-------|----------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | TS_MSG_TYPE_EN       | R/W  | 0h    | Time Sync Message Type Enable - Each bit in this field enables the corresponding message type in receive and transmit time sync messages (Bit 0 enables message type 0 etc.) |
| 15:12 | RESERVED             | NONE | 0h    | Reserved                                                                                                                                                                     |
| 11    | TS_TX_HOST_TS_EN     | R/W  | 0h    | Time Sync Transmit Host Time Stamp Enable                                                                                                                                    |
| 10    | TS_TX_ANNEX_E_EN     | R/W  | 0h    | Time Synce Transmit Annex E Enable                                                                                                                                           |
| 9     | TS_RX_ANNEX_E_EN     | R/W  | 0h    | Time Synce Receive Annex E Enable                                                                                                                                            |
| 8     | TS_LTYPE2_EN         | R/W  | 0h    | Time Sync LTYPE 2 Enable (transmit and receive)                                                                                                                              |
| 7     | TS_TX_ANNEX_D_EN     | R/W  | 0h    | Time Synce Transmit Annex D Enable                                                                                                                                           |
| 6     | TS_TX_VLAN_LTYPE2_EN | R/W  | 0h    | Time Sync Transmit VLAN LTYPE 2 enable                                                                                                                                       |
| 5     | TS_TX_VLAN_LTYPE1_EN | R/W  | 0h    | Time Sync Transmit VLAN LTYPE 1 enable                                                                                                                                       |
| 4     | TS_TX_ANNEX_F_EN     | R/W  | 0h    | Time Synce Transmit Annex F Enable                                                                                                                                           |
| 3     | TS_RX_ANNEX_D_EN     | R/W  | 0h    | Time Synce Receive Annex D Enable                                                                                                                                            |
| 2     | TS_RX_VLAN_LTYPE2_EN | R/W  | 0h    | Time Sync Receive VLAN LTYPE 2 enable                                                                                                                                        |

**Table 5-454. CPSW\_NC\_ETH\_MAC\_PN\_TS\_CTL\_REG\_K Register Field Descriptions (continued)**

| Bit | Field                | Type | Reset | Description                           |
|-----|----------------------|------|-------|---------------------------------------|
| 1   | TS_RX_VLAN_LTYPE1_EN | R/W  | 0h    | Time Sync Receive VLAN LTYPE 1 enable |
| 0   | TS_RX_ANNEX_F_EN     | R/W  | 0h    | Time Synce Receive Annex F Enable     |

### 5.1.2.152 CPSW\_NC\_ETH\_MAC\_PN\_TS\_SEQ\_LTYPE\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_TS\_SEQ\_LTYPE\_REG\_K Register (Offset = 22314h) [reset = 1E0000h]

Enet Port N Time Sync LTYPE (and SEQ\_ID\_OFFSET)

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-455. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2314h + formula |

**Figure 5-152. CPSW\_NC\_ETH\_MAC\_PN\_TS\_SEQ\_LTYPE\_REG\_K Name Register**

|           |    |                  |    |    |    |    |    |
|-----------|----|------------------|----|----|----|----|----|
| 31        | 30 | 29               | 28 | 27 | 26 | 25 | 24 |
| RESERVED  |    |                  |    |    |    |    |    |
| NONE      |    |                  |    |    |    |    |    |
| 0h        |    |                  |    |    |    |    |    |
| 23        | 22 | 21               | 20 | 19 | 18 | 17 | 16 |
| RESERVED  |    | TS_SEQ_ID_OFFSET |    |    |    |    |    |
| NONE      |    | R/W              |    |    |    |    |    |
| 0h        |    | 1Eh              |    |    |    |    |    |
| 15        | 14 | 13               | 12 | 11 | 10 | 9  | 8  |
| TS_LTYPE1 |    |                  |    |    |    |    |    |
| R/W       |    |                  |    |    |    |    |    |
| 0h        |    |                  |    |    |    |    |    |
| 7         | 6  | 5                | 4  | 3  | 2  | 1  | 0  |
| TS_LTYPE1 |    |                  |    |    |    |    |    |
| R/W       |    |                  |    |    |    |    |    |
| 0h        |    |                  |    |    |    |    |    |

**Table 5-457. CPSW\_NC\_ETH\_MAC\_PN\_TS\_SEQ\_LTYPE\_REG\_K Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                   |
|-------|------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:22 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                      |
| 21:16 | TS_SEQ_ID_OFFSET | R/W  | 1Eh   | Time Sync Sequence ID Offset - This is the number of octets that the sequence ID is offset in the tx and rx time sync message header. The minimum value is 6. |
| 15:0  | TS_LTYPE1        | R/W  | 0h    | Time Sync LTYPE1 - This is the port time sync LTYPE1 value                                                                                                    |

### 5.1.2.153 CPSW\_NC\_ETH\_MAC\_PN\_TS\_VLAN\_LTYPE\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_TS\_VLAN\_LTYPE\_REG\_K Register (Offset = 22318h) [reset = 0h]

Enet Port N Time Sync VLAN2 and VLAN2

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-458. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2318h + formula |

**Figure 5-153. CPSW\_NC\_ETH\_MAC\_PN\_TS\_VLAN\_LTYPE\_REG\_K Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TS_VLAN_LTYPE2 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TS_VLAN_LTYPE2 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TS_VLAN_LTYPE1 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TS_VLAN_LTYPE1 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-460. CPSW\_NC\_ETH\_MAC\_PN\_TS\_VLAN\_LTYPE\_REG\_K Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description           |
|-------|----------------|------|-------|-----------------------|
| 31:16 | TS_VLAN_LTYPE2 | R/W  | 0h    | Time Sync VLAN LTYPE2 |
| 15:0  | TS_VLAN_LTYPE1 | R/W  | 0h    | Time Sync VLAN LTYPE1 |

### 5.1.2.154 CPSW\_NC\_ETH\_MAC\_PN\_TS\_CTL\_LTYPE2\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_TS\_CTL\_LTYPE2\_REG\_K Register (Offset = 2231Ch) [reset = 0h]

Enet Port N Time Sync Control and LTYPE 2

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-461. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 231Ch + formula |

**Figure 5-154. CPSW\_NC\_ETH\_MAC\_PN\_TS\_CTL\_LTYPE2\_REG\_K Name Register**

|                |        |        |        |        |        |        |           |
|----------------|--------|--------|--------|--------|--------|--------|-----------|
| 31             | 30     | 29     | 28     | 27     | 26     | 25     | 24        |
| RESERVED       |        |        |        |        |        |        | TS_UNI_EN |
| NONE           |        |        |        |        |        |        | R/W       |
| 0h             |        |        |        |        |        |        | 0h        |
| 23             | 22     | 21     | 20     | 19     | 18     | 17     | 16        |
| TS_TTL_NONZERO | TS_320 | TS_319 | TS_132 | TS_131 | TS_130 | TS_129 | TS_107    |
| R/W            | R/W    | R/W    | R/W    | R/W    | R/W    | R/W    | R/W       |
| 0h             | 0h     | 0h     | 0h     | 0h     | 0h     | 0h     | 0h        |
| 15             | 14     | 13     | 12     | 11     | 10     | 9      | 8         |
| TS_LTYPE2      |        |        |        |        |        |        |           |
| R/W            |        |        |        |        |        |        |           |
| 0h             |        |        |        |        |        |        |           |
| 7              | 6      | 5      | 4      | 3      | 2      | 1      | 0         |
| TS_LTYPE2      |        |        |        |        |        |        |           |
| R/W            |        |        |        |        |        |        |           |
| 0h             |        |        |        |        |        |        |           |

**Table 5-463. CPSW\_NC\_ETH\_MAC\_PN\_TS\_CTL\_LTYPE2\_REG\_K Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                  |
|-------|----------------|------|-------|----------------------------------------------|
| 31:25 | RESERVED       | NONE | 0h    | Reserved                                     |
| 24    | TS_UNI_EN      | R/W  | 0h    | Time Sync Unicast Enable                     |
| 23    | TS_TTL_NONZERO | R/W  | 0h    | Time Sync Time to Live Non-zero Enable       |
| 22    | TS_320         | R/W  | 0h    | Time Sync Destination Port Number 320 Enable |
| 21    | TS_319         | R/W  | 0h    | Time Sync Destination Port Number 319 Enable |
| 20    | TS_132         | R/W  | 0h    | Time Sync Destination IP Address 132 Enable  |
| 19    | TS_131         | R/W  | 0h    | Time Sync Destination IP Address 131 Enable  |
| 18    | TS_130         | R/W  | 0h    | Time Sync Destination IP Address 130 Enable  |
| 17    | TS_129         | R/W  | 0h    | Time Sync Destination IP Address 129 Enable  |
| 16    | TS_107         | R/W  | 0h    | Time Sync Destination IP Address 107 Enable  |
| 15:0  | TS_LTYPE2      | R/W  | 0h    | Time Sync LTYPE2 value                       |

### 5.1.2.155 CPSW\_NC\_ETH\_MAC\_PN\_TS\_CTL2\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_TS\_CTL2\_REG\_K Register (Offset = 22320h) [reset = 40000h]

Enet Port N Time Sync Control 2

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-464. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2320h + formula |

**Figure 5-155. CPSW\_NC\_ETH\_MAC\_PN\_TS\_CTL2\_REG\_K Name Register**

|                  |    |                  |    |    |    |    |    |
|------------------|----|------------------|----|----|----|----|----|
| 31               | 30 | 29               | 28 | 27 | 26 | 25 | 24 |
| RESERVED         |    |                  |    |    |    |    |    |
| NONE             |    |                  |    |    |    |    |    |
| 0h               |    |                  |    |    |    |    |    |
| 23               | 22 | 21               | 20 | 19 | 18 | 17 | 16 |
| RESERVED         |    | TS_DOMAIN_OFFSET |    |    |    |    |    |
| NONE             |    | R/W              |    |    |    |    |    |
| 0h               |    | 4h               |    |    |    |    |    |
| 15               | 14 | 13               | 12 | 11 | 10 | 9  | 8  |
| TS_MCAST_TYPE_EN |    |                  |    |    |    |    |    |
| R/W              |    |                  |    |    |    |    |    |
| 0h               |    |                  |    |    |    |    |    |
| 7                | 6  | 5                | 4  | 3  | 2  | 1  | 0  |
| TS_MCAST_TYPE_EN |    |                  |    |    |    |    |    |
| R/W              |    |                  |    |    |    |    |    |
| 0h               |    |                  |    |    |    |    |    |

**Table 5-466. CPSW\_NC\_ETH\_MAC\_PN\_TS\_CTL2\_REG\_K Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                         |
|-------|------------------|------|-------|-----------------------------------------------------|
| 31:22 | RESERVED         | NONE | 0h    | Reserved                                            |
| 21:16 | TS_DOMAIN_OFFSET | R/W  | 4h    | Time Sync Domain Offset                             |
| 15:0  | TS_MCAST_TYPE_EN | R/W  | 0h    | Time Sync Multicast Destination Address Type Enable |



### 5.1.2.156 CPSW\_NC\_ETH\_MAC\_PN\_MAC\_CONTROL\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_MAC\_CONTROL\_REG\_K Register (Offset = 22330h) [reset = 0h]

Enet Port N Mac Control

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-467. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2330h + formula |

**Figure 5-156. CPSW\_NC\_ETH\_MAC\_PN\_MAC\_CONTROL\_REG\_K Name Register**

| 31        | 30        | 29                      | 28                 | 27                 | 26                      | 25        | 24         |
|-----------|-----------|-------------------------|--------------------|--------------------|-------------------------|-----------|------------|
| RESERVED  |           |                         |                    |                    |                         |           | RX_CMF_EN  |
| NONE      |           |                         |                    |                    |                         |           | R/W        |
| 0h        |           |                         |                    |                    |                         |           | 0h         |
| 23        | 22        | 21                      | 20                 | 19                 | 18                      | 17        | 16         |
| RX_CSF_EN | RX_CEF_EN | TX_SHORT_G<br>AP_LIM_EN | EXT_TX_FLOW<br>_EN | EXT_RX_FLO<br>W_EN | EXT_EN                  | GIG_FORCE | IFCTL_B    |
| R/W       | R/W       | R/W                     | R/W                | R/W                | R/W                     | R/W       | R/W        |
| 0h        | 0h        | 0h                      | 0h                 | 0h                 | 0h                      | 0h        | 0h         |
| 15        | 14        | 13                      | 12                 | 11                 | 10                      | 9         | 8          |
| IFCTL_A   | RESERVED  |                         | CRC_TYPE           | CMD_IDLE           | TX_SHORT_G<br>AP_ENABLE | RESERVED  |            |
| R/W       | NONE      |                         | R/W                | R/W                | R/W                     | NONE      |            |
| 0h        | 0h        |                         | 0h                 | 0h                 | 0h                      | 0h        |            |
| 7         | 6         | 5                       | 4                  | 3                  | 2                       | 1         | 0          |
| GIG       | TX_PACE   | GMII_EN                 | TX_FLOW_EN         | RX_FLOW_EN         | MTEST                   | LOOPBACK  | FULLDUPLEX |
| R/W       | R/W       | R/W                     | R/W                | R/W                | R/W                     | R/W       | R/W        |
| 0h        | 0h        | 0h                      | 0h                 | 0h                 | 0h                      | 0h        | 0h         |

**Table 5-469. CPSW\_NC\_ETH\_MAC\_PN\_MAC\_CONTROL\_REG\_K Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:25 | RESERVED  | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 24    | RX_CMF_EN | R/W  | 0h    | RX Copy MAC Control Frames Enable - Enables MAC control frames to be transferred to memory. MAC control frames are normally acted upon (if enabled), but not copied/transferred to memory. MAC control frames that are pause frames will be acted upon if enabled in the MacControl register, regardless of the value of pn_rx_cmf_en. Frames transferred to memory due to pn_rx_cmf_en will have the mac_control bit set in their EOP buffer descriptor.<br>0 - MAC control frames are filtered (but are acted upon if enabled).<br>1 - MAC control frames are transferred to the host.                                                                                |
| 23    | RX_CSF_EN | R/W  | 0h    | RX Copy Short Frames Enable - Enables frames or fragments shorter than 64 bytes to be sent to the host. Frames transferred to the host due to pn_rx_csf_en will have the fragment or undersized bit set in their buffer descriptor. Short and fragment frame transfer is not guaranteed for all packet conditions and is best case only. Frames shorter than 33 bytes will be dropped in all cases. Fragments are short frames that contain CRC/align/code errors and undersized are short frames without errors. The pn_rx_cef_en bit must also be set to transfer fragment frames.<br>0 - Short frames are filtered.<br>1 - Short frames are transferred to the host. |

**Table 5-469. CPSW\_NC\_ETH\_MAC\_PN\_MAC\_CONTROL\_REG\_K Register Field Descriptions (continued)**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|---------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 22    | RX_CEF_EN           | R/W  | 0h    | RX Copy Error Frames Enable - Enables frames containing errors to be transferred to memory. The appropriate error bit will be set in the frame receive buffer descriptor. Frames containing errors will be filtered when this bit is not set.<br>0 - Frames containing errors are filtered.<br>1 - Frames containing errors are transferred to the host.                                                                                                                                                                                                                                            |
| 21    | TX_SHORT_GAP_LIM_EN | R/W  | 0h    | Transmit Short Gap Limit Enable - When set this bit limits the number of short gap packets transmitted to 100ppm. The pn_tx_short_gap_en bit must also be set. Each time a short gap packet is sent, a counter is loaded with 10,000 and decremented on each wireside clock. Another short gap packet will not be sent out until the counter decrements to zero. This mode is included to preclude the host from filling up the FIFO and sending every packet out with short gap which would violate the maximum number of packets per second allowed. This bit is used only with GMII (not XGMII). |
| 20    | EXT_TX_FLOW_EN      | R/W  | 0h    | External Transmit Flow Control Enable - Enables the pn_tx_flow_en to be selected from the EXT_TX_FLOW_EN input signal and not from the pn_tx_flow_en bit in this register.                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 19    | EXT_RX_FLOW_EN      | R/W  | 0h    | External Receive Flow Control Enable - Enables the pn_rx_flow_en to be selected from the EXT_RX_FLOW_EN input signal and not from the pn_rx_flow_en bit in this register.                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 18    | EXT_EN              | R/W  | 0h    | External Control Enable - Enables the full duplex and gigabit mode to be selected from the FULLDUPLEX_IN and GIG_IN input signals and not from the pn_full duplex and pn_gig bits in this register. The FULLDUPLEX_MODE bit reflects the actual full duplex mode selected.                                                                                                                                                                                                                                                                                                                          |
| 17    | GIG_FORCE           | R/W  | 0h    | Gigabit Mode Force - This bit is used to force the Enet Mac into gigabit mode if the input GMII_MTCLK has been stopped by the PHY.<br>0 - GIG mode not forced<br>1 - GIG mode forced regardless of transmit clock                                                                                                                                                                                                                                                                                                                                                                                   |
| 16    | IFCTL_B             | R/W  | 0h    | Interface Control B - Intended as a general purpose output bit to be used to control external gaskets associated with the GMII (GMII to RGMII etc).                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 15    | IFCTL_A             | R/W  | 0h    | Interface Control A - Intended as a general purpose output bit to be used to control external gaskets associated with the GMII (GMII to RGMII etc).                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 14:13 | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 12    | CRC_TYPE            | R/W  | 0h    | Port CRC Type -<br>0 - Ethernet CRC.<br>1 - Castagnoli CRC.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 11    | CMD_IDLE            | R/W  | 0h    | Command Idle -<br>0 - Idle not commanded.<br>1 - Idle Commanded (read pn_idle in Enet_Pn_Mac_Status).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 10    | TX_SHORT_GAP_ENABLE | R/W  | 0h    | Transmit Short Gap Enable<br>0 - Transmit with a short IPG is disabled.<br>1 - Transmit with a short IPG is enabled.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 9:8   | RESERVED            | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 7     | GIG                 | R/W  | 0h    | Gigabit Mode -<br>0 - 10/100 mode.<br>1 - Gigabit mode (full duplex only)<br>The GIG_OUT output is the value of this bit. This bit is a don't care when pn_xgig is set.                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 6     | TX_PACE             | R/W  | 0h    | Transmit Pacing Enable -<br>0 - Transmit Pacing Disabled.<br>1 - Transmit Pacing Enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

**Table 5-469. CPSW\_NC\_ETH\_MAC\_PN\_MAC\_CONTROL\_REG\_K Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-----|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | GMII_EN    | R/W  | 0h    | GMII Enable -<br>0 - GMII RX and TX held in reset.<br>1 - GMII RX and TX released from reset.<br>This bit should be written with a logic high before the other bits in this register are written.                                                                                                                                                                                                                                                                                                        |
| 4   | TX_FLOW_EN | R/W  | 0h    | Transmit Flow Control Enable - Determines if incoming pause frames are acted upon in full-duplex mode. Incoming pause frames are not acted upon in half-duplex mode regardless of this bit setting. The RX_MBP_Enable bits determine whether or not received pause frames are transferred to memory.<br>0 - Transmit Flow Control Disabled. Full-duplex mode - Incoming pause frames are not acted upon.<br>1 - Transmit Flow Control Enabled . Full-duplex mode - Incoming pause frames are acted upon. |
| 3   | RX_FLOW_EN | R/W  | 0h    | Receive Flow Control Enable -<br>0 - Receive Flow Control Disabled:<br>Half-duplex mode - No flow control generated collisions are sent. Full-duplex mode - No outgoing pause frames are sent.<br>1 - Receive Flow Control Enabled:<br>Half-duplex mode - Collisions are initiated when receive flow control is triggered.<br>Full-duplex mode - Outgoing pause frames are sent when receive flow control is triggered.                                                                                  |
| 2   | MTEST      | R/W  | 0h    | Manufacturing Test mode - This bit must be set to allow writes to the Backoff_Test and PauseTimer registers.                                                                                                                                                                                                                                                                                                                                                                                             |
| 1   | LOOPBACK   | R/W  | 0h    | Loop Back Mode - Loopback mode forces internal fullduplex mode regardless of whether the pn_fullduplex bit is set or not. The pn_loopback bit should be changed only when pn_gmii_en is de-asserted. Loopback is used only with GMII (not XGMII). Loopback is not compatible with timestamp operations (CPTS).<br>0 - Loop Back Mode disabled.<br>1 - Loop Back Mode enabled.                                                                                                                            |
| 0   | FULLDUPLEX | R/W  | 0h    | Full Duplex mode - Gigabit mode forces fullduplex mode regardless of whether the pn_fullduplex bit is set or not. The FULLDUPLEX_OUT output is the value of this register bit.<br>0 - half duplex mode.<br>1 - full duplex mode.                                                                                                                                                                                                                                                                         |

### 5.1.2.157 CPSW\_NC\_ETH\_MAC\_PN\_MAC\_STATUS\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_MAC\_STATUS\_REG\_K Register (Offset = 22334h) [reset = D0000000h]

Enet Port N Mac Status

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-470. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2334h + formula |

**Figure 5-157. CPSW\_NC\_ETH\_MAC\_PN\_MAC\_STATUS\_REG\_K Name Register**

| 31              | 30             | 29             | 28          | 27             | 26       | 25          | 24          |
|-----------------|----------------|----------------|-------------|----------------|----------|-------------|-------------|
| IDLE            | E_IDLE         | RESERVED       | MAC_TX_IDLE | TORF           | TORF_PRI |             |             |
| R               | R              | NONE           | R           | R              | R        |             |             |
| 1h              | 1h             | 0h             | 1h          | 0h             | 0h       |             |             |
| 23              | 22             | 21             | 20          | 19             | 18       | 17          | 16          |
| TX_PFC_FLOW_ACT |                |                |             |                |          |             |             |
| R               |                |                |             |                |          |             |             |
| 0h              |                |                |             |                |          |             |             |
| 15              | 14             | 13             | 12          | 11             | 10       | 9           | 8           |
| RX_PFC_FLOW_ACT |                |                |             |                |          |             |             |
| R               |                |                |             |                |          |             |             |
| 0h              |                |                |             |                |          |             |             |
| 7               | 6              | 5              | 4           | 3              | 2        | 1           | 0           |
| RESERVED        | EXT_TX_FLOW_EN | EXT_RX_FLOW_EN | EXT_GIG     | EXT_FULLDUPLEX | RESERVED | RX_FLOW_ACT | TX_FLOW_ACT |
| NONE            | R              | R              | R           | R              | NONE     | R           | R           |
| 0h              | 0h             | 0h             | 0h          | 0h             | 0h       | 0h          | 0h          |

**Table 5-472. CPSW\_NC\_ETH\_MAC\_PN\_MAC\_STATUS\_REG\_K Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                        |
|-------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | IDLE            | R    | 1h    | Enet IDLE - The Ethernet port (express and preempt) is in the idle state when high.                                                                |
| 30    | E_IDLE          | R    | 1h    | Express MAC is idle when high                                                                                                                      |
| 29    | RESERVED        | NONE | 0h    | Reserved                                                                                                                                           |
| 28    | MAC_TX_IDLE     | R    | 1h    | Mac Transmit Idle - Both Preempt (if iet_incl) and Express MAC Transmit are in idle state. The transmit clock must be running for this to go idle. |
| 27    | TORF            | R    | 0h    | Top of receive FIFO flow control trigger occurred. This bit is write one to clear.                                                                 |
| 26:24 | TORF_PRI        | R    | 0h    | The lowest priority that caused top of receive FIFO flow control trigger since the last write to clear. This field is write 0x7 to clear.          |
| 23:16 | TX_PFC_FLOW_ACT | R    | 0h    | Receive Priority Based Flow Control Active (priority 7 down to 0).                                                                                 |
| 15:8  | RX_PFC_FLOW_ACT | R    | 0h    | Transmit Priority Based Flow Control Active (priority 7 down to 0).                                                                                |
| 7     | RESERVED        | NONE | 0h    | Reserved                                                                                                                                           |
| 6     | EXT_TX_FLOW_EN  | R    | 0h    | External Transmit Flow Control Enable - This is the value of the EXT_TX_FLOW_EN input bit.                                                         |
| 5     | EXT_RX_FLOW_EN  | R    | 0h    | External Receive Flow Control Enable - This is the value of the EXT_RX_FLOW_EN input bit.                                                          |

**Table 5-472. CPSW\_NC\_ETH\_MAC\_PN\_MAC\_STATUS\_REG\_K Register Field Descriptions (continued)**

| Bit | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                             |
|-----|----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | EXT_GIG        | R    | 0h    | External GIG - This is the value of the EXT_GIG input bit.                                                                                                                                                                                                                                                              |
| 3   | EXT_FULLDUPLEX | R    | 0h    | External Fullduplex - This is the value of the EXT_FULLDUPLEX input bit.                                                                                                                                                                                                                                                |
| 2   | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                |
| 1   | RX_FLOW_ACT    | R    | 0h    | Receive Flow Control Active - When asserted, indicates that receive flow control is enabled and triggered.                                                                                                                                                                                                              |
| 0   | TX_FLOW_ACT    | R    | 0h    | Transmit Flow Control Active - When asserted, this bit indicates that the pause time period is being observed for a received pause frame. No new transmissions will begin while this bit is asserted except for the transmission of pause frames. Any transmission in progress when this bit is asserted will complete. |

### 5.1.2.158 CPSW\_NC\_ETH\_MAC\_PN\_MAC\_SOFT\_RESET\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_MAC\_SOFT\_RESET\_REG\_K Register (Offset = 22338h) [reset = 0h]

Enet Port N Mac Soft Reset

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-473. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2338h + formula |

**Figure 5-158. CPSW\_NC\_ETH\_MAC\_PN\_MAC\_SOFT\_RESET\_REG\_K Name Register**

|          |    |    |    |    |    |    |            |
|----------|----|----|----|----|----|----|------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24         |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16         |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8          |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0          |
| RESERVED |    |    |    |    |    |    | SOFT_RESET |
| NONE     |    |    |    |    |    |    | R/W        |
| 0h       |    |    |    |    |    |    | 0h         |

**Table 5-475. CPSW\_NC\_ETH\_MAC\_PN\_MAC\_SOFT\_RESET\_REG\_K Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description    |
|------|------------|------|-------|----------------|
| 31:1 | RESERVED   | NONE | 0h    | Reserved       |
| 0    | SOFT_RESET | R/W  | 0h    | Software reset |

### 5.1.2.159 CPSW\_NC\_ETH\_MAC\_PN\_MAC\_BOFFTEST\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_MAC\_BOFFTEST\_REG\_K Register (Offset = 2233Ch) [reset = 0h]

Enet Port N Mac Backoff Test

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-476. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 233Ch + formula |

**Figure 5-159. CPSW\_NC\_ETH\_MAC\_PN\_MAC\_BOFFTEST\_REG\_K Name Register**

|            |         |    |    |          |    |            |    |
|------------|---------|----|----|----------|----|------------|----|
| 31         | 30      | 29 | 28 | 27       | 26 | 25         | 24 |
| RESERVED   | PACEVAL |    |    |          |    | RNDNUM     |    |
| NONE       | R/W     |    |    |          |    | R/W        |    |
| 0h         | 0h      |    |    |          |    | 0h         |    |
| 23         | 22      | 21 | 20 | 19       | 18 | 17         | 16 |
| RNDNUM     |         |    |    |          |    |            |    |
| R/W        |         |    |    |          |    |            |    |
| 0h         |         |    |    |          |    |            |    |
| 15         | 14      | 13 | 12 | 11       | 10 | 9          | 8  |
| COLL_COUNT |         |    |    | RESERVED |    | TX_BACKOFF |    |
| R          |         |    |    | NONE     |    | R          |    |
| 0h         |         |    |    | 0h       |    | 0h         |    |
| 7          | 6       | 5  | 4  | 3        | 2  | 1          | 0  |
| TX_BACKOFF |         |    |    |          |    |            |    |
| R          |         |    |    |          |    |            |    |
| 0h         |         |    |    |          |    |            |    |

**Table 5-478. CPSW\_NC\_ETH\_MAC\_PN\_MAC\_BOFFTEST\_REG\_K Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | RESERVED   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 30:26 | PACEVAL    | R/W  | 0h    | Pacing Current Value - A non-zero value in this field indicates that transmit pacing is active. A transmit frame collision or deferral causes paceval to loaded with decimal 31, good frame transmissions (with no collisions or deferrals) cause paceval to be decremented down to zero. When paceval is nonzero, the transmitter delays 4 IPGs between new frame transmissions after each successfully transmitted frame that had no deferrals or collisions. Transmit pacing helps reduce capture effects improving overall network bandwidth. |
| 25:16 | RNDNUM     | R/W  | 0h    | Backoff Random Number Generator - This field allows the Backoff Random Number Generator to be read (or written in test mode only). This field can be written only when pn_mtest has previously been set. Reading this field returns the generator's current value. The value is reset to zero and begins counting on the clock after the de-assertion of reset.                                                                                                                                                                                   |
| 15:12 | COLL_COUNT | R    | 0h    | Collision Count - The number of collisions the current frame has experienced.                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 11:10 | RESERVED   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

**Table 5-478. CPSW\_NC\_ETH\_MAC\_PN\_MAC\_BOFFTEST\_REG\_K Register Field Descriptions  
(continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                           |
|-----|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9:0 | TX_BACKOFF | R    | 0h    | Backoff Count - This field allows the current value of the backoff counter to be observed for test purposes. This field is loaded automatically according to the backoff algorithm, and is decremented by one for each slot time after the collision. |



### 5.1.2.160 CPSW\_NC\_ETH\_MAC\_PN\_MAC\_RX\_PAUSETIMER\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_MAC\_RX\_PAUSETIMER\_REG\_K Register (Offset = 22340h) [reset = 0h]

Enet Port N 802.3 Receive Pause Timer

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-479. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2340h + formula |

**Figure 5-160. CPSW\_NC\_ETH\_MAC\_PN\_MAC\_RX\_PAUSETIMER\_REG\_K Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RX_PAUSETIMER |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RX_PAUSETIMER |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 5-481. CPSW\_NC\_ETH\_MAC\_PN\_MAC\_RX\_PAUSETIMER\_REG\_K Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|---------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED      | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 15:0  | RX_PAUSETIMER | R/W  | 0h    | RX Pause Timer Value - This field allows the contents of the receive pause timer to be observed (and written in test mode). The receive pause timer is loaded with 0xFF00 when the Enet port sends an outgoing pause frame (with pause time of 0xFFFF). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.3 Based flow control and is not used for 802.1Qbb Priority Based Flow Control (PFC). |

### 5.1.2.161 CPSW\_NC\_ETH\_MAC\_PN\_MAC\_RXN\_PAUSETIMER\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_MAC\_RXN\_PAUSETIMER\_REG\_K Register (Offset = 22350h) [reset = 0h]

Enet Port N PFC Priority 0 Rx Pause Timer

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-482. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2350h + formula |

**Figure 5-161. CPSW\_NC\_ETH\_MAC\_PN\_MAC\_RXN\_PAUSETIMER\_REG\_K Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RX0_PAUSETIMER |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RX0_PAUSETIMER |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-484. CPSW\_NC\_ETH\_MAC\_PN\_MAC\_RXN\_PAUSETIMER\_REG\_K Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 15:0  | RX0_PAUSETIMER | R/W  | 0h    | Rx N Pause Timer Value - This field allows the contents of the receive pause timer to be observed (and written in test mode). The receive pause timer is loaded with 0xFF00 when the Enet port sends an outgoing pause frame (with pause time of 0xFFFF). The receive pause timer is decremented at slot time intervals. If the receive pause timer decrements to zero, then another outgoing pause frame will be sent and the load/decrement process will be repeated. This register is for 802.1qbb Priority Based flow control (PFC) |

### 5.1.2.162 CPSW\_NC\_ETH\_MAC\_PN\_MAC\_TX\_PAUSETIMER\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_MAC\_TX\_PAUSETIMER\_REG\_K Register (Offset = 22370h) [reset = 0h]

Enet Port N 802.3 Tx Pause Timer

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-485. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2370h + formula |

**Figure 5-162. CPSW\_NC\_ETH\_MAC\_PN\_MAC\_TX\_PAUSETIMER\_REG\_K Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED      |    |    |    |    |    |    |    |
| NONE          |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TX_PAUSETIMER |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TX_PAUSETIMER |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 5-487. CPSW\_NC\_ETH\_MAC\_PN\_MAC\_TX\_PAUSETIMER\_REG\_K Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|---------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED      | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 15:0  | TX_PAUSETIMER | R/W  | 0h    | 802.3 Tx Pause Timer Value - This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.3 Based flow control and is not used for 802.1qbb Priority Based Flow Control (PFC). |

### 5.1.2.163 CPSW\_NC\_ETH\_MAC\_PN\_MAC\_TX0\_PAUSETIMER\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_MAC\_TX0\_PAUSETIMER\_REG\_K Register (Offset = 22380h) [reset = 0h]

Enet Port N PFC Priority 0 Tx Pause Timer

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-488. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 2380h + formula |

**Figure 5-163. CPSW\_NC\_ETH\_MAC\_PN\_MAC\_TX0\_PAUSETIMER\_REG\_K Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TX0_PAUSETIMER |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TX0_PAUSETIMER |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-490. CPSW\_NC\_ETH\_MAC\_PN\_MAC\_TX0\_PAUSETIMER\_REG\_K Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                             |
| 15:0  | TX0_PAUSETIMER | R/W  | 0h    | PFC Tx N Pause Timer Value - This field allows the contents of the transmit pause timer to be observed (and written in test mode). The transmit pause timer is loaded by a received (incoming) pause frame, and then decremented, at slottime intervals, down to zero at which time Ethernet Port transmit frames are again enabled. This register is for 802.1qbb Priority Based flow control (PFC) |

### 5.1.2.164 CPSW\_NC\_ETH\_MAC\_PN\_MAC\_EMCONTROL\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_MAC\_EMCONTROL\_REG\_K Register (Offset = 223A0h) [reset = 0h]

Enet Port N Emulation Control

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-491. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 23A0h + formula |

**Figure 5-164. CPSW\_NC\_ETH\_MAC\_PN\_MAC\_EMCONTROL\_REG\_K Name Register**

|          |    |    |    |    |    |      |      |
|----------|----|----|----|----|----|------|------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25   | 24   |
| RESERVED |    |    |    |    |    |      |      |
| NONE     |    |    |    |    |    |      |      |
| 0h       |    |    |    |    |    |      |      |
| 23       | 22 | 21 | 20 | 19 | 18 | 17   | 16   |
| RESERVED |    |    |    |    |    |      |      |
| NONE     |    |    |    |    |    |      |      |
| 0h       |    |    |    |    |    |      |      |
| 15       | 14 | 13 | 12 | 11 | 10 | 9    | 8    |
| RESERVED |    |    |    |    |    |      |      |
| NONE     |    |    |    |    |    |      |      |
| 0h       |    |    |    |    |    |      |      |
| 7        | 6  | 5  | 4  | 3  | 2  | 1    | 0    |
| RESERVED |    |    |    |    |    | SOFT | FREE |
| NONE     |    |    |    |    |    | R/W  | R/W  |
| 0h       |    |    |    |    |    | 0h   | 0h   |

**Table 5-493. CPSW\_NC\_ETH\_MAC\_PN\_MAC\_EMCONTROL\_REG\_K Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description        |
|------|----------|------|-------|--------------------|
| 31:2 | RESERVED | NONE | 0h    | Reserved           |
| 1    | SOFT     | R/W  | 0h    | Emulation Soft Bit |
| 0    | FREE     | R/W  | 0h    | Emulation Free Bit |

### 5.1.2.165 CPSW\_NC\_ETH\_MAC\_PN\_MAC\_TX\_GAP\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_MAC\_TX\_GAP\_REG\_K Register (Offset = 223A4h) [reset = Ch]

Enet Port N Tx Inter Packet Gap

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-494. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 23A4h + formula |

**Figure 5-165. CPSW\_NC\_ETH\_MAC\_PN\_MAC\_TX\_GAP\_REG\_K Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TX_GAP   |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| Ch       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TX_GAP   |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| Ch       |    |    |    |    |    |    |    |

**Table 5-496. CPSW\_NC\_ETH\_MAC\_PN\_MAC\_TX\_GAP\_REG\_K Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                               |
|-------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                  |
| 15:0  | TX_GAP   | R/W  | Ch    | Transmit Inter-Packet Gap -<br>GMII modes - This is the default gap value and only bits 8:0 are used. This can be increased from 12 to increase the gap between packets.<br>XGMII mode - In 10 gigabit mode this is the short gap rate and should be changed to 5000 (0x1388) to get approximately 200ppm faster when short gap is triggered and enabled. |

### 5.1.2.166 CPSW\_NC\_ETH\_MAC\_PN\_MAC\_PORT\_CONFIG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_MAC\_PORT\_CONFIG\_K Register (Offset = 223A8h) [reset = 2h]

Enet Port N Port Configuration

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-497. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 23A8h + formula |

**Figure 5-166. CPSW\_NC\_ETH\_MAC\_PN\_MAC\_PORT\_CONFIG\_K Name Register**

|                  |    |    |    |    |    |     |       |
|------------------|----|----|----|----|----|-----|-------|
| 31               | 30 | 29 | 28 | 27 | 26 | 25  | 24    |
| RESERVED         |    |    |    |    |    |     |       |
| NONE             |    |    |    |    |    |     |       |
| 0h               |    |    |    |    |    |     |       |
| 23               | 22 | 21 | 20 | 19 | 18 | 17  | 16    |
| RESERVED         |    |    |    |    |    |     |       |
| NONE             |    |    |    |    |    |     |       |
| 0h               |    |    |    |    |    |     |       |
| 15               | 14 | 13 | 12 | 11 | 10 | 9   | 8     |
| RESERVED         |    |    |    |    |    | IET | XGMII |
| NONE             |    |    |    |    |    | R   | R     |
| 0h               |    |    |    |    |    | 0h  | 0h    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1   | 0     |
| INTERVLAN_ROUTES |    |    |    |    |    |     |       |
| R                |    |    |    |    |    |     |       |
| 2h               |    |    |    |    |    |     |       |

**Table 5-499. CPSW\_NC\_ETH\_MAC\_PN\_MAC\_PORT\_CONFIG\_K Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                    |
|-------|------------------|------|-------|----------------------------------------------------------------|
| 31:10 | RESERVED         | NONE | 0h    | Reserved                                                       |
| 9     | IET              | R    | 0h    | IET support                                                    |
| 8     | XGMII            | R    | 0h    | No XGMII support on this port                                  |
| 7:0   | INTERVLAN_ROUTES | R    | 2h    | The number of InterVLAN routes supported on this port (egress) |

### 5.1.2.167 CPSW\_NC\_ETH\_MAC\_PN\_INTERVLAN\_OPX\_POINTER\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_INTERVLAN\_OPX\_POINTER\_REG\_K Register (Offset = 223ACh) [reset = 0h]

Enet Port N Tx Egress InterVLAN Operation Pointer

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-500. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 23ACh + formula |

**Figure 5-167. CPSW\_NC\_ETH\_MAC\_PN\_INTERVLAN\_OPX\_POINTER\_REG\_K Name Register**

|          |    |    |    |    |    |         |    |
|----------|----|----|----|----|----|---------|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25      | 24 |
| RESERVED |    |    |    |    |    |         |    |
| NONE     |    |    |    |    |    |         |    |
| 0h       |    |    |    |    |    |         |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17      | 16 |
| RESERVED |    |    |    |    |    |         |    |
| NONE     |    |    |    |    |    |         |    |
| 0h       |    |    |    |    |    |         |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9       | 8  |
| RESERVED |    |    |    |    |    |         |    |
| NONE     |    |    |    |    |    |         |    |
| 0h       |    |    |    |    |    |         |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1       | 0  |
| RESERVED |    |    |    |    |    | POINTER |    |
| NONE     |    |    |    |    |    | R/W     |    |
| 0h       |    |    |    |    |    | 0h      |    |

**Table 5-502. CPSW\_NC\_ETH\_MAC\_PN\_INTERVLAN\_OPX\_POINTER\_REG\_K Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                              |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                 |
| 1:0  | POINTER  | R/W  | 0h    | InterVLAN location pointer - This field points to the InterVLAN location that will be read/written by accesses to Enet_Pn_InterVLANx_A/B/C (the InterVLAN locations are accessed by a mailbox). Valid pointer locations are 1 to x (where x is the number of locations - pointer location zero is unused). For example, if configured with 2 intervlan routes then only the values of 1 and 2 are valid. |



### 5.1.2.168 CPSW\_NC\_ETH\_MAC\_PN\_INTERVLAN\_OPX\_A\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_INTERVLAN\_OPX\_A\_REG\_K Register (Offset = 223B0h) [reset = 0h]

Enet Port N Tx Egress InterVLAN A

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-503. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 23B0h + formula |

**Figure 5-168. CPSW\_NC\_ETH\_MAC\_PN\_INTERVLAN\_OPX\_A\_REG\_K Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DA_23_16 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DA_31_24 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DA_39_32 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DA_47_40 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-505. CPSW\_NC\_ETH\_MAC\_PN\_INTERVLAN\_OPX\_A\_REG\_K Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                    |
|-------|----------|------|-------|--------------------------------|
| 31:24 | DA_23_16 | R/W  | 0h    | Destination Address bits 23:16 |
| 23:16 | DA_31_24 | R/W  | 0h    | Destination Address bits 31:24 |
| 15:8  | DA_39_32 | R/W  | 0h    | Destination Address bits 39:32 |
| 7:0   | DA_47_40 | R/W  | 0h    | Destination Address bits 47:40 |

### 5.1.2.169 CPSW\_NC\_ETH\_MAC\_PN\_INTERVLAN\_OPX\_B\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_INTERVLAN\_OPX\_B\_REG\_K Register (Offset = 223B4h) [reset = 0h]

Enet Port N Tx Egress InterVLAN B

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-506. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 23B4h + formula |

**Figure 5-169. CPSW\_NC\_ETH\_MAC\_PN\_INTERVLAN\_OPX\_B\_REG\_K Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SA_39_32 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SA_47_40 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DA_7_0   |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DA_15_8  |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-508. CPSW\_NC\_ETH\_MAC\_PN\_INTERVLAN\_OPX\_B\_REG\_K Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                   |
|-------|----------|------|-------|-------------------------------|
| 31:24 | SA_39_32 | R/W  | 0h    | Source Address bits 39:32     |
| 23:16 | SA_47_40 | R/W  | 0h    | Source Address bits 47:40     |
| 15:8  | DA_7_0   | R/W  | 0h    | Destination Address bits 7:0  |
| 7:0   | DA_15_8  | R/W  | 0h    | Destination Address bits 15:8 |

### 5.1.2.170 CPSW\_NC\_ETH\_MAC\_PN\_INTERVLAN\_OPX\_C\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_INTERVLAN\_OPX\_C\_REG\_K Register (Offset = 223B8h) [reset = 0h]

Enet Port N Tx Egress InterVLAN C

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-509. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 23B8h + formula |

**Figure 5-170. CPSW\_NC\_ETH\_MAC\_PN\_INTERVLAN\_OPX\_C\_REG\_K Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SA_7_0   |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SA_15_8  |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SA_23_16 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SA_31_24 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-511. CPSW\_NC\_ETH\_MAC\_PN\_INTERVLAN\_OPX\_C\_REG\_K Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description               |
|-------|----------|------|-------|---------------------------|
| 31:24 | SA_7_0   | R/W  | 0h    | Source Address bits 7:0   |
| 23:16 | SA_15_8  | R/W  | 0h    | Source Address bits 15:8  |
| 15:8  | SA_23_16 | R/W  | 0h    | Source Address bits 23:16 |
| 7:0   | SA_31_24 | R/W  | 0h    | Source Address bits 31:24 |

### 5.1.2.171 CPSW\_NC\_ETH\_MAC\_PN\_INTERVLAN\_OPX\_D\_REG\_K Register

#### 1 CPSW\_NC\_ETH\_MAC\_PN\_INTERVLAN\_OPX\_D\_REG\_K Register (Offset = 223BCh) [reset = 0h]

Enet Port N Tx Egress InterVLAN D

Return to [Summary Table](#)

Offset = Base + (k \* 1000h); where k = 0 to 1d

**Table 5-512. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5282 23BCh + formula |

**Figure 5-171. CPSW\_NC\_ETH\_MAC\_PN\_INTERVLAN\_OPX\_D\_REG\_K Name Register**

|               |                            |               |             |     |    |    |    |
|---------------|----------------------------|---------------|-------------|-----|----|----|----|
| 31            | 30                         | 29            | 28          | 27  | 26 | 25 | 24 |
| RESERVED      |                            |               |             |     |    |    |    |
| NONE          |                            |               |             |     |    |    |    |
| 0h            |                            |               |             |     |    |    |    |
| 23            | 22                         | 21            | 20          | 19  | 18 | 17 | 16 |
| RESERVED      |                            |               |             |     |    |    |    |
| NONE          |                            |               |             |     |    |    |    |
| 0h            |                            |               |             |     |    |    |    |
| 15            | 14                         | 13            | 12          | 11  | 10 | 9  | 8  |
| DECREMENT_TTL | DEST_FORCE_UNTAGGED_EGRESS | REPLACE_DA_SA | REPLACE_VID | VID |    |    |    |
| R/W           | R/W                        | R/W           | R/W         | R/W |    |    |    |
| 0h            | 0h                         | 0h            | 0h          | 0h  |    |    |    |
| 7             | 6                          | 5             | 4           | 3   | 2  | 1  | 0  |
| VID           |                            |               |             |     |    |    |    |
| R/W           |                            |               |             |     |    |    |    |
| 0h            |                            |               |             |     |    |    |    |

**Table 5-514. CPSW\_NC\_ETH\_MAC\_PN\_INTERVLAN\_OPX\_D\_REG\_K Register Field Descriptions**

| Bit   | Field                      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|----------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED                   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 15    | DECREMENT_TTL              | R/W  | 0h    | Decrement Time To Live - When set, the Time To Live (TTL) field in the header is decremented.<br>IPV4 - Decrement the TTL byte and update the Header Checksum.<br>IPV6 - Decrement the Hop Limit.<br>note: When this bit is set, the ALE should be configured to send any IPv4/6 packet with a zero or one TTL field to the host with the ALE egress operation ttl_check bit. When this bit is cleared the TTL/Hop Limit fields are not checked or modified. |
| 14    | DEST_FORCE_UNTAGGED_EGRESS | R/W  | 0h    | Destination VLAN Force Untagged Egress - When set, this bit indicates that the VLAN should be removed on egress for the routed packet. The replace_vid bit should be set for this bit to be used, otherwise force untagged egress comes from the address lookup engine.                                                                                                                                                                                      |
| 13    | REPLACE_DA_SA              | R/W  | 0h    | Replace Destination Address and Source Address - When set this bit indicates that the routed packet destination address should be replaced by da[47:0] and the source address should be replaced by sa[47:0].                                                                                                                                                                                                                                                |
| 12    | REPLACE_VID                | R/W  | 0h    | Replace VLAN ID - When set this bit indicates that the VLAN ID should be replaced for the routed packet.                                                                                                                                                                                                                                                                                                                                                     |

**Table 5-514. CPSW\_NC\_ETH\_MAC\_PN\_INTERVLAN\_OPX\_D\_REG\_K Register Field Descriptions  
(continued)**

| Bit  | Field | Type | Reset | Description |
|------|-------|------|-------|-------------|
| 11:0 | VID   | R/W  | 0h    | VLAN ID     |

### 5.1.2.172 CPSW\_NC\_EST\_FETCH\_LOC Register

#### 1 CPSW\_NC\_EST\_FETCH\_LOC Register (Offset = 32000h) [reset = 0h]

The Revision Register contains the ID and revision information.

Return to [Summary Table](#)

**Table 5-515. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 2000h       |

**Figure 5-172. CPSW\_NC\_EST\_FETCH\_LOC Name Register**

|          |    |    |    |     |    |    |    |
|----------|----|----|----|-----|----|----|----|
| 31       | 30 | 29 | 28 | 27  | 26 | 25 | 24 |
| RESERVED |    |    |    |     |    |    |    |
| NONE     |    |    |    |     |    |    |    |
| 0h       |    |    |    |     |    |    |    |
| 23       | 22 | 21 | 20 | 19  | 18 | 17 | 16 |
| RESERVED |    |    |    | LOC |    |    |    |
| NONE     |    |    |    | R/W |    |    |    |
| 0h       |    |    |    | 0h  |    |    |    |
| 15       | 14 | 13 | 12 | 11  | 10 | 9  | 8  |
| LOC      |    |    |    |     |    |    |    |
| R/W      |    |    |    |     |    |    |    |
| 0h       |    |    |    |     |    |    |    |
| 7        | 6  | 5  | 4  | 3   | 2  | 1  | 0  |
| LOC      |    |    |    |     |    |    |    |
| R/W      |    |    |    |     |    |    |    |
| 0h       |    |    |    |     |    |    |    |

**Table 5-517. CPSW\_NC\_EST\_FETCH\_LOC Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description  |
|-------|----------|------|-------|--------------|
| 31:22 | RESERVED | NONE | 0h    | Reserved     |
| 21:0  | LOC      | R/W  | 0h    | RAM Location |

### 5.1.2.173 CPSW\_NC\_CPDMA\_REGS\_FH\_IDVER\_REG Register

#### 1 CPSW\_NC\_CPDMA\_REGS\_FH\_IDVER\_REG Register (Offset = 34000h) [reset = 18010Ah]

CPDMA FHost IDVER

Return to [Summary Table](#)

**Table 5-518. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4000h       |

**Figure 5-173. CPSW\_NC\_CPDMA\_REGS\_FH\_IDVER\_REG Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FH_IDVER |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 18010Ah  |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FH_IDVER |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 18010Ah  |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FH_IDVER |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 18010Ah  |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FH_IDVER |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 18010Ah  |    |    |    |    |    |    |    |

**Table 5-520. CPSW\_NC\_CPDMA\_REGS\_FH\_IDVER\_REG Register Field Descriptions**

| Bit  | Field    | Type | Reset   | Description       |
|------|----------|------|---------|-------------------|
| 31:0 | FH_IDVER | R    | 18010Ah | CPDMA FHost IDVER |

### 5.1.2.174 CPSW\_NC\_CPDMA\_REGS\_FH\_CONTROL\_REG Register

#### 1 CPSW\_NC\_CPDMA\_REGS\_FH\_CONTROL\_REG Register (Offset = 34004h) [reset = 0h]

CPDMA FHost Control Register

Return to [Summary Table](#)

**Table 5-521. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4004h       |

**Figure 5-174. CPSW\_NC\_CPDMA\_REGS\_FH\_CONTROL\_REG Name Register**

|          |    |    |    |    |    |    |       |
|----------|----|----|----|----|----|----|-------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24    |
| RESERVED |    |    |    |    |    |    |       |
| NONE     |    |    |    |    |    |    |       |
| 0h       |    |    |    |    |    |    |       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16    |
| RESERVED |    |    |    |    |    |    |       |
| NONE     |    |    |    |    |    |    |       |
| 0h       |    |    |    |    |    |    |       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8     |
| RESERVED |    |    |    |    |    |    |       |
| NONE     |    |    |    |    |    |    |       |
| 0h       |    |    |    |    |    |    |       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0     |
| RESERVED |    |    |    |    |    |    | FH_EN |
| NONE     |    |    |    |    |    |    | R/W   |
| 0h       |    |    |    |    |    |    | 0h    |

**Table 5-523. CPSW\_NC\_CPDMA\_REGS\_FH\_CONTROL\_REG Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                 |
|------|----------|------|-------|---------------------------------------------|
| 31:1 | RESERVED | NONE | 0h    | Reserved                                    |
| 0    | FH_EN    | R/W  | 0h    | FHost Enable<br>0 - Disabled<br>1 - Enabled |



### 5.1.2.175 CPSW\_NC\_CPDMA\_REGS\_FH\_TEARDOWN\_REG Register

#### 1 CPSW\_NC\_CPDMA\_REGS\_FH\_TEARDOWN\_REG Register (Offset = 34008h) [reset = 0h]

CPDMA FHost Teardown Register

Return to [Summary Table](#)

**Table 5-524. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4008h       |

**Figure 5-175. CPSW\_NC\_CPDMA\_REGS\_FH\_TEARDOWN\_REG Name Register**

|          |    |    |    |    |           |    |    |
|----------|----|----|----|----|-----------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26        | 25 | 24 |
| RESERVED |    |    |    |    |           |    |    |
| NONE     |    |    |    |    |           |    |    |
| 0h       |    |    |    |    |           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18        | 17 | 16 |
| RESERVED |    |    |    |    |           |    |    |
| NONE     |    |    |    |    |           |    |    |
| 0h       |    |    |    |    |           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10        | 9  | 8  |
| RESERVED |    |    |    |    |           |    |    |
| NONE     |    |    |    |    |           |    |    |
| 0h       |    |    |    |    |           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2         | 1  | 0  |
| RESERVED |    |    |    |    | FH_TDN_CH |    |    |
| NONE     |    |    |    |    | R/W       |    |    |
| 0h       |    |    |    |    | 0h        |    |    |

**Table 5-526. CPSW\_NC\_CPDMA\_REGS\_FH\_TEARDOWN\_REG Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                           |
|------|-----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED  | NONE | 0h    | Reserved                                                                                                                                                                                                                              |
| 2:0  | FH_TDN_CH | R/W  | 0h    | CPDMA FHost Teardown Channel - FHost channel teardown is commanded by writing the encoded value of the channel to be torn down. The teardown register is read as zero.<br>000 - teardown channel 0<br>...<br>111 - teardown channel 7 |

### 5.1.2.176 CPSW\_NC\_CPDMA\_REGS\_FH\_CONTROL2\_REG Register

#### 1 CPSW\_NC\_CPDMA\_REGS\_FH\_CONTROL2\_REG Register (Offset = 3400Ch) [reset = 0h]

CPDMA FHost Control Two Register

Return to [Summary Table](#)

**Table 5-527. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 400Ch       |

**Figure 5-176. CPSW\_NC\_CPDMA\_REGS\_FH\_CONTROL2\_REG Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FH_EOQ_INT |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-529. CPSW\_NC\_CPDMA\_REGS\_FH\_CONTROL2\_REG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                        |
|------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED   | NONE | 0h    | Reserved                                                                                                                                                                                                           |
| 7:0  | FH_EOQ_INT | R/W  | 0h    | FHost Interrupt on EOQ only - When set, a corresponding channel issues an FH_PEND[7:0] interrupt only on end of queue (EOQ). When clear, a corresponding channel issues an interrupt at every end of packet (EOP). |

### 5.1.2.177 CPSW\_NC\_CPDMA\_REGS\_TH\_IDVER\_REG Register

#### 1 CPSW\_NC\_CPDMA\_REGS\_TH\_IDVER\_REG Register (Offset = 34010h) [reset = 18010Ah]

CPDMA THost IDVER

Return to [Summary Table](#)

**Table 5-530. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4010h       |

**Figure 5-177. CPSW\_NC\_CPDMA\_REGS\_TH\_IDVER\_REG Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TH_IDVER |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 18010Ah  |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TH_IDVER |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 18010Ah  |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TH_IDVER |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 18010Ah  |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH_IDVER |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 18010Ah  |    |    |    |    |    |    |    |

**Table 5-532. CPSW\_NC\_CPDMA\_REGS\_TH\_IDVER\_REG Register Field Descriptions**

| Bit  | Field    | Type | Reset   | Description       |
|------|----------|------|---------|-------------------|
| 31:0 | TH_IDVER | R    | 18010Ah | CPDMA THost IDVER |

### 5.1.2.178 CPSW\_NC\_CPDMA\_REGS\_TH\_CONTROL\_REG Register

#### 1 CPSW\_NC\_CPDMA\_REGS\_TH\_CONTROL\_REG Register (Offset = 34014h) [reset = 0h]

CPDMA THost Control Register

Return to [Summary Table](#)

**Table 5-533. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4014h       |

**Figure 5-178. CPSW\_NC\_CPDMA\_REGS\_TH\_CONTROL\_REG Name Register**

|          |    |    |    |    |    |    |       |
|----------|----|----|----|----|----|----|-------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24    |
| RESERVED |    |    |    |    |    |    |       |
| NONE     |    |    |    |    |    |    |       |
| 0h       |    |    |    |    |    |    |       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16    |
| RESERVED |    |    |    |    |    |    |       |
| NONE     |    |    |    |    |    |    |       |
| 0h       |    |    |    |    |    |    |       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8     |
| RESERVED |    |    |    |    |    |    |       |
| NONE     |    |    |    |    |    |    |       |
| 0h       |    |    |    |    |    |    |       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0     |
| RESERVED |    |    |    |    |    |    | TH_EN |
| NONE     |    |    |    |    |    |    | R/W   |
| 0h       |    |    |    |    |    |    | 0h    |

**Table 5-535. CPSW\_NC\_CPDMA\_REGS\_TH\_CONTROL\_REG Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                     |
|------|----------|------|-------|-------------------------------------------------|
| 31:1 | RESERVED | NONE | 0h    | Reserved                                        |
| 0    | TH_EN    | R/W  | 0h    | THost DMA Enable<br>0 - Disabled<br>1 - Enabled |

### 5.1.2.179 CPSW\_NC\_CPDMA\_REGS\_TH\_TEARDOWN\_REG Register

#### 1 CPSW\_NC\_CPDMA\_REGS\_TH\_TEARDOWN\_REG Register (Offset = 34018h) [reset = 0h]

CPDMA THost Teardown Register

Return to [Summary Table](#)

**Table 5-536. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4018h       |

**Figure 5-179. CPSW\_NC\_CPDMA\_REGS\_TH\_TEARDOWN\_REG Name Register**

|          |    |    |    |    |           |    |    |
|----------|----|----|----|----|-----------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26        | 25 | 24 |
| RESERVED |    |    |    |    |           |    |    |
| NONE     |    |    |    |    |           |    |    |
| 0h       |    |    |    |    |           |    |    |
| 23       | 22 | 21 | 20 | 19 | 18        | 17 | 16 |
| RESERVED |    |    |    |    |           |    |    |
| NONE     |    |    |    |    |           |    |    |
| 0h       |    |    |    |    |           |    |    |
| 15       | 14 | 13 | 12 | 11 | 10        | 9  | 8  |
| RESERVED |    |    |    |    |           |    |    |
| NONE     |    |    |    |    |           |    |    |
| 0h       |    |    |    |    |           |    |    |
| 7        | 6  | 5  | 4  | 3  | 2         | 1  | 0  |
| RESERVED |    |    |    |    | TH_TDN_CH |    |    |
| NONE     |    |    |    |    | R/W       |    |    |
| 0h       |    |    |    |    | 0h        |    |    |

**Table 5-538. CPSW\_NC\_CPDMA\_REGS\_TH\_TEARDOWN\_REG Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                     |
|------|-----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED  | NONE | 0h    | Reserved                                                                                                                                                                                                                        |
| 2:0  | TH_TDN_CH | R/W  | 0h    | THost Teardown Channel - THost channel teardown is commanded by writing the encoded value of the channel to be torn down. The teardown register is read as zero.<br>000 - teardown channel 0<br>...<br>111 - teardown channel 7 |

### 5.1.2.180 CPSW\_NC\_CPDMA\_REGS\_SOFT\_RESET\_REG Register

#### 1 CPSW\_NC\_CPDMA\_REGS\_SOFT\_RESET\_REG Register (Offset = 3401Ch) [reset = 0h]

CPDMA Soft Reset Register

Return to [Summary Table](#)

**Table 5-539. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 401Ch       |

**Figure 5-180. CPSW\_NC\_CPDMA\_REGS\_SOFT\_RESET\_REG Name Register**

|          |    |    |    |    |    |    |            |
|----------|----|----|----|----|----|----|------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24         |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16         |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8          |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0          |
| RESERVED |    |    |    |    |    |    | SOFT_RESET |
| NONE     |    |    |    |    |    |    | R/W        |
| 0h       |    |    |    |    |    |    | 0h         |

**Table 5-541. CPSW\_NC\_CPDMA\_REGS\_SOFT\_RESET\_REG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                        |
|------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                           |
| 0    | SOFT_RESET | R/W  | 0h    | Software reset - Writing a one to this bit causes the entire CPSW logic to be reset. Software reset occurs when the DMA Controllers are in an idle state to avoid locking up the VBUSP bus. After writing a one to this bit, it may be polled to determine if the reset has occurred. If a one is read, the reset has not yet occurred. If a zero is read then reset has occurred. |

### 5.1.2.181 CPSW\_NC\_CPDMA\_REGS\_CONTROL\_REG Register

#### 1 CPSW\_NC\_CPDMA\_REGS\_CONTROL\_REG Register (Offset = 34020h) [reset = 0h]

CPDMA Control Register

Return to [Summary Table](#)

**Table 5-542. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4020h       |

**Figure 5-181. CPSW\_NC\_CPDMA\_REGS\_CONTROL\_REG Name Register**

|                    |             |                   |        |          |                     |                  |                  |
|--------------------|-------------|-------------------|--------|----------|---------------------|------------------|------------------|
| 31                 | 30          | 29                | 28     | 27       | 26                  | 25               | 24               |
| RESERVED           |             |                   |        |          |                     |                  |                  |
| NONE               |             |                   |        |          |                     |                  |                  |
| 0h                 |             |                   |        |          |                     |                  |                  |
| 23                 | 22          | 21                | 20     | 19       | 18                  | 17               | 16               |
| RESERVED           |             |                   |        |          |                     |                  |                  |
| NONE               |             |                   |        |          |                     |                  |                  |
| 0h                 |             |                   |        |          |                     |                  |                  |
| 15                 | 14          | 13                | 12     | 11       | 10                  | 9                | 8                |
| RESERVED           |             |                   |        |          |                     |                  | FH_OWNERSH<br>IP |
| NONE               |             |                   |        |          |                     |                  | R/W              |
| 0h                 |             |                   |        |          |                     |                  | 0h               |
| 7                  | 6           | 5                 | 4      | 3        | 2                   | 1                | 0                |
| TH_CH_OVER<br>RIDE | TH_TS_ENCAP | TH_VLAN_ENC<br>AP | TH_CEF | CMD_IDLE | TH_OFFLEN_B<br>LOCK | TH_OWNERSH<br>IP | FH_PTYPE         |
| R/W                | R/W         | R/W               | R/W    | R/W      | R/W                 | R/W              | R/W              |
| 0h                 | 0h          | 0h                | 0h     | 0h       | 0h                  | 0h               | 0h               |

**Table 5-544. CPSW\_NC\_CPDMA\_REGS\_CONTROL\_REG Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|------|----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:9 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 8    | FH_OWNERSHIP   | R/W  | 0h    | CPDMA FHost Ownership Write Bit Value.<br>0 - The CPDMA writes the FHost buffer descriptor ownership bit to zero at the end of packet processing as specified in CPPI 3.0.<br>1 - The CPDMA writes the FHost buffer descriptor ownership bit to one at the end of packet processing. Users who do not use the ownership mechanism can use this mode to preclude the necessity of software having to set this bit each time the buffer descriptor is used. Software must set this bit when building the packet chain. |
| 7    | TH_CH_OVERRIDE | R/W  | 0h    | CPDMA THost Channel Classification Match Override Enable<br>0 - The THost channel is not overridden with the ALE classification match.<br>1 - The THOST channel is overridden with the lower 3-bits of the ALE classification match value (if a classification match occurred).                                                                                                                                                                                                                                      |
| 6    | TH_TS_ENCAP    | R/W  | 0h    | CPDMA THost Packet Timestamp Encapsulation<br>0 - THost packets do not contain a 64-bit timestamp<br>1 - THost packets contain a 64-bit timestamp prepended to the packet data (32-bit lword first).                                                                                                                                                                                                                                                                                                                 |
| 5    | TH_VLAN_ENCAP  | R/W  | 0h    | CPDMA THost Packet VLAN Encapsulation<br>0 - THost packets are not VLAN encapsulated<br>1 - THost packets are VLAN encapsulated                                                                                                                                                                                                                                                                                                                                                                                      |

**Table 5-544. CPSW\_NC\_CPDMA\_REGS\_CONTROL\_REG Register Field Descriptions (continued)**

| Bit | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | TH_CEF          | R/W  | 0h    | CPDMA THost Copy Error Frames Enable - Enables THost DMA overrun frames to be transferred to memory (up to the point of buffer overrun). The overrun error bit will be set in the frame EOP buffer descriptor. Overrun frame data will be filtered when thost_cef is not set. THost frames with other error bits set are not affected by this bit. This is related only to frames that overrun on the THost DMA due to buffer limitations.<br>0 - Frames containing overrun errors are filtered.<br>1 - Frames containing overrun errors are transferred to memory. |
| 3   | CMD_IDLE        | R/W  | 0h    | CPDMA Command Idle<br>0 - Idle not commanded<br>1 - Idle Commanded (read idle in CPDMA_Status register)                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 2   | TH_OFFLEN_BLOCK | R/W  | 0h    | CPDMA THost Offset/Length word write block<br>0 - Do not block the DMA writes to the THost buffer descriptor offset/buffer length word. The offset/buffer length word is written as specified in CPPI 3.0.<br>1 - Block all CPDMA DMA controller writes to the THost buffer descriptor offset/buffer length words during CPPI packet processing. When this bit is set, the CPDMA will never write the third word to any THost buffer descriptor.                                                                                                                    |
| 1   | TH_OWNERSHIP    | R/W  | 0h    | CPDMA THost Ownership Write Bit Value<br>0 - The CPDMA writes the THost buffer descriptor ownership bit to zero at the end of packet processing as specified in CPPI 3.0.<br>1 - The CPDMA writes the THost buffer descriptor ownership bit to one at the end of packet processing. Users who do not use the ownership mechanism can use this mode to preclude the necessity of software having to set this bit each time the buffer descriptor is used. Software must set this bit when building the packet chain.                                                 |
| 0   | FH_PTYPE        | R/W  | 0h    | CPDMA FHost Queue Priority Type<br>0 - The queue uses a round robin scheme to select the next channel.<br>1 - The queue uses a fixed (channel 7 highest priority) priority scheme to select the next channel.                                                                                                                                                                                                                                                                                                                                                       |



### 5.1.2.182 CPSW\_NC\_CPDMA\_REGS\_STATUS\_REG Register

#### 1 CPSW\_NC\_CPDMA\_REGS\_STATUS\_REG Register (Offset = 34024h) [reset = 80000000h]

CPDMA Status Register

Return to [Summary Table](#)

**Table 5-545. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4024h       |

**Figure 5-182. CPSW\_NC\_CPDMA\_REGS\_STATUS\_REG Name Register**

|                    |          |    |    |          |           |    |    |
|--------------------|----------|----|----|----------|-----------|----|----|
| 31                 | 30       | 29 | 28 | 27       | 26        | 25 | 24 |
| IDLE               | RESERVED |    |    |          |           |    |    |
| R                  | NONE     |    |    |          |           |    |    |
| 1h                 | 0h       |    |    |          |           |    |    |
| 23                 | 22       | 21 | 20 | 19       | 18        | 17 | 16 |
| FH_HOST_ERROR_CODE |          |    |    | RESERVED | FH_ERR_CH |    |    |
| R                  |          |    |    | NONE     | R         |    |    |
| 0h                 |          |    |    | 0h       | 0h        |    |    |
| 15                 | 14       | 13 | 12 | 11       | 10        | 9  | 8  |
| TH_HOST_ERROR_CODE |          |    |    | RESERVED | TH_ERR_CH |    |    |
| R                  |          |    |    | NONE     | R         |    |    |
| 0h                 |          |    |    | 0h       | 0h        |    |    |
| 7                  | 6        | 5  | 4  | 3        | 2         | 1  | 0  |
| RESERVED           |          |    |    |          |           |    |    |
| NONE               |          |    |    |          |           |    |    |
| 0h                 |          |    |    |          |           |    |    |

**Table 5-547. CPSW\_NC\_CPDMA\_REGS\_STATUS\_REG Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|--------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | IDLE               | R    | 1h    | CPDMA Idle Status Bit - Indicates when set that the CPDMA is not transferring a packet FHost or THost.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 30:24 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 23:20 | FH_HOST_ERROR_CODE | R    | 0h    | CPDMA FHost Error Code - This field is set to indicate CPDMA detected FHost DMA related host errors. The host should read this field after a HOST_ERR_INT to determine the error. Host error Interrupts require hardware reset in order to recover. A zero packet length is an error, but it is not detected.<br>0000 - No error<br>0001 - SOP error<br>0010 - Ownership bit not set in SOP buffer<br>0011 - Zero Next Buffer Descriptor Pointer Without EOP<br>0100 - Zero Buffer Pointer<br>0101 - Zero Buffer Length<br>0110 - Packet Length Error (sum of buffers < packet length)<br>0111 - reserved<br>...<br>1111 - reserved |
| 19    | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 18:16 | FH_ERR_CH          | R    | 0h    | CPDMA FHost Error Channel - This field indicates the FHost channel that had a host error.<br>000 - The host error occurred on TX channel 0<br>...<br>111 - The host error occurred on TX channel 7                                                                                                                                                                                                                                                                                                                                                                                                                                  |

**Table 5-547. CPSW\_NC\_CPDMA\_REGS\_STATUS\_REG Register Field Descriptions (continued)**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|--------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:12 | TH_HOST_ERROR_CODE | R    | 0h    | CPDMA THost Error Code - This field is set to indicate CPDMA detected RX DMA related host errors. The host should read this field after a HOST_ERR_INT to determine the error. Host error Interrupts require hardware reset in order to recover.<br>0000 - No error<br>0001 - reserved<br>0010 - Ownership bit not set in input buffer.<br>0011 - reserved<br>0100 - Zero Buffer Pointer.<br>0101 - Zero buffer length on non-SOP descriptor<br>0110 - SOP buffer length not greater than offset<br>...<br>1111 - reserved |
| 11    | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 10:8  | TH_ERR_CH          | R    | 0h    | CPDMA THost Host Error Channel - This field indicates which THost channel had a host error.<br>000 - The host error occurred on THost channel 0<br>...<br>111 - The host error occurred on RX channel 7                                                                                                                                                                                                                                                                                                                    |
| 7:0   | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

### 5.1.2.183 CPSW\_NC\_CPDMA\_REGS\_TH\_BUFFER\_OFFSET\_REG Register

#### 1 CPSW\_NC\_CPDMA\_REGS\_TH\_BUFFER\_OFFSET\_REG Register (Offset = 34028h) [reset = 0h]

CPDMA THost Buffer Offset Register

Return to [Summary Table](#)

**Table 5-548. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4028h       |

**Figure 5-183. CPSW\_NC\_CPDMA\_REGS\_TH\_BUFFER\_OFFSET\_REG Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| RESERVED         |    |    |    | TH_BUFFER_OFFSET |    |    |    |
| NONE             |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| TH_BUFFER_OFFSET |    |    |    |                  |    |    |    |
| R/W              |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |

**Table 5-550. CPSW\_NC\_CPDMA\_REGS\_TH\_BUFFER\_OFFSET\_REG Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 11:0  | TH_BUFFER_OFFSET | R/W  | 0h    | CPDMA THost Buffer Offset Value - The thost_buffer_offset will be written by the port into each frame SOP buffer descriptor buffer_offset field. The frame data will begin after the thost_buffer_offset value of bytes. A value of 0x0 indicates that there are no unused bytes at the beginning of the data and that valid data begins on the first byte of the buffer. A value of 0xF (decimal 15) indicates that the first 15 bytes of the buffer are to be ignored by the port and that valid buffer data starts on byte 16 of the buffer. This value is used for all channels. |

### 5.1.2.184 CPSW\_NC\_CPDMA\_REGS\_EMULATION\_CONTROL\_REG Register

#### 1 CPSW\_NC\_CPDMA\_REGS\_EMULATION\_CONTROL\_REG Register (Offset = 3402Ch) [reset = 0h]

CPDMA Emulation Control Register

Return to [Summary Table](#)

**Table 5-551. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 402Ch       |

**Figure 5-184. CPSW\_NC\_CPDMA\_REGS\_EMULATION\_CONTROL\_REG Name Register**

|          |    |    |    |    |    |      |      |
|----------|----|----|----|----|----|------|------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25   | 24   |
| RESERVED |    |    |    |    |    |      |      |
| NONE     |    |    |    |    |    |      |      |
| 0h       |    |    |    |    |    |      |      |
| 23       | 22 | 21 | 20 | 19 | 18 | 17   | 16   |
| RESERVED |    |    |    |    |    |      |      |
| NONE     |    |    |    |    |    |      |      |
| 0h       |    |    |    |    |    |      |      |
| 15       | 14 | 13 | 12 | 11 | 10 | 9    | 8    |
| RESERVED |    |    |    |    |    |      |      |
| NONE     |    |    |    |    |    |      |      |
| 0h       |    |    |    |    |    |      |      |
| 7        | 6  | 5  | 4  | 3  | 2  | 1    | 0    |
| RESERVED |    |    |    |    |    | FREE | SOFT |
| NONE     |    |    |    |    |    | R/W  | R/W  |
| 0h       |    |    |    |    |    | 0h   | 0h   |

**Table 5-553. CPSW\_NC\_CPDMA\_REGS\_EMULATION\_CONTROL\_REG Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description    |
|------|----------|------|-------|----------------|
| 31:2 | RESERVED | NONE | 0h    | Reserved       |
| 1    | FREE     | R/W  | 0h    | CPDMA Free bit |
| 0    | SOFT     | R/W  | 0h    | CPDMA Soft bit |

### 5.1.2.185 CPSW\_NC\_CPDMA\_INT\_FH\_INTSTAT\_RAW\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_FH\_INTSTAT\_RAW\_REG Register (Offset = 34080h) [reset = 0h]

CPDMA FHost Interrupt Status RAW

Return to [Summary Table](#)

**Table 5-554. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4080h       |

**Figure 5-185. CPSW\_NC\_CPDMA\_INT\_FH\_INTSTAT\_RAW\_REG Name Register**

|                  |                  |                  |                  |                  |                  |                  |                  |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| 31               | 30               | 29               | 28               | 27               | 26               | 25               | 24               |
| RESERVED         |                  |                  |                  |                  |                  |                  |                  |
| NONE             |                  |                  |                  |                  |                  |                  |                  |
| 0h               |                  |                  |                  |                  |                  |                  |                  |
| 23               | 22               | 21               | 20               | 19               | 18               | 17               | 16               |
| RESERVED         |                  |                  |                  |                  |                  |                  |                  |
| NONE             |                  |                  |                  |                  |                  |                  |                  |
| 0h               |                  |                  |                  |                  |                  |                  |                  |
| 15               | 14               | 13               | 12               | 11               | 10               | 9                | 8                |
| RESERVED         |                  |                  |                  |                  |                  |                  |                  |
| NONE             |                  |                  |                  |                  |                  |                  |                  |
| 0h               |                  |                  |                  |                  |                  |                  |                  |
| 7                | 6                | 5                | 4                | 3                | 2                | 1                | 0                |
| FH7_PEND_RA<br>W | FH6_PEND_RA<br>W | FH5_PEND_RA<br>W | FH4_PEND_RA<br>W | FH3_PEND_RA<br>W | FH2_PEND_RA<br>W | FH1_PEND_RA<br>W | FH0_PEND_RA<br>W |
| R                | R                | R                | R                | R                | R                | R                | R                |
| 0h               | 0h               | 0h               | 0h               | 0h               | 0h               | 0h               | 0h               |

**Table 5-556. CPSW\_NC\_CPDMA\_INT\_FH\_INTSTAT\_RAW\_REG Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                    |
|------|--------------|------|-------|----------------------------------------------------------------|
| 31:8 | RESERVED     | NONE | 0h    | Reserved                                                       |
| 7    | FH7_PEND_RAW | R    | 0h    | CPDMA FHost Channel 7 Interrupt Pending RAW read (before mask) |
| 6    | FH6_PEND_RAW | R    | 0h    | CPDMA FHost Channel 6 Interrupt Pending RAW read (before mask) |
| 5    | FH5_PEND_RAW | R    | 0h    | CPDMA FHost Channel 5 Interrupt Pending RAW read (before mask) |
| 4    | FH4_PEND_RAW | R    | 0h    | CPDMA FHost Channel 4 Interrupt Pending RAW read (before mask) |
| 3    | FH3_PEND_RAW | R    | 0h    | CPDMA FHost Channel 3 Interrupt Pending RAW read (before mask) |
| 2    | FH2_PEND_RAW | R    | 0h    | CPDMA FHost Channel 2 Interrupt Pending RAW read (before mask) |
| 1    | FH1_PEND_RAW | R    | 0h    | CPDMA FHost Channel 1 Interrupt Pending RAW read (before mask) |
| 0    | FH0_PEND_RAW | R    | 0h    | CPDMA FHost Channel 0 Interrupt Pending RAW read (before mask) |

### 5.1.2.186 CPSW\_NC\_CPDMA\_INT\_FH\_INTSTAT\_MASKED\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_FH\_INTSTAT\_MASKED\_REG Register (Offset = 34084h) [reset = 0h]

CPDMA FHost Interrupt Status MASKED

Return to [Summary Table](#)

**Table 5-557. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4084h       |

**Figure 5-186. CPSW\_NC\_CPDMA\_INT\_FH\_INTSTAT\_MASKED\_REG Name Register**

|                     |                     |                     |                     |                     |                     |                     |                     |
|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| 31                  | 30                  | 29                  | 28                  | 27                  | 26                  | 25                  | 24                  |
| RESERVED            |                     |                     |                     |                     |                     |                     |                     |
| NONE                |                     |                     |                     |                     |                     |                     |                     |
| 0h                  |                     |                     |                     |                     |                     |                     |                     |
| 23                  | 22                  | 21                  | 20                  | 19                  | 18                  | 17                  | 16                  |
| RESERVED            |                     |                     |                     |                     |                     |                     |                     |
| NONE                |                     |                     |                     |                     |                     |                     |                     |
| 0h                  |                     |                     |                     |                     |                     |                     |                     |
| 15                  | 14                  | 13                  | 12                  | 11                  | 10                  | 9                   | 8                   |
| RESERVED            |                     |                     |                     |                     |                     |                     |                     |
| NONE                |                     |                     |                     |                     |                     |                     |                     |
| 0h                  |                     |                     |                     |                     |                     |                     |                     |
| 7                   | 6                   | 5                   | 4                   | 3                   | 2                   | 1                   | 0                   |
| FH7_PEND_M<br>ASKED | FH6_PEND_M<br>ASKED | FH5_PEND_M<br>ASKED | FH4_PEND_M<br>ASKED | FH3_PEND_M<br>ASKED | FH2_PEND_M<br>ASKED | FH1_PEND_M<br>ASKED | FH0_PEND_M<br>ASKED |
| R                   | R                   | R                   | R                   | R                   | R                   | R                   | R                   |
| 0h                  | 0h                  | 0h                  | 0h                  | 0h                  | 0h                  | 0h                  | 0h                  |

**Table 5-559. CPSW\_NC\_CPDMA\_INT\_FH\_INTSTAT\_MASKED\_REG Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                   |
|------|-----------------|------|-------|---------------------------------------------------------------|
| 31:8 | RESERVED        | NONE | 0h    | Reserved                                                      |
| 7    | FH7_PEND_MASKED | R    | 0h    | CPDMA FHost Channel 7 Interrupt Pending MASKED interrupt read |
| 6    | FH6_PEND_MASKED | R    | 0h    | CPDMA FHost Channel 6 Interrupt Pending MASKED interrupt read |
| 5    | FH5_PEND_MASKED | R    | 0h    | CPDMA FHost Channel 5 Interrupt Pending MASKED interrupt read |
| 4    | FH4_PEND_MASKED | R    | 0h    | CPDMA FHost Channel 4 Interrupt Pending MASKED interrupt read |
| 3    | FH3_PEND_MASKED | R    | 0h    | CPDMA FHost Channel 3 Interrupt Pending MASKED interrupt read |
| 2    | FH2_PEND_MASKED | R    | 0h    | CPDMA FHost Channel 2 Interrupt Pending MASKED interrupt read |
| 1    | FH1_PEND_MASKED | R    | 0h    | CPDMA FHost Channel 1 Interrupt Pending MASKED interrupt read |
| 0    | FH0_PEND_MASKED | R    | 0h    | CPDMA FHost Channel 0 Interrupt Pending MASKED interrupt read |

### 5.1.2.187 CPSW\_NC\_CPDMA\_INT\_FH\_INTMASK\_SET\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_FH\_INTMASK\_SET\_REG Register (Offset = 34088h) [reset = 0h]

CPDMA FHost Interrupt Masked SET

Return to [Summary Table](#)

**Table 5-560. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4088h       |

**Figure 5-187. CPSW\_NC\_CPDMA\_INT\_FH\_INTMASK\_SET\_REG Name Register**

|                         |                         |                         |                         |                         |                         |                         |                         |
|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| 31                      | 30                      | 29                      | 28                      | 27                      | 26                      | 25                      | 24                      |
| RESERVED                |                         |                         |                         |                         |                         |                         |                         |
| NONE                    |                         |                         |                         |                         |                         |                         |                         |
| 0h                      |                         |                         |                         |                         |                         |                         |                         |
| 23                      | 22                      | 21                      | 20                      | 19                      | 18                      | 17                      | 16                      |
| RESERVED                |                         |                         |                         |                         |                         |                         |                         |
| NONE                    |                         |                         |                         |                         |                         |                         |                         |
| 0h                      |                         |                         |                         |                         |                         |                         |                         |
| 15                      | 14                      | 13                      | 12                      | 11                      | 10                      | 9                       | 8                       |
| RESERVED                |                         |                         |                         |                         |                         |                         |                         |
| NONE                    |                         |                         |                         |                         |                         |                         |                         |
| 0h                      |                         |                         |                         |                         |                         |                         |                         |
| 7                       | 6                       | 5                       | 4                       | 3                       | 2                       | 1                       | 0                       |
| FH7_PEND_M<br>ASKED_SET | FH6_PEND_M<br>ASKED_SET | FH5_PEND_M<br>ASKED_SET | FH4_PEND_M<br>ASKED_SET | FH3_PEND_M<br>ASKED_SET | FH2_PEND_M<br>ASKED_SET | FH1_PEND_M<br>ASKED_SET | FH0_PEND_M<br>ASKED_SET |
| R/W1TS                  | R/W1TS                  | R/W1TS                  | R/W1TS                  | R/W1TS                  | R/W1TS                  | R/W1TS                  | R/W1TS                  |
| 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 5-562. CPSW\_NC\_CPDMA\_INT\_FH\_INTMASK\_SET\_REG Register Field Descriptions**

| Bit  | Field                   | Type   | Reset | Description                                                                        |
|------|-------------------------|--------|-------|------------------------------------------------------------------------------------|
| 31:8 | RESERVED                | NONE   | 0h    | Reserved                                                                           |
| 7    | FH7_PEND_MASKED_SE<br>T | R/W1TS | 0h    | CPDMA FHost Channel 7 Interrupt Pending MASKED Set - write one to enable interrupt |
| 6    | FH6_PEND_MASKED_SE<br>T | R/W1TS | 0h    | CPDMA FHost Channel 6 Interrupt Pending MASKED Set - write one to enable interrupt |
| 5    | FH5_PEND_MASKED_SE<br>T | R/W1TS | 0h    | CPDMA FHost Channel 5 Interrupt Pending MASKED Set - write one to enable interrupt |
| 4    | FH4_PEND_MASKED_SE<br>T | R/W1TS | 0h    | CPDMA FHost Channel 4 Interrupt Pending MASKED Set - write one to enable interrupt |
| 3    | FH3_PEND_MASKED_SE<br>T | R/W1TS | 0h    | CPDMA FHost Channel 3 Interrupt Pending MASKED Set - write one to enable interrupt |
| 2    | FH2_PEND_MASKED_SE<br>T | R/W1TS | 0h    | CPDMA FHost Channel 2 Interrupt Pending MASKED Set - write one to enable interrupt |
| 1    | FH1_PEND_MASKED_SE<br>T | R/W1TS | 0h    | CPDMA FHost Channel 1 Interrupt Pending MASKED Set - write one to enable interrupt |
| 0    | FH0_PEND_MASKED_SE<br>T | R/W1TS | 0h    | CPDMA FHost Channel 0 Interrupt Pending MASKED Set - write one to enable interrupt |

### 5.1.2.188 CPSW\_NC\_CPDMA\_INT\_FH\_INTMASK\_CLEAR\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_FH\_INTMASK\_CLEAR\_REG Register (Offset = 3408Ch) [reset = 0h]

CPDMA FHost Interrupt Masked CLR

Return to [Summary Table](#)

**Table 5-563. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 408Ch       |

**Figure 5-188. CPSW\_NC\_CPDMA\_INT\_FH\_INTMASK\_CLEAR\_REG Name Register**

|                         |                         |                         |                         |                         |                         |                         |                         |
|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| 31                      | 30                      | 29                      | 28                      | 27                      | 26                      | 25                      | 24                      |
| RESERVED                |                         |                         |                         |                         |                         |                         |                         |
| NONE                    |                         |                         |                         |                         |                         |                         |                         |
| 0h                      |                         |                         |                         |                         |                         |                         |                         |
| 23                      | 22                      | 21                      | 20                      | 19                      | 18                      | 17                      | 16                      |
| RESERVED                |                         |                         |                         |                         |                         |                         |                         |
| NONE                    |                         |                         |                         |                         |                         |                         |                         |
| 0h                      |                         |                         |                         |                         |                         |                         |                         |
| 15                      | 14                      | 13                      | 12                      | 11                      | 10                      | 9                       | 8                       |
| RESERVED                |                         |                         |                         |                         |                         |                         |                         |
| NONE                    |                         |                         |                         |                         |                         |                         |                         |
| 0h                      |                         |                         |                         |                         |                         |                         |                         |
| 7                       | 6                       | 5                       | 4                       | 3                       | 2                       | 1                       | 0                       |
| FH7_PEND_M<br>ASKED_CLR | FH6_PEND_M<br>ASKED_CLR | FH5_PEND_M<br>ASKED_CLR | FH4_PEND_M<br>ASKED_CLR | FH3_PEND_M<br>ASKED_CLR | FH2_PEND_M<br>ASKED_CLR | FH1_PEND_M<br>ASKED_CLR | FH0_PEND_M<br>ASKED_CLR |
| R/W1TC                  | R/W1TC                  | R/W1TC                  | R/W1TC                  | R/W1TC                  | R/W1TC                  | R/W1TC                  | R/W1TC                  |
| 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 5-565. CPSW\_NC\_CPDMA\_INT\_FH\_INTMASK\_CLEAR\_REG Register Field Descriptions**

| Bit  | Field               | Type   | Reset | Description                                                                         |
|------|---------------------|--------|-------|-------------------------------------------------------------------------------------|
| 31:8 | RESERVED            | NONE   | 0h    | Reserved                                                                            |
| 7    | FH7_PEND_MASKED_CLR | R/W1TC | 0h    | CPDMA FHost Channel 7 Interrupt Pending MASKED Clr - write one to disable interrupt |
| 6    | FH6_PEND_MASKED_CLR | R/W1TC | 0h    | CPDMA FHost Channel 6 Interrupt Pending MASKED Clr - write one to disable interrupt |
| 5    | FH5_PEND_MASKED_CLR | R/W1TC | 0h    | CPDMA FHost Channel 5 Interrupt Pending MASKED Clr - write one to disable interrupt |
| 4    | FH4_PEND_MASKED_CLR | R/W1TC | 0h    | CPDMA FHost Channel 4 Interrupt Pending MASKED Clr - write one to disable interrupt |
| 3    | FH3_PEND_MASKED_CLR | R/W1TC | 0h    | CPDMA FHost Channel 3 Interrupt Pending MASKED Clr - write one to disable interrupt |
| 2    | FH2_PEND_MASKED_CLR | R/W1TC | 0h    | CPDMA FHost Channel 2 Interrupt Pending MASKED Clr - write one to disable interrupt |
| 1    | FH1_PEND_MASKED_CLR | R/W1TC | 0h    | CPDMA FHost Channel 1 Interrupt Pending MASKED Clr - write one to disable interrupt |
| 0    | FH0_PEND_MASKED_CLR | R/W1TC | 0h    | CPDMA FHost Channel 0 Interrupt Pending MASKED Clr - write one to disable interrupt |



### 5.1.2.189 CPSW\_NC\_CPDMA\_INT\_IN\_VECTOR\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_IN\_VECTOR\_REG Register (Offset = 34090h) [reset = 0h]

CPDMA DMA IN Vector

Return to [Summary Table](#)

**Table 5-566. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4090h       |

**Figure 5-189. CPSW\_NC\_CPDMA\_INT\_IN\_VECTOR\_REG Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DMA_IN_VECTOR |    |    |    |    |    |    |    |
| R             |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DMA_IN_VECTOR |    |    |    |    |    |    |    |
| R             |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DMA_IN_VECTOR |    |    |    |    |    |    |    |
| R             |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DMA_IN_VECTOR |    |    |    |    |    |    |    |
| R             |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 5-568. CPSW\_NC\_CPDMA\_INT\_IN\_VECTOR\_REG Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                                                                                                                                                                                                                         |
|------|---------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | DMA_IN_VECTOR | R    | 0h    | The value of CPDMA_In_Vector is reset to zero, but will change to the IN_VECTOR input bus value one clock after reset is deasserted. Thereafter, this value will change to a new IN_VECTOR input value one clock after the IN_VECTOR value changes. |

### 5.1.2.190 CPSW\_NC\_CPDMA\_INT\_EOI\_VECTOR\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_EOI\_VECTOR\_REG Register (Offset = 34094h) [reset = 0h]

The CPDMA\_EOI\_VECTOR(4:0) output bus reflects the value written to this location one VBUSP\_GCLK cycle after a write to this location. The EOI\_WR signal is asserted for a single clock cycle after a latency of two VBUSP\_GCLK cycles when a write is performed to this location.

Return to [Summary Table](#)

**Table 5-569. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4094h       |

**Figure 5-190. CPSW\_NC\_CPDMA\_INT\_EOI\_VECTOR\_REG Name Register**

|          |    |    |    |                |    |    |    |
|----------|----|----|----|----------------|----|----|----|
| 31       | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 23       | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 15       | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| RESERVED |    |    |    |                |    |    |    |
| NONE     |    |    |    |                |    |    |    |
| 0h       |    |    |    |                |    |    |    |
| 7        | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| RESERVED |    |    |    | DMA_EOI_VECTOR |    |    |    |
| NONE     |    |    |    | R/W            |    |    |    |
| 0h       |    |    |    | 0h             |    |    |    |

**Table 5-571. CPSW\_NC\_CPDMA\_INT\_EOI\_VECTOR\_REG Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description          |
|------|----------------|------|-------|----------------------|
| 31:5 | RESERVED       | NONE | 0h    | Reserved             |
| 4:0  | DMA_EOI_VECTOR | R/W  | 0h    | CPDMA DMA EOI Vector |

### 5.1.2.191 CPSW\_NC\_CPDMA\_INT\_TH\_INTSTAT\_RAW\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_TH\_INTSTAT\_RAW\_REG Register (Offset = 340A0h) [reset = 0h]

CPDMA Receive Interrupt Status RAW

Return to [Summary Table](#)

**Table 5-572. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 40A0h       |

**Figure 5-191. CPSW\_NC\_CPDMA\_INT\_TH\_INTSTAT\_RAW\_REG Name Register**

|                     |                     |                     |                     |                     |                     |                     |                     |
|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| 31                  | 30                  | 29                  | 28                  | 27                  | 26                  | 25                  | 24                  |
| RESERVED            |                     |                     |                     |                     |                     |                     |                     |
| NONE                |                     |                     |                     |                     |                     |                     |                     |
| 0h                  |                     |                     |                     |                     |                     |                     |                     |
| 23                  | 22                  | 21                  | 20                  | 19                  | 18                  | 17                  | 16                  |
| RESERVED            |                     |                     |                     |                     |                     |                     |                     |
| NONE                |                     |                     |                     |                     |                     |                     |                     |
| 0h                  |                     |                     |                     |                     |                     |                     |                     |
| 15                  | 14                  | 13                  | 12                  | 11                  | 10                  | 9                   | 8                   |
| TH7_THRESH_PEND_RAW | TH6_THRESH_PEND_RAW | TH5_THRESH_PEND_RAW | TH4_THRESH_PEND_RAW | TH3_THRESH_PEND_RAW | TH2_THRESH_PEND_RAW | TH1_THRESH_PEND_RAW | TH0_THRESH_PEND_RAW |
| R                   | R                   | R                   | R                   | R                   | R                   | R                   | R                   |
| 0h                  | 0h                  | 0h                  | 0h                  | 0h                  | 0h                  | 0h                  | 0h                  |
| 7                   | 6                   | 5                   | 4                   | 3                   | 2                   | 1                   | 0                   |
| TH7_PEND_RAW        | TH6_PEND_RAW        | TH5_PEND_RAW        | TH4_PEND_RAW        | TH3_PEND_RAW        | TH2_PEND_RAW        | TH1_PEND_RAW        | TH0_PEND_RAW        |
| R                   | R                   | R                   | R                   | R                   | R                   | R                   | R                   |
| 0h                  | 0h                  | 0h                  | 0h                  | 0h                  | 0h                  | 0h                  | 0h                  |

**Table 5-574. CPSW\_NC\_CPDMA\_INT\_TH\_INTSTAT\_RAW\_REG Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                |
|-------|---------------------|------|-------|----------------------------------------------------------------------------|
| 31:16 | RESERVED            | NONE | 0h    | Reserved                                                                   |
| 15    | TH7_THRESH_PEND_RAW | R    | 0h    | CPDMA Receive Channel 7 Threshold Interrupt Pending RAW read (before mask) |
| 14    | TH6_THRESH_PEND_RAW | R    | 0h    | CPDMA Receive Channel 6 Threshold Interrupt Pending RAW read (before mask) |
| 13    | TH5_THRESH_PEND_RAW | R    | 0h    | CPDMA Receive Channel 5 Threshold Interrupt Pending RAW read (before mask) |
| 12    | TH4_THRESH_PEND_RAW | R    | 0h    | CPDMA Receive Channel 4 Threshold Interrupt Pending RAW read (before mask) |
| 11    | TH3_THRESH_PEND_RAW | R    | 0h    | CPDMA Receive Channel 3 Threshold Interrupt Pending RAW read (before mask) |
| 10    | TH2_THRESH_PEND_RAW | R    | 0h    | CPDMA Receive Channel 2 Threshold Interrupt Pending RAW read (before mask) |
| 9     | TH1_THRESH_PEND_RAW | R    | 0h    | CPDMA Receive Channel 1 Threshold Interrupt Pending RAW read (before mask) |
| 8     | TH0_THRESH_PEND_RAW | R    | 0h    | CPDMA Receive Channel 0 Threshold Interrupt Pending RAW read (before mask) |
| 7     | TH7_PEND_RAW        | R    | 0h    | CPDMA Receive Channel 7 Interrupt Pending RAW read (before mask)           |

**Table 5-574. CPSW\_NC\_CPDMA\_INT\_TH\_INTSTAT\_RAW\_REG Register Field Descriptions (continued)**

| Bit | Field        | Type | Reset | Description                                                      |
|-----|--------------|------|-------|------------------------------------------------------------------|
| 6   | TH6_PEND_RAW | R    | 0h    | CPDMA Receive Channel 6 Interrupt Pending RAW read (before mask) |
| 5   | TH5_PEND_RAW | R    | 0h    | CPDMA Receive Channel 5 Interrupt Pending RAW read (before mask) |
| 4   | TH4_PEND_RAW | R    | 0h    | CPDMA Receive Channel 4 Interrupt Pending RAW read (before mask) |
| 3   | TH3_PEND_RAW | R    | 0h    | CPDMA Receive Channel 3 Interrupt Pending RAW read (before mask) |
| 2   | TH2_PEND_RAW | R    | 0h    | CPDMA Receive Channel 2 Interrupt Pending RAW read (before mask) |
| 1   | TH1_PEND_RAW | R    | 0h    | CPDMA Receive Channel 1 Interrupt Pending RAW read (before mask) |
| 0   | TH0_PEND_RAW | R    | 0h    | CPDMA Receive Channel 0 Interrupt Pending RAW read (before mask) |

### 5.1.2.192 CPSW\_NC\_CPDMA\_INT\_TH\_INTSTAT\_MASKED\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_TH\_INTSTAT\_MASKED\_REG Register (Offset = 340A4h) [reset = 0h]

CPDMA Receive Interrupt Status MASKED

Return to [Summary Table](#)

**Table 5-575. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 40A4h       |

**Figure 5-192. CPSW\_NC\_CPDMA\_INT\_TH\_INTSTAT\_MASKED\_REG Name Register**

|                            |                            |                            |                            |                            |                            |                            |                            |
|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| 31                         | 30                         | 29                         | 28                         | 27                         | 26                         | 25                         | 24                         |
| RESERVED                   |                            |                            |                            |                            |                            |                            |                            |
| NONE                       |                            |                            |                            |                            |                            |                            |                            |
| 0h                         |                            |                            |                            |                            |                            |                            |                            |
| 23                         | 22                         | 21                         | 20                         | 19                         | 18                         | 17                         | 16                         |
| RESERVED                   |                            |                            |                            |                            |                            |                            |                            |
| NONE                       |                            |                            |                            |                            |                            |                            |                            |
| 0h                         |                            |                            |                            |                            |                            |                            |                            |
| 15                         | 14                         | 13                         | 12                         | 11                         | 10                         | 9                          | 8                          |
| TH7_THRESH_PEND_MASKE<br>D | TH6_THRESH_PEND_MASKE<br>D | TH5_THRESH_PEND_MASKE<br>D | TH4_THRESH_PEND_MASKE<br>D | TH3_THRESH_PEND_MASKE<br>D | TH2_THRESH_PEND_MASKE<br>D | TH1_THRESH_PEND_MASKE<br>D | TH0_THRESH_PEND_MASKE<br>D |
| R                          | R                          | R                          | R                          | R                          | R                          | R                          | R                          |
| 0h                         | 0h                         | 0h                         | 0h                         | 0h                         | 0h                         | 0h                         | 0h                         |
| 7                          | 6                          | 5                          | 4                          | 3                          | 2                          | 1                          | 0                          |
| TH7_PEND_M<br>ASKED        | TH6_PEND_M<br>ASKED        | TH5_PEND_M<br>ASKED        | TH4_PEND_M<br>ASKED        | TH3_PEND_M<br>ASKED        | TH2_PEND_M<br>ASKED        | TH1_PEND_M<br>ASKED        | TH0_PEND_M<br>ASKED        |
| R                          | R                          | R                          | R                          | R                          | R                          | R                          | R                          |
| 0h                         | 0h                         | 0h                         | 0h                         | 0h                         | 0h                         | 0h                         | 0h                         |

**Table 5-577. CPSW\_NC\_CPDMA\_INT\_TH\_INTSTAT\_MASKED\_REG Register Field Descriptions**

| Bit   | Field                      | Type | Reset | Description                                                     |
|-------|----------------------------|------|-------|-----------------------------------------------------------------|
| 31:16 | RESERVED                   | NONE | 0h    | Reserved                                                        |
| 15    | TH7_THRESH_PEND_M<br>ASKED | R    | 0h    | CPDMA Receive Channel 7 Threshold Interrupt Pending MASKED read |
| 14    | TH6_THRESH_PEND_M<br>ASKED | R    | 0h    | CPDMA Receive Channel 6 Threshold Interrupt Pending MASKED read |
| 13    | TH5_THRESH_PEND_M<br>ASKED | R    | 0h    | CPDMA Receive Channel 5 Threshold Interrupt Pending MASKED read |
| 12    | TH4_THRESH_PEND_M<br>ASKED | R    | 0h    | CPDMA Receive Channel 4 Threshold Interrupt Pending MASKED read |
| 11    | TH3_THRESH_PEND_M<br>ASKED | R    | 0h    | CPDMA Receive Channel 3 Threshold Interrupt Pending MASKED read |
| 10    | TH2_THRESH_PEND_M<br>ASKED | R    | 0h    | CPDMA Receive Channel 2 Threshold Interrupt Pending MASKED read |
| 9     | TH1_THRESH_PEND_M<br>ASKED | R    | 0h    | CPDMA Receive Channel 1 Threshold Interrupt Pending MASKED read |
| 8     | TH0_THRESH_PEND_M<br>ASKED | R    | 0h    | CPDMA Receive Channel 0 Threshold Interrupt Pending MASKED read |
| 7     | TH7_PEND_MASKED            | R    | 0h    | CPDMA Receive Channel 7 Interrupt Pending MASKED read           |

**Table 5-577. CPSW\_NC\_CPDMA\_INT\_TH\_INTSTAT\_MASKED\_REG Register Field Descriptions  
(continued)**

| Bit | Field           | Type | Reset | Description                                           |
|-----|-----------------|------|-------|-------------------------------------------------------|
| 6   | TH6_PEND_MASKED | R    | 0h    | CPDMA Receive Channel 6 Interrupt Pending MASKED read |
| 5   | TH5_PEND_MASKED | R    | 0h    | CPDMA Receive Channel 5 Interrupt Pending MASKED read |
| 4   | TH4_PEND_MASKED | R    | 0h    | CPDMA Receive Channel 4 Interrupt Pending MASKED read |
| 3   | TH3_PEND_MASKED | R    | 0h    | CPDMA Receive Channel 3 Interrupt Pending MASKED read |
| 2   | TH2_PEND_MASKED | R    | 0h    | CPDMA Receive Channel 2 Interrupt Pending MASKED read |
| 1   | TH1_PEND_MASKED | R    | 0h    | CPDMA Receive Channel 1 Interrupt Pending MASKED read |
| 0   | TH0_PEND_MASKED | R    | 0h    | CPDMA Receive Channel 0 Interrupt Pending MASKED read |

### 5.1.2.193 CPSW\_NC\_CPDMA\_INT\_TH\_INTMASK\_SET\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_TH\_INTMASK\_SET\_REG Register (Offset = 340A8h) [reset = 0h]

CPDMA THost Interrupt Masked SET

Return to [Summary Table](#)

**Table 5-578. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 40A8h       |

**Figure 5-193. CPSW\_NC\_CPDMA\_INT\_TH\_INTMASK\_SET\_REG Name Register**

|                             |                             |                             |                             |                             |                             |                             |                             |
|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| 31                          | 30                          | 29                          | 28                          | 27                          | 26                          | 25                          | 24                          |
| RESERVED                    |                             |                             |                             |                             |                             |                             |                             |
| NONE                        |                             |                             |                             |                             |                             |                             |                             |
| 0h                          |                             |                             |                             |                             |                             |                             |                             |
| 23                          | 22                          | 21                          | 20                          | 19                          | 18                          | 17                          | 16                          |
| RESERVED                    |                             |                             |                             |                             |                             |                             |                             |
| NONE                        |                             |                             |                             |                             |                             |                             |                             |
| 0h                          |                             |                             |                             |                             |                             |                             |                             |
| 15                          | 14                          | 13                          | 12                          | 11                          | 10                          | 9                           | 8                           |
| TH7_THRESH_PEND_MASKE_D_SET | TH6_THRESH_PEND_MASKE_D_SET | TH5_THRESH_PEND_MASKE_D_SET | TH4_THRESH_PEND_MASKE_D_SET | TH3_THRESH_PEND_MASKE_D_SET | TH2_THRESH_PEND_MASKE_D_SET | TH1_THRESH_PEND_MASKE_D_SET | TH0_THRESH_PEND_MASKE_D_SET |
| R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                      |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                          | 0h                          | 0h                          | 0h                          |
| 7                           | 6                           | 5                           | 4                           | 3                           | 2                           | 1                           | 0                           |
| TH7_PEND_M ASKED_SET        | TH6_PEND_M ASKED_SET        | TH5_PEND_M ASKED_SET        | TH4_PEND_M ASKED_SET        | TH3_PEND_M ASKED_SET        | TH2_PEND_M ASKED_SET        | TH1_PEND_M ASKED_SET        | TH0_PEND_M ASKED_SET        |
| R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                      | R/W1TS                      |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                          | 0h                          | 0h                          | 0h                          |

**Table 5-580. CPSW\_NC\_CPDMA\_INT\_TH\_INTMASK\_SET\_REG Register Field Descriptions**

| Bit   | Field                       | Type   | Reset | Description                                                                           |
|-------|-----------------------------|--------|-------|---------------------------------------------------------------------------------------|
| 31:16 | RESERVED                    | NONE   | 0h    | Reserved                                                                              |
| 15    | TH7_THRESH_PEND_M ASKED_SET | R/W1TS | 0h    | CPDMA THost Channel 7 Threshold Interrupt Pending SET - write one to enable interrupt |
| 14    | TH6_THRESH_PEND_M ASKED_SET | R/W1TS | 0h    | CPDMA THost Channel 6 Threshold Interrupt Pending SET - write one to enable interrupt |
| 13    | TH5_THRESH_PEND_M ASKED_SET | R/W1TS | 0h    | CPDMA THost Channel 5 Threshold Interrupt Pending SET - write one to enable interrupt |
| 12    | TH4_THRESH_PEND_M ASKED_SET | R/W1TS | 0h    | CPDMA THost Channel 4 Threshold Interrupt Pending SET - write one to enable interrupt |
| 11    | TH3_THRESH_PEND_M ASKED_SET | R/W1TS | 0h    | CPDMA THost Channel 3 Threshold Interrupt Pending SET - write one to enable interrupt |
| 10    | TH2_THRESH_PEND_M ASKED_SET | R/W1TS | 0h    | CPDMA THost Channel 2 Threshold Interrupt Pending SET - write one to enable interrupt |
| 9     | TH1_THRESH_PEND_M ASKED_SET | R/W1TS | 0h    | CPDMA THost Channel 1 Threshold Interrupt Pending SET - write one to enable interrupt |
| 8     | TH0_THRESH_PEND_M ASKED_SET | R/W1TS | 0h    | CPDMA THost Channel 0 Threshold Interrupt Pending SET - write one to enable interrupt |
| 7     | TH7_PEND_MASKED_SE T        | R/W1TS | 0h    | CPDMA THost Channel 7 Interrupt Pending SET - write one to enable interrupt           |

**Table 5-580. CPSW\_NC\_CPDMA\_INT\_TH\_INTMASK\_SET\_REG Register Field Descriptions (continued)**

| Bit | Field               | Type   | Reset | Description                                                                 |
|-----|---------------------|--------|-------|-----------------------------------------------------------------------------|
| 6   | TH6_PEND_MASKED_SET | R/W1TS | 0h    | CPDMA THost Channel 6 Interrupt Pending SET - write one to enable interrupt |
| 5   | TH5_PEND_MASKED_SET | R/W1TS | 0h    | CPDMA THost Channel 5 Interrupt Pending SET - write one to enable interrupt |
| 4   | TH4_PEND_MASKED_SET | R/W1TS | 0h    | CPDMA THost Channel 4 Interrupt Pending SET - write one to enable interrupt |
| 3   | TH3_PEND_MASKED_SET | R/W1TS | 0h    | CPDMA THost Channel 3 Interrupt Pending SET - write one to enable interrupt |
| 2   | TH2_PEND_MASKED_SET | R/W1TS | 0h    | CPDMA THost Channel 2 Interrupt Pending SET - write one to enable interrupt |
| 1   | TH1_PEND_MASKED_SET | R/W1TS | 0h    | CPDMA THost Channel 1 Interrupt Pending SET - write one to enable interrupt |
| 0   | TH0_PEND_MASKED_SET | R/W1TS | 0h    | CPDMA THost Channel 0 Interrupt Pending SET - write one to enable interrupt |



### 5.1.2.194 CPSW\_NC\_CPDMA\_INT\_TH\_INTMASK\_CLEAR\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_TH\_INTMASK\_CLEAR\_REG Register (Offset = 340ACh) [reset = 0h]

CPDMA THost Interrupt Masked CLR

Return to [Summary Table](#)

**Table 5-581. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 40ACh       |

**Figure 5-194. CPSW\_NC\_CPDMA\_INT\_TH\_INTMASK\_CLEAR\_REG Name Register**

|                             |                             |                             |                             |                             |                             |                             |                             |
|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| 31                          | 30                          | 29                          | 28                          | 27                          | 26                          | 25                          | 24                          |
| RESERVED                    |                             |                             |                             |                             |                             |                             |                             |
| NONE                        |                             |                             |                             |                             |                             |                             |                             |
| 0h                          |                             |                             |                             |                             |                             |                             |                             |
| 23                          | 22                          | 21                          | 20                          | 19                          | 18                          | 17                          | 16                          |
| RESERVED                    |                             |                             |                             |                             |                             |                             |                             |
| NONE                        |                             |                             |                             |                             |                             |                             |                             |
| 0h                          |                             |                             |                             |                             |                             |                             |                             |
| 15                          | 14                          | 13                          | 12                          | 11                          | 10                          | 9                           | 8                           |
| TH7_THRESH_PEND_MASKE_D_CLR | TH6_THRESH_PEND_MASKE_D_CLR | TH5_THRESH_PEND_MASKE_D_CLR | TH4_THRESH_PEND_MASKE_D_CLR | TH3_THRESH_PEND_MASKE_D_CLR | TH2_THRESH_PEND_MASKE_D_CLR | TH1_THRESH_PEND_MASKE_D_CLR | TH0_THRESH_PEND_MASKE_D_CLR |
| R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                      |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                          | 0h                          | 0h                          | 0h                          |
| 7                           | 6                           | 5                           | 4                           | 3                           | 2                           | 1                           | 0                           |
| TH7_PEND_M ASKED_CLR        | TH6_PEND_M ASKED_CLR        | TH5_PEND_M ASKED_CLR        | TH4_PEND_M ASKED_CLR        | TH3_PEND_M ASKED_CLR        | TH2_PEND_M ASKED_CLR        | TH1_PEND_M ASKED_CLR        | TH0_PEND_M ASKED_CLR        |
| R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                      | R/W1TC                      |
| 0h                          | 0h                          | 0h                          | 0h                          | 0h                          | 0h                          | 0h                          | 0h                          |

**Table 5-583. CPSW\_NC\_CPDMA\_INT\_TH\_INTMASK\_CLEAR\_REG Register Field Descriptions**

| Bit   | Field                       | Type   | Reset | Description                                                                            |
|-------|-----------------------------|--------|-------|----------------------------------------------------------------------------------------|
| 31:16 | RESERVED                    | NONE   | 0h    | Reserved                                                                               |
| 15    | TH7_THRESH_PEND_M ASKED_CLR | R/W1TC | 0h    | CPDMA THost Channel 7 Threshold Interrupt Pending CLR - write one to disable interrupt |
| 14    | TH6_THRESH_PEND_M ASKED_CLR | R/W1TC | 0h    | CPDMA THost Channel 6 Threshold Interrupt Pending CLR - write one to disable interrupt |
| 13    | TH5_THRESH_PEND_M ASKED_CLR | R/W1TC | 0h    | CPDMA THost Channel 5 Threshold Interrupt Pending CLR - write one to disable interrupt |
| 12    | TH4_THRESH_PEND_M ASKED_CLR | R/W1TC | 0h    | CPDMA THost Channel 4 Threshold Interrupt Pending CLR - write one to disable interrupt |
| 11    | TH3_THRESH_PEND_M ASKED_CLR | R/W1TC | 0h    | CPDMA THost Channel 3 Threshold Interrupt Pending CLR - write one to disable interrupt |
| 10    | TH2_THRESH_PEND_M ASKED_CLR | R/W1TC | 0h    | CPDMA THost Channel 2 Threshold Interrupt Pending CLR - write one to disable interrupt |
| 9     | TH1_THRESH_PEND_M ASKED_CLR | R/W1TC | 0h    | CPDMA THost Channel 1 Threshold Interrupt Pending CLR - write one to disable interrupt |
| 8     | TH0_THRESH_PEND_M ASKED_CLR | R/W1TC | 0h    | CPDMA THost Channel 0 Threshold Interrupt Pending CLR - write one to disable interrupt |
| 7     | TH7_PEND_MASKED_CLR         | R/W1TC | 0h    | CPDMA THost Channel 7 Interrupt Pending CLR - write one to disable interrupt           |

**Table 5-583. CPSW\_NC\_CPDMA\_INT\_TH\_INTMASK\_CLEAR\_REG Register Field Descriptions  
(continued)**

| Bit | Field               | Type   | Reset | Description                                                                  |
|-----|---------------------|--------|-------|------------------------------------------------------------------------------|
| 6   | TH6_PEND_MASKED_CLR | R/W1TC | 0h    | CPDMA THost Channel 6 Interrupt Pending CLR - write one to disable interrupt |
| 5   | TH5_PEND_MASKED_CLR | R/W1TC | 0h    | CPDMA THost Channel 5 Interrupt Pending CLR - write one to disable interrupt |
| 4   | TH4_PEND_MASKED_CLR | R/W1TC | 0h    | CPDMA THost Channel 4 Interrupt Pending CLR - write one to disable interrupt |
| 3   | TH3_PEND_MASKED_CLR | R/W1TC | 0h    | CPDMA THost Channel 3 Interrupt Pending CLR - write one to disable interrupt |
| 2   | TH2_PEND_MASKED_CLR | R/W1TC | 0h    | CPDMA THost Channel 2 Interrupt Pending CLR - write one to disable interrupt |
| 1   | TH1_PEND_MASKED_CLR | R/W1TC | 0h    | CPDMA THost Channel 1 Interrupt Pending CLR - write one to disable interrupt |
| 0   | TH0_PEND_MASKED_CLR | R/W1TC | 0h    | CPDMA THost Channel 0 Interrupt Pending CLR - write one to disable interrupt |

### 5.1.2.195 CPSW\_NC\_CPDMA\_INT\_INTSTAT\_RAW\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_INTSTAT\_RAW\_REG Register (Offset = 340B0h) [reset = 0h]

CPDMA DMA Interrupt Status RAW

Return to [Summary Table](#)

**Table 5-584. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 40B0h       |

**Figure 5-195. CPSW\_NC\_CPDMA\_INT\_INTSTAT\_RAW\_REG Name Register**

|          |    |    |    |    |    |               |               |
|----------|----|----|----|----|----|---------------|---------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25            | 24            |
| RESERVED |    |    |    |    |    |               |               |
| NONE     |    |    |    |    |    |               |               |
| 0h       |    |    |    |    |    |               |               |
| 23       | 22 | 21 | 20 | 19 | 18 | 17            | 16            |
| RESERVED |    |    |    |    |    |               |               |
| NONE     |    |    |    |    |    |               |               |
| 0h       |    |    |    |    |    |               |               |
| 15       | 14 | 13 | 12 | 11 | 10 | 9             | 8             |
| RESERVED |    |    |    |    |    |               |               |
| NONE     |    |    |    |    |    |               |               |
| 0h       |    |    |    |    |    |               |               |
| 7        | 6  | 5  | 4  | 3  | 2  | 1             | 0             |
| RESERVED |    |    |    |    |    | HOST_PEND_RAW | STAT_PEND_RAW |
| NONE     |    |    |    |    |    | R             | R             |
| 0h       |    |    |    |    |    | 0h            | 0h            |

**Table 5-586. CPSW\_NC\_CPDMA\_INT\_INTSTAT\_RAW\_REG Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                                 |
|------|---------------|------|-------|-------------------------------------------------------------|
| 31:2 | RESERVED      | NONE | 0h    | Reserved                                                    |
| 1    | HOST_PEND_RAW | R    | 0h    | CPDMA HOST Interrupt Pending RAW - read (before mask)       |
| 0    | STAT_PEND_RAW | R    | 0h    | CPDMA Statistics Interrupt Pending RAW - read (before mask) |

### 5.1.2.196 CPSW\_NC\_CPDMA\_INT\_INTSTAT\_MASKED\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_INTSTAT\_MASKED\_REG Register (Offset = 340B4h) [reset = 0h]

CPDMA DMA Interrupt Status MASKED

Return to [Summary Table](#)

**Table 5-587. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 40B4h       |

**Figure 5-196. CPSW\_NC\_CPDMA\_INT\_INTSTAT\_MASKED\_REG Name Register**

|          |    |    |    |    |    |           |           |
|----------|----|----|----|----|----|-----------|-----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25        | 24        |
| RESERVED |    |    |    |    |    |           |           |
| NONE     |    |    |    |    |    |           |           |
| 0h       |    |    |    |    |    |           |           |
| 23       | 22 | 21 | 20 | 19 | 18 | 17        | 16        |
| RESERVED |    |    |    |    |    |           |           |
| NONE     |    |    |    |    |    |           |           |
| 0h       |    |    |    |    |    |           |           |
| 15       | 14 | 13 | 12 | 11 | 10 | 9         | 8         |
| RESERVED |    |    |    |    |    |           |           |
| NONE     |    |    |    |    |    |           |           |
| 0h       |    |    |    |    |    |           |           |
| 7        | 6  | 5  | 4  | 3  | 2  | 1         | 0         |
| RESERVED |    |    |    |    |    | HOST_PEND | STAT_PEND |
| NONE     |    |    |    |    |    | R         | R         |
| 0h       |    |    |    |    |    | 0h        | 0h        |

**Table 5-589. CPSW\_NC\_CPDMA\_INT\_INTSTAT\_MASKED\_REG Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                    |
|------|-----------|------|-------|------------------------------------------------|
| 31:2 | RESERVED  | NONE | 0h    | Reserved                                       |
| 1    | HOST_PEND | R    | 0h    | CPDMA HOST Interrupt Pending MASKED read       |
| 0    | STAT_PEND | R    | 0h    | CPDMA Statistics Interrupt Pending MASKED read |

### 5.1.2.197 CPSW\_NC\_CPDMA\_INT\_INTMASK\_SET\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_INTMASK\_SET\_REG Register (Offset = 340B8h) [reset = 0h]

CPDMA DMA Interrupt Status SET

Return to [Summary Table](#)

**Table 5-590. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 40B8h       |

**Figure 5-197. CPSW\_NC\_CPDMA\_INT\_INTMASK\_SET\_REG Name Register**

|          |    |    |    |    |    |                      |                          |
|----------|----|----|----|----|----|----------------------|--------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25                   | 24                       |
| RESERVED |    |    |    |    |    |                      |                          |
| NONE     |    |    |    |    |    |                      |                          |
| 0h       |    |    |    |    |    |                      |                          |
| 23       | 22 | 21 | 20 | 19 | 18 | 17                   | 16                       |
| RESERVED |    |    |    |    |    |                      |                          |
| NONE     |    |    |    |    |    |                      |                          |
| 0h       |    |    |    |    |    |                      |                          |
| 15       | 14 | 13 | 12 | 11 | 10 | 9                    | 8                        |
| RESERVED |    |    |    |    |    |                      |                          |
| NONE     |    |    |    |    |    |                      |                          |
| 0h       |    |    |    |    |    |                      |                          |
| 7        | 6  | 5  | 4  | 3  | 2  | 1                    | 0                        |
| RESERVED |    |    |    |    |    | HOST_PEND_MASKED_SET | STAT_PEND_M<br>ASKED_SET |
| NONE     |    |    |    |    |    | R/W1TS               | R/W1TS                   |
| 0h       |    |    |    |    |    | 0h                   | 0h                       |

**Table 5-592. CPSW\_NC\_CPDMA\_INT\_INTMASK\_SET\_REG Register Field Descriptions**

| Bit  | Field                | Type   | Reset | Description                                                           |
|------|----------------------|--------|-------|-----------------------------------------------------------------------|
| 31:2 | RESERVED             | NONE   | 0h    | Reserved                                                              |
| 1    | HOST_PEND_MASKED_SET | R/W1TS | 0h    | CPDMA HOST Interrupt Masked SET - write one to enable interrupt       |
| 0    | STAT_PEND_MASKED_SET | R/W1TS | 0h    | CPDMA Statistics Interrupt Masked SET - write one to enable interrupt |

### 5.1.2.198 CPSW\_NC\_CPDMA\_INT\_INTMASK\_CLEAR\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_INTMASK\_CLEAR\_REG Register (Offset = 340BCh) [reset = 0h]

CPDMA DMA Interrupt Status CLR

Return to [Summary Table](#)

**Table 5-593. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 40BCh       |

**Figure 5-198. CPSW\_NC\_CPDMA\_INT\_INTMASK\_CLEAR\_REG Name Register**

|          |    |    |    |    |    |                      |                          |
|----------|----|----|----|----|----|----------------------|--------------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25                   | 24                       |
| RESERVED |    |    |    |    |    |                      |                          |
| NONE     |    |    |    |    |    |                      |                          |
| 0h       |    |    |    |    |    |                      |                          |
| 23       | 22 | 21 | 20 | 19 | 18 | 17                   | 16                       |
| RESERVED |    |    |    |    |    |                      |                          |
| NONE     |    |    |    |    |    |                      |                          |
| 0h       |    |    |    |    |    |                      |                          |
| 15       | 14 | 13 | 12 | 11 | 10 | 9                    | 8                        |
| RESERVED |    |    |    |    |    |                      |                          |
| NONE     |    |    |    |    |    |                      |                          |
| 0h       |    |    |    |    |    |                      |                          |
| 7        | 6  | 5  | 4  | 3  | 2  | 1                    | 0                        |
| RESERVED |    |    |    |    |    | HOST_PEND_MASKED_CLR | STAT_PEND_M<br>ASKED_CLR |
| NONE     |    |    |    |    |    | R/W1TS               | R/W1TS                   |
| 0h       |    |    |    |    |    | 0h                   | 0h                       |

**Table 5-595. CPSW\_NC\_CPDMA\_INT\_INTMASK\_CLEAR\_REG Register Field Descriptions**

| Bit  | Field                | Type   | Reset | Description                                                            |
|------|----------------------|--------|-------|------------------------------------------------------------------------|
| 31:2 | RESERVED             | NONE   | 0h    | Reserved                                                               |
| 1    | HOST_PEND_MASKED_CLR | R/W1TS | 0h    | CPDMA HOST Interrupt Masked CLR - write one to disable interrupt       |
| 0    | STAT_PEND_MASKED_CLR | R/W1TS | 0h    | CPDMA Statistics Interrupt Masked CLR - write one to disable interrupt |

### 5.1.2.199 CPSW\_NC\_CPDMA\_INT\_TH0\_PENDTHRESH\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_TH0\_PENDTHRESH\_REG Register (Offset = 340C0h) [reset = 0h]

CPDMA THost Threshold Pending Register

Return to [Summary Table](#)

**Table 5-596. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 40C0h       |

**Figure 5-199. CPSW\_NC\_CPDMA\_INT\_TH0\_PENDTHRESH\_REG Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH0_PENDTHRESH |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-598. CPSW\_NC\_CPDMA\_INT\_TH0\_PENDTHRESH\_REG Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                     |
|------|----------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED       | NONE | 0h    | Reserved                                                                                        |
| 7:0  | TH0_PENDTHRESH | R/W  | 0h    | This field contains the threshold value for issuing threshold pending interrupts (when enabled) |

### 5.1.2.200 CPSW\_NC\_CPDMA\_INT\_TH1\_PENDTHRESH\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_TH1\_PENDTHRESH\_REG Register (Offset = 340C4h) [reset = 0h]

CPDMA THost Threshold Pending Register

Return to [Summary Table](#)

**Table 5-599. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 40C4h       |

**Figure 5-200. CPSW\_NC\_CPDMA\_INT\_TH1\_PENDTHRESH\_REG Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH1_PENDTHRESH |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-601. CPSW\_NC\_CPDMA\_INT\_TH1\_PENDTHRESH\_REG Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                     |
|------|----------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED       | NONE | 0h    | Reserved                                                                                        |
| 7:0  | TH1_PENDTHRESH | R/W  | 0h    | This field contains the threshold value for issuing threshold pending interrupts (when enabled) |



### 5.1.2.201 CPSW\_NC\_CPDMA\_INT\_TH2\_PENDTHRESH\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_TH2\_PENDTHRESH\_REG Register (Offset = 340C8h) [reset = 0h]

CPDMA THost Threshold Pending Register

Return to [Summary Table](#)

**Table 5-602. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 40C8h       |

**Figure 5-201. CPSW\_NC\_CPDMA\_INT\_TH2\_PENDTHRESH\_REG Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH2_PENDTHRESH |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-604. CPSW\_NC\_CPDMA\_INT\_TH2\_PENDTHRESH\_REG Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                     |
|------|----------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED       | NONE | 0h    | Reserved                                                                                        |
| 7:0  | TH2_PENDTHRESH | R/W  | 0h    | This field contains the threshold value for issuing threshold pending interrupts (when enabled) |

### 5.1.2.202 CPSW\_NC\_CPDMA\_INT\_TH3\_PENDTHRESH\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_TH3\_PENDTHRESH\_REG Register (Offset = 340CCh) [reset = 0h]

CPDMA THost Threshold Pending Register

Return to [Summary Table](#)

**Table 5-605. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 40CCh       |

**Figure 5-202. CPSW\_NC\_CPDMA\_INT\_TH3\_PENDTHRESH\_REG Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH3_PENDTHRESH |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-607. CPSW\_NC\_CPDMA\_INT\_TH3\_PENDTHRESH\_REG Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                     |
|------|----------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED       | NONE | 0h    | Reserved                                                                                        |
| 7:0  | TH3_PENDTHRESH | R/W  | 0h    | This field contains the threshold value for issuing threshold pending interrupts (when enabled) |

### 5.1.2.203 CPSW\_NC\_CPDMA\_INT\_TH4\_PENDTHRESH\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_TH4\_PENDTHRESH\_REG Register (Offset = 340D0h) [reset = 0h]

CPDMA THost Threshold Pending Register

Return to [Summary Table](#)

**Table 5-608. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 40D0h       |

**Figure 5-203. CPSW\_NC\_CPDMA\_INT\_TH4\_PENDTHRESH\_REG Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH4_PENDTHRESH |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-610. CPSW\_NC\_CPDMA\_INT\_TH4\_PENDTHRESH\_REG Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                     |
|------|----------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED       | NONE | 0h    | Reserved                                                                                        |
| 7:0  | TH4_PENDTHRESH | R/W  | 0h    | This field contains the threshold value for issuing threshold pending interrupts (when enabled) |

### 5.1.2.204 CPSW\_NC\_CPDMA\_INT\_TH5\_PENDTHRESH\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_TH5\_PENDTHRESH\_REG Register (Offset = 340D4h) [reset = 0h]

CPDMA THost Threshold Pending Register

Return to [Summary Table](#)

**Table 5-611. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 40D4h       |

**Figure 5-204. CPSW\_NC\_CPDMA\_INT\_TH5\_PENDTHRESH\_REG Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH5_PENDTHRESH |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-613. CPSW\_NC\_CPDMA\_INT\_TH5\_PENDTHRESH\_REG Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                     |
|------|----------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED       | NONE | 0h    | Reserved                                                                                        |
| 7:0  | TH5_PENDTHRESH | R/W  | 0h    | This field contains the threshold value for issuing threshold pending interrupts (when enabled) |

### 5.1.2.205 CPSW\_NC\_CPDMA\_INT\_TH6\_PENDTHRESH\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_TH6\_PENDTHRESH\_REG Register (Offset = 340D8h) [reset = 0h]

CPDMA THost Threshold Pending Register

Return to [Summary Table](#)

**Table 5-614. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 40D8h       |

**Figure 5-205. CPSW\_NC\_CPDMA\_INT\_TH6\_PENDTHRESH\_REG Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH6_PENDTHRESH |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-616. CPSW\_NC\_CPDMA\_INT\_TH6\_PENDTHRESH\_REG Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                     |
|------|----------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED       | NONE | 0h    | Reserved                                                                                        |
| 7:0  | TH6_PENDTHRESH | R/W  | 0h    | This field contains the threshold value for issuing threshold pending interrupts (when enabled) |

### 5.1.2.206 CPSW\_NC\_CPDMA\_INT\_TH7\_PENDTHRESH\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_TH7\_PENDTHRESH\_REG Register (Offset = 340DCh) [reset = 0h]

CPDMA THost Threshold Pending Register

Return to [Summary Table](#)

**Table 5-617. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 40DCh       |

**Figure 5-206. CPSW\_NC\_CPDMA\_INT\_TH7\_PENDTHRESH\_REG Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH7_PENDTHRESH |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-619. CPSW\_NC\_CPDMA\_INT\_TH7\_PENDTHRESH\_REG Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                     |
|------|----------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED       | NONE | 0h    | Reserved                                                                                        |
| 7:0  | TH7_PENDTHRESH | R/W  | 0h    | This field contains the threshold value for issuing threshold pending interrupts (when enabled) |

### 5.1.2.207 CPSW\_NC\_CPDMA\_INT\_TH0\_FREEBUFFER\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_TH0\_FREEBUFFER\_REG Register (Offset = 340E0h) [reset = 0h]

CPDMA THost Free Buffer Count Register

Return to [Summary Table](#)

**Table 5-620. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 40E0h       |

**Figure 5-207. CPSW\_NC\_CPDMA\_INT\_TH0\_FREEBUFFER\_REG Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TH0_FREEBUFFER |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH0_FREEBUFFER |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-622. CPSW\_NC\_CPDMA\_INT\_TH0\_FREEBUFFER\_REG Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 15:0  | TH0_FREEBUFFER | R/W  | 0h    | This field contains the count of host free buffers available. The th(0..7)_pendthresh value is compared with this field to determine if the THost threshold pending interrupt should be asserted (if enabled). This is a write to increment field. This field rolls over to zero on overflow. If THost threshold pending interrupts are used, the host must initialize this field to the number of available buffers (one register per channel). The port decrements (by the number of buffers in the frame) the associated channel register for each frame. This is a write to increment field. The host must write this field with the number of buffers that have been freed due to host processing. |

### 5.1.2.208 CPSW\_NC\_CPDMA\_INT\_TH1\_FREEBUFFER\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_TH1\_FREEBUFFER\_REG Register (Offset = 340E4h) [reset = 0h]

CPDMA THost Free Buffer Count Register

Return to [Summary Table](#)

**Table 5-623. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 40E4h       |

**Figure 5-208. CPSW\_NC\_CPDMA\_INT\_TH1\_FREEBUFFER\_REG Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TH1_FREEBUFFER |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH1_FREEBUFFER |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-625. CPSW\_NC\_CPDMA\_INT\_TH1\_FREEBUFFER\_REG Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 15:0  | TH1_FREEBUFFER | R/W  | 0h    | This field contains the count of host free buffers available. The th(0..7)_pendthresh value is compared with this field to determine if the THost threshold pending interrupt should be asserted (if enabled). This is a write to increment field. This field rolls over to zero on overflow. If THost threshold pending interrupts are used, the host must initialize this field to the number of available buffers (one register per channel). The port decrements (by the number of buffers in the frame) the associated channel register for each frame. This is a write to increment field. The host must write this field with the number of buffers that have been freed due to host processing. |



### 5.1.2.209 CPSW\_NC\_CPDMA\_INT\_TH2\_FREEBUFFER\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_TH2\_FREEBUFFER\_REG Register (Offset = 340E8h) [reset = 0h]

CPDMA THost Free Buffer Count Register

Return to [Summary Table](#)

**Table 5-626. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 40E8h       |

**Figure 5-209. CPSW\_NC\_CPDMA\_INT\_TH2\_FREEBUFFER\_REG Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TH2_FREEBUFFER |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH2_FREEBUFFER |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-628. CPSW\_NC\_CPDMA\_INT\_TH2\_FREEBUFFER\_REG Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 15:0  | TH2_FREEBUFFER | R/W  | 0h    | This field contains the count of host free buffers available. The th(0..7)_pendthresh value is compared with this field to determine if the THost threshold pending interrupt should be asserted (if enabled). This is a write to increment field. This field rolls over to zero on overflow. If THost threshold pending interrupts are used, the host must initialize this field to the number of available buffers (one register per channel). The port decrements (by the number of buffers in the frame) the associated channel register for each frame. This is a write to increment field. The host must write this field with the number of buffers that have been freed due to host processing. |

### 5.1.2.210 CPSW\_NC\_CPDMA\_INT\_TH3\_FREEBUFFER\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_TH3\_FREEBUFFER\_REG Register (Offset = 340ECh) [reset = 0h]

CPDMA THost Free Buffer Count Register

Return to [Summary Table](#)

**Table 5-629. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 40ECh       |

**Figure 5-210. CPSW\_NC\_CPDMA\_INT\_TH3\_FREEBUFFER\_REG Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TH3_FREEBUFFER |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH3_FREEBUFFER |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-631. CPSW\_NC\_CPDMA\_INT\_TH3\_FREEBUFFER\_REG Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 15:0  | TH3_FREEBUFFER | R/W  | 0h    | This field contains the count of host free buffers available. The th(0..7)_pendthresh value is compared with this field to determine if the THost threshold pending interrupt should be asserted (if enabled). This is a write to increment field. This field rolls over to zero on overflow. If THost threshold pending interrupts are used, the host must initialize this field to the number of available buffers (one register per channel). The port decrements (by the number of buffers in the frame) the associated channel register for each frame. This is a write to increment field. The host must write this field with the number of buffers that have been freed due to host processing. |

### 5.1.2.211 CPSW\_NC\_CPDMA\_INT\_TH4\_FREEBUFFER\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_TH4\_FREEBUFFER\_REG Register (Offset = 340F0h) [reset = 0h]

CPDMA THost Free Buffer Count Register

Return to [Summary Table](#)

**Table 5-632. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 40F0h       |

**Figure 5-211. CPSW\_NC\_CPDMA\_INT\_TH4\_FREEBUFFER\_REG Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TH4_FREEBUFFER |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH4_FREEBUFFER |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-634. CPSW\_NC\_CPDMA\_INT\_TH4\_FREEBUFFER\_REG Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 15:0  | TH4_FREEBUFFER | R/W  | 0h    | This field contains the count of host free buffers available. The th(0..7)_pendthresh value is compared with this field to determine if the THost threshold pending interrupt should be asserted (if enabled). This is a write to increment field. This field rolls over to zero on overflow. If THost threshold pending interrupts are used, the host must initialize this field to the number of available buffers (one register per channel). The port decrements (by the number of buffers in the frame) the associated channel register for each frame. This is a write to increment field. The host must write this field with the number of buffers that have been freed due to host processing. |

### 5.1.2.212 CPSW\_NC\_CPDMA\_INT\_TH5\_FREEBUFFER\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_TH5\_FREEBUFFER\_REG Register (Offset = 340F4h) [reset = 0h]

CPDMA THost Free Buffer Count Register

Return to [Summary Table](#)

**Table 5-635. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 40F4h       |

**Figure 5-212. CPSW\_NC\_CPDMA\_INT\_TH5\_FREEBUFFER\_REG Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TH5_FREEBUFFER |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH5_FREEBUFFER |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-637. CPSW\_NC\_CPDMA\_INT\_TH5\_FREEBUFFER\_REG Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 15:0  | TH5_FREEBUFFER | R/W  | 0h    | This field contains the count of host free buffers available. The th(0..7)_pendthresh value is compared with this field to determine if the THost threshold pending interrupt should be asserted (if enabled). This is a write to increment field. This field rolls over to zero on overflow. If THost threshold pending interrupts are used, the host must initialize this field to the number of available buffers (one register per channel). The port decrements (by the number of buffers in the frame) the associated channel register for each frame. This is a write to increment field. The host must write this field with the number of buffers that have been freed due to host processing. |

### 5.1.2.213 CPSW\_NC\_CPDMA\_INT\_TH6\_FREEBUFFER\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_TH6\_FREEBUFFER\_REG Register (Offset = 340F8h) [reset = 0h]

CPDMA THost Free Buffer Count Register

Return to [Summary Table](#)

**Table 5-638. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 40F8h       |

**Figure 5-213. CPSW\_NC\_CPDMA\_INT\_TH6\_FREEBUFFER\_REG Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TH6_FREEBUFFER |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH6_FREEBUFFER |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-640. CPSW\_NC\_CPDMA\_INT\_TH6\_FREEBUFFER\_REG Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 15:0  | TH6_FREEBUFFER | R/W  | 0h    | This field contains the count of host free buffers available. The th(0..7)_pendthresh value is compared with this field to determine if the THost threshold pending interrupt should be asserted (if enabled). This is a write to increment field. This field rolls over to zero on overflow. If THost threshold pending interrupts are used, the host must initialize this field to the number of available buffers (one register per channel). The port decrements (by the number of buffers in the frame) the associated channel register for each frame. This is a write to increment field. The host must write this field with the number of buffers that have been freed due to host processing. |

### 5.1.2.214 CPSW\_NC\_CPDMA\_INT\_TH7\_FREEBUFFER\_REG Register

#### 1 CPSW\_NC\_CPDMA\_INT\_TH7\_FREEBUFFER\_REG Register (Offset = 340FCh) [reset = 0h]

CPDMA THost Free Buffer Count Register

Return to [Summary Table](#)

**Table 5-641. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 40FCh       |

**Figure 5-214. CPSW\_NC\_CPDMA\_INT\_TH7\_FREEBUFFER\_REG Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED       |    |    |    |    |    |    |    |
| NONE           |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TH7_FREEBUFFER |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH7_FREEBUFFER |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-643. CPSW\_NC\_CPDMA\_INT\_TH7\_FREEBUFFER\_REG Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 15:0  | TH7_FREEBUFFER | R/W  | 0h    | This field contains the count of host free buffers available. The th(0..7)_pendthresh value is compared with this field to determine if the THost threshold pending interrupt should be asserted (if enabled). This is a write to increment field. This field rolls over to zero on overflow. If THost threshold pending interrupts are used, the host must initialize this field to the number of available buffers (one register per channel). The port decrements (by the number of buffers in the frame) the associated channel register for each frame. This is a write to increment field. The host must write this field with the number of buffers that have been freed due to host processing. |

### 5.1.2.215 CPSW\_NC\_CPDMA\_SRAM\_FH0\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_FH0\_HDP\_REG Register (Offset = 34200h) [reset = 0h]

CPDMA FHost Channel 0 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-644. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4200h       |

**Figure 5-215. CPSW\_NC\_CPDMA\_SRAM\_FH0\_HDP\_REG Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FH0_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FH0_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FH0_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FH0_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-646. CPSW\_NC\_CPDMA\_SRAM\_FH0\_HDP\_REG Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                   |
|------|---------|------|-------|-----------------------------------------------|
| 31:0 | FH0_HDP | R/W  | 0h    | CPDMA FHost Channel 0 Head Descriptor Pointer |

### 5.1.2.216 CPSW\_NC\_CPDMA\_SRAM\_FH1\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_FH1\_HDP\_REG Register (Offset = 34204h) [reset = 0h]

CPDMA FHost Channel 1 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-647. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4204h       |

**Figure 5-216. CPSW\_NC\_CPDMA\_SRAM\_FH1\_HDP\_REG Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FH1_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FH1_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FH1_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FH1_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-649. CPSW\_NC\_CPDMA\_SRAM\_FH1\_HDP\_REG Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                   |
|------|---------|------|-------|-----------------------------------------------|
| 31:0 | FH1_HDP | R/W  | 0h    | CPDMA FHost Channel 1 Head Descriptor Pointer |



### 5.1.2.217 CPSW\_NC\_CPDMA\_SRAM\_FH2\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_FH2\_HDP\_REG Register (Offset = 34208h) [reset = 0h]

CPDMA FHost Channel 2 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-650. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4208h       |

**Figure 5-217. CPSW\_NC\_CPDMA\_SRAM\_FH2\_HDP\_REG Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FH2_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FH2_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FH2_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FH2_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-652. CPSW\_NC\_CPDMA\_SRAM\_FH2\_HDP\_REG Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                   |
|------|---------|------|-------|-----------------------------------------------|
| 31:0 | FH2_HDP | R/W  | 0h    | CPDMA FHost Channel 2 Head Descriptor Pointer |

### 5.1.2.218 CPSW\_NC\_CPDMA\_SRAM\_FH3\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_FH3\_HDP\_REG Register (Offset = 3420Ch) [reset = 0h]

CPDMA FHost Channel 3 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-653. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 420Ch       |

**Figure 5-218. CPSW\_NC\_CPDMA\_SRAM\_FH3\_HDP\_REG Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FH3_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FH3_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FH3_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FH3_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-655. CPSW\_NC\_CPDMA\_SRAM\_FH3\_HDP\_REG Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                   |
|------|---------|------|-------|-----------------------------------------------|
| 31:0 | FH3_HDP | R/W  | 0h    | CPDMA FHost Channel 3 Head Descriptor Pointer |

### 5.1.2.219 CPSW\_NC\_CPDMA\_SRAM\_FH4\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_FH4\_HDP\_REG Register (Offset = 34210h) [reset = 0h]

CPDMA FHost Channel 4 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-656. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4210h       |

**Figure 5-219. CPSW\_NC\_CPDMA\_SRAM\_FH4\_HDP\_REG Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FH4_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FH4_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FH4_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FH4_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-658. CPSW\_NC\_CPDMA\_SRAM\_FH4\_HDP\_REG Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                   |
|------|---------|------|-------|-----------------------------------------------|
| 31:0 | FH4_HDP | R/W  | 0h    | CPDMA FHost Channel 4 Head Descriptor Pointer |

### 5.1.2.220 CPSW\_NC\_CPDMA\_SRAM\_FH5\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_FH5\_HDP\_REG Register (Offset = 34214h) [reset = 0h]

CPDMA FHost Channel 5 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-659. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4214h       |

**Figure 5-220. CPSW\_NC\_CPDMA\_SRAM\_FH5\_HDP\_REG Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FH5_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FH5_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FH5_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FH5_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-661. CPSW\_NC\_CPDMA\_SRAM\_FH5\_HDP\_REG Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                   |
|------|---------|------|-------|-----------------------------------------------|
| 31:0 | FH5_HDP | R/W  | 0h    | CPDMA FHost Channel 5 Head Descriptor Pointer |

### 5.1.2.221 CPSW\_NC\_CPDMA\_SRAM\_FH6\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_FH6\_HDP\_REG Register (Offset = 34218h) [reset = 0h]

CPDMA FHost Channel 6 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-662. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4218h       |

**Figure 5-221. CPSW\_NC\_CPDMA\_SRAM\_FH6\_HDP\_REG Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FH6_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FH6_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FH6_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FH6_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-664. CPSW\_NC\_CPDMA\_SRAM\_FH6\_HDP\_REG Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                   |
|------|---------|------|-------|-----------------------------------------------|
| 31:0 | FH6_HDP | R/W  | 0h    | CPDMA FHost Channel 6 Head Descriptor Pointer |

### 5.1.2.222 CPSW\_NC\_CPDMA\_SRAM\_FH7\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_FH7\_HDP\_REG Register (Offset = 3421Ch) [reset = 0h]

CPDMA FHost Channel 7 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-665. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 421Ch       |

**Figure 5-222. CPSW\_NC\_CPDMA\_SRAM\_FH7\_HDP\_REG Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FH7_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FH7_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FH7_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FH7_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-667. CPSW\_NC\_CPDMA\_SRAM\_FH7\_HDP\_REG Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                   |
|------|---------|------|-------|-----------------------------------------------|
| 31:0 | FH7_HDP | R/W  | 0h    | CPDMA FHost Channel 7 Head Descriptor Pointer |

### 5.1.2.223 CPSW\_NC\_CPDMA\_SRAM\_TH0\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TH0\_HDP\_REG Register (Offset = 34220h) [reset = 0h]

CPDMA THost Channel 0 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-668. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4220h       |

**Figure 5-223. CPSW\_NC\_CPDMA\_SRAM\_TH0\_HDP\_REG Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TH0_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TH0_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TH0_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH0_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-670. CPSW\_NC\_CPDMA\_SRAM\_TH0\_HDP\_REG Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                   |
|------|---------|------|-------|-----------------------------------------------|
| 31:0 | TH0_HDP | R/W  | 0h    | CPDMA THost Channel 0 Head Descriptor Pointer |

### 5.1.2.224 CPSW\_NC\_CPDMA\_SRAM\_TH1\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TH1\_HDP\_REG Register (Offset = 34224h) [reset = 0h]

CPDMA THost Channel 1 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-671. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4224h       |

**Figure 5-224. CPSW\_NC\_CPDMA\_SRAM\_TH1\_HDP\_REG Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TH1_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TH1_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TH1_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH1_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-673. CPSW\_NC\_CPDMA\_SRAM\_TH1\_HDP\_REG Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                   |
|------|---------|------|-------|-----------------------------------------------|
| 31:0 | TH1_HDP | R/W  | 0h    | CPDMA THost Channel 1 Head Descriptor Pointer |



### 5.1.2.225 CPSW\_NC\_CPDMA\_SRAM\_TH2\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TH2\_HDP\_REG Register (Offset = 34228h) [reset = 0h]

CPDMA THost Channel 2 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-674. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4228h       |

**Figure 5-225. CPSW\_NC\_CPDMA\_SRAM\_TH2\_HDP\_REG Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TH2_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TH2_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TH2_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH2_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-676. CPSW\_NC\_CPDMA\_SRAM\_TH2\_HDP\_REG Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                   |
|------|---------|------|-------|-----------------------------------------------|
| 31:0 | TH2_HDP | R/W  | 0h    | CPDMA THost Channel 2 Head Descriptor Pointer |

### 5.1.2.226 CPSW\_NC\_CPDMA\_SRAM\_TH3\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TH3\_HDP\_REG Register (Offset = 3422Ch) [reset = 0h]

CPDMA THost Channel 3 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-677. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 422Ch       |

**Figure 5-226. CPSW\_NC\_CPDMA\_SRAM\_TH3\_HDP\_REG Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TH3_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TH3_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TH3_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH3_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-679. CPSW\_NC\_CPDMA\_SRAM\_TH3\_HDP\_REG Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                   |
|------|---------|------|-------|-----------------------------------------------|
| 31:0 | TH3_HDP | R/W  | 0h    | CPDMA THost Channel 3 Head Descriptor Pointer |

### 5.1.2.227 CPSW\_NC\_CPDMA\_SRAM\_TH4\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TH4\_HDP\_REG Register (Offset = 34230h) [reset = 0h]

CPDMA THost Channel 4 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-680. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4230h       |

**Figure 5-227. CPSW\_NC\_CPDMA\_SRAM\_TH4\_HDP\_REG Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TH4_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TH4_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TH4_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH4_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-682. CPSW\_NC\_CPDMA\_SRAM\_TH4\_HDP\_REG Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                   |
|------|---------|------|-------|-----------------------------------------------|
| 31:0 | TH4_HDP | R/W  | 0h    | CPDMA THost Channel 4 Head Descriptor Pointer |

### 5.1.2.228 CPSW\_NC\_CPDMA\_SRAM\_TH5\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TH5\_HDP\_REG Register (Offset = 34234h) [reset = 0h]

CPDMA THost Channel 5 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-683. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4234h       |

**Figure 5-228. CPSW\_NC\_CPDMA\_SRAM\_TH5\_HDP\_REG Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TH5_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TH5_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TH5_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH5_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-685. CPSW\_NC\_CPDMA\_SRAM\_TH5\_HDP\_REG Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                   |
|------|---------|------|-------|-----------------------------------------------|
| 31:0 | TH5_HDP | R/W  | 0h    | CPDMA THost Channel 5 Head Descriptor Pointer |

### 5.1.2.229 CPSW\_NC\_CPDMA\_SRAM\_TH6\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TH6\_HDP\_REG Register (Offset = 34238h) [reset = 0h]

CPDMA THost Channel 6 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-686. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4238h       |

**Figure 5-229. CPSW\_NC\_CPDMA\_SRAM\_TH6\_HDP\_REG Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TH6_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TH6_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TH6_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH6_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-688. CPSW\_NC\_CPDMA\_SRAM\_TH6\_HDP\_REG Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                   |
|------|---------|------|-------|-----------------------------------------------|
| 31:0 | TH6_HDP | R/W  | 0h    | CPDMA THost Channel 6 Head Descriptor Pointer |

### 5.1.2.230 CPSW\_NC\_CPDMA\_SRAM\_TH7\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TH7\_HDP\_REG Register (Offset = 3423Ch) [reset = 0h]

CPDMA THost Channel 7 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-689. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 423Ch       |

**Figure 5-230. CPSW\_NC\_CPDMA\_SRAM\_TH7\_HDP\_REG Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TH7_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TH7_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TH7_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH7_HDP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-691. CPSW\_NC\_CPDMA\_SRAM\_TH7\_HDP\_REG Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                   |
|------|---------|------|-------|-----------------------------------------------|
| 31:0 | TH7_HDP | R/W  | 0h    | CPDMA THost Channel 7 Head Descriptor Pointer |

### 5.1.2.231 CPSW\_NC\_CPDMA\_SRAM\_FH0\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_FH0\_CP\_REG Register (Offset = 34240h) [reset = 0h]

CPDMA FHost Channel 0 Completion Pointer

Return to [Summary Table](#)

**Table 5-692. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4240h       |

**Figure 5-231. CPSW\_NC\_CPDMA\_SRAM\_FH0\_CP\_REG Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FH0_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FH0_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FH0_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FH0_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-694. CPSW\_NC\_CPDMA\_SRAM\_FH0\_CP\_REG Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                              |
|------|--------|------|-------|------------------------------------------|
| 31:0 | FH0_CP | R/W  | 0h    | CPDMA FHost Channel 0 Completion Pointer |

### 5.1.2.232 CPSW\_NC\_CPDMA\_SRAM\_FH1\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_FH1\_CP\_REG Register (Offset = 34244h) [reset = 0h]

CPDMA FHost Channel 1 Completion Pointer

Return to [Summary Table](#)

**Table 5-695. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4244h       |

**Figure 5-232. CPSW\_NC\_CPDMA\_SRAM\_FH1\_CP\_REG Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FH1_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FH1_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FH1_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FH1_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-697. CPSW\_NC\_CPDMA\_SRAM\_FH1\_CP\_REG Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                              |
|------|--------|------|-------|------------------------------------------|
| 31:0 | FH1_CP | R/W  | 0h    | CPDMA FHost Channel 1 Completion Pointer |



### 5.1.2.233 CPSW\_NC\_CPDMA\_SRAM\_FH2\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_FH2\_CP\_REG Register (Offset = 34248h) [reset = 0h]

CPDMA FHost Channel 2 Completion Pointer

Return to [Summary Table](#)

**Table 5-698. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4248h       |

**Figure 5-233. CPSW\_NC\_CPDMA\_SRAM\_FH2\_CP\_REG Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FH2_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FH2_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FH2_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FH2_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-700. CPSW\_NC\_CPDMA\_SRAM\_FH2\_CP\_REG Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                              |
|------|--------|------|-------|------------------------------------------|
| 31:0 | FH2_CP | R/W  | 0h    | CPDMA FHost Channel 2 Completion Pointer |

### 5.1.2.234 CPSW\_NC\_CPDMA\_SRAM\_FH3\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_FH3\_CP\_REG Register (Offset = 3424Ch) [reset = 0h]

CPDMA FHost Channel 3 Completion Pointer

Return to [Summary Table](#)

**Table 5-701. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 424Ch       |

**Figure 5-234. CPSW\_NC\_CPDMA\_SRAM\_FH3\_CP\_REG Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FH3_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FH3_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FH3_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FH3_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-703. CPSW\_NC\_CPDMA\_SRAM\_FH3\_CP\_REG Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                              |
|------|--------|------|-------|------------------------------------------|
| 31:0 | FH3_CP | R/W  | 0h    | CPDMA FHost Channel 3 Completion Pointer |

### 5.1.2.235 CPSW\_NC\_CPDMA\_SRAM\_FH4\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_FH4\_CP\_REG Register (Offset = 34250h) [reset = 0h]

CPDMA FHost Channel 4 Completion Pointer

Return to [Summary Table](#)

**Table 5-704. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4250h       |

**Figure 5-235. CPSW\_NC\_CPDMA\_SRAM\_FH4\_CP\_REG Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FH4_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FH4_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FH4_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FH4_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-706. CPSW\_NC\_CPDMA\_SRAM\_FH4\_CP\_REG Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                              |
|------|--------|------|-------|------------------------------------------|
| 31:0 | FH4_CP | R/W  | 0h    | CPDMA FHost Channel 4 Completion Pointer |

### 5.1.2.236 CPSW\_NC\_CPDMA\_SRAM\_FH5\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_FH5\_CP\_REG Register (Offset = 34254h) [reset = 0h]

CPDMA FHost Channel 5 Completion Pointer

Return to [Summary Table](#)

**Table 5-707. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4254h       |

**Figure 5-236. CPSW\_NC\_CPDMA\_SRAM\_FH5\_CP\_REG Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FH5_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FH5_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FH5_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FH5_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-709. CPSW\_NC\_CPDMA\_SRAM\_FH5\_CP\_REG Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                              |
|------|--------|------|-------|------------------------------------------|
| 31:0 | FH5_CP | R/W  | 0h    | CPDMA FHost Channel 5 Completion Pointer |

### 5.1.2.237 CPSW\_NC\_CPDMA\_SRAM\_FH6\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_FH6\_CP\_REG Register (Offset = 34258h) [reset = 0h]

CPDMA FHost Channel 6 Completion Pointer

Return to [Summary Table](#)

**Table 5-710. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4258h       |

**Figure 5-237. CPSW\_NC\_CPDMA\_SRAM\_FH6\_CP\_REG Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FH6_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FH6_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FH6_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FH6_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-712. CPSW\_NC\_CPDMA\_SRAM\_FH6\_CP\_REG Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                              |
|------|--------|------|-------|------------------------------------------|
| 31:0 | FH6_CP | R/W  | 0h    | CPDMA FHost Channel 6 Completion Pointer |

### 5.1.2.238 CPSW\_NC\_CPDMA\_SRAM\_FH7\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_FH7\_CP\_REG Register (Offset = 3425Ch) [reset = 0h]

CPDMA FHost Channel 7 Completion Pointer

Return to [Summary Table](#)

**Table 5-713. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 425Ch       |

**Figure 5-238. CPSW\_NC\_CPDMA\_SRAM\_FH7\_CP\_REG Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FH7_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FH7_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FH7_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FH7_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-715. CPSW\_NC\_CPDMA\_SRAM\_FH7\_CP\_REG Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                              |
|------|--------|------|-------|------------------------------------------|
| 31:0 | FH7_CP | R/W  | 0h    | CPDMA FHost Channel 7 Completion Pointer |

### 5.1.2.239 CPSW\_NC\_CPDMA\_SRAM\_TH0\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TH0\_CP\_REG Register (Offset = 34260h) [reset = 0h]

CPDMA THost Channel 0 Completion Pointer

Return to [Summary Table](#)

**Table 5-716. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4260h       |

**Figure 5-239. CPSW\_NC\_CPDMA\_SRAM\_TH0\_CP\_REG Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TH0_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TH0_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TH0_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH0_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-718. CPSW\_NC\_CPDMA\_SRAM\_TH0\_CP\_REG Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                              |
|------|--------|------|-------|------------------------------------------|
| 31:0 | TH0_CP | R/W  | 0h    | CPDMA THost Channel 0 Completion Pointer |

### 5.1.2.240 CPSW\_NC\_CPDMA\_SRAM\_TH1\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TH1\_CP\_REG Register (Offset = 34264h) [reset = 0h]

CPDMA THost Channel 1 Completion Pointer

Return to [Summary Table](#)

**Table 5-719. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4264h       |

**Figure 5-240. CPSW\_NC\_CPDMA\_SRAM\_TH1\_CP\_REG Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TH1_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TH1_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TH1_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH1_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-721. CPSW\_NC\_CPDMA\_SRAM\_TH1\_CP\_REG Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                              |
|------|--------|------|-------|------------------------------------------|
| 31:0 | TH1_CP | R/W  | 0h    | CPDMA THost Channel 1 Completion Pointer |



### 5.1.2.241 CPSW\_NC\_CPDMA\_SRAM\_TH2\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TH2\_CP\_REG Register (Offset = 34268h) [reset = 0h]

CPDMA THost Channel 2 Completion Pointer

Return to [Summary Table](#)

**Table 5-722. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4268h       |

**Figure 5-241. CPSW\_NC\_CPDMA\_SRAM\_TH2\_CP\_REG Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TH2_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TH2_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TH2_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH2_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-724. CPSW\_NC\_CPDMA\_SRAM\_TH2\_CP\_REG Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                              |
|------|--------|------|-------|------------------------------------------|
| 31:0 | TH2_CP | R/W  | 0h    | CPDMA THost Channel 2 Completion Pointer |

### 5.1.2.242 CPSW\_NC\_CPDMA\_SRAM\_TH3\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TH3\_CP\_REG Register (Offset = 3426Ch) [reset = 0h]

CPDMA THost Channel 3 Completion Pointer

Return to [Summary Table](#)

**Table 5-725. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 426Ch       |

**Figure 5-242. CPSW\_NC\_CPDMA\_SRAM\_TH3\_CP\_REG Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TH3_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TH3_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TH3_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH3_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-727. CPSW\_NC\_CPDMA\_SRAM\_TH3\_CP\_REG Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                              |
|------|--------|------|-------|------------------------------------------|
| 31:0 | TH3_CP | R/W  | 0h    | CPDMA THost Channel 3 Completion Pointer |

### 5.1.2.243 CPSW\_NC\_CPDMA\_SRAM\_TH4\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TH4\_CP\_REG Register (Offset = 34270h) [reset = 0h]

CPDMA THost Channel 4 Completion Pointer

Return to [Summary Table](#)

**Table 5-728. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4270h       |

**Figure 5-243. CPSW\_NC\_CPDMA\_SRAM\_TH4\_CP\_REG Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TH4_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TH4_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TH4_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH4_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-730. CPSW\_NC\_CPDMA\_SRAM\_TH4\_CP\_REG Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                              |
|------|--------|------|-------|------------------------------------------|
| 31:0 | TH4_CP | R/W  | 0h    | CPDMA THost Channel 4 Completion Pointer |

### 5.1.2.244 CPSW\_NC\_CPDMA\_SRAM\_TH5\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TH5\_CP\_REG Register (Offset = 34274h) [reset = 0h]

CPDMA THost Channel 5 Completion Pointer

Return to [Summary Table](#)

**Table 5-731. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4274h       |

**Figure 5-244. CPSW\_NC\_CPDMA\_SRAM\_TH5\_CP\_REG Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TH5_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TH5_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TH5_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH5_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-733. CPSW\_NC\_CPDMA\_SRAM\_TH5\_CP\_REG Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                              |
|------|--------|------|-------|------------------------------------------|
| 31:0 | TH5_CP | R/W  | 0h    | CPDMA THost Channel 5 Completion Pointer |

### 5.1.2.245 CPSW\_NC\_CPDMA\_SRAM\_TH6\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TH6\_CP\_REG Register (Offset = 34278h) [reset = 0h]

CPDMA THost Channel 6 Completion Pointer

Return to [Summary Table](#)

**Table 5-734. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4278h       |

**Figure 5-245. CPSW\_NC\_CPDMA\_SRAM\_TH6\_CP\_REG Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TH6_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TH6_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TH6_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH6_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-736. CPSW\_NC\_CPDMA\_SRAM\_TH6\_CP\_REG Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                              |
|------|--------|------|-------|------------------------------------------|
| 31:0 | TH6_CP | R/W  | 0h    | CPDMA THost Channel 6 Completion Pointer |

### 5.1.2.246 CPSW\_NC\_CPDMA\_SRAM\_TH7\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TH7\_CP\_REG Register (Offset = 3427Ch) [reset = 0h]

CPDMA THost Channel 7 Completion Pointer

Return to [Summary Table](#)

**Table 5-737. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 427Ch       |

**Figure 5-246. CPSW\_NC\_CPDMA\_SRAM\_TH7\_CP\_REG Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TH7_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TH7_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TH7_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TH7_CP |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-739. CPSW\_NC\_CPDMA\_SRAM\_TH7\_CP\_REG Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                              |
|------|--------|------|-------|------------------------------------------|
| 31:0 | TH7_CP | R/W  | 0h    | CPDMA THost Channel 7 Completion Pointer |

### 5.1.2.247 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH0\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH0\_HDP\_REG Register (Offset = 34300h) [reset = 0h]

Test CPDMA FHost Channel 0 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-740. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4300h       |

**Figure 5-247. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH0\_HDP\_REG Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_FH0_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_FH0_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_FH0_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_FH0_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-742. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH0\_HDP\_REG Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                        |
|------|--------------|------|-------|----------------------------------------------------|
| 31:0 | TEST_FH0_HDP | R/W  | 0h    | Test CPDMA FHost Channel 0 Head Descriptor Pointer |

### 5.1.2.248 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH1\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH1\_HDP\_REG Register (Offset = 34304h) [reset = 0h]

Test CPDMA FHost Channel 1 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-743. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4304h       |

**Figure 5-248. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH1\_HDP\_REG Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_FH1_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_FH1_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_FH1_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_FH1_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-745. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH1\_HDP\_REG Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                        |
|------|--------------|------|-------|----------------------------------------------------|
| 31:0 | TEST_FH1_HDP | R/W  | 0h    | Test CPDMA FHost Channel 1 Head Descriptor Pointer |



### 5.1.2.249 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH2\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH2\_HDP\_REG Register (Offset = 34308h) [reset = 0h]

Test CPDMA FHost Channel 2 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-746. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4308h       |

**Figure 5-249. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH2\_HDP\_REG Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_FH2_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_FH2_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_FH2_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_FH2_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-748. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH2\_HDP\_REG Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                        |
|------|--------------|------|-------|----------------------------------------------------|
| 31:0 | TEST_FH2_HDP | R/W  | 0h    | Test CPDMA FHost Channel 2 Head Descriptor Pointer |

### 5.1.2.250 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH3\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH3\_HDP\_REG Register (Offset = 3430Ch) [reset = 0h]

Test CPDMA FHost Channel 3 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-749. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 430Ch       |

**Figure 5-250. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH3\_HDP\_REG Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_FH3_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_FH3_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_FH3_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_FH3_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-751. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH3\_HDP\_REG Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                        |
|------|--------------|------|-------|----------------------------------------------------|
| 31:0 | TEST_FH3_HDP | R/W  | 0h    | Test CPDMA FHost Channel 3 Head Descriptor Pointer |

### 5.1.2.251 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH4\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH4\_HDP\_REG Register (Offset = 34310h) [reset = 0h]

Test CPDMA FHost Channel 4 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-752. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4310h       |

**Figure 5-251. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH4\_HDP\_REG Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_FH4_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_FH4_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_FH4_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_FH4_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-754. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH4\_HDP\_REG Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                        |
|------|--------------|------|-------|----------------------------------------------------|
| 31:0 | TEST_FH4_HDP | R/W  | 0h    | Test CPDMA FHost Channel 4 Head Descriptor Pointer |

### 5.1.2.252 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH5\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH5\_HDP\_REG Register (Offset = 34314h) [reset = 0h]

Test CPDMA FHost Channel 5 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-755. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4314h       |

**Figure 5-252. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH5\_HDP\_REG Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_FH5_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_FH5_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_FH5_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_FH5_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-757. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH5\_HDP\_REG Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                        |
|------|--------------|------|-------|----------------------------------------------------|
| 31:0 | TEST_FH5_HDP | R/W  | 0h    | Test CPDMA FHost Channel 5 Head Descriptor Pointer |

### 5.1.2.253 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH6\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH6\_HDP\_REG Register (Offset = 34318h) [reset = 0h]

Test CPDMA FHost Channel 6 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-758. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4318h       |

**Figure 5-253. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH6\_HDP\_REG Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_FH6_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_FH6_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_FH6_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_FH6_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-760. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH6\_HDP\_REG Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                        |
|------|--------------|------|-------|----------------------------------------------------|
| 31:0 | TEST_FH6_HDP | R/W  | 0h    | Test CPDMA FHost Channel 6 Head Descriptor Pointer |

### 5.1.2.254 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH7\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH7\_HDP\_REG Register (Offset = 3431Ch) [reset = 0h]

Test CPDMA FHost Channel 7 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-761. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 431Ch       |

**Figure 5-254. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH7\_HDP\_REG Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_FH7_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_FH7_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_FH7_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_FH7_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-763. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH7\_HDP\_REG Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                        |
|------|--------------|------|-------|----------------------------------------------------|
| 31:0 | TEST_FH7_HDP | R/W  | 0h    | Test CPDMA FHost Channel 7 Head Descriptor Pointer |

### 5.1.2.255 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH0\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH0\_HDP\_REG Register (Offset = 34320h) [reset = 0h]

Test CPDMA THost Channel 0 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-764. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4320h       |

**Figure 5-255. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH0\_HDP\_REG Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_TH0_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_TH0_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_TH0_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_TH0_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-766. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH0\_HDP\_REG Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                        |
|------|--------------|------|-------|----------------------------------------------------|
| 31:0 | TEST_TH0_HDP | R/W  | 0h    | Test CPDMA THost Channel 0 Head Descriptor Pointer |

### 5.1.2.256 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH1\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH1\_HDP\_REG Register (Offset = 34324h) [reset = 0h]

Test CPDMA THost Channel 1 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-767. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4324h       |

**Figure 5-256. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH1\_HDP\_REG Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_TH1_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_TH1_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_TH1_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_TH1_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-769. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH1\_HDP\_REG Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                        |
|------|--------------|------|-------|----------------------------------------------------|
| 31:0 | TEST_TH1_HDP | R/W  | 0h    | Test CPDMA THost Channel 1 Head Descriptor Pointer |



### 5.1.2.257 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH2\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH2\_HDP\_REG Register (Offset = 34328h) [reset = 0h]

Test CPDMA THost Channel 2 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-770. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4328h       |

**Figure 5-257. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH2\_HDP\_REG Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_TH2_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_TH2_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_TH2_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_TH2_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-772. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH2\_HDP\_REG Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                        |
|------|--------------|------|-------|----------------------------------------------------|
| 31:0 | TEST_TH2_HDP | R/W  | 0h    | Test CPDMA THost Channel 2 Head Descriptor Pointer |

### 5.1.2.258 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH3\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH3\_HDP\_REG Register (Offset = 3432Ch) [reset = 0h]

Test CPDMA THost Channel 3 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-773. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 432Ch       |

**Figure 5-258. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH3\_HDP\_REG Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_TH3_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_TH3_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_TH3_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_TH3_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-775. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH3\_HDP\_REG Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                        |
|------|--------------|------|-------|----------------------------------------------------|
| 31:0 | TEST_TH3_HDP | R/W  | 0h    | Test CPDMA THost Channel 3 Head Descriptor Pointer |

### 5.1.2.259 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH4\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH4\_HDP\_REG Register (Offset = 34330h) [reset = 0h]

Test CPDMA THost Channel 4 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-776. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4330h       |

**Figure 5-259. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH4\_HDP\_REG Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_TH4_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_TH4_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_TH4_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_TH4_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-778. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH4\_HDP\_REG Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                        |
|------|--------------|------|-------|----------------------------------------------------|
| 31:0 | TEST_TH4_HDP | R/W  | 0h    | Test CPDMA THost Channel 4 Head Descriptor Pointer |

### 5.1.2.260 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH5\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH5\_HDP\_REG Register (Offset = 34334h) [reset = 0h]

Test CPDMA THost Channel 5 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-779. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4334h       |

**Figure 5-260. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH5\_HDP\_REG Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_TH5_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_TH5_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_TH5_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_TH5_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-781. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH5\_HDP\_REG Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                        |
|------|--------------|------|-------|----------------------------------------------------|
| 31:0 | TEST_TH5_HDP | R/W  | 0h    | Test CPDMA THost Channel 5 Head Descriptor Pointer |

### 5.1.2.261 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH6\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH6\_HDP\_REG Register (Offset = 34338h) [reset = 0h]

Test CPDMA THost Channel 6 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-782. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4338h       |

**Figure 5-261. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH6\_HDP\_REG Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_TH6_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_TH6_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_TH6_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_TH6_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-784. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH6\_HDP\_REG Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                        |
|------|--------------|------|-------|----------------------------------------------------|
| 31:0 | TEST_TH6_HDP | R/W  | 0h    | Test CPDMA THost Channel 6 Head Descriptor Pointer |

### 5.1.2.262 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH7\_HDP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH7\_HDP\_REG Register (Offset = 3433Ch) [reset = 0h]

Test CPDMA THost Channel 7 Head Descriptor Pointer

Return to [Summary Table](#)

**Table 5-785. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 433Ch       |

**Figure 5-262. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH7\_HDP\_REG Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_TH7_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_TH7_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_TH7_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_TH7_HDP |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-787. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH7\_HDP\_REG Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                        |
|------|--------------|------|-------|----------------------------------------------------|
| 31:0 | TEST_TH7_HDP | R/W  | 0h    | Test CPDMA THost Channel 7 Head Descriptor Pointer |

### 5.1.2.263 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH0\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH0\_CP\_REG Register (Offset = 34340h) [reset = 0h]

Test CPDMA FHost Channel 0 Completion Pointer

Return to [Summary Table](#)

**Table 5-788. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4340h       |

**Figure 5-263. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH0\_CP\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_FH0_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_FH0_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_FH0_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_FH0_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-790. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH0\_CP\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                   |
|------|-------------|------|-------|-----------------------------------------------|
| 31:0 | TEST_FH0_CP | R/W  | 0h    | Test CPDMA FHost Channel 0 Completion Pointer |

### 5.1.2.264 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH1\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH1\_CP\_REG Register (Offset = 34344h) [reset = 0h]

Test CPDMA FHost Channel 1 Completion Pointer

Return to [Summary Table](#)

**Table 5-791. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4344h       |

**Figure 5-264. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH1\_CP\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_FH1_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_FH1_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_FH1_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_FH1_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-793. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH1\_CP\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                   |
|------|-------------|------|-------|-----------------------------------------------|
| 31:0 | TEST_FH1_CP | R/W  | 0h    | Test CPDMA FHost Channel 1 Completion Pointer |



### 5.1.2.265 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH2\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH2\_CP\_REG Register (Offset = 34348h) [reset = 0h]

Test CPDMA FHost Channel 2 Completion Pointer

Return to [Summary Table](#)

**Table 5-794. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4348h       |

**Figure 5-265. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH2\_CP\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_FH2_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_FH2_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_FH2_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_FH2_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-796. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH2\_CP\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                   |
|------|-------------|------|-------|-----------------------------------------------|
| 31:0 | TEST_FH2_CP | R/W  | 0h    | Test CPDMA FHost Channel 2 Completion Pointer |

### 5.1.2.266 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH3\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH3\_CP\_REG Register (Offset = 3434Ch) [reset = 0h]

Test CPDMA FHost Channel 3 Completion Pointer

Return to [Summary Table](#)

**Table 5-797. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 434Ch       |

**Figure 5-266. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH3\_CP\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_FH3_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_FH3_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_FH3_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_FH3_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-799. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH3\_CP\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                   |
|------|-------------|------|-------|-----------------------------------------------|
| 31:0 | TEST_FH3_CP | R/W  | 0h    | Test CPDMA FHost Channel 3 Completion Pointer |

### 5.1.2.267 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH4\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH4\_CP\_REG Register (Offset = 34350h) [reset = 0h]

Test CPDMA FHost Channel 4 Completion Pointer

Return to [Summary Table](#)

**Table 5-800. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4350h       |

**Figure 5-267. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH4\_CP\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_FH4_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_FH4_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_FH4_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_FH4_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-802. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH4\_CP\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                   |
|------|-------------|------|-------|-----------------------------------------------|
| 31:0 | TEST_FH4_CP | R/W  | 0h    | Test CPDMA FHost Channel 4 Completion Pointer |

### 5.1.2.268 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH5\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH5\_CP\_REG Register (Offset = 34354h) [reset = 0h]

Test CPDMA FHost Channel 5 Completion Pointer

Return to [Summary Table](#)

**Table 5-803. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4354h       |

**Figure 5-268. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH5\_CP\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_FH5_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_FH5_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_FH5_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_FH5_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-805. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH5\_CP\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                   |
|------|-------------|------|-------|-----------------------------------------------|
| 31:0 | TEST_FH5_CP | R/W  | 0h    | Test CPDMA FHost Channel 5 Completion Pointer |

### 5.1.2.269 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH6\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH6\_CP\_REG Register (Offset = 34358h) [reset = 0h]

Test CPDMA FHost Channel 6 Completion Pointer

Return to [Summary Table](#)

**Table 5-806. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4358h       |

**Figure 5-269. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH6\_CP\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_FH6_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_FH6_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_FH6_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_FH6_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-808. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH6\_CP\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                   |
|------|-------------|------|-------|-----------------------------------------------|
| 31:0 | TEST_FH6_CP | R/W  | 0h    | Test CPDMA FHost Channel 6 Completion Pointer |

### 5.1.2.270 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH7\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH7\_CP\_REG Register (Offset = 3435Ch) [reset = 0h]

Test CPDMA FHost Channel 7 Completion Pointer

Return to [Summary Table](#)

**Table 5-809. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 435Ch       |

**Figure 5-270. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH7\_CP\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_FH7_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_FH7_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_FH7_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_FH7_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-811. CPSW\_NC\_CPDMA\_SRAM\_TEST\_FH7\_CP\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                   |
|------|-------------|------|-------|-----------------------------------------------|
| 31:0 | TEST_FH7_CP | R/W  | 0h    | Test CPDMA FHost Channel 7 Completion Pointer |

### 5.1.2.271 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH0\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH0\_CP\_REG Register (Offset = 34360h) [reset = 0h]

Test CPDMA THost Channel 0 Completion Pointer

Return to [Summary Table](#)

**Table 5-812. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4360h       |

**Figure 5-271. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH0\_CP\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_TH0_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_TH0_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_TH0_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_TH0_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-814. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH0\_CP\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                   |
|------|-------------|------|-------|-----------------------------------------------|
| 31:0 | TEST_TH0_CP | R/W  | 0h    | Test CPDMA THost Channel 0 Completion Pointer |

### 5.1.2.272 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH1\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH1\_CP\_REG Register (Offset = 34364h) [reset = 0h]

Test CPDMA THost Channel 1 Completion Pointer

Return to [Summary Table](#)

**Table 5-815. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4364h       |

**Figure 5-272. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH1\_CP\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_TH1_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_TH1_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_TH1_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_TH1_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-817. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH1\_CP\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                   |
|------|-------------|------|-------|-----------------------------------------------|
| 31:0 | TEST_TH1_CP | R/W  | 0h    | Test CPDMA THost Channel 1 Completion Pointer |



### 5.1.2.273 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH2\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH2\_CP\_REG Register (Offset = 34368h) [reset = 0h]

Test CPDMA THost Channel 2 Completion Pointer

Return to [Summary Table](#)

**Table 5-818. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4368h       |

**Figure 5-273. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH2\_CP\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_TH2_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_TH2_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_TH2_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_TH2_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-820. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH2\_CP\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                   |
|------|-------------|------|-------|-----------------------------------------------|
| 31:0 | TEST_TH2_CP | R/W  | 0h    | Test CPDMA THost Channel 2 Completion Pointer |

### 5.1.2.274 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH3\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH3\_CP\_REG Register (Offset = 3436Ch) [reset = 0h]

Test CPDMA THost Channel 3 Completion Pointer

Return to [Summary Table](#)

**Table 5-821. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 436Ch       |

**Figure 5-274. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH3\_CP\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_TH3_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_TH3_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_TH3_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_TH3_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-823. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH3\_CP\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                   |
|------|-------------|------|-------|-----------------------------------------------|
| 31:0 | TEST_TH3_CP | R/W  | 0h    | Test CPDMA THost Channel 3 Completion Pointer |

### 5.1.2.275 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH4\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH4\_CP\_REG Register (Offset = 34370h) [reset = 0h]

Test CPDMA THost Channel 4 Completion Pointer

Return to [Summary Table](#)

**Table 5-824. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4370h       |

**Figure 5-275. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH4\_CP\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_TH4_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_TH4_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_TH4_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_TH4_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-826. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH4\_CP\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                   |
|------|-------------|------|-------|-----------------------------------------------|
| 31:0 | TEST_TH4_CP | R/W  | 0h    | Test CPDMA THost Channel 4 Completion Pointer |

### 5.1.2.276 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH5\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH5\_CP\_REG Register (Offset = 34374h) [reset = 0h]

Test CPDMA THost Channel 5 Completion Pointer

Return to [Summary Table](#)

**Table 5-827. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4374h       |

**Figure 5-276. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH5\_CP\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_TH5_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_TH5_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_TH5_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_TH5_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-829. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH5\_CP\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                   |
|------|-------------|------|-------|-----------------------------------------------|
| 31:0 | TEST_TH5_CP | R/W  | 0h    | Test CPDMA THost Channel 5 Completion Pointer |

### 5.1.2.277 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH6\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH6\_CP\_REG Register (Offset = 34378h) [reset = 0h]

Test CPDMA THost Channel 6 Completion Pointer

Return to [Summary Table](#)

**Table 5-830. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 4378h       |

**Figure 5-277. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH6\_CP\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_TH6_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_TH6_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_TH6_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_TH6_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-832. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH6\_CP\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                   |
|------|-------------|------|-------|-----------------------------------------------|
| 31:0 | TEST_TH6_CP | R/W  | 0h    | Test CPDMA THost Channel 6 Completion Pointer |

### 5.1.2.278 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH7\_CP\_REG Register

#### 1 CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH7\_CP\_REG Register (Offset = 3437Ch) [reset = 0h]

Test CPDMA THost Channel 7 Completion Pointer

Return to [Summary Table](#)

**Table 5-833. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 437Ch       |

**Figure 5-278. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH7\_CP\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TEST_TH7_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TEST_TH7_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TEST_TH7_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TEST_TH7_CP |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-835. CPSW\_NC\_CPDMA\_SRAM\_TEST\_TH7\_CP\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                   |
|------|-------------|------|-------|-----------------------------------------------|
| 31:0 | TEST_TH7_CP | R/W  | 0h    | Test CPDMA THost Channel 7 Completion Pointer |

### 5.1.2.279 CPSW\_NC\_STAT\_RXGOODFRAMES\_K Register

#### 1 CPSW\_NC\_STAT\_RXGOODFRAMES\_K Register (Offset = 3A000h) [reset = 0h]

Total number of good frames received

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-836. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A000h + formula |

**Figure 5-279. CPSW\_NC\_STAT\_RXGOODFRAMES\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-838. CPSW\_NC\_STAT\_RXGOODFRAMES\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                          |
|------|-------|------|-------|--------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of good frames received |

### 5.1.2.280 CPSW\_NC\_STAT\_RXBROADCASTFRAMES\_K Register

#### 1 CPSW\_NC\_STAT\_RXBROADCASTFRAMES\_K Register (Offset = 3A004h) [reset = 0h]

Total number of good broadcast frames received

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-839. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A004h + formula |

**Figure 5-280. CPSW\_NC\_STAT\_RXBROADCASTFRAMES\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-841. CPSW\_NC\_STAT\_RXBROADCASTFRAMES\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                    |
|------|-------|------|-------|------------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of good broadcast frames received |



### 5.1.2.281 CPSW\_NC\_STAT\_RXMULTICASTFRAMES\_K Register

#### 1 CPSW\_NC\_STAT\_RXMULTICASTFRAMES\_K Register (Offset = 3A008h) [reset = 0h]

Total number of good multicast frames received

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-842. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A008h + formula |

**Figure 5-281. CPSW\_NC\_STAT\_RXMULTICASTFRAMES\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-844. CPSW\_NC\_STAT\_RXMULTICASTFRAMES\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                    |
|------|-------|------|-------|------------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of good multicast frames received |

### 5.1.2.282 CPSW\_NC\_STAT\_RXPAUSEFRAMES\_K Register

#### 1 CPSW\_NC\_STAT\_RXPAUSEFRAMES\_K Register (Offset = 3A00Ch) [reset = 0h]

Total number of pause frames received

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-845. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A00Ch + formula |

**Figure 5-282. CPSW\_NC\_STAT\_RXPAUSEFRAMES\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-847. CPSW\_NC\_STAT\_RXPAUSEFRAMES\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                           |
|------|-------|------|-------|---------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of pause frames received |

### 5.1.2.283 CPSW\_NC\_STAT\_RXCRCERRORS\_K Register

#### 1 CPSW\_NC\_STAT\_RXCRCERRORS\_K Register (Offset = 3A010h) [reset = 0h]

Total number of CRC errors frames received

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-848. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A010h + formula |

**Figure 5-283. CPSW\_NC\_STAT\_RXCRCERRORS\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-850. CPSW\_NC\_STAT\_RXCRCERRORS\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                |
|------|-------|------|-------|--------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of CRC errors frames received |

### 5.1.2.284 CPSW\_NC\_STAT\_RXALIGNCODEERRORS\_K Register

#### 1 CPSW\_NC\_STAT\_RXALIGNCODEERRORS\_K Register (Offset = 3A014h) [reset = 0h]

Total number of alignment/code errors received

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-851. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A014h + formula |

**Figure 5-284. CPSW\_NC\_STAT\_RXALIGNCODEERRORS\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-853. CPSW\_NC\_STAT\_RXALIGNCODEERRORS\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                    |
|------|-------|------|-------|------------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of alignment/code errors received |

### 5.1.2.285 CPSW\_NC\_STAT\_RXOVERSIZEDFRAMES\_K Register

#### 1 CPSW\_NC\_STAT\_RXOVERSIZEDFRAMES\_K Register (Offset = 3A018h) [reset = 0h]

Total number of oversized frames received

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-854. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A018h + formula |

**Figure 5-285. CPSW\_NC\_STAT\_RXOVERSIZEDFRAMES\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-856. CPSW\_NC\_STAT\_RXOVERSIZEDFRAMES\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                               |
|------|-------|------|-------|-------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of oversized frames received |

### 5.1.2.286 CPSW\_NC\_STAT\_RXJABBERFRAMES\_K Register

#### 1 CPSW\_NC\_STAT\_RXJABBERFRAMES\_K Register (Offset = 3A01Ch) [reset = 0h]

Total number of jabber frames received

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-857. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A01Ch + formula |

**Figure 5-286. CPSW\_NC\_STAT\_RXJABBERFRAMES\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-859. CPSW\_NC\_STAT\_RXJABBERFRAMES\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                            |
|------|-------|------|-------|----------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of jabber frames received |

### 5.1.2.287 CPSW\_NC\_STAT\_RXUNDERSIZEDFRAMES\_K Register

#### 1 CPSW\_NC\_STAT\_RXUNDERSIZEDFRAMES\_K Register (Offset = 3A020h) [reset = 0h]

Total number of undersized frames received

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-860. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A020h + formula |

**Figure 5-287. CPSW\_NC\_STAT\_RXUNDERSIZEDFRAMES\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-862. CPSW\_NC\_STAT\_RXUNDERSIZEDFRAMES\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                |
|------|-------|------|-------|--------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of undersized frames received |

### 5.1.2.288 CPSW\_NC\_STAT\_RXFRAGMENTS\_K Register

#### 1 CPSW\_NC\_STAT\_RXFRAGMENTS\_K Register (Offset = 3A024h) [reset = 0h]

Total number of fragmented frames received

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-863. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A024h + formula |

**Figure 5-288. CPSW\_NC\_STAT\_RXFRAGMENTS\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-865. CPSW\_NC\_STAT\_RXFRAGMENTS\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                |
|------|-------|------|-------|--------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of fragmented frames received |



### 5.1.2.289 CPSW\_NC\_STAT\_ALE\_DROP\_K Register

#### 1 CPSW\_NC\_STAT\_ALE\_DROP\_K Register (Offset = 3A028h) [reset = 0h]

Total number of frames dropped by the ALE

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-866. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A028h + formula |

**Figure 5-289. CPSW\_NC\_STAT\_ALE\_DROP\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-868. CPSW\_NC\_STAT\_ALE\_DROP\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                               |
|------|-------|------|-------|-------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of frames dropped by the ALE |

### 5.1.2.290 CPSW\_NC\_STAT\_ALE\_OVERRUN\_DROP\_K Register

#### 1 CPSW\_NC\_STAT\_ALE\_OVERRUN\_DROP\_K Register (Offset = 3A02Ch) [reset = 0h]

Total number of overrun frames dropped by the ALE

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-869. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A02Ch + formula |

**Figure 5-290. CPSW\_NC\_STAT\_ALE\_OVERRUN\_DROP\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-871. CPSW\_NC\_STAT\_ALE\_OVERRUN\_DROP\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                       |
|------|-------|------|-------|---------------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of overrun frames dropped by the ALE |

### 5.1.2.291 CPSW\_NC\_STAT\_RXOCTETS\_K Register

#### 1 CPSW\_NC\_STAT\_RXOCTETS\_K Register (Offset = 3A030h) [reset = 0h]

Total number of received bytes in good frames

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-872. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A030h + formula |

**Figure 5-291. CPSW\_NC\_STAT\_RXOCTETS\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-874. CPSW\_NC\_STAT\_RXOCTETS\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                   |
|------|-------|------|-------|-----------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of received bytes in good frames |

### 5.1.2.292 CPSW\_NC\_STAT\_TXGOODFRAMES\_K Register

#### 1 CPSW\_NC\_STAT\_TXGOODFRAMES\_K Register (Offset = 3A034h) [reset = 0h]

Total number of good frames transmitted

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-875. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A034h + formula |

**Figure 5-292. CPSW\_NC\_STAT\_TXGOODFRAMES\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-877. CPSW\_NC\_STAT\_TXGOODFRAMES\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                             |
|------|-------|------|-------|-----------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of good frames transmitted |

### 5.1.2.293 CPSW\_NC\_STAT\_TXBROADCASTFRAMES\_K Register

#### 1 CPSW\_NC\_STAT\_TXBROADCASTFRAMES\_K Register (Offset = 3A038h) [reset = 0h]

Total number of good broadcast frames transmitted

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-878. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A038h + formula |

**Figure 5-293. CPSW\_NC\_STAT\_TXBROADCASTFRAMES\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-880. CPSW\_NC\_STAT\_TXBROADCASTFRAMES\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                       |
|------|-------|------|-------|---------------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of good broadcast frames transmitted |

### 5.1.2.294 CPSW\_NC\_STAT\_TXMULTICASTFRAMES\_K Register

#### 1 CPSW\_NC\_STAT\_TXMULTICASTFRAMES\_K Register (Offset = 3A03Ch) [reset = 0h]

Total number of good multicast frames transmitted

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-881. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A03Ch + formula |

**Figure 5-294. CPSW\_NC\_STAT\_TXMULTICASTFRAMES\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-883. CPSW\_NC\_STAT\_TXMULTICASTFRAMES\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                       |
|------|-------|------|-------|---------------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of good multicast frames transmitted |

### 5.1.2.295 CPSW\_NC\_STAT\_TXPAUSEFRAMES\_K Register

#### 1 CPSW\_NC\_STAT\_TXPAUSEFRAMES\_K Register (Offset = 3A040h) [reset = 0h]

Total number of pause frames transmitted

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-884. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A040h + formula |

**Figure 5-295. CPSW\_NC\_STAT\_TXPAUSEFRAMES\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-886. CPSW\_NC\_STAT\_TXPAUSEFRAMES\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                              |
|------|-------|------|-------|------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of pause frames transmitted |

### 5.1.2.296 CPSW\_NC\_STAT\_TXDEFERREDFRAMES\_K Register

#### 1 CPSW\_NC\_STAT\_TXDEFERREDFRAMES\_K Register (Offset = 3A044h) [reset = 0h]

Total number of deferred frames transmitted

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-887. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A044h + formula |

**Figure 5-296. CPSW\_NC\_STAT\_TXDEFERREDFRAMES\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-889. CPSW\_NC\_STAT\_TXDEFERREDFRAMES\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                 |
|------|-------|------|-------|---------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of deferred frames transmitted |



### 5.1.2.297 CPSW\_NC\_STAT\_TXCOLLISIONFRAMES\_K Register

#### 1 CPSW\_NC\_STAT\_TXCOLLISIONFRAMES\_K Register (Offset = 3A048h) [reset = 0h]

Total number of transmitted frames experiencing a collision

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-890. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A048h + formula |

**Figure 5-297. CPSW\_NC\_STAT\_TXCOLLISIONFRAMES\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-892. CPSW\_NC\_STAT\_TXCOLLISIONFRAMES\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                 |
|------|-------|------|-------|-------------------------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of transmitted frames experiencing a collision |

### 5.1.2.298 CPSW\_NC\_STAT\_TXSINGLECOLLFRAMES\_K Register

#### 1 CPSW\_NC\_STAT\_TXSINGLECOLLFRAMES\_K Register (Offset = 3A04Ch) [reset = 0h]

Total number of transmitted frames experiencing a single collision

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-893. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A04Ch + formula |

**Figure 5-298. CPSW\_NC\_STAT\_TXSINGLECOLLFRAMES\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-895. CPSW\_NC\_STAT\_TXSINGLECOLLFRAMES\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                        |
|------|-------|------|-------|--------------------------------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of transmitted frames experiencing a single collision |

### 5.1.2.299 CPSW\_NC\_STAT\_TXMULTCOLLFRAMES\_K Register

#### 1 CPSW\_NC\_STAT\_TXMULTCOLLFRAMES\_K Register (Offset = 3A050h) [reset = 0h]

Total number of transmitted frames experiencing multiple collisions

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-896. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A050h + formula |

**Figure 5-299. CPSW\_NC\_STAT\_TXMULTCOLLFRAMES\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-898. CPSW\_NC\_STAT\_TXMULTCOLLFRAMES\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                         |
|------|-------|------|-------|---------------------------------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of transmitted frames experiencing multiple collisions |

### 5.1.2.300 CPSW\_NC\_STAT\_TXEXCESSIVECOLLISIONS\_K Register

#### 1 CPSW\_NC\_STAT\_TXEXCESSIVECOLLISIONS\_K Register (Offset = 3A054h) [reset = 0h]

Total number of transmitted frames abandoned due to excessive collisions

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-899. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A054h + formula |

**Figure 5-300. CPSW\_NC\_STAT\_TXEXCESSIVECOLLISIONS\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-901. CPSW\_NC\_STAT\_TXEXCESSIVECOLLISIONS\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                              |
|------|-------|------|-------|--------------------------------------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of transmitted frames abandoned due to excessive collisions |

### 5.1.2.301 CPSW\_NC\_STAT\_TXLATECOLLISIONS\_K Register

#### 1 CPSW\_NC\_STAT\_TXLATECOLLISIONS\_K Register (Offset = 3A058h) [reset = 0h]

Total number of transmitted frames abandoned due to a late collision

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-902. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A058h + formula |

**Figure 5-301. CPSW\_NC\_STAT\_TXLATECOLLISIONS\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-904. CPSW\_NC\_STAT\_TXLATECOLLISIONS\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                          |
|------|-------|------|-------|----------------------------------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of transmitted frames abandoned due to a late collision |

### 5.1.2.302 CPSW\_NC\_STAT\_RXIPGERROR\_K Register

#### 1 CPSW\_NC\_STAT\_RXIPGERROR\_K Register (Offset = 3A05Ch) [reset = 0h]

Total number of receive inter-packet gap errors (10G only)

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-905. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A05Ch + formula |

**Figure 5-302. CPSW\_NC\_STAT\_RXIPGERROR\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-907. CPSW\_NC\_STAT\_RXIPGERROR\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                |
|------|-------|------|-------|------------------------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of receive inter-packet gap errors (10G only) |

### 5.1.2.303 CPSW\_NC\_STAT\_TXCARRIERSENSEERRORS\_K Register

#### 1 CPSW\_NC\_STAT\_TXCARRIERSENSEERRORS\_K Register (Offset = 3A060h) [reset = 0h]

Total number of transmitted frames that experienced a carrier loss

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-908. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A060h + formula |

**Figure 5-303. CPSW\_NC\_STAT\_TXCARRIERSENSEERRORS\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-910. CPSW\_NC\_STAT\_TXCARRIERSENSEERRORS\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                        |
|------|-------|------|-------|--------------------------------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of transmitted frames that experienced a carrier loss |

### 5.1.2.304 CPSW\_NC\_STAT\_TXOCTETS\_K Register

#### 1 CPSW\_NC\_STAT\_TXOCTETS\_K Register (Offset = 3A064h) [reset = 0h]

Total number of bytes in all good frames transmitted

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-911. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A064h + formula |

**Figure 5-304. CPSW\_NC\_STAT\_TXOCTETS\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-913. CPSW\_NC\_STAT\_TXOCTETS\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                          |
|------|-------|------|-------|------------------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of bytes in all good frames transmitted |



### 5.1.2.305 CPSW\_NC\_STAT\_OCTETFRAMES64\_K Register

#### 1 CPSW\_NC\_STAT\_OCTETFRAMES64\_K Register (Offset = 3A068h) [reset = 0h]

Total number of 64-byte frames received and transmitted

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-914. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A068h + formula |

**Figure 5-305. CPSW\_NC\_STAT\_OCTETFRAMES64\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-916. CPSW\_NC\_STAT\_OCTETFRAMES64\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                             |
|------|-------|------|-------|---------------------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of 64-byte frames received and transmitted |

### 5.1.2.306 CPSW\_NC\_STAT\_OCTETFRAMES65T127\_K Register

#### 1 CPSW\_NC\_STAT\_OCTETFRAMES65T127\_K Register (Offset = 3A06Ch) [reset = 0h]

Total number of frames of size 65 to 127 bytes received and transmitted

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-917. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A06Ch + formula |

**Figure 5-306. CPSW\_NC\_STAT\_OCTETFRAMES65T127\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-919. CPSW\_NC\_STAT\_OCTETFRAMES65T127\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                             |
|------|-------|------|-------|-------------------------------------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of frames of size 65 to 127 bytes received and transmitted |

### 5.1.2.307 CPSW\_NC\_STAT\_OCTETFRAMES128T255\_K Register

#### 1 CPSW\_NC\_STAT\_OCTETFRAMES128T255\_K Register (Offset = 3A070h) [reset = 0h]

Total number of frames of size 128 to 255 bytes received and transmitted

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-920. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A070h + formula |

**Figure 5-307. CPSW\_NC\_STAT\_OCTETFRAMES128T255\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-922. CPSW\_NC\_STAT\_OCTETFRAMES128T255\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                              |
|------|-------|------|-------|--------------------------------------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of frames of size 128 to 255 bytes received and transmitted |

### 5.1.2.308 CPSW\_NC\_STAT\_OCTETFRAMES256T511\_K Register

#### 1 CPSW\_NC\_STAT\_OCTETFRAMES256T511\_K Register (Offset = 3A074h) [reset = 0h]

Total number of frames of size 256 to 511 bytes received and transmitted

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-923. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A074h + formula |

**Figure 5-308. CPSW\_NC\_STAT\_OCTETFRAMES256T511\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-925. CPSW\_NC\_STAT\_OCTETFRAMES256T511\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                              |
|------|-------|------|-------|--------------------------------------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of frames of size 256 to 511 bytes received and transmitted |

### 5.1.2.309 CPSW\_NC\_STAT\_OCTETFRAMES512T1023\_K Register

#### 1 CPSW\_NC\_STAT\_OCTETFRAMES512T1023\_K Register (Offset = 3A078h) [reset = 0h]

Total number of frames of size 512 to 1023 bytes received and transmitted

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-926. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A078h + formula |

**Figure 5-309. CPSW\_NC\_STAT\_OCTETFRAMES512T1023\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-928. CPSW\_NC\_STAT\_OCTETFRAMES512T1023\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                               |
|------|-------|------|-------|---------------------------------------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of frames of size 512 to 1023 bytes received and transmitted |

### 5.1.2.310 CPSW\_NC\_STAT\_OCTETFRAMES1024TUP\_K Register

#### 1 CPSW\_NC\_STAT\_OCTETFRAMES1024TUP\_K Register (Offset = 3A07Ch) [reset = 0h]

Total number of frames of size 1024 to rx\_maxlen bytes received and 1024 bytes or greater transmitted

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-929. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A07Ch + formula |

**Figure 5-310. CPSW\_NC\_STAT\_OCTETFRAMES1024TUP\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-931. CPSW\_NC\_STAT\_OCTETFRAMES1024TUP\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                           |
|------|-------|------|-------|-------------------------------------------------------------------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of frames of size 1024 to rx_maxlen bytes received and 1024 bytes or greater transmitted |

### 5.1.2.311 CPSW\_NC\_STAT\_NETOCTETS\_K Register

#### 1 CPSW\_NC\_STAT\_NETOCTETS\_K Register (Offset = 3A080h) [reset = 0h]

Total number of bytes received and transmitted

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-932. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A080h + formula |

**Figure 5-311. CPSW\_NC\_STAT\_NETOCTETS\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-934. CPSW\_NC\_STAT\_NETOCTETS\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                    |
|------|-------|------|-------|------------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of bytes received and transmitted |

### 5.1.2.312 CPSW\_NC\_STAT\_RX\_BOTTOM\_OF\_FIFO\_DROP\_K Register

#### 1 CPSW\_NC\_STAT\_RX\_BOTTOM\_OF\_FIFO\_DROP\_K Register (Offset = 3A084h) [reset = 0h]

Receive Bottom of FIFO Drop

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-935. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A084h + formula |

**Figure 5-312. CPSW\_NC\_STAT\_RX\_BOTTOM\_OF\_FIFO\_DROP\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-937. CPSW\_NC\_STAT\_RX\_BOTTOM\_OF\_FIFO\_DROP\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                 |
|------|-------|------|-------|-----------------------------|
| 31:0 | COUNT | R/W  | 0h    | Receive Bottom of FIFO Drop |



### 5.1.2.313 CPSW\_NC\_STAT\_PORTMASK\_DROP\_K Register

#### 1 CPSW\_NC\_STAT\_PORTMASK\_DROP\_K Register (Offset = 3A088h) [reset = 0h]

Total number of dropped frames received due to portmask

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-938. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A088h + formula |

**Figure 5-313. CPSW\_NC\_STAT\_PORTMASK\_DROP\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-940. CPSW\_NC\_STAT\_PORTMASK\_DROP\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                             |
|------|-------|------|-------|---------------------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of dropped frames received due to portmask |

### 5.1.2.314 CPSW\_NC\_STAT\_RX\_TOP\_OF\_FIFO\_DROP\_K Register

#### 1 CPSW\_NC\_STAT\_RX\_TOP\_OF\_FIFO\_DROP\_K Register (Offset = 3A08Ch) [reset = 0h]

Receive Top of FIFO Drop

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-941. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A08Ch + formula |

**Figure 5-314. CPSW\_NC\_STAT\_RX\_TOP\_OF\_FIFO\_DROP\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-943. CPSW\_NC\_STAT\_RX\_TOP\_OF\_FIFO\_DROP\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description              |
|------|-------|------|-------|--------------------------|
| 31:0 | COUNT | R/W  | 0h    | Receive Top of FIFO Drop |

### 5.1.2.315 CPSW\_NC\_STAT\_ALE\_RATE\_LIMIT\_DROP\_K Register

#### 1 CPSW\_NC\_STAT\_ALE\_RATE\_LIMIT\_DROP\_K Register (Offset = 3A090h) [reset = 0h]

Total number of dropped frames due to ALE Rate Limiting

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-944. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A090h + formula |

**Figure 5-315. CPSW\_NC\_STAT\_ALE\_RATE\_LIMIT\_DROP\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-946. CPSW\_NC\_STAT\_ALE\_RATE\_LIMIT\_DROP\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                             |
|------|-------|------|-------|---------------------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of dropped frames due to ALE Rate Limiting |

### 5.1.2.316 CPSW\_NC\_STAT\_ALE\_VID\_INGRESS\_DROP\_K Register

#### 1 CPSW\_NC\_STAT\_ALE\_VID\_INGRESS\_DROP\_K Register (Offset = 3A094h) [reset = 0h]

Total number of dropped frames due to ALE VID Ingress

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-947. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A094h + formula |

**Figure 5-316. CPSW\_NC\_STAT\_ALE\_VID\_INGRESS\_DROP\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-949. CPSW\_NC\_STAT\_ALE\_VID\_INGRESS\_DROP\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                           |
|------|-------|------|-------|-------------------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of dropped frames due to ALE VID Ingress |

### 5.1.2.317 CPSW\_NC\_STAT\_ALE\_DA\_EQ\_SA\_DROP\_K Register

#### 1 CPSW\_NC\_STAT\_ALE\_DA\_EQ\_SA\_DROP\_K Register (Offset = 3A098h) [reset = 0h]

Total number of dropped frames due to DA=SA

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-950. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A098h + formula |

**Figure 5-317. CPSW\_NC\_STAT\_ALE\_DA\_EQ\_SA\_DROP\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-952. CPSW\_NC\_STAT\_ALE\_DA\_EQ\_SA\_DROP\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                 |
|------|-------|------|-------|---------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of dropped frames due to DA=SA |

### 5.1.2.318 CPSW\_NC\_STAT\_ALE\_BLOCK\_DROP\_K Register

#### 1 CPSW\_NC\_STAT\_ALE\_BLOCK\_DROP\_K Register (Offset = 3A09Ch) [reset = 0h]

Total number of dropped frames due to ALE Block Mode

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-953. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A09Ch + formula |

**Figure 5-318. CPSW\_NC\_STAT\_ALE\_BLOCK\_DROP\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-955. CPSW\_NC\_STAT\_ALE\_BLOCK\_DROP\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                          |
|------|-------|------|-------|------------------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of dropped frames due to ALE Block Mode |

### 5.1.2.319 CPSW\_NC\_STAT\_ALE\_SECURE\_DROP\_K Register

#### 1 CPSW\_NC\_STAT\_ALE\_SECURE\_DROP\_K Register (Offset = 3A0A0h) [reset = 0h]

Total number of dropped frames due to ALE Secure Mode

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-956. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A0A0h + formula |

**Figure 5-319. CPSW\_NC\_STAT\_ALE\_SECURE\_DROP\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-958. CPSW\_NC\_STAT\_ALE\_SECURE\_DROP\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                           |
|------|-------|------|-------|-------------------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of dropped frames due to ALE Secure Mode |

### 5.1.2.320 CPSW\_NC\_STAT\_ALE\_AUTH\_DROP\_K Register

#### 1 CPSW\_NC\_STAT\_ALE\_AUTH\_DROP\_K Register (Offset = 3A0A4h) [reset = 0h]

Total number of dropped frames due to ALE Authentication

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-959. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A0A4h + formula |

**Figure 5-320. CPSW\_NC\_STAT\_ALE\_AUTH\_DROP\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-961. CPSW\_NC\_STAT\_ALE\_AUTH\_DROP\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                              |
|------|-------|------|-------|----------------------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | Total number of dropped frames due to ALE Authentication |



### 5.1.2.321 CPSW\_NC\_STAT\_ALE\_UNKN\_UNI\_K Register

#### 1 CPSW\_NC\_STAT\_ALE\_UNKN\_UNI\_K Register (Offset = 3A0A8h) [reset = 0h]

ALE Receive Unknown Unicast

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-962. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A0A8h + formula |

**Figure 5-321. CPSW\_NC\_STAT\_ALE\_UNKN\_UNI\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-964. CPSW\_NC\_STAT\_ALE\_UNKN\_UNI\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                 |
|------|-------|------|-------|-----------------------------|
| 31:0 | COUNT | R/W  | 0h    | ALE Receive Unknown Unicast |

### 5.1.2.322 CPSW\_NC\_STAT\_ALE\_UNKN\_UNI\_BCNT\_K Register

#### 1 CPSW\_NC\_STAT\_ALE\_UNKN\_UNI\_BCNT\_K Register (Offset = 3A0ACh) [reset = 0h]

ALE Receive Unknown Unicast Bytecount

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-965. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A0ACh + formula |

**Figure 5-322. CPSW\_NC\_STAT\_ALE\_UNKN\_UNI\_BCNT\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-967. CPSW\_NC\_STAT\_ALE\_UNKN\_UNI\_BCNT\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                           |
|------|-------|------|-------|---------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | ALE Receive Unknown Unicast Bytecount |

### 5.1.2.323 CPSW\_NC\_STAT\_ALE\_UNKN\_MLT\_K Register

#### 1 CPSW\_NC\_STAT\_ALE\_UNKN\_MLT\_K Register (Offset = 3A0B0h) [reset = 0h]

ALE Receive Unknown Multicast

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-968. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A0B0h + formula |

**Figure 5-323. CPSW\_NC\_STAT\_ALE\_UNKN\_MLT\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-970. CPSW\_NC\_STAT\_ALE\_UNKN\_MLT\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                   |
|------|-------|------|-------|-------------------------------|
| 31:0 | COUNT | R/W  | 0h    | ALE Receive Unknown Multicast |

### 5.1.2.324 CPSW\_NC\_STAT\_ALE\_UNKN\_MLT\_BCNT\_K Register

#### 1 CPSW\_NC\_STAT\_ALE\_UNKN\_MLT\_BCNT\_K Register (Offset = 3A0B4h) [reset = 0h]

ALE Receive Unknown Multicast Bytecount

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-971. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A0B4h + formula |

**Figure 5-324. CPSW\_NC\_STAT\_ALE\_UNKN\_MLT\_BCNT\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-973. CPSW\_NC\_STAT\_ALE\_UNKN\_MLT\_BCNT\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                             |
|------|-------|------|-------|-----------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | ALE Receive Unknown Multicast Bytecount |

### 5.1.2.325 CPSW\_NC\_STAT\_ALE\_UNKN\_BRD\_K Register

#### 1 CPSW\_NC\_STAT\_ALE\_UNKN\_BRD\_K Register (Offset = 3A0B8h) [reset = 0h]

ALE Receive Unknown Broadcast

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-974. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A0B8h + formula |

**Figure 5-325. CPSW\_NC\_STAT\_ALE\_UNKN\_BRD\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-976. CPSW\_NC\_STAT\_ALE\_UNKN\_BRD\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                   |
|------|-------|------|-------|-------------------------------|
| 31:0 | COUNT | R/W  | 0h    | ALE Receive Unknown Broadcast |

### 5.1.2.326 CPSW\_NC\_STAT\_ALE\_UNKN\_BRD\_BCNT\_K Register

#### 1 CPSW\_NC\_STAT\_ALE\_UNKN\_BRD\_BCNT\_K Register (Offset = 3A0BCh) [reset = 0h]

ALE Receive Unknown Broadcast Bytecount

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-977. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A0BCh + formula |

**Figure 5-326. CPSW\_NC\_STAT\_ALE\_UNKN\_BRD\_BCNT\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-979. CPSW\_NC\_STAT\_ALE\_UNKN\_BRD\_BCNT\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                             |
|------|-------|------|-------|-----------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | ALE Receive Unknown Broadcast Bytecount |

### 5.1.2.327 CPSW\_NC\_STAT\_ALE\_POL\_MATCH\_K Register

#### 1 CPSW\_NC\_STAT\_ALE\_POL\_MATCH\_K Register (Offset = 3A0C0h) [reset = 0h]

ALE Policer Matched

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-980. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A0C0h + formula |

**Figure 5-327. CPSW\_NC\_STAT\_ALE\_POL\_MATCH\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-982. CPSW\_NC\_STAT\_ALE\_POL\_MATCH\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description         |
|------|-------|------|-------|---------------------|
| 31:0 | COUNT | R/W  | 0h    | ALE Policer Matched |

### 5.1.2.328 CPSW\_NC\_STAT\_ALE\_POL\_MATCH\_RED\_K Register

#### 1 CPSW\_NC\_STAT\_ALE\_POL\_MATCH\_RED\_K Register (Offset = 3A0C4h) [reset = 0h]

ALE Policer Matched and Condition Red

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-983. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A0C4h + formula |

**Figure 5-328. CPSW\_NC\_STAT\_ALE\_POL\_MATCH\_RED\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-985. CPSW\_NC\_STAT\_ALE\_POL\_MATCH\_RED\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                           |
|------|-------|------|-------|---------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | ALE Policer Matched and Condition Red |



### 5.1.2.329 CPSW\_NC\_STAT\_ALE\_POL\_MATCH\_YELLOW\_K Register

#### 1 CPSW\_NC\_STAT\_ALE\_POL\_MATCH\_YELLOW\_K Register (Offset = 3A0C8h) [reset = 0h]

ALE Policer Matched and Condition Yellow

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-986. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A0C8h + formula |

**Figure 5-329. CPSW\_NC\_STAT\_ALE\_POL\_MATCH\_YELLOW\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-988. CPSW\_NC\_STAT\_ALE\_POL\_MATCH\_YELLOW\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                              |
|------|-------|------|-------|------------------------------------------|
| 31:0 | COUNT | R/W  | 0h    | ALE Policer Matched and Condition Yellow |

### 5.1.2.330 CPSW\_NC\_STAT\_ALE\_MULT\_SA\_DROP\_K Register

#### 1 CPSW\_NC\_STAT\_ALE\_MULT\_SA\_DROP\_K Register (Offset = 3A0CCh) [reset = 0h]

ALE Multicast Source Address Drop

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-989. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A0CCh + formula |

**Figure 5-330. CPSW\_NC\_STAT\_ALE\_MULT\_SA\_DROP\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-991. CPSW\_NC\_STAT\_ALE\_MULT\_SA\_DROP\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                       |
|------|-------|------|-------|-----------------------------------|
| 31:0 | COUNT | R/W  | 0h    | ALE Multicast Source Address drop |

### 5.1.2.331 CPSW\_NC\_STAT\_ALE\_DUAL\_VLAN\_DROP\_K Register

#### 1 CPSW\_NC\_STAT\_ALE\_DUAL\_VLAN\_DROP\_K Register (Offset = 3A0D0h) [reset = 0h]

ALE Dual VLAN Drop

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-992. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A0D0h + formula |

**Figure 5-331. CPSW\_NC\_STAT\_ALE\_DUAL\_VLAN\_DROP\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-994. CPSW\_NC\_STAT\_ALE\_DUAL\_VLAN\_DROP\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description        |
|------|-------|------|-------|--------------------|
| 31:0 | COUNT | R/W  | 0h    | ALE Dual VLAN drop |

### 5.1.2.332 CPSW\_NC\_STAT\_ALE\_LEN\_ERROR\_DROP\_K Register

#### 1 CPSW\_NC\_STAT\_ALE\_LEN\_ERROR\_DROP\_K Register (Offset = 3A0D4h) [reset = 0h]

ALE Length Error Drop

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-995. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A0D4h + formula |

**Figure 5-332. CPSW\_NC\_STAT\_ALE\_LEN\_ERROR\_DROP\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-997. CPSW\_NC\_STAT\_ALE\_LEN\_ERROR\_DROP\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description           |
|------|-------|------|-------|-----------------------|
| 31:0 | COUNT | R/W  | 0h    | ALE Length Error drop |

### 5.1.2.333 CPSW\_NC\_STAT\_ALE\_IP\_NEXT\_HDR\_DROP\_K Register

#### 1 CPSW\_NC\_STAT\_ALE\_IP\_NEXT\_HDR\_DROP\_K Register (Offset = 3A0D8h) [reset = 0h]

ALE IP Next Header Drop

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-998. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A0D8h + formula |

**Figure 5-333. CPSW\_NC\_STAT\_ALE\_IP\_NEXT\_HDR\_DROP\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-1000. CPSW\_NC\_STAT\_ALE\_IP\_NEXT\_HDR\_DROP\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description          |
|------|-------|------|-------|----------------------|
| 31:0 | COUNT | R/W  | 0h    | ALE Next Header drop |

### 5.1.2.334 CPSW\_NC\_STAT\_ALE\_IPV4\_FRAG\_DROP\_K Register

#### 1 CPSW\_NC\_STAT\_ALE\_IPV4\_FRAG\_DROP\_K Register (Offset = 3A0DCh) [reset = 0h]

ALE IPV4 Frag Drop

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-1001. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A0DCh + formula |

**Figure 5-334. CPSW\_NC\_STAT\_ALE\_IPV4\_FRAG\_DROP\_K Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-1003. CPSW\_NC\_STAT\_ALE\_IPV4\_FRAG\_DROP\_K Register Field Descriptions**

| Bit  | Field | Type | Reset | Description            |
|------|-------|------|-------|------------------------|
| 31:0 | COUNT | R/W  | 0h    | ALE IPV4 Fragment drop |

### 5.1.2.335 CPSW\_NC\_STAT\_TX\_MEMORY\_PROTECT\_ERROR\_K Register

#### 1 CPSW\_NC\_STAT\_TX\_MEMORY\_PROTECT\_ERROR\_K Register (Offset = 3A17Ch) [reset = 0h]

Transmit Memory Protect CRC Error

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-1004. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A17Ch + formula |

**Figure 5-335. CPSW\_NC\_STAT\_TX\_MEMORY\_PROTECT\_ERROR\_K Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-1006. CPSW\_NC\_STAT\_TX\_MEMORY\_PROTECT\_ERROR\_K Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                       |
|------|----------|------|-------|-----------------------------------|
| 31:8 | RESERVED | NONE | 0h    | Reserved                          |
| 7:0  | COUNT    | R/W  | 0h    | Transmit Memory Protect CRC Error |

### 5.1.2.336 CPSW\_NC\_STAT\_ENET\_PN\_TX\_PRI\_REG\_K Register

#### 1 CPSW\_NC\_STAT\_ENET\_PN\_TX\_PRI\_REG\_K Register (Offset = 3A180h) [reset = 0h]

ENET Port n PRIORITY N Packet Count

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-1007. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A180h + formula |

**Figure 5-336. CPSW\_NC\_STAT\_ENET\_PN\_TX\_PRI\_REG\_K Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PN_TX_PRIN |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PN_TX_PRIN |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PN_TX_PRIN |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PN_TX_PRIN |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-1009. CPSW\_NC\_STAT\_ENET\_PN\_TX\_PRI\_REG\_K Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                   |
|------|------------|------|-------|-------------------------------|
| 31:0 | PN_TX_PRIN | R/W  | 0h    | ENET TX Priority Packet Count |



### 5.1.2.337 CPSW\_NC\_STAT\_ENET\_PN\_TX\_PRI\_BCNT\_REG\_K Register

#### 1 CPSW\_NC\_STAT\_ENET\_PN\_TX\_PRI\_BCNT\_REG\_K Register (Offset = 3A1A0h) [reset = 0h]

ENET Port n PRIORITY N Packet Byte Count

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-1010. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A1A0h + formula |

**Figure 5-337. CPSW\_NC\_STAT\_ENET\_PN\_TX\_PRI\_BCNT\_REG\_K Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PN_TX_PRIN_BCNT |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PN_TX_PRIN_BCNT |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PN_TX_PRIN_BCNT |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PN_TX_PRIN_BCNT |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 5-1012. CPSW\_NC\_STAT\_ENET\_PN\_TX\_PRI\_BCNT\_REG\_K Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                              |
|------|-----------------|------|-------|------------------------------------------|
| 31:0 | PN_TX_PRIN_BCNT | R/W  | 0h    | ENET Port n PRIORITY N Packet Byte Count |

### 5.1.2.338 CPSW\_NC\_STAT\_ENET\_PN\_TX\_PRI\_DROP\_REG\_K Register

#### 1 CPSW\_NC\_STAT\_ENET\_PN\_TX\_PRI\_DROP\_REG\_K Register (Offset = 3A1C0h) [reset = 0h]

ENET Port n PRIORITY N Packet Drop Count

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-1013. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A1C0h + formula |

**Figure 5-338. CPSW\_NC\_STAT\_ENET\_PN\_TX\_PRI\_DROP\_REG\_K Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PN_TX_PRIN_DROP |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PN_TX_PRIN_DROP |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PN_TX_PRIN_DROP |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PN_TX_PRIN_DROP |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 5-1015. CPSW\_NC\_STAT\_ENET\_PN\_TX\_PRI\_DROP\_REG\_K Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                              |
|------|-----------------|------|-------|------------------------------------------|
| 31:0 | PN_TX_PRIN_DROP | R/W  | 0h    | ENET Port n PRIORITY N Packet Drop Count |

### 5.1.2.339 CPSW\_NC\_STAT\_ENET\_PN\_TX\_PRI\_DROP\_BCNT\_REG\_K Register

#### 1 CPSW\_NC\_STAT\_ENET\_PN\_TX\_PRI\_DROP\_BCNT\_REG\_K Register (Offset = 3A1E0h) [reset = 0h]

ENET Port n PRIORITY N Packet Drop Byte Count

Return to [Summary Table](#)

Offset = Base + (k \* 200h); where k = 0 to 2d

**Table 5-1016. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 A1E0h + formula |

**Figure 5-339. CPSW\_NC\_STAT\_ENET\_PN\_TX\_PRI\_DROP\_BCNT\_REG\_K Name Register**

|                      |    |    |    |    |    |    |    |
|----------------------|----|----|----|----|----|----|----|
| 31                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PN_TX_PRIN_DROP_BCNT |    |    |    |    |    |    |    |
| R/W                  |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 23                   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PN_TX_PRIN_DROP_BCNT |    |    |    |    |    |    |    |
| R/W                  |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 15                   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PN_TX_PRIN_DROP_BCNT |    |    |    |    |    |    |    |
| R/W                  |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |
| 7                    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PN_TX_PRIN_DROP_BCNT |    |    |    |    |    |    |    |
| R/W                  |    |    |    |    |    |    |    |
| 0h                   |    |    |    |    |    |    |    |

**Table 5-1018. CPSW\_NC\_STAT\_ENET\_PN\_TX\_PRI\_DROP\_BCNT\_REG\_K Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                   |
|------|----------------------|------|-------|-----------------------------------------------|
| 31:0 | PN_TX_PRIN_DROP_BCNT | R/W  | 0h    | ENET Port n PRIORITY N Packet Drop Byte Count |

### 5.1.2.340 CPSW\_NC\_CPTS\_IDVER\_REG Register

#### 1 CPSW\_NC\_CPTS\_IDVER\_REG Register (Offset = 3D000h) [reset = 4E8A010Dh]

Identification and Version Register

Return to [Summary Table](#)

**Table 5-1019. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 D000h       |

**Figure 5-340. CPSW\_NC\_CPTS\_IDVER\_REG Name Register**

|           |    |    |    |           |    |    |    |
|-----------|----|----|----|-----------|----|----|----|
| 31        | 30 | 29 | 28 | 27        | 26 | 25 | 24 |
| IDENT     |    |    |    |           |    |    |    |
| R         |    |    |    |           |    |    |    |
| 4E8Ah     |    |    |    |           |    |    |    |
| 23        | 22 | 21 | 20 | 19        | 18 | 17 | 16 |
| IDENT     |    |    |    |           |    |    |    |
| R         |    |    |    |           |    |    |    |
| 4E8Ah     |    |    |    |           |    |    |    |
| 15        | 14 | 13 | 12 | 11        | 10 | 9  | 8  |
| RTL_VER   |    |    |    | MAJOR_VER |    |    |    |
| R         |    |    |    | R         |    |    |    |
| 0h        |    |    |    | 1h        |    |    |    |
| 7         | 6  | 5  | 4  | 3         | 2  | 1  | 0  |
| MINOR_VER |    |    |    |           |    |    |    |
| R         |    |    |    |           |    |    |    |
| Dh        |    |    |    |           |    |    |    |

**Table 5-1021. CPSW\_NC\_CPTS\_IDVER\_REG Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description          |
|-------|-----------|------|-------|----------------------|
| 31:16 | IDENT     | R    | 4E8Ah | Identification value |
| 15:11 | RTL_VER   | R    | 0h    | RTL version value    |
| 10:8  | MAJOR_VER | R    | 1h    | Major version value  |
| 7:0   | MINOR_VER | R    | Dh    | Minor version value  |

### 5.1.2.341 CPSW\_NC\_CPTS\_CONTROL\_REG Register

#### 1 CPSW\_NC\_CPTS\_CONTROL\_REG Register (Offset = 3D004h) [reset = 4h]

Time Sync Control Register

Return to [Summary Table](#)

**Table 5-1022. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 D004h       |

**Figure 5-341. CPSW\_NC\_CPTS\_CONTROL\_REG Name Register**

| 31             | 30             | 29             | 28             | 27             | 26               | 25             | 24             |
|----------------|----------------|----------------|----------------|----------------|------------------|----------------|----------------|
| TS_SYNC_SEL    |                |                |                | RESERVED       |                  |                |                |
| R/W            |                |                |                | NONE           |                  |                |                |
| 0h             |                |                |                | 0h             |                  |                |                |
| 23             | 22             | 21             | 20             | 19             | 18               | 17             | 16             |
| RESERVED       |                |                |                |                |                  | TS_GENF_CLR_EN | TS_RX_NO_EVENT |
| NONE           |                |                |                |                |                  | R/W            | R/W            |
| 0h             |                |                |                |                |                  | 0h             | 0h             |
| 15             | 14             | 13             | 12             | 11             | 10               | 9              | 8              |
| HW8_TS_PUSH_EN | HW7_TS_PUSH_EN | HW6_TS_PUSH_EN | HW5_TS_PUSH_EN | HW4_TS_PUSH_EN | HW3_TS_PUSH_EN   | HW2_TS_PUSH_EN | HW1_TS_PUSH_EN |
| R/W            | R/W            | R/W            | R/W            | R/W            | R/W              | R/W            | R/W            |
| 0h             | 0h             | 0h             | 0h             | 0h             | 0h               | 0h             | 0h             |
| 7              | 6              | 5              | 4              | 3              | 2                | 1              | 0              |
| TS_PPM_DIR     | TS_COMP_TOG    | MODE           | SEQUENCE_EN    | TSTAMP_EN      | TS_COMP_POLARITY | INT_TEST       | CPTS_EN        |
| R/W            | R/W            | R/W            | R/W            | R/W            | R/W              | R/W            | R/W            |
| 0h             | 0h             | 0h             | 0h             | 0h             | 1h               | 0h             | 0h             |

**Table 5-1024. CPSW\_NC\_CPTS\_CONTROL\_REG Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                              |
|-------|----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28 | TS_SYNC_SEL    | R/W  | 0h    | TS_SYNC output timestamp counter bit select -<br>0000 - TS_SYNC disabled.<br>0001 - TS_SYNC is timestamp counter bit 17<br>0010 - TS_SYNC is timestamp counter bit 18<br>...<br>1110 - TS_SYNC is timestamp counter bit 30<br>1111 - TS_SYNC is timestamp counter bit 31 |
| 27:18 | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                 |
| 17    | TS_GENF_CLR_EN | R/W  | 0h    | GENF (and ESTF) Clear Enable -<br>0 - A TS_GENF <sub>n</sub> output is not cleared when the associated ts_genf_length[31:0] is cleared to zero.<br>1 - A TS_GENF <sub>n</sub> output is cleared when the associated ts_genf_length[31:0] is cleared to zero.             |
| 16    | TS_RX_NO_EVENT | R/W  | 0h    | Timestamp Ethernet Receive produces no events -<br>0 - Ethernet receive timesync events enabled.<br>1 - Ethernet receive timesync events disabled.                                                                                                                       |
| 15    | HW8_TS_PUSH_EN | R/W  | 0h    | Hardware push 8 enable                                                                                                                                                                                                                                                   |
| 14    | HW7_TS_PUSH_EN | R/W  | 0h    | Hardware push 7 enable                                                                                                                                                                                                                                                   |
| 13    | HW6_TS_PUSH_EN | R/W  | 0h    | Hardware push 6 enable                                                                                                                                                                                                                                                   |
| 12    | HW5_TS_PUSH_EN | R/W  | 0h    | Hardware push 5 enable                                                                                                                                                                                                                                                   |

**Table 5-1024. CPSW\_NC\_CPTS\_CONTROL\_REG Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                    |
|-----|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11  | HW4_TS_PUSH_EN   | R/W  | 0h    | Hardware push 4 enable                                                                                                                                                                                                                                                         |
| 10  | HW3_TS_PUSH_EN   | R/W  | 0h    | Hardware push 3 enable                                                                                                                                                                                                                                                         |
| 9   | HW2_TS_PUSH_EN   | R/W  | 0h    | Hardware push 2 enable                                                                                                                                                                                                                                                         |
| 8   | HW1_TS_PUSH_EN   | R/W  | 0h    | Hardware push 1 enable                                                                                                                                                                                                                                                         |
| 7   | TS_PPM_DIR       | R/W  | 0h    | PPM Correction Direction -<br>0 - Increase the time_stamp[63:0] value by the PPM value.<br>1 - Decrease the time_stamp[63:0] value by the PPM value.                                                                                                                           |
| 6   | TS_COMP_TOG      | R/W  | 0h    | Timestamp Compare Toggle mode -<br>0 - TS_COMP is in non-toggle mode.<br>1 - TS_COMP is in toggle mode.                                                                                                                                                                        |
| 5   | MODE             | R/W  | 0h    | 64-Bit Mode -<br>0 - The timestamp is 32-bits with the upper 32-bits forced to zero.<br>1 - The timestamp is 64-bits.                                                                                                                                                          |
| 4   | SEQUENCE_EN      | R/W  | 0h    | Sequence Enable -<br>0 - The timestamp value increments with the selected RFTCLK (normal operation).<br>1 - The timestamp for received packets is the sequence number of the received packet (first packet is 1, second packet is 2, etc). This can be used for test purposes. |
| 3   | TSTAMP_EN        | R/W  | 0h    | Host Receive Timestamp Enable -<br>0 - Timestamps are disabled on received packets to host.<br>1 - Timestamps enabled on received packets to host (cpts_en must be set).                                                                                                       |
| 2   | TS_COMP_POLARITY | R/W  | 1h    | TS_COMP Polarity<br>0 - TS_COMP is asserted low<br>1 - TS_COMP is asserted high                                                                                                                                                                                                |
| 1   | INT_TEST         | R/W  | 0h    | Interrupt Test - When set, this bit allows the raw interrupt to be written to facilitate interrupt test.                                                                                                                                                                       |
| 0   | CPTS_EN          | R/W  | 0h    | Time Sync Enable - When disabled (cleared to zero), the CPTS RCLK domain is held in reset.                                                                                                                                                                                     |

### 5.1.2.342 CPSW\_NC\_CPTS\_RFTCLK\_SEL\_REG Register

#### 1 CPSW\_NC\_CPTS\_RFTCLK\_SEL\_REG Register (Offset = 3D008h) [reset = 0h]

RFTCLK Select Register

Return to [Summary Table](#)
**Table 5-1025. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 D008h       |

**Figure 5-342. CPSW\_NC\_CPTS\_RFTCLK\_SEL\_REG Name Register**

|          |    |    |    |            |    |    |    |
|----------|----|----|----|------------|----|----|----|
| 31       | 30 | 29 | 28 | 27         | 26 | 25 | 24 |
| RESERVED |    |    |    |            |    |    |    |
| NONE     |    |    |    |            |    |    |    |
| 0h       |    |    |    |            |    |    |    |
| 23       | 22 | 21 | 20 | 19         | 18 | 17 | 16 |
| RESERVED |    |    |    |            |    |    |    |
| NONE     |    |    |    |            |    |    |    |
| 0h       |    |    |    |            |    |    |    |
| 15       | 14 | 13 | 12 | 11         | 10 | 9  | 8  |
| RESERVED |    |    |    |            |    |    |    |
| NONE     |    |    |    |            |    |    |    |
| 0h       |    |    |    |            |    |    |    |
| 7        | 6  | 5  | 4  | 3          | 2  | 1  | 0  |
| RESERVED |    |    |    | RFTCLK_SEL |    |    |    |
| NONE     |    |    |    | R/W        |    |    |    |
| 0h       |    |    |    | 0h         |    |    |    |

**Table 5-1027. CPSW\_NC\_CPTS\_RFTCLK\_SEL\_REG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                |
|------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:5 | RESERVED   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                   |
| 4:0  | RFTCLK_SEL | R/W  | 0h    | Reference Clock Select - This signal is used to control an external multiplexor that selects one of up to 32 clocks for time sync reference (RFTCLK). This rftclk_sel value can be written only when the cpts_en bit and the tstamp_en bit are cleared to zero in the TS_Control register. |

### 5.1.2.343 CPSW\_NC\_CPTS\_TS\_PUSH\_REG Register

#### 1 CPSW\_NC\_CPTS\_TS\_PUSH\_REG Register (Offset = 3D00Ch) [reset = 0h]

Time Stamp Event Push Register

Return to [Summary Table](#)

**Table 5-1028. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 D00Ch       |

**Figure 5-343. CPSW\_NC\_CPTS\_TS\_PUSH\_REG Name Register**

|          |    |    |    |    |    |    |         |
|----------|----|----|----|----|----|----|---------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24      |
| RESERVED |    |    |    |    |    |    |         |
| NONE     |    |    |    |    |    |    |         |
| 0h       |    |    |    |    |    |    |         |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16      |
| RESERVED |    |    |    |    |    |    |         |
| NONE     |    |    |    |    |    |    |         |
| 0h       |    |    |    |    |    |    |         |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8       |
| RESERVED |    |    |    |    |    |    |         |
| NONE     |    |    |    |    |    |    |         |
| 0h       |    |    |    |    |    |    |         |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0       |
| RESERVED |    |    |    |    |    |    | TS_PUSH |
| NONE     |    |    |    |    |    |    | W       |
| 0h       |    |    |    |    |    |    | 0h      |

**Table 5-1030. CPSW\_NC\_CPTS\_TS\_PUSH\_REG Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|------|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 0    | TS_PUSH  | W    | 0h    | Time stamp event push - When a logic high is written to this bit a time stamp event is pushed onto the event FIFO. The time stamp value is the time of the write of this register, not the time of the event read. The time stamp value can then be read on interrupt via the event registers. Software should not push a second time stamp event onto the event FIFO until the first time stamp value has been read from the event FIFO (there should be only one time stamp event in the event FIFO at any given time). This bit is write only and always reads zero. |



### 5.1.2.344 CPSW\_NC\_CPTS\_TS\_LOAD\_VAL\_REG Register

#### 1 CPSW\_NC\_CPTS\_TS\_LOAD\_VAL\_REG Register (Offset = 3D010h) [reset = 0h]

Time Stamp Load Low Value Register

Return to [Summary Table](#)

**Table 5-1031. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 D010h       |

**Figure 5-344. CPSW\_NC\_CPTS\_TS\_LOAD\_VAL\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TS_LOAD_VAL |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TS_LOAD_VAL |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TS_LOAD_VAL |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TS_LOAD_VAL |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-1033. CPSW\_NC\_CPTS\_TS\_LOAD\_VAL\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                 |
|------|-------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | TS_LOAD_VAL | R/W  | 0h    | Time Stamp Load Low Value - Writing the ts_load_en bit causes ts_load[63:0] to be written into the time stamp. The time stamp value is read by initiating a time stamp push event, not by reading this register. When reading this register, the value read is not the time stamp, but is the value that was last written to this register. |

### 5.1.2.345 CPSW\_NC\_CPTS\_TS\_LOAD\_EN\_REG Register

#### 1 CPSW\_NC\_CPTS\_TS\_LOAD\_EN\_REG Register (Offset = 3D014h) [reset = 0h]

Time Stamp Load Enable Register

Return to [Summary Table](#)

**Table 5-1034. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 D014h       |

**Figure 5-345. CPSW\_NC\_CPTS\_TS\_LOAD\_EN\_REG Name Register**

|          |    |    |    |    |    |    |            |
|----------|----|----|----|----|----|----|------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24         |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16         |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8          |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0          |
| RESERVED |    |    |    |    |    |    | TS_LOAD_EN |
| NONE     |    |    |    |    |    |    | W          |
| 0h       |    |    |    |    |    |    | 0h         |

**Table 5-1036. CPSW\_NC\_CPTS\_TS\_LOAD\_EN\_REG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                               |
|------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                  |
| 0    | TS_LOAD_EN | W    | 0h    | Time Stamp Load - Writing a one to this bit enables the time stamp value to be written with the value in ts_load[63:0]. This bit is write only and will be cleared by the hardware after one clock. The upper 32-bits of the timestamp are forced to zero in 32-bit mode. |

### 5.1.2.346 CPSW\_NC\_CPTS\_TS\_COMP\_VAL\_REG Register

#### 1 CPSW\_NC\_CPTS\_TS\_COMP\_VAL\_REG Register (Offset = 3D018h) [reset = 0h]

Time Stamp Comparison Low Value Register

Return to [Summary Table](#)

**Table 5-1037. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 D018h       |

**Figure 5-346. CPSW\_NC\_CPTS\_TS\_COMP\_VAL\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TS_COMP_VAL |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TS_COMP_VAL |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TS_COMP_VAL |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TS_COMP_VAL |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-1039. CPSW\_NC\_CPTS\_TS\_COMP\_VAL\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                                                                                                                |
|------|-------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | TS_COMP_VAL | R/W  | 0h    | Time Stamp Comparison Low Value - Writing a non-zero value to the TS_Comp_Length[31:0] register causes a pulse of TS_Comp_Length RCLK periods on the TS_COMP output and a comparison event when the time_stamp counter value is equivalent to ts_comp_val. |

### 5.1.2.347 CPSW\_NC\_CPTS\_TS\_COMP\_LEN\_REG Register

#### 1 CPSW\_NC\_CPTS\_TS\_COMP\_LEN\_REG Register (Offset = 3D01Ch) [reset = 0h]

Time Stamp Comparison Length Register

Return to [Summary Table](#)

**Table 5-1040. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 D01Ch       |

**Figure 5-347. CPSW\_NC\_CPTS\_TS\_COMP\_LEN\_REG Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TS_COMP_LENGTH |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TS_COMP_LENGTH |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TS_COMP_LENGTH |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TS_COMP_LENGTH |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-1042. CPSW\_NC\_CPTS\_TS\_COMP\_LEN\_REG Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                                                                                                                                      |
|------|----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | TS_COMP_LENGTH | R/W  | 0h    | Time Stamp Comparison Length - Writing a non-zero value to this field enables the time stamp comparison event and output. This value should be zero when the TS_Comp_Low and TS_Comp_High registers are written. |

### 5.1.2.348 CPSW\_NC\_CPTS\_INTSTAT\_RAW\_REG Register

#### 1 CPSW\_NC\_CPTS\_INTSTAT\_RAW\_REG Register (Offset = 3D020h) [reset = 0h]

Interrupt Status Register Raw

Return to [Summary Table](#)

**Table 5-1043. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 D020h       |

**Figure 5-348. CPSW\_NC\_CPTS\_INTSTAT\_RAW\_REG Name Register**

|          |    |    |    |    |    |    |             |
|----------|----|----|----|----|----|----|-------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24          |
| RESERVED |    |    |    |    |    |    |             |
| NONE     |    |    |    |    |    |    |             |
| 0h       |    |    |    |    |    |    |             |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16          |
| RESERVED |    |    |    |    |    |    |             |
| NONE     |    |    |    |    |    |    |             |
| 0h       |    |    |    |    |    |    |             |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8           |
| RESERVED |    |    |    |    |    |    |             |
| NONE     |    |    |    |    |    |    |             |
| 0h       |    |    |    |    |    |    |             |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0           |
| RESERVED |    |    |    |    |    |    | TS_PEND_RAW |
| NONE     |    |    |    |    |    |    | R/W         |
| 0h       |    |    |    |    |    |    | 0h          |

**Table 5-1045. CPSW\_NC\_CPTS\_INTSTAT\_RAW\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                          |
|------|-------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED    | NONE | 0h    | Reserved                                                                                                                                             |
| 0    | TS_PEND_RAW | R/W  | 0h    | TS_PEND_RAW int read (before enable). Writable when int_test = 1<br>A one in this bit indicates that there are one or more events in the event FIFO. |

### 5.1.2.349 CPSW\_NC\_CPTS\_INTSTAT\_MASKED\_REG Register

#### 1 CPSW\_NC\_CPTS\_INTSTAT\_MASKED\_REG Register (Offset = 3D024h) [reset = 0h]

Interrupt Status Register Masked

Return to [Summary Table](#)

**Table 5-1046. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 D024h       |

**Figure 5-349. CPSW\_NC\_CPTS\_INTSTAT\_MASKED\_REG Name Register**

|          |    |    |    |    |    |    |         |
|----------|----|----|----|----|----|----|---------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24      |
| RESERVED |    |    |    |    |    |    |         |
| NONE     |    |    |    |    |    |    |         |
| 0h       |    |    |    |    |    |    |         |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16      |
| RESERVED |    |    |    |    |    |    |         |
| NONE     |    |    |    |    |    |    |         |
| 0h       |    |    |    |    |    |    |         |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8       |
| RESERVED |    |    |    |    |    |    |         |
| NONE     |    |    |    |    |    |    |         |
| 0h       |    |    |    |    |    |    |         |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0       |
| RESERVED |    |    |    |    |    |    | TS_PEND |
| NONE     |    |    |    |    |    |    | R       |
| 0h       |    |    |    |    |    |    | 0h      |

**Table 5-1048. CPSW\_NC\_CPTS\_INTSTAT\_MASKED\_REG Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                  |
|------|----------|------|-------|----------------------------------------------|
| 31:1 | RESERVED | NONE | 0h    | Reserved                                     |
| 0    | TS_PEND  | R    | 0h    | TS_PEND masked interrupt read (after enable) |

### 5.1.2.350 CPSW\_NC\_CPTS\_INT\_ENABLE\_REG Register

#### 1 CPSW\_NC\_CPTS\_INT\_ENABLE\_REG Register (Offset = 3D028h) [reset = 0h]

Interrupt Enable Register

Return to [Summary Table](#)

**Table 5-1049. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 D028h       |

**Figure 5-350. CPSW\_NC\_CPTS\_INT\_ENABLE\_REG Name Register**

|          |    |    |    |    |    |    |            |
|----------|----|----|----|----|----|----|------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24         |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16         |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8          |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0          |
| RESERVED |    |    |    |    |    |    | TS_PEND_EN |
| NONE     |    |    |    |    |    |    | R/W        |
| 0h       |    |    |    |    |    |    | 0h         |

**Table 5-1051. CPSW\_NC\_CPTS\_INT\_ENABLE\_REG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                     |
|------|------------|------|-------|---------------------------------|
| 31:1 | RESERVED   | NONE | 0h    | Reserved                        |
| 0    | TS_PEND_EN | R/W  | 0h    | TS_PEND masked interrupt enable |

### 5.1.2.351 CPSW\_NC\_CPTS\_TS\_COMP\_NUDGE\_REG Register

#### 1 CPSW\_NC\_CPTS\_TS\_COMP\_NUDGE\_REG Register (Offset = 3D02Ch) [reset = 0h]

Time Stamp Comparison Nudge Register

Return to [Summary Table](#)

**Table 5-1052. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 D02Ch       |

**Figure 5-351. CPSW\_NC\_CPTS\_TS\_COMP\_NUDGE\_REG Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| NUDGE    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-1054. CPSW\_NC\_CPTS\_TS\_COMP\_NUDGE\_REG Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                  |
|------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                     |
| 7:0  | NUDGE    | R/W  | 0h    | Timestamp Comparison Nudge Value -<br>This two's complement number is added to the ts_comp_length[31:0] value to increase or decrease the TS_COMP length by the ts_comp_nudge amount. Only a single high or low time is adjusted and the ts_comp_nudge value is cleared to zero when the nudge has occurred. |



### 5.1.2.352 CPSW\_NC\_CPTS\_EVENT\_POP\_REG Register

#### 1 CPSW\_NC\_CPTS\_EVENT\_POP\_REG Register (Offset = 3D030h) [reset = 0h]

Event Pop Register

Return to [Summary Table](#)

**Table 5-1055. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 D030h       |

**Figure 5-352. CPSW\_NC\_CPTS\_EVENT\_POP\_REG Name Register**

|          |    |    |    |    |    |    |           |
|----------|----|----|----|----|----|----|-----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24        |
| RESERVED |    |    |    |    |    |    |           |
| NONE     |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16        |
| RESERVED |    |    |    |    |    |    |           |
| NONE     |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8         |
| RESERVED |    |    |    |    |    |    |           |
| NONE     |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0         |
| RESERVED |    |    |    |    |    |    | EVENT_POP |
| NONE     |    |    |    |    |    |    | W         |
| 0h       |    |    |    |    |    |    | 0h        |

**Table 5-1057. CPSW\_NC\_CPTS\_EVENT\_POP\_REG Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                             |
|------|-----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED  | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                |
| 0    | EVENT_POP | W    | 0h    | Event Pop - When a logic high is written to this bit an event is popped off the event FIFO. The event FIFO pop occurs as part of the interrupt process after the event has been read from the Event_0-3 registers. Popping an event discards the event and causes the next event, if any, to be moved to the top of the FIFO ready to be read by software on interrupt. |

### 5.1.2.353 CPSW\_NC\_CPTS\_EVENT\_0\_REG Register

#### 1 CPSW\_NC\_CPTS\_EVENT\_0\_REG Register (Offset = 3D034h) [reset = 0h]

Event 0 Register

Return to [Summary Table](#)

**Table 5-1058. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 D034h       |

**Figure 5-353. CPSW\_NC\_CPTS\_EVENT\_0\_REG Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TIME_STAMP |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TIME_STAMP |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TIME_STAMP |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TIME_STAMP |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-1060. CPSW\_NC\_CPTS\_EVENT\_0\_REG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                              |
|------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | TIME_STAMP | R    | 0h    | Time Stamp lower 32-bits - The timestamp is valid for transmit, receive, and time stamp push event types. The timestamp value is not valid for counter roll event types. |

### 5.1.2.354 CPSW\_NC\_CPTS\_EVENT\_1\_REG Register

#### 1 CPSW\_NC\_CPTS\_EVENT\_1\_REG Register (Offset = 3D038h) [reset = 0h]

Event 1 Register

Return to [Summary Table](#)

**Table 5-1061. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 D038h       |

**Figure 5-354. CPSW\_NC\_CPTS\_EVENT\_1\_REG Name Register**

|             |    |              |             |              |    |    |    |
|-------------|----|--------------|-------------|--------------|----|----|----|
| 31          | 30 | 29           | 28          | 27           | 26 | 25 | 24 |
| RESERVED    |    | PREMPT_QUEUE | PORT_NUMBER |              |    |    |    |
| NONE        |    | R            | R           |              |    |    |    |
| 0h          |    | 0h           | 0h          |              |    |    |    |
| 23          | 22 | 21           | 20          | 19           | 18 | 17 | 16 |
| EVENT_TYPE  |    |              |             | MESSAGE_TYPE |    |    |    |
| R           |    |              |             | R            |    |    |    |
| 0h          |    |              |             | 0h           |    |    |    |
| 15          | 14 | 13           | 12          | 11           | 10 | 9  | 8  |
| SEQUENCE_ID |    |              |             |              |    |    |    |
| R           |    |              |             |              |    |    |    |
| 0h          |    |              |             |              |    |    |    |
| 7           | 6  | 5            | 4           | 3            | 2  | 1  | 0  |
| SEQUENCE_ID |    |              |             |              |    |    |    |
| R           |    |              |             |              |    |    |    |
| 0h          |    |              |             |              |    |    |    |

**Table 5-1063. CPSW\_NC\_CPTS\_EVENT\_1\_REG Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                   |
|-------|--------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | RESERVED     | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                      |
| 29    | PREMPT_QUEUE | R    | 0h    | Prompt Queue (iet_incl = 1) -<br>0 - The packet was received/transmitted on the express queue.<br>1 - The packet was received/transmitted on the preempt queue.                                                                                                                                                                                               |
| 28:24 | PORT_NUMBER  | R    | 0h    | Port Number - indicates the port number (encoded) of an Ethernet event or the encoded hardware timestamp number.                                                                                                                                                                                                                                              |
| 23:20 | EVENT_TYPE   | R    | 0h    | Time Sync Event Type -<br>0000 - Time Stamp Push Event<br>0001 - Time Stamp Rollover Event<br>0010 - Time Stamp Half Rollover Event<br>0011 - Hardware Time Stamp Push Event<br>0100 - Ethernet Receive Event<br>0101 - Ethernet Transmit Event<br>0110 - Time Stamp Compare Event<br>0111 - Host Transmit Event<br>1000 - reserved<br>...<br>1111 - reserved |
| 19:16 | MESSAGE_TYPE | R    | 0h    | Message type - The message type value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events.                                                                                                                                                                               |

**Table 5-1063. CPSW\_NC\_CPTS\_EVENT\_1\_REG Register Field Descriptions (continued)**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                                                 |
|------|-------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:0 | SEQUENCE_ID | R    | 0h    | Sequence ID - The 16-bit sequence id is the value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events. |

### 5.1.2.355 CPSW\_NC\_CPTS\_EVENT\_2\_REG Register

#### 1 CPSW\_NC\_CPTS\_EVENT\_2\_REG Register (Offset = 3D03Ch) [reset = 0h]

Event 2 Register

Return to [Summary Table](#)

**Table 5-1064. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 D03Ch       |

**Figure 5-355. CPSW\_NC\_CPTS\_EVENT\_2\_REG Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DOMAIN   |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-1066. CPSW\_NC\_CPTS\_EVENT\_2\_REG Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                      |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                         |
| 7:0  | DOMAIN   | R    | 0h    | Domain - The 8-bit domain is the value that was contained in an Ethernet transmit or receive time sync packet. This field is valid only for Ethernet transmit or receive events. |

### 5.1.2.356 CPSW\_NC\_CPTS\_EVENT\_3\_REG Register

#### 1 CPSW\_NC\_CPTS\_EVENT\_3\_REG Register (Offset = 3D040h) [reset = 0h]

Event 3 Register

Return to [Summary Table](#)

**Table 5-1067. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 D040h       |

**Figure 5-356. CPSW\_NC\_CPTS\_EVENT\_3\_REG Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TIME_STAMP |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TIME_STAMP |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TIME_STAMP |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TIME_STAMP |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-1069. CPSW\_NC\_CPTS\_EVENT\_3\_REG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                   |
|------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | TIME_STAMP | R    | 0h    | Time Stamp - The timestamp upper 32-bits are valid for transmit, receive, and time stamp push event types. This value is zero in 32-bit mode. |

### 5.1.2.357 CPSW\_NC\_CPTS\_TS\_LOAD\_HIGH\_VAL\_REG Register

#### 1 CPSW\_NC\_CPTS\_TS\_LOAD\_HIGH\_VAL\_REG Register (Offset = 3D044h) [reset = 0h]

Time Stamp Load High Value Register

Return to [Summary Table](#)

**Table 5-1070. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 D044h       |

**Figure 5-357. CPSW\_NC\_CPTS\_TS\_LOAD\_HIGH\_VAL\_REG Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TS_LOAD_VAL |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TS_LOAD_VAL |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TS_LOAD_VAL |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TS_LOAD_VAL |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-1072. CPSW\_NC\_CPTS\_TS\_LOAD\_HIGH\_VAL\_REG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|-------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | TS_LOAD_VAL | R/W  | 0h    | Time Stamp Load high Value - Writing the ts_load_en bit causes the value contained in this register (and the ts_load[63:0]) to be written into the time stamp. The time stamp value is read by initiating a time stamp push event, not by reading this register. When reading this register, the value read is not the time stamp, but is the value that was last written to this register. This value is unused in 32-bit mode. |

### 5.1.2.358 CPSW\_NC\_CPTS\_TS\_COMP\_HIGH\_VAL\_REG Register

#### 1 CPSW\_NC\_CPTS\_TS\_COMP\_HIGH\_VAL\_REG Register (Offset = 3D048h) [reset = 0h]

Time Stamp Comparison High Value Register

Return to [Summary Table](#)

**Table 5-1073. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 D048h       |

**Figure 5-358. CPSW\_NC\_CPTS\_TS\_COMP\_HIGH\_VAL\_REG Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TS_COMP_HIGH_VAL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TS_COMP_HIGH_VAL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TS_COMP_HIGH_VAL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TS_COMP_HIGH_VAL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 5-1075. CPSW\_NC\_CPTS\_TS\_COMP\_HIGH\_VAL\_REG Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                       |
|------|------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | TS_COMP_HIGH_VAL | R/W  | 0h    | Time Stamp Comparison High Value - Writing a non-zero value to the TS_Comp_Length[31:0] register causes a pulse of TS_Comp_Length RCLK periods on the TS_COMP output and a comparison event when the time_stamp counter value is equivalent to ts_comp_val[63:0]. This value is unused in 32-bit mode. The upper 32-bits in this register should be written before the lower 32-bits in the TS_Comp_Low register. |



### 5.1.2.359 CPSW\_NC\_CPTS\_TS\_ADD\_VAL\_REG Register

#### 1 CPSW\_NC\_CPTS\_TS\_ADD\_VAL\_REG Register (Offset = 3D04Ch) [reset = 0h]

TS Add Value Register

Return to [Summary Table](#)

**Table 5-1076. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 D04Ch       |

**Figure 5-359. CPSW\_NC\_CPTS\_TS\_ADD\_VAL\_REG Name Register**

|          |    |    |    |    |    |         |    |
|----------|----|----|----|----|----|---------|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25      | 24 |
| RESERVED |    |    |    |    |    |         |    |
| NONE     |    |    |    |    |    |         |    |
| 0h       |    |    |    |    |    |         |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17      | 16 |
| RESERVED |    |    |    |    |    |         |    |
| NONE     |    |    |    |    |    |         |    |
| 0h       |    |    |    |    |    |         |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9       | 8  |
| RESERVED |    |    |    |    |    |         |    |
| NONE     |    |    |    |    |    |         |    |
| 0h       |    |    |    |    |    |         |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1       | 0  |
| RESERVED |    |    |    |    |    | ADD_VAL |    |
| NONE     |    |    |    |    |    | R/W     |    |
| 0h       |    |    |    |    |    | 0h      |    |

**Table 5-1078. CPSW\_NC\_CPTS\_TS\_ADD\_VAL\_REG Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                         |
|------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                            |
| 2:0  | ADD_VAL  | R/W  | 0h    | The ts_add_value[2:0] is added to 1 to comprise the timestamp increment value. The timestamp increment value is added to the current timestamp (time_stamp[63:0]) on each RCLK. The timestamp increment value can be adjusted by nudge and ppm also. The ts_add_val[2:0] value may be non-zero in 64-bit mode only. |

### 5.1.2.360 CPSW\_NC\_CPTS\_TS\_PPM\_LOW\_VAL\_REG Register

#### 1 CPSW\_NC\_CPTS\_TS\_PPM\_LOW\_VAL\_REG Register (Offset = 3D050h) [reset = 0h]

Time Stamp PPM Low Value Register

Return to [Summary Table](#)

**Table 5-1079. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 D050h       |

**Figure 5-360. CPSW\_NC\_CPTS\_TS\_PPM\_LOW\_VAL\_REG Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TS_PPM_LOW_VAL |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TS_PPM_LOW_VAL |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TS_PPM_LOW_VAL |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TS_PPM_LOW_VAL |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-1081. CPSW\_NC\_CPTS\_TS\_PPM\_LOW\_VAL\_REG Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                                                                                                                                                                                              |
|------|----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | TS_PPM_LOW_VAL | R/W  | 0h    | Time Stamp PPM Low Value - The 64-bit PPM value takes effect when this low value is written. The high value should be written first. Note: There should be at least 10 clocks in between writes to the low register to ensure that the previous operation has been seen. |

### 5.1.2.361 CPSW\_NC\_CPTS\_TS\_PPM\_HIGH\_VAL\_REG Register

#### 1 CPSW\_NC\_CPTS\_TS\_PPM\_HIGH\_VAL\_REG Register (Offset = 3D054h) [reset = 0h]

Time Stamp PPM High Value Register

Return to [Summary Table](#)

**Table 5-1082. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 D054h       |

**Figure 5-361. CPSW\_NC\_CPTS\_TS\_PPM\_HIGH\_VAL\_REG Name Register**

|                 |    |    |    |    |    |                 |    |
|-----------------|----|----|----|----|----|-----------------|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25              | 24 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17              | 16 |
| RESERVED        |    |    |    |    |    |                 |    |
| NONE            |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9               | 8  |
| RESERVED        |    |    |    |    |    | TS_PPM_HIGH_VAL |    |
| NONE            |    |    |    |    |    | R/W             |    |
| 0h              |    |    |    |    |    | 0h              |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1               | 0  |
| TS_PPM_HIGH_VAL |    |    |    |    |    |                 |    |
| R/W             |    |    |    |    |    |                 |    |
| 0h              |    |    |    |    |    |                 |    |

**Table 5-1084. CPSW\_NC\_CPTS\_TS\_PPM\_HIGH\_VAL\_REG Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                               |
|-------|-----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                  |
| 9:0   | TS_PPM_HIGH_VAL | R/W  | 0h    | Time Stamp PPM High Value - This value should be written first (before the low value is written). The minimum value of the ts_ppm is 0x400 (all 42 bits). |

### 5.1.2.362 CPSW\_NC\_CPTS\_TS\_NUDGE\_VAL\_REG Register

#### 1 CPSW\_NC\_CPTS\_TS\_NUDGE\_VAL\_REG Register (Offset = 3D058h) [reset = 0h]

Time Stamp Nudge Value Register

Return to [Summary Table](#)

**Table 5-1085. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 D058h       |

**Figure 5-362. CPSW\_NC\_CPTS\_TS\_NUDGE\_VAL\_REG Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED     |    |    |    |    |    |    |    |
| NONE         |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED     |    |    |    |    |    |    |    |
| NONE         |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED     |    |    |    |    |    |    |    |
| NONE         |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TS_NUDGE_VAL |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-1087. CPSW\_NC\_CPTS\_TS\_NUDGE\_VAL\_REG Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                                                                                                                                                        |
|------|--------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED     | NONE | 0h    | Reserved                                                                                                                                                                                                                           |
| 7:0  | TS_NUDGE_VAL | R/W  | 0h    | Timestamp Nudge Value - This two's complement number is added to the time_stamp[63:0] value to increase or decrease the timestamp value by the ts_nudge amount. The ts_nudge value is cleared to zero when the nudge has occurred. |

### 5.1.2.363 CPSW\_NC\_CPTS\_TS\_CONFIG Register

#### 1 CPSW\_NC\_CPTS\_TS\_CONFIG Register (Offset = 3D0D0h) [reset = 2002h]

Time Stamp Configuration Read

Return to [Summary Table](#)
**Table 5-1088. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 D0D0h       |

**Figure 5-363. CPSW\_NC\_CPTS\_TS\_CONFIG Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED        |    |    |    |    |    |    |    |
| NONE            |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| EVNT_FIFO_DEPTH |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 20h             |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| NUM_GENF        |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 2h              |    |    |    |    |    |    |    |

**Table 5-1090. CPSW\_NC\_CPTS\_TS\_CONFIG Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                     |
|-------|-----------------|------|-------|-----------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED        | NONE | 0h    | Reserved                                                                                                        |
| 15:8  | EVNT_FIFO_DEPTH | R    | 20h   | This is the configured value for the depth of the event FIFO. This parameter is passed in at module generation. |
| 7:0   | NUM_GENF        | R    | 2h    | This is the configured value for the number of GENF outputs. This parameter is passed in at module generation.  |

### 5.1.2.364 CPSW\_NC\_CPTS\_TS\_GENF\_COMP\_LOW\_REG\_L Register

#### 1 CPSW\_NC\_CPTS\_TS\_GENF\_COMP\_LOW\_REG\_L Register (Offset = 3D0E0h) [reset = 0h]

Time Stamp Generate Function Comparison Low Value

Return to [Summary Table](#)

Offset = Base + (I \* 20h); where I = 0 to 1d

**Table 5-1091. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 D0E0h + formula |

**Figure 5-364. CPSW\_NC\_CPTS\_TS\_GENF\_COMP\_LOW\_REG\_L Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COMP_LOW |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COMP_LOW |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COMP_LOW |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COMP_LOW |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-1093. CPSW\_NC\_CPTS\_TS\_GENF\_COMP\_LOW\_REG\_L Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                               |
|------|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | COMP_LOW | R/W  | 0h    | GENFn comparison value lower 32-bits. This value should be written after the upper 32-bits. The ts_GENFn_comp high and low should only be written when the ts_GENFn_length value is zero. |

### 5.1.2.365 CPSW\_NC\_CPTS\_TS\_GENF\_COMP\_HIGH\_REG\_L Register

#### 1 CPSW\_NC\_CPTS\_TS\_GENF\_COMP\_HIGH\_REG\_L Register (Offset = 3D0E4h) [reset = 0h]

Time Stamp Generate Function Comparison high Value

Return to [Summary Table](#)

Offset = Base + (I \* 20h); where I = 0 to 1d

**Table 5-1094. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 D0E4h + formula |

**Figure 5-365. CPSW\_NC\_CPTS\_TS\_GENF\_COMP\_HIGH\_REG\_L Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COMP_HIGH |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COMP_HIGH |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COMP_HIGH |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COMP_HIGH |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 5-1096. CPSW\_NC\_CPTS\_TS\_GENF\_COMP\_HIGH\_REG\_L Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                            |
|------|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | COMP_HIGH | R/W  | 0h    | GENFn comparison value upper 32-bits. This value should be written before the lower 32-bits are written. The ts_GENFn_comp high and low should only be written when the ts_GENFn_length value is zero. |

### 5.1.2.366 CPSW\_NC\_CPTS\_TS\_GENF\_CONTROL\_REG\_L Register

#### 1 CPSW\_NC\_CPTS\_TS\_GENF\_CONTROL\_REG\_L Register (Offset = 3D0E8h) [reset = 0h]

Time Stamp Generate Function Control

Return to [Summary Table](#)

Offset = Base + (I \* 20h); where I = 0 to 1d

**Table 5-1097. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 D0E8h + formula |

**Figure 5-366. CPSW\_NC\_CPTS\_TS\_GENF\_CONTROL\_REG\_L Name Register**

|          |    |    |    |    |    |         |              |
|----------|----|----|----|----|----|---------|--------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25      | 24           |
| RESERVED |    |    |    |    |    |         |              |
| NONE     |    |    |    |    |    |         |              |
| 0h       |    |    |    |    |    |         |              |
| 23       | 22 | 21 | 20 | 19 | 18 | 17      | 16           |
| RESERVED |    |    |    |    |    |         |              |
| NONE     |    |    |    |    |    |         |              |
| 0h       |    |    |    |    |    |         |              |
| 15       | 14 | 13 | 12 | 11 | 10 | 9       | 8            |
| RESERVED |    |    |    |    |    |         |              |
| NONE     |    |    |    |    |    |         |              |
| 0h       |    |    |    |    |    |         |              |
| 7        | 6  | 5  | 4  | 3  | 2  | 1       | 0            |
| RESERVED |    |    |    |    |    | PPM_DIR | POLARITY_INV |
| NONE     |    |    |    |    |    | R/W     | R/W          |
| 0h       |    |    |    |    |    | 0h      | 0h           |

**Table 5-1099. CPSW\_NC\_CPTS\_TS\_GENF\_CONTROL\_REG\_L Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                          |
|------|--------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED     | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                             |
| 1    | PPM_DIR      | R/W  | 0h    | Generate function N PPM direction -<br>0 - A single RCLK is added to the generate function counter at the PPM rate which has the effect of decreasing the generate function frequency by the PPM amount.<br>1 - A single RCLK is subtracted from the generate function counter at the PPM rate which has the effect of increasing the generate function frequency by the PPM amount. |
| 0    | POLARITY_INV | R/W  | 0h    | Generate function N Polarity -<br>0 - The output TS_GENFn signal asserts high.<br>1 - The output TS_GENFn signal asserts low                                                                                                                                                                                                                                                         |



### 5.1.2.367 CPSW\_NC\_CPTS\_TS\_GENF\_LENGTH\_REG\_L Register

#### 1 CPSW\_NC\_CPTS\_TS\_GENF\_LENGTH\_REG\_L Register (Offset = 3D0ECh) [reset = 0h]

Time Stamp Generate Function Length Value

Return to [Summary Table](#)

Offset = Base + (I \* 20h); where I = 0 to 1d

**Table 5-1100. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 D0ECh + formula |

**Figure 5-367. CPSW\_NC\_CPTS\_TS\_GENF\_LENGTH\_REG\_L Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| LENGTH |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LENGTH |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| LENGTH |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LENGTH |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-1102. CPSW\_NC\_CPTS\_TS\_GENF\_LENGTH\_REG\_L Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                       |
|------|--------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | LENGTH | R/W  | 0h    | GENFn length - The minimum operational value is decimal 5.<br>Note: Software is advised to write and then read the comparison value before writing a non-zero value to the genf length to ensure that the comparison value is synchronized across the boundary before the length. |

### 5.1.2.368 CPSW\_NC\_CPTS\_TS\_GENF\_PPM\_LOW\_REG\_L Register

#### 1 CPSW\_NC\_CPTS\_TS\_GENF\_PPM\_LOW\_REG\_L Register (Offset = 3D0F0h) [reset = 0h]

Time Stamp Generate Function PPM Low Value

Return to [Summary Table](#)

Offset = Base + (I \* 20h); where I = 0 to 1d

**Table 5-1103. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 D0F0h + formula |

**Figure 5-368. CPSW\_NC\_CPTS\_TS\_GENF\_PPM\_LOW\_REG\_L Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PPM_LOW |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PPM_LOW |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PPM_LOW |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PPM_LOW |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-1105. CPSW\_NC\_CPTS\_TS\_GENF\_PPM\_LOW\_REG\_L Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                     |
|------|---------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PPM_LOW | R/W  | 0h    | GENFn PPM Low Value - The 64-bit PPM value takes effect when this low value is written. The high value should be written first. |

### 5.1.2.369 CPSW\_NC\_CPTS\_TS\_GENF\_PPM\_HIGH\_REG\_L Register

#### 1 CPSW\_NC\_CPTS\_TS\_GENF\_PPM\_HIGH\_REG\_L Register (Offset = 3D0F4h) [reset = 0h]

Time Stamp Generate Function PPM High Value

Return to [Summary Table](#)

Offset = Base + (I \* 20h); where I = 0 to 1d

**Table 5-1106. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 D0F4h + formula |

**Figure 5-369. CPSW\_NC\_CPTS\_TS\_GENF\_PPM\_HIGH\_REG\_L Name Register**

|          |    |    |    |    |    |          |    |
|----------|----|----|----|----|----|----------|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25       | 24 |
| RESERVED |    |    |    |    |    |          |    |
| NONE     |    |    |    |    |    |          |    |
| 0h       |    |    |    |    |    |          |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17       | 16 |
| RESERVED |    |    |    |    |    |          |    |
| NONE     |    |    |    |    |    |          |    |
| 0h       |    |    |    |    |    |          |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9        | 8  |
| RESERVED |    |    |    |    |    | PPM_HIGH |    |
| NONE     |    |    |    |    |    | R/W      |    |
| 0h       |    |    |    |    |    | 0h       |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1        | 0  |
| PPM_HIGH |    |    |    |    |    |          |    |
| R/W      |    |    |    |    |    |          |    |
| 0h       |    |    |    |    |    |          |    |

**Table 5-1108. CPSW\_NC\_CPTS\_TS\_GENF\_PPM\_HIGH\_REG\_L Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                  |
|-------|----------|------|-------|----------------------------------------------------------------------------------------------|
| 31:10 | RESERVED | NONE | 0h    | Reserved                                                                                     |
| 9:0   | PPM_HIGH | R/W  | 0h    | GENFn PPM High Value - This value should be written first (before the low value is written). |

### 5.1.2.370 CPSW\_NC\_CPTS\_TS\_GENF\_NUDGE\_REG\_L Register

#### 1 CPSW\_NC\_CPTS\_TS\_GENF\_NUDGE\_REG\_L Register (Offset = 3D0F8h) [reset = 0h]

Time Stamp Generate Function Nudge Value

Return to [Summary Table](#)

Offset = Base + (I \* 20h); where I = 0 to 1d

**Table 5-1109. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 D0F8h + formula |

**Figure 5-370. CPSW\_NC\_CPTS\_TS\_GENF\_NUDGE\_REG\_L Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| NUDGE    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-1111. CPSW\_NC\_CPTS\_TS\_GENF\_NUDGE\_REG\_L Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                      |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                         |
| 7:0  | NUDGE    | R/W  | 0h    | GENFn Nudge Value - This two's complement number is added to the generate counter value to increase or decrease the length by the ts_genfN_nudge amount. Only a single high or low time is adjusted and the ts_genfN_nudge value is cleared to zero when the nudge has occurred. |

### 5.1.2.371 CPSW\_NC\_CPTS\_TS\_ESTF\_COMP\_LOW\_REG\_L Register

#### 1 CPSW\_NC\_CPTS\_TS\_ESTF\_COMP\_LOW\_REG\_L Register (Offset = 3D200h) [reset = 0h]

Time Stamp ESTF Generate Function Comparison Low Value

Return to [Summary Table](#)

Offset = Base + (I \* 20h); where I = 0 to 1d

**Table 5-1112. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 D200h + formula |

**Figure 5-371. CPSW\_NC\_CPTS\_TS\_ESTF\_COMP\_LOW\_REG\_L Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COMP_LOW |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COMP_LOW |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COMP_LOW |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COMP_LOW |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-1114. CPSW\_NC\_CPTS\_TS\_ESTF\_COMP\_LOW\_REG\_L Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                               |
|------|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | COMP_LOW | R/W  | 0h    | ESTFn comparison value lower 32-bits. This value should be written after the upper 32-bits. The ts_ESTFn_comp high and low should only be written when the ts_ESTFn_length value is zero. |

### 5.1.2.372 CPSW\_NC\_CPTS\_TS\_ESTF\_COMP\_HIGH\_REG\_L Register

#### 1 CPSW\_NC\_CPTS\_TS\_ESTF\_COMP\_HIGH\_REG\_L Register (Offset = 3D204h) [reset = 0h]

Time Stamp ESTF Generate Function Comparison high Value

Return to [Summary Table](#)

Offset = Base + (I \* 20h); where I = 0 to 1d

**Table 5-1115. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 D204h + formula |

**Figure 5-372. CPSW\_NC\_CPTS\_TS\_ESTF\_COMP\_HIGH\_REG\_L Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COMP_HIGH |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COMP_HIGH |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COMP_HIGH |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COMP_HIGH |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 5-1117. CPSW\_NC\_CPTS\_TS\_ESTF\_COMP\_HIGH\_REG\_L Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                            |
|------|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | COMP_HIGH | R/W  | 0h    | ESTFn comparison value upper 32-bits. This value should be written before the lower 32-bits are written. The ts_ESTFn_comp high and low should only be written when the ts_ESTFn_length value is zero. |

### 5.1.2.373 CPSW\_NC\_CPTS\_TS\_ESTF\_CONTROL\_REG\_L Register

#### 1 CPSW\_NC\_CPTS\_TS\_ESTF\_CONTROL\_REG\_L Register (Offset = 3D208h) [reset = 0h]

Time Stamp ESTF Generate Function Control

Return to [Summary Table](#)

Offset = Base + (I \* 20h); where I = 0 to 1d

**Table 5-1118. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 D208h + formula |

**Figure 5-373. CPSW\_NC\_CPTS\_TS\_ESTF\_CONTROL\_REG\_L Name Register**

|          |    |    |    |    |    |         |              |
|----------|----|----|----|----|----|---------|--------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25      | 24           |
| RESERVED |    |    |    |    |    |         |              |
| NONE     |    |    |    |    |    |         |              |
| 0h       |    |    |    |    |    |         |              |
| 23       | 22 | 21 | 20 | 19 | 18 | 17      | 16           |
| RESERVED |    |    |    |    |    |         |              |
| NONE     |    |    |    |    |    |         |              |
| 0h       |    |    |    |    |    |         |              |
| 15       | 14 | 13 | 12 | 11 | 10 | 9       | 8            |
| RESERVED |    |    |    |    |    |         |              |
| NONE     |    |    |    |    |    |         |              |
| 0h       |    |    |    |    |    |         |              |
| 7        | 6  | 5  | 4  | 3  | 2  | 1       | 0            |
| RESERVED |    |    |    |    |    | PPM_DIR | POLARITY_INV |
| NONE     |    |    |    |    |    | R/W     | R/W          |
| 0h       |    |    |    |    |    | 0h      | 0h           |

**Table 5-1120. CPSW\_NC\_CPTS\_TS\_ESTF\_CONTROL\_REG\_L Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                          |
|------|--------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED     | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                             |
| 1    | PPM_DIR      | R/W  | 0h    | Generate function N PPM direction -<br>0 - A single RCLK is added to the generate function counter at the PPM rate which has the effect of decreasing the generate function frequency by the PPM amount.<br>1 - A single RCLK is subtracted from the generate function counter at the PPM rate which has the effect of increasing the generate function frequency by the PPM amount. |
| 0    | POLARITY_INV | R/W  | 0h    | Generate function N Polarity -<br>0 - The output TS_ESTFn signal asserts low.<br>1 - The output TS_ESTFn signal asserts high.                                                                                                                                                                                                                                                        |

### 5.1.2.374 CPSW\_NC\_CPTS\_TS\_ESTF\_LENGTH\_REG\_L Register

#### 1 CPSW\_NC\_CPTS\_TS\_ESTF\_LENGTH\_REG\_L Register (Offset = 3D20Ch) [reset = 0h]

Time Stamp ESTF Generate Function Length Value

Return to [Summary Table](#)

Offset = Base + (I \* 20h); where I = 0 to 1d

**Table 5-1121. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 D20Ch + formula |

**Figure 5-374. CPSW\_NC\_CPTS\_TS\_ESTF\_LENGTH\_REG\_L Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| LENGTH |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| LENGTH |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| LENGTH |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LENGTH |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-1123. CPSW\_NC\_CPTS\_TS\_ESTF\_LENGTH\_REG\_L Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                       |
|------|--------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | LENGTH | R/W  | 0h    | ESTFn length - The minimum operational value is decimal 5.<br>Note: Software is advised to write and then read the comparison value before writing a non-zero value to the genf length to ensure that the comparison value is synchronized across the boundary before the length. |



### 5.1.2.375 CPSW\_NC\_CPTS\_TS\_ESTF\_PPM\_LOW\_REG\_L Register

#### 1 CPSW\_NC\_CPTS\_TS\_ESTF\_PPM\_LOW\_REG\_L Register (Offset = 3D210h) [reset = 0h]

Time Stamp ESTF Generate Function PPM Low Value

Return to [Summary Table](#)

Offset = Base + (I \* 20h); where I = 0 to 1d

**Table 5-1124. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 D210h + formula |

**Figure 5-375. CPSW\_NC\_CPTS\_TS\_ESTF\_PPM\_LOW\_REG\_L Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PPM_LOW |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PPM_LOW |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PPM_LOW |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PPM_LOW |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-1126. CPSW\_NC\_CPTS\_TS\_ESTF\_PPM\_LOW\_REG\_L Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                     |
|------|---------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PPM_LOW | R/W  | 0h    | ESTFn PPM Low Value - The 64-bit PPM value takes effect when this low value is written. The high value should be written first. |

### 5.1.2.376 CPSW\_NC\_CPTS\_TS\_ESTF\_PPM\_HIGH\_REG\_L Register

#### 1 CPSW\_NC\_CPTS\_TS\_ESTF\_PPM\_HIGH\_REG\_L Register (Offset = 3D214h) [reset = 0h]

Time Stamp ESTF Generate Function PPM High Value

Return to [Summary Table](#)

Offset = Base + (I \* 20h); where I = 0 to 1d

**Table 5-1127. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 D214h + formula |

**Figure 5-376. CPSW\_NC\_CPTS\_TS\_ESTF\_PPM\_HIGH\_REG\_L Name Register**

|          |    |    |    |    |    |          |    |
|----------|----|----|----|----|----|----------|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25       | 24 |
| RESERVED |    |    |    |    |    |          |    |
| NONE     |    |    |    |    |    |          |    |
| 0h       |    |    |    |    |    |          |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17       | 16 |
| RESERVED |    |    |    |    |    |          |    |
| NONE     |    |    |    |    |    |          |    |
| 0h       |    |    |    |    |    |          |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9        | 8  |
| RESERVED |    |    |    |    |    | PPM_HIGH |    |
| NONE     |    |    |    |    |    | R/W      |    |
| 0h       |    |    |    |    |    | 0h       |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1        | 0  |
| PPM_HIGH |    |    |    |    |    |          |    |
| R/W      |    |    |    |    |    |          |    |
| 0h       |    |    |    |    |    |          |    |

**Table 5-1129. CPSW\_NC\_CPTS\_TS\_ESTF\_PPM\_HIGH\_REG\_L Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                  |
|-------|----------|------|-------|----------------------------------------------------------------------------------------------|
| 31:10 | RESERVED | NONE | 0h    | Reserved                                                                                     |
| 9:0   | PPM_HIGH | R/W  | 0h    | ESTFn PPM High Value - This value should be written first (before the low value is written). |

### 5.1.2.377 CPSW\_NC\_CPTS\_TS\_ESTF\_NUDGE\_REG\_L Register

#### 1 CPSW\_NC\_CPTS\_TS\_ESTF\_NUDGE\_REG\_L Register (Offset = 3D218h) [reset = 0h]

Time Stamp ESTF Generate Function Nudge Value

Return to [Summary Table](#)

Offset = Base + (I \* 20h); where I = 0 to 1d

**Table 5-1130. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| CPSW0         | 5283 D218h + formula |

**Figure 5-377. CPSW\_NC\_CPTS\_TS\_ESTF\_NUDGE\_REG\_L Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| NUDGE    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-1132. CPSW\_NC\_CPTS\_TS\_ESTF\_NUDGE\_REG\_L Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                      |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                         |
| 7:0  | NUDGE    | R/W  | 0h    | ESTFn Nudge Value - This two's complement number is added to the generate counter value to increase or decrease the length by the ts_estfN_nudge amount. Only a single high or low time is adjusted and the ts_estfN_nudge value is cleared to zero when the nudge has occurred. |

### 5.1.2.378 CPSW\_NC\_ALE\_MOD\_VER Register

#### 1 CPSW\_NC\_ALE\_MOD\_VER Register (Offset = 3E000h) [reset = 291105h]

The Module and Version Register identifies the module identifier and revision of the ALE\_3g512e module.

Return to [Summary Table](#)

**Table 5-1133. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E000h       |

**Figure 5-378. CPSW\_NC\_ALE\_MOD\_VER Name Register**

|                 |    |                |    |                |    |    |    |
|-----------------|----|----------------|----|----------------|----|----|----|
| 31              | 30 | 29             | 28 | 27             | 26 | 25 | 24 |
| MODULE_ID       |    |                |    |                |    |    |    |
| R               |    |                |    |                |    |    |    |
| 29h             |    |                |    |                |    |    |    |
| 23              | 22 | 21             | 20 | 19             | 18 | 17 | 16 |
| MODULE_ID       |    |                |    |                |    |    |    |
| R               |    |                |    |                |    |    |    |
| 29h             |    |                |    |                |    |    |    |
| 15              | 14 | 13             | 12 | 11             | 10 | 9  | 8  |
| RTL_VERSION     |    |                |    | MAJOR_REVISION |    |    |    |
| R               |    |                |    | R              |    |    |    |
| 2h              |    |                |    | 1h             |    |    |    |
| 7               | 6  | 5              | 4  | 3              | 2  | 1  | 0  |
| CUSTOM_REVISION |    | MINOR_REVISION |    |                |    |    |    |
| R               |    | R              |    |                |    |    |    |
| 0h              |    | 5h             |    |                |    |    |    |

**Table 5-1135. CPSW\_NC\_ALE\_MOD\_VER Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description           |
|-------|-----------------|------|-------|-----------------------|
| 31:16 | MODULE_ID       | R    | 29h   | ALE_3g512e module ID. |
| 15:11 | RTL_VERSION     | R    | 2h    | RTL Version.          |
| 10:8  | MAJOR_REVISION  | R    | 1h    | Major Revision.       |
| 7:6   | CUSTOM_REVISION | R    | 0h    | Custom Revision.      |
| 5:0   | MINOR_REVISION  | R    | 5h    | Minor Revision.       |

### 5.1.2.379 CPSW\_NC\_ALE\_STATUS Register

#### 1 CPSW\_NC\_ALE\_STATUS Register (Offset = 3E004h) [reset = 80000400h]

The ALE status provides information on the ALE configuration and state. The ramdepth is used to determine how IPv6 entries are stored in the table. IPv6 entries are stored in two entries where IPv6 Entry Hi is designated by the odd slice index and Lo is designated by the even slice index. The slice index is above the ram depth like {SliceIndex,RamIndex}. So, for a 64 deep RAM index of 0x005, the Hi portion of the IPv6 entry is located at 0x005(0x040) and the Lo portion is located at 0x005 & (~0x040).

Return to [Summary Table](#)

**Table 5-1136. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E004h       |

**Figure 5-379. CPSW\_NC\_ALE\_STATUS Name Register**

| 31                  | 30                  | 29       | 28          | 27 | 26 | 25 | 24 |
|---------------------|---------------------|----------|-------------|----|----|----|----|
| UREGANDREG<br>MSK12 | UREGANDREG<br>MSK08 | RESERVED |             |    |    |    |    |
| R                   | R                   | NONE     |             |    |    |    |    |
| 1h                  | 0h                  | 0h       |             |    |    |    |    |
| 23                  | 22                  | 21       | 20          | 19 | 18 | 17 | 16 |
| RESERVED            |                     |          |             |    |    |    |    |
| NONE                |                     |          |             |    |    |    |    |
| 0h                  |                     |          |             |    |    |    |    |
| 15                  | 14                  | 13       | 12          | 11 | 10 | 9  | 8  |
| POLCNTDIV8          |                     |          |             |    |    |    |    |
| R                   |                     |          |             |    |    |    |    |
| 4h                  |                     |          |             |    |    |    |    |
| 7                   | 6                   | 5        | 4           | 3  | 2  | 1  | 0  |
| RAMDEPTH12<br>8     | RAMDEPTH32          | RESERVED | KLUMENTRIES |    |    |    |    |
| R                   | R                   | NONE     | R           |    |    |    |    |
| 0h                  | 0h                  | 0h       | 0h          |    |    |    |    |

**Table 5-1138. CPSW\_NC\_ALE\_STATUS Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                  |
|-------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | UREGANDREGMSK12 | R    | 1h    | When set, the unregistered multicast field is a mask versus an index on 12 bit boundary in the ALE table.                                                    |
| 30    | UREGANDREGMSK08 | R    | 0h    | When set, the unregistered multicast field is a mask versus an index on 8 bit boundary in the ALE table.                                                     |
| 29:16 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                     |
| 15:8  | POLCNTDIV8      | R    | 4h    | This is the number of Classifiers the ALE implements divided by 8. A value of 4 indicates 32 policer engines total.                                          |
| 7     | RAMDEPTH128     | R    | 0h    | The number of ALE entries per slice of the table when this is set it indicates the depth is 128 if both ramdepth128 and ramdepth32 are zero the depth is 64. |
| 6     | RAMDEPTH32      | R    | 0h    | The number of ALE entries per slice of the table when this is set it indicates the depth is 32 if both ramdepth128 and ramdepth32 are zero the depth is 64.  |
| 5     | RESERVED        | NONE | 0h    | Reserved                                                                                                                                                     |

**Table 5-1138. CPSW\_NC\_ALE\_STATUS Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                      |
|-----|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | KLUENTRIES | R    | 0h    | This is the number of table entries total divided by 1024. A value of 1 indicates 1024 table entries. A value of 8 indicates 8192 table entries. |

### 5.1.2.380 CPSW\_NC\_ALE\_CONTROL Register

#### 1 CPSW\_NC\_ALE\_CONTROL Register (Offset = 3E008h) [reset = 0h]

The ALE Control Register is used to set the ALE modes used for all ports.

Return to [Summary Table](#)

**Table 5-1139. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E008h       |

**Figure 5-380. CPSW\_NC\_ALE\_CONTROL Name Register**

| 31              | 30              | 29             | 28            | 27              | 26             | 25              | 24                |
|-----------------|-----------------|----------------|---------------|-----------------|----------------|-----------------|-------------------|
| ENABLE_ALE      | CLEAR_TABLE     | AGE_OUT_NOW    | RESERVED      |                 |                | MIRROR_DP       |                   |
| R/W             | R/W             | R/W            | NONE          |                 |                | R/W             |                   |
| 0h              | 0h              | 0h             | 0h            |                 |                | 0h              |                   |
| 23              | 22              | 21             | 20            | 19              | 18             | 17              | 16                |
| UPD_BW_CTRL     |                 |                | RESERVED      |                 |                | MIRROR_TOP      |                   |
| R/W             |                 |                | NONE          |                 |                | R/W             |                   |
| 0h              |                 |                | 0h            |                 |                | 0h              |                   |
| 15              | 14              | 13             | 12            | 11              | 10             | 9               | 8                 |
| UPD_STATIC      | LRN_HOST_DST    | UVLAN_NO_LEARN | MIRROR_MEN    | MIRROR_DEN      | MIRROR_SEN     | RESERVED        | EN_HOST_UNIFLOOD  |
| R/W             | R/W             | R/W            | R/W           | R/W             | R/W            | NONE            | R/W               |
| 0h              | 0h              | 0h             | 0h            | 0h              | 0h             | 0h              | 0h                |
| 7               | 6               | 5              | 4             | 3               | 2              | 1               | 0                 |
| LEARN_NO_VLANID | ENABLE_VIDOMODE | ENABLE_OUIDENY | ENABLE_BYPASS | BCAST_MCAS_TCTL | ALE_VLAN_AWARE | ENABLE_AUTHMODE | ENABLE_RATE_LIMIT |
| R/W             | R/W             | R/W            | R/W           | R/W             | R/W            | R/W             | R/W               |
| 0h              | 0h              | 0h             | 0h            | 0h              | 0h             | 0h              | 0h                |

**Table 5-1141. CPSW\_NC\_ALE\_CONTROL Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | ENABLE_ALE  | R/W  | 0h    | Enable ALE<br>0 - Drop all packets<br>1 - Enable ALE packet processing                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 30    | CLEAR_TABLE | R/W  | 0h    | Clear ALE address table - Setting this bit causes the ALE hardware to write all table bit values to zero. Software must perform a clear table operation as part of the ALE setup/configuration process. Setting this bit causes all ALE accesses to be held up for 64 clocks while the clear is performed. Access to all ALE registers will be blocked (wait states) until the 64 clocks have completed. This bit cannot be read as one because the read is blocked until the clear table is completed at which time this bit is cleared to zero. |
| 29    | AGE_OUT_NOW | R/W  | 0h    | Age Out Address Table Now - Setting this bit causes the ALE hardware to remove (free up) any ageable table entry that does not have a set touch bit. This bit is cleared when the age out process has completed. This bit may be read. The age out process takes four times the number of table entries clock cycles (4096 cycles for 1K addresses) best case (no ale packet processing during ageout) and sixty five times the number of table entries clock cycles (66560 cycles for 1K addresses) absolute worst case.                         |
| 28:26 | RESERVED    | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

**Table 5-1141. CPSW\_NC\_ALE\_CONTROL Register Field Descriptions (continued)**

| Bit   | Field             | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|-------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 25:24 | MIRROR_DP         | R/W  | 0h    | Mirror Destination Port - This field defines the port to which destination traffic destined will be duplicated. That is all traffic that is forwarded to this port will also be mirrored to the mirror_top port.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 23:21 | UPD_BW_CTRL       | R/W  | 0h    | The upd_bw_ctrl field allows for up to 8 times the rate in which adds, updates, touches, writes, and aging updates can occur. At frequencies of 350Mhz, the table update rate should be at it lowest or 5 Million updates per second. When operating the switch core at frequencies or above, the upd_bw_ctrl can be programmed more aggressive. If the upd_bw_ctrl is set but the frequency of the switch subsystem is below the associated value, ALE will drop packets due to insufficient time to complete lookup under high traffic loads.<br>0 - 350Mhz, 5M<br>1 - 359Mhz, 11M<br>2 - 367Mhz, 16M<br>3 - 375Mhz, 22M<br>4 - 384Mhz, 28M<br>5 - 392Mhz, 34M<br>6 - 400Mhz, 39M<br>7 - 409Mhz, 45M |
| 20:18 | RESERVED          | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 17:16 | MIRROR_TOP        | R/W  | 0h    | Mirror To Port - This field defines the destination port for the mirror traffic. If the traffic is received or transmitted on the mirror destination port it will not be duplicated. Traffic defined as mirror traffic only may be dropped by the switch due to congestion.                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 15    | UPD_STATIC        | R/W  | 0h    | Update Static Entries - A static Entry is an entry that is not agable. When clear this bit will prevent any static entry (agable bit clear) from being updated due to port change. When set it allows static entries (agable bit clear) to update the source port if required. This bit should normally be '0' for most switch configurations.                                                                                                                                                                                                                                                                                                                                                         |
| 14    | LRN_HOST_DST      | R/W  | 0h    | Learn Host Destination - This field is set to only learn unicast packet source addresses that are destined to the host port. This bit is only valid for 3 port switches and allows the ALE table to only contain addresses the host port is concerned about. This bit is affectively disabled when en_host_uni_flood is set since any unknown unicast is also sent to the host port for extended bridging operations.                                                                                                                                                                                                                                                                                  |
| 13    | UVLAN_NO_LEARN    | R/W  | 0h    | Unknown VLAN No Learn - This field when set will prevent source addresses of unknown VLAN IDs from being automatically added into the look up table if learning is enabled.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 12    | MIRROR_MEN        | R/W  | 0h    | Mirror Match Entry Enable - This field enables the match mirror option. When this bit is set any traffic whose destination, source, VLAN or OUI matches the mirror_midx entry index will have that traffic also sent to the mirror_top port.                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 11    | MIRROR_DEN        | R/W  | 0h    | Mirror Destination Port Enable - This field enables the destination port mirror option. When this bit is set any traffic destined for the mirror_dp port will have its transmit traffic also sent to the mirror_top port.                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 10    | MIRROR_SEN        | R/W  | 0h    | Mirror Source Port Enable - This field enables the source port mirror option. When this bit is set any port with the pX_mirror_sp set in the ALE Port Control registers set will have its received traffic also sent to the mirror_top port.                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 9     | RESERVED          | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 8     | EN_HOST_UNI_FLOOD | R/W  | 0h    | Unknown unicast packets flood to host<br>0 - unknown unicast packets are not sent to the host<br>1 - unknown unicast packets flood to host port as well as other ports                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 7     | LEARN_NO_VLANID   | R/W  | 0h    | Learn No VID -<br>0 - VID is learned with the source address<br>1 - VID is not learned with the source address (source address is not tied to VID). Determines the entry type.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |



**Table 5-1141. CPSW\_NC\_ALE\_CONTROL Register Field Descriptions (continued)**

| Bit | Field             | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-----|-------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6   | ENABLE_VID0_MODE  | R/W  | 0h    | Enable VLAN ID = 0 Mode<br>0 - Process the priority tagged packet with VID = PORT_VLAN[11:0].<br>1 - Process the priority tagged packet with VID = 0.                                                                                                                                                                                                                                                                                        |
| 5   | ENABLE_OUI_DENY   | R/W  | 0h    | Enable OUI Deny Mode - When set, any packet with a non-matching OUI source address will be dropped to the host unless the packet destination address matches a supervisory destination address table entry. When cleared, any packet source address matching an OUI address table entry will be dropped to the host unless the destination address matches with a supervisory destination address table entry.                               |
| 4   | ENABLE_BYPASS     | R/W  | 0h    | ALE Bypass - When set, packets received on non-host ports are sent to the host. It is expected that packets from the host are directed to the particular port.<br>0 - no bypass<br>1 - bypass the ALE                                                                                                                                                                                                                                        |
| 3   | BCAST_MCAST_CTL   | R/W  | 0h    | Rate Limit Transmit mode<br>0 - Broadcast and multicast rate limit counters are received port based<br>1 - Broadcast and multicast rate limit counters are transmit port based                                                                                                                                                                                                                                                               |
| 2   | ALE_VLAN_AWARE    | R/W  | 0h    | ALE VLAN Aware - Determines how traffic is forwarded using VLAN rules.<br>0 - Simple switch rules, packets forwarded to all ports for unknown destinations.<br>1 - VLAN Aware rules, packets forwarded based on VLAN members                                                                                                                                                                                                                 |
| 1   | ENABLE_AUTH_MODE  | R/W  | 0h    | Enable MAC Authorization Mode - Mac authorization mode requires that all table entries be made by the host software. There is no auto learning of addresses in authorization mode and the packet will be dropped if the source address is not found (and the destination address is not a multicast address with the super table entry bit set).<br>0 - The ALE is not in MAC authorization mode<br>1 - The ALE is in MAC authorization mode |
| 0   | ENABLE_RATE_LIMIT | R/W  | 0h    | Enable Broadcast and Multicast Rate Limit<br>0 - Broadcast/Multicast rates not limited<br>1 - Broadcast/Multicast packet reception limited to the port control register rate limit fields.                                                                                                                                                                                                                                                   |

### 5.1.2.381 CPSW\_NC\_ALE\_CTRL2 Register

#### 1 CPSW\_NC\_ALE\_CTRL2 Register (Offset = 3E00Ch) [reset = 0h]

The ALE Control 2 Register is used to set the extended features used for all ports.

Return to [Summary Table](#)

**Table 5-1142. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E00Ch       |

**Figure 5-381. CPSW\_NC\_ALE\_CTRL2 Name Register**

| 31          | 30             | 29         | 28           | 27           | 26       | 25         | 24          |
|-------------|----------------|------------|--------------|--------------|----------|------------|-------------|
| TRK_EN_DST  | TRK_EN_SRC     | TRK_EN_PRI | RESERVED     | TRK_EN_IVLAN | RESERVED | TRK_EN_SIP | TRK_EN_DIP  |
| R/W         | R/W            | R/W        | NONE         | R/W          | NONE     | R/W        | R/W         |
| 0h          | 0h             | 0h         | 0h           | 0h           | 0h       | 0h         | 0h          |
| 23          | 22             | 21         | 20           | 19           | 18       | 17         | 16          |
| DROP_BADLEN | NODROP_SRCMCST | DEFNOFRAG  | DEFLMTNXTHDR | RESERVED     | TRK_BASE |            |             |
| R/W         | R/W            | R/W        | R/W          | NONE         | R/W      |            |             |
| 0h          | 0h             | 0h         | 0h           | 0h           | 0h       |            |             |
| 15          | 14             | 13         | 12           | 11           | 10       | 9          | 8           |
| MULTIHOST   | RESERVED       |            |              |              |          |            | MIRROR_MIDX |
| R/W         | NONE           |            |              |              |          |            | R/W         |
| 0h          | 0h             |            |              |              |          |            | 0h          |
| 7           | 6              | 5          | 4            | 3            | 2        | 1          | 0           |
| MIRROR_MIDX |                |            |              |              |          |            |             |
| R/W         |                |            |              |              |          |            |             |
| 0h          |                |            |              |              |          |            |             |

**Table 5-1144. CPSW\_NC\_ALE\_CTRL2 Register Field Descriptions**

| Bit | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                |
|-----|--------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31  | TRK_EN_DST   | R/W  | 0h    | Trunk Enable Destination Address - This field enables the destination MAC address to be used with the hash function $G(X) = 1 + X + X^3$ and affect the trunk port transmit link determination.                                                                                                                                                            |
| 30  | TRK_EN_SRC   | R/W  | 0h    | Trunk Enable Source Address - This field enables the source MAC address to be used with the hash function $G(X) = 1 + X + X^3$ and affect the trunk port transmit link determination.                                                                                                                                                                      |
| 29  | TRK_EN_PRI   | R/W  | 0h    | Trunk Enable Priority - This field enables the VLAN Priority bits to be used with the hash function $G(X) = 1 + X + X^3$ and affect the trunk port transmit link determination. In the event that DSCP mapping is enabled and there is no VLAN the DSCP priority will be used. For all other non IP frames without VLAN the port default priority is used. |
| 28  | RESERVED     | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                   |
| 27  | TRK_EN_IVLAN | R/W  | 0h    | Trunk Enable Inner VLAN - This field enables the inner VLAN ID value (C-VLANID) to be used with the hash function $G(X) = 1 + X + X^3$ and affect the trunk port transmit link determination.                                                                                                                                                              |
| 26  | RESERVED     | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                   |
| 25  | TRK_EN_SIP   | R/W  | 0h    | Trunk Enable Source IP Address - This field enables the source IP address to be used with the hash function $G(X) = 1 + X + X^3$ and affect the trunk port transmit link determination. This feature supports No tag, Priority tagged, VLAN tagged, Q-in-Q double tagging for both IPV6 and IPV4.                                                          |

**Table 5-1144. CPSW\_NC\_ALE\_CTRL2 Register Field Descriptions (continued)**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24    | TRK_EN_DIP     | R/W  | 0h    | Trunk Enable Destination IP Address - This field enables the destination IP address to be used with the hash function $G(X) = 1 + X + X^3$ and affect the trunk port transmit link determination. This feature supports No tag, Priority tagged, VLAN tagged, Q-in-Q double tagging for both IPV6 and IPV4.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 23    | DROP_BADLEN    | R/W  | 0h    | Drop Bad Length will drop any packet that the 802.3 length field is larger than the packet. Ethertypes 0-1500 are 802.3 lengths, all others are Ether types.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 22    | NODROP_SRCMCST | R/W  | 0h    | No Drop Source Multicast will disable the dropping of any source address with the multicast bit set.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 21    | DEFNOFRAG      | R/W  | 0h    | Default No Frag field will cause an IPv4 fragmented packet to be dropped if a VLAN entry is not found.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 20    | DEFLMTNXTHDR   | R/W  | 0h    | Default limit next header field will cause an IPv4 protocol or IPv6 next header packet to be dropped if a VLAN entry is not found and the protocol or next header does not match the ALE_NXT_HDR register values.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 19    | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 18:16 | TRK_BASE       | R/W  | 0h    | Trunk Base - This field is the hash formula starting value. Changing this value will cause the packet distribution on trunk ports to be changed. If all the trk_en_dst, trk_en_src, trk_en_pri and trk_en_vlan are '0', this value is used as the distribution index. That is a '0' will select the 1st bit of an 'N' link trunk, a '1' will select the second, etc. Below is the distribution across the trunk links. The first number in the italic sequence indicates the traffic is sent to the lowest numbered port of a trunk group. For example if you have a 3 port trunk, the hash result 0 will go to the base port (0), hash result 1 will go to the highest port of the trunk group (2), hash result 2 will go to the middle port (1), etc.<br>1 - 00000000<br>2 - 01010101<br>3 - 02102102<br>4 - 03210321 |
| 15    | MULTIHOST      | R/W  | 0h    | The ~multihost allows host traffic to be sent back to the host if the DA is market for the host port.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 14:9  | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 8:0   | MIRROR_MIDX    | R/W  | 0h    | Mirror Index - This field is the ALE lookup table entry index that when a match occurs will cause this traffic to be mirrored to the mirror_top port. That is any VLAN, ONU or address with or without VLAN can be selected for traffic mirroring.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

### 5.1.2.382 CPSW\_NC\_ALE\_PRESCALE Register

#### 1 CPSW\_NC\_ALE\_PRESCALE Register (Offset = 3E010h) [reset = 0h]

The ALE Prescale Register is used to set the Broadcast and Multicast rate limiting prescaler value.

Return to [Summary Table](#)

**Table 5-1145. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E010h       |

**Figure 5-382. CPSW\_NC\_ALE\_PRESCALE Name Register**

|              |    |    |    |              |    |    |    |
|--------------|----|----|----|--------------|----|----|----|
| 31           | 30 | 29 | 28 | 27           | 26 | 25 | 24 |
| RESERVED     |    |    |    |              |    |    |    |
| NONE         |    |    |    |              |    |    |    |
| 0h           |    |    |    |              |    |    |    |
| 23           | 22 | 21 | 20 | 19           | 18 | 17 | 16 |
| RESERVED     |    |    |    | ALE_PRESCALE |    |    |    |
| NONE         |    |    |    | R/W          |    |    |    |
| 0h           |    |    |    | 0h           |    |    |    |
| 15           | 14 | 13 | 12 | 11           | 10 | 9  | 8  |
| ALE_PRESCALE |    |    |    |              |    |    |    |
| R/W          |    |    |    |              |    |    |    |
| 0h           |    |    |    |              |    |    |    |
| 7            | 6  | 5  | 4  | 3            | 2  | 1  | 0  |
| ALE_PRESCALE |    |    |    |              |    |    |    |
| R/W          |    |    |    |              |    |    |    |
| 0h           |    |    |    |              |    |    |    |

**Table 5-1147. CPSW\_NC\_ALE\_PRESCALE Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                                                                                                 |
|-------|--------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED     | NONE | 0h    | Reserved                                                                                                                                                                                    |
| 19:0  | ALE_PRESCALE | R/W  | 0h    | ALE Prescale - The input clock is divided by this value for use in the multicast/broadcast rate limiters. The minimum operating value is 0x10. The prescaler is off when the value is zero. |

### 5.1.2.383 CPSW\_NC\_ALE\_AGING\_CTRL Register

#### 1 CPSW\_NC\_ALE\_AGING\_CTRL Register (Offset = 3E014h) [reset = 0h]

The ALE Aging Control sets the aging interval which will cause periodic aging to occur. This value specifies the minimum time between aging starts.

Return to [Summary Table](#)

**Table 5-1148. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E014h       |

**Figure 5-383. CPSW\_NC\_ALE\_AGING\_CTRL Name Register**

| 31                 | 30                 | 29       | 28 | 27 | 26 | 25 | 24 |
|--------------------|--------------------|----------|----|----|----|----|----|
| PRESCALE_2_DISABLE | PRESCALE_1_DISABLE | RESERVED |    |    |    |    |    |
| R/W                | R/W                | NONE     |    |    |    |    |    |
| 0h                 | 0h                 | 0h       |    |    |    |    |    |
| 23                 | 22                 | 21       | 20 | 19 | 18 | 17 | 16 |
| ALE_AGING_TIMER    |                    |          |    |    |    |    |    |
| R/W                |                    |          |    |    |    |    |    |
| 0h                 |                    |          |    |    |    |    |    |
| 15                 | 14                 | 13       | 12 | 11 | 10 | 9  | 8  |
| ALE_AGING_TIMER    |                    |          |    |    |    |    |    |
| R/W                |                    |          |    |    |    |    |    |
| 0h                 |                    |          |    |    |    |    |    |
| 7                  | 6                  | 5        | 4  | 3  | 2  | 1  | 0  |
| ALE_AGING_TIMER    |                    |          |    |    |    |    |    |
| R/W                |                    |          |    |    |    |    |    |
| 0h                 |                    |          |    |    |    |    |    |

**Table 5-1150. CPSW\_NC\_ALE\_AGING\_CTRL Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | PRESCALE_2_DISABLE | R/W  | 0h    | ALE Prescaler 2 Disable - When set will divide the aging interval by 1000. This bit is designed for device verification and should not be used in production software. Combination of PreScale1Disable and PreScale2Disable will divide the aging interval by 1,000,000 for test purposes. |
| 30    | PRESCALE_1_DISABLE | R/W  | 0h    | ALE Prescaler 1 Disable - When set will divide the aging interval by 1000. This bit is designed for device verification and should not be used in production software. Combination of PreScale1Disable and PreScale2Disable will divide the aging interval by 1,000,000 for test purposes. |
| 29:24 | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                   |
| 23:0  | ALE_AGING_TIMER    | R/W  | 0h    | ALE Aging Timer - This field specifies the number of clock cycles times 1,000,000 between aging operations.                                                                                                                                                                                |

### 5.1.2.384 CPSW\_NC\_ALE\_NXT\_HDR Register

#### 1 CPSW\_NC\_ALE\_NXT\_HDR Register (Offset = 3E01Ch) [reset = 0h]

The ALE Next Header is used to limit the IPv6 Next header or IPv4 Protocol values found in the IP header. It is enabled via the ~iLmtNxtHdr bit in the VLAN entry. All four ~iip\_nxt\_hdr0-3 are compared when enabled, so if only one is required, set them all to the one value to be tested.

Return to [Summary Table](#)

**Table 5-1151. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E01Ch       |

**Figure 5-384. CPSW\_NC\_ALE\_NXT\_HDR Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| IP_NXT_HDR3 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| IP_NXT_HDR2 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| IP_NXT_HDR1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| IP_NXT_HDR0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-1153. CPSW\_NC\_ALE\_NXT\_HDR Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                  |
|-------|-------------|------|-------|------------------------------------------------------------------------------|
| 31:24 | IP_NXT_HDR3 | R/W  | 0h    | The ip_nxt_hdr3 is the forth protocol or next header compared when enabled.  |
| 23:16 | IP_NXT_HDR2 | R/W  | 0h    | The ip_nxt_hdr2 is the third protocol or next header compared when enabled.  |
| 15:8  | IP_NXT_HDR1 | R/W  | 0h    | The ip_nxt_hdr1 is the second protocol or next header compared when enabled. |
| 7:0   | IP_NXT_HDR0 | R/W  | 0h    | The ip_nxt_hdr0 is the first protocol or next header compared when enabled.  |

### 5.1.2.385 CPSW\_NC\_ALE\_TBLCTL Register

#### 1 CPSW\_NC\_ALE\_TBLCTL Register (Offset = 3E020h) [reset = 0h]

The ALE table control register is used to read or write that ALE table entries. After writing to this register any read or write to any ALE register will be stalled until the read or write operation completes.

Return to [Summary Table](#)

**Table 5-1154. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E020h       |

**Figure 5-385. CPSW\_NC\_ALE\_TBLCTL Name Register**

|          |          |    |    |    |    |    |          |
|----------|----------|----|----|----|----|----|----------|
| 31       | 30       | 29 | 28 | 27 | 26 | 25 | 24       |
| TABLEWR  | RESERVED |    |    |    |    |    |          |
| R/W      | NONE     |    |    |    |    |    |          |
| 0h       | 0h       |    |    |    |    |    |          |
| 23       | 22       | 21 | 20 | 19 | 18 | 17 | 16       |
| RESERVED |          |    |    |    |    |    |          |
| NONE     |          |    |    |    |    |    |          |
| 0h       |          |    |    |    |    |    |          |
| 15       | 14       | 13 | 12 | 11 | 10 | 9  | 8        |
| RESERVED |          |    |    |    |    |    | TABLEIDX |
| NONE     |          |    |    |    |    |    | R/W      |
| 0h       |          |    |    |    |    |    | 0h       |
| 7        | 6        | 5  | 4  | 3  | 2  | 1  | 0        |
| TABLEIDX |          |    |    |    |    |    |          |
| R/W      |          |    |    |    |    |    |          |
| 0h       |          |    |    |    |    |    |          |

**Table 5-1156. CPSW\_NC\_ALE\_TBLCTL Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                            |
|------|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31   | TABLEWR  | R/W  | 0h    | Table Write - This bit is used to write the table words to the lookup table.<br>0 - Table Read Operation is performed. The contents of the TABLEIDX entry will be read into the ALE_TBLWx registers<br>1 - Table write operation is performed. This will take the current contents from the ALE_TBLWx registers and write them to the table at the specified TABLEIDX. |
| 30:9 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                               |
| 8:0  | TABLEIDX | R/W  | 0h    | The table index is used to determine which lookup table entry is read or written.                                                                                                                                                                                                                                                                                      |

### 5.1.2.386 CPSW\_NC\_ALE\_TBLW2 Register

#### 1 CPSW\_NC\_ALE\_TBLW2 Register (Offset = 3E034h) [reset = 0h]

The ALE Table Word 2 is the most significant word of an ALE table entry.

Return to [Summary Table](#)

**Table 5-1157. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E034h       |

**Figure 5-386. CPSW\_NC\_ALE\_TBLW2 Name Register**

|          |           |    |    |    |    |    |    |
|----------|-----------|----|----|----|----|----|----|
| 31       | 30        | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |           |    |    |    |    |    |    |
| NONE     |           |    |    |    |    |    |    |
| 0h       |           |    |    |    |    |    |    |
| 23       | 22        | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |           |    |    |    |    |    |    |
| NONE     |           |    |    |    |    |    |    |
| 0h       |           |    |    |    |    |    |    |
| 15       | 14        | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |           |    |    |    |    |    |    |
| NONE     |           |    |    |    |    |    |    |
| 0h       |           |    |    |    |    |    |    |
| 7        | 6         | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED | TABLEWRD2 |    |    |    |    |    |    |
| NONE     | R/W       |    |    |    |    |    |    |
| 0h       | 0h        |    |    |    |    |    |    |

**Table 5-1159. CPSW\_NC\_ALE\_TBLW2 Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description              |
|------|-----------|------|-------|--------------------------|
| 31:7 | RESERVED  | NONE | 0h    | Reserved                 |
| 6:0  | TABLEWRD2 | R/W  | 0h    | Table Entry bits [71:64] |



### 5.1.2.387 CPSW\_NC\_ALE\_TBLW1 Register

#### 1 CPSW\_NC\_ALE\_TBLW1 Register (Offset = 3E038h) [reset = 0h]

The ALE Table Word 1 is the middle word of an ALE table entry.

Return to [Summary Table](#)

**Table 5-1160. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E038h       |

**Figure 5-387. CPSW\_NC\_ALE\_TBLW1 Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TABLEWRD1 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TABLEWRD1 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TABLEWRD1 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TABLEWRD1 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 5-1162. CPSW\_NC\_ALE\_TBLW1 Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description              |
|------|-----------|------|-------|--------------------------|
| 31:0 | TABLEWRD1 | R/W  | 0h    | Table Entry bits [63:32] |

### 5.1.2.388 CPSW\_NC\_ALE\_TBLW0 Register

#### 1 CPSW\_NC\_ALE\_TBLW0 Register (Offset = 3E03Ch) [reset = 0h]

The ALE Table Word 0 is the least significant word of an ALE table entry.

Return to [Summary Table](#)

**Table 5-1163. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E03Ch       |

**Figure 5-388. CPSW\_NC\_ALE\_TBLW0 Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TABLEWRD0 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TABLEWRD0 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TABLEWRD0 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TABLEWRD0 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 5-1165. CPSW\_NC\_ALE\_TBLW0 Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description             |
|------|-----------|------|-------|-------------------------|
| 31:0 | TABLEWRD0 | R/W  | 0h    | Table Entry bits [31:0] |

### 5.1.2.389 CPSW\_NC\_ALE\_I0\_PORTCTL0 Register

#### 1 CPSW\_NC\_ALE\_I0\_PORTCTL0 Register (Offset = 3E040h) [reset = 0h]

The ALE Port Control Register sets the port specific modes of operation.

Return to [Summary Table](#)

**Table 5-1166. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E040h       |

**Figure 5-389. CPSW\_NC\_ALE\_I0\_PORTCTL0 Name Register**

| 31                             | 30                       | 29                         | 28                            | 27                                  | 26                             | 25                  | 24 |
|--------------------------------|--------------------------|----------------------------|-------------------------------|-------------------------------------|--------------------------------|---------------------|----|
| I0_REG_P0_BCAST_LIMIT          |                          |                            |                               |                                     |                                |                     |    |
| R/W                            |                          |                            |                               |                                     |                                |                     |    |
| 0h                             |                          |                            |                               |                                     |                                |                     |    |
| 23                             | 22                       | 21                         | 20                            | 19                                  | 18                             | 17                  | 16 |
| I0_REG_P0_MCAST_LIMIT          |                          |                            |                               |                                     |                                |                     |    |
| R/W                            |                          |                            |                               |                                     |                                |                     |    |
| 0h                             |                          |                            |                               |                                     |                                |                     |    |
| 15                             | 14                       | 13                         | 12                            | 11                                  | 10                             | 9                   | 8  |
| I0_REG_P0_DROP_DOUBLE_VLAN     | I0_REG_P0_DROP_DUAL_VLAN | I0_REG_P0_MCAST_ONLY_CAF   | I0_REG_P0_DROP_PACKET_AUTHMOD | I0_REG_P0_MCAST_ONLY                | I0_REG_P0_DROP_PACKET_UNK      | I0_REG_P0_TRUNKNUM  |    |
| R/W                            | R/W                      | R/W                        | R/W                           | R/W                                 | R/W                            | R/W                 |    |
| 0h                             | 0h                       | 0h                         | 0h                            | 0h                                  | 0h                             | 0h                  |    |
| 7                              | 6                        | 5                          | 4                             | 3                                   | 2                              | 1                   | 0  |
| I0_REG_P0_DROP_PACKET_ERROR_SP | RESERVED                 | I0_REG_P0_N_DROP_SA_UPDATE | I0_REG_P0_N_DROP_O_LEARN      | I0_REG_P0_DROP_PACKET_INGRESS_CHECK | I0_REG_P0_DROP_PACKET_UNTAGGED | I0_REG_P0_PORTSTATE |    |
| R/W                            | NONE                     | R/W                        | R/W                           | R/W                                 | R/W                            | R/W                 |    |
| 0h                             | 0h                       | 0h                         | 0h                            | 0h                                  | 0h                             | 0h                  |    |

**Table 5-1168. CPSW\_NC\_ALE\_I0\_PORTCTL0 Register Field Descriptions**

| Bit   | Field                      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|----------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | I0_REG_P0_BCAST_LIMIT      | R/W  | 0h    | Broadcast Packet Rate Limit - Each prescale pulse loads this field into the port broadcast rate limit counter. The port counters are decremented with each packet received or transmitted depending on whether the mode is transmit or receive. If the counters decrement to zero, then further packets are rate limited until the next prescale pulse.<br>Broadcast rate limiting is enabled by a non-zero value in this field.                                                                                                  |
| 23:16 | I0_REG_P0_MCAST_LIMIT      | R/W  | 0h    | Multicast Packet Rate Limit - Each prescale pulse loads this field into the port multicast rate limit counter. The port counters are decremented with each packet received or transmitted depending on whether the mode is transmit or receive. If the counters decrement to zero, then further packets are rate limited until the next prescale pulse.<br>Multicast rate limiting is enabled by a non-zero value in this field. The mcast_limit is the number of Multicast packets that will be forwarded per ale_prescale time. |
| 15    | I0_REG_P0_DROP_DOUBLE_VLAN | R/W  | 0h    | Drop Double VLAN - When set cause any received packet with double VLANs to be dropped. That is if there are two ctag or two stag fields in the packet it will be dropped.                                                                                                                                                                                                                                                                                                                                                         |
| 14    | I0_REG_P0_DROP_DUAL_VLAN   | R/W  | 0h    | Drop Dual VLAN - When set will cause any received packet with dual VLAN stag followed by ctag to be dropped.                                                                                                                                                                                                                                                                                                                                                                                                                      |

**Table 5-1168. CPSW\_NC\_ALE\_I0\_PORTCTL0 Register Field Descriptions (continued)**

| Bit | Field                       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-----|-----------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 13  | I0_REG_P0_MACONLY_CAF       | R/W  | 0h    | Mac Only Copy All Frames - When set a Mac Only port will transfer all received good frames to the host. When clear a Mac Only port will transfer packets to the host based on ALE destination address lookup operation (which operates more like an Ethernet Mac). A Mac Only port is a port with maonly set.                                                                                                                                                                                                                                                                           |
| 12  | I0_REG_P0_DIS_PAUTH_MOD     | R/W  | 0h    | Disable Port authorization - When set will allow unknown addresses to arrive on a switch in authorization mode. It is intended for device to device network connection on ports which do not require MACSEC encryption.                                                                                                                                                                                                                                                                                                                                                                 |
| 11  | I0_REG_P0_MACONLY           | R/W  | 0h    | MAC Only - When set enables this port be treated like a MAC port for the host. All traffic received is only sent to the host. The host must direct traffic to this port as the lookup engine will not send traffic to the ports with the p0_maonly bit set and the p0_no_learn also set. If p0_maonly bit is set and the p0_no_learn is not set, the host can send non-directed packets that can be sent to the destination of a MacOnly port. It is also possible that The host can broadcast to all ports including MacOnly ports in this mode.                                       |
| 10  | I0_REG_P0_TRUNKEN           | R/W  | 0h    | Trunk Enable - This field is used to enable a port into a trunk. Any port can be used as a trunk port, any two or more ports with the p0_trunken its set and having the same p0_trunknum will be placed in the same trunk. There is no requirement for trunk ports to be adjacent. If all ports are enabled in the same trunk, no traffic can flow as traffic received within a trunk is never trasnmitted out the same trunk. If only a single port is a member of a trunk, it looks like a normal port with exception of entries in the look up table will be noted as a trunk entry. |
| 9:8 | I0_REG_P0_TRUNKNUM          | R/W  | 0h    | Trunk Number - This field is used as the trunk number when the p0_trunken is also set. Ports with the same trunk number that have the p0_trunken also set will have traffic distributed within the trunk based on the result of the hash function described above.                                                                                                                                                                                                                                                                                                                      |
| 7   | I0_REG_P0_MIRROR_SP         | R/W  | 0h    | Mirror Source Port - This field enables the source port mirror option. When this bit is set any traffic received on the port with the reg_p0_mirror_sp bit set will have its received traffic also sent to the mirror_top port.                                                                                                                                                                                                                                                                                                                                                         |
| 6   | RESERVED                    | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 5   | I0_REG_P0_NO_SA_UP_DATE     | R/W  | 0h    | No Source Address Update - When set will not update the source addresses for this port.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 4   | I0_REG_P0_NO_LEARN          | R/W  | 0h    | No Learn - When set will not learn the source addresses for this port.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 3   | I0_REG_P0_VID_INGRESS_CHECK | R/W  | 0h    | VLAN Ingress Check - When set if a packet received is not a member of the VLAN, the packet will be dropped.                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 2   | I0_REG_P0_DROP_UNTAGGED     | R/W  | 0h    | If Drop Untagged - When set will drop packets without a VLAN tag.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 1:0 | I0_REG_P0_PORTSTATE         | R/W  | 0h    | Port State - Defines the current port state used for lookup operations.<br>0 - Disabled<br>1 - Blocked<br>2 - Learning<br>3 - Forwarding                                                                                                                                                                                                                                                                                                                                                                                                                                                |

### 5.1.2.390 CPSW\_NC\_ALE\_UVLAN\_MEMBER Register

#### 1 CPSW\_NC\_ALE\_UVLAN\_MEMBER Register (Offset = 3E090h) [reset = 0h]

The ALE Unknown VLAN Member Mask Register is used to specify the member list for unknown VLAN ID.

Return to [Summary Table](#)

**Table 5-1169. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E090h       |

**Figure 5-390. CPSW\_NC\_ALE\_UVLAN\_MEMBER Name Register**

|          |    |    |    |    |                   |    |    |
|----------|----|----|----|----|-------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                | 25 | 24 |
| RESERVED |    |    |    |    |                   |    |    |
| NONE     |    |    |    |    |                   |    |    |
| 0h       |    |    |    |    |                   |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                | 17 | 16 |
| RESERVED |    |    |    |    |                   |    |    |
| NONE     |    |    |    |    |                   |    |    |
| 0h       |    |    |    |    |                   |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                | 9  | 8  |
| RESERVED |    |    |    |    |                   |    |    |
| NONE     |    |    |    |    |                   |    |    |
| 0h       |    |    |    |    |                   |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                 | 1  | 0  |
| RESERVED |    |    |    |    | UVLAN_MEMBER_LIST |    |    |
| NONE     |    |    |    |    | R/W               |    |    |
| 0h       |    |    |    |    | 0h                |    |    |

**Table 5-1171. CPSW\_NC\_ALE\_UVLAN\_MEMBER Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                                                                              |
|------|-------------------|------|-------|------------------------------------------------------------------------------------------|
| 31:3 | RESERVED          | NONE | 0h    | Reserved                                                                                 |
| 2:0  | UVLAN_MEMBER_LIST | R/W  | 0h    | Unknown VLAN Member List - Each bit represents the port member status for unknown VLANs. |

### 5.1.2.391 CPSW\_NC\_ALE\_UVLAN\_URCAST Register

#### 1 CPSW\_NC\_ALE\_UVLAN\_URCAST Register (Offset = 3E094h) [reset = 0h]

The ALE Unknown VLAN Unregistered Multicast Flood Mask Register is used to specify which egress ports unregistered multicast addresses egress for the unregistered VLAN ID.

Return to [Summary Table](#)

**Table 5-1172. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E094h       |

**Figure 5-391. CPSW\_NC\_ALE\_UVLAN\_URCAST Name Register**

|          |    |    |    |    |                              |    |    |
|----------|----|----|----|----|------------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                           | 25 | 24 |
| RESERVED |    |    |    |    |                              |    |    |
| NONE     |    |    |    |    |                              |    |    |
| 0h       |    |    |    |    |                              |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                           | 17 | 16 |
| RESERVED |    |    |    |    |                              |    |    |
| NONE     |    |    |    |    |                              |    |    |
| 0h       |    |    |    |    |                              |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                           | 9  | 8  |
| RESERVED |    |    |    |    |                              |    |    |
| NONE     |    |    |    |    |                              |    |    |
| 0h       |    |    |    |    |                              |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                            | 1  | 0  |
| RESERVED |    |    |    |    | UVLAN_UNREG_MCAST_FLOOD_MASK |    |    |
| NONE     |    |    |    |    | R/W                          |    |    |
| 0h       |    |    |    |    | 0h                           |    |    |

**Table 5-1174. CPSW\_NC\_ALE\_UVLAN\_URCAST Register Field Descriptions**

| Bit  | Field                        | Type | Reset | Description                                                                                                                                  |
|------|------------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                     | NONE | 0h    | Reserved                                                                                                                                     |
| 2:0  | UVLAN_UNREG_MCAST_FLOOD_MASK | R/W  | 0h    | Unknown VLAN Unregister Multicast Flood Mask - Each bit represents the port to which unregistered multicast are sent for unregistered VLANs. |

### 5.1.2.392 CPSW\_NC\_ALE\_UVLAN\_RMCAST Register

#### 1 CPSW\_NC\_ALE\_UVLAN\_RMCAST Register (Offset = 3E098h) [reset = 0h]

The ALE Unknown VLAN Registered Multicast Flood Mask Register is used to specify which egress ports registered multicast addresses egress for the unregistered VLAN ID.

Return to [Summary Table](#)

**Table 5-1175. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E098h       |

**Figure 5-392. CPSW\_NC\_ALE\_UVLAN\_RMCAST Name Register**

|          |    |    |    |    |                            |    |    |
|----------|----|----|----|----|----------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                         | 25 | 24 |
| RESERVED |    |    |    |    |                            |    |    |
| NONE     |    |    |    |    |                            |    |    |
| 0h       |    |    |    |    |                            |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                         | 17 | 16 |
| RESERVED |    |    |    |    |                            |    |    |
| NONE     |    |    |    |    |                            |    |    |
| 0h       |    |    |    |    |                            |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                         | 9  | 8  |
| RESERVED |    |    |    |    |                            |    |    |
| NONE     |    |    |    |    |                            |    |    |
| 0h       |    |    |    |    |                            |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                          | 1  | 0  |
| RESERVED |    |    |    |    | UVLAN_REG_MCAST_FLOOD_MASK |    |    |
| NONE     |    |    |    |    | R/W                        |    |    |
| 0h       |    |    |    |    | 0h                         |    |    |

**Table 5-1177. CPSW\_NC\_ALE\_UVLAN\_RMCAST Register Field Descriptions**

| Bit  | Field                      | Type | Reset | Description                                                                                                                                                                                                                                           |
|------|----------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                   | NONE | 0h    | Reserved                                                                                                                                                                                                                                              |
| 2:0  | UVLAN_REG_MCAST_FLOOD_MASK | R/W  | 0h    | Unknown VLAN Register Multicast Flood Mask - Each bit represents the port to which registered multicast are sent for unregistered VLANs. This field is ANDed with the registered multicast mask to determine the destinations for unregistered VLANs. |

### 5.1.2.393 CPSW\_NC\_ALE\_UVLAN\_UNTAG Register

#### 1 CPSW\_NC\_ALE\_UVLAN\_UNTAG Register (Offset = 3E09Ch) [reset = 0h]

The ALE Unknown VLAN force Untagged Egress Mask Register is used to specify which egress ports the VLAN ID will be removed.

Return to [Summary Table](#)

**Table 5-1178. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E09Ch       |

**Figure 5-393. CPSW\_NC\_ALE\_UVLAN\_UNTAG Name Register**

|          |    |    |    |    |                             |    |    |
|----------|----|----|----|----|-----------------------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26                          | 25 | 24 |
| RESERVED |    |    |    |    |                             |    |    |
| NONE     |    |    |    |    |                             |    |    |
| 0h       |    |    |    |    |                             |    |    |
| 23       | 22 | 21 | 20 | 19 | 18                          | 17 | 16 |
| RESERVED |    |    |    |    |                             |    |    |
| NONE     |    |    |    |    |                             |    |    |
| 0h       |    |    |    |    |                             |    |    |
| 15       | 14 | 13 | 12 | 11 | 10                          | 9  | 8  |
| RESERVED |    |    |    |    |                             |    |    |
| NONE     |    |    |    |    |                             |    |    |
| 0h       |    |    |    |    |                             |    |    |
| 7        | 6  | 5  | 4  | 3  | 2                           | 1  | 0  |
| RESERVED |    |    |    |    | UVLAN_FORCE_UNTAGGED_EGRESS |    |    |
| NONE     |    |    |    |    | R/W                         |    |    |
| 0h       |    |    |    |    | 0h                          |    |    |

**Table 5-1180. CPSW\_NC\_ALE\_UVLAN\_UNTAG Register Field Descriptions**

| Bit  | Field                       | Type | Reset | Description                                                                                                                   |
|------|-----------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED                    | NONE | 0h    | Reserved                                                                                                                      |
| 2:0  | UVLAN_FORCE_UNTAGGED_EGRESS | R/W  | 0h    | Unknown VLAN Force Untagged Egress Mask - Each bit represents the port where the VLAN will be removed for unregistered VLANs. |



### 5.1.2.394 CPSW\_NC\_ALE\_FAST\_LUT Register

#### 1 CPSW\_NC\_ALE\_FAST\_LUT Register (Offset = 3E0B4h) [reset = 0h]

The Fast LUT registers allows the ports to be placed in Fast LUT mode.

Return to [Summary Table](#)

**Table 5-1181. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E0B4h       |

**Figure 5-394. CPSW\_NC\_ALE\_FAST\_LUT Name Register**

|          |    |    |    |    |          |    |    |
|----------|----|----|----|----|----------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26       | 25 | 24 |
| RESERVED |    |    |    |    |          |    |    |
| NONE     |    |    |    |    |          |    |    |
| 0h       |    |    |    |    |          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18       | 17 | 16 |
| RESERVED |    |    |    |    |          |    |    |
| NONE     |    |    |    |    |          |    |    |
| 0h       |    |    |    |    |          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10       | 9  | 8  |
| RESERVED |    |    |    |    |          |    |    |
| NONE     |    |    |    |    |          |    |    |
| 0h       |    |    |    |    |          |    |    |
| 7        | 6  | 5  | 4  | 3  | 2        | 1  | 0  |
| RESERVED |    |    |    |    | FAST_LUT |    |    |
| NONE     |    |    |    |    | R/W      |    |    |
| 0h       |    |    |    |    | 0h       |    |    |

**Table 5-1183. CPSW\_NC\_ALE\_FAST\_LUT Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                     |
|------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                        |
| 2:0  | FAST_LUT | R/W  | 0h    | The ~Fast_LUT field allows any port to be Fast_LUT mode, which will cause all lookup operations to start based on DA/SA and VLAN only. That is any data beyond the first 32 are not used in the lookup process. |

### 5.1.2.395 CPSW\_NC\_ALE\_STAT\_DIAG Register

#### 1 CPSW\_NC\_ALE\_STAT\_DIAG Register (Offset = 3E0B8h) [reset = 0h]

The ALE Statistic Output Diagnostic Register allows the output statistics to diagnose the SW counters. This register is for diagnostic only.

Return to [Summary Table](#)

**Table 5-1184. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E0B8h       |

**Figure 5-395. CPSW\_NC\_ALE\_STAT\_DIAG Name Register**

|             |          |    |    |           |    |           |    |
|-------------|----------|----|----|-----------|----|-----------|----|
| 31          | 30       | 29 | 28 | 27        | 26 | 25        | 24 |
| RESERVED    |          |    |    |           |    |           |    |
| NONE        |          |    |    |           |    |           |    |
| 0h          |          |    |    |           |    |           |    |
| 23          | 22       | 21 | 20 | 19        | 18 | 17        | 16 |
| RESERVED    |          |    |    |           |    |           |    |
| NONE        |          |    |    |           |    |           |    |
| 0h          |          |    |    |           |    |           |    |
| 15          | 14       | 13 | 12 | 11        | 10 | 9         | 8  |
| PBCAST_DIAG | RESERVED |    |    |           |    | PORT_DIAG |    |
| R/W         | NONE     |    |    |           |    | R/W       |    |
| 0h          | 0h       |    |    |           |    | 0h        |    |
| 7           | 6        | 5  | 4  | 3         | 2  | 1         | 0  |
| RESERVED    |          |    |    | STAT_DIAG |    |           |    |
| NONE        |          |    |    | R/W       |    |           |    |
| 0h          |          |    |    | 0h        |    |           |    |

**Table 5-1186. CPSW\_NC\_ALE\_STAT\_DIAG Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                |
|-------|-------------|------|-------|------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED    | NONE | 0h    | Reserved                                                                                                   |
| 15    | PBCAST_DIAG | R/W  | 0h    | When set and the port_diag is set to zero, will allow all ports to see the same stat diagnostic increment. |
| 14:10 | RESERVED    | NONE | 0h    | Reserved                                                                                                   |
| 9:8   | PORT_DIAG   | R/W  | 0h    | The port selected that a received packet will cause the selected error to increment                        |
| 7:4   | RESERVED    | NONE | 0h    | Reserved                                                                                                   |

**Table 5-1186. CPSW\_NC\_ALE\_STAT\_DIAG Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-----|-----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0 | STAT_DIAG | R/W  | 0h    | <p>When non-zero will cause the selected statistic to increment on the next frame received. For the selected Port.</p> <p>0: Disabled</p> <p>1: Destination Equal Source Drop Stat will count</p> <p>2: VLAN Ingress Check Drop Stat will count</p> <p>3: Source Multicast Drop Stat will count</p> <p>4: Dual VLAN Drop Stat will count</p> <p>5: Ether Type length error Drop Stat will count</p> <p>6: Next Hop Limit Drop Stat will count</p> <p>7: IPv4 Fragment Drop Stat will count</p> <p>8: Classifier Hit Stat will count</p> <p>9: Classifier Red Drop Stat will count</p> <p>10: Classifier Yellow Drop Stat will count</p> <p>11: ALE Overflow Drop Stat will count</p> <p>12: Rate Limit Drop Stat will count</p> <p>13: Blocked Address Drop Stat will count</p> <p>14: Secure Address Drop Stat will count</p> <p>15: Authorization Drop Stat will count.</p> |

### 5.1.2.396 CPSW\_NC\_ALE\_OAM\_LB\_CTRL Register

#### 1 CPSW\_NC\_ALE\_OAM\_LB\_CTRL Register (Offset = 3E0BCh) [reset = 0h]

The ALE OAM Control allows ports to be put into OAM Loopback, only non-supervisor packet are looped back to the source port.

Return to [Summary Table](#)

**Table 5-1187. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E0BCh       |

**Figure 5-396. CPSW\_NC\_ALE\_OAM\_LB\_CTRL Name Register**

|          |    |    |    |    |             |    |    |
|----------|----|----|----|----|-------------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26          | 25 | 24 |
| RESERVED |    |    |    |    |             |    |    |
| NONE     |    |    |    |    |             |    |    |
| 0h       |    |    |    |    |             |    |    |
| 23       | 22 | 21 | 20 | 19 | 18          | 17 | 16 |
| RESERVED |    |    |    |    |             |    |    |
| NONE     |    |    |    |    |             |    |    |
| 0h       |    |    |    |    |             |    |    |
| 15       | 14 | 13 | 12 | 11 | 10          | 9  | 8  |
| RESERVED |    |    |    |    |             |    |    |
| NONE     |    |    |    |    |             |    |    |
| 0h       |    |    |    |    |             |    |    |
| 7        | 6  | 5  | 4  | 3  | 2           | 1  | 0  |
| RESERVED |    |    |    |    | OAM_LB_CTRL |    |    |
| NONE     |    |    |    |    | R/W         |    |    |
| 0h       |    |    |    |    | 0h          |    |    |

**Table 5-1189. CPSW\_NC\_ALE\_OAM\_LB\_CTRL Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                     |
|------|-------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED    | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                        |
| 2:0  | OAM_LB_CTRL | R/W  | 0h    | The oam_lb_ctrl allows any port to be put into OAM loopback, that is any packet received will be returned to the same port with an egressop of 0xFF which swaps the source and destination address. BPDUs will still flow through as normal so that OAM can be remotely requested and disabled. |

### 5.1.2.397 CPSW\_NC\_ALE\_EGRESSOP Register

#### 1 CPSW\_NC\_ALE\_EGRESSOP Register (Offset = 3E0FCh) [reset = 0h]

The Egress Operation register allows enabled classifiers with any match like IPSA or IPDA match to use the CPSW Egress Packet Operations Inter VLAN Routing sub functions. If the packet was destined for the host or is destined to any port without any errors, but matches a classifier that has a programmed egress opcode, it will be forwarded to the destination ports where the destination ports will use the thier egress opcode entry to modify the packet. InterVLAN Routing and mirroring need to be understood, they are orthogonal functions. Care must be taken not to violate VLAN rules as this can redirect packets based on classifier matches.

Return to [Summary Table](#)

**Table 5-1190. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E0FCh       |

**Figure 5-397. CPSW\_NC\_ALE\_EGRESSOP Name Register**

|            |    |    |           |          |            |    |    |
|------------|----|----|-----------|----------|------------|----|----|
| 31         | 30 | 29 | 28        | 27       | 26         | 25 | 24 |
| EGRESS_OP  |    |    |           |          |            |    |    |
| R/W        |    |    |           |          |            |    |    |
| 0h         |    |    |           |          |            |    |    |
| 23         | 22 | 21 | 20        | 19       | 18         | 17 | 16 |
| EGRESS_TRK |    |    | TTL_CHECK | RESERVED |            |    |    |
| R/W        |    |    | R/W       | NONE     |            |    |    |
| 0h         |    |    | 0h        | 0h       |            |    |    |
| 15         | 14 | 13 | 12        | 11       | 10         | 9  | 8  |
| RESERVED   |    |    |           |          |            |    |    |
| NONE       |    |    |           |          |            |    |    |
| 0h         |    |    |           |          |            |    |    |
| 7          | 6  | 5  | 4         | 3        | 2          | 1  | 0  |
| RESERVED   |    |    |           |          | DEST_PORTS |    |    |
| NONE       |    |    |           |          | R/W        |    |    |
| 0h         |    |    |           |          | 0h         |    |    |

**Table 5-1192. CPSW\_NC\_ALE\_EGRESSOP Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                             |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | EGRESS_OP  | R/W  | 0h    | The Egress Operation defines the operation performed by the CPSW Egress Packet Operations<br>0: NOP<br>: 1-n: Defines which egress Operation will be performed. This allows Inter VLAN routing to be configured for high bandwidth traffic, reducing CPU load.<br>0xff: Swap SA and DA of packet, this is intended to allow OAM diagnostics for a link. |
| 23:21 | EGRESS_TRK | R/W  | 0h    | The Egress Trunk Index is the calculated trunk index from the SA, DA or VLAN if modified to that InterVLAN routing will work on trunks as well. The DA, SA and VLAN are ignored for trunk generation on InterVLAN Routing so that this field is the index generated from the Egress Op replacements elclusive or'd together into a three bit index.     |
| 20    | TTL_CHECK  | R/W  | 0h    | The TTL Check will cause any packet that fails TTL checks to not be routed to the Inter VLAN Routing sub functions. The packet will be routed to the host it was destined to.                                                                                                                                                                           |
| 19:3  | RESERVED   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                |

**Table 5-1192. CPSW\_NC\_ALE\_EGRESSOP Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                                   |
|-----|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0 | DEST_PORTS | R/W  | 0h    | The Destination Ports is a list of the ports the classified packet will be set to. If a destination is a Trunk, all the port bits for that trunk must be set. |

### 5.1.2.398 CPSW\_NC\_ALE\_POLICECFG0 Register

#### 1 CPSW\_NC\_ALE\_POLICECFG0 Register (Offset = 3E100h) [reset = 0h]

The Policing Config 0 holds the port, frame priority and ONU address index as well as match enables for port, frame priority and ONU address matching.

Return to [Summary Table](#)

**Table 5-1193. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E100h       |

**Figure 5-398. CPSW\_NC\_ALE\_POLICECFG0 Name Register**

|           |          |          |    |         |          |    |           |
|-----------|----------|----------|----|---------|----------|----|-----------|
| 31        | 30       | 29       | 28 | 27      | 26       | 25 | 24        |
| PORT_MEN  | TRUNKID  | RESERVED |    |         | PORT_NUM |    | RESERVED  |
| R/W       | R/W      | NONE     |    |         | R/W      |    | NONE      |
| 0h        | 0h       | 0h       |    |         | 0h       |    | 0h        |
| 23        | 22       | 21       | 20 | 19      | 18       | 17 | 16        |
| RESERVED  |          |          |    | PRI_MEN | PRI_VAL  |    |           |
| NONE      |          |          |    | R/W     | R/W      |    |           |
| 0h        |          |          |    | 0h      | 0h       |    |           |
| 15        | 14       | 13       | 12 | 11      | 10       | 9  | 8         |
| ONU_MEN   | RESERVED |          |    |         |          |    | ONU_INDEX |
| R/W       | NONE     |          |    |         |          |    | R/W       |
| 0h        | 0h       |          |    |         |          |    | 0h        |
| 7         | 6        | 5        | 4  | 3       | 2        | 1  | 0         |
| ONU_INDEX |          |          |    |         |          |    |           |
| R/W       |          |          |    |         |          |    |           |
| 0h        |          |          |    |         |          |    |           |

**Table 5-1195. CPSW\_NC\_ALE\_POLICECFG0 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                  |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------|
| 31    | PORT_MEN  | R/W  | 0h    | Port Match Enable - Enabled port match for the selected policing/classifier entry                                            |
| 30    | TRUNKID   | R/W  | 0h    | Trunk ID - When set indicates the port number is a trunk group.                                                              |
| 29:27 | RESERVED  | NONE | 0h    | Reserved                                                                                                                     |
| 26:25 | PORT_NUM  | R/W  | 0h    | Port Number - Specifies the port address to match for the selected policing/classifier entry                                 |
| 24:20 | RESERVED  | NONE | 0h    | Reserved                                                                                                                     |
| 19    | PRI_MEN   | R/W  | 0h    | Priority Match Enable - Enables frame priority match for the selected policing/classifier entry                              |
| 18:16 | PRI_VAL   | R/W  | 0h    | Priority Value - Specifies the frame priority to match for the selected policing/classifier entry                            |
| 15    | ONU_MEN   | R/W  | 0h    | OUI Match Enable - Enables frame ONU address match for the selected policing/classifier entry                                |
| 14:9  | RESERVED  | NONE | 0h    | Reserved                                                                                                                     |
| 8:0   | ONU_INDEX | R/W  | 0h    | OUI Table Entry Index - Specifies the ALE ONU address lookup table index to match for the selected policing/classifier entry |

### 5.1.2.399 CPSW\_NC\_ALE\_POLICECFG1 Register

#### 1 CPSW\_NC\_ALE\_POLICECFG1 Register (Offset = 3E104h) [reset = 0h]

The Policing Config 1 holds the match enable/match index for the L2 Destination and L2 source addresses

Return to [Summary Table](#)

**Table 5-1196. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E104h       |

**Figure 5-399. CPSW\_NC\_ALE\_POLICECFG1 Name Register**

|           |          |    |    |    |    |    |           |
|-----------|----------|----|----|----|----|----|-----------|
| 31        | 30       | 29 | 28 | 27 | 26 | 25 | 24        |
| DST_MEN   | RESERVED |    |    |    |    |    | DST_INDEX |
| R/W       | NONE     |    |    |    |    |    | R/W       |
| 0h        | 0h       |    |    |    |    |    | 0h        |
| 23        | 22       | 21 | 20 | 19 | 18 | 17 | 16        |
| DST_INDEX |          |    |    |    |    |    |           |
| R/W       |          |    |    |    |    |    |           |
| 0h        |          |    |    |    |    |    |           |
| 15        | 14       | 13 | 12 | 11 | 10 | 9  | 8         |
| SRC_MEN   | RESERVED |    |    |    |    |    | SRC_INDEX |
| R/W       | NONE     |    |    |    |    |    | R/W       |
| 0h        | 0h       |    |    |    |    |    | 0h        |
| 7         | 6        | 5  | 4  | 3  | 2  | 1  | 0         |
| SRC_INDEX |          |    |    |    |    |    |           |
| R/W       |          |    |    |    |    |    |           |
| 0h        |          |    |    |    |    |    |           |

**Table 5-1198. CPSW\_NC\_ALE\_POLICECFG1 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                             |
|-------|-----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | DST_MEN   | R/W  | 0h    | Destination Address Match Enable - Enables frame L2 destination address match for the selected policing/classifier entry                                |
| 30:25 | RESERVED  | NONE | 0h    | Reserved                                                                                                                                                |
| 24:16 | DST_INDEX | R/W  | 0h    | Destination Address Table Entry Index - Specifies the ALE L2 destination address lookup table index to match for the selected policing/classifier entry |
| 15    | SRC_MEN   | R/W  | 0h    | Source Address Match Enable - Enables frame L2 source address match for the selected policing/classifier entry                                          |
| 14:9  | RESERVED  | NONE | 0h    | Reserved                                                                                                                                                |
| 8:0   | SRC_INDEX | R/W  | 0h    | Source Address Table Entry Index - Specifies the ALE L2 source address lookup table index to match for the selected policing/classifier entry           |



### 5.1.2.400 CPSW\_NC\_ALE\_POLICECFG2 Register

#### 1 CPSW\_NC\_ALE\_POLICECFG2 Register (Offset = 3E108h) [reset = 0h]

The Policing Config 2 holds the match enable/match index for the Outer VLAN and Inner VLAN addresses

Return to [Summary Table](#)

**Table 5-1199. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E108h       |

**Figure 5-400. CPSW\_NC\_ALE\_POLICECFG2 Name Register**

|             |          |    |    |    |    |    |             |
|-------------|----------|----|----|----|----|----|-------------|
| 31          | 30       | 29 | 28 | 27 | 26 | 25 | 24          |
| OVLAN_MEN   | RESERVED |    |    |    |    |    | OVLAN_INDEX |
| R/W         | NONE     |    |    |    |    |    | R/W         |
| 0h          | 0h       |    |    |    |    |    | 0h          |
| 23          | 22       | 21 | 20 | 19 | 18 | 17 | 16          |
| OVLAN_INDEX |          |    |    |    |    |    |             |
| R/W         |          |    |    |    |    |    |             |
| 0h          |          |    |    |    |    |    |             |
| 15          | 14       | 13 | 12 | 11 | 10 | 9  | 8           |
| IVLAN_MEN   | RESERVED |    |    |    |    |    | IVLAN_INDEX |
| R/W         | NONE     |    |    |    |    |    | R/W         |
| 0h          | 0h       |    |    |    |    |    | 0h          |
| 7           | 6        | 5  | 4  | 3  | 2  | 1  | 0           |
| IVLAN_INDEX |          |    |    |    |    |    |             |
| R/W         |          |    |    |    |    |    |             |
| 0h          |          |    |    |    |    |    |             |

**Table 5-1201. CPSW\_NC\_ALE\_POLICECFG2 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                |
|-------|-------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | OVLAN_MEN   | R/W  | 0h    | Outer VLAN Match Enable - Enables frame Outer VLAN address match for the selected policing/classifier entry                                |
| 30:25 | RESERVED    | NONE | 0h    | Reserved                                                                                                                                   |
| 24:16 | OVLAN_INDEX | R/W  | 0h    | Outer VLAN Table Entry Index - Specifies the ALE Outer VLAN address lookup table index to match for the selected policing/classifier entry |
| 15    | IVLAN_MEN   | R/W  | 0h    | Inner VLAN Match Enable - Enables frame Inner VLAN address match for the selected policing/classifier entry                                |
| 14:9  | RESERVED    | NONE | 0h    | Reserved                                                                                                                                   |
| 8:0   | IVLAN_INDEX | R/W  | 0h    | Inner VLAN Table Entry Index - Specifies the ALE Inner VLAN address lookup table index to match for the selected policing/classifier entry |

### 5.1.2.401 CPSW\_NC\_ALE\_POLICECFG3 Register

#### 1 CPSW\_NC\_ALE\_POLICECFG3 Register (Offset = 3E10Ch) [reset = 0h]

The Policing Config 3 holds the match enable/match index for the Ether Type and IP Source address

Return to [Summary Table](#)

**Table 5-1202. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E10Ch       |

**Figure 5-401. CPSW\_NC\_ALE\_POLICECFG3 Name Register**

|                 |          |    |    |    |    |    |                 |
|-----------------|----------|----|----|----|----|----|-----------------|
| 31              | 30       | 29 | 28 | 27 | 26 | 25 | 24              |
| ETHERTYPE_MEN   | RESERVED |    |    |    |    |    | ETHERTYPE_INDEX |
| R/W             | NONE     |    |    |    |    |    | R/W             |
| 0h              | 0h       |    |    |    |    |    | 0h              |
| 23              | 22       | 21 | 20 | 19 | 18 | 17 | 16              |
| ETHERTYPE_INDEX |          |    |    |    |    |    |                 |
| R/W             |          |    |    |    |    |    |                 |
| 0h              |          |    |    |    |    |    |                 |
| 15              | 14       | 13 | 12 | 11 | 10 | 9  | 8               |
| IPSRC_MEN       | RESERVED |    |    |    |    |    | IPSRC_INDEX     |
| R/W             | NONE     |    |    |    |    |    | R/W             |
| 0h              | 0h       |    |    |    |    |    | 0h              |
| 7               | 6        | 5  | 4  | 3  | 2  | 1  | 0               |
| IPSRC_INDEX     |          |    |    |    |    |    |                 |
| R/W             |          |    |    |    |    |    |                 |
| 0h              |          |    |    |    |    |    |                 |

**Table 5-1204. CPSW\_NC\_ALE\_POLICECFG3 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                      |
|-------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | ETHERTYPE_MEN   | R/W  | 0h    | EtherType Match Enable - Enables frame Ether Type match for the selected policing/classifier entry                                               |
| 30:25 | RESERVED        | NONE | 0h    | Reserved                                                                                                                                         |
| 24:16 | ETHERTYPE_INDEX | R/W  | 0h    | EtherType Table Entry Index - Specifies the ALE Ether Type lookup table index to match for the selected policing/classifier entry                |
| 15    | IPSRC_MEN       | R/W  | 0h    | IP Source Address Match Enable - Enables frame IP Source address match for the selected policing/classifier entry                                |
| 14:9  | RESERVED        | NONE | 0h    | Reserved                                                                                                                                         |
| 8:0   | IPSRC_INDEX     | R/W  | 0h    | IP Source Address Table Entry Index - Specifies the ALE IP Source address lookup table index to match for the selected policing/classifier entry |

### 5.1.2.402 CPSW\_NC\_ALE\_POLICECFG4 Register

#### 1 CPSW\_NC\_ALE\_POLICECFG4 Register (Offset = 3E110h) [reset = 0h]

The Policing Config 4 holds the match enable/match index for the IP Destination address

Return to [Summary Table](#)

**Table 5-1205. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E110h       |

**Figure 5-402. CPSW\_NC\_ALE\_POLICECFG4 Name Register**

|             |          |    |    |    |    |    |             |
|-------------|----------|----|----|----|----|----|-------------|
| 31          | 30       | 29 | 28 | 27 | 26 | 25 | 24          |
| IPDST_MEN   | RESERVED |    |    |    |    |    | IPDST_INDEX |
| R/W         | NONE     |    |    |    |    |    | R/W         |
| 0h          | 0h       |    |    |    |    |    | 0h          |
| 23          | 22       | 21 | 20 | 19 | 18 | 17 | 16          |
| IPDST_INDEX |          |    |    |    |    |    |             |
| R/W         |          |    |    |    |    |    |             |
| 0h          |          |    |    |    |    |    |             |
| 15          | 14       | 13 | 12 | 11 | 10 | 9  | 8           |
| RESERVED    |          |    |    |    |    |    |             |
| NONE        |          |    |    |    |    |    |             |
| 0h          |          |    |    |    |    |    |             |
| 7           | 6        | 5  | 4  | 3  | 2  | 1  | 0           |
| RESERVED    |          |    |    |    |    |    |             |
| NONE        |          |    |    |    |    |    |             |
| 0h          |          |    |    |    |    |    |             |

**Table 5-1207. CPSW\_NC\_ALE\_POLICECFG4 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                |
|-------|-------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | IPDST_MEN   | R/W  | 0h    | IP Destination Address Match Enable - Enables frame IP Destination address match for the selected policing/classifier entry                                |
| 30:25 | RESERVED    | NONE | 0h    | Reserved                                                                                                                                                   |
| 24:16 | IPDST_INDEX | R/W  | 0h    | IP Destination Address Table Entry Index - Specifies the ALE IP Destination address lookup table index to match for the selected policing/classifier entry |
| 15:0  | RESERVED    | NONE | 0h    | Reserved                                                                                                                                                   |

### 5.1.2.403 CPSW\_NC\_ALE\_POLICECFG6 Register

#### 1 CPSW\_NC\_ALE\_POLICECFG6 Register (Offset = 3E118h) [reset = 0h]

The PIR counter is a 37 bit internal counter where ~ipir\_idle\_inc\_val is added every clock and the frame size << 18 is subtracted at EOF if not RED at LUT time. If the counter is negative the packet will be marked RED, else it can be YELLOW or GREEN based on the CIR counter. If only this counter is used (aka cir\_idle\_inc\_val==0) Packet are marked RED or GREEN based on PIR counter only.

Return to [Summary Table](#)

**Table 5-1208. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E118h       |

**Figure 5-403. CPSW\_NC\_ALE\_POLICECFG6 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PIR_IDLE_INC_VAL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PIR_IDLE_INC_VAL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PIR_IDLE_INC_VAL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PIR_IDLE_INC_VAL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 5-1210. CPSW\_NC\_ALE\_POLICECFG6 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                   |
|------|------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | PIR_IDLE_INC_VAL | R/W  | 0h    | Peak Information Rate Idle Increment Value - The number added to the PIR counter every clock cycle. If zero the PIR counter is disabled and packets will never be marked or processed as RED. |

### 5.1.2.404 CPSW\_NC\_ALE\_POLICECFG7 Register

#### 1 CPSW\_NC\_ALE\_POLICECFG7 Register (Offset = 3E11Ch) [reset = 0h]

The CIR counter is a 37 bit internal counter where ~icir\_idle\_inc\_val is added every clock and the frame size << 18 is subtracted at EOF if not RED or YELLOW at LUT time. If the counter is positive the packet will be marked GREEN, else it can be YELLOW or RED based on the PIR counter. If only this counter is used (aka pir\_idle\_inc\_val==0) Packet are marked YELLOW or GREEN based on CIR counter only.

Return to [Summary Table](#)

**Table 5-1211. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E11Ch       |

**Figure 5-404. CPSW\_NC\_ALE\_POLICECFG7 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CIR_IDLE_INC_VAL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CIR_IDLE_INC_VAL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CIR_IDLE_INC_VAL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CIR_IDLE_INC_VAL |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 5-1213. CPSW\_NC\_ALE\_POLICECFG7 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                      |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CIR_IDLE_INC_VAL | R/W  | 0h    | Committed Information Idle Increment Value - The number added to the CIR counter every clock cycle. If zero the CIR counter is disabled and packets will never be marked or processed as YELLOW. |

### 5.1.2.405 CPSW\_NC\_ALE\_POLICETBLCTL Register

#### 1 CPSW\_NC\_ALE\_POLICETBLCTL Register (Offset = 3E120h) [reset = 0h]

The Policing Table Control is used to read or write the selected policing/classifier entry. The selected policing/classifier entry is only read or written after this register is written based on the value of the ~iwrite\_enable bit.

Return to [Summary Table](#)

**Table 5-1214. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E120h       |

**Figure 5-405. CPSW\_NC\_ALE\_POLICETBLCTL Name Register**

|              |          |    |             |    |    |    |    |
|--------------|----------|----|-------------|----|----|----|----|
| 31           | 30       | 29 | 28          | 27 | 26 | 25 | 24 |
| WRITE_ENABLE | RESERVED |    |             |    |    |    |    |
| R/W          | NONE     |    |             |    |    |    |    |
| 0h           | 0h       |    |             |    |    |    |    |
| 23           | 22       | 21 | 20          | 19 | 18 | 17 | 16 |
| RESERVED     |          |    |             |    |    |    |    |
| NONE         |          |    |             |    |    |    |    |
| 0h           |          |    |             |    |    |    |    |
| 15           | 14       | 13 | 12          | 11 | 10 | 9  | 8  |
| RESERVED     |          |    |             |    |    |    |    |
| NONE         |          |    |             |    |    |    |    |
| 0h           |          |    |             |    |    |    |    |
| 7            | 6        | 5  | 4           | 3  | 2  | 1  | 0  |
| RESERVED     |          |    | POL_TBL_IDX |    |    |    |    |
| NONE         |          |    | R/W         |    |    |    |    |
| 0h           |          |    | 0h          |    |    |    |    |

**Table 5-1216. CPSW\_NC\_ALE\_POLICETBLCTL Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                               |
|------|--------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31   | WRITE_ENABLE | R/W  | 0h    | Write Enable - Setting this bit will write the POLICECFG0-7 to the pol_tbl_idx selected policing/classifier entry. Clearing this bit will read the pol_tbl_idx selected policing/classifier entry into the POLICECFG0-7 registers.                                                                                                                                                                                        |
| 30:5 | RESERVED     | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 4:0  | POL_TBL_IDX  | R/W  | 0h    | Policer Entry Index - This field specifies the policing/classifier entry to be read or written. When writing to this field without setting the write_enable=1 will cause the selected policing/classifier entry to be loaded into the POLICECFG0-7 registers. When writing to this field with setting the write_enable=1 will cause the selected policing/classifier entry to be updated from the POLICECFG0-7 registers. |

### 5.1.2.406 CPSW\_NC\_ALE\_POLICECONTROL Register

#### 1 CPSW\_NC\_ALE\_POLICECONTROL Register (Offset = 3E124h) [reset = 0h]

The Control Enables color marking as well as internal ALE packet dropping rules.

Return to [Summary Table](#)

**Table 5-1217. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E124h       |

**Figure 5-406. CPSW\_NC\_ALE\_POLICECONTROL Name Register**

|             |          |                     |                  |          |              |    |    |
|-------------|----------|---------------------|------------------|----------|--------------|----|----|
| 31          | 30       | 29                  | 28               | 27       | 26           | 25 | 24 |
| POLICING_EN | RESERVED | RED_DROP_EN         | YELLOW_DROP_EN   | RESERVED | YELLOWTHRESH |    |    |
| R/W         | NONE     | R/W                 | R/W              | NONE     | R/W          |    |    |
| 0h          | 0h       | 0h                  | 0h               | 0h       | 0h           |    |    |
| 23          | 22       | 21                  | 20               | 19       | 18           | 17 | 16 |
| POLMCHMODE  |          | PRIORITY_TH_READ_EN | MAC_ONLY_DEF_DIS | RESERVED |              |    |    |
| R/W         |          | R/W                 | R/W              | NONE     |              |    |    |
| 0h          |          | 0h                  | 0h               | 0h       |              |    |    |
| 15          | 14       | 13                  | 12               | 11       | 10           | 9  | 8  |
| RESERVED    |          |                     |                  |          |              |    |    |
| NONE        |          |                     |                  |          |              |    |    |
| 0h          |          |                     |                  |          |              |    |    |
| 7           | 6        | 5                   | 4                | 3        | 2            | 1  | 0  |
| RESERVED    |          |                     |                  |          |              |    |    |
| NONE        |          |                     |                  |          |              |    |    |
| 0h          |          |                     |                  |          |              |    |    |

**Table 5-1219. CPSW\_NC\_ALE\_POLICECONTROL Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                      |
|-------|----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | POLICING_EN    | R/W  | 0h    | Policing Enable - Enables the policing to color the packets, this also enables red or yellow drop capabilities.                                                                                                                                                                                                                  |
| 30    | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                         |
| 29    | RED_DROP_EN    | R/W  | 0h    | RED Drop Enable - Enables the ALE to drop the red colored packets.                                                                                                                                                                                                                                                               |
| 28    | YELLOW_DROP_EN | R/W  | 0h    | YELLOW Drop Enable - Enables the ALE to drop yellow packets based on the yellowthresh value. This field would normally not be used as to let the switch drop packets at a buffer threshold instead. In the event that the switch does not enable buffer threshold dropping, YELLOW packets can be dropped based on this feature. |
| 27    | RESERVED       | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                         |
| 26:24 | YELLOWTHRESH   | R/W  | 0h    | Yellow Threshold - When set enables a portion of the yellow packets to be dropped based on the yellow_drop_en enable.<br>0-100%<br>1=50%<br>2=33%<br>3=25%<br>4=20%<br>5=17%<br>6=14%<br>7=13%                                                                                                                                   |

**Table 5-1219. CPSW\_NC\_ALE\_POLICECONTROL Register Field Descriptions (continued)**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                                                                                                                                          |
|-------|--------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:22 | POLMCHMODE         | R/W  | 0h    | Policing Match Mode - This field determines what happens to packets that fail to hit any policing/classifier entry.<br>0 - No Hit packets are marked GREEN<br>1 - No Hit packets are marked YELLOW<br>2 - No Hit packets are marked RED<br>3 - No Hit packets are marked based on policing/classifier entry=0 state. |
| 21    | PRIORITY_THREAD_EN | R/W  | 0h    | Priority Thread Enable - This field determines if priority is OR'd to the default thread when no classifiers hit and the default thread is enabled.                                                                                                                                                                  |
| 20    | MAC_ONLY_DEF_DIS   | R/W  | 0h    | MAC Only Default Disable - This field when set disables the default thread on MAC Only Ports. That is the default thread will be {port,priority}. If the traffic matches a classifier with a thread mapping, the classifier thread mapping still occurs.                                                             |
| 19:0  | RESERVED           | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                             |



### 5.1.2.407 CPSW\_NC\_ALE\_POLICETESTCTL Register

#### 1 CPSW\_NC\_ALE\_POLICETESTCTL Register (Offset = 3E128h) [reset = 0h]

The Policing Test Control enables the ability to determine which policing entry has been hit and whether they reported a red or yellow rate condition.

Return to [Summary Table](#)

**Table 5-1220. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E128h       |

**Figure 5-407. CPSW\_NC\_ALE\_POLICETESTCTL Name Register**

| 31             | 30                | 29                   | 28             | 27       | 26 | 25 | 24 |
|----------------|-------------------|----------------------|----------------|----------|----|----|----|
| POL_CLRALL_HIT | POL_CLRALL_REDHIT | POL_CLRALL_YELLOWHIT | POL_CLRSEL_ALL | RESERVED |    |    |    |
| R/W            | R/W               | R/W                  | R/W            | NONE     |    |    |    |
| 0h             | 0h                | 0h                   | 0h             | 0h       |    |    |    |
| 23             | 22                | 21                   | 20             | 19       | 18 | 17 | 16 |
| RESERVED       |                   |                      |                |          |    |    |    |
| NONE           |                   |                      |                |          |    |    |    |
| 0h             |                   |                      |                |          |    |    |    |
| 15             | 14                | 13                   | 12             | 11       | 10 | 9  | 8  |
| RESERVED       |                   |                      |                |          |    |    |    |
| NONE           |                   |                      |                |          |    |    |    |
| 0h             |                   |                      |                |          |    |    |    |
| 7              | 6                 | 5                    | 4              | 3        | 2  | 1  | 0  |
| RESERVED       |                   |                      | POL_TEST_IDX   |          |    |    |    |
| NONE           |                   |                      | R/W            |          |    |    |    |
| 0h             |                   |                      | 0h             |          |    |    |    |

**Table 5-1222. CPSW\_NC\_ALE\_POLICETESTCTL Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                                                                                                                                                                               |
|------|----------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31   | POL_CLRALL_HIT       | R/W  | 0h    | Policer Clear - This bit clears all the policing/classifier hit bits. This bit is self clearing. This can be used to test the fact that a policing/classifier entry has been hit.                                         |
| 30   | POL_CLRALL_REDHIT    | R/W  | 0h    | Policer Clear RED - This bit clears all the policing/classifier RED hit bits. This bit is self clearing. This can be used to test the fact that a policing/classifier entry has been hit during a RED condition.          |
| 29   | POL_CLRALL_YELLOWHIT | R/W  | 0h    | Policer Clear YELLOW - This bit clears all the policing/classifier YELLOW hit bits. This bit is self clearing. This can be used to test the fact that a policing/classifier entry has been hit during a YELLOW condition. |
| 28   | POL_CLRSEL_ALL       | R/W  | 0h    | Police Clear Selected - This bit clears the selected policing/classifier hit, redhit and yellowhit bits. This bit is self clearing.                                                                                       |
| 27:5 | RESERVED             | NONE | 0h    | Reserved                                                                                                                                                                                                                  |
| 4:0  | POL_TEST_IDX         | R/W  | 0h    | Policer Test Index - This field selects which policing/classifier hit bits will be read or written.                                                                                                                       |

### 5.1.2.408 CPSW\_NC\_ALE\_POLICEHSTAT Register

#### 1 CPSW\_NC\_ALE\_POLICEHSTAT Register (Offset = 3E12Ch) [reset = 0h]

The policing hit status is a read only register that reads the hit bits of the selected policing/classifier.

Return to [Summary Table](#)

**Table 5-1223. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E12Ch       |

**Figure 5-408. CPSW\_NC\_ALE\_POLICEHSTAT Name Register**

|          |            |                   |          |    |    |    |    |
|----------|------------|-------------------|----------|----|----|----|----|
| 31       | 30         | 29                | 28       | 27 | 26 | 25 | 24 |
| POL_HIT  | POL_REDHIT | POL_YELLOW<br>HIT | RESERVED |    |    |    |    |
| R        | R          | R                 | NONE     |    |    |    |    |
| 0h       | 0h         | 0h                | 0h       |    |    |    |    |
| 23       | 22         | 21                | 20       | 19 | 18 | 17 | 16 |
| RESERVED |            |                   |          |    |    |    |    |
| NONE     |            |                   |          |    |    |    |    |
| 0h       |            |                   |          |    |    |    |    |
| 15       | 14         | 13                | 12       | 11 | 10 | 9  | 8  |
| RESERVED |            |                   |          |    |    |    |    |
| NONE     |            |                   |          |    |    |    |    |
| 0h       |            |                   |          |    |    |    |    |
| 7        | 6          | 5                 | 4        | 3  | 2  | 1  | 0  |
| RESERVED |            |                   |          |    |    |    |    |
| NONE     |            |                   |          |    |    |    |    |
| 0h       |            |                   |          |    |    |    |    |

**Table 5-1225. CPSW\_NC\_ALE\_POLICEHSTAT Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                                                                                                                                                                                                |
|------|---------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31   | POL_HIT       | R    | 0h    | Policer Hit - This indicates that the selected policing/classifier via the pol_test_idx field has been hit by a packet seen on any port that matches the policing/classifier entry match.                                  |
| 30   | POL_REDHIT    | R    | 0h    | Policer Hit RED - This indicates that the selected policing/classifier via the pol_test_idx field has been hit during a RED condition by a packet seen on any port that matches the policing/classifier entry match.       |
| 29   | POL_YELLOWHIT | R    | 0h    | Policer Hit YELLOW - This indicates that the selected policing/classifier via the pol_test_idx field has been hit during a YELLOW condition by a packet seen on any port that matches the policing/classifier entry match. |
| 28:0 | RESERVED      | NONE | 0h    | Reserved                                                                                                                                                                                                                   |

### 5.1.2.409 CPSW\_NC\_ALE\_THREADMAPDEF Register

#### 1 CPSW\_NC\_ALE\_THREADMAPDEF Register (Offset = 3E134h) [reset = 0h]

The THREAD Mapping Default Value register is used to set the default thread ID when no classifier is matched,

Return to [Summary Table](#)

**Table 5-1226. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E134h       |

**Figure 5-409. CPSW\_NC\_ALE\_THREADMAPDEF Name Register**

|              |          |              |    |    |    |    |    |
|--------------|----------|--------------|----|----|----|----|----|
| 31           | 30       | 29           | 28 | 27 | 26 | 25 | 24 |
| RESERVED     |          |              |    |    |    |    |    |
| NONE         |          |              |    |    |    |    |    |
| 0h           |          |              |    |    |    |    |    |
| 23           | 22       | 21           | 20 | 19 | 18 | 17 | 16 |
| RESERVED     |          |              |    |    |    |    |    |
| NONE         |          |              |    |    |    |    |    |
| 0h           |          |              |    |    |    |    |    |
| 15           | 14       | 13           | 12 | 11 | 10 | 9  | 8  |
| DEFTHREAD_EN | RESERVED |              |    |    |    |    |    |
| R/W          | NONE     |              |    |    |    |    |    |
| 0h           | 0h       |              |    |    |    |    |    |
| 7            | 6        | 5            | 4  | 3  | 2  | 1  | 0  |
| RESERVED     |          | DEFTHREADVAL |    |    |    |    |    |
| NONE         |          | R/W          |    |    |    |    |    |
| 0h           |          | 0h           |    |    |    |    |    |

**Table 5-1228. CPSW\_NC\_ALE\_THREADMAPDEF Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                                                                                                                                                       |
|-------|--------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED     | NONE | 0h    | Reserved                                                                                                                                                                                                                                          |
| 15    | DEFTHREAD_EN | R/W  | 0h    | Default Tread Enable - When set the switch will use the deftheadval for the host interface thread ID if no classifier is matched. If clear the switch will generate its own thread ID based on port and priority if there is no classifier match. |
| 14:6  | RESERVED     | NONE | 0h    | Reserved                                                                                                                                                                                                                                          |
| 5:0   | DEFTHREADVAL | R/W  | 0h    | Default Thread Value - This field specifies the default thread ID value.                                                                                                                                                                          |

### 5.1.2.410 CPSW\_NC\_ALE\_THREADMAPCTL Register

#### 1 CPSW\_NC\_ALE\_THREADMAPCTL Register (Offset = 3E138h) [reset = 0h]

The THREAD Mapping Control register allows the highest matched classifier to return a particular thread ID for traffic sent to the host. This allows particular classifier matched traffic to be placed an a particular hosts queue.

Return to [Summary Table](#)

**Table 5-1229. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E138h       |

**Figure 5-410. CPSW\_NC\_ALE\_THREADMAPCTL Name Register**

|          |    |    |    |            |    |    |    |
|----------|----|----|----|------------|----|----|----|
| 31       | 30 | 29 | 28 | 27         | 26 | 25 | 24 |
| RESERVED |    |    |    |            |    |    |    |
| NONE     |    |    |    |            |    |    |    |
| 0h       |    |    |    |            |    |    |    |
| 23       | 22 | 21 | 20 | 19         | 18 | 17 | 16 |
| RESERVED |    |    |    |            |    |    |    |
| NONE     |    |    |    |            |    |    |    |
| 0h       |    |    |    |            |    |    |    |
| 15       | 14 | 13 | 12 | 11         | 10 | 9  | 8  |
| RESERVED |    |    |    |            |    |    |    |
| NONE     |    |    |    |            |    |    |    |
| 0h       |    |    |    |            |    |    |    |
| 7        | 6  | 5  | 4  | 3          | 2  | 1  | 0  |
| RESERVED |    |    |    | CLASSINDEX |    |    |    |
| NONE     |    |    |    | R/W        |    |    |    |
| 0h       |    |    |    | 0h         |    |    |    |

**Table 5-1231. CPSW\_NC\_ALE\_THREADMAPCTL Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                         |
|------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:5 | RESERVED   | NONE | 0h    | Reserved                                                                                                                                            |
| 4:0  | CLASSINDEX | R/W  | 0h    | Classifier Index - This is the classifier index entry that the thread enable and thread value will be read or written by the THREADMAPVAL register. |

### 5.1.2.411 CPSW\_NC\_ALE\_THREADMAPVAL Register

#### 1 CPSW\_NC\_ALE\_THREADMAPVAL Register (Offset = 3E13Ch) [reset = 0h]

The THREAD Mapping Value register is used to set the thread ID for a particular classifier entry.

Return to [Summary Table](#)

**Table 5-1232. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 E13Ch       |

**Figure 5-411. CPSW\_NC\_ALE\_THREADMAPVAL Name Register**

|           |          |           |    |    |    |    |    |
|-----------|----------|-----------|----|----|----|----|----|
| 31        | 30       | 29        | 28 | 27 | 26 | 25 | 24 |
| RESERVED  |          |           |    |    |    |    |    |
| NONE      |          |           |    |    |    |    |    |
| 0h        |          |           |    |    |    |    |    |
| 23        | 22       | 21        | 20 | 19 | 18 | 17 | 16 |
| RESERVED  |          |           |    |    |    |    |    |
| NONE      |          |           |    |    |    |    |    |
| 0h        |          |           |    |    |    |    |    |
| 15        | 14       | 13        | 12 | 11 | 10 | 9  | 8  |
| THREAD_EN | RESERVED |           |    |    |    |    |    |
| R/W       | NONE     |           |    |    |    |    |    |
| 0h        | 0h       |           |    |    |    |    |    |
| 7         | 6        | 5         | 4  | 3  | 2  | 1  | 0  |
| RESERVED  |          | THREADVAL |    |    |    |    |    |
| NONE      |          | R/W       |    |    |    |    |    |
| 0h        |          | 0h        |    |    |    |    |    |

**Table 5-1234. CPSW\_NC\_ALE\_THREADMAPVAL Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                        |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED  | NONE | 0h    | Reserved                                                                                                                                                                           |
| 15    | THREAD_EN | R/W  | 0h    | Thread Enable - When set the switch will use the threadval for the selected classifier match. If clear the the thread ID will be determined by the THREADMAPDEF register settings. |
| 14:6  | RESERVED  | NONE | 0h    | Reserved                                                                                                                                                                           |
| 5:0   | THREADVAL | R/W  | 0h    | Thread Value - This field is the thread ID value that is used to map a classifier hit to thread ID for host traffic.                                                               |

### 5.1.2.412 CPSW\_NC\_ECC\_REV Register

#### 1 CPSW\_NC\_ECC\_REV Register (Offset = 3F000h) [reset = 66A03201h]

Revision parameters

Return to [Summary Table](#)

**Table 5-1235. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 F000h       |

**Figure 5-412. CPSW\_NC\_ECC\_REV Name Register**

|           |    |        |    |           |        |    |    |
|-----------|----|--------|----|-----------|--------|----|----|
| 31        | 30 | 29     | 28 | 27        | 26     | 25 | 24 |
| SCHEME    |    | BU     |    | MODULE_ID |        |    |    |
| R         |    | R      |    | R         |        |    |    |
| 1h        |    | 2h     |    | 6A0h      |        |    |    |
| 23        | 22 | 21     | 20 | 19        | 18     | 17 | 16 |
| MODULE_ID |    |        |    |           |        |    |    |
| R         |    |        |    |           |        |    |    |
| 6A0h      |    |        |    |           |        |    |    |
| 15        | 14 | 13     | 12 | 11        | 10     | 9  | 8  |
| REVRTL    |    |        |    |           | REVMAJ |    |    |
| R         |    |        |    |           | R      |    |    |
| 6h        |    |        |    |           | 2h     |    |    |
| 7         | 6  | 5      | 4  | 3         | 2      | 1  | 0  |
| CUSTOM    |    | REVMIN |    |           |        |    |    |
| R         |    | R      |    |           |        |    |    |
| 0h        |    | 1h     |    |           |        |    |    |

**Table 5-1237. CPSW\_NC\_ECC\_REV Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description    |
|-------|-----------|------|-------|----------------|
| 31:30 | SCHEME    | R    | 1h    | Scheme         |
| 29:28 | BU        | R    | 2h    | bu             |
| 27:16 | MODULE_ID | R    | 6A0h  | Module ID      |
| 15:11 | REVRTL    | R    | 6h    | RTL version    |
| 10:8  | REVMAJ    | R    | 2h    | Major version  |
| 7:6   | CUSTOM    | R    | 0h    | Custom version |
| 5:0   | REVMIN    | R    | 1h    | Minor version  |

### 5.1.2.413 CPSW\_NC\_ECC\_VECTOR Register

#### 1 CPSW\_NC\_ECC\_VECTOR Register (Offset = 3F008h) [reset = 0h]

ECC Vector Register

Return to [Summary Table](#)

**Table 5-1238. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 F008h       |

**Figure 5-413. CPSW\_NC\_ECC\_VECTOR Name Register**

|                  |          |    |    |    |            |    |                   |
|------------------|----------|----|----|----|------------|----|-------------------|
| 31               | 30       | 29 | 28 | 27 | 26         | 25 | 24                |
| RESERVED         |          |    |    |    |            |    | RD_SVBUS_D<br>ONE |
| NONE             |          |    |    |    |            |    | R/W1TC            |
| 0h               |          |    |    |    |            |    | 0h                |
| 23               | 22       | 21 | 20 | 19 | 18         | 17 | 16                |
| RD_SVBUS_ADDRESS |          |    |    |    |            |    |                   |
| R/W              |          |    |    |    |            |    |                   |
| 0h               |          |    |    |    |            |    |                   |
| 15               | 14       | 13 | 12 | 11 | 10         | 9  | 8                 |
| RD_SVBUS         | RESERVED |    |    |    | ECC_VECTOR |    |                   |
| R/W1TS           | NONE     |    |    |    | R/W        |    |                   |
| 0h               | 0h       |    |    |    | 0h         |    |                   |
| 7                | 6        | 5  | 4  | 3  | 2          | 1  | 0                 |
| ECC_VECTOR       |          |    |    |    |            |    |                   |
| R/W              |          |    |    |    |            |    |                   |
| 0h               |          |    |    |    |            |    |                   |

**Table 5-1240. CPSW\_NC\_ECC\_VECTOR Register Field Descriptions**

| Bit   | Field            | Type   | Reset | Description                                                                                    |
|-------|------------------|--------|-------|------------------------------------------------------------------------------------------------|
| 31:25 | RESERVED         | NONE   | 0h    | Reserved                                                                                       |
| 24    | RD_SVBUS_DONE    | R/W1TC | 0h    | Status to indicate if read on serial VBUS is complete, write of any value will clear this bit. |
| 23:16 | RD_SVBUS_ADDRESS | R/W    | 0h    | Read address                                                                                   |
| 15    | RD_SVBUS         | R/W1TS | 0h    | Write 1 to trigger a read on the serial VBUS                                                   |
| 14:11 | RESERVED         | NONE   | 0h    | Reserved                                                                                       |
| 10:0  | ECC_VECTOR       | R/W    | 0h    | Value written to select the corresponding ECC RAM for control or status                        |

### 5.1.2.414 CPSW\_NC\_ECC\_STAT Register

#### 1 CPSW\_NC\_ECC\_STAT Register (Offset = 3F00Ch) [reset = 14h]

Misc Status

Return to [Summary Table](#)

**Table 5-1241. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 F00Ch       |

**Figure 5-414. CPSW\_NC\_ECC\_STAT Name Register**

|          |    |    |    |    |          |    |    |
|----------|----|----|----|----|----------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26       | 25 | 24 |
| RESERVED |    |    |    |    |          |    |    |
| NONE     |    |    |    |    |          |    |    |
| 0h       |    |    |    |    |          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18       | 17 | 16 |
| RESERVED |    |    |    |    |          |    |    |
| NONE     |    |    |    |    |          |    |    |
| 0h       |    |    |    |    |          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10       | 9  | 8  |
| RESERVED |    |    |    |    | NUM_RAMs |    |    |
| NONE     |    |    |    |    | R        |    |    |
| 0h       |    |    |    |    | 14h      |    |    |
| 7        | 6  | 5  | 4  | 3  | 2        | 1  | 0  |
| NUM_RAMs |    |    |    |    |          |    |    |
| R        |    |    |    |    |          |    |    |
| 14h      |    |    |    |    |          |    |    |

**Table 5-1243. CPSW\_NC\_ECC\_STAT Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                 |
|-------|----------|------|-------|-------------------------------------------------------------|
| 31:11 | RESERVED | NONE | 0h    | Reserved                                                    |
| 10:0  | NUM_RAMs | R    | 14h   | Indicates the number of RAMs serviced by the ECC aggregator |



### 5.1.2.415 CPSW\_NC\_ECC\_RESERVED\_SVBUS Register

#### 1 CPSW\_NC\_ECC\_RESERVED\_SVBUS Register (Offset = 3F010h) [reset = 0h]

Reference other documents that contain the ECC RAM wrapper and EDC controller serial vbus register sets.

Return to [Summary Table](#)

**Table 5-1244. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 F010h       |

**Figure 5-415. CPSW\_NC\_ECC\_RESERVED\_SVBUS Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-1246. CPSW\_NC\_ECC\_RESERVED\_SVBUS Register Field Descriptions**

| Bit  | Field | Type | Reset | Description               |
|------|-------|------|-------|---------------------------|
| 31:0 | DATA  | R/W  | 0h    | Serial VBUS register data |

### 5.1.2.416 CPSW\_NC\_ECC\_SEC\_EOI\_REG Register

#### 1 CPSW\_NC\_ECC\_SEC\_EOI\_REG Register (Offset = 3F03Ch) [reset = 0h]

EOI Register

Return to [Summary Table](#)

**Table 5-1247. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 F03Ch       |

**Figure 5-416. CPSW\_NC\_ECC\_SEC\_EOI\_REG Name Register**

|          |    |    |    |    |    |    |        |
|----------|----|----|----|----|----|----|--------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24     |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16     |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8      |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0      |
| RESERVED |    |    |    |    |    |    | EOI_WR |
| NONE     |    |    |    |    |    |    | R/W1TS |
| 0h       |    |    |    |    |    |    | 0h     |

**Table 5-1249. CPSW\_NC\_ECC\_SEC\_EOI\_REG Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description  |
|------|----------|--------|-------|--------------|
| 31:1 | RESERVED | NONE   | 0h    | Reserved     |
| 0    | EOI_WR   | R/W1TS | 0h    | EOI Register |

### 5.1.2.417 CPSW\_NC\_ECC\_SEC\_STATUS\_REG0 Register

#### 1 CPSW\_NC\_ECC\_SEC\_STATUS\_REG0 Register (Offset = 3F040h) [reset = 0h]

Interrupt Status Register 0

Return to [Summary Table](#)

**Table 5-1250. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 F040h       |

**Figure 5-417. CPSW\_NC\_ECC\_SEC\_STATUS\_REG0 Name Register**

|                   |                   |                   |                   |                   |                   |                   |                   |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| 31                | 30                | 29                | 28                | 27                | 26                | 25                | 24                |
| RESERVED          |                   |                   |                   |                   |                   |                   |                   |
| NONE              |                   |                   |                   |                   |                   |                   |                   |
| 0h                |                   |                   |                   |                   |                   |                   |                   |
| 23                | 22                | 21                | 20                | 19                | 18                | 17                | 16                |
| RESERVED          |                   |                   |                   | RAMECC19_P<br>END | RAMECC18_P<br>END | RAMECC17_P<br>END | RAMECC16_P<br>END |
| NONE              |                   |                   |                   | R/W1TS            | R/W1TS            | R/W1TS            | R/W1TS            |
| 0h                |                   |                   |                   | 0h                | 0h                | 0h                | 0h                |
| 15                | 14                | 13                | 12                | 11                | 10                | 9                 | 8                 |
| RAMECC15_P<br>END | RAMECC14_P<br>END | RAMECC13_P<br>END | RAMECC12_P<br>END | RAMECC11_P<br>END | RAMECC10_P<br>END | RAMECC9_P<br>END  | RAMECC8_P<br>END  |
| R/W1TS            | R/W1TS            | R/W1TS            | R/W1TS            | R/W1TS            | R/W1TS            | R/W1TS            | R/W1TS            |
| 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                |
| 7                 | 6                 | 5                 | 4                 | 3                 | 2                 | 1                 | 0                 |
| RAMECC7_P<br>END  | RAMECC6_P<br>END  | RAMECC5_P<br>END  | RAMECC4_P<br>END  | RAMECC3_P<br>END  | RAMECC2_P<br>END  | RAMECC1_P<br>END  | RAMECC0_P<br>END  |
| R/W1TS            | R/W1TS            | R/W1TS            | R/W1TS            | R/W1TS            | R/W1TS            | R/W1TS            | R/W1TS            |
| 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                |

**Table 5-1252. CPSW\_NC\_ECC\_SEC\_STATUS\_REG0 Register Field Descriptions**

| Bit   | Field         | Type   | Reset | Description                                |
|-------|---------------|--------|-------|--------------------------------------------|
| 31:20 | RESERVED      | NONE   | 0h    | Reserved                                   |
| 19    | RAMECC19_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc19_pend |
| 18    | RAMECC18_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc18_pend |
| 17    | RAMECC17_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc17_pend |
| 16    | RAMECC16_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc16_pend |
| 15    | RAMECC15_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc15_pend |
| 14    | RAMECC14_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc14_pend |
| 13    | RAMECC13_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc13_pend |
| 12    | RAMECC12_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc12_pend |
| 11    | RAMECC11_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc11_pend |
| 10    | RAMECC10_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc10_pend |
| 9     | RAMECC9_PEND  | R/W1TS | 0h    | Interrupt Pending Status for ramecc9_pend  |
| 8     | RAMECC8_PEND  | R/W1TS | 0h    | Interrupt Pending Status for ramecc8_pend  |
| 7     | RAMECC7_PEND  | R/W1TS | 0h    | Interrupt Pending Status for ramecc7_pend  |
| 6     | RAMECC6_PEND  | R/W1TS | 0h    | Interrupt Pending Status for ramecc6_pend  |
| 5     | RAMECC5_PEND  | R/W1TS | 0h    | Interrupt Pending Status for ramecc5_pend  |

**Table 5-1252. CPSW\_NC\_ECC\_SEC\_STATUS\_REG0 Register Field Descriptions (continued)**

| Bit | Field        | Type   | Reset | Description                               |
|-----|--------------|--------|-------|-------------------------------------------|
| 4   | RAMECC4_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc4_pend |
| 3   | RAMECC3_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc3_pend |
| 2   | RAMECC2_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc2_pend |
| 1   | RAMECC1_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc1_pend |
| 0   | RAMECC0_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc0_pend |

### 5.1.2.418 CPSW\_NC\_ECC\_SEC\_ENABLE\_SET\_REG0 Register

#### 1 CPSW\_NC\_ECC\_SEC\_ENABLE\_SET\_REG0 Register (Offset = 3F080h) [reset = 0h]

Interrupt Enable Set Register 0

Return to [Summary Table](#)

**Table 5-1253. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 F080h       |

**Figure 5-418. CPSW\_NC\_ECC\_SEC\_ENABLE\_SET\_REG0 Name Register**

|                         |                         |                         |                         |                         |                         |                         |                         |
|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| 31                      | 30                      | 29                      | 28                      | 27                      | 26                      | 25                      | 24                      |
| RESERVED                |                         |                         |                         |                         |                         |                         |                         |
| NONE                    |                         |                         |                         |                         |                         |                         |                         |
| 0h                      |                         |                         |                         |                         |                         |                         |                         |
| 23                      | 22                      | 21                      | 20                      | 19                      | 18                      | 17                      | 16                      |
| RESERVED                |                         |                         |                         | RAMECC19_E<br>NABLE_SET | RAMECC18_E<br>NABLE_SET | RAMECC17_E<br>NABLE_SET | RAMECC16_E<br>NABLE_SET |
| NONE                    |                         |                         |                         | R/W1TS                  | R/W1TS                  | R/W1TS                  | R/W1TS                  |
| 0h                      |                         |                         |                         | 0h                      | 0h                      | 0h                      | 0h                      |
| 15                      | 14                      | 13                      | 12                      | 11                      | 10                      | 9                       | 8                       |
| RAMECC15_E<br>NABLE_SET | RAMECC14_E<br>NABLE_SET | RAMECC13_E<br>NABLE_SET | RAMECC12_E<br>NABLE_SET | RAMECC11_E<br>NABLE_SET | RAMECC10_E<br>NABLE_SET | RAMECC9_EN<br>ABLE_SET  | RAMECC8_EN<br>ABLE_SET  |
| R/W1TS                  | R/W1TS                  | R/W1TS                  | R/W1TS                  | R/W1TS                  | R/W1TS                  | R/W1TS                  | R/W1TS                  |
| 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      |
| 7                       | 6                       | 5                       | 4                       | 3                       | 2                       | 1                       | 0                       |
| RAMECC7_EN<br>ABLE_SET  | RAMECC6_EN<br>ABLE_SET  | RAMECC5_EN<br>ABLE_SET  | RAMECC4_EN<br>ABLE_SET  | RAMECC3_EN<br>ABLE_SET  | RAMECC2_EN<br>ABLE_SET  | RAMECC1_EN<br>ABLE_SET  | RAMECC0_EN<br>ABLE_SET  |
| R/W1TS                  | R/W1TS                  | R/W1TS                  | R/W1TS                  | R/W1TS                  | R/W1TS                  | R/W1TS                  | R/W1TS                  |
| 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 5-1255. CPSW\_NC\_ECC\_SEC\_ENABLE\_SET\_REG0 Register Field Descriptions**

| Bit   | Field                   | Type   | Reset | Description                                     |
|-------|-------------------------|--------|-------|-------------------------------------------------|
| 31:20 | RESERVED                | NONE   | 0h    | Reserved                                        |
| 19    | RAMECC19_ENABLE_SE<br>T | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc19_pend |
| 18    | RAMECC18_ENABLE_SE<br>T | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc18_pend |
| 17    | RAMECC17_ENABLE_SE<br>T | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc17_pend |
| 16    | RAMECC16_ENABLE_SE<br>T | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc16_pend |
| 15    | RAMECC15_ENABLE_SE<br>T | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc15_pend |
| 14    | RAMECC14_ENABLE_SE<br>T | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc14_pend |
| 13    | RAMECC13_ENABLE_SE<br>T | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc13_pend |
| 12    | RAMECC12_ENABLE_SE<br>T | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc12_pend |
| 11    | RAMECC11_ENABLE_SE<br>T | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc11_pend |

**Table 5-1255. CPSW\_NC\_ECC\_SEC\_ENABLE\_SET\_REG0 Register Field Descriptions (continued)**

| Bit | Field               | Type   | Reset | Description                                     |
|-----|---------------------|--------|-------|-------------------------------------------------|
| 10  | RAMECC10_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc10_pend |
| 9   | RAMECC9_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc9_pend  |
| 8   | RAMECC8_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc8_pend  |
| 7   | RAMECC7_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc7_pend  |
| 6   | RAMECC6_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc6_pend  |
| 5   | RAMECC5_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc5_pend  |
| 4   | RAMECC4_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc4_pend  |
| 3   | RAMECC3_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc3_pend  |
| 2   | RAMECC2_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc2_pend  |
| 1   | RAMECC1_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc1_pend  |
| 0   | RAMECC0_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc0_pend  |

### 5.1.2.419 CPSW\_NC\_ECC\_SEC\_ENABLE\_CLR\_REG0 Register

#### 1 CPSW\_NC\_ECC\_SEC\_ENABLE\_CLR\_REG0 Register (Offset = 3F0C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to [Summary Table](#)

**Table 5-1256. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 F0C0h       |

**Figure 5-419. CPSW\_NC\_ECC\_SEC\_ENABLE\_CLR\_REG0 Name Register**

|                         |                         |                         |                         |                         |                         |                         |                         |
|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| 31                      | 30                      | 29                      | 28                      | 27                      | 26                      | 25                      | 24                      |
| RESERVED                |                         |                         |                         |                         |                         |                         |                         |
| NONE                    |                         |                         |                         |                         |                         |                         |                         |
| 0h                      |                         |                         |                         |                         |                         |                         |                         |
| 23                      | 22                      | 21                      | 20                      | 19                      | 18                      | 17                      | 16                      |
| RESERVED                |                         |                         |                         | RAMECC19_E<br>NABLE_CLR | RAMECC18_E<br>NABLE_CLR | RAMECC17_E<br>NABLE_CLR | RAMECC16_E<br>NABLE_CLR |
| NONE                    |                         |                         |                         | R/W1TC                  | R/W1TC                  | R/W1TC                  | R/W1TC                  |
| 0h                      |                         |                         |                         | 0h                      | 0h                      | 0h                      | 0h                      |
| 15                      | 14                      | 13                      | 12                      | 11                      | 10                      | 9                       | 8                       |
| RAMECC15_E<br>NABLE_CLR | RAMECC14_E<br>NABLE_CLR | RAMECC13_E<br>NABLE_CLR | RAMECC12_E<br>NABLE_CLR | RAMECC11_E<br>NABLE_CLR | RAMECC10_E<br>NABLE_CLR | RAMECC9_EN<br>ABLE_CLR  | RAMECC8_EN<br>ABLE_CLR  |
| R/W1TC                  | R/W1TC                  | R/W1TC                  | R/W1TC                  | R/W1TC                  | R/W1TC                  | R/W1TC                  | R/W1TC                  |
| 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      |
| 7                       | 6                       | 5                       | 4                       | 3                       | 2                       | 1                       | 0                       |
| RAMECC7_EN<br>ABLE_CLR  | RAMECC6_EN<br>ABLE_CLR  | RAMECC5_EN<br>ABLE_CLR  | RAMECC4_EN<br>ABLE_CLR  | RAMECC3_EN<br>ABLE_CLR  | RAMECC2_EN<br>ABLE_CLR  | RAMECC1_EN<br>ABLE_CLR  | RAMECC0_EN<br>ABLE_CLR  |
| R/W1TC                  | R/W1TC                  | R/W1TC                  | R/W1TC                  | R/W1TC                  | R/W1TC                  | R/W1TC                  | R/W1TC                  |
| 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 5-1258. CPSW\_NC\_ECC\_SEC\_ENABLE\_CLR\_REG0 Register Field Descriptions**

| Bit   | Field               | Type   | Reset | Description                                       |
|-------|---------------------|--------|-------|---------------------------------------------------|
| 31:20 | RESERVED            | NONE   | 0h    | Reserved                                          |
| 19    | RAMECC19_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc19_pend |
| 18    | RAMECC18_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc18_pend |
| 17    | RAMECC17_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc17_pend |
| 16    | RAMECC16_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc16_pend |
| 15    | RAMECC15_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc15_pend |
| 14    | RAMECC14_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc14_pend |
| 13    | RAMECC13_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc13_pend |
| 12    | RAMECC12_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc12_pend |
| 11    | RAMECC11_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc11_pend |

**Table 5-1258. CPSW\_NC\_ECC\_SEC\_ENABLE\_CLR\_REG0 Register Field Descriptions (continued)**

| Bit | Field               | Type   | Reset | Description                                       |
|-----|---------------------|--------|-------|---------------------------------------------------|
| 10  | RAMECC10_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc10_pend |
| 9   | RAMECC9_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc9_pend  |
| 8   | RAMECC8_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc8_pend  |
| 7   | RAMECC7_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc7_pend  |
| 6   | RAMECC6_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc6_pend  |
| 5   | RAMECC5_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc5_pend  |
| 4   | RAMECC4_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc4_pend  |
| 3   | RAMECC3_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc3_pend  |
| 2   | RAMECC2_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc2_pend  |
| 1   | RAMECC1_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc1_pend  |
| 0   | RAMECC0_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc0_pend  |



### 5.1.2.420 CPSW\_NC\_ECC\_DED\_EOI\_REG Register

#### 1 CPSW\_NC\_ECC\_DED\_EOI\_REG Register (Offset = 3F13Ch) [reset = 0h]

EOI Register

Return to [Summary Table](#)

**Table 5-1259. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 F13Ch       |

**Figure 5-420. CPSW\_NC\_ECC\_DED\_EOI\_REG Name Register**

|          |    |    |    |    |    |    |        |
|----------|----|----|----|----|----|----|--------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24     |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16     |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8      |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0      |
| RESERVED |    |    |    |    |    |    | EOI_WR |
| NONE     |    |    |    |    |    |    | R/W1TS |
| 0h       |    |    |    |    |    |    | 0h     |

**Table 5-1261. CPSW\_NC\_ECC\_DED\_EOI\_REG Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description  |
|------|----------|--------|-------|--------------|
| 31:1 | RESERVED | NONE   | 0h    | Reserved     |
| 0    | EOI_WR   | R/W1TS | 0h    | EOI Register |

### 5.1.2.421 CPSW\_NC\_ECC\_DED\_STATUS\_REG0 Register

#### 1 CPSW\_NC\_ECC\_DED\_STATUS\_REG0 Register (Offset = 3F140h) [reset = 0h]

Interrupt Status Register 0

Return to [Summary Table](#)

**Table 5-1262. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 F140h       |

**Figure 5-421. CPSW\_NC\_ECC\_DED\_STATUS\_REG0 Name Register**

|                   |                   |                   |                   |                   |                   |                   |                   |
|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| 31                | 30                | 29                | 28                | 27                | 26                | 25                | 24                |
| RESERVED          |                   |                   |                   |                   |                   |                   |                   |
| NONE              |                   |                   |                   |                   |                   |                   |                   |
| 0h                |                   |                   |                   |                   |                   |                   |                   |
| 23                | 22                | 21                | 20                | 19                | 18                | 17                | 16                |
| RESERVED          |                   |                   |                   | RAMECC19_P<br>END | RAMECC18_P<br>END | RAMECC17_P<br>END | RAMECC16_P<br>END |
| NONE              |                   |                   |                   | R/W1TS            | R/W1TS            | R/W1TS            | R/W1TS            |
| 0h                |                   |                   |                   | 0h                | 0h                | 0h                | 0h                |
| 15                | 14                | 13                | 12                | 11                | 10                | 9                 | 8                 |
| RAMECC15_P<br>END | RAMECC14_P<br>END | RAMECC13_P<br>END | RAMECC12_P<br>END | RAMECC11_P<br>END | RAMECC10_P<br>END | RAMECC9_P<br>END  | RAMECC8_P<br>END  |
| R/W1TS            | R/W1TS            | R/W1TS            | R/W1TS            | R/W1TS            | R/W1TS            | R/W1TS            | R/W1TS            |
| 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                |
| 7                 | 6                 | 5                 | 4                 | 3                 | 2                 | 1                 | 0                 |
| RAMECC7_P<br>END  | RAMECC6_P<br>END  | RAMECC5_P<br>END  | RAMECC4_P<br>END  | RAMECC3_P<br>END  | RAMECC2_P<br>END  | RAMECC1_P<br>END  | RAMECC0_P<br>END  |
| R/W1TS            | R/W1TS            | R/W1TS            | R/W1TS            | R/W1TS            | R/W1TS            | R/W1TS            | R/W1TS            |
| 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                | 0h                |

**Table 5-1264. CPSW\_NC\_ECC\_DED\_STATUS\_REG0 Register Field Descriptions**

| Bit   | Field         | Type   | Reset | Description                                |
|-------|---------------|--------|-------|--------------------------------------------|
| 31:20 | RESERVED      | NONE   | 0h    | Reserved                                   |
| 19    | RAMECC19_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc19_pend |
| 18    | RAMECC18_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc18_pend |
| 17    | RAMECC17_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc17_pend |
| 16    | RAMECC16_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc16_pend |
| 15    | RAMECC15_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc15_pend |
| 14    | RAMECC14_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc14_pend |
| 13    | RAMECC13_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc13_pend |
| 12    | RAMECC12_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc12_pend |
| 11    | RAMECC11_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc11_pend |
| 10    | RAMECC10_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc10_pend |
| 9     | RAMECC9_PEND  | R/W1TS | 0h    | Interrupt Pending Status for ramecc9_pend  |
| 8     | RAMECC8_PEND  | R/W1TS | 0h    | Interrupt Pending Status for ramecc8_pend  |
| 7     | RAMECC7_PEND  | R/W1TS | 0h    | Interrupt Pending Status for ramecc7_pend  |
| 6     | RAMECC6_PEND  | R/W1TS | 0h    | Interrupt Pending Status for ramecc6_pend  |
| 5     | RAMECC5_PEND  | R/W1TS | 0h    | Interrupt Pending Status for ramecc5_pend  |

**Table 5-1264. CPSW\_NC\_ECC\_DED\_STATUS\_REG0 Register Field Descriptions (continued)**

| Bit | Field        | Type   | Reset | Description                               |
|-----|--------------|--------|-------|-------------------------------------------|
| 4   | RAMECC4_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc4_pend |
| 3   | RAMECC3_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc3_pend |
| 2   | RAMECC2_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc2_pend |
| 1   | RAMECC1_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc1_pend |
| 0   | RAMECC0_PEND | R/W1TS | 0h    | Interrupt Pending Status for ramecc0_pend |

### 5.1.2.422 CPSW\_NC\_ECC\_DED\_ENABLE\_SET\_REG0 Register

#### 1 CPSW\_NC\_ECC\_DED\_ENABLE\_SET\_REG0 Register (Offset = 3F180h) [reset = 0h]

Interrupt Enable Set Register 0

Return to [Summary Table](#)

**Table 5-1265. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 F180h       |

**Figure 5-422. CPSW\_NC\_ECC\_DED\_ENABLE\_SET\_REG0 Name Register**

|                         |                         |                         |                         |                         |                         |                         |                         |
|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| 31                      | 30                      | 29                      | 28                      | 27                      | 26                      | 25                      | 24                      |
| RESERVED                |                         |                         |                         |                         |                         |                         |                         |
| NONE                    |                         |                         |                         |                         |                         |                         |                         |
| 0h                      |                         |                         |                         |                         |                         |                         |                         |
| 23                      | 22                      | 21                      | 20                      | 19                      | 18                      | 17                      | 16                      |
| RESERVED                |                         |                         |                         | RAMECC19_E<br>NABLE_SET | RAMECC18_E<br>NABLE_SET | RAMECC17_E<br>NABLE_SET | RAMECC16_E<br>NABLE_SET |
| NONE                    |                         |                         |                         | R/W1TS                  | R/W1TS                  | R/W1TS                  | R/W1TS                  |
| 0h                      |                         |                         |                         | 0h                      | 0h                      | 0h                      | 0h                      |
| 15                      | 14                      | 13                      | 12                      | 11                      | 10                      | 9                       | 8                       |
| RAMECC15_E<br>NABLE_SET | RAMECC14_E<br>NABLE_SET | RAMECC13_E<br>NABLE_SET | RAMECC12_E<br>NABLE_SET | RAMECC11_E<br>NABLE_SET | RAMECC10_E<br>NABLE_SET | RAMECC9_EN<br>ABLE_SET  | RAMECC8_EN<br>ABLE_SET  |
| R/W1TS                  | R/W1TS                  | R/W1TS                  | R/W1TS                  | R/W1TS                  | R/W1TS                  | R/W1TS                  | R/W1TS                  |
| 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      |
| 7                       | 6                       | 5                       | 4                       | 3                       | 2                       | 1                       | 0                       |
| RAMECC7_EN<br>ABLE_SET  | RAMECC6_EN<br>ABLE_SET  | RAMECC5_EN<br>ABLE_SET  | RAMECC4_EN<br>ABLE_SET  | RAMECC3_EN<br>ABLE_SET  | RAMECC2_EN<br>ABLE_SET  | RAMECC1_EN<br>ABLE_SET  | RAMECC0_EN<br>ABLE_SET  |
| R/W1TS                  | R/W1TS                  | R/W1TS                  | R/W1TS                  | R/W1TS                  | R/W1TS                  | R/W1TS                  | R/W1TS                  |
| 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 5-1267. CPSW\_NC\_ECC\_DED\_ENABLE\_SET\_REG0 Register Field Descriptions**

| Bit   | Field                   | Type   | Reset | Description                                     |
|-------|-------------------------|--------|-------|-------------------------------------------------|
| 31:20 | RESERVED                | NONE   | 0h    | Reserved                                        |
| 19    | RAMECC19_ENABLE_SE<br>T | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc19_pend |
| 18    | RAMECC18_ENABLE_SE<br>T | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc18_pend |
| 17    | RAMECC17_ENABLE_SE<br>T | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc17_pend |
| 16    | RAMECC16_ENABLE_SE<br>T | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc16_pend |
| 15    | RAMECC15_ENABLE_SE<br>T | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc15_pend |
| 14    | RAMECC14_ENABLE_SE<br>T | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc14_pend |
| 13    | RAMECC13_ENABLE_SE<br>T | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc13_pend |
| 12    | RAMECC12_ENABLE_SE<br>T | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc12_pend |
| 11    | RAMECC11_ENABLE_SE<br>T | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc11_pend |

**Table 5-1267. CPSW\_NC\_ECC\_DED\_ENABLE\_SET\_REG0 Register Field Descriptions (continued)**

| Bit | Field               | Type   | Reset | Description                                     |
|-----|---------------------|--------|-------|-------------------------------------------------|
| 10  | RAMECC10_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc10_pend |
| 9   | RAMECC9_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc9_pend  |
| 8   | RAMECC8_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc8_pend  |
| 7   | RAMECC7_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc7_pend  |
| 6   | RAMECC6_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc6_pend  |
| 5   | RAMECC5_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc5_pend  |
| 4   | RAMECC4_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc4_pend  |
| 3   | RAMECC3_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc3_pend  |
| 2   | RAMECC2_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc2_pend  |
| 1   | RAMECC1_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc1_pend  |
| 0   | RAMECC0_ENABLE_SET  | R/W1TS | 0h    | Interrupt Enable Set Register for ramecc0_pend  |

### 5.1.2.423 CPSW\_NC\_ECC\_DED\_ENABLE\_CLR\_REG0 Register

#### 1 CPSW\_NC\_ECC\_DED\_ENABLE\_CLR\_REG0 Register (Offset = 3F1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to [Summary Table](#)

**Table 5-1268. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 F1C0h       |

**Figure 5-423. CPSW\_NC\_ECC\_DED\_ENABLE\_CLR\_REG0 Name Register**

|                         |                         |                         |                         |                         |                         |                         |                         |
|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| 31                      | 30                      | 29                      | 28                      | 27                      | 26                      | 25                      | 24                      |
| RESERVED                |                         |                         |                         |                         |                         |                         |                         |
| NONE                    |                         |                         |                         |                         |                         |                         |                         |
| 0h                      |                         |                         |                         |                         |                         |                         |                         |
| 23                      | 22                      | 21                      | 20                      | 19                      | 18                      | 17                      | 16                      |
| RESERVED                |                         |                         |                         | RAMECC19_E<br>NABLE_CLR | RAMECC18_E<br>NABLE_CLR | RAMECC17_E<br>NABLE_CLR | RAMECC16_E<br>NABLE_CLR |
| NONE                    |                         |                         |                         | R/W1TC                  | R/W1TC                  | R/W1TC                  | R/W1TC                  |
| 0h                      |                         |                         |                         | 0h                      | 0h                      | 0h                      | 0h                      |
| 15                      | 14                      | 13                      | 12                      | 11                      | 10                      | 9                       | 8                       |
| RAMECC15_E<br>NABLE_CLR | RAMECC14_E<br>NABLE_CLR | RAMECC13_E<br>NABLE_CLR | RAMECC12_E<br>NABLE_CLR | RAMECC11_E<br>NABLE_CLR | RAMECC10_E<br>NABLE_CLR | RAMECC9_EN<br>ABLE_CLR  | RAMECC8_EN<br>ABLE_CLR  |
| R/W1TC                  | R/W1TC                  | R/W1TC                  | R/W1TC                  | R/W1TC                  | R/W1TC                  | R/W1TC                  | R/W1TC                  |
| 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      |
| 7                       | 6                       | 5                       | 4                       | 3                       | 2                       | 1                       | 0                       |
| RAMECC7_EN<br>ABLE_CLR  | RAMECC6_EN<br>ABLE_CLR  | RAMECC5_EN<br>ABLE_CLR  | RAMECC4_EN<br>ABLE_CLR  | RAMECC3_EN<br>ABLE_CLR  | RAMECC2_EN<br>ABLE_CLR  | RAMECC1_EN<br>ABLE_CLR  | RAMECC0_EN<br>ABLE_CLR  |
| R/W1TC                  | R/W1TC                  | R/W1TC                  | R/W1TC                  | R/W1TC                  | R/W1TC                  | R/W1TC                  | R/W1TC                  |
| 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      | 0h                      |

**Table 5-1270. CPSW\_NC\_ECC\_DED\_ENABLE\_CLR\_REG0 Register Field Descriptions**

| Bit   | Field               | Type   | Reset | Description                                       |
|-------|---------------------|--------|-------|---------------------------------------------------|
| 31:20 | RESERVED            | NONE   | 0h    | Reserved                                          |
| 19    | RAMECC19_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc19_pend |
| 18    | RAMECC18_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc18_pend |
| 17    | RAMECC17_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc17_pend |
| 16    | RAMECC16_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc16_pend |
| 15    | RAMECC15_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc15_pend |
| 14    | RAMECC14_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc14_pend |
| 13    | RAMECC13_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc13_pend |
| 12    | RAMECC12_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc12_pend |
| 11    | RAMECC11_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc11_pend |

**Table 5-1270. CPSW\_NC\_ECC\_DED\_ENABLE\_CLR\_REG0 Register Field Descriptions (continued)**

| Bit | Field               | Type   | Reset | Description                                       |
|-----|---------------------|--------|-------|---------------------------------------------------|
| 10  | RAMECC10_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc10_pend |
| 9   | RAMECC9_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc9_pend  |
| 8   | RAMECC8_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc8_pend  |
| 7   | RAMECC7_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc7_pend  |
| 6   | RAMECC6_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc6_pend  |
| 5   | RAMECC5_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc5_pend  |
| 4   | RAMECC4_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc4_pend  |
| 3   | RAMECC3_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc3_pend  |
| 2   | RAMECC2_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc2_pend  |
| 1   | RAMECC1_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc1_pend  |
| 0   | RAMECC0_ENABLE_CLR  | R/W1TC | 0h    | Interrupt Enable Clear Register for ramecc0_pend  |

### 5.1.2.424 CPSW\_NC\_ECC\_AGGR\_ENABLE\_SET Register

#### 1 CPSW\_NC\_ECC\_AGGR\_ENABLE\_SET Register (Offset = 3F200h) [reset = 0h]

AGGR interrupt enable set Register

Return to [Summary Table](#)

**Table 5-1271. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 F200h       |

**Figure 5-424. CPSW\_NC\_ECC\_AGGR\_ENABLE\_SET Name Register**

|          |    |    |    |    |    |         |        |
|----------|----|----|----|----|----|---------|--------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25      | 24     |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 23       | 22 | 21 | 20 | 19 | 18 | 17      | 16     |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 15       | 14 | 13 | 12 | 11 | 10 | 9       | 8      |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 7        | 6  | 5  | 4  | 3  | 2  | 1       | 0      |
| RESERVED |    |    |    |    |    | TIMEOUT | PARITY |
| NONE     |    |    |    |    |    | R/W1TS  | R/W1TS |
| 0h       |    |    |    |    |    | 0h      | 0h     |

**Table 5-1273. CPSW\_NC\_ECC\_AGGR\_ENABLE\_SET Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description                                   |
|------|----------|--------|-------|-----------------------------------------------|
| 31:2 | RESERVED | NONE   | 0h    | Reserved                                      |
| 1    | TIMEOUT  | R/W1TS | 0h    | interrupt enable set for svbus timeout errors |
| 0    | PARITY   | R/W1TS | 0h    | interrupt enable set for parity errors        |



### 5.1.2.425 CPSW\_NC\_ECC\_AGGR\_ENABLE\_CLR Register

#### 1 CPSW\_NC\_ECC\_AGGR\_ENABLE\_CLR Register (Offset = 3F204h) [reset = 0h]

AGGR interrupt enable clear Register

Return to [Summary Table](#)

**Table 5-1274. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 F204h       |

**Figure 5-425. CPSW\_NC\_ECC\_AGGR\_ENABLE\_CLR Name Register**

|          |    |    |    |    |    |         |        |
|----------|----|----|----|----|----|---------|--------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25      | 24     |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 23       | 22 | 21 | 20 | 19 | 18 | 17      | 16     |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 15       | 14 | 13 | 12 | 11 | 10 | 9       | 8      |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 7        | 6  | 5  | 4  | 3  | 2  | 1       | 0      |
| RESERVED |    |    |    |    |    | TIMEOUT | PARITY |
| NONE     |    |    |    |    |    | R/W1TC  | R/W1TC |
| 0h       |    |    |    |    |    | 0h      | 0h     |

**Table 5-1276. CPSW\_NC\_ECC\_AGGR\_ENABLE\_CLR Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description                                     |
|------|----------|--------|-------|-------------------------------------------------|
| 31:2 | RESERVED | NONE   | 0h    | Reserved                                        |
| 1    | TIMEOUT  | R/W1TC | 0h    | interrupt enable clear for svbus timeout errors |
| 0    | PARITY   | R/W1TC | 0h    | interrupt enable clear for parity errors        |

### 5.1.2.426 CPSW\_NC\_ECC\_AGGR\_STATUS\_SET Register

#### 1 CPSW\_NC\_ECC\_AGGR\_STATUS\_SET Register (Offset = 3F208h) [reset = 0h]

AGGR interrupt status set Register

Return to [Summary Table](#)

**Table 5-1277. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 F208h       |

**Figure 5-426. CPSW\_NC\_ECC\_AGGR\_STATUS\_SET Name Register**

|          |    |    |    |         |    |        |    |
|----------|----|----|----|---------|----|--------|----|
| 31       | 30 | 29 | 28 | 27      | 26 | 25     | 24 |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 23       | 22 | 21 | 20 | 19      | 18 | 17     | 16 |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 15       | 14 | 13 | 12 | 11      | 10 | 9      | 8  |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 7        | 6  | 5  | 4  | 3       | 2  | 1      | 0  |
| RESERVED |    |    |    | TIMEOUT |    | PARITY |    |
| NONE     |    |    |    | R/WI    |    | R/WI   |    |
| 0h       |    |    |    | 0h      |    | 0h     |    |

**Table 5-1279. CPSW\_NC\_ECC\_AGGR\_STATUS\_SET Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                   |
|------|----------|------|-------|-----------------------------------------------|
| 31:4 | RESERVED | NONE | 0h    | Reserved                                      |
| 3:2  | TIMEOUT  | R/WI | 0h    | interrupt status set for svbus timeout errors |
| 1:0  | PARITY   | R/WI | 0h    | interrupt status set for parity errors        |

### 5.1.2.427 CPSW\_NC\_ECC\_AGGR\_STATUS\_CLR Register

#### 1 CPSW\_NC\_ECC\_AGGR\_STATUS\_CLR Register (Offset = 3F20Ch) [reset = 0h]

AGGR interrupt status clear Register

Return to [Summary Table](#)

**Table 5-1280. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| CPSW0         | 5283 F20Ch       |

**Figure 5-427. CPSW\_NC\_ECC\_AGGR\_STATUS\_CLR Name Register**

|          |    |    |    |         |    |        |    |
|----------|----|----|----|---------|----|--------|----|
| 31       | 30 | 29 | 28 | 27      | 26 | 25     | 24 |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 23       | 22 | 21 | 20 | 19      | 18 | 17     | 16 |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 15       | 14 | 13 | 12 | 11      | 10 | 9      | 8  |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 7        | 6  | 5  | 4  | 3       | 2  | 1      | 0  |
| RESERVED |    |    |    | TIMEOUT |    | PARITY |    |
| NONE     |    |    |    | R/WD    |    | R/WD   |    |
| 0h       |    |    |    | 0h      |    | 0h     |    |

**Table 5-1282. CPSW\_NC\_ECC\_AGGR\_STATUS\_CLR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                     |
|------|----------|------|-------|-------------------------------------------------|
| 31:4 | RESERVED | NONE | 0h    | Reserved                                        |
| 3:2  | TIMEOUT  | R/WD | 0h    | interrupt status clear for svbus timeout errors |
| 1:0  | PARITY   | R/WD | 0h    | interrupt status clear for parity errors        |

## 5.2 DCC

### DCC

#### 5.2.1 DCC Summaries

#### DCC Summaries

**Table 5-1283. MSS\_DCC Registers, Base Address=52B0 0000h, Length=64**

| Offset | Length | Register Name                         | DCC0 Physical Address | DCC1 Physical Address | DCC2 Physical Address |
|--------|--------|---------------------------------------|-----------------------|-----------------------|-----------------------|
| 0h     | 32     | <a href="#">MSS_DCC_DCCGCTRL</a>      | 52B0 0000h            | 52B0 1000h            | 52B0 2000h            |
| 4h     | 32     | <a href="#">MSS_DCC_DCCREV</a>        | 52B0 0004h            | 52B0 1004h            | 52B0 2004h            |
| 8h     | 32     | <a href="#">MSS_DCC_DCCCNTSEED0</a>   | 52B0 0008h            | 52B0 1008h            | 52B0 2008h            |
| Ch     | 32     | <a href="#">MSS_DCC_DCCVALIDSEED0</a> | 52B0 000Ch            | 52B0 100Ch            | 52B0 200Ch            |
| 10h    | 32     | <a href="#">MSS_DCC_DCCCNTSEED1</a>   | 52B0 0010h            | 52B0 1010h            | 52B0 2010h            |
| 14h    | 32     | <a href="#">MSS_DCC_DCCSTATUS</a>     | 52B0 0014h            | 52B0 1014h            | 52B0 2014h            |
| 18h    | 32     | <a href="#">MSS_DCC_DCCCNT0</a>       | 52B0 0018h            | 52B0 1018h            | 52B0 2018h            |
| 1Ch    | 32     | <a href="#">MSS_DCC_DCCVALID0</a>     | 52B0 001Ch            | 52B0 101Ch            | 52B0 201Ch            |
| 20h    | 32     | <a href="#">MSS_DCC_DCCCNT1</a>       | 52B0 0020h            | 52B0 1020h            | 52B0 2020h            |
| 24h    | 32     | <a href="#">MSS_DCC_DCCCLKSRC1</a>    | 52B0 0024h            | 52B0 1024h            | 52B0 2024h            |
| 28h    | 32     | <a href="#">MSS_DCC_DCCCLKSRC0</a>    | 52B0 0028h            | 52B0 1028h            | 52B0 2028h            |
| 2Ch    | 32     | <a href="#">MSS_DCC_DCCGCTRL2</a>     | 52B0 002Ch            | 52B0 102Ch            | 52B0 202Ch            |
| 30h    | 32     | <a href="#">MSS_DCC_DCCSTATUS2</a>    | 52B0 0030h            | 52B0 1030h            | 52B0 2030h            |
| 34h    | 32     | <a href="#">MSS_DCC_DCCERRCNT</a>     | 52B0 0034h            | 52B0 1034h            | 52B0 2034h            |

**Table 5-1284. MSS\_DCC Registers, Base Address=52B0 0000h, Length=64**

| Offset | Length | Register Name                         | DCC3 Physical Address |
|--------|--------|---------------------------------------|-----------------------|
| 0h     | 32     | <a href="#">MSS_DCC_DCCGCTRL</a>      | 52B0 3000h            |
| 4h     | 32     | <a href="#">MSS_DCC_DCCREV</a>        | 52B0 3004h            |
| 8h     | 32     | <a href="#">MSS_DCC_DCCCNTSEED0</a>   | 52B0 3008h            |
| Ch     | 32     | <a href="#">MSS_DCC_DCCVALIDSEED0</a> | 52B0 300Ch            |
| 10h    | 32     | <a href="#">MSS_DCC_DCCCNTSEED1</a>   | 52B0 3010h            |
| 14h    | 32     | <a href="#">MSS_DCC_DCCSTATUS</a>     | 52B0 3014h            |
| 18h    | 32     | <a href="#">MSS_DCC_DCCCNT0</a>       | 52B0 3018h            |
| 1Ch    | 32     | <a href="#">MSS_DCC_DCCVALID0</a>     | 52B0 301Ch            |
| 20h    | 32     | <a href="#">MSS_DCC_DCCCNT1</a>       | 52B0 3020h            |
| 24h    | 32     | <a href="#">MSS_DCC_DCCCLKSRC1</a>    | 52B0 3024h            |
| 28h    | 32     | <a href="#">MSS_DCC_DCCCLKSRC0</a>    | 52B0 3028h            |
| 2Ch    | 32     | <a href="#">MSS_DCC_DCCGCTRL2</a>     | 52B0 302Ch            |
| 30h    | 32     | <a href="#">MSS_DCC_DCCSTATUS2</a>    | 52B0 3030h            |
| 34h    | 32     | <a href="#">MSS_DCC_DCCERRCNT</a>     | 52B0 3034h            |

#### 5.2.2 DCC Registers

#### DCC Registers

### 5.2.2.1 MSS\_DCC\_DCCGCTRL Register

#### 1 MSS\_DCC\_DCCGCTRL Register (Offset = 0h) [reset = 5555h]

Starts / stops the counters. Clears the error signal.

Return to [Summary Table](#)

**Table 5-1285. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| DCC0          | 52B0 0000h       |
| DCC1          | 52B0 1000h       |
| DCC2          | 52B0 2000h       |
| DCC3          | 52B0 3000h       |

**Figure 5-428. MSS\_DCC\_DCCGCTRL Name Register**

|          |    |    |    |            |    |    |    |
|----------|----|----|----|------------|----|----|----|
| 31       | 30 | 29 | 28 | 27         | 26 | 25 | 24 |
| RESERVED |    |    |    |            |    |    |    |
| NONE     |    |    |    |            |    |    |    |
| 0h       |    |    |    |            |    |    |    |
| 23       | 22 | 21 | 20 | 19         | 18 | 17 | 16 |
| RESERVED |    |    |    |            |    |    |    |
| NONE     |    |    |    |            |    |    |    |
| 0h       |    |    |    |            |    |    |    |
| 15       | 14 | 13 | 12 | 11         | 10 | 9  | 8  |
| DONEENA  |    |    |    | SINGLESLOT |    |    |    |
| R/W      |    |    |    | R/W        |    |    |    |
| 5h       |    |    |    | 5h         |    |    |    |
| 7        | 6  | 5  | 4  | 3          | 2  | 1  | 0  |
| ERRENA   |    |    |    | DCCENA     |    |    |    |
| R/W      |    |    |    | R/W        |    |    |    |
| 5h       |    |    |    | 5h         |    |    |    |

**Table 5-1287. MSS\_DCC\_DCCGCTRL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 15:12 | DONEENA    | R/W  | 5h    | The DONEENA bit enables/disables the done interrupt signal, but has no effect on the done status flag in DCCSTAT register.<br>User, privilege, and debug mode (read):<br>0101= the done signal is disabled<br>others = the done signal is enabled<br>Privilege and debug mode (write):<br>0101= Disable done signal generation<br>others<br>1010 = Enable done signal generation. It is recommended to write 1010 to enable each feature to avoid single soft errors.                |
| 11:8  | SINGLESLOT | R/W  | 5h    | The SINGLESLOT bit enables/disables repetitive operation of the DCC.<br>User, privilege, and debug mode (read):<br>1010= stop counting when counter0 and valid0 both reach zero<br>1011= stop counting when counter1 reaches zero<br>others = continuously repeat (until error)<br>Privilege and debug mode (write):<br>1010= stop counting when counter0 and valid0 both reach zero<br>1011= stop counting when counter1 reaches zero<br>others = continuously repeat (until error) |

**Table 5-1287. MSS\_DCC\_DCCGCTRL Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----|--------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | ERRENA | R/W  | 5h    | The ERRENA bit enables/disables the error signal.<br>User, privilege, and debug mode (read):<br>0101= the error signal is disabled<br>others = the error signal is enabled<br>Privilege and debug mode (write):<br>0101= disable error signal generation<br>others<br>1010 = enable error signal generation. It is recommended to write 1010 to enable each feature to avoid single soft errors.                           |
| 3:0 | DCCENA | R/W  | 5h    | The DCCENA bit starts and stops the operation of the dcc.<br>User, privilege, and debug mode (read):<br>0101= counters are stopped<br>others = counters are running<br>Privilege and debug mode (write):<br>0101= stop counters and error-checking<br>others<br>1010 = load the counters with their seed values and begin counting.<br>It is recommended to write 1010 to enable each feature to avoid single soft errors. |

### 5.2.2.2 MSS\_DCC\_DCCREV Register

#### 1 MSS\_DCC\_DCCREV Register (Offset = 4h) [reset = 40010300h]

Specifies the module version.

Return to [Summary Table](#)

**Table 5-1288. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| DCC0          | 52B0 0004h       |
| DCC1          | 52B0 1004h       |
| DCC2          | 52B0 2004h       |
| DCC3          | 52B0 3004h       |

**Figure 5-429. MSS\_DCC\_DCCREV Name Register**

|        |    |          |    |       |    |    |    |
|--------|----|----------|----|-------|----|----|----|
| 31     | 30 | 29       | 28 | 27    | 26 | 25 | 24 |
| SCHEME |    | RESERVED |    | FUNC  |    |    |    |
| R      |    | NONE     |    | R     |    |    |    |
| 1h     |    | 0h       |    | 1h    |    |    |    |
| 23     | 22 | 21       | 20 | 19    | 18 | 17 | 16 |
| FUNC   |    |          |    |       |    |    |    |
| R      |    |          |    |       |    |    |    |
| 1h     |    |          |    |       |    |    |    |
| 15     | 14 | 13       | 12 | 11    | 10 | 9  | 8  |
| RTL    |    |          |    | MAJOR |    |    |    |
| R      |    |          |    | R     |    |    |    |
| 0h     |    |          |    | 3h    |    |    |    |
| 7      | 6  | 5        | 4  | 3     | 2  | 1  | 0  |
| CUSTOM |    | MINOR    |    |       |    |    |    |
| R      |    | R        |    |       |    |    |    |
| 0h     |    | 0h       |    |       |    |    |    |

**Table 5-1290. MSS\_DCC\_DCCREV Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                          |
|-------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | SCHEME   | R    | 1h    | User, privilege, and debug mode (read): Returns 01.<br>Privilege and debug mode (write): Writes have no effect.                                                                                                                                                                      |
| 29:28 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                             |
| 27:16 | FUNC     | R    | 1h    | Reflects software-compatibility. If there is no level of software compatibility, a unique func number is assigned; for compatible modules, the same number is maintained.<br>User, privilege, and debug mode (read): 0x0<br>Privilege and debug mode (write): Writes have no effect. |
| 15:11 | RTL      | R    | 0h    | Incremented for releases due to spec changes or post-release design changes. Reset to 0 when either MAJOR or MINOR is incremented.<br>User, privilege, and debug mode (read): 0x0<br>Privilege and debug mode (write): Writes have no effect.                                        |
| 10:8  | MAJOR    | R    | 3h    | Represents major changes to the module (e.g. entirely new features are added/changed). The major revision number for this module.<br>User, privilege, and debug mode (read): 0x2<br>Privilege and debug mode (write): Writes have no effect.                                         |

**Table 5-1290. MSS\_DCC\_DCCREV Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                                                            |
|-----|--------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | CUSTOM | R    | 0h    | Indicates a special version of the module. May not be supported by standard software.<br>User, privilege, and debug mode (read): 0x0<br>Privilege and debug mode (write): Writes have no effect.                                       |
| 5:0 | MINOR  | R    | 0h    | Represents minor changes to the module (e.g. enhancements to existing features). The minor revision number for this module.<br>User, privilege, and debug mode (read): 0x4<br>Privilege and debug mode (write): Writes have no effect. |



### 5.2.2.3 MSS\_DCC\_DCCNTSEED0 Register

#### 1 MSS\_DCC\_DCCNTSEED0 Register (Offset = 8h) [reset = 0h]

Seed value for the counter attached to clock source 0

Return to [Summary Table](#)

**Table 5-1291. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| DCC0          | 52B0 0008h       |
| DCC1          | 52B0 1008h       |
| DCC2          | 52B0 2008h       |
| DCC3          | 52B0 3008h       |

**Figure 5-430. MSS\_DCC\_DCCNTSEED0 Name Register**

|            |    |    |    |            |    |    |    |
|------------|----|----|----|------------|----|----|----|
| 31         | 30 | 29 | 28 | 27         | 26 | 25 | 24 |
| RESERVED   |    |    |    |            |    |    |    |
| NONE       |    |    |    |            |    |    |    |
| 0h         |    |    |    |            |    |    |    |
| 23         | 22 | 21 | 20 | 19         | 18 | 17 | 16 |
| RESERVED   |    |    |    | COUNTSEED0 |    |    |    |
| NONE       |    |    |    | R/W        |    |    |    |
| 0h         |    |    |    | 0h         |    |    |    |
| 15         | 14 | 13 | 12 | 11         | 10 | 9  | 8  |
| COUNTSEED0 |    |    |    |            |    |    |    |
| R/W        |    |    |    |            |    |    |    |
| 0h         |    |    |    |            |    |    |    |
| 7          | 6  | 5  | 4  | 3          | 2  | 1  | 0  |
| COUNTSEED0 |    |    |    |            |    |    |    |
| R/W        |    |    |    |            |    |    |    |
| 0h         |    |    |    |            |    |    |    |

**Table 5-1293. MSS\_DCC\_DCCNTSEED0 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                          |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                             |
| 19:0  | COUNTSEED0 | R/W  | 0h    | This field contains the seed value that gets loaded into counter 0 (clock source 0).<br>User, privilege, and debug mode (read):<br>Returns the current seed value for counter 0.<br>Privilege and debug mode (write):<br>Sets the current seed value for counter 0.<br>NOTE: Operating the DCC with 0 in the COUNTSEED0 register will result in undefined operation. |

### 5.2.2.4 MSS\_DCC\_DCCVALIDSEED0 Register

#### 1 MSS\_DCC\_DCCVALIDSEED0 Register (Offset = Ch) [reset = 0h]

Seed value for the timeout counter attached to clock source 0.

Return to [Summary Table](#)

**Table 5-1294. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| DCC0          | 52B0 000Ch       |
| DCC1          | 52B0 100Ch       |
| DCC2          | 52B0 200Ch       |
| DCC3          | 52B0 300Ch       |

**Figure 5-431. MSS\_DCC\_DCCVALIDSEED0 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| VALIDSEED0 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| VALIDSEED0 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-1296. MSS\_DCC\_DCCVALIDSEED0 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 15:0  | VALIDSEED0 | R/W  | 0h    | <p>This field contains the seed value that gets loaded into the valid duration counter for clock source 0.</p> <p>User, privilege, and debug mode (read):<br/>Returns the current seed value for VALID0.</p> <p>Privilege and debug mode (write):<br/>Sets the current seed value for VALID0.</p> <p>NOTE: Operating the DCC with 0 in the VALIDSEED0 register will result in undefined operation. VALID0 defines a window in which COUNT1 expires. This window is meant to be at least four cycles wide. Do not program a value less than 4 into the VALID0 register.</p> |

### 5.2.2.5 MSS\_DCC\_DCCNTSEED1 Register

#### 1 MSS\_DCC\_DCCNTSEED1 Register (Offset = 10h) [reset = 0h]

Seed value for the counter attached to clock source 1.

Return to [Summary Table](#)

**Table 5-1297. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| DCC0          | 52B0 0010h       |
| DCC1          | 52B0 1010h       |
| DCC2          | 52B0 2010h       |
| DCC3          | 52B0 3010h       |

**Figure 5-432. MSS\_DCC\_DCCNTSEED1 Name Register**

|            |    |    |    |            |    |    |    |
|------------|----|----|----|------------|----|----|----|
| 31         | 30 | 29 | 28 | 27         | 26 | 25 | 24 |
| RESERVED   |    |    |    |            |    |    |    |
| NONE       |    |    |    |            |    |    |    |
| 0h         |    |    |    |            |    |    |    |
| 23         | 22 | 21 | 20 | 19         | 18 | 17 | 16 |
| RESERVED   |    |    |    | COUNTSEED1 |    |    |    |
| NONE       |    |    |    | R/W        |    |    |    |
| 0h         |    |    |    | 0h         |    |    |    |
| 15         | 14 | 13 | 12 | 11         | 10 | 9  | 8  |
| COUNTSEED1 |    |    |    |            |    |    |    |
| R/W        |    |    |    |            |    |    |    |
| 0h         |    |    |    |            |    |    |    |
| 7          | 6  | 5  | 4  | 3          | 2  | 1  | 0  |
| COUNTSEED1 |    |    |    |            |    |    |    |
| R/W        |    |    |    |            |    |    |    |
| 0h         |    |    |    |            |    |    |    |

**Table 5-1299. MSS\_DCC\_DCCNTSEED1 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                          |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                             |
| 19:0  | COUNTSEED1 | R/W  | 0h    | This field contains the seed value that gets loaded into counter 1 (clock source 1).<br>User, privilege, and debug mode (read):<br>Returns the current seed value for counter 1.<br>Privilege and debug mode (write):<br>Sets the current seed value for counter 1.<br>NOTE: Operating the DCC with 0 in the COUNTSEED1 register will result in undefined operation. |

### 5.2.2.6 MSS\_DCC\_DCCSTATUS Register

#### 1 MSS\_DCC\_DCCSTATUS Register (Offset = 14h) [reset = 0h]

Specifies the status of the DCC Module.

Return to [Summary Table](#)

**Table 5-1300. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| DCC0          | 52B0 0014h       |
| DCC1          | 52B0 1014h       |
| DCC2          | 52B0 2014h       |
| DCC3          | 52B0 3014h       |

**Figure 5-433. MSS\_DCC\_DCCSTATUS Name Register**

|          |    |    |    |    |    |         |        |
|----------|----|----|----|----|----|---------|--------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25      | 24     |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 23       | 22 | 21 | 20 | 19 | 18 | 17      | 16     |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 15       | 14 | 13 | 12 | 11 | 10 | 9       | 8      |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 7        | 6  | 5  | 4  | 3  | 2  | 1       | 0      |
| RESERVED |    |    |    |    |    | DONEFLG | ERRFLG |
| NONE     |    |    |    |    |    | R/W1TC  | R/W1TC |
| 0h       |    |    |    |    |    | 0h      | 0h     |

**Table 5-1302. MSS\_DCC\_DCCSTATUS Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description                                                                                                                                                                                                                                                                                         |
|------|----------|--------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED | NONE   | 0h    | Reserved                                                                                                                                                                                                                                                                                            |
| 1    | DONEFLG  | R/W1TC | 0h    | Indicates when single-shot mode is complete without error. Writing a 1 to this bit clears the flag.<br>User, privilege, and debug mode (read):<br>0 = single-shot mode is not done<br>1 = single-shot mode is done<br>Privilege and debug mode (write):<br>0 = no effect<br>1 = clear the done flag |
| 0    | ERRFLG   | R/W1TC | 0h    | Indicates whether or not an error has occurred. Writing a 1 to this bit clears the flag.<br>User, privilege, and debug mode (read):<br>0 = an error has not occurred<br>1 = an error has occurred<br>Privilege and debug mode (write):<br>0 = no effect<br>1 = clear the error flag                 |

### 5.2.2.7 MSS\_DCC\_DCCCNT0 Register

#### 1 MSS\_DCC\_DCCCNT0 Register (Offset = 18h) [reset = 0h]

Value of the counter attached to clock source 0.

Return to [Summary Table](#)

**Table 5-1303. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| DCC0          | 52B0 0018h       |
| DCC1          | 52B0 1018h       |
| DCC2          | 52B0 2018h       |
| DCC3          | 52B0 3018h       |

**Figure 5-434. MSS\_DCC\_DCCCNT0 Name Register**

|          |    |    |    |        |    |    |    |
|----------|----|----|----|--------|----|----|----|
| 31       | 30 | 29 | 28 | 27     | 26 | 25 | 24 |
| RESERVED |    |    |    |        |    |    |    |
| NONE     |    |    |    |        |    |    |    |
| 0h       |    |    |    |        |    |    |    |
| 23       | 22 | 21 | 20 | 19     | 18 | 17 | 16 |
| RESERVED |    |    |    | COUNT0 |    |    |    |
| NONE     |    |    |    | R      |    |    |    |
| 0h       |    |    |    | 0h     |    |    |    |
| 15       | 14 | 13 | 12 | 11     | 10 | 9  | 8  |
| COUNT0   |    |    |    |        |    |    |    |
| R        |    |    |    |        |    |    |    |
| 0h       |    |    |    |        |    |    |    |
| 7        | 6  | 5  | 4  | 3      | 2  | 1  | 0  |
| COUNT0   |    |    |    |        |    |    |    |
| R        |    |    |    |        |    |    |    |
| 0h       |    |    |    |        |    |    |    |

**Table 5-1305. MSS\_DCC\_DCCCNT0 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                         |
| 19:0  | COUNT0   | R    | 0h    | This field contains the current value of counter 0.<br>User, privilege, and debug mode (read):<br>Returns either the current value of Count 0 or the Count 0 FIFO location, depending upon DCCGCTRL2.FIFO_READ.<br>Privilege and debug mode (write):<br>Writes have no effect.<br>NOTE - Reads of the counter value may not be exact since the read operation is synchronized to the vbus clock. |

### 5.2.2.8 MSS\_DCC\_DCCVALID0 Register

#### 1 MSS\_DCC\_DCCVALID0 Register (Offset = 1Ch) [reset = 0h]

Value of the valid counter attached to clock source 0.

Return to [Summary Table](#)

**Table 5-1306. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| DCC0          | 52B0 001Ch       |
| DCC1          | 52B0 101Ch       |
| DCC2          | 52B0 201Ch       |
| DCC3          | 52B0 301Ch       |

**Figure 5-435. MSS\_DCC\_DCCVALID0 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| VALID0   |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| VALID0   |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-1308. MSS\_DCC\_DCCVALID0 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                              |
| 15:0  | VALID0   | R    | 0h    | This field contains the current value of valid counter 0.<br>User, privilege, and debug mode (read):<br>Returns either the current value of Valid 0 or the Valid 0 FIFO location depending upon DCCGCTRL2.FIFO_READ.<br>Privilege and debug mode (write):<br>writes have no effect.<br>NOTE - Reads of the counter value may not be exact since the read operation is synchronized to the vbus clock. |

### 5.2.2.9 MSS\_DCC\_DCCCNT1 Register

#### 1 MSS\_DCC\_DCCCNT1 Register (Offset = 20h) [reset = 0h]

Value of the counter attached to clock source 1.

Return to [Summary Table](#)

**Table 5-1309. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| DCC0          | 52B0 0020h       |
| DCC1          | 52B0 1020h       |
| DCC2          | 52B0 2020h       |
| DCC3          | 52B0 3020h       |

**Figure 5-436. MSS\_DCC\_DCCCNT1 Name Register**

|          |    |    |    |        |    |    |    |
|----------|----|----|----|--------|----|----|----|
| 31       | 30 | 29 | 28 | 27     | 26 | 25 | 24 |
| RESERVED |    |    |    |        |    |    |    |
| NONE     |    |    |    |        |    |    |    |
| 0h       |    |    |    |        |    |    |    |
| 23       | 22 | 21 | 20 | 19     | 18 | 17 | 16 |
| RESERVED |    |    |    | COUNT1 |    |    |    |
| NONE     |    |    |    | R      |    |    |    |
| 0h       |    |    |    | 0h     |    |    |    |
| 15       | 14 | 13 | 12 | 11     | 10 | 9  | 8  |
| COUNT1   |    |    |    |        |    |    |    |
| R        |    |    |    |        |    |    |    |
| 0h       |    |    |    |        |    |    |    |
| 7        | 6  | 5  | 4  | 3      | 2  | 1  | 0  |
| COUNT1   |    |    |    |        |    |    |    |
| R        |    |    |    |        |    |    |    |
| 0h       |    |    |    |        |    |    |    |

**Table 5-1311. MSS\_DCC\_DCCCNT1 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                          |
| 19:0  | COUNT1   | R    | 0h    | This field contains the current value of counter 1.<br>User, privilege, and debug mode (read):<br>Returns either the current value of Count 1 or the Count 1 FIFO location depending upon DCCGCTRL2.FIFO_READ 1.<br>Privilege and debug mode (write):<br>writes have no effect.<br>NOTE - Reads of the counter value may not be exact since the read operation is synchronized to the vbus clock. |

### 5.2.2.10 MSS\_DCC\_DCCCLKSRC1 Register

#### 1 MSS\_DCC\_DCCCLKSRC1 Register (Offset = 24h) [reset = 0h]

Selects the clock source for counter 1.

Return to [Summary Table](#)

**Table 5-1312. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| DCC0          | 52B0 0024h       |
| DCC1          | 52B0 1024h       |
| DCC2          | 52B0 2024h       |
| DCC3          | 52B0 3024h       |

**Figure 5-437. MSS\_DCC\_DCCCLKSRC1 Name Register**

|          |    |    |    |          |    |    |    |
|----------|----|----|----|----------|----|----|----|
| 31       | 30 | 29 | 28 | 27       | 26 | 25 | 24 |
| RESERVED |    |    |    |          |    |    |    |
| NONE     |    |    |    |          |    |    |    |
| 0h       |    |    |    |          |    |    |    |
| 23       | 22 | 21 | 20 | 19       | 18 | 17 | 16 |
| RESERVED |    |    |    |          |    |    |    |
| NONE     |    |    |    |          |    |    |    |
| 0h       |    |    |    |          |    |    |    |
| 15       | 14 | 13 | 12 | 11       | 10 | 9  | 8  |
| KEY      |    |    |    | RESERVED |    |    |    |
| R/W      |    |    |    | NONE     |    |    |    |
| 0h       |    |    |    | 0h       |    |    |    |
| 7        | 6  | 5  | 4  | 3        | 2  | 1  | 0  |
| RESERVED |    |    |    | CLKSRC1  |    |    |    |
| NONE     |    |    |    | R/W      |    |    |    |
| 0h       |    |    |    | 0h       |    |    |    |

**Table 5-1314. MSS\_DCC\_DCCCLKSRC1 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                         |
|-------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                            |
| 15:12 | KEY      | R/W  | 0h    | This field enables or disables clock source selection for counter 1.<br>User, privilege, and debug mode (read):<br>Returns the current value of the key.<br>Privilege and debug mode (write):<br>Sets the key value.<br>Key values:<br>1010 The CLKSRC field selects the clock source for counter 1.<br>others: Clock source selection is disabled. |
| 11:5  | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                            |



**Table 5-1314. MSS\_DCC\_DCCCLKSRC1 Register Field Descriptions (continued)**

| Bit | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-----|---------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4:0 | CLKSRC1 | R/W  | 0h    | <p>This field specifies the clock source for counter 1, when the KEY field enables this feature.</p> <p>User, privilege, and debug mode (read):<br/>Returns the current value of CLKSRC1.</p> <p>Privilege and debug mode (write):<br/>Sets the value of CLKSRC1.</p> <p>0000 Clk source 0 is selected for COUNT1<br/> 0001 Clk source 1 is selected for COUNT1<br/> 0010 Clk source 2 is selected for COUNT1<br/> 0011 Clk source 3 is selected for COUNT1<br/> 0100 Clk source 4 is selected for COUNT1<br/> 0101 Clk source 5 is selected for COUNT1<br/> 0110 Clk source 6 is selected for COUNT1<br/> 0111 Clk source 7 is selected for COUNT1<br/> 1000- VCLK is selected for COUNT1<br/> 1111</p> |

### 5.2.2.11 MSS\_DCC\_DCCCLKSRC0 Register

#### 1 MSS\_DCC\_DCCCLKSRC0 Register (Offset = 28h) [reset = 0h]

Selects the clock source for counter 0.

Return to [Summary Table](#)

**Table 5-1315. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| DCC0          | 52B0 0028h       |
| DCC1          | 52B0 1028h       |
| DCC2          | 52B0 2028h       |
| DCC3          | 52B0 3028h       |

**Figure 5-438. MSS\_DCC\_DCCCLKSRC0 Name Register**

|          |    |    |    |          |    |    |    |
|----------|----|----|----|----------|----|----|----|
| 31       | 30 | 29 | 28 | 27       | 26 | 25 | 24 |
| RESERVED |    |    |    |          |    |    |    |
| NONE     |    |    |    |          |    |    |    |
| 0h       |    |    |    |          |    |    |    |
| 23       | 22 | 21 | 20 | 19       | 18 | 17 | 16 |
| RESERVED |    |    |    |          |    |    |    |
| NONE     |    |    |    |          |    |    |    |
| 0h       |    |    |    |          |    |    |    |
| 15       | 14 | 13 | 12 | 11       | 10 | 9  | 8  |
| KEY      |    |    |    | RESERVED |    |    |    |
| R/W      |    |    |    | NONE     |    |    |    |
| 0h       |    |    |    | 0h       |    |    |    |
| 7        | 6  | 5  | 4  | 3        | 2  | 1  | 0  |
| RESERVED |    |    |    | CLKSRC0  |    |    |    |
| NONE     |    |    |    | R/W      |    |    |    |
| 0h       |    |    |    | 0h       |    |    |    |

**Table 5-1317. MSS\_DCC\_DCCCLKSRC0 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                         |
|-------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                            |
| 15:12 | KEY      | R/W  | 0h    | This field enables or disables clock source selection for counter 0.<br>User, privilege, and debug mode (read):<br>Returns the current value of the key.<br>Privilege and debug mode (write):<br>Sets the key value.<br>Key values:<br>1010 The CLKSRC field selects the clock source for counter 0.<br>others: Clock source selection is disabled. |
| 11:4  | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                            |

**Table 5-1317. MSS\_DCC\_DCCCLKSRC0 Register Field Descriptions (continued)**

| Bit | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-----|---------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0 | CLKSRC0 | R/W  | 0h    | <p>This field specifies the clock source for counter 0, when the KEY field enables this feature.</p> <p>User, privilege, and debug mode (read):<br/>Returns the current value of CLKSRC0.</p> <p>Privilege and debug mode (write):<br/>Sets the value of CLKSRC0.</p> <p>0000 Clock0[0] is selected as source for COUNT0<br/> 0001 Clock0[1] is selected as source for COUNT0<br/> 0010 Clock0[2] is selected as source for COUNT0<br/> other VCLK is selected as source for COUNT0<br/> value<br/> s</p> |

### 5.2.2.12 MSS\_DCC\_DCCGCTRL2 Register

#### 1 MSS\_DCC\_DCCGCTRL2 Register (Offset = 2Ch) [reset = 555h]

Allows configuring different modes of operation for DCC.

Return to [Summary Table](#)

**Table 5-1318. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| DCC0          | 52B0 002Ch       |
| DCC1          | 52B0 102Ch       |
| DCC2          | 52B0 202Ch       |
| DCC3          | 52B0 302Ch       |

**Figure 5-439. MSS\_DCC\_DCCGCTRL2 Name Register**

|           |    |    |    |             |    |    |    |
|-----------|----|----|----|-------------|----|----|----|
| 31        | 30 | 29 | 28 | 27          | 26 | 25 | 24 |
| RESERVED  |    |    |    |             |    |    |    |
| NONE      |    |    |    |             |    |    |    |
| 0h        |    |    |    |             |    |    |    |
| 23        | 22 | 21 | 20 | 19          | 18 | 17 | 16 |
| RESERVED  |    |    |    |             |    |    |    |
| NONE      |    |    |    |             |    |    |    |
| 0h        |    |    |    |             |    |    |    |
| 15        | 14 | 13 | 12 | 11          | 10 | 9  | 8  |
| RESERVED  |    |    |    | FIFO_NONERR |    |    |    |
| NONE      |    |    |    | R/W         |    |    |    |
| 0h        |    |    |    | 5h          |    |    |    |
| 7         | 6  | 5  | 4  | 3           | 2  | 1  | 0  |
| FIFO_READ |    |    |    | CONT_ON_ERR |    |    |    |
| R/W       |    |    |    | R/W         |    |    |    |
| 5h        |    |    |    | 5h          |    |    |    |

**Table 5-1320. MSS\_DCC\_DCCGCTRL2 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|-------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED    | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 11:8  | FIFO_NONERR | R/W  | 5h    | Enables/disables FIFO writes without the error event on completion of comparison window.<br>User, privilege, and debug mode (read):<br>Returns the current field value.<br>Privilege and debug mode (write):<br>Sets the value of field value.<br>Source values:<br>0101 Counter values are captured to non-full FIFO only upon Error event.<br>Others<br>1010 : Write counter values to non-full FIFO upon completion of comparison window regardless of error or not. It is recommended to write 1010 to avoid single soft errors. |

**Table 5-1320. MSS\_DCC\_DCCGCTRL2 Register Field Descriptions (continued)**

| Bit | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-----|-------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | FIFO_READ   | R/W  | 5h    | <p>Enables the counter read registers reflect FIFO output instead of the live counter value.</p> <p>User, privilege, and debug mode (read):<br/>Returns the current field value.</p> <p>Privilege and debug mode (write):<br/>Sets the value of field value.</p> <p>Source values:<br/>0101 Counter value is read directly.<br/>Others<br/>1010 : Counters FIFO output is read. It is recommended to write 1010 to avoid single soft errors.</p>                                                                            |
| 3:0 | CONT_ON_ERR | R/W  | 5h    | <p>Continues to next window of comparison despite the error condition.</p> <p>User, privilege, and debug mode (read):<br/>Returns the current field value.</p> <p>Privilege and debug mode (write):<br/>Sets the value of field value.</p> <p>Enable values:<br/>0101 Comparison and counter reload is stopped from advancing if error is detected.<br/>Others<br/>1010:Counters get reloaded with seed and continue counting despite the error condition. It is recommended to write 1010 to avoid single soft errors.</p> |

### 5.2.2.13 MSS\_DCC\_DCCSTATUS2 Register

#### 1 MSS\_DCC\_DCCSTATUS2 Register (Offset = 30h) [reset = 7h]

Specifies the status of the DCC FIFOs.

Return to [Summary Table](#)

**Table 5-1321. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| DCC0          | 52B0 0030h       |
| DCC1          | 52B0 1030h       |
| DCC2          | 52B0 2030h       |
| DCC3          | 52B0 3030h       |

**Figure 5-440. MSS\_DCC\_DCCSTATUS2 Name Register**

|          |                  |                  |                  |                   |                   |                   |    |
|----------|------------------|------------------|------------------|-------------------|-------------------|-------------------|----|
| 31       | 30               | 29               | 28               | 27                | 26                | 25                | 24 |
| RESERVED |                  |                  |                  |                   |                   |                   |    |
| NONE     |                  |                  |                  |                   |                   |                   |    |
| 0h       |                  |                  |                  |                   |                   |                   |    |
| 23       | 22               | 21               | 20               | 19                | 18                | 17                | 16 |
| RESERVED |                  |                  |                  |                   |                   |                   |    |
| NONE     |                  |                  |                  |                   |                   |                   |    |
| 0h       |                  |                  |                  |                   |                   |                   |    |
| 15       | 14               | 13               | 12               | 11                | 10                | 9                 | 8  |
| RESERVED |                  |                  |                  |                   |                   |                   |    |
| NONE     |                  |                  |                  |                   |                   |                   |    |
| 0h       |                  |                  |                  |                   |                   |                   |    |
| 7        | 6                | 5                | 4                | 3                 | 2                 | 1                 | 0  |
| RESERVED | COUNT1_FIFO_FULL | VALID0_FIFO_FULL | COUNT0_FIFO_FULL | COUNT1_FIFO_EMPTY | VALID0_FIFO_EMPTY | COUNT0_FIFO_EMPTY |    |
| NONE     | R                | R                | R                | R                 | R                 | R                 | R  |
| 0h       | 0h               | 0h               | 0h               | 0h                | 1h                | 1h                | 1h |

**Table 5-1323. MSS\_DCC\_DCCSTATUS2 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                                                                            |
|------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:6 | RESERVED         | NONE | 0h    | Reserved                                                                                                                                                                                                               |
| 5    | COUNT1_FIFO_FULL | R    | 0h    | Count1 FIFO Full. Indicates whether Count1 FIFO is full.<br>User, privilege, and debug mode (read):<br>0:Count1 FIFO is not full<br>1:Count1 FIFO is full.<br>Privilege and debug mode (write): Writes have no effect. |
| 4    | VALID0_FIFO_FULL | R    | 0h    | Valid0 FIFO Full. Indicates whether Valid0 FIFO is full.<br>User, privilege, and debug mode (read):<br>0:Valid0 FIFO is not full<br>1:Valid0 FIFO is full.<br>Privilege and debug mode (write): Writes have no effect. |
| 3    | COUNT0_FIFO_FULL | R    | 0h    | Count0 FIFO Full. Indicates whether Count0 FIFO is full.<br>User, privilege, and debug mode (read):<br>0:Count0 FIFO is not full<br>1:Count0 FIFO is full.<br>Privilege and debug mode (write): Writes have no effect. |

**Table 5-1323. MSS\_DCC\_DCCSTATUS2 Register Field Descriptions (continued)**

| Bit | Field             | Type | Reset | Description                                                                                                                                                                                                                |
|-----|-------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | COUNT1_FIFO_EMPTY | R    | 1h    | Count1 FIFO Empty. Indicates whether Count1 FIFO is empty.<br>User, privilege, and debug mode (read):<br>0:Count1 FIFO is not empty<br>1:Count1 FIFO is empty.<br>Privilege and debug mode (write): Writes have no effect. |
| 1   | VALID0_FIFO_EMPTY | R    | 1h    | Valid0 FIFO Empty. Indicates whether Valid0 FIFO is empty.<br>User, privilege, and debug mode (read):<br>0:Valid0 FIFO is not empty<br>1:Valid0 FIFO is empty.<br>Privilege and debug mode (write): Writes have no effect. |
| 0   | COUNT0_FIFO_EMPTY | R    | 1h    | Count0 FIFO Empty. Indicates whether Count0 FIFO is empty.<br>User, privilege, and debug mode (read):<br>0:Count0 FIFO is not empty<br>1:Count0 FIFO is empty.<br>Privilege and debug mode (write): Writes have no effect. |

### 5.2.2.14 MSS\_DCC\_DCCERRCNT Register

#### 1 MSS\_DCC\_DCCERRCNT Register (Offset = 34h) [reset = 0h]

Counts number of errors since last clear.

Return to [Summary Table](#)

**Table 5-1324. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| DCC0          | 52B0 0034h       |
| DCC1          | 52B0 1034h       |
| DCC2          | 52B0 2034h       |
| DCC3          | 52B0 3034h       |

**Figure 5-441. MSS\_DCC\_DCCERRCNT Name Register**

|          |    |    |    |    |    |        |    |
|----------|----|----|----|----|----|--------|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25     | 24 |
| RESERVED |    |    |    |    |    |        |    |
| NONE     |    |    |    |    |    |        |    |
| 0h       |    |    |    |    |    |        |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17     | 16 |
| RESERVED |    |    |    |    |    |        |    |
| NONE     |    |    |    |    |    |        |    |
| 0h       |    |    |    |    |    |        |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9      | 8  |
| RESERVED |    |    |    |    |    | ERRCNT |    |
| NONE     |    |    |    |    |    | R/W    |    |
| 0h       |    |    |    |    |    | 0h     |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1      | 0  |
| ERRCNT   |    |    |    |    |    |        |    |
| R/W      |    |    |    |    |    |        |    |
| 0h       |    |    |    |    |    |        |    |

**Table 5-1326. MSS\_DCC\_DCCERRCNT Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                      |
|-------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | RESERVED | NONE | 0h    | Reserved                                                                                                                                         |
| 9:0   | ERRCNT   | R/W  | 0h    | Counts the number of errors after the last write to this register or reset. If reached terminal count the count freezes. User needs to clear it. |



## 5.3 ECC\_AGGR

### ECC\_AGGR

#### 5.3.1 ECC\_AGGR Summaries

#### ECC\_AGGR Summaries

**Table 5-1327. ECC\_AGGR Registers, Base Address=5301 0000h, Length=1024**

| Offset | Length | Register Name                                | ECC_AGGR Physical Address |
|--------|--------|----------------------------------------------|---------------------------|
| 0h     | 32     | <a href="#">ECC_AGGR_AGGR_REVISION</a>       | 5301 0000h                |
| 8h     | 32     | <a href="#">ECC_AGGR_ECC_VECTOR</a>          | 5301 0008h                |
| Ch     | 32     | <a href="#">ECC_AGGR_MISC_STATUS</a>         | 5301 000Ch                |
| 10h    | 32     | <a href="#">ECC_AGGR_ECC_WRAP_REVISION</a>   | 5301 0010h                |
| 14h    | 32     | <a href="#">ECC_AGGR_CONTROL</a>             | 5301 0014h                |
| 18h    | 32     | <a href="#">ECC_AGGR_ERROR_CTRL1</a>         | 5301 0018h                |
| 1Ch    | 32     | <a href="#">ECC_AGGR_ERROR_CTRL2</a>         | 5301 001Ch                |
| 20h    | 32     | <a href="#">ECC_AGGR_ERROR_STATUS1</a>       | 5301 0020h                |
| 24h    | 32     | <a href="#">ECC_AGGR_ERROR_STATUS2</a>       | 5301 0024h                |
| 28h    | 32     | <a href="#">ECC_AGGR_ERROR_STATUS3</a>       | 5301 0028h                |
| 3Ch    | 32     | <a href="#">ECC_AGGR_SEC_EOI_REG</a>         | 5301 003Ch                |
| 40h    | 32     | <a href="#">ECC_AGGR_SEC_STATUS_REG0</a>     | 5301 0040h                |
| 80h    | 32     | <a href="#">ECC_AGGR_SEC_ENABLE_SET_REG0</a> | 5301 0080h                |
| C0h    | 32     | <a href="#">ECC_AGGR_SEC_ENABLE_CLR_REG0</a> | 5301 00C0h                |
| 13Ch   | 32     | <a href="#">ECC_AGGR_DED_EOI_REG</a>         | 5301 013Ch                |
| 140h   | 32     | <a href="#">ECC_AGGR_DED_STATUS_REG0</a>     | 5301 0140h                |
| 180h   | 32     | <a href="#">ECC_AGGR_DED_ENABLE_SET_REG0</a> | 5301 0180h                |
| 1C0h   | 32     | <a href="#">ECC_AGGR_DED_ENABLE_CLR_REG0</a> | 5301 01C0h                |
| 200h   | 32     | <a href="#">ECC_AGGR_AGGR_ENABLE_SET</a>     | 5301 0200h                |
| 204h   | 32     | <a href="#">ECC_AGGR_AGGR_ENABLE_CLR</a>     | 5301 0204h                |
| 208h   | 32     | <a href="#">ECC_AGGR_AGGR_STATUS_SET</a>     | 5301 0208h                |
| 20Ch   | 32     | <a href="#">ECC_AGGR_AGGR_STATUS_CLR</a>     | 5301 020Ch                |

#### 5.3.2 ECC\_AGGR Registers

#### ECC\_AGGR Registers

### 5.3.2.1 ECC\_AGGR\_AGGR\_REVISION Register

#### 1 ECC\_AGGR\_AGGR\_REVISION Register (Offset = 0h) [reset = 66A0C200h]

The Revision Register contains the major and minor revisions for the ECC aggregator module. It does not support byte accesses.

Return to [Summary Table](#)

**Table 5-1328. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECC_AGGR      | 5301 0000h       |

**Figure 5-442. ECC\_AGGR\_AGGR\_REVISION Name Register**

|           |    |        |    |           |        |    |    |
|-----------|----|--------|----|-----------|--------|----|----|
| 31        | 30 | 29     | 28 | 27        | 26     | 25 | 24 |
| SCHEME    |    | BU     |    | MODULE_ID |        |    |    |
| R         |    | R      |    | R         |        |    |    |
| 1h        |    | 2h     |    | 6A0h      |        |    |    |
| 23        | 22 | 21     | 20 | 19        | 18     | 17 | 16 |
| MODULE_ID |    |        |    |           |        |    |    |
| R         |    |        |    |           |        |    |    |
| 6A0h      |    |        |    |           |        |    |    |
| 15        | 14 | 13     | 12 | 11        | 10     | 9  | 8  |
| REVRTL    |    |        |    |           | REVMAJ |    |    |
| R         |    |        |    |           | R      |    |    |
| 18h       |    |        |    |           | 2h     |    |    |
| 7         | 6  | 5      | 4  | 3         | 2      | 1  | 0  |
| CUSTOM    |    | REVMIN |    |           |        |    |    |
| R         |    | R      |    |           |        |    |    |
| 0h        |    | 0h     |    |           |        |    |    |

**Table 5-1330. ECC\_AGGR\_AGGR\_REVISION Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description    |
|-------|-----------|------|-------|----------------|
| 31:30 | SCHEME    | R    | 1h    | Scheme         |
| 29:28 | BU        | R    | 2h    | Business unit  |
| 27:16 | MODULE_ID | R    | 6A0h  | Module ID      |
| 15:11 | REVRTL    | R    | 18h   | RTL version    |
| 10:8  | REVMAJ    | R    | 2h    | Major version  |
| 7:6   | CUSTOM    | R    | 0h    | Custom version |
| 5:0   | REVMIN    | R    | 0h    | Minor version  |

### 5.3.2.2 ECC\_AGGR\_ECC\_VECTOR Register

#### 1 ECC\_AGGR\_ECC\_VECTOR Register (Offset = 8h) [reset = 0h]

ECC RAM ID to select which ECC RAM to control or read status from.

Return to [Summary Table](#)

**Table 5-1331. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECC_AGGR      | 5301 0008h       |

**Figure 5-443. ECC\_AGGR\_ECC\_VECTOR Name Register**

| 31               | 30       | 29 | 28 | 27 | 26         | 25 | 24            |
|------------------|----------|----|----|----|------------|----|---------------|
| RESERVED         |          |    |    |    |            |    | RD_SVBUS_DONE |
| NONE             |          |    |    |    |            |    | R             |
| 0h               |          |    |    |    |            |    | 0h            |
| 23               | 22       | 21 | 20 | 19 | 18         | 17 | 16            |
| RD_SVBUS_ADDRESS |          |    |    |    |            |    |               |
| R/W              |          |    |    |    |            |    |               |
| 0h               |          |    |    |    |            |    |               |
| 15               | 14       | 13 | 12 | 11 | 10         | 9  | 8             |
| RD_SVBUS         | RESERVED |    |    |    | ECC_VECTOR |    |               |
| R/W1TS           | NONE     |    |    |    | R/W        |    |               |
| 0h               | 0h       |    |    |    | 0h         |    |               |
| 7                | 6        | 5  | 4  | 3  | 2          | 1  | 0             |
| ECC_VECTOR       |          |    |    |    |            |    |               |
| R/W              |          |    |    |    |            |    |               |
| 0h               |          |    |    |    |            |    |               |

**Table 5-1333. ECC\_AGGR\_ECC\_VECTOR Register Field Descriptions**

| Bit   | Field            | Type   | Reset | Description                                                                                                                                                                                  |
|-------|------------------|--------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:25 | RESERVED         | NONE   | 0h    | Reserved                                                                                                                                                                                     |
| 24    | RD_SVBUS_DONE    | R      | 0h    | Status to indicate if read on serial bus is complete                                                                                                                                         |
| 23:16 | RD_SVBUS_ADDRESS | R/W    | 0h    | Read address                                                                                                                                                                                 |
| 15    | RD_SVBUS         | R/W1TS | 0h    | Trigger a read operation to the specified read address that requires a serial bus access. In normal operation, the trigger bit is only '1' for a single cycle and thus can not be read back. |
| 14:11 | RESERVED         | NONE   | 0h    | Reserved                                                                                                                                                                                     |
| 10:0  | ECC_VECTOR       | R/W    | 0h    | Value written to select the corresponding ECC RAM for control or status                                                                                                                      |

### 5.3.2.3 ECC\_AGGR\_MISC\_STATUS Register

#### 1 ECC\_AGGR\_MISC\_STATUS Register (Offset = Ch) [reset = 1Ch]

Contains misc status such as number of ECC RAMs serviced by the ECC aggregator.

Return to [Summary Table](#)

**Table 5-1334. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECC_AGGR      | 5301 000Ch       |

**Figure 5-444. ECC\_AGGR\_MISC\_STATUS Name Register**

|          |    |    |    |    |          |    |    |
|----------|----|----|----|----|----------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26       | 25 | 24 |
| RESERVED |    |    |    |    |          |    |    |
| NONE     |    |    |    |    |          |    |    |
| 0h       |    |    |    |    |          |    |    |
| 23       | 22 | 21 | 20 | 19 | 18       | 17 | 16 |
| RESERVED |    |    |    |    |          |    |    |
| NONE     |    |    |    |    |          |    |    |
| 0h       |    |    |    |    |          |    |    |
| 15       | 14 | 13 | 12 | 11 | 10       | 9  | 8  |
| RESERVED |    |    |    |    | NUM_RAMs |    |    |
| NONE     |    |    |    |    | R        |    |    |
| 0h       |    |    |    |    | 1Ch      |    |    |
| 7        | 6  | 5  | 4  | 3  | 2        | 1  | 0  |
| NUM_RAMs |    |    |    |    |          |    |    |
| R        |    |    |    |    |          |    |    |
| 1Ch      |    |    |    |    |          |    |    |

**Table 5-1336. ECC\_AGGR\_MISC\_STATUS Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                 |
|-------|----------|------|-------|-------------------------------------------------------------|
| 31:11 | RESERVED | NONE | 0h    | Reserved                                                    |
| 10:0  | NUM_RAMs | R    | 1Ch   | Indicates the number of RAMs serviced by the ECC aggregator |

### 5.3.2.4 ECC\_AGGR\_ECC\_WRAP\_REVISION Register

#### 1 ECC\_AGGR\_ECC\_WRAP\_REVISION Register (Offset = 10h) [reset = 66A40202h]

Revision parameters.

Return to [Summary Table](#)

**Table 5-1337. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECC_AGGR      | 5301 0010h       |

**Figure 5-445. ECC\_AGGR\_ECC\_WRAP\_REVISION Name Register**

|           |    |        |    |           |        |    |    |
|-----------|----|--------|----|-----------|--------|----|----|
| 31        | 30 | 29     | 28 | 27        | 26     | 25 | 24 |
| SCHEME    |    | BU     |    | MODULE_ID |        |    |    |
| R         |    | R      |    | R         |        |    |    |
| 1h        |    | 2h     |    | 6A4h      |        |    |    |
| 23        | 22 | 21     | 20 | 19        | 18     | 17 | 16 |
| MODULE_ID |    |        |    |           |        |    |    |
| R         |    |        |    |           |        |    |    |
| 6A4h      |    |        |    |           |        |    |    |
| 15        | 14 | 13     | 12 | 11        | 10     | 9  | 8  |
| REVRTL    |    |        |    |           | REVMAJ |    |    |
| R         |    |        |    |           | R      |    |    |
| 0h        |    |        |    |           | 2h     |    |    |
| 7         | 6  | 5      | 4  | 3         | 2      | 1  | 0  |
| CUSTOM    |    | REVMIN |    |           |        |    |    |
| R         |    | R      |    |           |        |    |    |
| 0h        |    | 2h     |    |           |        |    |    |

**Table 5-1339. ECC\_AGGR\_ECC\_WRAP\_REVISION Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description    |
|-------|-----------|------|-------|----------------|
| 31:30 | SCHEME    | R    | 1h    | Scheme         |
| 29:28 | BU        | R    | 2h    | Business unit  |
| 27:16 | MODULE_ID | R    | 6A4h  | Module ID      |
| 15:11 | REVRTL    | R    | 0h    | RTL version    |
| 10:8  | REVMAJ    | R    | 2h    | Major version  |
| 7:6   | CUSTOM    | R    | 0h    | Custom version |
| 5:0   | REVMIN    | R    | 2h    | Minor version  |

### 5.3.2.5 ECC\_AGGR\_CONTROL Register

#### 1 ECC\_AGGR\_CONTROL Register (Offset = 14h) [reset = 187h]

ECC Control Register.

Return to [Summary Table](#)

**Table 5-1340. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECC_AGGR      | 5301 0014h       |

**Figure 5-446. ECC\_AGGR\_CONTROL Name Register**

|                  |            |             |           |           |            |           |                         |
|------------------|------------|-------------|-----------|-----------|------------|-----------|-------------------------|
| 31               | 30         | 29          | 28        | 27        | 26         | 25        | 24                      |
| RESERVED         |            |             |           |           |            |           |                         |
| NONE             |            |             |           |           |            |           |                         |
| 0h               |            |             |           |           |            |           |                         |
| 23               | 22         | 21          | 20        | 19        | 18         | 17        | 16                      |
| RESERVED         |            |             |           |           |            |           |                         |
| NONE             |            |             |           |           |            |           |                         |
| 0h               |            |             |           |           |            |           |                         |
| 15               | 14         | 13          | 12        | 11        | 10         | 9         | 8                       |
| RESERVED         |            |             |           |           |            |           | CHECK_SVBU<br>S_TIMEOUT |
| NONE             |            |             |           |           |            |           | R/W                     |
| 0h               |            |             |           |           |            |           | 1h                      |
| 7                | 6          | 5           | 4         | 3         | 2          | 1         | 0                       |
| CHECK_PARIT<br>Y | ERROR_ONCE | FORCE_N_ROW | FORCE_DED | FORCE_SEC | ENABLE_RMW | ECC_CHECK | ECC_ENABLE              |
| R/W              | R/W        | R/W         | R/W       | R/W       | R/W        | R/W       | R/W                     |
| 1h               | 0h         | 0h          | 0h        | 0h        | 1h         | 1h        | 1h                      |

**Table 5-1342. ECC\_AGGR\_CONTROL Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description                    |
|------|---------------------|------|-------|--------------------------------|
| 31:9 | RESERVED            | NONE | 0h    | Reserved                       |
| 8    | CHECK_SVBUS_TIMEOUT | R/W  | 1h    | check for svbus timeout errors |
| 7    | CHECK_PARITY        | R/W  | 1h    | check for parity errors        |
| 6    | ERROR_ONCE          | R/W  | 0h    | Force Error only once          |
| 5    | FORCE_N_ROW         | R/W  | 0h    | Force Error on any RAM read    |
| 4    | FORCE_DED           | R/W  | 0h    | Force Double Bit Error         |
| 3    | FORCE_SEC           | R/W  | 0h    | Force Single Bit Error         |
| 2    | ENABLE_RMW          | R/W  | 1h    | Enable rmw                     |
| 1    | ECC_CHECK           | R/W  | 1h    | Enable ECC check               |
| 0    | ECC_ENABLE          | R/W  | 1h    | Enable ECC                     |

### 5.3.2.6 ECC\_AGGR\_ERROR\_CTRL1 Register

#### 1 ECC\_AGGR\_ERROR\_CTRL1 Register (Offset = 18h) [reset = 0h]

ECC Error Control1 Register.

Return to [Summary Table](#)

**Table 5-1343. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECC_AGGR      | 5301 0018h       |

**Figure 5-447. ECC\_AGGR\_ERROR\_CTRL1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ECC_ROW |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ECC_ROW |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ECC_ROW |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ECC_ROW |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-1345. ECC\_AGGR\_ERROR\_CTRL1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                             |
|------|---------|------|-------|---------------------------------------------------------------------------------------------------------|
| 31:0 | ECC_ROW | R/W  | 0h    | Row address where single or double-bit error needs to be applied. This is ignored if force_n_row is set |

### 5.3.2.7 ECC\_AGGR\_ERROR\_CTRL2 Register

#### 1 ECC\_AGGR\_ERROR\_CTRL2 Register (Offset = 1Ch) [reset = 0h]

ECC Error Control2 Register.

Return to [Summary Table](#)

**Table 5-1346. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECC_AGGR      | 5301 001Ch       |

**Figure 5-448. ECC\_AGGR\_ERROR\_CTRL2 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ECC_BIT2 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ECC_BIT2 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ECC_BIT1 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ECC_BIT1 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-1348. ECC\_AGGR\_ERROR\_CTRL2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                              |
|-------|----------|------|-------|--------------------------------------------------------------------------|
| 31:16 | ECC_BIT2 | R/W  | 0h    | Data bit that needs to be flipped if double bit error needs to be forced |
| 15:0  | ECC_BIT1 | R/W  | 0h    | Data bit that needs to be flipped when force_sec is set                  |



### 5.3.2.8 ECC\_AGGR\_ERROR\_STATUS1 Register

#### 1 ECC\_AGGR\_ERROR\_STATUS1 Register (Offset = 20h) [reset = 0h]

ECC Error Status1 Register.

Return to [Summary Table](#)

**Table 5-1349. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECC_AGGR      | 5301 0020h       |

**Figure 5-449. ECC\_AGGR\_ERROR\_STATUS1 Name Register**

|                  |                |    |               |             |    |             |    |
|------------------|----------------|----|---------------|-------------|----|-------------|----|
| 31               | 30             | 29 | 28            | 27          | 26 | 25          | 24 |
| ECC_BIT1         |                |    |               |             |    |             |    |
| R                |                |    |               |             |    |             |    |
| 0h               |                |    |               |             |    |             |    |
| 23               | 22             | 21 | 20            | 19          | 18 | 17          | 16 |
| ECC_BIT1         |                |    |               |             |    |             |    |
| R                |                |    |               |             |    |             |    |
| 0h               |                |    |               |             |    |             |    |
| 15               | 14             | 13 | 12            | 11          | 10 | 9           | 8  |
| CLR_CTRL_REG_ERR | CLR_PARITY_ERR |    | CLR_ECC_OTHER | CLR_ECC_DED |    | CLR_ECC_SEC |    |
| R/W1TC           | R/WD           |    | R/W1TC        | R/WD        |    | R/WD        |    |
| 0h               | 0h             |    | 0h            | 0h          |    | 0h          |    |
| 7                | 6              | 5  | 4             | 3           | 2  | 1           | 0  |
| CTR_REG_ERR      | PARITY_ERR     |    | ECC_OTHER     | ECC_DED     |    | ECC_SEC     |    |
| R/W1TS           | R/W1TS         |    | R/W1TS        | R/WI        |    | R/WI        |    |
| 0h               | 0h             |    | 0h            | 0h          |    | 0h          |    |

**Table 5-1351. ECC\_AGGR\_ERROR\_STATUS1 Register Field Descriptions**

| Bit   | Field            | Type   | Reset | Description                                                                                            |
|-------|------------------|--------|-------|--------------------------------------------------------------------------------------------------------|
| 31:16 | ECC_BIT1         | R      | 0h    | Data bit that corresponds to the single-bit error                                                      |
| 15    | CLR_CTRL_REG_ERR | R/W1TC | 0h    | Clear control reg error Error Status, you must also re write the control register itself to clear this |
| 14:13 | CLR_PARITY_ERR   | R/WD   | 0h    | Clear parity Error Status                                                                              |
| 12    | CLR_ECC_OTHER    | R/W1TC | 0h    | Clear other Error Status                                                                               |
| 11:10 | CLR_ECC_DED      | R/WD   | 0h    | Clear Double Bit Error Status                                                                          |
| 9:8   | CLR_ECC_SEC      | R/WD   | 0h    | Clear Single Bit Error Status                                                                          |
| 7     | CTR_REG_ERR      | R/W1TS | 0h    | control register error pending, Level interrupt                                                        |
| 6:5   | PARITY_ERR       | R/W1TS | 0h    | Level parity error Error Status                                                                        |
| 4     | ECC_OTHER        | R/W1TS | 0h    | Successive single-bit errors have occurred while a writeback is still pending, Level interrupt         |
| 3:2   | ECC_DED          | R/WI   | 0h    | Level Double Bit Error Status                                                                          |
| 1:0   | ECC_SEC          | R/WI   | 0h    | Level Single Bit Error Status                                                                          |

### 5.3.2.9 ECC\_AGGR\_ERROR\_STATUS2 Register

#### 1 ECC\_AGGR\_ERROR\_STATUS2 Register (Offset = 24h) [reset = 0h]

ECC Error Status2 Register.

Return to [Summary Table](#)

**Table 5-1352. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECC_AGGR      | 5301 0024h       |

**Figure 5-450. ECC\_AGGR\_ERROR\_STATUS2 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ECC_ROW |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ECC_ROW |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ECC_ROW |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ECC_ROW |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-1354. ECC\_AGGR\_ERROR\_STATUS2 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                   |
|------|---------|------|-------|---------------------------------------------------------------|
| 31:0 | ECC_ROW | R    | 0h    | Row address where the single or double-bit error has occurred |

### 5.3.2.10 ECC\_AGGR\_ERROR\_STATUS3 Register

#### 1 ECC\_AGGR\_ERROR\_STATUS3 Register (Offset = 28h) [reset = 0h]

ECC Error Status3 Register.

Return to [Summary Table](#)

**Table 5-1355. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECC_AGGR      | 5301 0028h       |

**Figure 5-451. ECC\_AGGR\_ERROR\_STATUS3 Name Register**

|          |    |    |    |    |    |                           |          |
|----------|----|----|----|----|----|---------------------------|----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25                        | 24       |
| RESERVED |    |    |    |    |    |                           |          |
| NONE     |    |    |    |    |    |                           |          |
| 0h       |    |    |    |    |    |                           |          |
| 23       | 22 | 21 | 20 | 19 | 18 | 17                        | 16       |
| RESERVED |    |    |    |    |    |                           |          |
| NONE     |    |    |    |    |    |                           |          |
| 0h       |    |    |    |    |    |                           |          |
| 15       | 14 | 13 | 12 | 11 | 10 | 9                         | 8        |
| RESERVED |    |    |    |    |    | CLR_SVBUS_T<br>IMEOUT_ERR | RESERVED |
| NONE     |    |    |    |    |    | R/W1TC                    | NONE     |
| 0h       |    |    |    |    |    | 0h                        | 0h       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1                         | 0        |
| RESERVED |    |    |    |    |    | SVBUS_TIMEO<br>UT_ERR     | WB_PEND  |
| NONE     |    |    |    |    |    | R/W1TS                    | R        |
| 0h       |    |    |    |    |    | 0h                        | 0h       |

**Table 5-1357. ECC\_AGGR\_ERROR\_STATUS3 Register Field Descriptions**

| Bit   | Field                 | Type   | Reset | Description                            |
|-------|-----------------------|--------|-------|----------------------------------------|
| 31:10 | RESERVED              | NONE   | 0h    | Reserved                               |
| 9     | CLR_SVBUS_TIMEOUT_ERR | R/W1TC | 0h    | Clear svbus timeout Error Status       |
| 8:2   | RESERVED              | NONE   | 0h    | Reserved                               |
| 1     | SVBUS_TIMEOUT_ERR     | R/W1TS | 0h    | Level svbus timeout error Error Status |
| 0     | WB_PEND               | R      | 0h    | delayed write back pending Status      |

### 5.3.2.11 ECC\_AGGR\_SEC\_EOI\_REG Register

#### 1 ECC\_AGGR\_SEC\_EOI\_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register.

Return to [Summary Table](#)

**Table 5-1358. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECC_AGGR      | 5301 003Ch       |

**Figure 5-452. ECC\_AGGR\_SEC\_EOI\_REG Name Register**

|          |    |    |    |    |    |    |        |
|----------|----|----|----|----|----|----|--------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24     |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16     |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8      |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0      |
| RESERVED |    |    |    |    |    |    | EOI_WR |
| NONE     |    |    |    |    |    |    | R/W1TS |
| 0h       |    |    |    |    |    |    | 0h     |

**Table 5-1360. ECC\_AGGR\_SEC\_EOI\_REG Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description                                                                                                                                                                                     |
|------|----------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED | NONE   | 0h    | Reserved                                                                                                                                                                                        |
| 0    | EOI_WR   | R/W1TS | 0h    | Write of 1 to this register indicates that software has acknowledged the pending interrupt and the next interrupt can be sent to the host. The bit is self clearing and will be read as a zero. |

### 5.3.2.12 ECC\_AGGR\_SEC\_STATUS\_REG0 Register

#### 1 ECC\_AGGR\_SEC\_STATUS\_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

Return to [Summary Table](#)

**Table 5-1361. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECC_AGGR      | 5301 0040h       |

**Figure 5-453. ECC\_AGGR\_SEC\_STATUS\_REG0 Name Register**

|          |              |              |               |                 |                 |                 |                 |
|----------|--------------|--------------|---------------|-----------------|-----------------|-----------------|-----------------|
| 31       | 30           | 29           | 28            | 27              | 26              | 25              | 24              |
| RESERVED |              |              |               |                 |                 |                 |                 |
| NONE     |              |              |               |                 |                 |                 |                 |
| 0h       |              |              |               |                 |                 |                 |                 |
| 23       | 22           | 21           | 20            | 19              | 18              | 17              | 16              |
| RESERVED |              |              |               |                 |                 |                 |                 |
| NONE     |              |              |               |                 |                 |                 |                 |
| 0h       |              |              |               |                 |                 |                 |                 |
| 15       | 14           | 13           | 12            | 11              | 10              | 9               | 8               |
| RESERVED |              |              |               |                 |                 |                 |                 |
| NONE     |              |              |               |                 |                 |                 |                 |
| 0h       |              |              |               |                 |                 |                 |                 |
| 7        | 6            | 5            | 4             | 3               | 2               | 1               | 0               |
| RESERVED | TPTC_A1_PEND | TPTC_A0_PEND | MSS_MBOX_PEND | MSS_L2SLV3_PEND | MSS_L2SLV2_PEND | MSS_L2SLV1_PEND | MSS_L2SLV0_PEND |
| NONE     | R/W1TS       | R/W1TS       | R/W1TS        | R/W1TS          | R/W1TS          | R/W1TS          | R/W1TS          |
| 0h       | 0h           | 0h           | 0h            | 0h              | 0h              | 0h              | 0h              |

**Table 5-1363. ECC\_AGGR\_SEC\_STATUS\_REG0 Register Field Descriptions**

| Bit  | Field           | Type   | Reset | Description                                  |
|------|-----------------|--------|-------|----------------------------------------------|
| 31:7 | RESERVED        | NONE   | 0h    | Reserved                                     |
| 6    | TPTC_A1_PEND    | R/W1TS | 0h    | Interrupt Pending Status for tptc_a1_pend    |
| 5    | TPTC_A0_PEND    | R/W1TS | 0h    | Interrupt Pending Status for tptc_a0_pend    |
| 4    | MSS_MBOX_PEND   | R/W1TS | 0h    | Interrupt Pending Status for mss_mbox_pend   |
| 3    | MSS_L2SLV3_PEND | R/W1TS | 0h    | Interrupt Pending Status for mss_l2slv3_pend |
| 2    | MSS_L2SLV2_PEND | R/W1TS | 0h    | Interrupt Pending Status for mss_l2slv2_pend |
| 1    | MSS_L2SLV1_PEND | R/W1TS | 0h    | Interrupt Pending Status for mss_l2slv1_pend |
| 0    | MSS_L2SLV0_PEND | R/W1TS | 0h    | Interrupt Pending Status for mss_l2slv0_pend |

### 5.3.2.13 ECC\_AGGR\_SEC\_ENABLE\_SET\_REG0 Register

#### 1 ECC\_AGGR\_SEC\_ENABLE\_SET\_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

Return to [Summary Table](#)

**Table 5-1364. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECC_AGGR      | 5301 0080h       |

**Figure 5-454. ECC\_AGGR\_SEC\_ENABLE\_SET\_REG0 Name Register**

|          |                     |                    |                     |                       |                       |                       |                       |
|----------|---------------------|--------------------|---------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| 31       | 30                  | 29                 | 28                  | 27                    | 26                    | 25                    | 24                    |
| RESERVED |                     |                    |                     |                       |                       |                       |                       |
| NONE     |                     |                    |                     |                       |                       |                       |                       |
| 0h       |                     |                    |                     |                       |                       |                       |                       |
| 23       | 22                  | 21                 | 20                  | 19                    | 18                    | 17                    | 16                    |
| RESERVED |                     |                    |                     |                       |                       |                       |                       |
| NONE     |                     |                    |                     |                       |                       |                       |                       |
| 0h       |                     |                    |                     |                       |                       |                       |                       |
| 15       | 14                  | 13                 | 12                  | 11                    | 10                    | 9                     | 8                     |
| RESERVED |                     |                    |                     |                       |                       |                       |                       |
| NONE     |                     |                    |                     |                       |                       |                       |                       |
| 0h       |                     |                    |                     |                       |                       |                       |                       |
| 7        | 6                   | 5                  | 4                   | 3                     | 2                     | 1                     | 0                     |
| RESERVED | TPTC_A1_ENABLE_SETT | TPTC_A0_ENABLE_SET | MSS_MBOX_ENABLE_SET | MSS_L2SLV3_ENABLE_SET | MSS_L2SLV2_ENABLE_SET | MSS_L2SLV1_ENABLE_SET | MSS_L2SLV0_ENABLE_SET |
| NONE     | R/W1TS              | R/W1TS             | R/W1TS              | R/W1TS                | R/W1TS                | R/W1TS                | R/W1TS                |
| 0h       | 0h                  | 0h                 | 0h                  | 0h                    | 0h                    | 0h                    | 0h                    |

**Table 5-1366. ECC\_AGGR\_SEC\_ENABLE\_SET\_REG0 Register Field Descriptions**

| Bit  | Field                 | Type   | Reset | Description                                       |
|------|-----------------------|--------|-------|---------------------------------------------------|
| 31:7 | RESERVED              | NONE   | 0h    | Reserved                                          |
| 6    | TPTC_A1_ENABLE_SETT   | R/W1TS | 0h    | Interrupt Enable Set Register for tptc_a1_pend    |
| 5    | TPTC_A0_ENABLE_SET    | R/W1TS | 0h    | Interrupt Enable Set Register for tptc_a0_pend    |
| 4    | MSS_MBOX_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for mss_mbox_pend   |
| 3    | MSS_L2SLV3_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for mss_l2slv3_pend |
| 2    | MSS_L2SLV2_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for mss_l2slv2_pend |
| 1    | MSS_L2SLV1_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for mss_l2slv1_pend |
| 0    | MSS_L2SLV0_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for mss_l2slv0_pend |

### 5.3.2.14 ECC\_AGGR\_SEC\_ENABLE\_CLR\_REG0 Register

#### 1 ECC\_AGGR\_SEC\_ENABLE\_CLR\_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to [Summary Table](#)

**Table 5-1367. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECC_AGGR      | 5301 00C0h       |

**Figure 5-455. ECC\_AGGR\_SEC\_ENABLE\_CLR\_REG0 Name Register**

|          |                    |                    |                     |                       |                       |                       |                       |
|----------|--------------------|--------------------|---------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| 31       | 30                 | 29                 | 28                  | 27                    | 26                    | 25                    | 24                    |
| RESERVED |                    |                    |                     |                       |                       |                       |                       |
| NONE     |                    |                    |                     |                       |                       |                       |                       |
| 0h       |                    |                    |                     |                       |                       |                       |                       |
| 23       | 22                 | 21                 | 20                  | 19                    | 18                    | 17                    | 16                    |
| RESERVED |                    |                    |                     |                       |                       |                       |                       |
| NONE     |                    |                    |                     |                       |                       |                       |                       |
| 0h       |                    |                    |                     |                       |                       |                       |                       |
| 15       | 14                 | 13                 | 12                  | 11                    | 10                    | 9                     | 8                     |
| RESERVED |                    |                    |                     |                       |                       |                       |                       |
| NONE     |                    |                    |                     |                       |                       |                       |                       |
| 0h       |                    |                    |                     |                       |                       |                       |                       |
| 7        | 6                  | 5                  | 4                   | 3                     | 2                     | 1                     | 0                     |
| RESERVED | TPTC_A1_ENABLE_CLR | TPTC_A0_ENABLE_CLR | MSS_MBOX_ENABLE_CLR | MSS_L2SLV3_ENABLE_CLR | MSS_L2SLV2_ENABLE_CLR | MSS_L2SLV1_ENABLE_CLR | MSS_L2SLV0_ENABLE_CLR |
| NONE     | R/W1TC             | R/W1TC             | R/W1TC              | R/W1TC                | R/W1TC                | R/W1TC                | R/W1TC                |
| 0h       | 0h                 | 0h                 | 0h                  | 0h                    | 0h                    | 0h                    | 0h                    |

**Table 5-1369. ECC\_AGGR\_SEC\_ENABLE\_CLR\_REG0 Register Field Descriptions**

| Bit  | Field                 | Type   | Reset | Description                                         |
|------|-----------------------|--------|-------|-----------------------------------------------------|
| 31:7 | RESERVED              | NONE   | 0h    | Reserved                                            |
| 6    | TPTC_A1_ENABLE_CLR    | R/W1TC | 0h    | Interrupt Enable Clear Register for tptc_a1_pend    |
| 5    | TPTC_A0_ENABLE_CLR    | R/W1TC | 0h    | Interrupt Enable Clear Register for tptc_a0_pend    |
| 4    | MSS_MBOX_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for mss_mbox_pend   |
| 3    | MSS_L2SLV3_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for mss_l2slv3_pend |
| 2    | MSS_L2SLV2_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for mss_l2slv2_pend |
| 1    | MSS_L2SLV1_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for mss_l2slv1_pend |
| 0    | MSS_L2SLV0_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for mss_l2slv0_pend |

### 5.3.2.15 ECC\_AGGR\_DED\_EOI\_REG Register

#### 1 ECC\_AGGR\_DED\_EOI\_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register.

Return to [Summary Table](#)

**Table 5-1370. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECC_AGGR      | 5301 013Ch       |

**Figure 5-456. ECC\_AGGR\_DED\_EOI\_REG Name Register**

|          |    |    |    |    |    |    |        |
|----------|----|----|----|----|----|----|--------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24     |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16     |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8      |
| RESERVED |    |    |    |    |    |    |        |
| NONE     |    |    |    |    |    |    |        |
| 0h       |    |    |    |    |    |    |        |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0      |
| RESERVED |    |    |    |    |    |    | EOI_WR |
| NONE     |    |    |    |    |    |    | R/W1TS |
| 0h       |    |    |    |    |    |    | 0h     |

**Table 5-1372. ECC\_AGGR\_DED\_EOI\_REG Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description                                                                                                                                                                                     |
|------|----------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED | NONE   | 0h    | Reserved                                                                                                                                                                                        |
| 0    | EOI_WR   | R/W1TS | 0h    | Write of 1 to this register indicates that software has acknowledged the pending interrupt and the next interrupt can be sent to the host. The bit is self clearing and will be read as a zero. |



### 5.3.2.16 ECC\_AGGR\_DED\_STATUS\_REG0 Register

#### 1 ECC\_AGGR\_DED\_STATUS\_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

Return to [Summary Table](#)

**Table 5-1373. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECC_AGGR      | 5301 0140h       |

**Figure 5-457. ECC\_AGGR\_DED\_STATUS\_REG0 Name Register**

|          |              |              |               |                 |                 |                 |                 |
|----------|--------------|--------------|---------------|-----------------|-----------------|-----------------|-----------------|
| 31       | 30           | 29           | 28            | 27              | 26              | 25              | 24              |
| RESERVED |              |              |               |                 |                 |                 |                 |
| NONE     |              |              |               |                 |                 |                 |                 |
| 0h       |              |              |               |                 |                 |                 |                 |
| 23       | 22           | 21           | 20            | 19              | 18              | 17              | 16              |
| RESERVED |              |              |               |                 |                 |                 |                 |
| NONE     |              |              |               |                 |                 |                 |                 |
| 0h       |              |              |               |                 |                 |                 |                 |
| 15       | 14           | 13           | 12            | 11              | 10              | 9               | 8               |
| RESERVED |              |              |               |                 |                 |                 |                 |
| NONE     |              |              |               |                 |                 |                 |                 |
| 0h       |              |              |               |                 |                 |                 |                 |
| 7        | 6            | 5            | 4             | 3               | 2               | 1               | 0               |
| RESERVED | TPTC_A1_PEND | TPTC_A0_PEND | MSS_MBOX_PEND | MSS_L2SLV3_PEND | MSS_L2SLV2_PEND | MSS_L2SLV1_PEND | MSS_L2SLV0_PEND |
| NONE     | R/W1TS       | R/W1TS       | R/W1TS        | R/W1TS          | R/W1TS          | R/W1TS          | R/W1TS          |
| 0h       | 0h           | 0h           | 0h            | 0h              | 0h              | 0h              | 0h              |

**Table 5-1375. ECC\_AGGR\_DED\_STATUS\_REG0 Register Field Descriptions**

| Bit  | Field           | Type   | Reset | Description                                  |
|------|-----------------|--------|-------|----------------------------------------------|
| 31:7 | RESERVED        | NONE   | 0h    | Reserved                                     |
| 6    | TPTC_A1_PEND    | R/W1TS | 0h    | Interrupt Pending Status for tptc_a1_pend    |
| 5    | TPTC_A0_PEND    | R/W1TS | 0h    | Interrupt Pending Status for tptc_a0_pend    |
| 4    | MSS_MBOX_PEND   | R/W1TS | 0h    | Interrupt Pending Status for mss_mbox_pend   |
| 3    | MSS_L2SLV3_PEND | R/W1TS | 0h    | Interrupt Pending Status for mss_l2slv3_pend |
| 2    | MSS_L2SLV2_PEND | R/W1TS | 0h    | Interrupt Pending Status for mss_l2slv2_pend |
| 1    | MSS_L2SLV1_PEND | R/W1TS | 0h    | Interrupt Pending Status for mss_l2slv1_pend |
| 0    | MSS_L2SLV0_PEND | R/W1TS | 0h    | Interrupt Pending Status for mss_l2slv0_pend |

### 5.3.2.17 ECC\_AGGR\_DED\_ENABLE\_SET\_REG0 Register

#### 1 ECC\_AGGR\_DED\_ENABLE\_SET\_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

Return to [Summary Table](#)

**Table 5-1376. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECC_AGGR      | 5301 0180h       |

**Figure 5-458. ECC\_AGGR\_DED\_ENABLE\_SET\_REG0 Name Register**

|          |                     |                    |                     |                       |                       |                       |                       |
|----------|---------------------|--------------------|---------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| 31       | 30                  | 29                 | 28                  | 27                    | 26                    | 25                    | 24                    |
| RESERVED |                     |                    |                     |                       |                       |                       |                       |
| NONE     |                     |                    |                     |                       |                       |                       |                       |
| 0h       |                     |                    |                     |                       |                       |                       |                       |
| 23       | 22                  | 21                 | 20                  | 19                    | 18                    | 17                    | 16                    |
| RESERVED |                     |                    |                     |                       |                       |                       |                       |
| NONE     |                     |                    |                     |                       |                       |                       |                       |
| 0h       |                     |                    |                     |                       |                       |                       |                       |
| 15       | 14                  | 13                 | 12                  | 11                    | 10                    | 9                     | 8                     |
| RESERVED |                     |                    |                     |                       |                       |                       |                       |
| NONE     |                     |                    |                     |                       |                       |                       |                       |
| 0h       |                     |                    |                     |                       |                       |                       |                       |
| 7        | 6                   | 5                  | 4                   | 3                     | 2                     | 1                     | 0                     |
| RESERVED | TPTC_A1_ENABLE_SETT | TPTC_A0_ENABLE_SET | MSS_MBOX_ENABLE_SET | MSS_L2SLV3_ENABLE_SET | MSS_L2SLV2_ENABLE_SET | MSS_L2SLV1_ENABLE_SET | MSS_L2SLV0_ENABLE_SET |
| NONE     | R/W1TS              | R/W1TS             | R/W1TS              | R/W1TS                | R/W1TS                | R/W1TS                | R/W1TS                |
| 0h       | 0h                  | 0h                 | 0h                  | 0h                    | 0h                    | 0h                    | 0h                    |

**Table 5-1378. ECC\_AGGR\_DED\_ENABLE\_SET\_REG0 Register Field Descriptions**

| Bit  | Field                 | Type   | Reset | Description                                       |
|------|-----------------------|--------|-------|---------------------------------------------------|
| 31:7 | RESERVED              | NONE   | 0h    | Reserved                                          |
| 6    | TPTC_A1_ENABLE_SETT   | R/W1TS | 0h    | Interrupt Enable Set Register for tptc_a1_pend    |
| 5    | TPTC_A0_ENABLE_SET    | R/W1TS | 0h    | Interrupt Enable Set Register for tptc_a0_pend    |
| 4    | MSS_MBOX_ENABLE_SET   | R/W1TS | 0h    | Interrupt Enable Set Register for mss_mbox_pend   |
| 3    | MSS_L2SLV3_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for mss_l2slv3_pend |
| 2    | MSS_L2SLV2_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for mss_l2slv2_pend |
| 1    | MSS_L2SLV1_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for mss_l2slv1_pend |
| 0    | MSS_L2SLV0_ENABLE_SET | R/W1TS | 0h    | Interrupt Enable Set Register for mss_l2slv0_pend |

### 5.3.2.18 ECC\_AGGR\_DED\_ENABLE\_CLR\_REG0 Register

#### 1 ECC\_AGGR\_DED\_ENABLE\_CLR\_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to [Summary Table](#)

**Table 5-1379. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECC_AGGR      | 5301 01C0h       |

**Figure 5-459. ECC\_AGGR\_DED\_ENABLE\_CLR\_REG0 Name Register**

|          |                    |                    |                     |                       |                       |                       |                       |
|----------|--------------------|--------------------|---------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| 31       | 30                 | 29                 | 28                  | 27                    | 26                    | 25                    | 24                    |
| RESERVED |                    |                    |                     |                       |                       |                       |                       |
| NONE     |                    |                    |                     |                       |                       |                       |                       |
| 0h       |                    |                    |                     |                       |                       |                       |                       |
| 23       | 22                 | 21                 | 20                  | 19                    | 18                    | 17                    | 16                    |
| RESERVED |                    |                    |                     |                       |                       |                       |                       |
| NONE     |                    |                    |                     |                       |                       |                       |                       |
| 0h       |                    |                    |                     |                       |                       |                       |                       |
| 15       | 14                 | 13                 | 12                  | 11                    | 10                    | 9                     | 8                     |
| RESERVED |                    |                    |                     |                       |                       |                       |                       |
| NONE     |                    |                    |                     |                       |                       |                       |                       |
| 0h       |                    |                    |                     |                       |                       |                       |                       |
| 7        | 6                  | 5                  | 4                   | 3                     | 2                     | 1                     | 0                     |
| RESERVED | TPTC_A1_ENABLE_CLR | TPTC_A0_ENABLE_CLR | MSS_MBOX_ENABLE_CLR | MSS_L2SLV3_ENABLE_CLR | MSS_L2SLV2_ENABLE_CLR | MSS_L2SLV1_ENABLE_CLR | MSS_L2SLV0_ENABLE_CLR |
| NONE     | R/W1TC             | R/W1TC             | R/W1TC              | R/W1TC                | R/W1TC                | R/W1TC                | R/W1TC                |
| 0h       | 0h                 | 0h                 | 0h                  | 0h                    | 0h                    | 0h                    | 0h                    |

**Table 5-1381. ECC\_AGGR\_DED\_ENABLE\_CLR\_REG0 Register Field Descriptions**

| Bit  | Field                 | Type   | Reset | Description                                         |
|------|-----------------------|--------|-------|-----------------------------------------------------|
| 31:7 | RESERVED              | NONE   | 0h    | Reserved                                            |
| 6    | TPTC_A1_ENABLE_CLR    | R/W1TC | 0h    | Interrupt Enable Clear Register for tptc_a1_pend    |
| 5    | TPTC_A0_ENABLE_CLR    | R/W1TC | 0h    | Interrupt Enable Clear Register for tptc_a0_pend    |
| 4    | MSS_MBOX_ENABLE_CLR   | R/W1TC | 0h    | Interrupt Enable Clear Register for mss_mbox_pend   |
| 3    | MSS_L2SLV3_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for mss_l2slv3_pend |
| 2    | MSS_L2SLV2_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for mss_l2slv2_pend |
| 1    | MSS_L2SLV1_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for mss_l2slv1_pend |
| 0    | MSS_L2SLV0_ENABLE_CLR | R/W1TC | 0h    | Interrupt Enable Clear Register for mss_l2slv0_pend |

### 5.3.2.19 ECC\_AGGR\_AGGR\_ENABLE\_SET Register

#### 1 ECC\_AGGR\_AGGR\_ENABLE\_SET Register (Offset = 200h) [reset = 0h]

Enable set register for aggregator interrupts.

Return to [Summary Table](#)

**Table 5-1382. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECC_AGGR      | 5301 0200h       |

**Figure 5-460. ECC\_AGGR\_AGGR\_ENABLE\_SET Name Register**

|          |    |    |    |    |    |         |        |
|----------|----|----|----|----|----|---------|--------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25      | 24     |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 23       | 22 | 21 | 20 | 19 | 18 | 17      | 16     |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 15       | 14 | 13 | 12 | 11 | 10 | 9       | 8      |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 7        | 6  | 5  | 4  | 3  | 2  | 1       | 0      |
| RESERVED |    |    |    |    |    | TIMEOUT | PARITY |
| NONE     |    |    |    |    |    | R/W1TS  | R/W1TS |
| 0h       |    |    |    |    |    | 0h      | 0h     |

**Table 5-1384. ECC\_AGGR\_AGGR\_ENABLE\_SET Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description                                   |
|------|----------|--------|-------|-----------------------------------------------|
| 31:2 | RESERVED | NONE   | 0h    | Reserved                                      |
| 1    | TIMEOUT  | R/W1TS | 0h    | Interrupt enable set for svbus timeout errors |
| 0    | PARITY   | R/W1TS | 0h    | Interrupt enable set for parity errors        |

### 5.3.2.20 ECC\_AGGR\_AGGR\_ENABLE\_CLR Register

#### 1 ECC\_AGGR\_AGGR\_ENABLE\_CLR Register (Offset = 204h) [reset = 0h]

Enable clear register for aggregator interrupts.

Return to [Summary Table](#)

**Table 5-1385. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECC_AGGR      | 5301 0204h       |

**Figure 5-461. ECC\_AGGR\_AGGR\_ENABLE\_CLR Name Register**

|          |    |    |    |    |    |         |        |
|----------|----|----|----|----|----|---------|--------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25      | 24     |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 23       | 22 | 21 | 20 | 19 | 18 | 17      | 16     |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 15       | 14 | 13 | 12 | 11 | 10 | 9       | 8      |
| RESERVED |    |    |    |    |    |         |        |
| NONE     |    |    |    |    |    |         |        |
| 0h       |    |    |    |    |    |         |        |
| 7        | 6  | 5  | 4  | 3  | 2  | 1       | 0      |
| RESERVED |    |    |    |    |    | TIMEOUT | PARITY |
| NONE     |    |    |    |    |    | R/W1TC  | R/W1TC |
| 0h       |    |    |    |    |    | 0h      | 0h     |

**Table 5-1387. ECC\_AGGR\_AGGR\_ENABLE\_CLR Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description                                     |
|------|----------|--------|-------|-------------------------------------------------|
| 31:2 | RESERVED | NONE   | 0h    | Reserved                                        |
| 1    | TIMEOUT  | R/W1TC | 0h    | Interrupt enable clear for svbus timeout errors |
| 0    | PARITY   | R/W1TC | 0h    | Interrupt enable clear for parity errors        |

### 5.3.2.21 ECC\_AGGR\_AGGR\_STATUS\_SET Register

#### 1 ECC\_AGGR\_AGGR\_STATUS\_SET Register (Offset = 208h) [reset = 0h]

Status set register for aggregator interrupts.

Return to [Summary Table](#)

**Table 5-1388. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECC_AGGR      | 5301 0208h       |

**Figure 5-462. ECC\_AGGR\_AGGR\_STATUS\_SET Name Register**

|          |    |    |    |         |    |        |    |
|----------|----|----|----|---------|----|--------|----|
| 31       | 30 | 29 | 28 | 27      | 26 | 25     | 24 |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 23       | 22 | 21 | 20 | 19      | 18 | 17     | 16 |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 15       | 14 | 13 | 12 | 11      | 10 | 9      | 8  |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 7        | 6  | 5  | 4  | 3       | 2  | 1      | 0  |
| RESERVED |    |    |    | TIMEOUT |    | PARITY |    |
| NONE     |    |    |    | R/WI    |    | R/WI   |    |
| 0h       |    |    |    | 0h      |    | 0h     |    |

**Table 5-1390. ECC\_AGGR\_AGGR\_STATUS\_SET Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 3:2  | TIMEOUT  | R/WI | 0h    | 2-bit saturating counter of the number of timeout errors that have occurred since last cleared.<br>2'b00 - No timeout errors have occurred<br>2'b01 - 1 timeout error has occurred<br>2'b10 - 2 timeout error has occurred<br>2'b11 - 3 or more timeout errors have occurred<br>A write of a non-zero value to this register increments that many from the timeout fields. If the value written is less than the current value of the counter, then the pending level interrupt stays asserted. . If this register goes from 0 to non zero a level interrupt will be asserted as well as a pulse interrupt. If the value was non zero to non zero then the level interrupt would remain asserted, but no new pulse interrupt would be asserted. You must write the eoi register to get a new pulse interrupt. |

**Table 5-1390. ECC\_AGGR\_AGGR\_STATUS\_SET Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-----|--------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0 | PARITY | R/WI | 0h    | <p>2-bit saturating counter of the number of parity errors that have occurred since last cleared.</p> <p>2'b00 - No parity errors have occurred</p> <p>2'b01 - 1 parity error has occurred</p> <p>2'b10 - 2 parity error has occurred</p> <p>2'b11 - 3 or more parity error have occurred</p> <p>A write of a non-zero value to this register increments that many from the parity fields. If the value written is less than the current value of the counter, then the pending level interrupt stays asserted. If this register goes from 0 to non zero a level interrupt will be asserted as well as a pulse interrupt. If the value was non zero to non zero then the level interrupt would remain asserted, but no new pulse interrupt would be asserted. You must write the eoi register to get a new pulse interrupt.</p> |

### 5.3.2.22 ECC\_AGGR\_AGGR\_STATUS\_CLR Register

#### 1 ECC\_AGGR\_AGGR\_STATUS\_CLR Register (Offset = 20Ch) [reset = 0h]

Status clear register for aggregator interrupts.

Return to [Summary Table](#)

**Table 5-1391. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ECC_AGGR      | 5301 020Ch       |

**Figure 5-463. ECC\_AGGR\_AGGR\_STATUS\_CLR Name Register**

|          |    |    |    |         |    |        |    |
|----------|----|----|----|---------|----|--------|----|
| 31       | 30 | 29 | 28 | 27      | 26 | 25     | 24 |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 23       | 22 | 21 | 20 | 19      | 18 | 17     | 16 |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 15       | 14 | 13 | 12 | 11      | 10 | 9      | 8  |
| RESERVED |    |    |    |         |    |        |    |
| NONE     |    |    |    |         |    |        |    |
| 0h       |    |    |    |         |    |        |    |
| 7        | 6  | 5  | 4  | 3       | 2  | 1      | 0  |
| RESERVED |    |    |    | TIMEOUT |    | PARITY |    |
| NONE     |    |    |    | R/WD    |    | R/WD   |    |
| 0h       |    |    |    | 0h      |    | 0h     |    |

**Table 5-1393. ECC\_AGGR\_AGGR\_STATUS\_CLR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 3:2  | TIMEOUT  | R/WD | 0h    | 2'b00 - No timeout errors have occurred<br>2'b01 - 1 timeout error has occurred<br>2'b10 - 2 timeout error has occurred<br>2'b11 - 3 or more timeout errors have occurred<br>A write of a non-zero value to this register decrements that many from the timeout fields. If the resulting written value is non zero, then the pending level interrupt stays asserted. A new pulse interrupt will not be asserted, you must write the eoi register for that to occur. If you write a value more than the counter value the result will be zero. |
| 1:0  | PARITY   | R/WD | 0h    | 2'b00 - No parity errors have occurred<br>2'b01 - 1 parity error has occurred<br>2'b10 - 2 parity error has occurred<br>2'b11 - 3 or more parity error have occurred<br>A write of a non-zero value to this register decrements that many from the parity fields. If the resulting written value is non zero, then the pending level interrupt stays asserted. A new pulse interrupt will not be asserted, you must write the eoi register for that to occur. If you write a value more than the counter value the result will be zero.       |



## 5.4 ELM

### ELM

#### 5.4.1 ELM Summaries

#### ELM Summaries

**Table 5-1394. ELM Registers, Base Address=527F 0000h, Length=4096**

| Offset | Length | Register Name                           | ELM0 Physical Address |
|--------|--------|-----------------------------------------|-----------------------|
| 0h     | 32     | <a href="#">ELM_REVISION</a>            | 527F 0000h            |
| 14h    | 32     | <a href="#">ELM_SYSSTS</a>              | 527F 0014h            |
| 18h    | 32     | <a href="#">ELM_IRQSTS</a>              | 527F 0018h            |
| 1Ch    | 32     | <a href="#">ELM_IRQEN</a>               | 527F 001Ch            |
| 20h    | 32     | <a href="#">ELM_LOCATION_CONFIG</a>     | 527F 0020h            |
| 80h    | 32     | <a href="#">ELM_PAGE_CTRL</a>           | 527F 0080h            |
| 400h   | 32     | <a href="#">ELM_SYNDROME_FRAGMENT_0</a> | 527F 0400h + formula  |
| 404h   | 32     | <a href="#">ELM_SYNDROME_FRAGMENT_1</a> | 527F 0404h + formula  |
| 408h   | 32     | <a href="#">ELM_SYNDROME_FRAGMENT_2</a> | 527F 0408h + formula  |
| 40Ch   | 32     | <a href="#">ELM_SYNDROME_FRAGMENT_3</a> | 527F 040Ch + formula  |
| 410h   | 32     | <a href="#">ELM_SYNDROME_FRAGMENT_4</a> | 527F 0410h + formula  |
| 414h   | 32     | <a href="#">ELM_SYNDROME_FRAGMENT_5</a> | 527F 0414h + formula  |
| 418h   | 32     | <a href="#">ELM_SYNDROME_FRAGMENT_6</a> | 527F 0418h + formula  |
| 800h   | 32     | <a href="#">ELM_LOCATION_STS</a>        | 527F 0800h + formula  |
| 880h   | 32     | <a href="#">ELM_ERROR_LOCATION_0</a>    | 527F 0880h + formula  |
| 884h   | 32     | <a href="#">ELM_ERROR_LOCATION_1</a>    | 527F 0884h + formula  |
| 888h   | 32     | <a href="#">ELM_ERROR_LOCATION_2</a>    | 527F 0888h + formula  |
| 88Ch   | 32     | <a href="#">ELM_ERROR_LOCATION_3</a>    | 527F 088Ch + formula  |
| 890h   | 32     | <a href="#">ELM_ERROR_LOCATION_4</a>    | 527F 0890h + formula  |
| 894h   | 32     | <a href="#">ELM_ERROR_LOCATION_5</a>    | 527F 0894h + formula  |
| 898h   | 32     | <a href="#">ELM_ERROR_LOCATION_6</a>    | 527F 0898h + formula  |
| 89Ch   | 32     | <a href="#">ELM_ERROR_LOCATION_7</a>    | 527F 089Ch + formula  |
| 8A0h   | 32     | <a href="#">ELM_ERROR_LOCATION_8</a>    | 527F 08A0h + formula  |
| 8A4h   | 32     | <a href="#">ELM_ERROR_LOCATION_9</a>    | 527F 08A4h + formula  |
| 8A8h   | 32     | <a href="#">ELM_ERROR_LOCATION_10</a>   | 527F 08A8h + formula  |
| 8ACh   | 32     | <a href="#">ELM_ERROR_LOCATION_11</a>   | 527F 08ACh + formula  |
| 8B0h   | 32     | <a href="#">ELM_ERROR_LOCATION_12</a>   | 527F 08B0h + formula  |
| 8B4h   | 32     | <a href="#">ELM_ERROR_LOCATION_13</a>   | 527F 08B4h + formula  |
| 8B8h   | 32     | <a href="#">ELM_ERROR_LOCATION_14</a>   | 527F 08B8h + formula  |
| 8BCh   | 32     | <a href="#">ELM_ERROR_LOCATION_15</a>   | 527F 08BCh + formula  |

#### 5.4.2 ELM Registers

#### ELM Registers

### 5.4.2.1 ELM\_REVISION Register

#### 1 ELM\_REVISION Register (Offset = 0h) [reset = 20h]

This register contains the IP revision code.  
(A write to this register has no effect, the same as the reset).

Return to [Summary Table](#)

**Table 5-1395. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ELM0          | 527F 0000h       |

**Figure 5-464. ELM\_REVISION Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_0 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_0 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_0 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| REV_NUMBER |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 20h        |    |    |    |    |    |    |    |

**Table 5-1397. ELM\_REVISION Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                        |
|------|------------|------|-------|--------------------------------------------------------------------|
| 31:8 | RESERVED_0 | R    | 0h    | Read returns 0                                                     |
| 7:0  | REV_NUMBER | R    | 20h   | IP revision number [RTL] [7:4] Major revision [3:0] Minor revision |

### 5.4.2.2 ELM\_SYSSTS Register

#### 1 ELM\_SYSSTS Register (Offset = 14h) [reset = 0h]

Internal Reset monitoring (OCP domain)

Undefined since:

From HW perspective reset state is 0

From SW user perspective when module is accessible is 1

Return to [Summary Table](#)

**Table 5-1398. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ELM0          | 527F 0014h       |

**Figure 5-465. ELM\_SYSSTS Name Register**

|            |    |    |    |    |    |    |           |
|------------|----|----|----|----|----|----|-----------|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24        |
| RESERVED_0 |    |    |    |    |    |    |           |
| R          |    |    |    |    |    |    |           |
| 0h         |    |    |    |    |    |    |           |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16        |
| RESERVED_0 |    |    |    |    |    |    |           |
| R          |    |    |    |    |    |    |           |
| 0h         |    |    |    |    |    |    |           |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8         |
| RESERVED_0 |    |    |    |    |    |    |           |
| R          |    |    |    |    |    |    |           |
| 0h         |    |    |    |    |    |    |           |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0         |
| RESERVED_0 |    |    |    |    |    |    | RESETDONE |
| R          |    |    |    |    |    |    | R         |
| 0h         |    |    |    |    |    |    | 0h        |

**Table 5-1400. ELM\_SYSSTS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                   |
|------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED_0 | R    | 0h    | Reserved                                                                                                                                                      |
| 0    | RESETDONE  | R    | 0h    | Internal Reset monitoring (OCP domain)<br>Undefined since:<br>From HW perspective reset state is 0<br>From SW user perspective when module is accessible is 1 |

### 5.4.2.3 ELM\_IRQSTS Register

#### 1 ELM\_IRQSTS Register (Offset = 18h) [reset = 0h]

Interrupt status. This register doubles as a status register for the error location processes.

Return to [Summary Table](#)

**Table 5-1401. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ELM0          | 527F 0018h       |

**Figure 5-466. ELM\_IRQSTS Name Register**

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 31          | 30          | 29          | 28          | 27          | 26          | 25          | 24          |
| RESERVED_0  |             |             |             |             |             |             |             |
| R           |             |             |             |             |             |             |             |
| 0h          |             |             |             |             |             |             |             |
| 23          | 22          | 21          | 20          | 19          | 18          | 17          | 16          |
| RESERVED_0  |             |             |             |             |             |             |             |
| R           |             |             |             |             |             |             |             |
| 0h          |             |             |             |             |             |             |             |
| 15          | 14          | 13          | 12          | 11          | 10          | 9           | 8           |
| RESERVED_0  |             |             |             |             |             |             | PAGE_VALID  |
| R           |             |             |             |             |             |             | R/W1TC      |
| 0h          |             |             |             |             |             |             | 0h          |
| 7           | 6           | 5           | 4           | 3           | 2           | 1           | 0           |
| LOC_VALID_7 | LOC_VALID_6 | LOC_VALID_5 | LOC_VALID_4 | LOC_VALID_3 | LOC_VALID_2 | LOC_VALID_1 | LOC_VALID_0 |
| R/W1TC      | R/W1TC      | R/W1TC      | R/W1TC      | R/W1TC      | R/W1TC      | R/W1TC      | R/W1TC      |
| 0h          | 0h          | 0h          | 0h          | 0h          | 0h          | 0h          | 0h          |

**Table 5-1403. ELM\_IRQSTS Register Field Descriptions**

| Bit  | Field       | Type   | Reset | Description                                                                                                                                                                                                                                                          |
|------|-------------|--------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:9 | RESERVED_0  | R      | 0h    | Reserved                                                                                                                                                                                                                                                             |
| 8    | PAGE_VALID  | R/W1TC | 0h    | Error location status for a full page, based on the mask definition<br>Read 0x0: error locations invalid for all polynomials enabled in the ECC_INTERRUPT_MASK register<br>Read 0x1: all error locations valid<br>Write 0x0: no effect<br>Write 0x1: clear interrupt |
| 7    | LOC_VALID_7 | R/W1TC | 0h    | Error location status for syndrome polynomial 7<br>Read 0x0: no syndrome processed or process in progress<br>Read 0x1: error location process completed<br>Write 0x0: no effect<br>Write 0x1: clear interrupt                                                        |
| 6    | LOC_VALID_6 | R/W1TC | 0h    | Error location status for syndrome polynomial 6                                                                                                                                                                                                                      |
| 5    | LOC_VALID_5 | R/W1TC | 0h    | Error location status for syndrome polynomial 5                                                                                                                                                                                                                      |
| 4    | LOC_VALID_4 | R/W1TC | 0h    | Error location status for syndrome polynomial 4                                                                                                                                                                                                                      |
| 3    | LOC_VALID_3 | R/W1TC | 0h    | Error location status for syndrome polynomial 3                                                                                                                                                                                                                      |
| 2    | LOC_VALID_2 | R/W1TC | 0h    | Error location status for syndrome polynomial 2                                                                                                                                                                                                                      |
| 1    | LOC_VALID_1 | R/W1TC | 0h    | Error location status for syndrome polynomial 1                                                                                                                                                                                                                      |
| 0    | LOC_VALID_0 | R/W1TC | 0h    | Error location status for syndrome polynomial 0                                                                                                                                                                                                                      |

#### 5.4.2.4 ELM\_IRQEN Register

##### 1 ELM\_IRQEN Register (Offset = 1Ch) [reset = 0h]

Interrupt enable.

Return to [Summary Table](#)

**Table 5-1404. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ELM0          | 527F 001Ch       |

**Figure 5-467. ELM\_IRQEN Name Register**

|                     |                     |                     |                     |                     |                     |                     |                     |
|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| 31                  | 30                  | 29                  | 28                  | 27                  | 26                  | 25                  | 24                  |
| RESERVED_0          |                     |                     |                     |                     |                     |                     |                     |
| R                   |                     |                     |                     |                     |                     |                     |                     |
| 0h                  |                     |                     |                     |                     |                     |                     |                     |
| 23                  | 22                  | 21                  | 20                  | 19                  | 18                  | 17                  | 16                  |
| RESERVED_0          |                     |                     |                     |                     |                     |                     |                     |
| R                   |                     |                     |                     |                     |                     |                     |                     |
| 0h                  |                     |                     |                     |                     |                     |                     |                     |
| 15                  | 14                  | 13                  | 12                  | 11                  | 10                  | 9                   | 8                   |
| RESERVED_0          |                     |                     |                     |                     |                     |                     | PAGE_MASK           |
| R                   |                     |                     |                     |                     |                     |                     | R/W                 |
| 0h                  |                     |                     |                     |                     |                     |                     | 0h                  |
| 7                   | 6                   | 5                   | 4                   | 3                   | 2                   | 1                   | 0                   |
| LOCATION_MA<br>SK_7 | LOCATION_MA<br>SK_6 | LOCATION_MA<br>SK_5 | LOCATION_MA<br>SK_4 | LOCATION_MA<br>SK_3 | LOCATION_MA<br>SK_2 | LOCATION_MA<br>SK_1 | LOCATION_MA<br>SK_0 |
| R/W                 | R/W                 | R/W                 | R/W                 | R/W                 | R/W                 | R/W                 | R/W                 |
| 0h                  | 0h                  | 0h                  | 0h                  | 0h                  | 0h                  | 0h                  | 0h                  |

**Table 5-1406. ELM\_IRQEN Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                              |
|------|-----------------|------|-------|----------------------------------------------------------------------------------------------------------|
| 31:9 | RESERVED_0      | R    | 0h    | Reserved                                                                                                 |
| 8    | PAGE_MASK       | R/W  | 0h    | Page interrupt mask bit<br>0:disable interrupt<br>1:enable interrupt                                     |
| 7    | LOCATION_MASK_7 | R/W  | 0h    | Error location interrupt mask bit for syndrome polynomial 7                                              |
| 6    | LOCATION_MASK_6 | R/W  | 0h    | Error location interrupt mask bit for syndrome polynomial 6                                              |
| 5    | LOCATION_MASK_5 | R/W  | 0h    | Error location interrupt mask bit for syndrome polynomial 5                                              |
| 4    | LOCATION_MASK_4 | R/W  | 0h    | Error location interrupt mask bit for syndrome polynomial 4                                              |
| 3    | LOCATION_MASK_3 | R/W  | 0h    | Error location interrupt mask bit for syndrome polynomial 3                                              |
| 2    | LOCATION_MASK_2 | R/W  | 0h    | Error location interrupt mask bit for syndrome polynomial 2                                              |
| 1    | LOCATION_MASK_1 | R/W  | 0h    | Error location interrupt mask bit for syndrome polynomial 1                                              |
| 0    | LOCATION_MASK_0 | R/W  | 0h    | Error location interrupt mask bit for syndrome polynomial 0<br>0:disable interrupt<br>1:enable interrupt |

### 5.4.2.5 ELM\_LOCATION\_CONFIG Register

#### 1 ELM\_LOCATION\_CONFIG Register (Offset = 20h) [reset = 0h]

ECC algorithm parameters.

Return to [Summary Table](#)

**Table 5-1407. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ELM0          | 527F 0020h       |

**Figure 5-468. ELM\_LOCATION\_CONFIG Name Register**

|            |    |    |    |    |    |               |    |
|------------|----|----|----|----|----|---------------|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25            | 24 |
| RESERVED_1 |    |    |    |    |    | ECC_SIZE      |    |
| R          |    |    |    |    |    | R/W           |    |
| 0h         |    |    |    |    |    | 0h            |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17            | 16 |
| ECC_SIZE   |    |    |    |    |    |               |    |
| R/W        |    |    |    |    |    |               |    |
| 0h         |    |    |    |    |    |               |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9             | 8  |
| RESERVED_0 |    |    |    |    |    |               |    |
| R          |    |    |    |    |    |               |    |
| 0h         |    |    |    |    |    |               |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1             | 0  |
| RESERVED_0 |    |    |    |    |    | ECC_BCH_LEVEL |    |
| R          |    |    |    |    |    | R/W           |    |
| 0h         |    |    |    |    |    | 0h            |    |

**Table 5-1409. ELM\_LOCATION\_CONFIG Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                     |
|-------|---------------|------|-------|-----------------------------------------------------------------------------------------------------------------|
| 31:27 | RESERVED_1    | R    | 0h    | Reserved                                                                                                        |
| 26:16 | ECC_SIZE      | R/W  | 0h    | Maximum size of the buffers for which the error location engine is used, in number of nibbles [4-bits entities] |
| 15:2  | RESERVED_0    | R    | 0h    | Reserved                                                                                                        |
| 1:0   | ECC_BCH_LEVEL | R/W  | 0h    | Error correction level 0x0: 4 bits 0x1: 8 bits 0x2: 16 bits 0x3: reserved                                       |

### 5.4.2.6 ELM\_PAGE\_CTRL Register

#### 1 ELM\_PAGE\_CTRL Register (Offset = 80h) [reset = 0h]

Page definition.

Return to [Summary Table](#)

**Table 5-1410. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ELM0          | 527F 0080h       |

**Figure 5-469. ELM\_PAGE\_CTRL Name Register**

|            |          |          |          |          |          |          |          |
|------------|----------|----------|----------|----------|----------|----------|----------|
| 31         | 30       | 29       | 28       | 27       | 26       | 25       | 24       |
| RESERVED_0 |          |          |          |          |          |          |          |
| R          |          |          |          |          |          |          |          |
| 0h         |          |          |          |          |          |          |          |
| 23         | 22       | 21       | 20       | 19       | 18       | 17       | 16       |
| RESERVED_0 |          |          |          |          |          |          |          |
| R          |          |          |          |          |          |          |          |
| 0h         |          |          |          |          |          |          |          |
| 15         | 14       | 13       | 12       | 11       | 10       | 9        | 8        |
| RESERVED_0 |          |          |          |          |          |          |          |
| R          |          |          |          |          |          |          |          |
| 0h         |          |          |          |          |          |          |          |
| 7          | 6        | 5        | 4        | 3        | 2        | 1        | 0        |
| SECTOR_7   | SECTOR_6 | SECTOR_5 | SECTOR_4 | SECTOR_3 | SECTOR_2 | SECTOR_1 | SECTOR_0 |
| R/W        | R/W      | R/W      | R/W      | R/W      | R/W      | R/W      | R/W      |
| 0h         | 0h       | 0h       | 0h       | 0h       | 0h       | 0h       | 0h       |

**Table 5-1412. ELM\_PAGE\_CTRL Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                        |
|------|------------|------|-------|----------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED_0 | R    | 0h    | Reserved                                                                                           |
| 7    | SECTOR_7   | R/W  | 0h    | Set to 1 if syndrome polynomial 7 is part of the page in page mode<br>Must be 0 in continuous mode |
| 6    | SECTOR_6   | R/W  | 0h    | Set to 1 if syndrome polynomial 6 is part of the page in page mode<br>Must be 0 in continuous mode |
| 5    | SECTOR_5   | R/W  | 0h    | Set to 1 if syndrome polynomial 5 is part of the page in page mode<br>Must be 0 in continuous mode |
| 4    | SECTOR_4   | R/W  | 0h    | Set to 1 if syndrome polynomial 4 is part of the page in page mode<br>Must be 0 in continuous mode |
| 3    | SECTOR_3   | R/W  | 0h    | Set to 1 if syndrome polynomial 3 is part of the page in page mode<br>Must be 0 in continuous mode |
| 2    | SECTOR_2   | R/W  | 0h    | Set to 1 if syndrome polynomial 2 is part of the page in page mode<br>Must be 0 in continuous mode |
| 1    | SECTOR_1   | R/W  | 0h    | Set to 1 if syndrome polynomial 1 is part of the page in page mode<br>Must be 0 in continuous mode |
| 0    | SECTOR_0   | R/W  | 0h    | Set to 1 if syndrome polynomial 0 is part of the page in page mode<br>Must be 0 in continuous mode |

### 5.4.2.7 ELM\_SYNDROME\_FRAGMENT\_0 Register

#### 1 ELM\_SYNDROME\_FRAGMENT\_0 Register (Offset = 400h) [reset = 0h]

Input syndrome polynomial bits 0 to 31.

Return to [Summary Table](#)

Offset = Base + (j \* 40h); where j = 0 to 7d

**Table 5-1413. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ELM0          | 527F 0400h + formula |

**Figure 5-470. ELM\_SYNDROME\_FRAGMENT\_0 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SYNDROME_0 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SYNDROME_0 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SYNDROME_0 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SYNDROME_0 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-1415. ELM\_SYNDROME\_FRAGMENT\_0 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description           |
|------|------------|------|-------|-----------------------|
| 31:0 | SYNDROME_0 | R/W  | 0h    | Syndrome bits 0 to 31 |



### 5.4.2.8 ELM\_SYNDROME\_FRAGMENT\_1 Register

#### 1 ELM\_SYNDROME\_FRAGMENT\_1 Register (Offset = 404h) [reset = 0h]

Input syndrome polynomial bits 32 to 63.

Return to [Summary Table](#)

Offset = Base + (j \* 40h); where j = 0 to 7d

**Table 5-1416. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ELM0          | 527F 0404h + formula |

**Figure 5-471. ELM\_SYNDROME\_FRAGMENT\_1 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SYNDROME_1 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SYNDROME_1 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SYNDROME_1 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SYNDROME_1 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-1418. ELM\_SYNDROME\_FRAGMENT\_1 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description            |
|------|------------|------|-------|------------------------|
| 31:0 | SYNDROME_1 | R/W  | 0h    | Syndrome bits 32 to 63 |

### 5.4.2.9 ELM\_SYNDROME\_FRAGMENT\_2 Register

#### 1 ELM\_SYNDROME\_FRAGMENT\_2 Register (Offset = 408h) [reset = 0h]

Input syndrome polynomial bits 64 to 95.

Return to [Summary Table](#)

Offset = Base + (j \* 40h); where j = 0 to 7d

**Table 5-1419. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ELM0          | 527F 0408h + formula |

**Figure 5-472. ELM\_SYNDROME\_FRAGMENT\_2 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SYNDROME_2 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SYNDROME_2 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SYNDROME_2 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SYNDROME_2 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-1421. ELM\_SYNDROME\_FRAGMENT\_2 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description            |
|------|------------|------|-------|------------------------|
| 31:0 | SYNDROME_2 | R/W  | 0h    | Syndrome bits 64 to 95 |

### 5.4.2.10 ELM\_SYNDROME\_FRAGMENT\_3 Register

#### 1 ELM\_SYNDROME\_FRAGMENT\_3 Register (Offset = 40Ch) [reset = 0h]

Input syndrome polynomial bits 96 to 127

Return to [Summary Table](#)

Offset = Base + (j \* 40h); where j = 0 to 7d

**Table 5-1422. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ELM0          | 527F 040Ch + formula |

**Figure 5-473. ELM\_SYNDROME\_FRAGMENT\_3 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SYNDROME_3 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SYNDROME_3 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SYNDROME_3 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SYNDROME_3 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-1424. ELM\_SYNDROME\_FRAGMENT\_3 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description             |
|------|------------|------|-------|-------------------------|
| 31:0 | SYNDROME_3 | R/W  | 0h    | Syndrome bits 96 to 127 |

### 5.4.2.11 ELM\_SYNDROME\_FRAGMENT\_4 Register

#### 1 ELM\_SYNDROME\_FRAGMENT\_4 Register (Offset = 410h) [reset = 0h]

Input syndrome polynomial bits 128 to 159.

Return to [Summary Table](#)

Offset = Base + (j \* 40h); where j = 0 to 7d

**Table 5-1425. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ELM0          | 527F 0410h + formula |

**Figure 5-474. ELM\_SYNDROME\_FRAGMENT\_4 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SYNDROME_4 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SYNDROME_4 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SYNDROME_4 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SYNDROME_4 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-1427. ELM\_SYNDROME\_FRAGMENT\_4 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description              |
|------|------------|------|-------|--------------------------|
| 31:0 | SYNDROME_4 | R/W  | 0h    | Syndrome bits 128 to 159 |

### 5.4.2.12 ELM\_SYNDROME\_FRAGMENT\_5 Register

#### 1 ELM\_SYNDROME\_FRAGMENT\_5 Register (Offset = 414h) [reset = 0h]

Input syndrome polynomial bits 160 to 191.

Return to [Summary Table](#)

Offset = Base + (j \* 40h); where j = 0 to 7d

**Table 5-1428. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ELM0          | 527F 0414h + formula |

**Figure 5-475. ELM\_SYNDROME\_FRAGMENT\_5 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SYNDROME_5 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SYNDROME_5 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SYNDROME_5 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SYNDROME_5 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-1430. ELM\_SYNDROME\_FRAGMENT\_5 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description              |
|------|------------|------|-------|--------------------------|
| 31:0 | SYNDROME_5 | R/W  | 0h    | Syndrome bits 160 to 191 |

### 5.4.2.13 ELM\_SYNDROME\_FRAGMENT\_6 Register

#### 1 ELM\_SYNDROME\_FRAGMENT\_6 Register (Offset = 418h) [reset = 0h]

Input syndrome polynomial bits 192 to 207.

Return to [Summary Table](#)

Offset = Base + (j \* 40h); where j = 0 to 7d

**Table 5-1431. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ELM0          | 527F 0418h + formula |

**Figure 5-476. ELM\_SYNDROME\_FRAGMENT\_6 Name Register**

|            |    |    |    |    |    |    |                    |
|------------|----|----|----|----|----|----|--------------------|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24                 |
| RESERVED   |    |    |    |    |    |    |                    |
| R          |    |    |    |    |    |    |                    |
| 0h         |    |    |    |    |    |    |                    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16                 |
| RESERVED   |    |    |    |    |    |    | SYNDROME_V<br>ALID |
| R          |    |    |    |    |    |    | R/W                |
| 0h         |    |    |    |    |    |    | 0h                 |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8                  |
| SYNDROME_6 |    |    |    |    |    |    |                    |
| R/W        |    |    |    |    |    |    |                    |
| 0h         |    |    |    |    |    |    |                    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0                  |
| SYNDROME_6 |    |    |    |    |    |    |                    |
| R/W        |    |    |    |    |    |    |                    |
| 0h         |    |    |    |    |    |    |                    |

**Table 5-1433. ELM\_SYNDROME\_FRAGMENT\_6 Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                              |
|-------|----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------|
| 31:17 | RESERVED       | R    | 0h    | Reserved                                                                                                                 |
| 16    | SYNDROME_VALID | R/W  | 0h    | Syndrome valid bit 0x0: this syndrome polynomial should not be processed 0x1: this syndrome polynomial must be processed |
| 15:0  | SYNDROME_6     | R/W  | 0h    | Syndrome bits 192 to 207                                                                                                 |

### 5.4.2.14 ELM\_LOCATION\_STS Register

#### 1 ELM\_LOCATION\_STS Register (Offset = 800h) [reset = 0h]

Exit status for the syndrome polynomial processing

Return to [Summary Table](#)

Offset = Base + (j \* 100h); where j = 0 to 7d

**Table 5-1434. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ELM0          | 527F 0800h + formula |

**Figure 5-477. ELM\_LOCATION\_STS Name Register**

|            |    |    |               |    |    |    |                     |
|------------|----|----|---------------|----|----|----|---------------------|
| 31         | 30 | 29 | 28            | 27 | 26 | 25 | 24                  |
| RESERVED_0 |    |    |               |    |    |    |                     |
| R          |    |    |               |    |    |    |                     |
| 0h         |    |    |               |    |    |    |                     |
| 23         | 22 | 21 | 20            | 19 | 18 | 17 | 16                  |
| RESERVED_0 |    |    |               |    |    |    |                     |
| R          |    |    |               |    |    |    |                     |
| 0h         |    |    |               |    |    |    |                     |
| 15         | 14 | 13 | 12            | 11 | 10 | 9  | 8                   |
| RESERVED_0 |    |    |               |    |    |    | ECC_CORREC<br>TABLE |
| R          |    |    |               |    |    |    | R                   |
| 0h         |    |    |               |    |    |    | 0h                  |
| 7          | 6  | 5  | 4             | 3  | 2  | 1  | 0                   |
| RESERVED_1 |    |    | ECC_NB_ERRORS |    |    |    |                     |
| R          |    |    | R             |    |    |    |                     |
| 0h         |    |    | 0h            |    |    |    |                     |

**Table 5-1436. ELM\_LOCATION\_STS Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                                                                                                                         |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:9 | RESERVED_0      | R    | 0h    | Reserved                                                                                                                                                                                                            |
| 8    | ECC_CORRECTABLE | R    | 0h    | Error location process exit status 0x0: ECC error location process failed Number of errors and error locations are invalid 0x1: all errors were successfully located Number of errors and error locations are valid |
| 7:5  | RESERVED_1      | R    | 0h    | Reserved                                                                                                                                                                                                            |
| 4:0  | ECC_NB_ERRORS   | R    | 0h    | Number of errors detected and located                                                                                                                                                                               |

### 5.4.2.15 ELM\_ERROR\_LOCATION\_0 Register

#### 1 ELM\_ERROR\_LOCATION\_0 Register (Offset = 880h) [reset = 0h]

Error location register

Return to [Summary Table](#)

Offset = Base + (j \* 100h); where j = 0 to 7d

**Table 5-1437. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ELM0          | 527F 0880h + formula |

**Figure 5-478. ELM\_ERROR\_LOCATION\_0 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED_0         |    |    |    | ECC_ERROR_LOCATION |    |    |    |
| R                  |    |    |    | R                  |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| ECC_ERROR_LOCATION |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 5-1439. ELM\_ERROR\_LOCATION\_0 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                |
|-------|--------------------|------|-------|----------------------------|
| 31:13 | RESERVED_0         | R    | 0h    | Reserved                   |
| 12:0  | ECC_ERROR_LOCATION | R    | 0h    | Error location bit address |



### 5.4.2.16 ELM\_ERROR\_LOCATION\_1 Register

#### 1 ELM\_ERROR\_LOCATION\_1 Register (Offset = 884h) [reset = 0h]

Error location register

Return to [Summary Table](#)

Offset = Base + (j \* 100h); where j = 0 to 7d

**Table 5-1440. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ELM0          | 527F 0884h + formula |

**Figure 5-479. ELM\_ERROR\_LOCATION\_1 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED_0         |    |    |    | ECC_ERROR_LOCATION |    |    |    |
| R                  |    |    |    | R                  |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| ECC_ERROR_LOCATION |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 5-1442. ELM\_ERROR\_LOCATION\_1 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                |
|-------|--------------------|------|-------|----------------------------|
| 31:13 | RESERVED_0         | R    | 0h    | Reserved                   |
| 12:0  | ECC_ERROR_LOCATION | R    | 0h    | Error location bit address |

### 5.4.2.17 ELM\_ERROR\_LOCATION\_2 Register

#### 1 ELM\_ERROR\_LOCATION\_2 Register (Offset = 888h) [reset = 0h]

Error location register

Return to [Summary Table](#)

Offset = Base + (j \* 100h); where j = 0 to 7d

**Table 5-1443. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ELM0          | 527F 0888h + formula |

**Figure 5-480. ELM\_ERROR\_LOCATION\_2 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED_0         |    |    |    | ECC_ERROR_LOCATION |    |    |    |
| R                  |    |    |    | R                  |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| ECC_ERROR_LOCATION |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 5-1445. ELM\_ERROR\_LOCATION\_2 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                |
|-------|--------------------|------|-------|----------------------------|
| 31:13 | RESERVED_0         | R    | 0h    | Reserved                   |
| 12:0  | ECC_ERROR_LOCATION | R    | 0h    | Error location bit address |

### 5.4.2.18 ELM\_ERROR\_LOCATION\_3 Register

#### 1 ELM\_ERROR\_LOCATION\_3 Register (Offset = 88Ch) [reset = 0h]

Error location register

Return to [Summary Table](#)

Offset = Base + (j \* 100h); where j = 0 to 7d

**Table 5-1446. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ELM0          | 527F 088Ch + formula |

**Figure 5-481. ELM\_ERROR\_LOCATION\_3 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED_0         |    |    |    | ECC_ERROR_LOCATION |    |    |    |
| R                  |    |    |    | R                  |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| ECC_ERROR_LOCATION |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 5-1448. ELM\_ERROR\_LOCATION\_3 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                |
|-------|--------------------|------|-------|----------------------------|
| 31:13 | RESERVED_0         | R    | 0h    | Reserved                   |
| 12:0  | ECC_ERROR_LOCATION | R    | 0h    | Error location bit address |

### 5.4.2.19 ELM\_ERROR\_LOCATION\_4 Register

#### 1 ELM\_ERROR\_LOCATION\_4 Register (Offset = 890h) [reset = 0h]

Error location register

Return to [Summary Table](#)

Offset = Base + (j \* 100h); where j = 0 to 7d

**Table 5-1449. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ELM0          | 527F 0890h + formula |

**Figure 5-482. ELM\_ERROR\_LOCATION\_4 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED_0         |    |    |    | ECC_ERROR_LOCATION |    |    |    |
| R                  |    |    |    | R                  |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| ECC_ERROR_LOCATION |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 5-1451. ELM\_ERROR\_LOCATION\_4 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                |
|-------|--------------------|------|-------|----------------------------|
| 31:13 | RESERVED_0         | R    | 0h    | Reserved                   |
| 12:0  | ECC_ERROR_LOCATION | R    | 0h    | Error location bit address |

### 5.4.2.20 ELM\_ERROR\_LOCATION\_5 Register

#### 1 ELM\_ERROR\_LOCATION\_5 Register (Offset = 894h) [reset = 0h]

Error location register

Return to [Summary Table](#)

Offset = Base + (j \* 100h); where j = 0 to 7d

**Table 5-1452. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ELM0          | 527F 0894h + formula |

**Figure 5-483. ELM\_ERROR\_LOCATION\_5 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED_0         |    |    |    | ECC_ERROR_LOCATION |    |    |    |
| R                  |    |    |    | R                  |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| ECC_ERROR_LOCATION |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 5-1454. ELM\_ERROR\_LOCATION\_5 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                |
|-------|--------------------|------|-------|----------------------------|
| 31:13 | RESERVED_0         | R    | 0h    | Reserved                   |
| 12:0  | ECC_ERROR_LOCATION | R    | 0h    | Error location bit address |

### 5.4.2.21 ELM\_ERROR\_LOCATION\_6 Register

#### 1 ELM\_ERROR\_LOCATION\_6 Register (Offset = 898h) [reset = 0h]

Error location register

Return to [Summary Table](#)

Offset = Base + (j \* 100h); where j = 0 to 7d

**Table 5-1455. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ELM0          | 527F 0898h + formula |

**Figure 5-484. ELM\_ERROR\_LOCATION\_6 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED_0         |    |    |    | ECC_ERROR_LOCATION |    |    |    |
| R                  |    |    |    | R                  |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| ECC_ERROR_LOCATION |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 5-1457. ELM\_ERROR\_LOCATION\_6 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                |
|-------|--------------------|------|-------|----------------------------|
| 31:13 | RESERVED_0         | R    | 0h    | Reserved                   |
| 12:0  | ECC_ERROR_LOCATION | R    | 0h    | Error location bit address |

### 5.4.2.22 ELM\_ERROR\_LOCATION\_7 Register

#### 1 ELM\_ERROR\_LOCATION\_7 Register (Offset = 89Ch) [reset = 0h]

Error location register

Return to [Summary Table](#)

Offset = Base + (j \* 100h); where j = 0 to 7d

**Table 5-1458. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ELM0          | 527F 089Ch + formula |

**Figure 5-485. ELM\_ERROR\_LOCATION\_7 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED_0         |    |    |    | ECC_ERROR_LOCATION |    |    |    |
| R                  |    |    |    | R                  |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| ECC_ERROR_LOCATION |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 5-1460. ELM\_ERROR\_LOCATION\_7 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                |
|-------|--------------------|------|-------|----------------------------|
| 31:13 | RESERVED_0         | R    | 0h    | Reserved                   |
| 12:0  | ECC_ERROR_LOCATION | R    | 0h    | Error location bit address |

### 5.4.2.23 ELM\_ERROR\_LOCATION\_8 Register

#### 1 ELM\_ERROR\_LOCATION\_8 Register (Offset = 8A0h) [reset = 0h]

Error location register

Return to [Summary Table](#)

Offset = Base + (j \* 100h); where j = 0 to 7d

**Table 5-1461. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ELM0          | 527F 08A0h + formula |

**Figure 5-486. ELM\_ERROR\_LOCATION\_8 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED_0         |    |    |    | ECC_ERROR_LOCATION |    |    |    |
| R                  |    |    |    | R                  |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| ECC_ERROR_LOCATION |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 5-1463. ELM\_ERROR\_LOCATION\_8 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                |
|-------|--------------------|------|-------|----------------------------|
| 31:13 | RESERVED_0         | R    | 0h    | Reserved                   |
| 12:0  | ECC_ERROR_LOCATION | R    | 0h    | Error location bit address |



### 5.4.2.24 ELM\_ERROR\_LOCATION\_9 Register

#### 1 ELM\_ERROR\_LOCATION\_9 Register (Offset = 8A4h) [reset = 0h]

Error location register

Return to [Summary Table](#)

Offset = Base + (j \* 100h); where j = 0 to 7d

**Table 5-1464. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ELM0          | 527F 08A4h + formula |

**Figure 5-487. ELM\_ERROR\_LOCATION\_9 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED_0         |    |    |    | ECC_ERROR_LOCATION |    |    |    |
| R                  |    |    |    | R                  |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| ECC_ERROR_LOCATION |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 5-1466. ELM\_ERROR\_LOCATION\_9 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                |
|-------|--------------------|------|-------|----------------------------|
| 31:13 | RESERVED_0         | R    | 0h    | Reserved                   |
| 12:0  | ECC_ERROR_LOCATION | R    | 0h    | Error location bit address |

### 5.4.2.25 ELM\_ERROR\_LOCATION\_10 Register

#### 1 ELM\_ERROR\_LOCATION\_10 Register (Offset = 8A8h) [reset = 0h]

Error location register

Return to [Summary Table](#)

Offset = Base + (j \* 100h); where j = 0 to 7d

**Table 5-1467. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ELM0          | 527F 08A8h + formula |

**Figure 5-488. ELM\_ERROR\_LOCATION\_10 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED_0         |    |    |    | ECC_ERROR_LOCATION |    |    |    |
| R                  |    |    |    | R                  |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| ECC_ERROR_LOCATION |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 5-1469. ELM\_ERROR\_LOCATION\_10 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                |
|-------|--------------------|------|-------|----------------------------|
| 31:13 | RESERVED_0         | R    | 0h    | Reserved                   |
| 12:0  | ECC_ERROR_LOCATION | R    | 0h    | Error location bit address |

### 5.4.2.26 ELM\_ERROR\_LOCATION\_11 Register

#### 1 ELM\_ERROR\_LOCATION\_11 Register (Offset = 8ACh) [reset = 0h]

Error location register

Return to [Summary Table](#)

Offset = Base + (j \* 100h); where j = 0 to 7d

**Table 5-1470. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ELM0          | 527F 08ACh + formula |

**Figure 5-489. ELM\_ERROR\_LOCATION\_11 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED_0         |    |    |    | ECC_ERROR_LOCATION |    |    |    |
| R                  |    |    |    | R                  |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| ECC_ERROR_LOCATION |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 5-1472. ELM\_ERROR\_LOCATION\_11 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                |
|-------|--------------------|------|-------|----------------------------|
| 31:13 | RESERVED_0         | R    | 0h    | Reserved                   |
| 12:0  | ECC_ERROR_LOCATION | R    | 0h    | Error location bit address |

### 5.4.2.27 ELM\_ERROR\_LOCATION\_12 Register

#### 1 ELM\_ERROR\_LOCATION\_12 Register (Offset = 8B0h) [reset = 0h]

Error location register

Return to [Summary Table](#)

Offset = Base + (j \* 100h); where j = 0 to 7d

**Table 5-1473. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ELM0          | 527F 08B0h + formula |

**Figure 5-490. ELM\_ERROR\_LOCATION\_12 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED_0         |    |    |    | ECC_ERROR_LOCATION |    |    |    |
| R                  |    |    |    | R                  |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| ECC_ERROR_LOCATION |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 5-1475. ELM\_ERROR\_LOCATION\_12 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                |
|-------|--------------------|------|-------|----------------------------|
| 31:13 | RESERVED_0         | R    | 0h    | Reserved                   |
| 12:0  | ECC_ERROR_LOCATION | R    | 0h    | Error location bit address |

### 5.4.2.28 ELM\_ERROR\_LOCATION\_13 Register

#### 1 ELM\_ERROR\_LOCATION\_13 Register (Offset = 8B4h) [reset = 0h]

Error location register

Return to [Summary Table](#)

Offset = Base + (j \* 100h); where j = 0 to 7d

**Table 5-1476. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ELM0          | 527F 08B4h + formula |

**Figure 5-491. ELM\_ERROR\_LOCATION\_13 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED_0         |    |    |    | ECC_ERROR_LOCATION |    |    |    |
| R                  |    |    |    | R                  |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| ECC_ERROR_LOCATION |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 5-1478. ELM\_ERROR\_LOCATION\_13 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                |
|-------|--------------------|------|-------|----------------------------|
| 31:13 | RESERVED_0         | R    | 0h    | Reserved                   |
| 12:0  | ECC_ERROR_LOCATION | R    | 0h    | Error location bit address |

### 5.4.2.29 ELM\_ERROR\_LOCATION\_14 Register

#### 1 ELM\_ERROR\_LOCATION\_14 Register (Offset = 8B8h) [reset = 0h]

Error location register

Return to [Summary Table](#)

Offset = Base + (j \* 100h); where j = 0 to 7d

**Table 5-1479. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ELM0          | 527F 08B8h + formula |

**Figure 5-492. ELM\_ERROR\_LOCATION\_14 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED_0         |    |    |    | ECC_ERROR_LOCATION |    |    |    |
| R                  |    |    |    | R                  |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| ECC_ERROR_LOCATION |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 5-1481. ELM\_ERROR\_LOCATION\_14 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                |
|-------|--------------------|------|-------|----------------------------|
| 31:13 | RESERVED_0         | R    | 0h    | Reserved                   |
| 12:0  | ECC_ERROR_LOCATION | R    | 0h    | Error location bit address |

### 5.4.2.30 ELM\_ERROR\_LOCATION\_15 Register

#### 1 ELM\_ERROR\_LOCATION\_15 Register (Offset = 8BCh) [reset = 0h]

Error location register

Return to [Summary Table](#)

Offset = Base + (j \* 100h); where j = 0 to 7d

**Table 5-1482. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ELM0          | 527F 08BCh + formula |

**Figure 5-493. ELM\_ERROR\_LOCATION\_15 Name Register**

|                    |    |    |    |                    |    |    |    |
|--------------------|----|----|----|--------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                 | 26 | 25 | 24 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 23                 | 22 | 21 | 20 | 19                 | 18 | 17 | 16 |
| RESERVED_0         |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9  | 8  |
| RESERVED_0         |    |    |    | ECC_ERROR_LOCATION |    |    |    |
| R                  |    |    |    | R                  |    |    |    |
| 0h                 |    |    |    | 0h                 |    |    |    |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1  | 0  |
| ECC_ERROR_LOCATION |    |    |    |                    |    |    |    |
| R                  |    |    |    |                    |    |    |    |
| 0h                 |    |    |    |                    |    |    |    |

**Table 5-1484. ELM\_ERROR\_LOCATION\_15 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                |
|-------|--------------------|------|-------|----------------------------|
| 31:13 | RESERVED_0         | R    | 0h    | Reserved                   |
| 12:0  | ECC_ERROR_LOCATION | R    | 0h    | Error location bit address |

## 5.5 ESM

### ESM

#### 5.5.1 ESM Summaries

#### ESM Summaries

**Table 5-1485. ESM Registers, Base Address=52D0 0000h, Length=2048**

| Offset | Length | Register Name                                                      | ESM0 Physical Address |
|--------|--------|--------------------------------------------------------------------|-----------------------|
| 0h     | 32     | <a href="#">ESM_PID</a>                                            | 52D0 0000h            |
| 4h     | 32     | <a href="#">ESM_INFO</a>                                           | 52D0 0004h            |
| 8h     | 32     | <a href="#">ESM_EN</a>                                             | 52D0 0008h            |
| Ch     | 32     | <a href="#">ESM_SFT_RST</a>                                        | 52D0 000Ch            |
| 10h    | 32     | <a href="#">ESM_ERR_RAW</a>                                        | 52D0 0010h            |
| 14h    | 32     | <a href="#">ESM_ERR_STS</a>                                        | 52D0 0014h            |
| 18h    | 32     | <a href="#">ESM_ERR_EN_SET</a>                                     | 52D0 0018h            |
| 1Ch    | 32     | <a href="#">ESM_ERR_EN_CLR</a>                                     | 52D0 001Ch            |
| 20h    | 32     | <a href="#">ESM_LOW_PRI</a>                                        | 52D0 0020h            |
| 24h    | 32     | <a href="#">ESM_HI_PRI</a>                                         | 52D0 0024h            |
| 28h    | 32     | <a href="#">ESM_LOW</a>                                            | 52D0 0028h            |
| 2Ch    | 32     | <a href="#">ESM_HI</a>                                             | 52D0 002Ch            |
| 30h    | 32     | <a href="#">ESM_EOI</a>                                            | 52D0 0030h            |
| 40h    | 32     | <a href="#">ESM_PIN_CTRL</a>                                       | 52D0 0040h            |
| 44h    | 32     | <a href="#">ESM_PIN_STS</a>                                        | 52D0 0044h            |
| 48h    | 32     | <a href="#">ESM_PIN_CNTR</a>                                       | 52D0 0048h            |
| 4Ch    | 32     | <a href="#">ESM_PIN_CNTR_PRE</a>                                   | 52D0 004Ch            |
| 50h    | 32     | <a href="#">ESM_PWMH_PIN_CNTR</a>                                  | 52D0 0050h            |
| 54h    | 32     | <a href="#">ESM_PWMH_PIN_CNTR_PRE</a>                              | 52D0 0054h            |
| 58h    | 32     | <a href="#">ESM_PWML_PIN_CNTR</a>                                  | 52D0 0058h            |
| 5Ch    | 32     | <a href="#">ESM_PWML_PIN_CNTR_PRE</a>                              | 52D0 005Ch            |
| 400h   | 32     | <a href="#">ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_RAW_J</a>         | 52D0 0400h + formula  |
| 404h   | 32     | <a href="#">ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_STS_J</a>         | 52D0 0404h + formula  |
| 408h   | 32     | <a href="#">ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_INTR_EN_SET_J</a> | 52D0 0408h + formula  |
| 40Ch   | 32     | <a href="#">ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_INTR_EN_CLR_J</a> | 52D0 040Ch + formula  |
| 410h   | 32     | <a href="#">ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_INT_PRIO_J</a>    | 52D0 0410h + formula  |
| 414h   | 32     | <a href="#">ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_PIN_EN_SET_J</a>  | 52D0 0414h + formula  |
| 418h   | 32     | <a href="#">ESM_PCR_GENERATED_MEMORY_MAP_ERR_GRP_PIN_EN_CLR_J</a>  | 52D0 0418h + formula  |

#### 5.5.2 ESM Registers

#### ESM Registers



### 5.5.2.1 ESM\_PID Register

#### 1 ESM\_PID Register (Offset = 0h) [reset = 6FE04900h]

The Revision Register contains the major and minor revisions for the module.

Return to [Summary Table](#)

**Table 5-1486. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ESM0          | 52D0 0000h       |

**Figure 5-494. ESM\_PID Name Register**

|        |    |       |    |      |       |    |    |
|--------|----|-------|----|------|-------|----|----|
| 31     | 30 | 29    | 28 | 27   | 26    | 25 | 24 |
| SCHEME |    | BU    |    | FUNC |       |    |    |
| R      |    | R     |    | R    |       |    |    |
| 1h     |    | 2h    |    | FE0h |       |    |    |
| 23     | 22 | 21    | 20 | 19   | 18    | 17 | 16 |
| FUNC   |    |       |    |      |       |    |    |
| R      |    |       |    |      |       |    |    |
| FE0h   |    |       |    |      |       |    |    |
| 15     | 14 | 13    | 12 | 11   | 10    | 9  | 8  |
| RTL    |    |       |    |      | MAJOR |    |    |
| R      |    |       |    |      | R     |    |    |
| 9h     |    |       |    |      | 1h    |    |    |
| 7      | 6  | 5     | 4  | 3    | 2     | 1  | 0  |
| CUSTOM |    | MINOR |    |      |       |    |    |
| R      |    | R     |    |      |       |    |    |
| 0h     |    | 0h    |    |      |       |    |    |

**Table 5-1488. ESM\_PID Register Field Descriptions**

| Bit   | Field  | Type | Reset | Description                                   |
|-------|--------|------|-------|-----------------------------------------------|
| 31:30 | SCHEME | R    | 1h    | PID register scheme                           |
| 29:28 | BU     | R    | 2h    | Business Unit: 10 = Processors                |
| 27:16 | FUNC   | R    | FE0h  | Module ID                                     |
| 15:11 | RTL    | R    | 9h    | RTL revision. Will vary depending on release. |
| 10:8  | MAJOR  | R    | 1h    | Major revision                                |
| 7:6   | CUSTOM | R    | 0h    | Custom                                        |
| 5:0   | MINOR  | R    | 0h    | Minor revision                                |

### 5.5.2.2 ESM\_INFO Register

#### 1 ESM\_INFO Register (Offset = 4h) [reset = 103h]

The Info Register gives the configuration Information of this ESM.

Return to [Summary Table](#)

**Table 5-1489. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ESM0          | 52D0 0004h       |

**Figure 5-495. ESM\_INFO Name Register**

|              |    |          |    |    |    |    |    |
|--------------|----|----------|----|----|----|----|----|
| 31           | 30 | 29       | 28 | 27 | 26 | 25 | 24 |
| LAST_RESET   |    | RESERVED |    |    |    |    |    |
| R            |    | NONE     |    |    |    |    |    |
| 0h           |    | 0h       |    |    |    |    |    |
| 23           | 22 | 21       | 20 | 19 | 18 | 17 | 16 |
| RESERVED     |    |          |    |    |    |    |    |
| NONE         |    |          |    |    |    |    |    |
| 0h           |    |          |    |    |    |    |    |
| 15           | 14 | 13       | 12 | 11 | 10 | 9  | 8  |
| PULSE_GROUPS |    |          |    |    |    |    |    |
| R            |    |          |    |    |    |    |    |
| 1h           |    |          |    |    |    |    |    |
| 7            | 6  | 5        | 4  | 3  | 2  | 1  | 0  |
| GROUPS       |    |          |    |    |    |    |    |
| R            |    |          |    |    |    |    |    |
| 3h           |    |          |    |    |    |    |    |

**Table 5-1491. ESM\_INFO Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                            |
|-------|--------------|------|-------|------------------------------------------------------------------------------------------------------------------------|
| 31    | LAST_RESET   | R    | 0h    | Indicates the Source of the last Reset<br>1'b0 : Last reset was a Power On Reset<br>1'b1 : Last reset was a Warm Reset |
| 30:16 | RESERVED     | NONE | 0h    | Reserved                                                                                                               |
| 15:8  | PULSE_GROUPS | R    | 1h    | Number of Pulse Error Groups                                                                                           |
| 7:0   | GROUPS       | R    | 3h    | Total number of Error Groups                                                                                           |

### 5.5.2.3 ESM\_EN Register

#### 1 ESM\_EN Register (Offset = 8h) [reset = 0h]

The Global Enable Register has the master interrupt mask.

Return to [Summary Table](#)

**Table 5-1492. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ESM0          | 52D0 0008h       |

**Figure 5-496. ESM\_EN Name Register**

|          |    |    |    |     |    |    |    |
|----------|----|----|----|-----|----|----|----|
| 31       | 30 | 29 | 28 | 27  | 26 | 25 | 24 |
| RESERVED |    |    |    |     |    |    |    |
| NONE     |    |    |    |     |    |    |    |
| 0h       |    |    |    |     |    |    |    |
| 23       | 22 | 21 | 20 | 19  | 18 | 17 | 16 |
| RESERVED |    |    |    |     |    |    |    |
| NONE     |    |    |    |     |    |    |    |
| 0h       |    |    |    |     |    |    |    |
| 15       | 14 | 13 | 12 | 11  | 10 | 9  | 8  |
| RESERVED |    |    |    |     |    |    |    |
| NONE     |    |    |    |     |    |    |    |
| 0h       |    |    |    |     |    |    |    |
| 7        | 6  | 5  | 4  | 3   | 2  | 1  | 0  |
| RESERVED |    |    |    | KEY |    |    |    |
| NONE     |    |    |    | R/W |    |    |    |
| 0h       |    |    |    | 0h  |    |    |    |

**Table 5-1494. ESM\_EN Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                    |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                       |
| 3:0  | KEY      | R/W  | 0h    | This field is a global mask to all interrupts. It is reset by the warm reset. The purpose is to leave all of the raw status and per-interrupt enable bits alone so that, after a warm reset, software may observe the state of the ESM before the warm reset and try to debug what may have caused the reset.<br>4'b0000: All events are disabled<br>4'b1111: All events are enabled<br>All others are invalid |

### 5.5.2.4 ESM\_SFT\_RST Register

#### 1 ESM\_SFT\_RST Register (Offset = Ch) [reset = 0h]

The Global Soft Reset Register controls the global clear for raw status and enables.

Return to [Summary Table](#)

**Table 5-1495. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ESM0          | 52D0 000Ch       |

**Figure 5-497. ESM\_SFT\_RST Name Register**

|          |    |    |    |     |    |    |    |
|----------|----|----|----|-----|----|----|----|
| 31       | 30 | 29 | 28 | 27  | 26 | 25 | 24 |
| RESERVED |    |    |    |     |    |    |    |
| NONE     |    |    |    |     |    |    |    |
| 0h       |    |    |    |     |    |    |    |
| 23       | 22 | 21 | 20 | 19  | 18 | 17 | 16 |
| RESERVED |    |    |    |     |    |    |    |
| NONE     |    |    |    |     |    |    |    |
| 0h       |    |    |    |     |    |    |    |
| 15       | 14 | 13 | 12 | 11  | 10 | 9  | 8  |
| RESERVED |    |    |    |     |    |    |    |
| NONE     |    |    |    |     |    |    |    |
| 0h       |    |    |    |     |    |    |    |
| 7        | 6  | 5  | 4  | 3   | 2  | 1  | 0  |
| RESERVED |    |    |    | KEY |    |    |    |
| NONE     |    |    |    | W   |    |    |    |
| 0h       |    |    |    | 0h  |    |    |    |

**Table 5-1497. ESM\_SFT\_RST Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                 |
|------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                    |
| 3:0  | KEY      | W    | 0h    | Writing to this field can cause all of the raw status and all enables to be cleared. This can be used to reset the ESM state after debugging because of a warm reset.<br>Write:<br>4'b1111: Clear all raw status and enable bits<br>All others no effect<br>Read:<br>Always read as 4'b0000 |

### 5.5.2.5 ESM\_ERR\_RAW Register

#### 1 ESM\_ERR\_RAW Register (Offset = 10h) [reset = 0h]

Raw Status/Set Register for Configuration Errors.

Return to [Summary Table](#)

**Table 5-1498. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ESM0          | 52D0 0010h       |

**Figure 5-498. ESM\_ERR\_RAW Name Register**

|          |    |    |    |    |    |        |    |
|----------|----|----|----|----|----|--------|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25     | 24 |
| RESERVED |    |    |    |    |    |        |    |
| NONE     |    |    |    |    |    |        |    |
| 0h       |    |    |    |    |    |        |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17     | 16 |
| RESERVED |    |    |    |    |    |        |    |
| NONE     |    |    |    |    |    |        |    |
| 0h       |    |    |    |    |    |        |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9      | 8  |
| RESERVED |    |    |    |    |    |        |    |
| NONE     |    |    |    |    |    |        |    |
| 0h       |    |    |    |    |    |        |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1      | 0  |
| RESERVED |    |    |    |    |    | STS    |    |
| NONE     |    |    |    |    |    | R/W1TS |    |
| 0h       |    |    |    |    |    | 0h     |    |

**Table 5-1500. ESM\_ERR\_RAW Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|----------|--------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED | NONE   | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                               |
| 2:0  | STS      | R/W1TS | 0h    | This is the raw status for errors in the configuration for Group N. This field is only reset by a Power-On-Reset and not by warm reset. A global soft reset will set this field to 0<br>Read:<br>1'b0:Inactive<br>1'b1:Active/Pending<br>Write 1'b1 to set event raw status<br>Bits associated with groups that are not implemented in a certain configuration are Reserved, Read as 0 and writes will have no effect. |

### 5.5.2.6 ESM\_ERR\_STS Register

#### 1 ESM\_ERR\_STS Register (Offset = 14h) [reset = 0h]

Config Error Enable and Clear Register.

Return to [Summary Table](#)

**Table 5-1501. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ESM0          | 52D0 0014h       |

**Figure 5-499. ESM\_ERR\_STS Name Register**

|          |    |    |    |    |        |    |    |
|----------|----|----|----|----|--------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26     | 25 | 24 |
| RESERVED |    |    |    |    |        |    |    |
| NONE     |    |    |    |    |        |    |    |
| 0h       |    |    |    |    |        |    |    |
| 23       | 22 | 21 | 20 | 19 | 18     | 17 | 16 |
| RESERVED |    |    |    |    |        |    |    |
| NONE     |    |    |    |    |        |    |    |
| 0h       |    |    |    |    |        |    |    |
| 15       | 14 | 13 | 12 | 11 | 10     | 9  | 8  |
| RESERVED |    |    |    |    |        |    |    |
| NONE     |    |    |    |    |        |    |    |
| 0h       |    |    |    |    |        |    |    |
| 7        | 6  | 5  | 4  | 3  | 2      | 1  | 0  |
| RESERVED |    |    |    |    | MSK    |    |    |
| NONE     |    |    |    |    | R/W1TC |    |    |
| 0h       |    |    |    |    | 0h     |    |    |

**Table 5-1503. ESM\_ERR\_STS Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------|----------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED | NONE   | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 2:0  | MSK      | R/W1TC | 0h    | This is the masked status for errors in the configuration for Group N. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0.<br>Read:<br>1'b0:Inactive<br>1'b1:Active/Pending and Enabled<br>Write 1'b1 to clear event raw status.<br>Bits associated with groups that are not implemented in a certain configuration are Reserved, Read as 0 and writes will have no effect |

### 5.5.2.7 ESM\_ERR\_EN\_SET Register

#### 1 ESM\_ERR\_EN\_SET Register (Offset = 18h) [reset = 0h]

Config Error Enable Set Register.

Return to [Summary Table](#)

**Table 5-1504. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ESM0          | 52D0 0018h       |

**Figure 5-500. ESM\_ERR\_EN\_SET Name Register**

|          |    |    |    |    |        |    |    |
|----------|----|----|----|----|--------|----|----|
| 31       | 30 | 29 | 28 | 27 | 26     | 25 | 24 |
| RESERVED |    |    |    |    |        |    |    |
| NONE     |    |    |    |    |        |    |    |
| 0h       |    |    |    |    |        |    |    |
| 23       | 22 | 21 | 20 | 19 | 18     | 17 | 16 |
| RESERVED |    |    |    |    |        |    |    |
| NONE     |    |    |    |    |        |    |    |
| 0h       |    |    |    |    |        |    |    |
| 15       | 14 | 13 | 12 | 11 | 10     | 9  | 8  |
| RESERVED |    |    |    |    |        |    |    |
| NONE     |    |    |    |    |        |    |    |
| 0h       |    |    |    |    |        |    |    |
| 7        | 6  | 5  | 4  | 3  | 2      | 1  | 0  |
| RESERVED |    |    |    |    | MSK    |    |    |
| NONE     |    |    |    |    | R/W1TS |    |    |
| 0h       |    |    |    |    | 0h     |    |    |

**Table 5-1506. ESM\_ERR\_EN\_SET Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|----------|--------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED | NONE   | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 2:0  | MSK      | R/W1TS | 0h    | <p>This is the mask enable for errors in the configuration for Group N. If the corresponding bit and the global_enable are set, then then interrupt is unmasked. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0.</p> <p>Read:<br/>1'b0:Disabled<br/>1'b1:Enabled</p> <p>Write 1'b1 to set enable</p> <p>Bits associated with groups that are not implemented in a certain configuration are Reserved, Read as 0 and writes will have no effect.</p> |

### 5.5.2.8 ESM\_ERR\_EN\_CLR Register

#### 1 ESM\_ERR\_EN\_CLR Register (Offset = 1Ch) [reset = 0h]

Config Error Interrupt Enabled Clear register.

Return to [Summary Table](#)

**Table 5-1507. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ESM0          | 52D0 001Ch       |

**Figure 5-501. ESM\_ERR\_EN\_CLR Name Register**

|          |    |    |    |    |    |        |    |
|----------|----|----|----|----|----|--------|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25     | 24 |
| RESERVED |    |    |    |    |    |        |    |
| NONE     |    |    |    |    |    |        |    |
| 0h       |    |    |    |    |    |        |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17     | 16 |
| RESERVED |    |    |    |    |    |        |    |
| NONE     |    |    |    |    |    |        |    |
| 0h       |    |    |    |    |    |        |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9      | 8  |
| RESERVED |    |    |    |    |    |        |    |
| NONE     |    |    |    |    |    |        |    |
| 0h       |    |    |    |    |    |        |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1      | 0  |
| RESERVED |    |    |    |    |    | MSK    |    |
| NONE     |    |    |    |    |    | R/W1TC |    |
| 0h       |    |    |    |    |    | 0h     |    |

**Table 5-1509. ESM\_ERR\_EN\_CLR Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|------|----------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED | NONE   | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 2:0  | MSK      | R/W1TC | 0h    | <p>This is the mask clear for errors in the configuration for Group N. If the corresponding bit and the global_enable are set, then then interrupt is unmasked. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0.</p> <p>Read:<br/>1'b0:Disabled<br/>1'b1:Enabled</p> <p>Write 1'b1 to clear enable</p> <p>Bits associated with groups that are not implemented in a certain configuration are Reserved, Read as 0 and writes will have no effect.</p> |



### 5.5.2.9 ESM\_LOW\_PRI Register

#### 1 ESM\_LOW\_PRI Register (Offset = 20h) [reset = FFFFFFFFh]

Shows which is the highest priority outstanding low priority interrupt.

Return to [Summary Table](#)

**Table 5-1510. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ESM0          | 52D0 0020h       |

**Figure 5-502. ESM\_LOW\_PRI Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PLS   |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PLS   |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| LVL   |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LVL   |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |

**Table 5-1512. ESM\_LOW\_PRI Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | PLS   | R    | FFFFh | Indicates what the highest priority Low Priority interrupt caused by a pulse number is. The lowest event has the highest priority. i.e. if Global Events 0, 1, 2, 3, and 4 are pending, and Global Event 0, and 1 are configured for High Priority while Global Events 2, 3, and 4 are configured for Low Priority, then the value of this field will be 0x2. A value of all ones (0xFFFF) indicates that there are no low priority interrupts pending. This field is updated whenever a new, higher priority event comes in. Software cannot read this field multiple times during an interrupt service routine to keep track of which interrupt is being serviced, because this field may have been updated with a higher priority event. |
| 15:0  | LVL   | R    | FFFFh | Indicates what the highest priority Low Priority interrupt caused by a level number is. The lowest event has the highest priority. i.e. if Global Events 0, 1, 2, 3, and 4 are pending, and Global Event 0, and 1 are configured for High Priority while Global Events 2, 3, and 4 are configured for Low Priority, then the value of this field will be 0x2. A value of all ones (0xFFFF) indicates that there are no low priority interrupts pending. This field is updated whenever a new, higher priority event comes in. Software cannot read this field multiple times during an interrupt service routine to keep track of which interrupt is being serviced, because this field may have been updated with a higher priority event. |

### 5.5.2.10 ESM\_HI\_PRI Register

#### 1 ESM\_HI\_PRI Register (Offset = 24h) [reset = FFFFFFFFh]

Shows which is the highest priority outstanding high priority interrupt.

Return to [Summary Table](#)

**Table 5-1513. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ESM0          | 52D0 0024h       |

**Figure 5-503. ESM\_HI\_PRI Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PLS   |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PLS   |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| LVL   |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| LVL   |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |

**Table 5-1515. ESM\_HI\_PRI Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | PLS   | R    | FFFFh | Indicates what the highest priority High Priority interrupt caused by a pulse number is. The lowest event has the highest priority. i.e. if Global Events 0, 1, 2, 3, and 4 are pending, and Global Event 0, and 1 are configured for High Priority while Global Events 2, 3, and 4 are configured for Low Priority, then the value of this field will be 0x0. A value of all ones (0xFFFF) indicates that there are no high priority interrupts pending. This field is updated whenever a new, higher priority event comes in. Software cannot read this field multiple times during an interrupt service routine to keep track of which interrupt is being serviced, because this field may have been updated with a higher priority event. |
| 15:0  | LVL   | R    | FFFFh | Indicates what the highest priority Low Priority interrupt caused by a level number is. The lowest event has the highest priority. i.e. if Global Events 0, 1, 2, 3, and 4 are pending, and Global Event 0, and 1 are configured for High Priority while Global Events 2, 3, and 4 are configured for Low Priority, then the value of this field will be 0x0. A value of all ones (0xFFFF) indicates that there are no high priority interrupts pending. This field is updated whenever a new, higher priority event comes in. Software cannot read this field multiple times during an interrupt service routine to keep track of which interrupt is being serviced, because this field may have been updated with a higher priority event.  |

### 5.5.2.11 ESM\_LOW Register

#### 1 ESM\_LOW Register (Offset = 28h) [reset = 0h]

Shows which groups have outstanding low priority interrupts.

Return to [Summary Table](#)

**Table 5-1516. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ESM0          | 52D0 0028h       |

**Figure 5-504. ESM\_LOW Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| STS |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| STS |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| STS |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| STS |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 5-1518. ESM\_LOW Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                 |
|------|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | STS   | R    | 0h    | Indicates which Event Groups have one or more Low Priority interrupts pending. This register is bit oriented where bit 0 is for Event Group 0, bit 1 is for Event Group 1, etc (bit N is for Event Group N) |

### 5.5.2.12 ESM\_HI Register

#### 1 ESM\_HI Register (Offset = 2Ch) [reset = 0h]

Shows which groups have outstanding high priority interrupts.

Return to [Summary Table](#)

**Table 5-1519. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ESM0          | 52D0 002Ch       |

**Figure 5-505. ESM\_HI Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| STS |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| STS |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| STS |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| STS |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 5-1521. ESM\_HI Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                  |
|------|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | STS   | R    | 0h    | Indicates which Event Groups have one or more High Priority interrupts pending. This register is bit oriented where bit 0 is for Event Group 0, bit 1 is for Event Group 1, etc (bit N is for Event Group N) |

### 5.5.2.13 ESM\_EOI Register

#### 1 ESM\_EOI Register (Offset = 30h) [reset = 0h]

End of Interrupt Register.

Return to [Summary Table](#)

**Table 5-1522. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ESM0          | 52D0 0030h       |

**Figure 5-506. ESM\_EOI Name Register**

|          |    |    |    |    |    |     |    |
|----------|----|----|----|----|----|-----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25  | 24 |
| RESERVED |    |    |    |    |    |     |    |
| NONE     |    |    |    |    |    |     |    |
| 0h       |    |    |    |    |    |     |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17  | 16 |
| RESERVED |    |    |    |    |    |     |    |
| NONE     |    |    |    |    |    |     |    |
| 0h       |    |    |    |    |    |     |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9   | 8  |
| RESERVED |    |    |    |    |    | KEY |    |
| NONE     |    |    |    |    |    | W   |    |
| 0h       |    |    |    |    |    | 0h  |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1   | 0  |
| KEY      |    |    |    |    |    |     |    |
| W        |    |    |    |    |    |     |    |
| 0h       |    |    |    |    |    |     |    |

**Table 5-1524. ESM\_EOI Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                             |
|-------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:11 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                |
| 10:0  | KEY      | W    | 0h    | Writing the corresponding vector to this field will cause a re-evaluation of interrupts. If, when the vector is written, there are still pending interrupts, a new pulse will be generated.<br>0 : Configuration Error Interrupt<br>1 : Low Priority Error Interrupt<br>2 : High Priority Error Interrupt<br>3<br>2047:Reserved (writes have no effect) |

### 5.5.2.14 ESM\_PIN\_CTRL Register

#### 1 ESM\_PIN\_CTRL Register (Offset = 40h) [reset = 0h]

This register controls the error\_pin\_n output.

Return to [Summary Table](#)

**Table 5-1525. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ESM0          | 52D0 0040h       |

**Figure 5-507. ESM\_PIN\_CTRL Name Register**

|          |    |    |    |     |    |    |    |
|----------|----|----|----|-----|----|----|----|
| 31       | 30 | 29 | 28 | 27  | 26 | 25 | 24 |
| RESERVED |    |    |    |     |    |    |    |
| NONE     |    |    |    |     |    |    |    |
| 0h       |    |    |    |     |    |    |    |
| 23       | 22 | 21 | 20 | 19  | 18 | 17 | 16 |
| RESERVED |    |    |    |     |    |    |    |
| NONE     |    |    |    |     |    |    |    |
| 0h       |    |    |    |     |    |    |    |
| 15       | 14 | 13 | 12 | 11  | 10 | 9  | 8  |
| RESERVED |    |    |    |     |    |    |    |
| NONE     |    |    |    |     |    |    |    |
| 0h       |    |    |    |     |    |    |    |
| 7        | 6  | 5  | 4  | 3   | 2  | 1  | 0  |
| PWM_EN   |    |    |    | KEY |    |    |    |
| R/W      |    |    |    | R/W |    |    |    |
| 0h       |    |    |    | 0h  |    |    |    |

**Table 5-1527. ESM\_PIN\_CTRL Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                               |
|------|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                  |
| 7:4  | PWM_EN   | R/W  | 0h    | PWM mode enable. This field should only be modified when the ESM is disabled, from the Global Enable register. This field is only reset by a Power-On-Reset (not warm reset).<br>4'b0000:Error output pin is a level<br>4'b1111:Error output pin is a PWM signal<br>All other are invalid |

**Table 5-1527. ESM\_PIN\_CTRL Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-----|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0 | KEY   | R/W  | 0h    | <p>This field controls behavior of the Error Pin. Note, during reset the field is 4'b0000, but the Error Pin is asserted (active low). Immediately after reset, the Error Pin de-asserts. This field is only reset by a Power-On-Reset (not warm reset).</p> <p>4'b0000 : Normal Mode - Error Pin will activate when an enabled Error Event occurs</p> <p>4'b1010 : Force Error Mode - Forces the Error Pin active. To clear the Error Pin (return to the ESM_IDLE state) write this field back to Normal Mode (Writing a CLEAR event will also work). You may only write to Force Error Mode while in IDLE. Attempting Force Error while in another state will have no effect</p> <p>4'b0101 : CLEAR Event - generates a CLEAR event to the ESM state machine. key will return to Normal Mode (4'b0000) on the next cycle.</p> <p>All Other Values - Normal Mode. Writing any of these values will have no effect. Reading any of these values indicate that one or more bits have experienced a single event upset and software should write the field back to 4'b0000. The ESM will continue to operate in Normal Mode</p> |

### 5.5.2.15 ESM\_PIN\_STS Register

#### 1 ESM\_PIN\_STS Register (Offset = 44h) [reset = 0h]

This register reflects the status of the error\_pin\_n output.

Return to [Summary Table](#)

**Table 5-1528. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ESM0          | 52D0 0044h       |

**Figure 5-508. ESM\_PIN\_STS Name Register**

|          |    |    |    |    |    |    |     |
|----------|----|----|----|----|----|----|-----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24  |
| RESERVED |    |    |    |    |    |    |     |
| NONE     |    |    |    |    |    |    |     |
| 0h       |    |    |    |    |    |    |     |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16  |
| RESERVED |    |    |    |    |    |    |     |
| NONE     |    |    |    |    |    |    |     |
| 0h       |    |    |    |    |    |    |     |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8   |
| RESERVED |    |    |    |    |    |    |     |
| NONE     |    |    |    |    |    |    |     |
| 0h       |    |    |    |    |    |    |     |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0   |
| RESERVED |    |    |    |    |    |    | VAL |
| NONE     |    |    |    |    |    |    | R   |
| 0h       |    |    |    |    |    |    | 0h  |

**Table 5-1530. ESM\_PIN\_STS Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 0    | VAL      | R    | 0h    | This field indicates the status of the Error Pin as looped back from the I/O. This field reflects the state of SAFETY_ERRORn I/O.<br>1'b1 - De-Asserted<br>1'b0 - Asserted<br>Note, while in reset the error pin is actually active (asserted low), but goes inactive immediately after the de-assertion of Power-on-Reset. Hence, the value that will be read after Power-on-Reset is 1, but may be 0 after a warm reset. |



### 5.5.2.16 ESM\_PIN\_CNTR Register

#### 1 ESM\_PIN\_CNTR Register (Offset = 48h) [reset = 30D40h]

This register shows the current value of the error pin counter.

Return to [Summary Table](#)

**Table 5-1531. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ESM0          | 52D0 0048h       |

**Figure 5-509. ESM\_PIN\_CNTR Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT    |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 30D40h   |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT    |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 30D40h   |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT    |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 30D40h   |    |    |    |    |    |    |    |

**Table 5-1533. ESM\_PIN\_CNTR Register Field Descriptions**

| Bit   | Field    | Type | Reset  | Description                                                                                                                                                                                                                                                                                                                                        |
|-------|----------|------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED | NONE | 0h     | Reserved                                                                                                                                                                                                                                                                                                                                           |
| 23:0  | COUNT    | R    | 30D40h | This field indicates the current value of the Time Interval Counter. Register is reloaded to the counter preload value on entry to the ESM_ERROR state from ESM_IDLE and counts down by one per clock cycle. Once the counter has reached 0, the Minimum Time Interval has expired. This field is only reset by a Power-On-Reset (not warm reset). |

### 5.5.2.17 ESM\_PIN\_CNTR\_PRE Register

#### 1 ESM\_PIN\_CNTR\_PRE Register (Offset = 4Ch) [reset = 30D40h]

This register contains the value that is loaded in to the Error Counter.

Return to [Summary Table](#)

**Table 5-1534. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ESM0          | 52D0 004Ch       |

**Figure 5-510. ESM\_PIN\_CNTR\_PRE Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 30D40h   |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 30D40h   |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 30D40h   |    |    |    |    |    |    |    |

**Table 5-1536. ESM\_PIN\_CNTR\_PRE Register Field Descriptions**

| Bit   | Field    | Type | Reset  | Description                                                                                                                                                                                                                        |
|-------|----------|------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED | NONE | 0h     | Reserved                                                                                                                                                                                                                           |
| 23:0  | COUNT    | R/W  | 30D40h | This is the value that will be loaded in to the counter field of the Error Pin Counter Value Register whenever the ESM enters the ESM_ERROR state from ESM_IDLE.<br>This field is only reset by a Power-On-Reset (not warm reset). |

### 5.5.2.18 ESM\_PWMH\_PIN\_CNTR Register

#### 1 ESM\_PWMH\_PIN\_CNTR Register (Offset = 50h) [reset = 186A0h]

This register shows the current value of the error pin PWM high counter.

Return to [Summary Table](#)

**Table 5-1537. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ESM0          | 52D0 0050h       |

**Figure 5-511. ESM\_PWMH\_PIN\_CNTR Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT    |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 186A0h   |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT    |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 186A0h   |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT    |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 186A0h   |    |    |    |    |    |    |    |

**Table 5-1539. ESM\_PWMH\_PIN\_CNTR Register Field Descriptions**

| Bit   | Field    | Type | Reset  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|----------|------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED | NONE | 0h     | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 23:0  | COUNT    | R    | 186A0h | This field indicates the current value of the PWM High Time Interval Counter. The reset value is the 24'h0186A0. If pwm_en is set to PWM mode, then this register is enabled. This register is reloaded to the PWM high PIN_CNTR_PRE.count value when the error output pin toggles high. It will decrement by 1 each cycle when the error output pin is high. Once the counter has reached 0, the error output pin will toggle low. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 24'h0186A0 |

### 5.5.2.19 ESM\_PWMH\_PIN\_CNTR\_PRE Register

#### 1 ESM\_PWMH\_PIN\_CNTR\_PRE Register (Offset = 54h) [reset = 186A0h]

This register contains the value that is loaded in to the Error PWM High Counter.

Return to [Summary Table](#)

**Table 5-1540. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ESM0          | 52D0 0054h       |

**Figure 5-512. ESM\_PWMH\_PIN\_CNTR\_PRE Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 186A0h   |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 186A0h   |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 186A0h   |    |    |    |    |    |    |    |

**Table 5-1542. ESM\_PWMH\_PIN\_CNTR\_PRE Register Field Descriptions**

| Bit   | Field    | Type | Reset  | Description                                                                                                                                                                                                                                                                         |
|-------|----------|------|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED | NONE | 0h     | Reserved                                                                                                                                                                                                                                                                            |
| 23:0  | COUNT    | R/W  | 186A0h | This is the value that will be loaded in to the counter field of the Error Pin PWM High Counter Value Register whenever the error output pin toggles high.<br>This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 24'h0186A0. |

### 5.5.2.20 ESM\_PWML\_PIN\_CNTR Register

#### 1 ESM\_PWML\_PIN\_CNTR Register (Offset = 58h) [reset = 186A0h]

This register shows the current value of the error pin PWM low counter.

Return to [Summary Table](#)

**Table 5-1543. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ESM0          | 52D0 0058h       |

**Figure 5-513. ESM\_PWML\_PIN\_CNTR Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT    |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 186A0h   |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT    |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 186A0h   |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT    |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 186A0h   |    |    |    |    |    |    |    |

**Table 5-1545. ESM\_PWML\_PIN\_CNTR Register Field Descriptions**

| Bit   | Field    | Type | Reset  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|----------|------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED | NONE | 0h     | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 23:0  | COUNT    | R    | 186A0h | This field indicates the current value of the PWM Low Time Interval Counter. The reset value is the 24'h0186A0. If pwm_en is set to PWM mode, then this register is enabled. This register is reloaded to the PWM low counter_preload value when the error output pin toggles low. It will decrement by 1 each cycle when the error output pin is low. Once the counter has reached 0, the error output pin will toggle high. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 24'h0186A0. |

### 5.5.2.21 ESM\_PWML\_PIN\_CNTR\_PRE Register

#### 1 ESM\_PWML\_PIN\_CNTR\_PRE Register (Offset = 5Ch) [reset = 186A0h]

This register contains the value that is loaded in to the Error PWM Low Counter.

Return to [Summary Table](#)

**Table 5-1546. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| ESM0          | 52D0 005Ch       |

**Figure 5-514. ESM\_PWML\_PIN\_CNTR\_PRE Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COUNT    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 186A0h   |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COUNT    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 186A0h   |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COUNT    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 186A0h   |    |    |    |    |    |    |    |

**Table 5-1548. ESM\_PWML\_PIN\_CNTR\_PRE Register Field Descriptions**

| Bit   | Field    | Type | Reset  | Description                                                                                                                                                                                                                                                                       |
|-------|----------|------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED | NONE | 0h     | Reserved                                                                                                                                                                                                                                                                          |
| 23:0  | COUNT    | R/W  | 186A0h | This is the value that will be loaded in to the counter field of the Error Pin PWM Low Counter Value Register whenever the error output pin toggles low.<br>This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 24'h0186A0. |

### 5.5.2.22 ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_RAW\_J Register

#### 1 ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_RAW\_J Register (Offset = 400h) [reset = 0h]

Raw Status/Set Register for Group A Errors

Return to [Summary Table](#)

Offset = Base + (j \* 20h); where j = 0 to 2d

**Table 5-1549. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ESM0          | 52D0 0400h + formula |

**Figure 5-515. ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_RAW\_J Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| STS    |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| STS    |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| STS    |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| STS    |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-1551. ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_RAW\_J Register Field Descriptions**

| Bit  | Field | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|------|-------|--------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | STS   | R/W1TS | 0h    | <p>This is the raw status of the events in group N. Each bit corresponds to event Q where Q = N*32+Bit (Example: bit 0 is event N*32+0, bit 1 is N*32 + 1 etc).</p> <p>For Level events, the raw status is the event input synchronized to the ESM clock and stored in a multi-bit (for redundancy) internal register.</p> <p>For Pulse events, the raw status is multi-bit (for redundancy) internal register that is set when two of the three edge detection circuits on the redundant event capture a rising edge.</p> <p>This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0.</p> <p>Read:<br/>1'b0: Inactive<br/>1'b1: Active/Pending<br/>Write 1'b1 to set interrupt raw status</p> |

### 5.5.2.23 ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_STS\_J Register

#### 1 ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_STS\_J Register (Offset = 404h) [reset = 0h]

Error Enable and Clear Register

Return to [Summary Table](#)

Offset = Base + (j \* 20h); where j = 0 to 2d

**Table 5-1552. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ESM0          | 52D0 0404h + formula |

**Figure 5-516. ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_STS\_J Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSK    |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSK    |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSK    |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSK    |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-1554. ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_STS\_J Register Field Descriptions**

| Bit  | Field | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|-------|--------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSK   | R/W1TC | 0h    | <p>This is the masked status of the events in group N. Each bit corresponds to event Q where Q = N*32+Bit (Example: bit 0 is event N*32+0, bit 1 is N*32 + 1 etc...).</p> <p>This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0.</p> <p>Read:</p> <p>1'b0: Inactive</p> <p>1'b1: Active/Pending</p> <p>Write 1'b1 to clear interrupt raw status</p> |



### 5.5.2.24 ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_INTR\_EN\_SET\_J Register

**1 ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_INTR\_EN\_SET\_J Register (Offset = 408h) [reset = 0h]**

Level Error Enable Set Register

Return to [Summary Table](#)

Offset = Base + (j \* 20h); where j = 0 to 2d

**Table 5-1555. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ESM0          | 52D0 0408h + formula |

**Figure 5-517. ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_INTR\_EN\_SET\_J Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSK    |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSK    |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSK    |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSK    |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-1557. ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_INTR\_EN\_SET\_J Register Field Descriptions**

| Bit  | Field | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                     |
|------|-------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSK   | R/W1TS | 0h    | This field is used to enable the mask of events in group N. Each bit corresponds to event Q where Q = N*32+Bit.<br>If the corresponding bit and the global_enable are set, then the interrupt is unmasked. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0.<br>Read:<br>1'b0: Disabled<br>1'b1: Enabled<br>Write 1'b1 to set enable |

### 5.5.2.25 ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_INTR\_EN\_CLR\_J Register

#### 1 ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_INTR\_EN\_CLR\_J Register (Offset = 40Ch) [reset = 0h]

Level Error Interrupt Enabled Clear register

Return to [Summary Table](#)

Offset = Base + (j \* 20h); where j = 0 to 2d

**Table 5-1558. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ESM0          | 52D0 040Ch + formula |

**Figure 5-518. ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_INTR\_EN\_CLR\_J Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSK    |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSK    |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSK    |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSK    |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-1560. ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_INTR\_EN\_CLR\_J Register Field Descriptions**

| Bit  | Field | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                         |
|------|-------|--------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSK   | R/W1TC | 0h    | This field is used to disable the mask of events in group N. Each bit corresponds to event Q where Q = N*32+Bit.<br>If the corresponding bit and the global_enable are set, then then interrupt is unmasked. This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0.<br>Read:<br>1'b0: Disabled<br>1'b1: Enabled<br>Write 1'b1 to clear enable |

### 5.5.2.26 ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_INT\_PRIO\_J Register

#### 1 ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_INT\_PRIO\_J Register (Offset = 410h) [reset = 0h]

Level Error Interrupt Enabled Clear register

Return to [Summary Table](#)

Offset = Base + (j \* 20h); where j = 0 to 2d

**Table 5-1561. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ESM0          | 52D0 0410h + formula |

**Figure 5-519. ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_INT\_PRIO\_J Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSK |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSK |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSK |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSK |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 5-1563. ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_INT\_PRIO\_J Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                        |
|------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSK   | R/W  | 0h    | This field is used to indicate which interrupt the corresponding event influences (if enabled) for event group N. Each bit corresponds to event Q where Q = N*32+Bit.<br>This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0.<br>0 - Low Priority Interrupt<br>1 - High Priority Interrupt |

### 5.5.2.27 ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_PIN\_EN\_SET\_J Register

**1 ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_PIN\_EN\_SET\_J Register (Offset = 414h) [reset = 0h]**

Level Error Interrupt Enabled Clear register

Return to [Summary Table](#)

Offset = Base + (j \* 20h); where j = 0 to 2d

**Table 5-1564. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ESM0          | 52D0 0414h + formula |

**Figure 5-520. ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_PIN\_EN\_SET\_J Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSK    |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSK    |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSK    |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSK    |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-1566. ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_PIN\_EN\_SET\_J Register Field Descriptions**

| Bit  | Field | Type   | Reset | Description                                                                                                                                                                                                                                                                                             |
|------|-------|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSK   | R/W1TS | 0h    | This field is used to enable the mask of events in group N. Each bit corresponds to event Q where Q = N*32+Bit.<br>This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0.<br>Read:<br>1'b0: Disabled<br>1'b1: Enabled<br>Write 1'b1 to set enable |

### 5.5.2.28 ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_PIN\_EN\_CLR\_J Register

#### 1 ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_PIN\_EN\_CLR\_J Register (Offset = 418h) [reset = 0h]

Level Error Interrupt Enabled Clear register

Return to [Summary Table](#)

Offset = Base + (j \* 20h); where j = 0 to 2d

**Table 5-1567. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| ESM0          | 52D0 0418h + formula |

**Figure 5-521. ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_PIN\_EN\_CLR\_J Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MSK    |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MSK    |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MSK    |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MSK    |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-1569. ESM\_PCR\_GENERATED\_MEMORY\_MAP\_ERR\_GRP\_PIN\_EN\_CLR\_J Register Field Descriptions**

| Bit  | Field | Type   | Reset | Description                                                                                                                                                                                                                                                                                               |
|------|-------|--------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | MSK   | R/W1TC | 0h    | This field is used to enable the mask of events in group N. Each bit corresponds to event Q where Q = N*32+Bit.<br>This field is only reset by a Power-On-Reset (not warm reset). A global soft reset will set this field to 0.<br>Read:<br>1'b0: Disabled<br>1'b1: Enabled<br>Write 1'b1 to clear enable |

## 5.6 EXT\_FLASH

### EXT\_FLASH

#### 5.6.1 EXT\_FLASH Summaries

#### EXT\_FLASH Summaries

**Table 5-1570. EXT\_FLASH Registers, Base Address=6000 0000h, Length=33554432**

| Offset        | Length | Register Name                   | EXT_FLASH0 Physical Address | EXT_FLASH1 Physical Address |
|---------------|--------|---------------------------------|-----------------------------|-----------------------------|
| 0h            | 32     | <a href="#">EXT_FLASH_START</a> | 6000 0000h                  | 6200 0000h                  |
| 1FFFFFFC<br>h | 32     | <a href="#">EXT_FLASH_END</a>   | 61FF FFFCh                  | 63FF FFFCh                  |

#### 5.6.2 EXT\_FLASH Registers

#### EXT\_FLASH Registers

### 5.6.2.1 EXT\_FLASH\_START Register

#### 1 EXT\_FLASH\_START Register (Offset = 0h) [reset = 0h]

Return to [Summary Table](#)

**Table 5-1571. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EXT_FLASH0    | 6000 0000h       |
| EXT_FLASH1    | 6200 0000h       |

**Figure 5-522. EXT\_FLASH\_START Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MEM_START |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MEM_START |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MEM_START |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MEM_START |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 5-1573. EXT\_FLASH\_START Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                  |
|------|-----------|------|-------|------------------------------|
| 31:0 | MEM_START | R/W  | 0h    | External flash start Address |

### 5.6.2.2 EXT\_FLASH\_END Register

1 EXT\_FLASH\_END Register (Offset = 1FFFFFFCh) [reset = 0h]

Return to [Summary Table](#)

**Table 5-1574. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| EXT_FLASH0    | 61FF FFFCh       |
| EXT_FLASH1    | 63FF FFFCh       |

**Figure 5-523. EXT\_FLASH\_END Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| MEM_END |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| MEM_END |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| MEM_END |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MEM_END |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-1576. EXT\_FLASH\_END Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                |
|------|---------|------|-------|----------------------------|
| 31:0 | MEM_END | R/W  | 0h    | External flash end address |



## 5.7 GPIO

### GPIO

#### 5.7.1 GPIO Summaries

#### GPIO Summaries

**Table 5-1577. GPIO Registers, Base Address=5200 0000h, Length=256**

| Offset | Length | Register Name                       | GPIO0 Physical Address | GPIO1 Physical Address | GPIO2 Physical Address |
|--------|--------|-------------------------------------|------------------------|------------------------|------------------------|
| 0h     | 32     | <a href="#">GPIO_PID</a>            | 5200 0000h             | 5200 1000h             | 5200 2000h             |
| 4h     | 32     | <a href="#">GPIO_PCR</a>            | 5200 0004h             | 5200 1004h             | 5200 2004h             |
| 8h     | 32     | <a href="#">GPIO_BINTEN</a>         | 5200 0008h             | 5200 1008h             | 5200 2008h             |
| 10h    | 32     | <a href="#">GPIO_DIR01</a>          | 5200 0010h             | 5200 1010h             | 5200 2010h             |
| 14h    | 32     | <a href="#">GPIO_OUT_DATA01</a>     | 5200 0014h             | 5200 1014h             | 5200 2014h             |
| 18h    | 32     | <a href="#">GPIO_SET_DATA01</a>     | 5200 0018h             | 5200 1018h             | 5200 2018h             |
| 1Ch    | 32     | <a href="#">GPIO_CLR_DATA01</a>     | 5200 001Ch             | 5200 101Ch             | 5200 201Ch             |
| 20h    | 32     | <a href="#">GPIO_IN_DATA01</a>      | 5200 0020h             | 5200 1020h             | 5200 2020h             |
| 24h    | 32     | <a href="#">GPIO_SET_RIS_TRIG01</a> | 5200 0024h             | 5200 1024h             | 5200 2024h             |
| 28h    | 32     | <a href="#">GPIO_CLR_RIS_TRIG01</a> | 5200 0028h             | 5200 1028h             | 5200 2028h             |
| 2Ch    | 32     | <a href="#">GPIO_SET_FAL_TRIG01</a> | 5200 002Ch             | 5200 102Ch             | 5200 202Ch             |
| 30h    | 32     | <a href="#">GPIO_CLR_FAL_TRIG01</a> | 5200 0030h             | 5200 1030h             | 5200 2030h             |
| 34h    | 32     | <a href="#">GPIO_INTSTAT01</a>      | 5200 0034h             | 5200 1034h             | 5200 2034h             |
| 38h    | 32     | <a href="#">GPIO_DIR23</a>          | 5200 0038h             | 5200 1038h             | 5200 2038h             |
| 3Ch    | 32     | <a href="#">GPIO_OUT_DATA23</a>     | 5200 003Ch             | 5200 103Ch             | 5200 203Ch             |
| 40h    | 32     | <a href="#">GPIO_SET_DATA23</a>     | 5200 0040h             | 5200 1040h             | 5200 2040h             |
| 44h    | 32     | <a href="#">GPIO_CLR_DATA23</a>     | 5200 0044h             | 5200 1044h             | 5200 2044h             |
| 48h    | 32     | <a href="#">GPIO_IN_DATA23</a>      | 5200 0048h             | 5200 1048h             | 5200 2048h             |
| 4Ch    | 32     | <a href="#">GPIO_SET_RIS_TRIG23</a> | 5200 004Ch             | 5200 104Ch             | 5200 204Ch             |
| 50h    | 32     | <a href="#">GPIO_CLR_RIS_TRIG23</a> | 5200 0050h             | 5200 1050h             | 5200 2050h             |
| 54h    | 32     | <a href="#">GPIO_SET_FAL_TRIG23</a> | 5200 0054h             | 5200 1054h             | 5200 2054h             |
| 58h    | 32     | <a href="#">GPIO_CLR_FAL_TRIG23</a> | 5200 0058h             | 5200 1058h             | 5200 2058h             |
| 5Ch    | 32     | <a href="#">GPIO_INTSTAT23</a>      | 5200 005Ch             | 5200 105Ch             | 5200 205Ch             |
| 60h    | 32     | <a href="#">GPIO_DIR45</a>          | 5200 0060h             | 5200 1060h             | 5200 2060h             |
| 64h    | 32     | <a href="#">GPIO_OUT_DATA45</a>     | 5200 0064h             | 5200 1064h             | 5200 2064h             |
| 68h    | 32     | <a href="#">GPIO_SET_DATA45</a>     | 5200 0068h             | 5200 1068h             | 5200 2068h             |
| 6Ch    | 32     | <a href="#">GPIO_CLR_DATA45</a>     | 5200 006Ch             | 5200 106Ch             | 5200 206Ch             |
| 70h    | 32     | <a href="#">GPIO_IN_DATA45</a>      | 5200 0070h             | 5200 1070h             | 5200 2070h             |
| 74h    | 32     | <a href="#">GPIO_SET_RIS_TRIG45</a> | 5200 0074h             | 5200 1074h             | 5200 2074h             |
| 78h    | 32     | <a href="#">GPIO_CLR_RIS_TRIG45</a> | 5200 0078h             | 5200 1078h             | 5200 2078h             |
| 7Ch    | 32     | <a href="#">GPIO_SET_FAL_TRIG45</a> | 5200 007Ch             | 5200 107Ch             | 5200 207Ch             |
| 80h    | 32     | <a href="#">GPIO_CLR_FAL_TRIG45</a> | 5200 0080h             | 5200 1080h             | 5200 2080h             |
| 84h    | 32     | <a href="#">GPIO_INTSTAT45</a>      | 5200 0084h             | 5200 1084h             | 5200 2084h             |
| 88h    | 32     | <a href="#">GPIO_DIR67</a>          | 5200 0088h             | 5200 1088h             | 5200 2088h             |
| 8Ch    | 32     | <a href="#">GPIO_OUT_DATA67</a>     | 5200 008Ch             | 5200 108Ch             | 5200 208Ch             |
| 90h    | 32     | <a href="#">GPIO_SET_DATA67</a>     | 5200 0090h             | 5200 1090h             | 5200 2090h             |
| 94h    | 32     | <a href="#">GPIO_CLR_DATA67</a>     | 5200 0094h             | 5200 1094h             | 5200 2094h             |
| 98h    | 32     | <a href="#">GPIO_IN_DATA67</a>      | 5200 0098h             | 5200 1098h             | 5200 2098h             |

**Table 5-1577. GPIO Registers, Base Address=5200 0000h, Length=256 (continued)**

| Offset | Length | Register Name                       | GPIO0 Physical Address | GPIO1 Physical Address | GPIO2 Physical Address |
|--------|--------|-------------------------------------|------------------------|------------------------|------------------------|
| 9Ch    | 32     | <a href="#">GPIO_SET_RIS_TRIG67</a> | 5200 009Ch             | 5200 109Ch             | 5200 209Ch             |
| A0h    | 32     | <a href="#">GPIO_CLR_RIS_TRIG67</a> | 5200 00A0h             | 5200 10A0h             | 5200 20A0h             |
| A4h    | 32     | <a href="#">GPIO_SET_FAL_TRIG67</a> | 5200 00A4h             | 5200 10A4h             | 5200 20A4h             |
| A8h    | 32     | <a href="#">GPIO_CLR_FAL_TRIG67</a> | 5200 00A8h             | 5200 10A8h             | 5200 20A8h             |
| ACH    | 32     | <a href="#">GPIO_INTSTAT67</a>      | 5200 00ACH             | 5200 10ACH             | 5200 20ACH             |
| B0h    | 32     | <a href="#">GPIO_DIR8</a>           | 5200 00B0h             | 5200 10B0h             | 5200 20B0h             |
| B4h    | 32     | <a href="#">GPIO_OUT_DATA8</a>      | 5200 00B4h             | 5200 10B4h             | 5200 20B4h             |
| B8h    | 32     | <a href="#">GPIO_SET_DATA8</a>      | 5200 00B8h             | 5200 10B8h             | 5200 20B8h             |
| BCh    | 32     | <a href="#">GPIO_CLR_DATA8</a>      | 5200 00BCh             | 5200 10BCh             | 5200 20BCh             |
| C0h    | 32     | <a href="#">GPIO_IN_DATA8</a>       | 5200 00C0h             | 5200 10C0h             | 5200 20C0h             |
| C4h    | 32     | <a href="#">GPIO_SET_RIS_TRIG8</a>  | 5200 00C4h             | 5200 10C4h             | 5200 20C4h             |
| C8h    | 32     | <a href="#">GPIO_CLR_RIS_TRIG8</a>  | 5200 00C8h             | 5200 10C8h             | 5200 20C8h             |
| CCh    | 32     | <a href="#">GPIO_SET_FAL_TRIG8</a>  | 5200 00CCh             | 5200 10CCh             | 5200 20CCh             |
| D0h    | 32     | <a href="#">GPIO_CLR_FAL_TRIG8</a>  | 5200 00D0h             | 5200 10D0h             | 5200 20D0h             |
| D4h    | 32     | <a href="#">GPIO_INTSTAT8</a>       | 5200 00D4h             | 5200 10D4h             | 5200 20D4h             |

**Table 5-1578. GPIO Registers, Base Address=5200 0000h, Length=256**

| Offset | Length | Register Name                       | GPIO3 Physical Address |
|--------|--------|-------------------------------------|------------------------|
| 0h     | 32     | <a href="#">GPIO_PID</a>            | 5200 3000h             |
| 4h     | 32     | <a href="#">GPIO_PCR</a>            | 5200 3004h             |
| 8h     | 32     | <a href="#">GPIO_BINTEN</a>         | 5200 3008h             |
| 10h    | 32     | <a href="#">GPIO_DIR01</a>          | 5200 3010h             |
| 14h    | 32     | <a href="#">GPIO_OUT_DATA01</a>     | 5200 3014h             |
| 18h    | 32     | <a href="#">GPIO_SET_DATA01</a>     | 5200 3018h             |
| 1Ch    | 32     | <a href="#">GPIO_CLR_DATA01</a>     | 5200 301Ch             |
| 20h    | 32     | <a href="#">GPIO_IN_DATA01</a>      | 5200 3020h             |
| 24h    | 32     | <a href="#">GPIO_SET_RIS_TRIG01</a> | 5200 3024h             |
| 28h    | 32     | <a href="#">GPIO_CLR_RIS_TRIG01</a> | 5200 3028h             |
| 2Ch    | 32     | <a href="#">GPIO_SET_FAL_TRIG01</a> | 5200 302Ch             |
| 30h    | 32     | <a href="#">GPIO_CLR_FAL_TRIG01</a> | 5200 3030h             |
| 34h    | 32     | <a href="#">GPIO_INTSTAT01</a>      | 5200 3034h             |
| 38h    | 32     | <a href="#">GPIO_DIR23</a>          | 5200 3038h             |
| 3Ch    | 32     | <a href="#">GPIO_OUT_DATA23</a>     | 5200 303Ch             |
| 40h    | 32     | <a href="#">GPIO_SET_DATA23</a>     | 5200 3040h             |
| 44h    | 32     | <a href="#">GPIO_CLR_DATA23</a>     | 5200 3044h             |
| 48h    | 32     | <a href="#">GPIO_IN_DATA23</a>      | 5200 3048h             |
| 4Ch    | 32     | <a href="#">GPIO_SET_RIS_TRIG23</a> | 5200 304Ch             |
| 50h    | 32     | <a href="#">GPIO_CLR_RIS_TRIG23</a> | 5200 3050h             |
| 54h    | 32     | <a href="#">GPIO_SET_FAL_TRIG23</a> | 5200 3054h             |
| 58h    | 32     | <a href="#">GPIO_CLR_FAL_TRIG23</a> | 5200 3058h             |
| 5Ch    | 32     | <a href="#">GPIO_INTSTAT23</a>      | 5200 305Ch             |
| 60h    | 32     | <a href="#">GPIO_DIR45</a>          | 5200 3060h             |
| 64h    | 32     | <a href="#">GPIO_OUT_DATA45</a>     | 5200 3064h             |
| 68h    | 32     | <a href="#">GPIO_SET_DATA45</a>     | 5200 3068h             |
| 6Ch    | 32     | <a href="#">GPIO_CLR_DATA45</a>     | 5200 306Ch             |

**Table 5-1578. GPIO Registers, Base Address=5200 0000h, Length=256 (continued)**

| Offset | Length | Register Name                       | GPIO3 Physical Address |
|--------|--------|-------------------------------------|------------------------|
| 70h    | 32     | <a href="#">GPIO_IN_DATA45</a>      | 5200 3070h             |
| 74h    | 32     | <a href="#">GPIO_SET_RIS_TRIG45</a> | 5200 3074h             |
| 78h    | 32     | <a href="#">GPIO_CLR_RIS_TRIG45</a> | 5200 3078h             |
| 7Ch    | 32     | <a href="#">GPIO_SET_FAL_TRIG45</a> | 5200 307Ch             |
| 80h    | 32     | <a href="#">GPIO_CLR_FAL_TRIG45</a> | 5200 3080h             |
| 84h    | 32     | <a href="#">GPIO_INTSTAT45</a>      | 5200 3084h             |
| 88h    | 32     | <a href="#">GPIO_DIR67</a>          | 5200 3088h             |
| 8Ch    | 32     | <a href="#">GPIO_OUT_DATA67</a>     | 5200 308Ch             |
| 90h    | 32     | <a href="#">GPIO_SET_DATA67</a>     | 5200 3090h             |
| 94h    | 32     | <a href="#">GPIO_CLR_DATA67</a>     | 5200 3094h             |
| 98h    | 32     | <a href="#">GPIO_IN_DATA67</a>      | 5200 3098h             |
| 9Ch    | 32     | <a href="#">GPIO_SET_RIS_TRIG67</a> | 5200 309Ch             |
| A0h    | 32     | <a href="#">GPIO_CLR_RIS_TRIG67</a> | 5200 30A0h             |
| A4h    | 32     | <a href="#">GPIO_SET_FAL_TRIG67</a> | 5200 30A4h             |
| A8h    | 32     | <a href="#">GPIO_CLR_FAL_TRIG67</a> | 5200 30A8h             |
| ACh    | 32     | <a href="#">GPIO_INTSTAT67</a>      | 5200 30ACh             |
| B0h    | 32     | <a href="#">GPIO_DIR8</a>           | 5200 30B0h             |
| B4h    | 32     | <a href="#">GPIO_OUT_DATA8</a>      | 5200 30B4h             |
| B8h    | 32     | <a href="#">GPIO_SET_DATA8</a>      | 5200 30B8h             |
| BCh    | 32     | <a href="#">GPIO_CLR_DATA8</a>      | 5200 30BCh             |
| C0h    | 32     | <a href="#">GPIO_IN_DATA8</a>       | 5200 30C0h             |
| C4h    | 32     | <a href="#">GPIO_SET_RIS_TRIG8</a>  | 5200 30C4h             |
| C8h    | 32     | <a href="#">GPIO_CLR_RIS_TRIG8</a>  | 5200 30C8h             |
| CCh    | 32     | <a href="#">GPIO_SET_FAL_TRIG8</a>  | 5200 30CCh             |
| D0h    | 32     | <a href="#">GPIO_CLR_FAL_TRIG8</a>  | 5200 30D0h             |
| D4h    | 32     | <a href="#">GPIO_INTSTAT8</a>       | 5200 30D4h             |

## 5.7.2 GPIO Registers

### GPIO Registers

### 5.7.2.1 GPIO\_PID Register

#### 1 GPIO\_PID Register (Offset = 0h) [reset = 44832905h]

GPIO Peripheral ID Register.

Return to [Summary Table](#)

**Table 5-1579. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0000h       |
| GPIO1         | 5200 1000h       |
| GPIO2         | 5200 2000h       |
| GPIO3         | 5200 3000h       |

**Figure 5-524. GPIO\_PID Name Register**

|        |    |          |    |       |    |    |    |
|--------|----|----------|----|-------|----|----|----|
| 31     | 30 | 29       | 28 | 27    | 26 | 25 | 24 |
| SCHEME |    | RESERVED |    | FUNC  |    |    |    |
| R      |    | R        |    | R     |    |    |    |
| 1h     |    | 0h       |    | 483h  |    |    |    |
| 23     | 22 | 21       | 20 | 19    | 18 | 17 | 16 |
| FUNC   |    |          |    |       |    |    |    |
| R      |    |          |    |       |    |    |    |
| 483h   |    |          |    |       |    |    |    |
| 15     | 14 | 13       | 12 | 11    | 10 | 9  | 8  |
| RTL    |    |          |    | MAJOR |    |    |    |
| R      |    |          |    | R     |    |    |    |
| 5h     |    |          |    | 1h    |    |    |    |
| 7      | 6  | 5        | 4  | 3     | 2  | 1  | 0  |
| CUSTOM |    | MINOR    |    |       |    |    |    |
| R      |    | R        |    |       |    |    |    |
| 0h     |    | 5h       |    |       |    |    |    |

**Table 5-1581. GPIO\_PID Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                    |
|-------|----------|------|-------|--------------------------------|
| 31:30 | SCHEME   | R    | 1h    | Current scheme                 |
| 29:28 | RESERVED | R    | 0h    | RESERVED                       |
| 27:16 | FUNC     | R    | 483h  | Function code assigned to TCP3 |
| 15:11 | RTL      | R    | 5h    | RTL Version R code             |
| 10:8  | MAJOR    | R    | 1h    | Major revision X code          |
| 7:6   | CUSTOM   | R    | 0h    | Custom version code            |
| 5:0   | MINOR    | R    | 5h    | Minor revision Y code          |

### 5.7.2.2 GPIO\_PCR Register

#### 1 GPIO\_PCR Register (Offset = 4h) [reset = 1h]

Peripheral Control Register.

Return to [Summary Table](#)

**Table 5-1582. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0004h       |
| GPIO1         | 5200 1004h       |
| GPIO2         | 5200 2004h       |
| GPIO3         | 5200 3004h       |

**Figure 5-525. GPIO\_PCR Name Register**

|          |    |    |    |    |    |      |      |
|----------|----|----|----|----|----|------|------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25   | 24   |
| RESERVED |    |    |    |    |    |      |      |
| NONE     |    |    |    |    |    |      |      |
| 0h       |    |    |    |    |    |      |      |
| 23       | 22 | 21 | 20 | 19 | 18 | 17   | 16   |
| RESERVED |    |    |    |    |    |      |      |
| NONE     |    |    |    |    |    |      |      |
| 0h       |    |    |    |    |    |      |      |
| 15       | 14 | 13 | 12 | 11 | 10 | 9    | 8    |
| RESERVED |    |    |    |    |    |      |      |
| NONE     |    |    |    |    |    |      |      |
| 0h       |    |    |    |    |    |      |      |
| 7        | 6  | 5  | 4  | 3  | 2  | 1    | 0    |
| RESERVED |    |    |    |    |    | SOFT | FREE |
| NONE     |    |    |    |    |    | R    | R    |
| 0h       |    |    |    |    |    | 0h   | 1h   |

**Table 5-1584. GPIO\_PCR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                            |
|------|----------|------|-------|----------------------------------------------------------------------------------------|
| 31:2 | RESERVED | NONE | 0h    | Reserved                                                                               |
| 1    | SOFT     | R    | 0h    | Used in conjunction with FREE bit to determine the emulation suspend mode.             |
| 0    | FREE     | R    | 1h    | For GPIO, the FREE bit is fixed at 1, which means GPIO runs free in emulation suspend. |

### 5.7.2.3 GPIO\_BINTEN Register

#### 1 GPIO\_BINTEN Register (Offset = 8h) [reset = 0h]

Bit Interrupt Enable Register.

Return to [Summary Table](#)

**Table 5-1585. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0008h       |
| GPIO1         | 5200 1008h       |
| GPIO2         | 5200 2008h       |
| GPIO3         | 5200 3008h       |

**Figure 5-526. GPIO\_BINTEN Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| EN       |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| EN       |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-1587. GPIO\_BINTEN Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                         |
|-------|----------|------|-------|-----------------------------------------------------|
| 31:16 | RESERVED | R    | 0h    | RESERVED                                            |
| 15:0  | EN       | R/W  | 0h    | Per bank interrupt enable. 0 = disable, 1 = enable. |

### 5.7.2.4 GPIO\_DIR01 Register

#### 1 GPIO\_DIR01 Register (Offset = 10h) [reset = FFFFFFFFh]

Direction Register.

Return to [Summary Table](#)

**Table 5-1588. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0010h       |
| GPIO1         | 5200 1010h       |
| GPIO2         | 5200 2010h       |
| GPIO3         | 5200 3010h       |

**Figure 5-527. GPIO\_DIR01 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DIR1  |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DIR1  |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DIR0  |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DIR0  |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |

**Table 5-1590. GPIO\_DIR01 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                           |
|-------|-------|------|-------|-------------------------------------------------------|
| 31:16 | DIR1  | R/W  | FFFFh | Direction of GPIO bank 1 bits, 0 = output, 1 = input. |
| 15:0  | DIR0  | R/W  | FFFFh | Direction of GPIO bank 0 bits, 0 = output, 1 = input. |

### 5.7.2.5 GPIO\_OUT\_DATA01 Register

#### 1 GPIO\_OUT\_DATA01 Register (Offset = 14h) [reset = 0h]

Output Drive State Register.

Return to [Summary Table](#)

**Table 5-1591. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0014h       |
| GPIO1         | 5200 1014h       |
| GPIO2         | 5200 2014h       |
| GPIO3         | 5200 3014h       |

**Figure 5-528. GPIO\_OUT\_DATA01 Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUT1 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUT1 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUT0 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUT0 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-1593. GPIO\_OUT\_DATA01 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                  |
|-------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | OUT1  | R/W  | 0h    | Output drive state of GPIO bank 1 bits, does not effect operation when it is configured as input. Reading it returns the output drive state. |
| 15:0  | OUT0  | R/W  | 0h    | Output drive state of GPIO bank 0 bits, does not effect operation when it is configured as input. Reading it returns the output drive state. |



### 5.7.2.6 GPIO\_SET\_DATA01 Register

#### 1 GPIO\_SET\_DATA01 Register (Offset = 18h) [reset = 0h]

Set Output Drive State Register.

Return to [Summary Table](#)

**Table 5-1594. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0018h       |
| GPIO1         | 5200 1018h       |
| GPIO2         | 5200 2018h       |
| GPIO3         | 5200 3018h       |

**Figure 5-529. GPIO\_SET\_DATA01 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SET1   |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SET1   |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SET0   |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SET0   |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-1596. GPIO\_SET\_DATA01 Register Field Descriptions**

| Bit   | Field | Type   | Reset | Description                                                                                           |
|-------|-------|--------|-------|-------------------------------------------------------------------------------------------------------|
| 31:16 | SET1  | R/W1TS | 0h    | Writing 1 sets the output drive state of GPIO bank 1 bits. Reading it returns the output drive state. |
| 15:0  | SET0  | R/W1TS | 0h    | Writing 1 sets the output drive state of GPIO bank 0 bits. Reading it returns the output drive state. |

### 5.7.2.7 GPIO\_CLR\_DATA01 Register

#### 1 GPIO\_CLR\_DATA01 Register (Offset = 1Ch) [reset = 0h]

Clear Output Drive State Register.

Return to [Summary Table](#)

**Table 5-1597. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 001Ch       |
| GPIO1         | 5200 101Ch       |
| GPIO2         | 5200 201Ch       |
| GPIO3         | 5200 301Ch       |

**Figure 5-530. GPIO\_CLR\_DATA01 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CLR1   |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CLR1   |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CLR0   |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CLR0   |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-1599. GPIO\_CLR\_DATA01 Register Field Descriptions**

| Bit   | Field | Type   | Reset | Description                                                                                 |
|-------|-------|--------|-------|---------------------------------------------------------------------------------------------|
| 31:16 | CLR1  | R/W1TC | 0h    | Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. |
| 15:0  | CLR0  | R/W1TC | 0h    | Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. |

### 5.7.2.8 GPIO\_IN\_DATA01 Register

#### 1 GPIO\_IN\_DATA01 Register (Offset = 20h) [reset = 0h]

Bank Status Register.

Return to [Summary Table](#)

**Table 5-1600. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0020h       |
| GPIO1         | 5200 1020h       |
| GPIO2         | 5200 2020h       |
| GPIO3         | 5200 3020h       |

**Figure 5-531. GPIO\_IN\_DATA01 Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| IN1 |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| IN1 |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| IN0 |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| IN0 |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 5-1602. GPIO\_IN\_DATA01 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                 |
|-------|-------|------|-------|-----------------------------|
| 31:16 | IN1   | R    | 0h    | Status of GPIO bank 1 bits. |
| 15:0  | IN0   | R    | 0h    | Status of GPIO bank 0 bits. |

### 5.7.2.9 GPIO\_SET\_RIS\_TRIG01 Register

#### 1 GPIO\_SET\_RIS\_TRIG01 Register (Offset = 24h) [reset = 0h]

Set Rising Edge Detection Register.

Return to [Summary Table](#)

**Table 5-1603. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0024h       |
| GPIO1         | 5200 1024h       |
| GPIO2         | 5200 2024h       |
| GPIO3         | 5200 3024h       |

**Figure 5-532. GPIO\_SET\_RIS\_TRIG01 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SETRIS1 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SETRIS1 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SETRIS0 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SETRIS0 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-1605. GPIO\_SET\_RIS\_TRIG01 Register Field Descriptions**

| Bit   | Field   | Type   | Reset | Description                                                   |
|-------|---------|--------|-------|---------------------------------------------------------------|
| 31:16 | SETRIS1 | R/W1TS | 0h    | Writing 1 enables rising edge detection for GPIO bank 1 bits. |
| 15:0  | SETRIS0 | R/W1TS | 0h    | Writing 1 enables rising edge detection for GPIO bank 0 bits. |

### 5.7.2.10 GPIO\_CLR\_RIS\_TRIG01 Register

#### 1 GPIO\_CLR\_RIS\_TRIG01 Register (Offset = 28h) [reset = 0h]

Clear Rising Edge Detection Register.

Return to [Summary Table](#)

**Table 5-1606. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0028h       |
| GPIO1         | 5200 1028h       |
| GPIO2         | 5200 2028h       |
| GPIO3         | 5200 3028h       |

**Figure 5-533. GPIO\_CLR\_RIS\_TRIG01 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CLRRIS1 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CLRRIS1 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CLRRIS0 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CLRRIS0 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-1608. GPIO\_CLR\_RIS\_TRIG01 Register Field Descriptions**

| Bit   | Field   | Type   | Reset | Description                                                  |
|-------|---------|--------|-------|--------------------------------------------------------------|
| 31:16 | CLRRIS1 | R/W1TC | 0h    | Writing 1 clears rising edge detection for GPIO bank 1 bits. |
| 15:0  | CLRRIS0 | R/W1TC | 0h    | Writing 1 clears rising edge detection for GPIO bank 0 bits. |

### 5.7.2.11 GPIO\_SET\_FAL\_TRIG01 Register

#### 1 GPIO\_SET\_FAL\_TRIG01 Register (Offset = 2Ch) [reset = 0h]

Set Falling Edge Detection Register.

Return to [Summary Table](#)

**Table 5-1609. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 002Ch       |
| GPIO1         | 5200 102Ch       |
| GPIO2         | 5200 202Ch       |
| GPIO3         | 5200 302Ch       |

**Figure 5-534. GPIO\_SET\_FAL\_TRIG01 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SETFAL1 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SETFAL1 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SETFAL0 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SETFAL0 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-1611. GPIO\_SET\_FAL\_TRIG01 Register Field Descriptions**

| Bit   | Field   | Type   | Reset | Description                                                        |
|-------|---------|--------|-------|--------------------------------------------------------------------|
| 31:16 | SETFAL1 | R/W1TS | 0h    | Writing 1 enables falling edge detection for for GPIO bank 1 bits. |
| 15:0  | SETFAL0 | R/W1TS | 0h    | Writing 1 enables falling edge detection for for GPIO bank 0 bits. |

### 5.7.2.12 GPIO\_CLR\_FAL\_TRIG01 Register

#### 1 GPIO\_CLR\_FAL\_TRIG01 Register (Offset = 30h) [reset = 0h]

Clear Falling Edge Detection Register.

Return to [Summary Table](#)

**Table 5-1612. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0030h       |
| GPIO1         | 5200 1030h       |
| GPIO2         | 5200 2030h       |
| GPIO3         | 5200 3030h       |

**Figure 5-535. GPIO\_CLR\_FAL\_TRIG01 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CLRFAL1 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CLRFAL1 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CLRFAL0 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CLRFAL0 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-1614. GPIO\_CLR\_FAL\_TRIG01 Register Field Descriptions**

| Bit   | Field   | Type   | Reset | Description                                                       |
|-------|---------|--------|-------|-------------------------------------------------------------------|
| 31:16 | CLRFAL1 | R/W1TC | 0h    | Writing 1 clears falling edge detection for for GPIO bank 1 bits. |
| 15:0  | CLRFAL0 | R/W1TC | 0h    | Writing 1 clears falling edge detection for for GPIO bank 0 bits. |

### 5.7.2.13 GPIO\_INTSTAT01 Register

#### 1 GPIO\_INTSTAT01 Register (Offset = 34h) [reset = 0h]

Bank Interrupt Status Register.

Return to [Summary Table](#)

**Table 5-1615. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0034h       |
| GPIO1         | 5200 1034h       |
| GPIO2         | 5200 2034h       |
| GPIO3         | 5200 3034h       |

**Figure 5-536. GPIO\_INTSTAT01 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| STAT1  |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| STAT1  |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| STAT0  |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| STAT0  |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-1617. GPIO\_INTSTAT01 Register Field Descriptions**

| Bit   | Field | Type   | Reset | Description                                                                                                                                                                      |
|-------|-------|--------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | STAT1 | R/W1TC | 0h    | Status of GPIO bank 0 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. |
| 15:0  | STAT0 | R/W1TC | 0h    | Status of GPIO bank 0 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. |



### 5.7.2.14 GPIO\_DIR23 Register

#### 1 GPIO\_DIR23 Register (Offset = 38h) [reset = FFFFFFFFh]

Direction Register.

Return to [Summary Table](#)

**Table 5-1618. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0038h       |
| GPIO1         | 5200 1038h       |
| GPIO2         | 5200 2038h       |
| GPIO3         | 5200 3038h       |

**Figure 5-537. GPIO\_DIR23 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DIR3  |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DIR3  |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DIR2  |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DIR2  |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |

**Table 5-1620. GPIO\_DIR23 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                           |
|-------|-------|------|-------|-------------------------------------------------------|
| 31:16 | DIR3  | R/W  | FFFFh | Direction of GPIO bank 3 bits, 0 = output, 1 = input. |
| 15:0  | DIR2  | R/W  | FFFFh | Direction of GPIO bank 2 bits, 0 = output, 1 = input. |

### 5.7.2.15 GPIO\_OUT\_DATA23 Register

#### 1 GPIO\_OUT\_DATA23 Register (Offset = 3Ch) [reset = 0h]

Output Drive State Register.

Return to [Summary Table](#)

**Table 5-1621. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 003Ch       |
| GPIO1         | 5200 103Ch       |
| GPIO2         | 5200 203Ch       |
| GPIO3         | 5200 303Ch       |

**Figure 5-538. GPIO\_OUT\_DATA23 Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUT3 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUT3 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUT2 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUT2 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-1623. GPIO\_OUT\_DATA23 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                  |
|-------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | OUT3  | R/W  | 0h    | Output drive state of GPIO bank 3 bits, does not effect operation when it is configured as input. Reading it returns the output drive state. |
| 15:0  | OUT2  | R/W  | 0h    | Output drive state of GPIO bank 2 bits, does not effect operation when it is configured as input. Reading it returns the output drive state. |

### 5.7.2.16 GPIO\_SET\_DATA23 Register

#### 1 GPIO\_SET\_DATA23 Register (Offset = 40h) [reset = 0h]

Set Output Drive State Register.

Return to [Summary Table](#)

**Table 5-1624. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0040h       |
| GPIO1         | 5200 1040h       |
| GPIO2         | 5200 2040h       |
| GPIO3         | 5200 3040h       |

**Figure 5-539. GPIO\_SET\_DATA23 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SET3   |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SET3   |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SET2   |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SET2   |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-1626. GPIO\_SET\_DATA23 Register Field Descriptions**

| Bit   | Field | Type   | Reset | Description                                                                                           |
|-------|-------|--------|-------|-------------------------------------------------------------------------------------------------------|
| 31:16 | SET3  | R/W1TS | 0h    | Writing 1 sets the output drive state of GPIO bank 3 bits. Reading it returns the output drive state. |
| 15:0  | SET2  | R/W1TS | 0h    | Writing 1 sets the output drive state of GPIO bank 2 bits. Reading it returns the output drive state. |

### 5.7.2.17 GPIO\_CLR\_DATA23 Register

#### 1 GPIO\_CLR\_DATA23 Register (Offset = 44h) [reset = 0h]

Clear Output Drive State Register.

Return to [Summary Table](#)

**Table 5-1627. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0044h       |
| GPIO1         | 5200 1044h       |
| GPIO2         | 5200 2044h       |
| GPIO3         | 5200 3044h       |

**Figure 5-540. GPIO\_CLR\_DATA23 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CLR3   |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CLR3   |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CLR2   |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CLR2   |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-1629. GPIO\_CLR\_DATA23 Register Field Descriptions**

| Bit   | Field | Type   | Reset | Description                                                                                 |
|-------|-------|--------|-------|---------------------------------------------------------------------------------------------|
| 31:16 | CLR3  | R/W1TC | 0h    | Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. |
| 15:0  | CLR2  | R/W1TC | 0h    | Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. |

### 5.7.2.18 GPIO\_IN\_DATA23 Register

#### 1 GPIO\_IN\_DATA23 Register (Offset = 48h) [reset = 0h]

Bank Status Register.

Return to [Summary Table](#)

**Table 5-1630. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0048h       |
| GPIO1         | 5200 1048h       |
| GPIO2         | 5200 2048h       |
| GPIO3         | 5200 3048h       |

**Figure 5-541. GPIO\_IN\_DATA23 Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| IN3 |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| IN3 |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| IN2 |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| IN2 |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 5-1632. GPIO\_IN\_DATA23 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                 |
|-------|-------|------|-------|-----------------------------|
| 31:16 | IN3   | R    | 0h    | Status of GPIO bank 3 bits. |
| 15:0  | IN2   | R    | 0h    | Status of GPIO bank 2 bits. |

### 5.7.2.19 GPIO\_SET\_RIS\_TRIG23 Register

#### 1 GPIO\_SET\_RIS\_TRIG23 Register (Offset = 4Ch) [reset = 0h]

Set Rising Edge Detection Register.

Return to [Summary Table](#)

**Table 5-1633. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 004Ch       |
| GPIO1         | 5200 104Ch       |
| GPIO2         | 5200 204Ch       |
| GPIO3         | 5200 304Ch       |

**Figure 5-542. GPIO\_SET\_RIS\_TRIG23 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SETRIS3 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SETRIS3 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SETRIS2 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SETRIS2 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-1635. GPIO\_SET\_RIS\_TRIG23 Register Field Descriptions**

| Bit   | Field   | Type   | Reset | Description                                                   |
|-------|---------|--------|-------|---------------------------------------------------------------|
| 31:16 | SETRIS3 | R/W1TS | 0h    | Writing 1 enables rising edge detection for GPIO bank 3 bits. |
| 15:0  | SETRIS2 | R/W1TS | 0h    | Writing 1 enables rising edge detection for GPIO bank 2 bits. |

### 5.7.2.20 GPIO\_CLR\_RIS\_TRIG23 Register

#### 1 GPIO\_CLR\_RIS\_TRIG23 Register (Offset = 50h) [reset = 0h]

Clear Rising Edge Detection Register.

Return to [Summary Table](#)

**Table 5-1636. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0050h       |
| GPIO1         | 5200 1050h       |
| GPIO2         | 5200 2050h       |
| GPIO3         | 5200 3050h       |

**Figure 5-543. GPIO\_CLR\_RIS\_TRIG23 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CLRRIS3 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CLRRIS3 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CLRRIS2 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CLRRIS2 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-1638. GPIO\_CLR\_RIS\_TRIG23 Register Field Descriptions**

| Bit   | Field   | Type   | Reset | Description                                                  |
|-------|---------|--------|-------|--------------------------------------------------------------|
| 31:16 | CLRRIS3 | R/W1TC | 0h    | Writing 1 clears rising edge detection for GPIO bank 3 bits. |
| 15:0  | CLRRIS2 | R/W1TC | 0h    | Writing 1 clears rising edge detection for GPIO bank 2 bits. |

### 5.7.2.21 GPIO\_SET\_FAL\_TRIG23 Register

#### 1 GPIO\_SET\_FAL\_TRIG23 Register (Offset = 54h) [reset = 0h]

Set Falling Edge Detection Register.

Return to [Summary Table](#)

**Table 5-1639. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0054h       |
| GPIO1         | 5200 1054h       |
| GPIO2         | 5200 2054h       |
| GPIO3         | 5200 3054h       |

**Figure 5-544. GPIO\_SET\_FAL\_TRIG23 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SETFAL3 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SETFAL3 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SETFAL2 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SETFAL2 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-1641. GPIO\_SET\_FAL\_TRIG23 Register Field Descriptions**

| Bit   | Field   | Type   | Reset | Description                                                        |
|-------|---------|--------|-------|--------------------------------------------------------------------|
| 31:16 | SETFAL3 | R/W1TS | 0h    | Writing 1 enables falling edge detection for for GPIO bank 3 bits. |
| 15:0  | SETFAL2 | R/W1TS | 0h    | Writing 1 enables falling edge detection for for GPIO bank 2 bits. |



### 5.7.2.22 GPIO\_CLR\_FAL\_TRIG23 Register

#### 1 GPIO\_CLR\_FAL\_TRIG23 Register (Offset = 58h) [reset = 0h]

Clear Falling Edge Detection Register.

Return to [Summary Table](#)

**Table 5-1642. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0058h       |
| GPIO1         | 5200 1058h       |
| GPIO2         | 5200 2058h       |
| GPIO3         | 5200 3058h       |

**Figure 5-545. GPIO\_CLR\_FAL\_TRIG23 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CLRFAL3 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CLRFAL3 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CLRFAL2 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CLRFAL2 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-1644. GPIO\_CLR\_FAL\_TRIG23 Register Field Descriptions**

| Bit   | Field   | Type   | Reset | Description                                                       |
|-------|---------|--------|-------|-------------------------------------------------------------------|
| 31:16 | CLRFAL3 | R/W1TC | 0h    | Writing 1 clears falling edge detection for for GPIO bank 3 bits. |
| 15:0  | CLRFAL2 | R/W1TC | 0h    | Writing 1 clears falling edge detection for for GPIO bank 2 bits. |

### 5.7.2.23 GPIO\_INTSTAT23 Register

#### 1 GPIO\_INTSTAT23 Register (Offset = 5Ch) [reset = 0h]

Bank Interrupt Status Register.

Return to [Summary Table](#)

**Table 5-1645. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 005Ch       |
| GPIO1         | 5200 105Ch       |
| GPIO2         | 5200 205Ch       |
| GPIO3         | 5200 305Ch       |

**Figure 5-546. GPIO\_INTSTAT23 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| STAT3  |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| STAT3  |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| STAT2  |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| STAT2  |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-1647. GPIO\_INTSTAT23 Register Field Descriptions**

| Bit   | Field | Type   | Reset | Description                                                                                                                                                                      |
|-------|-------|--------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | STAT3 | R/W1TC | 0h    | Status of GPIO bank 2 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. |
| 15:0  | STAT2 | R/W1TC | 0h    | Status of GPIO bank 2 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. |

### 5.7.2.24 GPIO\_DIR45 Register

#### 1 GPIO\_DIR45 Register (Offset = 60h) [reset = FFFFFFFFh]

Direction Register.

Return to [Summary Table](#)

**Table 5-1648. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0060h       |
| GPIO1         | 5200 1060h       |
| GPIO2         | 5200 2060h       |
| GPIO3         | 5200 3060h       |

**Figure 5-547. GPIO\_DIR45 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DIR5  |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DIR5  |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DIR4  |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DIR4  |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |

**Table 5-1650. GPIO\_DIR45 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                           |
|-------|-------|------|-------|-------------------------------------------------------|
| 31:16 | DIR5  | R/W  | FFFFh | Direction of GPIO bank 5 bits, 0 = output, 1 = input. |
| 15:0  | DIR4  | R/W  | FFFFh | Direction of GPIO bank 4 bits, 0 = output, 1 = input. |

### 5.7.2.25 GPIO\_OUT\_DATA45 Register

#### 1 GPIO\_OUT\_DATA45 Register (Offset = 64h) [reset = 0h]

Output Drive State Register.

Return to [Summary Table](#)

**Table 5-1651. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0064h       |
| GPIO1         | 5200 1064h       |
| GPIO2         | 5200 2064h       |
| GPIO3         | 5200 3064h       |

**Figure 5-548. GPIO\_OUT\_DATA45 Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUT5 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUT5 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUT4 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUT4 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-1653. GPIO\_OUT\_DATA45 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                  |
|-------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | OUT5  | R/W  | 0h    | Output drive state of GPIO bank 5 bits, does not effect operation when it is configured as input. Reading it returns the output drive state. |
| 15:0  | OUT4  | R/W  | 0h    | Output drive state of GPIO bank 4 bits, does not effect operation when it is configured as input. Reading it returns the output drive state. |

### 5.7.2.26 GPIO\_SET\_DATA45 Register

#### 1 GPIO\_SET\_DATA45 Register (Offset = 68h) [reset = 0h]

Set Output Drive State Register.

Return to [Summary Table](#)

**Table 5-1654. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0068h       |
| GPIO1         | 5200 1068h       |
| GPIO2         | 5200 2068h       |
| GPIO3         | 5200 3068h       |

**Figure 5-549. GPIO\_SET\_DATA45 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SET5   |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SET5   |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SET4   |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SET4   |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-1656. GPIO\_SET\_DATA45 Register Field Descriptions**

| Bit   | Field | Type   | Reset | Description                                                                                           |
|-------|-------|--------|-------|-------------------------------------------------------------------------------------------------------|
| 31:16 | SET5  | R/W1TS | 0h    | Writing 1 sets the output drive state of GPIO bank 5 bits. Reading it returns the output drive state. |
| 15:0  | SET4  | R/W1TS | 0h    | Writing 1 sets the output drive state of GPIO bank 4 bits. Reading it returns the output drive state. |

### 5.7.2.27 GPIO\_CLR\_DATA45 Register

#### 1 GPIO\_CLR\_DATA45 Register (Offset = 6Ch) [reset = 0h]

Clear Output Drive State Register.

Return to [Summary Table](#)

**Table 5-1657. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 006Ch       |
| GPIO1         | 5200 106Ch       |
| GPIO2         | 5200 206Ch       |
| GPIO3         | 5200 306Ch       |

**Figure 5-550. GPIO\_CLR\_DATA45 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CLR5   |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CLR5   |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CLR4   |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CLR4   |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-1659. GPIO\_CLR\_DATA45 Register Field Descriptions**

| Bit   | Field | Type   | Reset | Description                                                                                 |
|-------|-------|--------|-------|---------------------------------------------------------------------------------------------|
| 31:16 | CLR5  | R/W1TC | 0h    | Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. |
| 15:0  | CLR4  | R/W1TC | 0h    | Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. |

### 5.7.2.28 GPIO\_IN\_DATA45 Register

#### 1 GPIO\_IN\_DATA45 Register (Offset = 70h) [reset = 0h]

Bank Status Register.

Return to [Summary Table](#)

**Table 5-1660. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0070h       |
| GPIO1         | 5200 1070h       |
| GPIO2         | 5200 2070h       |
| GPIO3         | 5200 3070h       |

**Figure 5-551. GPIO\_IN\_DATA45 Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| IN5 |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| IN5 |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| IN4 |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| IN4 |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 5-1662. GPIO\_IN\_DATA45 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                 |
|-------|-------|------|-------|-----------------------------|
| 31:16 | IN5   | R    | 0h    | Status of GPIO bank 5 bits. |
| 15:0  | IN4   | R    | 0h    | Status of GPIO bank 4 bits. |

### 5.7.2.29 GPIO\_SET\_RIS\_TRIG45 Register

#### 1 GPIO\_SET\_RIS\_TRIG45 Register (Offset = 74h) [reset = 0h]

Set Rising Edge Detection Register.

Return to [Summary Table](#)

**Table 5-1663. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0074h       |
| GPIO1         | 5200 1074h       |
| GPIO2         | 5200 2074h       |
| GPIO3         | 5200 3074h       |

**Figure 5-552. GPIO\_SET\_RIS\_TRIG45 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SETRIS5 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SETRIS5 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SETRIS4 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SETRIS4 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-1665. GPIO\_SET\_RIS\_TRIG45 Register Field Descriptions**

| Bit   | Field   | Type   | Reset | Description                                                   |
|-------|---------|--------|-------|---------------------------------------------------------------|
| 31:16 | SETRIS5 | R/W1TS | 0h    | Writing 1 enables rising edge detection for GPIO bank 5 bits. |
| 15:0  | SETRIS4 | R/W1TS | 0h    | Writing 1 enables rising edge detection for GPIO bank 4 bits. |



### 5.7.2.30 GPIO\_CLR\_RIS\_TRIG45 Register

#### 1 GPIO\_CLR\_RIS\_TRIG45 Register (Offset = 78h) [reset = 0h]

Clear Rising Edge Detection Register.

Return to [Summary Table](#)

**Table 5-1666. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0078h       |
| GPIO1         | 5200 1078h       |
| GPIO2         | 5200 2078h       |
| GPIO3         | 5200 3078h       |

**Figure 5-553. GPIO\_CLR\_RIS\_TRIG45 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CLRRIS5 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CLRRIS5 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CLRRIS4 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CLRRIS4 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-1668. GPIO\_CLR\_RIS\_TRIG45 Register Field Descriptions**

| Bit   | Field   | Type   | Reset | Description                                                  |
|-------|---------|--------|-------|--------------------------------------------------------------|
| 31:16 | CLRRIS5 | R/W1TC | 0h    | Writing 1 clears rising edge detection for GPIO bank 5 bits. |
| 15:0  | CLRRIS4 | R/W1TC | 0h    | Writing 1 clears rising edge detection for GPIO bank 4 bits. |

### 5.7.2.31 GPIO\_SET\_FAL\_TRIG45 Register

#### 1 GPIO\_SET\_FAL\_TRIG45 Register (Offset = 7Ch) [reset = 0h]

Set Falling Edge Detection Register.

Return to [Summary Table](#)

**Table 5-1669. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 007Ch       |
| GPIO1         | 5200 107Ch       |
| GPIO2         | 5200 207Ch       |
| GPIO3         | 5200 307Ch       |

**Figure 5-554. GPIO\_SET\_FAL\_TRIG45 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SETFAL5 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SETFAL5 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SETFAL4 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SETFAL4 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-1671. GPIO\_SET\_FAL\_TRIG45 Register Field Descriptions**

| Bit   | Field   | Type   | Reset | Description                                                        |
|-------|---------|--------|-------|--------------------------------------------------------------------|
| 31:16 | SETFAL5 | R/W1TS | 0h    | Writing 1 enables falling edge detection for for GPIO bank 5 bits. |
| 15:0  | SETFAL4 | R/W1TS | 0h    | Writing 1 enables falling edge detection for for GPIO bank 4 bits. |

### 5.7.2.32 GPIO\_CLR\_FAL\_TRIG45 Register

#### 1 GPIO\_CLR\_FAL\_TRIG45 Register (Offset = 80h) [reset = 0h]

Clear Falling Edge Detection Register.

Return to [Summary Table](#)

**Table 5-1672. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0080h       |
| GPIO1         | 5200 1080h       |
| GPIO2         | 5200 2080h       |
| GPIO3         | 5200 3080h       |

**Figure 5-555. GPIO\_CLR\_FAL\_TRIG45 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CLRFAL5 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CLRFAL5 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CLRFAL4 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CLRFAL4 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-1674. GPIO\_CLR\_FAL\_TRIG45 Register Field Descriptions**

| Bit   | Field   | Type   | Reset | Description                                                       |
|-------|---------|--------|-------|-------------------------------------------------------------------|
| 31:16 | CLRFAL5 | R/W1TC | 0h    | Writing 1 clears falling edge detection for for GPIO bank 5 bits. |
| 15:0  | CLRFAL4 | R/W1TC | 0h    | Writing 1 clears falling edge detection for for GPIO bank 4 bits. |

### 5.7.2.33 GPIO\_INTSTAT45 Register

#### 1 GPIO\_INTSTAT45 Register (Offset = 84h) [reset = 0h]

Bank Interrupt Status Register.

Return to [Summary Table](#)

**Table 5-1675. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0084h       |
| GPIO1         | 5200 1084h       |
| GPIO2         | 5200 2084h       |
| GPIO3         | 5200 3084h       |

**Figure 5-556. GPIO\_INTSTAT45 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| STAT5  |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| STAT5  |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| STAT4  |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| STAT4  |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-1677. GPIO\_INTSTAT45 Register Field Descriptions**

| Bit   | Field | Type   | Reset | Description                                                                                                                                                                      |
|-------|-------|--------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | STAT5 | R/W1TC | 0h    | Status of GPIO bank 4 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. |
| 15:0  | STAT4 | R/W1TC | 0h    | Status of GPIO bank 4 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. |

### 5.7.2.34 GPIO\_DIR67 Register

#### 1 GPIO\_DIR67 Register (Offset = 88h) [reset = FFFFFFFFh]

Direction Register.

Return to [Summary Table](#)

**Table 5-1678. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0088h       |
| GPIO1         | 5200 1088h       |
| GPIO2         | 5200 2088h       |
| GPIO3         | 5200 3088h       |

**Figure 5-557. GPIO\_DIR67 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DIR7  |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DIR7  |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DIR6  |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DIR6  |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |

**Table 5-1680. GPIO\_DIR67 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                           |
|-------|-------|------|-------|-------------------------------------------------------|
| 31:16 | DIR7  | R/W  | FFFFh | Direction of GPIO bank 7 bits, 0 = output, 1 = input. |
| 15:0  | DIR6  | R/W  | FFFFh | Direction of GPIO bank 6 bits, 0 = output, 1 = input. |

### 5.7.2.35 GPIO\_OUT\_DATA67 Register

#### 1 GPIO\_OUT\_DATA67 Register (Offset = 8Ch) [reset = 0h]

Output Drive State Register.

Return to [Summary Table](#)

**Table 5-1681. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 008Ch       |
| GPIO1         | 5200 108Ch       |
| GPIO2         | 5200 208Ch       |
| GPIO3         | 5200 308Ch       |

**Figure 5-558. GPIO\_OUT\_DATA67 Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| OUT7 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OUT7 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUT6 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUT6 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-1683. GPIO\_OUT\_DATA67 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                  |
|-------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | OUT7  | R/W  | 0h    | Output drive state of GPIO bank 7 bits, does not effect operation when it is configured as input. Reading it returns the output drive state. |
| 15:0  | OUT6  | R/W  | 0h    | Output drive state of GPIO bank 6 bits, does not effect operation when it is configured as input. Reading it returns the output drive state. |

### 5.7.2.36 GPIO\_SET\_DATA67 Register

#### 1 GPIO\_SET\_DATA67 Register (Offset = 90h) [reset = 0h]

Set Output Drive State Register.

Return to [Summary Table](#)

**Table 5-1684. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0090h       |
| GPIO1         | 5200 1090h       |
| GPIO2         | 5200 2090h       |
| GPIO3         | 5200 3090h       |

**Figure 5-559. GPIO\_SET\_DATA67 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SET7   |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SET7   |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SET6   |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SET6   |    |    |    |    |    |    |    |
| R/W1TS |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-1686. GPIO\_SET\_DATA67 Register Field Descriptions**

| Bit   | Field | Type   | Reset | Description                                                                                           |
|-------|-------|--------|-------|-------------------------------------------------------------------------------------------------------|
| 31:16 | SET7  | R/W1TS | 0h    | Writing 1 sets the output drive state of GPIO bank 7 bits. Reading it returns the output drive state. |
| 15:0  | SET6  | R/W1TS | 0h    | Writing 1 sets the output drive state of GPIO bank 6 bits. Reading it returns the output drive state. |

### 5.7.2.37 GPIO\_CLR\_DATA67 Register

#### 1 GPIO\_CLR\_DATA67 Register (Offset = 94h) [reset = 0h]

Clear Output Drive State Register.

Return to [Summary Table](#)

**Table 5-1687. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0094h       |
| GPIO1         | 5200 1094h       |
| GPIO2         | 5200 2094h       |
| GPIO3         | 5200 3094h       |

**Figure 5-560. GPIO\_CLR\_DATA67 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CLR7   |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CLR7   |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CLR6   |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CLR6   |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-1689. GPIO\_CLR\_DATA67 Register Field Descriptions**

| Bit   | Field | Type   | Reset | Description                                                                                 |
|-------|-------|--------|-------|---------------------------------------------------------------------------------------------|
| 31:16 | CLR7  | R/W1TC | 0h    | Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. |
| 15:0  | CLR6  | R/W1TC | 0h    | Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. |



### 5.7.2.38 GPIO\_IN\_DATA67 Register

#### 1 GPIO\_IN\_DATA67 Register (Offset = 98h) [reset = 0h]

Bank Status Register.

Return to [Summary Table](#)

**Table 5-1690. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 0098h       |
| GPIO1         | 5200 1098h       |
| GPIO2         | 5200 2098h       |
| GPIO3         | 5200 3098h       |

**Figure 5-561. GPIO\_IN\_DATA67 Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| IN7 |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| IN7 |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| IN6 |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| IN6 |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 5-1692. GPIO\_IN\_DATA67 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                 |
|-------|-------|------|-------|-----------------------------|
| 31:16 | IN7   | R    | 0h    | Status of GPIO bank 7 bits. |
| 15:0  | IN6   | R    | 0h    | Status of GPIO bank 6 bits. |

### 5.7.2.39 GPIO\_SET\_RIS\_TRIG67 Register

#### 1 GPIO\_SET\_RIS\_TRIG67 Register (Offset = 9Ch) [reset = 0h]

Set Rising Edge Detection Register.

Return to [Summary Table](#)

**Table 5-1693. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 009Ch       |
| GPIO1         | 5200 109Ch       |
| GPIO2         | 5200 209Ch       |
| GPIO3         | 5200 309Ch       |

**Figure 5-562. GPIO\_SET\_RIS\_TRIG67 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SETRIS7 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SETRIS7 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SETRIS6 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SETRIS6 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-1695. GPIO\_SET\_RIS\_TRIG67 Register Field Descriptions**

| Bit   | Field   | Type   | Reset | Description                                                   |
|-------|---------|--------|-------|---------------------------------------------------------------|
| 31:16 | SETRIS7 | R/W1TS | 0h    | Writing 1 enables rising edge detection for GPIO bank 7 bits. |
| 15:0  | SETRIS6 | R/W1TS | 0h    | Writing 1 enables rising edge detection for GPIO bank 6 bits. |

### 5.7.2.40 GPIO\_CLR\_RIS\_TRIG67 Register

#### 1 GPIO\_CLR\_RIS\_TRIG67 Register (Offset = A0h) [reset = 0h]

Clear Rising Edge Detection Register.

Return to [Summary Table](#)

**Table 5-1696. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 00A0h       |
| GPIO1         | 5200 10A0h       |
| GPIO2         | 5200 20A0h       |
| GPIO3         | 5200 30A0h       |

**Figure 5-563. GPIO\_CLR\_RIS\_TRIG67 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CLRRIS7 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CLRRIS7 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CLRRIS6 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CLRRIS6 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-1698. GPIO\_CLR\_RIS\_TRIG67 Register Field Descriptions**

| Bit   | Field   | Type   | Reset | Description                                                  |
|-------|---------|--------|-------|--------------------------------------------------------------|
| 31:16 | CLRRIS7 | R/W1TC | 0h    | Writing 1 clears rising edge detection for GPIO bank 7 bits. |
| 15:0  | CLRRIS6 | R/W1TC | 0h    | Writing 1 clears rising edge detection for GPIO bank 6 bits. |

### 5.7.2.41 GPIO\_SET\_FAL\_TRIG67 Register

#### 1 GPIO\_SET\_FAL\_TRIG67 Register (Offset = A4h) [reset = 0h]

Set Falling Edge Detection Register.

Return to [Summary Table](#)

**Table 5-1699. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 00A4h       |
| GPIO1         | 5200 10A4h       |
| GPIO2         | 5200 20A4h       |
| GPIO3         | 5200 30A4h       |

**Figure 5-564. GPIO\_SET\_FAL\_TRIG67 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SETFAL7 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SETFAL7 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SETFAL6 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SETFAL6 |    |    |    |    |    |    |    |
| R/W1TS  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-1701. GPIO\_SET\_FAL\_TRIG67 Register Field Descriptions**

| Bit   | Field   | Type   | Reset | Description                                                        |
|-------|---------|--------|-------|--------------------------------------------------------------------|
| 31:16 | SETFAL7 | R/W1TS | 0h    | Writing 1 enables falling edge detection for for GPIO bank 7 bits. |
| 15:0  | SETFAL6 | R/W1TS | 0h    | Writing 1 enables falling edge detection for for GPIO bank 6 bits. |

### 5.7.2.42 GPIO\_CLR\_FAL\_TRIG67 Register

#### 1 GPIO\_CLR\_FAL\_TRIG67 Register (Offset = A8h) [reset = 0h]

Clear Falling Edge Detection Register.

Return to [Summary Table](#)

**Table 5-1702. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 00A8h       |
| GPIO1         | 5200 10A8h       |
| GPIO2         | 5200 20A8h       |
| GPIO3         | 5200 30A8h       |

**Figure 5-565. GPIO\_CLR\_FAL\_TRIG67 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CLRFAL7 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CLRFAL7 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CLRFAL6 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CLRFAL6 |    |    |    |    |    |    |    |
| R/W1TC  |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-1704. GPIO\_CLR\_FAL\_TRIG67 Register Field Descriptions**

| Bit   | Field   | Type   | Reset | Description                                                       |
|-------|---------|--------|-------|-------------------------------------------------------------------|
| 31:16 | CLRFAL7 | R/W1TC | 0h    | Writing 1 clears falling edge detection for for GPIO bank 7 bits. |
| 15:0  | CLRFAL6 | R/W1TC | 0h    | Writing 1 clears falling edge detection for for GPIO bank 6 bits. |

### 5.7.2.43 GPIO\_INTSTAT67 Register

#### 1 GPIO\_INTSTAT67 Register (Offset = ACh) [reset = 0h]

Bank Interrupt Status Register.

Return to [Summary Table](#)

**Table 5-1705. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 00ACh       |
| GPIO1         | 5200 10ACh       |
| GPIO2         | 5200 20ACh       |
| GPIO3         | 5200 30ACh       |

**Figure 5-566. GPIO\_INTSTAT67 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| STAT7  |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| STAT7  |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| STAT6  |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| STAT6  |    |    |    |    |    |    |    |
| R/W1TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-1707. GPIO\_INTSTAT67 Register Field Descriptions**

| Bit   | Field | Type   | Reset | Description                                                                                                                                                                      |
|-------|-------|--------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | STAT7 | R/W1TC | 0h    | Status of GPIO bank 6 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. |
| 15:0  | STAT6 | R/W1TC | 0h    | Status of GPIO bank 6 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. |

### 5.7.2.44 GPIO\_DIR8 Register

#### 1 GPIO\_DIR8 Register (Offset = B0h) [reset = FFFFFFFFh]

Direction Register.

Return to [Summary Table](#)

**Table 5-1708. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 00B0h       |
| GPIO1         | 5200 10B0h       |
| GPIO2         | 5200 20B0h       |
| GPIO3         | 5200 30B0h       |

**Figure 5-567. GPIO\_DIR8 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| FFFFh    |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| FFFFh    |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DIR8     |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| FFFFh    |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DIR8     |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| FFFFh    |    |    |    |    |    |    |    |

**Table 5-1710. GPIO\_DIR8 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                           |
|-------|----------|------|-------|-------------------------------------------------------|
| 31:16 | RESERVED | R    | FFFFh | RESERVED                                              |
| 15:0  | DIR8     | R/W  | FFFFh | Direction of GPIO bank 8 bits, 0 = output, 1 = input. |

### 5.7.2.45 GPIO\_OUT\_DATA8 Register

#### 1 GPIO\_OUT\_DATA8 Register (Offset = B4h) [reset = 0h]

Output Drive State Register.

Return to [Summary Table](#)

**Table 5-1711. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 00B4h       |
| GPIO1         | 5200 10B4h       |
| GPIO2         | 5200 20B4h       |
| GPIO3         | 5200 30B4h       |

**Figure 5-568. GPIO\_OUT\_DATA8 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| OUT8     |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OUT8     |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-1713. GPIO\_OUT\_DATA8 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                  |
|-------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED | R    | 0h    | RESERVED                                                                                                                                     |
| 15:0  | OUT8     | R/W  | 0h    | Output drive state of GPIO bank 8 bits, does not effect operation when it is configured as input. Reading it returns the output drive state. |



### 5.7.2.46 GPIO\_SET\_DATA8 Register

#### 1 GPIO\_SET\_DATA8 Register (Offset = B8h) [reset = 0h]

Set Output Drive State Register.

Return to [Summary Table](#)

**Table 5-1714. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 00B8h       |
| GPIO1         | 5200 10B8h       |
| GPIO2         | 5200 20B8h       |
| GPIO3         | 5200 30B8h       |

**Figure 5-569. GPIO\_SET\_DATA8 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SET8     |    |    |    |    |    |    |    |
| R/W1TS   |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SET8     |    |    |    |    |    |    |    |
| R/W1TS   |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-1716. GPIO\_SET\_DATA8 Register Field Descriptions**

| Bit   | Field    | Type   | Reset | Description                                                                                           |
|-------|----------|--------|-------|-------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED | R      | 0h    | RESERVED                                                                                              |
| 15:0  | SET8     | R/W1TS | 0h    | Writing 1 sets the output drive state of GPIO bank 8 bits. Reading it returns the output drive state. |

### 5.7.2.47 GPIO\_CLR\_DATA8 Register

#### 1 GPIO\_CLR\_DATA8 Register (Offset = BCh) [reset = 0h]

Clear Output Drive State Register.

Return to [Summary Table](#)

**Table 5-1717. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 00BCh       |
| GPIO1         | 5200 10BCh       |
| GPIO2         | 5200 20BCh       |
| GPIO3         | 5200 30BCh       |

**Figure 5-570. GPIO\_CLR\_DATA8 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CLR8     |    |    |    |    |    |    |    |
| R/W1TC   |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CLR8     |    |    |    |    |    |    |    |
| R/W1TC   |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-1719. GPIO\_CLR\_DATA8 Register Field Descriptions**

| Bit   | Field    | Type   | Reset | Description                                                                                 |
|-------|----------|--------|-------|---------------------------------------------------------------------------------------------|
| 31:16 | RESERVED | R      | 0h    | RESERVED                                                                                    |
| 15:0  | CLR8     | R/W1TC | 0h    | Writing 1 clears the output drive state of GPIO. Reading it returns the output drive state. |

### 5.7.2.48 GPIO\_IN\_DATA8 Register

#### 1 GPIO\_IN\_DATA8 Register (Offset = C0h) [reset = 0h]

Bank Status Register.

Return to [Summary Table](#)

**Table 5-1720. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 00C0h       |
| GPIO1         | 5200 10C0h       |
| GPIO2         | 5200 20C0h       |
| GPIO3         | 5200 30C0h       |

**Figure 5-571. GPIO\_IN\_DATA8 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| IN8      |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| IN8      |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-1722. GPIO\_IN\_DATA8 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                 |
|-------|----------|------|-------|-----------------------------|
| 31:16 | RESERVED | R    | 0h    | RESERVED                    |
| 15:0  | IN8      | R    | 0h    | Status of GPIO bank 8 bits. |

### 5.7.2.49 GPIO\_SET\_RIS\_TRIG8 Register

#### 1 GPIO\_SET\_RIS\_TRIG8 Register (Offset = C4h) [reset = 0h]

Set Rising Edge Detection Register.

Return to [Summary Table](#)

**Table 5-1723. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 00C4h       |
| GPIO1         | 5200 10C4h       |
| GPIO2         | 5200 20C4h       |
| GPIO3         | 5200 30C4h       |

**Figure 5-572. GPIO\_SET\_RIS\_TRIG8 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SETRIS8  |    |    |    |    |    |    |    |
| R/W1TS   |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SETRIS8  |    |    |    |    |    |    |    |
| R/W1TS   |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-1725. GPIO\_SET\_RIS\_TRIG8 Register Field Descriptions**

| Bit   | Field    | Type   | Reset | Description                                                   |
|-------|----------|--------|-------|---------------------------------------------------------------|
| 31:16 | RESERVED | NONE   | 0h    | Reserved                                                      |
| 15:0  | SETRIS8  | R/W1TS | 0h    | Writing 1 enables rising edge detection for GPIO bank 8 bits. |

### 5.7.2.50 GPIO\_CLR\_RIS\_TRIG8 Register

#### 1 GPIO\_CLR\_RIS\_TRIG8 Register (Offset = C8h) [reset = 0h]

Clear Rising Edge Detection Register.

Return to [Summary Table](#)

**Table 5-1726. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 00C8h       |
| GPIO1         | 5200 10C8h       |
| GPIO2         | 5200 20C8h       |
| GPIO3         | 5200 30C8h       |

**Figure 5-573. GPIO\_CLR\_RIS\_TRIG8 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CLRRIS8  |    |    |    |    |    |    |    |
| R/W1TC   |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CLRRIS8  |    |    |    |    |    |    |    |
| R/W1TC   |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-1728. GPIO\_CLR\_RIS\_TRIG8 Register Field Descriptions**

| Bit   | Field    | Type   | Reset | Description                                                  |
|-------|----------|--------|-------|--------------------------------------------------------------|
| 31:16 | RESERVED | NONE   | 0h    | Reserved                                                     |
| 15:0  | CLRRIS8  | R/W1TC | 0h    | Writing 1 clears rising edge detection for GPIO bank 8 bits. |

### 5.7.2.51 GPIO\_SET\_FAL\_TRIG8 Register

#### 1 GPIO\_SET\_FAL\_TRIG8 Register (Offset = CCh) [reset = 0h]

Set Falling Edge Detection Register.

Return to [Summary Table](#)

**Table 5-1729. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 00CCh       |
| GPIO1         | 5200 10CCh       |
| GPIO2         | 5200 20CCh       |
| GPIO3         | 5200 30CCh       |

**Figure 5-574. GPIO\_SET\_FAL\_TRIG8 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SETFAL8  |    |    |    |    |    |    |    |
| R/W1TS   |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SETFAL8  |    |    |    |    |    |    |    |
| R/W1TS   |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-1731. GPIO\_SET\_FAL\_TRIG8 Register Field Descriptions**

| Bit   | Field    | Type   | Reset | Description                                                        |
|-------|----------|--------|-------|--------------------------------------------------------------------|
| 31:16 | RESERVED | NONE   | 0h    | Reserved                                                           |
| 15:0  | SETFAL8  | R/W1TS | 0h    | Writing 1 enables falling edge detection for for GPIO bank 8 bits. |

### 5.7.2.52 GPIO\_CLR\_FAL\_TRIG8 Register

#### 1 GPIO\_CLR\_FAL\_TRIG8 Register (Offset = D0h) [reset = 0h]

Clear Falling Edge Detection Register.

Return to [Summary Table](#)

**Table 5-1732. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 00D0h       |
| GPIO1         | 5200 10D0h       |
| GPIO2         | 5200 20D0h       |
| GPIO3         | 5200 30D0h       |

**Figure 5-575. GPIO\_CLR\_FAL\_TRIG8 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CLRFAL8  |    |    |    |    |    |    |    |
| R/W1TC   |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CLRFAL8  |    |    |    |    |    |    |    |
| R/W1TC   |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-1734. GPIO\_CLR\_FAL\_TRIG8 Register Field Descriptions**

| Bit   | Field    | Type   | Reset | Description                                                       |
|-------|----------|--------|-------|-------------------------------------------------------------------|
| 31:16 | RESERVED | NONE   | 0h    | Reserved                                                          |
| 15:0  | CLRFAL8  | R/W1TC | 0h    | Writing 1 clears falling edge detection for for GPIO bank 8 bits. |

### 5.7.2.53 GPIO\_INTSTAT8 Register

#### 1 GPIO\_INTSTAT8 Register (Offset = D4h) [reset = 0h]

Bank Interrupt Status Register.

Return to [Summary Table](#)

**Table 5-1735. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPIO0         | 5200 00D4h       |
| GPIO1         | 5200 10D4h       |
| GPIO2         | 5200 20D4h       |
| GPIO3         | 5200 30D4h       |

**Figure 5-576. GPIO\_INTSTAT8 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| STAT8    |    |    |    |    |    |    |    |
| R/W1TC   |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| STAT8    |    |    |    |    |    |    |    |
| R/W1TC   |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-1737. GPIO\_INTSTAT8 Register Field Descriptions**

| Bit   | Field    | Type   | Reset | Description                                                                                                                                                                      |
|-------|----------|--------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED | R      | 0h    | RESERVED                                                                                                                                                                         |
| 15:0  | STAT8    | R/W1TC | 0h    | Status of GPIO bank 8 bits interrupt. Reading back 1 = interrupt occurred. 0 = interrupt hasnt occurred since last cleared. Writing 1 clears the corresponding interrupt status. |



## 5.8 GPIO\_XBAR\_INTR

### GPIO\_XBAR\_INTR

#### 5.8.1 GPIO\_XBAR\_INTR Summaries

#### GPIO\_XBAR\_INTR Summaries

**Table 5-1738. GPIO\_XBAR\_INTR Registers, Base Address=52E0 2000h, Length=1024**

| Offset | Length | Register Name                            | GPIO_XBAR_INTR Physical Address |
|--------|--------|------------------------------------------|---------------------------------|
| 0h     | 32     | <a href="#">GPIO_XBAR_INTR_PID</a>       | 52E0 2000h                      |
| 4h     | 32     | <a href="#">GPIO_XBAR_INTR_MUXCNTL_J</a> | 52E0 2004h + formula            |

#### 5.8.2 GPIO\_XBAR\_INTR Registers

#### GPIO\_XBAR\_INTR Registers

### 5.8.2.1 GPIO\_XBAR\_INTR\_PID Register

#### 1 GPIO\_XBAR\_INTR\_PID Register (Offset = 0h) [reset = 66948100h]

Identification register.

Return to [Summary Table](#)

**Table 5-1739. Instance Table**

| Instance Name  | Physical Address |
|----------------|------------------|
| GPIO_XBAR_INTR | 52E0 2000h       |

**Figure 5-577. GPIO\_XBAR\_INTR\_PID Name Register**

|          |    |        |    |          |        |    |    |
|----------|----|--------|----|----------|--------|----|----|
| 31       | 30 | 29     | 28 | 27       | 26     | 25 | 24 |
| SCHEME   |    | BU     |    | FUNCTION |        |    |    |
| R        |    | R      |    | R        |        |    |    |
| 1h       |    | 2h     |    | 694h     |        |    |    |
| 23       | 22 | 21     | 20 | 19       | 18     | 17 | 16 |
| FUNCTION |    |        |    |          |        |    |    |
| R        |    |        |    |          |        |    |    |
| 694h     |    |        |    |          |        |    |    |
| 15       | 14 | 13     | 12 | 11       | 10     | 9  | 8  |
| RTLVER   |    |        |    |          | MAJREV |    |    |
| R        |    |        |    |          | R      |    |    |
| 10h      |    |        |    |          | 1h     |    |    |
| 7        | 6  | 5      | 4  | 3        | 2      | 1  | 0  |
| CUSTOM   |    | MINREV |    |          |        |    |    |
| R        |    | R      |    |          |        |    |    |
| 0h       |    | 0h     |    |          |        |    |    |

**Table 5-1741. GPIO\_XBAR\_INTR\_PID Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description   |
|-------|----------|------|-------|---------------|
| 31:30 | SCHEME   | R    | 1h    | Scheme        |
| 29:28 | BU       | R    | 2h    | bu            |
| 27:16 | FUNCTION | R    | 694h  | function      |
| 15:11 | RTLVER   | R    | 10h   | Rtl version   |
| 10:8  | MAJREV   | R    | 1h    | major version |
| 7:6   | CUSTOM   | R    | 0h    | custom id     |
| 5:0   | MINREV   | R    | 0h    | minor version |

### 5.8.2.2 GPIO\_XBAR\_INTR\_MUXCNTL\_j Register

#### 1 GPIO\_XBAR\_INTR\_MUXCNTL\_j Register (Offset = 4h + formula) [reset = 0h]

Interrupt mux control register.

Return to [Summary Table](#)

Offset = (j \* 4h); where j = 0 to 29d

**Table 5-1742. Instance Table**

| Instance Name  | Physical Address     |
|----------------|----------------------|
| GPIO_XBAR_INTR | 52E0 2004h + formula |

**Figure 5-578. GPIO\_XBAR\_INTR\_MUXCNTL\_j Name Register**

|          |    |    |    |    |    |    |            |
|----------|----|----|----|----|----|----|------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24         |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16         |
| RESERVED |    |    |    |    |    |    | INT_ENABLE |
| NONE     |    |    |    |    |    |    | R/W        |
| 0h       |    |    |    |    |    |    | 0h         |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8          |
| RESERVED |    |    |    |    |    |    |            |
| NONE     |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0          |
| MUX_CNTL |    |    |    |    |    |    |            |
| R/W      |    |    |    |    |    |    |            |
| 0h       |    |    |    |    |    |    |            |

**Table 5-1744. GPIO\_XBAR\_INTR\_MUXCNTL\_j Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                           |
|-------|------------|------|-------|-------------------------------------------------------|
| 31:17 | RESERVED   | NONE | 0h    | Reserved                                              |
| 16    | INT_ENABLE | R/W  | 0h    | Interrupt j Output Enable.<br>0 Disabled<br>1 Enabled |
| 15:8  | RESERVED   | NONE | 0h    | Reserved                                              |
| 7:0   | MUX_CNTL   | R/W  | 0h    | Mux Control for Interrupt j.                          |

## 5.9 GPMC

### GPMC

#### 5.9.1 GPMC Summaries

#### GPMC Summaries

**Table 5-1745. GPMC Registers, Base Address=4840 0000h, Length=1024**

| Offset | Length | Register Name                         | GPMC0 Physical Address |
|--------|--------|---------------------------------------|------------------------|
| 0h     | 32     | <a href="#">GPMC_REVISION</a>         | 4840 0000h             |
| 14h    | 32     | <a href="#">GPMC_SYSSTATUS</a>        | 4840 0014h             |
| 18h    | 32     | <a href="#">GPMC_IRQSTATUS</a>        | 4840 0018h             |
| 1Ch    | 32     | <a href="#">GPMC_IRQENABLE</a>        | 4840 001Ch             |
| 40h    | 32     | <a href="#">GPMC_TIMEOUT_CONTROL</a>  | 4840 0040h             |
| 44h    | 32     | <a href="#">GPMC_ERR_ADDRESS</a>      | 4840 0044h             |
| 48h    | 32     | <a href="#">GPMC_ERR_TYPE</a>         | 4840 0048h             |
| 50h    | 32     | <a href="#">GPMC_CONFIG</a>           | 4840 0050h             |
| 54h    | 32     | <a href="#">GPMC_STATUS</a>           | 4840 0054h             |
| 1E0h   | 32     | <a href="#">GPMC_PREFETCH_CONFIG1</a> | 4840 01E0h             |
| 1E4h   | 32     | <a href="#">GPMC_PREFETCH_CONFIG2</a> | 4840 01E4h             |
| 1ECh   | 32     | <a href="#">GPMC_PREFETCH_CONTROL</a> | 4840 01ECh             |
| 1F0h   | 32     | <a href="#">GPMC_PREFETCH_STATUS</a>  | 4840 01F0h             |
| 1F4h   | 32     | <a href="#">GPMC_ECC_CONFIG</a>       | 4840 01F4h             |
| 1F8h   | 32     | <a href="#">GPMC_ECC_CONTROL</a>      | 4840 01F8h             |
| 1FCh   | 32     | <a href="#">GPMC_ECC_SIZE_CONFIG</a>  | 4840 01FCh             |
| 200h   | 32     | <a href="#">GPMC_ECC_RESULT_J</a>     | 4840 0200h + formula   |
| 2D0h   | 32     | <a href="#">GPMC_BCH_SWDATA</a>       | 4840 02D0h             |
| 60h    | 32     | <a href="#">GPMC_CONFIG1</a>          | 4840 0060h + formula   |
| 64h    | 32     | <a href="#">GPMC_CONFIG2</a>          | 4840 0064h + formula   |
| 68h    | 32     | <a href="#">GPMC_CONFIG3</a>          | 4840 0068h + formula   |
| 6Ch    | 32     | <a href="#">GPMC_CONFIG4</a>          | 4840 006Ch + formula   |
| 70h    | 32     | <a href="#">GPMC_CONFIG5</a>          | 4840 0070h + formula   |
| 74h    | 32     | <a href="#">GPMC_CONFIG6</a>          | 4840 0074h + formula   |
| 78h    | 32     | <a href="#">GPMC_CONFIG7</a>          | 4840 0078h + formula   |
| 7Ch    | 32     | <a href="#">GPMC_NAND_COMMAND</a>     | 4840 007Ch + formula   |
| 80h    | 32     | <a href="#">GPMC_NAND_ADDRESS</a>     | 4840 0080h + formula   |
| 84h    | 32     | <a href="#">GPMC_NAND_DATA</a>        | 4840 0084h + formula   |
| 240h   | 32     | <a href="#">GPMC_BCH_RESULT_0</a>     | 4840 0240h + formula   |
| 244h   | 32     | <a href="#">GPMC_BCH_RESULT_1</a>     | 4840 0244h + formula   |
| 248h   | 32     | <a href="#">GPMC_BCH_RESULT_2</a>     | 4840 0248h + formula   |
| 24Ch   | 32     | <a href="#">GPMC_BCH_RESULT_3</a>     | 4840 024Ch + formula   |
| 300h   | 32     | <a href="#">GPMC_BCH_RESULT_4</a>     | 4840 0300h + formula   |
| 304h   | 32     | <a href="#">GPMC_BCH_RESULT_5</a>     | 4840 0304h + formula   |
| 308h   | 32     | <a href="#">GPMC_BCH_RESULT_6</a>     | 4840 0308h + formula   |

## **5.9.2 GPMC Registers**

### **GPMC Registers**

### 5.9.2.1 GPMC\_REVISION Register

#### 1 GPMC\_REVISION Register (Offset = 0h) [reset = 60h]

This register contains the IP revision code .

Return to [Summary Table](#)

**Table 5-1746. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPMC0         | 4840 0000h       |

**Figure 5-579. GPMC\_REVISION Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_230 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_230 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_230 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| REV          |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 60h          |    |    |    |    |    |    |    |

**Table 5-1748. GPMC\_REVISION Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                               |
|------|--------------|------|-------|-----------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED_230 | R    | 0h    | Reads returns 0                                                                                           |
| 7:0  | REV          | R    | 60h   | IP revision<br>[7:4]<br>Major revision<br>[3:0]<br>Minor revision<br>Examples: 0x10 for 1.0, 0x21 for 2.1 |

### 5.9.2.2 GPMC\_SYSSTATUS Register

#### 1 GPMC\_SYSSTATUS Register (Offset = 14h) [reset = 0h]

This register provides status information about the module, excluding the interrupt status information

Return to [Summary Table](#)

**Table 5-1749. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPMC0         | 4840 0014h       |

**Figure 5-580. GPMC\_SYSSTATUS Name Register**

|              |    |    |    |    |    |    |           |
|--------------|----|----|----|----|----|----|-----------|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24        |
| RESERVED_235 |    |    |    |    |    |    |           |
| R            |    |    |    |    |    |    |           |
| 0h           |    |    |    |    |    |    |           |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16        |
| RESERVED_235 |    |    |    |    |    |    |           |
| R            |    |    |    |    |    |    |           |
| 0h           |    |    |    |    |    |    |           |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8         |
| RESERVED_235 |    |    |    |    |    |    |           |
| R            |    |    |    |    |    |    |           |
| 0h           |    |    |    |    |    |    |           |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0         |
| RESERVED     |    |    |    |    |    |    | RESETDONE |
| R            |    |    |    |    |    |    | R         |
| 0h           |    |    |    |    |    |    | 0h        |

**Table 5-1751. GPMC\_SYSSTATUS Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                     |
|------|--------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED_235 | R    | 0h    | Reads returns 0                                                                                 |
| 7:1  | RESERVED     | R    | 0h    | Reads returns 0 [reserved for OCP-socket status information]                                    |
| 0    | RESETDONE    | R    | 0h    | Internal reset monitoring<br>1      Reset completed<br>0      Internal module reset in on-going |

### 5.9.2.3 GPMC\_IRQSTATUS Register

#### 1 GPMC\_IRQSTATUS Register (Offset = 18h) [reset = 0h]

This interrupt status register regroups all the status of the module internal events that can generate an interrupt.

Return to [Summary Table](#)

**Table 5-1752. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPMC0         | 4840 0018h       |

**Figure 5-581. GPMC\_IRQSTATUS Name Register**

|              |    |    |    |                          |                          |                          |                          |
|--------------|----|----|----|--------------------------|--------------------------|--------------------------|--------------------------|
| 31           | 30 | 29 | 28 | 27                       | 26                       | 25                       | 24                       |
| RESERVED_218 |    |    |    |                          |                          |                          |                          |
| R            |    |    |    |                          |                          |                          |                          |
| 0h           |    |    |    |                          |                          |                          |                          |
| 23           | 22 | 21 | 20 | 19                       | 18                       | 17                       | 16                       |
| RESERVED_218 |    |    |    |                          |                          |                          |                          |
| R            |    |    |    |                          |                          |                          |                          |
| 0h           |    |    |    |                          |                          |                          |                          |
| 15           | 14 | 13 | 12 | 11                       | 10                       | 9                        | 8                        |
| RESERVED_218 |    |    |    | WAIT3EDGEDETECTIONSTATUS | WAIT2EDGEDETECTIONSTATUS | WAIT1EDGEDETECTIONSTATUS | WAIT0EDGEDETECTIONSTATUS |
| R            |    |    |    | R/W1TC                   | R/W1TC                   | R/W1TC                   | R/W1TC                   |
| 0h           |    |    |    | 0h                       | 0h                       | 0h                       | 0h                       |
| 7            | 6  | 5  | 4  | 3                        | 2                        | 1                        | 0                        |
| RESERVED_219 |    |    |    |                          |                          | TERMINALCOUNTSTATUS      | FIFOEVENTSTATUS          |
| R            |    |    |    |                          |                          | R/W1TC                   | R/W1TC                   |
| 0h           |    |    |    |                          |                          | 0h                       | 0h                       |

**Table 5-1754. GPMC\_IRQSTATUS Register Field Descriptions**

| Bit   | Field                    | Type   | Reset | Description                                                                                                                                                                                                                                                                               |
|-------|--------------------------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED_218             | R      | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                                                                                                                        |
| 11    | WAIT3EDGEDETECTIONSTATUS | R/W1TC | 0h    | Status of the Wait3 Edge Detection interrupt<br>1 Read 1: A transition on WAIT3 input pin has been detected<br>1 Write 1: wait3EdgeDetection status bit is reset<br>0 Read 0: A transition on WAIT3 input pin has not been detected<br>0 Write 0: wait3EdgeDetection status bit unchanged |
| 10    | WAIT2EDGEDETECTIONSTATUS | R/W1TC | 0h    | Status of the Wait2 Edge Detection interrupt<br>1 Read 1: A transition on WAIT2 input pin has been detected<br>1 Write 1: wait2EdgeDetection status bit is reset<br>0 Read 0: A transition on WAIT2 input pin has not been detected<br>0 Write 0: wait2EdgeDetection status bit unchanged |



**Table 5-1754. GPMC\_IRQSTATUS Register Field Descriptions (continued)**

| Bit | Field                        | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-----|------------------------------|--------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9   | WAIT1EDGEDETECTION<br>STATUS | R/W1TC | 0h    | <p>Status of the Wait1 Edge Detection interrupt</p> <p>1      Read 1: A transition on WAIT1 input pin has been detected</p> <p>1      Write 1: wait1EdgeDetection status bit is reset</p> <p>0      Read 0: A transition on WAIT1 input pin has not been detected</p> <p>0      Write 0: wait1EdgeDetection status bit unchanged</p>                                                                                                                                                                                        |
| 8   | WAIT0EDGEDETECTION<br>STATUS | R/W1TC | 0h    | <p>Status of the Wait0 Edge Detection interrupt</p> <p>1      Read 1: A transition on WAIT0 input pin has been detected</p> <p>1      Write 1: wait0EdgeDetection status bit is reset</p> <p>0      Read 0: A transition on WAIT0 input pin has not been detected</p> <p>0      Write 0: wait0EdgeDetection status bit unchanged</p>                                                                                                                                                                                        |
| 7:2 | RESERVED_219                 | R      | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 1   | TERMINALCOUNTSTATU<br>S      | R/W1TC | 0h    | <p>Status of the TerminalCountEvent interrupt</p> <p>1      Read 1: Indicates that CountValue is equal to 0</p> <p>1      Write 1: TerminalCountEvent status bit is reset</p> <p>0      Read 0: Indicates that CountValue is greater than 0</p> <p>0      Write 0: TerminalCountEvent status bit unchanged</p>                                                                                                                                                                                                              |
| 0   | FIFOEVENTSTATUS              | R/W1TC | 0h    | <p>Status of the FIFOEvent interrupt</p> <p>1      Read 1: Indicates than at least FIFOThreshold bytes are available in prefetch mode and at least FIFOThreshold bytes free places are available in write posting mode.</p> <p>1      Write 1: FIFOEvent status bit is reset</p> <p>0      Read 0: Indicates than less than FIFOThreshold bytes are available in prefetch mode and less than FIFOThreshold bytes free places are available in write posting mode.</p> <p>0      Write 0: FIFOEvent status bit unchanged</p> |

### 5.9.2.4 GPMC\_IRQENABLE Register

#### 1 GPMC\_IRQENABLE Register (Offset = 1Ch) [reset = 0h]

The interrupt enable register allows to mask/unmask the module internal sources of interrupt, on a event-by-event basis.

Return to [Summary Table](#)

**Table 5-1755. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPMC0         | 4840 001Ch       |

**Figure 5-582. GPMC\_IRQENABLE Name Register**

|              |    |    |    |                          |                          |                          |                          |
|--------------|----|----|----|--------------------------|--------------------------|--------------------------|--------------------------|
| 31           | 30 | 29 | 28 | 27                       | 26                       | 25                       | 24                       |
| RESERVED_216 |    |    |    |                          |                          |                          |                          |
| R            |    |    |    |                          |                          |                          |                          |
| 0h           |    |    |    |                          |                          |                          |                          |
| 23           | 22 | 21 | 20 | 19                       | 18                       | 17                       | 16                       |
| RESERVED_216 |    |    |    |                          |                          |                          |                          |
| R            |    |    |    |                          |                          |                          |                          |
| 0h           |    |    |    |                          |                          |                          |                          |
| 15           | 14 | 13 | 12 | 11                       | 10                       | 9                        | 8                        |
| RESERVED_216 |    |    |    | WAIT3EDGEDETECTIONENABLE | WAIT2EDGEDETECTIONENABLE | WAIT1EDGEDETECTIONENABLE | WAIT0EDGEDETECTIONENABLE |
| R            |    |    |    | R/W                      | R/W                      | R/W                      | R/W                      |
| 0h           |    |    |    | 0h                       | 0h                       | 0h                       | 0h                       |
| 7            | 6  | 5  | 4  | 3                        | 2                        | 1                        | 0                        |
| RESERVED_217 |    |    |    |                          |                          | TERMINALCOUNTENABLE      | FIFOEVENTENABLE          |
| R            |    |    |    |                          |                          | R/W                      | R/W                      |
| 0h           |    |    |    |                          |                          | 0h                       | 0h                       |

**Table 5-1757. GPMC\_IRQENABLE Register Field Descriptions**

| Bit   | Field                    | Type | Reset | Description                                                                                                                                           |
|-------|--------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED_216             | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                    |
| 11    | WAIT3EDGEDETECTIONENABLE | R/W  | 0h    | Enables the Wait3 Edge Detection interrupt<br>1 wait3EdgeDetection event generates an interrupt if occurs<br>0 wait3EdgeDetection interrupt is masked |
| 10    | WAIT2EDGEDETECTIONENABLE | R/W  | 0h    | Enables the Wait2 Edge Detection interrupt<br>1 wait2EdgeDetection event generates an interrupt if occurs<br>0 wait2EdgeDetection interrupt is masked |
| 9     | WAIT1EDGEDETECTIONENABLE | R/W  | 0h    | Enables the Wait1 Edge Detection interrupt<br>1 wait1EdgeDetection event generates an interrupt if occurs<br>0 wait1EdgeDetection interrupt is masked |
| 8     | WAIT0EDGEDETECTIONENABLE | R/W  | 0h    | Enables the Wait0 Edge Detection interrupt<br>1 wait0EdgeDetection event generates an interrupt if occurs<br>0 wait0EdgeDetection interrupt is masked |

**Table 5-1757. GPMC\_IRQENABLE Register Field Descriptions (continued)**

| Bit | Field                    | Type | Reset | Description                                                                                                                                                                           |
|-----|--------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:2 | RESERVED_217             | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                    |
| 1   | TERMINALCOUNTEVENTENABLE | R/W  | 0h    | Enables TerminalCountEvent interrupt issuing in pre-fetch or write posting mode<br>1      TerminalCountEvent interrupt is not masked<br>0      TerminalCountEvent interrupt is masked |
| 0   | FIFOEVENTENABLE          | R/W  | 0h    | Enables the FIFOEvent interrupt<br>1      FIFOEvent interrupt is not masked<br>0      FIFOEvent interrupt is masked                                                                   |

### 5.9.2.5 GPMC\_TIMEOUT\_CONTROL Register

#### 1 GPMC\_TIMEOUT\_CONTROL Register (Offset = 40h) [reset = 1FF0h]

The GPMC\_TIMEOUT\_CONTROL register allows the user to set the start value of the timeout counter

Return to [Summary Table](#)

**Table 5-1758. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPMC0         | 4840 0040h       |

**Figure 5-583. GPMC\_TIMEOUT\_CONTROL Name Register**

|                   |    |    |    |                   |    |               |    |
|-------------------|----|----|----|-------------------|----|---------------|----|
| 31                | 30 | 29 | 28 | 27                | 26 | 25            | 24 |
| RESERVED_237      |    |    |    |                   |    |               |    |
| R                 |    |    |    |                   |    |               |    |
| 0h                |    |    |    |                   |    |               |    |
| 23                | 22 | 21 | 20 | 19                | 18 | 17            | 16 |
| RESERVED_237      |    |    |    |                   |    |               |    |
| R                 |    |    |    |                   |    |               |    |
| 0h                |    |    |    |                   |    |               |    |
| 15                | 14 | 13 | 12 | 11                | 10 | 9             | 8  |
| RESERVED_237      |    |    |    | TIMEOUTSTARTVALUE |    |               |    |
| R                 |    |    |    | R/W               |    |               |    |
| 0h                |    |    |    | 1FFh              |    |               |    |
| 7                 | 6  | 5  | 4  | 3                 | 2  | 1             | 0  |
| TIMEOUTSTARTVALUE |    |    |    | RESERVED_238      |    | TIMEOUTENABLE |    |
| R/W               |    |    |    | R                 |    | R/W           |    |
| 1FFh              |    |    |    | 0h                |    | 0h            |    |

**Table 5-1760. GPMC\_TIMEOUT\_CONTROL Register Field Descriptions**

| Bit   | Field             | Type | Reset | Description                                                                                                                                                       |
|-------|-------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:13 | RESERVED_237      | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                |
| 12:4  | TIMEOUTSTARTVALUE | R/W  | 1FFh  | Start value of the time-out counter [0x000 corresponds to 0 GPMC.FCLK cycle, 0x001 corresponds to 1 GmpcClk cycle, &, 0x1FF corresponds to 511 GPMC.FCLK cycles.] |
| 3:1   | RESERVED_238      | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                |
| 0     | TIMEOUTENABLE     | R/W  | 0h    | Enable bit of the TimeOut feature<br>1 TimeOut feature is enabled<br>0 TimeOut feature is disabled                                                                |

### 5.9.2.6 GPMC\_ERR\_ADDRESS Register

#### 1 GPMC\_ERR\_ADDRESS Register (Offset = 44h) [reset = 0h]

The GPMC\_ERR\_ADDRESS register stores the address of the illegal access when an error occurs .

Return to [Summary Table](#)

**Table 5-1761. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPMC0         | 4840 0044h       |

**Figure 5-584. GPMC\_ERR\_ADDRESS Name Register**

|             |            |    |    |    |    |    |    |
|-------------|------------|----|----|----|----|----|----|
| 31          | 30         | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_21 | ILLEGALADD |    |    |    |    |    |    |
| 2           |            |    |    |    |    |    |    |
| R           | R          |    |    |    |    |    |    |
| 0h          | 0h         |    |    |    |    |    |    |
| 23          | 22         | 21 | 20 | 19 | 18 | 17 | 16 |
| ILLEGALADD  |            |    |    |    |    |    |    |
| R           |            |    |    |    |    |    |    |
| 0h          |            |    |    |    |    |    |    |
| 15          | 14         | 13 | 12 | 11 | 10 | 9  | 8  |
| ILLEGALADD  |            |    |    |    |    |    |    |
| R           |            |    |    |    |    |    |    |
| 0h          |            |    |    |    |    |    |    |
| 7           | 6          | 5  | 4  | 3  | 2  | 1  | 0  |
| ILLEGALADD  |            |    |    |    |    |    |    |
| R           |            |    |    |    |    |    |    |
| 0h          |            |    |    |    |    |    |    |

**Table 5-1763. GPMC\_ERR\_ADDRESS Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                                   |
|------|--------------|------|-------|---------------------------------------------------------------------------------------------------------------|
| 31   | RESERVED_212 | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                            |
| 30:0 | ILLEGALADD   | R    | 0h    | Address of illegal access : A30[0 for memory region, 1 for GPMC register region] and A29-A0[1 GBytes maximum] |

### 5.9.2.7 GPMC\_ERR\_TYPE Register

#### 1 GPMC\_ERR\_TYPE Register (Offset = 48h) [reset = 0h]

The GPMC\_ERR\_TYPE register stores the type of error when an error occurs .

Return to [Summary Table](#)

**Table 5-1764. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPMC0         | 4840 0048h       |

**Figure 5-585. GPMC\_ERR\_TYPE Name Register**

|              |    |    |                     |                      |                  |                  |            |
|--------------|----|----|---------------------|----------------------|------------------|------------------|------------|
| 31           | 30 | 29 | 28                  | 27                   | 26               | 25               | 24         |
| RESERVED_215 |    |    |                     |                      |                  |                  |            |
| R            |    |    |                     |                      |                  |                  |            |
| 0h           |    |    |                     |                      |                  |                  |            |
| 23           | 22 | 21 | 20                  | 19                   | 18               | 17               | 16         |
| RESERVED_215 |    |    |                     |                      |                  |                  |            |
| R            |    |    |                     |                      |                  |                  |            |
| 0h           |    |    |                     |                      |                  |                  |            |
| 15           | 14 | 13 | 12                  | 11                   | 10               | 9                | 8          |
| RESERVED_215 |    |    |                     | ILLEGALMCMD          |                  |                  |            |
| R            |    |    |                     | R                    |                  |                  |            |
| 0h           |    |    |                     | 0h                   |                  |                  |            |
| 7            | 6  | 5  | 4                   | 3                    | 2                | 1                | 0          |
| RESERVED_213 |    |    | ERRORNOTSU<br>PPADD | ERRORNOTSU<br>PPMCMD | ERRORTIMEO<br>UT | RESERVED_21<br>4 | ERRORVALID |
| R            |    |    | R                   | R                    | R                | R                | R/W1TC     |
| 0h           |    |    | 0h                  | 0h                   | 0h               | 0h               | 0h         |

**Table 5-1766. GPMC\_ERR\_TYPE Register Field Descriptions**

| Bit   | Field            | Type   | Reset | Description                                                                                                                                                                  |
|-------|------------------|--------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:11 | RESERVED_215     | R      | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                           |
| 10:8  | ILLEGALMCMD      | R      | 0h    | System Command of the transaction that caused the error                                                                                                                      |
| 7:5   | RESERVED_213     | R      | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                           |
| 4     | ERRORNOTSUPPADD  | R      | 0h    | Not supported Address error<br>1 The error is due to a non supported Address<br>0 No error occurs                                                                            |
| 3     | ERRORNOTSUPPMCMD | R      | 0h    | Not supported Command error<br>1 The error is due to a non supported Command<br>0 No error occurs                                                                            |
| 2     | ERRORTIMEOUT     | R      | 0h    | Time-out error<br>1 The error is due to a time out<br>0 No error occurs                                                                                                      |
| 1     | RESERVED_214     | R      | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                           |
| 0     | ERRORVALID       | R/W1TC | 0h    | Error validity status - Must be explicitly cleared with a write 1 transaction<br>1 Error detected and logged in the other error fields<br>0 All error fields no longer valid |

### 5.9.2.8 GPMC\_CONFIG Register

#### 1 GPMC\_CONFIG Register (Offset = 50h) [reset = A00h]

The configuration register allows global configuration of the GPMC .

Return to [Summary Table](#)

**Table 5-1767. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPMC0         | 4840 0050h       |

**Figure 5-586. GPMC\_CONFIG Name Register**

|            |    |    |              |                  |                  |                  |                      |
|------------|----|----|--------------|------------------|------------------|------------------|----------------------|
| 31         | 30 | 29 | 28           | 27               | 26               | 25               | 24                   |
| RESERVED_1 |    |    |              |                  |                  |                  |                      |
| R          |    |    |              |                  |                  |                  |                      |
| 0h         |    |    |              |                  |                  |                  |                      |
| 23         | 22 | 21 | 20           | 19               | 18               | 17               | 16                   |
| RESERVED_1 |    |    |              |                  |                  |                  |                      |
| R          |    |    |              |                  |                  |                  |                      |
| 0h         |    |    |              |                  |                  |                  |                      |
| 15         | 14 | 13 | 12           | 11               | 10               | 9                | 8                    |
| RESERVED_1 |    |    |              | WAIT3PINPOLARITY | WAIT2PINPOLARITY | WAIT1PINPOLARITY | WAIT0PINPOLARITY     |
| R          |    |    |              | R/W              | R/W              | R/W              | R/W                  |
| 0h         |    |    |              | 1h               | 0h               | 1h               | 0h                   |
| 7          | 6  | 5  | 4            | 3                | 2                | 1                | 0                    |
| RESERVED_0 |    |    | WRITEPROTECT | RESERVED_2       |                  | LIMITEDADDRESS   | NANDFORCEPOSTEDWRITE |
| R          |    |    | R/W          | R                |                  | R/W              | R/W                  |
| 0h         |    |    | 0h           | 0h               |                  | 0h               | 0h                   |

**Table 5-1769. GPMC\_CONFIG Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                           |
|-------|------------------|------|-------|---------------------------------------------------------------------------------------|
| 31:12 | RESERVED_1       | R    | 0h    | Write 0's for future compatibility. Read returns 0                                    |
| 11    | WAIT3PINPOLARITY | R/W  | 1h    | Selects the polarity of input pin WAIT3<br>1 WAIT3 active high<br>0 WAIT3 active low  |
| 10    | WAIT2PINPOLARITY | R/W  | 0h    | Selects the polarity of input pin WAIT2<br>1 WAIT2 active high<br>0 WAIT2 active low  |
| 9     | WAIT1PINPOLARITY | R/W  | 1h    | Selects the polarity of input pin WAIT1<br>1 WAIT1 active high<br>0 WAIT1 active low  |
| 8     | WAIT0PINPOLARITY | R/W  | 0h    | Selects the polarity of input pin WAIT0<br>1 WAIT0 active high<br>0 WAIT0 active low  |
| 7:5   | RESERVED_0       | R    | 0h    | Write 0's for future compatibility. Read returns 0                                    |
| 4     | WRITEPROTECT     | R/W  | 0h    | Controls the WP output pin level<br>1 WP output pin is high<br>0 WP output pin is low |
| 3:2   | RESERVED_2       | R    | 0h    | Write 0's for future compatibility. Read returns 0                                    |

**Table 5-1769. GPMC\_CONFIG Register Field Descriptions (continued)**

| Bit | Field                | Type | Reset | Description                                                                                                                           |
|-----|----------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------|
| 1   | LIMITEDADDRESS       | R/W  | 0h    | Limited Address device support<br>1 A26-A11 are not modified during an external memory access.<br>0 No effect                         |
| 0   | NANDFORCEPOSTEDWRITE | R/W  | 0h    | Enables the Force Posted Write feature to NAND Cmd/Add/Data location<br>1 Enables Force Posted write<br>0 Disables Force Posted write |



### 5.9.2.9 GPMC\_STATUS Register

#### 1 GPMC\_STATUS Register (Offset = 54h) [reset = 1h]

The status register provides global status bits of the GPMC .

Return to [Summary Table](#)

**Table 5-1770. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPMC0         | 4840 0054h       |

**Figure 5-587. GPMC\_STATUS Name Register**

|              |    |    |    |             |             |             |                            |
|--------------|----|----|----|-------------|-------------|-------------|----------------------------|
| 31           | 30 | 29 | 28 | 27          | 26          | 25          | 24                         |
| RESERVED_231 |    |    |    |             |             |             |                            |
| R            |    |    |    |             |             |             |                            |
| 0h           |    |    |    |             |             |             |                            |
| 23           | 22 | 21 | 20 | 19          | 18          | 17          | 16                         |
| RESERVED_231 |    |    |    |             |             |             |                            |
| R            |    |    |    |             |             |             |                            |
| 0h           |    |    |    |             |             |             |                            |
| 15           | 14 | 13 | 12 | 11          | 10          | 9           | 8                          |
| RESERVED_231 |    |    |    | WAIT3STATUS | WAIT2STATUS | WAIT1STATUS | WAIT0STATUS                |
| R            |    |    |    | R           | R           | R           | R                          |
| 0h           |    |    |    | 0h          | 0h          | 0h          | 0h                         |
| 7            | 6  | 5  | 4  | 3           | 2           | 1           | 0                          |
| RESERVED_232 |    |    |    |             |             |             | EMPTYWRITE<br>BUFFERSTATUS |
| R            |    |    |    |             |             |             | R                          |
| 0h           |    |    |    |             |             |             | 1h                         |

**Table 5-1772. GPMC\_STATUS Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                                                 |
|-------|--------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED_231 | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                          |
| 11    | WAIT3STATUS  | R    | 0h    | Is a copy of input pin WAIT3. [Reset value is WAIT3 input pin sampled at IC reset]<br><br>1      WAIT3 asserted<br>0      WAIT3 de-asserted |
| 10    | WAIT2STATUS  | R    | 0h    | Is a copy of input pin WAIT2. [Reset value is WAIT2 input pin sampled at IC reset]<br><br>1      WAIT2 asserted<br>0      WAIT2 de-asserted |
| 9     | WAIT1STATUS  | R    | 0h    | Is a copy of input pin WAIT1. [Reset value is WAIT1 input pin sampled at IC reset]<br><br>1      WAIT1 asserted<br>0      WAIT1 de-asserted |
| 8     | WAIT0STATUS  | R    | 0h    | Is a copy of input pin WAIT0. [Reset value is WAIT0 input pin sampled at IC reset]<br><br>1      WAIT0 asserted<br>0      WAIT0 de-asserted |
| 7:1   | RESERVED_232 | R    | 0h    | Write 0's for future compatibility Reads returns 0                                                                                          |

**Table 5-1772. GPMC\_STATUS Register Field Descriptions (continued)**

| Bit | Field                      | Type | Reset | Description                                                                                                     |
|-----|----------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------|
| 0   | EMPTYWRITEBUFFERS<br>TATUS | R    | 1h    | Stores the empty status of the write buffer<br>1      write Buffer is empty<br>0      write Buffer is not empty |

### 5.9.2.10 GPMC\_PREFETCH\_CONFIG1 Register

#### 1 GPMC\_PREFETCH\_CONFIG1 Register (Offset = 1E0h) [reset = 4000h]

Prefetch engine configuration 1 .

Return to [Summary Table](#)

**Table 5-1773. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPMC0         | 4840 01E0h       |

**Figure 5-588. GPMC\_PREFETCH\_CONFIG1 Name Register**

| 31                   | 30                | 29              | 28 | 27                        | 26               | 25               | 24         |
|----------------------|-------------------|-----------------|----|---------------------------|------------------|------------------|------------|
| RESERVED_22<br>1     | CYCLEOPTIMIZATION |                 |    | ENABLEOPTIM<br>IZEDACCESS | ENGINECSSELECTOR |                  |            |
| R                    | R/W               |                 |    | R/W                       | R/W              |                  |            |
| 0h                   | 0h                |                 |    | 0h                        | 0h               |                  |            |
| 23                   | 22                | 21              | 20 | 19                        | 18               | 17               | 16         |
| PFPWENROUN<br>DROBIN | RESERVED_224      |                 |    | PFPWWEIGHTEDPRIO          |                  |                  |            |
| R/W                  | R                 |                 |    | R/W                       |                  |                  |            |
| 0h                   | 0h                |                 |    | 0h                        |                  |                  |            |
| 15                   | 14                | 13              | 12 | 11                        | 10               | 9                | 8          |
| RESERVED_22<br>0     | FIFOTHRESHOLD     |                 |    |                           |                  |                  |            |
| R                    | R/W               |                 |    |                           |                  |                  |            |
| 0h                   | 40h               |                 |    |                           |                  |                  |            |
| 7                    | 6                 | 5               | 4  | 3                         | 2                | 1                | 0          |
| ENABLEENGIN<br>E     | RESERVED_22<br>3  | WAITPINSELECTOR |    | SYNCHROMO<br>DE           | DMAMODE          | RESERVED_22<br>2 | ACCESSMODE |
| R/W                  | R                 | R/W             |    | R/W                       | R/W              | R/W              | R/W        |
| 0h                   | 0h                | 0h              |    | 0h                        | 0h               | 0h               | 0h         |

**Table 5-1775. GPMC\_PREFETCH\_CONFIG1 Register Field Descriptions**

| Bit   | Field                 | Type | Reset | Description                                                                                                                                                                                                                                                                                         |
|-------|-----------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | RESERVED_221          | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                                                                                                                                  |
| 30:28 | CYCLEOPTIMIZATION     | R/W  | 0h    | Define the number of GPMC.FCLK cycles to be subtracted from RdCycleTime, WrCycleTime, AccessTime, CSRdOffTime, CSWrOffTime, ADVRdOffTime, ADVWrOffTime, OEOffTime, WEOffTime [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0x7 corresponds to 7 GPMC.FCLK cycles] |
| 27    | ENABLEOPTIMIZEDACCESS | R/W  | 0h    | Enables access cycle optimization<br>1 Access cycle optimization is enabled<br>0 Access cycle optimization is disabled                                                                                                                                                                              |
| 26:24 | ENGINECSSELECTOR      | R/W  | 0h    | Selects the CS where Prefetch Postwrite engine is active [0x0 corresponds to CS0, 0x1 corresponds to CS1, &, 0x7 corresponds to CS7]                                                                                                                                                                |
| 23    | PFPWENROUNDROBIN      | R/W  | 0h    | Enables the PFPW RoundRobin arbitration<br>1 Prefetch Postwrite engine round robin arbitration is enabled<br>0 Prefetch Postwrite engine round robin arbitration is disabled                                                                                                                        |
| 22:20 | RESERVED_224          | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                                                                                                                                  |

**Table 5-1775. GPMC\_PREFETCH\_CONFIG1 Register Field Descriptions (continued)**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                             |
|-------|------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19:16 | PFPWWEIGHTEDPRIO | R/W  | 0h    | When an arbitration occurs between a direct memory access and a PFPW engine access, the direct memory access is always serviced. If the PFPWEnRoundRobin is enabled, 0x0 means : the next access is granted to the PFPW engine, 0x1 means : the two next accesses are granted to the PFPW engine, ..., 0xF means : the 16 next accesses are granted to the PFPW engine. |
| 15    | RESERVED_220     | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                                                                                                                                                                                                      |
| 14:8  | FIFOTHRESHOLD    | R/W  | 40h   | Selects the maximum number of bytes read from the FIFO or written to the FIFO by the host on a DMA or interrupt request [0x00 corresponds to 0 byte, 0x01 corresponds to 1 byte, &, 0x40 corresponds to 64 bytes]                                                                                                                                                       |
| 7     | ENABLEENGINE     | R/W  | 0h    | Enables the Prefetch Postwrite engine<br>1 Prefetch Postwrite engine is enabled<br>0 Prefetch Postwrite engine is disabled                                                                                                                                                                                                                                              |
| 6     | RESERVED_223     | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                                                                                                                                                                                                      |
| 5:4   | WAITPINSELECTOR  | R/W  | 0h    | Select which wait pin edge detector should start the engine in synchronized mode<br>3 Selects wait3EdgeDetection<br>2 Selects wait2EdgeDetection<br>1 Selects wait1EdgeDetection<br>0 Selects wait0EdgeDetection                                                                                                                                                        |
| 3     | SYNCHROMODE      | R/W  | 0h    | Selects when the engine starts the access to CS<br>1 Engine starts the access to CS as soon as StartEngine is set AND wait to non wait edge detection on the selected wait pin<br>0 Engine starts the access to CS as soon as StartEngine is set                                                                                                                        |
| 2     | DMAMODE          | R/W  | 0h    | Selects interrupt synchronization or DMA request synchronization<br>1 DMA request synchronization is enabled. A DMA request protocol is used.<br>0 Interrupt synchronization is enabled. Only interrupt line will be activated on FIFO threshold crossing.                                                                                                              |
| 1     | RESERVED_222     | R/W  | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                                                                                                                                                                                                      |
| 0     | ACCESSMODE       | R/W  | 0h    | Selects pre-fetch read or write posting accesses<br>1 write posting mode<br>0 Pre-fetch read mode                                                                                                                                                                                                                                                                       |

### 5.9.2.11 GPMC\_PREFETCH\_CONFIG2 Register

#### 1 GPMC\_PREFETCH\_CONFIG2 Register (Offset = 1E4h) [reset = 0h]

Prefetch engine configuration 2 .

Return to [Summary Table](#)

**Table 5-1776. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPMC0         | 4840 01E4h       |

**Figure 5-589. GPMC\_PREFETCH\_CONFIG2 Name Register**

|               |    |               |    |    |    |    |    |
|---------------|----|---------------|----|----|----|----|----|
| 31            | 30 | 29            | 28 | 27 | 26 | 25 | 24 |
| RESERVED_224  |    |               |    |    |    |    |    |
| R             |    |               |    |    |    |    |    |
| 0h            |    |               |    |    |    |    |    |
| 23            | 22 | 21            | 20 | 19 | 18 | 17 | 16 |
| RESERVED_224  |    |               |    |    |    |    |    |
| R             |    |               |    |    |    |    |    |
| 0h            |    |               |    |    |    |    |    |
| 15            | 14 | 13            | 12 | 11 | 10 | 9  | 8  |
| RESERVED_224  |    | TRANSFERCOUNT |    |    |    |    |    |
| R             |    | R/W           |    |    |    |    |    |
| 0h            |    | 0h            |    |    |    |    |    |
| 7             | 6  | 5             | 4  | 3  | 2  | 1  | 0  |
| TRANSFERCOUNT |    |               |    |    |    |    |    |
| R/W           |    |               |    |    |    |    |    |
| 0h            |    |               |    |    |    |    |    |

**Table 5-1778. GPMC\_PREFETCH\_CONFIG2 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                                                        |
|-------|---------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:14 | RESERVED_224  | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                 |
| 13:0  | TRANSFERCOUNT | R/W  | 0h    | Selects the number of bytes to be read or written by the engine to the selected CS [0x0000 corresponds to 0 byte, 0x0001 corresponds to 1 byte, &, 0x2000 corresponds to 8 Kbytes] |

### 5.9.2.12 GPMC\_PREFETCH\_CONTROL Register

#### 1 GPMC\_PREFETCH\_CONTROL Register (Offset = 1ECh) [reset = 0h]

Prefetch engine control .

Return to [Summary Table](#)

**Table 5-1779. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPMC0         | 4840 01ECh       |

**Figure 5-590. GPMC\_PREFETCH\_CONTROL Name Register**

|              |    |    |    |    |    |    |             |
|--------------|----|----|----|----|----|----|-------------|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24          |
| RESERVED_225 |    |    |    |    |    |    |             |
| R            |    |    |    |    |    |    |             |
| 0h           |    |    |    |    |    |    |             |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16          |
| RESERVED_225 |    |    |    |    |    |    |             |
| R            |    |    |    |    |    |    |             |
| 0h           |    |    |    |    |    |    |             |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8           |
| RESERVED_225 |    |    |    |    |    |    |             |
| R            |    |    |    |    |    |    |             |
| 0h           |    |    |    |    |    |    |             |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0           |
| RESERVED_225 |    |    |    |    |    |    | STARTENGINE |
| R            |    |    |    |    |    |    | R/W         |
| 0h           |    |    |    |    |    |    | 0h          |

**Table 5-1781. GPMC\_PREFETCH\_CONTROL Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                                                                                                                                                                    |
|------|--------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED_225 | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                                                                             |
| 0    | STARTENGINE  | R/W  | 0h    | Resets the FIFO pointer and starts the engine<br>1 write 1 resets the FIFO pointer to 0x0 in prefetch mode and 0x40 in postwrite mode and starts the engine. Read 1: engine is running<br>0 write 0 stops the engine Read 0: engine is stopped |

### 5.9.2.13 GPMC\_PREFETCH\_STATUS Register

#### 1 GPMC\_PREFETCH\_STATUS Register (Offset = 1F0h) [reset = 0h]

Prefetch engine status .

Return to [Summary Table](#)

**Table 5-1782. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPMC0         | 4840 01F0h       |

**Figure 5-591. GPMC\_PREFETCH\_STATUS Name Register**

|              |             |    |    |    |    |    |                     |
|--------------|-------------|----|----|----|----|----|---------------------|
| 31           | 30          | 29 | 28 | 27 | 26 | 25 | 24                  |
| RESERVED_227 | FIFOPOINTER |    |    |    |    |    |                     |
| R            | R           |    |    |    |    |    |                     |
| 0h           | 0h          |    |    |    |    |    |                     |
| 23           | 22          | 21 | 20 | 19 | 18 | 17 | 16                  |
| RESERVED_228 |             |    |    |    |    |    | FIFOTHRESHOLDSTATUS |
| R            |             |    |    |    |    |    | R                   |
| 0h           |             |    |    |    |    |    | 0h                  |
| 15           | 14          | 13 | 12 | 11 | 10 | 9  | 8                   |
| RESERVED_226 | COUNTVALUE  |    |    |    |    |    |                     |
| R            | R           |    |    |    |    |    |                     |
| 0h           | 0h          |    |    |    |    |    |                     |
| 7            | 6           | 5  | 4  | 3  | 2  | 1  | 0                   |
| COUNTVALUE   |             |    |    |    |    |    |                     |
| R            |             |    |    |    |    |    |                     |
| 0h           |             |    |    |    |    |    |                     |

**Table 5-1784. GPMC\_PREFETCH\_STATUS Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                                               |
|-------|---------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | RESERVED_227        | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                                                                                                                                                        |
| 30:24 | FIFOPOINTER         | R    | 0h    | Number of available bytes to be read or number of free empty byte places to be written [0x00 corresponds to 0 byte available to be read or 0 free empty place to be written, & 0x40 corresponds to 64 bytes available to be read or 64 empty places to be written]                                                        |
| 23:17 | RESERVED_228        | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                                                                                                                                                        |
| 16    | FIFOTHRESHOLDSTATUS | R    | 0h    | Set when FIFOPointer exceeds FIFOThreshold value<br>1 FIFOPointer greater than FIFOThreshold. writing to this bit has no effect<br>0 FIFOPointer smaller or equal to FIFOThreshold. writing to this bit has no effect                                                                                                     |
| 15:14 | RESERVED_226        | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                                                                                                                                                        |
| 13:0  | COUNTVALUE          | R    | 0h    | Number of remaining bytes to be read or to be written by the engine according to the TransferCount value [0x0000 corresponds to 0 byte remaining to be read or to be written, 0x0001 corresponds to 1 byte remaining to be read or to be written, & 0x2000 corresponds to 8 Kbytes remaining to be read or to be written] |

### 5.9.2.14 GPMC\_ECC\_CONFIG Register

#### 1 GPMC\_ECC\_CONFIG Register (Offset = 1F4h) [reset = 1030h]

ECC configuration .

Return to [Summary Table](#)

**Table 5-1785. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPMC0         | 4840 01F4h       |

**Figure 5-592. GPMC\_ECC\_CONFIG Name Register**

|              |              |            |    |             |    |           |              |
|--------------|--------------|------------|----|-------------|----|-----------|--------------|
| 31           | 30           | 29         | 28 | 27          | 26 | 25        | 24           |
| RESERVED_206 |              |            |    |             |    |           |              |
| R            |              |            |    |             |    |           |              |
| 0h           |              |            |    |             |    |           |              |
| 23           | 22           | 21         | 20 | 19          | 18 | 17        | 16           |
| RESERVED_206 |              |            |    |             |    |           | ECCALGORITHM |
| R            |              |            |    |             |    |           | R/W          |
| 0h           |              |            |    |             |    |           | 0h           |
| 15           | 14           | 13         | 12 | 11          | 10 | 9         | 8            |
| RESERVED_205 |              | ECCBCHTSEL |    | ECCWRAPMODE |    |           |              |
| R            |              | R/W        |    | R/W         |    |           |              |
| 0h           |              | 1h         |    | 0h          |    |           |              |
| 7            | 6            | 5          | 4  | 3           | 2  | 1         | 0            |
| ECC16B       | ECCTOPSECTOR |            |    | ECCCS       |    | ECCENABLE |              |
| R/W          | R/W          |            |    | R/W         |    | R/W       |              |
| 0h           | 3h           |            |    | 0h          |    | 0h        |              |

**Table 5-1787. GPMC\_ECC\_CONFIG Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                                                                                                       |
|-------|--------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | RESERVED_206 | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                                |
| 16    | ECCALGORITHM | R/W  | 0h    | ECC algorithm used<br>0x0: Hamming code<br>0x1: BCH code                                                                                                                                          |
| 15:14 | RESERVED_205 | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                                |
| 13:12 | ECCBCHTSEL   | R/W  | 1h    | Error correction capability used for BCH<br>0x0: up to 4 bits error correction [t = 4]<br>0x1: up to 8 bits error correction [t=8]<br>0x2: up to 16 bits error correction [t=16]<br>0x3: reserved |
| 11:8  | ECCWRAPMODE  | R/W  | 0h    | Spare area organization definition for the BCH algorithm. See the BCH syndrome/parity calculator module functional specification for more details                                                 |
| 7     | ECC16B       | R/W  | 0h    | Selects an ECC calculated on 16 columns<br>1 ECC calculated on 16 columns<br>0 ECC calculated on 8 columns                                                                                        |



**Table 5-1787. GPMC\_ECC\_CONFIG Register Field Descriptions (continued)**

| Bit | Field        | Type | Reset | Description                                                                                                                                                                                                                              |
|-----|--------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6:4 | ECCTOPSECTOR | R/W  | 3h    | Number of sectors to process with the BCH algorithm<br>0x0: 1 sector [512kB page]<br>0x1: 2 sectors<br>...<br>0x3: 4 sectors [2kB page]<br>...<br>0x7: 8 sectors [4kB page]                                                              |
| 3:1 | ECCCS        | R/W  | 0h    | Selects the CS where ECC is computed<br><br>7      Chip select 7<br>6      Chip select 6<br>5      Chip select 5<br>4      Chip select 4<br>3      Chip select 3<br>2      Chip select 2<br>1      Chip select 1<br>0      Chip select 0 |
| 0   | ECCENABLE    | R/W  | 0h    | Enables the ECC feature<br><br>1      ECC enabled<br>0      ECC disabled                                                                                                                                                                 |

### 5.9.2.15 GPMC\_ECC\_CONTROL Register

#### 1 GPMC\_ECC\_CONTROL Register (Offset = 1F8h) [reset = 0h]

ECC control .

Return to [Summary Table](#)

**Table 5-1788. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPMC0         | 4840 01F8h       |

**Figure 5-593. GPMC\_ECC\_CONTROL Name Register**

|              |    |    |    |            |    |    |          |
|--------------|----|----|----|------------|----|----|----------|
| 31           | 30 | 29 | 28 | 27         | 26 | 25 | 24       |
| RESERVED_207 |    |    |    |            |    |    |          |
| R            |    |    |    |            |    |    |          |
| 0h           |    |    |    |            |    |    |          |
| 23           | 22 | 21 | 20 | 19         | 18 | 17 | 16       |
| RESERVED_207 |    |    |    |            |    |    |          |
| R            |    |    |    |            |    |    |          |
| 0h           |    |    |    |            |    |    |          |
| 15           | 14 | 13 | 12 | 11         | 10 | 9  | 8        |
| RESERVED_207 |    |    |    |            |    |    | ECCCLEAR |
| R            |    |    |    |            |    |    | R/W1TC   |
| 0h           |    |    |    |            |    |    | 0h       |
| 7            | 6  | 5  | 4  | 3          | 2  | 1  | 0        |
| RESERVED_208 |    |    |    | ECCPOINTER |    |    |          |
| R            |    |    |    | R/W        |    |    |          |
| 0h           |    |    |    | 0h         |    |    |          |

**Table 5-1790. GPMC\_ECC\_CONTROL Register Field Descriptions**

| Bit  | Field        | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|--------------|--------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:9 | RESERVED_207 | R      | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 8    | ECCCLEAR     | R/W1TC | 0h    | Clear all ECC result registers [Reads returns 0 - Writes 1 to this field clear all ECC result registers - Writes 0 are ignored]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 7:4  | RESERVED_208 | R      | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 3:0  | ECCPOINTER   | R/W    | 0h    | Selects ECC result register [Reads to this field give the dynamic position of the ECC pointer - Writes to this field select the ECC result register where the first ECC computation will be stored]; Other enums: Writing other values disables the ECC engine [ECCEnable bit of GPMC_ECC_CONFIG set to 0]<br>9 ECC result register 9 is selected<br>8 ECC result register 8 is selected<br>7 ECC result register 7 is selected<br>6 ECC result register 6 is selected<br>5 ECC result register 5 is selected<br>4 ECC result register 4 is selected<br>3 ECC result register 3 is selected<br>2 ECC result register 2 is selected<br>1 ECC result register 1 is selected<br>0 writing 0000 disables the ECC engine (ECCEnable bit of GPMC_ECC_CONFIG set to 0) |

### 5.9.2.16 GPMC\_ECC\_SIZE\_CONFIG Register

#### 1 GPMC\_ECC\_SIZE\_CONFIG Register (Offset = 1FCh) [reset = FFFF000h]

ECC size .

Return to [Summary Table](#)

**Table 5-1791. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPMC0         | 4840 01FCh       |

**Figure 5-594. GPMC\_ECC\_SIZE\_CONFIG Name Register**

|                    |                    |                    |                    |                    |                    |                    |                    |
|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| 31                 | 30                 | 29                 | 28                 | 27                 | 26                 | 25                 | 24                 |
| RESERVED_210       |                    | ECCSIZE1           |                    |                    |                    |                    |                    |
| R/W                |                    | R/W                |                    |                    |                    |                    |                    |
| 3h                 |                    | FFh                |                    |                    |                    |                    |                    |
| 23                 | 22                 | 21                 | 20                 | 19                 | 18                 | 17                 | 16                 |
| ECCSIZE1           |                    | RESERVED_211       |                    | ECCSIZE0           |                    |                    |                    |
| R/W                |                    | R/W                |                    | R/W                |                    |                    |                    |
| FFh                |                    | 3h                 |                    | FFh                |                    |                    |                    |
| 15                 | 14                 | 13                 | 12                 | 11                 | 10                 | 9                  | 8                  |
| ECCSIZE0           |                    |                    |                    | RESERVED_209       |                    |                    | ECC9RESULTS<br>IZE |
| R/W                |                    |                    |                    | R                  |                    |                    | R/W                |
| FFh                |                    |                    |                    | 0h                 |                    |                    | 0h                 |
| 7                  | 6                  | 5                  | 4                  | 3                  | 2                  | 1                  | 0                  |
| ECC8RESULTS<br>IZE | ECC7RESULTS<br>IZE | ECC6RESULTS<br>IZE | ECC5RESULTS<br>IZE | ECC4RESULTS<br>IZE | ECC3RESULTS<br>IZE | ECC2RESULTS<br>IZE | ECC1RESULTS<br>IZE |
| R/W                | R/W                | R/W                | R/W                | R/W                | R/W                | R/W                | R/W                |
| 0h                 | 0h                 | 0h                 | 0h                 | 0h                 | 0h                 | 0h                 | 0h                 |

**Table 5-1793. GPMC\_ECC\_SIZE\_CONFIG Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                               |
|-------|--------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | RESERVED_210       | R/W  | 3h    | Write 0's for future compatibility. Read returns 3                                                                                                                        |
| 29:22 | ECCSIZE1           | R/W  | FFh   | Defines ECC size 1 [0x00 corresponds to 2 Bytes, 0x01 corresponds to 4 Bytes, 0x02 corresponds to 6 Bytes, 0x03 corresponds to 8 Bytes, &, 0xFF corresponds to 512 Bytes] |
| 21:20 | RESERVED_211       | R/W  | 3h    | Write 0's for future compatibility. Read returns 3                                                                                                                        |
| 19:12 | ECCSIZE0           | R/W  | FFh   | Defines ECC size 0 [0x00 corresponds to 2 Bytes, 0x01 corresponds to 4 Bytes, 0x02 corresponds to 6 Bytes, 0x03 corresponds to 8 Bytes, &, 0xFF corresponds to 512 Bytes] |
| 11:9  | RESERVED_209       | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                        |
| 8     | ECC9RESULTS<br>IZE | R/W  | 0h    | Selects ECC size for ECC 9 result register<br>1 ECCSize1 is selected<br>0 ECCSize0 is selected                                                                            |
| 7     | ECC8RESULTS<br>IZE | R/W  | 0h    | Selects ECC size for ECC 8 result register<br>1 ECCSize1 is selected<br>0 ECCSize0 is selected                                                                            |
| 6     | ECC7RESULTS<br>IZE | R/W  | 0h    | Selects ECC size for ECC 7 result register<br>1 ECCSize1 is selected<br>0 ECCSize0 is selected                                                                            |

**Table 5-1793. GPMC\_ECC\_SIZE\_CONFIG Register Field Descriptions (continued)**

| Bit | Field         | Type | Reset | Description                                                                                              |
|-----|---------------|------|-------|----------------------------------------------------------------------------------------------------------|
| 5   | ECC6RESULTSIZ | R/W  | 0h    | Selects ECC size for ECC 6 result register<br>1      ECCSize1 is selected<br>0      ECCSize0 is selected |
| 4   | ECC5RESULTSIZ | R/W  | 0h    | Selects ECC size for ECC 5 result register<br>1      ECCSize1 is selected<br>0      ECCSize0 is selected |
| 3   | ECC4RESULTSIZ | R/W  | 0h    | Selects ECC size for ECC 4 result register<br>1      ECCSize1 is selected<br>0      ECCSize0 is selected |
| 2   | ECC3RESULTSIZ | R/W  | 0h    | Selects ECC size for ECC 3 result register<br>1      ECCSize1 is selected<br>0      ECCSize0 is selected |
| 1   | ECC2RESULTSIZ | R/W  | 0h    | Selects ECC size for ECC 2 result register<br>1      ECCSize1 is selected<br>0      ECCSize0 is selected |
| 0   | ECC1RESULTSIZ | R/W  | 0h    | Selects ECC size for ECC 1 result register<br>1      ECCSize1 is selected<br>0      ECCSize0 is selected |

### 5.9.2.17 GPMC\_ECC\_RESULT\_J Register

#### 1 GPMC\_ECC\_RESULT\_J Register (Offset = 200h) [reset = 0h]

ECC result register .

Return to [Summary Table](#)

Offset = Base + (j \* 4h); where j = 0 to 8d

**Table 5-1794. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| GPMC0         | 4840 0200h + formula |

**Figure 5-595. GPMC\_ECC\_RESULT\_J Name Register**

| 31           | 30   | 29   | 28   | 27     | 26     | 25    | 24    |
|--------------|------|------|------|--------|--------|-------|-------|
| RESERVED_188 |      |      |      | P2048O | P1024O | P512O | P256O |
| R            |      |      |      | R      | R      | R     | R     |
| 0h           |      |      |      | 0h     | 0h     | 0h    | 0h    |
| 23           | 22   | 21   | 20   | 19     | 18     | 17    | 16    |
| P128O        | P64O | P32O | P16O | P8O    | P4O    | P2O   | P1O   |
| R            | R    | R    | R    | R      | R      | R     | R     |
| 0h           | 0h   | 0h   | 0h   | 0h     | 0h     | 0h    | 0h    |
| 15           | 14   | 13   | 12   | 11     | 10     | 9     | 8     |
| RESERVED_187 |      |      |      | P2048E | P1024E | P512E | P256E |
| R            |      |      |      | R      | R      | R     | R     |
| 0h           |      |      |      | 0h     | 0h     | 0h    | 0h    |
| 7            | 6    | 5    | 4    | 3      | 2      | 1     | 0     |
| P128E        | P64E | P32E | P16E | P8E    | P4E    | P2E   | P1E   |
| R            | R    | R    | R    | R      | R      | R     | R     |
| 0h           | 0h   | 0h   | 0h   | 0h     | 0h     | 0h    | 0h    |

**Table 5-1796. GPMC\_ECC\_RESULT\_J Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                         |
|-------|--------------|------|-------|---------------------------------------------------------------------|
| 31:28 | RESERVED_188 | R    | 0h    | Write 0's for future compatibility. Read returns 0                  |
| 27    | P2048O       | R    | 0h    | Odd Row Parity bit<br>2048 only used for ECC computed on 512 Bytes  |
| 26    | P1024O       | R    | 0h    | Odd Row Parity bit 1024                                             |
| 25    | P512O        | R    | 0h    | Odd Row Parity bit 512                                              |
| 24    | P256O        | R    | 0h    | Odd Row Parity bit 256                                              |
| 23    | P128O        | R    | 0h    | Odd Row Parity bit 128                                              |
| 22    | P64O         | R    | 0h    | Odd Row Parity bit 64                                               |
| 21    | P32O         | R    | 0h    | Odd Row Parity bit 32                                               |
| 20    | P16O         | R    | 0h    | Odd Row Parity bit 16                                               |
| 19    | P8O          | R    | 0h    | Odd Row Parity bit 8                                                |
| 18    | P4O          | R    | 0h    | Odd Column Parity bit 4                                             |
| 17    | P2O          | R    | 0h    | Odd Column Parity bit 2                                             |
| 16    | P1O          | R    | 0h    | Odd Column Parity bit 1                                             |
| 15:12 | RESERVED_187 | R    | 0h    | Write 0's for future compatibility. Read returns 0                  |
| 11    | P2048E       | R    | 0h    | Even Row Parity bit<br>2048 only used for ECC computed on 512 Bytes |

**Table 5-1796. GPMC\_ECC\_RESULT\_J Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description              |
|-----|--------|------|-------|--------------------------|
| 10  | P1024E | R    | 0h    | Even Row Parity bit 1024 |
| 9   | P512E  | R    | 0h    | Even Row Parity bit 512  |
| 8   | P256E  | R    | 0h    | Even Row Parity bit 256  |
| 7   | P128E  | R    | 0h    | Even Row Parity bit 128  |
| 6   | P64E   | R    | 0h    | Even Row Parity bit 64   |
| 5   | P32E   | R    | 0h    | Even Row Parity bit 32   |
| 4   | P16E   | R    | 0h    | Even Row Parity bit 16   |
| 3   | P8E    | R    | 0h    | Even Row Parity bit 8    |
| 2   | P4E    | R    | 0h    | Even Column Parity bit 4 |
| 1   | P2E    | R    | 0h    | Even Column Parity bit 2 |
| 0   | P1E    | R    | 0h    | Even Column Parity bit 1 |

### 5.9.2.18 GPMC\_BCH\_SWDATA Register

#### 1 GPMC\_BCH\_SWDATA Register (Offset = 2D0h) [reset = 0h]

This register is used to directly pass data to the BCH ECC calculator without accessing the actual NAND flash interface.

Return to [Summary Table](#)

**Table 5-1797. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| GPMC0         | 4840 02D0h       |

**Figure 5-596. GPMC\_BCH\_SWDATA Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| BCH_DATA |    |    |    |    |    |    |    |
| W        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| BCH_DATA |    |    |    |    |    |    |    |
| W        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-1799. GPMC\_BCH\_SWDATA Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                         |
|-------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED | R    | 0h    | Reserved                                                                                                                                            |
| 15:0  | BCH_DATA | W    | 0h    | Data to be included in the BCH calculation. Only bits 0 to 7 are taken into account if the calculator is configured to use 8 bits data [ECC16B = 0] |

### 5.9.2.19 GPMC\_CONFIG1 Register

#### 1 GPMC\_CONFIG1 Register (Offset = 60h) [reset = 0h]

The configuration 1 register sets signal control parameters per chip select

Return to [Summary Table](#)

Offset = Base + (j \* 30h); where j = 0 to 3d

**Table 5-1800. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| GPMC0         | 4840 0060h + formula |

**Figure 5-597. GPMC\_CONFIG1 Name Register**

| 31                               | 30                 | 29                  | 28                        | 27                 | 26                | 25                               | 24 |
|----------------------------------|--------------------|---------------------|---------------------------|--------------------|-------------------|----------------------------------|----|
| WRAPBURST                        | READMULTIPLE       | READTYPE            | WRITEMULTIPLE             | WRITETYPE          | CLKACTIVATIONTIME | ATTACHEDDE<br>VICEPAGELEN<br>GTH |    |
| R/W                              | R/W                | R/W                 | R/W                       | R/W                | R/W               | R/W                              |    |
| 0h                               | 0h                 | 0h                  | 0h                        | 0h                 | 0h                | 0h                               | 0h |
| 23                               | 22                 | 21                  | 20                        | 19                 | 18                | 17                               | 16 |
| ATTACHEDDE<br>VICEPAGELEN<br>GTH | WAITREADMONITORING | WAITWRITEMONITORING | RESERVED_9                | WAITMONITORINGTIME |                   | WAITPINSELECT                    |    |
| R/W                              | R/W                | R/W                 | R                         | R/W                |                   | R/W                              |    |
| 0h                               | 0h                 | 0h                  | 0h                        | 0h                 |                   | 0h                               | 0h |
| 15                               | 14                 | 13                  | 12                        | 11                 | 10                | 9                                | 8  |
| RESERVED_11                      |                    | DEVICESIZE          |                           | DEVICETYPE         |                   | MUXADDDATA                       |    |
| R                                |                    | R/W                 |                           | R/W                |                   | R/W                              |    |
| 0h                               |                    | 0h                  |                           | 0h                 |                   | 0h                               | 0h |
| 7                                | 6                  | 5                   | 4                         | 3                  | 2                 | 1                                | 0  |
| RESERVED_12                      |                    |                     | TIMEPARAGRAPH<br>NULARITY | RESERVED_10        |                   | GPMCFCLKDIVIDER                  |    |
| R                                |                    |                     | R/W                       | R                  |                   | R/W                              |    |
| 0h                               |                    |                     | 0h                        | 0h                 |                   | 0h                               | 0h |

**Table 5-1802. GPMC\_CONFIG1 Register Field Descriptions**

| Bit | Field         | Type | Reset | Description                                                                                                                                                                                       |
|-----|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31  | WRAPBURST     | R/W  | 0h    | Enables the wrapping burst capability. Must be set if the attached device is configured in wrapping burst<br>1 Synchronous wrapping burst supported<br>0 Synchronous wrapping burst not supported |
| 30  | READMULTIPLE  | R/W  | 0h    | Selects the read single or multiple access<br>1 multiple access (burst if synchronous, page if asynchronous)<br>0 single access                                                                   |
| 29  | READTYPE      | R/W  | 0h    | Selects the read mode operation<br>1 Read Synchronous<br>0 Read Asynchronous                                                                                                                      |
| 28  | WRITEMULTIPLE | R/W  | 0h    | Selects the write single or multiple access<br>1 multiple access (burst if synchronous, considered as single if asynchronous)<br>0 single access                                                  |



**Table 5-1802. GPMC\_CONFIG1 Register Field Descriptions (continued)**

| Bit   | Field                    | Type | Reset | Description                                                                                                                                                                                                                                                             |
|-------|--------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 27    | WRITETYPE                | R/W  | 0h    | Selects the write mode operation<br>1 write Synchronous<br>0 write Asynchronous                                                                                                                                                                                         |
| 26:25 | CLKACTIVATIONTIME        | R/W  | 0h    | Output GPMC.CLK activation time<br>3 not defined<br>2 First rising edge of GPMC.CLK two GPMC.FCLK cycles after Start Access Time<br>1 First rising edge of GPMC.CLK one GPMC.FCLK cycle after Start Access Time<br>0 First rising edge of GPMC.CLK at Start Access Time |
| 24:23 | ATTACHEDDEVICEPAGELENGTH | R/W  | 0h    | Specifies the attached device page [burst] length<br>3 32 words<br>2 16 words<br>1 8 words<br>0 4 words                                                                                                                                                                 |
| 22    | WAITREADMONITORING       | R/W  | 0h    | Selects the Wait monitoring configuration for Read accesses [Reset value is BOOTWAITEN input pin sampled at IC reset]<br>1 wait pin is monitored for read accesses<br>0 wait pin is not monitored for read accesses                                                     |
| 21    | WAITWRITEMONITORING      | R/W  | 0h    | Selects the Wait monitoring configuration for Write accesses<br>1 wait pin is monitored for write accesses<br>0 wait pin is not monitored for write accesses                                                                                                            |
| 20    | RESERVED_9               | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                                                                                                      |
| 19:18 | WAITMONITORINGTIME       | R/W  | 0h    | Selects input pin Wait monitoring time<br>3 not defined<br>2 wait pin is monitored two GPMC.CLK cycle before valid data<br>1 wait pin is monitored one GPMC.CLK cycle before valid data<br>0 wait pin is monitored with valid data                                      |
| 17:16 | WAITPINSELECT            | R/W  | 0h    | Selects the input WAIT pin for this chip select [Reset value is BOOTWAITSELECT input pin sampled at IC reset for CS0 and 0 for CS1-7]<br>3 wait input pin is WAIT3<br>2 wait input pin is WAIT2<br>1 wait input pin is WAIT1<br>0 wait input pin is WAIT0               |
| 15:14 | RESERVED_11              | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                                                                                                      |
| 13:12 | DEVICESTYPE              | R/W  | 0h    | Selects the device size attached [Reset value is BOOTDEVICESTYPE input pin sampled at IC reset for CS0 and 01 for CS1-7]<br>3 reserved<br>2 32 bit<br>1 16 bit<br>0 8 bit                                                                                               |
| 11:10 | DEVICETYPE               | R/W  | 0h    | Selects the attached device type<br>3 reserved<br>2 NAND Flash stream mode<br>1 reserved<br>0 NOR Flash, pSRAM, asynchronous devices                                                                                                                                    |

**Table 5-1802. GPMC\_CONFIG1 Register Field Descriptions (continued)**

| Bit | Field               | Type | Reset | Description                                                                                                                                                                                                                                                                                               |
|-----|---------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9:8 | MUXADDDATA          | R/W  | 0h    | <p>Enables the Address and data multiplexed protocol [Reset value is CS0MUXDEVICE input pin sampled at IC reset for CS0 and 0 for CS1-7]</p> <p>3      Reserved<br/>2      Address and data multiplexed attached device<br/>1      AAD-Mux protocol device<br/>0      Non Multiplexed attached device</p> |
| 7:5 | RESERVED_12         | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                                                                                                                                        |
| 4   | TIMEPARAGRANULARITY | R/W  | 0h    | <p>Signals timing latencies scalar factor [Rd/WRCycleTime, AccessTime, PageBurstAccessTime, CSOnTime, CSRd/WrOffTime, ADVOnTime, ADVRd/WrOffTime, OEOnTime, OEOffTime, WEOnTime, WEOffTime, Cycle2CycleDelay, BusTurnAround, TimeOutStartValue]</p> <p>1      x2 latencies<br/>0      x1 latencies</p>    |
| 3:2 | RESERVED_10         | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                                                                                                                                        |
| 1:0 | GPMC_FCLKDIVIDER    | R/W  | 0h    | <p>Divides the GPMC.FCLK clock</p> <p>3      GPMC.CLK frequency = GPMC.FCLK frequency / 4<br/>2      GPMC.CLK frequency = GPMC.FCLK frequency / 3<br/>1      GPMC.CLK frequency = GPMC.FCLK frequency / 2<br/>0      GPMC.CLK frequency = GPMC.FCLK frequency</p>                                         |

### 5.9.2.20 GPMC\_CONFIG2 Register

#### 1 GPMC\_CONFIG2 Register (Offset = 64h) [reset = 101001h]

Chip-select signal timing parameter configuration

Return to [Summary Table](#)

Offset = Base + (j \* 30h); where j = 0 to 3d

**Table 5-1803. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| GPMC0         | 4840 0064h + formula |

**Figure 5-598. GPMC\_CONFIG2 Name Register**

|              |             |    |    |             |    |    |    |
|--------------|-------------|----|----|-------------|----|----|----|
| 31           | 30          | 29 | 28 | 27          | 26 | 25 | 24 |
| RESERVED_43  |             |    |    |             |    |    |    |
| R            |             |    |    |             |    |    |    |
| 0h           |             |    |    |             |    |    |    |
| 23           | 22          | 21 | 20 | 19          | 18 | 17 | 16 |
| RESERVED_43  |             |    |    | CSWROFFTIME |    |    |    |
| R            |             |    |    | R/W         |    |    |    |
| 0h           |             |    |    | 10h         |    |    |    |
| 15           | 14          | 13 | 12 | 11          | 10 | 9  | 8  |
| RESERVED_45  |             |    |    | CSRDOFFTIME |    |    |    |
| R            |             |    |    | R/W         |    |    |    |
| 0h           |             |    |    | 10h         |    |    |    |
| 7            | 6           | 5  | 4  | 3           | 2  | 1  | 0  |
| CSEXTRADelay | RESERVED_44 |    |    | CSONTIME    |    |    |    |
| R/W          | R           |    |    | R/W         |    |    |    |
| 0h           | 0h          |    |    | 1h          |    |    |    |

**Table 5-1805. GPMC\_CONFIG2 Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                                                                                                  |
|-------|--------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:21 | RESERVED_43  | R    | 0h    | Write 0's for future compatibility<br>Reads returns 0                                                                                                                                        |
| 20:16 | CSWROFFTIME  | R/W  | 10h   | CS# de-assertion time from start cycle time for write accesses<br>[0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] |
| 15:13 | RESERVED_45  | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                           |
| 12:8  | CSRDOFFTIME  | R/W  | 10h   | CS# de-assertion time from start cycle time for read accesses<br>[0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles]  |
| 7     | CSEXTRADelay | R/W  | 0h    | CS# Add Extra Half GPMC.FCLK cycle<br>1 CS# Timing control signal is delayed of half GPMC.FCLK clock cycle<br>0 CS# Timing control signal is not delayed                                     |
| 6:4   | RESERVED_44  | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                           |
| 3:0   | CSONTIME     | R/W  | 1h    | CS# assertion time from start cycle time [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles]                             |

### 5.9.2.21 GPMC\_CONFIG3 Register

#### 1 GPMC\_CONFIG3 Register (Offset = 68h) [reset = 22060514h]

ADV# signal timing parameter configuration

Return to [Summary Table](#)

Offset = Base + (j \* 30h); where j = 0 to 3d

**Table 5-1806. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| GPMC0         | 4840 0068h + formula |

**Figure 5-599. GPMC\_CONFIG3 Name Register**

|                   |                    |    |              |            |                    |    |    |
|-------------------|--------------------|----|--------------|------------|--------------------|----|----|
| 31                | 30                 | 29 | 28           | 27         | 26                 | 25 | 24 |
| RESERVED_1        | ADVAADMUXWROFFTIME |    |              | RESERVED_0 | ADVAADMUXRDOFFTIME |    |    |
| R                 | R/W                |    |              | R          | R/W                |    |    |
| 0h                | 2h                 |    |              | 0h         | 2h                 |    |    |
| 23                | 22                 | 21 | 20           | 19         | 18                 | 17 | 16 |
| RESERVED_68       |                    |    | ADVWROFFTIME |            |                    |    |    |
| R                 |                    |    | R/W          |            |                    |    |    |
| 0h                |                    |    | 6h           |            |                    |    |    |
| 15                | 14                 | 13 | 12           | 11         | 10                 | 9  | 8  |
| RESERVED_69       |                    |    | ADVRDOFFTIME |            |                    |    |    |
| R                 |                    |    | R/W          |            |                    |    |    |
| 0h                |                    |    | 5h           |            |                    |    |    |
| 7                 | 6                  | 5  | 4            | 3          | 2                  | 1  | 0  |
| ADVEXTRADE<br>LAY | ADVAADMUXONTIME    |    |              | ADVONTIME  |                    |    |    |
| R/W               | R/W                |    |              | R/W        |                    |    |    |
| 0h                | 1h                 |    |              | 4h         |                    |    |    |

**Table 5-1808. GPMC\_CONFIG3 Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description                                                                                                                                                                                |
|-------|--------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | RESERVED_1         | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                         |
| 30:28 | ADVAADMUXWROFFTIME | R/W  | 2h    | ADV# de-assertion for first address phase when using the AAD-Mux protocol                                                                                                                  |
| 27    | RESERVED_0         | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                         |
| 26:24 | ADVAADMUXRDOFFTIME | R/W  | 2h    | ADV# assertion for first address phase when using the AAD-Mux protocol                                                                                                                     |
| 23:21 | RESERVED_68        | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                         |
| 20:16 | ADVWROFFTIME       | R/W  | 6h    | ADV# de-assertion time from start cycle time for write accesses [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] |
| 15:13 | RESERVED_69        | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                         |
| 12:8  | ADVRDOFFTIME       | R/W  | 5h    | ADV# de-assertion time from start cycle time for read accesses [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles]  |
| 7     | ADVEXTRADELAY      | R/W  | 0h    | ADV# Add Extra Half GPMC.FCLK cycle<br>1 ADV# Timing control signal is delayed of half GPMC.FCLK clock cycle<br>0 ADV# Timing control signal is not delayed                                |

**Table 5-1808. GPMC\_CONFIG3 Register Field Descriptions (continued)**

| Bit | Field           | Type | Reset | Description                                                                                                                                                       |
|-----|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6:4 | ADVAADMUXONTIME | R/W  | 1h    | ADV# assertion for first address phase when using the AAD-Mux protocol                                                                                            |
| 3:0 | ADVONTIME       | R/W  | 4h    | ADV# assertion time from start cycle time [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles] |

### 5.9.2.22 GPMC\_CONFIG4 Register

#### 1 GPMC\_CONFIG4 Register (Offset = 6Ch) [reset = 10057016h]

WE# and OE# signals timing parameter configuration

Return to [Summary Table](#)

Offset = Base + (j \* 30h); where j = 0 to 3d

**Table 5-1809. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| GPMC0         | 4840 006Ch + formula |

**Figure 5-600. GPMC\_CONFIG4 Name Register**

| 31              | 30             | 29 | 28 | 27        | 26       | 25 | 24 |
|-----------------|----------------|----|----|-----------|----------|----|----|
| RESERVED        |                |    |    | WEOFFTIME |          |    |    |
| R               |                |    |    | R/W       |          |    |    |
| 0h              |                |    |    | 10h       |          |    |    |
| 23              | 22             | 21 | 20 | 19        | 18       | 17 | 16 |
| WEEXTRADELAY    | RESERVED_92    |    |    |           | WEONTIME |    |    |
| R/W             | R              |    |    |           | R/W      |    |    |
| 0h              | 0h             |    |    |           | 5h       |    |    |
| 15              | 14             | 13 | 12 | 11        | 10       | 9  | 8  |
| OEAADMUXOFFTIME |                |    |    | OEOFFTIME |          |    |    |
| R/W             |                |    |    | R/W       |          |    |    |
| 3h              |                |    |    | 10h       |          |    |    |
| 7               | 6              | 5  | 4  | 3         | 2        | 1  | 0  |
| OEEXTRADELAY    | OEAADMUXONTIME |    |    |           | OEONTIME |    |    |
| R/W             | R/W            |    |    |           | R/W      |    |    |
| 0h              | 1h             |    |    |           | 6h       |    |    |

**Table 5-1811. GPMC\_CONFIG4 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                            |
|-------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED        | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                     |
| 28:24 | WEOFFTIME       | R/W  | 10h   | WE# de-assertion time from start cycle time [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] |
| 23    | WEEXTRADELAY    | R/W  | 0h    | WE# Add Extra Half GPMC.FCLK cycle<br>1 WE# Timing control signal is delayed of half GPMC.FCLK clock cycle<br>0 WE# Timing control signal is not delayed               |
| 22:20 | RESERVED_92     | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                     |
| 19:16 | WEONTIME        | R/W  | 5h    | WE# assertion time from start cycle time [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles]       |
| 15:13 | OEAADMUXOFFTIME | R/W  | 3h    | OE# de-assertion time for the first address phase in an AAD-Mux access                                                                                                 |
| 12:8  | OEOFFTIME       | R/W  | 10h   | OE# de-assertion time from start cycle time [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] |

**Table 5-1811. GPMC\_CONFIG4 Register Field Descriptions (continued)**

| Bit | Field          | Type | Reset | Description                                                                                                                                                      |
|-----|----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | OEEXTRADELAY   | R/W  | 0h    | OE# Add Extra Half GPMC.FCLK cycle<br>1 OE# Timing control signal is delayed of half GPMC.FCLK clock cycle<br>0 OE# Timing control signal is not delayed         |
| 6:4 | OEAADMUXONTIME | R/W  | 1h    | OE# assertion time for the first address phase in an AAD-Mux access                                                                                              |
| 3:0 | OEONTIME       | R/W  | 6h    | OE# assertion time from start cycle time [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles] |

### 5.9.2.23 GPMC\_CONFIG5 Register

#### 1 GPMC\_CONFIG5 Register (Offset = 70h) [reset = 10F1111h]

RdAccessTime and CycleTime timing parameters configuration

Return to [Summary Table](#)

Offset = Base + (j \* 30h); where j = 0 to 3d

**Table 5-1812. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| GPMC0         | 4840 0070h + formula |

**Figure 5-601. GPMC\_CONFIG5 Name Register**

|              |    |    |    |                     |    |    |    |
|--------------|----|----|----|---------------------|----|----|----|
| 31           | 30 | 29 | 28 | 27                  | 26 | 25 | 24 |
| RESERVED_124 |    |    |    | PAGEBURSTACCESSTIME |    |    |    |
| R            |    |    |    | R/W                 |    |    |    |
| 0h           |    |    |    | 1h                  |    |    |    |
| 23           | 22 | 21 | 20 | 19                  | 18 | 17 | 16 |
| RESERVED_125 |    |    |    | RDACCESSTIME        |    |    |    |
| R            |    |    |    | R/W                 |    |    |    |
| 0h           |    |    |    | Fh                  |    |    |    |
| 15           | 14 | 13 | 12 | 11                  | 10 | 9  | 8  |
| RESERVED_126 |    |    |    | WRCYCLETIME         |    |    |    |
| R            |    |    |    | R/W                 |    |    |    |
| 0h           |    |    |    | 11h                 |    |    |    |
| 7            | 6  | 5  | 4  | 3                   | 2  | 1  | 0  |
| RESERVED_123 |    |    |    | RDCYCLETIME         |    |    |    |
| R            |    |    |    | R/W                 |    |    |    |
| 0h           |    |    |    | 11h                 |    |    |    |

**Table 5-1814. GPMC\_CONFIG5 Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description                                                                                                                                                                    |
|-------|---------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28 | RESERVED_124        | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                             |
| 27:24 | PAGEBURSTACCESSTIME | R/W  | 1h    | Delay between successive words in a multiple access [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles]    |
| 23:21 | RESERVED_125        | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                             |
| 20:16 | RDACCESSTIME        | R/W  | Fh    | Delay between start cycle time and first data valid [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] |
| 15:13 | RESERVED_126        | R    | 0h    | Write 0's for future compatibility<br>Reads returns 0                                                                                                                          |
| 12:8  | WRCYCLETIME         | R/W  | 11h   | Total write cycle time [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles]                              |
| 7:5   | RESERVED_123        | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                             |
| 4:0   | RDCYCLETIME         | R/W  | 11h   | Total read cycle time [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles]                               |



### 5.9.2.24 GPMC\_CONFIG6 Register

#### 1 GPMC\_CONFIG6 Register (Offset = 74h) [reset = 8F070000h]

WrAccessTime, WrDataOnAdmxBus, Cycle2Cycle and BusTurnAround parameters configuration

Return to [Summary Table](#)

Offset = Base + (j \* 30h); where j = 0 to 3d

**Table 5-1815. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| GPMC0         | 4840 0074h + formula |

**Figure 5-602. GPMC\_CONFIG6 Name Register**

|                         |                         |              |              |                  |    |    |    |
|-------------------------|-------------------------|--------------|--------------|------------------|----|----|----|
| 31                      | 30                      | 29           | 28           | 27               | 26 | 25 | 24 |
| RESERVED                | RESERVED_0              |              | WRACCESSTIME |                  |    |    |    |
| R/W                     | R                       |              | R/W          |                  |    |    |    |
| 1h                      | 0h                      |              | Fh           |                  |    |    |    |
| 23                      | 22                      | 21           | 20           | 19               | 18 | 17 | 16 |
| RESERVED_155            |                         |              |              | WRDATAONADMUXBUS |    |    |    |
| R                       |                         |              |              | R/W              |    |    |    |
| 0h                      |                         |              |              | 7h               |    |    |    |
| 15                      | 14                      | 13           | 12           | 11               | 10 | 9  | 8  |
| RESERVED_1              |                         |              |              | CYCLE2CYCLEDELAY |    |    |    |
| R                       |                         |              |              | R/W              |    |    |    |
| 0h                      |                         |              |              | 0h               |    |    |    |
| 7                       | 6                       | 5            | 4            | 3                | 2  | 1  | 0  |
| CYCLE2CYCLE<br>SAMECSEN | CYCLE2CYCLE<br>DIFFCSEN | RESERVED_156 |              | BUSTURNAROUND    |    |    |    |
| R/W                     | R/W                     | R            |              | R/W              |    |    |    |
| 0h                      | 0h                      | 0h           |              | 0h               |    |    |    |

**Table 5-1817. GPMC\_CONFIG6 Register Field Descriptions**

| Bit   | Field                   | Type | Reset | Description                                                                                                                                                                                                                                                                          |
|-------|-------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | RESERVED                | R/W  | 1h    | TI Internal use - Do not modify                                                                                                                                                                                                                                                      |
| 30:29 | RESERVED_0              | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                                                                                                                   |
| 28:24 | WRACCESSTIME            | R/W  | Fh    | Delay from StartAccessTime to the GPMC.FCLK rising edge corresponding the the GPMC.CLK rising edge used by the attached memory for the first data capture [0x00 corresponds to 0 GPMC.FCLK cycle, 0x01 corresponds to 1 GPMC.FCLK cycle, &, 0x1F corresponds to 31 GPMC.FCLK cycles] |
| 23:20 | RESERVED_155            | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                                                                                                                   |
| 19:16 | WRDATAONADMUXBUS        | R/W  | 7h    | Specifies on which GPMC.FCLK rising edge the first data of the synchronous burst write is driven in the add/data mux bus                                                                                                                                                             |
| 15:12 | RESERVED_1              | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                                                                                                                                                                                                   |
| 11:8  | CYCLE2CYCLEDELAY        | R/W  | 0h    | Chip select high pulse delay between two successive accesses [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles]                                                                                                 |
| 7     | CYCLE2CYCLESAMECS<br>EN | R/W  | 0h    | Add Cycle2CycleDelay between two successive accesses to the same chip-select [any access type]<br>1 Add cycle2cycleDelay<br>0 No delay between the two accesses                                                                                                                      |

**Table 5-1817. GPMC\_CONFIG6 Register Field Descriptions (continued)**

| Bit | Field                   | Type | Reset | Description                                                                                                                                                                                                                                                                       |
|-----|-------------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6   | CYCLE2CYCLEDIFFCSE<br>N | R/W  | 0h    | Add Cycle2CycleDelay between two successive accesses to a different chip-select [any access type]<br><br>1        Add Cycle2CycleDelay<br>0        No delay between the two accesses                                                                                              |
| 5:4 | RESERVED_156            | R    | 0h    | Write 0's for future compatibility<br>Reads returns 0                                                                                                                                                                                                                             |
| 3:0 | BUSTURNAROUND           | R/W  | 0h    | Bus turn around latency between two successive accesses to the same chip-select [rd to wr] or to a different chip-select [read to read and read to write] [0x0 corresponds to 0 GPMC.FCLK cycle, 0x1 corresponds to 1 GPMC.FCLK cycle, &, 0xF corresponds to 15 GPMC.FCLK cycles] |

### 5.9.2.25 GPMC\_CONFIG7 Register

#### 1 GPMC\_CONFIG7 Register (Offset = 78h) [reset = F40h]

Chip-select address mapping configuration Note: For CS0, the register reset is 0xf40 while for all the other instances CS1-CS7, the reset is 0xf00.

Return to [Summary Table](#)

Offset = Base + (j \* 30h); where j = 0 to 3d

**Table 5-1818. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| GPMC0         | 4840 0078h + formula |

**Figure 5-603. GPMC\_CONFIG7 Name Register**

|              |         |             |    |             |    |    |    |
|--------------|---------|-------------|----|-------------|----|----|----|
| 31           | 30      | 29          | 28 | 27          | 26 | 25 | 24 |
| RESERVED_171 |         |             |    |             |    |    |    |
| R            |         |             |    |             |    |    |    |
| 0h           |         |             |    |             |    |    |    |
| 23           | 22      | 21          | 20 | 19          | 18 | 17 | 16 |
| RESERVED_171 |         |             |    |             |    |    |    |
| R            |         |             |    |             |    |    |    |
| 0h           |         |             |    |             |    |    |    |
| 15           | 14      | 13          | 12 | 11          | 10 | 9  | 8  |
| RESERVED_171 |         |             |    | MASKADDRESS |    |    |    |
| R            |         |             |    | R/W         |    |    |    |
| 0h           |         |             |    | Fh          |    |    |    |
| 7            | 6       | 5           | 4  | 3           | 2  | 1  | 0  |
| RESERVED_172 | CSVALID | BASEADDRESS |    |             |    |    |    |
| R            | R/W     | R/W         |    |             |    |    |    |
| 0h           | 1h      | 0h          |    |             |    |    |    |

**Table 5-1820. GPMC\_CONFIG7 Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                      |
|-------|--------------|------|-------|------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED_171 | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                               |
| 11:8  | MASKADDRESS  | R/W  | Fh    | Chip-select mask address                                                                                         |
| 7     | RESERVED_172 | R    | 0h    | Write 0's for future compatibility. Read returns 0                                                               |
| 6     | CSVALID      | R/W  | 1h    | Chip-select enable [reset value is 1 for CS0 and 0 for CS1-7]<br>1 Chip-select enabled<br>0 Chip-select disabled |
| 5:0   | BASEADDRESS  | R/W  | 0h    | Chip-select base address                                                                                         |

### 5.9.2.26 GPMC\_NAND\_COMMAND Register

#### 1 GPMC\_NAND\_COMMAND Register (Offset = 7Ch) [reset = 0h]

This Register is not a true register, just a address location.

Return to [Summary Table](#)

Offset = Base + (j \* 30h); where j = 0 to 7d

**Table 5-1821. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| GPMC0         | 4840 007Ch + formula |

**Figure 5-604. GPMC\_NAND\_COMMAND Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| GPMC_NAND_COMMAND_0 |    |    |    |    |    |    |    |
| W                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| GPMC_NAND_COMMAND_0 |    |    |    |    |    |    |    |
| W                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| GPMC_NAND_COMMAND_0 |    |    |    |    |    |    |    |
| W                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| GPMC_NAND_COMMAND_0 |    |    |    |    |    |    |    |
| W                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 5-1823. GPMC\_NAND\_COMMAND Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description |
|------|---------------------|------|-------|-------------|
| 31:0 | GPMC_NAND_COMMAND_0 | W    | 0h    |             |

### 5.9.2.27 GPMC\_NAND\_ADDRESS Register

#### 1 GPMC\_NAND\_ADDRESS Register (Offset = 80h) [reset = 0h]

This Register is not a true register, just a address location.

Return to [Summary Table](#)

Offset = Base + (j \* 30h); where j = 0 to 7d

**Table 5-1824. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| GPMC0         | 4840 0080h + formula |

**Figure 5-605. GPMC\_NAND\_ADDRESS Name Register**

|                     |    |    |    |    |    |    |    |
|---------------------|----|----|----|----|----|----|----|
| 31                  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| GPMC_NAND_ADDRESS_0 |    |    |    |    |    |    |    |
| W                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 23                  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| GPMC_NAND_ADDRESS_0 |    |    |    |    |    |    |    |
| W                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 15                  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| GPMC_NAND_ADDRESS_0 |    |    |    |    |    |    |    |
| W                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |
| 7                   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| GPMC_NAND_ADDRESS_0 |    |    |    |    |    |    |    |
| W                   |    |    |    |    |    |    |    |
| 0h                  |    |    |    |    |    |    |    |

**Table 5-1826. GPMC\_NAND\_ADDRESS Register Field Descriptions**

| Bit  | Field               | Type | Reset | Description |
|------|---------------------|------|-------|-------------|
| 31:0 | GPMC_NAND_ADDRESS_0 | W    | 0h    |             |

### 5.9.2.28 GPMC\_NAND\_DATA Register

#### 1 GPMC\_NAND\_DATA Register (Offset = 84h) [reset = 0h]

This Register is not a true register, just a address location.

Return to [Summary Table](#)

Offset = Base + (j \* 30h); where j = 0 to 7d

**Table 5-1827. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| GPMC0         | 4840 0084h + formula |

**Figure 5-606. GPMC\_NAND\_DATA Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| GPMC_NAND_DATA_0 |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| GPMC_NAND_DATA_0 |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| GPMC_NAND_DATA_0 |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| GPMC_NAND_DATA_0 |    |    |    |    |    |    |    |
| R/W              |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 5-1829. GPMC\_NAND\_DATA Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description |
|------|------------------|------|-------|-------------|
| 31:0 | GPMC_NAND_DATA_0 | R/W  | 0h    |             |

### 5.9.2.29 GPMC\_BCH\_RESULT\_0 Register

#### 1 GPMC\_BCH\_RESULT\_0 Register (Offset = 240h) [reset = 0h]

BCH ECC result, bits 0 to 31

Return to [Summary Table](#)

Offset = Base + (j \* 10h); where j = 0 to 7d

**Table 5-1830. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| GPMC0         | 4840 0240h + formula |

**Figure 5-607. GPMC\_BCH\_RESULT\_0 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BCH_RESULT_0 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BCH_RESULT_0 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| BCH_RESULT_0 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| BCH_RESULT_0 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-1832. GPMC\_BCH\_RESULT\_0 Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                  |
|------|--------------|------|-------|------------------------------|
| 31:0 | BCH_RESULT_0 | R    | 0h    | BCH ECC result, bits 0 to 31 |

### 5.9.2.30 GPMC\_BCH\_RESULT\_1 Register

#### 1 GPMC\_BCH\_RESULT\_1 Register (Offset = 244h) [reset = 0h]

BCH ECC result, bits 32 to 63

Return to [Summary Table](#)

Offset = Base + (j \* 10h); where j = 0 to 7d

**Table 5-1833. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| GPMC0         | 4840 0244h + formula |

**Figure 5-608. GPMC\_BCH\_RESULT\_1 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BCH_RESULT_1 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BCH_RESULT_1 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| BCH_RESULT_1 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| BCH_RESULT_1 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-1835. GPMC\_BCH\_RESULT\_1 Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                   |
|------|--------------|------|-------|-------------------------------|
| 31:0 | BCH_RESULT_1 | R    | 0h    | BCH ECC result, bits 32 to 63 |



### 5.9.2.31 GPMC\_BCH\_RESULT\_2 Register

#### 1 GPMC\_BCH\_RESULT\_2 Register (Offset = 248h) [reset = 0h]

BCH ECC result, bits 64 to 95

Return to [Summary Table](#)

Offset = Base + (j \* 10h); where j = 0 to 7d

**Table 5-1836. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| GPMC0         | 4840 0248h + formula |

**Figure 5-609. GPMC\_BCH\_RESULT\_2 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BCH_RESULT_2 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BCH_RESULT_2 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| BCH_RESULT_2 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| BCH_RESULT_2 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-1838. GPMC\_BCH\_RESULT\_2 Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                   |
|------|--------------|------|-------|-------------------------------|
| 31:0 | BCH_RESULT_2 | R    | 0h    | BCH ECC result, bits 64 to 95 |

### 5.9.2.32 GPMC\_BCH\_RESULT\_3 Register

#### 1 GPMC\_BCH\_RESULT\_3 Register (Offset = 24Ch) [reset = 0h]

BCH ECC result, bits 96 to 127

Return to [Summary Table](#)

Offset = Base + (j \* 10h); where j = 0 to 7d

**Table 5-1839. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| GPMC0         | 4840 024Ch + formula |

**Figure 5-610. GPMC\_BCH\_RESULT\_3 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BCH_RESULT_3 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BCH_RESULT_3 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| BCH_RESULT_3 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| BCH_RESULT_3 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-1841. GPMC\_BCH\_RESULT\_3 Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                    |
|------|--------------|------|-------|--------------------------------|
| 31:0 | BCH_RESULT_3 | R    | 0h    | BCH ECC result, bits 96 to 127 |

### 5.9.2.33 GPMC\_BCH\_RESULT\_4 Register

#### 1 GPMC\_BCH\_RESULT\_4 Register (Offset = 300h) [reset = 0h]

BCH ECC result, bits 128 to 159

Return to [Summary Table](#)

Offset = Base + (j \* 10h); where j = 0 to 7d

**Table 5-1842. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| GPMC0         | 4840 0300h + formula |

**Figure 5-611. GPMC\_BCH\_RESULT\_4 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BCH_RESULT_4 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BCH_RESULT_4 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| BCH_RESULT_4 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| BCH_RESULT_4 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-1844. GPMC\_BCH\_RESULT\_4 Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                     |
|------|--------------|------|-------|---------------------------------|
| 31:0 | BCH_RESULT_4 | R    | 0h    | BCH ECC result, bits 128 to 159 |

### 5.9.2.34 GPMC\_BCH\_RESULT\_5 Register

#### 1 GPMC\_BCH\_RESULT\_5 Register (Offset = 304h) [reset = 0h]

BCH ECC result, bits 160 to 191

Return to [Summary Table](#)

Offset = Base + (j \* 10h); where j = 0 to 7d

**Table 5-1845. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| GPMC0         | 4840 0304h + formula |

**Figure 5-612. GPMC\_BCH\_RESULT\_5 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| BCH_RESULT_5 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| BCH_RESULT_5 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| BCH_RESULT_5 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| BCH_RESULT_5 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-1847. GPMC\_BCH\_RESULT\_5 Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                     |
|------|--------------|------|-------|---------------------------------|
| 31:0 | BCH_RESULT_5 | R    | 0h    | BCH ECC result, bits 160 to 191 |

### 5.9.2.35 GPMC\_BCH\_RESULT\_6 Register

#### 1 GPMC\_BCH\_RESULT\_6 Register (Offset = 308h) [reset = 0h]

BCH ECC result, bits 192 to 207

Return to [Summary Table](#)

Offset = Base + (j \* 10h); where j = 0 to 7d

**Table 5-1848. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| GPMC0         | 4840 0308h + formula |

**Figure 5-613. GPMC\_BCH\_RESULT\_6 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED     |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED     |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| BCH_RESULT_6 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| BCH_RESULT_6 |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-1850. GPMC\_BCH\_RESULT\_6 Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                     |
|-------|--------------|------|-------|---------------------------------|
| 31:16 | RESERVED     | R    | 0h    | Reserved                        |
| 15:0  | BCH_RESULT_6 | R    | 0h    | BCH ECC result, bits 192 to 207 |

## 5.10 I2C

### I2C

#### 5.10.1 I2C Summaries

#### I2C Summaries

**Table 5-1851. I2C Registers, Base Address=5250 0000h, Length=128**

| Offset | Length | Register Name               | I2C0 Physical Address | I2C1 Physical Address | I2C2 Physical Address |
|--------|--------|-----------------------------|-----------------------|-----------------------|-----------------------|
| 0h     | 32     | <a href="#">I2C_ICOAR</a>   | 5250 0000h            | 5250 1000h            | 5250 2000h            |
| 4h     | 32     | <a href="#">I2C_ICIMR</a>   | 5250 0004h            | 5250 1004h            | 5250 2004h            |
| 8h     | 32     | <a href="#">I2C_ICSTR</a>   | 5250 0008h            | 5250 1008h            | 5250 2008h            |
| Ch     | 32     | <a href="#">I2C_ICCLKL</a>  | 5250 000Ch            | 5250 100Ch            | 5250 200Ch            |
| 10h    | 32     | <a href="#">I2C_ICCLKH</a>  | 5250 0010h            | 5250 1010h            | 5250 2010h            |
| 14h    | 32     | <a href="#">I2C_ICCNT</a>   | 5250 0014h            | 5250 1014h            | 5250 2014h            |
| 18h    | 32     | <a href="#">I2C_ICDRR</a>   | 5250 0018h            | 5250 1018h            | 5250 2018h            |
| 1Ch    | 32     | <a href="#">I2C_ICSAR</a>   | 5250 001Ch            | 5250 101Ch            | 5250 201Ch            |
| 20h    | 32     | <a href="#">I2C_ICDXR</a>   | 5250 0020h            | 5250 1020h            | 5250 2020h            |
| 24h    | 32     | <a href="#">I2C_ICMDR</a>   | 5250 0024h            | 5250 1024h            | 5250 2024h            |
| 28h    | 32     | <a href="#">I2C_ICIVR</a>   | 5250 0028h            | 5250 1028h            | 5250 2028h            |
| 2Ch    | 32     | <a href="#">I2C_ICEMDR</a>  | 5250 002Ch            | 5250 102Ch            | 5250 202Ch            |
| 30h    | 32     | <a href="#">I2C_ICPSC</a>   | 5250 0030h            | 5250 1030h            | 5250 2030h            |
| 34h    | 32     | <a href="#">I2C_ICPID1</a>  | 5250 0034h            | 5250 1034h            | 5250 2034h            |
| 38h    | 32     | <a href="#">I2C_ICPID2</a>  | 5250 0038h            | 5250 1038h            | 5250 2038h            |
| 3Ch    | 32     | <a href="#">I2C_ICDMAC</a>  | 5250 003Ch            | 5250 103Ch            | 5250 203Ch            |
| 48h    | 32     | <a href="#">I2C_ICPFUNC</a> | 5250 0048h            | 5250 1048h            | 5250 2048h            |
| 4Ch    | 32     | <a href="#">I2C_ICPDIR</a>  | 5250 004Ch            | 5250 104Ch            | 5250 204Ch            |
| 50h    | 32     | <a href="#">I2C_ICPDIN</a>  | 5250 0050h            | 5250 1050h            | 5250 2050h            |
| 54h    | 32     | <a href="#">I2C_ICPDOUT</a> | 5250 0054h            | 5250 1054h            | 5250 2054h            |
| 58h    | 32     | <a href="#">I2C_ICPDSET</a> | 5250 0058h            | 5250 1058h            | 5250 2058h            |
| 5Ch    | 32     | <a href="#">I2C_ICPDCLR</a> | 5250 005Ch            | 5250 105Ch            | 5250 205Ch            |
| 60h    | 32     | <a href="#">I2C_ICPDRV</a>  | 5250 0060h            | 5250 1060h            | 5250 2060h            |

**Table 5-1852. I2C Registers, Base Address=5250 0000h, Length=128**

| Offset | Length | Register Name              | I2C3 Physical Address |
|--------|--------|----------------------------|-----------------------|
| 0h     | 32     | <a href="#">I2C_ICOAR</a>  | 5250 3000h            |
| 4h     | 32     | <a href="#">I2C_ICIMR</a>  | 5250 3004h            |
| 8h     | 32     | <a href="#">I2C_ICSTR</a>  | 5250 3008h            |
| Ch     | 32     | <a href="#">I2C_ICCLKL</a> | 5250 300Ch            |
| 10h    | 32     | <a href="#">I2C_ICCLKH</a> | 5250 3010h            |
| 14h    | 32     | <a href="#">I2C_ICCNT</a>  | 5250 3014h            |
| 18h    | 32     | <a href="#">I2C_ICDRR</a>  | 5250 3018h            |
| 1Ch    | 32     | <a href="#">I2C_ICSAR</a>  | 5250 301Ch            |
| 20h    | 32     | <a href="#">I2C_ICDXR</a>  | 5250 3020h            |
| 24h    | 32     | <a href="#">I2C_ICMDR</a>  | 5250 3024h            |
| 28h    | 32     | <a href="#">I2C_ICIVR</a>  | 5250 3028h            |

**Table 5-1852. I2C Registers, Base Address=5250 0000h, Length=128 (continued)**

| Offset | Length | Register Name               | I2C3 Physical Address |
|--------|--------|-----------------------------|-----------------------|
| 2Ch    | 32     | <a href="#">I2C_ICEMDR</a>  | 5250 302Ch            |
| 30h    | 32     | <a href="#">I2C_ICPSC</a>   | 5250 3030h            |
| 34h    | 32     | <a href="#">I2C_ICPID1</a>  | 5250 3034h            |
| 38h    | 32     | <a href="#">I2C_ICPID2</a>  | 5250 3038h            |
| 3Ch    | 32     | <a href="#">I2C_ICDMAC</a>  | 5250 303Ch            |
| 48h    | 32     | <a href="#">I2C_ICPFUNC</a> | 5250 3048h            |
| 4Ch    | 32     | <a href="#">I2C_ICPDIR</a>  | 5250 304Ch            |
| 50h    | 32     | <a href="#">I2C_ICPDIN</a>  | 5250 3050h            |
| 54h    | 32     | <a href="#">I2C_ICPDOUT</a> | 5250 3054h            |
| 58h    | 32     | <a href="#">I2C_ICPDSET</a> | 5250 3058h            |
| 5Ch    | 32     | <a href="#">I2C_ICPDCLR</a> | 5250 305Ch            |
| 60h    | 32     | <a href="#">I2C_ICPDRV</a>  | 5250 3060h            |

### 5.10.2 I2C Registers

#### I2C Registers

### 5.10.2.1 I2C\_ICOAR Register

#### 1 I2C\_ICOAR Register (Offset = 0h) [reset = 0h]

I2C Own Address register

Return to [Summary Table](#)

**Table 5-1853. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| I2C0          | 5250 0000h       |
| I2C1          | 5250 1000h       |
| I2C2          | 5250 2000h       |
| I2C3          | 5250 3000h       |

**Figure 5-614. I2C\_ICOAR Name Register**

|       |    |    |    |    |    |       |    |
|-------|----|----|----|----|----|-------|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25    | 24 |
| NU    |    |    |    |    |    |       |    |
| R/W   |    |    |    |    |    |       |    |
| 0h    |    |    |    |    |    |       |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17    | 16 |
| NU    |    |    |    |    |    |       |    |
| R/W   |    |    |    |    |    |       |    |
| 0h    |    |    |    |    |    |       |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9     | 8  |
| NU    |    |    |    |    |    | A9_A0 |    |
| R/W   |    |    |    |    |    | R/W   |    |
| 0h    |    |    |    |    |    | 0h    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1     | 0  |
| A9_A0 |    |    |    |    |    |       |    |
| R/W   |    |    |    |    |    |       |    |
| 0h    |    |    |    |    |    |       |    |

**Table 5-1855. I2C\_ICOAR Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                           |
|-------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:10 | NU    | R/W  | 0h    | Reserved                                                                                                                                                                              |
| 9:0   | A9_A0 | R/W  | 0h    | Own address. Use in both 7- and 10-bit address mode. Note that user can program the I2C own address to any value as long as it does not conflict with other components in the system. |



### 5.10.2.2 I2C\_ICIMR Register

#### 1 I2C\_ICIMR Register (Offset = 4h) [reset = 0h]

I2C Interrupt Mask/Status register

Return to [Summary Table](#)
**Table 5-1856. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| I2C0          | 5250 0004h       |
| I2C1          | 5250 1004h       |
| I2C2          | 5250 2004h       |
| I2C3          | 5250 3004h       |

**Figure 5-615. I2C\_ICIMR Name Register**

|     |     |     |        |        |      |      |     |
|-----|-----|-----|--------|--------|------|------|-----|
| 31  | 30  | 29  | 28     | 27     | 26   | 25   | 24  |
| NU  |     |     |        |        |      |      |     |
| R/W |     |     |        |        |      |      |     |
| 0h  |     |     |        |        |      |      |     |
| 23  | 22  | 21  | 20     | 19     | 18   | 17   | 16  |
| NU  |     |     |        |        |      |      |     |
| R/W |     |     |        |        |      |      |     |
| 0h  |     |     |        |        |      |      |     |
| 15  | 14  | 13  | 12     | 11     | 10   | 9    | 8   |
| NU  |     |     |        |        |      |      |     |
| R/W |     |     |        |        |      |      |     |
| 0h  |     |     |        |        |      |      |     |
| 7   | 6   | 5   | 4      | 3      | 2    | 1    | 0   |
| NU  | AAS | SCD | ICXRDY | ICRRDY | ARDY | NACK | AL  |
| R/W | R/W | R/W | R/W    | R/W    | R/W  | R/W  | R/W |
| 0h  | 0h  | 0h  | 0h     | 0h     | 0h   | 0h   | 0h  |

**Table 5-1858. I2C\_ICIMR Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                                                                          |
|------|--------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | NU     | R/W  | 0h    | Reserved                                                                                                                                                                             |
| 6    | AAS    | R/W  | 0h    | Address As Target interrupt mask bit. Setting a "1" to this bit unmask the Address As Target interrupt. Setting a "0" to this bit masks the Address As Target interrupt.             |
| 5    | SCD    | R/W  | 0h    | Stop Condition Detection mask bit. Setting a "1" to this bit unmask the Stop Condition Detection interrupt. Setting a "0" to this bit masks the Stop Condition Detection interrupt.  |
| 4    | ICXRDY | R/W  | 0h    | Transmit Data Ready interrupt mask bit. Setting a "1" to this bit unmask the Transmit Data Ready interrupt. Setting a "0" to this bit masks the Transmit Data Ready interrupt.       |
| 3    | ICRRDY | R/W  | 0h    | Receive Data Ready interrupt mask bit. Setting a "1" to this bit unmask the Receive Data Ready interrupt. Setting a "0" to this bit masks the Receive Data Ready interrupt.          |
| 2    | ARDY   | R/W  | 0h    | Register access ready interrupt mask bit. Setting a "1" to this bit unmask the Register access ready interrupt. Setting a "0" to this bit masks the Register access ready interrupt. |
| 1    | NACK   | R/W  | 0h    | No Acknowledgement interrupt mask bit. Setting a "1" to this bit unmask the No Acknowledgement interrupt. Setting a "0" to this bit masks the No Acknowledgement interrupt.          |

**Table 5-1858. I2C\_ICIMR Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                             |
|-----|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | AL    | R/W  | 0h    | Arbitration Lost interrupt mask bit. Setting a "1" to this bit unmaskes the Arbitration Lost interrupt. Setting a "0" to this bit masks the Arbitration Lost interrupt. |

### 5.10.2.3 I2C\_ICSTR Register

#### 1 I2C\_ICSTR Register (Offset = 8h) [reset = 0h]

I2C Interrupt Status register

Return to [Summary Table](#)

**Table 5-1859. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| I2C0          | 5250 0008h       |
| I2C1          | 5250 1008h       |
| I2C2          | 5250 2008h       |
| I2C3          | 5250 3008h       |

**Figure 5-616. I2C\_ICSTR Name Register**

|     |      |         |        |        |      |      |     |
|-----|------|---------|--------|--------|------|------|-----|
| 31  | 30   | 29      | 28     | 27     | 26   | 25   | 24  |
| NU2 |      |         |        |        |      |      |     |
| NU2 |      |         |        |        |      |      |     |
| 0h  |      |         |        |        |      |      |     |
| 23  | 22   | 21      | 20     | 19     | 18   | 17   | 16  |
| NU2 |      |         |        |        |      |      |     |
| NU2 |      |         |        |        |      |      |     |
| 0h  |      |         |        |        |      |      |     |
| 15  | 14   | 13      | 12     | 11     | 10   | 9    | 8   |
| NU2 | SDIR | NACKSNT | BB     | RSFULL | XSMT | AAS  | AD0 |
| NU2 | R/W  | R/W     | R/W    | R/W    | R/W  | R/W  | R/W |
| 0h  | 0h   | 0h      | 0h     | 0h     | 0h   | 0h   | 0h  |
| 7   | 6    | 5       | 4      | 3      | 2    | 1    | 0   |
| NU1 |      | SCD     | ICXRDY | ICRRDY | ARDY | NACK | AL  |
| NU1 |      | R/W     | R/W    | R/W    | R/W  | R/W  | R/W |
| 0h  |      | 0h      | 0h     | 0h     | 0h   | 0h   | 0h  |

**Table 5-1861. I2C\_ICSTR Register Field Descriptions**

| Bit   | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|---------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:15 | NU2     | NU2  | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 14    | SDIR    | R/W  | 0h    | Target Direction. This bit is clear to '0' indicating the I2C is a controller transmitter/receiver or a target receiver. This bit is also clear by STOP condition or START condition. It is set to '1' when the I2C target is a transmitter. In DLB mode [which the configuration should be controller-transmitter target-receiver] this bit is clear to '0'. Writing a "1" to this bit to clear it.                                                                                                                         |
| 13    | NACKSNT | R/W  | 0h    | A No Acknowledge is sent due to NACKMOD is set to a "1".<br>NACKSNT<br>0:A No Acknowledge is not sent. NACKSNT<br>1:A No Acknowledge is sent. Writing a "1" to this bit to clear it.                                                                                                                                                                                                                                                                                                                                         |
| 12    | BB      | R/W  | 0h    | Bus Busy. This bit indicates the state of the serial bus. BB<br>0:The bus is free. BB<br>1:The bus is occupied. On reception of a "start" condition the device sets BB to 1. This bit is also set if the I2C detects SCL low state. BB is clear to 0 after reception of a "stop" condition. BB is kept to "0" regardless SCL state when the I2C is in reset [IRS_ =0]. If the IRS_ is set to "1" during transaction between other I2C devices the BB bit is set at the first falling edge of SCL or START condition. - [RW ] |

**Table 5-1861. I2C\_ICSTR Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|--------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11  | RSFULL | R/W  | 0h    | Receive shift full. This bit indicates whether the receiver has experienced overrun. Overrun occurs when the receive shift register [ICRSR] is full and ICDRR has not been read since the ICRSR-to-ICDRR transfer. The FSM is holding for ICDRR read access. RSFULL is clear when Reading the ICDRR. RSFULL is set to "1" when the I2C has recognized an overrun. The contents of ICDRR are NOT lost in this case. In repeat mode since double buffer [ICRSR and ICDRR] behaves like a single buffer RSFULL is set to "1" every time the data is received. RSFULL is clear as a result of Reading the ICDRR. - [RW ]                                                                                                                 |
| 10  | XSMT   | R/W  | 0h    | Transmit shift empty not. This bit indicates whether the transmitter has experienced underflow. Underflow occurs when the transmit shift register [ICXSR] is empty and ICDXR has not been loaded. The FSM is holding for ICDXR write access. XSMT_ is cleared when underflow has occurred. XSMT_ is set to "1" as a result of Writing to ICDXR. In repeat mode if the I2C in controller transmitter mode is holding transfer with XSMT_ =0 [i.e. waiting for further action] and the STT or STP bit is set XSMT_ is set to "1" by hardware.                                                                                                                                                                                          |
| 9   | AAS    | R/W  | 0h    | Address As Target. This bit is set to 1 by the device when it has recognized its own target address or an address of all [8] zeros. The AAS bit is reset by stop condition or detection of any address byte that does not match ICOAR. - [RW ]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 8   | AD0    | R/W  | 0h    | Address Zero Status: This bit is set to 1 by device if it detects the address of all [8] zeros [i.e. general call]. The AD0 bit is reset to 0 [default value] when a "start" or "stop" condition is detected. - [RW ]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 7:6 | NU1    | NU1  | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 5   | SCD    | R/W  | 0h    | Stop Condition Detection bit SCD is set when the I2C sends or receives STOP condition. This bit is cleared by Reading ICIVR [as 110] or Writing '1' to itself.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 4   | ICXRDY | R/W  | 0h    | Transmit Data Ready interrupt flag bit. ICXRDY is set to "1" is generated when the transmitted data has been copied from ICDXR to the transmit-shift register [ICXSR]. ICXRDY is clear to "0" when the ICDXR is written. This bit can also be polled by the CPU to write a new transmitted data into the ICDXR. Write '1' to this bit will set it and DXR Write will clear it.                                                                                                                                                                                                                                                                                                                                                       |
| 3   | ICRRDY | R/W  | 0h    | Receive Data Ready interrupt flag bit. ICRRDY is set to "1" when the received data has been copied from ICRSR into the ICDRR. ICRRDY is cleared to "0" when the ICDRR is read. This bit can also be polled by the CPU to read the received data in the ICDRR. Write '1' or DRR Read will clear it.                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 2   | ARDY   | R/W  | 0h    | Register-access-ready interrupt flag bit. ARDY is generated by the hardware if the I2C is in the controller mode when the previously programmed data and command has been performed and status bit has been updated. This flag is used by the CPU to let it knows that the I2C registers are ready to be accessed again. When RM=0 ARDY is set when the internal data count is passed 0 if STP register bit has not been set. When RM=1 ARDY is set at each byte end. If the I2C is in FDF mode[FDF=1] ARDY is set just after Start condition. This bit is automatically cleared by hardware when Writing data to ICDXR in transmit mode Reading data from ICDRR in receive mode or setting STT or STP bit. Write '1' will clear it. |
| 1   | NACK   | R/W  | 0h    | No-Acknowledgement interrupt flag bit. The No Acknowledge flag bit is set when the hardware in "controller" mode detects no acknowledge has been received. This bit is NOT set by no-acknowledgement after Start byte Write '1' or Read the ICIVR [as 010] will clear it.                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

**Table 5-1861. I2C\_ICSTR Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | AL    | R/W  | 0h    | Arbitration-Lost interrupt flag bit. The Arbitration Lost flag bit is set to 1 when the device in the "controller" mode senses it has lost an arbitration when two or more transmitters start a transmission almost simultaneously or when the I2C attempts to start a transfer while BB [bus busy] is 1. When this is set to 1 due to arbitration lost the MST/STT/STP bits are clear the I2C becomes a target. Write '1' or Read the ICIVR [as 001] will clear it. |

### 5.10.2.4 I2C\_ICCLKL Register

#### 1 I2C\_ICCLKL Register (Offset = Ch) [reset = 0h]

I2C Clock Divider Low register

Return to [Summary Table](#)

**Table 5-1862. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| I2C0          | 5250 000Ch       |
| I2C1          | 5250 100Ch       |
| I2C2          | 5250 200Ch       |
| I2C3          | 5250 300Ch       |

**Figure 5-617. I2C\_ICCLKL Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| NU           |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| NU           |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICCL15_ICCL0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICCL15_ICCL0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-1864. I2C\_ICCLKL Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                                                                                                                            |
|-------|--------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | NU           | R/W  | 0h    | Reserved                                                                                                                                                                                                               |
| 15:0  | ICCL15_ICCL0 | R/W  | 0h    | Low time I2C SCL Clock Division Factor. They are used to divide down the controller clock to create the SCL low time transition frequency. This register must be configured while the I2C is still in reset [IRS_ =0]. |

### 5.10.2.5 I2C\_ICCLKH Register

#### 1 I2C\_ICCLKH Register (Offset = 10h) [reset = 0h]

I2C Clock Divider High register

Return to [Summary Table](#)

**Table 5-1865. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| I2C0          | 5250 0010h       |
| I2C1          | 5250 1010h       |
| I2C2          | 5250 2010h       |
| I2C3          | 5250 3010h       |

**Figure 5-618. I2C\_ICCLKH Name Register**

|               |    |    |    |    |    |    |    |
|---------------|----|----|----|----|----|----|----|
| 31            | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| NU            |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 23            | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| NU            |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 15            | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICCH15_ICCLH0 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |
| 7             | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICCH15_ICCLH0 |    |    |    |    |    |    |    |
| R/W           |    |    |    |    |    |    |    |
| 0h            |    |    |    |    |    |    |    |

**Table 5-1867. I2C\_ICCLKH Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                                                                                                |
|-------|---------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | NU            | R/W  | 0h    | Reserved                                                                                                                                                                                                                   |
| 15:0  | ICCH15_ICCLH0 | R/W  | 0h    | High time I 2 C SCL Clock Division Factor. They are used to divide down the controller clock to create the SCL high time transition frequency. This register must be configured while the I2C is still in reset [IRS_ =0]. |

### 5.10.2.6 I2C\_ICCNT Register

#### 1 I2C\_ICCNT Register (Offset = 14h) [reset = 0h]

I2C Data Count register

Return to [Summary Table](#)

**Table 5-1868. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| I2C0          | 5250 0014h       |
| I2C1          | 5250 1014h       |
| I2C2          | 5250 2014h       |
| I2C3          | 5250 3014h       |

**Figure 5-619. I2C\_ICCNT Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| NU           |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| NU           |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ICDC15_ICDC0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ICDC15_ICDC0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-1870. I2C\_ICCNT Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                         |
|-------|--------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | NU           | R/W  | 0h    | Reserved                                                                                                                                                                                                                                                                            |
| 15:0  | ICDC15_ICDC0 | R/W  | 0h    | Data count. This data count register is used to generate a Stop condition if a Stop condition is specified [STP=1].<br>ICCNT=1 data count is 1<br>.....<br>ICCNT=0FFFFh data count is 65535<br>ICCNT=0data counter is 65536<br>Note that ICCNT is a don't care when RM is set to 1. |



### 5.10.2.7 I2C\_ICDRR Register

#### 1 I2C\_ICDRR Register (Offset = 18h) [reset = 0h]

I2C Data Receive register

Return to [Summary Table](#)
**Table 5-1871. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| I2C0          | 5250 0018h       |
| I2C1          | 5250 1018h       |
| I2C2          | 5250 2018h       |
| I2C3          | 5250 3018h       |

**Figure 5-620. I2C\_ICDRR Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| NU    |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| NU    |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| NU    |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| D7_D0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-1873. I2C\_ICDRR Register Field Descriptions**

| Bit  | Field | Type | Reset | Description  |
|------|-------|------|-------|--------------|
| 31:8 | NU    | R/W  | 0h    | Reserved     |
| 7:0  | D7_D0 | R/W  | 0h    | Receive data |

### 5.10.2.8 I2C\_ICSAR Register

#### 1 I2C\_ICSAR Register (Offset = 1Ch) [reset = 0h]

I2C Target Address register

Return to [Summary Table](#)

**Table 5-1874. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| I2C0          | 5250 001Ch       |
| I2C1          | 5250 101Ch       |
| I2C2          | 5250 201Ch       |
| I2C3          | 5250 301Ch       |

**Figure 5-621. I2C\_ICSAR Name Register**

|       |    |    |    |    |    |       |    |
|-------|----|----|----|----|----|-------|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25    | 24 |
| NU    |    |    |    |    |    |       |    |
| R/W   |    |    |    |    |    |       |    |
| 0h    |    |    |    |    |    |       |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17    | 16 |
| NU    |    |    |    |    |    |       |    |
| R/W   |    |    |    |    |    |       |    |
| 0h    |    |    |    |    |    |       |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9     | 8  |
| NU    |    |    |    |    |    | A9_A0 |    |
| R/W   |    |    |    |    |    | R/W   |    |
| 0h    |    |    |    |    |    | 0h    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1     | 0  |
| A9_A0 |    |    |    |    |    |       |    |
| R/W   |    |    |    |    |    |       |    |
| 0h    |    |    |    |    |    |       |    |

**Table 5-1876. I2C\_ICSAR Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                             |
|-------|-------|------|-------|---------------------------------------------------------|
| 31:10 | NU    | R/W  | 0h    | Reserved                                                |
| 9:0   | A9_A0 | R/W  | 0h    | Target address. Use in both 7- and 10-bit address mode. |

### 5.10.2.9 I2C\_ICDXR Register

#### 1 I2C\_ICDXR Register (Offset = 20h) [reset = 0h]

I2C Data Transmit register

Return to [Summary Table](#)
**Table 5-1877. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| I2C0          | 5250 0020h       |
| I2C1          | 5250 1020h       |
| I2C2          | 5250 2020h       |
| I2C3          | 5250 3020h       |

**Figure 5-622. I2C\_ICDXR Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| NU    |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| NU    |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| NU    |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| D7_D0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-1879. I2C\_ICDXR Register Field Descriptions**

| Bit  | Field | Type | Reset | Description   |
|------|-------|------|-------|---------------|
| 31:8 | NU    | R/W  | 0h    | Reserved      |
| 7:0  | D7_D0 | R/W  | 0h    | Transmit data |

### 5.10.2.10 I2C\_ICMDR Register

#### 1 I2C\_ICMDR Register (Offset = 24h) [reset = 0h]

I2C Mode register

Return to [Summary Table](#)
**Table 5-1880. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| I2C0          | 5250 0024h       |
| I2C1          | 5250 1024h       |
| I2C2          | 5250 2024h       |
| I2C3          | 5250 3024h       |

**Figure 5-623. I2C\_ICMDR Name Register**

|         |      |     |     |     |             |     |     |
|---------|------|-----|-----|-----|-------------|-----|-----|
| 31      | 30   | 29  | 28  | 27  | 26          | 25  | 24  |
| NU2     |      |     |     |     |             |     |     |
| NU2     |      |     |     |     |             |     |     |
| 0h      |      |     |     |     |             |     |     |
| 23      | 22   | 21  | 20  | 19  | 18          | 17  | 16  |
| NU2     |      |     |     |     |             |     |     |
| NU2     |      |     |     |     |             |     |     |
| 0h      |      |     |     |     |             |     |     |
| 15      | 14   | 13  | 12  | 11  | 10          | 9   | 8   |
| NACKMOD | FREE | STT | NU1 | STP | MST         | TRX | XA  |
| R/W     | R/W  | R/W | NU1 | R/W | R/W         | R/W | R/W |
| 0h      | 0h   | 0h  | 0h  | 0h  | 0h          | 0h  | 0h  |
| 7       | 6    | 5   | 4   | 3   | 2           | 1   | 0   |
| RM      | DLB  | IRS | STB | FDF | BC2_BC1_BC0 |     |     |
| R/W     | R/W  | R/W | R/W | R/W | R/W         |     |     |
| 0h      | 0h   | 0h  | 0h  | 0h  | 0h          |     |     |

**Table 5-1882. I2C\_ICMDR Register Field Descriptions**

| Bit   | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|---------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | NU2     | NU2  | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 15    | NACKMOD | R/W  | 0h    | No Acknowledge [NACK] mode. This bit is used to send an Acknowledge [ACK] or a No Acknowledge [NACK] to the transmitter. This bit is only applicable when the I2C is in receiver mode. In controller receiver mode when the internal data count counter decrements to zero the I2C sends a NACK. The controller receiver I2C finishes a transfer when it sends a NACK. The I2C ignores ICCNT when NACKMOD is '1'. The NACKMOD bit should be set before the rising edge of the last data bit [bit 8] if a NACK must be sent and this bit is cleared once a NACK has been sent. NACKMOD=0 the I2C sends an ACK to the transmitter during the acknowledge cycle. NACKMOD=1 the I2C sends a NACK to the transmitter during the acknowledge cycle. |
| 14    | FREE    | R/W  | 0h    | Free Running. This bit is used to determine the state of the I2C when a breakpoint is encountered in the HLL debugger. FREE 0:[default] Stops immediately if SCL is low and keep driving SCL low whether I2C is controller transmitter/receiver. If SCL is high I2C waits until SCL becomes low and then stops. If the I2C is a target it will stop when the transmission/receiving completes. FREE 1:The I2C runs free.                                                                                                                                                                                                                                                                                                                      |

**Table 5-1882. I2C\_ICMDR Register Field Descriptions (continued)**

| Bit | Field | Type                     | Reset           | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                                                                                                    |     |            |                 |   |   |                   |       |   |                      |      |   |                       |   |                       |                          |   |   |                  |               |
|-----|-------|--------------------------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|------------|-----------------|---|---|-------------------|-------|---|----------------------|------|---|-----------------------|---|-----------------------|--------------------------|---|---|------------------|---------------|
| 13  | STT   | R/W                      | 0h              | <p>Start Condition [Controller only mode]. This bit can be set to a"1" by the CPU to generate a Start condition. In controller mode when setting Start to"1" generates a Start condition. It is reset to "0" by the hardware after the Start condition has been generated. The Start/ Stop bits can be configured to generate different transfer formats. Note that the STT and STP can be used to terminate the repeat mode.</p> <table><tr><th>STT</th><th>STP</th><th>Conditions</th><th>Bus Activities</th></tr><tr><td>1</td><td>0</td><td>Start</td><td>S-A-D</td></tr><tr><td>0</td><td>1</td><td>Stop</td><td>P</td></tr><tr><td>1</td><td>1</td><td>Start-Stop [ICCNT= n]</td><td>S-A-D..[n]..D-P</td></tr><tr><td>1</td><td>0</td><td>Start [ICCNT= n]</td><td>S-A-D..[n]..D</td></tr></table> | STT                                                                                                                                                                                                                                                                                                                | STP | Conditions | Bus Activities  | 1 | 0 | Start             | S-A-D | 0 | 1                    | Stop | P | 1                     | 1 | Start-Stop [ICCNT= n] | S-A-D..[n]..D-P          | 1 | 0 | Start [ICCNT= n] | S-A-D..[n]..D |
| STT | STP   | Conditions               | Bus Activities  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                                                                                                                                                                                                                                                                    |     |            |                 |   |   |                   |       |   |                      |      |   |                       |   |                       |                          |   |   |                  |               |
| 1   | 0     | Start                    | S-A-D           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                                                                                                                                                                                                                                                                    |     |            |                 |   |   |                   |       |   |                      |      |   |                       |   |                       |                          |   |   |                  |               |
| 0   | 1     | Stop                     | P               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                                                                                                                                                                                                                                                                    |     |            |                 |   |   |                   |       |   |                      |      |   |                       |   |                       |                          |   |   |                  |               |
| 1   | 1     | Start-Stop [ICCNT= n]    | S-A-D..[n]..D-P |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                                                                                                                                                                                                                                                                    |     |            |                 |   |   |                   |       |   |                      |      |   |                       |   |                       |                          |   |   |                  |               |
| 1   | 0     | Start [ICCNT= n]         | S-A-D..[n]..D   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                                                                                                                                                                                                                                                                    |     |            |                 |   |   |                   |       |   |                      |      |   |                       |   |                       |                          |   |   |                  |               |
| 12  | NU1   | NU1                      | 0h              | Reserved for IDLEEN [IDLE Enable on 5509. - [RW ]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                                                                                                                                                                                                                                                                                                    |     |            |                 |   |   |                   |       |   |                      |      |   |                       |   |                       |                          |   |   |                  |               |
| 11  | STP   | R/W                      | 0h              | Stop Condition [Controller mode only]. This bit can be set to a"1" by the CPU to generate a Stop condition. It is reset to "0" by the hardware after the Stop condition has been generated. The Stop condition is generated when ICCNT passes 0 when the I2C is in non-repeat mode[RM=0].                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                                                                                                    |     |            |                 |   |   |                   |       |   |                      |      |   |                       |   |                       |                          |   |   |                  |               |
| 10  | MST   | R/W                      | 0h              | Controller. MST<br>0:The I 2 C peripheral is in the"target" mode and clock is received from the"controller" device. MST<br>1:The I 2 C peripheral is in the"controller" mode and it generates the clock. This bit is clear when the transfer completed.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                                                                                                                                                                                                                                                                                                                    |     |            |                 |   |   |                   |       |   |                      |      |   |                       |   |                       |                          |   |   |                  |               |
| 9   | TRX   | R/W                      | 0h              | Transmitter. TRX<br>0:The I 2 C is in the"receiver" mode and data on data line SDA is shifted into the data register ICDRR. TRX<br>1:The I 2 C is in the"transmitter" mode and the data in ICDXR is shifted out on data line SDA. The operating modes [not in FDF mode] are defined as follows. In FDF mode TRX must be configured even if the I2C is in target mode because there is no address/ direction byte in FDF mode.                                                                                                                                                                                                                                                                                                                                                                            | <table><tr><th>MST</th><th>TRX</th><th>Operating Modes</th></tr><tr><td>0</td><td>x</td><td>"target receiver"</td></tr><tr><td>0</td><td>x</td><td>"target transmitter"</td></tr><tr><td>1</td><td>0</td><td>"controller receiver"</td></tr><tr><td>1</td><td>1</td><td>"controller transmitter"</td></tr></table> | MST | TRX        | Operating Modes | 0 | x | "target receiver" | 0     | x | "target transmitter" | 1    | 0 | "controller receiver" | 1 | 1                     | "controller transmitter" |   |   |                  |               |
| MST | TRX   | Operating Modes          |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                                                                                                                                                                                                                                                                    |     |            |                 |   |   |                   |       |   |                      |      |   |                       |   |                       |                          |   |   |                  |               |
| 0   | x     | "target receiver"        |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                                                                                                                                                                                                                                                                    |     |            |                 |   |   |                   |       |   |                      |      |   |                       |   |                       |                          |   |   |                  |               |
| 0   | x     | "target transmitter"     |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                                                                                                                                                                                                                                                                    |     |            |                 |   |   |                   |       |   |                      |      |   |                       |   |                       |                          |   |   |                  |               |
| 1   | 0     | "controller receiver"    |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                                                                                                                                                                                                                                                                    |     |            |                 |   |   |                   |       |   |                      |      |   |                       |   |                       |                          |   |   |                  |               |
| 1   | 1     | "controller transmitter" |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                                                                                                                                                                                                                                                                    |     |            |                 |   |   |                   |       |   |                      |      |   |                       |   |                       |                          |   |   |                  |               |
| 8   | XA    | R/W                      | 0h              | Expanded Address. XA<br>0:[default] 7-bit address mode [normal address mode]. XA<br>1:10-bit address mode [expanded address mode] Please note that XA needs to be configured even if the I2C is in target mode.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                                                                                                                                                                                                                                                                    |     |            |                 |   |   |                   |       |   |                      |      |   |                       |   |                       |                          |   |   |                  |               |

**Table 5-1882. I2C\_ICMDR Register Field Descriptions (continued)**

| Bit | Field       | Type | Reset                               | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |          |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
|-----|-------------|------|-------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|-----|-----|------------------|------------------|------|---|------------------------|---------------|---------------|------|------------------------------------|---|---|---|-------------------------------------|---|----|---|-----------------------------|---|-----------|---------------|--------------------------------|---|---|---|---------------------------------|-----------------|----------|---|------------------------------------|---|------|------|----|---|---|---|------|---|----|---|---|---|-----------|----------|--|-----|--|--|------------|--|--|---|---|---|----------|------|----|
| 7   | RM          | R/W  | 0h                                  | <p>Repeat Mode. This bit is set to a"1" by the CPU to put the I2C in the repeat mode. In this mode data is continuously transmitted out of the ICDXR until the STP bit is set to"1" regardless of ICCNT value. This bit is don't care if the I2C is configured in target mode.</p> <table><tr><td>RM</td><td>STT</td><td>STP</td><td>Conditions</td><td>Bus Activities</td><td>Mode</td></tr><tr><td>0</td><td>0</td><td>0</td><td>Idle</td><td>None</td><td>NA</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Stop</td><td>P</td><td>NA</td></tr><tr><td>0</td><td>1</td><td>0</td><td>[Re]Start</td><td>S-A-D..[n]..D</td><td>Repeat n</td></tr><tr><td>0</td><td>1</td><td>1</td><td>[Re]Start-Stop</td><td>S-A-D..[n]..D-P</td><td>Repeat n</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Idle</td><td>none</td><td>NA</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Stop</td><td>P</td><td>NA</td></tr><tr><td>1</td><td>1</td><td>0</td><td>[Re]Start</td><td>S-A-D-D-</td><td></td></tr><tr><td>D..</td><td></td><td></td><td>Continuous</td><td></td><td></td></tr><tr><td>1</td><td>1</td><td>1</td><td>Reserved</td><td>None</td><td>NA</td></tr></table> | RM       | STT | STP | Conditions       | Bus Activities   | Mode | 0 | 0                      | 0             | Idle          | None | NA                                 | 0 | 0 | 1 | Stop                                | P | NA | 0 | 1                           | 0 | [Re]Start | S-A-D..[n]..D | Repeat n                       | 0 | 1 | 1 | [Re]Start-Stop                  | S-A-D..[n]..D-P | Repeat n | 1 | 0                                  | 0 | Idle | none | NA | 1 | 0 | 1 | Stop | P | NA | 1 | 1 | 0 | [Re]Start | S-A-D-D- |  | D.. |  |  | Continuous |  |  | 1 | 1 | 1 | Reserved | None | NA |
| RM  | STT         | STP  | Conditions                          | Bus Activities                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Mode     |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 0   | 0           | 0    | Idle                                | None                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | NA       |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 0   | 0           | 1    | Stop                                | P                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | NA       |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 0   | 1           | 0    | [Re]Start                           | S-A-D..[n]..D                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Repeat n |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 0   | 1           | 1    | [Re]Start-Stop                      | S-A-D..[n]..D-P                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Repeat n |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 1   | 0           | 0    | Idle                                | none                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | NA       |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 1   | 0           | 1    | Stop                                | P                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | NA       |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 1   | 1           | 0    | [Re]Start                           | S-A-D-D-                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |          |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| D.. |             |      | Continuous                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |          |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 1   | 1           | 1    | Reserved                            | None                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | NA       |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 6   | DLB         | R/W  | 0h                                  | Digital Loop Back [in controller transmit mode only]. This bit is set to a"1" by the CPU to put the I2C in the loop back mode. In this mode data transmitted out of the ICDXR will be received in the ICDRR after [[CPU freq/I2C freq]8] CPU cycles via an internal path. The address of the ICOAR is output on SDA.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |          |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 5   | IRS         | R/W  | 0h                                  | I2C Reset Not. This can be set to a"0" by the CPU to put the I2C in reset or to a"1" to take the I2C out of reset. When this bit is reset to 0 all status bits in ICSTR and ICIVR are set to default values. Note that if this bit is reset during a transfer it can cause the I2C bus hang [SDA and SCL are tri-stated].                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |          |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 4   | STB         | R/W  | 0h                                  | Start Byte [Controller only mode]. The Start Byte mode bit is set to 1 by the CPU to configure the I2C in Start byte mode the I2C sends "00000001" regardless ICSAR value. Refer to the Philip I2C spec for more details.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |          |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 3   | FDF         | R/W  | 0h                                  | <p>Free Data Format.<br/>This bit can be set to"1" by the CPU to configure the I2C in Free Data Format mode.</p> <table><tr><td>FDF</td><td>MST</td><td>TRX</td><td>Operating mode</td></tr><tr><td>0</td><td>0</td><td>x</td><td>Target in non FDF mode</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Controller receive in non FDF mode</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Controller transmit in non FDF mode</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Target receiver in FDF mode</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Target transmitter in FDF mode</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Controller receiver in FDF mode</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Controller transmitter in FDF mode</td></tr></table>                                                                                                                                                                                                                                                                                                                                                                                             | FDF      | MST | TRX | Operating mode   | 0                | 0    | x | Target in non FDF mode | 0             | 1             | 0    | Controller receive in non FDF mode | 0 | 1 | 1 | Controller transmit in non FDF mode | 1 | 0  | 0 | Target receiver in FDF mode | 1 | 0         | 1             | Target transmitter in FDF mode | 1 | 1 | 0 | Controller receiver in FDF mode | 1               | 1        | 1 | Controller transmitter in FDF mode |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| FDF | MST         | TRX  | Operating mode                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |          |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 0   | 0           | x    | Target in non FDF mode              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |          |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 0   | 1           | 0    | Controller receive in non FDF mode  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |          |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 0   | 1           | 1    | Controller transmit in non FDF mode |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |          |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 1   | 0           | 0    | Target receiver in FDF mode         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |          |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 1   | 0           | 1    | Target transmitter in FDF mode      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |          |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 1   | 1           | 0    | Controller receiver in FDF mode     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |          |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 1   | 1           | 1    | Controller transmitter in FDF mode  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |          |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 2:0 | BC2_BC1_BC0 | R/W  | 0h                                  | <p>Bit Count : Bit Count 2, Bit Count 1 and Bit Count 0 define the number of bits starting from the lsb [excluding the acknowledge bit] of the next byte which are yet to be received or transmitted.</p> <table><tr><td>BC2</td><td>BC1</td><td>BC0</td><td>Bits/byte in FDF</td><td>Bits/byte w/ ACK</td></tr><tr><td>0</td><td>0</td><td>1</td><td>NA [reserved]</td><td>NA [reserved]</td></tr><tr><td>0</td><td>1</td><td>0</td><td>2</td><td>3</td></tr><tr><td>0</td><td>1</td><td>1</td><td>3</td><td>4</td></tr><tr><td>1</td><td>0</td><td>0</td><td>4</td><td>5</td></tr><tr><td>1</td><td>0</td><td>1</td><td>5</td><td>6</td></tr><tr><td>1</td><td>1</td><td>0</td><td>6</td><td>7</td></tr><tr><td>1</td><td>1</td><td>1</td><td>7</td><td>8</td></tr><tr><td>0</td><td>0</td><td>0</td><td>8</td><td>9</td></tr></table>                                                                                                                                                                                                                                                                                                                              | BC2      | BC1 | BC0 | Bits/byte in FDF | Bits/byte w/ ACK | 0    | 0 | 1                      | NA [reserved] | NA [reserved] | 0    | 1                                  | 0 | 2 | 3 | 0                                   | 1 | 1  | 3 | 4                           | 1 | 0         | 0             | 4                              | 5 | 1 | 0 | 1                               | 5               | 6        | 1 | 1                                  | 0 | 6    | 7    | 1  | 1 | 1 | 7 | 8    | 0 | 0  | 0 | 8 | 9 |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| BC2 | BC1         | BC0  | Bits/byte in FDF                    | Bits/byte w/ ACK                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |          |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 0   | 0           | 1    | NA [reserved]                       | NA [reserved]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |          |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 0   | 1           | 0    | 2                                   | 3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |          |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 0   | 1           | 1    | 3                                   | 4                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |          |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 1   | 0           | 0    | 4                                   | 5                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |          |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 1   | 0           | 1    | 5                                   | 6                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |          |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 1   | 1           | 0    | 6                                   | 7                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |          |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 1   | 1           | 1    | 7                                   | 8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |          |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |
| 0   | 0           | 0    | 8                                   | 9                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |          |     |     |                  |                  |      |   |                        |               |               |      |                                    |   |   |   |                                     |   |    |   |                             |   |           |               |                                |   |   |   |                                 |                 |          |   |                                    |   |      |      |    |   |   |   |      |   |    |   |   |   |           |          |  |     |  |  |            |  |  |   |   |   |          |      |    |

### 5.10.2.11 I2C\_ICIVR Register

#### 1 I2C\_ICIVR Register (Offset = 28h) [reset = 0h]

I2C Interrupt Vector register

Return to [Summary Table](#)

**Table 5-1883. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| I2C0          | 5250 0028h       |
| I2C1          | 5250 1028h       |
| I2C2          | 5250 2028h       |
| I2C3          | 5250 3028h       |

**Figure 5-624. I2C\_ICIVR Name Register**

|     |    |    |    |         |    |    |    |
|-----|----|----|----|---------|----|----|----|
| 31  | 30 | 29 | 28 | 27      | 26 | 25 | 24 |
| NU2 |    |    |    |         |    |    |    |
| NU2 |    |    |    |         |    |    |    |
| 0h  |    |    |    |         |    |    |    |
| 23  | 22 | 21 | 20 | 19      | 18 | 17 | 16 |
| NU2 |    |    |    |         |    |    |    |
| NU2 |    |    |    |         |    |    |    |
| 0h  |    |    |    |         |    |    |    |
| 15  | 14 | 13 | 12 | 11      | 10 | 9  | 8  |
| NU2 |    |    |    | TESTMD  |    |    |    |
| NU2 |    |    |    | R/W     |    |    |    |
| 0h  |    |    |    | 0h      |    |    |    |
| 7   | 6  | 5  | 4  | 3       | 2  | 1  | 0  |
| NU1 |    |    |    | INTCODE |    |    |    |
| NU1 |    |    |    | R/W     |    |    |    |
| 0h  |    |    |    | 0h      |    |    |    |

**Table 5-1885. I2C\_ICIVR Register Field Descriptions**

| Bit   | Field  | Type | Reset | Description                    |
|-------|--------|------|-------|--------------------------------|
| 31:12 | NU2    | NU2  | 0h    | Reserved.                      |
| 11:8  | TESTMD | R/W  | 0h    | Reserved for internal testing. |
| 7:3   | NU1    | NU1  | 0h    | Reserved.                      |

**Table 5-1885. I2C\_ICIVR Register Field Descriptions (continued)**

| Bit                     | Field                           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                |                    |                |      |                         |                            |      |                              |      |                                 |      |                              |      |                               |      |                          |                        |                          |
|-------------------------|---------------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|--------------------|----------------|------|-------------------------|----------------------------|------|------------------------------|------|---------------------------------|------|------------------------------|------|-------------------------------|------|--------------------------|------------------------|--------------------------|
| 2:0                     | INTCODE                         | R/W  | 0h    | <p>Interrupt code. The binary-coded-interrupt vector indicates which interrupt has occurred. Reading the ICIVR clears the interrupt code except ARDY[011] RRDY[100] and XRDY[101]. Interrupt code for ARDY RRDY and XRDY is cleared when ARDY ICRRDY and ICXRDY bits in the ICSTR is cleared to default value respectively. If other interrupts are pending a new interrupt is generated. If there are more than one interrupt flag Reading the ICIVR clears the highest priority interrupt code. Reading the ICIVR also clears corresponding status bit in the ICSTR except ARDY ICRRDY ICXRDY and AAS. Note that users must read [clear] the ICIVR before doing another start otherwise the ICIVR could contain incorrect [old interrupt flags] value.</p> <table><tr><td>Interrupt Code</td><td>Interrupt Occurred</td></tr><tr><td>_000_[default]</td><td>None</td></tr><tr><td>_001_[highest priority]</td><td>Arbitration Lost interrupt</td></tr><tr><td>_010</td><td>No Acknowledgement interrupt</td></tr><tr><td>_011</td><td>Register Access Ready interrupt</td></tr><tr><td>_100</td><td>Receive Data Ready interrupt</td></tr><tr><td>_101</td><td>Transmit Data Ready interrupt</td></tr><tr><td>_110</td><td>Stop Condition Detection</td></tr><tr><td>_111_[lowest priority]</td><td>Address As Target - [RW]</td></tr></table> | Interrupt Code | Interrupt Occurred | _000_[default] | None | _001_[highest priority] | Arbitration Lost interrupt | _010 | No Acknowledgement interrupt | _011 | Register Access Ready interrupt | _100 | Receive Data Ready interrupt | _101 | Transmit Data Ready interrupt | _110 | Stop Condition Detection | _111_[lowest priority] | Address As Target - [RW] |
| Interrupt Code          | Interrupt Occurred              |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                |                    |                |      |                         |                            |      |                              |      |                                 |      |                              |      |                               |      |                          |                        |                          |
| _000_[default]          | None                            |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                |                    |                |      |                         |                            |      |                              |      |                                 |      |                              |      |                               |      |                          |                        |                          |
| _001_[highest priority] | Arbitration Lost interrupt      |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                |                    |                |      |                         |                            |      |                              |      |                                 |      |                              |      |                               |      |                          |                        |                          |
| _010                    | No Acknowledgement interrupt    |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                |                    |                |      |                         |                            |      |                              |      |                                 |      |                              |      |                               |      |                          |                        |                          |
| _011                    | Register Access Ready interrupt |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                |                    |                |      |                         |                            |      |                              |      |                                 |      |                              |      |                               |      |                          |                        |                          |
| _100                    | Receive Data Ready interrupt    |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                |                    |                |      |                         |                            |      |                              |      |                                 |      |                              |      |                               |      |                          |                        |                          |
| _101                    | Transmit Data Ready interrupt   |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                |                    |                |      |                         |                            |      |                              |      |                                 |      |                              |      |                               |      |                          |                        |                          |
| _110                    | Stop Condition Detection        |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                |                    |                |      |                         |                            |      |                              |      |                                 |      |                              |      |                               |      |                          |                        |                          |
| _111_[lowest priority]  | Address As Target - [RW]        |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                |                    |                |      |                         |                            |      |                              |      |                                 |      |                              |      |                               |      |                          |                        |                          |



### 5.10.2.12 I2C\_ICEMDR Register

#### 1 I2C\_ICEMDR Register (Offset = 2Ch) [reset = 0h]

I2C Extended Mode register

Return to [Summary Table](#)
**Table 5-1886. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| I2C0          | 5250 002Ch       |
| I2C1          | 5250 102Ch       |
| I2C2          | 5250 202Ch       |
| I2C3          | 5250 302Ch       |

**Figure 5-625. I2C\_ICEMDR Name Register**

|     |    |    |    |    |    |        |     |
|-----|----|----|----|----|----|--------|-----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25     | 24  |
| NU  |    |    |    |    |    |        |     |
| R/W |    |    |    |    |    |        |     |
| 0h  |    |    |    |    |    |        |     |
| 23  | 22 | 21 | 20 | 19 | 18 | 17     | 16  |
| NU  |    |    |    |    |    |        |     |
| R/W |    |    |    |    |    |        |     |
| 0h  |    |    |    |    |    |        |     |
| 15  | 14 | 13 | 12 | 11 | 10 | 9      | 8   |
| NU  |    |    |    |    |    |        |     |
| R/W |    |    |    |    |    |        |     |
| 0h  |    |    |    |    |    |        |     |
| 7   | 6  | 5  | 4  | 3  | 2  | 1      | 0   |
| NU  |    |    |    |    |    | IGNACK | BCM |
| R/W |    |    |    |    |    | R/W    | R/W |
| 0h  |    |    |    |    |    | 0h     | 0h  |

**Table 5-1888. I2C\_ICEMDR Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                     |
|------|--------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | NU     | R/W  | 0h    | Reserved. - [RW ]                                                                                                                                                                                                                                                               |
| 1    | IGNACK | R/W  | 0h    | Ignore NACK mode IGNACK=0 The controller transmitter will operate normally discontinue the data transfer and set the ARDY and NACK status bits when a NACK signal is received from the target. IGNACK=1 The controller transmitter will ignore a NACK received from the target. |
| 0    | BCM    | R/W  | 0h    | Backward Compatibility Mode. This bit affects the I2C interrupt behavior. Refer to appendix A for details.                                                                                                                                                                      |

### 5.10.2.13 I2C\_ICPSC Register

#### 1 I2C\_ICPSC Register (Offset = 30h) [reset = 0h]

I2C Prescaler register

Return to [Summary Table](#)

**Table 5-1889. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| I2C0          | 5250 0030h       |
| I2C1          | 5250 1030h       |
| I2C2          | 5250 2030h       |
| I2C3          | 5250 3030h       |

**Figure 5-626. I2C\_ICPSC Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| NU          |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| NU          |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| NU          |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| IPSC7_IPSC0 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-1891. I2C\_ICPSC Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                                                                                   |
|------|-------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | NU          | R/W  | 0h    | Reserved.                                                                                                                                                                                                                     |
| 7:0  | IPSC7_IPSC0 | R/W  | 0h    | 8-bit prescaler to divide the system clock down to 4/8/12Mhz clock and used by the I2C module. This register must be initialized while the I2C is still in reset [IRS_=0]. The value takes effect on the rising edge of IRS_. |

### 5.10.2.14 I2C\_ICPID1 Register

#### 1 I2C\_ICPID1 Register (Offset = 34h) [reset = 0h]

I2C Peripheral ID register 1

Return to [Summary Table](#)

**Table 5-1892. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| I2C0          | 5250 0034h       |
| I2C1          | 5250 1034h       |
| I2C2          | 5250 2034h       |
| I2C3          | 5250 3034h       |

**Figure 5-627. I2C\_ICPID1 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| NU       |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| NU       |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CLASS    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| REVISION |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-1894. I2C\_ICPID1 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                         |
|-------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:16 | NU       | R/W  | 0h    | Reserved.                                                                                                           |
| 15:8  | CLASS    | R/W  | 0h    | Identifies the class of peripheral. This value should be 0x01 - [RW ]                                               |
| 7:0   | REVISION | R/W  | 0h    | Identifies the revision level of the I2C. This value should be incremented each time the design is revised. - [RW ] |

### 5.10.2.15 I2C\_ICPID2 Register

#### 1 I2C\_ICPID2 Register (Offset = 38h) [reset = 0h]

I2C Peripheral ID register 2

Return to [Summary Table](#)

**Table 5-1895. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| I2C0          | 5250 0038h       |
| I2C1          | 5250 1038h       |
| I2C2          | 5250 2038h       |
| I2C3          | 5250 3038h       |

**Figure 5-628. I2C\_ICPID2 Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| NU   |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| NU   |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| NU   |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TYPE |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-1897. I2C\_ICPID2 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                          |
|------|-------|------|-------|----------------------------------------------------------------------|
| 31:8 | NU    | R/W  | 0h    | Reserved.                                                            |
| 7:0  | TYPE  | R/W  | 0h    | Identifies the type of peripheral. This value should be 0x05 - [RW ] |

### 5.10.2.16 I2C\_ICDMAC Register

#### 1 I2C\_ICDMAC Register (Offset = 3Ch) [reset = 0h]

I2C DMA Control Register

Return to [Summary Table](#)
**Table 5-1898. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| I2C0          | 5250 003Ch       |
| I2C1          | 5250 103Ch       |
| I2C2          | 5250 203Ch       |
| I2C3          | 5250 303Ch       |

**Figure 5-629. I2C\_ICDMAC Name Register**

|     |    |    |    |    |    |         |         |
|-----|----|----|----|----|----|---------|---------|
| 31  | 30 | 29 | 28 | 27 | 26 | 25      | 24      |
| NU  |    |    |    |    |    |         |         |
| R/W |    |    |    |    |    |         |         |
| 0h  |    |    |    |    |    |         |         |
| 23  | 22 | 21 | 20 | 19 | 18 | 17      | 16      |
| NU  |    |    |    |    |    |         |         |
| R/W |    |    |    |    |    |         |         |
| 0h  |    |    |    |    |    |         |         |
| 15  | 14 | 13 | 12 | 11 | 10 | 9       | 8       |
| NU  |    |    |    |    |    |         |         |
| R/W |    |    |    |    |    |         |         |
| 0h  |    |    |    |    |    |         |         |
| 7   | 6  | 5  | 4  | 3  | 2  | 1       | 0       |
| NU  |    |    |    |    |    | TXDMAEN | RXDMAEN |
| R/W |    |    |    |    |    | R/W     | R/W     |
| 0h  |    |    |    |    |    | 0h      | 0h      |

**Table 5-1900. I2C\_ICDMAC Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                  |
|------|---------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | NU      | R/W  | 0h    | Reserved. - [RW ]                                                                                                                                                                                                                                                                                                                                            |
| 1    | TXDMAEN | R/W  | 0h    | Transmit DMA enable. This bit controls the receive DMA event pin to the system. When this bit is 1 the DMA event is enabled and ICTEVT_POR pin is asserted when the DMA transfer is required. When this bit is 0 the ICTEVT_POR pin is never asserted.<br>RXDMAEN<br>0:DMA transmit event is disabled. RXDMAEN<br>1:DMA transmit event is enabled. [Default] |
| 0    | RXDMAEN | R/W  | 0h    | Receive DMA enable. This bit controls the receive DMA event pin to the system. When this bit is 1 the DMA event is enabled and ICREVT_POR pin is asserted when the DMA transfer is required. When this bit is 0 the ICREVT_POR pin is never asserted.<br>RXDMAEN<br>0:DMA receive event is disabled. RXDMAEN<br>1:DMA receive event is enabled. [Default]    |

### 5.10.2.17 I2C\_ICPFUNC Register

#### 1 I2C\_ICPFUNC Register (Offset = 48h) [reset = 0h]

I2C Pin Function register

Return to [Summary Table](#)
**Table 5-1901. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| I2C0          | 5250 0048h       |
| I2C1          | 5250 1048h       |
| I2C2          | 5250 2048h       |
| I2C3          | 5250 3048h       |

**Figure 5-630. I2C\_ICPFUNC Name Register**

|     |    |    |    |    |    |    |        |
|-----|----|----|----|----|----|----|--------|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24     |
| NU  |    |    |    |    |    |    |        |
| R/W |    |    |    |    |    |    |        |
| 0h  |    |    |    |    |    |    |        |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16     |
| NU  |    |    |    |    |    |    |        |
| R/W |    |    |    |    |    |    |        |
| 0h  |    |    |    |    |    |    |        |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8      |
| NU  |    |    |    |    |    |    |        |
| R/W |    |    |    |    |    |    |        |
| 0h  |    |    |    |    |    |    |        |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0      |
| NU  |    |    |    |    |    |    | PFUNC0 |
| R/W |    |    |    |    |    |    | R/W    |
| 0h  |    |    |    |    |    |    | 0h     |

**Table 5-1903. I2C\_ICPFUNC Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|--------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | NU     | R/W  | 0h    | Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 0    | PFUNC0 | R/W  | 0h    | Controls the function of the I2C SCL and SDA pins. 0 = Pins function as SCL and SDA 1 = Pins functions as GPIO Note: No hardware protection is required to disable I2C function when the PFUNC[0] and IRS_ bits are both set to one. When PFUNC[0] is "1" [GPIO mode] the sub-module which controls the I2C function receives the value "1" for SCL and SDA. IRS_ can be set to "1" regardless of PFUNC[0] and the I2C function works whenever the IRS_ bit is "1". The user is expected to hold I2C in reset via IRS_ bit when changing to/from GPIO mode via the PFUNC[0] bit. |

### 5.10.2.18 I2C\_ICPDIR Register

#### 1 I2C\_ICPDIR Register (Offset = 4Ch) [reset = 0h]

I2C Pin Direction register

Return to [Summary Table](#)
**Table 5-1904. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| I2C0          | 5250 004Ch       |
| I2C1          | 5250 104Ch       |
| I2C2          | 5250 204Ch       |
| I2C3          | 5250 304Ch       |

**Figure 5-631. I2C\_ICPDIR Name Register**

|     |    |    |    |    |    |       |       |
|-----|----|----|----|----|----|-------|-------|
| 31  | 30 | 29 | 28 | 27 | 26 | 25    | 24    |
| NU  |    |    |    |    |    |       |       |
| R/W |    |    |    |    |    |       |       |
| 0h  |    |    |    |    |    |       |       |
| 23  | 22 | 21 | 20 | 19 | 18 | 17    | 16    |
| NU  |    |    |    |    |    |       |       |
| R/W |    |    |    |    |    |       |       |
| 0h  |    |    |    |    |    |       |       |
| 15  | 14 | 13 | 12 | 11 | 10 | 9     | 8     |
| NU  |    |    |    |    |    |       |       |
| R/W |    |    |    |    |    |       |       |
| 0h  |    |    |    |    |    |       |       |
| 7   | 6  | 5  | 4  | 3  | 2  | 1     | 0     |
| NU  |    |    |    |    |    | PDIR1 | PDIR0 |
| R/W |    |    |    |    |    | R/W   | R/W   |
| 0h  |    |    |    |    |    | 0h    | 0h    |

**Table 5-1906. I2C\_ICPDIR Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                          |
|------|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | NU    | R/W  | 0h    | Reserved                                                                                                                             |
| 1    | PDIR1 | R/W  | 0h    | Controls the direction of the I2C SDA pin when configured as GPIO.<br>0 = SDA pin functions as input 1 = SDA pin functions as output |
| 0    | PDIR0 | R/W  | 0h    | Controls the direction of the I2C SCL pin when configured as GPIO.<br>0 = SCL pin functions as input 1 = SCL pin functions as output |

### 5.10.2.19 I2C\_ICPDIN Register

#### 1 I2C\_ICPDIN Register (Offset = 50h) [reset = 0h]

I2C Pin Data In register

Return to [Summary Table](#)
**Table 5-1907. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| I2C0          | 5250 0050h       |
| I2C1          | 5250 1050h       |
| I2C2          | 5250 2050h       |
| I2C3          | 5250 3050h       |

**Figure 5-632. I2C\_ICPDIN Name Register**

|     |    |    |    |    |    |       |       |
|-----|----|----|----|----|----|-------|-------|
| 31  | 30 | 29 | 28 | 27 | 26 | 25    | 24    |
| NU  |    |    |    |    |    |       |       |
| R/W |    |    |    |    |    |       |       |
| 0h  |    |    |    |    |    |       |       |
| 23  | 22 | 21 | 20 | 19 | 18 | 17    | 16    |
| NU  |    |    |    |    |    |       |       |
| R/W |    |    |    |    |    |       |       |
| 0h  |    |    |    |    |    |       |       |
| 15  | 14 | 13 | 12 | 11 | 10 | 9     | 8     |
| NU  |    |    |    |    |    |       |       |
| R/W |    |    |    |    |    |       |       |
| 0h  |    |    |    |    |    |       |       |
| 7   | 6  | 5  | 4  | 3  | 2  | 1     | 0     |
| NU  |    |    |    |    |    | PDIN1 | PDIN0 |
| R/W |    |    |    |    |    | R/W   | R/W   |
| 0h  |    |    |    |    |    | 0h    | 0h    |

**Table 5-1909. I2C\_ICPDIN Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                 |
|------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | NU    | R/W  | 0h    | Reserved                                                                                                                                                                                                                    |
| 1    | PDIN1 | R/W  | 0h    | Indicates the logic level present on the SDA pin. Reads: 0 = Logic low present at SDA pin regardless of PFUNC setting. 1 = Logic high present at SDA pin regardless of PFUNC setting. Writes: Writes have no effect. - [RW] |
| 0    | PDIN0 | R/W  | 0h    | Indicates the logic level present on the SCL pin. Reads: 0 = Logic low present at SCL pin regardless of PFUNC setting. 1 = Logic high present at SCL pin regardless of PFUNC setting. Writes: Writes have no effect - [RW]  |



### 5.10.2.20 I2C\_ICPDOUT Register

#### 1 I2C\_ICPDOUT Register (Offset = 54h) [reset = 0h]

I2C Pin Data Out register

Return to [Summary Table](#)
**Table 5-1910. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| I2C0          | 5250 0054h       |
| I2C1          | 5250 1054h       |
| I2C2          | 5250 2054h       |
| I2C3          | 5250 3054h       |

**Figure 5-633. I2C\_ICPDOUT Name Register**

|     |    |    |    |    |    |        |        |
|-----|----|----|----|----|----|--------|--------|
| 31  | 30 | 29 | 28 | 27 | 26 | 25     | 24     |
| NU  |    |    |    |    |    |        |        |
| R/W |    |    |    |    |    |        |        |
| 0h  |    |    |    |    |    |        |        |
| 23  | 22 | 21 | 20 | 19 | 18 | 17     | 16     |
| NU  |    |    |    |    |    |        |        |
| R/W |    |    |    |    |    |        |        |
| 0h  |    |    |    |    |    |        |        |
| 15  | 14 | 13 | 12 | 11 | 10 | 9      | 8      |
| NU  |    |    |    |    |    |        |        |
| R/W |    |    |    |    |    |        |        |
| 0h  |    |    |    |    |    |        |        |
| 7   | 6  | 5  | 4  | 3  | 2  | 1      | 0      |
| NU  |    |    |    |    |    | PDOUT1 | PDOUT0 |
| R/W |    |    |    |    |    | R/W    | R/W    |
| 0h  |    |    |    |    |    | 0h     | 0h     |

**Table 5-1912. I2C\_ICPDOUT Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                     |
|------|--------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | NU     | R/W  | 0h    | Reserved                                                                                                                                                                                                                                                                                        |
| 1    | PDOUT1 | R/W  | 0h    | Controls the level driven on the SDA pin when configured as GPIO output. Reads: Reads return register values not GPIO pin levels. Writes: 0 = SDA pin driven low 1 = SDA pin driven high. Note: If SDA is connected to an open-drain buffer at the chip level the I2C cannot drive SDA to high. |
| 0    | PDOUT0 | R/W  | 0h    | Controls the level driven on the SCL pin when configured as GPIO output. Reads: Reads return register values not GPIO pin levels. Writes: 0 = SCL pin driven low 1 = SCL pin driven high Note: If SCL is connected to an open-drain buffer at the chip level the I2C cannot drive SCL to high.  |

### 5.10.2.21 I2C\_ICPDSET Register

#### 1 I2C\_ICPDSET Register (Offset = 58h) [reset = 0h]

I2C Pin Data Set register

Return to [Summary Table](#)
**Table 5-1913. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| I2C0          | 5250 0058h       |
| I2C1          | 5250 1058h       |
| I2C2          | 5250 2058h       |
| I2C3          | 5250 3058h       |

**Figure 5-634. I2C\_ICPDSET Name Register**

|     |    |    |    |    |    |        |        |
|-----|----|----|----|----|----|--------|--------|
| 31  | 30 | 29 | 28 | 27 | 26 | 25     | 24     |
| NU  |    |    |    |    |    |        |        |
| R/W |    |    |    |    |    |        |        |
| 0h  |    |    |    |    |    |        |        |
| 23  | 22 | 21 | 20 | 19 | 18 | 17     | 16     |
| NU  |    |    |    |    |    |        |        |
| R/W |    |    |    |    |    |        |        |
| 0h  |    |    |    |    |    |        |        |
| 15  | 14 | 13 | 12 | 11 | 10 | 9      | 8      |
| NU  |    |    |    |    |    |        |        |
| R/W |    |    |    |    |    |        |        |
| 0h  |    |    |    |    |    |        |        |
| 7   | 6  | 5  | 4  | 3  | 2  | 1      | 0      |
| NU  |    |    |    |    |    | PDSET1 | PDSET0 |
| R/W |    |    |    |    |    | R/W    | R/W    |
| 0h  |    |    |    |    |    | 0h     | 0h     |

**Table 5-1915. I2C\_ICPDSET Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                                                                                                       |
|------|--------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | NU     | R/W  | 0h    | Reserved                                                                                                                                                                                                          |
| 1    | PDSET1 | R/W  | 0h    | Used to set PDOUT[1] bit which corresponds to the SDA GPIO pin. Reads: Reads should return 0. User documentation should say reads are indeterminate. Writes: 0 = no effect 1 = PDOUT[1] bit is set to logic high. |
| 0    | PDSET0 | R/W  | 0h    | Used to set PDOUT[0] bit which corresponds to the SCL GPIO pin. Reads: Reads should return 0. User documentation should say reads are indeterminate. Writes: 0 = no effect 1 = PDOUT[0] bit is set to logic high. |

### 5.10.2.22 I2C\_ICPDCLR Register

#### 1 I2C\_ICPDCLR Register (Offset = 5Ch) [reset = 0h]

I2C Pin Data Clear register

Return to [Summary Table](#)

**Table 5-1916. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| I2C0          | 5250 005Ch       |
| I2C1          | 5250 105Ch       |
| I2C2          | 5250 205Ch       |
| I2C3          | 5250 305Ch       |

**Figure 5-635. I2C\_ICPDCLR Name Register**

|     |    |    |    |    |    |        |        |
|-----|----|----|----|----|----|--------|--------|
| 31  | 30 | 29 | 28 | 27 | 26 | 25     | 24     |
| NU  |    |    |    |    |    |        |        |
| R/W |    |    |    |    |    |        |        |
| 0h  |    |    |    |    |    |        |        |
| 23  | 22 | 21 | 20 | 19 | 18 | 17     | 16     |
| NU  |    |    |    |    |    |        |        |
| R/W |    |    |    |    |    |        |        |
| 0h  |    |    |    |    |    |        |        |
| 15  | 14 | 13 | 12 | 11 | 10 | 9      | 8      |
| NU  |    |    |    |    |    |        |        |
| R/W |    |    |    |    |    |        |        |
| 0h  |    |    |    |    |    |        |        |
| 7   | 6  | 5  | 4  | 3  | 2  | 1      | 0      |
| NU  |    |    |    |    |    | PDCLR1 | PDCLR0 |
| R/W |    |    |    |    |    | R/W    | R/W    |
| 0h  |    |    |    |    |    | 0h     | 0h     |

**Table 5-1918. I2C\_ICPDCLR Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                                                                                                       |
|------|--------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | NU     | R/W  | 0h    | Reserved                                                                                                                                                                                                          |
| 1    | PDCLR1 | R/W  | 0h    | Used to clear PDOUT[1] bit which corresponds to the SDA pin. Reads: Reads should return 0. User documentation should say reads are indeterminate. Writes: 0 = no effect 1 = PDOUT[1] bit is cleared to logic low. |
| 0    | PDCLR0 | R/W  | 0h    | Used to clear PDOUT[0] bit which corresponds to the SCL pin. Reads: Reads should return 0. User documentation should say reads are indeterminate. Writes: 0 = no effect 1 = PDOUT[0] bit is cleared to logic low. |

### 5.10.2.23 I2C\_ICPDRV Register

#### 1 I2C\_ICPDRV Register (Offset = 60h) [reset = 0h]

I2C Pin Driver Mode Register

Return to [Summary Table](#)
**Table 5-1919. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| I2C0          | 5250 0060h       |
| I2C1          | 5250 1060h       |
| I2C2          | 5250 2060h       |
| I2C3          | 5250 3060h       |

**Figure 5-636. I2C\_ICPDRV Name Register**

|     |    |    |    |    |    |       |       |
|-----|----|----|----|----|----|-------|-------|
| 31  | 30 | 29 | 28 | 27 | 26 | 25    | 24    |
| NU  |    |    |    |    |    |       |       |
| R/W |    |    |    |    |    |       |       |
| 0h  |    |    |    |    |    |       |       |
| 23  | 22 | 21 | 20 | 19 | 18 | 17    | 16    |
| NU  |    |    |    |    |    |       |       |
| R/W |    |    |    |    |    |       |       |
| 0h  |    |    |    |    |    |       |       |
| 15  | 14 | 13 | 12 | 11 | 10 | 9     | 8     |
| NU  |    |    |    |    |    |       |       |
| R/W |    |    |    |    |    |       |       |
| 0h  |    |    |    |    |    |       |       |
| 7   | 6  | 5  | 4  | 3  | 2  | 1     | 0     |
| NU  |    |    |    |    |    | PDRV1 | PDRV0 |
| R/W |    |    |    |    |    | R/W   | R/W   |
| 0h  |    |    |    |    |    | 0h    | 0h    |

**Table 5-1921. I2C\_ICPDRV Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                              |
|------|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | NU    | R/W  | 0h    | Reserved                                                                                                                                                                                                                 |
| 1    | PDRV1 | R/W  | 0h    | Used to select driver mode of output buffer for SDA pin. 0 = I2C mode. 1 = GPIO mode. Note: Value of this register is reflected on the PDRV_SDA_POR port. Actual function depends on I/O buffer and chip implementation. |
| 0    | PDRV0 | R/W  | 0h    | Used to select driver mode of output buffer for SCL pin. 0 = I2C mode. 1 = GPIO mode. Note: Value of this register is reflected on the PDRV_SCL_POR port. Actual function depends on I/O buffer and chip implementation. |

## 5.11 LIN

### LIN

#### 5.11.1 LIN Summaries

#### LIN Summaries

**Table 5-1922. LIN Registers, Base Address=5240 0000h, Length=256**

| Offset | Length | Register Name                       | LIN0 Physical Address | LIN1 Physical Address | LIN2 Physical Address |
|--------|--------|-------------------------------------|-----------------------|-----------------------|-----------------------|
| 0h     | 32     | <a href="#">LIN_SCIGCR0</a>         | 5240 0000h            | 5240 1000h            | 5240 2000h            |
| 4h     | 32     | <a href="#">LIN_SCIGCR1</a>         | 5240 0004h            | 5240 1004h            | 5240 2004h            |
| 8h     | 32     | <a href="#">LIN_SCIGCR2</a>         | 5240 0008h            | 5240 1008h            | 5240 2008h            |
| Ch     | 32     | <a href="#">LIN_SCISSETINT</a>      | 5240 000Ch            | 5240 100Ch            | 5240 200Ch            |
| 10h    | 32     | <a href="#">LIN_SCICLEARINT</a>     | 5240 0010h            | 5240 1010h            | 5240 2010h            |
| 14h    | 32     | <a href="#">LIN_SCISSETINTLV</a>    | 5240 0014h            | 5240 1014h            | 5240 2014h            |
| 18h    | 32     | <a href="#">LIN_SCICLEARINTLV</a>   | 5240 0018h            | 5240 1018h            | 5240 2018h            |
| 1Ch    | 32     | <a href="#">LIN_SCIFLR</a>          | 5240 001Ch            | 5240 101Ch            | 5240 201Ch            |
| 20h    | 32     | <a href="#">LIN_SCIINTVECT0</a>     | 5240 0020h            | 5240 1020h            | 5240 2020h            |
| 24h    | 32     | <a href="#">LIN_SCIINTVECT1</a>     | 5240 0024h            | 5240 1024h            | 5240 2024h            |
| 28h    | 32     | <a href="#">LIN_SCIFORMAT</a>       | 5240 0028h            | 5240 1028h            | 5240 2028h            |
| 2Ch    | 32     | <a href="#">LIN_BRSR</a>            | 5240 002Ch            | 5240 102Ch            | 5240 202Ch            |
| 30h    | 32     | <a href="#">LIN_SCIED</a>           | 5240 0030h            | 5240 1030h            | 5240 2030h            |
| 34h    | 32     | <a href="#">LIN_SCIRD</a>           | 5240 0034h            | 5240 1034h            | 5240 2034h            |
| 38h    | 32     | <a href="#">LIN_SCITD</a>           | 5240 0038h            | 5240 1038h            | 5240 2038h            |
| 3Ch    | 32     | <a href="#">LIN_SCIPIO0</a>         | 5240 003Ch            | 5240 103Ch            | 5240 203Ch            |
| 40h    | 32     | <a href="#">LIN_SCIPIO1</a>         | 5240 0040h            | 5240 1040h            | 5240 2040h            |
| 44h    | 32     | <a href="#">LIN_SCIPIO2</a>         | 5240 0044h            | 5240 1044h            | 5240 2044h            |
| 48h    | 32     | <a href="#">LIN_SCIPIO3</a>         | 5240 0048h            | 5240 1048h            | 5240 2048h            |
| 4Ch    | 32     | <a href="#">LIN_SCIPIO4</a>         | 5240 004Ch            | 5240 104Ch            | 5240 204Ch            |
| 50h    | 32     | <a href="#">LIN_SCIPIO5</a>         | 5240 0050h            | 5240 1050h            | 5240 2050h            |
| 54h    | 32     | <a href="#">LIN_SCIPIO6</a>         | 5240 0054h            | 5240 1054h            | 5240 2054h            |
| 58h    | 32     | <a href="#">LIN_SCIPIO7</a>         | 5240 0058h            | 5240 1058h            | 5240 2058h            |
| 5Ch    | 32     | <a href="#">LIN_SCIPIO8</a>         | 5240 005Ch            | 5240 105Ch            | 5240 205Ch            |
| 60h    | 32     | <a href="#">LIN_LINCOMP</a>         | 5240 0060h            | 5240 1060h            | 5240 2060h            |
| 64h    | 32     | <a href="#">LIN_LINRD0</a>          | 5240 0064h            | 5240 1064h            | 5240 2064h            |
| 68h    | 32     | <a href="#">LIN_LINRD1</a>          | 5240 0068h            | 5240 1068h            | 5240 2068h            |
| 6Ch    | 32     | <a href="#">LIN_LINMASK</a>         | 5240 006Ch            | 5240 106Ch            | 5240 206Ch            |
| 70h    | 32     | <a href="#">LIN_LINID</a>           | 5240 0070h            | 5240 1070h            | 5240 2070h            |
| 74h    | 32     | <a href="#">LIN_LINTD0</a>          | 5240 0074h            | 5240 1074h            | 5240 2074h            |
| 78h    | 32     | <a href="#">LIN_LINTD1</a>          | 5240 0078h            | 5240 1078h            | 5240 2078h            |
| 7Ch    | 32     | <a href="#">LIN_MBRSR</a>           | 5240 007Ch            | 5240 107Ch            | 5240 207Ch            |
| 80h    | 32     | <a href="#">LIN_RESERVED_1_J</a>    | 5240 0080h + formula  | 5240 1080h + formula  | 5240 2080h + formula  |
| 90h    | 32     | <a href="#">LIN_IODFTCTRL</a>       | 5240 0090h            | 5240 1090h            | 5240 2090h            |
| 94h    | 32     | <a href="#">LIN_RESERVED_2_J</a>    | 5240 0094h + formula  | 5240 1094h + formula  | 5240 2094h + formula  |
| E0h    | 32     | <a href="#">LIN_LIN_GLB_INT_EN</a>  | 5240 00E0h            | 5240 10E0h            | 5240 20E0h            |
| E4h    | 32     | <a href="#">LIN_LIN_GLB_INT_FLG</a> | 5240 00E4h            | 5240 10E4h            | 5240 20E4h            |

**Table 5-1922. LIN Registers, Base Address=5240 0000h, Length=256 (continued)**

| Offset | Length | Register Name                       | LIN0 Physical Address | LIN1 Physical Address | LIN2 Physical Address |
|--------|--------|-------------------------------------|-----------------------|-----------------------|-----------------------|
| E8h    | 32     | <a href="#">LIN_LIN_GLB_INT_CLR</a> | 5240 00E8h            | 5240 10E8h            | 5240 20E8h            |

**Table 5-1923. LIN Registers, Base Address=5240 0000h, Length=256**

| Offset | Length | Register Name                       | LIN3 Physical Address | LIN4 Physical Address |
|--------|--------|-------------------------------------|-----------------------|-----------------------|
| 0h     | 32     | <a href="#">LIN_SCIGCR0</a>         | 5240 3000h            | 5240 4000h            |
| 4h     | 32     | <a href="#">LIN_SCIGCR1</a>         | 5240 3004h            | 5240 4004h            |
| 8h     | 32     | <a href="#">LIN_SCIGCR2</a>         | 5240 3008h            | 5240 4008h            |
| Ch     | 32     | <a href="#">LIN_SCISSETINT</a>      | 5240 300Ch            | 5240 400Ch            |
| 10h    | 32     | <a href="#">LIN_SCISCLEARINT</a>    | 5240 3010h            | 5240 4010h            |
| 14h    | 32     | <a href="#">LIN_SCISSETINTLVL</a>   | 5240 3014h            | 5240 4014h            |
| 18h    | 32     | <a href="#">LIN_SCISCLEARINTLVL</a> | 5240 3018h            | 5240 4018h            |
| 1Ch    | 32     | <a href="#">LIN_SCIFLR</a>          | 5240 301Ch            | 5240 401Ch            |
| 20h    | 32     | <a href="#">LIN_SCIINTVECT0</a>     | 5240 3020h            | 5240 4020h            |
| 24h    | 32     | <a href="#">LIN_SCIINTVECT1</a>     | 5240 3024h            | 5240 4024h            |
| 28h    | 32     | <a href="#">LIN_SCIFORMAT</a>       | 5240 3028h            | 5240 4028h            |
| 2Ch    | 32     | <a href="#">LIN_BRSR</a>            | 5240 302Ch            | 5240 402Ch            |
| 30h    | 32     | <a href="#">LIN_SCIED</a>           | 5240 3030h            | 5240 4030h            |
| 34h    | 32     | <a href="#">LIN_SCIRD</a>           | 5240 3034h            | 5240 4034h            |
| 38h    | 32     | <a href="#">LIN_SCITD</a>           | 5240 3038h            | 5240 4038h            |
| 3Ch    | 32     | <a href="#">LIN_SCIPIO0</a>         | 5240 303Ch            | 5240 403Ch            |
| 40h    | 32     | <a href="#">LIN_SCIPIO1</a>         | 5240 3040h            | 5240 4040h            |
| 44h    | 32     | <a href="#">LIN_SCIPIO2</a>         | 5240 3044h            | 5240 4044h            |
| 48h    | 32     | <a href="#">LIN_SCIPIO3</a>         | 5240 3048h            | 5240 4048h            |
| 4Ch    | 32     | <a href="#">LIN_SCIPIO4</a>         | 5240 304Ch            | 5240 404Ch            |
| 50h    | 32     | <a href="#">LIN_SCIPIO5</a>         | 5240 3050h            | 5240 4050h            |
| 54h    | 32     | <a href="#">LIN_SCIPIO6</a>         | 5240 3054h            | 5240 4054h            |
| 58h    | 32     | <a href="#">LIN_SCIPIO7</a>         | 5240 3058h            | 5240 4058h            |
| 5Ch    | 32     | <a href="#">LIN_SCIPIO8</a>         | 5240 305Ch            | 5240 405Ch            |
| 60h    | 32     | <a href="#">LIN_LINCOMP</a>         | 5240 3060h            | 5240 4060h            |
| 64h    | 32     | <a href="#">LIN_LINRD0</a>          | 5240 3064h            | 5240 4064h            |
| 68h    | 32     | <a href="#">LIN_LINRD1</a>          | 5240 3068h            | 5240 4068h            |
| 6Ch    | 32     | <a href="#">LIN_LINMASK</a>         | 5240 306Ch            | 5240 406Ch            |
| 70h    | 32     | <a href="#">LIN_LINID</a>           | 5240 3070h            | 5240 4070h            |
| 74h    | 32     | <a href="#">LIN_LINTD0</a>          | 5240 3074h            | 5240 4074h            |
| 78h    | 32     | <a href="#">LIN_LINTD1</a>          | 5240 3078h            | 5240 4078h            |
| 7Ch    | 32     | <a href="#">LIN_MBRSR</a>           | 5240 307Ch            | 5240 407Ch            |
| 80h    | 32     | <a href="#">LIN_RESERVED_1_J</a>    | 5240 3080h + formula  | 5240 4080h + formula  |
| 90h    | 32     | <a href="#">LIN_IODFTCTRL</a>       | 5240 3090h            | 5240 4090h            |
| 94h    | 32     | <a href="#">LIN_RESERVED_2_J</a>    | 5240 3094h + formula  | 5240 4094h + formula  |
| E0h    | 32     | <a href="#">LIN_LIN_GLB_INT_EN</a>  | 5240 30E0h            | 5240 40E0h            |
| E4h    | 32     | <a href="#">LIN_LIN_GLB_INT_FLG</a> | 5240 30E4h            | 5240 40E4h            |
| E8h    | 32     | <a href="#">LIN_LIN_GLB_INT_CLR</a> | 5240 30E8h            | 5240 40E8h            |

### **5.11.2 LIN Registers**

#### **LIN Registers**

### 5.11.2.1 LIN\_SCIGCR0 Register

#### 1 LIN\_SCIGCR0 Register (Offset = 0h) [reset = 0h]

The SCIGCR0 register defines the module reset.

Return to [Summary Table](#)

**Table 5-1924. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 0000h       |
| LIN1          | 5240 1000h       |
| LIN2          | 5240 2000h       |
| LIN3          | 5240 3000h       |
| LIN4          | 5240 4000h       |

**Figure 5-637. LIN\_SCIGCR0 Name Register**

|            |    |    |    |    |    |    |       |
|------------|----|----|----|----|----|----|-------|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24    |
| RESERVED_2 |    |    |    |    |    |    |       |
| R          |    |    |    |    |    |    |       |
| 0h         |    |    |    |    |    |    |       |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16    |
| RESERVED_2 |    |    |    |    |    |    |       |
| R          |    |    |    |    |    |    |       |
| 0h         |    |    |    |    |    |    |       |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8     |
| RESERVED_1 |    |    |    |    |    |    |       |
| R          |    |    |    |    |    |    |       |
| 0h         |    |    |    |    |    |    |       |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0     |
| RESERVED_1 |    |    |    |    |    |    | RESET |
| R          |    |    |    |    |    |    | R/W   |
| 0h         |    |    |    |    |    |    | 0h    |

**Table 5-1926. LIN\_SCIGCR0 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                           |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                              |
| 15:1  | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                              |
| 0     | RESET      | R/W  | 0h    | <p>This bit resets the SCI/LIN module. This bit is effective in LIN or SCI-compatible mode.. This bit affects the reset state of the SCI/LIN module.</p> <p>0      SCI/LIN module is in held in reset.<br/>1      SCI/LIN module is out of reset.</p> |



### 5.11.2.2 LIN\_SCIGCR1 Register

#### 1 LIN\_SCIGCR1 Register (Offset = 4h) [reset = 0h]

The SCIGCR1 register defines the frame format, protocol, and communication mode used by the SCI.

Return to [Summary Table](#)

**Table 5-1927. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 0004h       |
| LIN1          | 5240 1004h       |
| LIN2          | 5240 2004h       |
| LIN3          | 5240 3004h       |
| LIN4          | 5240 4004h       |

**Figure 5-638. LIN\_SCIGCR1 Name Register**

|            |         |                  |          |        |           |            |          |
|------------|---------|------------------|----------|--------|-----------|------------|----------|
| 31         | 30      | 29               | 28       | 27     | 26        | 25         | 24       |
| RESERVED_3 |         |                  |          |        |           | TXENA      | RXENA    |
| R          |         |                  |          |        |           | R/W        | R/W      |
| 0h         |         |                  |          |        |           | 0h         | 0h       |
| 23         | 22      | 21               | 20       | 19     | 18        | 17         | 16       |
| RESERVED_2 |         |                  |          |        |           | CONT       | LOOPBACK |
| R          |         |                  |          |        |           | R/W        | R/W      |
| 0h         |         |                  |          |        |           | 0h         | 0h       |
| 15         | 14      | 13               | 12       | 11     | 10        | 9          | 8        |
| RESERVED_1 |         | STOPEXTFRA<br>ME | HGENCTRL | CTYPE  | MBUFMODE  | ADAPT      | SLEEP    |
| R          |         | R/W              | R/W      | R/W    | R/W       | R/W        | R/W      |
| 0h         |         | 0h               | 0h       | 0h     | 0h        | 0h         | 0h       |
| 7          | 6       | 5                | 4        | 3      | 2         | 1          | 0        |
| SWNRST     | LINMODE | CLK_MASTER       | STOP     | PARITY | PARITYENA | TIMINGMODE | COMMMODE |
| R/W        | R/W     | R/W              | R/W      | R/W    | R/W       | R/W        | R/W      |
| 0h         | 0h      | 0h               | 0h       | 0h     | 0h        | 0h         | 0h       |

**Table 5-1929. LIN\_SCIGCR1 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:26 | RESERVED_3 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 25    | TXENA      | R/W  | 0h    | <p>Transmit enable.</p> <p>This bit is effective in LIN and SCI modes. Data is transferred from SCITD or the TDy [with y=0, 1,...7] buffers in LIN mode to the SCITXSHF shift out register only when the TXENA bit is set.</p> <p>Note: Data written to SCITD or the transmit multi-buffer before TXENA is set is not transmitted. If TXENA is cleared while transmission is ongoing, the data previously written to SCITD is sent [including the checksum byte in LIN mode].</p> <p>0 Disable transfers from SCITD or TDy to SCITXSHF</p> <p>1 Enable transfers of data from SCITD or TDy to SCITXSHF</p> |

**Table 5-1929. LIN\_SCIGCR1 Register Field Descriptions (continued)**

| Bit   | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|--------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24    | RXENA        | R/W  | 0h    | <p>Receive enable.</p> <p>This bit is effective in LIN or SCI-compatible mode. RXENA allows or prevents the transfer of data from SCIRXSHF to SCIRD or the receive multibuffers.</p> <p>Note: Clearing RXENA stops received characters from being transferred into the receive buffer or multi-buffers, prevents the RX status flags [see Table 7] from being updated by receive data, and inhibits both receive and error interrupts. However, the shift register continues to assemble data regardless of the state of RXENA.</p> <p>Note: If RXENA is cleared before the time the reception of a frame is complete, the data from the frame is not transferred into the receive buffer.</p> <p>Note: If RXENA is set before the time the reception of a frame is complete, the data from the frame is transferred into the receive buffer. If RXENA is set while SCIRXSHF is in the process of assembling a frame, the status flags are not guaranteed to be accurate for that frame. To ensure that the status flags correctly reflect what was detected on the bus during a particular frame, RXENA should be set before the detection of that frame</p> <p>0 Prevents the receiver from transferring data from the shift buffer to the receive buffer or multi-buffers</p> <p>1 Allows the receiver to transfer data from the shift buffer to the receive buffer or multi-buffers</p> |
| 23:18 | RESERVED_2   | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 17    | CONT         | R/W  | 0h    | <p>Continue on suspend.</p> <p>This bit has an effect only when a program is being debugged with an emulator, and it determines how the SCI/LIN operates when the program is suspended. This bit affects the LIN counters. When this bit is set, the counters are not stopped during debug. When this bit is cleared, the counters are stopped during debug.</p> <p>0 when debug mode is entered, the SCI/LIN state machine is frozen. Transmissions and LIN counters are halted and resume when debug mode is exited.</p> <p>1 when debug mode is entered, the SCI/LIN continues to operate until the current transmit and receive functions are complete.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 16    | LOOPBACK     | R/W  | 0h    | <p>Loopback bit.</p> <p>This bit is effective in LIN or SCI-compatible mode. The self-checking option for the SCI/LIN can be selected with this bit. If the LINTX and LINRX pins are configured with SCI/LIN functionality, then the LINTX pin is internally connected to the LINRX pin. Externally, during loop back operation, the LINTX pin outputs a high value and the LINRX pin is in a high-impedance state. If this bit value is changed while the SCI/LIN is transmitting or receiving data, errors may result.</p> <p>0 Loopback mode is disabled.</p> <p>1 Loopback mode is enabled.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 15:14 | RESERVED_1   | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 13    | STOPEXTFRAME | R/W  | 0h    | <p>Stop extended frame communication.</p> <p>This bit is effective in LIN mode only. This bit can be written only during extended frame communication. When the extended frame communication is stopped, this bit is cleared automatically.</p> <p>0 No effect</p> <p>1 Extended frame communication will be stopped, once current frame transmission/reception is completed.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

**Table 5-1929. LIN\_SCIGCR1 Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12  | HGENCTRL | R/W  | 0h    | <p>HGEN control bit.</p> <p>This bit is effective in LIN mode only. This bit controls the type of mask filtering comparison.</p> <p>0 ID filtering using ID-Byte.</p> <p>RECEIVEDID and IDBYTE fields in the LINID register are used for detecting a match (using TX/RXMASK values). Mask of 0xFF in LINMASK register will result in NO match.</p> <p>1 ID filtering using ID-SlaveTask byte (Recommended).</p> <p>RECEIVEDID and IDSLAVETASKBYTE fields in the LINID register are used for detecting a match (using TX/RXMASK values). Mask of 0xFF in LINMASK register will result in ALWAYS match</p>                                                                                                                                                                                                                                                                                            |
| 11  | CTYPE    | R/W  | 0h    | <p>Checksum type.</p> <p>This bit is effective in LIN mode only. This bit controls the type of checksum to be used: classic or enhanced.</p> <p>0 Classic checksum is used.</p> <p>This checksum is compatible with LIN 1.3 slave nodes. The classic checksum contains the modulo-256 sum with carry over all data bytes. Frames sent with Identifier 60 (0x3C) to 63 (0x3F) must always use the classic checksum.</p> <p>1 Enhanced checksum is used.</p> <p>The enhanced checksum is compatible with LIN 2.0 and newer slave nodes. The enhanced checksum contains the modulo-256 sum with carry over all data bytes AND the protected Identifier.</p>                                                                                                                                                                                                                                            |
| 10  | MBUFMODE | R/W  | 0h    | <p>Multibuffer mode.</p> <p>This bit is effective in LIN or SCI-compatible mode. This bit controls receive/transmit buffer usage, that is, whether the RX/TX multibuffers are used or a single register, RD0/TD0, is used.</p> <p>0 The multi-buffer mode is disabled.</p> <p>1 The multi-buffer mode is enabled.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 9   | ADAPT    | R/W  | 0h    | <p>Adapt mode enable.</p> <p>This mode is effective in LIN mode only. This bit has an effect during the detection of the Sync Field. There are two LIN protocol bit rate modes that could be enabled with this bit according to the Node capability file definition: automatic or select. Software and network configuration will decide which of the previous two modes. When this bit is cleared, the LIN 2.0 protocol fixed bit rate should be used. If the ADAPT bit is set, a LIN slave node detecting the baudrate will compare it to the prescalers in BRSR register and update it if they are different. The BRSR register will be updated with the new value. If this bit is not set there will be no adjustment to the BRSR register. This field is writable in LIN mode only.</p> <p>0 Automatic baudrate adjustment is disabled.</p> <p>1 Automatic baudrate adjustment is enabled.</p> |

**Table 5-1929. LIN\_SCIGCR1 Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8   | SLEEP      | R/W  | 0h    | <p>SCI sleep.</p> <p>SCI compatibility mode only. In a multiprocessor configuration, this bit controls the receive sleep function. Clearing this bit brings the SCI out of sleep mode.</p> <p>The receiver still operates when the SLEEP bit is set; however, RXRDY is updated and SCIRD is loaded with new data only when an address frame is detected. The remaining receiver status flags are updated and an error interrupt is requested if the corresponding interrupt enable bit is set, regardless of the value of the SLEEP bit. In this way, if an error is detected on the receive data line while the SCI is asleep, software can promptly deal with the error condition. The SLEEP bit is not automatically cleared when an address byte is detected.</p> <p>This field is writable in SCI mode only.</p> <p>0 Sleep mode is disabled.<br/>1 Sleep mode is enabled.</p> |
| 7   | SWNRST     | R/W  | 0h    | <p>Software reset [active low].</p> <p>This bit is effective in LIN or SCI-compatible mode. The SCI/LIN should only be configured while SWnRST = 0.</p> <p>Only the following configuration bits can be changed in runtime [i.e., while SWnRESET = 1]:</p> <ul style="list-style-type: none"> <li>- STOP EXT Frame [SCIGCR1[13]]</li> <li>- CC bit [SCIGCR2[17]]</li> <li>- SC bit [SCIGCR2[16]]</li> </ul> <p>0 The SCI/LIN is in its reset state; no data will be transmitted or received. Writing a 0 to this bit initializes the SCI/LIN state machines and operating flags. All affected logic is held in the reset state until a 1 is written to this bit.</p> <p>1 The SCI/LIN is in its ready state; transmission and reception can occur. After this bit is set to 1, the configuration of the module should not change.</p>                                               |
| 6   | LINMODE    | R/W  | 0h    | <p>LIN mode</p> <p>This bit controls the mode of operation of the module.</p> <p>0 LIN mode is disabled; SCI compatibility mode is enabled.<br/>1 LIN mode is enabled; SCI compatibility mode is disabled.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 5   | CLK_MASTER | R/W  | 0h    | <p>SCI internal clock enable or LIN Master/Slave configuration.</p> <p>In the SCI mode, this bit enables the clock to the SCI module. In LIN mode, this bit determines whether a LIN node is a slave or master.</p> <p>0 SCI-compatible mode: Reserved.<br/>LIN mode: The module is in slave mode.<br/>1 SCI-compatible mode: Enable clock to the SCI module.<br/>LIN mode: The node is in master mode.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 4   | STOP       | R/W  | 0h    | <p>SCI number of stop bits.</p> <p>This bit is effective in SCI-compatible mode only.</p> <p>Note: The receiver checks for only one stop bit. However in idle-line mode, the receiver waits until the end of the second stop bit [if STOP = 1] to begin checking for an idle period.</p> <p>This field is writable in SCI mode only.</p> <p>0 One stop bit is used.<br/>1 Two stop bits are used.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |

**Table 5-1929. LIN\_SCIGCR1 Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-----|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3   | PARITY     | R/W  | 0h    | <p>SCI parity odd/even selection.</p> <p>This bit is effective in SCI-compatible mode only. If the PARITY ENA bit [SCIGCR1.2] is set, PARITY designates odd or even parity. The parity bit is calculated based on the data bits in each frame and the address bit [in address-bit mode]. The start and stop fields in the frame are not included in the parity calculation.</p> <p>This field is writable in SCI mode only.</p> <p>0      Odd parity is used. The SCI transmits and expects to receive a value in the parity bit that makes odd the total number of bits in the frame with the value of 1.</p> <p>1      Even parity is used. The SCI transmits and expects to receive a value in the parity bit that makes even the total number of bits in the frame with the value of 1.</p> |
| 2   | PARITYENA  | R/W  | 0h    | <p>Parity enable.</p> <p>Enables or disables the parity function.</p> <p>0      SCI-compatible mode: Parity disabled; no parity bit is generated during transmission or is expected during reception.</p> <p>LIN mode: ID-parity verification is disabled.</p> <p>1      SCI compatible mode: Parity enabled. A parity bit is generated during transmission and is expected during reception.</p> <p>LIN mode: ID-parity verification is enabled.</p>                                                                                                                                                                                                                                                                                                                                           |
| 1   | TIMINGMODE | R/W  | 0h    | <p>SCI timing mode bit.</p> <p>This bit is effective in SCI-compatible mode only. It must be set to 1 when the SCI mode is used. This bit configures the SCI for asynchronous operation.</p> <p>0      Reserved.</p> <p>1      Must be set to 1 when module is configured for SCI operation</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 0   | COMMMODE   | R/W  | 0h    | <p>SCI/LIN communication mode bit.</p> <p>In compatibility mode, it selects the SCI communication mode. In LIN mode it selects length control option for ID-field bits ID4 and ID5.</p> <p>0      SCI-compatible mode: Idle-line mode is used.</p> <p>LIN mode: ID4 and ID5 are not used for length control.</p> <p>1      SCI-compatible mode: Address-bit mode is used.</p> <p>LIN mode: ID4 and ID5 are used for length control.</p>                                                                                                                                                                                                                                                                                                                                                         |

### 5.11.2.3 LIN\_SCIGCR2 Register

#### 1 LIN\_SCIGCR2 Register (Offset = 8h) [reset = 0h]

The SCIGCR2 register is used to send or compare a checksum byte during extended frames, to generate a wakeup and for low-power mode control of the LIN module.

Return to [Summary Table](#)

**Table 5-1930. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 0008h       |
| LIN1          | 5240 1008h       |
| LIN2          | 5240 2008h       |
| LIN3          | 5240 3008h       |
| LIN4          | 5240 4008h       |

**Figure 5-639. LIN\_SCIGCR2 Name Register**

|            |    |    |    |    |    |     |           |
|------------|----|----|----|----|----|-----|-----------|
| 31         | 30 | 29 | 28 | 27 | 26 | 25  | 24        |
| RESERVED_3 |    |    |    |    |    |     |           |
| R          |    |    |    |    |    |     |           |
| 0h         |    |    |    |    |    |     |           |
| 23         | 22 | 21 | 20 | 19 | 18 | 17  | 16        |
| RESERVED_3 |    |    |    |    |    | CC  | SC        |
| R          |    |    |    |    |    | R/W | R/W       |
| 0h         |    |    |    |    |    | 0h  | 0h        |
| 15         | 14 | 13 | 12 | 11 | 10 | 9   | 8         |
| RESERVED_2 |    |    |    |    |    |     | GENWU     |
| R          |    |    |    |    |    |     | R/W       |
| 0h         |    |    |    |    |    |     | 0h        |
| 7          | 6  | 5  | 4  | 3  | 2  | 1   | 0         |
| RESERVED_1 |    |    |    |    |    |     | POWERDOWN |
| R          |    |    |    |    |    |     | R/W       |
| 0h         |    |    |    |    |    |     | 0h        |

**Table 5-1932. LIN\_SCIGCR2 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description |
|-------|------------|------|-------|-------------|
| 31:18 | RESERVED_3 | R    | 0h    | Reserved    |

**Table 5-1932. LIN\_SCIGCR2 Register Field Descriptions (continued)**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 17   | CC         | R/W  | 0h    | <p>Compare Checksum.</p> <p>This mode is effective in LIN mode only. This bit is used by the receiver for extended frames to trigger a checksum compare. The user will initiate this transaction by Writing a one to this bit.</p> <p>In non multibuffer mode, once the CC bit is set, the checksum will be compared on the byte that is currently being received, expected to be the checkbyte.</p> <p>During Multi-buffer mode, following are the scenarios associated with the CC bit :</p> <ul style="list-style-type: none"> <li>- If CC bit is set during the reception of the data, then the byte that is received after the reception of the programmed no. of data bytes indicated by SCIFORMAT[18:16], is treated as a checksum byte.</li> <li>- If CC bit is set during the IDLE period [i.e. during inter-frame space], then the next immediate byte will be treated as a checksum byte.</li> </ul> <p>A CE will immediatly be flagged if there is a checksum error.</p> <p>This bit is automatically cleared once the checksum is successfully compared.</p> <p>0 No effect<br/>1 Compare checksum on expected checkbyte</p> |
| 16   | SC         | R/W  | 0h    | <p>Send Checksum</p> <p>This mode is effective in LIN mode only. This bit is used by the transmitter with extended frames to send a checkbyte. In non multibuffer mode the checkbyte will be sent after the current byte transmission. In multibuffer mode the checkbyte will be sent after the last byte count, indicated by the SCIFORMAT[18:16].</p> <p>This field is writable in LIN mode only.</p> <p>0 No checkbyte will be sent.<br/>1 A checkbyte will be sent. This bit will automatically get cleared after the checkbyte is transmitted. The checksum will not be sent if this bit is set before transmitting the very first byte, that is, during interframe space.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 15:9 | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 8    | GENWU      | R/W  | 0h    | <p>Generate wakeup signal.</p> <p>This bit controls the generation of a wakeup signal, by transmitting the TDO buffer value. This bit is cleared on reception of a valid sync break.</p> <p>0 No effect<br/>1 Transmit TDO for wakeup. This bit will be cleared on a SWNRST (SCIGCR1.7)</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 7:1  | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 0    | POWERDOWN  | R/W  | 0h    | <p>Power down.</p> <p>This bit is effective in LIN or SCI-compatible mode. When the powerdown bit is set, the SCI/LIN module attempts to enter local low-power mode. If the POWERDOWN bit is set while the receiver is actively receiving data and the wakeup interrupt is disabled, then the SCI/LIN will delay low-power mode from being entered until completion of reception. In LIN mode the user may set the POWERDOWN bit on Sleep Command reception or on idle bus detection [more than 4 seconds, i.e. 80,000 cycles at 20kHz]</p> <p>0 Normal operation<br/>1 Request local low-power mode</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

### 5.11.2.4 LIN\_SCISSETINT Register

#### 1 LIN\_SCISSETINT Register (Offset = Ch) [reset = 0h]

The SCISSETINT register is used to enable the various interrupts available in the LIN module.

Return to [Summary Table](#)

**Table 5-1933. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 000Ch       |
| LIN1          | 5240 100Ch       |
| LIN2          | 5240 200Ch       |
| LIN3          | 5240 300Ch       |
| LIN4          | 5240 400Ch       |

**Figure 5-640. LIN\_SCISSETINT Name Register**

|               |              |            |               |            |                |              |             |
|---------------|--------------|------------|---------------|------------|----------------|--------------|-------------|
| 31            | 30           | 29         | 28            | 27         | 26             | 25           | 24          |
| SETBEINT      | SETPBEINT    | SETCEINT   | SETISFEINT    | SETNREINT  | SETFEINT       | SETOEINT     | SETPEINT    |
| R/W1TS        | R/W1TS       | R/W1TS     | R/W1TS        | R/W1TS     | R/W1TS         | R/W1TS       | R/W1TS      |
| 0h            | 0h           | 0h         | 0h            | 0h         | 0h             | 0h           | 0h          |
| 23            | 22           | 21         | 20            | 19         | 18             | 17           | 16          |
| RESERVED_5    |              |            |               |            | SET_RX_DMA_ALL | SET_RX_DMA   | SET_TX_DMA  |
| R             |              |            |               |            | R/W1TS         | R/W1TS       | R/W1TS      |
| 0h            |              |            |               |            | 0h             | 0h           | 0h          |
| 15            | 14           | 13         | 12            | 11         | 10             | 9            | 8           |
| RESERVED_4    |              | SETIDINT   | RESERVED_3    |            |                | SETRXINT     | SETTXINT    |
| R             |              | R/W1TS     | R             |            |                | R/W1TS       | R/W1TS      |
| 0h            |              | 0h         | 0h            |            |                | 0h           | 0h          |
| 7             | 6            | 5          | 4             | 3          | 2              | 1            | 0           |
| SETTOA3WUSINT | SETTOAWUSINT | RESERVED_2 | SETTIMEOUTINT | RESERVED_1 |                | SETWAKEUPINT | SETBRKDTINT |
| R/W1TS        | R/W1TS       | R          | R/W1TS        | R          |                | R/W1TS       | R/W1TS      |
| 0h            | 0h           | 0h         | 0h            | 0h         |                | 0h           | 0h          |

**Table 5-1935. LIN\_SCISSETINT Register Field Descriptions**

| Bit | Field     | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                              |
|-----|-----------|--------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31  | SETBEINT  | R/W1TS | 0h    | Set bit error interrupt.<br>This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN module to generate an interrupt when there is a bit error. This field is writable in LIN mode only.<br><br>0      Interrupt is disabled. writing a 0 to this bit has no effect.<br>1      Interrupt is enabled.                 |
| 30  | SETPBEINT | R/W1TS | 0h    | Set physical bus error interrupt.<br>This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN module to generate an interrupt when a physical bus error occurs. This field is writable in LIN mode only.<br><br>0      Interrupt is disabled. writing a 0 to this bit has no effect.<br>1      Interrupt is enabled. |



**Table 5-1935. LIN\_SCISSETINT Register Field Descriptions (continued)**

| Bit   | Field          | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|----------------|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29    | SETCEINT       | R/W1TS | 0h    | <p>Set checksum-error Interrupt.</p> <p>This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN module to generate an interrupt when there is a checksum error.</p> <p>This field is writable in LIN mode only.</p> <p>0      Interrupt is disabled. Writing a 0 to this bit has no effect.</p> <p>1      Interrupt is enabled.</p>                                                                                                                                                                                                      |
| 28    | SETISFEINT     | R/W1TS | 0h    | <p>Set inconsistent-sync-field-error interrupt.</p> <p>This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN module to generate an interrupt when there is an inconsistent sync field error.</p> <p>This field is writable in LIN mode only.</p> <p>0      Interrupt is disabled. Writing a 0 to this bit has no effect.</p> <p>1      Interrupt is enabled.</p>                                                                                                                                                                       |
| 27    | SETNREINT      | R/W1TS | 0h    | <p>Set no-response-error interrupt.</p> <p>This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN module to generate an interrupt when a no-response error occurs.</p> <p>This field is writable in LIN mode only.</p> <p>0      Interrupt is disabled. Writing a 0 to this bit has no effect.</p> <p>1      Interrupt is enabled.</p>                                                                                                                                                                                                  |
| 26    | SETFEINT       | R/W1TS | 0h    | <p>Set framing-error interrupt.</p> <p>This bit is effective in LIN or SCI-compatible mode. Setting this bit enables the SCI/LIN module to generate an interrupt when a framing error occurs.</p> <p>0      Interrupt is disabled. Writing a 0 to this bit has no effect.</p> <p>1      Interrupt is enabled.</p>                                                                                                                                                                                                                                             |
| 25    | SETOEINT       | R/W1TS | 0h    | <p>Set overrun-error interrupt.</p> <p>This bit is effective in LIN or SCI-compatible mode. Setting this bit enables the SCI/LIN module to generate an interrupt when an overrun error occurs.</p> <p>0      Interrupt is disabled. Writing a 0 to this bit has no effect.</p> <p>1      Interrupt is enabled.</p>                                                                                                                                                                                                                                            |
| 24    | SETPEINT       | R/W1TS | 0h    | <p>Set parity interrupt.</p> <p>This bit is effective in LIN or SCI-compatible mode. Setting this bit enables the SCI/LIN module to generate an interrupt when a parity error occurs.</p> <p>0      Interrupt is disabled. Writing a 0 to this bit has no effect.</p> <p>1      Interrupt is enabled.</p>                                                                                                                                                                                                                                                     |
| 23:19 | RESERVED_5     | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 18    | SET_RX_DMA_ALL | R/W1TS | 0h    | <p>Set receiver DMA for Address &amp; Data frames.</p> <p>This bit is effective in LIN or SCI-compatible mode. To enable RX DMA request for address and data frames this bit must be set. If it is cleared, RX interrupt request is generated for address frames and DMA requests are generated for data frames.</p> <p>0      Receiver DMA request is disabled for address frames (RX interrupt request is enabled for address frames). Writing a 0 to this bit has no effect.</p> <p>1      Receiver DMA request is enabled for address and data frames</p> |

**Table 5-1935. LIN\_SCISSETINT Register Field Descriptions (continued)**

| Bit   | Field         | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                         |
|-------|---------------|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 17    | SET_RX_DMA    | R/W1TS | 0h    | Set receiver DMA.<br>This bit is effective in LIN or SCI-compatible mode. To enable DMA requests for the receiver this bit must be set. If it is cleared, interrupt requests are generated depending on SETRXINT.<br><br>0 Receiver DMA request is disabled. Writing a 0 to this bit has no effect.<br>1 Receiver DMA request is enabled.                           |
| 16    | SET_TX_DMA    | R/W1TS | 0h    | Set transmit DMA.<br>This bit is effective in LIN or SCI-compatible mode. To enable DMA requests for the transmitter, this bit must be set. If it is cleared, interrupt requests are generated depending on SETTXINT.<br><br>0 Transmit DMA request is disabled. Writing a 0 to this bit has no effect.<br>1 Transmit DMA request is enabled                        |
| 15:14 | RESERVED_4    | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                            |
| 13    | SETIDINT      | R/W1TS | 0h    | Set Identification interrupt.<br>This bit is effective in LIN mode only. This bit is set to enable interrupt once a valid matching identifier is received.<br><br>0 Interrupt is disabled. Writing a 0 to this bit has no effect.<br>1 Interrupt is enabled.                                                                                                        |
| 12:10 | RESERVED_3    | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                            |
| 9     | SETRXINT      | R/W1TS | 0h    | Set Receiver interrupt.<br>Setting this bit enables the SCI/LIN to generate a receive interrupt after a frame has been completely received and the data is being transferred from SCIRXSHF to SCIRD.<br><br>0 Interrupt is disabled. Writing a 0 to this bit has no effect.<br>1 Interrupt is enabled.                                                              |
| 8     | SETTXINT      | R/W1TS | 0h    | Set Transmitter interrupt.<br>Setting this bit enables the SCI/LIN to generate a transmit interrupt as data is being transferred from SCITD to SCITXSHF and the TXRDY bit is being set.<br><br>0 Interrupt is disabled. Writing a 0 to this bit has no effect.<br>1 Interrupt is enabled.                                                                           |
| 7     | SETTOA3WUSINT | R/W1TS | 0h    | Set Timeout After 3 Wakeup Signals interrupt.<br>This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN to generate an interrupt when there is a timeout after 3 wakeup signals have been sent.<br>This field is writable in LIN mode only.<br><br>0 Interrupt is disabled. Writing a 0 to this bit has no effect.<br>1 Interrupt is enabled. |
| 6     | SETTOAWUSINT  | R/W1TS | 0h    | Set Timeout After Wakeup Signal interrupt.<br>This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN to generate an interrupt when there is a timeout after one wakeup signal has been sent.<br>This field is writable in LIN mode only.<br><br>0 Interrupt is disabled. Writing a 0 to this bit has no effect.<br>1 Interrupt is enabled.    |
| 5     | RESERVED_2    | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                            |

**Table 5-1935. LIN\_SCISSETINT Register Field Descriptions (continued)**

| Bit | Field         | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-----|---------------|--------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | SETTIMEOUTINT | R/W1TS | 0h    | <p>Set timeout interrupt.</p> <p>This bit is effective in LIN mode only. Setting this bit enables the SCI/LIN to generate an interrupt when no LIN bus activity [bus idle] occurs for at least 4 seconds.</p> <p>This field is writable in LIN mode only.</p> <p>0        Interrupt is disabled. Writing a 0 to this bit has no effect.</p> <p>1        Interrupt is enabled.</p>                                                                                                                                                                                                                                                                                                |
| 3:2 | RESERVED_1    | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 1   | SETWAKEUPINT  | R/W1TS | 0h    | <p>Set wake-up interrupt.</p> <p>This bit is effective in LIN or SCI-compatible mode. Setting this bit enables the SCI/LIN to generate a wake-up interrupt and thereby exit low-power mode. The wake-up interrupt is asserted on falling edge of the wake-up pulse. If enabled, the wake-up interrupt is asserted when local low-power mode is requested while the receiver is busy or if a low level is detected on the SCIRX pin during low-power mode. Wake-up interrupt is not asserted upon a wakeup pulse if the module is not in power down mode.</p> <p>0        Interrupt is disabled. Writing a 0 to this bit has no effect.</p> <p>1        Interrupt is enabled.</p> |
| 0   | SETBRKDTINT   | R/W1TS | 0h    | <p>Set break-detect interrupt.</p> <p>This bit is effective in SCI-compatible mode only. Setting this bit enables the SCI/LIN to generate an interrupt if a break condition is detected on the LINRX pin.</p> <p>This field is writable in SCI mode only.</p> <p>0        Interrupt is disabled. Writing a 0 to this bit has no effect.</p> <p>1        Interrupt is enabled.</p>                                                                                                                                                                                                                                                                                                |

### 5.11.2.5 LIN\_SCICLEARINT Register

#### 1 LIN\_SCICLEARINT Register (Offset = 10h) [reset = 0h]

The SCICLEARINT register is used to disable the enabled interrupts without accessing the SCISSETINT register.

Return to [Summary Table](#)

**Table 5-1936. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 0010h       |
| LIN1          | 5240 1010h       |
| LIN2          | 5240 2010h       |
| LIN3          | 5240 3010h       |
| LIN4          | 5240 4010h       |

**Figure 5-641. LIN\_SCICLEARINT Name Register**

|                   |                  |            |                   |            |            |                  |            |
|-------------------|------------------|------------|-------------------|------------|------------|------------------|------------|
| 31                | 30               | 29         | 28                | 27         | 26         | 25               | 24         |
| CLRBEINT          | CLRPBEINT        | CLRCEINT   | CLRISFEINT        | CLRNREINT  | CLRFEINT   | CLROEINT         | CLRPEINT   |
| R/W1TC            | R/W1TC           | R/W1TC     | R/W1TC            | R/W1TC     | R/W1TC     | R/W1TC           | R/W1TC     |
| 0h                | 0h               | 0h         | 0h                | 0h         | 0h         | 0h               | 0h         |
| 23                | 22               | 21         | 20                | 19         | 18         | 17               | 16         |
| RESERVED_6        |                  |            |                   |            | RESERVED_5 | SETRXDMA         | CLRTXDMA   |
| R                 |                  |            |                   |            | R          | R/W1TC           | R/W1TC     |
| 0h                |                  |            |                   |            | 0h         | 0h               | 0h         |
| 15                | 14               | 13         | 12                | 11         | 10         | 9                | 8          |
| RESERVED_4        |                  | CLRIDINT   | RESERVED_3        |            |            | CLRRXINT         | CLRTXINT   |
| R                 |                  | R/W1TC     | R                 |            |            | R/W1TC           | R/W1TC     |
| 0h                |                  | 0h         | 0h                |            |            | 0h               | 0h         |
| 7                 | 6                | 5          | 4                 | 3          | 2          | 1                | 0          |
| CLRTOA3WUSI<br>NT | CLRTOAWUSI<br>NT | RESERVED_2 | CLRTIMEOUTI<br>NT | RESERVED_1 |            | CLRWAKEUPI<br>NT | CLRBKDTINT |
| R/W1TC            | R/W1TC           | R          | R/W1TC            | R          |            | R/W1TC           | R/W1TC     |
| 0h                | 0h               | 0h         | 0h                | 0h         |            | 0h               | 0h         |

**Table 5-1938. LIN\_SCICLEARINT Register Field Descriptions**

| Bit | Field     | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                 |
|-----|-----------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31  | CLRBEINT  | R/W1TC | 0h    | Clear Bit Error Interrupt.<br>This bit is effective in LIN mode only. Setting this bit disables the bit error interrupt.<br>This field is writable in LIN mode only.<br>0 Interrupt is disabled. writing a 0 to this bit has no effect.<br>1 Interrupt is enabled. writing a 1 to this bit will disable the interrupt and clear this bit.                   |
| 30  | CLRPBEINT | R/W1TC | 0h    | Clear Physical Bus Error Interrupt.<br>This bit is effective in LIN mode only. Setting this bit disables the physical-bus error interrupt.<br>This field is writable in LIN mode only.<br>0 Interrupt is disabled. writing a 0 to this bit has no effect.<br>1 Interrupt is enabled. writing a 1 to this bit will disable the interrupt and clear this bit. |

**Table 5-1938. LIN\_SCICLEARINT Register Field Descriptions (continued)**

| Bit   | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                      |
|-------|------------|--------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29    | CLRCEINT   | R/W1TC | 0h    | <p>Clear checksum-error Interrupt.<br/>This bit is effective in LIN mode only. Setting this bit disables the checksum-error interrupt.<br/>This field is writable in LIN mode only.</p> <p>0      Interrupt is disabled. writing a 0 to this bit has no effect.<br/>1      Interrupt is enabled. writing a 1 to this bit will disable the interrupt and clear this bit.</p>      |
| 28    | CLRISFEINT | R/W1TC | 0h    | <p>Clear Inconsistent-Sync-Field-Error Interrupt.<br/>This bit is effective in LIN mode only. Setting this bit disables the ISFE interrupt.<br/>This field is writable in LIN mode only.</p> <p>0      Interrupt is disabled. writing a 0 to this bit has no effect.<br/>1      Interrupt is enabled. writing a 1 to this bit will disable the interrupt and clear this bit.</p> |
| 27    | CLRNREINT  | R/W1TC | 0h    | <p>Clear No-Reponse-Error Interrupt.<br/>This bit is effective in LIN mode only. Setting this bit disables the no-response error interrupt.<br/>This field is writable in LIN mode only.</p> <p>0      Interrupt is disabled. writing a 0 to this bit has no effect.<br/>1      Interrupt is enabled. writing a 1 to this bit will disable the interrupt and clear this bit.</p> |
| 26    | CLRFEINT   | R/W1TC | 0h    | <p>Clear Framing-Error Interrupt.<br/>This bit is effective in LIN or SCI-compatible mode. Setting this bit disables framing-error interrupt.</p> <p>0      Interrupt is disabled. writing a 0 to this bit has no effect.<br/>1      Interrupt is enabled. writing a 1 to this bit will disable the interrupt and clear this bit.</p>                                            |
| 25    | CLROEINT   | R/W1TC | 0h    | <p>Clear Overrun-Error Interrupt.<br/>This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the overrun interrupt.</p> <p>0      Interrupt is disabled. writing a 0 to this bit has no effect.<br/>1      Interrupt is enabled. writing a 1 to this bit will disable the interrupt and clear this bit.</p>                                              |
| 24    | CLRPEINT   | R/W1TC | 0h    | <p>Clear Parity Interrupt.<br/>This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the parity error interrupt.</p> <p>0      Interrupt is disabled. writing a 0 to this bit has no effect.<br/>1      Interrupt is enabled. writing a 1 to this bit will disable the interrupt and clear this bit.</p>                                                |
| 23:19 | RESERVED_6 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                         |
| 18    | RESERVED_5 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                         |

**Table 5-1938. LIN\_SCICLEARINT Register Field Descriptions (continued)**

| Bit   | Field         | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                             |
|-------|---------------|--------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 17    | SETRXDMA      | R/W1TC | 0h    | Clear receiver DMA.<br>This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the receive DMA request.<br><br>0 Receiver DMA request is disabled. writing a 0 to this bit has no effect.<br>1 Receiver DMA request is enabled. writing a 1 to this bit will disable the DMA request and clear this bit.                                                         |
| 16    | CLRTXDMA      | R/W1TC | 0h    | Clear transmit DMA.<br>This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the transmit DMA request.<br><br>0 Transmit DMA request is disabled. writing a 0 to this bit has no effect.<br>1 Transmit DMA request is enabled. writing a 1 to this bit will disable the DMA request and clear this bit.                                                        |
| 15:14 | RESERVED_4    | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                |
| 13    | CLRIDINT      | R/W1TC | 0h    | Clear Identifier interrupt.<br>This bit is effective in LIN mode only. Setting this bit disables the ID interrupt.<br><br>0 Interrupt is disabled. writing a 0 to this bit has no effect.<br>1 Interrupt is enabled. writing a 1 to this bit will disable the interrupt and clear this bit.                                                                                             |
| 12:10 | RESERVED_3    | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                |
| 9     | CLRRXINT      | R/W1TC | 0h    | Clear Receiver interrupt.<br>This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the receiver interrupt.<br><br>0 Interrupt is disabled. writing a 0 to this bit has no effect.<br>1 Interrupt is enabled. writing a 1 to this bit will disable the interrupt and clear this bit.                                                                            |
| 8     | CLRTXINT      | R/W1TC | 0h    | Clear Transmitter interrupt.<br>This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the transmitter interrupt.<br><br>0 Interrupt is disabled. writing a 0 to this bit has no effect.<br>1 Interrupt is enabled. writing a 1 to this bit will disable the interrupt and clear this bit.                                                                      |
| 7     | CLRTOA3WUSINT | R/W1TC | 0h    | Clear Timeout After 3 Wakeup Signals interrupt.<br>This bit is effective in LIN mode only. Setting this bit disables the timeout after 3 wakeup signals interrupt.<br>This field is writable in LIN mode only.<br><br>0 Interrupt is disabled. writing a 0 to this bit has no effect.<br>1 Interrupt is enabled. writing a 1 to this bit will disable the interrupt and clear this bit. |
| 6     | CLRTOAWUSINT  | R/W1TC | 0h    | Clear Timeout After Wakeup Signal interrupt.<br>This bit is effective in LIN mode only. Setting this bit disables the timeout after one wakeup signal interrupt.<br>This field is writable in LIN mode only.<br><br>0 Interrupt is disabled. writing a 0 to this bit has no effect.<br>1 Interrupt is enabled. writing a 1 to this bit will disable the interrupt and clear this bit.   |

**Table 5-1938. LIN\_SCICLEARINT Register Field Descriptions (continued)**

| Bit | Field         | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                        |
|-----|---------------|--------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | RESERVED_2    | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                           |
| 4   | CLRTIMEOUTINT | R/W1TC | 0h    | <p>Clear Timeout interrupt.<br/>This bit is effective in LIN mode only. Setting this bit disables the timeout [LIN bus idle] interrupt.<br/>This field is writable in LIN mode only.</p> <p>0      Interrupt is disabled. writing a 0 to this bit has no effect.<br/>1      Interrupt is enabled. writing a 1 to this bit will disable the interrupt and clear this bit.</p>       |
| 3:2 | RESERVED_1    | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                           |
| 1   | CLRWAKEUPINT  | R/W1TC | 0h    | <p>Clear Wake-up interrupt.<br/>This bit is effective in LIN or SCI-compatible mode. Setting this bit disables the wake-up interrupt.</p> <p>0      Interrupt is disabled. writing a 0 to this bit has no effect.<br/>1      Interrupt is enabled. writing a 1 to this bit will disable the interrupt and clear this bit.</p>                                                      |
| 0   | CLRBKDTINT    | R/W1TC | 0h    | <p>Clear Break-detect interrupt.<br/>This bit is effective in SCI-compatible mode only. Setting this bit disables the Break-detect interrupt.<br/>This field is writable in SCI mode only.</p> <p>0      Interrupt is disabled. writing a 0 to this bit has no effect.<br/>1      Interrupt is enabled. writing a 1 to this bit will disable the interrupt and clear this bit.</p> |

### 5.11.2.6 LIN\_SCISSETINTLVL Register

#### 1 LIN\_SCISSETINTLVL Register (Offset = 14h) [reset = 0h]

The SCISSETINTLVL register is used to map individual interrupt sources to the INT1 interrupt line.

Return to [Summary Table](#)

**Table 5-1939. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 0014h       |
| LIN1          | 5240 1014h       |
| LIN2          | 5240 2014h       |
| LIN3          | 5240 3014h       |
| LIN4          | 5240 4014h       |

**Figure 5-642. LIN\_SCISSETINTLVL Name Register**

|                  |                 |             |                  |              |             |                 |                |
|------------------|-----------------|-------------|------------------|--------------|-------------|-----------------|----------------|
| 31               | 30              | 29          | 28               | 27           | 26          | 25              | 24             |
| SETBEINTLVL      | SETPBEINTLVL    | SETCEINTLVL | SETISFEINTLVL    | SETNREINTLVL | SETFEINTLVL | SETOEINTLVL     | SETPEINTLVL    |
| R/W1TS           | R/W1TS          | R/W1TS      | R/W1TS           | R/W1TS       | R/W1TS      | R/W1TS          | R/W1TS         |
| 0h               | 0h              | 0h          | 0h               | 0h           | 0h          | 0h              | 0h             |
| 23               | 22              | 21          | 20               | 19           | 18          | 17              | 16             |
| RESERVED_7       |                 |             |                  |              | RESERVED_6  | RESERVED_5      |                |
| R                |                 |             |                  |              | R           | R               |                |
| 0h               |                 |             |                  |              | 0h          | 0h              |                |
| 15               | 14              | 13          | 12               | 11           | 10          | 9               | 8              |
| RESERVED_4       |                 | SETIDINTLVL | RESERVED_3       |              |             | SETRXINTOVO     | SETTXINTLVL    |
| R                |                 | R/W1TS      | R                |              |             | R/W1TS          | R/W1TS         |
| 0h               |                 | 0h          | 0h               |              |             | 0h              | 0h             |
| 7                | 6               | 5           | 4                | 3            | 2           | 1               | 0              |
| SETTOA3WUSINTLVL | SETTOAWUSINTLVL | RESERVED_2  | SETTIMEOUTINTLVL | RESERVED_1   |             | SETWAKEUPINTLVL | SETBRKDTINTLVL |
| R/W1TS           | R/W1TS          | R           | R/W1TS           | R            |             | R/W1TS          | R/W1TS         |
| 0h               | 0h              | 0h          | 0h               | 0h           |             | 0h              | 0h             |

**Table 5-1941. LIN\_SCISSETINTLVL Register Field Descriptions**

| Bit | Field        | Type   | Reset | Description                                                                                                                                                                                                                                                                                                        |
|-----|--------------|--------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31  | SETBEINTLVL  | R/W1TS | 0h    | Set Bit Error interrupt level.<br>This bit is effective in LIN mode only. Writing to this bit maps the Bit Error interrupt level to the INT1 line.<br>This field is writable in LIN mode only.<br><br>0      Interrupt level mapped to INT0 line.<br>1      Interrupt level mapped to INT1 line.                   |
| 30  | SETPBEINTLVL | R/W1TS | 0h    | Set Physical Bus Error interrupt level.<br>This bit is effective in LIN mode only. Writing to this bit maps the Physical Bus Error interrupt level to the INT1 line.<br>This field is writable in LIN mode only.<br><br>0      Interrupt level mapped to INT0 line.<br>1      Interrupt level mapped to INT1 line. |



**Table 5-1941. LIN\_SCISSETINTLVL Register Field Descriptions (continued)**

| Bit   | Field         | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|---------------|--------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29    | SETCEINTLVL   | R/W1TS | 0h    | Set Checksum-error interrupt level.<br>This bit is effective in LIN mode only. Writing to this bit maps the Checksum-error interrupt level to the INT1 line.<br>This field is writable in LIN mode only.<br><br>0        Interrupt level mapped to INT0 line.<br>1        Interrupt level mapped to INT1 line.                               |
| 28    | SETISFEINTLVL | R/W1TS | 0h    | Set Inconsistent-Sync-Field-Error interrupt level.<br>This bit is effective in LIN mode only. Writing to this bit maps the Inconsistent-Sync-Field-Error interrupt level to the INT1 line.<br>This field is writable in LIN mode only.<br><br>0        Interrupt level mapped to INT0 line.<br>1        Interrupt level mapped to INT1 line. |
| 27    | SETNREINTLVL  | R/W1TS | 0h    | Set No-Reponse-Error interrupt level.<br>This bit is effective in LIN mode only. Writing to this bit maps the No-Response-Error interrupt level to the INT1 line.<br>This field is writable in LIN mode only.<br><br>0        Interrupt level mapped to INT0 line.<br>1        Interrupt level mapped to INT1 line.                          |
| 26    | SETFEINTLVL   | R/W1TS | 0h    | Set Framing-Error interrupt level.<br>This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Framing-Error interrupt level to the INT1 line.<br><br>0        Interrupt level mapped to INT0 line.<br>1        Interrupt level mapped to INT1 line.                                                                |
| 25    | SETOEINTLVL   | R/W1TS | 0h    | Set Overrun-Error Interrupt Level.<br>This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Overrun-Error interrupt level to the INT1 line.<br><br>0        Interrupt level mapped to INT0 line.<br>1        Interrupt level mapped to INT1 line.                                                                |
| 24    | SETPEINTLVL   | R/W1TS | 0h    | Set Parity Error interrupt level.<br>This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Parity error interrupt level to the INT1 line.<br><br>0        Interrupt level mapped to INT0 line.<br>1        Interrupt level mapped to INT1 line.                                                                  |
| 23:19 | RESERVED_7    | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 18    | RESERVED_6    | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 17:16 | RESERVED_5    | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 15:14 | RESERVED_4    | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 13    | SETIDINTLVL   | R/W1TS | 0h    | Set ID interrupt level.<br>This bit is effective in LIN mode only. Writing to this bit maps the ID interrupt level to the INT1 line.<br>This field is writable in LIN mode only.<br><br>0        Interrupt level mapped to INT0 line.<br>1        Interrupt level mapped to INT1 line.                                                       |
| 12:10 | RESERVED_3    | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                     |
| 9     | SETRXINTOVO   | R/W1TS | 0h    | Set Receiver interrupt level.<br>This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the receiver interrupt level to the INT1 line.<br><br>0        Interrupt level mapped to INT0 line.<br>1        Interrupt level mapped to INT1 line.                                                                          |
| 8     | SETTXINTLVL   | R/W1TS | 0h    | Set Transmitter interrupt level.<br>This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the transmitter interrupt level to the INT1 line.<br><br>0        Interrupt level mapped to INT0 line.<br>1        Interrupt level mapped to INT1 line.                                                                    |

**Table 5-1941. LIN\_SCISSETINTLVL Register Field Descriptions (continued)**

| Bit | Field            | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                    |
|-----|------------------|--------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | SETTOA3WUSINTLVL | R/W1TS | 0h    | Set Timeout After 3 Wakeup Signals interrupt level.<br>This bit is effective in LIN mode only. Writing to this bit maps the timeout after 3 wakeup signals interrupt level to the INT1 line.<br>This field is writable in LIN mode only.<br><br>0        Interrupt level mapped to INT0 line.<br>1        Interrupt level mapped to INT1 line. |
| 6   | SETTOAWUSINTLVL  | R/W1TS | 0h    | Set Timeout After Wakeup Signal interrupt level.<br>This bit is effective in LIN mode only. Writing to this bit maps the the timeout after wakeup interrupt level to the INT1 line.<br>This field is writable in LIN mode only.<br><br>0        Interrupt level mapped to INT0 line.<br>1        Interrupt level mapped to INT1 line.          |
| 5   | RESERVED_2       | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                       |
| 4   | SETTIMEOUTINTLVL | R/W1TS | 0h    | Set Timeout interrupt level.<br>This bit is effective in LIN mode only. Writing to this bit maps the timeout interrupt level to the INT1 line.<br>This field is writable in LIN mode only.<br><br>0        Interrupt level mapped to INT0 line.<br>1        Interrupt level mapped to INT1 line.                                               |
| 3:2 | RESERVED_1       | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                       |
| 1   | SETWAKEUPINTLVL  | R/W1TS | 0h    | Set Wake-up interrupt level.<br>This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Wake-up interrupt level to the INT1 line.<br><br>0        Interrupt level mapped to INT0 line.<br>1        Interrupt level mapped to INT1 line.                                                                              |
| 0   | SETBRKDTINTLVL   | R/W1TS | 0h    | Set Break-detect interrupt level.<br>This bit is effective in SCI-compatible mode only. Writing to this bit maps the Break-detect interrupt level to the INT1 line.<br>This field is writable in SCI mode only.<br><br>0        Interrupt level mapped to INT0 line.<br>1        Interrupt level mapped to INT1 line.                          |

### 5.11.2.7 LIN\_SCICLEARINTLVL Register

#### 1 LIN\_SCICLEARINTLVL Register (Offset = 18h) [reset = 0h]

The SCICLEARINTLVL register is used to map individual interrupt sources to the INT0 line.

Return to [Summary Table](#)

**Table 5-1942. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 0018h       |
| LIN1          | 5240 1018h       |
| LIN2          | 5240 2018h       |
| LIN3          | 5240 3018h       |
| LIN4          | 5240 4018h       |

**Figure 5-643. LIN\_SCICLEARINTLVL Name Register**

| 31               | 30              | 29          | 28               | 27           | 26          | 25              | 24            |
|------------------|-----------------|-------------|------------------|--------------|-------------|-----------------|---------------|
| CLRBEINTLVL      | CLRPBEINTLVL    | CLRCINTLVL  | CLRSFEINTLVL     | CLRNREINTLVL | CLRFEINTLVL | CLROEINTLVL     | CLRPEINTLVL   |
| R/W1TC           | R/W1TC          | R/W1TC      | R/W1TC           | R/W1TC       | R/W1TC      | R/W1TC          | R/W1TC        |
| 0h               | 0h              | 0h          | 0h               | 0h           | 0h          | 0h              | 0h            |
| 23               | 22              | 21          | 20               | 19           | 18          | 17              | 16            |
| RESERVED_7       |                 |             |                  |              | RESERVED_6  | RESERVED_5      |               |
| R                |                 |             |                  |              | R           | R               |               |
| 0h               |                 |             |                  |              | 0h          | 0h              |               |
| 15               | 14              | 13          | 12               | 11           | 10          | 9               | 8             |
| RESERVED_4       |                 | CLRIDINTLVL | RESERVED_3       |              |             | CLRRXINTLVL     | CLRTXINTLVL   |
| R                |                 | R/W1TC      | R                |              |             | R/W1TC          | R/W1TC        |
| 0h               |                 | 0h          | 0h               |              |             | 0h              | 0h            |
| 7                | 6               | 5           | 4                | 3            | 2           | 1               | 0             |
| CLRTOA3WUSINTLVL | CLRTOAWUSINTLVL | RESERVED_2  | CLRTIMEOUTINTLVL | RESERVED_1   |             | CLRWAKEUPINTLVL | CLRBKDTINTLVL |
| R/W1TC           | R/W1TC          | R           | R/W1TC           | R            |             | R/W1TC          | R/W1TC        |
| 0h               | 0h              | 0h          | 0h               | 0h           |             | 0h              | 0h            |

**Table 5-1944. LIN\_SCICLEARINTLVL Register Field Descriptions**

| Bit | Field        | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|-----|--------------|--------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31  | CLRBEINTLVL  | R/W1TC | 0h    | Clear Bit Error interrupt level.<br>This bit is effective in LIN mode only. Writing to this bit maps the Bit Error interrupt level to the INT0 line.<br>This field is writable in LIN mode only.<br><br>0      Interrupt level mapped to INT0 line.<br>1      Interrupt level mapped to INT1 line.<br>Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.                   |
| 30  | CLRPBEINTLVL | R/W1TC | 0h    | Clear Physical Bus Error interrupt level.<br>This bit is effective in LIN mode only. Writing to this bit maps the Physical Bus Error interrupt level to the INT0 line.<br>This field is writable in LIN mode only.<br><br>0      Interrupt level mapped to INT0 line.<br>1      Interrupt level mapped to INT1 line.<br>Writing a 1 to this bit will map the interrupt to INT0 and clear this bit. |

**Table 5-1944. LIN\_SCICLEARINTLVL Register Field Descriptions (continued)**

| Bit   | Field         | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|---------------|--------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29    | CLRCEINTLVL   | R/W1TC | 0h    | Clear Checksum-error interrupt level.<br>This bit is effective in LIN mode only. Writing to this bit maps the Checksum-error interrupt level to the INT0 line.<br>This field is writable in LIN mode only.<br><br>0      Interrupt level mapped to INT0 line.<br>1      Interrupt level mapped to INT1 line.<br>Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.                               |
| 28    | CLRISFEINTLVL | R/W1TC | 0h    | Clear Inconsistent-Sync-Field-Error interrupt level.<br>This bit is effective in LIN mode only. Writing to this bit maps the Inconsistent-Sync-Field-Error interrupt level to the INT0 line.<br>This field is writable in LIN mode only.<br><br>0      Interrupt level mapped to INT0 line.<br>1      Interrupt level mapped to INT1 line.<br>Writing a 1 to this bit will map the interrupt to INT0 and clear this bit. |
| 27    | CLRNREINTLVL  | R/W1TC | 0h    | Clear No-Reponse-Error interrupt level.<br>This bit is effective in LIN mode only. Writing to this bit maps the No-Response-Error interrupt level to the INT0 line.<br>This field is writable in LIN mode only.<br><br>0      Interrupt level mapped to INT0 line.<br>1      Interrupt level mapped to INT1 line.<br>Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.                          |
| 26    | CLRFEINTLVL   | R/W1TC | 0h    | Clear Framing-Error interrupt level.<br>This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Framing-Error interrupt level to the INT0 line.<br><br>0      Interrupt level mapped to INT0 line.<br>1      Interrupt level mapped to INT1 line.<br>Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.                                                                |
| 25    | CLROEINTLVL   | R/W1TC | 0h    | Clear Overrun-Error Interrupt Level.<br>This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Overrun-Error interrupt level to the INT0 line.<br><br>0      Interrupt level mapped to INT0 line.<br>1      Interrupt level mapped to INT1 line.<br>Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.                                                                |
| 24    | CLRPEINTLVL   | R/W1TC | 0h    | Clear Parity Error interrupt level.<br>This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Parity Error interrupt level to the INT0 line.<br><br>0      Interrupt level mapped to INT0 line.<br>1      Interrupt level mapped to INT1 line.<br>Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.                                                                  |
| 23:19 | RESERVED_7    | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 18    | RESERVED_6    | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 17:16 | RESERVED_5    | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 15:14 | RESERVED_4    | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 13    | CLRIDINTLVL   | R/W1TC | 0h    | Clear ID interrupt level.<br>This bit is effective in LIN mode only. Writing to this bit maps the ID interrupt level to the INT0 line.<br>This field is writable in LIN mode only.<br><br>0      Interrupt level mapped to INT0 line.<br>1      Interrupt level mapped to INT1 line.<br>Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.                                                       |
| 12:10 | RESERVED_3    | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                 |

**Table 5-1944. LIN\_SCICLEARINTLVL Register Field Descriptions (continued)**

| Bit | Field            | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|------------------|--------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9   | CLRRXINTLVL      | R/W1TC | 0h    | <p>Clear Receiver interrupt level.</p> <p>This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the receiver interrupt level to the INT0 line.</p> <p>0      Interrupt level mapped to INT0 line.<br/> 1      Interrupt level mapped to INT1 line.<br/> Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.</p>                                                                         |
| 8   | CLRTXINTLVL      | R/W1TC | 0h    | <p>Clear Transmitter interrupt level.</p> <p>This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the transmitter interrupt level to the INT0 line.</p> <p>0      Interrupt level mapped to INT0 line.<br/> 1      Interrupt level mapped to INT1 line.<br/> Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.</p>                                                                   |
| 7   | CLRTOA3WUSINTLVL | R/W1TC | 0h    | <p>Clear Timeout After 3 Wakeup Signals interrupt level.</p> <p>This bit is effective in LIN mode only. Writing to this bit maps the timeout after 3 wakeup signals interrupt level to the INT0 line. This field is writable in LIN mode only.</p> <p>0      Interrupt level mapped to INT0 line.<br/> 1      Interrupt level mapped to INT1 line.<br/> Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.</p> |
| 6   | CLRTOAWUSINTLVL  | R/W1TC | 0h    | <p>Clear Timeout After Wakeup Signal interrupt level.</p> <p>This bit is effective in LIN mode only. Writing to this bit maps the the timeout after wakeup interrupt level to the INT0 line. This field is writable in LIN mode only.</p> <p>0      Interrupt level mapped to INT0 line.<br/> 1      Interrupt level mapped to INT1 line.<br/> Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.</p>          |
| 5   | RESERVED_2       | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 4   | CLRTIMEOUTINTLVL | R/W1TC | 0h    | <p>Clear Timeout interrupt level.</p> <p>This bit is effective in LIN mode only. Writing to this bit maps the timeout interrupt level to the INT0 line. This field is writable in LIN mode only.</p> <p>0      Interrupt level mapped to INT0 line.<br/> 1      Interrupt level mapped to INT1 line.<br/> Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.</p>                                               |
| 3:2 | RESERVED_1       | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 1   | CLRWAKEUPINTLVL  | R/W1TC | 0h    | <p>Clear Wake-up interrupt level.</p> <p>This bit is effective in LIN or SCI-compatible mode. Writing to this bit maps the Wake-up interrupt level to the INT0 line.</p> <p>0      Interrupt level mapped to INT0 line.<br/> Writing a 0 to this bit has no effect.<br/> 1      Interrupt level mapped to INT1 line.<br/> Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.</p>                               |
| 0   | CLRBKDTINTLVL    | R/W1TC | 0h    | <p>Clear Break-detect interrupt level.</p> <p>This bit is effective in SCI-compatible mode only. Writing to this bit maps the Break-detect interrupt level to the INT0 line. This field is writable in SCI mode only.</p> <p>0      Interrupt level mapped to INT0 line.<br/> 1      Interrupt level mapped to INT1 line.<br/> Writing a 1 to this bit will map the interrupt to INT0 and clear this bit.</p>                          |

### 5.11.2.8 LIN\_SCIFLR Register

#### 1 LIN\_SCIFLR Register (Offset = 1Ch) [reset = 904h]

The SCIFLR register indicates the current status of the various interrupt sources of the LIN module.

Return to [Summary Table](#)

**Table 5-1945. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 001Ch       |
| LIN1          | 5240 101Ch       |
| LIN2          | 5240 201Ch       |
| LIN3          | 5240 301Ch       |
| LIN4          | 5240 401Ch       |

**Figure 5-644. LIN\_SCIFLR Name Register**

|            |          |            |         |         |        |        |        |
|------------|----------|------------|---------|---------|--------|--------|--------|
| 31         | 30       | 29         | 28      | 27      | 26     | 25     | 24     |
| BE         | PBE      | CE         | ISFE    | NRE     | FE     | OE     | PE     |
| R/W1TC     | R/W1TC   | R/W1TC     | R/W1TC  | R/W1TC  | R/W1TC | R/W1TC | R/W1TC |
| 0h         | 0h       | 0h         | 0h      | 0h      | 0h     | 0h     | 0h     |
| 23         | 22       | 21         | 20      | 19      | 18     | 17     | 16     |
| RESERVED_3 |          |            |         |         |        |        |        |
| R          |          |            |         |         |        |        |        |
| 0h         |          |            |         |         |        |        |        |
| 15         | 14       | 13         | 12      | 11      | 10     | 9      | 8      |
| RESERVED_2 | IDRXFLAG | IDTXFLAG   | RXWAKE  | TXEMPTY | TXWAKE | RXRDY  | TXRDY  |
| R          | R/W1TC   | R/W1TC     | R       | R       | R/W    | R/W1TC | R      |
| 0h         | 0h       | 0h         | 0h      | 1h      | 0h     | 0h     | 1h     |
| 7          | 6        | 5          | 4       | 3       | 2      | 1      | 0      |
| TOA3WUS    | TOAWUS   | RESERVED_1 | TIMEOUT | BUSY    | IDLE   | WAKEUP | BRKDT  |
| R/W1TC     | R/W1TC   | R          | R/W1TC  | R       | R      | R/W1TC | R/W1TC |
| 0h         | 0h       | 0h         | 0h      | 0h      | 1h     | 0h     | 0h     |

**Table 5-1947. LIN\_SCIFLR Register Field Descriptions**

| Bit | Field | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|-------|--------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31  | BE    | R/W1TC | 0h    | <p>Bit Error Flag.</p> <p>This bit is effective in LIN mode only. This bit is set when there has been a bit error. This is detected by the bit monitor in the internal bit monitor. This bit is cleared by:</p> <ul style="list-style-type: none"> <li>- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register</li> <li>- Setting the SWnRESET bit [SCIGCR1.7]</li> <li>- RESET bit [SCIGCR0.0]</li> <li>- System reset</li> <li>- Writing a 1 to this bit</li> <li>- Reception of a new sync break</li> </ul> <p>This field is writable in LIN mode only.</p> <p>0 No bit error detected.</p> <p>1 Bit error detected.</p> |

**Table 5-1947. LIN\_SCIFLR Register Field Descriptions (continued)**

| Bit | Field | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-----|-------|--------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 30  | PBE   | R/W1TC | 0h    | <p>Physical Bus Error Flag.</p> <p>This bit is effective in LIN mode only. This bit is set when there has been a physical bus error. This is detected by the bit monitor in TED. This bit is cleared by:</p> <ul style="list-style-type: none"> <li>- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register</li> <li>- Setting the SWnRESET bit [SCIGCR1.7]</li> <li>- RESET bit [SCIGCR0.0]</li> <li>- System reset</li> <li>- Writing a 1 to this bit</li> <li>- Reception of a new sync break</li> </ul> <p>Note: this PBE will only be flagged if no sync break can be generated. [because of a bus shortage to VBAT] or if no sync break delimiter can be generated [because of a bus shortage to GND]. This field is writable in LIN mode only.</p> <p>0 No physical bus error detected.<br/>1 Physical bus error detected.</p> |
| 29  | CE    | R/W1TC | 0h    | <p>Checksum Error Flag.</p> <p>This bit is effective in LIN mode only. This bit is set when there is checksum error detected by a receiving node. The type of checksum to be used depends on the SCIGCR1.CTYPE bit. This bit is cleared by:</p> <ul style="list-style-type: none"> <li>- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register</li> <li>- Setting the SWnRESET bit [SCIGCR1.7]</li> <li>- RESET bit [SCIGCR0.0]</li> <li>- System reset</li> <li>- Writing a 1 to this bit</li> <li>- Reception of a new sync break</li> </ul> <p>This field is writable in LIN mode only.</p> <p>0 No Checksum error detected.<br/>1 Checksum error detected.</p>                                                                                                                                                                    |
| 28  | ISFE  | R/W1TC | 0h    | <p>Inconsistent Sync Field Error Flag.</p> <p>This bit is effective in LIN mode only. This bit is set when there has been an inconsistent Sync Field error detected by the synchronizer during header reception. See the "Header Reception and Adaptive Baudrate" section for more information. This bit is cleared by:</p> <ul style="list-style-type: none"> <li>- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register</li> <li>- Setting the SWnRESET bit [SCIGCR1.7]</li> <li>- RESET bit [SCIGCR0.0]</li> <li>- System reset</li> <li>- Writing a 1 to this bit</li> <li>- Reception of a new sync break</li> </ul> <p>This field is writable in LIN mode only.</p> <p>0 No Inconsistent Sync Field error detected.<br/>1 Inconsistent Sync Field error detected.</p>                                                          |

**Table 5-1947. LIN\_SCIFLR Register Field Descriptions (continued)**

| Bit | Field | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----|-------|--------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 27  | NRE   | R/W1TC | 0h    | <p>No-Response Error Flag.</p> <p>This bit is effective in LIN mode only. This bit is set when there is no response to a master's header completed within TFRAME_MAX. This timeout period is applied for message frames of unknown length [identifiers 0 to 61]. This error is detected by the synchronizer of the module. This bit is cleared by:</p> <ul style="list-style-type: none"> <li>- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register</li> <li>- Setting the SWnRESET bit [SCIGCR1.7]</li> <li>- RESET bit [SCIGCR0.0]</li> <li>- System reset</li> <li>- Writing a 1 to this bit</li> <li>- Reception of a new sync break</li> </ul> <p>This field is writable in LIN mode only.</p> <p>0 No No-Response error detected.<br/>1 No-Response error detected.</p>                                                                                                                                                                                         |
| 26  | FE    | R/W1TC | 0h    | <p>Framing error flag.</p> <p>This bit is effective in LIN or SCI-compatible mode. This bit is set when an expected stop bit is not found. In SCI compatible mode, only the first stop bit is checked. The missing stop bit indicates that synchronization with the start bit has been lost and that the character is incorrectly framed. Detection of a framing error causes the SCI to generate an error interrupt if the RXERR INT ENA bit is set. This bit is cleared by:</p> <ul style="list-style-type: none"> <li>- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register</li> <li>- Setting the SWnRESET bit [SCIGCR1.7]</li> <li>- RESET bit [SCIGCR0.0]</li> <li>- System reset</li> <li>- Writing a 1 to this bit</li> <li>- Reception of a new character [SCI-compatible mode], or frame [LIN mode]</li> </ul> <p>In multibuffer mode the frame is defined in the SCIFORMAT register.</p> <p>0 No framing error detected.<br/>1 Framing error detected.</p> |
| 25  | OE    | R/W1TC | 0h    | <p>Overrun error flag.</p> <p>This bit is effective in LIN or SCI-compatible mode. This bit is set when the transfer of data from SCIRXSHF to SCIRD overwrites unread data already in SCIRD or the RDy buffers. Detection of an overrun error causes the LIN to generate an error interrupt if the SET OE INT bit is one. This bit is cleared by:</p> <ul style="list-style-type: none"> <li>- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register</li> <li>- Setting the SWnRESET bit [SCIGCR1.7]</li> <li>- RESET bit [SCIGCR0.0]</li> <li>- System reset</li> <li>- Writing a 1 to this bit</li> </ul> <p>0 No overrun error detected.<br/>1 Overrun error detected.</p>                                                                                                                                                                                                                                                                                           |



**Table 5-1947. LIN\_SCIFLR Register Field Descriptions (continued)**

| Bit   | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|------------|--------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24    | PE         | R/W1TC | 0h    | <p>Parity error flag.</p> <p>This bit is effective in LIN or SCI-compatible mode. This bit is set when a parity error is detected in the received data. In SCI address-bit mode, the parity is calculated on the data and address bit fields of the received frame. In idle-line mode, only the data is used to calculate parity. An error is generated when a character is received with a mismatch between the number of 1s and its parity bit. For more information on parity checking, see the "SCI Global Control Register [SCIGCR1]" description. If the parity function is disabled [that is, SCIGCR1.2 = 0], the PE flag is disabled and read as 0. Detection of a parity error causes the LIN to generate an error interrupt if the SET PE INT bit = 1. This bit is cleared by:</p> <ul style="list-style-type: none"> <li>- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register</li> <li>- Setting the SWnRESET bit [SCIGCR1.7]</li> <li>- RESET bit [SCIGCR0.0]</li> <li>- System reset</li> <li>- Reception of a new character [SCI-compatible mode] or frame [LIN mode]</li> <li>- Writing a 1 to this bit</li> </ul> <p>0 No parity error or parity disabled.<br/>1 Parity error detected.</p> |
| 23:16 | RESERVED_3 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 15    | RESERVED_2 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 14    | IDRXFLAG   | R/W1TC | 0h    | <p>Identifier On Receive Flag.</p> <p>This bit is effective in LIN mode only. This flag is set once an identifier is received with an RX match and no ID-parity error. See the "Message Filtering and Validation" section for more details. When this flag is set it indicates that a new valid identifier has been received on an RX match. This bit is cleared by:</p> <ul style="list-style-type: none"> <li>- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register</li> <li>- Setting the SWnRESET bit [SCIGCR1.7]</li> <li>- RESET bit [SCIGCR0.0]</li> <li>- System reset</li> <li>- Reading the LINID register</li> <li>- Writing a 1 to this bit</li> </ul> <p>This field is writable in LIN mode only.</p> <p>0 No valid ID received.<br/>1 Valid ID RX received in LINID[23:16] on RX match.</p>                                                                                                                                                                                                                                                                                                                                                                                                    |
| 13    | IDTXFLAG   | R/W1TC | 0h    | <p>Identifier On Transmit Flag.</p> <p>This bit is effective in LIN mode only. This flag is set once an identifier is received with a TX match and no ID-parity error. See the "Message Filtering and Validation" section for more details. When this flag is set it indicates that a new valid identifier has been received on a TX match. This bit is cleared by:</p> <ul style="list-style-type: none"> <li>- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register</li> <li>- RESET bit [SCIGCR0.0]</li> <li>- Setting SWnRESET</li> <li>- System reset</li> <li>- Reading the LINID register</li> <li>- Writing a 1 to this bit</li> </ul> <p>This field is writable in LIN mode only.</p> <p>0 No valid ID received.<br/>1 Valid ID received in LINID[23:16] on TX match.</p>                                                                                                                                                                                                                                                                                                                                                                                                                            |

**Table 5-1947. LIN\_SCIFLR Register Field Descriptions (continued)**

| Bit | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|---------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12  | RXWAKE  | R    | 0h    | <p>Receiver wakeup detect flag.</p> <p>This bit is effective in SCI-compatible mode only. The SCI sets this bit to indicate that the data currently in SCIRD is an address. This bit is cleared by:</p> <ul style="list-style-type: none"> <li>- RESET bit</li> <li>- Setting the SWnRESET bit [SCIGCR1.7]</li> <li>- System reset</li> <li>- Receipt of a data frame</li> </ul> <p>This bit is writable in SCI mode only.</p> <p>0      The data in SCIRD is not an address.<br/> 1      The data in SCIRD is an address.<br/> See      [1] Section 3.4.4, sleep mode for Multiprocessor Communication, on page 16 for more information on using the RXWAKE bit with sleep mode.</p>                                                                                                                                                                                                                                                                                                                                                                                                  |
| 11  | TXEMPTY | R    | 1h    | <p>Transmitter Empty flag.</p> <p>The value of this flag indicates the contents of the transmitter's buffer register[s] [SCITD/TDy] and shift register [SCITXSHF]. In multibuffer mode, this flag indicates the value of the TDx registers and shift register [SCITXSHF]. In non multibuffer mode, this flag indicates the value of LINTD0 [byte] and shift register [SCITXSHF]. This bit is set by:</p> <ul style="list-style-type: none"> <li>- RESET bit [SCIGCR0.0]</li> <li>- Setting the SWnRESET bit [SCIGCR1.7]</li> <li>- System reset.</li> </ul> <p>Note: This bit does not cause an interrupt request.</p> <p>0      Compatible mode or LIN with no multibuffer:<br/> Transmitter buffer or shift register (or both) are loaded with data.<br/> In LIN mode using multibuffer mode:<br/> Multibuffer or shift register (or all) are loaded with data.<br/> 1      Compatible mode or LIN with no multibuffer:<br/> Transmitter buffer and shift registers are both empty.<br/> In LIN mode using multibuffer mode:<br/> Multibuffer and shift registers are all empty.</p> |

**Table 5-1947. LIN\_SCIFLR Register Field Descriptions (continued)**

| Bit | Field  | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|--------|--------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | TXWAKE | R/W    | 0h    | <p>SCI transmitter wakeup method select.</p> <p>This bit is effective in SCI-compatible mode only. The TXWAKE bit controls whether the data in SCITD should be sent as an address or data frame using multiprocessor communication format. This bit is set to 1 or 0 by software before a byte is written to SCITD and is cleared by the SCI when data is transferred from SCITD to SCITXSHF or by a system reset. TXWAKE is not cleared by the SWnRESET bit [SCIGCR1.7].</p> <p>0 Address-bit mode: Frame to be transmitted will be data (address bit = 0).</p> <p>Idle-line mode: Frame to be transmitted will be data.</p> <p>1 Address-bit mode: Frame to be transmitted will be an address (address bit=1).</p> <p>Idle-line mode: Following frame to be transmitted will be an address (writing a 1 to this bit followed by writing dummy data to the SCITD will result in a idle period of 11 bit periods before the next frame is transmitted).</p>                                                                                                                                                          |
| 9   | RXRDY  | R/W1TC | 0h    | <p>Receiver ready flag.</p> <p>In SCI compatibility mode, the receiver sets this bit to indicate that the SCIRD contains new data and is ready to be read by the CPU. In LIN mode, RXRDY is set once a valid frame is received in multibuffer mode, a valid frame being a message frame received with no errors. In non multibuffer mode RXRDY is set for each received byte and will be set for the last byte of the frame if there are no errors. The SCI/LIN generates a receive interrupt when RXRDY flag bit is set if the interrupt-enable bit is set [SCISSETINT.9]. RXRDY is cleared by:</p> <ul style="list-style-type: none"> <li>- RESET bit [SCIGCR0.0]</li> <li>- Setting the SWnRESET</li> <li>- System reset</li> <li>- Writing a 1 to this bit</li> <li>- Reading SCIRD in while in SCI compatibility mode</li> <li>- Reading last data byte RDy of the response in LIN mode</li> </ul> <p>Note: The RXRDY flag cannot be cleared by Reading the corresponding interrupt offset in the SCIINTVECT0/1 register.</p> <p>0 No new data in SCIRD/RDy.</p> <p>1 New data ready to be read from SCIRD.</p> |

**Table 5-1947. LIN\_SCIFLR Register Field Descriptions (continued)**

| Bit | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|------------|--------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8   | TXRDY      | R      | 1h    | <p>Transmitter buffer register ready flag.</p> <p>When set, this bit indicates that the transmit buffer[s] register [SCITD in compatibility mode and LINTD0, LINTD1 in MBUF mode] is/are ready to get another character from a CPU write.</p> <p>In SCI compatibility mode, Writing data to SCITD automatically clears this bit. In LIN mode, this bit is cleared once byte 0 [TD0] is written to LINTD0. This bit is set after the data of the TX buffer are shifted into the SCITXSHF register. This event can trigger a transmit DMA event if the DMA enable bit is set. This bit is set to 1 by:</p> <ul style="list-style-type: none"> <li>- RESET bit [SCIGCR0.0]</li> <li>- Setting the SWnRESET [SCIGCR1.7]</li> <li>- System reset</li> </ul> <p>Note: The TXRDY flag cannot be cleared by Reading the corresponding interrupt offset in the SCIINTVECT0/1 register.</p> <p>Note: The transmit interrupt request can be eliminated until the next series of data is written into the transmit buffers LINTD0 and LINTD1, by disaLINg the corresponding interrupt via the SCICLEARINT register or by disaLINg the transmitter via the TXENA bit [SCIGCR1.25=0].</p> <p>0      Compatible mode: SCITD is full.<br/>LIN<br/>mode: The multibuffers are full.</p> <p>1      Compatible mode: SCITD is ready to receive the next character.<br/>LIN mode: The multibuffers are ready to receive the next character(s).</p> |
| 7   | TOA3WUS    | R/W1TC | 0h    | <p>Timeout After 3 Wakeup Signals flag.</p> <p>This bit is effective in LIN mode only. This flag is set if there is no Sync Break received after 3 wakeup signals and a period of 1.5 seconds have passed. Such expiration time is used before issuing another round of wakeup signals. This bit is cleared by:</p> <ul style="list-style-type: none"> <li>- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register</li> <li>- Setting the SWnRESET bit [SCIGCR1.7]</li> <li>- RESET bit [SCIGCR0.0]</li> <li>- System reset</li> <li>- Writing a 1 to this bit</li> </ul> <p>This field is writable in LIN mode only.</p> <p>0      No timeout after 3 wakeup signals.<br/>1      Timeout after 3 wakeup signals and 1.5s time.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 6   | TOAWUS     | R/W1TC | 0h    | <p>Timeout After Wakeup Signal flag.</p> <p>This bit is effective in LIN mode only. This bit is set if there is no Sync Break received after a wakeup signal has been sent. A minimum of 150 ms expiration time is used before issuing another wakeup signal. This bit is cleared by:</p> <ul style="list-style-type: none"> <li>- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register</li> <li>- Setting the SWnRESET bit [SCIGCR1.7]</li> <li>- RESET bit [SCIGCR0.0]</li> <li>- System reset</li> <li>- Writing a 1 to this bit</li> </ul> <p>This field is writable in LIN mode only.</p> <p>0      No timeout after one wakeup signal (150 ms).<br/>1      Timeout after one wakeup signal.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 5   | RESERVED_1 | R      | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

**Table 5-1947. LIN\_SCIFLR Register Field Descriptions (continued)**

| Bit | Field   | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-----|---------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | TIMEOUT | R/W1TC | 0h    | <p>LIN Bus IDLE timeout flag.</p> <p>This bit is effective in LIN mode only. This bit is set if there is no LIN bus activity for at least 4 seconds. LIN bus activity being a transition from recessive to dominant. This bit is cleared by:</p> <ul style="list-style-type: none"> <li>- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register</li> <li>- Setting the SWnRESET bit [SCIGCR1.7]</li> <li>- RESET bit [SCIGCR0.0]</li> <li>- System reset</li> <li>- Writing a 1 to this bit</li> </ul> <p>This field is writable in LIN mode only.</p> <p>0 No bus idle detected.<br/>1 LIN bus idle detected.</p>                                                                                                                                                                                                                       |
| 3   | BUSY    | R      | 0h    | <p>Bus BUSY flag.</p> <p>This bit is effective in LIN mode and SCI-compatible mode. This bit indicates whether the receiver is in the process of receiving a frame. As soon as the receiver detects the beginning of a start bit, the BUSY bit is set to 1. When the reception of a frame is complete, the BUSY bit is cleared. If SET WAKEUP INT is set and power down is requested while this bit is set, the SCI/LIN automatically prevents low-power mode from being entered and generates wakeup interrupt. The BUSY bit is controlled directly by the SCI receiver but can be cleared by:</p> <ul style="list-style-type: none"> <li>- Setting the SWnRESET bit [SCIGCR1.7]</li> <li>- RESET bit [SCIGCR0.0]</li> <li>- System reset.</li> </ul> <p>0 Receiver is not currently receiving a frame.<br/>1 Receiver is currently receiving a frame.</p> |
| 2   | IDLE    | R      | 1h    | <p>SCI receiver in idle state.</p> <p>This bit is effective in SCI-compatible mode only. While this bit is set, the SCI looks for an idle period to resynchronize itself with the bit stream. The receiver does not receive any data while the bit is set. The bus must be idle for 11 bit periods to clear this bit. The SCI enters this state:</p> <ul style="list-style-type: none"> <li>- After a system reset</li> <li>- Setting the SWnRESET bit [SCIGCR1.7]</li> <li>- After coming out of power down</li> </ul> <p>This bit is writable in SCI mode only.</p> <p>0 Idle period detected, the SCI is ready to receive.<br/>1 Idle period not detected, the SCI will not receive any data.</p>                                                                                                                                                        |
| 1   | WAKEUP  | R/W1TC | 0h    | <p>Wake-up flag.</p> <p>This bit is effective in LIN mode only. This bit is set by the SCI/LIN when receiver or transmitter activity has taken the module out of power-down mode. An interrupt is generated if the SET WAKEUP INT bit [SCISETINT.1] is set. This bit is cleared by:</p> <ul style="list-style-type: none"> <li>- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register.</li> <li>- Setting the SWnRESET bit [SCIGCR1.7]</li> <li>- RESET bit [SCIGCR0.0]</li> <li>- System reset</li> <li>- Writing a 1 to this bit.</li> </ul> <p>This field is writable in LIN mode only.</p> <p>0 Do not wake up from power-down mode.<br/>1 wake up from power-down mode.</p>                                                                                                                                                        |

**Table 5-1947. LIN\_SCIFLR Register Field Descriptions (continued)**

| Bit | Field | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|-------|--------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | BRKDT | R/W1TC | 0h    | <p>SCI break-detect flag.</p> <p>This bit is effective in SCI-compatible mode only. This bit is set when the SCI detects a break condition on the LINRX pin. A break condition occurs when the LINRX pin remains continuously low for at least 10 bits after a missing first stop bit, that is, after a framing error. Detection of a break condition causes the SCI to generate an error interrupt if the BRKDT INT ENA bit is set. The BRKDT bit is cleared by the following:</p> <ul style="list-style-type: none"> <li>- Reading the corresponding interrupt offset in the SCIINTVECT0/1 register.</li> <li>- Setting the SWnRESET bit [SCIGCR1.7]</li> <li>- RESET bit [SCIGCR0.0]</li> <li>- System reset</li> <li>- By Writing a 1 to this bit.</li> </ul> <p>This bit is writable in SCI mode only.</p> <p>0        No break condition detected.<br/>1        Break condition detected.</p> |

### 5.11.2.9 LIN\_SCIINTVECT0 Register

#### 1 LIN\_SCIINTVECT0 Register (Offset = 20h) [reset = 0h]

The SCIINTVECT0 register indicates the offset for the INT0 interrupt line.

Return to [Summary Table](#)

**Table 5-1948. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 0020h       |
| LIN1          | 5240 1020h       |
| LIN2          | 5240 2020h       |
| LIN3          | 5240 3020h       |
| LIN4          | 5240 4020h       |

**Figure 5-645. LIN\_SCIINTVECT0 Name Register**

|            |    |    |    |          |    |    |    |
|------------|----|----|----|----------|----|----|----|
| 31         | 30 | 29 | 28 | 27       | 26 | 25 | 24 |
| RESERVED_2 |    |    |    |          |    |    |    |
| R          |    |    |    |          |    |    |    |
| 0h         |    |    |    |          |    |    |    |
| 23         | 22 | 21 | 20 | 19       | 18 | 17 | 16 |
| RESERVED_2 |    |    |    |          |    |    |    |
| R          |    |    |    |          |    |    |    |
| 0h         |    |    |    |          |    |    |    |
| 15         | 14 | 13 | 12 | 11       | 10 | 9  | 8  |
| RESERVED_1 |    |    |    |          |    |    |    |
| R          |    |    |    |          |    |    |    |
| 0h         |    |    |    |          |    |    |    |
| 7          | 6  | 5  | 4  | 3        | 2  | 1  | 0  |
| RESERVED_1 |    |    |    | INTVECT0 |    |    |    |
| R          |    |    |    | R        |    |    |    |
| 0h         |    |    |    | 0h       |    |    |    |

**Table 5-1950. LIN\_SCIINTVECT0 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 15:5  | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 4:0   | INTVECT0   | R    | 0h    | Interrupt vector offset for INT0.<br>This register indicates the offset for interrupt line INT0. A read to this register updates its value to the next highest priority pending interrupt in SCIFLR and clears the flag corresponding to the offset that was read.<br>Note: The flags for the receive [SCIFLR.9] and the transmit [SCIFLR.8] interrupts cannot be cleared by Reading the corresponding offset vector in this register [see detailed description in SCIFLR register]. |

### 5.11.2.10 LIN\_SCIINTVECT1 Register

#### 1 LIN\_SCIINTVECT1 Register (Offset = 24h) [reset = 0h]

The SCIINTVECT1 register indicates the offset for the INT1 interrupt line.

Return to [Summary Table](#)

**Table 5-1951. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 0024h       |
| LIN1          | 5240 1024h       |
| LIN2          | 5240 2024h       |
| LIN3          | 5240 3024h       |
| LIN4          | 5240 4024h       |

**Figure 5-646. LIN\_SCIINTVECT1 Name Register**

|            |    |    |    |          |    |    |    |
|------------|----|----|----|----------|----|----|----|
| 31         | 30 | 29 | 28 | 27       | 26 | 25 | 24 |
| RESERVED_2 |    |    |    |          |    |    |    |
| R          |    |    |    |          |    |    |    |
| 0h         |    |    |    |          |    |    |    |
| 23         | 22 | 21 | 20 | 19       | 18 | 17 | 16 |
| RESERVED_2 |    |    |    |          |    |    |    |
| R          |    |    |    |          |    |    |    |
| 0h         |    |    |    |          |    |    |    |
| 15         | 14 | 13 | 12 | 11       | 10 | 9  | 8  |
| RESERVED_1 |    |    |    |          |    |    |    |
| R          |    |    |    |          |    |    |    |
| 0h         |    |    |    |          |    |    |    |
| 7          | 6  | 5  | 4  | 3        | 2  | 1  | 0  |
| RESERVED_1 |    |    |    | INTVECT1 |    |    |    |
| R          |    |    |    | R        |    |    |    |
| 0h         |    |    |    | 0h       |    |    |    |

**Table 5-1953. LIN\_SCIINTVECT1 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 15:5  | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 4:0   | INTVECT1   | R    | 0h    | Interrupt vector offset for INT1.<br>This register indicates the offset for interrupt line INT1. A read to this register updates its value to the next highest priority pending interrupt in SCIFLR and clears the flag corresponding to the offset that was read.<br>Note: The flags for the receive [SCIFLR.9] and the transmit [SCIFLR.8] interrupts cannot be cleared by Reading the corresponding offset vector in this register [see detailed description in SCIFLR register]. |



### 5.11.2.11 LIN\_SCIFORMAT Register

#### 1 LIN\_SCIFORMAT Register (Offset = 28h) [reset = 0h]

The SCIFORMAT register is used to set up the character and frame lengths.

Return to [Summary Table](#)

**Table 5-1954. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 0028h       |
| LIN1          | 5240 1028h       |
| LIN2          | 5240 2028h       |
| LIN3          | 5240 3028h       |
| LIN4          | 5240 4028h       |

**Figure 5-647. LIN\_SCIFORMAT Name Register**

|            |    |    |    |        |    |    |    |
|------------|----|----|----|--------|----|----|----|
| 31         | 30 | 29 | 28 | 27     | 26 | 25 | 24 |
| RESERVED_2 |    |    |    |        |    |    |    |
| R          |    |    |    |        |    |    |    |
| 0h         |    |    |    |        |    |    |    |
| 23         | 22 | 21 | 20 | 19     | 18 | 17 | 16 |
| RESERVED_2 |    |    |    | LENGTH |    |    |    |
| R          |    |    |    | R/W    |    |    |    |
| 0h         |    |    |    | 0h     |    |    |    |
| 15         | 14 | 13 | 12 | 11     | 10 | 9  | 8  |
| RESERVED_1 |    |    |    |        |    |    |    |
| R          |    |    |    |        |    |    |    |
| 0h         |    |    |    |        |    |    |    |
| 7          | 6  | 5  | 4  | 3      | 2  | 1  | 0  |
| RESERVED_1 |    |    |    | CHAR   |    |    |    |
| R          |    |    |    | R/W    |    |    |    |
| 0h         |    |    |    | 0h     |    |    |    |

**Table 5-1956. LIN\_SCIFORMAT Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:19 | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 18:16 | LENGTH     | R/W  | 0h    | <p>Frame length control bits.</p> <p>In LIN mode, these bits indicate the number of bytes in the response field from 1 to 8 bytes. In buffered SCI mode, these bits indicate the number of characters. When these bits are used to indicate LIN response length [SCIGCR1[0] = 1], then when there is an ID RX match, this value should be updated with the expected length of the response. In buffered SCI mode, these bits indicate the number of characters with SCIFORMAT[2:0] bits per character. i.e. these bits indicate the transmitter/receiver format for the number of characters: 1 to 8. There can be up to eight characters with eight bits each.</p> <p>0 The response field has 1 bytes/characters.<br/> 1 The response field has 2 bytes/characters.<br/> 2 The response field has 3 bytes/characters.<br/> 3 The response field has 4 bytes/characters.<br/> 4 The response field has 5 bytes/characters.<br/> 5 The response field has 6 bytes/characters.<br/> 6 The response field has 7 bytes/characters.<br/> 7 The response field has 8 bytes/characters.</p> |

**Table 5-1956. LIN\_SCIFORMAT Register Field Descriptions (continued)**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:3 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 2:0  | CHAR       | R/W  | 0h    | <p>Character length control bits.</p> <p>These bits are effective in SCI compatible mode only. These bits set the SCI character length from 1 to 8 bits.</p> <p>Note: In compatibility mode or buffered SCI mode, when data of fewer than eight bits in length is received, it is left justified in SCIRD/RDy and padded with trailing zeros. Data read from the SCIRD should be shifted by software to make the received data right justified.</p> <p>Note: Data written to the SCITD should be right justified but does not need to be padded with leading zeros.</p> <p>These bits are writable in SCI mode only.</p> <p>0      The character is 1 bits long.<br/> 1      The character is 2 bits long.<br/> 2      The character is 3 bits long.<br/> 3      The character is 4 bits long.<br/> 4      The character is 5 bits long.<br/> 5      The character is 6 bits long.<br/> 6      The character is 7 bits long.<br/> 7      The character is 8 bits long.</p> |

### 5.11.2.12 LIN\_BRSR Register

#### 1 LIN\_BRSR Register (Offset = 2Ch) [reset = 0h]

The BRSR register is used to configure the baud rate of the LIN module.

Return to [Summary Table](#)

**Table 5-1957. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 002Ch       |
| LIN1          | 5240 102Ch       |
| LIN2          | 5240 202Ch       |
| LIN3          | 5240 302Ch       |
| LIN4          | 5240 402Ch       |

**Figure 5-648. LIN\_BRSR Name Register**

|             |    |     |    |    |    |     |    |
|-------------|----|-----|----|----|----|-----|----|
| 31          | 30 | 29  | 28 | 27 | 26 | 25  | 24 |
| RESERVED_1  |    | U   |    |    |    | M   |    |
| R           |    | R/W |    |    |    | R/W |    |
| 0h          |    | 0h  |    |    |    | 0h  |    |
| 23          | 22 | 21  | 20 | 19 | 18 | 17  | 16 |
| SCI_LIN_PSH |    |     |    |    |    |     |    |
| R/W         |    |     |    |    |    |     |    |
| 0h          |    |     |    |    |    |     |    |
| 15          | 14 | 13  | 12 | 11 | 10 | 9   | 8  |
| SCI_LIN_PSL |    |     |    |    |    |     |    |
| R/W         |    |     |    |    |    |     |    |
| 0h          |    |     |    |    |    |     |    |
| 7           | 6  | 5   | 4  | 3  | 2  | 1   | 0  |
| SCI_LIN_PSL |    |     |    |    |    |     |    |
| R/W         |    |     |    |    |    |     |    |
| 0h          |    |     |    |    |    |     |    |

**Table 5-1959. LIN\_BRSR Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                       |
| 30:28 | U          | R/W  | 0h    | Superfractional Divider Selection. [U]<br>These bits are an additional fractional part for the baudrate specification. These bits allow a super fine tuning of the fractional baudrate with 7 more intermediate values for each of the M fractional divider values. See the Superfractional Divider section for more details.                                                                  |
| 27:24 | M          | R/W  | 0h    | SCI/LIN 4-bit Fractional Divider Selection. [M]<br>These bits are effective in LIN or SCI asynchronous mode. These bits are used to select a baud rate for the SCI/LIN module, and they are a fractional part for the baud rate specification. The M divider allows fine-tuning of the baud rate over the P prescaler with 15 additional intermediate values for each of the P integer values. |

**Table 5-1959. LIN\_BRSR Register Field Descriptions (continued)**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|-------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:16 | SCI_LIN_PSH | R/W  | 0h    | <p>PRESCALER P [High Bits].</p> <p>SCI/LIN 24-bit Integer Prescaler Selection.</p> <p>These bits are used to select a baudrate for the SCI/LIN module. These bits are effective in LIN mode and SCI compatible mode. The SCI/LIN has an internally generated serial clock determined by the LIN module input clock and the prescalers P and M in this register. The SCI/LIN uses the 24-bit integer prescaler P value to select 1 of over 16,700,000 available baud rates. The additional 4-bit fractional prescaler M refines the baudrate selection.</p> |
| 15:0  | SCI_LIN_PSL | R/W  | 0h    | <p>PRESCALER P [Low Bits].</p> <p>SCI/LIN 24-bit Integer Prescaler Selection.</p> <p>These bits are used to select a baudrate for the SCI/LIN module. These bits are effective in LIN mode and SCI compatible mode. The SCI/LIN has an internally generated serial clock determined by the LIN module input clock and the prescalers P and M in this register. The SCI/LIN uses the 24-bit integer prescaler P value to select 1 of over 16,700,000 available baud rates. The additional 4-bit fractional prescaler M refines the baudrate selection.</p>  |

### 5.11.2.13 LIN\_SCIED Register

#### 1 LIN\_SCIED Register (Offset = 30h) [reset = 0h]

The SCIED register is a duplicate copy of SCIRD register that has no effect on the RXRDY flag for use with an emulator.

Return to [Summary Table](#)

**Table 5-1960. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 0030h       |
| LIN1          | 5240 1030h       |
| LIN2          | 5240 2030h       |
| LIN3          | 5240 3030h       |
| LIN4          | 5240 4030h       |

**Figure 5-649. LIN\_SCIED Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_1 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_1 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_1 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ED         |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-1962. LIN\_SCIED Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                    |
|------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                       |
| 7:0  | ED         | R    | 0h    | Receiver Emulation Data.<br>This bit is effective in SCI-compatible mode only. Reading SCIED[7-0] does not clear the RXRDY flag. This register should be used only by an emulator that must continually read the data buffer without affecting the RXRDY flag. |

### 5.11.2.14 LIN\_SCIRD Register

#### 1 LIN\_SCIRD Register (Offset = 34h) [reset = 0h]

The SCIRD register is where received data is stored and can be read from.

Return to [Summary Table](#)

**Table 5-1963. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 0034h       |
| LIN1          | 5240 1034h       |
| LIN2          | 5240 2034h       |
| LIN3          | 5240 3034h       |
| LIN4          | 5240 4034h       |

**Figure 5-650. LIN\_SCIRD Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_1 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_1 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_1 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RD         |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-1965. LIN\_SCIRD Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 7:0  | RD         | R    | 0h    | Received Data.<br>This bit is effective in SCI-compatible mode only. When a frame has been completely received, the data in the frame is transferred from the receiver shift register SCIRXSHF to this register. As this transfer occurs, the RXRDY flag is set and a receive interrupt is generated if RX INT ENA [SCISSETINT0.9] is set. When the data is read from SCIRD, the RXRDY flag is automatically cleared.<br>When the SCI receives data that is fewer than eight bits in length, it loads the data into this register in a left justified format padded with trailing zeros. Therefore, your software should perform a logical shift on the data by the correct number of positions to make it right justified. |

### 5.11.2.15 LIN\_SCITD Register

#### 1 LIN\_SCITD Register (Offset = 38h) [reset = 0h]

The SCITD register is where data to be transmitted is written to by application software.

Return to [Summary Table](#)

**Table 5-1966. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 0038h       |
| LIN1          | 5240 1038h       |
| LIN2          | 5240 2038h       |
| LIN3          | 5240 3038h       |
| LIN4          | 5240 4038h       |

**Figure 5-651. LIN\_SCITD Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_1 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_1 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_1 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TD         |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-1968. LIN\_SCITD Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 7:0  | TD         | R/W  | 0h    | Transmit data<br>This bit is effective in SCI-compatible mode only. Data to be transmitted is written to this register. The transfer of data from this register to the transmit shift register SCITXSHF sets the TXRDY flag [SCIFLR.23], which indicates that SCITD is ready to be loaded with another byte of data. Note: If TX INT ENA [SCISSETINT.8] is set, this data transfer also causes an interrupt.<br>Note: Data written to the SCIRD register that is fewer than eight bits long must be right justified, but it does not need to be padded with leading zeros. |

### 5.11.2.16 LIN\_SCIPIO0 Register

#### 1 LIN\_SCIPIO0 Register (Offset = 3Ch) [reset = 0h]

The SCIPIO0 register is used to enable the LINTX and LINRX pins.

Return to [Summary Table](#)

**Table 5-1969. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 003Ch       |
| LIN1          | 5240 103Ch       |
| LIN2          | 5240 203Ch       |
| LIN3          | 5240 303Ch       |
| LIN4          | 5240 403Ch       |

**Figure 5-652. LIN\_SCIPIO0 Name Register**

|            |    |    |    |    |        |        |            |
|------------|----|----|----|----|--------|--------|------------|
| 31         | 30 | 29 | 28 | 27 | 26     | 25     | 24         |
| RESERVED_3 |    |    |    |    |        |        |            |
| R          |    |    |    |    |        |        |            |
| 0h         |    |    |    |    |        |        |            |
| 23         | 22 | 21 | 20 | 19 | 18     | 17     | 16         |
| RESERVED_3 |    |    |    |    |        |        |            |
| R          |    |    |    |    |        |        |            |
| 0h         |    |    |    |    |        |        |            |
| 15         | 14 | 13 | 12 | 11 | 10     | 9      | 8          |
| RESERVED_2 |    |    |    |    |        |        |            |
| R          |    |    |    |    |        |        |            |
| 0h         |    |    |    |    |        |        |            |
| 7          | 6  | 5  | 4  | 3  | 2      | 1      | 0          |
| RESERVED_2 |    |    |    |    | TXFUNC | RXFUNC | RESERVED_1 |
| R          |    |    |    |    | R/W    | R/W    | R          |
| 0h         |    |    |    |    | 0h     | 0h     | 0h         |

**Table 5-1971. LIN\_SCIPIO0 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                   |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED_3 | R    | 0h    | Reserved                                                                                                                                                                      |
| 15:3  | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                      |
| 2     | TXFUNC     | R/W  | 0h    | Transmit pin function.<br>This bit is effective in LIN or SCI mode. This bit defines the function of LINTX pin.<br><br>0 LINTX pin is disabled.<br>1 LINTX pin is enabled.    |
| 1     | RXFUNC     | R/W  | 0h    | Receive pin function.<br>This bit is effective in LIN or SCI mode. This bit defines the function of the LINRX pin.<br><br>0 LINRX pin is disabled.<br>1 LINRX pin is enabled. |
| 0     | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                      |



### 5.11.2.17 LIN\_SCIPIO1 Register

#### 1 LIN\_SCIPIO1 Register (Offset = 40h) [reset = 0h]

Pin control Register 1

Return to [Summary Table](#)

**Table 5-1972. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 0040h       |
| LIN1          | 5240 1040h       |
| LIN2          | 5240 2040h       |
| LIN3          | 5240 3040h       |
| LIN4          | 5240 4040h       |

**Figure 5-653. LIN\_SCIPIO1 Name Register**

|            |    |    |    |    |       |       |            |
|------------|----|----|----|----|-------|-------|------------|
| 31         | 30 | 29 | 28 | 27 | 26    | 25    | 24         |
| RESERVED_3 |    |    |    |    |       |       |            |
| R          |    |    |    |    |       |       |            |
| 0h         |    |    |    |    |       |       |            |
| 23         | 22 | 21 | 20 | 19 | 18    | 17    | 16         |
| RESERVED_3 |    |    |    |    |       |       |            |
| R          |    |    |    |    |       |       |            |
| 0h         |    |    |    |    |       |       |            |
| 15         | 14 | 13 | 12 | 11 | 10    | 9     | 8          |
| RESERVED_2 |    |    |    |    |       |       |            |
| R          |    |    |    |    |       |       |            |
| 0h         |    |    |    |    |       |       |            |
| 7          | 6  | 5  | 4  | 3  | 2     | 1     | 0          |
| RESERVED_2 |    |    |    |    | TXDIR | RXDIR | RESERVED_1 |
| R          |    |    |    |    | R/W   | R/W   | R          |
| 0h         |    |    |    |    | 0h    | 0h    | 0h         |

**Table 5-1974. LIN\_SCIPIO1 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                            |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED_3 | R    | 0h    | Reserved                                                                                                                                                                                                                                                               |
| 15:3  | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                               |
| 2     | TXDIR      | R/W  | 0h    | Transmit pin direction.<br>This bit is effective in LIN or SCI mode. This bit determines the data direction on the LINTX pin if it is configured with general-purpose I/O functionality [TX FUNC = 0].<br>0:general purpose input pin.<br>1:general-purpose output pin |
| 1     | RXDIR      | R/W  | 0h    | Receive pin direction.<br>This bit is effective in LIN or SCI mode. This bit determines the data direction on the LINRX pin if it is configured with general-purpose I/O functionality [RX FUNC = 0].<br>0:general purpose input pin.<br>1:general-purpose output pin  |
| 0     | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                               |

### 5.11.2.18 LIN\_SCIPIO2 Register

#### 1 LIN\_SCIPIO2 Register (Offset = 44h) [reset = 0h]

The SCIO2 register indicates the current status of the LINTX and LINRX pins.

Return to [Summary Table](#)

**Table 5-1975. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 0044h       |
| LIN1          | 5240 1044h       |
| LIN2          | 5240 2044h       |
| LIN3          | 5240 3044h       |
| LIN4          | 5240 4044h       |

**Figure 5-654. LIN\_SCIPIO2 Name Register**

|            |    |    |    |    |      |      |            |
|------------|----|----|----|----|------|------|------------|
| 31         | 30 | 29 | 28 | 27 | 26   | 25   | 24         |
| RESERVED_3 |    |    |    |    |      |      |            |
| R          |    |    |    |    |      |      |            |
| 0h         |    |    |    |    |      |      |            |
| 23         | 22 | 21 | 20 | 19 | 18   | 17   | 16         |
| RESERVED_3 |    |    |    |    |      |      |            |
| R          |    |    |    |    |      |      |            |
| 0h         |    |    |    |    |      |      |            |
| 15         | 14 | 13 | 12 | 11 | 10   | 9    | 8          |
| RESERVED_2 |    |    |    |    |      |      |            |
| R          |    |    |    |    |      |      |            |
| 0h         |    |    |    |    |      |      |            |
| 7          | 6  | 5  | 4  | 3  | 2    | 1    | 0          |
| RESERVED_2 |    |    |    |    | TXIN | RXIN | RESERVED_1 |
| R          |    |    |    |    | R    | R    | R          |
| 0h         |    |    |    |    | 0h   | 0h   | 0h         |

**Table 5-1977. LIN\_SCIPIO2 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                     |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED_3 | R    | 0h    | Reserved                                                                                                                        |
| 15:3  | RESERVED_2 | R    | 0h    | Reserved                                                                                                                        |
| 2     | TXIN       | R    | 0h    | Transmit data in.<br>This bit is effective in LIN or SCI-compatible mode. This bit contains the current value on the LINTX pin. |
| 1     | RXIN       | R    | 0h    | Receive data in.<br>This bit is effective in LIN or SCI-compatible mode. This bit contains the current value on the LINRX pin.  |
| 0     | RESERVED_1 | R    | 0h    | Reserved                                                                                                                        |

### 5.11.2.19 LIN\_SCIPIO3 Register

#### 1 LIN\_SCIPIO3 Register (Offset = 48h) [reset = 0h]

Pin control Register 3

Return to [Summary Table](#)

**Table 5-1978. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 0048h       |
| LIN1          | 5240 1048h       |
| LIN2          | 5240 2048h       |
| LIN3          | 5240 3048h       |
| LIN4          | 5240 4048h       |

**Figure 5-655. LIN\_SCIPIO3 Name Register**

|            |    |    |    |    |       |       |            |
|------------|----|----|----|----|-------|-------|------------|
| 31         | 30 | 29 | 28 | 27 | 26    | 25    | 24         |
| RESERVED_3 |    |    |    |    |       |       |            |
| R          |    |    |    |    |       |       |            |
| 0h         |    |    |    |    |       |       |            |
| 23         | 22 | 21 | 20 | 19 | 18    | 17    | 16         |
| RESERVED_3 |    |    |    |    |       |       |            |
| R          |    |    |    |    |       |       |            |
| 0h         |    |    |    |    |       |       |            |
| 15         | 14 | 13 | 12 | 11 | 10    | 9     | 8          |
| RESERVED_2 |    |    |    |    |       |       |            |
| R          |    |    |    |    |       |       |            |
| 0h         |    |    |    |    |       |       |            |
| 7          | 6  | 5  | 4  | 3  | 2     | 1     | 0          |
| RESERVED_2 |    |    |    |    | TXOUT | RXOUT | RESERVED_1 |
| R          |    |    |    |    | R/W   | R/W   | R          |
| 0h         |    |    |    |    | 0h    | 0h    | 0h         |

**Table 5-1980. LIN\_SCIPIO3 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                            |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED_3 | R    | 0h    | Reserved                                                                                                               |
| 15:3  | RESERVED_2 | R    | 0h    | Reserved                                                                                                               |
| 2     | TXOUT      | R/W  | 0h    | Transmit pin out.<br>This bit is effective in LIN or SCI mode. This pin specifies the logic to be output on pin LINTX. |
| 1     | RXOUT      | R/W  | 0h    | Receive pin out.<br>This bit is effective in LIN or SCI mode. This pin specifies the logic to be output on pin LINRX.  |
| 0     | RESERVED_1 | R    | 0h    | Reserved                                                                                                               |

### 5.11.2.20 LIN\_SCIPIO4 Register

#### 1 LIN\_SCIPIO4 Register (Offset = 4Ch) [reset = 0h]

Pin control Register 4

Return to [Summary Table](#)

**Table 5-1981. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 004Ch       |
| LIN1          | 5240 104Ch       |
| LIN2          | 5240 204Ch       |
| LIN3          | 5240 304Ch       |
| LIN4          | 5240 404Ch       |

**Figure 5-656. LIN\_SCIPIO4 Name Register**

|            |    |    |    |    |        |        |            |
|------------|----|----|----|----|--------|--------|------------|
| 31         | 30 | 29 | 28 | 27 | 26     | 25     | 24         |
| RESERVED_3 |    |    |    |    |        |        |            |
| R          |    |    |    |    |        |        |            |
| 0h         |    |    |    |    |        |        |            |
| 23         | 22 | 21 | 20 | 19 | 18     | 17     | 16         |
| RESERVED_3 |    |    |    |    |        |        |            |
| R          |    |    |    |    |        |        |            |
| 0h         |    |    |    |    |        |        |            |
| 15         | 14 | 13 | 12 | 11 | 10     | 9      | 8          |
| RESERVED_2 |    |    |    |    |        |        |            |
| R          |    |    |    |    |        |        |            |
| 0h         |    |    |    |    |        |        |            |
| 7          | 6  | 5  | 4  | 3  | 2      | 1      | 0          |
| RESERVED_2 |    |    |    |    | TXSET  | RXSET  | RESERVED_1 |
| R          |    |    |    |    | R/W1TS | R/W1TS | R          |
| 0h         |    |    |    |    | 0h     | 0h     | 0h         |

**Table 5-1983. LIN\_SCIPIO4 Register Field Descriptions**

| Bit   | Field      | Type   | Reset | Description                                                                                                       |
|-------|------------|--------|-------|-------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED_3 | R      | 0h    | Reserved                                                                                                          |
| 15:3  | RESERVED_2 | R      | 0h    | Reserved                                                                                                          |
| 2     | TXSET      | R/W1TS | 0h    | Transmit pin set.<br>This bit is effective in LIN or SCI mode. This bit sets the logic to be output on pin LINTX. |
| 1     | RXSET      | R/W1TS | 0h    | Receive pin set.<br>This bit is effective in LIN or SCI mode. This bit sets the logic to be output on pin LINRX.  |
| 0     | RESERVED_1 | R      | 0h    | Reserved                                                                                                          |

### 5.11.2.21 LIN\_SCIPIO5 Register

#### 1 LIN\_SCIPIO5 Register (Offset = 50h) [reset = 0h]

Pin control Register 5

Return to [Summary Table](#)

**Table 5-1984. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 0050h       |
| LIN1          | 5240 1050h       |
| LIN2          | 5240 2050h       |
| LIN3          | 5240 3050h       |
| LIN4          | 5240 4050h       |

**Figure 5-657. LIN\_SCIPIO5 Name Register**

|            |    |    |    |    |        |        |            |
|------------|----|----|----|----|--------|--------|------------|
| 31         | 30 | 29 | 28 | 27 | 26     | 25     | 24         |
| RESERVED_3 |    |    |    |    |        |        |            |
| R          |    |    |    |    |        |        |            |
| 0h         |    |    |    |    |        |        |            |
| 23         | 22 | 21 | 20 | 19 | 18     | 17     | 16         |
| RESERVED_3 |    |    |    |    |        |        |            |
| R          |    |    |    |    |        |        |            |
| 0h         |    |    |    |    |        |        |            |
| 15         | 14 | 13 | 12 | 11 | 10     | 9      | 8          |
| RESERVED_2 |    |    |    |    |        |        |            |
| R          |    |    |    |    |        |        |            |
| 0h         |    |    |    |    |        |        |            |
| 7          | 6  | 5  | 4  | 3  | 2      | 1      | 0          |
| RESERVED_2 |    |    |    |    | TXCLR  | RXCLR  | RESERVED_1 |
| R          |    |    |    |    | R/W1TC | R/W1TC | R          |
| 0h         |    |    |    |    | 0h     | 0h     | 0h         |

**Table 5-1986. LIN\_SCIPIO5 Register Field Descriptions**

| Bit   | Field      | Type   | Reset | Description                                                                                                           |
|-------|------------|--------|-------|-----------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED_3 | R      | 0h    | Reserved                                                                                                              |
| 15:3  | RESERVED_2 | R      | 0h    | Reserved                                                                                                              |
| 2     | TXCLR      | R/W1TC | 0h    | Transmit pin clear.<br>This bit is effective in LIN or SCI mode. This bit clears the logic to be output on pin LINTX. |
| 1     | RXCLR      | R/W1TC | 0h    | Receive pin clear.<br>This bit is effective in LIN or SCI mode. This bit clears the logic to be output on pin LINRX.  |
| 0     | RESERVED_1 | R      | 0h    | Reserved                                                                                                              |

### 5.11.2.22 LIN\_SCIPIO6 Register

#### 1 LIN\_SCIPIO6 Register (Offset = 54h) [reset = 0h]

Pin control Register 6

Return to [Summary Table](#)

**Table 5-1987. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 0054h       |
| LIN1          | 5240 1054h       |
| LIN2          | 5240 2054h       |
| LIN3          | 5240 3054h       |
| LIN4          | 5240 4054h       |

**Figure 5-658. LIN\_SCIPIO6 Name Register**

|            |    |    |    |    |       |       |            |
|------------|----|----|----|----|-------|-------|------------|
| 31         | 30 | 29 | 28 | 27 | 26    | 25    | 24         |
| RESERVED_3 |    |    |    |    |       |       |            |
| R          |    |    |    |    |       |       |            |
| 0h         |    |    |    |    |       |       |            |
| 23         | 22 | 21 | 20 | 19 | 18    | 17    | 16         |
| RESERVED_3 |    |    |    |    |       |       |            |
| R          |    |    |    |    |       |       |            |
| 0h         |    |    |    |    |       |       |            |
| 15         | 14 | 13 | 12 | 11 | 10    | 9     | 8          |
| RESERVED_2 |    |    |    |    |       |       |            |
| R          |    |    |    |    |       |       |            |
| 0h         |    |    |    |    |       |       |            |
| 7          | 6  | 5  | 4  | 3  | 2     | 1     | 0          |
| RESERVED_2 |    |    |    |    | TXPDR | RXPDR | RESERVED_1 |
| R          |    |    |    |    | R/W   | R/W   | R          |
| 0h         |    |    |    |    | 0h    | 0h    | 0h         |

**Table 5-1989. LIN\_SCIPIO6 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                  |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED_3 | R    | 0h    | Reserved                                                                                                                                     |
| 15:3  | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                     |
| 2     | TXPDR      | R/W  | 0h    | Transmit pin open drain enable.<br>This bit is effective in LIN or SCI mode. This bit enables open-drain capability in the output pin LINTX. |
| 1     | RXPDR      | R/W  | 0h    | Receive pin open drain enable.<br>This bit is effective in LIN or SCI mode. This bit enables open-drain capability in the output pin LINRX.  |
| 0     | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                     |

### 5.11.2.23 LIN\_SCIPIO7 Register

#### 1 LIN\_SCIPIO7 Register (Offset = 58h) [reset = 0h]

Pin control Register 7

Return to [Summary Table](#)

**Table 5-1990. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 0058h       |
| LIN1          | 5240 1058h       |
| LIN2          | 5240 2058h       |
| LIN3          | 5240 3058h       |
| LIN4          | 5240 4058h       |

**Figure 5-659. LIN\_SCIPIO7 Name Register**

|            |    |    |    |    |      |      |            |
|------------|----|----|----|----|------|------|------------|
| 31         | 30 | 29 | 28 | 27 | 26   | 25   | 24         |
| RESERVED_3 |    |    |    |    |      |      |            |
| R          |    |    |    |    |      |      |            |
| 0h         |    |    |    |    |      |      |            |
| 23         | 22 | 21 | 20 | 19 | 18   | 17   | 16         |
| RESERVED_3 |    |    |    |    |      |      |            |
| R          |    |    |    |    |      |      |            |
| 0h         |    |    |    |    |      |      |            |
| 15         | 14 | 13 | 12 | 11 | 10   | 9    | 8          |
| RESERVED_2 |    |    |    |    |      |      |            |
| R          |    |    |    |    |      |      |            |
| 0h         |    |    |    |    |      |      |            |
| 7          | 6  | 5  | 4  | 3  | 2    | 1    | 0          |
| RESERVED_2 |    |    |    |    | TXPD | RXPD | RESERVED_1 |
| R          |    |    |    |    | R/W  | R/W  | R          |
| 0h         |    |    |    |    | 0h   | 0h   | 0h         |

**Table 5-1992. LIN\_SCIPIO7 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                       |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED_3 | R    | 0h    | Reserved                                                                                                                                          |
| 15:3  | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                          |
| 2     | TXPD       | R/W  | 0h    | Transmit pin pull control disable.<br>This bit is effective in LIN or SCI mode. This bit disables pull control capability on the input pin LINTX. |
| 1     | RXPD       | R/W  | 0h    | Receive pin pull control disable.<br>This bit is effective in LIN or SCI mode. This bit disables pull control capability on the input pin LINRX.  |
| 0     | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                          |

### 5.11.2.24 LIN\_SCIPIO8 Register

#### 1 LIN\_SCIPIO8 Register (Offset = 5Ch) [reset = 7h]

Pin control Register 8

Return to [Summary Table](#)

**Table 5-1993. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 005Ch       |
| LIN1          | 5240 105Ch       |
| LIN2          | 5240 205Ch       |
| LIN3          | 5240 305Ch       |
| LIN4          | 5240 405Ch       |

**Figure 5-660. LIN\_SCIPIO8 Name Register**

|            |    |    |    |    |       |       |            |
|------------|----|----|----|----|-------|-------|------------|
| 31         | 30 | 29 | 28 | 27 | 26    | 25    | 24         |
| RESERVED_3 |    |    |    |    |       |       |            |
| R          |    |    |    |    |       |       |            |
| 0h         |    |    |    |    |       |       |            |
| 23         | 22 | 21 | 20 | 19 | 18    | 17    | 16         |
| RESERVED_3 |    |    |    |    |       |       |            |
| R          |    |    |    |    |       |       |            |
| 0h         |    |    |    |    |       |       |            |
| 15         | 14 | 13 | 12 | 11 | 10    | 9     | 8          |
| RESERVED_2 |    |    |    |    |       |       |            |
| R          |    |    |    |    |       |       |            |
| 0h         |    |    |    |    |       |       |            |
| 7          | 6  | 5  | 4  | 3  | 2     | 1     | 0          |
| RESERVED_2 |    |    |    |    | TXPSL | RXPSL | RESERVED_1 |
| R          |    |    |    |    | R/W   | R/W   | R          |
| 0h         |    |    |    |    | 1h    | 1h    | 1h         |

**Table 5-1995. LIN\_SCIPIO8 Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                         |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED_3 | R    | 0h    | Reserved                                                                                                            |
| 15:3  | RESERVED_2 | R    | 0h    | Reserved                                                                                                            |
| 2     | TXPSL      | R/W  | 1h    | TX pin pull select.<br>This bit is effective in LIN or SCI mode. This bit selects pull type in the input pin LINTX. |
| 1     | RXPSL      | R/W  | 1h    | RX pin pull select.<br>This bit is effective in LIN or SCI mode. This bit selects pull type in the input pin LINRX. |
| 0     | RESERVED_1 | R    | 1h    | Reserved                                                                                                            |



### 5.11.2.25 LIN\_LINCOMP Register

#### 1 LIN\_LINCOMP Register (Offset = 60h) [reset = 0h]

The LINCOMPARE register is used to configure the sync delimiter and sync break extension.

Return to [Summary Table](#)

**Table 5-1996. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 0060h       |
| LIN1          | 5240 1060h       |
| LIN2          | 5240 2060h       |
| LIN3          | 5240 3060h       |
| LIN4          | 5240 4060h       |

**Figure 5-661. LIN\_LINCOMP Name Register**

|            |    |    |    |    |        |      |    |
|------------|----|----|----|----|--------|------|----|
| 31         | 30 | 29 | 28 | 27 | 26     | 25   | 24 |
| RESERVED_3 |    |    |    |    |        |      |    |
| R          |    |    |    |    |        |      |    |
| 0h         |    |    |    |    |        |      |    |
| 23         | 22 | 21 | 20 | 19 | 18     | 17   | 16 |
| RESERVED_3 |    |    |    |    |        |      |    |
| R          |    |    |    |    |        |      |    |
| 0h         |    |    |    |    |        |      |    |
| 15         | 14 | 13 | 12 | 11 | 10     | 9    | 8  |
| RESERVED_2 |    |    |    |    |        | SDEL |    |
| R          |    |    |    |    |        | R/W  |    |
| 0h         |    |    |    |    |        | 0h   |    |
| 7          | 6  | 5  | 4  | 3  | 2      | 1    | 0  |
| RESERVED_1 |    |    |    |    | SBREAK |      |    |
| R          |    |    |    |    | R/W    |      |    |
| 0h         |    |    |    |    | 0h     |      |    |

**Table 5-1998. LIN\_LINCOMP Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED_3 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 15:10 | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 9:8   | SDEL       | R/W  | 0h    | 2-bit Sync Delimiter compare.<br>These bits are effective in LIN mode only. These bits are used to configure the number of Tbit for the sync delimiter in the sync field. The time delay calculation for the synchronization delimiter is: $TSDEL = [SDEL + 1]Tbit$<br>These bits are writable in LIN mode only.<br>0 The sync delimiter has 1 Tbit.<br>1 The sync delimiter has 2 Tbit.<br>2 The sync delimiter has 3 Tbit.<br>3 The sync delimiter has 4 Tbit. |
| 7:3   | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

**Table 5-1998. LIN\_LINCOMP Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-----|--------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0 | SBREAK | R/W  | 0h    | <p>3-bit Sync Break extend.</p> <p>LIN mode only. These bits are used to configure the number of Tbits for the sync break to extend the minimum 13 Tbit in the Sync Field to a maximum of 20 Tbit.</p> <p>The time delay calculation for the sync break is:<br/> <math>TSYNBRK = 13Tbit + SBREAK \times Tbit</math></p> <p>These bits are writable in LIN mode only.</p> <p>0      The sync break has no additional Tbit.<br/> 1      The sync break has 1 additional Tbit.<br/> 2      The sync break has 2 additional Tbit.<br/> 3      The sync break has 3 additional Tbit.<br/> 4      The sync break has 4 additional Tbit.<br/> 5      The sync break has 5 additional Tbit.<br/> 6      The sync break has 6 additional Tbit.<br/> 7      The sync break has 7 additional Tbit.</p> |

### 5.11.2.26 LIN\_LINRD0 Register

#### 1 LIN\_LINRD0 Register (Offset = 64h) [reset = 0h]

The LINRD0 register contains the lower 4 bytes of the received LIN frame data.

Return to [Summary Table](#)

**Table 5-1999. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 0064h       |
| LIN1          | 5240 1064h       |
| LIN2          | 5240 2064h       |
| LIN3          | 5240 3064h       |
| LIN4          | 5240 4064h       |

**Figure 5-662. LIN\_LINRD0 Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RD0 |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RD1 |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RD2 |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RD3 |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 5-2001. LIN\_LINRD0 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                             |
|-------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RD0   | R    | 0h    | 8-bit Receive Buffer 0<br>Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.<br>A read of this byte clears the RXDY byte.<br>Note: RD<x-1> is equivalent to Data byte <x> of the LIN frame. |
| 23:16 | RD1   | R    | 0h    | 8-bit Receive Buffer 1.<br>Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.                                                                                                               |
| 15:8  | RD2   | R    | 0h    | 8-bit Receive Buffer 2.<br>Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.                                                                                                               |
| 7:0   | RD3   | R    | 0h    | 8-bit Receive Buffer 3.<br>Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.                                                                                                               |

### 5.11.2.27 LIN\_LINRD1 Register

#### 1 LIN\_LINRD1 Register (Offset = 68h) [reset = 0h]

The LINRD1 register contains the upper 4 bytes of the received LIN frame data.

Return to [Summary Table](#)

**Table 5-2002. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 0068h       |
| LIN1          | 5240 1068h       |
| LIN2          | 5240 2068h       |
| LIN3          | 5240 3068h       |
| LIN4          | 5240 4068h       |

**Figure 5-663. LIN\_LINRD1 Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RD4 |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RD5 |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RD6 |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RD7 |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 5-2004. LIN\_LINRD1 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                               |
|-------|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RD4   | R    | 0h    | 8-bit Receive Buffer 4<br>Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received.  |
| 23:16 | RD5   | R    | 0h    | 8-bit Receive Buffer 5.<br>Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received. |
| 15:8  | RD6   | R    | 0h    | 8-bit Receive Buffer 6.<br>Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received. |
| 7:0   | RD7   | R    | 0h    | 8-bit Receive Buffer 7.<br>Each response data-byte that is received in the SCIRXSHFT register is transferred to the corresponding RDy register according to the number of bytes received. |

### 5.11.2.28 LIN\_LINMASK Register

#### 1 LIN\_LINMASK Register (Offset = 6Ch) [reset = 0h]

The LINMASK register is used to configure the masks used for filtering incoming ID messages for receive and transmit frames.

Return to [Summary Table](#)

**Table 5-2005. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 006Ch       |
| LIN1          | 5240 106Ch       |
| LIN2          | 5240 206Ch       |
| LIN3          | 5240 306Ch       |
| LIN4          | 5240 406Ch       |

**Figure 5-664. LIN\_LINMASK Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_2 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RXIDMASK   |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_1 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TXIDMASK   |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2007. LIN\_LINMASK Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED_2 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 23:16 | RXIDMASK   | R/W  | 0h    | Receive ID mask.<br>This field is effective in LIN mode only. This 8-bit mask is used for filtering an incoming ID message and compare it to the ID-byte. A compare match of the received ID with the RX ID mask will set the ID RX flag and trigger an ID interrupt if enabled. A 0 bit in the mask indicates that that bit is compared to the ID-byte. A 1 bit in the mask indicates that that bit is filtered and therefore not used in the compare.<br>When HGENCTRL is set to 1, this field must be set to 0xFF. |
| 15:8  | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

**Table 5-2007. LIN\_LINMASK Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-----|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | TXIDMASK | R/W  | 0h    | <p>Transmit ID mask.</p> <p>This field is effective in LIN mode only. This 8-bit mask is used for filtering an incoming ID message and compare it to the ID-byte. A compare match of the received ID with the TX ID Mask will set the ID TX flag and trigger an ID interrupt if enabled. A 0 bit in the mask indicates that bit is compared to the ID-byte. A 1 bit in the mask indicates that bit is filtered and therefore not used for the compare. When HGENCTRL is set to 1, this field must be set to 0xFF.</p> |

### 5.11.2.29 LIN\_LINID Register

#### 1 LIN\_LINID Register (Offset = 70h) [reset = 0h]

The LINID register contains the identification fields for LIN communication.

NOTE: For software compatibility with future LIN modules, the HGEN CTRL bit must be set to 1, the RX ID MASK field must be set to FFh, and the TX ID MASK field must be set to FFh.

Return to [Summary Table](#)

**Table 5-2008. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 0070h       |
| LIN1          | 5240 1070h       |
| LIN2          | 5240 2070h       |
| LIN3          | 5240 3070h       |
| LIN4          | 5240 4070h       |

**Figure 5-665. LIN\_LINID Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_1      |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RECEIVEDID      |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| IDSLAVETASKBYTE |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| IDBYTE          |    |    |    |    |    |    |    |
| R/W             |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 5-2010. LIN\_LINID Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED_1      | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                |
| 23:16 | RECEIVEDID      | R    | 0h    | Received ID.<br>This bit is effective in LIN mode only. This byte contains the current message identifier. During header reception the received ID is copied from the SCIRXSHF register to this byte if there is no ID-parity error and there has been an RX/TX match.<br>Note: If a framing error [FE] is detected during ID reception, the received ID will also not be copied to the LINID register. |
| 15:8  | IDSLAVETASKBYTE | R/W  | 0h    | ID Slave Task byte.<br>This field is effective in LIN mode only. This byte contains the identifier to which the received ID of an incoming header will be compared in order to decide whether a RX response, a TX response, or no action needs to be done by the LIN node.<br>These bits are writable in LIN mode only.                                                                                 |

**Table 5-2010. LIN\_LINID Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                  |
|-----|--------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | IDBYTE | R/W  | 0h    | ID byte.<br>This field is effective in LIN mode only. This byte is the LIN mode message ID. On a master node, a write to this register by the CPU initiates a header transmission. For a slave task, this byte is used for message filtering when HGENCTRL [SCIGCR1.12] is '0'.<br>These bits are writable in LIN mode only. |



### 5.11.2.30 LIN\_LINTD0 Register

#### 1 LIN\_LINTD0 Register (Offset = 74h) [reset = 0h]

The LINTD0 register contains the lower 4 bytes of the data to be transmitted.

NOTE: TD<x-1> is equivalent to Data byte <x> of the LIN frame.

Return to [Summary Table](#)

**Table 5-2011. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 0074h       |
| LIN1          | 5240 1074h       |
| LIN2          | 5240 2074h       |
| LIN3          | 5240 3074h       |
| LIN4          | 5240 4074h       |

**Figure 5-666. LIN\_LINTD0 Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TD0 |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TD1 |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TD2 |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TD3 |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 5-2013. LIN\_LINTD0 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                            |
|-------|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | TD0   | R/W  | 0h    | 8-bit Transmit Buffer 0.<br>Byte 0 to be transmitted is written into this register and then copied to SCITXSHF for transmission. Once byte 0 is written in TDO buffer, transmission will be initiated. |
| 23:16 | TD1   | R/W  | 0h    | 8-bit Transmit Buffer 3.<br>Byte 1 to be transmitted is written into this register and then copied to SCITXSHF for transmission.                                                                       |
| 15:8  | TD2   | R/W  | 0h    | 8-bit Transmit Buffer 2.<br>Byte 2 to be transmitted is written into this register and then copied to SCITXSHF for transmission.                                                                       |
| 7:0   | TD3   | R/W  | 0h    | 8-bit Transmit Buffer 3.<br>Byte 3 to be transmitted is written into this register and then copied to SCITXSHF for transmission.                                                                       |

### 5.11.2.31 LIN\_LINTD1 Register

#### 1 LIN\_LINTD1 Register (Offset = 78h) [reset = 0h]

The LINTD1 register contains the upper 4 bytes of the data to be transmitted.

NOTE: TD<x-1> is equivalent to Data byte <x> of the LIN frame.

Return to [Summary Table](#)

**Table 5-2014. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 0078h       |
| LIN1          | 5240 1078h       |
| LIN2          | 5240 2078h       |
| LIN3          | 5240 3078h       |
| LIN4          | 5240 4078h       |

**Figure 5-667. LIN\_LINTD1 Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TD4 |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TD5 |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TD6 |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TD7 |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 5-2016. LIN\_LINTD1 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                      |
|-------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | TD4   | R/W  | 0h    | 8-bit Transmit Buffer 4.<br>Byte4 to be transmitted is written into this register and then copied to SCITXSHF for transmission.  |
| 23:16 | TD5   | R/W  | 0h    | 8-bit Transmit Buffer 5.<br>Byte 5 to be transmitted is written into this register and then copied to SCITXSHF for transmission. |
| 15:8  | TD6   | R/W  | 0h    | 8-bit Transmit Buffer 6.<br>Byte 6 to be transmitted is written into this register and then copied to SCITXSHF for transmission. |
| 7:0   | TD7   | R/W  | 0h    | 8-bit Transmit Buffer 7.<br>Byte 7 to be transmitted is written into this register and then copied to SCITXSHF for transmission. |

### 5.11.2.32 LIN\_MBRSR Register

#### 1 LIN\_MBRSR Register (Offset = 7Ch) [reset = DACH]

The MBRSR register is used to configure the expected maximum baud rate of the LIN network.

Return to [Summary Table](#)

**Table 5-2017. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 007Ch       |
| LIN1          | 5240 107Ch       |
| LIN2          | 5240 207Ch       |
| LIN3          | 5240 307Ch       |
| LIN4          | 5240 407Ch       |

**Figure 5-668. LIN\_MBRSR Name Register**

|            |    |    |    |      |    |    |    |
|------------|----|----|----|------|----|----|----|
| 31         | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
| RESERVED_1 |    |    |    |      |    |    |    |
| R          |    |    |    |      |    |    |    |
| 0h         |    |    |    |      |    |    |    |
| 23         | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| RESERVED_1 |    |    |    |      |    |    |    |
| R          |    |    |    |      |    |    |    |
| 0h         |    |    |    |      |    |    |    |
| 15         | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| RESERVED_1 |    |    |    | MBR  |    |    |    |
| R          |    |    |    | R/W  |    |    |    |
| 0h         |    |    |    | DACH |    |    |    |
| 7          | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| MBR        |    |    |    |      |    |    |    |
| R/W        |    |    |    |      |    |    |    |
| DACH       |    |    |    |      |    |    |    |

**Table 5-2019. LIN\_MBRSR Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:13 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 12:0  | MBR        | R/W  | DACH  | <p>Maximum Baud Rate Prescaler.</p> <p>This field is effective in LIN mode only. This 13-bit prescaler is used during the synchronization phase [see the "Header Reception and Adaptive Baudrate" section] of a slave module if the ADAPT bit is set. In this way, a SCI/LIN slave using an automatic or select bit rate modes detects any LIN bus legal rate automatically.</p> <p>The MBR value should be programmed to allow a maximum baud rate that is not more than 10% above the expected operating baud rate in the LIN network. Otherwise a s 0x00 data byte could mistakenly be detected as sync break.</p> <p>The default value is for a 70MHz LINCLK [0xDAC].</p> <p>This MBR prescaler is used by the wake-up and idle time counters for a constant expiration time relative to a 20kHz rate.</p> |

### 5.11.2.33 LIN\_RESERVED\_1\_j Register

1 LIN\_RESERVED\_1\_j Register (Offset = 80h + formula) [reset = 0h]

tbd.

Return to [Summary Table](#)

Offset = (j \* 4h); where j = 0 to 3d

**Table 5-2020. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| LIN0          | 5240 0080h + formula |
| LIN1          | 5240 1080h + formula |
| LIN2          | 5240 2080h + formula |
| LIN3          | 5240 3080h + formula |
| LIN4          | 5240 4080h + formula |

**Figure 5-669. LIN\_RESERVED\_1\_j Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2022. LIN\_RESERVED\_1\_j Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |

### 5.11.2.34 LIN\_IODFTCTRL Register

#### 1 LIN\_IODFTCTRL Register (Offset = 90h) [reset = 500h]

The IODFTCTRL register is used to emulate various error and test conditions.

Return to [Summary Table](#)

**Table 5-2023. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 0090h       |
| LIN1          | 5240 1090h       |
| LIN2          | 5240 2090h       |
| LIN3          | 5240 3090h       |
| LIN4          | 5240 4090h       |

**Figure 5-670. LIN\_IODFTCTRL Name Register**

| 31         | 30       | 29      | 28            | 27         | 26      | 25      | 24          |
|------------|----------|---------|---------------|------------|---------|---------|-------------|
| BERRENA    | PBERRENA | CERRENA | ISFERRENA     | RESERVED_4 | FERRENA | PERRENA | BRKDTERRENA |
| R/W        | R/W      | R/W     | R/W           | R          | R/W     | R/W     | R/W         |
| 0h         | 0h       | 0h      | 0h            | 0h         | 0h      | 0h      | 0h          |
| 23         | 22       | 21      | 20            | 19         | 18      | 17      | 16          |
| RESERVED_3 |          |         | PINSAMPLEMASK |            | TXSHIFT |         |             |
| R/W        |          |         | R/W           |            | R/W     |         |             |
| 0h         |          |         | 0h            |            | 0h      |         |             |
| 15         | 14       | 13      | 12            | 11         | 10      | 9       | 8           |
| RESERVED_2 |          |         |               | IODFTENA   |         |         |             |
| R          |          |         |               | R/W        |         |         |             |
| 0h         |          |         |               | 5h         |         |         |             |
| 7          | 6        | 5       | 4             | 3          | 2       | 1       | 0           |
| RESERVED_1 |          |         |               |            |         | LPBENA  | RXPENA      |
| R          |          |         |               |            |         | R/W     | R/W         |
| 0h         |          |         |               |            |         | 0h      | 0h          |

**Table 5-2025. LIN\_IODFTCTRL Register Field Descriptions**

| Bit | Field     | Type | Reset | Description                                                                                                                                                                                                                                                             |
|-----|-----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31  | BERRENA   | R/W  | 0h    | Bit Error Enable bit.<br>This bit is effective in LIN mode only. This bit is used to create a Bit error. When this bit is set, the bit received is ORed with 1 and passed to the Bit monitor circuitry.                                                                 |
| 30  | PBERRENA  | R/W  | 0h    | Physical Bus Error Enable bit.<br>This bit is effective in LIN mode only. This bit is used to create a Physical Bus Error. When this bit is set, the bit received during Sync Break field transmission is ORed with 1 and passed to the Bit monitor circuitry.          |
| 29  | CERRENA   | R/W  | 0h    | Checksum Error Enable bit.<br>This bit is effective in LIN mode only. This bit is used to create a checksum error. When this bit is set, the polarity of the CTYPE [checksum type] in the receive checksum calculator is changed so that a checksum error is generated. |
| 28  | ISFERRENA | R/W  | 0h    | Inconsistent Sync Field Error Enable bit.<br>This bit is effective in LIN mode only. This bit is used to create an ISF error. When this bit is set, the bit widths in the sync field are varied so that the ISF check fails and the error flag is set.                  |

**Table 5-2025. LIN\_IODFTCTRL Register Field Descriptions (continued)**

| Bit   | Field         | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|---------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 27    | RESERVED_4    | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 26    | FERRENA       | R/W  | 0h    | This bit is used to create a Frame Error.<br>This bit is effective in SCI-compatible mode only. When this bit is set, the stop bit received is ANDed with '0' and passed to the stop bit check circuitry.                                                                                                                                                                                                                                                                                                 |
| 25    | PERRENA       | R/W  | 0h    | Compatible Mode only<br>This bit is effective in SCI-compatible mode only. This bit is used to create a Parity Error. When this bit is set, in compatible mode, the parity bit received is toggled so that a parity error occurs.                                                                                                                                                                                                                                                                         |
| 24    | BRKDTERRRENA  | R/W  | 0h    | Compatible Mode only<br>This bit is effective in SCI-compatible mode only. This bit is used to create BRKDT error [SCI mode only]. When this bit is set, the stop bit of the frame is ANDed with '0' and passed to the RSM so that a frame error occurs. Then the RX Pin is forced to continuous low for 10 Tbits so that a BRKDT error occurs.                                                                                                                                                           |
| 23:21 | RESERVED_3    | R/W  | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 20:19 | PINSAMPLEMASK | R/W  | 0h    | Pin sample mask.<br>These bits define the sample number at which the TX Pin value that is being transmitted will be inverted to verify the receive pin samples correctly with the majority detection circuitry.<br>Note: During IODFT mode testing for the pin sample mask, the prescaler P must be programmed to be greater than 2.<br><br>0 No Mask<br>1 Invert the TX Pin value at TBIT_CENTER<br>2 Invert the TX Pin value at TBIT_CENTER + SCLK<br>3 Invert the TX Pin value at TBIT_CENTER + 2 SCLK |
| 18:16 | TXSHIFT       | R/W  | 0h    | Transmit shift.<br>These bits define the delay by which the value on LINTX is delayed so that the value on LINRX is asynchronous. [Not applicable to Start Bit]<br><br>0 No Delay<br>1 Delay by 1 SCLK<br>2 Delay by 2 SCLK<br>3 Delay by 3 SCLK<br>4 Delay by 4 SCLK<br>5 Delay by 5 SCLK<br>6 Delay by 6 SCLK<br>7 Delay by 7 SCLK                                                                                                                                                                      |
| 15:12 | RESERVED_2    | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 11:8  | IODFTENA      | R/W  | 5h    | IO DFT Enable Key<br>This field is used to enable the IODFT mode of the SCI/LIN module for testing.<br><br>0 IODFT is disabled<br>1 IODFT is disabled<br>2 IODFT is disabled<br>3 IODFT is disabled<br>4 IODFT is disabled<br>5 IODFT is disabled<br>6 IODFT is disabled<br>7 IODFT is disabled<br>8 IODFT is disabled<br>9 IODFT is disabled<br>10 IODFT is enabled<br>11 IODFT is disabled<br>12 IODFT is disabled<br>13 IODFT is disabled<br>14 IODFT is disabled<br>15 IODFT is disabled              |
| 7:2   | RESERVED_1    | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

**Table 5-2025. LIN\_IODFTCTRL Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                           |
|-----|--------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | LPBENA | R/W  | 0h    | <p>Module loopback enable.</p> <p>In analog loopback mode the complete communication path through the I/Os can be tested, whereas in digital loopback mode the I/O buffers are excluded from this path.</p> <p>0      Digital loopback is enabled.<br/> 1      Analog loopback is enabled in module I/O DFT mode (when IODFTENA = 1010)</p>           |
| 0   | RXPENA | R/W  | 0h    | <p>Module Analog loopback through receive pin enable.</p> <p>This bit defines whether the I/O buffers for the transmit or the receive pin are included in the communication path in analog loopback mode only.</p> <p>0      Analog loopback through the transmit pin is enabled.<br/> 1      Analog loopback through the receive pin is enabled.</p> |

### 5.11.2.35 LIN\_RESERVED\_2\_j Register

1 LIN\_RESERVED\_2\_j Register (Offset = 94h + formula) [reset = 0h]

tbd.

Return to [Summary Table](#)

Offset = (j \* 4h); where j = 0 to 18d

**Table 5-2026. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| LIN0          | 5240 0094h + formula |
| LIN1          | 5240 1094h + formula |
| LIN2          | 5240 2094h + formula |
| LIN3          | 5240 3094h + formula |
| LIN4          | 5240 4094h + formula |

**Figure 5-671. LIN\_RESERVED\_2\_j Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2028. LIN\_RESERVED\_2\_j Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | NONE | 0h    | Reserved    |



### 5.11.2.36 LIN\_LIN\_GLB\_INT\_EN Register

#### 1 LIN\_LIN\_GLB\_INT\_EN Register (Offset = E0h) [reset = 0h]

The LIN\_GLB\_INT\_EN register is used to enable the INT0 and INT1 interrupt lines to propagate to the PIE block.

Return to [Summary Table](#)

**Table 5-2029. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 00E0h       |
| LIN1          | 5240 10E0h       |
| LIN2          | 5240 20E0h       |
| LIN3          | 5240 30E0h       |
| LIN4          | 5240 40E0h       |

**Figure 5-672. LIN\_LIN\_GLB\_INT\_EN Name Register**

|            |    |    |    |    |    |            |            |
|------------|----|----|----|----|----|------------|------------|
| 31         | 30 | 29 | 28 | 27 | 26 | 25         | 24         |
| RESERVED_1 |    |    |    |    |    |            |            |
| R          |    |    |    |    |    |            |            |
| 0h         |    |    |    |    |    |            |            |
| 23         | 22 | 21 | 20 | 19 | 18 | 17         | 16         |
| RESERVED_1 |    |    |    |    |    |            |            |
| R          |    |    |    |    |    |            |            |
| 0h         |    |    |    |    |    |            |            |
| 15         | 14 | 13 | 12 | 11 | 10 | 9          | 8          |
| RESERVED_1 |    |    |    |    |    |            |            |
| R          |    |    |    |    |    |            |            |
| 0h         |    |    |    |    |    |            |            |
| 7          | 6  | 5  | 4  | 3  | 2  | 1          | 0          |
| RESERVED_1 |    |    |    |    |    | GLBINT1_EN | GLBINT0_EN |
| R          |    |    |    |    |    | R/W        | R/W        |
| 0h         |    |    |    |    |    | 0h         | 0h         |

**Table 5-2031. LIN\_LIN\_GLB\_INT\_EN Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                             |
|------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                |
| 1    | GLBINT1_EN | R/W  | 0h    | Global Interrupt Enable for LIN INT1.<br>This bit determines whether the INT1 interrupt line generates an interrupt to the PIE or not<br><br>0 LIN INT1 line does not generate an interrupt to the PIE.<br>1 LIN INT1 line generates an interrupt to the PIE if an enabled interrupt condition occurs.  |
| 0    | GLBINT0_EN | R/W  | 0h    | Global Interrupt Enable for LIN INT0.<br>This bit determines whether the INT0 interrupt line generates an interrupt to the PIE or not.<br><br>0 LIN INT0 line does not generate an interrupt to the PIE.<br>1 LIN INT0 line generates an interrupt to the PIE if an enabled interrupt condition occurs. |

### 5.11.2.37 LIN\_LIN\_GLB\_INT\_FLG Register

#### 1 LIN\_LIN\_GLB\_INT\_FLG Register (Offset = E4h) [reset = 0h]

The LIN\_GLB\_INT\_FLG register contains the current status of the INT0 and INT1 flags.

Return to [Summary Table](#)

**Table 5-2032. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 00E4h       |
| LIN1          | 5240 10E4h       |
| LIN2          | 5240 20E4h       |
| LIN3          | 5240 30E4h       |
| LIN4          | 5240 40E4h       |

**Figure 5-673. LIN\_LIN\_GLB\_INT\_FLG Name Register**

|            |    |    |    |    |    |          |          |
|------------|----|----|----|----|----|----------|----------|
| 31         | 30 | 29 | 28 | 27 | 26 | 25       | 24       |
| RESERVED_1 |    |    |    |    |    |          |          |
| R          |    |    |    |    |    |          |          |
| 0h         |    |    |    |    |    |          |          |
| 23         | 22 | 21 | 20 | 19 | 18 | 17       | 16       |
| RESERVED_1 |    |    |    |    |    |          |          |
| R          |    |    |    |    |    |          |          |
| 0h         |    |    |    |    |    |          |          |
| 15         | 14 | 13 | 12 | 11 | 10 | 9        | 8        |
| RESERVED_1 |    |    |    |    |    |          |          |
| R          |    |    |    |    |    |          |          |
| 0h         |    |    |    |    |    |          |          |
| 7          | 6  | 5  | 4  | 3  | 2  | 1        | 0        |
| RESERVED_1 |    |    |    |    |    | INT1_FLG | INT0_FLG |
| R          |    |    |    |    |    | R        | R        |
| 0h         |    |    |    |    |    | 0h       | 0h       |

**Table 5-2034. LIN\_LIN\_GLB\_INT\_FLG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED_1 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 1    | INT1_FLG   | R    | 0h    | Global Interrupt Flag for LIN INT1.<br>This bit indicates if an interrupt was generated to the PIE due to an enabled interrupt on the INT1 interrupt line. Refer to the LIN Interrupt Status Register for the condition that generated the interrupt.<br>This bit can be cleared by Writing a 1 to the corresponding bit in the LIN_GLB_INT_CLR register.<br><br>0 No interrupt is active on the INT1 line.<br>1 An interrupt was generated due to an enabled interrupt on the INT1 interrupt line. |

**Table 5-2034. LIN\_LIN\_GLB\_INT\_FLG Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | INT0_FLG | R    | 0h    | <p>Global Interrupt Flag for LIN INT0.</p> <p>This bit indicates if an interrupt was generated to the PIE due to an enabled interrupt on the INT0 interrupt line. Refer to the LIN Interrupt Status Register for the condition that generated the interrupt.</p> <p>This bit can be cleared by Writing a 1 to the corresponding bit in the LIN_GLB_INT_CLR register.</p> <p>0 No interrupt is active on the INT0 line.<br/>1 An interrupt was generated due to an enabled interrupt on the INT0 interrupt line.</p> |

### 5.11.2.38 LIN\_LIN\_GLB\_INT\_CLR Register

#### 1 LIN\_LIN\_GLB\_INT\_CLR Register (Offset = E8h) [reset = 0h]

The LIN\_GLB\_INT\_CLR register is used to clear the interrupt flags in LIN\_GLB\_INT\_FLG register.

Return to [Summary Table](#)

**Table 5-2035. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| LIN0          | 5240 00E8h       |
| LIN1          | 5240 10E8h       |
| LIN2          | 5240 20E8h       |
| LIN3          | 5240 30E8h       |
| LIN4          | 5240 40E8h       |

**Figure 5-674. LIN\_LIN\_GLB\_INT\_CLR Name Register**

|            |    |    |    |    |    |              |              |
|------------|----|----|----|----|----|--------------|--------------|
| 31         | 30 | 29 | 28 | 27 | 26 | 25           | 24           |
| RESERVED_1 |    |    |    |    |    |              |              |
| R          |    |    |    |    |    |              |              |
| 0h         |    |    |    |    |    |              |              |
| 23         | 22 | 21 | 20 | 19 | 18 | 17           | 16           |
| RESERVED_1 |    |    |    |    |    |              |              |
| R          |    |    |    |    |    |              |              |
| 0h         |    |    |    |    |    |              |              |
| 15         | 14 | 13 | 12 | 11 | 10 | 9            | 8            |
| RESERVED_1 |    |    |    |    |    |              |              |
| R          |    |    |    |    |    |              |              |
| 0h         |    |    |    |    |    |              |              |
| 7          | 6  | 5  | 4  | 3  | 2  | 1            | 0            |
| RESERVED_1 |    |    |    |    |    | INT1_FLG_CLR | INT0_FLG_CLR |
| R          |    |    |    |    |    | R/W1TC       | R/W1TC       |
| 0h         |    |    |    |    |    | 0h           | 0h           |

**Table 5-2037. LIN\_LIN\_GLB\_INT\_CLR Register Field Descriptions**

| Bit  | Field        | Type   | Reset | Description                                                                                                                                                                               |
|------|--------------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED_1   | R      | 0h    | Reserved                                                                                                                                                                                  |
| 1    | INT1_FLG_CLR | R/W1TC | 0h    | Global Interrupt flag clear for LIN INT1.<br>This bit is used to clear the corresponding bit in the LIN_GLB_INT_FLG register. Write 1 to clear the INT1_FLG bit. Writing 0 has no effect. |
| 0    | INT0_FLG_CLR | R/W1TC | 0h    | Global Interrupt flag clear for LIN INT0.<br>This bit is used to clear the corresponding bit in the LIN_GLB_INT_FLG register. Write 1 to clear the INT0_FLG bit. Writing 0 has no effect. |

## 5.12 MCAN

### MCAN

#### 5.12.1 MCAN Summaries

#### MCAN Summaries

**Table 5-2038. MSG\_RAM Registers, Base Address=5260 0000h, Length=32768**

| Offset | Length | Register Name                 | MCAN0 Physical Address | MCAN1 Physical Address | MCAN2 Physical Address |
|--------|--------|-------------------------------|------------------------|------------------------|------------------------|
| 0h     | 32     | <a href="#">MSG_RAM_START</a> | 5260 0000h             | 5261 0000h             | 5262 0000h             |
| 10FFCh | 32     | <a href="#">MSG_RAM_END</a>   | 5261 0FFCh             | 5262 0FFCh             | 5263 0FFCh             |

**Table 5-2039. MSG\_RAM Registers, Base Address=5260 0000h, Length=32768**

| Offset | Length | Register Name                 | MCAN3 Physical Address |
|--------|--------|-------------------------------|------------------------|
| 0h     | 32     | <a href="#">MSG_RAM_START</a> | 5263 0000h             |
| 10FFCh | 32     | <a href="#">MSG_RAM_END</a>   | 5264 0FFCh             |

**Table 5-2040. CFG Registers, Base Address=5260 8000h, Length=1024**

| Offset | Length | Register Name                      | MCAN0 Physical Address | MCAN1 Physical Address | MCAN2 Physical Address |
|--------|--------|------------------------------------|------------------------|------------------------|------------------------|
| 0h     | 32     | <a href="#">CFG_SS_PID</a>         | 5260 8000h             | 5261 8000h             | 5262 8000h             |
| 4h     | 32     | <a href="#">CFG_SS_CTRL</a>        | 5260 8004h             | 5261 8004h             | 5262 8004h             |
| 8h     | 32     | <a href="#">CFG_SS_STAT</a>        | 5260 8008h             | 5261 8008h             | 5262 8008h             |
| Ch     | 32     | <a href="#">CFG_SS_ICS</a>         | 5260 800Ch             | 5261 800Ch             | 5262 800Ch             |
| 10h    | 32     | <a href="#">CFG_SS_IRS</a>         | 5260 8010h             | 5261 8010h             | 5262 8010h             |
| 14h    | 32     | <a href="#">CFG_SS_IECS</a>        | 5260 8014h             | 5261 8014h             | 5262 8014h             |
| 18h    | 32     | <a href="#">CFG_SS_IE</a>          | 5260 8018h             | 5261 8018h             | 5262 8018h             |
| 1Ch    | 32     | <a href="#">CFG_SS_IES</a>         | 5260 801Ch             | 5261 801Ch             | 5262 801Ch             |
| 20h    | 32     | <a href="#">CFG_SS_EOI</a>         | 5260 8020h             | 5261 8020h             | 5262 8020h             |
| 24h    | 32     | <a href="#">CFG_SS_EXT_TS_PS</a>   | 5260 8024h             | 5261 8024h             | 5262 8024h             |
| 28h    | 32     | <a href="#">CFG_SS_EXT_TS_USIC</a> | 5260 8028h             | 5261 8028h             | 5262 8028h             |
| 200h   | 32     | <a href="#">CFG_CREL</a>           | 5260 8200h             | 5261 8200h             | 5262 8200h             |
| 204h   | 32     | <a href="#">CFG_ENDN</a>           | 5260 8204h             | 5261 8204h             | 5262 8204h             |
| 208h   | 32     | <a href="#">CFG_CUST</a>           | 5260 8208h             | 5261 8208h             | 5262 8208h             |
| 20Ch   | 32     | <a href="#">CFG_DBTP</a>           | 5260 820Ch             | 5261 820Ch             | 5262 820Ch             |
| 210h   | 32     | <a href="#">CFG_TEST</a>           | 5260 8210h             | 5261 8210h             | 5262 8210h             |
| 214h   | 32     | <a href="#">CFG_RWD</a>            | 5260 8214h             | 5261 8214h             | 5262 8214h             |
| 218h   | 32     | <a href="#">CFG_CCCR</a>           | 5260 8218h             | 5261 8218h             | 5262 8218h             |
| 21Ch   | 32     | <a href="#">CFG_NBTP</a>           | 5260 821Ch             | 5261 821Ch             | 5262 821Ch             |
| 220h   | 32     | <a href="#">CFG_TSCC</a>           | 5260 8220h             | 5261 8220h             | 5262 8220h             |
| 224h   | 32     | <a href="#">CFG_TSCV</a>           | 5260 8224h             | 5261 8224h             | 5262 8224h             |
| 228h   | 32     | <a href="#">CFG_TOCC</a>           | 5260 8228h             | 5261 8228h             | 5262 8228h             |
| 22Ch   | 32     | <a href="#">CFG_TOCV</a>           | 5260 822Ch             | 5261 822Ch             | 5262 822Ch             |
| 240h   | 32     | <a href="#">CFG_ECR</a>            | 5260 8240h             | 5261 8240h             | 5262 8240h             |
| 244h   | 32     | <a href="#">CFG_PSR</a>            | 5260 8244h             | 5261 8244h             | 5262 8244h             |

**Table 5-2040. CFG Registers, Base Address=5260 8000h, Length=1024 (continued)**

| Offset | Length | Register Name              | MCAN0 Physical Address | MCAN1 Physical Address | MCAN2 Physical Address |
|--------|--------|----------------------------|------------------------|------------------------|------------------------|
| 248h   | 32     | <a href="#">CFG_TDCR</a>   | 5260 8248h             | 5261 8248h             | 5262 8248h             |
| 250h   | 32     | <a href="#">CFG_IR</a>     | 5260 8250h             | 5261 8250h             | 5262 8250h             |
| 254h   | 32     | <a href="#">CFG_IE</a>     | 5260 8254h             | 5261 8254h             | 5262 8254h             |
| 258h   | 32     | <a href="#">CFG_ILS</a>    | 5260 8258h             | 5261 8258h             | 5262 8258h             |
| 25Ch   | 32     | <a href="#">CFG_ILE</a>    | 5260 825Ch             | 5261 825Ch             | 5262 825Ch             |
| 280h   | 32     | <a href="#">CFG_GFC</a>    | 5260 8280h             | 5261 8280h             | 5262 8280h             |
| 284h   | 32     | <a href="#">CFG_SIDFC</a>  | 5260 8284h             | 5261 8284h             | 5262 8284h             |
| 288h   | 32     | <a href="#">CFG_XIDFC</a>  | 5260 8288h             | 5261 8288h             | 5262 8288h             |
| 290h   | 32     | <a href="#">CFG_XIDAM</a>  | 5260 8290h             | 5261 8290h             | 5262 8290h             |
| 294h   | 32     | <a href="#">CFG_HPMS</a>   | 5260 8294h             | 5261 8294h             | 5262 8294h             |
| 298h   | 32     | <a href="#">CFG_NDAT1</a>  | 5260 8298h             | 5261 8298h             | 5262 8298h             |
| 29Ch   | 32     | <a href="#">CFG_NDAT2</a>  | 5260 829Ch             | 5261 829Ch             | 5262 829Ch             |
| 2A0h   | 32     | <a href="#">CFG_RXF0C</a>  | 5260 82A0h             | 5261 82A0h             | 5262 82A0h             |
| 2A4h   | 32     | <a href="#">CFG_RXF0S</a>  | 5260 82A4h             | 5261 82A4h             | 5262 82A4h             |
| 2A8h   | 32     | <a href="#">CFG_RXF0A</a>  | 5260 82A8h             | 5261 82A8h             | 5262 82A8h             |
| 2ACh   | 32     | <a href="#">CFG_RXBC</a>   | 5260 82ACh             | 5261 82ACh             | 5262 82ACh             |
| 2B0h   | 32     | <a href="#">CFG_RXF1C</a>  | 5260 82B0h             | 5261 82B0h             | 5262 82B0h             |
| 2B4h   | 32     | <a href="#">CFG_RXF1S</a>  | 5260 82B4h             | 5261 82B4h             | 5262 82B4h             |
| 2B8h   | 32     | <a href="#">CFG_RXF1A</a>  | 5260 82B8h             | 5261 82B8h             | 5262 82B8h             |
| 2BCh   | 32     | <a href="#">CFG_RXESC</a>  | 5260 82BCh             | 5261 82BCh             | 5262 82BCh             |
| 2C0h   | 32     | <a href="#">CFG_TXBC</a>   | 5260 82C0h             | 5261 82C0h             | 5262 82C0h             |
| 2C4h   | 32     | <a href="#">CFG_TXFQS</a>  | 5260 82C4h             | 5261 82C4h             | 5262 82C4h             |
| 2C8h   | 32     | <a href="#">CFG_TXESC</a>  | 5260 82C8h             | 5261 82C8h             | 5262 82C8h             |
| 2CCh   | 32     | <a href="#">CFG_TXBRP</a>  | 5260 82CCh             | 5261 82CCh             | 5262 82CCh             |
| 2D0h   | 32     | <a href="#">CFG_TXBAR</a>  | 5260 82D0h             | 5261 82D0h             | 5262 82D0h             |
| 2D4h   | 32     | <a href="#">CFG_TXBCR</a>  | 5260 82D4h             | 5261 82D4h             | 5262 82D4h             |
| 2D8h   | 32     | <a href="#">CFG_TXBTO</a>  | 5260 82D8h             | 5261 82D8h             | 5262 82D8h             |
| 2DCh   | 32     | <a href="#">CFG_TXBCF</a>  | 5260 82DCh             | 5261 82DCh             | 5262 82DCh             |
| 2E0h   | 32     | <a href="#">CFG_TXBTIE</a> | 5260 82E0h             | 5261 82E0h             | 5262 82E0h             |
| 2E4h   | 32     | <a href="#">CFG_TXBCIE</a> | 5260 82E4h             | 5261 82E4h             | 5262 82E4h             |
| 2F0h   | 32     | <a href="#">CFG_TXEFC</a>  | 5260 82F0h             | 5261 82F0h             | 5262 82F0h             |
| 2F4h   | 32     | <a href="#">CFG_TXEFS</a>  | 5260 82F4h             | 5261 82F4h             | 5262 82F4h             |
| 2F8h   | 32     | <a href="#">CFG_TXEFA</a>  | 5260 82F8h             | 5261 82F8h             | 5262 82F8h             |

**Table 5-2041. CFG Registers, Base Address=5260 8000h, Length=1024**

| Offset | Length | Register Name               | MCAN3 Physical Address |
|--------|--------|-----------------------------|------------------------|
| 0h     | 32     | <a href="#">CFG_SS_PID</a>  | 5263 8000h             |
| 4h     | 32     | <a href="#">CFG_SS_CTRL</a> | 5263 8004h             |
| 8h     | 32     | <a href="#">CFG_SS_STAT</a> | 5263 8008h             |
| Ch     | 32     | <a href="#">CFG_SS_ICS</a>  | 5263 800Ch             |
| 10h    | 32     | <a href="#">CFG_SS_IRS</a>  | 5263 8010h             |
| 14h    | 32     | <a href="#">CFG_SS_IECS</a> | 5263 8014h             |
| 18h    | 32     | <a href="#">CFG_SS_IE</a>   | 5263 8018h             |
| 1Ch    | 32     | <a href="#">CFG_SS_IES</a>  | 5263 801Ch             |

**Table 5-2041. CFG Registers, Base Address=5260 8000h, Length=1024 (continued)**

| Offset | Length | Register Name                      | MCAN3 Physical Address |
|--------|--------|------------------------------------|------------------------|
| 20h    | 32     | <a href="#">CFG_SS_EOI</a>         | 5263 8020h             |
| 24h    | 32     | <a href="#">CFG_SS_EXT_TS_PS</a>   | 5263 8024h             |
| 28h    | 32     | <a href="#">CFG_SS_EXT_TS_USIC</a> | 5263 8028h             |
| 200h   | 32     | <a href="#">CFG_CREL</a>           | 5263 8200h             |
| 204h   | 32     | <a href="#">CFG_ENDN</a>           | 5263 8204h             |
| 208h   | 32     | <a href="#">CFG_CUST</a>           | 5263 8208h             |
| 20Ch   | 32     | <a href="#">CFG_DBTP</a>           | 5263 820Ch             |
| 210h   | 32     | <a href="#">CFG_TEST</a>           | 5263 8210h             |
| 214h   | 32     | <a href="#">CFG_RWD</a>            | 5263 8214h             |
| 218h   | 32     | <a href="#">CFG_CCCR</a>           | 5263 8218h             |
| 21Ch   | 32     | <a href="#">CFG_NBTP</a>           | 5263 821Ch             |
| 220h   | 32     | <a href="#">CFG_TSCC</a>           | 5263 8220h             |
| 224h   | 32     | <a href="#">CFG_TSCV</a>           | 5263 8224h             |
| 228h   | 32     | <a href="#">CFG_TOCC</a>           | 5263 8228h             |
| 22Ch   | 32     | <a href="#">CFG_TOCV</a>           | 5263 822Ch             |
| 240h   | 32     | <a href="#">CFG_ECR</a>            | 5263 8240h             |
| 244h   | 32     | <a href="#">CFG_PSR</a>            | 5263 8244h             |
| 248h   | 32     | <a href="#">CFG_TDCR</a>           | 5263 8248h             |
| 250h   | 32     | <a href="#">CFG_IR</a>             | 5263 8250h             |
| 254h   | 32     | <a href="#">CFG_IE</a>             | 5263 8254h             |
| 258h   | 32     | <a href="#">CFG_ILS</a>            | 5263 8258h             |
| 25Ch   | 32     | <a href="#">CFG_ILE</a>            | 5263 825Ch             |
| 280h   | 32     | <a href="#">CFG_GFC</a>            | 5263 8280h             |
| 284h   | 32     | <a href="#">CFG_SIDFC</a>          | 5263 8284h             |
| 288h   | 32     | <a href="#">CFG_XIDFC</a>          | 5263 8288h             |
| 290h   | 32     | <a href="#">CFG_XIDAM</a>          | 5263 8290h             |
| 294h   | 32     | <a href="#">CFG_HPMS</a>           | 5263 8294h             |
| 298h   | 32     | <a href="#">CFG_NDAT1</a>          | 5263 8298h             |
| 29Ch   | 32     | <a href="#">CFG_NDAT2</a>          | 5263 829Ch             |
| 2A0h   | 32     | <a href="#">CFG_RXF0C</a>          | 5263 82A0h             |
| 2A4h   | 32     | <a href="#">CFG_RXF0S</a>          | 5263 82A4h             |
| 2A8h   | 32     | <a href="#">CFG_RXF0A</a>          | 5263 82A8h             |
| 2ACh   | 32     | <a href="#">CFG_RXBC</a>           | 5263 82ACh             |
| 2B0h   | 32     | <a href="#">CFG_RXF1C</a>          | 5263 82B0h             |
| 2B4h   | 32     | <a href="#">CFG_RXF1S</a>          | 5263 82B4h             |
| 2B8h   | 32     | <a href="#">CFG_RXF1A</a>          | 5263 82B8h             |
| 2BCh   | 32     | <a href="#">CFG_RXESC</a>          | 5263 82BCh             |
| 2C0h   | 32     | <a href="#">CFG_TXBC</a>           | 5263 82C0h             |
| 2C4h   | 32     | <a href="#">CFG_TXFQS</a>          | 5263 82C4h             |
| 2C8h   | 32     | <a href="#">CFG_TXESC</a>          | 5263 82C8h             |
| 2CCh   | 32     | <a href="#">CFG_TXBRP</a>          | 5263 82CCh             |
| 2D0h   | 32     | <a href="#">CFG_TXBAR</a>          | 5263 82D0h             |
| 2D4h   | 32     | <a href="#">CFG_TXBCR</a>          | 5263 82D4h             |
| 2D8h   | 32     | <a href="#">CFG_TXBTO</a>          | 5263 82D8h             |
| 2DCh   | 32     | <a href="#">CFG_TXBCF</a>          | 5263 82DCh             |

**Table 5-2041. CFG Registers, Base Address=5260 8000h, Length=1024 (continued)**

| Offset | Length | Register Name              | MCAN3 Physical Address |
|--------|--------|----------------------------|------------------------|
| 2E0h   | 32     | <a href="#">CFG_TXBTIE</a> | 5263 82E0h             |
| 2E4h   | 32     | <a href="#">CFG_TXBCIE</a> | 5263 82E4h             |
| 2F0h   | 32     | <a href="#">CFG_TXEFC</a>  | 5263 82F0h             |
| 2F4h   | 32     | <a href="#">CFG_TXEFS</a>  | 5263 82F4h             |
| 2F8h   | 32     | <a href="#">CFG_TXEFA</a>  | 5263 82F8h             |

**Table 5-2042. ECC Registers, Base Address=5270 0000h, Length=1024**

| Offset | Length | Register Name                           | MCAN0 Physical Address | MCAN1 Physical Address | MCAN2 Physical Address |
|--------|--------|-----------------------------------------|------------------------|------------------------|------------------------|
| 0h     | 32     | <a href="#">ECC_REV</a>                 | 5270 0000h             | 5270 1000h             | 5270 2000h             |
| 8h     | 32     | <a href="#">ECC_VECTOR</a>              | 5270 0008h             | 5270 1008h             | 5270 2008h             |
| Ch     | 32     | <a href="#">ECC_STAT</a>                | 5270 000Ch             | 5270 100Ch             | 5270 200Ch             |
| 14h    | 32     | <a href="#">ECC_CTRL</a>                | 5270 0014h             | 5270 1014h             | 5270 2014h             |
| 18h    | 32     | <a href="#">ECC_ERR_CTRL1</a>           | 5270 0018h             | 5270 1018h             | 5270 2018h             |
| 1Ch    | 32     | <a href="#">ECC_ERR_CTRL2</a>           | 5270 001Ch             | 5270 101Ch             | 5270 201Ch             |
| 20h    | 32     | <a href="#">ECC_ERR_STAT1</a>           | 5270 0020h             | 5270 1020h             | 5270 2020h             |
| 24h    | 32     | <a href="#">ECC_ERR_STAT2</a>           | 5270 0024h             | 5270 1024h             | 5270 2024h             |
| 28h    | 32     | <a href="#">ECC_ERR_STAT3</a>           | 5270 0028h             | 5270 1028h             | 5270 2028h             |
| 3Ch    | 32     | <a href="#">ECC_SEC_EOI_REG</a>         | 5270 003Ch             | 5270 103Ch             | 5270 203Ch             |
| 40h    | 32     | <a href="#">ECC_SEC_STATUS_REG0</a>     | 5270 0040h             | 5270 1040h             | 5270 2040h             |
| 80h    | 32     | <a href="#">ECC_SEC_ENABLE_SET_REG0</a> | 5270 0080h             | 5270 1080h             | 5270 2080h             |
| C0h    | 32     | <a href="#">ECC_SEC_ENABLE_CLR_REG0</a> | 5270 00C0h             | 5270 10C0h             | 5270 20C0h             |
| 13Ch   | 32     | <a href="#">ECC_DED_EOI_REG</a>         | 5270 013Ch             | 5270 113Ch             | 5270 213Ch             |
| 140h   | 32     | <a href="#">ECC_DED_STATUS_REG0</a>     | 5270 0140h             | 5270 1140h             | 5270 2140h             |
| 180h   | 32     | <a href="#">ECC_DED_ENABLE_SET_REG0</a> | 5270 0180h             | 5270 1180h             | 5270 2180h             |
| 1C0h   | 32     | <a href="#">ECC_DED_ENABLE_CLR_REG0</a> | 5270 01C0h             | 5270 11C0h             | 5270 21C0h             |
| 200h   | 32     | <a href="#">ECC_AGGR_ENABLE_SET</a>     | 5270 0200h             | 5270 1200h             | 5270 2200h             |
| 204h   | 32     | <a href="#">ECC_AGGR_ENABLE_CLR</a>     | 5270 0204h             | 5270 1204h             | 5270 2204h             |
| 208h   | 32     | <a href="#">ECC_AGGR_STATUS_SET</a>     | 5270 0208h             | 5270 1208h             | 5270 2208h             |
| 20Ch   | 32     | <a href="#">ECC_AGGR_STATUS_CLR</a>     | 5270 020Ch             | 5270 120Ch             | 5270 220Ch             |

**Table 5-2043. ECC Registers, Base Address=5270 0000h, Length=1024**

| Offset | Length | Register Name                       | MCAN3 Physical Address |
|--------|--------|-------------------------------------|------------------------|
| 0h     | 32     | <a href="#">ECC_REV</a>             | 5270 3000h             |
| 8h     | 32     | <a href="#">ECC_VECTOR</a>          | 5270 3008h             |
| Ch     | 32     | <a href="#">ECC_STAT</a>            | 5270 300Ch             |
| 14h    | 32     | <a href="#">ECC_CTRL</a>            | 5270 3014h             |
| 18h    | 32     | <a href="#">ECC_ERR_CTRL1</a>       | 5270 3018h             |
| 1Ch    | 32     | <a href="#">ECC_ERR_CTRL2</a>       | 5270 301Ch             |
| 20h    | 32     | <a href="#">ECC_ERR_STAT1</a>       | 5270 3020h             |
| 24h    | 32     | <a href="#">ECC_ERR_STAT2</a>       | 5270 3024h             |
| 28h    | 32     | <a href="#">ECC_ERR_STAT3</a>       | 5270 3028h             |
| 3Ch    | 32     | <a href="#">ECC_SEC_EOI_REG</a>     | 5270 303Ch             |
| 40h    | 32     | <a href="#">ECC_SEC_STATUS_REG0</a> | 5270 3040h             |



**Table 5-2043. ECC Registers, Base Address=5270 0000h, Length=1024 (continued)**

| Offset | Length | Register Name                           | MCAN3 Physical Address |
|--------|--------|-----------------------------------------|------------------------|
| 80h    | 32     | <a href="#">ECC_SEC_ENABLE_SET_REG0</a> | 5270 3080h             |
| C0h    | 32     | <a href="#">ECC_SEC_ENABLE_CLR_REG0</a> | 5270 30C0h             |
| 13Ch   | 32     | <a href="#">ECC_DED_EOI_REG</a>         | 5270 313Ch             |
| 140h   | 32     | <a href="#">ECC_DED_STATUS_REG0</a>     | 5270 3140h             |
| 180h   | 32     | <a href="#">ECC_DED_ENABLE_SET_REG0</a> | 5270 3180h             |
| 1C0h   | 32     | <a href="#">ECC_DED_ENABLE_CLR_REG0</a> | 5270 31C0h             |
| 200h   | 32     | <a href="#">ECC_AGGR_ENABLE_SET</a>     | 5270 3200h             |
| 204h   | 32     | <a href="#">ECC_AGGR_ENABLE_CLR</a>     | 5270 3204h             |
| 208h   | 32     | <a href="#">ECC_AGGR_STATUS_SET</a>     | 5270 3208h             |
| 20Ch   | 32     | <a href="#">ECC_AGGR_STATUS_CLR</a>     | 5270 320Ch             |

### 5.12.2 MCAN Registers

#### MCAN Registers

### 5.12.2.1 MSG\_RAM\_START Register

#### 1 MSG\_RAM\_START Register (Offset = 0h) [reset = 0h]

START.

Return to [Summary Table](#)

**Table 5-2044. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 0000h       |
| MCAN1         | 5261 0000h       |
| MCAN2         | 5262 0000h       |
| MCAN3         | 5263 0000h       |

**Figure 5-675. MSG\_RAM\_START Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-2046. MSG\_RAM\_START Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                    |
|------|-------|------|-------|--------------------------------|
| 31:0 | START | R/W  | 0h    | MCAN message mem Start address |

### 5.12.2.2 MSG\_RAM\_END Register

**1 MSG\_RAM\_END Register (Offset = 10FFCh) [reset = 0h]**

END.

Return to [Summary Table](#)

**Table 5-2047. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5261 0FFCh       |
| MCAN1         | 5262 0FFCh       |
| MCAN2         | 5263 0FFCh       |
| MCAN3         | 5264 0FFCh       |

**Figure 5-676. MSG\_RAM\_END Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 5-2049. MSG\_RAM\_END Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                  |
|------|-------|------|-------|------------------------------|
| 31:0 | END   | R/W  | 0h    | MCAN message mem End address |

### 5.12.2.3 CFG\_SS\_PID Register

#### 1 CFG\_SS\_PID Register (Offset = 0h) [reset = 68E05901h]

Revision Register. The Revision Register contains the major and minor revisions for the MCANSS.

Return to [Summary Table](#)

**Table 5-2050. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8000h       |
| MCAN1         | 5261 8000h       |
| MCAN2         | 5262 8000h       |
| MCAN3         | 5263 8000h       |

**Figure 5-677. CFG\_SS\_PID Name Register**

|           |    |       |    |           |       |    |    |
|-----------|----|-------|----|-----------|-------|----|----|
| 31        | 30 | 29    | 28 | 27        | 26    | 25 | 24 |
| SCHEME    |    | BU    |    | MODULE_ID |       |    |    |
| R         |    | R     |    | R         |       |    |    |
| 1h        |    | 2h    |    | 8E0h      |       |    |    |
| 23        | 22 | 21    | 20 | 19        | 18    | 17 | 16 |
| MODULE_ID |    |       |    |           |       |    |    |
| R         |    |       |    |           |       |    |    |
| 8E0h      |    |       |    |           |       |    |    |
| 15        | 14 | 13    | 12 | 11        | 10    | 9  | 8  |
| RTL       |    |       |    |           | MAJOR |    |    |
| R         |    |       |    |           | R     |    |    |
| Bh        |    |       |    |           | 1h    |    |    |
| 7         | 6  | 5     | 4  | 3         | 2     | 1  | 0  |
| CUSTOM    |    | MINOR |    |           |       |    |    |
| R         |    | R     |    |           |       |    |    |
| 0h        |    | 1h    |    |           |       |    |    |

**Table 5-2052. CFG\_SS\_PID Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                   |
|-------|-----------|------|-------|-----------------------------------------------|
| 31:30 | SCHEME    | R    | 1h    | PID register scheme                           |
| 29:28 | BU        | R    | 2h    | Business Unit: 10 = Processors                |
| 27:16 | MODULE_ID | R    | 8E0h  | Module ID                                     |
| 15:11 | RTL       | R    | Bh    | RTL revision. Will vary depending on release. |
| 10:8  | MAJOR     | R    | 1h    | Major revision                                |
| 7:6   | CUSTOM    | R    | 0h    | Custom                                        |
| 5:0   | MINOR     | R    | 1h    | Minor revision                                |

### 5.12.2.4 CFG\_SS\_CTRL Register

#### 1 CFG\_SS\_CTRL Register (Offset = 4h) [reset = 8h]

Control Register. The Control Register contains general control bits for the MCANSS.

Return to [Summary Table](#)

**Table 5-2053. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8004h       |
| MCAN1         | 5261 8004h       |
| MCAN2         | 5262 8004h       |
| MCAN3         | 5263 8004h       |

**Figure 5-678. CFG\_SS\_CTRL Name Register**

|     |                |            |             |              |    |    |    |
|-----|----------------|------------|-------------|--------------|----|----|----|
| 31  | 30             | 29         | 28          | 27           | 26 | 25 | 24 |
| NU0 |                |            |             |              |    |    |    |
| R   |                |            |             |              |    |    |    |
| 0h  |                |            |             |              |    |    |    |
| 23  | 22             | 21         | 20          | 19           | 18 | 17 | 16 |
| NU0 |                |            |             |              |    |    |    |
| R   |                |            |             |              |    |    |    |
| 0h  |                |            |             |              |    |    |    |
| 15  | 14             | 13         | 12          | 11           | 10 | 9  | 8  |
| NU0 |                |            |             |              |    |    |    |
| R   |                |            |             |              |    |    |    |
| 0h  |                |            |             |              |    |    |    |
| 7   | 6              | 5          | 4           | 3            | 2  | 1  | 0  |
| NU0 | EXT_TS_CNTR_EN | AUTOWAKEUP | WAKEUPREGEN | DBGSUSP_FREE | NU |    |    |
| R   | R/W            | R/W        | R/W         | R/W          | R  |    |    |
| 0h  | 0h             | 0h         | 0h          | 1h           | 0h |    |    |

**Table 5-2055. CFG\_SS\_CTRL Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                      |
|------|----------------|------|-------|--------------------------------------------------|
| 31:7 | NU0            | R    | 0h    | Reserved                                         |
| 6    | EXT_TS_CNTR_EN | R/W  | 0h    | External TimeStamp Counter Enable                |
| 5    | AUTOWAKEUP     | R/W  | 0h    | Automatic Wakeup Enable                          |
| 4    | WAKEUPREGEN    | R/W  | 0h    | Wakeup Request Enable                            |
| 3    | DBGSUSP_FREE   | R/W  | 1h    | 0-Honor Debug Suspend, 1-Disregard debug suspend |
| 2:0  | NU             | R    | 0h    | Reserved                                         |

### 5.12.2.5 CFG\_SS\_STAT Register

#### 1 CFG\_SS\_STAT Register (Offset = 8h) [reset = 6h]

Status Register. The Status Register provides general status bits for the MCANSS.

Return to [Summary Table](#)

**Table 5-2056. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8008h       |
| MCAN1         | 5261 8008h       |
| MCAN2         | 5262 8008h       |
| MCAN3         | 5263 8008h       |

**Figure 5-679. CFG\_SS\_STAT Name Register**

|     |    |    |    |    |         |          |    |
|-----|----|----|----|----|---------|----------|----|
| 31  | 30 | 29 | 28 | 27 | 26      | 25       | 24 |
| NU1 |    |    |    |    |         |          |    |
| NU1 |    |    |    |    |         |          |    |
| 0h  |    |    |    |    |         |          |    |
| 23  | 22 | 21 | 20 | 19 | 18      | 17       | 16 |
| NU1 |    |    |    |    |         |          |    |
| NU1 |    |    |    |    |         |          |    |
| 0h  |    |    |    |    |         |          |    |
| 15  | 14 | 13 | 12 | 11 | 10      | 9        | 8  |
| NU1 |    |    |    |    |         |          |    |
| NU1 |    |    |    |    |         |          |    |
| 0h  |    |    |    |    |         |          |    |
| 7   | 6  | 5  | 4  | 3  | 2       | 1        | 0  |
| NU1 |    |    |    |    | EN_FDOE | MMI_DONE | NU |
| NU1 |    |    |    |    | R       | R        | R  |
| 0h  |    |    |    |    | 1h      | 1h       | 0h |

**Table 5-2058. CFG\_SS\_STAT Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                          |
|------|----------|------|-------|--------------------------------------------------------------------------------------|
| 31:3 | NU1      | NU1  | 0h    | Reserved                                                                             |
| 2    | EN_FDOE  | R    | 1h    | Enable FD configuration. Reflects the value of mcanss_enable_fdoe configuration port |
| 1    | MMI_DONE | R    | 1h    | 0:Memory Initialization is in progress, 1:Memory Initialization Done                 |
| 0    | NU       | R    | 0h    | Reserved                                                                             |

### 5.12.2.6 CFG\_SS\_ICS Register

#### 1 CFG\_SS\_ICS Register (Offset = Ch) [reset = 0h]

Interrupt Clear Shadow Register. Write 1 to clear interrupt bits.

Return to [Summary Table](#)

**Table 5-2059. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 800Ch       |
| MCAN1         | 5261 800Ch       |
| MCAN2         | 5262 800Ch       |
| MCAN3         | 5263 800Ch       |

**Figure 5-680. CFG\_SS\_ICS Name Register**

|    |    |    |    |     |    |    |     |
|----|----|----|----|-----|----|----|-----|
| 31 | 30 | 29 | 28 | 27  | 26 | 25 | 24  |
|    |    |    |    | NU2 |    |    |     |
|    |    |    |    | NU2 |    |    |     |
|    |    |    |    | 0h  |    |    |     |
| 23 | 22 | 21 | 20 | 19  | 18 | 17 | 16  |
|    |    |    |    | NU2 |    |    |     |
|    |    |    |    | NU2 |    |    |     |
|    |    |    |    | 0h  |    |    |     |
| 15 | 14 | 13 | 12 | 11  | 10 | 9  | 8   |
|    |    |    |    | NU2 |    |    |     |
|    |    |    |    | NU2 |    |    |     |
|    |    |    |    | 0h  |    |    |     |
| 7  | 6  | 5  | 4  | 3   | 2  | 1  | 0   |
|    |    |    |    | NU2 |    |    | ICS |
|    |    |    |    | NU2 |    |    | W   |
|    |    |    |    | 0h  |    |    | 0h  |

**Table 5-2061. CFG\_SS\_ICS Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                  |
|------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | NU2   | NU2  | 0h    | Reserved                                                                                                                                     |
| 0    | ICS   | W    | 0h    | This bit contains the External TimeStamp Counter Overflow Interrupt status. Write '1' to clear bits. [ICS - Interrupt Clear Shadow Register] |

### 5.12.2.7 CFG\_SS\_IRS Register

#### 1 CFG\_SS\_IRS Register (Offset = 10h) [reset = 0h]

Interrupt Raw Status Register. Write 1 to set interrupt bits.

Return to [Summary Table](#)

**Table 5-2062. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8010h       |
| MCAN1         | 5261 8010h       |
| MCAN2         | 5262 8010h       |
| MCAN3         | 5263 8010h       |

**Figure 5-681. CFG\_SS\_IRS Name Register**

|     |    |    |    |    |    |    |     |
|-----|----|----|----|----|----|----|-----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24  |
| NU3 |    |    |    |    |    |    |     |
| R   |    |    |    |    |    |    |     |
| 0h  |    |    |    |    |    |    |     |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16  |
| NU3 |    |    |    |    |    |    |     |
| R   |    |    |    |    |    |    |     |
| 0h  |    |    |    |    |    |    |     |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8   |
| NU3 |    |    |    |    |    |    |     |
| R   |    |    |    |    |    |    |     |
| 0h  |    |    |    |    |    |    |     |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0   |
| NU3 |    |    |    |    |    |    | IRS |
| R   |    |    |    |    |    |    | R   |
| 0h  |    |    |    |    |    |    | 0h  |

**Table 5-2064. CFG\_SS\_IRS Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                            |
|------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------|
| 31:1 | NU3   | R    | 0h    | Reserved                                                                                                               |
| 0    | IRS   | R    | 0h    | External TimeStamp Counter Overflow Interrupt status. Read raw interrupt status. [IRS - Interrupt Raw Status Register] |



### 5.12.2.8 CFG\_SS\_IECS Register

#### 1 CFG\_SS\_IECS Register (Offset = 14h) [reset = 0h]

Interrupt Enable Clear Shadow Register. Write 1 to clear interrupt enable bits.

Return to [Summary Table](#)

**Table 5-2065. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8014h       |
| MCAN1         | 5261 8014h       |
| MCAN2         | 5262 8014h       |
| MCAN3         | 5263 8014h       |

**Figure 5-682. CFG\_SS\_IECS Name Register**

|     |    |    |    |    |    |    |      |
|-----|----|----|----|----|----|----|------|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24   |
| NU4 |    |    |    |    |    |    |      |
| R   |    |    |    |    |    |    |      |
| 0h  |    |    |    |    |    |    |      |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16   |
| NU4 |    |    |    |    |    |    |      |
| R   |    |    |    |    |    |    |      |
| 0h  |    |    |    |    |    |    |      |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8    |
| NU4 |    |    |    |    |    |    |      |
| R   |    |    |    |    |    |    |      |
| 0h  |    |    |    |    |    |    |      |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0    |
| NU4 |    |    |    |    |    |    | IECS |
| R   |    |    |    |    |    |    | W    |
| 0h  |    |    |    |    |    |    | 0h   |

**Table 5-2067. CFG\_SS\_IECS Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                             |
|------|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------|
| 31:1 | NU4   | R    | 0h    | Reserved                                                                                                                |
| 0    | IECS  | W    | 0h    | External TimeStamp Counter Overflow Interrupt. Write '1' to clear bits. [IECS - Interrupt Enable Clear Shadow Register] |

### 5.12.2.9 CFG\_SS\_IE Register

#### 1 CFG\_SS\_IE Register (Offset = 18h) [reset = 0h]

Interrupt Enable Register. Write 1 to set interrupt bits.

Return to [Summary Table](#)

**Table 5-2068. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8018h       |
| MCAN1         | 5261 8018h       |
| MCAN2         | 5262 8018h       |
| MCAN3         | 5263 8018h       |

**Figure 5-683. CFG\_SS\_IE Name Register**

|     |    |    |    |    |    |    |     |
|-----|----|----|----|----|----|----|-----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24  |
| NU5 |    |    |    |    |    |    |     |
| R   |    |    |    |    |    |    |     |
| 0h  |    |    |    |    |    |    |     |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16  |
| NU5 |    |    |    |    |    |    |     |
| R   |    |    |    |    |    |    |     |
| 0h  |    |    |    |    |    |    |     |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8   |
| NU5 |    |    |    |    |    |    |     |
| R   |    |    |    |    |    |    |     |
| 0h  |    |    |    |    |    |    |     |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0   |
| NU5 |    |    |    |    |    |    | IE  |
| R   |    |    |    |    |    |    | R/W |
| 0h  |    |    |    |    |    |    | 0h  |

**Table 5-2070. CFG\_SS\_IE Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                       |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | NU5   | R    | 0h    | Reserved                                                                                                                                          |
| 0    | IE    | R/W  | 0h    | External TimeStamp Counter Overflow Interrupt. Write '1' to set interrupt enable. Read returns interrupt enable. [IE - Interrupt Enable Register] |

### 5.12.2.10 CFG\_SS\_IES Register

#### 1 CFG\_SS\_IES Register (Offset = 1Ch) [reset = 0h]

Interrupt Enable Status Register. Read enabled interrupts.

Return to [Summary Table](#)

**Table 5-2071. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 801Ch       |
| MCAN1         | 5261 801Ch       |
| MCAN2         | 5262 801Ch       |
| MCAN3         | 5263 801Ch       |

**Figure 5-684. CFG\_SS\_IES Name Register**

|     |    |    |    |    |    |    |     |
|-----|----|----|----|----|----|----|-----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24  |
| NU6 |    |    |    |    |    |    |     |
| R   |    |    |    |    |    |    |     |
| 0h  |    |    |    |    |    |    |     |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16  |
| NU6 |    |    |    |    |    |    |     |
| R   |    |    |    |    |    |    |     |
| 0h  |    |    |    |    |    |    |     |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8   |
| NU6 |    |    |    |    |    |    |     |
| R   |    |    |    |    |    |    |     |
| 0h  |    |    |    |    |    |    |     |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0   |
| NU6 |    |    |    |    |    |    | IES |
| R   |    |    |    |    |    |    | R   |
| 0h  |    |    |    |    |    |    | 0h  |

**Table 5-2073. CFG\_SS\_IES Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                             |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------|
| 31:1 | NU6   | R    | 0h    | Reserved                                                                                                |
| 0    | IES   | R    | 0h    | External TimeStamp Counter Overflow Interrupt. Read Enabled Interrupts. [IES - Interrupt Enable Status] |

### 5.12.2.11 CFG\_SS\_EOI Register

#### 1 CFG\_SS\_EOI Register (Offset = 20h) [reset = 0h]

End Of Interrupt (EOI) Register. The EOI register is used to re-trigger the pulse interrupt signal to ensure that any nested interrupt events are serviced. For level interrupt signals the EOI register is not functional and must not be used.

Return to [Summary Table](#)

**Table 5-2074. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8020h       |
| MCAN1         | 5261 8020h       |
| MCAN2         | 5262 8020h       |
| MCAN3         | 5263 8020h       |

**Figure 5-685. CFG\_SS\_EOI Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| NU7 |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| NU7 |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| NU7 |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| EOI |    |    |    |    |    |    |    |
| W   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 5-2076. CFG\_SS\_EOI Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | NU7   | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                        |
| 7:0  | EOI   | W    | 0h    | Write with bit position of targeted interrupt. [E.g. Ext TS is bit 0]. Upon write, level interrupt will clear and if unserviced interrupt counter > 1 will issue another pulse interrupt.<br>Field values:<br>8'h00: EOI value for External TS interrupt<br>8'h01: EOI value for mcan[0] interrupt<br>8'h02: EOI value for mcan[1] interrupt<br>All other values are not applicable<br>[EOI - End Of Interrupt] |

### 5.12.2.12 CFG\_SS\_EXT\_TS\_PS Register

#### 1 CFG\_SS\_EXT\_TS\_PS Register (Offset = 24h) [reset = 0h]

External Timestamp Prescaler Register.

Return to [Summary Table](#)

**Table 5-2077. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8024h       |
| MCAN1         | 5261 8024h       |
| MCAN2         | 5262 8024h       |
| MCAN3         | 5263 8024h       |

**Figure 5-686. CFG\_SS\_EXT\_TS\_PS Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| NU8      |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PRESCALE |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PRESCALE |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PRESCALE |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2079. CFG\_SS\_EXT\_TS\_PS Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                      |
|-------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | NU8      | R    | 0h    | Reserved                                                                                                                                                                         |
| 23:0  | PRESCALE | R/W  | 0h    | External Timestamp Prescaler reload value.<br>External Timestamp count rate is host clock rate divided by this value with one exception: a value of 0 has the same effect as 1 . |

### 5.12.2.13 CFG\_SS\_EXT\_TS\_USIC Register

#### 1 CFG\_SS\_EXT\_TS\_USIC Register (Offset = 28h) [reset = 0h]

External Timestamp Unserved Interrupts Counter Register.

Return to [Summary Table](#)

**Table 5-2080. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8028h       |
| MCAN1         | 5261 8028h       |
| MCAN2         | 5262 8028h       |
| MCAN3         | 5263 8028h       |

**Figure 5-687. CFG\_SS\_EXT\_TS\_USIC Name Register**

|     |    |    |    |                  |    |    |    |
|-----|----|----|----|------------------|----|----|----|
| 31  | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| NU9 |    |    |    |                  |    |    |    |
| R   |    |    |    |                  |    |    |    |
| 0h  |    |    |    |                  |    |    |    |
| 23  | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| NU9 |    |    |    |                  |    |    |    |
| R   |    |    |    |                  |    |    |    |
| 0h  |    |    |    |                  |    |    |    |
| 15  | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| NU9 |    |    |    |                  |    |    |    |
| R   |    |    |    |                  |    |    |    |
| 0h  |    |    |    |                  |    |    |    |
| 7   | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| NU9 |    |    |    | EXT_TS_INTR_CNTR |    |    |    |
| R   |    |    |    | R                |    |    |    |
| 0h  |    |    |    | 0h               |    |    |    |

**Table 5-2082. CFG\_SS\_EXT\_TS\_USIC Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                                                                  |
|------|------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:5 | NU9              | R    | 0h    | Reserved                                                                                                                                                     |
| 4:0  | EXT_TS_INTR_CNTR | R    | 0h    | Number of unserved rollover interrupts. If >1 an EOI write will issue another pulse interrupt [EXT_TS_USIC - External TImeStamp Unserved Interrupts Counter] |

### 5.12.2.14 CFG\_CREL Register

#### 1 CFG\_CREL Register (Offset = 200h) [reset = 32380608h]

Core Release Register. Release dependent constant (version + date).

Return to [Summary Table](#)

**Table 5-2083. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8200h       |
| MCAN1         | 5261 8200h       |
| MCAN2         | 5262 8200h       |
| MCAN3         | 5263 8200h       |

**Figure 5-688. CFG\_CREL Name Register**

|         |    |    |    |      |    |    |    |
|---------|----|----|----|------|----|----|----|
| 31      | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
| REL     |    |    |    | STEP |    |    |    |
| R       |    |    |    | R    |    |    |    |
| 3h      |    |    |    | 2h   |    |    |    |
| 23      | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| SUBSTEP |    |    |    | YEAR |    |    |    |
| R       |    |    |    | R    |    |    |    |
| 3h      |    |    |    | 8h   |    |    |    |
| 15      | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| MON     |    |    |    |      |    |    |    |
| R       |    |    |    |      |    |    |    |
| 6h      |    |    |    |      |    |    |    |
| 7       | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| DAY     |    |    |    |      |    |    |    |
| R       |    |    |    |      |    |    |    |
| 8h      |    |    |    |      |    |    |    |

**Table 5-2085. CFG\_CREL Register Field Descriptions**

| Bit   | Field   | Type | Reset | Description              |
|-------|---------|------|-------|--------------------------|
| 31:28 | REL     | R    | 3h    | Core Release             |
| 27:24 | STEP    | R    | 2h    | Step of Core Release     |
| 23:20 | SUBSTEP | R    | 3h    | Sub-Step of Core Release |
| 19:16 | YEAR    | R    | 8h    | Time Stamp Year          |
| 15:8  | MON     | R    | 6h    | Time Stamp Month         |
| 7:0   | DAY     | R    | 8h    | Time Stamp Day           |

### 5.12.2.15 CFG\_ENDN Register

#### 1 CFG\_ENDN Register (Offset = 204h) [reset = 87654321h]

Endian Register. Constant 8765 4321h.

Return to [Summary Table](#)

**Table 5-2086. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8204h       |
| MCAN1         | 5261 8204h       |
| MCAN2         | 5262 8204h       |
| MCAN3         | 5263 8204h       |

**Figure 5-689. CFG\_ENDN Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ETV       |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 87654321h |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ETV       |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 87654321h |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ETV       |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 87654321h |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ETV       |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 87654321h |    |    |    |    |    |    |    |

**Table 5-2088. CFG\_ENDN Register Field Descriptions**

| Bit  | Field | Type | Reset     | Description          |
|------|-------|------|-----------|----------------------|
| 31:0 | ETV   | R    | 87654321h | Endianess test value |



### 5.12.2.16 CFG\_CUST Register

#### 1 CFG\_CUST Register (Offset = 208h) [reset = 0h]

Custom Register.

Return to [Summary Table](#)

**Table 5-2089. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8208h       |
| MCAN1         | 5261 8208h       |
| MCAN2         | 5262 8208h       |
| MCAN3         | 5263 8208h       |

**Figure 5-690. CFG\_CUST Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CUST |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CUST |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CUST |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CUST |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-2091. CFG\_CUST Register Field Descriptions**

| Bit  | Field | Type | Reset | Description |
|------|-------|------|-------|-------------|
| 31:0 | CUST  | R    | 0h    | Custom      |

### 5.12.2.17 CFG\_DBTP Register

#### 1 CFG\_DBTP Register (Offset = 20Ch) [reset = A33h]

Data Bit Timing & Prescaler Register.

Configuration of data phase bit timing, transmitter delay compensation enable. This register is only writable if the MCAN\_CCCR[1] CCE and MCAN\_CCCR[0] INIT bits are set. The CAN bit time may be programmed in the range of 4 to 49 time quanta. The CAN time quantum may be programmed in the range of 1 to 32 MCAN functional clock periods.  $t_q = (\text{MCAN\_DBTP}[20-16] \text{ DBRP} + 1) \text{ mtq}$  (minimum time quantum = CAN clock period (MCAN functional clock)). The MCAN\_DBTP[12-8] DTSEG1 field is the sum of Prop\_Seg and Phase\_Seg1. The MCAN\_DBTP[7-4] DTSEG2 field is Phase\_Seg2. Therefore the length of the bit time is (programmed values)  $[\text{MCAN\_DBTP}[12-8] \text{ DTSEG1} + \text{MCAN\_DBTP}[7-4] \text{ DTSEG2} + 3] t_q$  or (functional values)  $[\text{Sync\_Seg} + \text{Prop\_Seg} + \text{Phase\_Seg1} + \text{Phase\_Seg2}] t_q$ . The Information Processing Time (IPT) is zero, meaning the data for the next bit is available at the first clock edge after the sample point.

Note: With a CAN clock (MCAN functional clock) of 8 MHz, the reset value of 0000 0A33h configures the MCAN module for a data phase bit rate of 500 kbit/s.

Note: The bit rate configured for the CAN FD data phase via the MCAN\_DBTP register must be higher or equal to the bit rate configured for the arbitration phase via the MCAN\_DBTP register.

Return to [Summary Table](#)

**Table 5-2092. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 820Ch       |
| MCAN1         | 5261 820Ch       |
| MCAN2         | 5262 820Ch       |
| MCAN3         | 5263 820Ch       |

**Figure 5-691. CFG\_DBTP Name Register**

|        |      |    |    |        |    |    |    |
|--------|------|----|----|--------|----|----|----|
| 31     | 30   | 29 | 28 | 27     | 26 | 25 | 24 |
| NU13   |      |    |    |        |    |    |    |
| R      |      |    |    |        |    |    |    |
| 0h     |      |    |    |        |    |    |    |
| 23     | 22   | 21 | 20 | 19     | 18 | 17 | 16 |
| TDC    | NU12 |    |    | DBRP   |    |    |    |
| R/W    | R    |    |    | R/W    |    |    |    |
| 0h     | 0h   |    |    | 0h     |    |    |    |
| 15     | 14   | 13 | 12 | 11     | 10 | 9  | 8  |
| NU11   |      |    |    | DTSEG1 |    |    |    |
| R      |      |    |    | R/W    |    |    |    |
| 0h     |      |    |    | Ah     |    |    |    |
| 7      | 6    | 5  | 4  | 3      | 2  | 1  | 0  |
| DTSEG2 |      |    |    | DSJW   |    |    |    |
| R/W    |      |    |    | R/W    |    |    |    |
| 3h     |      |    |    | 3h     |    |    |    |

**Table 5-2094. CFG\_DBTP Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                       |
|-------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | NU13  | R    | 0h    | Reserved                                                                                                                          |
| 23    | TDC   | R/W  | 0h    | Transmitter Delay Compensation<br>1'b0 = Transmitter Delay Compensation disabled<br>1'b1 = Transmitter Delay Compensation enabled |

**Table 5-2094. CFG\_DBTP Register Field Descriptions (continued)**

| Bit   | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                              |
|-------|--------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 22:21 | NU12   | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                 |
| 20:16 | DBRP   | R/W  | 0h    | Data Baud Rate Prescaler<br>The value by which the oscillator frequency is divided for generating the bit time quanta. The bit time is built up from a multiple of this quanta.<br>The actual interpretation by the hardware of this value is such that one more than the value programmed here is used. |
| 15:13 | NU11   | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                 |
| 12:8  | DTSEG1 | R/W  | Ah    | Data time segment before sample point.<br>The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.                                                                                                                                          |
| 7:4   | DTSEG2 | R/W  | 3h    | Data time segment after sample point.<br>The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.                                                                                                                                           |
| 3:0   | DSJW   | R/W  | 3h    | Data resynchronization Jump Width.<br>The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.                                                                                                                                              |

### 5.12.2.18 CFG\_TEST Register

#### 1 CFG\_TEST Register (Offset = 210h) [reset = 0h]

Test Register. Test mode selection. Write access to the MCAN\_TEST register has to be enabled by setting the MCAN\_CCCR[7] TEST bit.

Return to [Summary Table](#)

**Table 5-2095. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8210h       |
| MCAN1         | 5261 8210h       |
| MCAN2         | 5262 8210h       |
| MCAN3         | 5263 8210h       |

**Figure 5-692. CFG\_TEST Name Register**

|      |     |    |      |      |    |    |    |
|------|-----|----|------|------|----|----|----|
| 31   | 30  | 29 | 28   | 27   | 26 | 25 | 24 |
| NU15 |     |    |      |      |    |    |    |
| R    |     |    |      |      |    |    |    |
| 0h   |     |    |      |      |    |    |    |
| 23   | 22  | 21 | 20   | 19   | 18 | 17 | 16 |
| NU15 |     |    |      |      |    |    |    |
| R    |     |    |      |      |    |    |    |
| 0h   |     |    |      |      |    |    |    |
| 15   | 14  | 13 | 12   | 11   | 10 | 9  | 8  |
| NU15 |     |    |      |      |    |    |    |
| R    |     |    |      |      |    |    |    |
| 0h   |     |    |      |      |    |    |    |
| 7    | 6   | 5  | 4    | 3    | 2  | 1  | 0  |
| RX   | TX  |    | LBCK | NU14 |    |    |    |
| R    | R/W |    | R/W  | R    |    |    |    |
| 0h   | 0h  |    | 0h   | 0h   |    |    |    |

**Table 5-2097. CFG\_TEST Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                     |
|------|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | NU15  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                        |
| 7    | RX    | R    | 0h    | Receive Pin<br>Monitors the actual value of the MCAN RX pin<br>1'b0 = The CAN bus is dominant<br>1'b1 = The CAN bus is recessive                                                                                                                                                                |
| 6:5  | TX    | R/W  | 0h    | Control of Transmit Pin<br>2'b00 = Reset value, the MCAN TX pin controlled by the CAN Core, updated at the end of the CAN bit time<br>2'b01 = Sample Point can be monitored at the MCAN TX pin<br>2'b10 = Dominant ('0') level at the MCAN TX pin<br>2'b11 = Recessive ('1') at the MCAN TX pin |
| 4    | LBCK  | R/W  | 0h    | Loop Back Mode<br>1'b0 = Reset value, Loopback Mode is disabled<br>1'b1 = Loopback Mode is enabled(see Test Modes)                                                                                                                                                                              |
| 3:0  | NU14  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                        |

### 5.12.2.19 CFG\_RWD Register

#### 1 CFG\_RWD Register (Offset = 214h) [reset = 0h]

RAM Watchdog. Monitors the READY output of the Message RAM.

Return to [Summary Table](#)

**Table 5-2098. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8214h       |
| MCAN1         | 5261 8214h       |
| MCAN2         | 5262 8214h       |
| MCAN3         | 5263 8214h       |

**Figure 5-693. CFG\_RWD Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| NU16 |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| NU16 |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| WDV  |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| WDC  |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-2100. CFG\_RWD Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                      |
|-------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | NU16  | R    | 0h    | Reserved                                                                                                                         |
| 15:8  | WDV   | R    | 0h    | Watchdog Value<br>Actual Message RAM Watchdog Counter Value.                                                                     |
| 7:0   | WDC   | R/W  | 0h    | Watchdog Counter Value<br>Start value of the Message RAM Watchdog Counter. With the reset value of 8'h0 the counter is disabled. |

### 5.12.2.20 CFG\_CCCR Register

#### 1 CFG\_CCCR Register (Offset = 218h) [reset = 1h]

CC Control Register. Operation mode configuration.

Return to [Summary Table](#)

**Table 5-2101. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8218h       |
| MCAN1         | 5261 8218h       |
| MCAN2         | 5262 8218h       |
| MCAN3         | 5263 8218h       |

**Figure 5-694. CFG\_CCCR Name Register**

|      |     |      |      |      |     |      |      |
|------|-----|------|------|------|-----|------|------|
| 31   | 30  | 29   | 28   | 27   | 26  | 25   | 24   |
| NU18 |     |      |      |      |     |      |      |
| R/W  |     |      |      |      |     |      |      |
| 0h   |     |      |      |      |     |      |      |
| 23   | 22  | 21   | 20   | 19   | 18  | 17   | 16   |
| NU18 |     |      |      |      |     |      |      |
| R/W  |     |      |      |      |     |      |      |
| 0h   |     |      |      |      |     |      |      |
| 15   | 14  | 13   | 12   | 11   | 10  | 9    | 8    |
| NU18 | TXP | EFBI | PXHD | NU17 |     | BRSE | FDOE |
| R/W  | R/W | R/W  | R/W  | R    |     | R/W  | R/W  |
| 0h   | 0h  | 0h   | 0h   | 0h   |     | 0h   | 0h   |
| 7    | 6   | 5    | 4    | 3    | 2   | 1    | 0    |
| TEST | DAR | MON  | CSR  | CSA  | ASM | CCE  | INIT |
| R/W  | R/W | R/W  | R/W  | R    | R/W | R/W  | R/W  |
| 0h   | 0h  | 0h   | 0h   | 0h   | 0h  | 0h   | 1h   |

**Table 5-2103. CFG\_CCCR Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                          |
|-------|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:15 | NU18  | R/W  | 0h    | Reserved                                                                                                                                                                                                                                                                             |
| 14    | TXP   | R/W  | 0h    | Transmit Pause<br>If this bit is set, the MCAN module pauses for two CAN bit times before starting the next transmission after itself has successfully transmitted a frame(see Tx Handling) .<br>1'b0 = Transmit pause disabled<br>1'b1 = Transmit pause enabled                     |
| 13    | EFBI  | R/W  | 0h    | Edge Filtering durign Bus Integration<br>1'b0 = Edge filtering disabled<br>1'b1 = Two consecutive dominant tq required to detect an edge for hard synchronization                                                                                                                    |
| 12    | PXHD  | R/W  | 0h    | Protocol Exception Handling Disable<br>1'b0 = Protocol exception handling enabled<br>1'b1 = Protocol exception handling disabled<br>Note: When protocol exception handling is disabled, the MCAN module will transmit an error frame when it detects a protocol exception condition. |
| 11:10 | NU17  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                             |

**Table 5-2103. CFG\_CCCR Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-----|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9   | BRSE  | R/W  | 0h    | Bit Rate Switch Enable<br>1'b0 = Bit rate switching for transmissions disabled<br>1'b1 = Bit rate switching for transmissions enabled<br>Note: When CAN FD operation is disabled the MCAN_CCCR[8] FDOE = 1'b0, the MCAN_CCCR[9] BRSE bit is not evaluated.                                                                                                                                                                                                               |
| 8   | FDOE  | R/W  | 0h    | FD Operation Enable<br>1'b0 = FD operation disabled<br>1'b1 = FD operation enabled                                                                                                                                                                                                                                                                                                                                                                                       |
| 7   | TEST  | R/W  | 0h    | Test Mode enable<br>1'b0 = Normal operation. The MCAN_TEST register holds reset values. 1'b1 = Test Mode. Write access to the MCAN_TEST register enabled                                                                                                                                                                                                                                                                                                                 |
| 6   | DAR   | R/W  | 0h    | Disable Automatic Regransmission<br>1'b0 = Automatic retransmission of messages not transmitted successfully enabled<br>1'b1 = Automatic retransmission disabled                                                                                                                                                                                                                                                                                                         |
| 5   | MON   | R/W  | 0h    | Bus Monitoring Mode<br>The MCAN_CCCR[5] MON bit can only be set by the Host CPU when both MCAN_CCCR[1] CCE and MCAN_CCCR[0] INIT bits are set to 1. The bit can be reset by the Host CPU at any time.<br>1'b0 = Bus Monitoring Mode is disabled<br>1'b1 = Bus Monitoring Mode is enabled                                                                                                                                                                                 |
| 4   | CSR   | R/W  | 0h    | Clock Stop Request<br>1'b0 = No clock stop is requested<br>1'b1 = Clock stop requested. When clock stop is requested, first the MCAN_CCCR[0] INIT bit and then the MCAN_CCCR[3] CSA bit will be set after all pending transfer requests have been completed and the CAN bus reached idle.                                                                                                                                                                                |
| 3   | CSA   | R    | 0h    | Clock Stop Acknowledge<br>1'b0 = No clock stop acknowledged<br>1'b1 = The MCAN module may be set in power down by stopping MCAN interface clock and MCAN functional clock                                                                                                                                                                                                                                                                                                |
| 2   | ASM   | R/W  | 0h    | Restricted Operation Mode<br>The MCAN_CCCR[2] ASM bit can only be set by the Host CPU when both MCAN_CCCR[1] CCE and MCAN_CCCR[0] INIT bits are set to 1. The bit can be reset by the Host CPU at any time. For a description of the Restricted Operation Mode, see Restricted Operation Mode.<br>1'b0 = Normal CAN operation<br>1'b1 = Restricted Operation Mode active                                                                                                 |
| 1   | CCE   | R/W  | 0h    | Configuration Change Enable<br>1'b0 = The Host CPU has no write access to the protected configuration registers<br>1'b1 = The Host CPU has write access to the protected configuration registers (while the MCAN_CCCR[0] INIT = 1)                                                                                                                                                                                                                                       |
| 0   | INIT  | R/W  | 1h    | Initialization<br>1'b0 = Normal Operation<br>1'b1 = Initialization is started<br>Note: Due to the synchronization mechanism between the two clock domains, there may be a delay until the value written to the MCAN_CCCR[0] INIT bit can be read back. Therefore the software has to assure that the previous value written to the MCAN_CCCR[0] INIT bit has been accepted by Reading the MCAN_CCCR[0] INIT bit before setting the MCAN_CCCR[0] INIT bit to a new value. |

### 5.12.2.21 CFG\_NBTP Register

#### 1 CFG\_NBTP Register (Offset = 21Ch) [reset = 6000A03h]

Nominal Bit Timing & Prescaler Register. Configuration of arbitration phase bit timing.

This register is only writable if the MCAN\_CCCR[1] CCE and MCAN\_CCCR[0] INIT bits are set. The CAN bit time may be programmed in the range of 4 to 385 time quanta. The CAN time quantum may be programmed in the range of 1 to 512 MCAN functional clock periods.  $t_q = (\text{MCAN\_NBTP}[24-16] \text{ NBRP} + 1) \text{ mtq}$ . The MCAN\_NBTP[15-8] NTSEG1 field is the sum of Prop\_Seg and Phase\_Seg1. The MCAN\_NBTP[6-0] NTSEG2 field is Phase\_Seg2.

Therefore the length of the bit time is (programmed values)  $[\text{MCAN\_NBTP}[15-8] \text{ NTSEG1} + \text{MCAN\_NBTP}[6-0] \text{ NTSEG2} + 3] t_q$  or (functional values)  $[\text{Sync\_Seg} + \text{Prop\_Seg} + \text{Phase\_Seg1} + \text{Phase\_Seg2}] t_q$ .

The Information Processing Time (IPT) is zero, meaning the data for the next bit is available at the first clock edge after the sample point.

Return to [Summary Table](#)

**Table 5-2104. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 821Ch       |
| MCAN1         | 5261 821Ch       |
| MCAN2         | 5262 821Ch       |
| MCAN3         | 5263 821Ch       |

**Figure 5-695. CFG\_NBTP Name Register**

|        |        |    |    |    |    |    |      |
|--------|--------|----|----|----|----|----|------|
| 31     | 30     | 29 | 28 | 27 | 26 | 25 | 24   |
| NSJW   |        |    |    |    |    |    | NBRP |
| R/W    |        |    |    |    |    |    | R/W  |
| 3h     |        |    |    |    |    |    | 0h   |
| 23     | 22     | 21 | 20 | 19 | 18 | 17 | 16   |
| NBRP   |        |    |    |    |    |    |      |
| R/W    |        |    |    |    |    |    |      |
| 0h     |        |    |    |    |    |    |      |
| 15     | 14     | 13 | 12 | 11 | 10 | 9  | 8    |
| NTSEG1 |        |    |    |    |    |    |      |
| R/W    |        |    |    |    |    |    |      |
| Ah     |        |    |    |    |    |    |      |
| 7      | 6      | 5  | 4  | 3  | 2  | 1  | 0    |
| NU19   | NTSEG2 |    |    |    |    |    |      |
| R      | R/W    |    |    |    |    |    |      |
| 0h     | 3h     |    |    |    |    |    |      |

**Table 5-2106. CFG\_NBTP Register Field Descriptions**

| Bit   | Field  | Type | Reset | Description                              |
|-------|--------|------|-------|------------------------------------------|
| 31:25 | NSJW   | R/W  | 3h    | Nominal Resynchronization Jump Width     |
| 24:16 | NBRP   | R/W  | 0h    | Nominal Baud Rate Prescaler              |
| 15:8  | NTSEG1 | R/W  | Ah    | Nominal Time segment before sample point |
| 7     | NU19   | R    | 0h    | Reserved                                 |
| 6:0   | NTSEG2 | R/W  | 3h    | Nominal Time segment after sample point  |



### 5.12.2.22 CFG\_TSCC Register

#### 1 CFG\_TSCC Register (Offset = 220h) [reset = 0h]

Timestamp Counter Configuration. Timestamp counter prescaler setting, selection of internal/external timestamp vector.

Return to [Summary Table](#)

**Table 5-2107. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8220h       |
| MCAN1         | 5261 8220h       |
| MCAN2         | 5262 8220h       |
| MCAN3         | 5263 8220h       |

**Figure 5-696. CFG\_TSCC Name Register**

|      |    |    |    |     |    |     |    |
|------|----|----|----|-----|----|-----|----|
| 31   | 30 | 29 | 28 | 27  | 26 | 25  | 24 |
| NU21 |    |    |    |     |    |     |    |
| R    |    |    |    |     |    |     |    |
| 0h   |    |    |    |     |    |     |    |
| 23   | 22 | 21 | 20 | 19  | 18 | 17  | 16 |
| NU21 |    |    |    | TCP |    |     |    |
| R    |    |    |    | R/W |    |     |    |
| 0h   |    |    |    | 0h  |    |     |    |
| 15   | 14 | 13 | 12 | 11  | 10 | 9   | 8  |
| NU20 |    |    |    |     |    |     |    |
| R    |    |    |    |     |    |     |    |
| 0h   |    |    |    |     |    |     |    |
| 7    | 6  | 5  | 4  | 3   | 2  | 1   | 0  |
| NU20 |    |    |    |     |    | TSS |    |
| R    |    |    |    |     |    | R/W |    |
| 0h   |    |    |    |     |    | 0h  |    |

**Table 5-2109. CFG\_TSCC Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                  |
|-------|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | NU21  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                     |
| 19:16 | TCP   | R/W  | 0h    | Timestamp Counter Prescaler<br>Configures the timestamp and timeout counters time unit in multiples of CAN bit times [1-16]. The actual interpretation by the hardware of this value is such that one more than the value programmed here is used.<br>Note: With CAN FD an external counter is required for timestamp generation. MCAN_TSCC[1-0] TSS = 2'b10 |
| 15:2  | NU20  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                     |
| 1:0   | TSS   | R/W  | 0h    | Timestamp Select<br>2'b00 = Timestamp counter value always 0<br>2'b01 = Timestamp counter value incremented according to the MCAN_TSCC[19-16] TCP field<br>2'b10 = External timestamp counter value used<br>2'b11 = Same as 2'b00                                                                                                                            |

### 5.12.2.23 CFG\_TSCV Register

#### 1 CFG\_TSCV Register (Offset = 224h) [reset = 0h]

Timestamp Counter Value.

Return to [Summary Table](#)

**Table 5-2110. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8224h       |
| MCAN1         | 5261 8224h       |
| MCAN2         | 5262 8224h       |
| MCAN3         | 5263 8224h       |

**Figure 5-697. CFG\_TSCV Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| NU22 |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| NU22 |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TSC  |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TSC  |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-2112. CFG\_TSCV Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | NU22  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 15:0  | TSC   | R/W  | 0h    | <p>Timestamp Counter</p> <p>The internal/external Timestamp Counter value is captured on start of frame (both Rx and Tx).</p> <p>When the MCAN_TSCC[1-0] TSS = 2'b01, the Timestamp Counter is incremented in multiples of CAN bit times [1-16] depending on the configuration of the MCAN_TSCC[19-16] TCP field. A wrap around sets interrupt flag MCAN_IR[16] TSW.</p> <p>Write access resets the counter to zero. When the MCAN_TSCC[1-0] TSS = 2'b10, the MCAN_TSCV[15-0] TSC field reflects the external Timestamp Counter value. A write access has no impact.</p> <p>Note: A 'wrap around' is a change of the Timestamp Counter value from non-zero to zero not caused by write access to the MCAN_TSCV register.</p> |

### 5.12.2.24 CFG\_TOCC Register

#### 1 CFG\_TOCC Register (Offset = 228h) [reset = FFFF0000h]

Timeout Counter Configuration

Configuration of timeout period, selection of timeout counter operation mode.

Return to [Summary Table](#)

**Table 5-2113. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8228h       |
| MCAN1         | 5261 8228h       |
| MCAN2         | 5262 8228h       |
| MCAN3         | 5263 8228h       |

**Figure 5-698. CFG\_TOCC Name Register**

|       |    |    |    |     |    |      |    |
|-------|----|----|----|-----|----|------|----|
| 31    | 30 | 29 | 28 | 27  | 26 | 25   | 24 |
| TOP   |    |    |    |     |    |      |    |
| R/W   |    |    |    |     |    |      |    |
| FFFFh |    |    |    |     |    |      |    |
| 23    | 22 | 21 | 20 | 19  | 18 | 17   | 16 |
| TOP   |    |    |    |     |    |      |    |
| R/W   |    |    |    |     |    |      |    |
| FFFFh |    |    |    |     |    |      |    |
| 15    | 14 | 13 | 12 | 11  | 10 | 9    | 8  |
| NU23  |    |    |    |     |    |      |    |
| R     |    |    |    |     |    |      |    |
| 0h    |    |    |    |     |    |      |    |
| 7     | 6  | 5  | 4  | 3   | 2  | 1    | 0  |
| NU23  |    |    |    | TOS |    | ETOC |    |
| R     |    |    |    | R/W |    | R/W  |    |
| 0h    |    |    |    | 0h  |    | 0h   |    |

**Table 5-2115. CFG\_TOCC Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | TOP   | R/W  | FFFFh | Timeout Period<br>Start value of the Timeout Counter (down-counter). Configures the Timeout Period.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 15:3  | NU23  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 2:1   | TOS   | R/W  | 0h    | Timeout Select<br>When operating in Continuous mode, a write to the MCAN_TOCV[15-0] TOC field presets the counter to the value configured by the MCAN_TOCC[31-16] TOP field and continues down-counting. When the Timeout Counter is controlled by one of the FIFOs, an empty FIFO presets the counter to the value configured by the MCAN_TOCC[31-16] TOP field. Down-counting is started when the first FIFO element is stored.<br>2'b00 = Continuous operation<br>2'b01 = Timeout controlled by Tx Event FIFO<br>2'b10 = Timeout controlled by Rx FIFO 0<br>2'b11 = Timeout controlled by Rx FIFO 1 |

**Table 5-2115. CFG\_TOCC Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                 |
|-----|-------|------|-------|---------------------------------------------------------------------------------------------|
| 0   | ETOC  | R/W  | 0h    | Enable Timeout Counter<br>1'b0 = Timeout Counter disabled<br>1'b1 = Timeout Counter enabled |

### 5.12.2.25 CFG\_TOCV Register

#### 1 CFG\_TOCV Register (Offset = 22Ch) [reset = FFFFh]

Timeout Counter Value. Read/reset timeout counter.

Return to [Summary Table](#)

**Table 5-2116. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 822Ch       |
| MCAN1         | 5261 822Ch       |
| MCAN2         | 5262 822Ch       |
| MCAN3         | 5263 822Ch       |

**Figure 5-699. CFG\_TOCV Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| NU24  |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| NU24  |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TOC   |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TOC   |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFFFh |    |    |    |    |    |    |    |

**Table 5-2118. CFG\_TOCV Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                          |
|-------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | NU24  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                             |
| 15:0  | TOC   | R/W  | FFFFh | Timeout Counter<br>The Timeout Counter is decremented in multiples of CAN bit times [1-16] depending on the configuration of the MCAN_TSCC[19-16] TCP field. When decremented to zero, interrupt flag MCAN_IR[18] TOO is set and the Timeout Counter is stopped. Start and reset/restart conditions are configured via the MCAN_TOCC[2-1] TOS field. |

### 5.12.2.26 CFG\_ECR Register

#### 1 CFG\_ECR Register (Offset = 240h) [reset = 0h]

Error Counter Register. State of Rx/Tx Error counter, CAN error logging.

Return to [Summary Table](#)

**Table 5-2119. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8240h       |
| MCAN1         | 5261 8240h       |
| MCAN2         | 5262 8240h       |
| MCAN3         | 5263 8240h       |

**Figure 5-700. CFG\_ECR Name Register**

|      |     |    |    |    |    |    |    |
|------|-----|----|----|----|----|----|----|
| 31   | 30  | 29 | 28 | 27 | 26 | 25 | 24 |
| NU25 |     |    |    |    |    |    |    |
| R    |     |    |    |    |    |    |    |
| 0h   |     |    |    |    |    |    |    |
| 23   | 22  | 21 | 20 | 19 | 18 | 17 | 16 |
| CEL  |     |    |    |    |    |    |    |
| R    |     |    |    |    |    |    |    |
| 0h   |     |    |    |    |    |    |    |
| 15   | 14  | 13 | 12 | 11 | 10 | 9  | 8  |
| RP   | REC |    |    |    |    |    |    |
| R    | R   |    |    |    |    |    |    |
| 0h   | 0h  |    |    |    |    |    |    |
| 7    | 6   | 5  | 4  | 3  | 2  | 1  | 0  |
| TEC  |     |    |    |    |    |    |    |
| R    |     |    |    |    |    |    |    |
| 0h   |     |    |    |    |    |    |    |

**Table 5-2121. CFG\_ECR Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                |
|-------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | NU25  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                   |
| 23:16 | CEL   | R    | 0h    | CAN Error Logging<br>The counter is incremented each time when a CAN protocol error causes the Transmit Error Counter or the Receive Error Counter to be incremented. It is reset by read access to the MCAN_ECR[23-16] CEL field. The counter stops at FFh; the next increment of the MCAN_ECR[7-0] TEC or MCAN_ECR[14-8] REC fields sets interrupt flag MCAN_IR[22] ELO. |
| 15    | RP    | R    | 0h    | Recieve Error Passive<br>1'b0 = The Receive Error Counter is below the error passive level of 128<br>1'b1 = The Receive Error Counter has reached the error passive level of 128                                                                                                                                                                                           |
| 14:8  | REC   | R    | 0h    | Recieve Error Counter<br>Actual state of the Receive Error Counter, values between 0 and 127.                                                                                                                                                                                                                                                                              |

**Table 5-2121. CFG\_ECR Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                     |
|-----|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | TEC   | R    | 0h    | <p>Transmit Error Counter</p> <p>Actual state of the Transmit Error Counter, values between 0 and 255.</p> <p>Note: When the MCAN_CCCR[2] ASM bit is set, the CAN protocol controller does not increment the MCAN_ECR[7-0] TEC and MCAN_ECR[14-8] REC fields when a CAN protocol error is detected, but the MCAN_ECR[23-16] CEL field is still incremented.</p> |

### 5.12.2.27 CFG\_PSR Register

#### 1 CFG\_PSR Register (Offset = 244h) [reset = 707h]

Protocol Status Register. CAN protocol controller status, transmitter delay compensation value.

Return to [Summary Table](#)

**Table 5-2122. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8244h       |
| MCAN1         | 5261 8244h       |
| MCAN2         | 5262 8244h       |
| MCAN3         | 5263 8244h       |

**Figure 5-701. CFG\_PSR Name Register**

|      |      |      |      |      |      |    |    |
|------|------|------|------|------|------|----|----|
| 31   | 30   | 29   | 28   | 27   | 26   | 25 | 24 |
| NU27 |      |      |      |      |      |    |    |
| R    |      |      |      |      |      |    |    |
| 0h   |      |      |      |      |      |    |    |
| 23   | 22   | 21   | 20   | 19   | 18   | 17 | 16 |
| NU27 | TDCV |      |      |      |      |    |    |
| R    | R    |      |      |      |      |    |    |
| 0h   | 0h   |      |      |      |      |    |    |
| 15   | 14   | 13   | 12   | 11   | 10   | 9  | 8  |
| NU26 | PXE  | RFDF | RBRS | RESI | DLEC |    |    |
| R    | R    | R    | R    | R    | R    |    |    |
| 0h   | 0h   | 0h   | 0h   | 0h   | 7h   |    |    |
| 7    | 6    | 5    | 4    | 3    | 2    | 1  | 0  |
| BO   | EW   | EP   | ACT  |      | LEC  |    |    |
| R    | R    | R    | R    |      | R    |    |    |
| 0h   | 0h   | 0h   | 0h   |      | 7h   |    |    |

**Table 5-2124. CFG\_PSR Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                     |
|-------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:23 | NU27  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                        |
| 22:16 | TDCV  | R    | 0h    | Transmitter Delay Compensation Value<br>Position of the secondary sample point, defined by the sum of the measured delay from the MCAN TX to MCAN RX pins and the MCAN_TDCR[14-8] TDCO field. The SSP position is, in the data phase, the number of mtq between the start of the transmitted bit and the secondary sample point. Valid values are 0 to 127 mtq. |
| 15    | NU26  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                        |
| 14    | PXE   | R    | 0h    | Protocol Exception Event<br>1'b0 = No protocol exception event occurred since last read access<br>1'b1 = Protocol exception event occurred                                                                                                                                                                                                                      |
| 13    | RFDF  | R    | 0h    | Received a CAN FD Message<br>This bit is set independent of acceptance filtering.<br>1'b0 = Since this bit was reset by the Host CPU, no CAN FD message has been received<br>1'b1 = Message in CAN FD format with FDF flag set has been received                                                                                                                |



**Table 5-2124. CFG\_PSR Register Field Descriptions (continued)**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                       |
|------|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12   | RBRB  | R    | 0h    | BRS flag of last received CAN FD Message<br>This bit is set together with the MCAN_PSR[13] RFDF bit, independent of acceptance filtering.<br>1'b0 = Last received CAN FD message did not have its BRS flag set<br>1'b1 = Last received CAN FD message had its BRS flag set                                                                                        |
| 11   | RESI  | R    | 0h    | ESI flag of last received CAN FD Message<br>This bit is set together with the MCAN_PSR[13] RFDF bit, independent of acceptance filtering.<br>1'b0 = Last received CAN FD message did not have its ESI flag set<br>1'b1 = Last received CAN FD message had its ESI flag set                                                                                        |
| 10:8 | DLEC  | R    | 7h    | Data Phase Last Error Code<br>Type of last error that occurred in the data phase of a CAN FD format frame with its BRS flag set.<br>Coding is the same as for the MCAN_PSR[2-0] LEC field. This field will be cleared to zero when a CAN FD format frame with its BRS flag set has been transferred (reception or transmission) without error.                    |
| 7    | BO    | R    | 0h    | Bus_Off status<br>1'b0 = The MCAN module is not Bus_Off<br>1'b1 = The MCAN module is in Bus_Off state                                                                                                                                                                                                                                                             |
| 6    | EW    | R    | 0h    | Warning Status<br>1'b0 = Both error counters are below the Error_Warning limit of 96<br>1'b1 = At least one of error counter has reached the Error_Warning limit of 96                                                                                                                                                                                            |
| 5    | EP    | R    | 0h    | Error Passive<br>1'b0 = The MCAN module is in the Error_Active state. It normally takes part in bus communication and sends an active error flag when an error has been detected<br>1'b1 = The MCAN module is in the Error_Passive state                                                                                                                          |
| 4:3  | ACT   | R    | 0h    | Activity<br>Monitors the module's CAN communication state.<br>2'b00 = Synchronizing - node is synchronizing on CAN communication<br>2'b01 = Idle - node is neither receiver nor transmitter<br>2'b10 = Receiver - node is operating as receiver<br>2'b11 = Transmitter - node is operating as transmitter<br>Note: ACT is set to 0 by a Protocol Exception Event. |

**Table 5-2124. CFG\_PSR Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-----|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2:0 | LEC   | R    | 7h    | <p>Last Error Code</p> <p>The MCAN_PSR[2-0] LEC field indicates the type of the last error to occur on the CAN bus. This field will be cleared to 0 when a message has been transferred (reception or transmission) without error.</p> <p>3'b000 = No Error: No error occurred since the MCAN_PSR[2-0] LEC field has been reset by successful reception or transmission.</p> <p>3'b001 = Stuff Error: More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed.</p> <p>3'b010 = Form Error: A fixed format part of a received frame has the wrong format.</p> <p>3'b011 = AckError: The message transmitted by the MCAN module was not acknowledged by another node.</p> <p>3'b100 = Bit1Error: During the transmission of a message (with the exception of the arbitration field), the device wanted to send a recessive level (bit of logical value '1'), but the monitored bus value was dominant.</p> <p>3'b101 = Bit0Error: During the transmission of a message (or acknowledge bit, or active error flag, or overload flag), the device wanted to send a dominant level (data or identifier bit logical value 0), but the monitored bus value was recessive. During Bus_Off recovery this status is set each time a sequence of 11 recessive bits has been monitored. This enables the Host CPU to monitor the proceeding of the Bus_Off recovery sequence (indicating the bus is not stuck at dominant or continuously disturbed).</p> <p>3'b110 = CRCErr: The CRC check sum of a received message was incorrect. The CRC of an incoming message does not match with the CRC calculated from the received data.</p> <p>3'b111 = NoChange: Any read access to the Protocol Status Register re-initializes the MCAN_PSR[2-0] LEC field to 3'b111. When the MCAN_PSR[2-0] LEC field shows the value 3'b111, no CAN bus event was detected since the last Host CPU read access to the Protocol Status Register.</p> <p>Note: When a frame in CAN FD format has reached the data phase with BRS flag set, the next CAN event (error or valid frame) will be shown in the MCAN_PSR[10-8] DLEC field instead of the MCAN_PSR[2-0] LEC field. An error in a fixed stuff bit of a CAN FD CRC sequence will be shown as a Form Error, not Stuff Error.</p> |

### 5.12.2.28 CFG\_TDCR Register

#### 1 CFG\_TDCR Register (Offset = 248h) [reset = 0h]

Transmitter Delay Compensation Register. Configuration of transmitter delay compensation offset and filter window length.

Return to [Summary Table](#)

**Table 5-2125. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8248h       |
| MCAN1         | 5261 8248h       |
| MCAN2         | 5262 8248h       |
| MCAN3         | 5263 8248h       |

**Figure 5-702. CFG\_TDCR Name Register**

|      |    |    |    |      |    |    |    |
|------|----|----|----|------|----|----|----|
| 31   | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
| NU29 |    |    |    |      |    |    |    |
| R    |    |    |    |      |    |    |    |
| 0h   |    |    |    |      |    |    |    |
| 23   | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| NU29 |    |    |    |      |    |    |    |
| R    |    |    |    |      |    |    |    |
| 0h   |    |    |    |      |    |    |    |
| 15   | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| NU29 |    |    |    | TDCO |    |    |    |
| R    |    |    |    | R/W  |    |    |    |
| 0h   |    |    |    | 0h   |    |    |    |
| 7    | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| NU28 |    |    |    | TDCF |    |    |    |
| R    |    |    |    | R/W  |    |    |    |
| 0h   |    |    |    | 0h   |    |    |    |

**Table 5-2127. CFG\_TDCR Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:15 | NU29  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                           |
| 14:8  | TDCO  | R/W  | 0h    | Transmitter Delay Compensation Offset<br>Offset value defining the distance between the measured delay from the MCAN RX and MCAN TX pins and the secondary sample point. Valid values are 0 to 127 mtq (0h7Fh).                                                                                                                                                                                    |
| 7     | NU28  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                           |
| 6:0   | TDCF  | R/W  | 0h    | Transmitter Delay Compensation Filter Window Length<br>Defines the minimum value for the SSP position, dominant edges on the MCAN RX pin that would result in an earlier SSP position are ignored for transmitter delay measurement. The feature is enabled when the MCAN_TDCR[6:0] TDCF field is configured to a value greater than the MCAN_TDCR[14:8] TDCO field. Valid values are 0 to 127 mtq |

### 5.12.2.29 CFG\_IR Register

#### 1 CFG\_IR Register (Offset = 250h) [reset = 0h]

Interrupt Register. The flags are set when one of the listed conditions is detected (edge-sensitive). The flags remain set until the Host CPU clears them. A flag is cleared by writing a 1h to the corresponding bit position. Writing a 0h has no effect.

Return to [Summary Table](#)

**Table 5-2128. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8250h       |
| MCAN1         | 5261 8250h       |
| MCAN2         | 5262 8250h       |
| MCAN3         | 5263 8250h       |

**Figure 5-703. CFG\_IR Name Register**

| 31   | 30   | 29   | 28   | 27   | 26   | 25   | 24   |
|------|------|------|------|------|------|------|------|
| NU30 |      | ARA  | PED  | PEA  | WDI  | BO   | EW   |
| R    |      | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |
| 0h   |      | 0h   | 0h   | 0h   | 0h   | 0h   | 0h   |
| 23   | 22   | 21   | 20   | 19   | 18   | 17   | 16   |
| EP   | ELO  | BEU  | BEC  | DRX  | TOO  | MRAF | TSW  |
| R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |
| 0h   | 0h   | 0h   | 0h   | 0h   | 0h   | 0h   | 0h   |
| 15   | 14   | 13   | 12   | 11   | 10   | 9    | 8    |
| TEFL | TEFF | TEFW | TEFN | TFE  | TCF  | TC   | HPM  |
| R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |
| 0h   | 0h   | 0h   | 0h   | 0h   | 0h   | 0h   | 0h   |
| 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
| RF1L | RF1F | RF1W | RF1N | RF0L | RF0F | RF0W | RF0N |
| R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  | R/W  |
| 0h   | 0h   | 0h   | 0h   | 0h   | 0h   | 0h   | 0h   |

**Table 5-2130. CFG\_IR Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                           |
|-------|-------|------|-------|---------------------------------------|
| 31:30 | NU30  | R    | 0h    | Reserved                              |
| 29    | ARA   | R/W  | 0h    | Access to Reserved Address            |
| 28    | PED   | R/W  | 0h    | Protocol Error in data Phase          |
| 27    | PEA   | R/W  | 0h    | Protocol Error in Arbitration Phase   |
| 26    | WDI   | R/W  | 0h    | Watchdog Interrupt                    |
| 25    | BO    | R/W  | 0h    | Bus_Off Status                        |
| 24    | EW    | R/W  | 0h    | Warning Status                        |
| 23    | EP    | R/W  | 0h    | Error Passive                         |
| 22    | ELO   | R/W  | 0h    | Error Logging Overflow                |
| 21    | BEU   | R/W  | 0h    | Bit Error Uncorrected                 |
| 20    | BEC   | R/W  | 0h    | Bit Error Corrected                   |
| 19    | DRX   | R/W  | 0h    | Message stored to Dedicated Rx Buffer |
| 18    | TOO   | R/W  | 0h    | Timeout Occurred                      |

**Table 5-2130. CFG\_IR Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-----|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 17  | MRAF  | R/W  | 0h    | <p>Message RAM Access Failure</p> <p>The flag is set, when the Rx Handler:</p> <ul style="list-style-type: none"> <li>i. has not completed acceptance filtering or storage of an accepted message until the arbitration field of the following message has been received. In this case acceptance filtering or message storage is aborted and the Rx Handler starts processing of the following message.</li> <li>ii. was not able to write a message to the Message RAM. In this case message storage is aborted.</li> </ul> <p>In both cases the FIFO put index is not updated respectively the New Data flag for a dedicated Rx Buffer is not set, a partly stored message is overwritten when the next message is stored to this location.</p> <p>The flag is also set when the Tx Handler was not able to read a message from the Message RAM in time. In this case message transmission is aborted. In case of a Tx Handler access failure the MCAN module is switched into Restricted Operation Mode (see Restricted Operation Mode). To leave Restricted Operation Mode, the Host CPU has to reset the MCAN_CCCR[2] ASM bit.</p> <p>1'b0 = No Message RAM access failure occurred<br/>1'b1 = Message RAM access failure occurred</p> |
| 16  | TSW   | R/W  | 0h    | Timestamp Wraparound                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 15  | TEFL  | R/W  | 0h    | Tx Event FIFO Element Lost                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 14  | TEFF  | R/W  | 0h    | Tx Event FIFO Full                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 13  | TEFW  | R/W  | 0h    | Tx Event FIFO Watermark Reached                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 12  | TEFN  | R/W  | 0h    | Tx Event FIFO New Entry                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 11  | TFE   | R/W  | 0h    | Tx FIFO Empty                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 10  | TCF   | R/W  | 0h    | Transmission Cancellation Finished                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 9   | TC    | R/W  | 0h    | Transmission Complete                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 8   | HPM   | R/W  | 0h    | High Priority Message                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 7   | RF1L  | R/W  | 0h    | Rx FIFO 1 Message Lost                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 6   | RF1F  | R/W  | 0h    | Rx FIFO 1 Full                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 5   | RF1W  | R/W  | 0h    | Rx FIFO 1 Watermark Reached                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 4   | RF1N  | R/W  | 0h    | Rx FIFO 1 New Message                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 3   | RF0L  | R/W  | 0h    | Rx FIFO 0 Message Lost                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 2   | RF0F  | R/W  | 0h    | Rx FIFO 0 Full                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 1   | RF0W  | R/W  | 0h    | Rx FIFO 0 Watermark Reached                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 0   | RF0N  | R/W  | 0h    | Rx FIFO 0 New Message                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

### 5.12.2.30 CFG\_IE Register

#### 1 CFG\_IE Register (Offset = 254h) [reset = 0h]

Interrupt Enable Register. The settings in the Interrupt Enable register determine which status changes in the MCAN\_IR register are signalled on an interrupt line.

Return to [Summary Table](#)

**Table 5-2131. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8254h       |
| MCAN1         | 5261 8254h       |
| MCAN2         | 5262 8254h       |
| MCAN3         | 5263 8254h       |

**Figure 5-704. CFG\_IE Name Register**

| 31    | 30    | 29    | 28    | 27    | 26    | 25    | 24    |
|-------|-------|-------|-------|-------|-------|-------|-------|
| NU31  |       | ARAE  | PEDE  | PEAE  | WDIE  | BOE   | EWE   |
| R     |       | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   |
| 0h    |       | 0h    | 0h    | 0h    | 0h    | 0h    | 0h    |
| 23    | 22    | 21    | 20    | 19    | 18    | 17    | 16    |
| EPE   | ELOE  | BEUE  | BECE  | DRX   | TOOE  | MRAFE | TSWE  |
| R/W   | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   |
| 0h    | 0h    | 0h    | 0h    | 0h    | 0h    | 0h    | 0h    |
| 15    | 14    | 13    | 12    | 11    | 10    | 9     | 8     |
| TEFLE | TEFFE | TEFWE | TEFNE | TFEE  | TCFE  | TCE   | HPME  |
| R/W   | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   |
| 0h    | 0h    | 0h    | 0h    | 0h    | 0h    | 0h    | 0h    |
| 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
| RF1LE | RF1FE | RF1WE | RF1NE | RF0LE | RF0FE | RF0WE | RF0NE |
| R/W   | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   |
| 0h    | 0h    | 0h    | 0h    | 0h    | 0h    | 0h    | 0h    |

**Table 5-2133. CFG\_IE Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                            |
|-------|-------|------|-------|--------------------------------------------------------|
| 31:30 | NU31  | R    | 0h    | Reserved                                               |
| 29    | ARAE  | R/W  | 0h    | Access to Reserve Address Interrupt Enable             |
| 28    | PEDE  | R/W  | 0h    | Protocol Error in Data Phase Interrupt Enable          |
| 27    | PEAE  | R/W  | 0h    | Protocol Error in Arbitration Phase Interrupt Enable   |
| 26    | WDIE  | R/W  | 0h    | Watchdog Interrupt Enable                              |
| 25    | BOE   | R/W  | 0h    | Bus_Off Status Interrupt Enable                        |
| 24    | EWE   | R/W  | 0h    | Warning Status Interrupt Enable                        |
| 23    | EPE   | R/W  | 0h    | Error Passive Interrupt Enable                         |
| 22    | ELOE  | R/W  | 0h    | Error Logging Overflow Interrupt Enable                |
| 21    | BEUE  | R/W  | 0h    | Bit Error Uncorrected Interrupt Enable                 |
| 20    | BECE  | R/W  | 0h    | Bit Error Corrected Interrupt Enable                   |
| 19    | DRX   | R/W  | 0h    | Message stored to Dedicated Rx Buffer Interrupt Enable |
| 18    | TOOE  | R/W  | 0h    | Timeout Occurred Interrupt Enable                      |
| 17    | MRAFE | R/W  | 0h    | Message RAM Access Failure Interrupt Enable            |

**Table 5-2133. CFG\_IE Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                         |
|-----|-------|------|-------|-----------------------------------------------------|
| 16  | TSWE  | R/W  | 0h    | Timestamp Wraparound Interrupt Enable               |
| 15  | TEFLE | R/W  | 0h    | Tx Event FIFO Event Lost Interrupt Enable           |
| 14  | TEFFE | R/W  | 0h    | Tx Event FIFO Full Interrupt Enable                 |
| 13  | TEFWE | R/W  | 0h    | Tx Event FIFO Watermark Reached Interrupt enable    |
| 12  | TEFNE | R/W  | 0h    | Tx Event FIFO New Entry Interrupt Enable            |
| 11  | TFEE  | R/W  | 0h    | Tx FIFO Empty Interrupt Enable                      |
| 10  | TCFE  | R/W  | 0h    | Transmission Cancellation Finished Interrupt Enable |
| 9   | TCE   | R/W  | 0h    | Transmission Completed Interrupt Enable             |
| 8   | HPME  | R/W  | 0h    | High Priority message Interrupt Enable              |
| 7   | RF1LE | R/W  | 0h    | Rx FIFO 1 Message Lost Interrupt Enable             |
| 6   | RF1FE | R/W  | 0h    | Rx FIFO 1 Full Interrupt Enable                     |
| 5   | RF1WE | R/W  | 0h    | Rx FIFO 1 Watermark Reached Interrupt Enable        |
| 4   | RF1NE | R/W  | 0h    | Rx FIFO 1 New Message Interrupt Enable              |
| 3   | RF0LE | R/W  | 0h    | Rx FIFO 0 Message Lost Interrupt Enable             |
| 2   | RF0FE | R/W  | 0h    | Rx FIFO 0 Full Interrupt Enable                     |
| 1   | RF0WE | R/W  | 0h    | Rx FIFO 0 Watermark Reached Interrupt Enable        |
| 0   | RF0NE | R/W  | 0h    | Rx FIFO 0 New Message Interrupt Enable              |

### 5.12.2.31 CFG\_ILS Register

#### 1 CFG\_ILS Register (Offset = 258h) [reset = 0h]

Interrupt line select. The Interrupt Line Select register assigns an interrupt generated by a specific interrupt flag from the MCAN\_IR register to one of the two module interrupt lines. For assigning interrupt to INT0, write 0 to corresponding bit field and for assigning interrupt to INT1, write 1 to corresponding bit field.

Return to [Summary Table](#)

**Table 5-2134. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8258h       |
| MCAN1         | 5261 8258h       |
| MCAN2         | 5262 8258h       |
| MCAN3         | 5263 8258h       |

**Figure 5-705. CFG\_ILS Name Register**

| 31    | 30    | 29    | 28    | 27    | 26    | 25    | 24    |
|-------|-------|-------|-------|-------|-------|-------|-------|
| NU32  |       | ARAL  | PEDL  | PEAL  | WDIL  | BOL   | EWL   |
| R     |       | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   |
| 0h    |       | 0h    | 0h    | 0h    | 0h    | 0h    | 0h    |
| 23    | 22    | 21    | 20    | 19    | 18    | 17    | 16    |
| EPL   | ELOL  | BEUL  | BECL  | DRXL  | TOOL  | MRAFL | TSWL  |
| R/W   | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   |
| 0h    | 0h    | 0h    | 0h    | 0h    | 0h    | 0h    | 0h    |
| 15    | 14    | 13    | 12    | 11    | 10    | 9     | 8     |
| TEFLL | TEFFL | TEFWL | TEFNL | TFEL  | TCFL  | TCL   | HPML  |
| R/W   | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   |
| 0h    | 0h    | 0h    | 0h    | 0h    | 0h    | 0h    | 0h    |
| 7     | 6     | 5     | 4     | 3     | 2     | 1     | 0     |
| RF1LL | RF1FL | RF1WL | RF1NL | RF0LL | RF0FL | RF0WL | RF0NL |
| R/W   | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   | R/W   |
| 0h    | 0h    | 0h    | 0h    | 0h    | 0h    | 0h    | 0h    |

**Table 5-2136. CFG\_ILS Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                          |
|-------|-------|------|-------|------------------------------------------------------|
| 31:30 | NU32  | R    | 0h    | Reserved                                             |
| 29    | ARAL  | R/W  | 0h    | Access to Reserve Address Interrupt Line             |
| 28    | PEDL  | R/W  | 0h    | Protocol Error in Data Phase Interrupt Line          |
| 27    | PEAL  | R/W  | 0h    | Protocol Error in Arbitration Phase Interrupt Line   |
| 26    | WDIL  | R/W  | 0h    | Watchdog Interrupt Line                              |
| 25    | BOL   | R/W  | 0h    | Bus_Off Status Interrupt Line                        |
| 24    | EWL   | R/W  | 0h    | Warning Status Interrupt Line                        |
| 23    | EPL   | R/W  | 0h    | Error Passive Interrupt Line                         |
| 22    | ELOL  | R/W  | 0h    | Error Logging Overflow Interrupt Line                |
| 21    | BEUL  | R/W  | 0h    | Bit Error Uncorrected Interrupt Line                 |
| 20    | BECL  | R/W  | 0h    | Bit Error Corrected Interrupt Line                   |
| 19    | DRXL  | R/W  | 0h    | Message stored to Dedicated Rx Buffer Interrupt Line |
| 18    | TOOL  | R/W  | 0h    | Timeout Occurred Interrupt Line                      |



**Table 5-2136. CFG\_ILS Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                       |
|-----|-------|------|-------|---------------------------------------------------|
| 17  | MRAFL | R/W  | 0h    | Message RAM Access Failure Interrupt Line         |
| 16  | TSWL  | R/W  | 0h    | Timestamp Wraparound Interrupt Line               |
| 15  | TEFLL | R/W  | 0h    | Tx Event FIFO Event Lost Interrupt Line           |
| 14  | TEFFL | R/W  | 0h    | Tx Event FIFO Full Interrupt Line                 |
| 13  | TEFWL | R/W  | 0h    | Tx Event FIFO Watermark Reached Interrupt Line    |
| 12  | TEFNL | R/W  | 0h    | Tx Event FIFO New Entry Interrupt Line            |
| 11  | TFEL  | R/W  | 0h    | Tx FIFO Empty Interrupt Line                      |
| 10  | TCFL  | R/W  | 0h    | Transmission Cancellation Finished Interrupt Line |
| 9   | TCL   | R/W  | 0h    | Transmission Completed Interrupt Line             |
| 8   | HPML  | R/W  | 0h    | High Priority message Interrupt Line              |
| 7   | RF1LL | R/W  | 0h    | Rx FIFO 1 Message Lost Interrupt Line             |
| 6   | RF1FL | R/W  | 0h    | Rx FIFO 1 Full Interrupt Line                     |
| 5   | RF1WL | R/W  | 0h    | Rx FIFO 1 Watermark Reached Interrupt Line        |
| 4   | RF1NL | R/W  | 0h    | Rx FIFO 1 New Message Interrupt Line              |
| 3   | RF0LL | R/W  | 0h    | Rx FIFO 0 Message Lost Interrupt Line             |
| 2   | RF0FL | R/W  | 0h    | Rx FIFO 0 Full Interrupt Line                     |
| 1   | RF0WL | R/W  | 0h    | Rx FIFO 0 Watermark Reached Interrupt Line        |
| 0   | RF0NL | R/W  | 0h    | Rx FIFO 0 New Message Interrupt Line              |

### 5.12.2.32 CFG\_ILE Register

#### 1 CFG\_ILE Register (Offset = 25Ch) [reset = 0h]

Interrupt line enable Register. Enable/Disable interrupt lines INT0/INT1.

Return to [Summary Table](#)

**Table 5-2137. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 825Ch       |
| MCAN1         | 5261 825Ch       |
| MCAN2         | 5262 825Ch       |
| MCAN3         | 5263 825Ch       |

**Figure 5-706. CFG\_ILE Name Register**

|      |    |    |    |    |    |       |       |
|------|----|----|----|----|----|-------|-------|
| 31   | 30 | 29 | 28 | 27 | 26 | 25    | 24    |
| NU33 |    |    |    |    |    |       |       |
| R    |    |    |    |    |    |       |       |
| 0h   |    |    |    |    |    |       |       |
| 23   | 22 | 21 | 20 | 19 | 18 | 17    | 16    |
| NU33 |    |    |    |    |    |       |       |
| R    |    |    |    |    |    |       |       |
| 0h   |    |    |    |    |    |       |       |
| 15   | 14 | 13 | 12 | 11 | 10 | 9     | 8     |
| NU33 |    |    |    |    |    |       |       |
| R    |    |    |    |    |    |       |       |
| 0h   |    |    |    |    |    |       |       |
| 7    | 6  | 5  | 4  | 3  | 2  | 1     | 0     |
| NU33 |    |    |    |    |    | EINT1 | EINT0 |
| R    |    |    |    |    |    | R/W   | R/W   |
| 0h   |    |    |    |    |    | 0h    | 0h    |

**Table 5-2139. CFG\_ILE Register Field Descriptions**

| Bit  | Field | Type | Reset | Description             |
|------|-------|------|-------|-------------------------|
| 31:2 | NU33  | R    | 0h    | Reserved                |
| 1    | EINT1 | R/W  | 0h    | Enable Interrupt Line 1 |
| 0    | EINT0 | R/W  | 0h    | Enable Interrupt Line 0 |

### 5.12.2.33 CFG\_GFC Register

#### 1 CFG\_GFC Register (Offset = 280h) [reset = 0h]

Global Filter Configuration. Handling of non-matching frames and remote frames. Global settings for Message ID filtering. The MCAN\_GFC register controls the filter path for standard and extended messages.

Return to [Summary Table](#)

**Table 5-2140. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8280h       |
| MCAN1         | 5261 8280h       |
| MCAN2         | 5262 8280h       |
| MCAN3         | 5263 8280h       |

**Figure 5-707. CFG\_GFC Name Register**

|      |      |    |      |    |      |      |    |
|------|------|----|------|----|------|------|----|
| 31   | 30   | 29 | 28   | 27 | 26   | 25   | 24 |
| NU34 |      |    |      |    |      |      |    |
| R    |      |    |      |    |      |      |    |
| 0h   |      |    |      |    |      |      |    |
| 23   | 22   | 21 | 20   | 19 | 18   | 17   | 16 |
| NU34 |      |    |      |    |      |      |    |
| R    |      |    |      |    |      |      |    |
| 0h   |      |    |      |    |      |      |    |
| 15   | 14   | 13 | 12   | 11 | 10   | 9    | 8  |
| NU34 |      |    |      |    |      |      |    |
| R    |      |    |      |    |      |      |    |
| 0h   |      |    |      |    |      |      |    |
| 7    | 6    | 5  | 4    | 3  | 2    | 1    | 0  |
| NU34 | ANFS |    | ANFE |    | RRFS | RRFE |    |
| R    | R/W  |    | R/W  |    | R/W  | R/W  |    |
| 0h   | 0h   |    | 0h   |    | 0h   | 0h   |    |

**Table 5-2142. CFG\_GFC Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                          |
|------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:6 | NU34  | R    | 0h    | Reserved                                                                                                                                                                                                                                             |
| 5:4  | ANFS  | R/W  | 0h    | Accept Non-matching Frames Standard<br>Defines how received messages with 11-bit IDs that do not match any element of the filter list are treated.<br>2'b00 = Accept in Rx FIFO 0<br>2'b01 = Accept in Rx FIFO 1<br>2'b10 = Reject<br>2'b11 = Reject |
| 3:2  | ANFE  | R/W  | 0h    | Accept Non-matching Frames Extended<br>Defines how received messages with 29-bit IDs that do not match any element of the filter list are treated.<br>2'b00 = Accept in Rx FIFO 0<br>2'b01 = Accept in Rx FIFO 1<br>2'b10 = Reject<br>2'b11 = Reject |
| 1    | RRFS  | R/W  | 0h    | Reject Remote Frames Standard<br>1'b0 = Filter remote frames with 11-bit standard IDs<br>1'b1 = Reject all remote frames with 11-bit standard IDs                                                                                                    |

**Table 5-2142. CFG\_GFC Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                       |
|-----|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | RRFE  | R/W  | 0h    | Reject Remote Frames Extended<br>1'b0 = Filter remote frames with 29-bit extended IDs<br>1'b1 = Reject all remote frames with 29-bit extended IDs |

### 5.12.2.34 CFG\_SIDFC Register

#### 1 CFG\_SIDFC Register (Offset = 284h) [reset = 0h]

Standard ID Filter Configuration. Settings for 11-bit standard Message ID filtering. The Standard ID Filter Configuration controls the filter path for standard messages.

Return to [Summary Table](#)

**Table 5-2143. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8284h       |
| MCAN1         | 5261 8284h       |
| MCAN2         | 5262 8284h       |
| MCAN3         | 5263 8284h       |

**Figure 5-708. CFG\_SIDFC Name Register**

|         |    |    |    |    |    |      |    |
|---------|----|----|----|----|----|------|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25   | 24 |
| NU36    |    |    |    |    |    |      |    |
| R       |    |    |    |    |    |      |    |
| 0h      |    |    |    |    |    |      |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17   | 16 |
| LSS_S   |    |    |    |    |    |      |    |
| R/W     |    |    |    |    |    |      |    |
| 0h      |    |    |    |    |    |      |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9    | 8  |
| FLSSA_S |    |    |    |    |    |      |    |
| R/W     |    |    |    |    |    |      |    |
| 0h      |    |    |    |    |    |      |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1    | 0  |
| FLSSA_S |    |    |    |    |    | NU35 |    |
| R/W     |    |    |    |    |    | R    |    |
| 0h      |    |    |    |    |    | 0h   |    |

**Table 5-2145. CFG\_SIDFC Register Field Descriptions**

| Bit   | Field   | Type | Reset | Description                                                                                                                                                                                          |
|-------|---------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | NU36    | R    | 0h    | Reserved                                                                                                                                                                                             |
| 23:16 | LSS_S   | R/W  | 0h    | List Size Standard<br>8'h00 = No standard Message ID filter<br>8'h01-8'h80 (1-128) = Number of standard Message ID filter elements<br>> 8'h80 (128) = Values greater than 128 are interpreted as 128 |
| 15:2  | FLSSA_S | R/W  | 0h    | Filter List Standard Start Address<br>Start address of standard Message ID filter list (32-bit word address, see Message RAM Configuration).                                                         |
| 1:0   | NU35    | R    | 0h    | Reserved                                                                                                                                                                                             |

### 5.12.2.35 CFG\_XIDFC Register

#### 1 CFG\_XIDFC Register (Offset = 288h) [reset = 0h]

Extended ID Filter Configuration. Settings for 29-bit extended Message ID filtering. The Extended ID Filter Configuration controls the filter path for standard messages.

Return to [Summary Table](#)

**Table 5-2146. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8288h       |
| MCAN1         | 5261 8288h       |
| MCAN2         | 5262 8288h       |
| MCAN3         | 5263 8288h       |

**Figure 5-709. CFG\_XIDFC Name Register**

|         |    |    |    |    |    |      |    |
|---------|----|----|----|----|----|------|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25   | 24 |
| NU38    |    |    |    |    |    |      |    |
| R       |    |    |    |    |    |      |    |
| 0h      |    |    |    |    |    |      |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17   | 16 |
| LSS_X   |    |    |    |    |    |      |    |
| R/W     |    |    |    |    |    |      |    |
| 0h      |    |    |    |    |    |      |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9    | 8  |
| FLSSA_X |    |    |    |    |    |      |    |
| R/W     |    |    |    |    |    |      |    |
| 0h      |    |    |    |    |    |      |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1    | 0  |
| FLSSA_X |    |    |    |    |    | NU37 |    |
| R/W     |    |    |    |    |    | R    |    |
| 0h      |    |    |    |    |    | 0h   |    |

**Table 5-2148. CFG\_XIDFC Register Field Descriptions**

| Bit   | Field   | Type | Reset | Description                                                                                                                                                                                      |
|-------|---------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | NU38    | R    | 0h    | Reserved                                                                                                                                                                                         |
| 23:16 | LSS_X   | R/W  | 0h    | List Size Extended<br>8'h00 = No extended Message ID filter<br>8'h01-8'h40 (1-64) = Number of extended Message ID filter elements<br>> 8'h40 (64) = Values greater than 64 are interpreted as 64 |
| 15:2  | FLSSA_X | R/W  | 0h    | Filter List Extended Start Address<br>Start address of extended Message ID filter list (32-bit word address, see Message RAM Configuration).                                                     |
| 1:0   | NU37    | R    | 0h    | Reserved                                                                                                                                                                                         |

### 5.12.2.36 CFG\_XIDAM Register

#### 1 CFG\_XIDAM Register (Offset = 290h) [reset = 1FFFFFFFh]

Extended ID and Mask.

Return to [Summary Table](#)

**Table 5-2149. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8290h       |
| MCAN1         | 5261 8290h       |
| MCAN2         | 5262 8290h       |
| MCAN3         | 5263 8290h       |

**Figure 5-710. CFG\_XIDAM Name Register**

|           |    |    |    |           |    |    |    |
|-----------|----|----|----|-----------|----|----|----|
| 31        | 30 | 29 | 28 | 27        | 26 | 25 | 24 |
| NU39      |    |    |    | EIDM      |    |    |    |
| R         |    |    |    | R/W       |    |    |    |
| 0h        |    |    |    | 1FFFFFFFh |    |    |    |
| 23        | 22 | 21 | 20 | 19        | 18 | 17 | 16 |
| EIDM      |    |    |    |           |    |    |    |
| R/W       |    |    |    |           |    |    |    |
| 1FFFFFFFh |    |    |    |           |    |    |    |
| 15        | 14 | 13 | 12 | 11        | 10 | 9  | 8  |
| EIDM      |    |    |    |           |    |    |    |
| R/W       |    |    |    |           |    |    |    |
| 1FFFFFFFh |    |    |    |           |    |    |    |
| 7         | 6  | 5  | 4  | 3         | 2  | 1  | 0  |
| EIDM      |    |    |    |           |    |    |    |
| R/W       |    |    |    |           |    |    |    |
| 1FFFFFFFh |    |    |    |           |    |    |    |

**Table 5-2151. CFG\_XIDAM Register Field Descriptions**

| Bit   | Field | Type | Reset     | Description                                                                                                                                                                                                                                                      |
|-------|-------|------|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | NU39  | R    | 0h        | Reserved                                                                                                                                                                                                                                                         |
| 28:0  | EIDM  | R/W  | 1FFFFFFFh | Extended ID Mask.<br>For acceptance filtering of extended frames the Extended ID AND Mask is ANDed with the Message ID of a received frame. Intended for masking of 29-bit IDs in SAE J1939. With the reset value of all bits set to one the mask is not active. |

### 5.12.2.37 CFG\_HPMS Register

#### 1 CFG\_HPMS Register (Offset = 294h) [reset = 0h]

High Priority Message Status. Status monitoring of incoming high priority messages. This register is updated every time a Message ID filter element configured to generate a priority event matches. This can be used to monitor the status of incoming high priority messages and to enable fast access to these messages.

Return to [Summary Table](#)

**Table 5-2152. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8294h       |
| MCAN1         | 5261 8294h       |
| MCAN2         | 5262 8294h       |
| MCAN3         | 5263 8294h       |

**Figure 5-711. CFG\_HPMS Name Register**

|      |      |      |    |    |    |    |    |
|------|------|------|----|----|----|----|----|
| 31   | 30   | 29   | 28 | 27 | 26 | 25 | 24 |
| NU40 |      |      |    |    |    |    |    |
| R    |      |      |    |    |    |    |    |
| 0h   |      |      |    |    |    |    |    |
| 23   | 22   | 21   | 20 | 19 | 18 | 17 | 16 |
| NU40 |      |      |    |    |    |    |    |
| R    |      |      |    |    |    |    |    |
| 0h   |      |      |    |    |    |    |    |
| 15   | 14   | 13   | 12 | 11 | 10 | 9  | 8  |
| FLST | FIDX |      |    |    |    |    |    |
| R    | R    |      |    |    |    |    |    |
| 0h   | 0h   |      |    |    |    |    |    |
| 7    | 6    | 5    | 4  | 3  | 2  | 1  | 0  |
| MSI  |      | BIDX |    |    |    |    |    |
| R    |      | R    |    |    |    |    |    |
| 0h   |      | 0h   |    |    |    |    |    |

**Table 5-2154. CFG\_HPMS Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                |
|-------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | NU40  | R    | 0h    | Reserved                                                                                                                                                   |
| 15    | FLST  | R    | 0h    | Filter List<br>Indicates the filter list of the matching filter element.<br>1'b0 = Standard Filter List<br>1'b1 = Extended Filter List                     |
| 14:8  | FIDX  | R    | 0h    | Filter Index<br>Index of matching filter element. Range is 0 to MCAN_SIDFC[23-16] LSS - 1 respectively MCAN_XIDFC[22-16] LSE - 1.                          |
| 7:6   | MSI   | R    | 0h    | Message Storage Indicator<br>2'b00 = No FIFO selected<br>2'b01 = FIFO message lost<br>2'b10 = Message stored in FIFO 0<br>2'b11 = Message stored in FIFO 1 |
| 5:0   | BIDX  | R    | 0h    | Buffer Index<br>Index of Rx FIFO element to which the message was stored. Only valid when the MCAN_HPMS[7-6] MSI = 1.                                      |



### 5.12.2.38 CFG\_NDAT1 Register

#### 1 CFG\_NDAT1 Register (Offset = 298h) [reset = 0h]

New Data 1 register. NewData flags of dedicated Rx buffers 0-31. The register holds the New Data flags of Rx Buffers 0 to 31. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host CPU clears them. Aflag is cleared by writing a 1h to the corresponding bit position. Writing a 0h has no effect. A hard reset will clear the register .

Return to [Summary Table](#)

**Table 5-2155. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 8298h       |
| MCAN1         | 5261 8298h       |
| MCAN2         | 5262 8298h       |
| MCAN3         | 5263 8298h       |

**Figure 5-712. CFG\_NDAT1 Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ND0_31 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ND0_31 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ND0_31 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ND0_31 |    |    |    |    |    |    |    |
| R/W    |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-2157. CFG\_NDAT1 Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description   |
|------|--------|------|-------|---------------|
| 31:0 | ND0_31 | R/W  | 0h    | New Data 31-0 |

### 5.12.2.39 CFG\_NDAT2 Register

#### 1 CFG\_NDAT2 Register (Offset = 29Ch) [reset = 0h]

New Data 2 register. NewData flags of dedicated Rx buffers 32-63. The register holds the New Data flags of Rx Buffers 32 to 63. The flags are set when the respective Rx Buffer has been updated from a received frame. The flags remain set until the Host CPU clears them. A flag is cleared by writing a 1h to the corresponding bit position. Writing a 0h has no effect. A hard reset will clear the register .

Return to [Summary Table](#)

**Table 5-2158. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 829Ch       |
| MCAN1         | 5261 829Ch       |
| MCAN2         | 5262 829Ch       |
| MCAN3         | 5263 829Ch       |

**Figure 5-713. CFG\_NDAT2 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ND32_63 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ND32_63 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ND32_63 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ND32_63 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-2160. CFG\_NDAT2 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description    |
|------|---------|------|-------|----------------|
| 31:0 | ND32_63 | R/W  | 0h    | New Data 63-32 |

### 5.12.2.40 CFG\_RXF0C Register

#### 1 CFG\_RXF0C Register (Offset = 2A0h) [reset = 0h]

Rx FIFO 0 Configuration register. FIFO 0 operation mode, watermark, size and start address.

Return to [Summary Table](#)

**Table 5-2161. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 82A0h       |
| MCAN1         | 5261 82A0h       |
| MCAN2         | 5262 82A0h       |
| MCAN3         | 5263 82A0h       |

**Figure 5-714. CFG\_RXF0C Name Register**

|        |    |    |      |      |    |    |      |
|--------|----|----|------|------|----|----|------|
| 31     | 30 | 29 | 28   | 27   | 26 | 25 | 24   |
| F0OM   |    |    |      | F0WM |    |    |      |
| R/W    |    |    |      | R/W  |    |    |      |
| 0h     |    |    |      | 0h   |    |    |      |
| 23     | 22 | 21 | 20   | 19   | 18 | 17 | 16   |
| NU42_1 |    |    |      | F0S  |    |    |      |
| R      |    |    |      | R/W  |    |    |      |
| 0h     |    |    |      | 0h   |    |    |      |
| 15     | 14 | 13 | 12   | 11   | 10 | 9  | 8    |
| NU42   |    |    |      | F0SA |    |    |      |
| R      |    |    |      | R/W  |    |    |      |
| 0h     |    |    |      | 0h   |    |    |      |
| 7      | 6  | 5  | 4    | 3    | 2  | 1  | 0    |
|        |    |    | F0SA |      |    |    | NU41 |
|        |    |    | R/W  |      |    |    | R    |
|        |    |    | 0h   |      |    |    | 0h   |

**Table 5-2163. CFG\_RXF0C Register Field Descriptions**

| Bit   | Field  | Type | Reset | Description                                                                                                                                                                                                                           |
|-------|--------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | F0OM   | R/W  | 0h    | Rx FIFO 0 Operation Mode<br>FIFO 0 can be operated in blocking or in overwrite mode (see Rx FIFOs).<br>1'b0 = FIFO 0 blocking mode<br>1'b1 = FIFO 0 overwrite mode                                                                    |
| 30:24 | F0WM   | R/W  | 0h    | Rx FIFO 0 Watermark<br>7'h00 = Watermark interrupt disabled<br>7'h01-7'h40 (1-64) = Level for Rx FIFO 0 watermark interrupt (MCAN_IR[1] RF0W)<br>> 7'h40 (64) = Watermark interrupt disabled                                          |
| 23    | NU42_1 | R    | 0h    | Reserved                                                                                                                                                                                                                              |
| 22:16 | F0S    | R/W  | 0h    | Rx FIFO 0 Size<br>7'h00 = No Rx FIFO 0<br>7'h01-7'h40 (1-64) = Number of Rx FIFO 0 elements<br>> 7'h40 (64) = Values greater than 64 are interpreted as 64<br>The Rx FIFO 0 elements are indexed from 0 to MCAN_RXF0C[22-16] F0S - 1. |
| 15    | NU42   | R    | 0h    | Reserved                                                                                                                                                                                                                              |

**Table 5-2163. CFG\_RXF0C Register Field Descriptions (continued)**

| Bit  | Field | Type | Reset | Description                                                                                                                |
|------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------|
| 14:2 | F0SA  | R/W  | 0h    | Rx FIFO 0 Start Address<br>Start address of Rx FIFO 0 in Message RAM (32-bit word address, see Message RAM Configuration). |
| 1:0  | NU41  | R    | 0h    | Reserved                                                                                                                   |

### 5.12.2.41 CFG\_RXF0S Register

#### 1 CFG\_RXF0S Register (Offset = 2A4h) [reset = 0h]

Rx FIFO 0 Status register. FIFO 0 message lost/full indication, put index, get index and fill level.

Return to [Summary Table](#)

**Table 5-2164. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 82A4h       |
| MCAN1         | 5261 82A4h       |
| MCAN2         | 5262 82A4h       |
| MCAN3         | 5263 82A4h       |

**Figure 5-715. CFG\_RXF0S Name Register**

|      |    |      |    |    |    |      |     |
|------|----|------|----|----|----|------|-----|
| 31   | 30 | 29   | 28 | 27 | 26 | 25   | 24  |
| NU46 |    |      |    |    |    | RF0L | F0F |
| R    |    |      |    |    |    | R    | R   |
| 0h   |    |      |    |    |    | 0h   | 0h  |
| 23   | 22 | 21   | 20 | 19 | 18 | 17   | 16  |
| NU45 |    | F0PI |    |    |    |      |     |
| R    |    | R    |    |    |    |      |     |
| 0h   |    | 0h   |    |    |    |      |     |
| 15   | 14 | 13   | 12 | 11 | 10 | 9    | 8   |
| NU44 |    | F0GI |    |    |    |      |     |
| R    |    | R    |    |    |    |      |     |
| 0h   |    | 0h   |    |    |    |      |     |
| 7    | 6  | 5    | 4  | 3  | 2  | 1    | 0   |
| NU43 |    | F0FL |    |    |    |      |     |
| R    |    | R    |    |    |    |      |     |
| 0h   |    | 0h   |    |    |    |      |     |

**Table 5-2166. CFG\_RXF0S Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                   |
|-------|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:26 | NU46  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                      |
| 25    | RF0L  | R    | 0h    | Rx FIFO 0 Message Lost<br>This bit is a copy of interrupt flag MCAN_IR[3] RF0L. When the MCAN_IR[3] RF0L flag is reset, this bit is also reset.<br>1'b0 = No Rx FIFO 0 message lost 1'b1 = Rx FIFO 0 message lost, also set after write attempt to Rx FIFO 0 of size zero<br>Note: OverWriting the oldest message when the MCAN_RXF0C[31] F0OM = 1'b1 will not set this flag. |
| 24    | F0F   | R    | 0h    | Rx FIFO 0 Full                                                                                                                                                                                                                                                                                                                                                                |
| 23:22 | NU45  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                      |
| 21:16 | F0PI  | R    | 0h    | Rx FIFO 0 Put Index                                                                                                                                                                                                                                                                                                                                                           |
| 15:14 | NU44  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                      |
| 13:8  | F0GI  | R    | 0h    | Rx FIFO 0 Get Index                                                                                                                                                                                                                                                                                                                                                           |
| 7     | NU43  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                      |
| 6:0   | F0FL  | R    | 0h    | Rx FIFO 0 Fill Level                                                                                                                                                                                                                                                                                                                                                          |

### 5.12.2.42 CFG\_RXF0A Register

#### 1 CFG\_RXF0A Register (Offset = 2A8h) [reset = 0h]

Rx FIFO 0 Acknowledge register. FIFO 0 acknowledge last index of read buffers, updates get index and fill level.

Return to [Summary Table](#)

**Table 5-2167. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 82A8h       |
| MCAN1         | 5261 82A8h       |
| MCAN2         | 5262 82A8h       |
| MCAN3         | 5263 82A8h       |

**Figure 5-716. CFG\_RXF0A Name Register**

|      |    |    |    |      |    |    |    |
|------|----|----|----|------|----|----|----|
| 31   | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
| NU47 |    |    |    |      |    |    |    |
| R    |    |    |    |      |    |    |    |
| 0h   |    |    |    |      |    |    |    |
| 23   | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| NU47 |    |    |    |      |    |    |    |
| R    |    |    |    |      |    |    |    |
| 0h   |    |    |    |      |    |    |    |
| 15   | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| NU47 |    |    |    |      |    |    |    |
| R    |    |    |    |      |    |    |    |
| 0h   |    |    |    |      |    |    |    |
| 7    | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| NU47 |    |    |    | F0AI |    |    |    |
| R    |    |    |    | R/W  |    |    |    |
| 0h   |    |    |    | 0h   |    |    |    |

**Table 5-2169. CFG\_RXF0A Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                    |
|------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:6 | NU47  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                       |
| 5:0  | F0AI  | R/W  | 0h    | Rx FIFO 0 Acknowledge Index<br>After the Host CPU has read a message or a sequence of messages from Rx FIFO 0 it has to write the buffer index of the last element read from Rx FIFO 0 to the MCAN_RXF0A[5-0] F0AI field. This will set the Rx FIFO 0 Get Index MCAN_RXF0S[13-8] F0GI field to the MCAN_RXF0A[5-0] F0AI field + 1 and update the FIFO 0 Fill Level MCAN_RXF0S[6-0] F0FL field. |

### 5.12.2.43 CFG\_RXBC Register

#### 1 CFG\_RXBC Register (Offset = 2ACh) [reset = 0h]

Rx Buffer Configuration register. Start address of Rx buffer section.

Return to [Summary Table](#)

**Table 5-2170. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 82ACh       |
| MCAN1         | 5261 82ACh       |
| MCAN2         | 5262 82ACh       |
| MCAN3         | 5263 82ACh       |

**Figure 5-717. CFG\_RXBC Name Register**

|      |    |    |    |    |    |      |    |
|------|----|----|----|----|----|------|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25   | 24 |
| NU49 |    |    |    |    |    |      |    |
| R    |    |    |    |    |    |      |    |
| 0h   |    |    |    |    |    |      |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17   | 16 |
| NU49 |    |    |    |    |    |      |    |
| R    |    |    |    |    |    |      |    |
| 0h   |    |    |    |    |    |      |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9    | 8  |
| RBSA |    |    |    |    |    |      |    |
| R/W  |    |    |    |    |    |      |    |
| 0h   |    |    |    |    |    |      |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1    | 0  |
| RBSA |    |    |    |    |    | NU48 |    |
| R/W  |    |    |    |    |    | R    |    |
| 0h   |    |    |    |    |    | 0h   |    |

**Table 5-2172. CFG\_RXBC Register Field Descriptions**

| Bit   | Field | Type | Reset | Description             |
|-------|-------|------|-------|-------------------------|
| 31:16 | NU49  | R    | 0h    | Reserved                |
| 15:2  | RBSA  | R/W  | 0h    | Rx Buffer Start Address |
| 1:0   | NU48  | R    | 0h    | Reserved                |

### 5.12.2.44 CFG\_RXF1C Register

#### 1 CFG\_RXF1C Register (Offset = 2B0h) [reset = 0h]

Rx FIFO 1 Configuration register. FIFO 1 operation mode, watermark, size and start address.

Return to [Summary Table](#)

**Table 5-2173. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 82B0h       |
| MCAN1         | 5261 82B0h       |
| MCAN2         | 5262 82B0h       |
| MCAN3         | 5263 82B0h       |

**Figure 5-718. CFG\_RXF1C Name Register**

|        |    |    |      |      |    |    |       |
|--------|----|----|------|------|----|----|-------|
| 31     | 30 | 29 | 28   | 27   | 26 | 25 | 24    |
| F1OM   |    |    |      | F1WM |    |    |       |
| R/W    |    |    |      | R/W  |    |    |       |
| 0h     |    |    |      | 0h   |    |    |       |
| 23     | 22 | 21 | 20   | 19   | 18 | 17 | 16    |
| NU50_1 |    |    |      | F1S  |    |    |       |
| R      |    |    |      | R/W  |    |    |       |
| 0h     |    |    |      | 0h   |    |    |       |
| 15     | 14 | 13 | 12   | 11   | 10 | 9  | 8     |
| NU50   |    |    |      | F1SA |    |    |       |
| R      |    |    |      | R/W  |    |    |       |
| 0h     |    |    |      | 0h   |    |    |       |
| 7      | 6  | 5  | 4    | 3    | 2  | 1  | 0     |
|        |    |    | F1SA |      |    |    | NU499 |
|        |    |    | R/W  |      |    |    | R     |
|        |    |    | 0h   |      |    |    | 0h    |

**Table 5-2175. CFG\_RXF1C Register Field Descriptions**

| Bit   | Field  | Type | Reset | Description                                                                                                                                                                                                                           |
|-------|--------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | F1OM   | R/W  | 0h    | Rx FIFO 1 Operation Mode<br>FIFO 1 can be operated in blocking or in overwrite mode (see Rx FIFOs).<br>1'b0 = FIFO 1 blocking mode<br>1'b1 = FIFO 1 overwrite mode                                                                    |
| 30:24 | F1WM   | R/W  | 0h    | Rx FIFO 1 Watermark<br>7'h00 = Watermark interrupt disabled<br>7'h01-7'h40 (1-64) = Level for Rx FIFO 1 watermark interrupt (MCAN_IR[5] RF1W)<br>> 7'h40 (64) = Watermark interrupt disabled                                          |
| 23    | NU50_1 | R    | 0h    | Reserved                                                                                                                                                                                                                              |
| 22:16 | F1S    | R/W  | 0h    | Rx FIFO 1 Size<br>7'h00 = No Rx FIFO 1<br>7'h01-7'h40 (1-64) = Number of Rx FIFO 1 elements<br>> 7'h40 (64) = Values greater than 64 are interpreted as 64<br>The Rx FIFO 1 elements are indexed from 0 to MCAN_RXF1C[22-16] F1S - 1. |
| 15    | NU50   | R    | 0h    | Reserved                                                                                                                                                                                                                              |



**Table 5-2175. CFG\_RXF1C Register Field Descriptions (continued)**

| Bit  | Field | Type | Reset | Description                                                                                                             |
|------|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------|
| 14:2 | F1SA  | R/W  | 0h    | Rx FIFO 1 Start Address Start address of Rx FIFO 1 in Message RAM (32-bit word address, see Message RAM Configuration). |
| 1:0  | NU499 | R    | 0h    | Reserved                                                                                                                |

### 5.12.2.45 CFG\_RXF1S Register

#### 1 CFG\_RXF1S Register (Offset = 2B4h) [reset = 0h]

Rx FIFO 1 Status register. FIFO 1 message lost/full indication, put index, get index and fill level.

Return to [Summary Table](#)

**Table 5-2176. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 82B4h       |
| MCAN1         | 5261 82B4h       |
| MCAN2         | 5262 82B4h       |
| MCAN3         | 5263 82B4h       |

**Figure 5-719. CFG\_RXF1S Name Register**

|      |    |      |    |    |    |      |     |
|------|----|------|----|----|----|------|-----|
| 31   | 30 | 29   | 28 | 27 | 26 | 25   | 24  |
| NU54 |    |      |    |    |    | RF1L | F1F |
| R    |    |      |    |    |    | R    | R   |
| 0h   |    |      |    |    |    | 0h   | 0h  |
| 23   | 22 | 21   | 20 | 19 | 18 | 17   | 16  |
| NU53 |    | F1PI |    |    |    |      |     |
| R    |    | R    |    |    |    |      |     |
| 0h   |    | 0h   |    |    |    |      |     |
| 15   | 14 | 13   | 12 | 11 | 10 | 9    | 8   |
| NU52 |    | F1GI |    |    |    |      |     |
| R    |    | R    |    |    |    |      |     |
| 0h   |    | 0h   |    |    |    |      |     |
| 7    | 6  | 5    | 4  | 3  | 2  | 1    | 0   |
| NU51 |    | F1FL |    |    |    |      |     |
| R    |    | R    |    |    |    |      |     |
| 0h   |    | 0h   |    |    |    |      |     |

**Table 5-2178. CFG\_RXF1S Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                      |
|-------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:26 | NU54  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                         |
| 25    | RF1L  | R    | 0h    | Rx FIFO 1 Message Lost<br>This bit is a copy of interrupt flag MCAN_IR[7] RF1L. When the MCAN_IR[7] RF1L flag is reset, this bit is also reset.<br>1'b0 = No Rx FIFO 1 message lost<br>1'b1 = Rx FIFO 1 message lost, also set after write attempt to Rx FIFO 1 of size zero<br>Note: OverWriting the oldest message when the MCAN_RXF1C[31] F1OM = 1'b1 will not set this flag. |
| 24    | F1F   | R    | 0h    | Rx FIFO 1 Full                                                                                                                                                                                                                                                                                                                                                                   |
| 23:22 | NU53  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                         |
| 21:16 | F1PI  | R    | 0h    | Rx FIFO 1 Put Index                                                                                                                                                                                                                                                                                                                                                              |
| 15:14 | NU52  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                         |
| 13:8  | F1GI  | R    | 0h    | Rx FIFO 1 Get Index                                                                                                                                                                                                                                                                                                                                                              |
| 7     | NU51  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                         |
| 6:0   | F1FL  | R    | 0h    | Rx FIFO 1 Fill Level                                                                                                                                                                                                                                                                                                                                                             |

### 5.12.2.46 CFG\_RXF1A Register

#### 1 CFG\_RXF1A Register (Offset = 2B8h) [reset = 0h]

Rx FIFO 1 Acknowledge register. FIFO 1 acknowledge last index of read buffers, updates get index and fill level.

Return to [Summary Table](#)

**Table 5-2179. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 82B8h       |
| MCAN1         | 5261 82B8h       |
| MCAN2         | 5262 82B8h       |
| MCAN3         | 5263 82B8h       |

**Figure 5-720. CFG\_RXF1A Name Register**

|      |    |      |    |    |    |    |    |
|------|----|------|----|----|----|----|----|
| 31   | 30 | 29   | 28 | 27 | 26 | 25 | 24 |
| NU55 |    |      |    |    |    |    |    |
| R    |    |      |    |    |    |    |    |
| 0h   |    |      |    |    |    |    |    |
| 23   | 22 | 21   | 20 | 19 | 18 | 17 | 16 |
| NU55 |    |      |    |    |    |    |    |
| R    |    |      |    |    |    |    |    |
| 0h   |    |      |    |    |    |    |    |
| 15   | 14 | 13   | 12 | 11 | 10 | 9  | 8  |
| NU55 |    |      |    |    |    |    |    |
| R    |    |      |    |    |    |    |    |
| 0h   |    |      |    |    |    |    |    |
| 7    | 6  | 5    | 4  | 3  | 2  | 1  | 0  |
| NU55 |    | F1AI |    |    |    |    |    |
| R    |    | R/W  |    |    |    |    |    |
| 0h   |    | 0h   |    |    |    |    |    |

**Table 5-2181. CFG\_RXF1A Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                    |
|------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:6 | NU55  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                       |
| 5:0  | F1AI  | R/W  | 0h    | Rx FIFO 1 Acknowledge Index<br>After the Host CPU has read a message or a sequence of messages from Rx FIFO 1 it has to write the buffer index of the last element read from Rx FIFO 1 to the MCAN_RXF1A[5-0] F1AI field. This will set the Rx FIFO 1 Get Index MCAN_RXF1S[13-8] F1GI field to the MCAN_RXF1A[5-0] F1AI field + 1 and update the FIFO 1 Fill Level MCAN_RXF1S[6-0] F1FL field. |

### 5.12.2.47 CFG\_RXESC Register

#### 1 CFG\_RXESC Register (Offset = 2BCh) [reset = 0h]

Rx Buffer/FIFO Element Size Configuration register. Configure data field size for storage of accepted frames.

Return to [Summary Table](#)

**Table 5-2182. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 82BCh       |
| MCAN1         | 5261 82BCh       |
| MCAN2         | 5262 82BCh       |
| MCAN3         | 5263 82BCh       |

**Figure 5-721. CFG\_RXESC Name Register**

|      |      |    |    |      |      |    |    |
|------|------|----|----|------|------|----|----|
| 31   | 30   | 29 | 28 | 27   | 26   | 25 | 24 |
| NU58 |      |    |    |      |      |    |    |
| R    |      |    |    |      |      |    |    |
| 0h   |      |    |    |      |      |    |    |
| 23   | 22   | 21 | 20 | 19   | 18   | 17 | 16 |
| NU58 |      |    |    |      |      |    |    |
| R    |      |    |    |      |      |    |    |
| 0h   |      |    |    |      |      |    |    |
| 15   | 14   | 13 | 12 | 11   | 10   | 9  | 8  |
| NU58 |      |    |    | RBDS |      |    |    |
| R    |      |    |    | R/W  |      |    |    |
| 0h   |      |    |    | 0h   |      |    |    |
| 7    | 6    | 5  | 4  | 3    | 2    | 1  | 0  |
| NU57 | F1DS |    |    | NU56 | F0DS |    |    |
| R    | R/W  |    |    | R    | R/W  |    |    |
| 0h   | 0h   |    |    | 0h   | 0h   |    |    |

**Table 5-2184. CFG\_RXESC Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                      |
|-------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:11 | NU58  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                         |
| 10:8  | RBDS  | R/W  | 0h    | Rx Buffer data Field Size<br>3'b000 = 8 byte data field<br>3'b001 = 12 byte data field<br>3'b010 = 16 byte data field<br>3'b011 = 20 byte data field<br>3'b100 = 24 byte data field<br>3'b101 = 32 byte data field<br>3'b110 = 48 byte data field<br>3'b111 = 64 byte data field |
| 7     | NU57  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                         |
| 6:4   | F1DS  | R/W  | 0h    | Rx FIFO 1 Data Field Size<br>3'b000 = 8 byte data field<br>3'b001 = 12 byte data field<br>3'b010 = 16 byte data field<br>3'b011 = 20 byte data field<br>3'b100 = 24 byte data field<br>3'b101 = 32 byte data field<br>3'b110 = 48 byte data field<br>3'b111 = 64 byte data field |

**Table 5-2184. CFG\_RXESC Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-----|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3   | NU56  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 2:0 | F0DS  | R/W  | 0h    | <p>Rx FIFO 0 Data Field Size</p> <p>3'b000 = 8 byte data field</p> <p>3'b001 = 12 byte data field</p> <p>3'b010 = 16 byte data field</p> <p>3'b011 = 20 byte data field</p> <p>3'b100 = 24 byte data field</p> <p>3'b101 = 32 byte data field</p> <p>3'b110 = 48 byte data field</p> <p>3'b111 = 64 byte data field</p> <p>Note: In case the data field size of an accepted CAN frame exceeds the data field size configured for the matching Rx Buffer or Rx FIFO, only the number of bytes as configured by the MCAN_RXESC register are stored to the Rx Buffer respectively Rx FIFO element. The rest of the frame's data field is ignored.</p> |

### 5.12.2.48 CFG\_TXBC Register

#### 1 CFG\_TXBC Register (Offset = 2C0h) [reset = 0h]

Tx Buffer Configuration register. Configure Tx FIFO/Queue mode, Tx FIFO/Queue size, number of dedicated Tx buffers, Tx buffer start address.

Return to [Summary Table](#)

**Table 5-2185. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 82C0h       |
| MCAN1         | 5261 82C0h       |
| MCAN2         | 5262 82C0h       |
| MCAN3         | 5263 82C0h       |

**Figure 5-722. CFG\_TXBC Name Register**

|      |      |      |    |    |    |      |    |
|------|------|------|----|----|----|------|----|
| 31   | 30   | 29   | 28 | 27 | 26 | 25   | 24 |
| NU61 | TFQM | TFQS |    |    |    |      |    |
| R    | R    | R    |    |    |    |      |    |
| 0h   | 0h   | 0h   |    |    |    |      |    |
| 23   | 22   | 21   | 20 | 19 | 18 | 17   | 16 |
| NU60 | NDTB |      |    |    |    |      |    |
| R    | R    |      |    |    |    |      |    |
| 0h   | 0h   |      |    |    |    |      |    |
| 15   | 14   | 13   | 12 | 11 | 10 | 9    | 8  |
| TBSA |      |      |    |    |    |      |    |
| R    |      |      |    |    |    |      |    |
| 0h   |      |      |    |    |    |      |    |
| 7    | 6    | 5    | 4  | 3  | 2  | 1    | 0  |
| TBSA |      |      |    |    |    | NU59 |    |
| R    |      |      |    |    |    | R    |    |
| 0h   |      |      |    |    |    | 0h   |    |

**Table 5-2187. CFG\_TXBC Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                   |
|-------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | NU61  | R    | 0h    | Reserved                                                                                                                                                                                      |
| 30    | TFQM  | R    | 0h    | Tx FIFO/Queue Mode<br>1'b0 = Tx FIFO operation<br>1'b1 = Tx Queue operation                                                                                                                   |
| 29:24 | TFQS  | R    | 0h    | Transmit FIFO/Queue Size<br>6'h00 = No Tx FIFO/Queue<br>6'b01-6'h20 (1-32) = Number of Tx Buffers used for Tx FIFO/Queue<br>> 6'h20 (32) = Values greater than 32 are interpreted as 32       |
| 23:22 | NU60  | R    | 0h    | Reserved                                                                                                                                                                                      |
| 21:16 | NDTB  | R    | 0h    | Number of Dedicated Transmit Buffers<br>6'h00 = No Dedicated Tx Buffers<br>6'h01-6'h20 (1-32) = Number of Dedicated Tx Buffers<br>> 6'h20 (32) = Values greater than 32 are interpreted as 32 |

**Table 5-2187. CFG\_TXBC Register Field Descriptions (continued)**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:2 | TBSA  | R    | 0h    | <p>Tx Buffers Start Address</p> <p>Start address of Tx Buffers section in Message RAM (32-bit word address, see Message RAM Configuration).</p> <p>Note: Be aware that the sum of the MCAN_TXBC[29-24] TFQS and MCAN_TXBC[21-16] NDTB fields may be not greater than 32. There is no check for erroneous configurations. The Tx Buffers section in the Message RAM starts with the dedicated Tx Buffers.</p> |
| 1:0  | NU59  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                     |

### 5.12.2.49 CFG\_TXFQS Register

#### 1 CFG\_TXFQS Register (Offset = 2C4h) [reset = 0h]

Tx FIFO/Queue Status register. Tx FIFO/Queue full indication and put index, Tx FIFO get index and fill level. The Tx FIFO/Queue status is related to the pending Tx requests listed in the MCAN\_TXBRP register. Therefore the effect of Add/Cancellation requests may be delayed due to a running Tx scan (the MCAN\_TXBRP register not yet updated).

Return to [Summary Table](#)

**Table 5-2188. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 82C4h       |
| MCAN1         | 5261 82C4h       |
| MCAN2         | 5262 82C4h       |
| MCAN3         | 5263 82C4h       |

**Figure 5-723. CFG\_TXFQS Name Register**

|      |    |      |       |    |    |    |    |
|------|----|------|-------|----|----|----|----|
| 31   | 30 | 29   | 28    | 27 | 26 | 25 | 24 |
| NU64 |    |      |       |    |    |    |    |
| R    |    |      |       |    |    |    |    |
| 0h   |    |      |       |    |    |    |    |
| 23   | 22 | 21   | 20    | 19 | 18 | 17 | 16 |
| NU64 |    | TFQF | TFQPI |    |    |    |    |
| R    |    | R    | R     |    |    |    |    |
| 0h   |    | 0h   | 0h    |    |    |    |    |
| 15   | 14 | 13   | 12    | 11 | 10 | 9  | 8  |
| NU63 |    |      | TFGI  |    |    |    |    |
| R    |    |      | R     |    |    |    |    |
| 0h   |    |      | 0h    |    |    |    |    |
| 7    | 6  | 5    | 4     | 3  | 2  | 1  | 0  |
| NU62 |    | TFFL |       |    |    |    |    |
| R    |    | R    |       |    |    |    |    |
| 0h   |    | 0h   |       |    |    |    |    |

**Table 5-2190. CFG\_TXFQS Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:22 | NU64  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 21    | TFQF  | R    | 0h    | Tx FIFO/Queue Full                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 20:16 | TFQPI | R    | 0h    | Tx FIFO/Queue Put Index                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 15:13 | NU63  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 12:8  | TFGI  | R    | 0h    | Tx Queue Get Index                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 7:6   | NU62  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 5:0   | TFFL  | R    | 0h    | Tx FIFO Free Level.<br>Number of consecutive free Tx FIFO elements starting from the MCAN_TXFQS[12-8] TFGI field, range 0 to 32. Read as zero when Tx Queue operation is configured (MCAN_TXBC[30] TFQM = 1'b1).<br>Note: In case of mixed configurations where dedicated Tx Buffers are combined with a Tx FIFO or a Tx Queue, the Put and Get Indices indicate the number of the Tx Buffer starting with the first dedicated Tx Buffers. |



### 5.12.2.50 CFG\_TXESC Register

#### 1 CFG\_TXESC Register (Offset = 2C8h) [reset = 0h]

Tx Buffer Element Size Configuration register. Configuration data field size for frame transmission. Configures the number of data bytes belonging to a Tx Buffer element. Data field sizes > 8 bytes are intended for CAN FD operation only.

Return to [Summary Table](#)

**Table 5-2191. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 82C8h       |
| MCAN1         | 5261 82C8h       |
| MCAN2         | 5262 82C8h       |
| MCAN3         | 5263 82C8h       |

**Figure 5-724. CFG\_TXESC Name Register**

|      |    |    |    |      |    |    |    |
|------|----|----|----|------|----|----|----|
| 31   | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
| NU65 |    |    |    |      |    |    |    |
| R    |    |    |    |      |    |    |    |
| 0h   |    |    |    |      |    |    |    |
| 23   | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| NU65 |    |    |    |      |    |    |    |
| R    |    |    |    |      |    |    |    |
| 0h   |    |    |    |      |    |    |    |
| 15   | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| NU65 |    |    |    |      |    |    |    |
| R    |    |    |    |      |    |    |    |
| 0h   |    |    |    |      |    |    |    |
| 7    | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| NU65 |    |    |    | TBDS |    |    |    |
| R    |    |    |    | R/W  |    |    |    |
| 0h   |    |    |    | 0h   |    |    |    |

**Table 5-2193. CFG\_TXESC Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | NU65  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 2:0  | TBDS  | R/W  | 0h    | <p>Tx Buffer Data Field Size</p> <p>3'b000 = 8 byte data field</p> <p>3'b001 = 12 byte data field</p> <p>3'b010 = 16 byte data field</p> <p>3'b011 = 20 byte data field</p> <p>3'b100 = 24 byte data field</p> <p>3'b101 = 32 byte data field</p> <p>3'b110 = 48 byte data field</p> <p>3'b111 = 64 byte data field</p> <p>Note: In case the data length code DLC of a Tx Buffer element is configured to a value higher than the Tx Buffer data field size MCAN_TXESC[2-0] TBDS, the bytes not defined by the Tx Buffer are transmitted as CCh (padding bytes).</p> |

### 5.12.2.51 CFG\_TXBRP Register

#### 1 CFG\_TXBRP Register (Offset = 2CCh) [reset = 0h]

Tx Buffer Request Pending register. PendingTx buffers with pending transmission request. Each Tx Buffer has its own Transmission Request Pending bit. The bits are set via the MCAN\_TXBAR register. The bits are reset after a requested transmission has completed or has been cancelled via the MCAN\_TXBCR register. The MCAN\_TXBRP bits are set only for those Tx Buffers configured via the MCAN\_TXBC register. After a MCAN\_TXBRP bit has been set, a Tx scan (see Tx Handling) is started to check for the pending Tx request with the highest priority (Tx Buffer with lowest Message ID).

Return to [Summary Table](#)

**Table 5-2194. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 82CCh       |
| MCAN1         | 5261 82CCh       |
| MCAN2         | 5262 82CCh       |
| MCAN3         | 5263 82CCh       |

**Figure 5-725. CFG\_TXBRP Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TRP |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TRP |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TRP |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TRP |    |    |    |    |    |    |    |
| R   |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 5-2196. CFG\_TXBRP Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                  |
|------|-------|------|-------|------------------------------|
| 31:0 | TRP   | R    | 0h    | Transmission Request Pending |

### 5.12.2.52 CFG\_TXBAR Register

#### 1 CFG\_TXBAR Register (Offset = 2D0h) [reset = 0h]

Tx Buffer Add Request register. Add transmission requests. Each Tx Buffer has its own Add Request bit. Writing 1h will set the corresponding Add Request bit; writing a 0h has no impact. This enables the Host CPU to set transmission requests for multiple Tx Buffers with one write to the MCAN\_TXBAR register. The MCAN\_TXBAR bits are set only for those Tx Buffers configured via the MCAN\_TXBC register. When no Tx scan is running, the bits are reset immediately, else the bits remain set until the Tx scan process has completed. Note: If an add request is applied for a Tx Buffer with pending transmission request (corresponding MCAN\_TXBRP bit already set), this add request is ignored.

Return to [Summary Table](#)

**Table 5-2197. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 82D0h       |
| MCAN1         | 5261 82D0h       |
| MCAN2         | 5262 82D0h       |
| MCAN3         | 5263 82D0h       |

**Figure 5-726. CFG\_TXBAR Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| AR     |    |    |    |    |    |    |    |
| R/W0TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| AR     |    |    |    |    |    |    |    |
| R/W0TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| AR     |    |    |    |    |    |    |    |
| R/W0TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| AR     |    |    |    |    |    |    |    |
| R/W0TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-2199. CFG\_TXBAR Register Field Descriptions**

| Bit  | Field | Type   | Reset | Description |
|------|-------|--------|-------|-------------|
| 31:0 | AR    | R/W0TC | 0h    | Add request |

### 5.12.2.53 CFG\_TXBCR Register

#### 1 CFG\_TXBCR Register (Offset = 2D4h) [reset = 0h]

Tx Buffer Cancellation Request register. Request cancellation of pending transmissions. Each Tx Buffer has its own Cancellation Request bit. Writing a 1h will set the corresponding Cancellation Request bit; writing a 0h has no impact. This enables the Host CPU to set cancellation requests for multiple Tx Buffers with one write to the MCAN\_TXBCR register. The MCAN\_TXBCR bits are set only for those Tx Buffers configured via the MCAN\_TXBC register. The bits remain set until the corresponding bit of the MCAN\_TXBRP register is reset.

Return to [Summary Table](#)

**Table 5-2200. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 82D4h       |
| MCAN1         | 5261 82D4h       |
| MCAN2         | 5262 82D4h       |
| MCAN3         | 5263 82D4h       |

**Figure 5-727. CFG\_TXBCR Name Register**

|        |    |    |    |    |    |    |    |
|--------|----|----|----|----|----|----|----|
| 31     | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CR     |    |    |    |    |    |    |    |
| R/W0TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 23     | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CR     |    |    |    |    |    |    |    |
| R/W0TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 15     | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CR     |    |    |    |    |    |    |    |
| R/W0TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |
| 7      | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CR     |    |    |    |    |    |    |    |
| R/W0TC |    |    |    |    |    |    |    |
| 0h     |    |    |    |    |    |    |    |

**Table 5-2202. CFG\_TXBCR Register Field Descriptions**

| Bit  | Field | Type   | Reset | Description          |
|------|-------|--------|-------|----------------------|
| 31:0 | CR    | R/W0TC | 0h    | Cancellation Request |

### 5.12.2.54 CFG\_TXBTO Register

#### 1 CFG\_TXBTO Register (Offset = 2D8h) [reset = 0h]

Tx Buffer Transmission Occurred register. Signals successful transmissions, set when corresponding MCAN\_TXBRP flag is cleared. Each Tx Buffer has its own Transmission Occurred bit. The bits are set when the corresponding MCAN\_TXBRP bit is cleared after a successful transmission. The bits are reset when a new transmission is requested by writing a 1h to the corresponding bit of register the MCAN\_TXBAR register.

Return to [Summary Table](#)

**Table 5-2203. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 82D8h       |
| MCAN1         | 5261 82D8h       |
| MCAN2         | 5262 82D8h       |
| MCAN3         | 5263 82D8h       |

**Figure 5-728. CFG\_TXBTO Name Register**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TO |    |    |    |    |    |    |    |
| R  |    |    |    |    |    |    |    |
| 0h |    |    |    |    |    |    |    |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TO |    |    |    |    |    |    |    |
| R  |    |    |    |    |    |    |    |
| 0h |    |    |    |    |    |    |    |
| 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TO |    |    |    |    |    |    |    |
| R  |    |    |    |    |    |    |    |
| 0h |    |    |    |    |    |    |    |
| 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TO |    |    |    |    |    |    |    |
| R  |    |    |    |    |    |    |    |
| 0h |    |    |    |    |    |    |    |

**Table 5-2205. CFG\_TXBTO Register Field Descriptions**

| Bit  | Field | Type | Reset | Description           |
|------|-------|------|-------|-----------------------|
| 31:0 | TO    | R    | 0h    | Transmission Occurred |

### 5.12.2.55 CFG\_TXBCF Register

#### 1 CFG\_TXBCF Register (Offset = 2DCh) [reset = 0h]

Tx Buffer Cancellation Finished register. Signals successful transmit cancellation, set when corresponding MCAN\_TXBRP flag is cleared after cancellation request. Each Tx Buffer has its own Cancellation Finished bit. The bits are set when the corresponding MCAN\_TXBRP bit is cleared after a cancellation was requested via the MCAN\_TXBCR register. In case the corresponding MCAN\_TXBRP bit was not set at the point of cancellation, MCAN\_TXBCF[n] CF bit is set immediately. The bits are reset when a new transmission is requested by writing a 1h to the corresponding bit of the MCAN\_TXBAR register.

Return to [Summary Table](#)

**Table 5-2206. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 82DCh       |
| MCAN1         | 5261 82DCh       |
| MCAN2         | 5262 82DCh       |
| MCAN3         | 5263 82DCh       |

**Figure 5-729. CFG\_TXBCF Name Register**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CF |    |    |    |    |    |    |    |
| R  |    |    |    |    |    |    |    |
| 0h |    |    |    |    |    |    |    |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CF |    |    |    |    |    |    |    |
| R  |    |    |    |    |    |    |    |
| 0h |    |    |    |    |    |    |    |
| 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CF |    |    |    |    |    |    |    |
| R  |    |    |    |    |    |    |    |
| 0h |    |    |    |    |    |    |    |
| 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CF |    |    |    |    |    |    |    |
| R  |    |    |    |    |    |    |    |
| 0h |    |    |    |    |    |    |    |

**Table 5-2208. CFG\_TXBCF Register Field Descriptions**

| Bit  | Field | Type | Reset | Description           |
|------|-------|------|-------|-----------------------|
| 31:0 | CF    | R    | 0h    | Cancellation Finished |

### 5.12.2.56 CFG\_TXBTIE Register

#### 1 CFG\_TXBTIE Register (Offset = 2E0h) [reset = 0h]

Tx Buffer Transmission Interrupt Enable register. Enable transmit interrupts for selected Tx buffers.

Return to [Summary Table](#)

**Table 5-2209. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 82E0h       |
| MCAN1         | 5261 82E0h       |
| MCAN2         | 5262 82E0h       |
| MCAN3         | 5263 82E0h       |

**Figure 5-730. CFG\_TXBTIE Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TIE |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TIE |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TIE |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TIE |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 5-2211. CFG\_TXBTIE Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                   |
|------|-------|------|-------|-------------------------------|
| 31:0 | TIE   | R/W  | 0h    | Transmission Interrupt Enable |

### 5.12.2.57 CFG\_TXBCIE Register

#### 1 CFG\_TXBCIE Register (Offset = 2E4h) [reset = 0h]

Tx Buffer Cancellation Finished Interrupt Enable register. Enable cancellation finished interrupts for selected Tx buffers.

Return to [Summary Table](#)

**Table 5-2212. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 82E4h       |
| MCAN1         | 5261 82E4h       |
| MCAN2         | 5262 82E4h       |
| MCAN3         | 5263 82E4h       |

**Figure 5-731. CFG\_TXBCIE Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CFIE |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CFIE |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CFIE |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CFIE |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-2214. CFG\_TXBCIE Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                            |
|------|-------|------|-------|----------------------------------------|
| 31:0 | CFIE  | R/W  | 0h    | Cancellation Finished Interrupt Enable |



### 5.12.2.58 CFG\_TXEFC Register

#### 1 CFG\_TXEFC Register (Offset = 2F0h) [reset = 0h]

Tx Event FIFO Configuration register. Tx event FIFO watermark, size and start address.

Return to [Summary Table](#)

**Table 5-2215. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 82F0h       |
| MCAN1         | 5261 82F0h       |
| MCAN2         | 5262 82F0h       |
| MCAN3         | 5263 82F0h       |

**Figure 5-732. CFG\_TXEFC Name Register**

|      |    |    |    |    |      |    |      |
|------|----|----|----|----|------|----|------|
| 31   | 30 | 29 | 28 | 27 | 26   | 25 | 24   |
| NU68 |    |    |    |    | EFWM |    |      |
| R/W  |    |    |    |    | R/W  |    |      |
| 0h   |    |    |    |    | 0h   |    |      |
| 23   | 22 | 21 | 20 | 19 | 18   | 17 | 16   |
| NU67 |    |    |    |    | EFS  |    |      |
| R/W  |    |    |    |    | R/W  |    |      |
| 0h   |    |    |    |    | 0h   |    |      |
| 15   | 14 | 13 | 12 | 11 | 10   | 9  | 8    |
|      |    |    |    |    | EFSA |    |      |
|      |    |    |    |    | R/W  |    |      |
|      |    |    |    |    | 0h   |    |      |
| 7    | 6  | 5  | 4  | 3  | 2    | 1  | 0    |
|      |    |    |    |    | EFSA |    | NU66 |
|      |    |    |    |    | R/W  |    | R/W  |
|      |    |    |    |    | 0h   |    | 0h   |

**Table 5-2217. CFG\_TXEFC Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                    |
|-------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | NU68  | R/W  | 0h    | Reserved                                                                                                                                                                                                                                                       |
| 29:24 | EFWM  | R/W  | 0h    | Event FIFO Watermark<br>6'h00 = Watermark interrupt disabled<br>6'h01-6'h20 (1-32) = Level for Tx Event FIFO watermark interrupt (MCAN_IR[13] TEFW)<br>> 6'h20 (32) = Watermark interrupt disabled                                                             |
| 23:22 | NU67  | R/W  | 0h    | Reserved                                                                                                                                                                                                                                                       |
| 21:16 | EFS   | R/W  | 0h    | Event FIFO Size<br>6'h00 = Tx Event FIFO disabled<br>6'h01-6'h20 (1-32) = Number of Tx Event FIFO elements<br>> 6'h20 (32) = Values greater than 32 are interpreted as 32<br>The Tx Event FIFO elements are indexed from 0 to MCAN_TXEFC[21-16] EFS field - 1. |
| 15:2  | EFSA  | R/W  | 0h    | Event FIFO Start Address<br>Start address of Tx Event FIFO in Message RAM (32-bit word address, see Message RAM Configuration).                                                                                                                                |
| 1:0   | NU66  | R/W  | 0h    | Reserved                                                                                                                                                                                                                                                       |

### 5.12.2.59 CFG\_TXEFS Register

#### 1 CFG\_TXEFS Register (Offset = 2F4h) [reset = 0h]

Tx Event FIFO Status register. Tx event FIFO element lost/full indication, put index, get index, and fill level.

Return to [Summary Table](#)

**Table 5-2218. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 82F4h       |
| MCAN1         | 5261 82F4h       |
| MCAN2         | 5262 82F4h       |
| MCAN3         | 5263 82F4h       |

**Figure 5-733. CFG\_TXEFS Name Register**

|      |    |      |    |      |    |      |     |
|------|----|------|----|------|----|------|-----|
| 31   | 30 | 29   | 28 | 27   | 26 | 25   | 24  |
| NU72 |    |      |    |      |    | TEFL | EFF |
| R    |    |      |    |      |    | R    | R   |
| 0h   |    |      |    |      |    | 0h   | 0h  |
| 23   | 22 | 21   | 20 | 19   | 18 | 17   | 16  |
| NU71 |    |      |    | EFPI |    |      |     |
| R    |    |      |    | R    |    |      |     |
| 0h   |    |      |    | 0h   |    |      |     |
| 15   | 14 | 13   | 12 | 11   | 10 | 9    | 8   |
| NU70 |    |      |    | EFGI |    |      |     |
| R    |    |      |    | R    |    |      |     |
| 0h   |    |      |    | 0h   |    |      |     |
| 7    | 6  | 5    | 4  | 3    | 2  | 1    | 0   |
| NU69 |    | EFFL |    |      |    |      |     |
| R    |    | R    |    |      |    |      |     |
| 0h   |    | 0h   |    |      |    |      |     |

**Table 5-2220. CFG\_TXEFS Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                     |
|-------|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:26 | NU72  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                        |
| 25    | TEFL  | R    | 0h    | Tx Event FIFO Element Lost<br>This bit is a copy of interrupt flag MCAN_IR[15] TEFL. When the MCAN_IR[15] TEFL flag is reset, this bit is also reset.<br>1'b0 = No Tx Event FIFO element lost<br>1'b1 = Tx Event FIFO element lost, also set after write attempt to Tx Event FIFO of size zero. |
| 24    | EFF   | R    | 0h    | Event FIFO Full                                                                                                                                                                                                                                                                                 |
| 23:21 | NU71  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                        |
| 20:16 | EFPI  | R    | 0h    | Event FIFO Put Index                                                                                                                                                                                                                                                                            |
| 15:13 | NU70  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                        |
| 12:8  | EFGI  | R    | 0h    | Event FIFO Get Index                                                                                                                                                                                                                                                                            |
| 7:6   | NU69  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                        |
| 5:0   | EFFL  | R    | 0h    | Event FIFO Fill Level                                                                                                                                                                                                                                                                           |

### 5.12.2.60 CFG\_TXEFA Register

#### 1 CFG\_TXEFA Register (Offset = 2F8h) [reset = 0h]

Tx Event FIFO Acknowledge register. Tx event FIFO acknowledge last index of read elements, updates get index and fill level.

Return to [Summary Table](#)

**Table 5-2221. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5260 82F8h       |
| MCAN1         | 5261 82F8h       |
| MCAN2         | 5262 82F8h       |
| MCAN3         | 5263 82F8h       |

**Figure 5-734. CFG\_TXEFA Name Register**

|      |    |    |    |      |    |    |    |
|------|----|----|----|------|----|----|----|
| 31   | 30 | 29 | 28 | 27   | 26 | 25 | 24 |
| NU73 |    |    |    |      |    |    |    |
| R    |    |    |    |      |    |    |    |
| 0h   |    |    |    |      |    |    |    |
| 23   | 22 | 21 | 20 | 19   | 18 | 17 | 16 |
| NU73 |    |    |    |      |    |    |    |
| R    |    |    |    |      |    |    |    |
| 0h   |    |    |    |      |    |    |    |
| 15   | 14 | 13 | 12 | 11   | 10 | 9  | 8  |
| NU73 |    |    |    |      |    |    |    |
| R    |    |    |    |      |    |    |    |
| 0h   |    |    |    |      |    |    |    |
| 7    | 6  | 5  | 4  | 3    | 2  | 1  | 0  |
| NU73 |    |    |    | EFAI |    |    |    |
| R    |    |    |    | R    |    |    |    |
| 0h   |    |    |    | 0h   |    |    |    |

**Table 5-2223. CFG\_TXEFA Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                   |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:5 | NU73  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                      |
| 4:0  | EFAI  | R    | 0h    | Event FIFO Acknowledge Index<br>After the Host CPU has read an element or a sequence of elements from the Tx Event FIFO it has to write the index of the last element read from Tx Event FIFO to the MCAN_TXEFA[4-0] EFAI field. This will set the Tx Event FIFO Get Index MCAN_TXEFS[12-8] EFGI field to the MCAN_TXEFA[4-0] EFAI field + 1 and update the Event FIFO Fill Level MCAN_TXEFS[5-0] EFFL field. |

### 5.12.2.61 ECC\_REV Register

#### 1 ECC\_REV Register (Offset = 0h) [reset = 66A0EA00h]

Aggregator Revision Register. The Aggregator Revision Register contains the revision parameters for the ECC Aggregator.

Return to [Summary Table](#)

**Table 5-2224. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5270 0000h       |
| MCAN1         | 5270 1000h       |
| MCAN2         | 5270 2000h       |
| MCAN3         | 5270 3000h       |

**Figure 5-735. ECC\_REV Name Register**

|           |    |        |    |           |        |    |    |
|-----------|----|--------|----|-----------|--------|----|----|
| 31        | 30 | 29     | 28 | 27        | 26     | 25 | 24 |
| SCHEME    |    | BU     |    | MODULE_ID |        |    |    |
| R         |    | R      |    | R         |        |    |    |
| 1h        |    | 2h     |    | 6A0h      |        |    |    |
| 23        | 22 | 21     | 20 | 19        | 18     | 17 | 16 |
| MODULE_ID |    |        |    |           |        |    |    |
| R         |    |        |    |           |        |    |    |
| 6A0h      |    |        |    |           |        |    |    |
| 15        | 14 | 13     | 12 | 11        | 10     | 9  | 8  |
| REVRTL    |    |        |    |           | REVMAJ |    |    |
| R         |    |        |    |           | R      |    |    |
| 1Dh       |    |        |    |           | 2h     |    |    |
| 7         | 6  | 5      | 4  | 3         | 2      | 1  | 0  |
| CUSTOM    |    | REVMIN |    |           |        |    |    |
| R         |    | R      |    |           |        |    |    |
| 0h        |    | 0h     |    |           |        |    |    |

**Table 5-2226. ECC\_REV Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description    |
|-------|-----------|------|-------|----------------|
| 31:30 | SCHEME    | R    | 1h    | Scheme         |
| 29:28 | BU        | R    | 2h    | Business Unit  |
| 27:16 | MODULE_ID | R    | 6A0h  | Module ID      |
| 15:11 | REVRTL    | R    | 1Dh   | RTL version    |
| 10:8  | REVMAJ    | R    | 2h    | Major version  |
| 7:6   | CUSTOM    | R    | 0h    | Custom version |
| 5:0   | REVMIN    | R    | 0h    | Minor version  |

### 5.12.2.62 ECC\_VECTOR Register

#### 1 ECC\_VECTOR Register (Offset = 8h) [reset = 0h]

ECC RAM ID to select which ECC RAM to control or read status from.

Return to [Summary Table](#)

**Table 5-2227. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5270 0008h       |
| MCAN1         | 5270 1008h       |
| MCAN2         | 5270 2008h       |
| MCAN3         | 5270 3008h       |

**Figure 5-736. ECC\_VECTOR Name Register**

|               |     |    |    |    |         |    |                   |
|---------------|-----|----|----|----|---------|----|-------------------|
| 31            | 30  | 29 | 28 | 27 | 26      | 25 | 24                |
| NU1           |     |    |    |    |         |    | RD_SVBUS_D<br>ONE |
| NU1           |     |    |    |    |         |    | R/W               |
| 0h            |     |    |    |    |         |    | 0h                |
| 23            | 22  | 21 | 20 | 19 | 18      | 17 | 16                |
| RD_SVBUS_ADDR |     |    |    |    |         |    |                   |
| R/W           |     |    |    |    |         |    |                   |
| 0h            |     |    |    |    |         |    |                   |
| 15            | 14  | 13 | 12 | 11 | 10      | 9  | 8                 |
| RD_SVBUS      | NU0 |    |    |    | ECC_VEC |    |                   |
| R/W           | R   |    |    |    | R/W     |    |                   |
| 0h            | 0h  |    |    |    | 0h      |    |                   |
| 7             | 6   | 5  | 4  | 3  | 2       | 1  | 0                 |
| ECC_VEC       |     |    |    |    |         |    |                   |
| R/W           |     |    |    |    |         |    |                   |
| 0h            |     |    |    |    |         |    |                   |

**Table 5-2229. ECC\_VECTOR Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                                                                       |
|-------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:25 | NU1           | NU1  | 0h    | Reserved                                                                                                                                                                                          |
| 24    | RD_SVBUS_DONE | R/W  | 0h    | Status to indicate if read on serial VBUS is complete, write of any value will clear this bit. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. |
| 23:16 | RD_SVBUS_ADDR | R/W  | 0h    | Read address                                                                                                                                                                                      |
| 15    | RD_SVBUS      | R/W  | 0h    | Write 1 to trigger a read on the serial VBUS. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.                                                     |
| 14:11 | NU0           | R    | 0h    | Reserved                                                                                                                                                                                          |
| 10:0  | ECC_VEC       | R/W  | 0h    | Value written to select the corresponding ECC RAM for control or status                                                                                                                           |

### 5.12.2.63 ECC\_STAT Register

#### 1 ECC\_STAT Register (Offset = Ch) [reset = 2h]

Contains misc status such as number of ECC RAMs serviced by the ECC aggregator.

Return to [Summary Table](#)

**Table 5-2230. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5270 000Ch       |
| MCAN1         | 5270 100Ch       |
| MCAN2         | 5270 200Ch       |
| MCAN3         | 5270 300Ch       |

**Figure 5-737. ECC\_STAT Name Register**

|          |    |    |    |          |    |    |    |
|----------|----|----|----|----------|----|----|----|
| 31       | 30 | 29 | 28 | 27       | 26 | 25 | 24 |
| NU2      |    |    |    |          |    |    |    |
| NU2      |    |    |    |          |    |    |    |
| 0h       |    |    |    |          |    |    |    |
| 23       | 22 | 21 | 20 | 19       | 18 | 17 | 16 |
| NU2      |    |    |    |          |    |    |    |
| NU2      |    |    |    |          |    |    |    |
| 0h       |    |    |    |          |    |    |    |
| 15       | 14 | 13 | 12 | 11       | 10 | 9  | 8  |
| NU2      |    |    |    | NUM_RAMs |    |    |    |
| NU2      |    |    |    | R        |    |    |    |
| 0h       |    |    |    | 2h       |    |    |    |
| 7        | 6  | 5  | 4  | 3        | 2  | 1  | 0  |
| NUM_RAMs |    |    |    |          |    |    |    |
| R        |    |    |    |          |    |    |    |
| 2h       |    |    |    |          |    |    |    |

**Table 5-2232. ECC\_STAT Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                 |
|-------|----------|------|-------|-------------------------------------------------------------|
| 31:11 | NU2      | NU2  | 0h    | Reserved                                                    |
| 10:0  | NUM_RAMs | R    | 2h    | Indicates the number of RAMs serviced by the ECC aggregator |

### 5.12.2.64 ECC\_CTRL Register

#### 1 ECC\_CTRL Register (Offset = 14h) [reset = 107h]

ECC Control Register.

Return to [Summary Table](#)

**Table 5-2233. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5270 0014h       |
| MCAN1         | 5270 1014h       |
| MCAN2         | 5270 2014h       |
| MCAN3         | 5270 3014h       |

**Figure 5-738. ECC\_CTRL Name Register**

|          |            |             |           |           |        |         |        |
|----------|------------|-------------|-----------|-----------|--------|---------|--------|
| 31       | 30         | 29          | 28        | 27        | 26     | 25      | 24     |
| NU3      |            |             |           |           |        |         |        |
| R        |            |             |           |           |        |         |        |
| 0h       |            |             |           |           |        |         |        |
| 23       | 22         | 21          | 20        | 19        | 18     | 17      | 16     |
| NU3      |            |             |           |           |        |         |        |
| R        |            |             |           |           |        |         |        |
| 0h       |            |             |           |           |        |         |        |
| 15       | 14         | 13          | 12        | 11        | 10     | 9       | 8      |
| NU3      |            |             |           |           |        |         | CHECK  |
| R        |            |             |           |           |        |         | R/W    |
| 0h       |            |             |           |           |        |         | 1h     |
| 7        | 6          | 5           | 4         | 3         | 2      | 1       | 0      |
| RESERVED | ERROR_ONCE | FORCE_N_ROW | FORCE_DED | FORCE_SEC | EN_RMW | ECC_CHK | ECC_EN |
| NONE     | W          | W           | W         | W         | W      | W       | W      |
| 0h       | 0h         | 0h          | 0h        | 0h        | 1h     | 1h      | 1h     |

**Table 5-2235. ECC\_CTRL Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                               |
|------|-------------|------|-------|-----------------------------------------------------------|
| 31:9 | NU3         | R    | 0h    | TI Internal : Reserved                                    |
| 8    | CHECK       | R/W  | 1h    | TI Internal : Check Parity<br>TI Internal : Check timeout |
| 7    | RESERVED    | NONE | 0h    | Reserved                                                  |
| 6    | ERROR_ONCE  | W    | 0h    | TI Internal : Force Error only once                       |
| 5    | FORCE_N_ROW | W    | 0h    | TI Internal : Force Error on any RAM read                 |
| 4    | FORCE_DED   | W    | 0h    | TI Internal : Force Double Bit Error                      |
| 3    | FORCE_SEC   | W    | 0h    | TI Internal : Force Single Bit Error                      |
| 2    | EN_RMW      | W    | 1h    | TI Internal : Enable rmw                                  |
| 1    | ECC_CHK     | W    | 1h    | TI Internal : Enable ECC check                            |
| 0    | ECC_EN      | W    | 1h    | TI Internal : Enable ECC                                  |

### 5.12.2.65 ECC\_ERR\_CTRL1 Register

#### 1 ECC\_ERR\_CTRL1 Register (Offset = 18h) [reset = 0h]

ECC Error Control1 Register.

Return to [Summary Table](#)

**Table 5-2236. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5270 0018h       |
| MCAN1         | 5270 1018h       |
| MCAN2         | 5270 2018h       |
| MCAN3         | 5270 3018h       |

**Figure 5-739. ECC\_ERR\_CTRL1 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ECC_ROW |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ECC_ROW |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ECC_ROW |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ECC_ROW |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-2238. ECC\_ERR\_CTRL1 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                           |
|------|---------|------|-------|-----------------------------------------------------------------------------------------------------------------------|
| 31:0 | ECC_ROW | R/W  | 0h    | TI Internal : Row address where single or double-bit error needs to be applied. This is ignored if force_n_row is set |



### 5.12.2.66 ECC\_ERR\_CTRL2 Register

#### 1 ECC\_ERR\_CTRL2 Register (Offset = 1Ch) [reset = 0h]

ECC Error Control2 Register.

Return to [Summary Table](#)

**Table 5-2239. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5270 001Ch       |
| MCAN1         | 5270 101Ch       |
| MCAN2         | 5270 201Ch       |
| MCAN3         | 5270 301Ch       |

**Figure 5-740. ECC\_ERR\_CTRL2 Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ECC_BIT2 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ECC_BIT2 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ECC_BIT1 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ECC_BIT1 |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2241. ECC\_ERR\_CTRL2 Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                            |
|-------|----------|------|-------|----------------------------------------------------------------------------------------|
| 31:16 | ECC_BIT2 | R/W  | 0h    | TI Internal : Data bit that needs to be flipped if double bit error needs to be forced |
| 15:0  | ECC_BIT1 | R/W  | 0h    | TI Internal : Data bit that needs to be flipped when force_sec is set                  |

### 5.12.2.67 ECC\_ERR\_STAT1 Register

#### 1 ECC\_ERR\_STAT1 Register (Offset = 20h) [reset = 0h]

ECC Error Status1 Register.

Return to [Summary Table](#)

**Table 5-2242. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5270 0020h       |
| MCAN1         | 5270 1020h       |
| MCAN2         | 5270 2020h       |
| MCAN3         | 5270 3020h       |

**Figure 5-741. ECC\_ERR\_STAT1 Name Register**

|                 |             |    |               |             |    |             |    |
|-----------------|-------------|----|---------------|-------------|----|-------------|----|
| 31              | 30          | 29 | 28            | 27          | 26 | 25          | 24 |
| ECC_BIT1_STS    |             |    |               |             |    |             |    |
| R               |             |    |               |             |    |             |    |
| 0h              |             |    |               |             |    |             |    |
| 23              | 22          | 21 | 20            | 19          | 18 | 17          | 16 |
| ECC_BIT1_STS    |             |    |               |             |    |             |    |
| R               |             |    |               |             |    |             |    |
| 0h              |             |    |               |             |    |             |    |
| 15              | 14          | 13 | 12            | 11          | 10 | 9           | 8  |
| CLR_ECC_CTL_REG | CLR_ECC_PAR |    | CLR_ECC_OTHER | CLR_ECC_DED |    | CLR_ECC_SEC |    |
| W               | W           |    | W             | W           |    | W           |    |
| 0h              | 0h          |    | 0h            | 0h          |    | 0h          |    |
| 7               | 6           | 5  | 4             | 3           | 2  | 1           | 0  |
| ECC_CTRL_REG    | ECC_PAR     |    | ECC_OTHER     | ECC_DED     |    | ECC_SEC     |    |
| W               | W           |    | W             | W           |    | W           |    |
| 0h              | 0h          |    | 0h            | 0h          |    | 0h          |    |

**Table 5-2244. ECC\_ERR\_STAT1 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                                                                                  |
|-------|------------------|------|-------|----------------------------------------------------------------------------------------------|
| 31:16 | ECC_BIT1_STS     | R    | 0h    | TI Internal : Data bit that corresponds to the single-bit error                              |
| 15    | CLR_ECC_CTRL_REG | W    | 0h    | TI Internal : Clear Ctrl Reg Error Status. Write 1 to clear. This bit is self clearing.      |
| 14:13 | CLR_ECC_PAR      | W    | 0h    | TI Internal : Clear Parity Error Status. Write 1 to clear. This bit is self clearing.        |
| 12    | CLR_ECC_OTHER    | W    | 0h    | TI Internal : Clear Other Error Status. Write 1 to clear. This bit is self clearing.         |
| 11:10 | CLR_ECC_DED      | W    | 0h    | TI Internal : Clear Double Bit Error Status. Write 1 to clear. This bit is self clearing.    |
| 9:8   | CLR_ECC_SEC      | W    | 0h    | TI Internal : Clear Single Bit Error Status. Write 1 to clear. This bit is self clearing.    |
| 7     | ECC_CTRL_REG     | W    | 0h    | TI Internal : Force ctrl reg pending interrupt. Write 1 to set. This bit is self clearing.   |
| 6:5   | ECC_PAR          | W    | 0h    | TI Internal : Force ECC parity pending interrupt. Write 1 to set. This bit is self clearing. |

**Table 5-2244. ECC\_ERR\_STAT1 Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description                                                                                 |
|-----|-----------|------|-------|---------------------------------------------------------------------------------------------|
| 4   | ECC_OTHER | W    | 0h    | TI Internal : Force ECC other pending interrupt. Write 1 to set. This bit is self clearing. |
| 3:2 | ECC_DED   | W    | 0h    | TI Internal : Force ECC DED pending interrupt. Write 1 to set. This bit is self clearing.   |
| 1:0 | ECC_SEC   | W    | 0h    | TI Internal : Force ECC SEC pending interrupt. Write 1 to set. This bit is self clearing.   |

### 5.12.2.68 ECC\_ERR\_STAT2 Register

#### 1 ECC\_ERR\_STAT2 Register (Offset = 24h) [reset = 0h]

ECC Error Status2 Register.

Return to [Summary Table](#)

**Table 5-2245. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5270 0024h       |
| MCAN1         | 5270 1024h       |
| MCAN2         | 5270 2024h       |
| MCAN3         | 5270 3024h       |

**Figure 5-742. ECC\_ERR\_STAT2 Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ECC_ROW |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ECC_ROW |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ECC_ROW |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ECC_ROW |    |    |    |    |    |    |    |
| R       |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-2247. ECC\_ERR\_STAT2 Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                 |
|------|---------|------|-------|-----------------------------------------------------------------------------|
| 31:0 | ECC_ROW | R    | 0h    | TI Internal : Row address where the single or double-bit error has occurred |

### 5.12.2.69 ECC\_ERR\_STAT3 Register

#### 1 ECC\_ERR\_STAT3 Register (Offset = 28h) [reset = 0h]

ECC Error Status3 Register.

Return to [Summary Table](#)

**Table 5-2248. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5270 0028h       |
| MCAN1         | 5270 1028h       |
| MCAN2         | 5270 2028h       |
| MCAN3         | 5270 3028h       |

**Figure 5-743. ECC\_ERR\_STAT3 Name Register**

|     |    |    |    |    |    |                  |     |
|-----|----|----|----|----|----|------------------|-----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25               | 24  |
| NU6 |    |    |    |    |    |                  |     |
| R   |    |    |    |    |    |                  |     |
| 0h  |    |    |    |    |    |                  |     |
| 23  | 22 | 21 | 20 | 19 | 18 | 17               | 16  |
| NU6 |    |    |    |    |    |                  |     |
| R   |    |    |    |    |    |                  |     |
| 0h  |    |    |    |    |    |                  |     |
| 15  | 14 | 13 | 12 | 11 | 10 | 9                | 8   |
| NU6 |    |    |    |    |    | CLR_TIMEOUT_PEND | NU5 |
| R   |    |    |    |    |    | W                | R   |
| 0h  |    |    |    |    |    | 0h               | 0h  |
| 7   | 6  | 5  | 4  | 3  | 2  | 1                | 0   |
| NU5 |    |    |    |    |    | TIMEOUT_PEND     | NU4 |
| R   |    |    |    |    |    | W                | R   |
| 0h  |    |    |    |    |    | 0h               | 0h  |

**Table 5-2250. ECC\_ERR\_STAT3 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description                         |
|-------|------------------|------|-------|-------------------------------------|
| 31:10 | NU6              | R    | 0h    | TI Internal : Reserved              |
| 9     | CLR_TIMEOUT_PEND | W    | 0h    | TI Internal : Clear timeout pending |
| 8:2   | NU5              | R    | 0h    | TI Internal : Reserved              |
| 1     | TIMEOUT_PEND     | W    | 0h    | TI Internal : Timeout pending       |
| 0     | NU4              | R    | 0h    | TI Internal : Reserved              |

### 5.12.2.70 ECC\_SEC\_EOI\_REG Register

#### 1 ECC\_SEC\_EOI\_REG Register (Offset = 3Ch) [reset = 0h]

EOI Register.

Return to [Summary Table](#)

**Table 5-2251. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5270 003Ch       |
| MCAN1         | 5270 103Ch       |
| MCAN2         | 5270 203Ch       |
| MCAN3         | 5270 303Ch       |

**Figure 5-744. ECC\_SEC\_EOI\_REG Name Register**

|     |    |    |    |    |    |    |            |
|-----|----|----|----|----|----|----|------------|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24         |
| NU7 |    |    |    |    |    |    |            |
| R   |    |    |    |    |    |    |            |
| 0h  |    |    |    |    |    |    |            |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16         |
| NU7 |    |    |    |    |    |    |            |
| R   |    |    |    |    |    |    |            |
| 0h  |    |    |    |    |    |    |            |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8          |
| NU7 |    |    |    |    |    |    |            |
| R   |    |    |    |    |    |    |            |
| 0h  |    |    |    |    |    |    |            |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0          |
| NU7 |    |    |    |    |    |    | SEC_EOI_WR |
| R   |    |    |    |    |    |    | R/W        |
| 0h  |    |    |    |    |    |    | 0h         |

**Table 5-2253. ECC\_SEC\_EOI\_REG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                              |
|------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | NU7        | R    | 0h    | Reserved                                                                                                                                                                 |
| 0    | SEC_EOI_WR | R/W  | 0h    | EOI Register. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field. This bit is self clearing, Reading this bit will return 0. |

### 5.12.2.71 ECC\_SEC\_STATUS\_REG0 Register

#### 1 ECC\_SEC\_STATUS\_REG0 Register (Offset = 40h) [reset = 0h]

Interrupt Status Register 0

Return to [Summary Table](#)

**Table 5-2254. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5270 0040h       |
| MCAN1         | 5270 1040h       |
| MCAN2         | 5270 2040h       |
| MCAN3         | 5270 3040h       |

**Figure 5-745. ECC\_SEC\_STATUS\_REG0 Name Register**

|     |    |    |    |    |    |                         |          |
|-----|----|----|----|----|----|-------------------------|----------|
| 31  | 30 | 29 | 28 | 27 | 26 | 25                      | 24       |
| NU8 |    |    |    |    |    |                         |          |
| R   |    |    |    |    |    |                         |          |
| 0h  |    |    |    |    |    |                         |          |
| 23  | 22 | 21 | 20 | 19 | 18 | 17                      | 16       |
| NU8 |    |    |    |    |    |                         |          |
| R   |    |    |    |    |    |                         |          |
| 0h  |    |    |    |    |    |                         |          |
| 15  | 14 | 13 | 12 | 11 | 10 | 9                       | 8        |
| NU8 |    |    |    |    |    |                         |          |
| R   |    |    |    |    |    |                         |          |
| 0h  |    |    |    |    |    |                         |          |
| 7   | 6  | 5  | 4  | 3  | 2  | 1                       | 0        |
| NU8 |    |    |    |    |    | CTRL_EDC_VB<br>USS_PEND | SEC_PEND |
| R   |    |    |    |    |    | R                       | R        |
| 0h  |    |    |    |    |    | 0h                      | 0h       |

**Table 5-2256. ECC\_SEC\_STATUS\_REG0 Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                       |
|------|-------------------------|------|-------|---------------------------------------------------|
| 31:2 | NU8                     | R    | 0h    | Reserved                                          |
| 1    | CTRL_EDC_VBUSS_PEN<br>D | R    | 0h    | Interrupt Pending Status for ctrl_edc_vbuss_pend. |
| 0    | SEC_PEND                | R    | 0h    | Interrupt Pending Status for msgmem_pend.         |

### 5.12.2.72 ECC\_SEC\_ENABLE\_SET\_REG0 Register

#### 1 ECC\_SEC\_ENABLE\_SET\_REG0 Register (Offset = 80h) [reset = 0h]

Interrupt Enable Set Register 0

Return to [Summary Table](#)

**Table 5-2257. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5270 0080h       |
| MCAN1         | 5270 1080h       |
| MCAN2         | 5270 2080h       |
| MCAN3         | 5270 3080h       |

**Figure 5-746. ECC\_SEC\_ENABLE\_SET\_REG0 Name Register**

|     |    |    |    |    |    |                                   |            |
|-----|----|----|----|----|----|-----------------------------------|------------|
| 31  | 30 | 29 | 28 | 27 | 26 | 25                                | 24         |
| NU9 |    |    |    |    |    |                                   |            |
| R   |    |    |    |    |    |                                   |            |
| 0h  |    |    |    |    |    |                                   |            |
| 23  | 22 | 21 | 20 | 19 | 18 | 17                                | 16         |
| NU9 |    |    |    |    |    |                                   |            |
| R   |    |    |    |    |    |                                   |            |
| 0h  |    |    |    |    |    |                                   |            |
| 15  | 14 | 13 | 12 | 11 | 10 | 9                                 | 8          |
| NU9 |    |    |    |    |    |                                   |            |
| R   |    |    |    |    |    |                                   |            |
| 0h  |    |    |    |    |    |                                   |            |
| 7   | 6  | 5  | 4  | 3  | 2  | 1                                 | 0          |
| NU9 |    |    |    |    |    | CTRL_EDC_VB<br>USS_ENABLE_<br>SET | SEC_EN_SET |
| R   |    |    |    |    |    | R/W                               | R/W        |
| 0h  |    |    |    |    |    | 0h                                | 0h         |

**Table 5-2259. ECC\_SEC\_ENABLE\_SET\_REG0 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                                                            |
|------|---------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | NU9                       | R    | 0h    | Reserved                                                                                                                                               |
| 1    | CTRL_EDC_VBUSS_ENABLE_SET | R/W  | 0h    | Interrupt Enable Set Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field. |
| 0    | SEC_EN_SET                | R/W  | 0h    | Interrupt Enable Set Register for msgmem_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.         |



### 5.12.2.73 ECC\_SEC\_ENABLE\_CLR\_REG0 Register

#### 1 ECC\_SEC\_ENABLE\_CLR\_REG0 Register (Offset = C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to [Summary Table](#)

**Table 5-2260. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5270 00C0h       |
| MCAN1         | 5270 10C0h       |
| MCAN2         | 5270 20C0h       |
| MCAN3         | 5270 30C0h       |

**Figure 5-747. ECC\_SEC\_ENABLE\_CLR\_REG0 Name Register**

|      |    |    |    |    |    |                                   |            |
|------|----|----|----|----|----|-----------------------------------|------------|
| 31   | 30 | 29 | 28 | 27 | 26 | 25                                | 24         |
| NU10 |    |    |    |    |    |                                   |            |
| R    |    |    |    |    |    |                                   |            |
| 0h   |    |    |    |    |    |                                   |            |
| 23   | 22 | 21 | 20 | 19 | 18 | 17                                | 16         |
| NU10 |    |    |    |    |    |                                   |            |
| R    |    |    |    |    |    |                                   |            |
| 0h   |    |    |    |    |    |                                   |            |
| 15   | 14 | 13 | 12 | 11 | 10 | 9                                 | 8          |
| NU10 |    |    |    |    |    |                                   |            |
| R    |    |    |    |    |    |                                   |            |
| 0h   |    |    |    |    |    |                                   |            |
| 7    | 6  | 5  | 4  | 3  | 2  | 1                                 | 0          |
| NU10 |    |    |    |    |    | CTRL_EDC_VB<br>USS_ENABLE_<br>CLR | SEC_EN_CLR |
| R    |    |    |    |    |    | R/W                               | R/W        |
| 0h   |    |    |    |    |    | 0h                                | 0h         |

**Table 5-2262. ECC\_SEC\_ENABLE\_CLR\_REG0 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                                                                                                 |
|------|---------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | NU10                      | R    | 0h    | Reserved                                                                                                                                                                                    |
| 1    | CTRL_EDC_VBUSS_ENABLE_CLR | R/W  | 0h    | Interrupt Enable Clear Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0. |
| 0    | SEC_EN_CLR                | R/W  | 0h    | Interrupt Enable Clear Register for msgmem_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.         |

### 5.12.2.74 ECC\_DED\_EOI\_REG Register

#### 1 ECC\_DED\_EOI\_REG Register (Offset = 13Ch) [reset = 0h]

EOI Register.

Return to [Summary Table](#)

**Table 5-2263. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5270 013Ch       |
| MCAN1         | 5270 113Ch       |
| MCAN2         | 5270 213Ch       |
| MCAN3         | 5270 313Ch       |

**Figure 5-748. ECC\_DED\_EOI\_REG Name Register**

|      |    |    |    |    |    |    |            |
|------|----|----|----|----|----|----|------------|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24         |
| NU11 |    |    |    |    |    |    |            |
| R    |    |    |    |    |    |    |            |
| 0h   |    |    |    |    |    |    |            |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16         |
| NU11 |    |    |    |    |    |    |            |
| R    |    |    |    |    |    |    |            |
| 0h   |    |    |    |    |    |    |            |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8          |
| NU11 |    |    |    |    |    |    |            |
| R    |    |    |    |    |    |    |            |
| 0h   |    |    |    |    |    |    |            |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0          |
| NU11 |    |    |    |    |    |    | DED_EOI_WR |
| R    |    |    |    |    |    |    | R/W        |
| 0h   |    |    |    |    |    |    | 0h         |

**Table 5-2265. ECC\_DED\_EOI\_REG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                              |
|------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | NU11       | R    | 0h    | Reserved                                                                                                                                                                 |
| 0    | DED_EOI_WR | R/W  | 0h    | EOI Register. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field. This bit is self clearing, Reading this bit will return 0. |

### 5.12.2.75 ECC\_DED\_STATUS\_REG0 Register

#### 1 ECC\_DED\_STATUS\_REG0 Register (Offset = 140h) [reset = 0h]

Interrupt Status Register 0

Return to [Summary Table](#)

**Table 5-2266. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5270 0140h       |
| MCAN1         | 5270 1140h       |
| MCAN2         | 5270 2140h       |
| MCAN3         | 5270 3140h       |

**Figure 5-749. ECC\_DED\_STATUS\_REG0 Name Register**

|      |    |    |    |    |    |                         |          |
|------|----|----|----|----|----|-------------------------|----------|
| 31   | 30 | 29 | 28 | 27 | 26 | 25                      | 24       |
| NU12 |    |    |    |    |    |                         |          |
| R    |    |    |    |    |    |                         |          |
| 0h   |    |    |    |    |    |                         |          |
| 23   | 22 | 21 | 20 | 19 | 18 | 17                      | 16       |
| NU12 |    |    |    |    |    |                         |          |
| R    |    |    |    |    |    |                         |          |
| 0h   |    |    |    |    |    |                         |          |
| 15   | 14 | 13 | 12 | 11 | 10 | 9                       | 8        |
| NU12 |    |    |    |    |    |                         |          |
| R    |    |    |    |    |    |                         |          |
| 0h   |    |    |    |    |    |                         |          |
| 7    | 6  | 5  | 4  | 3  | 2  | 1                       | 0        |
| NU12 |    |    |    |    |    | CTRL_EDC_VB<br>USS_PEND | DED_PEND |
| R    |    |    |    |    |    | R                       | R        |
| 0h   |    |    |    |    |    | 0h                      | 0h       |

**Table 5-2268. ECC\_DED\_STATUS\_REG0 Register Field Descriptions**

| Bit  | Field                   | Type | Reset | Description                                       |
|------|-------------------------|------|-------|---------------------------------------------------|
| 31:2 | NU12                    | R    | 0h    | Reserved                                          |
| 1    | CTRL_EDC_VBUSS_PEN<br>D | R    | 0h    | Interrupt Pending Status for ctrl_edc_vbuss_pend. |
| 0    | DED_PEND                | R    | 0h    | Interrupt Pending Status for msgmem_pend.         |

### 5.12.2.76 ECC\_DED\_ENABLE\_SET\_REG0 Register

#### 1 ECC\_DED\_ENABLE\_SET\_REG0 Register (Offset = 180h) [reset = 0h]

Interrupt Enable Set Register 0

Return to [Summary Table](#)

**Table 5-2269. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5270 0180h       |
| MCAN1         | 5270 1180h       |
| MCAN2         | 5270 2180h       |
| MCAN3         | 5270 3180h       |

**Figure 5-750. ECC\_DED\_ENABLE\_SET\_REG0 Name Register**

|      |    |    |    |    |    |                                   |            |
|------|----|----|----|----|----|-----------------------------------|------------|
| 31   | 30 | 29 | 28 | 27 | 26 | 25                                | 24         |
| NU13 |    |    |    |    |    |                                   |            |
| R    |    |    |    |    |    |                                   |            |
| 0h   |    |    |    |    |    |                                   |            |
| 23   | 22 | 21 | 20 | 19 | 18 | 17                                | 16         |
| NU13 |    |    |    |    |    |                                   |            |
| R    |    |    |    |    |    |                                   |            |
| 0h   |    |    |    |    |    |                                   |            |
| 15   | 14 | 13 | 12 | 11 | 10 | 9                                 | 8          |
| NU13 |    |    |    |    |    |                                   |            |
| R    |    |    |    |    |    |                                   |            |
| 0h   |    |    |    |    |    |                                   |            |
| 7    | 6  | 5  | 4  | 3  | 2  | 1                                 | 0          |
| NU13 |    |    |    |    |    | CTRL_EDC_VB<br>USS_ENABLE_<br>SET | DED_EN_SET |
| R    |    |    |    |    |    | R/W                               | R/W        |
| 0h   |    |    |    |    |    | 0h                                | 0h         |

**Table 5-2271. ECC\_DED\_ENABLE\_SET\_REG0 Register Field Descriptions**

| Bit  | Field                     | Type | Reset | Description                                                                                                                                            |
|------|---------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | NU13                      | R    | 0h    | Reserved                                                                                                                                               |
| 1    | CTRL_EDC_VBUSS_ENABLE_SET | R/W  | 0h    | Interrupt Enable Set Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field. |
| 0    | DED_EN_SET                | R/W  | 0h    | Interrupt Enable Set Register for msgmem_pend. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.         |

### 5.12.2.77 ECC\_DED\_ENABLE\_CLR\_REG0 Register

#### 1 ECC\_DED\_ENABLE\_CLR\_REG0 Register (Offset = 1C0h) [reset = 0h]

Interrupt Enable Clear Register 0

Return to [Summary Table](#)

**Table 5-2272. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5270 01C0h       |
| MCAN1         | 5270 11C0h       |
| MCAN2         | 5270 21C0h       |
| MCAN3         | 5270 31C0h       |

**Figure 5-751. ECC\_DED\_ENABLE\_CLR\_REG0 Name Register**

|      |    |    |    |    |    |                                   |            |
|------|----|----|----|----|----|-----------------------------------|------------|
| 31   | 30 | 29 | 28 | 27 | 26 | 25                                | 24         |
| NU14 |    |    |    |    |    |                                   |            |
| R    |    |    |    |    |    |                                   |            |
| 0h   |    |    |    |    |    |                                   |            |
| 23   | 22 | 21 | 20 | 19 | 18 | 17                                | 16         |
| NU14 |    |    |    |    |    |                                   |            |
| R    |    |    |    |    |    |                                   |            |
| 0h   |    |    |    |    |    |                                   |            |
| 15   | 14 | 13 | 12 | 11 | 10 | 9                                 | 8          |
| NU14 |    |    |    |    |    |                                   |            |
| R    |    |    |    |    |    |                                   |            |
| 0h   |    |    |    |    |    |                                   |            |
| 7    | 6  | 5  | 4  | 3  | 2  | 1                                 | 0          |
| NU14 |    |    |    |    |    | CTRL_EDC_VB<br>USS_ENABLE_<br>CLR | DED_EN_CLR |
| R    |    |    |    |    |    | R/W                               | R/W        |
| 0h   |    |    |    |    |    | 0h                                | 0h         |

**Table 5-2274. ECC\_DED\_ENABLE\_CLR\_REG0 Register Field Descriptions**

| Bit  | Field                         | Type | Reset | Description                                                                                                                                                                                 |
|------|-------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | NU14                          | R    | 0h    | Reserved                                                                                                                                                                                    |
| 1    | CTRL_EDC_VBUSS_ENA<br>BLE_CLR | R/W  | 0h    | Interrupt Enable Clear Register for ctrl_edc_vbuss_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0. |
| 0    | DED_EN_CLR                    | R/W  | 0h    | Interrupt Enable Clear Register for msgmem_pend. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.         |

### 5.12.2.78 ECC\_AGGR\_ENABLE\_SET Register

#### 1 ECC\_AGGR\_ENABLE\_SET Register (Offset = 200h) [reset = 0h]

AGGR interrupt enable set Register.

Return to [Summary Table](#)

**Table 5-2275. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5270 0200h       |
| MCAN1         | 5270 1200h       |
| MCAN2         | 5270 2200h       |
| MCAN3         | 5270 3200h       |

**Figure 5-752. ECC\_AGGR\_ENABLE\_SET Name Register**

|      |    |    |    |    |    |         |        |
|------|----|----|----|----|----|---------|--------|
| 31   | 30 | 29 | 28 | 27 | 26 | 25      | 24     |
| NU15 |    |    |    |    |    |         |        |
| R    |    |    |    |    |    |         |        |
| 0h   |    |    |    |    |    |         |        |
| 23   | 22 | 21 | 20 | 19 | 18 | 17      | 16     |
| NU15 |    |    |    |    |    |         |        |
| R    |    |    |    |    |    |         |        |
| 0h   |    |    |    |    |    |         |        |
| 15   | 14 | 13 | 12 | 11 | 10 | 9       | 8      |
| NU15 |    |    |    |    |    |         |        |
| R    |    |    |    |    |    |         |        |
| 0h   |    |    |    |    |    |         |        |
| 7    | 6  | 5  | 4  | 3  | 2  | 1       | 0      |
| NU15 |    |    |    |    |    | TIMEOUT | PARITY |
| R    |    |    |    |    |    | R/W     | R/W    |
| 0h   |    |    |    |    |    | 0h      | 0h     |

**Table 5-2277. ECC\_AGGR\_ENABLE\_SET Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                             |
|------|---------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | NU15    | R    | 0h    | Reserved                                                                                                                                                |
| 1    | TIMEOUT | R/W  | 0h    | Interrupt Enable Set Register for svbus timeout errors. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field. |
| 0    | PARITY  | R/W  | 0h    | Interrupt Enable Set Register for parity errors. Writing 1 to any bit will set the corresponding bit. Reads do not alter the value of the field.        |

### 5.12.2.79 ECC\_AGGR\_ENABLE\_CLR Register

#### 1 ECC\_AGGR\_ENABLE\_CLR Register (Offset = 204h) [reset = 0h]

AGGR interrupt enable clear Register.

Return to [Summary Table](#)

**Table 5-2278. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5270 0204h       |
| MCAN1         | 5270 1204h       |
| MCAN2         | 5270 2204h       |
| MCAN3         | 5270 3204h       |

**Figure 5-753. ECC\_AGGR\_ENABLE\_CLR Name Register**

|      |    |    |    |    |    |         |        |
|------|----|----|----|----|----|---------|--------|
| 31   | 30 | 29 | 28 | 27 | 26 | 25      | 24     |
| NU16 |    |    |    |    |    |         |        |
| R    |    |    |    |    |    |         |        |
| 0h   |    |    |    |    |    |         |        |
| 23   | 22 | 21 | 20 | 19 | 18 | 17      | 16     |
| NU16 |    |    |    |    |    |         |        |
| R    |    |    |    |    |    |         |        |
| 0h   |    |    |    |    |    |         |        |
| 15   | 14 | 13 | 12 | 11 | 10 | 9       | 8      |
| NU16 |    |    |    |    |    |         |        |
| R    |    |    |    |    |    |         |        |
| 0h   |    |    |    |    |    |         |        |
| 7    | 6  | 5  | 4  | 3  | 2  | 1       | 0      |
| NU16 |    |    |    |    |    | TIMEOUT | PARITY |
| R    |    |    |    |    |    | R/W     | R/W    |
| 0h   |    |    |    |    |    | 0h      | 0h     |

**Table 5-2280. ECC\_AGGR\_ENABLE\_CLR Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                         |
|------|---------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | NU16    | R    | 0h    | Reserved                                                                                                                                                                            |
| 1    | TIMEOUT | R/W  | 0h    | Interrupt Enable Clear for svbus timeout errors. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0. |
| 0    | PARITY  | R/W  | 0h    | Interrupt Enable Clear for parity errors. Writing 1 to any bit will clear the corresponding bits. Reads do not alter the value of the field. Reading this bit will return 0.        |

### 5.12.2.80 ECC\_AGGR\_STATUS\_SET Register

#### 1 ECC\_AGGR\_STATUS\_SET Register (Offset = 208h) [reset = 0h]

AGGR interrupt status set Register.

Return to [Summary Table](#)

**Table 5-2281. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5270 0208h       |
| MCAN1         | 5270 1208h       |
| MCAN2         | 5270 2208h       |
| MCAN3         | 5270 3208h       |

**Figure 5-754. ECC\_AGGR\_STATUS\_SET Name Register**

|      |    |    |    |         |    |        |    |
|------|----|----|----|---------|----|--------|----|
| 31   | 30 | 29 | 28 | 27      | 26 | 25     | 24 |
| NU17 |    |    |    |         |    |        |    |
| R    |    |    |    |         |    |        |    |
| 0h   |    |    |    |         |    |        |    |
| 23   | 22 | 21 | 20 | 19      | 18 | 17     | 16 |
| NU17 |    |    |    |         |    |        |    |
| R    |    |    |    |         |    |        |    |
| 0h   |    |    |    |         |    |        |    |
| 15   | 14 | 13 | 12 | 11      | 10 | 9      | 8  |
| NU17 |    |    |    |         |    |        |    |
| R    |    |    |    |         |    |        |    |
| 0h   |    |    |    |         |    |        |    |
| 7    | 6  | 5  | 4  | 3       | 2  | 1      | 0  |
| NU17 |    |    |    | TIMEOUT |    | PARITY |    |
| R    |    |    |    | R/W     |    | R/W    |    |
| 0h   |    |    |    | 0h      |    | 0h     |    |

**Table 5-2283. ECC\_AGGR\_STATUS\_SET Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|------|---------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | NU17    | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 3:2  | TIMEOUT | R/W  | 0h    | <p>2-bit saturating counter of the number of timeout errors that have occurred since last cleared.</p> <p>2'b00 - No timeout errors have occurred</p> <p>2'b01 - 1 timeout error has occurred</p> <p>2'b10 - 2 timeout error has occurred</p> <p>2'b11 - 3 or more timeout errors have occurred</p> <p>A write of a non-zero value to this register increments that many from the timeout fields. If the value written is less than the current value of the counter, then the pending level interrupt stays asserted. . If this register goes from 0 to non zero a level interrupt will be asserted as well as a pulse interrupt. If the value was non zero to non zero then the level interrupt would remain asserted, but no new pulse interrupt would be asserted. You must write the eoi register to get a new pulse interrupt.</p> |



**Table 5-2283. ECC\_AGGR\_STATUS\_SET Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-----|--------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0 | PARITY | R/W  | 0h    | <p>2-bit saturating counter of the number of parity errors that have occurred since last cleared.</p> <p>2'b00 - No parity errors have occurred</p> <p>2'b01 - 1 parity error has occurred</p> <p>2'b10 - 2 parity error has occurred</p> <p>2'b11 - 3 or more parity error have occurred</p> <p>A write of a non-zero value to this register increments that many from the parity fields. If the value written is less than the current value of the counter, then the pending level interrupt stays asserted. If this register goes from 0 to non zero a level interrupt will be asserted as well as a pulse interrupt. If the value was non zero to non zero then the level interrupt would remain asserted, but no new pulse interrupt would be asserted. You must write the eoi register to get a new pulse interrupt.</p> |

### 5.12.2.81 ECC\_AGGR\_STATUS\_CLR Register

#### 1 ECC\_AGGR\_STATUS\_CLR Register (Offset = 20Ch) [reset = 0h]

AGGR interrupt status clear Register.

Return to [Summary Table](#)

**Table 5-2284. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCAN0         | 5270 020Ch       |
| MCAN1         | 5270 120Ch       |
| MCAN2         | 5270 220Ch       |
| MCAN3         | 5270 320Ch       |

**Figure 5-755. ECC\_AGGR\_STATUS\_CLR Name Register**

|      |    |    |    |         |    |        |    |
|------|----|----|----|---------|----|--------|----|
| 31   | 30 | 29 | 28 | 27      | 26 | 25     | 24 |
| NU18 |    |    |    |         |    |        |    |
| R    |    |    |    |         |    |        |    |
| 0h   |    |    |    |         |    |        |    |
| 23   | 22 | 21 | 20 | 19      | 18 | 17     | 16 |
| NU18 |    |    |    |         |    |        |    |
| R    |    |    |    |         |    |        |    |
| 0h   |    |    |    |         |    |        |    |
| 15   | 14 | 13 | 12 | 11      | 10 | 9      | 8  |
| NU18 |    |    |    |         |    |        |    |
| R    |    |    |    |         |    |        |    |
| 0h   |    |    |    |         |    |        |    |
| 7    | 6  | 5  | 4  | 3       | 2  | 1      | 0  |
| NU18 |    |    |    | TIMEOUT |    | PARITY |    |
| R    |    |    |    | R/W     |    | R/W    |    |
| 0h   |    |    |    | 0h      |    | 0h     |    |

**Table 5-2286. ECC\_AGGR\_STATUS\_CLR Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|---------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | NU18    | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 3:2  | TIMEOUT | R/W  | 0h    | 2'b00 - No timeout errors have occurred<br>2'b01 - 1 timeout erro has occurred<br>2'b10 - 2 timeout error has occurred<br>2'b11 - 3 or more timeout errors have occurred<br>A write of a non-zero value to this register decrements that many from the timeout fields. If the resulting written value is non zero, then the pending level interrupt stays asserted. A new pulse interrupt will nto be asserted, you must write the eoi register for that to occur. If you write a value more than the counter value the result will be zero. |
| 1:0  | PARITY  | R/W  | 0h    | 2'b00 - No parity errors have occurred<br>2'b01 - 1 parity error has occurred<br>2'b10 - 2 parity error has occurred<br>2'b11 - 3 or more parity error have occurred<br>A write of a non-zero value to this register decrements that many from the parity fields. If the resulting written value is non zero, then the pending level interrupt stays asserted. A new pulse interrupt will nto be asserted, you must write the eoi register for that to occur. If you write a value more than the counter value the result will be zero.      |

## 5.13 MCRC

### MCRC

#### 5.13.1 MCRC Summaries

#### MCRC Summaries

**Table 5-2287. MSS\_MCRC Registers, Base Address=3500 0000h, Length=1024**

| Offset | Length | Register Name                               | MCRC0 Physical Address |
|--------|--------|---------------------------------------------|------------------------|
| 0h     | 32     | <a href="#">MSS_MCRC_CRC_CTRL0</a>          | 3500 0000h             |
| 8h     | 32     | <a href="#">MSS_MCRC_CRC_CTRL1</a>          | 3500 0008h             |
| 10h    | 32     | <a href="#">MSS_MCRC_CRC_CTRL2</a>          | 3500 0010h             |
| 18h    | 32     | <a href="#">MSS_MCRC_CRC_INTS</a>           | 3500 0018h             |
| 20h    | 32     | <a href="#">MSS_MCRC_CRC_INTR</a>           | 3500 0020h             |
| 28h    | 32     | <a href="#">MSS_MCRC_CRC_STATUS_REG</a>     | 3500 0028h             |
| 30h    | 32     | <a href="#">MSS_MCRC_CRC_INT_OFFSET_REG</a> | 3500 0030h             |
| 38h    | 32     | <a href="#">MSS_MCRC_CRC_BUSY</a>           | 3500 0038h             |
| 40h    | 32     | <a href="#">MSS_MCRC_CRC_PCOUNT_REG1</a>    | 3500 0040h             |
| 44h    | 32     | <a href="#">MSS_MCRC_CRC_SCOUNT_REG1</a>    | 3500 0044h             |
| 48h    | 32     | <a href="#">MSS_MCRC_CRC_CURSEC_REG1</a>    | 3500 0048h             |
| 4Ch    | 32     | <a href="#">MSS_MCRC_CRC_WDTPLD1</a>        | 3500 004Ch             |
| 50h    | 32     | <a href="#">MSS_MCRC_CRC_BCTOPLD1</a>       | 3500 0050h             |
| 60h    | 32     | <a href="#">MSS_MCRC_PSA_SIGREGL1</a>       | 3500 0060h             |
| 64h    | 32     | <a href="#">MSS_MCRC_PSA_SIGREGH1</a>       | 3500 0064h             |
| 68h    | 32     | <a href="#">MSS_MCRC_CRC_REGL1</a>          | 3500 0068h             |
| 6Ch    | 32     | <a href="#">MSS_MCRC_CRC_REGH1</a>          | 3500 006Ch             |
| 70h    | 32     | <a href="#">MSS_MCRC_PSA_SECSIGREGL1</a>    | 3500 0070h             |
| 74h    | 32     | <a href="#">MSS_MCRC_PSA_SECSIGREGH1</a>    | 3500 0074h             |
| 78h    | 32     | <a href="#">MSS_MCRC_RAW_DATAAREGL1</a>     | 3500 0078h             |
| 7Ch    | 32     | <a href="#">MSS_MCRC_RAW_DATAAREGH1</a>     | 3500 007Ch             |
| 80h    | 32     | <a href="#">MSS_MCRC_CRC_PCOUNT_REG2</a>    | 3500 0080h             |
| 84h    | 32     | <a href="#">MSS_MCRC_CRC_SCOUNT_REG2</a>    | 3500 0084h             |
| 88h    | 32     | <a href="#">MSS_MCRC_CRC_CURSEC_REG2</a>    | 3500 0088h             |
| 8Ch    | 32     | <a href="#">MSS_MCRC_CRC_WDTPLD2</a>        | 3500 008Ch             |
| 90h    | 32     | <a href="#">MSS_MCRC_CRC_BCTOPLD2</a>       | 3500 0090h             |
| A0h    | 32     | <a href="#">MSS_MCRC_PSA_SIGREGL2</a>       | 3500 00A0h             |
| A4h    | 32     | <a href="#">MSS_MCRC_PSA_SIGREGH2</a>       | 3500 00A4h             |
| A8h    | 32     | <a href="#">MSS_MCRC_CRC_REGL2</a>          | 3500 00A8h             |
| ACh    | 32     | <a href="#">MSS_MCRC_CRC_REGH2</a>          | 3500 00ACh             |
| B0h    | 32     | <a href="#">MSS_MCRC_PSA_SECSIGREGL2</a>    | 3500 00B0h             |
| B4h    | 32     | <a href="#">MSS_MCRC_PSA_SECSIGREGH2</a>    | 3500 00B4h             |
| B8h    | 32     | <a href="#">MSS_MCRC_RAW_DATAAREGL2</a>     | 3500 00B8h             |
| BCh    | 32     | <a href="#">MSS_MCRC_RAW_DATAAREGH2</a>     | 3500 00BCh             |
| C0h    | 32     | <a href="#">MSS_MCRC_CRC_PCOUNT_REG3</a>    | 3500 00C0h             |
| C4h    | 32     | <a href="#">MSS_MCRC_CRC_SCOUNT_REG3</a>    | 3500 00C4h             |
| C8h    | 32     | <a href="#">MSS_MCRC_CRC_CURSEC_REG3</a>    | 3500 00C8h             |
| CCh    | 32     | <a href="#">MSS_MCRC_CRC_WDTPLD3</a>        | 3500 00CCh             |

**Table 5-2287. MSS\_MCRC Registers, Base Address=3500 0000h, Length=1024 (continued)**

| Offset | Length | Register Name                            | MCRC0 Physical Address |
|--------|--------|------------------------------------------|------------------------|
| D0h    | 32     | <a href="#">MSS_MCRC_CRC_BCTOPLD3</a>    | 3500 00D0h             |
| E0h    | 32     | <a href="#">MSS_MCRC_PSA_SIGREGL3</a>    | 3500 00E0h             |
| E4h    | 32     | <a href="#">MSS_MCRC_PSA_SIGREGH3</a>    | 3500 00E4h             |
| E8h    | 32     | <a href="#">MSS_MCRC_CRC_REGL3</a>       | 3500 00E8h             |
| ECh    | 32     | <a href="#">MSS_MCRC_CRC_REGH3</a>       | 3500 00ECh             |
| F0h    | 32     | <a href="#">MSS_MCRC_PSA_SECSIGREGL3</a> | 3500 00F0h             |
| F4h    | 32     | <a href="#">MSS_MCRC_PSA_SECSIGREGH3</a> | 3500 00F4h             |
| F8h    | 32     | <a href="#">MSS_MCRC_RAW_DATAAREGL3</a>  | 3500 00F8h             |
| FCh    | 32     | <a href="#">MSS_MCRC_RAW_DATAAREGH3</a>  | 3500 00FCh             |
| 100h   | 32     | <a href="#">MSS_MCRC_CRC_PCOUNT_REG4</a> | 3500 0100h             |
| 104h   | 32     | <a href="#">MSS_MCRC_CRC_SCOUNT_REG4</a> | 3500 0104h             |
| 108h   | 32     | <a href="#">MSS_MCRC_CRC_CURSEC_REG4</a> | 3500 0108h             |
| 10Ch   | 32     | <a href="#">MSS_MCRC_CRC_WDTPD4</a>      | 3500 010Ch             |
| 110h   | 32     | <a href="#">MSS_MCRC_CRC_BCTOPLD4</a>    | 3500 0110h             |
| 120h   | 32     | <a href="#">MSS_MCRC_PSA_SIGREGL4</a>    | 3500 0120h             |
| 124h   | 32     | <a href="#">MSS_MCRC_PSA_SIGREGH4</a>    | 3500 0124h             |
| 128h   | 32     | <a href="#">MSS_MCRC_CRC_REGL4</a>       | 3500 0128h             |
| 12Ch   | 32     | <a href="#">MSS_MCRC_CRC_REGH4</a>       | 3500 012Ch             |
| 130h   | 32     | <a href="#">MSS_MCRC_PSA_SECSIGREGL4</a> | 3500 0130h             |
| 134h   | 32     | <a href="#">MSS_MCRC_PSA_SECSIGREGH4</a> | 3500 0134h             |
| 138h   | 32     | <a href="#">MSS_MCRC_RAW_DATAAREGL4</a>  | 3500 0138h             |
| 13Ch   | 32     | <a href="#">MSS_MCRC_RAW_DATAAREGH4</a>  | 3500 013Ch             |
| 140h   | 32     | <a href="#">MSS_MCRC_MCRC_BUS_SEL</a>    | 3500 0140h             |

### 5.13.2 MCRC Registers

#### MCRC Registers

### 5.13.2.1 MSS\_MCRC\_CRC\_CTRL0 Register

#### 1 MSS\_MCRC\_CRC\_CTRL0 Register (Offset = 0h) [reset = 0h]

Contains sw reset control bit to reset PSA.

Return to [Summary Table](#)

**Table 5-2288. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0000h       |

**Figure 5-756. MSS\_MCRC\_CRC\_CTRL0 Name Register**

| 31               | 30                | 29               | 28          | 27 | 26         | 25 | 24                 |
|------------------|-------------------|------------------|-------------|----|------------|----|--------------------|
| CH4_CRC_SEL<br>2 | CH4_BYTE_S<br>WAP | CH4_BIT_SWA<br>P | CH4_CRC_SEL |    | CH4_DW_SEL |    | CH4_PSA_SW<br>REST |
| R/W              | R/W               | R/W              | R/W         |    | R/W        |    | R/W                |
| 0h               | 0h                | 0h               | 0h          |    | 0h         |    | 0h                 |
| 23               | 22                | 21               | 20          | 19 | 18         | 17 | 16                 |
| CH3_CRC_SEL<br>2 | CH3_BYTE_S<br>WAP | CH3_BIT_SWA<br>P | CH3_CRC_SEL |    | CH3_DW_SEL |    | CH3_PSA_SW<br>REST |
| R/W              | R/W               | R/W              | R/W         |    | R/W        |    | R/W                |
| 0h               | 0h                | 0h               | 0h          |    | 0h         |    | 0h                 |
| 15               | 14                | 13               | 12          | 11 | 10         | 9  | 8                  |
| CH2_CRC_SEL<br>2 | CH2_BYTE_S<br>WAP | CH2_BIT_SWA<br>P | CH2_CRC_SEL |    | CH2_DW_SEL |    | CH2_PSA_SW<br>REST |
| R/W              | R/W               | R/W              | R/W         |    | R/W        |    | R/W                |
| 0h               | 0h                | 0h               | 0h          |    | 0h         |    | 0h                 |
| 7                | 6                 | 5                | 4           | 3  | 2          | 1  | 0                  |
| CH1_CRC_SEL<br>2 | CH1_BYTE_S<br>WAP | CH1_BIT_SWA<br>P | CH1_CRC_SEL |    | CH1_DW_SEL |    | CH1_PSA_SW<br>REST |
| R/W              | R/W               | R/W              | R/W         |    | R/W        |    | R/W                |
| 0h               | 0h                | 0h               | 0h          |    | 0h         |    | 0h                 |

**Table 5-2290. MSS\_MCRC\_CRC\_CTRL0 Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                                                                                      |
|-------|---------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31    | CH4_CRC_SEL2  | R/W  | 0h    | Refer "CH4_DW_SEL" field description                                                                                                                                                                             |
| 30    | CH4_BYTE_SWAP | R/W  | 0h    | BYTE SWAP Enable across Data Size<br>0 Byte Swap Disabled<br>1 Byte Swap enabled.                                                                                                                                |
| 29    | CH4_BIT_SWAP  | R/W  | 0h    | msb/lbs SWAPPING<br>0 msb [most significant bit First]<br>1 lsb [least significant bit First]                                                                                                                    |
| 28:27 | CH4_CRC_SEL   | R/W  | 0h    | CRC type select. {CH1_CRC_SEL2,CH1_CRC_SEL[1:0]}<br>000 CRC-64<br>001 - CRC-16<br>010 CRC-32<br>100 - VDA CAN, SAE-J1850 CRC-8<br>101 - H2F, Autosar 4.0<br>110 - CASTAGNOLI, iSCSI<br>111 / 011 - E2E Profile 4 |
| 26:25 | CH4_DW_SEL    | R/W  | 0h    | CRC Data Size select.<br>000 64 bit Data Size<br>001 - 16 bit Data Size<br>010 32 Bit Data Size                                                                                                                  |

**Table 5-2290. MSS\_MCRC\_CRC\_CTRL0 Register Field Descriptions (continued)**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                |
|-------|----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24    | CH4_PSA_SWREST | R/W  | 0h    | Channel 4 PSA Software Reset. When set, the PSA Signature Register is reset to all zero. Software reset does not reset software reset bit itself. Therefore, CPU is required to clear this bit by Writing a 0.<br>0 = PSA Signature Register not reset<br>1 = PSA Signature Register reset |
| 23    | CH3_CRC_SEL2   | R/W  | 0h    | Refer "CH3_DW_SEL" field description                                                                                                                                                                                                                                                       |
| 22    | CH3_BYTE_SWAP  | R/W  | 0h    | BYTE SWAP Enable across Data Size<br>0 Byte Swap Disabled<br>1 Byte Swap enabled.                                                                                                                                                                                                          |
| 21    | CH3_BIT_SWAP   | R/W  | 0h    | msb/lbs SWAPPING<br>0 msb [most significant bit First]<br>1 lsb [least significant bit First]                                                                                                                                                                                              |
| 20:19 | CH3_CRC_SEL    | R/W  | 0h    | CRC type select. {CH1_CRC_SEL2,CH1_CRC_SEL[1:0]}<br>000 CRC-64<br>001 - CRC-16<br>010 CRC-32<br>100 - VDA CAN, SAE-J1850 CRC-8<br>101 - H2F, Autosar 4.0<br>110 - CASTAGNOLI, iSCSI<br>111 / 011 - E2E Profile 4                                                                           |
| 18:17 | CH3_DW_SEL     | R/W  | 0h    | CRC Data Size select.<br>000 64 bit Data Size<br>001 - 16 bit Data Size<br>010 32 Bit Data Size                                                                                                                                                                                            |
| 16    | CH3_PSA_SWREST | R/W  | 0h    | Channel 3 PSA Software Reset. When set, the PSA Signature Register is reset to all zero. Software reset does not reset software reset bit itself. Therefore, CPU is required to clear this bit by Writing a 0.<br>0 = PSA Signature Register not reset<br>1 = PSA Signature Register reset |
| 15    | CH2_CRC_SEL2   | R/W  | 0h    | Refer "CH2_DW_SEL" field description                                                                                                                                                                                                                                                       |
| 14    | CH2_BYTE_SWAP  | R/W  | 0h    | BYTE SWAP Enable across Data Size<br>0 Byte Swap Disabled<br>1 Byte Swap enabled.                                                                                                                                                                                                          |
| 13    | CH2_BIT_SWAP   | R/W  | 0h    | msb/lbs SWAPPING<br>0 msb [most significant bit First]<br>1 lsb [least significant bit First]                                                                                                                                                                                              |
| 12:11 | CH2_CRC_SEL    | R/W  | 0h    | CRC type select. {CH1_CRC_SEL2,CH1_CRC_SEL[1:0]}<br>000 CRC-64<br>001 - CRC-16<br>010 CRC-32<br>100 - VDA CAN, SAE-J1850 CRC-8<br>101 - H2F, Autosar 4.0<br>110 - CASTAGNOLI, iSCSI<br>111 / 011 - E2E Profile 4                                                                           |
| 10:9  | CH2_DW_SEL     | R/W  | 0h    | CRC Data Size select.<br>000 64 bit Data Size<br>001 - 16 bit Data Size<br>010 32 Bit Data Size                                                                                                                                                                                            |
| 8     | CH2_PSA_SWREST | R/W  | 0h    | Channel 2 PSA Software Reset. When set, the PSA Signature Register is reset to all zero. Software reset does not reset software reset bit itself. Therefore, CPU is required to clear this bit by Writing a 0.<br>0 = PSA Signature Register not reset<br>1 = PSA Signature Register reset |
| 7     | CH1_CRC_SEL2   | R/W  | 0h    | Refer "CH1_DW_SEL" field description                                                                                                                                                                                                                                                       |

**Table 5-2290. MSS\_MCRC\_CRC\_CTRL0 Register Field Descriptions (continued)**

| Bit | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                |
|-----|----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6   | CH1_BYTE_SWAP  | R/W  | 0h    | BYTE SWAP Enable across Data Size<br>0 Byte Swap Disabled<br>1 Byte Swap enabled.                                                                                                                                                                                                          |
| 5   | CH1_BIT_SWAP   | R/W  | 0h    | msb/lbs SWAPPING<br>0 msb [most significant bit First]<br>1 lsb [least significant bit First]                                                                                                                                                                                              |
| 4:3 | CH1_CRC_SEL    | R/W  | 0h    | CRC type select. {CH1_CRC_SEL2,CH1_CRC_SEL[1:0]}<br>000 CRC-64<br>001 - CRC-16<br>010 CRC-32<br>100 - VDA CAN, SAE-J1850 CRC-8<br>101 - H2F, Autosar 4.0<br>110 - CASTAGNOLI, iSCSI<br>111 / 011 - E2E Profile 4                                                                           |
| 2:1 | CH1_DW_SEL     | R/W  | 0h    | CRC Data Size select.<br>000 64 bit Data Size<br>001 - 16 bit Data Size<br>010 32 Bit Data Size                                                                                                                                                                                            |
| 0   | CH1_PSA_SWREST | R/W  | 0h    | Channel 1 PSA Software Reset. When set, the PSA Signature Register is reset to all zero. Software reset does not reset software reset bit itself. Therefore, CPU is required to clear this bit by Writing a 0.<br>0 = PSA Signature Register not reset<br>1 = PSA Signature Register reset |

### 5.13.2.2 MSS\_MCRC\_CRC\_CTRL1 Register

#### 1 MSS\_MCRC\_CRC\_CTRL1 Register (Offset = 8h) [reset = 0h]

Contains power down control bit.

Return to [Summary Table](#)

**Table 5-2291. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0008h       |

**Figure 5-757. MSS\_MCRC\_CRC\_CTRL1 Name Register**

|           |    |    |    |    |    |    |      |
|-----------|----|----|----|----|----|----|------|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24   |
| RESERVED1 |    |    |    |    |    |    |      |
| R         |    |    |    |    |    |    |      |
| 0h        |    |    |    |    |    |    |      |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16   |
| RESERVED1 |    |    |    |    |    |    |      |
| R         |    |    |    |    |    |    |      |
| 0h        |    |    |    |    |    |    |      |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8    |
| RESERVED1 |    |    |    |    |    |    |      |
| R         |    |    |    |    |    |    |      |
| 0h        |    |    |    |    |    |    |      |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0    |
| RESERVED1 |    |    |    |    |    |    | PWDN |
| R         |    |    |    |    |    |    | R/W  |
| 0h        |    |    |    |    |    |    | 0h   |

**Table 5-2293. MSS\_MCRC\_CRC\_CTRL1 Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                     |
|------|-----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED1 | R    | 0h    |                                                                                                                                                 |
| 0    | PWDN      | R/W  | 0h    | Power Down. When set, MCRC moduleMCRC Module is put in power down mode.<br>0 = MCRC is not in power down mode<br>1 = MCRC is in power down mode |



### 5.13.2.3 MSS\_MCRC\_CRC\_CTRL2 Register

#### 1 MSS\_MCRC\_CRC\_CTRL2 Register (Offset = 10h) [reset = 0h]

Contains channel mode, data trace enable control bits.

Return to [Summary Table](#)

**Table 5-2294. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0010h       |

**Figure 5-758. MSS\_MCRC\_CRC\_CTRL2 Name Register**

| 31        | 30 | 29 | 28              | 27        | 26 | 25       | 24 |
|-----------|----|----|-----------------|-----------|----|----------|----|
| RESERVED5 |    |    |                 |           |    | CH4_MODE |    |
| R         |    |    |                 |           |    | R/W      |    |
| 0h        |    |    |                 |           |    | 0h       |    |
| 23        | 22 | 21 | 20              | 19        | 18 | 17       | 16 |
| RESERVED4 |    |    |                 |           |    | CH3_MODE |    |
| R         |    |    |                 |           |    | R/W      |    |
| 0h        |    |    |                 |           |    | 0h       |    |
| 15        | 14 | 13 | 12              | 11        | 10 | 9        | 8  |
| RESERVED3 |    |    |                 |           |    | CH2_MODE |    |
| R         |    |    |                 |           |    | R/W      |    |
| 0h        |    |    |                 |           |    | 0h       |    |
| 7         | 6  | 5  | 4               | 3         | 2  | 1        | 0  |
| RESERVED2 |    |    | CH1_TRACEE<br>N | RESERVED1 |    | CH1_MODE |    |
| R         |    |    | R/W             | R         |    | R/W      |    |
| 0h        |    |    | 0h              | 0h        |    | 0h       |    |

**Table 5-2296. MSS\_MCRC\_CRC\_CTRL2 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                  |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:26 | RESERVED5 | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                              |
| 25:24 | CH4_MODE  | R/W  | 0h    | Channel 4 Mode:<br>0 0 = Data Capture mode. In this mode, the PSA Signature Register does not compress data when it is written. Any data written to PSA Signature Register is simply captured by PSA Signature Register without any compression. This mode can be used to plant seed value into the PSA register<br>0 1 = AUTO mode<br>1 0 = reserved<br>1 1 = Full-CPU mode |
| 23:18 | RESERVED4 | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                              |
| 17:16 | CH3_MODE  | R/W  | 0h    | Channel 3 Mode:<br>0 0 = Data Capture mode. In this mode, the PSA Signature Register does not compress data when it is written. Any data written to PSA Signature Register is simply captured by PSA Signature Register without any compression. This mode can be used to plant seed value into the PSA register<br>0 1 = AUTO mode<br>1 0 = reserved<br>1 1 = Full-CPU mode |
| 15:10 | RESERVED3 | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                              |

**Table 5-2296. MSS\_MCRC\_CRC\_CTRL2 Register Field Descriptions (continued)**

| Bit | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                 |
|-----|-------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9:8 | CH2_MODE    | R/W  | 0h    | Channel 2 Mode:<br>0 0 = Data Capture mode. In this mode, the PSA Signature Register does not compress data when it is written. Any data written to PSA Signature Register is simply captured by PSA Signature Register without any compression. This mode can be used to plant seed value into the PSA register<br>0 1 = AUTO mode<br>1 0 = reserved<br>1 1 = Full-CPU mode                |
| 7:5 | RESERVED2   | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                             |
| 4   | CH1_TRACEEN | R/W  | 0h    | Channel 1 Data Trace Enable. When set, the channel is put into data trace mode. The channel snoops on the CPU VBUSM, ITCM, DTCM buses for any read transaction. Any read data on these buses is compressed by the PSA Signature Register. When suspend is on, the PSA Signature Register does not compress any read data on these buses.<br>0 = Data Trace disable<br>1 = Data Trace enable |
| 3:2 | RESERVED1   | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                             |
| 1:0 | CH1_MODE    | R/W  | 0h    | Channel 1 Mode:<br>0 0 = Data Capture mode. In this mode, the PSA Signature Register does not compress data when it is written. Any data written to PSA Signature Register is simply captured by PSA Signature Register without any compression. This mode can be used to plant seed value into the PSA register<br>0 1 = AUTO mode<br>1 0 = reserved<br>1 1 = Full-CPU mode                |

### 5.13.2.4 MSS\_MCRC\_CRC\_INTS Register

#### 1 MSS\_MCRC\_CRC\_INTS Register (Offset = 18h) [reset = 0h]

CRC interrupt enable register. Write one to a bit to enable a interrupt.

Return to [Summary Table](#)

**Table 5-2297. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0018h       |

**Figure 5-759. MSS\_MCRC\_CRC\_INTS Name Register**

| 31        | 30 | 29 | 28                 | 27               | 26              | 25                 | 24        |
|-----------|----|----|--------------------|------------------|-----------------|--------------------|-----------|
| RESERVED5 |    |    | CH4_TIMEOUT<br>ENS | CH4_UNDERE<br>NS | CH4_OVEREN<br>S | CH4_CRCFAIL<br>ENS | RESERVED4 |
| R         |    |    | R/W                | R/W              | R/W             | R/W                | R         |
| 0h        |    |    | 0h                 | 0h               | 0h              | 0h                 | 0h        |
| 23        | 22 | 21 | 20                 | 19               | 18              | 17                 | 16        |
| RESERVED4 |    |    | CH3_TIMEOUT<br>ENS | CH3_UNDERE<br>NS | CH3_OVEREN<br>S | CH3_CRCFAIL<br>ENS | RESERVED3 |
| R         |    |    | R/W                | R/W              | R/W             | R/W                | R         |
| 0h        |    |    | 0h                 | 0h               | 0h              | 0h                 | 0h        |
| 15        | 14 | 13 | 12                 | 11               | 10              | 9                  | 8         |
| RESERVED3 |    |    | CH2_TIMEOUT<br>ENS | CH2_UNDERE<br>NS | CH2_OVEREN<br>S | CH2_CRCFAIL<br>ENS | RESERVED2 |
| R         |    |    | R/W                | R/W              | R/W             | R/W                | R         |
| 0h        |    |    | 0h                 | 0h               | 0h              | 0h                 | 0h        |
| 7         | 6  | 5  | 4                  | 3                | 2               | 1                  | 0         |
| RESERVED2 |    |    | CH1_TIMEOUT<br>ENS | CH1_UNDERE<br>NS | CH1_OVEREN<br>S | CH1_CRCFAIL<br>ENS | RESERVED1 |
| R         |    |    | R/W                | R/W              | R/W             | R/W                | R         |
| 0h        |    |    | 0h                 | 0h               | 0h              | 0h                 | 0h        |

**Table 5-2299. MSS\_MCRC\_CRC\_INTS Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED5      | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                               |
| 28    | CH4_TIMEOUTENS | R/W  | 0h    | Channel 4 Timeout Interrupt Enable Bit. Writing a one to this bit enable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read:<br>0 = Timeout Interrupt disable<br>1 = Timeout Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = Timeout Interrupt enable      |
| 27    | CH4_UNDERENS   | R/W  | 0h    | Channel 4 Underrun Interrupt Enable Bit. Writing a one to this bit enable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read:<br>0 = Underrun Interrupt disable<br>1 = Underrun Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = Underrun Interrupt enable |

**Table 5-2299. MSS\_MCRC\_CRC\_INTS Register Field Descriptions (continued)**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26    | CH4_OVERENS    | R/W  | 0h    | Channel 4 Overrun Interrupt Enable Bit. Writing a one to this bit enable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read:<br>0 = Overrun Interrupt disable<br>1 = Overrun Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = Overrun Interrupt enable      |
| 25    | CH4_CRCFAILENS | R/W  | 0h    | Channel 4 CRC Fail Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read:<br>0 = CRC Fail Interrupt disable<br>1 = CRC Fail Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = CRC Fail Interrupt enable |
| 24:21 | RESERVED4      | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                               |
| 20    | CH3_TIMEOUTENS | R/W  | 0h    | Channel 3 Timeout Interrupt Enable Bit. Writing a one to this bit enable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read:<br>0 = Timeout Interrupt disable<br>1 = Timeout Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = Timeout Interrupt enable      |
| 19    | CH3_UNDERENS   | R/W  | 0h    | Channel 3 Underrun Interrupt Enable Bit. Writing a one to this bit enable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read:<br>0 = Underrun Interrupt disable<br>1 = Underrun Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = Underrun Interrupt enable |
| 18    | CH3_OVERENS    | R/W  | 0h    | Channel 3 Overrun Interrupt Enable Bit. Writing a one to this bit enable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read:<br>0 = Overrun Interrupt disable<br>1 = Overrun Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = Overrun Interrupt enable      |
| 17    | CH3_CRCFAILENS | R/W  | 0h    | Channel 3 CRC Fail Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read:<br>0 = CRC Fail Interrupt disable<br>1 = CRC Fail Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = CRC Fail Interrupt enable |
| 16:13 | RESERVED3      | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                               |

**Table 5-2299. MSS\_MCRC\_CRC\_INTS Register Field Descriptions (continued)**

| Bit | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                   |
|-----|----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12  | CH2_TIMEOUTENS | R/W  | 0h    | Channel 2 Timeout Interrupt Enable Bit. Writing a one to this bit enable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read:<br>0 = Timeout Interrupt disable<br>1 = Timeout Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = Timeout Interrupt enable      |
| 11  | CH2_UNDERENS   | R/W  | 0h    | Channel 2 Underrun Interrupt Enable Bit. Writing a one to this bit enable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read:<br>0 = Underrun Interrupt disable<br>1 = Underrun Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = Underrun Interrupt enable |
| 10  | CH2_OVERENS    | R/W  | 0h    | Channel 2 Overrun Interrupt Enable Bit. Writing a one to this bit enable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read:<br>0 = Overrun Interrupt disable<br>1 = Overrun Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = Overrun Interrupt enable      |
| 9   | CH2_CRCFAILENS | R/W  | 0h    | Channel 2 CRC Fail Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read:<br>0 = CRC Fail Interrupt disable<br>1 = CRC Fail Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = CRC Fail Interrupt enable |
| 8:5 | RESERVED2      | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                               |
| 4   | CH1_TIMEOUTENS | R/W  | 0h    | Channel 1 Timeout Interrupt Enable Bit. Writing a one to this bit enable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read:<br>0 = Timeout Interrupt disable<br>1 = Timeout Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = Timeout Interrupt enable      |
| 3   | CH1_UNDERENS   | R/W  | 0h    | Channel 1 Underrun Interrupt Enable Bit. Writing a one to this bit enable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read:<br>0 = Underrun Interrupt disable<br>1 = Underrun Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = Underrun Interrupt enable |

**Table 5-2299. MSS\_MCRC\_CRC\_INTS Register Field Descriptions (continued)**

| Bit | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                   |
|-----|----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | CH1_OVERENS    | R/W  | 0h    | Channel 1 Overrun Interrupt Enable Bit. Writing a one to this bit enable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read:<br>0 = Overrun Interrupt disable<br>1 = Overrun Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = Overrun Interrupt enable      |
| 1   | CH1_CRCFAILENS | R/W  | 0h    | Channel 1 CRC Fail Interrupt Enable Bit. Writing a one to this bit enable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read:<br>0 = CRC Fail Interrupt disable<br>1 = CRC Fail Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = CRC Fail Interrupt enable |
| 0   | RESERVED1      | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                               |

### 5.13.2.5 MSS\_MCRC\_CRC\_INTR Register

#### 1 MSS\_MCRC\_CRC\_INTR Register (Offset = 20h) [reset = 0h]

CRC interrupt disable register. Write one to a bit to disable a interrupt.

Return to [Summary Table](#)

**Table 5-2300. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0020h       |

**Figure 5-760. MSS\_MCRC\_CRC\_INTR Name Register**

| 31        | 30 | 29 | 28                 | 27               | 26              | 25                 | 24        |
|-----------|----|----|--------------------|------------------|-----------------|--------------------|-----------|
| RESERVED5 |    |    | CH4_TIMEOUT<br>ENR | CH4_UNDERE<br>NR | CH4_OVEREN<br>R | CH4_CRCFAIL<br>ENR | RESERVED4 |
| R         |    |    | R/W                | R/W              | R/W             | R/W                | R         |
| 0h        |    |    | 0h                 | 0h               | 0h              | 0h                 | 0h        |
| 23        | 22 | 21 | 20                 | 19               | 18              | 17                 | 16        |
| RESERVED4 |    |    | CH3_TIMEOUT<br>ENR | CH3_UNDERE<br>NR | CH3_OVEREN<br>R | CH3_CRCFAIL<br>ENR | RESERVED3 |
| R         |    |    | R/W                | R/W              | R/W             | R/W                | R         |
| 0h        |    |    | 0h                 | 0h               | 0h              | 0h                 | 0h        |
| 15        | 14 | 13 | 12                 | 11               | 10              | 9                  | 8         |
| RESERVED3 |    |    | CH2_TIMEOUT<br>ENR | CH2_UNDERE<br>NR | CH2_OVEREN<br>R | CH2_CRCFAIL<br>ENR | RESERVED2 |
| R         |    |    | R/W                | R/W              | R/W             | R/W                | R         |
| 0h        |    |    | 0h                 | 0h               | 0h              | 0h                 | 0h        |
| 7         | 6  | 5  | 4                  | 3                | 2               | 1                  | 0         |
| RESERVED2 |    |    | CH1_TIMEOUT<br>ENR | CH1_UNDERE<br>NR | CH1_OVEREN<br>R | CH1_CRCFAIL<br>ENR | RESERVED1 |
| R         |    |    | R/W                | R/W              | R/W             | R/W                | R         |
| 0h        |    |    | 0h                 | 0h               | 0h              | 0h                 | 0h        |

**Table 5-2302. MSS\_MCRC\_CRC\_INTR Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED5      | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                  |
| 28    | CH4_TIMEOUTENR | R/W  | 0h    | Channel 4 Timeout Interrupt Disable Bit. Writing a one to this bit disable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read:<br>0 = Timeout Interrupt disable<br>1 = Timeout Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = Timeout Interrupt disable      |
| 27    | CH4_UNDERENR   | R/W  | 0h    | Channel 4 Underrun Interrupt Disable Bit. Writing a one to this bit disable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read:<br>0 = Underrun Interrupt disable<br>1 = Underrun Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = Underrun Interrupt disable |

**Table 5-2302. MSS\_MCRC\_CRC\_INTR Register Field Descriptions (continued)**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26    | CH4_OVERENR    | R/W  | 0h    | Channel 4 Overrun Interrupt Disable Bit. Writing a one to this bit disable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read:<br>0 = Overrun Interrupt disable<br>1 = Overrun Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = Overrun Interrupt disable      |
| 25    | CH4_CRCFAILENR | R/W  | 0h    | Channel 4 CRC Fail Interrupt Disable Bit. Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read:<br>0 = CRC Fail Interrupt disable<br>1 = CRC Fail Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = CRC Fail Interrupt disable |
| 24:21 | RESERVED4      | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                  |
| 20    | CH3_TIMEOUTENR | R/W  | 0h    | Channel 3 Timeout Interrupt Disable Bit. Writing a one to this bit disable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read:<br>0 = Timeout Interrupt disable<br>1 = Timeout Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = Timeout Interrupt disable      |
| 19    | CH3_UNDERENR   | R/W  | 0h    | Channel 3 Underrun Interrupt Disable Bit. Writing a one to this bit disable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read:<br>0 = Underrun Interrupt disable<br>1 = Underrun Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = Underrun Interrupt disable |
| 18    | CH3_OVERENR    | R/W  | 0h    | Channel 3 Overrun Interrupt Disable Bit. Writing a one to this bit disable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read:<br>0 = Overrun Interrupt disable<br>1 = Overrun Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = Overrun Interrupt disable      |
| 17    | CH3_CRCFAILENR | R/W  | 0h    | Channel 3 CRC Fail Interrupt Disable Bit. Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read:<br>0 = CRC Fail Interrupt disable<br>1 = CRC Fail Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = CRC Fail Interrupt disable |
| 16:13 | RESERVED3      | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                  |



**Table 5-2302. MSS\_MCRC\_CRC\_INTR Register Field Descriptions (continued)**

| Bit | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12  | CH2_TIMEOUTENR | R/W  | 0h    | Channel 2 Timeout Interrupt Disable Bit. Writing a one to this bit disable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable].<br>User and privileged mode read:<br>0 = Timeout Interrupt disable<br>1 = Timeout Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = Timeout Interrupt disable      |
| 11  | CH2_UNDERENR   | R/W  | 0h    | Channel 2 Underrun Interrupt Disable Bit. Writing a one to this bit disable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable].<br>User and privileged mode read:<br>0 = Underrun Interrupt disable<br>1 = Underrun Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = Underrun Interrupt disable |
| 10  | CH2_OVERENR    | R/W  | 0h    | Channel 2 Overrun Interrupt Disable Bit. Writing a one to this bit disable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable].<br>User and privileged mode read:<br>0 = Overrun Interrupt disable<br>1 = Overrun Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = Overrun Interrupt disable      |
| 9   | CH2_CRCFAILENR | R/W  | 0h    | Channel 2 CRC Fail Interrupt Disable Bit. Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable].<br>User and privileged mode read:<br>0 = CRC Fail Interrupt disable<br>1 = CRC Fail Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = CRC Fail Interrupt disable |
| 8:5 | RESERVED2      | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                     |
| 4   | CH1_TIMEOUTENR | R/W  | 0h    | Channel 1 Timeout Interrupt Disable Bit. Writing a one to this bit disable the timeout interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable].<br>User and privileged mode read:<br>0 = Timeout Interrupt disable<br>1 = Timeout Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = Timeout Interrupt disable      |
| 3   | CH1_UNDERENR   | R/W  | 0h    | Channel 1 Underrun Interrupt Disable Bit. Writing a one to this bit disable the underrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable].<br>User and privileged mode read:<br>0 = Underrun Interrupt disable<br>1 = Underrun Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = Underrun Interrupt disable |

**Table 5-2302. MSS\_MCRC\_CRC\_INTR Register Field Descriptions (continued)**

| Bit | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                      |
|-----|----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | CH1_OVERENR    | R/W  | 0h    | Channel 1 Overrun Interrupt Disable Bit. Writing a one to this bit disable the overrun interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read:<br>0 = Overrun Interrupt disable<br>1 = Overrun Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = Overrun Interrupt disable      |
| 1   | CH1_CRCFAILENR | R/W  | 0h    | Channel 1 CRC Fail Interrupt Disable Bit. Writing a one to this bit disable the CRC fail interrupt. Writing a zero has no effect. Reading from this bit gives the status [interrupt enable/disable]. User and privileged mode read:<br>0 = CRC Fail Interrupt disable<br>1 = CRC Fail Interrupt enable<br>User and privileged mode write:<br>0 = Has no effect<br>1 = CRC Fail Interrupt disable |
| 0   | RESERVED1      | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                  |

### 5.13.2.6 MSS\_MCRC\_CRC\_STATUS\_REG Register

#### 1 MSS\_MCRC\_CRC\_STATUS\_REG Register (Offset = 28h) [reset = 0h]

CRC interrupt status register. Contains interrupt flags for different types of interrupt.

Return to [Summary Table](#)

**Table 5-2303. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0028h       |

**Figure 5-761. MSS\_MCRC\_CRC\_STATUS\_REG Name Register**

| 31        | 30 | 29 | 28          | 27        | 26       | 25          | 24        |
|-----------|----|----|-------------|-----------|----------|-------------|-----------|
| RESERVED5 |    |    | CH4_TIMEOUT | CH4_UNDER | CH4_OVER | CH4_CRCFAIL | RESERVED4 |
| R         |    |    | R/W         | R/W       | R/W      | R/W         | R         |
| 0h        |    |    | 0h          | 0h        | 0h       | 0h          | 0h        |
| 23        | 22 | 21 | 20          | 19        | 18       | 17          | 16        |
| RESERVED4 |    |    | CH3_TIMEOUT | CH3_UNDER | CH3_OVER | CH3_CRCFAIL | RESERVED3 |
| R         |    |    | R/W         | R/W       | R/W      | R/W         | R         |
| 0h        |    |    | 0h          | 0h        | 0h       | 0h          | 0h        |
| 15        | 14 | 13 | 12          | 11        | 10       | 9           | 8         |
| RESERVED3 |    |    | CH2_TIMEOUT | CH2_UNDER | CH2_OVER | CH2_CRCFAIL | RESERVED2 |
| R         |    |    | R/W         | R/W       | R/W      | R/W         | R         |
| 0h        |    |    | 0h          | 0h        | 0h       | 0h          | 0h        |
| 7         | 6  | 5  | 4           | 3         | 2        | 1           | 0         |
| RESERVED2 |    |    | CH1_TIMEOUT | CH1_UNDER | CH1_OVER | CH1_CRCFAIL | RESERVED1 |
| R         |    |    | R/W         | R/W       | R/W      | R/W         | R         |
| 0h        |    |    | 0h          | 0h        | 0h       | 0h          | 0h        |

**Table 5-2305. MSS\_MCRC\_CRC\_STATUS\_REG Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                   |
|-------|-------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED5   | R    | 0h    |                                                                                                                                                                                                                                               |
| 28    | CH4_TIMEOUT | R/W  | 0h    | Channel 4 CRC Timeout Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode.<br>0 = No timeout interrupt is active<br>1 = Timeout interrupt is active                             |
| 27    | CH4_UNDER   | R/W  | 0h    | Channel 4 CRC Underrun Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only<br>0 = No underrun interrupt is active<br>1 = Underrun interrupt is active                      |
| 26    | CH4_OVER    | R/W  | 0h    | Channel 4 CRC Overrun Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode<br>0 = No overrun interrupt is active<br>1 = Overrun interrupt is active                              |
| 25    | CH4_CRCFAIL | R/W  | 0h    | Channel 4 CRC Compare Fail Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only.<br>0 = No CRC compare fail interrupt is active<br>1 = CRC compare fail interrupt is active |
| 24:21 | RESERVED4   | R    | 0h    |                                                                                                                                                                                                                                               |

**Table 5-2305. MSS\_MCRC\_CRC\_STATUS\_REG Register Field Descriptions (continued)**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                   |
|-------|-------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 20    | CH3_TIMEOUT | R/W  | 0h    | Channel 3 CRC Timeout Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode.<br>0 = No timeout interrupt is active<br>1 = Timeout interrupt is active                             |
| 19    | CH3_UNDER   | R/W  | 0h    | Channel 3 CRC Underrun Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only<br>0 = No underrun interrupt is active<br>1 = Underrun interrupt is active                      |
| 18    | CH3_OVER    | R/W  | 0h    | Channel 3 CRC Overrun Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode<br>0 = No overrun interrupt is active<br>1 = Overrun interrupt is active                              |
| 17    | CH3_CRCFAIL | R/W  | 0h    | Channel 3 CRC Compare Fail Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only.<br>0 = No CRC compare fail interrupt is active<br>1 = CRC compare fail interrupt is active |
| 16:13 | RESERVED3   | R    | 0h    |                                                                                                                                                                                                                                               |
| 12    | CH2_TIMEOUT | R/W  | 0h    | Channel 2 CRC Timeout Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode.<br>0 = No timeout interrupt is active<br>1 = Timeout interrupt is active                             |
| 11    | CH2_UNDER   | R/W  | 0h    | Channel 2 CRC Underrun Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only<br>0 = No underrun interrupt is active<br>1 = Underrun interrupt is active                      |
| 10    | CH2_OVER    | R/W  | 0h    | Channel 2 CRC Overrun Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode<br>0 = No overrun interrupt is active<br>1 = Overrun interrupt is active                              |
| 9     | CH2_CRCFAIL | R/W  | 0h    | Channel 2 CRC Compare Fail Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only.<br>0 = No CRC compare fail interrupt is active<br>1 = CRC compare fail interrupt is active |
| 8:5   | RESERVED2   | R    | 0h    |                                                                                                                                                                                                                                               |
| 4     | CH1_TIMEOUT | R/W  | 0h    | Channel 1 CRC Timeout Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode.<br>0 = No timeout interrupt is active<br>1 = Timeout interrupt is active                             |
| 3     | CH1_UNDER   | R/W  | 0h    | Channel 1 CRC Underrun Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only<br>0 = No underrun interrupt is active<br>1 = Underrun interrupt is active                      |
| 2     | CH1_OVER    | R/W  | 0h    | Channel 1 CRC Overrun Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode<br>0 = No overrun interrupt is active<br>1 = Overrun interrupt is active                              |

**Table 5-2305. MSS\_MCRC\_CRC\_STATUS\_REG Register Field Descriptions (continued)**

| Bit | Field       | Type | Reset | Description                                                                                                                                                                                                                                   |
|-----|-------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | CH1_CRCFAIL | R/W  | 0h    | Channel 1 CRC Compare Fail Status Flag. This bit is cleared by Writing a 1 to it only. Writing 0 has no effect. This bit is set in AUTO mode only.<br>0 = No CRC compare fail interrupt is active<br>1 = CRC compare fail interrupt is active |
| 0   | RESERVED1   | R    | 0h    |                                                                                                                                                                                                                                               |

### 5.13.2.7 MSS\_MCRC\_CRC\_INT\_OFFSET\_REG Register

#### 1 MSS\_MCRC\_CRC\_INT\_OFFSET\_REG Register (Offset = 30h) [reset = 0h]

Register indicates highest priority pending interrupt vector address.

Return to [Summary Table](#)

**Table 5-2306. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0030h       |

**Figure 5-762. MSS\_MCRC\_CRC\_INT\_OFFSET\_REG Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED1 |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED1 |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED1 |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| OFSTREG   |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 5-2308. MSS\_MCRC\_CRC\_INT\_OFFSET\_REG Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                         |
|------|-----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED1 | R    | 0h    |                                                                                                                                                                                     |
| 7:0  | OFSTREG   | R/W  | 0h    | CRC Interrupt Offset. This register indicates the highest priority pending interrupt vector address. Reading the offset register automatically clear the respective interrupt flag. |

### 5.13.2.8 MSS\_MCRC\_CRC\_BUSY Register

#### 1 MSS\_MCRC\_CRC\_BUSY Register (Offset = 38h) [reset = 0h]

Register indicates CRC busy flag for each channel.

Return to [Summary Table](#)

**Table 5-2309. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0038h       |

**Figure 5-763. MSS\_MCRC\_CRC\_BUSY Name Register**

| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24       |
|-----------|----|----|----|----|----|----|----------|
| RESERVED4 |    |    |    |    |    |    | CH4_BUSY |
| R         |    |    |    |    |    |    | R        |
| 0h        |    |    |    |    |    |    | 0h       |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16       |
| RESERVED3 |    |    |    |    |    |    | CH3_BUSY |
| R         |    |    |    |    |    |    | R        |
| 0h        |    |    |    |    |    |    | 0h       |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8        |
| RESERVED2 |    |    |    |    |    |    | CH2_BUSY |
| R         |    |    |    |    |    |    | R        |
| 0h        |    |    |    |    |    |    | 0h       |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0        |
| RESERVED1 |    |    |    |    |    |    | CH1_BUSY |
| R         |    |    |    |    |    |    | R        |
| 0h        |    |    |    |    |    |    | 0h       |

**Table 5-2311. MSS\_MCRC\_CRC\_BUSY Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                    |
|-------|-----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:25 | RESERVED4 | R    | 0h    |                                                                                                                                                                                                                                                                |
| 24    | CH4_BUSY  | R    | 0h    | Ch4_BUSY. During AUTO mode, the busy flag is set when the first data pattern of the block is compressed and remains set until the the last data pattern of the block is compressed. The flag is cleared when the last data pattern of the block is compressed. |
| 23:17 | RESERVED3 | R    | 0h    |                                                                                                                                                                                                                                                                |
| 16    | CH3_BUSY  | R    | 0h    | Ch3_BUSY. During AUTO mode, the busy flag is set when the first data pattern of the block is compressed and remains set until the the last data pattern of the block is compressed. The flag is cleared when the last data pattern of the block is compressed. |
| 15:9  | RESERVED2 | R    | 0h    |                                                                                                                                                                                                                                                                |
| 8     | CH2_BUSY  | R    | 0h    | Ch2_BUSY. During AUTO mode, the busy flag is set when the first data pattern of the block is compressed and remains set until the the last data pattern of the block is compressed. The flag is cleared when the last data pattern of the block is compressed. |
| 7:1   | RESERVED1 | R    | 0h    |                                                                                                                                                                                                                                                                |
| 0     | CH1_BUSY  | R    | 0h    | CH1_BUSY. During AUTO mode, the busy flag is set when the first data pattern of the block is compressed and remains set until the the last data pattern of the block is compressed. The flag is cleared when the last data pattern of the block is compressed. |

### 5.13.2.9 MSS\_MCRC\_CRC\_PCOUNT\_REG1 Register

#### 1 MSS\_MCRC\_CRC\_PCOUNT\_REG1 Register (Offset = 40h) [reset = 0h]

Channel 1 preload register for the pattern count.

Return to [Summary Table](#)

**Table 5-2312. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0040h       |

**Figure 5-764. MSS\_MCRC\_CRC\_PCOUNT\_REG1 Name Register**

|                |    |    |    |                |    |    |    |
|----------------|----|----|----|----------------|----|----|----|
| 31             | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| RESERVED1      |    |    |    |                |    |    |    |
| R              |    |    |    |                |    |    |    |
| 0h             |    |    |    |                |    |    |    |
| 23             | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| RESERVED1      |    |    |    | CRC_PAT_COUNT1 |    |    |    |
| R              |    |    |    | R/W            |    |    |    |
| 0h             |    |    |    | 0h             |    |    |    |
| 15             | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| CRC_PAT_COUNT1 |    |    |    |                |    |    |    |
| R/W            |    |    |    |                |    |    |    |
| 0h             |    |    |    |                |    |    |    |
| 7              | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| CRC_PAT_COUNT1 |    |    |    |                |    |    |    |
| R/W            |    |    |    |                |    |    |    |
| 0h             |    |    |    |                |    |    |    |

**Table 5-2314. MSS\_MCRC\_CRC\_PCOUNT\_REG1 Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                              |
|-------|----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED1      | R    | 0h    |                                                                                                                                                          |
| 19:0  | CRC_PAT_COUNT1 | R/W  | 0h    | Channel 1 Pattern Counter Preload Register. This register contains the number of data patterns in one sector to be compressed before a CRC is performed. |



### 5.13.2.10 MSS\_MCRC\_CRC\_SCOUNT\_REG1 Register

#### 1 MSS\_MCRC\_CRC\_SCOUNT\_REG1 Register (Offset = 44h) [reset = 0h]

Channel 1 preload register for the sector count.

Return to [Summary Table](#)

**Table 5-2315. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0044h       |

**Figure 5-765. MSS\_MCRC\_CRC\_SCOUNT\_REG1 Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED1      |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED1      |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CRC_SEC_COUNT1 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CRC_SEC_COUNT1 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-2317. MSS\_MCRC\_CRC\_SCOUNT\_REG1 Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                     |
|-------|----------------|------|-------|-----------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED1      | R    | 0h    |                                                                                                                 |
| 15:0  | CRC_SEC_COUNT1 | R/W  | 0h    | Channel 1 Sector Counter Preload Register. This register contains the number of sectors in one block of memory. |

### 5.13.2.11 MSS\_MCRC\_CRC\_CURSEC\_REG1 Register

#### 1 MSS\_MCRC\_CRC\_CURSEC\_REG1 Register (Offset = 48h) [reset = 0h]

Channel 1 current sector register contains the sector number which causes CRC failure.

Return to [Summary Table](#)

**Table 5-2318. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0048h       |

**Figure 5-766. MSS\_MCRC\_CRC\_CURSEC\_REG1 Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED1   |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED1   |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CRC_CURSEC1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CRC_CURSEC1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-2320. MSS\_MCRC\_CRC\_CURSEC\_REG1 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED1   | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 15:0  | CRC_CURSEC1 | R/W  | 0h    | Channel 1 Current Sector ID Register. In AUTO mode, this register contains the current sector number of which the signature verification fails. The sector counter is a free running up counter. When a sector fails, the erroneous sector number is logged into current sector ID register and the CRC fail interrupt is generated. The sector ID register is frozen until it is read and the CRC fail status bit is cleared by CPU. While it is frozen, it does not capture another erroneous sector number. When this condition happens, an overrun interrupt is generated instead. Once the register is read and the CRC fail interrupt flag is cleared it can capture new erroneous sector number. |

### 5.13.2.12 MSS\_MCRC\_CRC\_WDTPLD1 Register

#### 1 MSS\_MCRC\_CRC\_WDTPLD1 Register (Offset = 4Ch) [reset = 0h]

Channel 1 timeout pre-load value to check if within a given time DMA initiates a block transfer.

Return to [Summary Table](#)

**Table 5-2321. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 004Ch       |

**Figure 5-767. MSS\_MCRC\_CRC\_WDTPLD1 Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED1   |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CRC_WDTPLD1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CRC_WDTPLD1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CRC_WDTPLD1 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-2323. MSS\_MCRC\_CRC\_WDTPLD1 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                |
|-------|-------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED1   | R    | 0h    |                                                                                                                                                                            |
| 23:0  | CRC_WDTPLD1 | R/W  | 0h    | Channel 1 Watchdog Timeout Counter Preload Register. This register contains the number of clock cycles within which the DMA must transfer the next block of data patterns. |

### 5.13.2.13 MSS\_MCRC\_CRC\_BCTOPLD1 Register

#### 1 MSS\_MCRC\_CRC\_BCTOPLD1 Register (Offset = 50h) [reset = 0h]

Channel 1 timeout pre-load value to check if one block of patterns are compressed with a given time.

Return to [Summary Table](#)

**Table 5-2324. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0050h       |

**Figure 5-768. MSS\_MCRC\_CRC\_BCTOPLD1 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED1    |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CRC_BCTOPLD1 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CRC_BCTOPLD1 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CRC_BCTOPLD1 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-2326. MSS\_MCRC\_CRC\_BCTOPLD1 Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                                                                                                                      |
|-------|--------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED1    | R    | 0h    |                                                                                                                                                                                                                  |
| 23:0  | CRC_BCTOPLD1 | R/W  | 0h    | Channel 1 Block Complete Timeout Counter Preload Register. This register contains the number of clock cycles within which the CRC for an entire block needs to complete before a timeout interrupt is generated. |

### 5.13.2.14 MSS\_MCRC\_PSA\_SIGREGL1 Register

#### 1 MSS\_MCRC\_PSA\_SIGREGL1 Register (Offset = 60h) [reset = 0h]

Channel 1 PSA signature low register.

Return to [Summary Table](#)

**Table 5-2327. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0060h       |

**Figure 5-769. MSS\_MCRC\_PSA\_SIGREGL1 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PSASIG1_31_0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PSASIG1_31_0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PSASIG1_31_0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PSASIG1_31_0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-2329. MSS\_MCRC\_PSA\_SIGREGL1 Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                              |
|------|--------------|------|-------|----------------------------------------------------------------------------------------------------------|
| 31:0 | PSASIG1_31_0 | R/W  | 0h    | Channel 1 PSA Signature Low Register. This register contains the value stored at PSASIG1[31:0] register. |

### 5.13.2.15 MSS\_MCRC\_PSA\_SIGREGH1 Register

#### 1 MSS\_MCRC\_PSA\_SIGREGH1 Register (Offset = 64h) [reset = 0h]

Channel 1 PSA signature high register.

Return to [Summary Table](#)

**Table 5-2330. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0064h       |

**Figure 5-770. MSS\_MCRC\_PSA\_SIGREGH1 Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PSA_SIG1_63_32 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PSA_SIG1_63_32 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PSA_SIG1_63_32 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PSA_SIG1_63_32 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-2332. MSS\_MCRC\_PSA\_SIGREGH1 Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                                |
|------|----------------|------|-------|------------------------------------------------------------------------------------------------------------|
| 31:0 | PSA_SIG1_63_32 | R/W  | 0h    | Channel 1 PSA Signature High Register. This register contains the value stored at PSASIG1[63:32] register. |

### 5.13.2.16 MSS\_MCRC\_CRC\_REGL1 Register

#### 1 MSS\_MCRC\_CRC\_REGL1 Register (Offset = 68h) [reset = 0h]

Channel 1 CRC value low register.

Return to [Summary Table](#)

**Table 5-2333. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0068h       |

**Figure 5-771. MSS\_MCRC\_CRC\_REGL1 Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CRC1_31_0 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CRC1_31_0 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CRC1_31_0 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CRC1_31_0 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 5-2335. MSS\_MCRC\_CRC\_REGL1 Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                    |
|------|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CRC1_31_0 | R/W  | 0h    | Channel 1 CRC Value Low Register. This register contains the current known good signature value stored at CRC1[31:0] register. |

### 5.13.2.17 MSS\_MCRC\_CRC\_REGH1 Register

#### 1 MSS\_MCRC\_CRC\_REGH1 Register (Offset = 6Ch) [reset = 0h]

Channel 1 CRC value high register.

Return to [Summary Table](#)

**Table 5-2336. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 006Ch       |

**Figure 5-772. MSS\_MCRC\_CRC\_REGH1 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CRC1_63_32 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CRC1_63_32 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CRC1_63_32 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CRC1_63_32 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2338. MSS\_MCRC\_CRC\_REGH1 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                      |
|------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CRC1_63_32 | R/W  | 0h    | Channel 1 CRC Value High Register. This register contains the current known good signature value stored at CRC1[63:32] register. |



### 5.13.2.18 MSS\_MCRC\_PSA\_SECSIGREGL1 Register

#### 1 MSS\_MCRC\_PSA\_SECSIGREGL1 Register (Offset = 70h) [reset = 0h]

Channel 1 PSA sector signature low register.

Return to [Summary Table](#)

**Table 5-2339. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0070h       |

**Figure 5-773. MSS\_MCRC\_PSA\_SECSIGREGL1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PSASECSIG1_31_0 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PSASECSIG1_31_0 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PSASECSIG1_31_0 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PSASECSIG1_31_0 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 5-2341. MSS\_MCRC\_PSA\_SECSIGREGL1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                        |
|------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------|
| 31:0 | PSASECSIG1_31_0 | R    | 0h    | Channel 1 PSA Sector Signature Low Register. This register contains the value stored at PSASECSIG1[31:0] register. |

### 5.13.2.19 MSS\_MCRC\_PSA\_SECSIGREGH1 Register

#### 1 MSS\_MCRC\_PSA\_SECSIGREGH1 Register (Offset = 74h) [reset = 0h]

Channel 1 PSA sector signature high register.

Return to [Summary Table](#)

**Table 5-2342. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0074h       |

**Figure 5-774. MSS\_MCRC\_PSA\_SECSIGREGH1 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PSASECSIG1_63_32 |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PSASECSIG1_63_32 |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PSASECSIG1_63_32 |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PSASECSIG1_63_32 |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 5-2344. MSS\_MCRC\_PSA\_SECSIGREGH1 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                          |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------|
| 31:0 | PSASECSIG1_63_32 | R    | 0h    | Channel 1 PSA Sector Signature High Register. This register contains the value stored at PSASECSIG1[63:32] register. |

### 5.13.2.20 MSS\_MCRC\_RAW\_DATAREGL1 Register

#### 1 MSS\_MCRC\_RAW\_DATAREGL1 Register (Offset = 78h) [reset = 0h]

Channel 1 un-compressed raw data low register.

Return to [Summary Table](#)

**Table 5-2345. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0078h       |

**Figure 5-775. MSS\_MCRC\_RAW\_DATAREGL1 Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAW_DATA1_31_0 |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAW_DATA1_31_0 |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RAW_DATA1_31_0 |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RAW_DATA1_31_0 |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-2347. MSS\_MCRC\_RAW\_DATAREGL1 Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                     |
|------|----------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | RAW_DATA1_31_0 | R    | 0h    | Channel 1 Raw Data Low Register. This register contains bit 31:0 of the un-compressed raw data. |

### 5.13.2.21 MSS\_MCRC\_RAW\_DATAREGH1 Register

#### 1 MSS\_MCRC\_RAW\_DATAREGH1 Register (Offset = 7Ch) [reset = 0h]

Channel 1 un-compressed raw data high register.

Return to [Summary Table](#)

**Table 5-2348. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 007Ch       |

**Figure 5-776. MSS\_MCRC\_RAW\_DATAREGH1 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAW_DATA1_63_32 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAW_DATA1_63_32 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RAW_DATA1_63_32 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RAW_DATA1_63_32 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 5-2350. MSS\_MCRC\_RAW\_DATAREGH1 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                       |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------|
| 31:0 | RAW_DATA1_63_32 | R    | 0h    | Channel 1 Raw Data High Register. This register contains bit 63:32 of the un-compressed raw data. |

### 5.13.2.22 MSS\_MCRC\_CRC\_PCOUNT\_REG2 Register

#### 1 MSS\_MCRC\_CRC\_PCOUNT\_REG2 Register (Offset = 80h) [reset = 0h]

Channel 2 preload register for the pattern count.

Return to [Summary Table](#)

**Table 5-2351. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0080h       |

**Figure 5-777. MSS\_MCRC\_CRC\_PCOUNT\_REG2 Name Register**

|                |    |    |    |                |    |    |    |
|----------------|----|----|----|----------------|----|----|----|
| 31             | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| RESERVED1      |    |    |    |                |    |    |    |
| R              |    |    |    |                |    |    |    |
| 0h             |    |    |    |                |    |    |    |
| 23             | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| RESERVED1      |    |    |    | CRC_PAT_COUNT2 |    |    |    |
| R              |    |    |    | R/W            |    |    |    |
| 0h             |    |    |    | 0h             |    |    |    |
| 15             | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| CRC_PAT_COUNT2 |    |    |    |                |    |    |    |
| R/W            |    |    |    |                |    |    |    |
| 0h             |    |    |    |                |    |    |    |
| 7              | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| CRC_PAT_COUNT2 |    |    |    |                |    |    |    |
| R/W            |    |    |    |                |    |    |    |
| 0h             |    |    |    |                |    |    |    |

**Table 5-2353. MSS\_MCRC\_CRC\_PCOUNT\_REG2 Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                              |
|-------|----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED1      | R    | 0h    |                                                                                                                                                          |
| 19:0  | CRC_PAT_COUNT2 | R/W  | 0h    | Channel 2 Pattern Counter Preload Register. This register contains the number of data patterns in one sector to be compressed before a CRC is performed. |

### 5.13.2.23 MSS\_MCRC\_CRC\_SCOUNT\_REG2 Register

#### 1 MSS\_MCRC\_CRC\_SCOUNT\_REG2 Register (Offset = 84h) [reset = 0h]

Channel 2 preload register for the sector count.

Return to [Summary Table](#)

**Table 5-2354. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0084h       |

**Figure 5-778. MSS\_MCRC\_CRC\_SCOUNT\_REG2 Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED1      |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED1      |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CRC_SEC_COUNT2 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CRC_SEC_COUNT2 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-2356. MSS\_MCRC\_CRC\_SCOUNT\_REG2 Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                     |
|-------|----------------|------|-------|-----------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED1      | R    | 0h    |                                                                                                                 |
| 15:0  | CRC_SEC_COUNT2 | R/W  | 0h    | Channel 2 Sector Counter Preload Register. This register contains the number of sectors in one block of memory. |

### 5.13.2.24 MSS\_MCRC\_CRC\_CURSEC\_REG2 Register

#### 1 MSS\_MCRC\_CRC\_CURSEC\_REG2 Register (Offset = 88h) [reset = 0h]

Channel 2 current sector register contains the sector number which causes CRC fail-ure.

Return to [Summary Table](#)

**Table 5-2357. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0088h       |

**Figure 5-779. MSS\_MCRC\_CRC\_CURSEC\_REG2 Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED1   |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED1   |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CRC_CURSEC2 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CRC_CURSEC2 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-2359. MSS\_MCRC\_CRC\_CURSEC\_REG2 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED1   | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 15:0  | CRC_CURSEC2 | R/W  | 0h    | Channel 2 Current Sector ID Register. In AUTO mode, this register contains the current sector number of which the signature verification fails. The sector counter is a free running up counter. When a sector fails, the erroneous sector number is logged into current sector ID register and the CRC fail interrupt is generated. The sector ID register is frozen until it is read and the CRC fail status bit is cleared by CPU. While it is frozen, it does not capture another erroneous sector number. When this condition happens, an overrun interrupt is generated instead. Once the register is read and the CRC fail interrupt flag is cleared it can capture new erroneous sector number. |

### 5.13.2.25 MSS\_MCRC\_CRC\_WDTPLD2 Register

#### 1 MSS\_MCRC\_CRC\_WDTPLD2 Register (Offset = 8Ch) [reset = 0h]

Channel 2 timeout pre-load value to check if within a given time DMA initiates a block transfer.

Return to [Summary Table](#)

**Table 5-2360. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 008Ch       |

**Figure 5-780. MSS\_MCRC\_CRC\_WDTPLD2 Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED1   |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CRC_WDTPLD2 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CRC_WDTPLD2 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CRC_WDTPLD2 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-2362. MSS\_MCRC\_CRC\_WDTPLD2 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                |
|-------|-------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED1   | R    | 0h    |                                                                                                                                                                            |
| 23:0  | CRC_WDTPLD2 | R/W  | 0h    | Channel 2 Watchdog Timeout Counter Preload Register. This register contains the number of clock cycles within which the DMA must transfer the next block of data patterns. |



### 5.13.2.26 MSS\_MCRC\_CRC\_BCTOPLD2 Register

#### 1 MSS\_MCRC\_CRC\_BCTOPLD2 Register (Offset = 90h) [reset = 0h]

Channel 2 timeout pre-load value to check if one block of patterns are compressed with a given time.

Return to [Summary Table](#)

**Table 5-2363. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0090h       |

**Figure 5-781. MSS\_MCRC\_CRC\_BCTOPLD2 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED1    |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CRC_BCTOPLD2 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CRC_BCTOPLD2 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CRC_BCTOPLD2 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-2365. MSS\_MCRC\_CRC\_BCTOPLD2 Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                                                                                                                      |
|-------|--------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED1    | R    | 0h    |                                                                                                                                                                                                                  |
| 23:0  | CRC_BCTOPLD2 | R/W  | 0h    | Channel 2 Block Complete Timeout Counter Preload Register. This register contains the number of clock cycles within which the CRC for an entire block needs to complete before a timeout interrupt is generated. |

### 5.13.2.27 MSS\_MCRC\_PSA\_SIGREGL2 Register

#### 1 MSS\_MCRC\_PSA\_SIGREGL2 Register (Offset = A0h) [reset = 0h]

Channel 2 PSA signature low register.

Return to [Summary Table](#)

**Table 5-2366. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 00A0h       |

**Figure 5-782. MSS\_MCRC\_PSA\_SIGREGL2 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PSASIG2_31_0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PSASIG2_31_0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PSASIG2_31_0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PSASIG2_31_0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-2368. MSS\_MCRC\_PSA\_SIGREGL2 Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                              |
|------|--------------|------|-------|----------------------------------------------------------------------------------------------------------|
| 31:0 | PSASIG2_31_0 | R/W  | 0h    | Channel 2 PSA Signature Low Register. This register contains the value stored at PSASIG2[31:0] register. |

### 5.13.2.28 MSS\_MCRC\_PSA\_SIGREGH2 Register

#### 1 MSS\_MCRC\_PSA\_SIGREGH2 Register (Offset = A4h) [reset = 0h]

Channel 2 PSA signature high register.

Return to [Summary Table](#)

**Table 5-2369. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 00A4h       |

**Figure 5-783. MSS\_MCRC\_PSA\_SIGREGH2 Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PSA_SIG2_63_32 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PSA_SIG2_63_32 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PSA_SIG2_63_32 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PSA_SIG2_63_32 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-2371. MSS\_MCRC\_PSA\_SIGREGH2 Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                                |
|------|----------------|------|-------|------------------------------------------------------------------------------------------------------------|
| 31:0 | PSA_SIG2_63_32 | R/W  | 0h    | Channel 2 PSA Signature High Register. This register contains the value stored at PSASIG2[63:32] register. |

### 5.13.2.29 MSS\_MCRC\_CRC\_REGL2 Register

#### 1 MSS\_MCRC\_CRC\_REGL2 Register (Offset = A8h) [reset = 0h]

Channel 2 CRC value low register.

Return to [Summary Table](#)

**Table 5-2372. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 00A8h       |

**Figure 5-784. MSS\_MCRC\_CRC\_REGL2 Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CRC2_31_0 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CRC2_31_0 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CRC2_31_0 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CRC2_31_0 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 5-2374. MSS\_MCRC\_CRC\_REGL2 Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                    |
|------|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CRC2_31_0 | R/W  | 0h    | Channel 2 CRC Value Low Register. This register contains the current known good signature value stored at CRC2[31:0] register. |

### 5.13.2.30 MSS\_MCRC\_CRC\_REGH2 Register

#### 1 MSS\_MCRC\_CRC\_REGH2 Register (Offset = ACh) [reset = 0h]

Channel 2 CRC value high register.

Return to [Summary Table](#)

**Table 5-2375. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 00ACh       |

**Figure 5-785. MSS\_MCRC\_CRC\_REGH2 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CRC2_63_32 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CRC2_63_32 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CRC2_63_32 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CRC2_63_32 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2377. MSS\_MCRC\_CRC\_REGH2 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                      |
|------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CRC2_63_32 | R/W  | 0h    | Channel 2 CRC Value High Register. This register contains the current known good signature value stored at CRC2[63:32] register. |

### 5.13.2.31 MSS\_MCRC\_PSA\_SECSIGREGL2 Register

#### 1 MSS\_MCRC\_PSA\_SECSIGREGL2 Register (Offset = B0h) [reset = 0h]

Channel 2 PSA sector signature low register.

Return to [Summary Table](#)

**Table 5-2378. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 00B0h       |

**Figure 5-786. MSS\_MCRC\_PSA\_SECSIGREGL2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PSASECSIG2_31_0 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PSASECSIG2_31_0 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PSASECSIG2_31_0 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PSASECSIG2_31_0 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 5-2380. MSS\_MCRC\_PSA\_SECSIGREGL2 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                        |
|------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------|
| 31:0 | PSASECSIG2_31_0 | R    | 0h    | Channel 2 PSA Sector Signature Low Register. This register contains the value stored at PSASECSIG2[31:0] register. |

### 5.13.2.32 MSS\_MCRC\_PSA\_SECSIGREGH2 Register

#### 1 MSS\_MCRC\_PSA\_SECSIGREGH2 Register (Offset = B4h) [reset = 0h]

Channel 2 PSA sector signature high register.

Return to [Summary Table](#)

**Table 5-2381. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 00B4h       |

**Figure 5-787. MSS\_MCRC\_PSA\_SECSIGREGH2 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PSASECSIG2_63_32 |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PSASECSIG2_63_32 |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PSASECSIG2_63_32 |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PSASECSIG2_63_32 |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 5-2383. MSS\_MCRC\_PSA\_SECSIGREGH2 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                          |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------|
| 31:0 | PSASECSIG2_63_32 | R    | 0h    | Channel 2 PSA Sector Signature High Register. This register contains the value stored at PSASECSIG2[63:32] register. |

### 5.13.2.33 MSS\_MCRC\_RAW\_DATAREGL2 Register

#### 1 MSS\_MCRC\_RAW\_DATAREGL2 Register (Offset = B8h) [reset = 0h]

Channel 2 un-compressed raw data low register.

Return to [Summary Table](#)

**Table 5-2384. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 00B8h       |

**Figure 5-788. MSS\_MCRC\_RAW\_DATAREGL2 Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAW_DATA2_31_0 |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAW_DATA2_31_0 |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RAW_DATA2_31_0 |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RAW_DATA2_31_0 |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-2386. MSS\_MCRC\_RAW\_DATAREGL2 Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                     |
|------|----------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | RAW_DATA2_31_0 | R    | 0h    | Channel 2 Raw Data Low Register. This register contains bit 31:0 of the un-compressed raw data. |



### 5.13.2.34 MSS\_MCRC\_RAW\_DATAREGH2 Register

#### 1 MSS\_MCRC\_RAW\_DATAREGH2 Register (Offset = BCh) [reset = 0h]

Channel 2 un-compressed raw data high Register.

Return to [Summary Table](#)

**Table 5-2387. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 00BCh       |

**Figure 5-789. MSS\_MCRC\_RAW\_DATAREGH2 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAW_DATA2_63_32 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAW_DATA2_63_32 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RAW_DATA2_63_32 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RAW_DATA2_63_32 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 5-2389. MSS\_MCRC\_RAW\_DATAREGH2 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                       |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------|
| 31:0 | RAW_DATA2_63_32 | R    | 0h    | Channel 2 Raw Data High Register. This register contains bit 63:32 of the un-compressed raw data. |

### 5.13.2.35 MSS\_MCRC\_CRC\_PCOUNT\_REG3 Register

#### 1 MSS\_MCRC\_CRC\_PCOUNT\_REG3 Register (Offset = C0h) [reset = 0h]

Channel 3 preload register for the pattern count.

Return to [Summary Table](#)

**Table 5-2390. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 00C0h       |

**Figure 5-790. MSS\_MCRC\_CRC\_PCOUNT\_REG3 Name Register**

|                |    |    |    |                |    |    |    |
|----------------|----|----|----|----------------|----|----|----|
| 31             | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| RESERVED1      |    |    |    |                |    |    |    |
| R              |    |    |    |                |    |    |    |
| 0h             |    |    |    |                |    |    |    |
| 23             | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| RESERVED1      |    |    |    | CRC_PAT_COUNT3 |    |    |    |
| R              |    |    |    | R/W            |    |    |    |
| 0h             |    |    |    | 0h             |    |    |    |
| 15             | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| CRC_PAT_COUNT3 |    |    |    |                |    |    |    |
| R/W            |    |    |    |                |    |    |    |
| 0h             |    |    |    |                |    |    |    |
| 7              | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| CRC_PAT_COUNT3 |    |    |    |                |    |    |    |
| R/W            |    |    |    |                |    |    |    |
| 0h             |    |    |    |                |    |    |    |

**Table 5-2392. MSS\_MCRC\_CRC\_PCOUNT\_REG3 Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                              |
|-------|----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED1      | R    | 0h    |                                                                                                                                                          |
| 19:0  | CRC_PAT_COUNT3 | R/W  | 0h    | Channel 3 Pattern Counter Preload Register. This register contains the number of data patterns in one sector to be compressed before a CRC is performed. |

### 5.13.2.36 MSS\_MCRC\_CRC\_SCOUNT\_REG3 Register

#### 1 MSS\_MCRC\_CRC\_SCOUNT\_REG3 Register (Offset = C4h) [reset = 0h]

Channel 3 preload register for the sector count.

Return to [Summary Table](#)

**Table 5-2393. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 00C4h       |

**Figure 5-791. MSS\_MCRC\_CRC\_SCOUNT\_REG3 Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED1      |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED1      |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CRC_SEC_COUNT3 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CRC_SEC_COUNT3 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-2395. MSS\_MCRC\_CRC\_SCOUNT\_REG3 Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                     |
|-------|----------------|------|-------|-----------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED1      | R    | 0h    |                                                                                                                 |
| 15:0  | CRC_SEC_COUNT3 | R/W  | 0h    | Channel 3 Sector Counter Preload Register. This register contains the number of sectors in one block of memory. |

### 5.13.2.37 MSS\_MCRC\_CRC\_CURSEC\_REG3 Register

#### 1 MSS\_MCRC\_CRC\_CURSEC\_REG3 Register (Offset = C8h) [reset = 0h]

Channel 3 current sector register contains the sector number which causes CRC fail-ure.

Return to [Summary Table](#)

**Table 5-2396. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 00C8h       |

**Figure 5-792. MSS\_MCRC\_CRC\_CURSEC\_REG3 Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED1   |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED1   |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CRC_CURSEC3 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CRC_CURSEC3 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-2398. MSS\_MCRC\_CRC\_CURSEC\_REG3 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED1   | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 15:0  | CRC_CURSEC3 | R/W  | 0h    | Channel 3 Current Sector ID Register. In AUTO mode, this register contains the current sector number of which the signature verification fails. The sector counter is a free running up counter. When a sector fails, the erroneous sector number is logged into current sector ID register and the CRC fail interrupt is generated. The sector ID register is frozen until it is read and the CRC fail status bit is cleared by CPU. While it is frozen, it does not capture another erroneous sector number. When this condition happens, an overrun interrupt is generated instead. Once the register is read and the CRC fail interrupt flag is cleared it can capture new erroneous sector number. |

### 5.13.2.38 MSS\_MCRC\_CRC\_WDTPLD3 Register

#### 1 MSS\_MCRC\_CRC\_WDTPLD3 Register (Offset = CCh) [reset = 0h]

Channel 3 timeout pre-load value to check if within a given time DMA initiates a block transfer.

Return to [Summary Table](#)

**Table 5-2399. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 00CCh       |

**Figure 5-793. MSS\_MCRC\_CRC\_WDTPLD3 Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED1   |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CRC_WDTPLD3 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CRC_WDTPLD3 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CRC_WDTPLD3 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-2401. MSS\_MCRC\_CRC\_WDTPLD3 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                |
|-------|-------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED1   | R    | 0h    |                                                                                                                                                                            |
| 23:0  | CRC_WDTPLD3 | R/W  | 0h    | Channel 3 Watchdog Timeout Counter Preload Register. This register contains the number of clock cycles within which the DMA must transfer the next block of data patterns. |

### 5.13.2.39 MSS\_MCRC\_CRC\_BCTOPLD3 Register

#### 1 MSS\_MCRC\_CRC\_BCTOPLD3 Register (Offset = D0h) [reset = 0h]

Channel 3 timeout pre-load value to check if one block of patterns are compressed with a given time.

Return to [Summary Table](#)

**Table 5-2402. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 00D0h       |

**Figure 5-794. MSS\_MCRC\_CRC\_BCTOPLD3 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED1    |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CRC_BCTOPLD3 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CRC_BCTOPLD3 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CRC_BCTOPLD3 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-2404. MSS\_MCRC\_CRC\_BCTOPLD3 Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                                                                                                                      |
|-------|--------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED1    | R    | 0h    |                                                                                                                                                                                                                  |
| 23:0  | CRC_BCTOPLD3 | R/W  | 0h    | Channel 3 Block Complete Timeout Counter Preload Register. This register contains the number of clock cycles within which the CRC for an entire block needs to complete before a timeout interrupt is generated. |

### 5.13.2.40 MSS\_MCRC\_PSA\_SIGREGL3 Register

#### 1 MSS\_MCRC\_PSA\_SIGREGL3 Register (Offset = E0h) [reset = 0h]

Channel 3 PSA signature low register.

Return to [Summary Table](#)

**Table 5-2405. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 00E0h       |

**Figure 5-795. MSS\_MCRC\_PSA\_SIGREGL3 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PSASIG3_31_0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PSASIG3_31_0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PSASIG3_31_0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PSASIG3_31_0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-2407. MSS\_MCRC\_PSA\_SIGREGL3 Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                              |
|------|--------------|------|-------|----------------------------------------------------------------------------------------------------------|
| 31:0 | PSASIG3_31_0 | R/W  | 0h    | Channel 3 PSA Signature Low Register. This register contains the value stored at PSASIG2[31:0] register. |

### 5.13.2.41 MSS\_MCRC\_PSA\_SIGREGH3 Register

#### 1 MSS\_MCRC\_PSA\_SIGREGH3 Register (Offset = E4h) [reset = 0h]

Channel 3 PSA signature high register.

Return to [Summary Table](#)

**Table 5-2408. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 00E4h       |

**Figure 5-796. MSS\_MCRC\_PSA\_SIGREGH3 Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PSA_SIG3_63_32 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PSA_SIG3_63_32 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PSA_SIG3_63_32 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PSA_SIG3_63_32 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-2410. MSS\_MCRC\_PSA\_SIGREGH3 Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                                |
|------|----------------|------|-------|------------------------------------------------------------------------------------------------------------|
| 31:0 | PSA_SIG3_63_32 | R/W  | 0h    | Channel 3 PSA Signature High Register. This register contains the value stored at PSASIG2[63:32] register. |



### 5.13.2.42 MSS\_MCRC\_CRC\_REGL3 Register

#### 1 MSS\_MCRC\_CRC\_REGL3 Register (Offset = E8h) [reset = 0h]

Channel 3 CRC value low register.

Return to [Summary Table](#)

**Table 5-2411. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 00E8h       |

**Figure 5-797. MSS\_MCRC\_CRC\_REGL3 Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CRC3_31_0 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CRC3_31_0 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CRC3_31_0 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CRC3_31_0 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 5-2413. MSS\_MCRC\_CRC\_REGL3 Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                    |
|------|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CRC3_31_0 | R/W  | 0h    | Channel 3 CRC Value Low Register. This register contains the current known good signature value stored at CRC2[31:0] register. |

### 5.13.2.43 MSS\_MCRC\_CRC\_REGH3 Register

#### 1 MSS\_MCRC\_CRC\_REGH3 Register (Offset = ECh) [reset = 0h]

Channel 3 CRC value high register.

Return to [Summary Table](#)

**Table 5-2414. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 00ECh       |

**Figure 5-798. MSS\_MCRC\_CRC\_REGH3 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CRC3_63_32 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CRC3_63_32 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CRC3_63_32 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CRC3_63_32 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2416. MSS\_MCRC\_CRC\_REGH3 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                      |
|------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CRC3_63_32 | R/W  | 0h    | Channel 3 CRC Value High Register. This register contains the current known good signature value stored at CRC2[63:32] register. |

### 5.13.2.44 MSS\_MCRC\_PSA\_SECSIGREGL3 Register

#### 1 MSS\_MCRC\_PSA\_SECSIGREGL3 Register (Offset = F0h) [reset = 0h]

Channel 3 PSA sector signature low register.

Return to [Summary Table](#)

**Table 5-2417. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 00F0h       |

**Figure 5-799. MSS\_MCRC\_PSA\_SECSIGREGL3 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PSASECSIG3_31_0 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PSASECSIG3_31_0 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PSASECSIG3_31_0 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PSASECSIG3_31_0 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 5-2419. MSS\_MCRC\_PSA\_SECSIGREGL3 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                        |
|------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------|
| 31:0 | PSASECSIG3_31_0 | R    | 0h    | Channel 3 PSA Sector Signature Low Register. This register contains the value stored at PSASECSIG2[31:0] register. |

### 5.13.2.45 MSS\_MCRC\_PSA\_SECSIGREGH3 Register

#### 1 MSS\_MCRC\_PSA\_SECSIGREGH3 Register (Offset = F4h) [reset = 0h]

Channel 3 PSA sector signature high register.

Return to [Summary Table](#)

**Table 5-2420. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 00F4h       |

**Figure 5-800. MSS\_MCRC\_PSA\_SECSIGREGH3 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PSASECSIG3_63_32 |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PSASECSIG3_63_32 |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PSASECSIG3_63_32 |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PSASECSIG3_63_32 |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 5-2422. MSS\_MCRC\_PSA\_SECSIGREGH3 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                          |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------|
| 31:0 | PSASECSIG3_63_32 | R    | 0h    | Channel 3 PSA Sector Signature High Register. This register contains the value stored at PSASECSIG2[63:32] register. |

### 5.13.2.46 MSS\_MCRC\_RAW\_DATAREGL3 Register

#### 1 MSS\_MCRC\_RAW\_DATAREGL3 Register (Offset = F8h) [reset = 0h]

Channel 3 un-compressed raw data low register.

Return to [Summary Table](#)

**Table 5-2423. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 00F8h       |

**Figure 5-801. MSS\_MCRC\_RAW\_DATAREGL3 Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAW_DATA3_31_0 |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAW_DATA3_31_0 |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RAW_DATA3_31_0 |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RAW_DATA3_31_0 |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-2425. MSS\_MCRC\_RAW\_DATAREGL3 Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                     |
|------|----------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | RAW_DATA3_31_0 | R    | 0h    | Channel 3 Raw Data Low Register. This register contains bit 31:0 of the un-compressed raw data. |

### 5.13.2.47 MSS\_MCRC\_RAW\_DATAREGH3 Register

#### 1 MSS\_MCRC\_RAW\_DATAREGH3 Register (Offset = FCh) [reset = 0h]

Channel 3 un-compressed raw data high Register.

Return to [Summary Table](#)

**Table 5-2426. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 00FCh       |

**Figure 5-802. MSS\_MCRC\_RAW\_DATAREGH3 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAW_DATA3_63_32 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAW_DATA3_63_32 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RAW_DATA3_63_32 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RAW_DATA3_63_32 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 5-2428. MSS\_MCRC\_RAW\_DATAREGH3 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                       |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------|
| 31:0 | RAW_DATA3_63_32 | R    | 0h    | Channel 3 Raw Data High Register. This register contains bit 63:32 of the un-compressed raw data. |

### 5.13.2.48 MSS\_MCRC\_CRC\_PCOUNT\_REG4 Register

#### 1 MSS\_MCRC\_CRC\_PCOUNT\_REG4 Register (Offset = 100h) [reset = 0h]

Channel 4 preload register for the pattern count.

Return to [Summary Table](#)

**Table 5-2429. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0100h       |

**Figure 5-803. MSS\_MCRC\_CRC\_PCOUNT\_REG4 Name Register**

|                |    |    |    |                |    |    |    |
|----------------|----|----|----|----------------|----|----|----|
| 31             | 30 | 29 | 28 | 27             | 26 | 25 | 24 |
| RESERVED1      |    |    |    |                |    |    |    |
| R              |    |    |    |                |    |    |    |
| 0h             |    |    |    |                |    |    |    |
| 23             | 22 | 21 | 20 | 19             | 18 | 17 | 16 |
| RESERVED1      |    |    |    | CRC_PAT_COUNT4 |    |    |    |
| R              |    |    |    | R/W            |    |    |    |
| 0h             |    |    |    | 0h             |    |    |    |
| 15             | 14 | 13 | 12 | 11             | 10 | 9  | 8  |
| CRC_PAT_COUNT4 |    |    |    |                |    |    |    |
| R/W            |    |    |    |                |    |    |    |
| 0h             |    |    |    |                |    |    |    |
| 7              | 6  | 5  | 4  | 3              | 2  | 1  | 0  |
| CRC_PAT_COUNT4 |    |    |    |                |    |    |    |
| R/W            |    |    |    |                |    |    |    |
| 0h             |    |    |    |                |    |    |    |

**Table 5-2431. MSS\_MCRC\_CRC\_PCOUNT\_REG4 Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                                              |
|-------|----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED1      | R    | 0h    |                                                                                                                                                          |
| 19:0  | CRC_PAT_COUNT4 | R/W  | 0h    | Channel 4 Pattern Counter Preload Register. This register contains the number of data patterns in one sector to be compressed before a CRC is performed. |

### 5.13.2.49 MSS\_MCRC\_CRC\_SCOUNT\_REG4 Register

#### 1 MSS\_MCRC\_CRC\_SCOUNT\_REG4 Register (Offset = 104h) [reset = 0h]

Channel 4 preload register for the sector count.

Return to [Summary Table](#)

**Table 5-2432. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0104h       |

**Figure 5-804. MSS\_MCRC\_CRC\_SCOUNT\_REG4 Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED1      |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED1      |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CRC_SEC_COUNT4 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CRC_SEC_COUNT4 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-2434. MSS\_MCRC\_CRC\_SCOUNT\_REG4 Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                     |
|-------|----------------|------|-------|-----------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED1      | R    | 0h    |                                                                                                                 |
| 15:0  | CRC_SEC_COUNT4 | R/W  | 0h    | Channel 4 Sector Counter Preload Register. This register contains the number of sectors in one block of memory. |



### 5.13.2.50 MSS\_MCRC\_CRC\_CURSEC\_REG4 Register

#### 1 MSS\_MCRC\_CRC\_CURSEC\_REG4 Register (Offset = 108h) [reset = 0h]

Channel 4 current sector register contains the sector number which causes CRC fail-ure.

Return to [Summary Table](#)

**Table 5-2435. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0108h       |

**Figure 5-805. MSS\_MCRC\_CRC\_CURSEC\_REG4 Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED1   |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED1   |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CRC_CURSEC4 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CRC_CURSEC4 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-2437. MSS\_MCRC\_CRC\_CURSEC\_REG4 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|-------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED1   | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 15:0  | CRC_CURSEC4 | R/W  | 0h    | Channel 4 Current Sector ID Register. In AUTO mode, this register contains the current sector number of which the signature verification fails. The sector counter is a free running up counter. When a sector fails, the erroneous sector number is logged into current sector ID register and the CRC fail interrupt is generated. The sector ID register is frozen until it is read and the CRC fail status bit is cleared by CPU. While it is frozen, it does not capture another erroneous sector number. When this condition happens, an overrun interrupt is generated instead. Once the register is read and the CRC fail interrupt flag is cleared it can capture new erroneous sector number. |

### 5.13.2.51 MSS\_MCRC\_CRC\_WDTPLD4 Register

#### 1 MSS\_MCRC\_CRC\_WDTPLD4 Register (Offset = 10Ch) [reset = 0h]

Channel 4 timeout pre-load value to check if within a given time DMA initiates a block transfer.

Return to [Summary Table](#)

**Table 5-2438. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 010Ch       |

**Figure 5-806. MSS\_MCRC\_CRC\_WDTPLD4 Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED1   |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CRC_WDTPLD4 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CRC_WDTPLD4 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CRC_WDTPLD4 |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-2440. MSS\_MCRC\_CRC\_WDTPLD4 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                |
|-------|-------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED1   | R    | 0h    |                                                                                                                                                                            |
| 23:0  | CRC_WDTPLD4 | R/W  | 0h    | Channel 4 Watchdog Timeout Counter Preload Register. This register contains the number of clock cycles within which the DMA must transfer the next block of data patterns. |

### 5.13.2.52 MSS\_MCRC\_CRC\_BCTOPLD4 Register

#### 1 MSS\_MCRC\_CRC\_BCTOPLD4 Register (Offset = 110h) [reset = 0h]

Channel 4 timeout pre-load value to check if one block of patterns are compressed with a given time.

Return to [Summary Table](#)

**Table 5-2441. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0110h       |

**Figure 5-807. MSS\_MCRC\_CRC\_BCTOPLD4 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED1    |    |    |    |    |    |    |    |
| R            |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CRC_BCTOPLD4 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CRC_BCTOPLD4 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CRC_BCTOPLD4 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-2443. MSS\_MCRC\_CRC\_BCTOPLD4 Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                                                                                                                      |
|-------|--------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED1    | R    | 0h    |                                                                                                                                                                                                                  |
| 23:0  | CRC_BCTOPLD4 | R/W  | 0h    | Channel 4 Block Complete Timeout Counter Preload Register. This register contains the number of clock cycles within which the CRC for an entire block needs to complete before a timeout interrupt is generated. |

### 5.13.2.53 MSS\_MCRC\_PSA\_SIGREGL4 Register

#### 1 MSS\_MCRC\_PSA\_SIGREGL4 Register (Offset = 120h) [reset = 0h]

Channel 4 PSA signature low register.

Return to [Summary Table](#)

**Table 5-2444. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0120h       |

**Figure 5-808. MSS\_MCRC\_PSA\_SIGREGL4 Name Register**

|              |    |    |    |    |    |    |    |
|--------------|----|----|----|----|----|----|----|
| 31           | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PSASIG4_31_0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 23           | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PSASIG4_31_0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 15           | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PSASIG4_31_0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |
| 7            | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PSASIG4_31_0 |    |    |    |    |    |    |    |
| R/W          |    |    |    |    |    |    |    |
| 0h           |    |    |    |    |    |    |    |

**Table 5-2446. MSS\_MCRC\_PSA\_SIGREGL4 Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                              |
|------|--------------|------|-------|----------------------------------------------------------------------------------------------------------|
| 31:0 | PSASIG4_31_0 | R/W  | 0h    | Channel 4 PSA Signature Low Register. This register contains the value stored at PSASIG2[31:0] register. |

### 5.13.2.54 MSS\_MCRC\_PSA\_SIGREGH4 Register

#### 1 MSS\_MCRC\_PSA\_SIGREGH4 Register (Offset = 124h) [reset = 0h]

Channel 4 PSA signature high register.

Return to [Summary Table](#)

**Table 5-2447. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0124h       |

**Figure 5-809. MSS\_MCRC\_PSA\_SIGREGH4 Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PSA_SIG4_63_32 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PSA_SIG4_63_32 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PSA_SIG4_63_32 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PSA_SIG4_63_32 |    |    |    |    |    |    |    |
| R/W            |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-2449. MSS\_MCRC\_PSA\_SIGREGH4 Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                                |
|------|----------------|------|-------|------------------------------------------------------------------------------------------------------------|
| 31:0 | PSA_SIG4_63_32 | R/W  | 0h    | Channel 4 PSA Signature High Register. This register contains the value stored at PSASIG2[63:32] register. |

### 5.13.2.55 MSS\_MCRC\_CRC\_REGL4 Register

#### 1 MSS\_MCRC\_CRC\_REGL4 Register (Offset = 128h) [reset = 0h]

Channel 4 CRC value low register.

Return to [Summary Table](#)

**Table 5-2450. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0128h       |

**Figure 5-810. MSS\_MCRC\_CRC\_REGL4 Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CRC4_31_0 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CRC4_31_0 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CRC4_31_0 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CRC4_31_0 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 5-2452. MSS\_MCRC\_CRC\_REGL4 Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                    |
|------|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CRC4_31_0 | R/W  | 0h    | Channel 4 CRC Value Low Register. This register contains the current known good signature value stored at CRC2[31:0] register. |

### 5.13.2.56 MSS\_MCRC\_CRC\_REGH4 Register

#### 1 MSS\_MCRC\_CRC\_REGH4 Register (Offset = 12Ch) [reset = 0h]

Channel 4 CRC value high register.

Return to [Summary Table](#)

**Table 5-2453. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 012Ch       |

**Figure 5-811. MSS\_MCRC\_CRC\_REGH4 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CRC4_63_32 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CRC4_63_32 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CRC4_63_32 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CRC4_63_32 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2455. MSS\_MCRC\_CRC\_REGH4 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                      |
|------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CRC4_63_32 | R/W  | 0h    | Channel 4 CRC Value High Register. This register contains the current known good signature value stored at CRC2[63:32] register. |

### 5.13.2.57 MSS\_MCRC\_PSA\_SECSIGREGL4 Register

#### 1 MSS\_MCRC\_PSA\_SECSIGREGL4 Register (Offset = 130h) [reset = 0h]

Channel 4 PSA sector signature low register.

Return to [Summary Table](#)

**Table 5-2456. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0130h       |

**Figure 5-812. MSS\_MCRC\_PSA\_SECSIGREGL4 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PSASECSIG4_31_0 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PSASECSIG4_31_0 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PSASECSIG4_31_0 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PSASECSIG4_31_0 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 5-2458. MSS\_MCRC\_PSA\_SECSIGREGL4 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                                        |
|------|-----------------|------|-------|--------------------------------------------------------------------------------------------------------------------|
| 31:0 | PSASECSIG4_31_0 | R    | 0h    | Channel 4 PSA Sector Signature Low Register. This register contains the value stored at PSASECSIG2[31:0] register. |



### 5.13.2.58 MSS\_MCRC\_PSA\_SECSIGREGH4 Register

#### 1 MSS\_MCRC\_PSA\_SECSIGREGH4 Register (Offset = 134h) [reset = 0h]

Channel 4 PSA sector signature high register.

Return to [Summary Table](#)

**Table 5-2459. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0134h       |

**Figure 5-813. MSS\_MCRC\_PSA\_SECSIGREGH4 Name Register**

|                  |    |    |    |    |    |    |    |
|------------------|----|----|----|----|----|----|----|
| 31               | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| PSASECSIG4_63_32 |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 23               | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| PSASECSIG4_63_32 |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 15               | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PSASECSIG4_63_32 |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |
| 7                | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PSASECSIG4_63_32 |    |    |    |    |    |    |    |
| R                |    |    |    |    |    |    |    |
| 0h               |    |    |    |    |    |    |    |

**Table 5-2461. MSS\_MCRC\_PSA\_SECSIGREGH4 Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                                                                                          |
|------|------------------|------|-------|----------------------------------------------------------------------------------------------------------------------|
| 31:0 | PSASECSIG4_63_32 | R    | 0h    | Channel 4 PSA Sector Signature High Register. This register contains the value stored at PSASECSIG2[63:32] register. |

### 5.13.2.59 MSS\_MCRC\_RAW\_DATAREGL4 Register

#### 1 MSS\_MCRC\_RAW\_DATAREGL4 Register (Offset = 138h) [reset = 0h]

Channel 4 un-compressed raw data low register.

Return to [Summary Table](#)

**Table 5-2462. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0138h       |

**Figure 5-814. MSS\_MCRC\_RAW\_DATAREGL4 Name Register**

|                |    |    |    |    |    |    |    |
|----------------|----|----|----|----|----|----|----|
| 31             | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAW_DATA4_31_0 |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 23             | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAW_DATA4_31_0 |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 15             | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RAW_DATA4_31_0 |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |
| 7              | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RAW_DATA4_31_0 |    |    |    |    |    |    |    |
| R              |    |    |    |    |    |    |    |
| 0h             |    |    |    |    |    |    |    |

**Table 5-2464. MSS\_MCRC\_RAW\_DATAREGL4 Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                     |
|------|----------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:0 | RAW_DATA4_31_0 | R    | 0h    | Channel 4 Raw Data Low Register. This register contains bit 31:0 of the un-compressed raw data. |

### 5.13.2.60 MSS\_MCRC\_RAW\_DATAREGH4 Register

#### 1 MSS\_MCRC\_RAW\_DATAREGH4 Register (Offset = 13Ch) [reset = 0h]

Channel 4 un-compressed raw data high Register.

Return to [Summary Table](#)

**Table 5-2465. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 013Ch       |

**Figure 5-815. MSS\_MCRC\_RAW\_DATAREGH4 Name Register**

|                 |    |    |    |    |    |    |    |
|-----------------|----|----|----|----|----|----|----|
| 31              | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RAW_DATA4_63_32 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 23              | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RAW_DATA4_63_32 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 15              | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RAW_DATA4_63_32 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |
| 7               | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RAW_DATA4_63_32 |    |    |    |    |    |    |    |
| R               |    |    |    |    |    |    |    |
| 0h              |    |    |    |    |    |    |    |

**Table 5-2467. MSS\_MCRC\_RAW\_DATAREGH4 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                                                       |
|------|-----------------|------|-------|---------------------------------------------------------------------------------------------------|
| 31:0 | RAW_DATA4_63_32 | R    | 0h    | Channel 4 Raw Data High Register. This register contains bit 63:32 of the un-compressed raw data. |

### 5.13.2.61 MSS\_MCRC\_MCRC\_BUS\_SEL Register

#### 1 MSS\_MCRC\_MCRC\_BUS\_SEL Register (Offset = 140h) [reset = 7h]

Disables either or all tracing of data buses.

Return to [Summary Table](#)

**Table 5-2468. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCRC0         | 3500 0140h       |

**Figure 5-816. MSS\_MCRC\_MCRC\_BUS\_SEL Name Register**

|      |    |    |    |    |     |        |        |
|------|----|----|----|----|-----|--------|--------|
| 31   | 30 | 29 | 28 | 27 | 26  | 25     | 24     |
| NU67 |    |    |    |    |     |        |        |
| R    |    |    |    |    |     |        |        |
| 0h   |    |    |    |    |     |        |        |
| 23   | 22 | 21 | 20 | 19 | 18  | 17     | 16     |
| NU67 |    |    |    |    |     |        |        |
| R    |    |    |    |    |     |        |        |
| 0h   |    |    |    |    |     |        |        |
| 15   | 14 | 13 | 12 | 11 | 10  | 9      | 8      |
| NU67 |    |    |    |    |     |        |        |
| R    |    |    |    |    |     |        |        |
| 0h   |    |    |    |    |     |        |        |
| 7    | 6  | 5  | 4  | 3  | 2   | 1      | 0      |
| NU67 |    |    |    |    | MEN | DTCMEN | ITCMEN |
| R    |    |    |    |    | R/W | R/W    | R/W    |
| 0h   |    |    |    |    | 1h  | 1h     | 1h     |

**Table 5-2470. MSS\_MCRC\_MCRC\_BUS\_SEL Register Field Descriptions**

| Bit  | Field  | Type | Reset | Description                                                                                                                                                                    |
|------|--------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | NU67   | R    | 0h    | Reserved                                                                                                                                                                       |
| 2    | MEN    | R/W  | 1h    | MEN. Enable/disables the tracing of VBUSM<br>0:Tracing of VBUSM master bus has been disabled<br>1:Tracing of VBUSM master bus has been enabled                                 |
| 1    | DTCMEN | R/W  | 1h    | DTCMEN. Enable/disables the tracing of data TCM<br>0:Tracing of DTCM_ODD and DTCM_EVEN buses have been disabled<br>1:Tracing of DTCM_ODD and DTCM_EVEN buses have been enabled |
| 0    | ITCMEN | R/W  | 1h    | ITCMEN. Enable/disables the tracing of instruction TCM<br>0:Tracing of ITCM bus has been disabled<br>1:Tracing of ITCM bus has been enabled                                    |

## 5.14 MCSPI

### MCSPI

#### 5.14.1 MCSPI Summaries

#### MCSPI Summaries

**Table 5-2471. MCSPI Registers, Base Address=5220 0000h, Length=1024**

| Offset | Length | Register Name                      | MCSPi0 Physical Address | MCSPi1 Physical Address | MCSPi2 Physical Address |
|--------|--------|------------------------------------|-------------------------|-------------------------|-------------------------|
| 0h     | 32     | <a href="#">MCSPi_HL_REV</a>       | 5220 0000h              | 5220 1000h              | 5220 2000h              |
| 4h     | 32     | <a href="#">MCSPi_HL_HWINFO</a>    | 5220 0004h              | 5220 1004h              | 5220 2004h              |
| 10h    | 32     | <a href="#">MCSPi_HL_SYSCONFIG</a> | 5220 0010h              | 5220 1010h              | 5220 2010h              |
| 100h   | 32     | <a href="#">MCSPi_REVISION</a>     | 5220 0100h              | 5220 1100h              | 5220 2100h              |
| 114h   | 32     | <a href="#">MCSPi_SYSSTATUS</a>    | 5220 0114h              | 5220 1114h              | 5220 2114h              |
| 118h   | 32     | <a href="#">MCSPi_IRQSTATUS</a>    | 5220 0118h              | 5220 1118h              | 5220 2118h              |
| 11Ch   | 32     | <a href="#">MCSPi_IRQENABLE</a>    | 5220 011Ch              | 5220 111Ch              | 5220 211Ch              |
| 120h   | 32     | <a href="#">MCSPi_WAKEUPENABLE</a> | 5220 0120h              | 5220 1120h              | 5220 2120h              |
| 124h   | 32     | <a href="#">MCSPi_SYST</a>         | 5220 0124h              | 5220 1124h              | 5220 2124h              |
| 128h   | 32     | <a href="#">MCSPi_MODULCTRL</a>    | 5220 0128h              | 5220 1128h              | 5220 2128h              |
| 12Ch   | 32     | <a href="#">MCSPi_CH0CONF</a>      | 5220 012Ch              | 5220 112Ch              | 5220 212Ch              |
| 130h   | 32     | <a href="#">MCSPi_CH0STAT</a>      | 5220 0130h              | 5220 1130h              | 5220 2130h              |
| 134h   | 32     | <a href="#">MCSPi_CH0CTRL</a>      | 5220 0134h              | 5220 1134h              | 5220 2134h              |
| 138h   | 32     | <a href="#">MCSPi_TX0</a>          | 5220 0138h              | 5220 1138h              | 5220 2138h              |
| 13Ch   | 32     | <a href="#">MCSPi_RX0</a>          | 5220 013Ch              | 5220 113Ch              | 5220 213Ch              |
| 140h   | 32     | <a href="#">MCSPi_CH1CONF</a>      | 5220 0140h              | 5220 1140h              | 5220 2140h              |
| 144h   | 32     | <a href="#">MCSPi_CH1STAT</a>      | 5220 0144h              | 5220 1144h              | 5220 2144h              |
| 148h   | 32     | <a href="#">MCSPi_CH1CTRL</a>      | 5220 0148h              | 5220 1148h              | 5220 2148h              |
| 14Ch   | 32     | <a href="#">MCSPi_TX1</a>          | 5220 014Ch              | 5220 114Ch              | 5220 214Ch              |
| 150h   | 32     | <a href="#">MCSPi_RX1</a>          | 5220 0150h              | 5220 1150h              | 5220 2150h              |
| 154h   | 32     | <a href="#">MCSPi_CH2CONF</a>      | 5220 0154h              | 5220 1154h              | 5220 2154h              |
| 158h   | 32     | <a href="#">MCSPi_CH2STAT</a>      | 5220 0158h              | 5220 1158h              | 5220 2158h              |
| 15Ch   | 32     | <a href="#">MCSPi_CH2CTRL</a>      | 5220 015Ch              | 5220 115Ch              | 5220 215Ch              |
| 160h   | 32     | <a href="#">MCSPi_TX2</a>          | 5220 0160h              | 5220 1160h              | 5220 2160h              |
| 164h   | 32     | <a href="#">MCSPi_RX2</a>          | 5220 0164h              | 5220 1164h              | 5220 2164h              |
| 168h   | 32     | <a href="#">MCSPi_CH3CONF</a>      | 5220 0168h              | 5220 1168h              | 5220 2168h              |
| 16Ch   | 32     | <a href="#">MCSPi_CH3STAT</a>      | 5220 016Ch              | 5220 116Ch              | 5220 216Ch              |
| 170h   | 32     | <a href="#">MCSPi_CH3CTRL</a>      | 5220 0170h              | 5220 1170h              | 5220 2170h              |
| 174h   | 32     | <a href="#">MCSPi_TX3</a>          | 5220 0174h              | 5220 1174h              | 5220 2174h              |
| 178h   | 32     | <a href="#">MCSPi_RX3</a>          | 5220 0178h              | 5220 1178h              | 5220 2178h              |
| 17Ch   | 32     | <a href="#">MCSPi_XFERLEVEL</a>    | 5220 017Ch              | 5220 117Ch              | 5220 217Ch              |
| 180h   | 32     | <a href="#">MCSPi_DAFTX</a>        | 5220 0180h              | 5220 1180h              | 5220 2180h              |
| 1A0h   | 32     | <a href="#">MCSPi_DAFRX</a>        | 5220 01A0h              | 5220 11A0h              | 5220 21A0h              |

**Table 5-2472. MCSPI Registers, Base Address=5220 0000h, Length=1024**

| Offset | Length | Register Name                | MCSPi3 Physical Address | MCSPi4 Physical Address |
|--------|--------|------------------------------|-------------------------|-------------------------|
| 0h     | 32     | <a href="#">MCSPi_HL_REV</a> | 5220 3000h              | 5220 4000h              |

**Table 5-2472. MCSPI Registers, Base Address=5220 0000h, Length=1024 (continued)**

| Offset | Length | Register Name                      | MCSPI3 Physical Address | MCSPI4 Physical Address |
|--------|--------|------------------------------------|-------------------------|-------------------------|
| 4h     | 32     | <a href="#">MCSPI_HL_HWINFO</a>    | 5220 3004h              | 5220 4004h              |
| 10h    | 32     | <a href="#">MCSPI_HL_SYSCONFIG</a> | 5220 3010h              | 5220 4010h              |
| 100h   | 32     | <a href="#">MCSPI_REVISION</a>     | 5220 3100h              | 5220 4100h              |
| 114h   | 32     | <a href="#">MCSPI_SYSSTATUS</a>    | 5220 3114h              | 5220 4114h              |
| 118h   | 32     | <a href="#">MCSPI_IRQSTATUS</a>    | 5220 3118h              | 5220 4118h              |
| 11Ch   | 32     | <a href="#">MCSPI_IRQENABLE</a>    | 5220 311Ch              | 5220 411Ch              |
| 120h   | 32     | <a href="#">MCSPI_WAKEUPENABLE</a> | 5220 3120h              | 5220 4120h              |
| 124h   | 32     | <a href="#">MCSPI_SYST</a>         | 5220 3124h              | 5220 4124h              |
| 128h   | 32     | <a href="#">MCSPI_MODULCTRL</a>    | 5220 3128h              | 5220 4128h              |
| 12Ch   | 32     | <a href="#">MCSPI_CH0CONF</a>      | 5220 312Ch              | 5220 412Ch              |
| 130h   | 32     | <a href="#">MCSPI_CH0STAT</a>      | 5220 3130h              | 5220 4130h              |
| 134h   | 32     | <a href="#">MCSPI_CH0CTRL</a>      | 5220 3134h              | 5220 4134h              |
| 138h   | 32     | <a href="#">MCSPI_TX0</a>          | 5220 3138h              | 5220 4138h              |
| 13Ch   | 32     | <a href="#">MCSPI_RX0</a>          | 5220 313Ch              | 5220 413Ch              |
| 140h   | 32     | <a href="#">MCSPI_CH1CONF</a>      | 5220 3140h              | 5220 4140h              |
| 144h   | 32     | <a href="#">MCSPI_CH1STAT</a>      | 5220 3144h              | 5220 4144h              |
| 148h   | 32     | <a href="#">MCSPI_CH1CTRL</a>      | 5220 3148h              | 5220 4148h              |
| 14Ch   | 32     | <a href="#">MCSPI_TX1</a>          | 5220 314Ch              | 5220 414Ch              |
| 150h   | 32     | <a href="#">MCSPI_RX1</a>          | 5220 3150h              | 5220 4150h              |
| 154h   | 32     | <a href="#">MCSPI_CH2CONF</a>      | 5220 3154h              | 5220 4154h              |
| 158h   | 32     | <a href="#">MCSPI_CH2STAT</a>      | 5220 3158h              | 5220 4158h              |
| 15Ch   | 32     | <a href="#">MCSPI_CH2CTRL</a>      | 5220 315Ch              | 5220 415Ch              |
| 160h   | 32     | <a href="#">MCSPI_TX2</a>          | 5220 3160h              | 5220 4160h              |
| 164h   | 32     | <a href="#">MCSPI_RX2</a>          | 5220 3164h              | 5220 4164h              |
| 168h   | 32     | <a href="#">MCSPI_CH3CONF</a>      | 5220 3168h              | 5220 4168h              |
| 16Ch   | 32     | <a href="#">MCSPI_CH3STAT</a>      | 5220 316Ch              | 5220 416Ch              |
| 170h   | 32     | <a href="#">MCSPI_CH3CTRL</a>      | 5220 3170h              | 5220 4170h              |
| 174h   | 32     | <a href="#">MCSPI_TX3</a>          | 5220 3174h              | 5220 4174h              |
| 178h   | 32     | <a href="#">MCSPI_RX3</a>          | 5220 3178h              | 5220 4178h              |
| 17Ch   | 32     | <a href="#">MCSPI_XFERLEVEL</a>    | 5220 317Ch              | 5220 417Ch              |
| 180h   | 32     | <a href="#">MCSPI_DAFTX</a>        | 5220 3180h              | 5220 4180h              |
| 1A0h   | 32     | <a href="#">MCSPI_DAFRX</a>        | 5220 31A0h              | 5220 41A0h              |

### 5.14.2 MCSPI Registers

#### MCSPI Registers

### 5.14.2.1 MCSPI\_HL\_REV Register

#### 1 MCSPI\_HL\_REV Register (Offset = 0h) [reset = 40301A0Bh]

IP Revision Identifier (X.Y.R)

Used by software to track features, bugs, and compatibility.

Return to [Summary Table](#)

**Table 5-2473. Instance Table**

| Instance Name | Physical Address  |
|---------------|-------------------|
| <b>MCSPi0</b> | <b>5220 0000h</b> |
| <b>MCSPi1</b> | <b>5220 1000h</b> |
| <b>MCSPi2</b> | <b>5220 2000h</b> |
| <b>MCSPi3</b> | <b>5220 3000h</b> |
| <b>MCSPi4</b> | <b>5220 4000h</b> |

**Figure 5-817. MCSPI\_HL\_REV Name Register**

|        |    |         |    |      |         |    |    |
|--------|----|---------|----|------|---------|----|----|
| 31     | 30 | 29      | 28 | 27   | 26      | 25 | 24 |
| SCHEME |    | RSVD    |    | FUNC |         |    |    |
| R      |    | R       |    | R    |         |    |    |
| 1h     |    | 0h      |    | 30h  |         |    |    |
| 23     | 22 | 21      | 20 | 19   | 18      | 17 | 16 |
| FUNC   |    |         |    |      |         |    |    |
| R      |    |         |    |      |         |    |    |
| 30h    |    |         |    |      |         |    |    |
| 15     | 14 | 13      | 12 | 11   | 10      | 9  | 8  |
| R_RTL  |    |         |    |      | X_MAJOR |    |    |
| R      |    |         |    |      | R       |    |    |
| 3h     |    |         |    |      | 2h      |    |    |
| 7      | 6  | 5       | 4  | 3    | 2       | 1  | 0  |
| CUSTOM |    | Y_MINOR |    |      |         |    |    |
| R      |    | R       |    |      |         |    |    |
| 0h     |    | Bh      |    |      |         |    |    |

**Table 5-2475. MCSPI\_HL\_REV Register Field Descriptions**

| Bit   | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|--------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | SCHEME | R    | 1h    | Used to distinguish between old scheme and current                                                                                                                                                                                                                                                                                                                                                                                  |
| 29:28 | RSVD   | R    | 0h    | Reserved These bits are initialized to zero, and writes to them are ignored                                                                                                                                                                                                                                                                                                                                                         |
| 27:16 | FUNC   | R    | 30h   | Function indicates a software compatible module family If there is no level of software compatibility a new Func number [and hence REVISION] should be assigned                                                                                                                                                                                                                                                                     |
| 15:11 | R_RTL  | R    | 3h    | RTL Version [R], maintained by IP design owner RTL follows a numbering such as XYZ which are explained in this table R changes ONLY when: [1] PDS uploads occur which may have been due to spec changes [2] Bug fixes occur [3] Resets to '0' when X or Y changes Design team has an internal 'Z' [customer invisible] number which increments on every drop that happens due to DV and RTL updates Z resets to 0 when R increments |

**Table 5-2475. MCSPI\_HL\_REV Register Field Descriptions (continued)**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------|---------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10:8 | X_MAJOR | R    | 2h    | Major Revision [X], maintained by IP specification owner X changes ONLY when: [1] There is a major feature addition An example would be adding Controller Mode to Utopia Level2 The Func field [or Class/ Type in old PID format] will remain the same X does NOT change due to: [1] Bug fixes [2] Change in feature parameters                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 7:6  | CUSTOM  | R    | 0h    | Indicates a special version for a particular device Consequence of use may avoid use of standard Chip Support Library [CSL] / Drivers                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 5:0  | Y_MINOR | R    | Bh    | Minor Revision [Y], maintained by IP specification owner Y changes ONLY when: [1] Features are scaled [up or down] Flexibility exists in that this feature scalability may either be represented in the Y change or a specific register in the IP that indicates which features are exactly available [2] When feature creeps from Is-Not list to Is list But this may not be the case once it sees silicon; in which case X will change Y does NOT change due to: [1] Bug fixes [2] Typos or clarifications [3] major functional/feature change/addition/ deletion Instead these changes may be reflected via R, S, X as applicable Spec owner maintains a customer-invisible number 'S' which changes due to: [1] Typos/clarifications [2] Bug documentation Note that this bug is not due to a spec change but due to implementation Nevertheless, the spec tracks the IP bugs An RTL release [say for silicon PG11] that occurs due to bug fix should document the corresponding spec number [XYS] in its release notes |



### 5.14.2.2 MCSPI\_HL\_HWINFO Register

#### 1 MCSPI\_HL\_HWINFO Register (Offset = 4h) [reset = 9h]

Information about the IP module's hardware configuration, i.e. typically the module's HDL generics (if any). Actual field format and encoding is up to the module's designer to decide.

Return to [Summary Table](#)

**Table 5-2476. Instance Table**

| Instance Name | Physical Address  |
|---------------|-------------------|
| <b>MCSPI0</b> | <b>5220 0004h</b> |
| <b>MCSPI1</b> | <b>5220 1004h</b> |
| <b>MCSPI2</b> | <b>5220 2004h</b> |
| <b>MCSPI3</b> | <b>5220 3004h</b> |
| <b>MCSPI4</b> | <b>5220 4004h</b> |

**Figure 5-818. MCSPI\_HL\_HWINFO Name Register**

|      |         |         |    |    |    |         |    |
|------|---------|---------|----|----|----|---------|----|
| 31   | 30      | 29      | 28 | 27 | 26 | 25      | 24 |
| RSVD |         |         |    |    |    |         |    |
| R    |         |         |    |    |    |         |    |
| 0h   |         |         |    |    |    |         |    |
| 23   | 22      | 21      | 20 | 19 | 18 | 17      | 16 |
| RSVD |         |         |    |    |    |         |    |
| R    |         |         |    |    |    |         |    |
| 0h   |         |         |    |    |    |         |    |
| 15   | 14      | 13      | 12 | 11 | 10 | 9       | 8  |
| RSVD |         |         |    |    |    |         |    |
| R    |         |         |    |    |    |         |    |
| 0h   |         |         |    |    |    |         |    |
| 7    | 6       | 5       | 4  | 3  | 2  | 1       | 0  |
| RSVD | RETMODE | FFNBYTE |    |    |    | USEFIFO |    |
| R    | R       | R       |    |    |    | R       |    |
| 0h   | 0h      | 4h      |    |    |    | 1h      |    |

**Table 5-2478. MCSPI\_HL\_HWINFO Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                               |
|------|---------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RSVD    | R    | 0h    | Reserved These bits are initialized to zero, and writes to them are ignored                                                                                                                                                                                                               |
| 6    | RETMODE | R    | 0h    | This bit field indicates whether the retention mode is supported using the pin PIRFFRET<br>0 Retention mode disabled<br>1 Retention mode enabled                                                                                                                                          |
| 5:1  | FFNBYTE | R    | 4h    | FIFO number of byte generic parameter This register defines the value of FFNBYTE generic parameter, only MSB bits from 8 down to 4 are taken into account<br>1 FIFO 16 bytes depth<br>2 FIFO 32 bytes depth<br>4 FIFO 64 bytes depth<br>8 FIFO 128 bytes depth<br>10 FIFO 256 bytes depth |

**Table 5-2478. MCSPI\_HL\_HWINFO Register Field Descriptions (continued)**

| Bit | Field   | Type | Reset | Description                                                                                                                                                                                                                                                             |
|-----|---------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | USEFIFO | R    | 1h    | <p>Use of a FIFO enable: This bit field indicates if a FIFO is integrated within controller design with its management</p> <p>0      FIFO not implemented in design<br/> 1      FIFO and its management implemented in design with depth defined by FFNBYTE generic</p> |

### 5.14.2.3 MCSPI\_HL\_SYSCONFIG Register

#### 1 MCSPI\_HL\_SYSCONFIG Register (Offset = 10h) [reset = 8h]

Clock management configuration.

Return to [Summary Table](#)

**Table 5-2479. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCSPI0        | 5220 0010h       |
| MCSPI1        | 5220 1010h       |
| MCSPI2        | 5220 2010h       |
| MCSPI3        | 5220 3010h       |
| MCSPI4        | 5220 4010h       |

**Figure 5-819. MCSPI\_HL\_SYSCONFIG Name Register**

|      |    |    |    |          |    |         |           |
|------|----|----|----|----------|----|---------|-----------|
| 31   | 30 | 29 | 28 | 27       | 26 | 25      | 24        |
| RSVD |    |    |    |          |    |         |           |
| R    |    |    |    |          |    |         |           |
| 0h   |    |    |    |          |    |         |           |
| 23   | 22 | 21 | 20 | 19       | 18 | 17      | 16        |
| RSVD |    |    |    |          |    |         |           |
| R    |    |    |    |          |    |         |           |
| 0h   |    |    |    |          |    |         |           |
| 15   | 14 | 13 | 12 | 11       | 10 | 9       | 8         |
| RSVD |    |    |    |          |    |         |           |
| R    |    |    |    |          |    |         |           |
| 0h   |    |    |    |          |    |         |           |
| 7    | 6  | 5  | 4  | 3        | 2  | 1       | 0         |
| RSVD |    |    |    | IDLEMODE |    | FREEEMU | SOFTRESET |
| R    |    |    |    | R/W      |    | R/W     | R/W       |
| 0h   |    |    |    | 2h       |    | 0h      | 0h        |

**Table 5-2481. MCSPI\_HL\_SYSCONFIG Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:4 | RSVD     | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 3:2  | IDLEMODE | R/W  | 2h    | Configuration of the local target state management mode By definition, target can handle read/write transaction as long as it is out of IDLE state<br>0 Force-idle mode: local target's IDLE state follows (acknowledges) the system's clock stop requests unconditionally, that is, regardless of the IP module's internal requirements. Backup mode, for debug only.<br>1 No-idle mode: local target never enters IDLE state. Backup mode, for debug only.<br>2 Smart-idle mode: local target's IDLE state eventually follows (acknowledges) the system's clock stop requests, depending on the IP module's internal requirements. IP module shall not generate (IRQ- or DMA-request-related) wake-up events. |

**Table 5-2481. MCSPI\_HL\_SYSCONFIG Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description                                                                                                                                                                           |
|-----|-----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | FREEEMU   | R/W  | 0h    | Sensitivity to emulation [debug] suspend input signal<br>0 IP module is sensitive to emulation suspend.<br>1 IP module is not sensitive to emulation suspend.                         |
| 0   | SOFTRESET | R/W  | 0h    | Software reset [Optional]<br>0 Read 0 - Reset done, no pending action<br>0 Write 0 - No Action<br>1 Read 1 - Reset (software or other) ongoing<br>1 Write 1 - Initiate software reset |

#### 5.14.2.4 MCSPI\_REVISION Register

##### 1 MCSPI\_REVISION Register (Offset = 100h) [reset = 2Bh]

This register contains the hard coded RTL revision number.

Return to [Summary Table](#)

**Table 5-2482. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCSPI0        | 5220 0100h       |
| MCSPI1        | 5220 1100h       |
| MCSPI2        | 5220 2100h       |
| MCSPI3        | 5220 3100h       |
| MCSPI4        | 5220 4100h       |

**Figure 5-820. MCSPI\_REVISION Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_13 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_13 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_13 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| REV         |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 2Bh         |    |    |    |    |    |    |    |

**Table 5-2484. MCSPI\_REVISION Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                              |
|------|-------------|------|-------|------------------------------------------------------------------------------------------|
| 31:8 | RESERVED_13 | R    | 0h    | Reads returns 0                                                                          |
| 7:0  | REV         | R    | 2Bh   | IP revision [7:4] Major revision [3:0] Minor revision Examples: 0x10 for 10, 0x21 for 21 |

### 5.14.2.5 MCSPI\_SYSSTATUS Register

#### 1 MCSPI\_SYSSTATUS Register (Offset = 114h) [reset = 1h]

This register provides status information about the module excluding the interrupt status information .

Return to [Summary Table](#)

**Table 5-2485. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCSPI0        | 5220 0114h       |
| MCSPI1        | 5220 1114h       |
| MCSPI2        | 5220 2114h       |
| MCSPI3        | 5220 3114h       |
| MCSPI4        | 5220 4114h       |

**Figure 5-821. MCSPI\_SYSSTATUS Name Register**

|             |    |    |    |    |    |    |           |
|-------------|----|----|----|----|----|----|-----------|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24        |
| RESERVED_16 |    |    |    |    |    |    |           |
| R           |    |    |    |    |    |    |           |
| 0h          |    |    |    |    |    |    |           |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16        |
| RESERVED_16 |    |    |    |    |    |    |           |
| R           |    |    |    |    |    |    |           |
| 0h          |    |    |    |    |    |    |           |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8         |
| RESERVED_16 |    |    |    |    |    |    |           |
| R           |    |    |    |    |    |    |           |
| 0h          |    |    |    |    |    |    |           |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0         |
| RESERVED_16 |    |    |    |    |    |    | RESETDONE |
| R           |    |    |    |    |    |    | R         |
| 0h          |    |    |    |    |    |    | 1h        |

**Table 5-2487. MCSPI\_SYSSTATUS Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                          |
|------|-------------|------|-------|--------------------------------------------------------------------------------------|
| 31:1 | RESERVED_16 | R    | 0h    | Reserved for module specific status information Read returns 0                       |
| 0    | RESETDONE   | R    | 1h    | Internal Reset Monitoring<br>0 Internal module reset is ongoing<br>1 Reset completed |

### 5.14.2.6 MCSPI\_IRQSTATUS Register

#### 1 MCSPI\_IRQSTATUS Register (Offset = 118h) [reset = 0h]

The interrupt status regroups all the status of the module internal events that can generate an interrupt .

Return to [Summary Table](#)

**Table 5-2488. Instance Table**

| Instance Name | Physical Address  |
|---------------|-------------------|
| <b>MCSPi0</b> | <b>5220 0118h</b> |
| <b>MCSPi1</b> | <b>5220 1118h</b> |
| <b>MCSPi2</b> | <b>5220 2118h</b> |
| <b>MCSPi3</b> | <b>5220 3118h</b> |
| <b>MCSPi4</b> | <b>5220 4118h</b> |

**Figure 5-822. MCSPI\_IRQSTATUS Name Register**

|             |          |                   |           |                  |          |                   |           |
|-------------|----------|-------------------|-----------|------------------|----------|-------------------|-----------|
| 31          | 30       | 29                | 28        | 27               | 26       | 25                | 24        |
| RESERVED_8  |          |                   |           |                  |          |                   |           |
| R           |          |                   |           |                  |          |                   |           |
| 0h          |          |                   |           |                  |          |                   |           |
| 23          | 22       | 21                | 20        | 19               | 18       | 17                | 16        |
| RESERVED_8  |          |                   |           |                  |          | EOW               | WKS       |
| R           |          |                   |           |                  |          | R/W1TS            | R/W1TS    |
| 0h          |          |                   |           |                  |          | 0h                | 0h        |
| 15          | 14       | 13                | 12        | 11               | 10       | 9                 | 8         |
| RESERVED_7  | RX3_FULL | TX3_UNDERFL<br>OW | TX3_EMPTY | RESERVED_9       | RX2_FULL | TX2_UNDERFL<br>OW | TX2_EMPTY |
| R           | R/W1TS   | R/W1TS            | R/W1TS    | R                | R/W1TS   | R/W1TS            | R/W1TS    |
| 0h          | 0h       | 0h                | 0h        | 0h               | 0h       | 0h                | 0h        |
| 7           | 6        | 5                 | 4         | 3                | 2        | 1                 | 0         |
| RESERVED_10 | RX1_FULL | TX1_UNDERFL<br>OW | TX1_EMPTY | RX0_OVERFL<br>OW | RX0_FULL | TX0_UNDERFL<br>OW | TX0_EMPTY |
| R           | R/W1TS   | R/W1TS            | R/W1TS    | R/W1TS           | R/W1TS   | R/W1TS            | R/W1TS    |
| 0h          | 0h       | 0h                | 0h        | 0h               | 0h       | 0h                | 0h        |

**Table 5-2490. MCSPI\_IRQSTATUS Register Field Descriptions**

| Bit   | Field      | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                  |
|-------|------------|--------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED_8 | R      | 0h    | Reads returns 0                                                                                                                                                                                                                                                                                                              |
| 17    | EOW        | R/W1TS | 0h    | End of word count event when a channel is enabled using the FIFO buffer and the channel had sent the number of SPI word defined by MCSPI_XFERLEVEL[WCNT]<br><br>0      Read 0 - Event false<br>0      Write 0 - Event status bit Unchanged<br>1      Read 1 - Event is Pending<br>1      Write 1 - Event status bit is reset |
| 16    | WKS        | R/W1TS | 0h    | Wake Up event in responder mode when an active control signal is detected on the SPIEN line programmed in the field MCSPI_CH0CONF[SPIENSLV]<br><br>0      Read 0 - Event false<br>0      Write 0 - Event status bit Unchanged<br>1      Read 1 - Event is Pending<br>1      Write 1 - Event status bit is reset              |
| 15    | RESERVED_7 | R      | 0h    | Reads returns 0                                                                                                                                                                                                                                                                                                              |

**Table 5-2490. MCSPI\_IRQSTATUS Register Field Descriptions (continued)**

| Bit | Field         | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-----|---------------|--------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14  | RX3_FULL      | R/W1TS | 0h    | Receiver register is full or almost full Only when Channel 3 is enabled<br>0 Read 0 - Event false<br>0 Write 0 - Event status bit Unchanged<br>1 Read 1 - Event is Pending<br>1 Write 1 - Event status bit is reset                                                                                                                                                                                                                               |
| 13  | TX3_UNDERFLOW | R/W1TS | 0h    | Transmitter register underflow Only when Channel 3 is enabled The transmitter register is empty [not updated by Host or DMA with new data] before its time slot assignment Exception: No TX_underflow event when no data has been loaded into the transmitter register since channel has been enabled<br>0 Read 0 - Event false<br>0 Write 0 - Event status bit Unchanged<br>1 Read 1 - Event is Pending<br>1 Write 1 - Event status bit is reset |
| 12  | TX3_EMPTY     | R/W1TS | 0h    | Transmitter register is empty or almost empty Note: Enabling the channel automatically rises this event<br>0 Read 0 - Event false<br>0 Write 0 - Event status bit Unchanged<br>1 Read 1 - Event is Pending<br>1 Write 1 - Event status bit is reset                                                                                                                                                                                               |
| 11  | RESERVED_9    | R      | 0h    | Reads returns 0                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 10  | RX2_FULL      | R/W1TS | 0h    | Receiver register full or almost full Channel 2<br>0 Read 0 - Event false<br>0 Write 0 - Event status bit Unchanged<br>1 Read 1 - Event is Pending<br>1 Write 1 - Event status bit is reset                                                                                                                                                                                                                                                       |
| 9   | TX2_UNDERFLOW | R/W1TS | 0h    | Transmitter register underflow Channel 2<br>0 Read 0 - Event false<br>0 Write 0 - Event status bit Unchanged<br>1 Read 1 - Event is Pending<br>1 Write 1 - Event status bit is reset                                                                                                                                                                                                                                                              |
| 8   | TX2_EMPTY     | R/W1TS | 0h    | Transmitter register empty or almost empty Channel 2<br>0 Read 0 - Event false<br>0 Write 0 - Event status bit Unchanged<br>1 Read 1 - Event is Pending<br>1 Write 1 - Event status bit is reset                                                                                                                                                                                                                                                  |
| 7   | RESERVED_10   | R      | 0h    | Reads returns 0                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 6   | RX1_FULL      | R/W1TS | 0h    | Receiver register full or almost full Channel 1<br>0 Read 0 - Event false<br>0 Write 0 - Event status bit Unchanged<br>1 Read 1 - Event is Pending<br>1 Write 1 - Event status bit is reset                                                                                                                                                                                                                                                       |
| 5   | TX1_UNDERFLOW | R/W1TS | 0h    | Transmitter register underflow Channel 1<br>0 Read 0 - Event false<br>0 Write 0 - Event status bit Unchanged<br>1 Read 1 - Event is Pending<br>1 Write 1 - Event status bit is reset                                                                                                                                                                                                                                                              |
| 4   | TX1_EMPTY     | R/W1TS | 0h    | Transmitter register empty or almost empty Channel 1<br>0 Read 0 - Event false<br>0 Write 0 - Event status bit Unchanged<br>1 Read 1 - Event is Pending<br>1 Write 1 - Event status bit is reset                                                                                                                                                                                                                                                  |
| 3   | RX0_OVERFLOW  | R/W1TS | 0h    | Receiver register overflow [responder mode only] Channel 0<br>0 Event status bit unchanged<br>1 Event is pending                                                                                                                                                                                                                                                                                                                                  |



**Table 5-2490. MCSPI\_IRQSTATUS Register Field Descriptions (continued)**

| Bit | Field         | Type   | Reset | Description                                                                                                                                                                                                              |
|-----|---------------|--------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | RX0_FULL      | R/W1TS | 0h    | Receiver register full or almost full Channel 0<br><br>0      Read 0 - Event false<br>0      Write 0 - Event status bit Unchanged<br>1      Read 1 - Event is Pending<br>1      Write 1 - Event status bit is reset      |
| 1   | TX0_UNDERFLOW | R/W1TS | 0h    | Transmitter register underflow Channel 0<br><br>0      Read 0 - Event false<br>0      Write 0 - Event status bit Unchanged<br>1      Read 1 - Event is Pending<br>1      Write 1 - Event status bit is reset             |
| 0   | TX0_EMPTY     | R/W1TS | 0h    | Transmitter register empty or almost empty Channel 0<br><br>0      Read 0 - Event false<br>0      Write 0 - Event status bit Unchanged<br>1      Read 1 - Event is Pending<br>1      Write 1 - Event status bit is reset |

### 5.14.2.7 MCSPI\_IRQENABLE Register

#### 1 MCSPI\_IRQENABLE Register (Offset = 11Ch) [reset = 0h]

This register allows to enable/disable the module internal sources of interrupt, on an event-by-event basis.

Return to [Summary Table](#)

**Table 5-2491. Instance Table**

| Instance Name | Physical Address  |
|---------------|-------------------|
| <b>MCSPI0</b> | <b>5220 011Ch</b> |
| <b>MCSPI1</b> | <b>5220 111Ch</b> |
| <b>MCSPI2</b> | <b>5220 211Ch</b> |
| <b>MCSPI3</b> | <b>5220 311Ch</b> |
| <b>MCSPI4</b> | <b>5220 411Ch</b> |

**Figure 5-823. MCSPI\_IRQENABLE Name Register**

|            |                 |                      |                  |                     |                 |                      |                  |
|------------|-----------------|----------------------|------------------|---------------------|-----------------|----------------------|------------------|
| 31         | 30              | 29                   | 28               | 27                  | 26              | 25                   | 24               |
| RESERVED_5 |                 |                      |                  |                     |                 |                      |                  |
| R          |                 |                      |                  |                     |                 |                      |                  |
| 0h         |                 |                      |                  |                     |                 |                      |                  |
| 23         | 22              | 21                   | 20               | 19                  | 18              | 17                   | 16               |
| RESERVED_5 |                 |                      |                  |                     |                 | EOW_ENABLE           | WKE              |
| R          |                 |                      |                  |                     |                 | R/W                  | R/W              |
| 0h         |                 |                      |                  |                     |                 | 0h                   | 0h               |
| 15         | 14              | 13                   | 12               | 11                  | 10              | 9                    | 8                |
| RESERVED_4 | RX3_FULL_ENABLE | TX3_UNDERFLOW_ENABLE | TX3_EMPTY_ENABLE | RESERVED_6          | RX2_FULL_ENABLE | TX2_UNDERFLOW_ENABLE | TX2_EMPTY_ENABLE |
| R          | R/W             | R/W                  | R/W              | R                   | R/W             | R/W                  | R/W              |
| 0h         | 0h              | 0h                   | 0h               | 0h                  | 0h              | 0h                   | 0h               |
| 7          | 6               | 5                    | 4                | 3                   | 2               | 1                    | 0                |
| RESERVED_3 | RX1_FULL_ENABLE | TX1_UNDERFLOW_ENABLE | TX1_EMPTY_ENABLE | RX0_OVERFLOW_ENABLE | RX0_FULL_ENABLE | TX0_UNDERFLOW_ENABLE | TX0_EMPTY_ENABLE |
| R          | R/W             | R/W                  | R/W              | R/W                 | R/W             | R/W                  | R/W              |
| 0h         | 0h              | 0h                   | 0h               | 0h                  | 0h              | 0h                   | 0h               |

**Table 5-2493. MCSPI\_IRQENABLE Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                 |
|-------|-----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:18 | RESERVED_5      | R    | 0h    | Reads return 0                                                                                                                                                                                              |
| 17    | EOW_ENABLE      | R/W  | 0h    | End of Word count Interrupt Enable<br>0 Interrupt disabled<br>1 Interrupt enabled                                                                                                                           |
| 16    | WKE             | R/W  | 0h    | Wake Up event interrupt Enable in responder mode when an active control signal is detected on the SPIEN line programmed in the field MCSPI_CH0CONF[SPIENSLV]<br>0 Interrupt disabled<br>1 Interrupt enabled |
| 15    | RESERVED_4      | R    | 0h    | Reads returns 0                                                                                                                                                                                             |
| 14    | RX3_FULL_ENABLE | R/W  | 0h    | Receiver register Full Interrupt Enable Ch 3<br>0 Interrupt disabled<br>1 Interrupt enabled                                                                                                                 |

**Table 5-2493. MCSPI\_IRQENABLE Register Field Descriptions (continued)**

| Bit | Field                | Type | Reset | Description                                                                                                   |
|-----|----------------------|------|-------|---------------------------------------------------------------------------------------------------------------|
| 13  | TX3_UNDERFLOW_ENABLE | R/W  | 0h    | Transmitter register Underflow Interrupt Enable Ch 3<br>0      Interrupt disabled<br>1      Interrupt enabled |
| 12  | TX3_EMPTY_ENABLE     | R/W  | 0h    | Transmitter register Empty Interrupt Enable Ch3<br>0      Interrupt disabled<br>1      Interrupt enabled      |
| 11  | RESERVED_6           | R    | 0h    | Reads return 0                                                                                                |
| 10  | RX2_FULL_ENABLE      | R/W  | 0h    | Receiver register Full Interrupt Enable Ch 2<br>0      Interrupt disabled<br>1      Interrupt enabled         |
| 9   | TX2_UNDERFLOW_ENABLE | R/W  | 0h    | Transmitter register Underflow Interrupt Enable Ch 2<br>0      Interrupt disabled<br>1      Interrupt enabled |
| 8   | TX2_EMPTY_ENABLE     | R/W  | 0h    | Transmitter register Empty Interrupt Enable Ch 2<br>0      Interrupt disabled<br>1      Interrupt enabled     |
| 7   | RESERVED_3           | R    | 0h    | Reads return 0                                                                                                |
| 6   | RX1_FULL_ENABLE      | R/W  | 0h    | Receiver register Full Interrupt Enable Ch 1<br>0      Interrupt disabled<br>1      Interrupt enabled         |
| 5   | TX1_UNDERFLOW_ENABLE | R/W  | 0h    | Transmitter register Underflow Interrupt Enable Ch 1<br>0      Interrupt disabled<br>1      Interrupt enabled |
| 4   | TX1_EMPTY_ENABLE     | R/W  | 0h    | Transmitter register Empty Interrupt Enable Ch 1<br>0      Interrupt disabled<br>1      Interrupt enabled     |
| 3   | RX0_OVERFLOW_ENABLE  | R/W  | 0h    | Receiver register Overflow Interrupt Enable Ch 0<br>0      Interrupt disabled<br>1      Interrupt enabled     |
| 2   | RX0_FULL_ENABLE      | R/W  | 0h    | Receiver register Full Interrupt Enable Ch 0<br>0      Interrupt disabled<br>1      Interrupt enabled         |
| 1   | TX0_UNDERFLOW_ENABLE | R/W  | 0h    | Transmitter register Underflow Interrupt Enable Ch 0<br>0      Interrupt disabled<br>1      Interrupt enabled |
| 0   | TX0_EMPTY_ENABLE     | R/W  | 0h    | Transmitter register Empty Interrupt Enable Ch 0<br>0      Interrupt disabled<br>1      Interrupt enabled     |

### 5.14.2.8 MCSPI\_WAKEUPENABLE Register

#### 1 MCSPI\_WAKEUPENABLE Register (Offset = 120h) [reset = 0h]

The wakeup enable register allows to enable/disable the module internal sources of wakeup on event-by-event basis.

Return to [Summary Table](#)

**Table 5-2494. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCSPI0        | 5220 0120h       |
| MCSPI1        | 5220 1120h       |
| MCSPI2        | 5220 2120h       |
| MCSPI3        | 5220 3120h       |
| MCSPI4        | 5220 4120h       |

**Figure 5-824. MCSPI\_WAKEUPENABLE Name Register**

|             |    |    |    |    |    |    |      |
|-------------|----|----|----|----|----|----|------|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24   |
| RESERVED_18 |    |    |    |    |    |    |      |
| R           |    |    |    |    |    |    |      |
| 0h          |    |    |    |    |    |    |      |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16   |
| RESERVED_18 |    |    |    |    |    |    |      |
| R           |    |    |    |    |    |    |      |
| 0h          |    |    |    |    |    |    |      |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8    |
| RESERVED_18 |    |    |    |    |    |    |      |
| R           |    |    |    |    |    |    |      |
| 0h          |    |    |    |    |    |    |      |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0    |
| RESERVED_18 |    |    |    |    |    |    | WKEN |
| R           |    |    |    |    |    |    | R/W  |
| 0h          |    |    |    |    |    |    | 0h   |

**Table 5-2496. MCSPI\_WAKEUPENABLE Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                               |
|------|-------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED_18 | R    | 0h    | Reads returns 0                                                                                                                                                                                                                                                                                                                                                                                           |
| 0    | WKEN        | R/W  | 0h    | <p>WakeUp functionality in responder mode when an active control signal is detected on the SPIEN line programmed in the field MCSPI_CH0CONF[SPIENSLV]</p> <p>0 The event is not allowed to wake-up the system, even if the global control bit MCSPI_SYSCONFIG[2] ENAWAKEUP is set.</p> <p>1 The event is allowed to wake-up the system if the global control bit MCSPI_SYSCONFIG[2] ENAWAKEUP is set.</p> |

### 5.14.2.9 MCSPI\_SYST Register

#### 1 MCSPI\_SYST Register (Offset = 124h) [reset = 0h]

This register is used to check the correctness of the system interconnect either internally to peripheral bus, or externally to device IO pads, when the module is configured in system test (SYSTEST) mode.

Return to [Summary Table](#)

**Table 5-2497. Instance Table**

| Instance Name | Physical Address  |
|---------------|-------------------|
| <b>MCSPI0</b> | <b>5220 0124h</b> |
| <b>MCSPI1</b> | <b>5220 1124h</b> |
| <b>MCSPI2</b> | <b>5220 2124h</b> |
| <b>MCSPI3</b> | <b>5220 3124h</b> |
| <b>MCSPI4</b> | <b>5220 4124h</b> |

**Figure 5-825. MCSPI\_SYST Name Register**

|             |        |          |          |         |          |            |            |
|-------------|--------|----------|----------|---------|----------|------------|------------|
| 31          | 30     | 29       | 28       | 27      | 26       | 25         | 24         |
| RESERVED_17 |        |          |          |         |          |            |            |
| R           |        |          |          |         |          |            |            |
| 0h          |        |          |          |         |          |            |            |
| 23          | 22     | 21       | 20       | 19      | 18       | 17         | 16         |
| RESERVED_17 |        |          |          |         |          |            |            |
| R           |        |          |          |         |          |            |            |
| 0h          |        |          |          |         |          |            |            |
| 15          | 14     | 13       | 12       | 11      | 10       | 9          | 8          |
| RESERVED_17 |        |          |          | SSB     | SPIENDIR | SPIDATDIR1 | SPIDATDIR0 |
| R           |        |          |          | R/W     | R/W      | R/W        | R/W        |
| 0h          |        |          |          | 0h      | 0h       | 0h         | 0h         |
| 7           | 6      | 5        | 4        | 3       | 2        | 1          | 0          |
| WAKD        | SPICLK | SPIDAT_1 | SPIDAT_0 | SPIEN_3 | SPIEN_2  | SPIEN_1    | SPIEN_0    |
| R/W         | R/W    | R/W      | R/W      | R/W     | R/W      | R/W        | R/W        |
| 0h          | 0h     | 0h       | 0h       | 0h      | 0h       | 0h         | 0h         |

**Table 5-2499. MCSPI\_SYST Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                    |
|-------|-------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED_17 | R    | 0h    | Reads returns 0                                                                                                                                                                                                                                                                                                                |
| 11    | SSB         | R/W  | 0h    | Set status bit<br>0 No action. writing 0 does not clear already set status bits. This bit must be cleared before trying to clear a status bit of the MCSPI_IRQSTATUS register.<br>1 Force to 1 all status bits of MCSPI_IRQSTATUS register. writing 1 into this bit sets to 1 all status bits in the MCSPI_IRQSTATUS register. |
| 10    | SPIENDIR    | R/W  | 0h    | Set the direction of the SPIEN[3:0] lines and SPICLK line<br>0 Output (as in controller mode)<br>1 Input (as in peripheral mode)                                                                                                                                                                                               |
| 9     | SPIDATDIR1  | R/W  | 0h    | Set the direction of the SPIDAT[1]<br>0 Output<br>1 Input                                                                                                                                                                                                                                                                      |

**Table 5-2499. MCSPI\_SYST Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                        |
|-----|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8   | SPIDATDIR0 | R/W  | 0h    | Set the direction of the SPIDAT[0]<br><br>0        Output<br>1        Input                                                                                                                                                                                                                                                                        |
| 7   | WAKD       | R/W  | 0h    | SWAKEUP output [signal data value of internal signal to system] The signal is driven high or low according to the value written into this register bit<br><br>0        The pin is driven low.<br>1        The pin is driven high.                                                                                                                  |
| 6   | SPICLK     | R/W  | 0h    | SPICLK line [signal data value] If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the CLKSPI line [high or low], and a write into this bit has no effect If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the CLKSPI line is driven high or low according to the value written into this register              |
| 5   | SPIDAT_1   | R/W  | 0h    | SPIDAT[1] line [signal data value] If MCSPI_SYST[SPIDATDIR1] = 0 [output mode direction], the SPIDAT[1] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIDATDIR1] = 1 [input mode direction], this bit returns the value on the SPIDAT[1] line [high or low], and a write into this bit has no effect |
| 4   | SPIDAT_0   | R/W  | 0h    | SPIDAT[0] line [signal data value] If MCSPI_SYST[SPIDATDIR0] = 0 [output mode direction], the SPIDAT[0] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIDATDIR0] = 1 [input mode direction], this bit returns the value on the SPIDAT[0] line [high or low], and a write into this bit has no effect |
| 3   | SPIEN_3    | R/W  | 0h    | SPIEN[3] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIEN[3] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[3] line [high or low], and a write into this bit has no effect        |
| 2   | SPIEN_2    | R/W  | 0h    | SPIEN[2] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIEN[2] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[2] line [high or low], and a write into this bit has no effect        |
| 1   | SPIEN_1    | R/W  | 0h    | SPIEN[1] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIEN[1] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[1] line [high or low], and a write into this bit has no effect        |
| 0   | SPIEN_0    | R/W  | 0h    | SPIEN[0] line [signal data value] If MCSPI_SYST[SPIENDIR] = 0 [output mode direction], the SPIEN[0] line is driven high or low according to the value written into this register If MCSPI_SYST[SPIENDIR] = 1 [input mode direction], this bit returns the value on the SPIEN[0] line [high or low], and a write into this bit has no effect        |

### 5.14.2.10 MCSPI\_MODULCTRL Register

#### 1 MCSPI\_MODULCTRL Register (Offset = 128h) [reset = 4h]

This register is dedicated to the configuration of the serial port interface.

Return to [Summary Table](#)

**Table 5-2500. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCSPI0        | 5220 0128h       |
| MCSPI1        | 5220 1128h       |
| MCSPI2        | 5220 2128h       |
| MCSPI3        | 5220 3128h       |
| MCSPI4        | 5220 4128h       |

**Figure 5-826. MCSPI\_MODULCTRL Name Register**

|             |         |    |    |             |     |       |        |
|-------------|---------|----|----|-------------|-----|-------|--------|
| 31          | 30      | 29 | 28 | 27          | 26  | 25    | 24     |
| RESERVED_11 |         |    |    |             |     |       |        |
| R           |         |    |    |             |     |       |        |
| 0h          |         |    |    |             |     |       |        |
| 23          | 22      | 21 | 20 | 19          | 18  | 17    | 16     |
| RESERVED_11 |         |    |    |             |     |       |        |
| R           |         |    |    |             |     |       |        |
| 0h          |         |    |    |             |     |       |        |
| 15          | 14      | 13 | 12 | 11          | 10  | 9     | 8      |
| RESERVED_11 |         |    |    |             |     |       | FDAA   |
| R           |         |    |    |             |     |       | R/W    |
| 0h          |         |    |    |             |     |       | 0h     |
| 7           | 6       | 5  | 4  | 3           | 2   | 1     | 0      |
| MOA         | INITDLY |    |    | SYSTEM_TEST | MS  | PIN34 | SINGLE |
| R/W         | R/W     |    |    | R/W         | R/W | R/W   | R/W    |
| 0h          | 0h      |    |    | 0h          | 1h  | 0h    | 0h     |

**Table 5-2502. MCSPI\_MODULCTRL Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|------|-------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:9 | RESERVED_11 | R    | 0h    | Reads returns 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 8    | FDAA        | R/W  | 0h    | FIFO DMA Address 256-bit aligned This register is used when a FIFO is managed by the module and DMA connected to the controller provides only 256 bit aligned address If this bit is set the enabled channel which uses the FIFO has its datas managed through MCSPI_DAFTX and MCSPI_DAFRX registers instead of MCSPI_TX[i] and MCSPI_RX[i] registers<br>0 FIFO data managed by MCSPI_TX(i) and MCSPI_RX(i) registers.<br>1 FIFO data managed by MCSPI_DAFTX and MCSPI_DAFRX registers. |
| 7    | MOA         | R/W  | 0h    | Multiple word ocp access: This register can only be used when a channel is enabled using a FIFO It allows the system to perform multiple SPI word access for a single 32-bit OCP word access This is possible for WL < 16<br>0 Multiple word access disabled<br>1 Multiple word access enabled with FIFO                                                                                                                                                                                |

**Table 5-2502. MCSPI\_MODULCTRL Register Field Descriptions (continued)**

| Bit | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----|-------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6:4 | INITDLY     | R/W  | 0h    | Initial spi delay for first transfer: This register is an option only available in SINGLE controller mode, The controller waits for a delay to transmit the first spi word after channel enabled and corresponding TX register filled This Delay is based on SPI output frequency clock, No clock output provided to the boundary and chip select is not active in 4 pin mode within this period<br><br>0 No delay for first MCSPI transfer.<br>1 The controller wait 4 MCSPI bus clock<br>2 The controller wait 8 MCSPI bus clock<br>3 The controller wait 16 MCSPI bus clock<br>4 The controller wait 32 MCSPI bus clock |
| 3   | SYSTEM_TEST | R/W  | 0h    | Enables the system test mode<br><br>0 Functional mode<br>1 System test mode (SYSTEST)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 2   | MS          | R/W  | 1h    | Controller/ Responder<br><br>0 Controller - The module generates the SPICLK and SPIEN[3:0].<br>1 Peripheral - The module receives the SPICLK and SPIEN[3:0].                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 1   | PIN34       | R/W  | 0h    | Pin mode selection: This register is used to configure the SPI pin mode, in controller or responder mode If asserted the controller only use SIMO,SOMI and SPICLK clock pin for spi transfers<br><br>0 SPIEN is used as a chip-select.<br>1 SPIEN is not used. In this mode all related options to chip-select have no meaning.                                                                                                                                                                                                                                                                                            |
| 0   | SINGLE      | R/W  | 0h    | Single channel / Multi Channel [controller mode only]<br><br>0 More than one channel will be used in controller mode.<br>1 Only one channel will be used in controller mode. This bit must be set in Force SPIEN[i] mode.                                                                                                                                                                                                                                                                                                                                                                                                  |



### 5.14.2.11 MCSPI\_CH0CONF Register

#### 1 MCSPI\_CH0CONF Register (Offset = 12Ch) [reset = 60000h]

This register is dedicated to the configuration of the channel 0

Return to [Summary Table](#)

**Table 5-2503. Instance Table**

| Instance Name | Physical Address  |
|---------------|-------------------|
| <b>MCSPI0</b> | <b>5220 012Ch</b> |
| <b>MCSPI1</b> | <b>5220 112Ch</b> |
| <b>MCSPI2</b> | <b>5220 212Ch</b> |
| <b>MCSPI3</b> | <b>5220 312Ch</b> |
| <b>MCSPI4</b> | <b>5220 412Ch</b> |

**Figure 5-827. MCSPI\_CH0CONF Name Register**

|            |          |      |       |       |      |      |       |
|------------|----------|------|-------|-------|------|------|-------|
| 31         | 30       | 29   | 28    | 27    | 26   | 25   | 24    |
| RESERVED_0 |          | CLKG | FFER  | FFEW  | TCS0 |      | SBPOL |
| R          |          | R/W  | R/W   | R/W   | R/W  |      | R/W   |
| 0h         |          | 0h   | 0h    | 0h    | 0h   |      | 0h    |
| 23         | 22       | 21   | 20    | 19    | 18   | 17   | 16    |
| SBE        | SPIENSLV |      | FORCE | TURBO | IS   | DPE1 | DPE0  |
| R/W        | R/W      |      | R/W   | R/W   | R/W  | R/W  | R/W   |
| 0h         | 0h       |      | 0h    | 0h    | 1h   | 1h   | 0h    |
| 15         | 14       | 13   | 12    | 11    | 10   | 9    | 8     |
| DMAR       | DMAW     | TRM  |       | WL    |      |      |       |
| R/W        | R/W      | R/W  |       | R/W   |      |      |       |
| 0h         | 0h       | 0h   |       | 0h    |      |      |       |
| 7          | 6        | 5    | 4     | 3     | 2    | 1    | 0     |
| WL         | EPOL     | CLKD |       |       |      | POL  | PHA   |
| R/W        | R/W      | R/W  |       |       |      | R/W  | R/W   |
| 0h         | 0h       | 0h   |       |       |      | 0h   | 0h    |

**Table 5-2505. MCSPI\_CH0CONF Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | RESERVED_0 | R    | 0h    | Read returns 0                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 29    | CLKG       | R/W  | 0h    | Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity<br>When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values<br>0 Clock granularity of power of 2<br>1 One clock cycle granularity |
| 28    | FFER       | R/W  | 0h    | FIFO enabled for receive:Only one channel can have this bit field set<br>0 The buffer is not used to receive data.<br>1 The buffer is used to receive data.                                                                                                                                                                                                                                                                                  |
| 27    | FFEW       | R/W  | 0h    | FIFO enabled for Transmit:Only one channel can have this bit field set<br>0 The buffer is not used to transmit data.<br>1 The buffer is used to transmit data.                                                                                                                                                                                                                                                                               |

**Table 5-2505. MCSPI\_CH0CONF Register Field Descriptions (continued)**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:25 | TCS0     | R/W  | 0h    | <p>Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock</p> <p>0      0.5 clock cycle<br/> 1      1.5 clock cycles<br/> 2      2.5 clock cycles<br/> 3      3.5 clock cycles</p>                                                                                                                                |
| 24    | SBPOL    | R/W  | 0h    | <p>Start bit polarity</p> <p>0      SPICLK is held low during the INACTIVE state<br/> 1      SPICLK is held high during the INACTIVE state</p>                                                                                                                                                                                                                                                             |
| 23    | SBE      | R/W  | 0h    | <p>Start bit enable for SPI transfer</p> <p>0      Default MCSPI transfer length as specified by WL bit field<br/> 1      Start bit D/CX added before MCSPI transfer polarity is defined by MCSPI_CHCONF_0[24] SBPOL</p>                                                                                                                                                                                   |
| 22:21 | SPIENSLV | R/W  | 0h    | <p>Channel 0 only and responder mode only: SPI responder select signal detection Reserved bits for other cases</p> <p>0      Detection enabled only on SPIEN[0]<br/> 1      Detection enabled only on SPIEN[1]<br/> 2      Detection enabled only on SPIEN[2]<br/> 3      Detection enabled only on SPIEN[3]</p>                                                                                           |
| 20    | FORCE    | R/W  | 0h    | <p>Manual SPIEN assertion to keep SPIEN active between SPI words [single channel controller mode only]</p> <p>0      writing 0 into this bit drives low the SPIEN line when MCSPI_CHCONF_0[6] EPOL=0, and drives it high when MCSPI_CHCONF_0[6] EPOL=1.<br/> 1      writing 1 into this bit drives high the SPIEN line when MCSPI_CHCONF_0[6] EPOL=0, and drives it low when MCSPI_CHCONF_0[6] EPOL=1.</p> |
| 19    | TURBO    | R/W  | 0h    | <p>Turbo mode</p> <p>0      Turbo is deactivated (recommended for single MCSPI word transfer).<br/> 1      Turbo is activated to maximize the throughput for multiple MCSPI words transfer.</p>                                                                                                                                                                                                            |
| 18    | IS       | R/W  | 1h    | <p>Input Select</p> <p>0      Data line 0 (SPIDAT[0]) selected for reception<br/> 1      Data line 1 (SPIDAT[1]) selected for reception</p>                                                                                                                                                                                                                                                                |
| 17    | DPE1     | R/W  | 1h    | <p>Transmission Enable for data line 1 [SPIDATAGZEN[1]]</p> <p>0      Data line 1 (SPIDAT[1]) selected for transmission<br/> 1      No transmission on Data Line1 (SPIDAT[1])</p>                                                                                                                                                                                                                          |
| 16    | DPE0     | R/W  | 0h    | <p>Transmission Enable for data line 0 [SPIDATAGZEN[0]]</p> <p>0      Data Line0 (SPIDAT[0]) selected for transmission<br/> 1      No transmission on data line 0 (SPIDAT[0])</p>                                                                                                                                                                                                                          |

**Table 5-2505. MCSPI\_CH0CONF Register Field Descriptions (continued)**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | DMAR  | R/W  | 0h    | <p>DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel</p> <p>0 DMA read request disabled<br/>1 DMA read request enabled</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 14    | DMAW  | R/W  | 0h    | <p>DMA Write request The DMA Write request line is asserted when The channel is enabled and the transmitter register of the channel is empty The DMA Write request line is deasserted on load completion of the transmitter register of the channel</p> <p>0 DMA write request disabled<br/>1 DMA write request enabled</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 13:12 | TRM   | R/W  | 0h    | <p>Transmit/Receive modes</p> <p>0 Transmit-and-receive mode<br/>1 Receive-only mode<br/>2 Transmit-only mode<br/>3 Reserved</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 11:7  | WL    | R/W  | 0h    | <p>SPI word length</p> <p>0 Reserved<br/>1 Reserved<br/>2 Reserved<br/>3 The MCSPI word is 4 bits long<br/>4 The MCSPI word is 5 bits long<br/>5 The MCSPI word is 6 bits long<br/>6 The MCSPI word is 7 bits long<br/>7 The MCSPI word is 8 bits long<br/>8 The MCSPI word is 9 bits long<br/>9 The MCSPI word is 10 bits long<br/>A The MCSPI word is 11 bits long<br/>B The MCSPI word is 12 bits long<br/>C The MCSPI word is 13 bits long<br/>D The MCSPI word is 14 bits long<br/>E The MCSPI word is 15 bits long<br/>F The MCSPI word is 16 bits long<br/>10 The MCSPI word is 17 bits long<br/>11 The MCSPI word is 18 bits long<br/>12 The MCSPI word is 19 bits long<br/>13 The MCSPI word is 20 bits long<br/>14 The MCSPI word is 21 bits long<br/>15 The MCSPI word is 22 bits long<br/>16 The MCSPI word is 23 bits long<br/>17 The MCSPI word is 24 bits long<br/>18 The MCSPI word is 25 bits long<br/>19 The MCSPI word is 26 bits long<br/>1A The MCSPI word is 27 bits long<br/>1B The MCSPI word is 28 bits long<br/>1C The MCSPI word is 29 bits long<br/>1D The MCSPI word is 30 bits long<br/>1E The MCSPI word is 31 bits long<br/>1F The MCSPI word is 32 bits long</p> |
| 6     | EPOL  | R/W  | 0h    | <p>SPIEN polarity</p> <p>0 SPICLK is held low during the INACTIVE state<br/>1 SPICLK is held high during the INACTIVE state</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

**Table 5-2505. MCSPI\_CH0CONF Register Field Descriptions (continued)**

| Bit | Field                                              | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |   |                                                   |   |                                                    |   |  |   |  |   |    |   |    |   |    |   |     |   |     |   |     |   |      |   |      |   |      |   |      |   |       |   |       |
|-----|----------------------------------------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|---------------------------------------------------|---|----------------------------------------------------|---|--|---|--|---|----|---|----|---|----|---|-----|---|-----|---|-----|---|------|---|------|---|------|---|------|---|-------|---|-------|
| 5:2 | CLKD                                               | R/W  | 0h    | <p>Frequency divider for SPICLK [only when the module is a Controller SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0</p> <table><tr><td>0</td><td></td></tr><tr><td>1</td><td></td></tr><tr><td>2</td><td></td></tr><tr><td>3</td><td></td></tr><tr><td>4</td><td>16</td></tr><tr><td>5</td><td>32</td></tr><tr><td>6</td><td>64</td></tr><tr><td>7</td><td>128</td></tr><tr><td>8</td><td>256</td></tr><tr><td>9</td><td>512</td></tr><tr><td>A</td><td>1024</td></tr><tr><td>B</td><td>2048</td></tr><tr><td>C</td><td>4096</td></tr><tr><td>D</td><td>8192</td></tr><tr><td>E</td><td>16384</td></tr><tr><td>F</td><td>32768</td></tr></table> | 0 |                                                   | 1 |                                                    | 2 |  | 3 |  | 4 | 16 | 5 | 32 | 6 | 64 | 7 | 128 | 8 | 256 | 9 | 512 | A | 1024 | B | 2048 | C | 4096 | D | 8192 | E | 16384 | F | 32768 |
| 0   |                                                    |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |   |                                                   |   |                                                    |   |  |   |  |   |    |   |    |   |    |   |     |   |     |   |     |   |      |   |      |   |      |   |      |   |       |   |       |
| 1   |                                                    |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |   |                                                   |   |                                                    |   |  |   |  |   |    |   |    |   |    |   |     |   |     |   |     |   |      |   |      |   |      |   |      |   |       |   |       |
| 2   |                                                    |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |   |                                                   |   |                                                    |   |  |   |  |   |    |   |    |   |    |   |     |   |     |   |     |   |      |   |      |   |      |   |      |   |       |   |       |
| 3   |                                                    |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |   |                                                   |   |                                                    |   |  |   |  |   |    |   |    |   |    |   |     |   |     |   |     |   |      |   |      |   |      |   |      |   |       |   |       |
| 4   | 16                                                 |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |   |                                                   |   |                                                    |   |  |   |  |   |    |   |    |   |    |   |     |   |     |   |     |   |      |   |      |   |      |   |      |   |       |   |       |
| 5   | 32                                                 |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |   |                                                   |   |                                                    |   |  |   |  |   |    |   |    |   |    |   |     |   |     |   |     |   |      |   |      |   |      |   |      |   |       |   |       |
| 6   | 64                                                 |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |   |                                                   |   |                                                    |   |  |   |  |   |    |   |    |   |    |   |     |   |     |   |     |   |      |   |      |   |      |   |      |   |       |   |       |
| 7   | 128                                                |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |   |                                                   |   |                                                    |   |  |   |  |   |    |   |    |   |    |   |     |   |     |   |     |   |      |   |      |   |      |   |      |   |       |   |       |
| 8   | 256                                                |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |   |                                                   |   |                                                    |   |  |   |  |   |    |   |    |   |    |   |     |   |     |   |     |   |      |   |      |   |      |   |      |   |       |   |       |
| 9   | 512                                                |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |   |                                                   |   |                                                    |   |  |   |  |   |    |   |    |   |    |   |     |   |     |   |     |   |      |   |      |   |      |   |      |   |       |   |       |
| A   | 1024                                               |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |   |                                                   |   |                                                    |   |  |   |  |   |    |   |    |   |    |   |     |   |     |   |     |   |      |   |      |   |      |   |      |   |       |   |       |
| B   | 2048                                               |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |   |                                                   |   |                                                    |   |  |   |  |   |    |   |    |   |    |   |     |   |     |   |     |   |      |   |      |   |      |   |      |   |       |   |       |
| C   | 4096                                               |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |   |                                                   |   |                                                    |   |  |   |  |   |    |   |    |   |    |   |     |   |     |   |     |   |      |   |      |   |      |   |      |   |       |   |       |
| D   | 8192                                               |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |   |                                                   |   |                                                    |   |  |   |  |   |    |   |    |   |    |   |     |   |     |   |     |   |      |   |      |   |      |   |      |   |       |   |       |
| E   | 16384                                              |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |   |                                                   |   |                                                    |   |  |   |  |   |    |   |    |   |    |   |     |   |     |   |     |   |      |   |      |   |      |   |      |   |       |   |       |
| F   | 32768                                              |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |   |                                                   |   |                                                    |   |  |   |  |   |    |   |    |   |    |   |     |   |     |   |     |   |      |   |      |   |      |   |      |   |       |   |       |
| 1   | POL                                                | R/W  | 0h    | <p>SPICLK polarity</p> <table><tr><td>0</td><td>SPICLK is held low during the INACTIVE state</td></tr><tr><td>1</td><td>SPICLK is held high during the INACTIVE state</td></tr></table>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 0 | SPICLK is held low during the INACTIVE state      | 1 | SPICLK is held high during the INACTIVE state      |   |  |   |  |   |    |   |    |   |    |   |     |   |     |   |     |   |      |   |      |   |      |   |      |   |       |   |       |
| 0   | SPICLK is held low during the INACTIVE state       |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |   |                                                   |   |                                                    |   |  |   |  |   |    |   |    |   |    |   |     |   |     |   |     |   |      |   |      |   |      |   |      |   |       |   |       |
| 1   | SPICLK is held high during the INACTIVE state      |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |   |                                                   |   |                                                    |   |  |   |  |   |    |   |    |   |    |   |     |   |     |   |     |   |      |   |      |   |      |   |      |   |       |   |       |
| 0   | PHA                                                | R/W  | 0h    | <p>SPICLK phase</p> <table><tr><td>0</td><td>Data are latched on odd-numbered edges of SPICLK.</td></tr><tr><td>1</td><td>Data are latched on even-numbered edges of SPICLK.</td></tr></table>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 0 | Data are latched on odd-numbered edges of SPICLK. | 1 | Data are latched on even-numbered edges of SPICLK. |   |  |   |  |   |    |   |    |   |    |   |     |   |     |   |     |   |      |   |      |   |      |   |      |   |       |   |       |
| 0   | Data are latched on odd-numbered edges of SPICLK.  |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |   |                                                   |   |                                                    |   |  |   |  |   |    |   |    |   |    |   |     |   |     |   |     |   |      |   |      |   |      |   |      |   |       |   |       |
| 1   | Data are latched on even-numbered edges of SPICLK. |      |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |   |                                                   |   |                                                    |   |  |   |  |   |    |   |    |   |    |   |     |   |     |   |     |   |      |   |      |   |      |   |      |   |       |   |       |

### 5.14.2.12 MCSPI\_CH0STAT Register

#### 1 MCSPI\_CH0STAT Register (Offset = 130h) [reset = 0h]

This register provides status information about transmitter and receiver registers of channel 0

Return to [Summary Table](#)

**Table 5-2506. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCSPI0        | 5220 0130h       |
| MCSPI1        | 5220 1130h       |
| MCSPI2        | 5220 2130h       |
| MCSPI3        | 5220 3130h       |
| MCSPI4        | 5220 4130h       |

**Figure 5-828. MCSPI\_CH0STAT Name Register**

|            |       |       |       |       |     |     |     |
|------------|-------|-------|-------|-------|-----|-----|-----|
| 31         | 30    | 29    | 28    | 27    | 26  | 25  | 24  |
| RESERVED_2 |       |       |       |       |     |     |     |
| R          |       |       |       |       |     |     |     |
| 0h         |       |       |       |       |     |     |     |
| 23         | 22    | 21    | 20    | 19    | 18  | 17  | 16  |
| RESERVED_2 |       |       |       |       |     |     |     |
| R          |       |       |       |       |     |     |     |
| 0h         |       |       |       |       |     |     |     |
| 15         | 14    | 13    | 12    | 11    | 10  | 9   | 8   |
| RESERVED_2 |       |       |       |       |     |     |     |
| R          |       |       |       |       |     |     |     |
| 0h         |       |       |       |       |     |     |     |
| 7          | 6     | 5     | 4     | 3     | 2   | 1   | 0   |
| RESERVED_2 | RXFFF | RXFFE | TXFFF | TXFFE | EOT | TXS | RXS |
| R          | R     | R     | R     | R     | R   | R   | R   |
| 0h         | 0h    | 0h    | 0h    | 0h    | 0h  | 0h  | 0h  |

**Table 5-2508. MCSPI\_CH0STAT Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                             |
|------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED_2 | R    | 0h    | Read returns 0                                                                                                          |
| 6    | RXFFF      | R    | 0h    | Channel "i" FIFO Receive Buffer Full Status<br>0 FIFO receive buffer is not full<br>1 FIFO receive buffer is full       |
| 5    | RXFFE      | R    | 0h    | Channel "i" FIFO Receive Buffer Empty Status<br>0 FIFO receive buffer is not empty<br>1 FIFO receive buffer is empty    |
| 4    | TXFFF      | R    | 0h    | Channel "i" FIFO Transmit Buffer Full Status<br>0 FIFO transmit buffer is not full<br>1 FIFO transmit buffer is full    |
| 3    | TXFFE      | R    | 0h    | Channel "i" FIFO Transmit Buffer Empty Status<br>0 FIFO transmit buffer is not empty<br>1 FIFO transmit buffer is empty |

**Table 5-2508. MCSPI\_CH0STAT Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-----|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | EOT   | R    | 0h    | <p>Channel "i" End of transfer Status The definitions of beginning and end of transfer vary with controller versus responder and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details</p> <p>0      This flag is automatically cleared when the shift register is loaded with the data from the transmitter register (beginning of transfer).</p> <p>1      This flag is automatically set to one at the end of an MCSPI transfer.</p> |
| 1   | TXS   | R    | 0h    | <p>Channel "i" Transmitter Register Status</p> <p>0      Register is full.</p> <p>1      Register is empty.</p>                                                                                                                                                                                                                                                                                                                                                               |
| 0   | RXS   | R    | 0h    | <p>Channel "i" Receiver Register Status</p> <p>0      Register is empty.</p> <p>1      Register is full.</p>                                                                                                                                                                                                                                                                                                                                                                  |

### 5.14.2.13 MCSPI\_CH0CTRL Register

#### 1 MCSPI\_CH0CTRL Register (Offset = 134h) [reset = 0h]

This register is dedicated to enable the channel 0

Return to [Summary Table](#)

**Table 5-2509. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCSPI0        | 5220 0134h       |
| MCSPI1        | 5220 1134h       |
| MCSPI2        | 5220 2134h       |
| MCSPI3        | 5220 3134h       |
| MCSPI4        | 5220 4134h       |

**Figure 5-829. MCSPI\_CH0CTRL Name Register**

|            |    |    |    |    |    |    |     |
|------------|----|----|----|----|----|----|-----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24  |
| RESERVED_2 |    |    |    |    |    |    |     |
| R          |    |    |    |    |    |    |     |
| 0h         |    |    |    |    |    |    |     |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16  |
| RESERVED_2 |    |    |    |    |    |    |     |
| R          |    |    |    |    |    |    |     |
| 0h         |    |    |    |    |    |    |     |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8   |
| EXTCLK     |    |    |    |    |    |    |     |
| R/W        |    |    |    |    |    |    |     |
| 0h         |    |    |    |    |    |    |     |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0   |
| RESERVED_1 |    |    |    |    |    |    | EN  |
| R          |    |    |    |    |    |    | R/W |
| 0h         |    |    |    |    |    |    | 0h  |

**Table 5-2511. MCSPI\_CH0CTRL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                        |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED_2 | R    | 0h    | Read returns 0                                                                                                                                                                                                                                                                                                                                                     |
| 15:8  | EXTCLK     | R/W  | 0h    | Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096clock divider ratio<br><br>0      Clock ratio is CLKD + 1.<br>1      Clock ratio is CLKD + 1 + 16.<br>FF     Clock ratio is CLKD + 1 + 4080. |
| 7:1   | RESERVED_1 | R    | 0h    | Read returns 0                                                                                                                                                                                                                                                                                                                                                     |
| 0     | EN         | R/W  | 0h    | Channel Enable<br><br>0      Channel i is not active.<br>1      Channel i is active.                                                                                                                                                                                                                                                                               |

#### 5.14.2.14 MCSPI\_TX0 Register

##### 1 MCSPI\_TX0 Register (Offset = 138h) [reset = 0h]

This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

Return to [Summary Table](#)

**Table 5-2512. Instance Table**

| Instance Name | Physical Address  |
|---------------|-------------------|
| <b>MCSPI0</b> | <b>5220 0138h</b> |
| <b>MCSPI1</b> | <b>5220 1138h</b> |
| <b>MCSPI2</b> | <b>5220 2138h</b> |
| <b>MCSPI3</b> | <b>5220 3138h</b> |
| <b>MCSPI4</b> | <b>5220 4138h</b> |

**Figure 5-830. MCSPI\_TX0 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TDATA |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TDATA |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TDATA |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TDATA |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-2514. MCSPI\_TX0 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                |
|------|-------|------|-------|----------------------------|
| 31:0 | TDATA | R/W  | 0h    | Channel 0 Data to transmit |



### 5.14.2.15 MCSPI\_RX0 Register

#### 1 MCSPI\_RX0 Register (Offset = 13Ch) [reset = 0h]

This register contains a single SPI word received through the serial link, what ever SPI word length is.

Return to [Summary Table](#)

**Table 5-2515. Instance Table**

| Instance Name | Physical Address  |
|---------------|-------------------|
| <b>MCSPI0</b> | <b>5220 013Ch</b> |
| <b>MCSPI1</b> | <b>5220 113Ch</b> |
| <b>MCSPI2</b> | <b>5220 213Ch</b> |
| <b>MCSPI3</b> | <b>5220 313Ch</b> |
| <b>MCSPI4</b> | <b>5220 413Ch</b> |

**Figure 5-831. MCSPI\_RX0 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RDATA |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RDATA |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RDATA |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RDATA |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-2517. MCSPI\_RX0 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description             |
|------|-------|------|-------|-------------------------|
| 31:0 | RDATA | R    | 0h    | Channel 0 Received Data |

### 5.14.2.16 MCSPI\_CH1CONF Register

#### 1 MCSPI\_CH1CONF Register (Offset = 140h) [reset = 60000h]

This register is dedicated to the configuration of the channel 1

Return to [Summary Table](#)

**Table 5-2518. Instance Table**

| Instance Name | Physical Address  |
|---------------|-------------------|
| <b>MCSPI0</b> | <b>5220 0140h</b> |
| <b>MCSPI1</b> | <b>5220 1140h</b> |
| <b>MCSPI2</b> | <b>5220 2140h</b> |
| <b>MCSPI3</b> | <b>5220 3140h</b> |
| <b>MCSPI4</b> | <b>5220 4140h</b> |

**Figure 5-832. MCSPI\_CH1CONF Name Register**

|            |            |      |       |       |      |      |       |
|------------|------------|------|-------|-------|------|------|-------|
| 31         | 30         | 29   | 28    | 27    | 26   | 25   | 24    |
| RESERVED_0 |            | CLKG | FFER  | FFEW  | TCS1 |      | SBPOL |
| R          |            | R/W  | R/W   | R/W   | R/W  |      | R/W   |
| 0h         |            | 0h   | 0h    | 0h    | 0h   |      | 0h    |
| 23         | 22         | 21   | 20    | 19    | 18   | 17   | 16    |
| SBE        | RESERVED_1 |      | FORCE | TURBO | IS   | DPE1 | DPE0  |
| R/W        | R          |      | R/W   | R/W   | R/W  | R/W  | R/W   |
| 0h         | 0h         |      | 0h    | 0h    | 1h   | 1h   | 0h    |
| 15         | 14         | 13   | 12    | 11    | 10   | 9    | 8     |
| DMAR       | DMAW       | TRM  |       | WL    |      |      |       |
| R/W        | R/W        | R/W  |       | R/W   |      |      |       |
| 0h         | 0h         | 0h   |       | 0h    |      |      |       |
| 7          | 6          | 5    | 4     | 3     | 2    | 1    | 0     |
| WL         | EPOL       | CLKD |       |       |      | POL  | PHA   |
| R/W        | R/W        | R/W  |       |       |      | R/W  | R/W   |
| 0h         | 0h         | 0h   |       |       |      | 0h   | 0h    |

**Table 5-2520. MCSPI\_CH1CONF Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | RESERVED_0 | R    | 0h    | Read returns 0                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 29    | CLKG       | R/W  | 0h    | Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity<br>When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values<br>0 Clock granularity of power of 2<br>1 One clock cycle granularity |
| 28    | FFER       | R/W  | 0h    | FIFO enabled for receive:Only one channel can have this bit field set<br>0 The buffer is not used to receive data.<br>1 The buffer is used to receive data.                                                                                                                                                                                                                                                                                  |
| 27    | FFEW       | R/W  | 0h    | FIFO enabled for Transmit:Only one channel can have this bit field set<br>0 The buffer is not used to transmit data.<br>1 The buffer is used to transmit data.                                                                                                                                                                                                                                                                               |

**Table 5-2520. MCSPI\_CH1CONF Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:25 | TCS1       | R/W  | 0h    | <p>Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock</p> <p>0      0.5 clock cycle<br/> 1      1.5 clock cycles<br/> 2      2.5 clock cycles<br/> 3      3.5 clock cycles</p>                                                                                                                                |
| 24    | SBPOL      | R/W  | 0h    | <p>Start bit polarity</p> <p>0      SPICLK is held low during the INACTIVE state<br/> 1      SPICLK is held high during the INACTIVE state</p>                                                                                                                                                                                                                                                             |
| 23    | SBE        | R/W  | 0h    | <p>Start bit enable for SPI transfer</p> <p>0      Default MCSPI transfer length as specified by WL bit field<br/> 1      Start bit D/CX added before MCSPI transfer polarity is defined by MCSPI_CHCONF_0[24] SBPOL</p>                                                                                                                                                                                   |
| 22:21 | RESERVED_1 | R    | 0h    | Read returns 0                                                                                                                                                                                                                                                                                                                                                                                             |
| 20    | FORCE      | R/W  | 0h    | <p>Manual SPIEN assertion to keep SPIEN active between SPI words [single channel controller mode only]</p> <p>0      Writing 0 into this bit drives low the SPIEN line when MCSPI_CHCONF_1[6] EPOL=0, and drives it high when MCSPI_CHCONF_1[6] EPOL=1.<br/> 1      Writing 1 into this bit drives high the SPIEN line when MCSPI_CHCONF_1[6] EPOL=0, and drives it low when MCSPI_CHCONF_1[6] EPOL=1.</p> |
| 19    | TURBO      | R/W  | 0h    | <p>Turbo mode</p> <p>0      Turbo is deactivated (recommended for single MCSPI word transfer).<br/> 1      Turbo is activated to maximize the throughput for multiple MCSPI words transfer.</p>                                                                                                                                                                                                            |
| 18    | IS         | R/W  | 1h    | <p>Input Select</p> <p>0      Data line 0 (SPIDAT[0]) selected for reception<br/> 1      Data line 1 (SPIDAT[1]) selected for reception</p>                                                                                                                                                                                                                                                                |
| 17    | DPE1       | R/W  | 1h    | <p>Transmission Enable for data line 1 [SPIDATAGZEN[1]]</p> <p>0      Data line 1 (SPIDAT[1]) selected for transmission<br/> 1      No transmission on Data Line1 (SPIDAT[1])</p>                                                                                                                                                                                                                          |
| 16    | DPE0       | R/W  | 0h    | <p>Transmission Enable for data line 0 [SPIDATAGZEN[0]]</p> <p>0      Data Line0 (SPIDAT[0]) selected for transmission<br/> 1      No transmission on data line 0 (SPIDAT[0])</p>                                                                                                                                                                                                                          |
| 15    | DMAR       | R/W  | 0h    | <p>DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel</p> <p>0      DMA read request disabled<br/> 1      DMA read request enabled</p>                                                                |

**Table 5-2520. MCSPI\_CH1CONF Register Field Descriptions (continued)**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14    | DMAW  | R/W  | 0h    | <p>DMA Write request The DMA Write request line is asserted when the channel is enabled and the transmitter register of the channel is empty. The DMA Write request line is deasserted on load completion of the transmitter register of the channel.</p> <p>0 DMA write request disabled<br/>1 DMA write request enabled</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 13:12 | TRM   | R/W  | 0h    | <p>Transmit/Receive modes</p> <p>0 Transmit-and-receive mode<br/>1 Receive-only mode<br/>2 Transmit-only mode<br/>3 Reserved</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 11:7  | WL    | R/W  | 0h    | <p>SPI word length</p> <p>0 Reserved<br/>1 Reserved<br/>2 Reserved<br/>3 The MCSPI word is 4 bits long<br/>4 The MCSPI word is 5 bits long<br/>5 The MCSPI word is 6 bits long<br/>6 The MCSPI word is 7 bits long<br/>7 The MCSPI word is 8 bits long<br/>8 The MCSPI word is 9 bits long<br/>9 The MCSPI word is 10 bits long<br/>A The MCSPI word is 11 bits long<br/>B The MCSPI word is 12 bits long<br/>C The MCSPI word is 13 bits long<br/>D The MCSPI word is 14 bits long<br/>E The MCSPI word is 15 bits long<br/>F The MCSPI word is 16 bits long<br/>10 The MCSPI word is 17 bits long<br/>11 The MCSPI word is 18 bits long<br/>12 The MCSPI word is 19 bits long<br/>13 The MCSPI word is 20 bits long<br/>14 The MCSPI word is 21 bits long<br/>15 The MCSPI word is 22 bits long<br/>16 The MCSPI word is 23 bits long<br/>17 The MCSPI word is 24 bits long<br/>18 The MCSPI word is 25 bits long<br/>19 The MCSPI word is 26 bits long<br/>1A The MCSPI word is 27 bits long<br/>1B The MCSPI word is 28 bits long<br/>1C The MCSPI word is 29 bits long<br/>1D The MCSPI word is 30 bits long<br/>1E The MCSPI word is 31 bits long<br/>1F The MCSPI word is 32 bits long</p> |
| 6     | EPOL  | R/W  | 0h    | <p>SPIEN polarity</p> <p>0 SPICLK is held low during the INACTIVE state<br/>1 SPICLK is held high during the INACTIVE state</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

**Table 5-2520. MCSPI\_CH1CONF Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5:2 | CLKD  | R/W  | 0h    | <p>Frequency divider for SPICLK [only when the module is a Controller SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0</p> <p>0<br/>1<br/>2<br/>3<br/>4      16<br/>5      32<br/>6      64<br/>7      128<br/>8      256<br/>9      512<br/>A      1024<br/>B      2048<br/>C      4096<br/>D      8192<br/>E      16384<br/>F      32768</p> |
| 1   | POL   | R/W  | 0h    | <p>SPICLK polarity</p> <p>0      SPICLK is held low during the INACTIVE state<br/>1      SPICLK is held high during the INACTIVE state</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 0   | PHA   | R/W  | 0h    | <p>SPICLK phase</p> <p>0      Data are latched on odd-numbered edges of SPICLK.<br/>1      Data are latched on even-numbered edges of SPICLK.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

### 5.14.2.17 MCSPI\_CH1STAT Register

#### 1 MCSPI\_CH1STAT Register (Offset = 144h) [reset = 0h]

This register provides status information about transmitter and receiver registers of channel 1

Return to [Summary Table](#)

**Table 5-2521. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCSPI0        | 5220 0144h       |
| MCSPI1        | 5220 1144h       |
| MCSPI2        | 5220 2144h       |
| MCSPI3        | 5220 3144h       |
| MCSPI4        | 5220 4144h       |

**Figure 5-833. MCSPI\_CH1STAT Name Register**

|            |       |       |       |       |     |     |     |
|------------|-------|-------|-------|-------|-----|-----|-----|
| 31         | 30    | 29    | 28    | 27    | 26  | 25  | 24  |
| RESERVED_2 |       |       |       |       |     |     |     |
| R          |       |       |       |       |     |     |     |
| 0h         |       |       |       |       |     |     |     |
| 23         | 22    | 21    | 20    | 19    | 18  | 17  | 16  |
| RESERVED_2 |       |       |       |       |     |     |     |
| R          |       |       |       |       |     |     |     |
| 0h         |       |       |       |       |     |     |     |
| 15         | 14    | 13    | 12    | 11    | 10  | 9   | 8   |
| RESERVED_2 |       |       |       |       |     |     |     |
| R          |       |       |       |       |     |     |     |
| 0h         |       |       |       |       |     |     |     |
| 7          | 6     | 5     | 4     | 3     | 2   | 1   | 0   |
| RESERVED_2 | RXFFF | RXFFE | TXFFF | TXFFE | EOT | TXS | RXS |
| R          | R     | R     | R     | R     | R   | R   | R   |
| 0h         | 0h    | 0h    | 0h    | 0h    | 0h  | 0h  | 0h  |

**Table 5-2523. MCSPI\_CH1STAT Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                             |
|------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED_2 | R    | 0h    | Read returns 0                                                                                                          |
| 6    | RXFFF      | R    | 0h    | Channel "i" FIFO Receive Buffer Full Status<br>0 FIFO receive buffer is not full<br>1 FIFO receive buffer is full       |
| 5    | RXFFE      | R    | 0h    | Channel "i" FIFO Receive Buffer Empty Status<br>0 FIFO receive buffer is not empty<br>1 FIFO receive buffer is empty    |
| 4    | TXFFF      | R    | 0h    | Channel "i" FIFO Transmit Buffer Full Status<br>0 FIFO transmit buffer is not full<br>1 FIFO transmit buffer is full    |
| 3    | TXFFE      | R    | 0h    | Channel "i" FIFO Transmit Buffer Empty Status<br>0 FIFO transmit buffer is not empty<br>1 FIFO transmit buffer is empty |

**Table 5-2523. MCSPI\_CH1STAT Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | EOT   | R    | 0h    | <p>Channel "i" End of transfer Status The definitions of beginning and end of transfer vary with controller versus responder and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details</p> <p>0 This flag is automatically cleared when the shift register is loaded with the data from the transmitter register (beginning of transfer).</p> <p>1 This flag is automatically set to one at the end of an MCSPI transfer.</p> |
| 1   | TXS   | R    | 0h    | <p>Channel "i" Transmitter Register Status</p> <p>0 Register is full.</p> <p>1 Register is empty.</p>                                                                                                                                                                                                                                                                                                                                                               |
| 0   | RXS   | R    | 0h    | <p>Channel "i" Receiver Register Status</p> <p>0 Register is empty.</p> <p>1 Register is full.</p>                                                                                                                                                                                                                                                                                                                                                                  |

### 5.14.2.18 MCSPI\_CH1CTRL Register

#### 1 MCSPI\_CH1CTRL Register (Offset = 148h) [reset = 0h]

This register is dedicated to enable the channel 1

Return to [Summary Table](#)

**Table 5-2524. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCSPI0        | 5220 0148h       |
| MCSPI1        | 5220 1148h       |
| MCSPI2        | 5220 2148h       |
| MCSPI3        | 5220 3148h       |
| MCSPI4        | 5220 4148h       |

**Figure 5-834. MCSPI\_CH1CTRL Name Register**

|            |    |    |    |    |    |    |     |
|------------|----|----|----|----|----|----|-----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24  |
| RESERVED_2 |    |    |    |    |    |    |     |
| R          |    |    |    |    |    |    |     |
| 0h         |    |    |    |    |    |    |     |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16  |
| RESERVED_2 |    |    |    |    |    |    |     |
| R          |    |    |    |    |    |    |     |
| 0h         |    |    |    |    |    |    |     |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8   |
| EXTCLK     |    |    |    |    |    |    |     |
| R/W        |    |    |    |    |    |    |     |
| 0h         |    |    |    |    |    |    |     |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0   |
| RESERVED_1 |    |    |    |    |    |    | EN  |
| R          |    |    |    |    |    |    | R/W |
| 0h         |    |    |    |    |    |    | 0h  |

**Table 5-2526. MCSPI\_CH1CTRL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                   |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED_2 | R    | 0h    | Read returns 0                                                                                                                                                                                                                                                                                                                                                                |
| 15:8  | EXTCLK     | R/W  | 0h    | <p>Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096clock divider ratio</p> <p>0      Clock ratio is CLKD + 1.<br/> 1      Clock ratio is CLKD + 1 + 16.<br/> FF     Clock ratio is CLKD + 1 + 4080.</p> |
| 7:1   | RESERVED_1 | R    | 0h    | Read returns 0                                                                                                                                                                                                                                                                                                                                                                |
| 0     | EN         | R/W  | 0h    | <p>Channel Enable</p> <p>0      Channel i is not active.<br/> 1      Channel i is active.</p>                                                                                                                                                                                                                                                                                 |



### 5.14.2.19 MCSPI\_TX1 Register

#### 1 MCSPI\_TX1 Register (Offset = 14Ch) [reset = 0h]

This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

Return to [Summary Table](#)

**Table 5-2527. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCSPI0        | 5220 014Ch       |
| MCSPI1        | 5220 114Ch       |
| MCSPI2        | 5220 214Ch       |
| MCSPI3        | 5220 314Ch       |
| MCSPI4        | 5220 414Ch       |

**Figure 5-835. MCSPI\_TX1 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TDATA |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TDATA |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TDATA |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TDATA |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-2529. MCSPI\_TX1 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                |
|------|-------|------|-------|----------------------------|
| 31:0 | TDATA | R/W  | 0h    | Channel 1 Data to transmit |

### 5.14.2.20 MCSPI\_RX1 Register

#### 1 MCSPI\_RX1 Register (Offset = 150h) [reset = 0h]

This register contains a single SPI word received through the serial link, what ever SPI word length is.

Return to [Summary Table](#)

**Table 5-2530. Instance Table**

| Instance Name | Physical Address  |
|---------------|-------------------|
| <b>MCSPI0</b> | <b>5220 0150h</b> |
| <b>MCSPI1</b> | <b>5220 1150h</b> |
| <b>MCSPI2</b> | <b>5220 2150h</b> |
| <b>MCSPI3</b> | <b>5220 3150h</b> |
| <b>MCSPI4</b> | <b>5220 4150h</b> |

**Figure 5-836. MCSPI\_RX1 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RDATA |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RDATA |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RDATA |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RDATA |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-2532. MCSPI\_RX1 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description             |
|------|-------|------|-------|-------------------------|
| 31:0 | RDATA | R    | 0h    | Channel 1 Received Data |

### 5.14.2.21 MCSPI\_CH2CONF Register

#### 1 MCSPI\_CH2CONF Register (Offset = 154h) [reset = 60000h]

This register is dedicated to the configuration of the channel 2

Return to [Summary Table](#)

**Table 5-2533. Instance Table**

| Instance Name | Physical Address  |
|---------------|-------------------|
| <b>MCSPI0</b> | <b>5220 0154h</b> |
| <b>MCSPI1</b> | <b>5220 1154h</b> |
| <b>MCSPI2</b> | <b>5220 2154h</b> |
| <b>MCSPI3</b> | <b>5220 3154h</b> |
| <b>MCSPI4</b> | <b>5220 4154h</b> |

**Figure 5-837. MCSPI\_CH2CONF Name Register**

|            |            |      |       |       |      |      |       |
|------------|------------|------|-------|-------|------|------|-------|
| 31         | 30         | 29   | 28    | 27    | 26   | 25   | 24    |
| RESERVED_0 |            | CLKG | FFER  | FFEW  | TCS2 |      | SBPOL |
| R          |            | R/W  | R/W   | R/W   | R/W  |      | R/W   |
| 0h         |            | 0h   | 0h    | 0h    | 0h   |      | 0h    |
| 23         | 22         | 21   | 20    | 19    | 18   | 17   | 16    |
| SBE        | RESERVED_1 |      | FORCE | TURBO | IS   | DPE1 | DPE0  |
| R/W        | R          |      | R/W   | R/W   | R/W  | R/W  | R/W   |
| 0h         | 0h         |      | 0h    | 0h    | 1h   | 1h   | 0h    |
| 15         | 14         | 13   | 12    | 11    | 10   | 9    | 8     |
| DMAR       | DMAW       | TRM  |       | WL    |      |      |       |
| R/W        | R/W        | R/W  |       | R/W   |      |      |       |
| 0h         | 0h         | 0h   |       | 0h    |      |      |       |
| 7          | 6          | 5    | 4     | 3     | 2    | 1    | 0     |
| WL         | EPOL       | CLKD |       |       |      | POL  | PHA   |
| R/W        | R/W        | R/W  |       |       |      | R/W  | R/W   |
| 0h         | 0h         | 0h   |       |       |      | 0h   | 0h    |

**Table 5-2535. MCSPI\_CH2CONF Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | RESERVED_0 | R    | 0h    | Read returns 0                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 29    | CLKG       | R/W  | 0h    | Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity<br>When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values<br>0 Clock granularity of power of 2<br>1 One clock cycle granularity |
| 28    | FFER       | R/W  | 0h    | FIFO enabled for receive:Only one channel can have this bit field set<br>0 The buffer is not used to receive data.<br>1 The buffer is used to receive data.                                                                                                                                                                                                                                                                                  |
| 27    | FFEW       | R/W  | 0h    | FIFO enabled for Transmit:Only one channel can have this bit field set<br>0 The buffer is not used to transmit data.<br>1 The buffer is used to transmit data.                                                                                                                                                                                                                                                                               |

**Table 5-2535. MCSPI\_CH2CONF Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:25 | TCS2       | R/W  | 0h    | <p>Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock</p> <p>0      0.5 clock cycle<br/> 1      1.5 clock cycles<br/> 2      2.5 clock cycles<br/> 3      3.5 clock cycles</p>                                                                                                                                |
| 24    | SBPOL      | R/W  | 0h    | <p>Start bit polarity</p> <p>0      SPICLK is held low during the INACTIVE state<br/> 1      SPICLK is held high during the INACTIVE state</p>                                                                                                                                                                                                                                                             |
| 23    | SBE        | R/W  | 0h    | <p>Start bit enable for SPI transfer</p> <p>0      Default MCSPI transfer length as specified by WL bit field<br/> 1      Start bit D/CX added before MCSPI transfer polarity is defined by MCSPI_CHCONF_0[24] SBPOL</p>                                                                                                                                                                                   |
| 22:21 | RESERVED_1 | R    | 0h    | Read returns 0                                                                                                                                                                                                                                                                                                                                                                                             |
| 20    | FORCE      | R/W  | 0h    | <p>Manual SPIEN assertion to keep SPIEN active between SPI words [single channel controller mode only]</p> <p>0      Writing 0 into this bit drives low the SPIEN line when MCSPI_CHCONF_2[6] EPOL=0, and drives it high when MCSPI_CHCONF_2[6] EPOL=1.<br/> 1      Writing 1 into this bit drives high the SPIEN line when MCSPI_CHCONF_2[6] EPOL=0, and drives it low when MCSPI_CHCONF_2[6] EPOL=1.</p> |
| 19    | TURBO      | R/W  | 0h    | <p>Turbo mode</p> <p>0      Turbo is deactivated (recommended for single MCSPI word transfer).<br/> 1      Turbo is activated to maximize the throughput for multiple MCSPI words transfer.</p>                                                                                                                                                                                                            |
| 18    | IS         | R/W  | 1h    | <p>Input Select</p> <p>0      Data line 0 (SPIDAT[0]) selected for reception<br/> 1      Data line 1 (SPIDAT[1]) selected for reception</p>                                                                                                                                                                                                                                                                |
| 17    | DPE1       | R/W  | 1h    | <p>Transmission Enable for data line 1 [SPIDATAGZEN[1]]</p> <p>0      Data line 1 (SPIDAT[1]) selected for transmission<br/> 1      No transmission on Data Line1 (SPIDAT[1])</p>                                                                                                                                                                                                                          |
| 16    | DPE0       | R/W  | 0h    | <p>Transmission Enable for data line 0 [SPIDATAGZEN[0]]</p> <p>0      Data Line0 (SPIDAT[0]) selected for transmission<br/> 1      No transmission on data line 0 (SPIDAT[0])</p>                                                                                                                                                                                                                          |
| 15    | DMAR       | R/W  | 0h    | <p>DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel</p> <p>0      DMA read request disabled<br/> 1      DMA read request enabled</p>                                                                |

**Table 5-2535. MCSPI\_CH2CONF Register Field Descriptions (continued)**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14    | DMAW  | R/W  | 0h    | <p>DMA Write request The DMA Write request line is asserted when the channel is enabled and the transmitter register of the channel is empty. The DMA Write request line is deasserted on load completion of the transmitter register of the channel.</p> <p>0 DMA write request disabled<br/>1 DMA write request enabled</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 13:12 | TRM   | R/W  | 0h    | <p>Transmit/Receive modes</p> <p>0 Transmit-and-receive mode<br/>1 Receive-only mode<br/>2 Transmit-only mode<br/>3 Reserved</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 11:7  | WL    | R/W  | 0h    | <p>SPI word length</p> <p>0 Reserved<br/>1 Reserved<br/>2 Reserved<br/>3 The MCSPI word is 4 bits long<br/>4 The MCSPI word is 5 bits long<br/>5 The MCSPI word is 6 bits long<br/>6 The MCSPI word is 7 bits long<br/>7 The MCSPI word is 8 bits long<br/>8 The MCSPI word is 9 bits long<br/>9 The MCSPI word is 10 bits long<br/>A The MCSPI word is 11 bits long<br/>B The MCSPI word is 12 bits long<br/>C The MCSPI word is 13 bits long<br/>D The MCSPI word is 14 bits long<br/>E The MCSPI word is 15 bits long<br/>F The MCSPI word is 16 bits long<br/>10 The MCSPI word is 17 bits long<br/>11 The MCSPI word is 18 bits long<br/>12 The MCSPI word is 19 bits long<br/>13 The MCSPI word is 20 bits long<br/>14 The MCSPI word is 21 bits long<br/>15 The MCSPI word is 22 bits long<br/>16 The MCSPI word is 23 bits long<br/>17 The MCSPI word is 24 bits long<br/>18 The MCSPI word is 25 bits long<br/>19 The MCSPI word is 26 bits long<br/>1A The MCSPI word is 27 bits long<br/>1B The MCSPI word is 28 bits long<br/>1C The MCSPI word is 29 bits long<br/>1D The MCSPI word is 30 bits long<br/>1E The MCSPI word is 31 bits long<br/>1F The MCSPI word is 32 bits long</p> |
| 6     | EPOL  | R/W  | 0h    | <p>SPIEN polarity</p> <p>0 SPICLK is held low during the INACTIVE state<br/>1 SPICLK is held high during the INACTIVE state</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

**Table 5-2535. MCSPI\_CH2CONF Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5:2 | CLKD  | R/W  | 0h    | <p>Frequency divider for SPICLK [only when the module is a Controller SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0</p> <p>0<br/>1<br/>2<br/>3<br/>4      16<br/>5      32<br/>6      64<br/>7      128<br/>8      256<br/>9      512<br/>A      1024<br/>B      2048<br/>C      4096<br/>D      8192<br/>E      16384<br/>F      32768</p> |
| 1   | POL   | R/W  | 0h    | <p>SPICLK polarity</p> <p>0      SPICLK is held low during the INACTIVE state<br/>1      SPICLK is held high during the INACTIVE state</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 0   | PHA   | R/W  | 0h    | <p>SPICLK phase</p> <p>0      Data are latched on odd-numbered edges of SPICLK.<br/>1      Data are latched on even-numbered edges of SPICLK.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

### 5.14.2.22 MCSPI\_CH2STAT Register

#### 1 MCSPI\_CH2STAT Register (Offset = 158h) [reset = 0h]

This register provides status information about transmitter and receiver registers of channel 2

Return to [Summary Table](#)

**Table 5-2536. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCSPI0        | 5220 0158h       |
| MCSPI1        | 5220 1158h       |
| MCSPI2        | 5220 2158h       |
| MCSPI3        | 5220 3158h       |
| MCSPI4        | 5220 4158h       |

**Figure 5-838. MCSPI\_CH2STAT Name Register**

|            |       |       |       |       |     |     |     |
|------------|-------|-------|-------|-------|-----|-----|-----|
| 31         | 30    | 29    | 28    | 27    | 26  | 25  | 24  |
| RESERVED_2 |       |       |       |       |     |     |     |
| R          |       |       |       |       |     |     |     |
| 0h         |       |       |       |       |     |     |     |
| 23         | 22    | 21    | 20    | 19    | 18  | 17  | 16  |
| RESERVED_2 |       |       |       |       |     |     |     |
| R          |       |       |       |       |     |     |     |
| 0h         |       |       |       |       |     |     |     |
| 15         | 14    | 13    | 12    | 11    | 10  | 9   | 8   |
| RESERVED_2 |       |       |       |       |     |     |     |
| R          |       |       |       |       |     |     |     |
| 0h         |       |       |       |       |     |     |     |
| 7          | 6     | 5     | 4     | 3     | 2   | 1   | 0   |
| RESERVED_2 | RXFFF | RXFFE | TXFFF | TXFFE | EOT | TXS | RXS |
| R          | R     | R     | R     | R     | R   | R   | R   |
| 0h         | 0h    | 0h    | 0h    | 0h    | 0h  | 0h  | 0h  |

**Table 5-2538. MCSPI\_CH2STAT Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                             |
|------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED_2 | R    | 0h    | Read returns 0                                                                                                          |
| 6    | RXFFF      | R    | 0h    | Channel "i" FIFO Receive Buffer Full Status<br>0 FIFO receive buffer is not full<br>1 FIFO receive buffer is full       |
| 5    | RXFFE      | R    | 0h    | Channel "i" FIFO Receive Buffer Empty Status<br>0 FIFO receive buffer is not empty<br>1 FIFO receive buffer is empty    |
| 4    | TXFFF      | R    | 0h    | Channel "i" FIFO Transmit Buffer Full Status<br>0 FIFO transmit buffer is not full<br>1 FIFO transmit buffer is full    |
| 3    | TXFFE      | R    | 0h    | Channel "i" FIFO Transmit Buffer Empty Status<br>0 FIFO transmit buffer is not empty<br>1 FIFO transmit buffer is empty |

**Table 5-2538. MCSPI\_CH2STAT Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | EOT   | R    | 0h    | <p>Channel "i" End of transfer Status The definitions of beginning and end of transfer vary with controller versus responder and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details</p> <p>0 This flag is automatically cleared when the shift register is loaded with the data from the transmitter register (beginning of transfer).</p> <p>1 This flag is automatically set to one at the end of an MCSPI transfer.</p> |
| 1   | TXS   | R    | 0h    | <p>Channel "i" Transmitter Register Status</p> <p>0 Register is full.</p> <p>1 Register is empty.</p>                                                                                                                                                                                                                                                                                                                                                               |
| 0   | RXS   | R    | 0h    | <p>Channel "i" Receiver Register Status</p> <p>0 Register is empty.</p> <p>1 Register is full.</p>                                                                                                                                                                                                                                                                                                                                                                  |



### 5.14.2.23 MCSPI\_CH2CTRL Register

#### 1 MCSPI\_CH2CTRL Register (Offset = 15Ch) [reset = 0h]

This register is dedicated to enable the channel 2

Return to [Summary Table](#)

**Table 5-2539. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCSPI0        | 5220 015Ch       |
| MCSPI1        | 5220 115Ch       |
| MCSPI2        | 5220 215Ch       |
| MCSPI3        | 5220 315Ch       |
| MCSPI4        | 5220 415Ch       |

**Figure 5-839. MCSPI\_CH2CTRL Name Register**

|            |    |    |    |    |    |    |     |
|------------|----|----|----|----|----|----|-----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24  |
| RESERVED_2 |    |    |    |    |    |    |     |
| R          |    |    |    |    |    |    |     |
| 0h         |    |    |    |    |    |    |     |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16  |
| RESERVED_2 |    |    |    |    |    |    |     |
| R          |    |    |    |    |    |    |     |
| 0h         |    |    |    |    |    |    |     |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8   |
| EXTCLK     |    |    |    |    |    |    |     |
| R/W        |    |    |    |    |    |    |     |
| 0h         |    |    |    |    |    |    |     |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0   |
| RESERVED_1 |    |    |    |    |    |    | EN  |
| R          |    |    |    |    |    |    | R/W |
| 0h         |    |    |    |    |    |    | 0h  |

**Table 5-2541. MCSPI\_CH2CTRL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                   |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED_2 | R    | 0h    | Read returns 0                                                                                                                                                                                                                                                                                                                                                                |
| 15:8  | EXTCLK     | R/W  | 0h    | <p>Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096clock divider ratio</p> <p>0      Clock ratio is CLKD + 1.<br/> 1      Clock ratio is CLKD + 1 + 16.<br/> FF     Clock ratio is CLKD + 1 + 4080.</p> |
| 7:1   | RESERVED_1 | R    | 0h    | Read returns 0                                                                                                                                                                                                                                                                                                                                                                |
| 0     | EN         | R/W  | 0h    | <p>Channel Enable</p> <p>0      Channel i is not active.<br/> 1      Channel i is active.</p>                                                                                                                                                                                                                                                                                 |

#### 5.14.2.24 MCSPI\_TX2 Register

##### 1 MCSPI\_TX2 Register (Offset = 160h) [reset = 0h]

This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

Return to [Summary Table](#)

**Table 5-2542. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCSPI0        | 5220 0160h       |
| MCSPI1        | 5220 1160h       |
| MCSPI2        | 5220 2160h       |
| MCSPI3        | 5220 3160h       |
| MCSPI4        | 5220 4160h       |

**Figure 5-840. MCSPI\_TX2 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TDATA |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TDATA |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TDATA |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TDATA |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-2544. MCSPI\_TX2 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                |
|------|-------|------|-------|----------------------------|
| 31:0 | TDATA | R/W  | 0h    | Channel 2 Data to transmit |

### 5.14.2.25 MCSPI\_RX2 Register

#### 1 MCSPI\_RX2 Register (Offset = 164h) [reset = 0h]

This register contains a single SPI word received through the serial link, what ever SPI word length is.

Return to [Summary Table](#)

**Table 5-2545. Instance Table**

| Instance Name | Physical Address  |
|---------------|-------------------|
| <b>MCSPI0</b> | <b>5220 0164h</b> |
| <b>MCSPI1</b> | <b>5220 1164h</b> |
| <b>MCSPI2</b> | <b>5220 2164h</b> |
| <b>MCSPI3</b> | <b>5220 3164h</b> |
| <b>MCSPI4</b> | <b>5220 4164h</b> |

**Figure 5-841. MCSPI\_RX2 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RDATA |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RDATA |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RDATA |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RDATA |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-2547. MCSPI\_RX2 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description             |
|------|-------|------|-------|-------------------------|
| 31:0 | RDATA | R    | 0h    | Channel 2 Received Data |

### 5.14.2.26 MCSPI\_CH3CONF Register

#### 1 MCSPI\_CH3CONF Register (Offset = 168h) [reset = 60000h]

This register is dedicated to the configuration of the channel 3

Return to [Summary Table](#)

**Table 5-2548. Instance Table**

| Instance Name | Physical Address  |
|---------------|-------------------|
| <b>MCSPI0</b> | <b>5220 0168h</b> |
| <b>MCSPI1</b> | <b>5220 1168h</b> |
| <b>MCSPI2</b> | <b>5220 2168h</b> |
| <b>MCSPI3</b> | <b>5220 3168h</b> |
| <b>MCSPI4</b> | <b>5220 4168h</b> |

**Figure 5-842. MCSPI\_CH3CONF Name Register**

|            |            |      |       |       |      |      |       |
|------------|------------|------|-------|-------|------|------|-------|
| 31         | 30         | 29   | 28    | 27    | 26   | 25   | 24    |
| RESERVED_0 |            | CLKG | FFER  | FFEW  | TCS3 |      | SBPOL |
| R          |            | R/W  | R/W   | R/W   | R/W  |      | R/W   |
| 0h         |            | 0h   | 0h    | 0h    | 0h   |      | 0h    |
| 23         | 22         | 21   | 20    | 19    | 18   | 17   | 16    |
| SBE        | RESERVED_1 |      | FORCE | TURBO | IS   | DPE1 | DPE0  |
| R/W        | R          |      | R/W   | R/W   | R/W  | R/W  | R/W   |
| 0h         | 0h         |      | 0h    | 0h    | 1h   | 1h   | 0h    |
| 15         | 14         | 13   | 12    | 11    | 10   | 9    | 8     |
| DMAR       | DMAW       | TRM  |       | WL    |      |      |       |
| R/W        | R/W        | R/W  |       | R/W   |      |      |       |
| 0h         | 0h         | 0h   |       | 0h    |      |      |       |
| 7          | 6          | 5    | 4     | 3     | 2    | 1    | 0     |
| WL         | EPOL       | CLKD |       |       |      | POL  | PHA   |
| R/W        | R/W        | R/W  |       |       |      | R/W  | R/W   |
| 0h         | 0h         | 0h   |       |       |      | 0h   | 0h    |

**Table 5-2550. MCSPI\_CH3CONF Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | RESERVED_0 | R    | 0h    | Read returns 0                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 29    | CLKG       | R/W  | 0h    | Clock divider granularity This register defines the granularity of channel clock divider: power of two or one clock cycle granularity<br>When this bit is set the register MCSPI_CHCTRL[EXTCLK] must be configured to reach a maximum of 4096clock divider ratio Then The clock divider ratio is a concatenation of MCSPI_CHCONF[CLKD] and MCSPI_CHCTRL[EXTCLK] values<br>0 Clock granularity of power of 2<br>1 One clock cycle granularity |
| 28    | FFER       | R/W  | 0h    | FIFO enabled for receive:Only one channel can have this bit field set<br>0 The buffer is not used to receive data.<br>1 The buffer is used to receive data.                                                                                                                                                                                                                                                                                  |
| 27    | FFEW       | R/W  | 0h    | FIFO enabled for Transmit:Only one channel can have this bit field set<br>0 The buffer is not used to transmit data.<br>1 The buffer is used to transmit data.                                                                                                                                                                                                                                                                               |

**Table 5-2550. MCSPI\_CH3CONF Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26:25 | TCS3       | R/W  | 0h    | <p>Chip Select Time Control This 2-bits field defines the number of interface clock cycles between CS toggling and first or last edge of SPI clock</p> <p>0      0.5 clock cycle<br/> 1      1.5 clock cycles<br/> 2      2.5 clock cycles<br/> 3      3.5 clock cycles</p>                                                                                                                                |
| 24    | SBPOL      | R/W  | 0h    | <p>Start bit polarity</p> <p>0      SPICLK is held low during the INACTIVE state<br/> 1      SPICLK is held high during the INACTIVE state</p>                                                                                                                                                                                                                                                             |
| 23    | SBE        | R/W  | 0h    | <p>Start bit enable for SPI transfer</p> <p>0      Default MCSPI transfer length as specified by WL bit field<br/> 1      Start bit D/CX added before MCSPI transfer polarity is defined by MCSPI_CHCONF_0[24] SBPOL</p>                                                                                                                                                                                   |
| 22:21 | RESERVED_1 | R    | 0h    | Read returns 0                                                                                                                                                                                                                                                                                                                                                                                             |
| 20    | FORCE      | R/W  | 0h    | <p>Manual SPIEN assertion to keep SPIEN active between SPI words [single channel controller mode only]</p> <p>0      Writing 0 into this bit drives low the SPIEN line when MCSPI_CHCONF_3[6] EPOL=0, and drives it high when MCSPI_CHCONF_3[6] EPOL=1.<br/> 1      Writing 1 into this bit drives high the SPIEN line when MCSPI_CHCONF_3[6] EPOL=0, and drives it low when MCSPI_CHCONF_3[6] EPOL=1.</p> |
| 19    | TURBO      | R/W  | 0h    | <p>Turbo mode</p> <p>0      Turbo is deactivated (recommended for single MCSPI word transfer).<br/> 1      Turbo is activated to maximize the throughput for multiple MCSPI words transfer.</p>                                                                                                                                                                                                            |
| 18    | IS         | R/W  | 1h    | <p>Input Select</p> <p>0      Data line 0 (SPIDAT[0]) selected for reception<br/> 1      Data line 1 (SPIDAT[1]) selected for reception</p>                                                                                                                                                                                                                                                                |
| 17    | DPE1       | R/W  | 1h    | <p>Transmission Enable for data line 1 [SPIDATAGZEN[1]]</p> <p>0      Data line 1 (SPIDAT[1]) selected for transmission<br/> 1      No transmission on Data Line1 (SPIDAT[1])</p>                                                                                                                                                                                                                          |
| 16    | DPE0       | R/W  | 0h    | <p>Transmission Enable for data line 0 [SPIDATAGZEN[0]]</p> <p>0      Data Line0 (SPIDAT[0]) selected for transmission<br/> 1      No transmission on data line 0 (SPIDAT[0])</p>                                                                                                                                                                                                                          |
| 15    | DMAR       | R/W  | 0h    | <p>DMA Read request The DMA Read request line is asserted when the channel is enabled and a new data is available in the receive register of the channel The DMA Read request line is deasserted on read completion of the receive register of the channel</p> <p>0      DMA read request disabled<br/> 1      DMA read request enabled</p>                                                                |

**Table 5-2550. MCSPI\_CH3CONF Register Field Descriptions (continued)**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14    | DMAW  | R/W  | 0h    | <p>DMA Write request The DMA Write request line is asserted when the channel is enabled and the transmitter register of the channel is empty. The DMA Write request line is deasserted on load completion of the transmitter register of the channel.</p> <p>0 DMA write request disabled<br/>1 DMA write request enabled</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 13:12 | TRM   | R/W  | 0h    | <p>Transmit/Receive modes</p> <p>0 Transmit-and-receive mode<br/>1 Receive-only mode<br/>2 Transmit-only mode<br/>3 Reserved</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 11:7  | WL    | R/W  | 0h    | <p>SPI word length</p> <p>0 Reserved<br/>1 Reserved<br/>2 Reserved<br/>3 The MCSPI word is 4 bits long<br/>4 The MCSPI word is 5 bits long<br/>5 The MCSPI word is 6 bits long<br/>6 The MCSPI word is 7 bits long<br/>7 The MCSPI word is 8 bits long<br/>8 The MCSPI word is 9 bits long<br/>9 The MCSPI word is 10 bits long<br/>A The MCSPI word is 11 bits long<br/>B The MCSPI word is 12 bits long<br/>C The MCSPI word is 13 bits long<br/>D The MCSPI word is 14 bits long<br/>E The MCSPI word is 15 bits long<br/>F The MCSPI word is 16 bits long<br/>10 The MCSPI word is 17 bits long<br/>11 The MCSPI word is 18 bits long<br/>12 The MCSPI word is 19 bits long<br/>13 The MCSPI word is 20 bits long<br/>14 The MCSPI word is 21 bits long<br/>15 The MCSPI word is 22 bits long<br/>16 The MCSPI word is 23 bits long<br/>17 The MCSPI word is 24 bits long<br/>18 The MCSPI word is 25 bits long<br/>19 The MCSPI word is 26 bits long<br/>1A The MCSPI word is 27 bits long<br/>1B The MCSPI word is 28 bits long<br/>1C The MCSPI word is 29 bits long<br/>1D The MCSPI word is 30 bits long<br/>1E The MCSPI word is 31 bits long<br/>1F The MCSPI word is 32 bits long</p> |
| 6     | EPOL  | R/W  | 0h    | <p>SPIEN polarity</p> <p>0 SPICLK is held low during the INACTIVE state<br/>1 SPICLK is held high during the INACTIVE state</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

**Table 5-2550. MCSPI\_CH3CONF Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5:2 | CLKD  | R/W  | 0h    | <p>Frequency divider for SPICLK [only when the module is a Controller SPI device] A programmable clock divider divides the SPI reference clock [CLKSPIREF] with a 4-bit value, and results in a new clock SPICLK available to shift-in and shift-out data By default the clock divider ratio has a power of two granularity when MCSPI_CHCONF[CLKG] is cleared, Otherwise this register is the 4 LSB bit of a 12-bit register concatenated with clock divider extension MCSPI_CHCTRL[EXTCLK] registerThe value description below defines the clock ratio when MCSPI_CHCONF[CLKG] is set to 0</p> <p>0<br/>1<br/>2<br/>3<br/>4      16<br/>5      32<br/>6      64<br/>7      128<br/>8      256<br/>9      512<br/>A      1024<br/>B      2048<br/>C      4096<br/>D      8192<br/>E      16384<br/>F      32768</p> |
| 1   | POL   | R/W  | 0h    | <p>SPICLK polarity</p> <p>0      SPICLK is held low during the INACTIVE state<br/>1      SPICLK is held high during the INACTIVE state</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 0   | PHA   | R/W  | 0h    | <p>SPICLK phase</p> <p>0      Data are latched on odd-numbered edges of SPICLK.<br/>1      Data are latched on even-numbered edges of SPICLK.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

### 5.14.2.27 MCSPI\_CH3STAT Register

#### 1 MCSPI\_CH3STAT Register (Offset = 16Ch) [reset = 0h]

This register provides status information about transmitter and receiver registers of channel 3

Return to [Summary Table](#)

**Table 5-2551. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCSPI0        | 5220 016Ch       |
| MCSPI1        | 5220 116Ch       |
| MCSPI2        | 5220 216Ch       |
| MCSPI3        | 5220 316Ch       |
| MCSPI4        | 5220 416Ch       |

**Figure 5-843. MCSPI\_CH3STAT Name Register**

|            |       |       |       |       |     |     |     |
|------------|-------|-------|-------|-------|-----|-----|-----|
| 31         | 30    | 29    | 28    | 27    | 26  | 25  | 24  |
| RESERVED_2 |       |       |       |       |     |     |     |
| R          |       |       |       |       |     |     |     |
| 0h         |       |       |       |       |     |     |     |
| 23         | 22    | 21    | 20    | 19    | 18  | 17  | 16  |
| RESERVED_2 |       |       |       |       |     |     |     |
| R          |       |       |       |       |     |     |     |
| 0h         |       |       |       |       |     |     |     |
| 15         | 14    | 13    | 12    | 11    | 10  | 9   | 8   |
| RESERVED_2 |       |       |       |       |     |     |     |
| R          |       |       |       |       |     |     |     |
| 0h         |       |       |       |       |     |     |     |
| 7          | 6     | 5     | 4     | 3     | 2   | 1   | 0   |
| RESERVED_2 | RXFFF | RXFFE | TXFFF | TXFFE | EOT | TXS | RXS |
| R          | R     | R     | R     | R     | R   | R   | R   |
| 0h         | 0h    | 0h    | 0h    | 0h    | 0h  | 0h  | 0h  |

**Table 5-2553. MCSPI\_CH3STAT Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                             |
|------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED_2 | R    | 0h    | Read returns 0                                                                                                          |
| 6    | RXFFF      | R    | 0h    | Channel "i" FIFO Receive Buffer Full Status<br>0 FIFO receive buffer is not full<br>1 FIFO receive buffer is full       |
| 5    | RXFFE      | R    | 0h    | Channel "i" FIFO Receive Buffer Empty Status<br>0 FIFO receive buffer is not empty<br>1 FIFO receive buffer is empty    |
| 4    | TXFFF      | R    | 0h    | Channel "i" FIFO Transmit Buffer Full Status<br>0 FIFO transmit buffer is not full<br>1 FIFO transmit buffer is full    |
| 3    | TXFFE      | R    | 0h    | Channel "i" FIFO Transmit Buffer Empty Status<br>0 FIFO transmit buffer is not empty<br>1 FIFO transmit buffer is empty |



**Table 5-2553. MCSPI\_CH3STAT Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | EOT   | R    | 0h    | <p>Channel "i" End of transfer Status The definitions of beginning and end of transfer vary with controller versus responder and the transfer format [Transmit/Receive modes, Turbo mode] See dedicated chapters for details</p> <p>0 This flag is automatically cleared when the shift register is loaded with the data from the transmitter register (beginning of transfer).</p> <p>1 This flag is automatically set to one at the end of an MCSPI transfer.</p> |
| 1   | TXS   | R    | 0h    | <p>Channel "i" Transmitter Register Status</p> <p>0 Register is full.</p> <p>1 Register is empty.</p>                                                                                                                                                                                                                                                                                                                                                               |
| 0   | RXS   | R    | 0h    | <p>Channel "i" Receiver Register Status</p> <p>0 Register is empty.</p> <p>1 Register is full.</p>                                                                                                                                                                                                                                                                                                                                                                  |

### 5.14.2.28 MCSPI\_CH3CTRL Register

#### 1 MCSPI\_CH3CTRL Register (Offset = 170h) [reset = 0h]

This register is dedicated to enable the channel 3

Return to [Summary Table](#)

**Table 5-2554. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCSPI0        | 5220 0170h       |
| MCSPI1        | 5220 1170h       |
| MCSPI2        | 5220 2170h       |
| MCSPI3        | 5220 3170h       |
| MCSPI4        | 5220 4170h       |

**Figure 5-844. MCSPI\_CH3CTRL Name Register**

|            |    |    |    |    |    |    |     |
|------------|----|----|----|----|----|----|-----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24  |
| RESERVED_2 |    |    |    |    |    |    |     |
| R          |    |    |    |    |    |    |     |
| 0h         |    |    |    |    |    |    |     |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16  |
| RESERVED_2 |    |    |    |    |    |    |     |
| R          |    |    |    |    |    |    |     |
| 0h         |    |    |    |    |    |    |     |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8   |
| EXTCLK     |    |    |    |    |    |    |     |
| R/W        |    |    |    |    |    |    |     |
| 0h         |    |    |    |    |    |    |     |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0   |
| RESERVED_1 |    |    |    |    |    |    | EN  |
| R          |    |    |    |    |    |    | R/W |
| 0h         |    |    |    |    |    |    | 0h  |

**Table 5-2556. MCSPI\_CH3CTRL Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                        |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED_2 | R    | 0h    | Read returns 0                                                                                                                                                                                                                                                                                                                                                     |
| 15:8  | EXTCLK     | R/W  | 0h    | Clock ratio extension: This register is used to concatenate with MCSPI_CHCONF[CLKD] register for clock ratio only when granularity is one clock cycle [MCSPI_CHCONF[CLKG] set to 1] Then the max value reached is 4096clock divider ratio<br><br>0      Clock ratio is CLKD + 1.<br>1      Clock ratio is CLKD + 1 + 16.<br>FF     Clock ratio is CLKD + 1 + 4080. |
| 7:1   | RESERVED_1 | R    | 0h    | Read returns 0                                                                                                                                                                                                                                                                                                                                                     |
| 0     | EN         | R/W  | 0h    | Channel Enable<br><br>0      Channel i is not active.<br>1      Channel i is active.                                                                                                                                                                                                                                                                               |

### 5.14.2.29 MCSPI\_TX3 Register

#### 1 MCSPI\_TX3 Register (Offset = 174h) [reset = 0h]

This register contains a single SPI word to transmit on the serial link, what ever SPI word length is.

Return to [Summary Table](#)

**Table 5-2557. Instance Table**

| Instance Name | Physical Address  |
|---------------|-------------------|
| <b>MCSPI0</b> | <b>5220 0174h</b> |
| <b>MCSPI1</b> | <b>5220 1174h</b> |
| <b>MCSPI2</b> | <b>5220 2174h</b> |
| <b>MCSPI3</b> | <b>5220 3174h</b> |
| <b>MCSPI4</b> | <b>5220 4174h</b> |

**Figure 5-845. MCSPI\_TX3 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TDATA |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TDATA |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TDATA |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TDATA |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-2559. MCSPI\_TX3 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                |
|------|-------|------|-------|----------------------------|
| 31:0 | TDATA | R/W  | 0h    | Channel 3 Data to transmit |

### 5.14.2.30 MCSPI\_RX3 Register

#### 1 MCSPI\_RX3 Register (Offset = 178h) [reset = 0h]

This register contains a single SPI word received through the serial link, what ever SPI word length is.

Return to [Summary Table](#)

**Table 5-2560. Instance Table**

| Instance Name | Physical Address  |
|---------------|-------------------|
| <b>MCSPI0</b> | <b>5220 0178h</b> |
| <b>MCSPI1</b> | <b>5220 1178h</b> |
| <b>MCSPI2</b> | <b>5220 2178h</b> |
| <b>MCSPI3</b> | <b>5220 3178h</b> |
| <b>MCSPI4</b> | <b>5220 4178h</b> |

**Figure 5-846. MCSPI\_RX3 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RDATA |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RDATA |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RDATA |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RDATA |    |    |    |    |    |    |    |
| R     |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-2562. MCSPI\_RX3 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description             |
|------|-------|------|-------|-------------------------|
| 31:0 | RDATA | R    | 0h    | Channel 3 Received Data |

### 5.14.2.31 MCSPI\_XFERLEVEL Register

#### 1 MCSPI\_XFERLEVEL Register (Offset = 17Ch) [reset = 0h]

This register provides transfer levels needed while using FIFO buffer during transfer.

Return to [Summary Table](#)

**Table 5-2563. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCSPI0        | 5220 017Ch       |
| MCSPI1        | 5220 117Ch       |
| MCSPI2        | 5220 217Ch       |
| MCSPI3        | 5220 317Ch       |
| MCSPI4        | 5220 417Ch       |

**Figure 5-847. MCSPI\_XFERLEVEL Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| WCNT |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| WCNT |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| AFL  |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| AEL  |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-2565. MCSPI\_XFERLEVEL Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                         |
|-------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | WCNT  | R/W  | 0h    | <p>Spi word counterThis register holds the programmable value of number of SPI word to be transferred on channel which is using the FIFO bufferWhen transfer had started, a read back in this register returns the current SPI word transfer index</p> <p>0 Counter not used<br/>1 One word<br/>FFFE 65534 MCSPI word<br/>FFFF 65535 MCSPI word</p> |

**Table 5-2565. MCSPI\_XFERLEVEL Register Field Descriptions (continued)**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | AFL   | R/W  | 0h    | <p>Buffer Almost Full This register holds the programmable almost full level value used to determine almost full buffer condition. If the user wants an interrupt or a DMA read request to be issued during a receive operation when the data buffer holds at least n bytes, then the buffer MCSPI_MODULCTRL[AFL] must be set with n-1. The size of this register is defined by the generic parameter FFBYTE.</p> <p>0      1 byte<br/> 1      2 bytes<br/> FE     255 bytes<br/> FF     256 bytes</p> |
| 7:0  | AEL   | R/W  | 0h    | <p>Buffer Almost Empty This register holds the programmable almost empty level value used to determine almost empty buffer condition. If the user wants an interrupt or a DMA write request to be issued during a transmit operation when the data buffer is able to receive n bytes, then the buffer MCSPI_MODULCTRL[AEL] must be set with n-1.</p> <p>0      1 byte<br/> 1      2 bytes<br/> FE     255 bytes<br/> FF     256 bytes</p>                                                              |

### 5.14.2.32 MCSPI\_DAFTX Register

#### 1 MCSPI\_DAFTX Register (Offset = 180h) [reset = 0h]

This register contains the SPI words to transmit on the serial link when FIFO used and DMA address is aligned on 256 bit. This register is an image of one of MCSPI\_TX(i) register corresponding to the channel which have its FIFO enabled.

Return to [Summary Table](#)

**Table 5-2566. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCSPI0        | 5220 0180h       |
| MCSPI1        | 5220 1180h       |
| MCSPI2        | 5220 2180h       |
| MCSPI3        | 5220 3180h       |
| MCSPI4        | 5220 4180h       |

**Figure 5-848. MCSPI\_DAFTX Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DAFTDATA |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DAFTDATA |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DAFTDATA |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DAFTDATA |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2568. MCSPI\_DAFTX Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                            |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | DAFTDATA | R/W  | 0h    | FIFO Data to transmit with DMA 256 bit aligned address This Register is only is used when MCSPI_MODULCTRL[FDA] is set to "1" and only one of the MCSPI_CH[i]CONF[FEW] of enabled channels is set If these conditions are not respected any access to this register return a null value |

### 5.14.2.33 MCSPI\_DAFRX Register

#### 1 MCSPI\_DAFRX Register (Offset = 1A0h) [reset = 0h]

This register contains the SPI words to received on the serial link when FIFO used and DMA address is aligned on 256 bit. This register is an image of one of MCSPI\_RX(i) register corresponding to the channel which have its FIFO enabled.

Return to [Summary Table](#)

**Table 5-2569. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MCSPI0        | 5220 01A0h       |
| MCSPI1        | 5220 11A0h       |
| MCSPI2        | 5220 21A0h       |
| MCSPI3        | 5220 31A0h       |
| MCSPI4        | 5220 41A0h       |

**Figure 5-849. MCSPI\_DAFRX Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DAFRDATA |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DAFRDATA |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DAFRDATA |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DAFRDATA |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2571. MCSPI\_DAFRX Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                            |
|------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | DAFRDATA | R    | 0h    | FIFO Data to transmit with DMA 256 bit aligned address This Register is only is used when MCSPI_MODULCTRL[FDA] is set to "1" and only one of the MCSPI_CH[i]CONF[FEW] of enabled channels is set If these conditions are not respected any access to this register return a null value |



## 5.15 MMCSD

### MMCSD

#### 5.15.1 MMCSD Summaries

#### MMCSD Summaries

**Table 5-2572. MMC Registers, Base Address=4830 0000h, Length=8192**

| Offset | Length | Register Name                     | MMCSD0 Physical Address |
|--------|--------|-----------------------------------|-------------------------|
| 4h     | 32     | <a href="#">MMC_HL_HWINFO</a>     | 4830 0004h              |
| 10h    | 32     | <a href="#">MMC_HL_SYSCONFIG</a>  | 4830 0010h              |
| 114h   | 32     | <a href="#">MMC_SYSSTATUS</a>     | 4830 0114h              |
| 124h   | 32     | <a href="#">MMC_CSRE</a>          | 4830 0124h              |
| 128h   | 32     | <a href="#">MMC_SYSTEST</a>       | 4830 0128h              |
| 12Ch   | 32     | <a href="#">MMC_CON</a>           | 4830 012Ch              |
| 130h   | 32     | <a href="#">MMC_PWCNT</a>         | 4830 0130h              |
| 134h   | 32     | <a href="#">MMC_DLL</a>           | 4830 0134h              |
| 200h   | 32     | <a href="#">MMC_SDMASA</a>        | 4830 0200h              |
| 204h   | 32     | <a href="#">MMC_BLK</a>           | 4830 0204h              |
| 208h   | 32     | <a href="#">MMC_ARG</a>           | 4830 0208h              |
| 20Ch   | 32     | <a href="#">MMC_CMD</a>           | 4830 020Ch              |
| 210h   | 32     | <a href="#">MMC_RSP10</a>         | 4830 0210h              |
| 214h   | 32     | <a href="#">MMC_RSP32</a>         | 4830 0214h              |
| 218h   | 32     | <a href="#">MMC_RSP54</a>         | 4830 0218h              |
| 21Ch   | 32     | <a href="#">MMC_RSP76</a>         | 4830 021Ch              |
| 220h   | 32     | <a href="#">MMC_DATA</a>          | 4830 0220h              |
| 224h   | 32     | <a href="#">MMC_PSTATE</a>        | 4830 0224h              |
| 228h   | 32     | <a href="#">MMC_HCTL</a>          | 4830 0228h              |
| 22Ch   | 32     | <a href="#">MMC_SYSCTL</a>        | 4830 022Ch              |
| 230h   | 32     | <a href="#">MMC_STAT</a>          | 4830 0230h              |
| 234h   | 32     | <a href="#">MMC_IE</a>            | 4830 0234h              |
| 238h   | 32     | <a href="#">MMC_ISE</a>           | 4830 0238h              |
| 23Ch   | 32     | <a href="#">MMC_AC12</a>          | 4830 023Ch              |
| 240h   | 32     | <a href="#">MMC_CAPA</a>          | 4830 0240h              |
| 244h   | 32     | <a href="#">MMC_CAPA2</a>         | 4830 0244h              |
| 248h   | 32     | <a href="#">MMC_CUR_CAPA</a>      | 4830 0248h              |
| 250h   | 32     | <a href="#">MMC_FE</a>            | 4830 0250h              |
| 254h   | 32     | <a href="#">MMC_ADMAES</a>        | 4830 0254h              |
| 258h   | 32     | <a href="#">MMC_ADMASAL</a>       | 4830 0258h              |
| 260h   | 32     | <a href="#">MMC_PVINITSD</a>      | 4830 0260h              |
| 264h   | 32     | <a href="#">MMC_PVHSSDR12</a>     | 4830 0264h              |
| 268h   | 32     | <a href="#">MMC_PVSDR25SDR50</a>  | 4830 0268h              |
| 26Ch   | 32     | <a href="#">MMC_PVSDR104DDR50</a> | 4830 026Ch              |
| 2FCh   | 32     | <a href="#">MMC_REV</a>           | 4830 02FCh              |

### **5.15.2 MMCSD Registers**

#### **MMCSD Registers**

### 5.15.2.1 MMC\_HL\_HWINFO Register

#### 1 MMC\_HL\_HWINFO Register (Offset = 4h) [reset = 8h]

Information about the IP module's hardware configuration, i.e. typically the module's HDL generics (if any). Actual field format and encoding is up to the module's designer to decide.

Return to [Summary Table](#)

**Table 5-2573. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCS0         | 4830 0004h       |

**Figure 5-850. MMC\_HL\_HWINFO Name Register**

|          |         |          |    |    |    |           |          |
|----------|---------|----------|----|----|----|-----------|----------|
| 31       | 30      | 29       | 28 | 27 | 26 | 25        | 24       |
| RESERVED |         |          |    |    |    |           |          |
| R        |         |          |    |    |    |           |          |
| 0h       |         |          |    |    |    |           |          |
| 23       | 22      | 21       | 20 | 19 | 18 | 17        | 16       |
| RESERVED |         |          |    |    |    |           |          |
| R        |         |          |    |    |    |           |          |
| 0h       |         |          |    |    |    |           |          |
| 15       | 14      | 13       | 12 | 11 | 10 | 9         | 8        |
| RESERVED |         |          |    |    |    |           |          |
| R        |         |          |    |    |    |           |          |
| 0h       |         |          |    |    |    |           |          |
| 7        | 6       | 5        | 4  | 3  | 2  | 1         | 0        |
| RESERVED | RETMODE | MEM_SIZE |    |    |    | MERGE_MEM | MADMA_EN |
| R        | R       | R        |    |    |    | R         | R        |
| 0h       | 0h      | 2h       |    |    |    | 0h        | 0h       |

**Table 5-2575. MMC\_HL\_HWINFO Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                   |
|------|-----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:7 | RESERVED  | R    | 0h    |                                                                                                                                                                                                                                                                                                                               |
| 6    | RETMODE   | R    | 0h    | Retention Mode generic parameter<br>This bit field indicates whether the retention mode is supported using the pin PIRFFRET.<br>0 Retention mode disabled<br>1 Retention mode enabled                                                                                                                                         |
| 5:2  | MEM_SIZE  | R    | 2h    | Memory size for FIFO buffer:<br>1 Memory of 512 bytes, max block length is 512 bytes<br>2 Memory of 1024 bytes, max block length is 1024 bytes<br>4 Memory of 2048 bytes, max block length is 2048 bytes<br>8 Memory of 4096 bytes, max block length is 2048 bytes                                                            |
| 1    | MERGE_MEM | R    | 0h    | Memory merged for FIFO buffer:<br>This register defines the configuration of FIFO buffer architecture. If the bit is set STA and DFT shall support clock multiplexing and balancing.<br>0 2 memories instantiated, one per data transfer direction.<br>1 A single memory is used with multiplexed addresses, data and clocks. |

**Table 5-2575. MMC\_HL\_HWINFO Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                              |
|-----|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | MADMA_EN | R    | 0h    | <p>Master DMA enabled generic parameter:<br/>This register defines the configuration of the controller to know if it supports the master DMA management called ADMA.</p> <p>0        No Master DMA (ADMA) management supported<br/>1        Controller supports ADMA</p> |

### 5.15.2.2 MMC\_HL\_SYSCONFIG Register

#### 1 MMC\_HL\_SYSCONFIG Register (Offset = 10h) [reset = 28h]

Clock Management Configuration Register.

Return to [Summary Table](#)

**Table 5-2576. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCS0         | 4830 0010h       |

**Figure 5-851. MMC\_HL\_SYSCONFIG Name Register**

|          |    |             |    |          |    |         |           |
|----------|----|-------------|----|----------|----|---------|-----------|
| 31       | 30 | 29          | 28 | 27       | 26 | 25      | 24        |
| RESERVED |    |             |    |          |    |         |           |
| R        |    |             |    |          |    |         |           |
| 0h       |    |             |    |          |    |         |           |
| 23       | 22 | 21          | 20 | 19       | 18 | 17      | 16        |
| RESERVED |    |             |    |          |    |         |           |
| R        |    |             |    |          |    |         |           |
| 0h       |    |             |    |          |    |         |           |
| 15       | 14 | 13          | 12 | 11       | 10 | 9       | 8         |
| RESERVED |    |             |    |          |    |         |           |
| R        |    |             |    |          |    |         |           |
| 0h       |    |             |    |          |    |         |           |
| 7        | 6  | 5           | 4  | 3        | 2  | 1       | 0         |
| RESERVED |    | STANDBYMODE |    | IDLEMODE |    | FREEEMU | SOFTRESET |
| R        |    | R/W         |    | R/W      |    | R/W     | R/W       |
| 0h       |    | 2h          |    | 2h       |    | 0h      | 0h        |

**Table 5-2578. MMC\_HL\_SYSCONFIG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------|-------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:6 | RESERVED    | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 5:4  | STANDBYMODE | R/W  | 2h    | <p>Configuration of the local initiator state management mode. By definition, initiator may generate read/write transaction as long as it is out of STANDBY state.</p> <p>0 Force-standby mode: local initiator is unconditionally placed in standby state.Backup mode, for debug only.</p> <p>1 No-standby mode: local initiator is unconditionally placed out of standby state.Backup mode, for debug only.</p> <p>2 Smart-standby mode: local initiator standby status depends on local conditions, i.e. the module's functional requirement from the initiator.IP module shall not generate (initiator-related) wakeup events.</p> <p>3 Smart-Standby wakeup-capable mode: local initiator standby status depends on local conditions, i.e. the module's functional requirement from the initiator. IP module may generate (master-related) wakeup events when in standby state.Mode is only relevant if the appropriate IP module "mwakeup" output is implemented.</p> |

**Table 5-2578. MMC\_HL\_SYSCONFIG Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-----|-----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:2 | IDLEMODE  | R/W  | 2h    | <p>Configuration of the local target state management mode. By definition, target can handle read/write transaction as long as it is out of IDLE state.</p> <p>0 Force-idle mode: local target's idle state follows (acknowledges) the system's idle requests unconditionally, i.e. regardless of the IP module's internal requirements.Backup mode, for debug only.</p> <p>1 No-idle mode: local target never enters idle state.Backup mode, for debug only.</p> <p>2 Smart-idle mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements.IP module shall not generate (IRQ- or DMA-request-related) wakeup events.</p> <p>3 Smart-idle wakeup-capable mode: local target's idle state eventually follows (acknowledges) the system's idle requests, depending on the IP module's internal requirements.IP module may generate (IRQ- or DMA-request-related) wakeup events when in idle state.Mode is only relevant if the appropriate IP module "swakeup" output(s) is (are) implemented.</p> |
| 1   | FREEEMU   | R/W  | 0h    | <p>Sensitivity to emulation [debug] suspend input signal. Functionality NOT implemented in MMCSD.</p> <p>0 IP module is sensitive to emulation suspend</p> <p>1 IP module is not sensitive to emulation suspend</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 0   | SOFTRESET | R/W  | 0h    | <p>Software reset. [Optional]</p> <p>0 No action</p> <p>0 Reset done, no pending action</p> <p>1 Reset (software or other) ongoing</p> <p>1 Initiate software reset</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

### 5.15.2.3 MMC\_SYSSTATUS Register

#### 1 MMC\_SYSSTATUS Register (Offset = 114h) [reset = 0h]

System Status Register

This register provides status information about the module excluding the interrupt status information.

Return to [Summary Table](#)

**Table 5-2579. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCSDB        | 4830 0114h       |

**Figure 5-852. MMC\_SYSSTATUS Name Register**

|          |    |    |    |    |    |    |           |
|----------|----|----|----|----|----|----|-----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24        |
| RESERVED |    |    |    |    |    |    |           |
| R        |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16        |
| RESERVED |    |    |    |    |    |    |           |
| R        |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8         |
| RESERVED |    |    |    |    |    |    |           |
| R        |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0         |
| RESERVED |    |    |    |    |    |    | RESETDONE |
| R        |    |    |    |    |    |    | R         |
| 0h       |    |    |    |    |    |    | 0h        |

**Table 5-2581. MMC\_SYSSTATUS Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                                                           |
|------|-----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED  | R    | 0h    |                                                                                                                                                                                                                                                                       |
| 0    | RESETDONE | R    | 0h    | Internal Reset Monitoring<br>Note: the debounce clock , the system clock [OCP] and the functional clock shall be provided to the MMC/SD/SDIO host controller to allow the internal reset monitoring.<br><br>0 Internal module reset is on-going<br>1 Reset completed. |

### 5.15.2.4 MMC\_CSRE Register

#### 1 MMC\_CSRE Register (Offset = 124h) [reset = 0h]

##### Card Status Response Error

This register enables the host controller to detect card status errors of response type R1, R1b for all cards and of R5, R5b and R6 response for cards types SD or SDIO.

When a bit MMCHS\_CSRE[i] is set to 1, if the corresponding bit at the same position in the response MMCHS\_RSP0[i] is set to 1, the host controller indicates a card error (MMCHS\_STAT[CERR]) interrupt status to avoid the host driver reading the response register (MMCHS\_RSP0).

Note: No automatic card error detection for autoCMD12 is implemented; the host system has to check autoCMD12 response register (MMCHS\_RESP76) for possible card errors.

Return to [Summary Table](#)

**Table 5-2582. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCS0         | 4830 0124h       |

**Figure 5-853. MMC\_CSRE Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CSRE |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CSRE |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CSRE |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CSRE |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-2584. MMC\_CSRE Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                |
|------|-------|------|-------|----------------------------|
| 31:0 | CSRE  | R/W  | 0h    | Card status response error |



### 5.15.2.5 MMC\_SYSTEST Register

#### 1 MMC\_SYSTEST Register (Offset = 128h) [reset = 0h]

##### System Test Register

This register is used to control the signals that connect to I/O pins when the module is configured in system test (SYSTEST) mode for boundary connectivity verification.

Note: In SYSTEST mode, a write into MMCHS\_CMD register will not start a transfer. The buffer behaves as a stack accessible only by the local host (push and pop operations). In this mode, the Transfer Block Size (MMCHS\_BLK[BLLEN]) and the Blocks count for current transfer (MMCHS\_BLK[NBLK]) are needed to generate a Buffer write ready interrupt (MMCHS\_STAT[BWR]) or a Buffer read ready interrupt (MMCHS\_STAT[BRR]) and DMA requests if enabled.

Return to [Summary Table](#)

**Table 5-2585. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCSD0        | 4830 0128h       |

**Figure 5-854. MMC\_SYSTEST Name Register**

|          |      |      |     |      |      |      |      |
|----------|------|------|-----|------|------|------|------|
| 31       | 30   | 29   | 28  | 27   | 26   | 25   | 24   |
| RESERVED |      |      |     |      |      |      |      |
| R        |      |      |     |      |      |      |      |
| 0h       |      |      |     |      |      |      |      |
| 23       | 22   | 21   | 20  | 19   | 18   | 17   | 16   |
| RESERVED |      |      |     |      |      |      | OBI  |
| R        |      |      |     |      |      |      | R    |
| 0h       |      |      |     |      |      |      | 0h   |
| 15       | 14   | 13   | 12  | 11   | 10   | 9    | 8    |
| SDCD     | SDWP | WAKD | SSB | D7D  | D6D  | D5D  | D4D  |
| R        | R    | R/W  | R/W | R/W  | R/W  | R/W  | R/W  |
| 0h       | 0h   | 0h   | 0h  | 0h   | 0h   | 0h   | 0h   |
| 7        | 6    | 5    | 4   | 3    | 2    | 1    | 0    |
| D3D      | D2D  | D1D  | D0D | DDIR | CDAT | CDIR | MCKD |
| R/W      | R/W  | R/W  | R/W | R/W  | R/W  | R/W  | R/W  |
| 0h       | 0h   | 0h   | 0h  | 0h   | 0h   | 0h   | 0h   |

**Table 5-2587. MMC\_SYSTEST Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                 |
|-------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:17 | RESERVED | R    | 0h    |                                                                                                                                             |
| 16    | OBI      | R    | 0h    | Out-Of-Band Interrupt [OBI] data value<br>0 The Out-of-Band Interrupt pin is driven low.<br>1 The Out-of-Band Interrupt pin is driven high. |
| 15    | SDCD     | R    | 0h    | Card detect input signal [SDCD] data value<br>0 The card detect pin is driven low.<br>1 The card detect pin is driven high.                 |
| 14    | SDWP     | R    | 0h    | Write protect input signal [SDWP] data value<br>0 The write protect pin SDWP is driven low.<br>1 The write protect pin SDWP is driven high. |

**Table 5-2587. MMC\_SYSTEST Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-----|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 13  | WAKD  | R/W  | 0h    | Wake request output signal data value<br>0 The pin SWAKEUP is driven low.<br>0 No action. Returns 0.<br>1 The pin SWAKEUP is driven high.<br>1 No action. Returns 1.                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 12  | SSB   | R/W  | 0h    | Set status bit<br>This bit must be cleared prior attempting to clear a status bit of the interrupt status register [MMCSD_STAT].<br>0 Clear this SSB bitfield. writing 0 does not clear already set status bits;<br>0 No action. Returns 0.<br>1 No action. Returns 1.<br>1 Force to 1 all status bits of the interrupt status register (MMCHS_STAT) only if the corresponding bitfield in the Interrupt signal enable register (MMCHS_ISE) is set.                                                                                                                                                                          |
| 11  | D7D   | R/W  | 0h    | DAT7 input/output signal data value<br>0 If SYSTEST[DDIR] = 0 (output mode direction), the DAT7 line is driven low. If SYSTEST[DDIR] = 1 (input mode direction), no effect.<br>0 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT7 line (low). If SYSTEST[DDIR] = 0 (output mode direction), returns 0<br>1 If SYSTEST[DDIR] = 0 (output mode direction), the DAT7 line is driven high. If SYSTEST[DDIR] = 1 (input mode direction), no effect.<br>1 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT7 line (high) If SYSTEST[DDIR] = 0 (output mode direction), returns 1 |
| 10  | D6D   | R/W  | 0h    | DAT6 input/output signal data value<br>0 If SYSTEST[DDIR] = 0 (output mode direction), the DAT6 line is driven low. If SYSTEST[DDIR] = 1 (input mode direction), no effect.<br>0 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT6 line (low). If SYSTEST[DDIR] = 0 (output mode direction), returns 0<br>1 If SYSTEST[DDIR] = 0 (output mode direction), the DAT6 line is driven high. If SYSTEST[DDIR] = 1 (input mode direction), no effect.<br>1 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT6 line (high) If SYSTEST[DDIR] = 0 (output mode direction), returns 1 |

**Table 5-2587. MMC\_SYSTEST Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9   | D5D   | R/W  | 0h    | <p>DAT5 input/output signal data value</p> <p>0 If SYSTEST[DDIR] = 0 (output mode direction), the DAT5 line is driven low. If SYSTEST[DDIR] = 1 (input mode direction), no effect.</p> <p>0 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT5 line (low). If SYSTEST[DDIR] = 0 (output mode direction), returns 0</p> <p>1 If SYSTEST[DDIR] = 0 (output mode direction), the DAT5 line is driven high. If SYSTEST[DDIR] = 1 (input mode direction), no effect.</p> <p>1 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT5 line (high) If SYSTEST[DDIR] = 0 (output mode direction), returns 1</p> |
| 8   | D4D   | R/W  | 0h    | <p>DAT4 input/output signal data value</p> <p>0 If SYSTEST[DDIR] = 0 (output mode direction), the DAT4 line is driven low. If SYSTEST[DDIR] = 1 (input mode direction), no effect.</p> <p>0 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT4 line (low). If SYSTEST[DDIR] = 0 (output mode direction), returns 0</p> <p>1 If SYSTEST[DDIR] = 0 (output mode direction), the DAT4 line is driven high. If SYSTEST[DDIR] = 1 (input mode direction), no effect.</p> <p>1 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT4 line (high) If SYSTEST[DDIR] = 0 (output mode direction), returns 1</p> |
| 7   | D3D   | R/W  | 0h    | <p>DAT3 input/output signal data value</p> <p>0 If SYSTEST[DDIR] = 0 (output mode direction), the DAT3 line is driven low. If SYSTEST[DDIR] = 1 (input mode direction), no effect.</p> <p>0 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT3 line (low). If SYSTEST[DDIR] = 0 (output mode direction), returns 0</p> <p>1 If SYSTEST[DDIR] = 0 (output mode direction), the DAT3 line is driven high. If SYSTEST[DDIR] = 1 (input mode direction), no effect.</p> <p>1 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT3 line (high) If SYSTEST[DDIR] = 0 (output mode direction), returns 1</p> |
| 6   | D2D   | R/W  | 0h    | <p>DAT2 input/output signal data value</p> <p>0 If SYSTEST[DDIR] = 0 (output mode direction), the DAT2 line is driven low. If SYSTEST[DDIR] = 1 (input mode direction), no effect.</p> <p>0 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT2 line (low). If SYSTEST[DDIR] = 0 (output mode direction), returns 0</p> <p>1 If SYSTEST[DDIR] = 0 (output mode direction), the DAT2 line is driven high. If SYSTEST[DDIR] = 1 (input mode direction), no effect.</p> <p>1 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT2 line (high) If SYSTEST[DDIR] = 0 (output mode direction), returns 1</p> |

**Table 5-2587. MMC\_SYSTEST Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | D1D   | R/W  | 0h    | <p>DAT1 input/output signal data value</p> <p>0 If SYSTEST[DDIR] = 0 (output mode direction), the DAT1 line is driven low. If SYSTEST[DDIR] = 1 (input mode direction), no effect.</p> <p>0 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT1 line (low). If SYSTEST[DDIR] = 0 (output mode direction), returns 0</p> <p>1 If SYSTEST[DDIR] = 0 (output mode direction), the DAT1 line is driven high. If SYSTEST[DDIR] = 1 (input mode direction), no effect.</p> <p>1 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT1 line (high) If SYSTEST[DDIR] = 0 (output mode direction), returns 1</p> |
| 4   | D0D   | R/W  | 0h    | <p>DAT0 input/output signal data value</p> <p>0 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT0 line (low). If SYSTEST[DDIR] = 0 (output mode direction), returns 0</p> <p>0 If SYSTEST[DDIR] = 0 (output mode direction), the DAT0 line is driven low. If SYSTEST[DDIR] = 1 (input mode direction), no effect.</p> <p>1 If SYSTEST[DDIR] = 0 (output mode direction), the DAT0 line is driven high. If SYSTEST[DDIR] = 1 (input mode direction), no effect.</p> <p>1 If SYSTEST[DDIR] = 1 (input mode direction), returns the value on the DAT0 line (high) If SYSTEST[DDIR] = 0 (output mode direction), returns 1</p> |
| 3   | DDIR  | R/W  | 0h    | <p>Control of the DAT[7:0] pins direction.</p> <p>0 The DAT lines are outputs (host to card)</p> <p>0 No action. Returns 0.</p> <p>1 The DAT lines are inputs (card to host)</p> <p>1 No action. Returns 1.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 2   | CDAT  | R/W  | 0h    | <p>CMD input/output signal data value</p> <p>0 If SYSTEST[CDIR] = 0 (output mode direction), the CMD line is driven low. If SYSTEST[CDIR] = 1 (input mode direction), no effect.</p> <p>0 If SYSTEST[CDIR] = 1 (input mode direction), returns the value on the CMD line (low). If SYSTEST[CDIR] = 0 (output mode direction), returns 0</p> <p>1 If SYSTEST[CDIR] = 0 (output mode direction), the CMD line is driven high. If SYSTEST[CDIR] = 1 (input mode direction), no effect.</p> <p>1 If SYSTEST[CDIR] = 1 (input mode direction), returns the value on the CMD line (high) If SYSTEST[CDIR] = 0 (output mode direction), returns 1</p>      |
| 1   | CDIR  | R/W  | 0h    | <p>Control of the CMD pin direction.</p> <p>0 The CMD line is an output (host to card)</p> <p>0 No action. Returns 0.</p> <p>1 The CMD line is an input (card to host)</p> <p>1 No action. Returns 1.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                           |

**Table 5-2587. MMC\_SYSTEST Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                             |
|-----|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | MCKD  | R/W  | 0h    | MMC clock output signal data value<br>0      The output clock is driven low.<br>0      No action. Returns 0.<br>1      The output clock is driven high.<br>1      No action. Returns 1. |

### 5.15.2.6 MMC\_CON Register

#### 1 MMC\_CON Register (Offset = 12Ch) [reset = 600h]

Configuration Register

This register is used:

- to select the functional mode or the SYSTEST mode for any card.
  - to send an initialization sequence to any card.
  - to enable the detection on DAT[1] of a card interrupt for SDIO cards only.
- and also to configure :
- specific data and command transfers for MMC cards only.
  - the parameters related to the card detect and write protect input signals.

Return to [Summary Table](#)

**Table 5-2588. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCSDB        | 4830 012Ch       |

**Figure 5-855. MMC\_CON Name Register**

|          |      |          |         |      |          |          |            |
|----------|------|----------|---------|------|----------|----------|------------|
| 31       | 30   | 29       | 28      | 27   | 26       | 25       | 24         |
| RESERVED |      |          |         |      |          |          |            |
| R        |      |          |         |      |          |          |            |
| 0h       |      |          |         |      |          |          |            |
| 23       | 22   | 21       | 20      | 19   | 18       | 17       | 16         |
| RESERVED |      | SDMA_LNE | DMA_MNS | DDR  | BOOT_CF0 | BOOT_ACK | CLKEXTFREE |
| R        |      | R/W      | R/W     | R/W  | R/W      | R/W      | R/W        |
| 0h       |      | 0h       | 0h      | 0h   | 0h       | 0h       | 0h         |
| 15       | 14   | 13       | 12      | 11   | 10       | 9        | 8          |
| PADEN    | OBIE | OBIP     | CEATA   | CTPL | DVAL     |          | WPP        |
| R/W      | R/W  | R/W      | R/W     | R/W  | R/W      |          | R/W        |
| 0h       | 0h   | 0h       | 0h      | 0h   | 3h       |          | 0h         |
| 7        | 6    | 5        | 4       | 3    | 2        | 1        | 0          |
| CDP      | MIT  | DW8      | MODE    | STR  | HR       | INIT     | OD         |
| R/W      | R/W  | R/W      | R/W     | R/W  | R/W      | R/W      | R/W        |
| 0h       | 0h   | 0h       | 0h      | 0h   | 0h       | 0h       | 0h         |

**Table 5-2590. MMC\_CON Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:22 | RESERVED | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                        |
| 21    | SDMA_LNE | R/W  | 0h    | <p>Slave DMA Level/Edge Request:</p> <p>The waveform of the DMA request can be configured either edge sensitive with early de-assertion on first access to MMCSDB_DATA register or late de-assertion, request remains active until last allowed data written into MMCSDB_DATA.</p> <p>0 Slave DMA edge sensitive, Early DMA de-assertion</p> <p>1 Slave DMA level sensitive, Late DMA de-assertion</p> |

**Table 5-2590. MMC\_CON Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-----|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 20  | DMA_MNS    | R/W  | 0h    | <p>DMA Master or Slave selection:</p> <p>When this bit is set and the controller is configured to use the DMA, Ocp master interface is used to get datas from system using ADMA2 procedure [direct access to the memory]. This option is only available if generic parameter MADMA_EN is asserted to '1'.</p> <p>0      The controller is slave on data transfers with system.</p> <p>1      The controller is master on data exchange with system, controller must be configured as using DMA.</p>                                                                                                                               |
| 19  | DDR        | R/W  | 0h    | <p>Dual Data Rate mode:</p> <p>When this register is set, the controller uses both clock edge to emit or receive data. Odd bytes are transmitted on falling edges and even bytes are transmitted on rise edges. It only applies on Data bytes and CRC, Start, end bits and CRC status are kept full cycle. This bit field is only meaningful and active for even clock divider ratio of MMCSD_SYSCTL[CLKD], it is insensitive to MMCSD_HCTL[HSPE] setting.</p> <p>0      Standard mode : data are transmitted on a single edge depending on MMCHS_HCTRL[HSPE].</p> <p>1      Data Bytes and CRC are transmitted on both edge.</p> |
| 18  | BOOT_CF0   | R/W  | 0h    | <p>Boot status supported:</p> <p>This register is set when the CMD line need to be forced to '0' for a boot sequence. CMD line is driven to '0' after Writing in MMCSD_CMD. The line is released when this bit field is de-asserted and abort data transfer in case of a pending transaction.</p> <p>0      CMD line is released when it was previously forced to '0' by a boot sequence.</p> <p>0      CMD line not forced</p> <p>1      CMD line forced to '0' is enabled and will be active after writing into MMCHS_CMD</p> <p>1      CMD line forced to '0' is enabled</p>                                                   |
| 17  | BOOT_ACK   | R/W  | 0h    | <p>Book acknowledge received:</p> <p>When this bit is set the controller should receive a boot status on DAT0 line after next command issued. If no status is received a data timeout will be generated.</p> <p>0      No acknowledge to be received</p> <p>1      A boot status will be received on DAT0 line after issuing a command.</p>                                                                                                                                                                                                                                                                                       |
| 16  | CLKEXTFREE | R/W  | 0h    | <p>External clock free running:</p> <p>This register is used to maintain card clock out of transfer transaction to enable slave module for example to generate a synchronous interrupt on DAT[1]. The Clock will be maintain only if MMCSD_SYSCTL[CEN] is set.</p> <p>0      External card clock is cut off outside active transaction period.</p> <p>1      External card clock is maintain even out of active transaction period only if MMCHS_SYSCTL[CEN] is set.</p>                                                                                                                                                          |
| 15  | PADEN      | R/W  | 0h    | <p>Control Power for MMC Lines:</p> <p>This register is only useful when MMC PADs contain power saving mechanism to minimize its leakage power. It works as a GPIO that directly control the ACTIVE pin of PADs. Excepted for DAT[1], the signal is also combine outside the module with the dedicated power control MMCSD_CON[CTPL] bit.</p> <p>0      ADPIDLE module pin is not forced, it is automatically generated by the MMC fsms.</p> <p>1      ADPIDLE module pin is forced to active state.</p>                                                                                                                          |

**Table 5-2590. MMC\_CON Register Field Descriptions (continued)**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 14   | OBIE  | R/W  | 0h    | <p>Out-of-Band Interrupt Enable</p> <p>MMC cards only:</p> <p>This bit enables the detection of Out-of-Band Interrupt on MMC_OBI input pin.</p> <p>The usage of the Out-of-Band signal [OBI] is optional and depends on the system integration.</p> <p>0 Out-of-Band interrupt detection disabled</p> <p>1 Out-of-Band interrupt detection enabled</p>                                                                                                                                                                                                                                                                                                                                       |
| 13   | OBIP  | R/W  | 0h    | <p>Out-of-Band Interrupt Polarity</p> <p>MMC cards only:</p> <p>This bit selects the active level of the out-of-band interrupt coming from MMC cards.</p> <p>The usage of the Out-of-Band signal [OBI] is optional and depends on the system integration.</p> <p>0 Active high level</p> <p>1 Active low level</p>                                                                                                                                                                                                                                                                                                                                                                           |
| 12   | CEATA | R/W  | 0h    | <p>CE-ATA control mode</p> <p>MMC cards compliant with CE-ATA: By default, this bit is set to 0. It is use to indicate that next commands are considered as specific CE-ATA commands that potentially use 'command completion' features.</p> <p>0 Standard MMC/SD/SDIO mode.</p> <p>1 CE-ATA mode next commands are considered as CE-ATA commands.</p>                                                                                                                                                                                                                                                                                                                                       |
| 11   | CTPL  | R/W  | 0h    | <p>Control Power for DAT[1] line</p> <p>MMC and SD cards:</p> <p>By default, this bit is set to 0 and the host controller automatically disables all the input buffers outside of a transaction to minimize the leakage current.</p> <p>SDIO cards:</p> <p>When this bit is set to 1, the host controller automatically disables all the input buffers except the buffer of DAT[1] outside of a transaction in order to detect asynchronous card interrupt on DAT[1] line and minimize the leakage current of the buffers.</p> <p>0 Disable all the input buffers outside of a transaction.</p> <p>1 Disable all the input buffers except the buffer of DAT[1] outside of a transaction.</p> |
| 10:9 | DVAL  | R/W  | 3h    | <p>Debounce filter value</p> <p>All cards</p> <p>This register is used to define a debounce period to filter the card detect input signal [SDCD].</p> <p>The usage of the card detect input signal [SDCD] is optional and depends on the system integration and the type of the connector housing that accommodates the card.</p> <p>0 33 us debounce period</p> <p>1 231 us debounce period</p> <p>2 1 ms debounce period</p> <p>3 8,4 ms debounce period</p>                                                                                                                                                                                                                               |
| 8    | WPP   | R/W  | 0h    | <p>Write protect polarity</p> <p>For SD and SDIO cards only</p> <p>This bit selects the active level of the write protect input signal [SDWP].</p> <p>The usage of the write protect input signal [SDWP] is optional and depends on the system integration and the type of the connector housing that accommodates the card.</p> <p>0 Active high level</p> <p>1 Active low level</p>                                                                                                                                                                                                                                                                                                        |



**Table 5-2590. MMC\_CON Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-----|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | CDP   | R/W  | 0h    | <p>Card detect polarity<br/>All cards<br/>This bit selects the active level of the card detect input signal [SDCD].<br/>The usage of the card detect input signal [SDCD] is optional and depends on the system integration and the type of the connector housing that accommodates the card.</p> <p>0      Active low level<br/>1      Active high level</p>                                                                                                                                                                                                                                                                  |
| 6   | MIT   | R/W  | 0h    | <p>MMC interrupt command<br/>Only for MMC cards.<br/>This bit must be set to 1, when the next write access to the command register [MMCSD_CMD] is for Writing a MMC interrupt command [CMD40] requiring the command timeout detection to be disabled for the command response.</p> <p>0      Command timeout enabled<br/>1      Command timeout disabled</p>                                                                                                                                                                                                                                                                  |
| 5   | DW8   | R/W  | 0h    | <p>8-bit mode MMC select<br/>For SD/SDIO cards, this bit must be set to 0.<br/>For MMC card,<br/>this bit must be set following a valid SWITCH command [CMD6] with the correct value and extend CSD index written in the argument.<br/>Prior to this command, the MMC card configuration register [CSD and EXT_CSD] must be verified for compliancy with MMC standard specification 4.x [see section 3.6].</p> <p>0      1-bit or 4-bit Data width (DAT[0] used, MMC, SD cards)<br/>1      8-bit Data width (DAT[7:0] used, MMC cards)</p>                                                                                    |
| 4   | MODE  | R/W  | 0h    | <p>Mode select<br/>All cards<br/>These bits select between Functional mode and SYSTEST mode.</p> <p>0      Functional mode. Transfers to the MMC/SD/SDIO cards follow the card protocol. MMC clock is enabled. MMC/SD transfers are operated under the control of the CMD register.</p> <p>1      SYSTEST mode The signal pins are configured as general-purpose input/output and the 1024-byte buffer is configured as a stack memory accessible only by the local host or system DMA. The pins retain their default type (input, output or in-out). SYSTEST mode is operated under the control of the SYSTEST register.</p> |
| 3   | STR   | R/W  | 0h    | <p>Stream command<br/>Only for MMC cards.<br/>This bit must be set to 1 only for the stream data transfers [read or write] of the adtc commands.<br/>Stream read is a class 1 command [CMD11: READ_DAT_UNTIL_STOP].<br/>Stream write is a class 3 command [CMD20: WRITE_DAT_UNTIL_STOP].</p> <p>0      Block oriented data transfer<br/>1      Stream oriented data transfer</p>                                                                                                                                                                                                                                              |

**Table 5-2590. MMC\_CON Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | HR    | R/W  | 0h    | <p>Broadcast host response<br/>Only for MMC cards.<br/>This register is used to force the host to generate a 48-bit response for bc command type.<br/>It can be used to terminate the interrupt mode by generating a CMD40 response by the core [see section 4.3, "Interrupt Mode", in the MMC [1] specification]. In order to have the host response to be generated in open drain mode, the register MMCSD_CON[OD] must be set to 1.<br/>When MMCSD_CON[CEATA] is set to 1 and MMCSD_ARG set to 0x00000000 when Writing 0x00000000 into MMCSD_CMD register, the host controller performs a 'command completion signal disable' token i.e. CMD line held to '0' during 47 cycles followed by a 1.</p> <p>0      The host does not generate a 48-bit response instead of a command.<br/>1      The host generates a 48-bit response instead of a command or a command completion signal disable token.</p> |
| 1   | INIT  | R/W  | 0h    | <p>Send initialization stream<br/>All cards.<br/>When this bit is set to 1, and the card is idle, an initialization sequence is sent to the card.<br/>An initialization sequence consists of setting the CMD line to 1 during 80 clock cycles. The initialization sequence is mandatory - but it is not required to do it through this bit - this bit makes it easier. Clock divider [MMCSD_SYSCCTL[CLKD]] should be set to ensure that 80 clock periods are greater than 1ms. [see section 9.3, "Power-Up", in the MMC card specification [1], or section 6.4 in the SD card specification [2]].<br/>Note: in this mode, there is no command sent to the card and no response is expected</p> <p>0      The host does not send an initialization sequence.<br/>1      The host sends an initialization sequence.</p>                                                                                      |
| 0   | OD    | R/W  | 0h    | <p>Card open drain mode.<br/>Only for MMC cards.<br/>This bit must be set to 1 for MMC card commands 1, 2, 3 and 40, and if the MMC card bus is operating in open-drain mode during the response phase to the command sent. Typically, during card identification mode when the card is either in idle, ready or ident state.<br/>It is also necessary to set this bit to 1, for a broadcast host response [see Broadcast host response register MMCSD_CON[HR]]</p> <p>0      No Open Drain<br/>1      Open Drain or Broadcast host response</p>                                                                                                                                                                                                                                                                                                                                                           |

### 5.15.2.7 MMC\_PWCNT Register

#### 1 MMC\_PWCNT Register (Offset = 130h) [reset = 0h]

Power Counter Register

This register is used to program a mmc counter to delay command transfers after activating the PAD power, this value depends on PAD characteristics and voltage.

Return to [Summary Table](#)

**Table 5-2591. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCS0         | 4830 0130h       |

**Figure 5-856. MMC\_PWCNT Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| PWCNT    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| PWCNT    |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2593. MMC\_PWCNT Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                               |
|-------|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED | R    | 0h    |                                                                                                                                                                                                                                                                                                                                           |
| 15:0  | PWCNT    | R/W  | 0h    | Power counter register.<br>This register is used to introduce a delay between the PAD ACTIVE pin assertion and the command issued.<br>0 No additional delay added<br>1 TCF delay (card clock period)<br>2 TCF x 2 delay (card clock period)<br>65534 TCF x 65534 delay (card clock period)<br>65535 TCF x 65535 delay (card clock period) |

### 5.15.2.8 MMC\_DLL Register

#### 1 MMC\_DLL Register (Offset = 134h) [reset = 80000000h]

DLL control and status register

This register is used for tuning procedure required for SDR104 speed mode.

It gives visibility and control on the DLL.

Return to [Summary Table](#)

**Table 5-2594. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCS0         | 4830 0134h       |

**Figure 5-857. MMC\_DLL Name Register**

| 31                 | 30         | 29            | 28              | 27                   | 26                    | 25        | 24       |
|--------------------|------------|---------------|-----------------|----------------------|-----------------------|-----------|----------|
| DLL_SOFT_RE<br>SET | LOCK_TIMER | MAX_LOCK_DIFF |                 |                      |                       |           |          |
| R/W                | R/W        | R/W           |                 |                      |                       |           |          |
| 1h                 | 0h         | 0h            |                 |                      |                       |           |          |
| 23                 | 22         | 21            | 20              | 19                   | 18                    | 17        | 16       |
| MAX_LOCK_DIFF      |            | FORCE_SR_F    |                 | FORCE_SR_C           |                       |           |          |
| R/W                |            | R/W           |                 | R/W                  |                       |           |          |
| 0h                 |            | 0h            |                 | 0h                   |                       |           |          |
| 15                 | 14         | 13            | 12              | 11                   | 10                    | 9         | 8        |
| FORCE_SR_C         |            |               | FORCE_VALU<br>E | SLAVE_RATIO          |                       |           |          |
| R/W                |            |               | R/W             | R/W                  |                       |           |          |
| 0h                 |            |               | 0h              | 0h                   |                       |           |          |
| 7                  | 6          | 5             | 4               | 3                    | 2                     | 1         | 0        |
| SLAVE_RATIO        |            | RESERVED      |                 | DLL_UNLOCK_<br>CLEAR | DLL_UNLOCK_<br>STICKY | DLL_CALIB | DLL_LOCK |
| R/W                |            | R             |                 | R/W                  | R                     | R/W       | R        |
| 0h                 |            | 0h            |                 | 0h                   | 0h                    | 0h        | 0h       |

**Table 5-2596. MMC\_DLL Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description                                                                                                                       |
|-------|----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------|
| 31    | DLL_SOFT_RESET | R/W  | 1h    | Soft reset for DLL, active HIGH.<br>0 Reset completed.<br>0 No action.<br>1 Reset is in progress<br>1 Issue soft reset            |
| 30    | LOCK_TIMER     | R/W  | 0h    | Timer for the dll_lock signal to be asserted after reset.<br>0 1024 cycles (equivalent to DLL fast mode lock)<br>1 66560 cycles   |
| 29:22 | MAX_LOCK_DIFF  | R/W  | 0h    | Maximum number of taps that the master DLLs clock period measurement can deviate without resulting in the master DLL losing lock. |
| 21:20 | FORCE_SR_F     | R/W  | 0h    | Forced fine delay value.                                                                                                          |
| 19:13 | FORCE_SR_C     | R/W  | 0h    | Forced coarse delay value                                                                                                         |

**Table 5-2596. MMC\_DLL Register Field Descriptions (continued)**

| Bit  | Field             | Type | Reset | Description                                                                                                                                                                                                                                                                                                                       |
|------|-------------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12   | FORCE_VALUE       | R/W  | 0h    | Put forced values to slave DLL, ignoring master DLL output and ratio value.<br>0 Do not put force value<br>1 Put force value.                                                                                                                                                                                                     |
| 11:6 | SLAVE_RATIO       | R/W  | 0h    | Fraction of a clock cycle for the shift to be implemented, in units of 256ths of a clock cycle.<br>0 0 degree delay<br>2 45 degrees delay<br>4 90 degrees delay<br>6 135 degrees delay<br>8 180 degrees delay<br>10 225 degrees delay<br>12 270 degrees delay<br>14 315 degrees delay<br>16 Full clock delay<br>63 4 clocks delay |
| 5:4  | RESERVED          | R    | 0h    |                                                                                                                                                                                                                                                                                                                                   |
| 3    | DLL_UNLOCK_CLEAR  | R/W  | 0h    | Clears the phy_reg_status_mdll_unlock_sticky flags of the DLL.<br>0 No effect.<br>1 Clears the flag.                                                                                                                                                                                                                              |
| 2    | DLL_UNLOCK_STICKY | R    | 0h    | Asserted when any single period measurement exceeds MAX_LOCK_DIFF.                                                                                                                                                                                                                                                                |
| 1    | DLL_CALIB         | R/W  | 0h    | Enables Slave DLL to update new delay values.<br>0 Disabled<br>1 Enabled                                                                                                                                                                                                                                                          |
| 0    | DLL_LOCK          | R    | 0h    | Master DLL lock status.<br>0 DLL is not locked<br>1 DLL is locked                                                                                                                                                                                                                                                                 |

### 5.15.2.9 MMC\_SDMA\_SA Register

#### 1 MMC\_SDMA\_SA Register (Offset = 200h) [reset = 0h]

SDMA System Address / Argument 2 Register.

Return to [Summary Table](#)

**Table 5-2597. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCSD0        | 4830 0200h       |

**Figure 5-858. MMC\_SDMA\_SA Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| SDMA_ARG2 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| SDMA_ARG2 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| SDMA_ARG2 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SDMA_ARG2 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 5-2599. MMC\_SDMA\_SA Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | SDMA_ARG2 | R/W  | 0h    | <p>SDMA System Address / Argument 2</p> <p>This register contains the physical system memory address used for DMA transfers or the second argument for the Auto CMD23.</p> <p>[1] SDMA System Address</p> <p>This register contains the system memory address for a SDMA transfer. When the Host Controller stops a SDMA transfer, this register shall point to the system address of the next contiguous data position. It can be accessed only if no transaction is executing [i.e., after a transaction has stopped]. Read operations during transfers may return an invalid value.</p> <p>The Host Driver shall initialize this register before starting a SDMA transaction. After SDMA has stopped, the next system address of the next contiguous data position can be read from this register. The SDMA transfer waits at the every boundary specified by the Host SDMA Buffer Boundary in the Block Size register. The Host Controller generates DMA Interrupt to request the Host Driver to update this register. The Host Driver sets the next system address of the next data position to this register. When the most upper byte of this register</p> <p>003h is written, the Host Controller restarts the SDMA transfer. When restarting SDMA by the Resume command or by setting Continue Request in the Block Gap Control register, the Host Controller shall start at the next contiguous address stored here in the SDMA System Address register.</p> <p>ADMA does not use this register.</p> <p>[2] Argument 2</p> <p>This register is used with the Auto CMD23 to set a 32-bit block count value to the argument of the CMD23 while executing Auto CMD23. If Auto CMD23 is used with ADMA, the full 32-bit block count value can be used. If Auto CMD23 is used without ADMA, the available block count value is limited by the Block Count register. 65535 blocks is the maximum value in this case.</p> |

### 5.15.2.10 MMC\_BLK Register

#### 1 MMC\_BLK Register (Offset = 204h) [reset = 0h]

Transfer Length Configuration Register

MMCHS\_BLK[BLK] is the block size register.

MMCHS\_BLK[NBLK] is the block count register.

This register shall be used for any card.

Return to [Summary Table](#)

**Table 5-2600. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCSD0        | 4830 0204h       |

**Figure 5-859. MMC\_BLK Name Register**

|          |    |    |    |     |    |    |    |
|----------|----|----|----|-----|----|----|----|
| 31       | 30 | 29 | 28 | 27  | 26 | 25 | 24 |
| NBLK     |    |    |    |     |    |    |    |
| R/W      |    |    |    |     |    |    |    |
| 0h       |    |    |    |     |    |    |    |
| 23       | 22 | 21 | 20 | 19  | 18 | 17 | 16 |
| NBLK     |    |    |    |     |    |    |    |
| R/W      |    |    |    |     |    |    |    |
| 0h       |    |    |    |     |    |    |    |
| 15       | 14 | 13 | 12 | 11  | 10 | 9  | 8  |
| RESERVED |    |    |    | BLK |    |    |    |
| R        |    |    |    | R/W |    |    |    |
| 0h       |    |    |    | 0h  |    |    |    |
| 7        | 6  | 5  | 4  | 3   | 2  | 1  | 0  |
| BLK      |    |    |    |     |    |    |    |
| R/W      |    |    |    |     |    |    |    |
| 0h       |    |    |    |     |    |    |    |

**Table 5-2602. MMC\_BLK Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | NBLK     | R/W  | 0h    | <p>Blocks count for current transfer</p> <p>This register is enabled when Block count Enable [MMCSD_CMD[BCE]] is set to 1 and is valid only for multiple block transfers. Setting the block count to 0 results no data blocks being transferred.</p> <p>Note: The host controller decrements the block count after each block transfer and stops when the count reaches zero.</p> <p>This register can be accessed only if no transaction is executing [i.e., after a transaction has stopped]. Read operations during transfers may return an invalid value and write operation will be ignored.</p> <p>In suspend context, the number of blocks yet to be transferred can be determined by Reading this register. When restoring transfer context prior to issuing a Resume command, The local host shall restore the previously saved block count.</p> <p>0      Stop count<br/>1      1 block<br/>2      2 blocks<br/>65535 65535 blocks</p> |
| 15:12 | RESERVED | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |



**Table 5-2602. MMC\_BLK Register Field Descriptions (continued)**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11:0 | BLEN  | R/W  | 0h    | <p>Transfer Block Size.</p> <p>This register specifies the block size for block data transfers. Read operations during transfers may return an invalid value, and write operations are ignored.</p> <p>When a CMD12 command is issued to stop the transfer, a read of the BLEN field after transfer completion [MMCSD_STAT[TC] set to 1] will not return the true byte number of data length while the stop occurs but the value written in this register before transfer is launched.</p> <p>0      No data transfer<br/> 1      1 byte block length<br/> 2      2 bytes block length<br/> 3      3 bytes block length<br/> 511    511 bytes block length<br/> 512    512 bytes block length<br/> 2047   2047 bytes block length<br/> 2048   2048 bytes block length</p> |

### 5.15.2.11 MMC\_ARG Register

#### 1 MMC\_ARG Register (Offset = 208h) [reset = 0h]

Command Argument Register

This register contains command argument specified as bit 39-8 of Command-Format

These registers must be initialized prior to sending the command itself to the card (write action into the register MMCHS\_CMD register). Only exception is for a command index specifying stuff bits in arguments, making a write unnecessary.

Return to [Summary Table](#)

**Table 5-2603. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCSD0        | 4830 0208h       |

**Figure 5-860. MMC\_ARG Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ARG |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ARG |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ARG |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ARG |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 5-2605. MMC\_ARG Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                  |
|------|-------|------|-------|------------------------------|
| 31:0 | ARG   | R/W  | 0h    | Command argument bits [31:0] |

### 5.15.2.12 MMC\_CMD Register

#### 1 MMC\_CMD Register (Offset = 20Ch) [reset = 0h]

Command and Transfer Mode Register

MMCHS\_CMD[31:16] = the command register

MMCHS\_CMD[15:0] = the transfer mode.

This register configures the data and command transfers. A write into the most significant byte send the command. A write into MMCHS\_CMD[15:0] registers during data transfer has no effect.

This register shall be used for any card.

Note: In SYSTEST mode, a write into MMCHS\_CMD register will not start a transfer.

Return to [Summary Table](#)

**Table 5-2606. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCS0         | 4830 020Ch       |

**Figure 5-861. MMC\_CMD Name Register**

| 31        | 30 | 29   | 28   | 27   | 26        | 25       | 24  |
|-----------|----|------|------|------|-----------|----------|-----|
| RESERVED2 |    | INDX |      |      |           |          |     |
| R         |    | R/W  |      |      |           |          |     |
| 0h        |    | 0h   |      |      |           |          |     |
| 23        | 22 | 21   | 20   | 19   | 18        | 17       | 16  |
| CMD_TYPE  |    | DP   | CICE | CCCE | RESERVED1 | RSP_TYPE |     |
| R/W       |    | R/W  | R/W  | R/W  | R         | R/W      |     |
| 0h        |    | 0h   | 0h   | 0h   | 0h        | 0h       |     |
| 15        | 14 | 13   | 12   | 11   | 10        | 9        | 8   |
| RESERVED  |    |      |      |      |           |          |     |
| R         |    |      |      |      |           |          |     |
| 0h        |    |      |      |      |           |          |     |
| 7         | 6  | 5    | 4    | 3    | 2         | 1        | 0   |
| RESERVED  |    | MSBS | DDIR | ACEN |           | BCE      | DE  |
| R         |    | R/W  | R/W  | R/W  |           | R/W      | R/W |
| 0h        |    | 0h   | 0h   | 0h   |           | 0h       | 0h  |

**Table 5-2608. MMC\_CMD Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description |
|-------|-----------|------|-------|-------------|
| 31:30 | RESERVED2 | R    | 0h    |             |

**Table 5-2608. MMC\_CMD Register Field Descriptions (continued)**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 29:24 | INDX  | R/W  | 0h    | <p>Command index<br/>Binary encoded value from 0 to 63 specifying the command number send to card</p> <p>0 CMD0 or ACMD0<br/>1 CMD1 or ACMD1<br/>2 CMD2 or ACMD2<br/>3 CMD3 or ACMD3<br/>4 CMD4 or ACMD4<br/>5 CMD5 or ACMD5<br/>6 CMD6 or ACMD6<br/>7 CMD7 or ACMD7<br/>8 CMD8 or ACMD8<br/>9 CMD9 or ACMD9<br/>10 CMD10 or ACMD10<br/>11 CMD11 or ACMD11<br/>12 CMD12 or ACMD12<br/>13 CMD13 or ACMD13<br/>14 CMD14 or ACMD14<br/>15 CMD15 or ACMD15<br/>16 CMD16 or ACMD16<br/>17 CMD17 or ACMD17<br/>18 CMD18 or ACMD18<br/>19 CMD19 or ACMD19<br/>20 CMD20 or ACMD20<br/>21 CMD21 or ACMD21<br/>22 CMD22 or ACMD22<br/>23 CMD23 or ACMD23<br/>24 CMD24 or ACMD24<br/>25 CMD25 or ACMD25<br/>26 CMD26 or ACMD26<br/>27 CMD27 or ACMD27<br/>28 CMD28 or ACMD28<br/>29 CMD29 or ACMD29<br/>30 CMD30 or ACMD30<br/>31 CMD31 or ACMD31<br/>32 CMD32 or ACMD32<br/>33 CMD33 or ACMD33<br/>34 CMD34 or ACMD34<br/>35 CMD35 or ACMD35<br/>36 CMD36 or ACMD36<br/>37 CMD37 or ACMD37<br/>38 CMD38 or ACMD38<br/>39 CMD39 or ACMD39<br/>40 CMD40 or ACMD40<br/>41 CMD41 or ACMD41<br/>42 CMD42 or ACMD42<br/>43 CMD43 or ACMD43<br/>44 CMD44 or ACMD44<br/>45 CMD45 or ACMD45<br/>46 CMD46 or ACMD46<br/>47 CMD47 or ACMD47<br/>48 CMD48 or ACMD48<br/>49 CMD49 or ACMD49<br/>50 CMD50 or ACMD50<br/>51 CMD51 or ACMD51<br/>52 CMD52 or ACMD52<br/>53 CMD53 or ACMD53<br/>54 CMD54 or ACMD54<br/>55 CMD55 or ACMD55<br/>56 CMD56 or ACMD56<br/>57 CMD57 or ACMD57<br/>58 CMD58 or ACMD58<br/>59 CMD59 or ACMD59<br/>60 CMD60 or ACMD60<br/>61 CMD61 or ACMD61<br/>62 CMD62 or ACMD62<br/>63 CMD63 or ACMD63</p> |

**Table 5-2608. MMC\_CMD Register Field Descriptions (continued)**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 23:22 | CMD_TYPE  | R/W  | 0h    | <p>Command type</p> <p>This register specifies three types of special command: Suspend, Resume and Abort.</p> <p>These bits shall be set to 00b for all other commands.</p> <p>0 Others Commands</p> <p>1 CMD52 for writing "Bus Suspend" in CCCR</p> <p>2 CMD52 for writing "Function Select" in CCCR</p> <p>3 Abort command CMD12, CMD52 for writing "I/O Abort" in CCCR</p>                                                                                                                                                             |
| 21    | DP        | R/W  | 0h    | <p>Data present select</p> <p>This register indicates that data is present and DAT line shall be used.</p> <p>It must be set to 0 in the following conditions:</p> <ul style="list-style-type: none"> <li>- command using only CMD line</li> <li>- command with no data transfer but using busy signal on DAT[0]</li> <li>- Resume command</li> </ul> <p>0 Command with no data transfer</p> <p>1 Command with data transfer</p>                                                                                                           |
| 20    | CICE      | R/W  | 0h    | <p>Command Index check enable</p> <p>This bit must be set to 1 to enable index check on command response to compare the index field in the response against the index of the command.</p> <p>If the index is not the same in the response as in the command, it is reported as a command index error [MMCSD_STAT[CIE] set to 1]</p> <p>Note: The register CICE cannot be configured for an Auto CMD12, then index check is automatically checked when this command is issued.</p> <p>0 Index check disable</p> <p>1 Index check enable</p> |
| 19    | CCCE      | R/W  | 0h    | <p>Command CRC check enable</p> <p>This bit must be set to 1 to enable CRC7 check on command response to protect the response against transmission errors on the bus.</p> <p>If an error is detected, it is reported as a command CRC error [MMCSD_STAT[CCRC] set to 1].</p> <p>Note: The register CCCE cannot be configured for an Auto CMD12, and then CRC check is automatically checked when this command is issued.</p> <p>0 CRC7 check disable</p> <p>1 CRC7 check enable</p>                                                        |
| 18    | RESERVED1 | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 17:16 | RSP_TYPE  | R/W  | 0h    | <p>Response type</p> <p>This bits defines the response type of the command</p> <p>0 No response</p> <p>1 Response Length 136 bits</p> <p>2 Response Length 48 bits</p> <p>3 Response Length 48 bits with busy after response</p>                                                                                                                                                                                                                                                                                                           |
| 15:6  | RESERVED  | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

**Table 5-2608. MMC\_CMD Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-----|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | MSBS  | R/W  | 0h    | <p>Multi/Single block select</p> <p>This bit must be set to 1 for data transfer in case of multi block command.</p> <p>For any others command this bit shall be set to 0.</p> <p>0 Single block. If this bit is 0, it is not necessary to set the register MMCHS_BLK[NBLK].</p> <p>1 Multi block. When Block Count is disabled (MMCHS_CMD[BCE] is set to 0) in Multiple block transfers (MMCHS_CMD[MSBS] is set to 1), the module can perform infinite transfer.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 4   | DDIR  | R/W  | 0h    | <p>Data transfer Direction Select</p> <p>This bit defines either data transfer will be a read or a write.</p> <p>0 Data write (host to card)</p> <p>1 Data Read (card to host)</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 3:2 | ACEN  | R/W  | 0h    | <p>Auto CMD Enable - SD card only.</p> <p>This field determines use of auto command functions.</p> <p>There are two methods to stop Multiple-block read and write operation</p> <p>[1] Auto CMD12 Enable</p> <p>When this field is set to 01b the Host Controller issues CMD12 automatically when last block transfer is completed. Auto CMD12 error is indicated to the Auto CMD Error Status register. The Host Driver shall not set this bit if the command does not require CMD12. In particular, secure commands defined in the Part 3 File Security specification do not require CMD12.</p> <p>[2] Auto CMD23 Enable</p> <p>When this bit field is set to 10b the Host Controller issues a CMD23 automatically before issuing a command specified in the Command Register. The Host Controller Version 3.00 and later shall support this function. The following conditions are required to use the Auto CMD23.</p> <p>Auto CMD23 Supported [Host Controller Version is 3.00 or later]</p> <p>A memory card that supports CMD23 [SCR[33]=1]</p> <p>If DMA is used, it shall be ADMA.</p> <p>Only when CMD18 or CMD25 is issued</p> <p>[Note, the Host Controller does not check command index.]</p> <p>Auto CMD23 can be used with or without ADMA. By Writing the Command register, the Host Controller issues a CMD23 first and then issues a command specified by the Command Index in Command register. If response errors of CMD23 are detected, the second command is not issued. A CMD23 error is indicated in the Auto CMD Error Status register. 32-bit block count value for CMD23 is set to SDMA System Address / Argument 2 register.</p> <p>0 Auto Command Disabled</p> <p>1 Auto CMD12 enable or CCS detection enabled.</p> <p>2 Auto CMD23 Enable</p> <p>3 Reserved</p> |
| 1   | BCE   | R/W  | 0h    | <p>Block Count Enable</p> <p>Multiple block transfers only.</p> <p>This bit is used to enable the block count register [MMCHS_BLK[NBLK]].</p> <p>When Block Count is disabled [MMCHS_CMD[BCE] is set to 0] in Multiple block transfers [MMCHS_CMD[MSBS] is set to 1], the module can perform infinite transfer.</p> <p>0 Block count disabled for infinite transfer.</p> <p>1 Block count enabled for multiple block transfer with known number of blocks</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

**Table 5-2608. MMC\_CMD Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                          |
|-----|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------|
| 0   | DE    | R/W  | 0h    | DMA Enable<br>This bit is used to enable DMA mode for host data access.<br><br>0        DMA mode disable<br>1        DMA mode enable |

### 5.15.2.13 MMC\_RSP10 Register

#### 1 MMC\_RSP10 Register (Offset = 210h) [reset = 0h]

Command Response[31:0] Register

This 32-bit register holds bits positions [31:0] of command response type R1/R1b/R2/R3/R4/R5/R5b/R6.

Return to [Summary Table](#)

**Table 5-2609. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCSD0        | 4830 0210h       |

**Figure 5-862. MMC\_RSP10 Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RSP1 |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RSP1 |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RSP0 |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RSP0 |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-2611. MMC\_RSP10 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description              |
|-------|-------|------|-------|--------------------------|
| 31:16 | RSP1  | R    | 0h    | Command Response [31:16] |
| 15:0  | RSP0  | R    | 0h    | Command Response [15:0]  |



### 5.15.2.14 MMC\_RSP32 Register

#### 1 MMC\_RSP32 Register (Offset = 214h) [reset = 0h]

Command Response[63:32] Register

This 32-bit register holds bits positions [63:32] of command response type R2.

Return to [Summary Table](#)

**Table 5-2612. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCSD0        | 4830 0214h       |

**Figure 5-863. MMC\_RSP32 Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RSP3 |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RSP3 |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RSP2 |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RSP2 |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-2614. MMC\_RSP32 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description              |
|-------|-------|------|-------|--------------------------|
| 31:16 | RSP3  | R    | 0h    | Command Response [63:48] |
| 15:0  | RSP2  | R    | 0h    | Command Response [47:32] |

### 5.15.2.15 MMC\_RSP54 Register

#### 1 MMC\_RSP54 Register (Offset = 218h) [reset = 0h]

Command Response[95:64] Register

This 32-bit register holds bits positions [95:64] of command response type R2.

Return to [Summary Table](#)

**Table 5-2615. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCSD0        | 4830 0218h       |

**Figure 5-864. MMC\_RSP54 Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RSP5 |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RSP5 |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RSP4 |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RSP4 |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-2617. MMC\_RSP54 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description              |
|-------|-------|------|-------|--------------------------|
| 31:16 | RSP5  | R    | 0h    | Command Response [95:80] |
| 15:0  | RSP4  | R    | 0h    | Command Response [79:64] |

### 5.15.2.16 MMC\_RSP76 Register

#### 1 MMC\_RSP76 Register (Offset = 21Ch) [reset = 0h]

Command Response[127:96] Register

This 32-bit register holds bits positions [127:96] of command response type R1(Auto CMD23)/R1b(Auto CMD12)/R2.

Return to [Summary Table](#)

**Table 5-2618. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCSD0        | 4830 021Ch       |

**Figure 5-865. MMC\_RSP76 Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RSP7 |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RSP7 |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RSP6 |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RSP6 |    |    |    |    |    |    |    |
| R    |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-2620. MMC\_RSP76 Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                |
|-------|-------|------|-------|----------------------------|
| 31:16 | RSP7  | R    | 0h    | Command Response [127:112] |
| 15:0  | RSP6  | R    | 0h    | Command Response [111:96]  |

### 5.15.2.17 MMC\_DATA Register

#### 1 MMC\_DATA Register (Offset = 220h) [reset = 0h]

##### Data Register

This register is the 32-bit entry point of the buffer for read or write data transfers.

The buffer size is 32bits x256(1024 bytes). Bytes within a word are stored and read in little endian format. This buffer can be used as two 512 byte buffers to transfer data efficiently without reducing the throughput.

Sequential and contiguous access is necessary to increment the pointer correctly. Random or skipped access is not allowed. In little endian, if the local host accesses this register byte-wise or 16bit-wise, the least significant byte (bits [7:0]) must always be written/read first. The update of the buffer address is done on the most significant byte write for full 32-bit DATA register or on the most significant byte of the last word of block transfer.

Example 1: Byte or 16-bit access

Mbyteen[3:0]=0001 (1-byte) => Mbyteen[3:0]=0010 (1-byte) => Mbyteen[3:0]=1100 (2-bytes) OK

Mbyteen[3:0]=0001 (1-byte) => Mbyteen[3:0]=0010 (1-byte) => Mbyteen[3:0]=0100 (1-byte) OK

Mbyteen[3:0]=0001 (1-byte) => Mbyteen[3:0]=0010 (1-byte) => Mbyteen[3:0]=1000 (1-byte) Bad .

Return to [Summary Table](#)

**Table 5-2621. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCSD0        | 4830 0220h       |

**Figure 5-866. MMC\_DATA Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-2623. MMC\_DATA Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | DATA  | R/W  | 0h    | Data Register [31:0]<br>In functional mode [MMCSD_CON[MODE]] set to the default value 0] ,<br>A read access to this register is allowed only when the buffer read enable status is set to 1 [MMCSD_PSTATE[BRE]], otherwise a bad access [MMCSD_STAT[BADA]] is signaled.<br>A write access to this register is allowed only when the buffer write enable status is set to 1[MMCSD_STATE[BWE]], otherwise a bad access [MMCSD_STAT[BADA]] is signaled and the data is not written. |

### 5.15.2.18 MMC\_PSTATE Register

#### 1 MMC\_PSTATE Register (Offset = 224h) [reset = 40000h]

Present State Register

The Host can get status of the Host Controller from this 32-bit read only register.

Return to [Summary Table](#)

**Table 5-2624. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCS0         | 4830 0224h       |

**Figure 5-867. MMC\_PSTATE Name Register**

| 31        | 30 | 29 | 28 | 27  | 26   | 25   | 24   |
|-----------|----|----|----|-----|------|------|------|
| RESERVED2 |    |    |    |     |      |      | CLEV |
| R         |    |    |    |     |      |      | R    |
| 0h        |    |    |    |     |      |      | 0h   |
| 23        | 22 | 21 | 20 | 19  | 18   | 17   | 16   |
| DLEV      |    |    |    | WP  | CDPL | CSS  | CINS |
| R         |    |    |    | R   | R    | R    | R    |
| 0h        |    |    |    | 0h  | 1h   | 0h   | 0h   |
| 15        | 14 | 13 | 12 | 11  | 10   | 9    | 8    |
| RESERVED1 |    |    |    | BRE | BWE  | RTA  | WTA  |
| R         |    |    |    | R   | R    | R    | R    |
| 0h        |    |    |    | 0h  | 0h   | 0h   | 0h   |
| 7         | 6  | 5  | 4  | 3   | 2    | 1    | 0    |
| RESERVED  |    |    |    | RTR | DLA  | DATI | CMDI |
| R         |    |    |    | R   | R    | R    | R    |
| 0h        |    |    |    | 0h  | 0h   | 0h   | 0h   |

**Table 5-2626. MMC\_PSTATE Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                             |
|-------|-----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:25 | RESERVED2 | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                         |
| 24    | CLEV      | R    | 0h    | CMD line signal level<br>This status is used to check the CMD line level to recover from errors, and for debugging.<br>The value of this register after reset depends on the CMD line level at that time.<br>0 The CMD line level is 0.<br>1 The CMD line level is 1.                                                                                                   |
| 23:20 | DLEV      | R    | 0h    | DAT[3:0] line signal level<br>DAT[3] => bit 23<br>DAT[2] => bit 22<br>DAT[1] => bit 21<br>DAT[0] => bit 20<br>This status is used to check DAT line level to recover from errors, and for debugging. This is especially useful in detecting the busy signal level from DAT[0].<br>The value of these registers after reset depends on the DAT lines level at that time. |

**Table 5-2626. MMC\_PSTATE Register Field Descriptions (continued)**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19    | WP        | R    | 0h    | <p>Write protect switch pin level<br/>For SDIO cards only.<br/>This bit reflects the write protect input pin [SDWP] level.<br/>The value of this register after reset depends on the protect input pin [SDWP] level at that time.</p> <p>0 If MMCHS_CON[WPP] is set to 0 (default), the card is write protected, otherwise the card is not protected.<br/>1 If MMCHS_CON[WPP] is set to 0 (default), the card is not write protected, otherwise the card is protected.</p>                                                                                                                                                                                                                                                                                                           |
| 18    | CDPL      | R    | 1h    | <p>Card detect pin level<br/>This bit reflects the inverse value of the card detect input pin [SDCD], debouncing is not performed on this bit and bit is valid only when Card State Stable [MMCSD_PSTATE[CSS]] is set to 1.<br/>Use of this bit is limited to testing since it must be debounced y software.<br/>The value of this register after reset depends on the card detect input pin [SDCD] level at that time.</p> <p>0 The value of the card detect input pin (SDCD) is 1<br/>1 The value of the card detect input pin (SDCD) is 0</p>                                                                                                                                                                                                                                     |
| 17    | CSS       | R    | 0h    | <p>Card State Stable<br/>This bit is used for testing. It is set to 1 only when Card Detect Pin Level is stable [MMCSD_PSTATE[CDPL]]. Debouncing is performed on the card detect input pin [SDCD] to detect card stability.<br/>This bit is not affected by a software reset.</p> <p>0 Reset or Debouncing<br/>1 No card or card inserted</p>                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 16    | CINS      | R    | 0h    | <p>Card inserted<br/>This bit is the debounced value of the card detect input pin [SDCD]. An inactive to active transition of the card detect input pin [SDCD] will generate a card insertion interrupt [MMCSD_STAT[CINS]]. A active to inactive transition of the card detect input pin [SDCD] will generate a card removal interrupt [MMCSD_STAT[REM]].<br/>This bit is not affected by a software reset.</p> <p>0 If MMCHS_CON[CDP] is set to 1, no card is detected. The card may have been removed from the card slot. If MMCHS_CON[CDP] is set to 0, the card has been inserted.<br/>1 If MMCHS_CON[CDP] is set to 1, the card has been inserted from the card slot. If MMCHS_CON[CDP] is set to 0 no card is detected. The card may have been removed from the card slot.</p> |
| 15:12 | RESERVED1 | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 11    | BRE       | R    | 0h    | <p>Buffer read enable<br/>This bit is used for non-DMA read transfers.<br/>It indicates that a complete block specified by MMCSD_BLK[BLN] has been written in the buffer and is ready to be read.<br/>It is set to 0 when the entire block is read from the buffer. It is set to 1 when a block data is ready in the buffer and generates the Buffer read ready status of interrupt [MMCSD_STAT[BRR]].</p> <p>0 Read BLN bytes disable<br/>1 Read BLN bytes enable. Readable data exists in the buffer.</p>                                                                                                                                                                                                                                                                          |

**Table 5-2626. MMC\_PSTATE Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-----|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | BWE      | R    | 0h    | <p>Buffer Write enable<br/>This status is used for non-DMA write transfers. It indicates if space is available for write data.</p> <p>0      There is no room left in the buffer to write BLEN bytes of data.<br/>1      There is enough space in the buffer to write BLEN bytes of data.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 9   | RTA      | R    | 0h    | <p>Read transfer active<br/>This status is used for detecting completion of a read transfer. It is set to 1 after the end bit of read command or by activating a continue request [MMCSH_HCTL[CR]] following a stop at block gap request. This bit is set to 0 when all data have been read by the local host after last block or after a stop at block gap request.</p> <p>0      No valid data on the DAT lines.<br/>1      read data transfer on going.</p>                                                                                                                                                                                                                                                                                                                                                                                    |
| 8   | WTA      | R    | 0h    | <p>Write transfer active<br/>This status indicates a write transfer active. It is set to 1 after the end bit of write command or by activating a continue request [MMCSH_HCTL[CR]] following a stop at block gap request. This bit is set to 0 when CRC status has been received after last block or after a stop at block gap request.</p> <p>0      No valid data on the DAT lines.<br/>1      write data transfer on going.</p>                                                                                                                                                                                                                                                                                                                                                                                                                |
| 7:4 | RESERVED | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 3   | RTR      | R    | 0h    | <p>Re-Tuning Request<br/>Host Controller may request Host Driver to execute re-tuning sequence by setting this bit when the data window is shifted by temperature drift and a tuned sampling point does not have a good margin to receive correct data. This bit is cleared when a command is issued with setting Execute Tuning in the Host Control 2 register. Changing of this bit from 0 to 1 generates Re-Tuning Event. Refer to Normal Interrupt Status registers for more detail. This bit isn't set to 1 if Sampling Clock Select in the Host Control 2 register is set to 0 [using fixed sampling clock]. Refer to Re-Tuning Modes in the Capabilities register for more detail.</p> <p>0      Fixed or well tuned sampling clock<br/>1      Sampling clock needs re-tuning</p>                                                          |
| 2   | DLA      | R    | 0h    | <p>DAT line active<br/>This status bit indicates whether one of the DAT line is in use. In the case of read transactions [card to host]: This bit is set to 1 after the end bit of read command or by activating continue request MMCSH_HCTL[CR]. This bit is set to 0 when the host controller received the end bit of the last data block or at the beginning of the read wait mode. In the case of write transactions [host to card]: This bit is set to 1 after the end bit of write command or by activating continue request MMCSH_HCTL[CR]. This bit is set to 0 on the end of busy event for the last block; host controller must wait 8 clock cycles with line not busy to really consider not "busy state" or after the busy block as a result of a stop at gap request.</p> <p>0      DAT Line inactive<br/>1      DAT Line active</p> |

**Table 5-2626. MMC\_PSTATE Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-----|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | DATI  | R    | 0h    | <p>Command inhibit[DAT]</p> <p>This status bit is generated if either DAT line is active [MMCSD_PSTATE[DLA]] or Read transfer is active [MMCSD_PSTATE[RTA]] or when a command with busy is issued. This bit prevents the local host to issue a command. A change of this bit from 1 to 0 generates a transfer complete interrupt [MMCSD_STAT[TC]].</p> <p>0 Issuing of command using the DAT lines is allowed</p> <p>1 Issuing of command using DAT lines is not allowed</p>                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 0   | CMDI  | R    | 0h    | <p>Command inhibit[CMD]</p> <p>This status bit indicates that the CMD line is in use. This bit is set to 0 when the most significant byte is written into the command register. This bit is not set when Auto CMD12 is transmitted.</p> <p>This bit is set to 0 in either the following cases:</p> <ul style="list-style-type: none"> <li>- After the end bit of the command response, excepted if there is a command conflict error [MMCSD_STAT[CCRC] or MMCSD_STAT[CEB] set to 1] or a Auto CMD12 is not executed [MMCSD_AC12[ACNE]].</li> <li>- After the end bit of the command without response [MMCSD_CMD[RSP_TYPE] set to "00"]</li> </ul> <p>In case of a command data error is detected [MMCSD_STAT[CTO] set to 1], this register is not automatically cleared.</p> <p>0 Issuing of command using CMD line is allowed</p> <p>1 Issuing of command using CMD line is not allowed</p> |



### 5.15.2.19 MMC\_HCTL Register

#### 1 MMC\_HCTL Register (Offset = 228h) [reset = 0h]

Host Control Register

This register defines the host controls to set power, wakeup and transfer parameters.

MMCHS\_HCTL[31:24] = Wakeup control

MMCHS\_HCTL[23:16] = Block gap control

MMCHS\_HCTL[15:8] = Power control

MMCHS\_HCTL[7:0] = Host control.

Return to [Summary Table](#)

**Table 5-2627. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCSD0        | 4830 0228h       |

**Figure 5-868. MMC\_HCTL Name Register**

| 31        | 30   | 29       | 28   | 27   | 26   | 25  | 24   |
|-----------|------|----------|------|------|------|-----|------|
| RESERVED3 |      |          |      | OBWE | REM  | INS | IWE  |
| R         |      |          |      | R/W  | R/W  | R/W | R/W  |
| 0h        |      |          |      | 0h   | 0h   | 0h  | 0h   |
| 23        | 22   | 21       | 20   | 19   | 18   | 17  | 16   |
| RESERVED2 |      |          |      | IBG  | RWC  | CR  | SBGR |
| R         |      |          |      | R/W  | R/W  | R/W | R/W  |
| 0h        |      |          |      | 0h   | 0h   | 0h  | 0h   |
| 15        | 14   | 13       | 12   | 11   | 10   | 9   | 8    |
| RESERVED1 |      |          |      | SDVS |      |     | SDBP |
| R         |      |          |      | R/W  |      |     | R/W  |
| 0h        |      |          |      | 0h   |      |     | 0h   |
| 7         | 6    | 5        | 4    | 3    | 2    | 1   | 0    |
| CDSS      | CDTL | RESERVED | DMAS |      | HSPE | DTW | LED  |
| R/W       | R/W  | R        | R/W  |      | R/W  | R/W | R    |
| 0h        | 0h   | 0h       | 0h   |      | 0h   | 0h  | 0h   |

**Table 5-2629. MMC\_HCTL Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                |
|-------|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28 | RESERVED3 | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                            |
| 27    | OBWE      | R/W  | 0h    | Wakeup event enable for 'Out-of-Band' Interrupt.<br>This bit enables wakeup events for 'Out-of-Band' assertion.<br>Wakeup is generated if the wakeup feature is enabled [MMCSD_SYSCONFIG[ENAWAKEUP]].<br>The write to this register is ignored when MMCSD_CON[OBIE] is not set.<br><br>0      Disable wakeup on 'Out-of-Band' Interrupt<br>1      Enable wakeup on 'Out-of-Band' Interrupt |
| 26    | REM       | R/W  | 0h    | Wakeup event enable on SD card removal<br>This bit enables wakeup events for card removal assertion.<br>Wakeup is generated if the wakeup feature is enabled [MMCSD_SYSCONFIG[ENAWAKEUP]].<br><br>0      Disable wakeup on card removal<br>1      Enable wakeup on card removal                                                                                                            |

**Table 5-2629. MMC\_HCTL Register Field Descriptions (continued)**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|-----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 25    | INS       | R/W  | 0h    | Wakeup event enable on SD card insertion<br>This bit enables wakeup events for card insertion assertion. Wakeup is generated if the wakeup feature is enabled [MMCSA_SYSCONFIG[ENAWAKEUP]].<br><br>0      Disable wakeup on card insertion<br>1      Enable wakeup on card insertion                                                                                                                                                                                                                                                                                                                                                      |
| 24    | IWE       | R/W  | 0h    | Wakeup event enable on SD card interrupt<br>This bit enables wakeup events for card interrupt assertion. Wakeup is generated if the wakeup feature is enabled [MMCSA_SYSCONFIG[ENAWAKEUP]].<br><br>0      Disable wakeup on card interrupt<br>1      Enable wakeup on card interrupt                                                                                                                                                                                                                                                                                                                                                      |
| 23:20 | RESERVED2 | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 19    | IBG       | R/W  | 0h    | Interrupt block at gap<br>This bit is valid only in 4-bit mode of SDIO card to enable interrupt detection in the interrupt cycle at block gap for a multiple block transfer. For MMC cards and for SD card this bit should be set to 0.<br><br>0      Disable interrupt detection at the block gap in 4-bit mode<br>1      Enable interrupt detection at the block gap in 4-bit mode                                                                                                                                                                                                                                                      |
| 18    | RWC       | R/W  | 0h    | Read wait control<br>The read wait function is optional only for SDIO cards. If the card supports read wait, this bit must be enabled, then requesting a stop at block gap [MMCSA_HCTL[SBGR]] generates a read wait period after the current end of block. Be careful, if read wait is not supported it may cause a conflict on DAT line.<br><br>0      Disable Read Wait Control. Suspend/Resume cannot be supported.<br>1      Enable Read Wait Control                                                                                                                                                                                 |
| 17    | CR        | R/W  | 0h    | Continue request<br>This bit is used to restart a transaction that was stopped by requesting a stop at block gap [MMCSA_HCTL[SBGR]]. Set this bit to 1 restarts the transfer. The bit is automatically set to 0 by the host controller when transfer has restarted i.e DAT line is active [MMCSA_PSTATE[DLA]] or transferring data [MMCSA_PSTATE[WT]].<br>The Stop at block gap request must be disabled [MMCSA_HCTL[SBGR]=0] before setting this bit.<br><br>0      No affect<br>1      transfer restart                                                                                                                                 |
| 16    | SBGR      | R/W  | 0h    | Stop at block gap request<br>This bit is used to stop executing a transaction at the next block gap. The transfer can restart with a continue request [MMCSA_HCTL[CR]] or during a suspend/resume sequence.<br>In case of read transfer, the card must support read wait control. In case of write transfer, the host driver shall set this bit after all block data written.<br>Until the transfer completion [MMCSA_STAT[TC] set to 1], the host driver shall leave this bit set to 1.<br>If this bit is set, the local host shall not write to the data register [MMCSA_DATA].<br><br>0      Transfer mode<br>1      Stop at block gap |
| 15:12 | RESERVED1 | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

**Table 5-2629. MMC\_HCTL Register Field Descriptions (continued)**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 11:9 | SDVS     | R/W  | 0h    | SD bus voltage select<br>All cards.<br>The host driver should set to these bits to select the voltage level for the card according to the voltage supported by the system [MMCSD_CAPA[VS18,VS30,VS33]] before starting a transfer.<br><br>5      1.8V (Typical)<br>6      3.0V (Typical)<br>7      3.3V (Typical)                                                                                                                                                                                                                           |
| 8    | SDBP     | R/W  | 0h    | SD bus power<br>Before setting this bit, the host driver shall select the SD bus voltage [MMCSD_HCTL[SDVS]]. If the host controller detects the No card state, this bit is automatically set to 0. If the module is power off, a write in the command register [MMCSD_CMD] will not start the transfer. A write to this bit has no effect if the selected SD bus voltage MMCSD_HCTL[SDVS] is not supported according to capability register [MMCSD_CAPA[VS*]].<br><br>0      Power off<br>1      Power on                                   |
| 7    | CDSS     | R/W  | 0h    | Card Detect Signal Selection<br>This bit selects source for the card detection. When the source for the card detection is switched, the interrupt should be disabled during the switching period by clearing the Interrupt Status/Signal Enable register in order to mask unexpected interrupt being caused by the glitch. The Interrupt Status/Signal Enable should be disabled during over the period of debouncing.<br><br>0      SDCD# is selected (for normal use)<br>1      The Card Detect Test Level is selected (for test purpose) |
| 6    | CDTL     | R/W  | 0h    | Card Detect Test Level:<br>This bit is enabled while the Card Detect Signal Selection is set to 1 and it indicates card inserted or not.<br><br>0      No Card<br>1      Card Inserted                                                                                                                                                                                                                                                                                                                                                      |
| 5    | RESERVED | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 4:3  | DMAS     | R/W  | 0h    | DMA Select Mode:<br>One of supported DMA modes can be selected. The host driver shall check support of DMA modes by referring the Capabilities register. Use of selected DMA is determined by DMA Enable of the Transfer Mode register. This register is only meaningful when MADMA_EN is set to 1. When MADMA_EN is set to 0 the bit field is read only and returned value is 0.<br><br>0      Reserved<br>1      Reserved<br>2      32-bit Address ADMA2 is selected<br>3      Reserved                                                   |
| 2    | HSPE     | R/W  | 0h    | High Speed Enable:<br>Before setting this bit, the Host Driver shall check the High Speed Support in the Capabilities register. If this bit is set to 0 [default], the Host Controller outputs CMD line and DAT lines at the falling edge of the SD Clock. If this bit is set to 1, the Host Controller outputs CMD line and DAT lines at the rising edge of the SD Clock. This bit shall not be set when dual data rate mode is activated in MMCSD_CON[DDR].<br><br>0      Normal speed mode<br>1      High speed mode                     |

**Table 5-2629. MMC\_HCTL Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-----|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | DTW   | R/W  | 0h    | <p>Data transfer width</p> <p>For MMC card, this bit must be set following a valid SWITCH command [CMD6] with the correct value and extend CSD index written in the argument. Prior to this command, the MMC card configuration register [CSD and EXT_CSD] must be verified for compliance with MMC standard specification 4.x [see section 3.6]. This register has no effect when the MMC 8-bit mode is selected [register MMCSD_CON[DW8] set to 1 ],</p> <p>For SD/SDIO cards, this bit must be set following a valid SET_BUS_WIDTH command [ACMD6] with the value written in bit 1 of the argument. Prior to this command, the SD card configuration register [SCR] must be verified for the supported bus width by the SD card.</p> <p>0        1-bit Data width (DAT[0] used)<br/> 1        4-bit Data width (DAT[3:0] used)</p> |
| 0   | LED   | R    | 0h    | <p>Reserved bit.</p> <p>LED control feature is not supported</p> <p>This bit is initialized to zero, and writes to it are ignored.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

### 5.15.2.20 MMC\_SYSCTL Register

#### 1 MMC\_SYSCTL Register (Offset = 22Ch) [reset = 0h]

##### SD System Control Register

This register defines the system controls to set software resets, clock frequency management and data timeout.

MMCHS\_SYSCTL[31:24] = Software resets

MMCHS\_SYSCTL[23:16] = Timeout control

MMCHS\_SYSCTL[15:0] = Clock control.

Return to [Summary Table](#)

**Table 5-2630. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCSD0        | 4830 022Ch       |

**Figure 5-869. MMC\_SYSCTL Name Register**

| 31        | 30  | 29       | 28 | 27  | 26  | 25  | 24  |
|-----------|-----|----------|----|-----|-----|-----|-----|
| RESERVED2 |     |          |    |     | SRD | SRC | SRA |
| R         |     |          |    |     | R/W | R/W | R/W |
| 0h        |     |          |    |     | 0h  | 0h  | 0h  |
| 23        | 22  | 21       | 20 | 19  | 18  | 17  | 16  |
| RESERVED1 |     |          |    | DTO |     |     |     |
| R         |     |          |    | R/W |     |     |     |
| 0h        |     |          |    | 0h  |     |     |     |
| 15        | 14  | 13       | 12 | 11  | 10  | 9   | 8   |
| CLKD      |     |          |    |     |     |     |     |
| R/W       |     |          |    |     |     |     |     |
| 0h        |     |          |    |     |     |     |     |
| 7         | 6   | 5        | 4  | 3   | 2   | 1   | 0   |
| CLKD      | CGS | RESERVED |    |     | CEN | ICS | ICE |
| R/W       | R   | R        |    |     | R/W | R   | R/W |
| 0h        | 0h  | 0h       |    |     | 0h  | 0h  | 0h  |

**Table 5-2632. MMC\_SYSCTL Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|-------|-----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:27 | RESERVED2 | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 26    | SRD       | R/W  | 0h    | <p>Software reset for DAT line</p> <p>This bit is set to 1 for reset and released to 0 when completed. DAT finite state machine in both clock domain are also reset. Here below are the registers cleared by MMCSD_SYSCTL[SRD]:</p> <ul style="list-style-type: none"> <li>- MMCSD_DATA</li> <li>- MMCSD_PSTATE: BRE, BWE, RTA, WTA, DLA and DATI</li> <li>- MMCSD_HCTL: SBGR and CR</li> <li>- MMCSD_STAT: BRR, BWR, BGE and TC</li> </ul> <p>OCF and MMC buffer data management is reinitialized.</p> <p>0      Reset completed</p> <p>1      Software reset for DAT line</p> |

**Table 5-2632. MMC\_SYSTL Register Field Descriptions (continued)**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 25    | SRC       | R/W  | 0h    | Software reset for CMD line<br>This bit is set to 1 for reset and released to 0 when completed.<br>CMD finite state machine in both clock domain are also reset.<br>Here below the registers cleared by MMCSD_SYSTL[SRC]:<br>- MMCSD_PSTATE: CMDI<br>- MMCSD_STAT: CC<br>OCP and MMC command status management is reinitialized.<br><br>0      Reset completed<br>1      Software reset for CMD line                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 24    | SRA       | R/W  | 0h    | Software reset for all<br>This bit is set to 1 for reset , and released to 0 when completed.<br>This reset affects the entire host controller except for the card detection circuit and capabilities registers.<br><br>0      Reset completed<br>1      Software reset for all the design                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 23:20 | RESERVED1 | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 19:16 | DTO       | R/W  | 0h    | Data timeout counter value and busy timeout.<br>This value determines the interval by which DAT lines timeouts are detected.<br>The host driver needs to set this bitfield based on<br>- the maximum read access time [NAC] [Refer to the SD Specification Part1 Physical Layer],<br>- the data read access time values [TAAC and NSAC] in the card specific data register [CSD] of the card,<br>- the timeout clock base frequency [MMCSD_CAPA[TCF]].<br>If the card does not respond within the specified number of cycles, a data timeout error occurs [MMCSD_STA[DTO]].<br>The MMCSD_SYSTL[DTO] register is also used to check busy duration, to generate busy timeout for commands with busy response or for busy programming during a write command. Timeout on CRC status is generated if no CRC token is present after a block write.<br><br>0      TCF x 2 <sup>13</sup><br>1      TCF x 2 <sup>14</sup><br>14    TCF x 2 <sup>27</sup><br>15    Reserved |
| 15:6  | CLKD      | R/W  | 0h    | Clock frequency select<br>These bits define the ratio between a reference clock frequency [system dependant] and the output clock frequency on the CLK pin of either the memory card [MMC, SD or SDIO].<br><br>0      Clock Ref bypass<br>1      Clock Ref bypass<br>2      Clock Ref / 2<br>3      Clock Ref / 3<br>1023   Clock Ref / 1023                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 5     | CGS       | R    | 0h    | Clock Generator Select - For SD cards<br>Host Controller Version 3.00 supports this bit. This bit is used to select the clock generator mode in SDCLK Frequency Select. If the Programmable Clock Mode is supported [non-zero value is set to Clock Multiplier in the Capabilities register], this bit attribute is RW, and if not supported, this bit attribute is RO and zero is read. This bit depends on the setting of Preset Value Enable in the Host Control 2 register. If the Preset Value Enable = 0, this bit is set by Host Driver. If the Preset Value Enable = 1, this bit is automatically set to a value specified in one of Preset Value registers.                                                                                                                                                                                                                                                                                               |
| 4:3   | RESERVED  | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

**Table 5-2632. MMC\_SYSCCTL Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | CEN   | R/W  | 0h    | <p>Clock enable<br/>This bit controls if the clock is provided to the card or not.</p> <p>0 The clock is not provided to the card .<br/>Clock frequency can be changed .</p> <p>1 The clock is provided to the card and can be automatically gated when MMCHS_SYSCONFIG[AUTOIDLE] is set to 1 (default value) . The host driver shall wait to set this bit to 1 until the Internal clock is stable (MMCHS_SYSCCTL[ICS]).</p>                                                                                                         |
| 1   | ICS   | R    | 0h    | <p>Internal clock stable [status]<br/>This bit indicates either the internal clock is stable or not.</p> <p>0 The internal clock is not stable.</p> <p>1 The internal clock is stable after enabling the clock (MMCHS_SYSCCTL[ICE]) or after changing the clock ratio (MMCHS_SYSCCTL[CLKD]).</p>                                                                                                                                                                                                                                     |
| 0   | ICE   | R/W  | 0h    | <p>Internal clock enable<br/>This register controls the internal clock activity.<br/>In very low power state, the internal clock is stopped.<br/>Note: The activity of the debounce clock [used for wakeup events] and the OCP clock [used for reads and writes to the module register map] are not affected by this register.</p> <p>0 The internal clock is stopped (very low power state).</p> <p>1 The internal clock oscillates and can be automatically gated when MMCHS_SYSCONFIG[AUTOIDLE] is set to 1 (default value) .</p> |

### 5.15.2.21 MMC\_STAT Register

#### 1 MMC\_STAT Register (Offset = 230h) [reset = 0h]

Interrupt Status Register

The interrupt status regroups all the status of the module internal events that can generate an interrupt.

MMCHS\_STAT[31:16] = Error Interrupt Status

MMCHS\_STAT[15:0] = Normal Interrupt Status.

Return to [Summary Table](#)

**Table 5-2633. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCSD0        | 4830 0230h       |

**Figure 5-870. MMC\_STAT Name Register**

| 31        | 30       | 29   | 28   | 27        | 26  | 25    | 24   |
|-----------|----------|------|------|-----------|-----|-------|------|
| RESERVED3 |          | BADA | CERR | RESERVED2 | TE  | ADMAE | ACE  |
| R         |          | R/W  | R/W  | R         | R/W | R/W   | R/W  |
| 0h        |          | 0h   | 0h   | 0h        | 0h  | 0h    | 0h   |
| 23        | 22       | 21   | 20   | 19        | 18  | 17    | 16   |
| CLE       | DEB      | DCRC | DTO  | CIE       | CEB | CCRC  | CTO  |
| R         | R/W      | R/W  | R/W  | R/W       | R/W | R/W   | R/W  |
| 0h        | 0h       | 0h   | 0h   | 0h        | 0h  | 0h    | 0h   |
| 15        | 14       | 13   | 12   | 11        | 10  | 9     | 8    |
| ERRI      | RESERVED |      |      |           | BSR | OBI   | CIRQ |
| R         | R        |      |      |           | R/W | R/W   | R    |
| 0h        | 0h       |      |      |           | 0h  | 0h    | 0h   |
| 7         | 6        | 5    | 4    | 3         | 2   | 1     | 0    |
| CREM      | CINS     | BRR  | BWR  | DMA       | BGE | TC    | CC   |
| R/W       | R/W      | R/W  | R/W  | R/W       | R/W | R/W   | R/W  |
| 0h        | 0h       | 0h   | 0h   | 0h        | 0h  | 0h    | 0h   |

**Table 5-2635. MMC\_STAT Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | RESERVED3 | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 29    | BADA      | R/W  | 0h    | <p>Bad access to data space</p> <p>This bit is set automatically to indicate a bad access to buffer when not allowed:</p> <ul style="list-style-type: none"> <li>-This bit is set during a read access to the data register [MMCSD_DATA] while buffer reads are not allowed [MMCSD_PSTATE[BRE] =0]</li> <li>-This bit is set during a write access to the data register [MMCSD_DATA] while buffer writes are not allowed [MMCSD_STATE[BWE] =0]</li> </ul> <p>0 No Interrupt.<br/>0 Status bit unchanged<br/>1 Bad Access<br/>1 Status is cleared</p> |



**Table 5-2635. MMC\_STAT Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-----|-----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 28  | CERR      | R/W  | 0h    | <p>Card error</p> <p>This bit is set automatically when there is at least one error in a response of type R1, R1b, R6, R5 or R5b. Only bits referenced as type E[error] in status field in the response can set a card status error. An error bit in the response is flagged only if corresponding bit in card status response error MMCSD_CSRE is set.</p> <p>There is no card error detection for autoCMD12 command. The host driver shall read MMCSD_RSP76 register to detect error bits in the command response.</p> <p>0 No Error<br/>0 Status bit unchanged<br/>1 Card error<br/>1 Status is cleared</p>                                                                                                                                                                                                                                                                                                                                                                                            |
| 27  | RESERVED2 | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 26  | TE        | R/W  | 0h    | <p>Tuning Error</p> <p>This bit is set when an unrecoverable error is detected in a tuning circuit except during tuning procedure [Occurrence of an error during tuning procedure is indicated by Sampling Select]. By detecting Tuning Error, Host Driver needs to abort a command executing and perform tuning. To reset tuning circuit, Sampling Clock shall be set to 0 before executing tuning procedure. The Tuning Error is higher priority than the other error interrupts generated during data transfer. By detecting Tuning Error, the Host Driver should discard data transferred by a current read/write command and retry data transfer after the Host Controller retrieved from tuning circuit error. The bit is set if the lock is lost [but not during the tuning process] or if the lock counter expires without the lock being asserted. If the latter happens, the SW can decide to ignore the interrupt and wait some more for the lock to be set.</p> <p>0 No Error<br/>1 Error</p> |
| 25  | ADMAE     | R/W  | 0h    | <p>ADMA Error:</p> <p>This bit is set when the Host Controller detects errors during ADMA based data transfer. The state of the ADMA at an error occurrence is saved in the ADMA Error Status Register. In addition, the Host Controller generates this interrupt when it detects invalid descriptor data [Valid=0] at the ST_FDS state. ADMA Error State in the ADMA Error Status indicates that an error occurs in ST_FDS state. The Host Driver may find that Valid bit is not set at the error descriptor.</p> <p>0 No Interrupt.<br/>0 Status bit unchanged<br/>1 ADMA error<br/>1 Status is cleared</p>                                                                                                                                                                                                                                                                                                                                                                                             |
| 24  | ACE       | R/W  | 0h    | <p>Auto CMD error</p> <p>Auto CMD12 and Auto CMD23 use this error status. This bit is set when detecting that one of the bits D00-D04 in Auto CMD Error Status register has changed from 0 to 1. In case of Auto CMD12, this bit is set to 1, not only when the errors in Auto CMD12 occur but also when Auto CMD12 is not executed due to the previous command error.</p> <p>0 No Error.<br/>0 Status bit unchanged<br/>1 Auto CMD error<br/>1 Status is cleared</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 23  | CLE       | R    | 0h    | <p>Reserved.</p> <p>Current limit error is not supported.</p> <p>These bits are initialized to zero, and writes to them are ignored.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

**Table 5-2635. MMC\_STAT Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 22  | DEB   | R/W  | 0h    | <p>Data End Bit error</p> <p>This bit is set automatically when detecting a 0 at the end bit position of read data on DAT line or at the end position of the CRC status in write mode.</p> <p>0 No Error<br/>0 Status bit unchanged<br/>1 Data end bit error<br/>1 Status is cleared</p>                                                                                                               |
| 21  | DCRC  | R/W  | 0h    | <p>Data CRC Error</p> <p>This bit is set automatically when there is a CRC16 error in the data phase response following a block read command or if there is a 3-bit CRC status different of a position "010" token during a block write command.</p> <p>0 No Error.<br/>0 Status bit unchanged<br/>1 Data CRC error<br/>1 Status is cleared</p>                                                        |
| 20  | DTO   | R/W  | 0h    | <p>Data timeout error</p> <p>This bit is set automatically according to the following conditions:</p> <ul style="list-style-type: none"> <li>- busy timeout for R1b, R5b response type</li> <li>- busy timeout after write CRC status</li> <li>- write CRC status timeout</li> <li>- read data timeout</li> </ul> <p>0 No error.<br/>0 Status bit unchanged<br/>1 Time out<br/>1 Status is cleared</p> |
| 19  | CIE   | R/W  | 0h    | <p>Command index error</p> <p>This bit is set automatically when response index differs from corresponding command index previously emitted. It depends on the enable in MMCSD_CMD[CICE] register.</p> <p>0 No error.<br/>0 Status bit unchanged<br/>1 Command index error<br/>1 Status is cleared</p>                                                                                                 |
| 18  | CEB   | R/W  | 0h    | <p>Command end bit error</p> <p>This bit is set automatically when detecting a 0 at the end bit position of a command response.</p> <p>0 No error.<br/>0 Status bit unchanged<br/>1 Command end bit error<br/>1 Status is cleared</p>                                                                                                                                                                  |
| 17  | CCRC  | R/W  | 0h    | <p>Command CRC Error</p> <p>This bit is set automatically when there is a CRC7 error in the command response depending on the enable in MMCSD_CMD[CCCE] register.</p> <p>0 No Error.<br/>0 Status bit unchanged<br/>1 Command CRC error<br/>1 Status is cleared</p>                                                                                                                                    |
| 16  | CTO   | R/W  | 0h    | <p>Command Timeout Error</p> <p>This bit is set automatically when no response is received within 64 clock cycles from the end bit of the command.</p> <p>For commands that reply within 5 clock cycles - the timeout is still detected at 64 clock cycles.</p> <p>0 No error<br/>0 Status bit unchanged<br/>1 Time Out<br/>1 Status is cleared</p>                                                    |

**Table 5-2635. MMC\_STAT Register Field Descriptions (continued)**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | ERRI     | R    | 0h    | <p>Error Interrupt</p> <p>If any of the bits in the Error Interrupt Status register [MMCSD_STAT[24:15]] are set, then this bit is set to 1. Therefore the host driver can efficiently test for an error by checking this bit first.</p> <p>Writes to this bit are ignored.</p> <p>0 No Interrupt.<br/>1 Error interrupt event(s) occurred</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 14:11 | RESERVED | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 10    | BSR      | R/W  | 0h    | <p>Boot status received interrupt</p> <p>This bit is set automatically when MMCSD_CON[BOOT] is set 0x1 or 0x2 and a boot status is received on DAT[0] line. This interrupt is only useful for MMC card.</p> <p>0 No Interrupt.<br/>0 Status bit unchanged<br/>1 Boot status received interrupt.<br/>1 Status is cleared</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 9     | OBI      | R/W  | 0h    | <p>Out-Of-Band interrupt</p> <p>This bit is set automatically when MMCSD_CON[OBIE] is set and an Out-of-Band interrupt occurs on OBI pin.</p> <p>The interrupt detection depends on polarity controlled by MMCSD_CON[OBIP].</p> <p>This interrupt is only useful for MMC card.</p> <p>The Out-of-Band interrupt signal is a system specific feature for future use, this signal is not required for existing specification implementation.</p> <p>0 No Out-Of-Band interrupt.<br/>0 Status bit unchanged<br/>1 Interrupt Out-Of-Band occurs<br/>1 Status is cleared</p>                                                                                                                                                                                                                                                                                       |
| 8     | CIRQ     | R    | 0h    | <p>Card interrupt</p> <p>This bit is only used for SD and SDIO and CE-ATA cards.</p> <p>In 1-bit mode, interrupt source is asynchronous [can be a source of asynchronous wakeup].</p> <p>In 4-bit mode, interrupt source is sampled during the interrupt cycle.</p> <p>In CE-ATA mode, interrupt source is detected when the card drives CMD line to zero during one cycle after data transmission end. All modes above are fully exclusive.</p> <p>The controller interrupt must be clear by setting MMCSD_IE[CIRQ] to 0, then the host driver must start the interrupt service with card [clearing card interrupt status] to remove card interrupt source. Otherwise the Controller interrupt will be reasserted as soon as MMCSD_IE[CIRQ] is set to 1.</p> <p>Writes to this bit are ignored.</p> <p>0 No card interrupt<br/>1 Generate card interrupt</p> |
| 7     | CREM     | R/W  | 0h    | <p>Card removal</p> <p>This bit is set automatically when MMCSD_PSTATE[CINS] changes from 1 to 0.</p> <p>A clear of this bit doesn't effect Card inserted present state [MMCSD_PSTATE[CINS]].</p> <p>0 Card state stable or Debouncing<br/>0 Status bit unchanged<br/>1 Card removed<br/>1 Status is cleared</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

**Table 5-2635. MMC\_STAT Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-----|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6   | CINS  | R/W  | 0h    | <p>Card insertion</p> <p>This bit is set automatically when MMCSD_PSTATE[CINS] changes from 0 to 1.</p> <p>A clear of this bit doesn't effect Card inserted present state [MMCSD_PSTATE[CINS]].</p> <p>0 Card state stable or debouncing<br/> 0 Status bit unchanged<br/> 1 Card inserted<br/> 1 Status is cleared</p>                                                                                                                                                                                                                                                                                                                                        |
| 5   | BRR   | R/W  | 0h    | <p>Buffer read ready</p> <p>This bit is set automatically during a read operation to the card [see class 2 - block oriented read commands] when one block specified by MMCSD_BLK[BLLEN] is completely written in the buffer. It indicates that the memory card has filled out the buffer and that the local host needs to empty the buffer by Reading it. Note: If the DMA receive-mode is enabled, this bit is never set; instead a DMA receive request to the main DMA controller of the system is generated.</p> <p>0 Not Ready to read buffer<br/> 0 Status bit unchanged<br/> 1 Ready to read buffer<br/> 1 Status is cleared</p>                        |
| 4   | BWR   | R/W  | 0h    | <p>Buffer write ready</p> <p>This bit is set automatically during a write operation to the card [see class 4 - block oriented write command] when the host can write a complete block as specified by MMCSD_BLK[BLLEN]. It indicates that the memory card has emptied one block from the buffer and that the local host is able to write one block of data into the buffer. Note: If the DMA transmit mode is enabled, this bit is never set; instead, a DMA transmit request to the main DMA controller of the system is generated.</p> <p>0 Not Ready to write buffer<br/> 0 Status bit unchanged<br/> 1 Ready to write buffer<br/> 1 Status is cleared</p> |
| 3   | DMA   | R/W  | 0h    | <p>DMA interrupt :</p> <p>This status is set when an interrupt is required in the ADMA instruction and after the data transfer completion.</p> <p>0 Dma interrupt detected<br/> 0 Status bit unchanged<br/> 1 No dma interrupt<br/> 1 Status is cleared</p>                                                                                                                                                                                                                                                                                                                                                                                                   |
| 2   | BGE   | R/W  | 0h    | <p>Block gap event</p> <p>When a stop at block gap is requested [MMCSD_HCTL[SBGR]], this bit is automatically set when transaction is stopped at the block gap during a read or write operation.</p> <p>This event does not occur when the stop at block gap is requested on the last block.</p> <p>In read mode, a 1-to-0 transition of the DAT Line active status [MMCSD_PSTATE[DLA]] between data blocks generates a Block gap event interrupt.</p> <p>0 No block gap event<br/> 0 Status bit unchanged<br/> 1 Transaction stopped at block gap<br/> 1 Status is cleared</p>                                                                               |

**Table 5-2635. MMC\_STAT Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | TC    | R/W  | 0h    | <p>Transfer completed</p> <p>This bit is always set when a read/write transfer is completed or between two blocks when the transfer is stopped due to a stop at block gap request [MMCSD_HCTL[SBGR]].</p> <p>In Read mode:<br/>This bit is automatically set on completion of a read transfer [MMCSD_PSTATE[RTA]].</p> <p>In write mode:<br/>This bit is set automatically on completion of the DAT line use [MMCSD_PSTATE[DLA]].</p> <p>0      No transfer complete<br/>0      Status bit unchanged<br/>1      Data transfer complete<br/>1      Status is cleared</p>                                                                                                             |
| 0   | CC    | R/W  | 0h    | <p>Command complete</p> <p>This bit is set when a 1-to-0 transition occurs in the register command inhibit [MMCSD_PSTATE[CMDI]].</p> <p>If the command is a type for which no response is expected, then the command complete interrupt is generated at the end of the command.</p> <p>A command timeout error [MMCSD_STAT[CTO]] has higher priority than command complete [MMCSD_STAT[CC]].</p> <p>If a response is expected but none is received, then a command timeout error is detected and signaled instead of the command complete interrupt.</p> <p>0      No Command complete<br/>0      Status bit unchanged<br/>1      Command complete<br/>1      Status is cleared</p> |

### 5.15.2.22 MMC\_IE Register

#### 1 MMC\_IE Register (Offset = 234h) [reset = 0h]

Interrupt Status Enable Register

This register allows to enable/disable the module to set status bits, on an event-by-event basis.

MMCHS\_IE[31:16] = Error Interrupt Status Enable

MMCHS\_IE[15:0] = Normal Interrupt Status Enable.

Return to [Summary Table](#)

**Table 5-2636. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCS0         | 4830 0234h       |

**Figure 5-871. MMC\_IE Name Register**

| 31          | 30          | 29          | 28          | 27         | 26         | 25           | 24          |
|-------------|-------------|-------------|-------------|------------|------------|--------------|-------------|
| RESERVED3   |             | BADA_ENABLE | CERR_ENABLE | RESERVED2  | TE_ENABLE  | ADMAE_ENABLE | ACE_ENABLE  |
| R           |             | R/W         | R/W         | R          | R/W        | R/W          | R/W         |
| 0h          |             | 0h          | 0h          | 0h         | 0h         | 0h           | 0h          |
| 23          | 22          | 21          | 20          | 19         | 18         | 17           | 16          |
| CLE         | DEB_ENABLE  | DCRC_ENABLE | DTO_ENABLE  | CIE_ENABLE | CEB_ENABLE | CCRC_ENABLE  | CTO_ENABLE  |
| R           | R/W         | R/W         | R/W         | R/W        | R/W        | R/W          | R/W         |
| 0h          | 0h          | 0h          | 0h          | 0h         | 0h         | 0h           | 0h          |
| 15          | 14          | 13          | 12          | 11         | 10         | 9            | 8           |
| NULL        | RESERVED    |             |             |            | BSR_ENABLE | OBI_ENABLE   | CIRQ_ENABLE |
| R           | R           |             |             |            | R/W        | R/W          | R/W         |
| 0h          | 0h          |             |             |            | 0h         | 0h           | 0h          |
| 7           | 6           | 5           | 4           | 3          | 2          | 1            | 0           |
| CREM_ENABLE | CINS_ENABLE | BRR_ENABLE  | BWR_ENABLE  | DMA_ENABLE | BGE_ENABLE | TC_ENABLE    | CC_ENABLE   |
| R/W         | R/W         | R/W         | R/W         | R/W        | R/W        | R/W          | R/W         |
| 0h          | 0h          | 0h          | 0h          | 0h         | 0h         | 0h           | 0h          |

**Table 5-2638. MMC\_IE Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                     |
|-------|--------------|------|-------|-----------------------------------------------------------------|
| 31:30 | RESERVED3    | R    | 0h    |                                                                 |
| 29    | BADA_ENABLE  | R/W  | 0h    | Bad access to data space Status Enable<br>0 Masked<br>1 Enabled |
| 28    | CERR_ENABLE  | R/W  | 0h    | Card Error Status Enable<br>0 Masked<br>1 Enabled               |
| 27    | RESERVED2    | R    | 0h    |                                                                 |
| 26    | TE_ENABLE    | R/W  | 0h    | Tuning Error Status Enable<br>0 Masked<br>1 Enabled             |
| 25    | ADMAE_ENABLE | R/W  | 0h    | ADMA Error Status Enable<br>0 Masked<br>1 Enabled               |

**Table 5-2638. MMC\_IE Register Field Descriptions (continued)**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                         |
|-------|-------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24    | ACE_ENABLE  | R/W  | 0h    | Auto CMD Error Status Enable<br>0 Masked<br>1 Enabled                                                                                                                                                                                                                               |
| 23    | CLE         | R    | 0h    | Reserved bit.<br>Current limit error is not supported.<br>These bits are initialized to zero, and writes to them are ignored.                                                                                                                                                       |
| 22    | DEB_ENABLE  | R/W  | 0h    | Data End Bit Error Status Enable<br>0 Masked<br>1 Enabled                                                                                                                                                                                                                           |
| 21    | DCRC_ENABLE | R/W  | 0h    | Data CRC Error Status Enable<br>0 Masked<br>1 Enabled                                                                                                                                                                                                                               |
| 20    | DTO_ENABLE  | R/W  | 0h    | Data Timeout Error Status Enable<br>0 The data timeout detection is deactivated. The host controller provides the clock to the card until the card sends the data or the transfer is aborted.<br>1 The data timeout detection is enabled.                                           |
| 19    | CIE_ENABLE  | R/W  | 0h    | Command Index Error Status Enable<br>0 Masked<br>1 Enabled                                                                                                                                                                                                                          |
| 18    | CEB_ENABLE  | R/W  | 0h    | Command End Bit Error Status Enable<br>0 Masked<br>1 Enabled                                                                                                                                                                                                                        |
| 17    | CCRC_ENABLE | R/W  | 0h    | Command CRC Error Status Enable<br>0 Masked<br>1 Enabled                                                                                                                                                                                                                            |
| 16    | CTO_ENABLE  | R/W  | 0h    | Command Timeout Error Status Enable<br>0 Masked<br>1 Enabled                                                                                                                                                                                                                        |
| 15    | NULL        | R    | 0h    | Fixed to 0<br>The host driver shall control error interrupts using the Error Interrupt Signal Enable register.<br>Writes to this bit are ignored                                                                                                                                    |
| 14:11 | RESERVED    | R    | 0h    |                                                                                                                                                                                                                                                                                     |
| 10    | BSR_ENABLE  | R/W  | 0h    | Boot Status Enable<br>A write to this register when MMCSD_CON[BOOT_ACK] is set to 0x0 is ignored.<br>0 Masked<br>1 Enabled                                                                                                                                                          |
| 9     | OBI_ENABLE  | R/W  | 0h    | Out-of-Band Status Enable<br>A write to this register when MMCSD_CON[OBIE] is set to '0' is ignored.<br>0 Masked<br>1 Enabled                                                                                                                                                       |
| 8     | CIRQ_ENABLE | R/W  | 0h    | Card Status Enable<br>A clear of this bit also clears the corresponding status bit.<br>During 1-bit mode, if the interrupt routine doesn't remove the source of a card interrupt in the SDIO card, the status bit is reasserted when this bit is set to 1.<br>0 Masked<br>1 Enabled |

**Table 5-2638. MMC\_IE Register Field Descriptions (continued)**

| Bit | Field       | Type | Reset | Description                                               |
|-----|-------------|------|-------|-----------------------------------------------------------|
| 7   | CREM_ENABLE | R/W  | 0h    | Card Removal Status Enable<br>0 Masked<br>1 Enabled       |
| 6   | CINS_ENABLE | R/W  | 0h    | Card Insertion Status Enable<br>0 Masked<br>1 Enabled     |
| 5   | BRR_ENABLE  | R/W  | 0h    | Buffer Read Ready Status Enable<br>0 Masked<br>1 Enabled  |
| 4   | BWR_ENABLE  | R/W  | 0h    | Buffer Write Ready Status Enable<br>0 Masked<br>1 Enabled |
| 3   | DMA_ENABLE  | R/W  | 0h    | DMA Status Enable<br>0 Masked<br>1 Enabled                |
| 2   | BGE_ENABLE  | R/W  | 0h    | Block Gap Event Status Enable<br>0 Masked<br>1 Enabled    |
| 1   | TC_ENABLE   | R/W  | 0h    | Transfer Complete Status Enable<br>0 Masked<br>1 Enabled  |
| 0   | CC_ENABLE   | R/W  | 0h    | Command Complete Status Enable<br>0 Masked<br>1 Enabled   |



### 5.15.2.23 MMC\_ISE Register

#### 1 MMC\_ISE Register (Offset = 238h) [reset = 0h]

Interrupt Signal Enable Register

This register allows to enable/disable the module internal sources of status, on an event-by-event basis.

MMCHS\_ISE[31:16] = Error Interrupt Signal Enable

MMCHS\_ISE[15:0] = Normal Interrupt Signal Enable.

Return to [Summary Table](#)

**Table 5-2639. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCS0         | 4830 0238h       |

**Figure 5-872. MMC\_ISE Name Register**

| 31         | 30         | 29         | 28        | 27        | 26          | 25         | 24         |
|------------|------------|------------|-----------|-----------|-------------|------------|------------|
| RESERVED3  | BADA_SIGEN | CERR_SIGEN | RESERVED2 | TE_SIGEN  | ADMAE_SIGEN | ACE_SIGEN  |            |
| R          | R/W        | R/W        | R         | R/W       | R/W         | R/W        | R/W        |
| 0h         | 0h         | 0h         | 0h        | 0h        | 0h          | 0h         | 0h         |
| 23         | 22         | 21         | 20        | 19        | 18          | 17         | 16         |
| CLE        | DEB_SIGEN  | DCRC_SIGEN | DTO_SIGEN | CIE_SIGEN | CEB_SIGEN   | CCRC_SIGEN | CTO_SIGEN  |
| R          | R/W        | R/W        | R/W       | R/W       | R/W         | R/W        | R/W        |
| 0h         | 0h         | 0h         | 0h        | 0h        | 0h          | 0h         | 0h         |
| 15         | 14         | 13         | 12        | 11        | 10          | 9          | 8          |
| NULL       | RESERVED   |            |           |           | BSR_SIGEN   | OBI_SIGEN  | CIRQ_SIGEN |
| R          | R          |            |           |           | R/W         | R/W        | R/W        |
| 0h         | 0h         |            |           |           | 0h          | 0h         | 0h         |
| 7          | 6          | 5          | 4         | 3         | 2           | 1          | 0          |
| CREM_SIGEN | CINS_SIGEN | BRR_SIGEN  | BWR_SIGEN | DMA_SIGEN | BGE_SIGEN   | TC_SIGEN   | CC_SIGEN   |
| R/W        | R/W        | R/W        | R/W       | R/W       | R/W         | R/W        | R/W        |
| 0h         | 0h         | 0h         | 0h        | 0h        | 0h          | 0h         | 0h         |

**Table 5-2641. MMC\_ISE Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                     |
|-------|-------------|------|-------|-----------------------------------------------------------------|
| 31:30 | RESERVED3   | R    | 0h    |                                                                 |
| 29    | BADA_SIGEN  | R/W  | 0h    | Bad access to data space Signal Enable<br>0 Masked<br>1 Enabled |
| 28    | CERR_SIGEN  | R/W  | 0h    | Card Error Interrupt Signal Enable<br>0 Masked<br>1 Enabled     |
| 27    | RESERVED2   | R    | 0h    |                                                                 |
| 26    | TE_SIGEN    | R/W  | 0h    | Tuning Error Signal Enable<br>0 Masked<br>1 Enabled             |
| 25    | ADMAE_SIGEN | R/W  | 0h    | ADMA Error Signal Enable<br>0 Masked<br>1 Enabled               |
| 24    | ACE_SIGEN   | R/W  | 0h    | Auto CMD Error Signal Enable<br>0 Masked<br>1 Enabled           |

**Table 5-2641. MMC\_ISE Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                      |
|-------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 23    | CLE        | R    | 0h    | Reserved bit.<br>Current limit error is not supported.<br>These bits are initialized to zero, and writes to them are ignored.                    |
| 22    | DEB_SIGEN  | R/W  | 0h    | Data End Bit Error Signal Enable<br>0 Masked<br>1 Enabled                                                                                        |
| 21    | DCRC_SIGEN | R/W  | 0h    | Data CRC Error Signal Enable<br>0 Masked<br>1 Enabled                                                                                            |
| 20    | DTO_SIGEN  | R/W  | 0h    | Data Timeout Error Signal Enable<br>0 Masked<br>1 Enabled                                                                                        |
| 19    | CIE_SIGEN  | R/W  | 0h    | Command Index Error Signal Enable<br>0 Masked<br>1 Enabled                                                                                       |
| 18    | CEB_SIGEN  | R/W  | 0h    | Command End Bit Error Signal Enable<br>0 Masked<br>1 Enabled                                                                                     |
| 17    | CCRC_SIGEN | R/W  | 0h    | Command CRC Error Signal Enable<br>0 Masked<br>1 Enabled                                                                                         |
| 16    | CTO_SIGEN  | R/W  | 0h    | Command timeout Error Signal Enable<br>0 Masked<br>1 Enabled                                                                                     |
| 15    | NULL       | R    | 0h    | Fixed to 0<br>The host driver shall control error interrupts using the Error Interrupt Signal Enable register.<br>Writes to this bit are ignored |
| 14:11 | RESERVED   | R    | 0h    |                                                                                                                                                  |
| 10    | BSR_SIGEN  | R/W  | 0h    | Boot Status Signal Enable<br>A write to this register when MMCSD_CON[BOOT_ACK] is set to 0x0 is ignored.<br>0 Masked<br>1 Enabled                |
| 9     | OBI_SIGEN  | R/W  | 0h    | Out-Of-Band Interrupt Signal Enable<br>A write to this register when MMCSD_CON[OBIE] is set to '0' is ignored.<br>0 Masked<br>1 Enabled          |
| 8     | CIRQ_SIGEN | R/W  | 0h    | Card Interrupt Signal Enable<br>0 Masked<br>1 Enabled                                                                                            |
| 7     | CREM_SIGEN | R/W  | 0h    | Card Removal Signal Enable<br>0 Masked<br>1 Enabled                                                                                              |
| 6     | CINS_SIGEN | R/W  | 0h    | Card Insertion Signal Enable<br>0 Masked<br>1 Enabled                                                                                            |
| 5     | BRR_SIGEN  | R/W  | 0h    | Buffer Read Ready Signal Enable<br>0 Masked<br>1 Enabled                                                                                         |

**Table 5-2641. MMC\_ISE Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description                                               |
|-----|-----------|------|-------|-----------------------------------------------------------|
| 4   | BWR_SIGEN | R/W  | 0h    | Buffer Write Ready Signal Enable<br>0 Masked<br>1 Enabled |
| 3   | DMA_SIGEN | R/W  | 0h    | DMA Interrupt Signal Enable<br>0 Masked<br>1 Enabled      |
| 2   | BGE_SIGEN | R/W  | 0h    | Black Gap Event Signal Enable<br>0 Masked<br>1 Enabled    |
| 1   | TC_SIGEN  | R/W  | 0h    | Transfer Completed Status Enable<br>0 Masked<br>1 Enabled |
| 0   | CC_SIGEN  | R/W  | 0h    | Command Complete Status Enable<br>0 Masked<br>1 Enabled   |

### 5.15.2.24 MMC\_AC12 Register

#### 1 MMC\_AC12 Register (Offset = 23Ch) [reset = 0h]

Host Control 2 Register and Auto CMD Error Status Register

This register is used to indicate CMD12 response error of Auto CMD12 and CMD23 response error of Auto CMD23. The Host driver can determine what kind of Auto CMD12 / CMD23 errors occur by this register. Auto CMD23 errors are indicated in bit 04-01. This register is valid only when the Auto CMD Error is set.

Return to [Summary Table](#)

**Table 5-2642. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCS0         | 4830 023Ch       |

**Figure 5-873. MMC\_AC12 Name Register**

| 31        | 30        | 29        | 28         | 27    | 26   | 25   | 24   |
|-----------|-----------|-----------|------------|-------|------|------|------|
| PV_ENABLE | AI_ENABLE | RESERVED2 |            |       |      |      |      |
| R/W       | R/W       | R         |            |       |      |      |      |
| 0h        | 0h        | 0h        |            |       |      |      |      |
| 23        | 22        | 21        | 20         | 19    | 18   | 17   | 16   |
| SCLK_SEL  | ET        | DS_SEL    | V1V8_SIGEN | UHSMS |      |      |      |
| R/W       | R/W       | R/W       | R/W        | R/W   |      |      |      |
| 0h        | 0h        | 0h        | 0h         | 0h    |      |      |      |
| 15        | 14        | 13        | 12         | 11    | 10   | 9    | 8    |
| RESERVED1 |           |           |            |       |      |      |      |
| R         |           |           |            |       |      |      |      |
| 0h        |           |           |            |       |      |      |      |
| 7         | 6         | 5         | 4          | 3     | 2    | 1    | 0    |
| CNI       | RESERVED  |           | ACIE       | ACEB  | ACCE | ACTO | ACNE |
| R         | R         |           | R          | R     | R    | R    | R    |
| 0h        | 0h        |           | 0h         | 0h    | 0h   | 0h   | 0h   |

**Table 5-2644. MMC\_AC12 Register Field Descriptions**

| Bit | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31  | PV_ENABLE | R/W  | 0h    | <p>Preset Value Enable</p> <p>Host Controller Version 3.00 supports this bit.</p> <p>As the operating SDCLK frequency and I/O driver strength depend on the Host System implementation, it is difficult to determine these parameters in the Standard Host Driver. When Preset Value Enable is set, automatic SDCLK frequency generation and driver strength selection is performed without considering system specific conditions. This bit enables the functions defined in the Preset Value registers.</p> <p>If this bit is set to 0, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Driver.</p> <p>If this bit is set to 1, SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select in Host Control 2 register are set by Host Controller as specified in the Preset Value registers.</p> <p>0 SDCLK and Driver Strength are controlled by Host Driver.</p> <p>1 Automatic Selection by Preset value are Enabled.</p> |

**Table 5-2644. MMC\_AC12 Register Field Descriptions (continued)**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 30    | AI_ENABLE | R/W  | 0h    | <p>Asynchronous Interrupt Enable</p> <p>This bit can be set to 1 if a card supports asynchronous interrupts and Asynchronous Interrupt Support is set to 1 in the Capabilities register. Asynchronous interrupt is effective when DAT[1] interrupt is used in 4-bit SD mode [and zero is set to Interrupt Pin Select in the Shared Bus Control register]. If this bit is set to 1, the Host Driver can stop the SDCLK during asynchronous interrupt period to save power. During this period, the Host Controller continues to deliver the Card Interrupt to the host when it is asserted by the Card.</p> <p>0 Disabled<br/>1 Enabled</p>                                                                                                                                                                                                                                                        |
| 29:24 | RESERVED2 | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 23    | SCLK_SEL  | R/W  | 0h    | <p>Sampling Clock Select</p> <p>Host Controller uses this bit to select sampling clock to receive CMD and DAT. This bit is set by tuning procedure and valid after the completion of tuning [when Execute Tuning is cleared]. Setting 1 means that tuning is completed successfully and setting 0 means that tuning is failed. Writing 1 to this bit is meaningless and ignored. A tuning circuit is reset by Writing to 0. This bit can be cleared with setting Execute Tuning. Once the tuning circuit is reset, it will take time to complete tuning sequence. Therefore, Host Driver should keep this bit to 1 to perform re-tuning sequence to complete re-tuning sequence in a short time. Change of this bit is not allowed while the Host Controller is receiving response or a read data block.</p> <p>0 Fixed clock is used to sample data<br/>1 Tuned clock is used to sample data</p> |
| 22    | ET        | R/W  | 0h    | <p>Execute Tuning</p> <p>This bit is set to 1 to start tuning procedure and automatically cleared when tuning procedure is completed. The result of tuning is indicated to Sampling Clock Select. Tuning procedure is aborted by Writing 0. This is Read-Write with automatic clear register</p> <p>0 Not Tuned or Tuning Completed<br/>1 Execute Tuning</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 21:20 | DS_SEL    | R/W  | 0h    | <p>Driver Strength Select</p> <p>Host Controller output driver in 1.8V signaling is selected by this bit. In 3.3V signaling, this field is not effective. This field can be set depends on Driver Type A, C and D support bits in the Capabilities register.</p> <p>This bit depends on setting of Preset Value Enable.<br/>If Preset Value Enable = 0, this field is set by Host Driver.<br/>If Preset Value Enable = 1, this field is automatically set by a value specified in the one of Preset Value registers.</p> <p>0 Driver Type B is selected (Default)<br/>1 Driver Type A is selected<br/>2 Driver Type C is selected<br/>3 Driver Type D is selected</p>                                                                                                                                                                                                                             |

**Table 5-2644. MMC\_AC12 Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19    | V1V8_SIGEN | R/W  | 0h    | <p>1.8V Signaling Enable</p> <p>This bit controls voltage regulator for I/O cell. 3.3V is supplied to the card regardless of signaling voltage.</p> <p>Setting this bit from 0 to 1 starts changing signal voltage from 3.3V to 1.8V. 1.8V regulator output shall be stable within 5ms. Host Controller clears this bit if switching to 1.8V signaling fails.</p> <p>Clearing this bit from 1 to 0 starts changing signal voltage from 1.8V to 3.3V. 3.3V regulator output shall be stable within 5ms.</p> <p>Host Driver can set this bit to 1 when Host Controller supports 1.8V signaling [One of support bits is set to 1:SDR50, SDR104 or DDR50 in the Capabilities register] and the card or device supports UHS-I [S18A=1. Refer to Bus Signal Voltage Switch Sequence in the Physical Layer Specification Version 3.0x].</p> <p>0      3.3v signaling<br/>1      1.8v Signaling</p>                                                                                                                            |
| 18:16 | UHSMS      | R/W  | 0h    | <p>UHS Mode Select</p> <p>This field is used to select one of UHS-I modes and effective when 1.8V Signaling Enable is set to 1.</p> <p>If Preset Value Enable in the Host Control 2 register is set to 1, Host Controller sets SDCLK Frequency Select, Clock Generator Select in the Clock Control register and Driver Strength Select according to Preset Value registers. In this case, one of preset value registers is selected by this field. Host Driver needs to reset SD Clock Enable before changing this field to avoid generating clock glitch. After setting this field, Host Driver sets SD Clock Enable again.</p> <p>When SDR50, SDR104 or DDR50 is selected for SDIO card, interrupt detection at the block gap shall not be used. Read Wait timing is changed for these modes. Refer to the SDIO Specification Version 3.00 for more detail.</p> <p>0      SDR12<br/>1      SDR25<br/>2      SDR50<br/>3      SDR104<br/>4      DDR50<br/>5      Reserved<br/>6      Reserved<br/>7      Reserved</p> |
| 15:8  | RESERVED1  | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 7     | CNI        | R    | 0h    | <p>Command Not Issued By Auto CMD12 Error</p> <p>Setting this bit to 1 means CMD_wo_DAT is not executed due to an Auto CMD12 Error [D04-D01] in this register.</p> <p>This bit is set to 0 when Auto CMD Error is generated by Auto CMD23.</p> <p>0      Not error<br/>1      Command not issued</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 6:5   | RESERVED   | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 4     | ACIE       | R    | 0h    | <p>Auto CMD Index Error</p> <p>This bit is set if the Command Index error occurs in response to a command.</p> <p>0      No error<br/>1      Error</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 3     | ACEB       | R    | 0h    | <p>Auto CMD End Bit Error</p> <p>This bit is set when detecting that the end bit of command response is 0.</p> <p>0      No error<br/>1      End bit Error Generated</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |

**Table 5-2644. MMC\_AC12 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-----|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | ACCE  | R    | 0h    | <p>Auto CMD CRC Error<br/>This bit is set when detecting a CRC error in the command response.</p> <p>0        No error<br/>1        CRC Error Generated</p>                                                                                                                                                                                                                                                                                                                                                                                              |
| 1   | ACTO  | R    | 0h    | <p>Auto CMD Timeout Error<br/>This bit is set if no response is returned within 64 SDCLK cycles from the end bit of command.<br/>If this bit is set to 1, the other error status bits [D04-D02] are meaningless.</p> <p>0        No error<br/>1        Auto CMD Time Out</p>                                                                                                                                                                                                                                                                             |
| 0   | ACNE  | R    | 0h    | <p>Auto CMD12 Not Executed<br/>If memory multiple block data transfer is not started due to command error, this bit is not set because it is not necessary to issue Auto CMD12. Setting this bit to 1 means the Host Controller cannot issue Auto CMD12 to stop memory multiple block data transfer due to some error. If this bit is set to 1, other error status bits [D04-D01] are meaningless.<br/>This bit is set to 0 when Auto CMD Error is generated by Auto CMD23.</p> <p>0        Auto CMD12 Executed<br/>1        Auto CMD12 Not Executed</p> |

### 5.15.2.25 MMC\_CAPA Register

#### 1 MMC\_CAPA Register (Offset = 240h) [reset = E10080h]

Capabilities Register

This register lists the capabilities of the MMC/SD/SDIO host controller.

Return to [Summary Table](#)

**Table 5-2645. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCSD0        | 4830 0240h       |

**Figure 5-874. MMC\_CAPA Name Register**

|           |          |     |           |           |           |      |      |
|-----------|----------|-----|-----------|-----------|-----------|------|------|
| 31        | 30       | 29  | 28        | 27        | 26        | 25   | 24   |
| RESERVED4 |          | AIS | BIT64     | RESERVED3 | VS18      | VS30 | VS33 |
| R         |          | R   | R         | R         | R/W       | R/W  | R/W  |
| 0h        |          | 0h  | 0h        | 0h        | 0h        | 0h   | 0h   |
| 23        | 22       | 21  | 20        | 19        | 18        | 17   | 16   |
| SRS       | DS       | HSS | RESERVED2 | AD2S      | RESERVED1 | MBL  |      |
| R         | R        | R   | R         | R         | R         | R    |      |
| 1h        | 1h       | 1h  | 0h        | 0h        | 0h        | 1h   |      |
| 15        | 14       | 13  | 12        | 11        | 10        | 9    | 8    |
| BCF       |          |     |           |           |           |      |      |
| R         |          |     |           |           |           |      |      |
| 0h        |          |     |           |           |           |      |      |
| 7         | 6        | 5   | 4         | 3         | 2         | 1    | 0    |
| TCU       | RESERVED |     |           |           | TCF       |      |      |
| R         | R        |     |           |           | R         |      |      |
| 1h        | 0h       |     |           |           | 0h        |      |      |

**Table 5-2647. MMC\_CAPA Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                    |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | RESERVED4 | R    | 0h    |                                                                                                                                                                                                                                                |
| 29    | AIS       | R    | 0h    | Asynchronous Interrupt Support<br>Refer to SDIO Specification Version 3.00 about asynchronous interrupt.<br><br>0 Asynchronous Interrupt Not Supported<br>1 Asynchronous Interrupt Supported                                                   |
| 28    | BIT64     | R    | 0h    | 64 Bit System Bus Support<br>Setting 1 to this bit indicates that the Host Controller supports 64-bit address descriptor mode and is connected to 64-bit address system bus.<br><br>0 32 bit system bus address<br>1 64 bit system bus address |
| 27    | RESERVED3 | R    | 0h    |                                                                                                                                                                                                                                                |



**Table 5-2647. MMC\_CAPA Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                |
|-----|-----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 26  | VS18      | R/W  | 0h    | <p>Voltage support 1.8V</p> <p>Initialization of this register [via a write access to this register] depends on the system capabilities. The host driver shall not modify this register after the initialization.</p> <p>This register is only reinitialized by a hard reset [via RESETN signal]</p> <p>0      1.8V Not supported<br/> 0      1.8V Not Supported<br/> 1      1.8V Supported<br/> 1      1.8V Supported</p> |
| 25  | VS30      | R/W  | 0h    | <p>Voltage support 3.0V</p> <p>Initialization of this register [via a write access to this register] depends on the system capabilities. The host driver shall not modify this register after the initialization.</p> <p>This register is only reinitialized by a hard reset [via RESETN signal]</p> <p>0      3.0V Not supported<br/> 0      3.0V Not Supported<br/> 1      3.0V Supported<br/> 1      3.0V Supported</p> |
| 24  | VS33      | R/W  | 0h    | <p>Voltage support 3.3V</p> <p>Initialization of this register [via a write access to this register] depends on the system capabilities. The host driver shall not modify this register after the initialization.</p> <p>This register is only reinitialized by a hard reset [via RESETN signal]</p> <p>0      3.3V Not supported<br/> 0      3.3V Not Supported<br/> 1      3.3V Supported<br/> 1      3.3V Supported</p> |
| 23  | SRS       | R    | 1h    | <p>Suspend/Resume support [SDIO cards only]</p> <p>This bit indicates whether the host controller supports Suspend/Resume functionality.</p> <p>0      The Host controller does not Suspend/Resume functionality.<br/> 1      The Host controller supports Suspend/Resume functionality.</p>                                                                                                                               |
| 22  | DS        | R    | 1h    | <p>DMA support</p> <p>This bit indicates that the Host Controller is able to use DMA to transfer data between system memory and the Host Controller directly.</p> <p>0      DMA Not Supported<br/> 1      DMA Supported</p>                                                                                                                                                                                                |
| 21  | HSS       | R    | 1h    | <p>High speed support</p> <p>This bit indicates that the host controller supports high speed operations and can supply an up-to maximum card frequency.</p> <p>0      High Speed Not Supported<br/> 1      High Speed Supported</p>                                                                                                                                                                                        |
| 20  | RESERVED2 | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 19  | AD2S      | R    | 0h    | <p>ADMA2 Support</p> <p>This bit indicates whether the Host Controller is capable of using ADMA2. It depends on setting of generic parameter MADMA_EN</p> <p>0      ADMA2 not Supported<br/> 1      ADMA2 Supported</p>                                                                                                                                                                                                    |
| 18  | RESERVED1 | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                            |

**Table 5-2647. MMC\_CAPA Register Field Descriptions (continued)**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|-------|----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 17:16 | MBL      | R    | 1h    | <p>Maximum block length</p> <p>This value indicates the maximum block size that the host driver can read and write to the buffer in the host controller.</p> <p>This value depends on definition of generic parameter with a max value of 2048bytes.</p> <p>The host controller supports 512 bytes and 1024bytes block transfers.</p> <p>0      512 bytes<br/>1      1024 bytes<br/>2      2048 bytes</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 15:8  | BCF      | R    | 0h    | <p>Base Clock Frequency For SD Clock</p> <p>This value indicates the base [maximum] clock frequency for the SD Clock.</p> <p>8-bit Base Clock Frequency</p> <p>This mode is supported by the Host Controller Version 3.00.</p> <p>Unit values are 1MHz. The supported clock range is 10MHz to 255MHz.</p> <p>FFh : 255MHz<br/>... : .....<br/>02h: 2MHz<br/>01h: 1MHz<br/>00h: Get information via another method</p> <p>If the real frequency is 16.5MHz, the lager value shall be set 00010001b [17MHz] because the Host Driver use this value to calculate the clock divider value [Refer to the SDCLK Frequency Select in the Clock Control register.] and it shall not exceed upper limit of the SD Clock frequency.</p> <p>If these bits are all 0, the Host System has to get information via another method.</p> <p>0      The value indicating the base (maximum) frequency for the output clock provided to the card is system dependent and is not available in this register. Get the information via another method.</p> |
| 7     | TCU      | R    | 1h    | <p>Timeout clock unit</p> <p>This bit shows the unit of base clock frequency used to detect Data Timeout Error [MMCSD_STAT[DTO]].</p> <p>0      KHZ<br/>1      MHZ</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 6     | RESERVED | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 5:0   | TCF      | R    | 0h    | <p>Timeout clock frequency</p> <p>The timeout clock frequency is used to detect Data Timeout Error [MMCSD_STAT[DTO]].</p> <p>0      The timeout clock frequency depends on the frequency of the clock provided to the card. The value of the timeout clock frequency is not available in this register.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

### 5.15.2.26 MMC\_CAPA2 Register

#### 1 MMC\_CAPA2 Register (Offset = 244h) [reset = 0h]

##### Capabilities 2 Register

This register provides the Host Driver with information specific to the Host Controller implementation. The Host Controller may implement these values as fixed or loaded from flash memory during power on initialization. Refer to Software Reset For All in the Software Reset register for loading from flash memory and completion timing control.

Return to [Summary Table](#)

**Table 5-2648. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCS0         | 4830 0244h       |

**Figure 5-875. MMC\_CAPA2 Name Register**

|           |     |        |           |          |       |        |       |
|-----------|-----|--------|-----------|----------|-------|--------|-------|
| 31        | 30  | 29     | 28        | 27       | 26    | 25     | 24    |
| RESERVED3 |     |        |           |          |       |        |       |
| R         |     |        |           |          |       |        |       |
| 0h        |     |        |           |          |       |        |       |
| 23        | 22  | 21     | 20        | 19       | 18    | 17     | 16    |
| CM        |     |        |           |          |       |        |       |
| R         |     |        |           |          |       |        |       |
| 0h        |     |        |           |          |       |        |       |
| 15        | 14  | 13     | 12        | 11       | 10    | 9      | 8     |
| RTM       |     | TSDR50 | RESERVED2 | TCRT     |       |        |       |
| R         |     | R      | R         | R        |       |        |       |
| 0h        |     | 0h     | 0h        | 0h       |       |        |       |
| 7         | 6   | 5      | 4         | 3        | 2     | 1      | 0     |
| RESERVED1 | DTD | DTC    | DTA       | RESERVED | DDR50 | SDR104 | SDR50 |
| R         | R   | R      | R         | R        | R     | R      | R     |
| 0h        | 0h  | 0h     | 0h        | 0h       | 0h    | 0h     | 0h    |

**Table 5-2650. MMC\_CAPA2 Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED3 | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                   |
| 23:16 | CM        | R    | 0h    | Clock Multiplier<br>This field indicates clock multiplier value of programmable clock generator. Refer to Clock Control register. Setting 00h means that Host Controller does not support programmable clock generator.<br>00h: Clock Multiplier is Not Supported<br>01h: Clock Multiplier M = 2<br>02h: Clock Multiplier M = 3<br>.... : .....<br>FFh : Clock Multiplier M = 256 |

**Table 5-2650. MMC\_CAPA2 Register Field Descriptions (continued)**

| Bit   | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|--------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | RTM    | R    | 0h    | <p><b>Re-Tuning Modes</b><br/>This field selects re-tuning method and limits the maximum data length.</p> <p><b>Bit47-46 Re-Tuning Mode Re-Tuning Method Data Length</b><br/>There are two re-tuning timings: Re-Tuning Request controlled by the Host Controller and expiration of a Re-Tuning Timer controlled by the Host Driver. By receiving either timing, the Host Driver executes the re-tuning procedure just before a next command issue. The maximum data length per read/write command is restricted so that re-tuning procedures can be inserted during data transfers.</p> <p><b>[1] Re-Tuning Mode 1</b><br/>The host controller does not have any internal logic to detect when the re-tuning needs to be performed. In this case, the Host Driver should maintain all re-tuning timings by using a Re-Tuning Timer. To enable inserting the re-tuning procedure during data transfers, the data length per read/write command shall be limited up to 4MB.</p> <p><b>[2] Re-Tuning Mode 2</b><br/>The host controller has the capability to indicate the re-tuning timing by Re-Tuning Request during data transfers. Then the data length per read/write command shall be limited up to 4MB. During non data transfer, re-tuning timing is determined by either Re-Tuning Request or Re-Tuning Timer. If Re-Tuning Request is used, Re-Tuning Timer should be disabled.</p> <p><b>[3] Re-Tuning Mode 3</b><br/>The host controller has the capability to take care of the re-tuning during data transfer [Auto Re-Tuning]. Re-Tuning Request shall not be generated during data transfers and there is no limitation to data length per read/write command. During non data transfer, re-tuning timing is determined by either Re-Tuning Request or Re-Tuning Timer. If Re-Tuning Request is used, Re-Tuning Timer should be disabled.</p> <p><b>Re-Tuning Timer Control Example for Re-Tuning Mode 1</b><br/>The initial value of re-tuning timer is provided by Timer Count for Re-Tuning field in this register. The timer starts counting by loading the initial value. When the timer expires, the Host Driver marks an expiration flag. On receiving a command request, the Host driver checks the expiration flag. If the expiration flag is set, then the Host Driver should perform the re-tuning procedure before issuing a command. If the expiration flag is not set, then the Host Driver issues a command without performing the re-tuning procedure. Every time the re-tuning procedure is performed, the timer loads the new initial value and the expiration flag is cleared.</p> <p><b>Re-Tuning Timer Control Example for Re-Tuning Mode 2 and Mode 3</b><br/>The timer control is almost the same as Re-Tuning Mode 1 except the timer loads the new initial value after data transfer [when receiving Transfer Complete]. In case of Mode 3, Timer Count for Re-Tuning is set either smaller value: Tuning effective time after re-tuning procedure or after data transfer. If a Host System goes into power down mode, the Host Driver should stop the re-tuning timer and set the expiration flag to 1 when the Host System resumes from power down mode.</p> <p>0      Timer - Max data length 4MB<br/>1      Timer and Re-Tuning Request - Max data length 4MB<br/>2      Auto Re-Tuning (for transfer) - Timer and Re-Tuning Request<br/>3      Reserved</p> |
| 13    | TSDR50 | R    | 0h    | <p><b>Use Tuning for SDR50</b><br/>If this bit is set to 1, this Host Controller requires tuning to operate SDR50.<br/>[Tuning is always required to operate SDR104.]</p> <p>0      SDR50 does not require tuning.<br/>1      SDR50 requires tuning.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

**Table 5-2650. MMC\_CAPA2 Register Field Descriptions (continued)**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------|-----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12   | RESERVED2 | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 11:8 | TCRT      | R    | 0h    | <p>Timer Count for Re-Tuning<br/>This field indicates an initial value of the Re-Tuning Timer for Re-Tuning Mode 1 to 3. Setting to 0 disables Re-Tuning Timer.</p> <p>0 Re-Tuning Timer disabled<br/>1 1 second<br/>2 2 seconds<br/>3 4 seconds<br/>4 8 seconds<br/>5 16 seconds<br/>6 32 seconds<br/>7 64 seconds<br/>8 128 seconds<br/>9 256 seconds<br/>10 512 seconds<br/>11 1024 seconds<br/>12 Reserved<br/>13 Reserved<br/>14 Reserved<br/>15 Get information from other source</p> |
| 7    | RESERVED1 | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 6    | DTD       | R    | 0h    | <p>Driver Type D Support<br/>This bit indicates support of Driver Type D for 1.8 Signaling.</p> <p>0 Driver Type D is Not Supported.<br/>1 Driver Type D is Supported</p>                                                                                                                                                                                                                                                                                                                   |
| 5    | DTC       | R    | 0h    | <p>Driver Type C Support<br/>This bit indicates support of Driver Type C for 1.8 Signaling.</p> <p>0 Driver Type C is Not Supported.<br/>1 Driver Type C is Supported.</p>                                                                                                                                                                                                                                                                                                                  |
| 4    | DTA       | R    | 0h    | <p>Driver Type A Support<br/>This bit indicates support of Driver Type A for 1.8 Signaling.</p> <p>0 Driver Type A is Not Supported.<br/>1 Driver Type A is Supported.</p>                                                                                                                                                                                                                                                                                                                  |
| 3    | RESERVED  | R    | 0h    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 2    | DDR50     | R    | 0h    | <p>DDR50 Support</p> <p>0 DDR50 is Not Supported.<br/>1 DDR50 is Supported.</p>                                                                                                                                                                                                                                                                                                                                                                                                             |
| 1    | SDR104    | R    | 0h    | <p>SDR104 Support<br/>SDR104 requires tuning.</p> <p>0 SDR104 is Not Supported.<br/>1 SDR104 is Supported.</p>                                                                                                                                                                                                                                                                                                                                                                              |
| 0    | SDR50     | R    | 0h    | <p>SDR50 Support<br/>If SDR104 is supported, this bit shall be set to 1. Bit 13 indicates whether SDR50 requires tuning or not.</p> <p>0 SDR50 is Not Supported.<br/>1 SDR50 is Supported.</p>                                                                                                                                                                                                                                                                                              |

### 5.15.2.27 MMC\_CUR\_CAPA Register

#### 1 MMC\_CUR\_CAPA Register (Offset = 248h) [reset = 0h]

##### Maximum Current Capabilities Register

This register indicates the maximum current capability for each voltage. The value is meaningful if the voltage support is set in the capabilities register (MMCHS\_CAPA).

Initialization of this register (via a write access to this register) depends on the system capabilities. The host driver shall not modify this register after the initialization.

This register is only reinitialized by a hard reset (via RESETN signal).

Return to [Summary Table](#)

**Table 5-2651. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCS0         | 4830 0248h       |

**Figure 5-876. MMC\_CUR\_CAPA Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CUR_1V8  |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CUR_3V0  |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CUR_3V3  |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2653. MMC\_CUR\_CAPA Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                              |
|-------|----------|------|-------|--------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RESERVED | R    | 0h    |                                                                                                                          |
| 23:16 | CUR_1V8  | R/W  | 0h    | Maximum current for 1.8V<br>0 The maximum current capability for this voltage is not available. Feature not implemented. |
| 15:8  | CUR_3V0  | R/W  | 0h    | Maximum current for 3.0V<br>0 The maximum current capability for this voltage is not available. Feature not implemented. |
| 7:0   | CUR_3V3  | R/W  | 0h    | Maximum current for 3.3V<br>0 The maximum current capability for this voltage is not available. Feature not implemented. |

### 5.15.2.28 MMC\_FE Register

#### 1 MMC\_FE Register (Offset = 250h) [reset = 0h]

Force Event Register for Auto CMD Error Status and Error Interrupt status

The Force Event Register is not a physically implemented register. Rather, it is an address at which the Auto CMD Error Status Register can be written.

Writing 1 : set each bit of the Auto CMD Error Status Register

Writing 0 : no effect

Rather, it is an address at which the Error Interrupt Status register can be written. The effect of a write to this address will be reflected in the Error Interrupt Status Register if the corresponding bit of the Error Interrupt Status Enable Register is set.

Writing 1 : set each bit of the Error Interrupt Status Register

Writing 0 : no effect

Note: By setting this register, the Error Interrupt can be set in the Error Interrupt Status register. In order to generate interrupt signal, both the Error Interrupt Status Enable and Error Interrupt Signal Enable shall be set.

Return to [Summary Table](#)

**Table 5-2654. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCSD0        | 4830 0250h       |

**Figure 5-877. MMC\_FE Name Register**

| 31        | 30       | 29      | 28      | 27        | 26      | 25       | 24      |
|-----------|----------|---------|---------|-----------|---------|----------|---------|
| RESERVED3 |          | FE_BADA | FE_CERR | RESERVED2 |         | FE_ADMAE | FE_ACE  |
|           |          | W       | W       |           |         | W        | W       |
| 0h        |          | 0h      | 0h      | 0h        |         | 0h       | 0h      |
| 23        | 22       | 21      | 20      | 19        | 18      | 17       | 16      |
| FE_CLE    | FE_DEB   | FE_DCRC | FE_DTO  | FE_CIE    | FE_CEB  | FE_CCRC  | FE_CTO  |
|           | W        | W       | W       | W         | W       | W        | W       |
| 0h        | 0h       | 0h      | 0h      | 0h        | 0h      | 0h       | 0h      |
| 15        | 14       | 13      | 12      | 11        | 10      | 9        | 8       |
| RESERVED1 |          |         |         |           |         |          |         |
| 0h        |          |         |         |           |         |          |         |
| 7         | 6        | 5       | 4       | 3         | 2       | 1        | 0       |
| FE_CNI    | RESERVED |         | FE_ACIE | FE_ACEB   | FE_ACCE | FE_ACTO  | FE_ACNE |
| W         |          |         | W       | W         | W       | W        | W       |
| 0h        | 0h       |         | 0h      | 0h        | 0h      | 0h       | 0h      |

**Table 5-2656. MMC\_FE Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                               |
|-------|-----------|------|-------|-------------------------------------------------------------------------------------------|
| 31:30 | RESERVED3 |      | 0h    |                                                                                           |
| 29    | FE_BADA   | W    | 0h    | Force Event Bad access to data space.<br>0 No effect, No Interrupt.<br>1 Interrupt Forced |
| 28    | FE_CERR   | W    | 0h    | Force Event Card error.<br>0 No effect, No Interrupt.<br>1 Interrupt Forced               |
| 27:26 | RESERVED2 |      | 0h    |                                                                                           |

**Table 5-2656. MMC\_FE Register Field Descriptions (continued)**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                       |
|------|-----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 25   | FE_ADMAE  | W    | 0h    | Force Event ADMA Error.<br>0 No effect, No Interrupt.<br>1 Interrupt Forced                                                                                                                                                                                                                       |
| 24   | FE_ACE    | W    | 0h    | Force Event for Auto CMD Error<br>0 No effect, No Interrupt.<br>1 Interrupt Forced                                                                                                                                                                                                                |
| 23   | FE_CLE    |      | 0h    | Reserved.<br>Current limit error is not supported.<br>These bits are initialized to zero, and writes to them are ignored.                                                                                                                                                                         |
| 22   | FE_DEB    | W    | 0h    | Force Event Data End Bit error.<br>0 No effect, No Interrupt.<br>1 Interrupt Forced                                                                                                                                                                                                               |
| 21   | FE_DCRC   | W    | 0h    | Force Event Data CRC Error.<br>0 No effect, No Interrupt.<br>1 Interrupt Forced                                                                                                                                                                                                                   |
| 20   | FE_DTO    | W    | 0h    | Force Event Data Timeout Error.<br>0 No effect, No Interrupt.<br>1 Interrupt Forced                                                                                                                                                                                                               |
| 19   | FE_CIE    | W    | 0h    | Force Event Command Index Error.<br>0 No effect, No Interrupt.<br>1 Interrupt Forced                                                                                                                                                                                                              |
| 18   | FE_CEB    | W    | 0h    | Force Event Command End Bit Error.<br>0 No effect, No Interrupt.<br>1 Interrupt Forced                                                                                                                                                                                                            |
| 17   | FE_CCRC   | W    | 0h    | Force Event Command CRC Error.<br>0 No effect, No Interrupt.<br>1 Interrupt Forced                                                                                                                                                                                                                |
| 16   | FE_CTO    | W    | 0h    | Command Timeout Error<br>This bit is set automatically when no response is received within 64 clock cycles from the end bit of the command.<br>For commands that reply within 5 clock cycles - the timeout is still detected at 64 clock cycles.<br>0 Status bit unchanged<br>1 Status is cleared |
| 15:8 | RESERVED1 |      | 0h    |                                                                                                                                                                                                                                                                                                   |
| 7    | FE_CNI    | W    | 0h    | Force Event Command not issue by Auto CMD12 error<br>0 No effect, No Interrupt.<br>1 Interrupt Forced                                                                                                                                                                                             |
| 6:5  | RESERVED  |      | 0h    |                                                                                                                                                                                                                                                                                                   |
| 4    | FE_ACIE   | W    | 0h    | Force Event for Auto CMD Index Error<br>0 No effect, No Interrupt.<br>1 Interrupt Forced                                                                                                                                                                                                          |
| 3    | FE_ACEB   | W    | 0h    | Force Event Auto CMD End Bit Error<br>0 No effect, No Interrupt.<br>1 Interrupt Forced                                                                                                                                                                                                            |
| 2    | FE_ACCE   | W    | 0h    | Force Event Auto CMD CRC Error<br>0 No effect, No Interrupt.<br>1 Interrupt Forced                                                                                                                                                                                                                |



**Table 5-2656. MMC\_FE Register Field Descriptions (continued)**

| Bit | Field   | Type | Reset | Description                                                                             |
|-----|---------|------|-------|-----------------------------------------------------------------------------------------|
| 1   | FE_ACTO | W    | 0h    | Force Event Auto CMD Timeout Error<br>0 No effect, No Interrupt.<br>1 Interrupt Forced  |
| 0   | FE_ACNE | W    | 0h    | Force Event Auto CMD12 Not Executed<br>0 No effect, No Interrupt.<br>1 Interrupt Forced |

### 5.15.2.29 MMC\_ADMAES Register

#### 1 MMC\_ADMAES Register (Offset = 254h) [reset = 0h]

##### ADMA Error Status Register

When ADMA Error Interrupt is occurred, the ADMA Error States field in this register holds the ADMA state and the ADMA System Address Register holds the address around the error descriptor. For recovering the error, the Host Driver requires the ADMA state to identify the error descriptor address as follows:

ST\_STOP: Previous location set in the ADMA System Address register is the error descriptor address

ST\_FDS: Current location set in the ADMA System Address register is the error descriptor address

ST\_CADR: This state is never set because do not generate ADMA error in this state.

ST\_TFR: Previous location set in the ADMA System Address register is the error descriptor address

In case of write operation, the Host Driver should use ACMD22 to get the number of written block rather than using this information, since unwritten data may exist in the Host Controller. The Host Controller generates the ADMA Error Interrupt when it detects invalid descriptor data (Valid=0) at the ST\_FDS state. In this case, ADMA Error State indicates that an error occurs at ST\_FDS state. The Host Driver may find that the Valid bit is not set in the error descriptor.

Return to [Summary Table](#)

**Table 5-2657. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCSD0        | 4830 0254h       |

**Figure 5-878. MMC\_ADMAES Name Register**

|          |    |    |    |    |     |     |    |
|----------|----|----|----|----|-----|-----|----|
| 31       | 30 | 29 | 28 | 27 | 26  | 25  | 24 |
| RESERVED |    |    |    |    |     |     |    |
| R        |    |    |    |    |     |     |    |
| 0h       |    |    |    |    |     |     |    |
| 23       | 22 | 21 | 20 | 19 | 18  | 17  | 16 |
| RESERVED |    |    |    |    |     |     |    |
| R        |    |    |    |    |     |     |    |
| 0h       |    |    |    |    |     |     |    |
| 15       | 14 | 13 | 12 | 11 | 10  | 9   | 8  |
| RESERVED |    |    |    |    |     |     |    |
| R        |    |    |    |    |     |     |    |
| 0h       |    |    |    |    |     |     |    |
| 7        | 6  | 5  | 4  | 3  | 2   | 1   | 0  |
| RESERVED |    |    |    |    | LME | AES |    |
| R        |    |    |    |    | R/W | R/W |    |
| 0h       |    |    |    |    | 0h  | 0h  |    |

**Table 5-2659. MMC\_ADMAES Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                    |
|------|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:3 | RESERVED | R    | 0h    |                                                                                                                                                                                                                                                                                                |
| 2    | LME      | R/W  | 0h    | ADMA Length Mismatch Error:<br>[1] While Block Count Enable being set, the total data length specified by the Descriptor table is different from that specified by the Block Count and Block Length.<br>[2] Total data length can not be divided by the block length.<br>0 No Error<br>1 Error |

**Table 5-2659. MMC\_ADMAES Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1:0 | AES   | R/W  | 0h    | <p>ADMA Error State</p> <p>This field indicates the state of ADMA when error is occurred during ADMA data transfer.</p> <p>This field never indicates "10" because ADMA never stops in this state.</p> <p>0 ST_STOP (Stop DMA)Contents of SYS_SDR register</p> <p>1 ST_STOP (Stop DMA)Points the error descriptor</p> <p>2 Never set this state(Not used)</p> <p>3 ST_TFR (Transfer Data)Points the next of the error descriptor</p> |

### 5.15.2.30 MMC\_ADMA\_SAL Register

#### 1 MMC\_ADMA\_SAL Register (Offset = 258h) [reset = 0h]

ADMA System address Low bits.

Return to [Summary Table](#)

**Table 5-2660. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCSD0        | 4830 0258h       |

**Figure 5-879. MMC\_ADMA\_SAL Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ADMA_A32B |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ADMA_A32B |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ADMA_A32B |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ADMA_A32B |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 5-2662. MMC\_ADMA\_SAL Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | ADMA_A32B | R/W  | 0h    | ADMA System address 32 bits. This register holds byte address of executing command of the Descriptor table. 32-bit Address Descriptor uses lower 32-bit of this register. At the start of ADMA, the Host Driver shall set start address of the Descriptor table. The ADMA increments this register address, which points to next line, when every fetching a Descriptor line. When the ADMA Error Interrupt is generated, this register shall hold valid Descriptor address depending on the ADMA state. The Host Driver shall program Descriptor Table on 32-bit boundary and set 32-bit boundary address to this register. ADMA2 ignores lower 2-bit of this register and assumes it to be 00b |

### 5.15.2.31 MMC\_PVINITSD Register

#### 1 MMC\_PVINITSD Register (Offset = 260h) [reset = 0h]

Preset Value for Initialization and Default Speed modes.

Return to [Summary Table](#)

**Table 5-2663. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCS0         | 4830 0260h       |

**Figure 5-880. MMC\_PVINITSD Name Register**

|               |    |           |    |    |                |               |    |
|---------------|----|-----------|----|----|----------------|---------------|----|
| 31            | 30 | 29        | 28 | 27 | 26             | 25            | 24 |
| DSDS_SEL      |    | RESERVED1 |    |    | DSCLKGEN_SEL   | DSSDCLK_SEL   |    |
| R             |    | R         |    |    | R              | R             |    |
| 0h            |    | 0h        |    |    | 0h             | 0h            |    |
| 23            | 22 | 21        | 20 | 19 | 18             | 17            | 16 |
| DSSDCLK_SEL   |    |           |    |    |                |               |    |
| R             |    |           |    |    |                |               |    |
| 0h            |    |           |    |    |                |               |    |
| 15            | 14 | 13        | 12 | 11 | 10             | 9             | 8  |
| INITDS_SEL    |    | RESERVED  |    |    | INITCLKGEN_SEL | INITSDCLK_SEL |    |
| R             |    | R         |    |    | R              | R             |    |
| 0h            |    | 0h        |    |    | 0h             | 0h            |    |
| 7             | 6  | 5         | 4  | 3  | 2              | 1             | 0  |
| INITSDCLK_SEL |    |           |    |    |                |               |    |
| R             |    |           |    |    |                |               |    |
| 0h            |    |           |    |    |                |               |    |

**Table 5-2665. MMC\_PVINITSD Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                            |
|-------|--------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | DSDS_SEL     | R    | 0h    | Driver Strength Select Value - Default Speed mode<br>Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling.<br><br>0 Driver Type B is Selected.<br>1 Driver Type A is Selected.<br>2 Driver Type C is Selected.<br>3 Driver Type D is Selected. |
| 29:27 | RESERVED1    | R    | 0h    |                                                                                                                                                                                                                                                                                                        |
| 26    | DSCLKGEN_SEL | R    | 0h    | Clock Generator Select Value - Default Speed mode<br>This bit is effective when Host Controller supports programmable clock generator.<br><br>0 Host Controller Ver2.00 Compatible Clock Generator.<br>1 Programmable Clock Generator.                                                                 |
| 25:16 | DSSDCLK_SEL  | R    | 0h    | SDCLK Frequency Select Value - Default Speed mode<br>10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system.                                                                                                                                    |

**Table 5-2665. MMC\_PVINITSD Register Field Descriptions (continued)**

| Bit   | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                             |
|-------|----------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | INITDS_SEL     | R    | 0h    | Driver Strength Select Value - Initialization mode<br>Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling.<br><br>0      Driver Type B is Selected<br>1      Driver Type A is Selected<br>2      Driver Type C is Selected<br>3      Driver Type D is Selected |
| 13:11 | RESERVED       | R    | 0h    |                                                                                                                                                                                                                                                                                                                         |
| 10    | INITCLKGEN_SEL | R    | 0h    | Clock Generator Select Value - Initialization mode<br>This bit is effective when Host Controller supports programmable clock generator.<br><br>0      Host Controller ver2.00 Compatible Clock Generator.<br>1      Programmable Clock Generator.                                                                       |
| 9:0   | INITSDCLK_SEL  | R    | 0h    | SDCLK Frequency Select Value - Initialization mode<br>10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system.                                                                                                                                                    |

### 5.15.2.32 MMC\_PVHSSDR12 Register

#### 1 MMC\_PVHSSDR12 Register (Offset = 264h) [reset = 0h]

Preset Value for High Speed and SDR12 speed modes.

Return to [Summary Table](#)

**Table 5-2666. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCSD0        | 4830 0264h       |

**Figure 5-881. MMC\_PVHSSDR12 Name Register**

|                |           |    |    |    |                 |                |    |
|----------------|-----------|----|----|----|-----------------|----------------|----|
| 31             | 30        | 29 | 28 | 27 | 26              | 25             | 24 |
| SDR12DS_SEL    | RESERVED1 |    |    |    | SDR12CLKGEN_SEL | SDR12SDCLK_SEL |    |
| R              | R         |    |    |    | R               | R              |    |
| 0h             | 0h        |    |    |    | 0h              | 0h             |    |
| 23             | 22        | 21 | 20 | 19 | 18              | 17             | 16 |
| SDR12SDCLK_SEL |           |    |    |    |                 |                |    |
| R              |           |    |    |    |                 |                |    |
| 0h             |           |    |    |    |                 |                |    |
| 15             | 14        | 13 | 12 | 11 | 10              | 9              | 8  |
| HSDS_SEL       | RESERVED  |    |    |    | HCLKGEN_SEL     | HSSDCLK_SEL    |    |
| R              | R         |    |    |    | R               | R              |    |
| 0h             | 0h        |    |    |    | 0h              | 0h             |    |
| 7              | 6         | 5  | 4  | 3  | 2               | 1              | 0  |
| HSSDCLK_SEL    |           |    |    |    |                 |                |    |
| R              |           |    |    |    |                 |                |    |
| 0h             |           |    |    |    |                 |                |    |

**Table 5-2668. MMC\_PVHSSDR12 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                    |
|-------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | SDR12DS_SEL     | R    | 0h    | Driver Strength Select Value - SDR12 mode<br>Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling.<br><br>0 Driver Type B is Selected.<br>1 Driver Type A is Selected.<br>2 Driver Type C is Selected.<br>3 Driver Type D is Selected. |
| 29:27 | RESERVED1       | R    | 0h    |                                                                                                                                                                                                                                                                                                |
| 26    | SDR12CLKGEN_SEL | R    | 0h    | Clock Generator Select Value - SDR12 mode<br>This bit is effective when Host Controller supports programmable clock generator.<br><br>0 Host Controller Ver2.00 Compatible Clock Generato.<br>1 Programmable Clock Generator.                                                                  |
| 25:16 | SDR12SDCLK_SEL  | R    | 0h    | SDCLK Frequency Select Value - SDR12 mode<br>10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system.                                                                                                                                    |

**Table 5-2668. MMC\_PVHSSDR12 Register Field Descriptions (continued)**

| Bit   | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                |
|-------|--------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | HSDS_SEL     | R    | 0h    | Driver Strength Select Value - High Speed mode<br>Driver Strength is supported by 1.8V signaling bus speed modes.<br>This field is meaningless for 3.3V signaling.<br><br>0      Driver Type B is Selected.<br>1      Driver Type A is Selected.<br>2      Driver Type C is Selected.<br>3      Driver Type D is Selected. |
| 13:11 | RESERVED     | R    | 0h    |                                                                                                                                                                                                                                                                                                                            |
| 10    | HSCLKGEN_SEL | R    | 0h    | Clock Generator Select Value - High Speed mode<br>This bit is effective when Host Controller supports programmable clock generator.<br><br>0      Host Controller ver2.00 Compatible Clock Generator.<br>1      Programmable Clock Generator.                                                                              |
| 9:0   | HSSDCLK_SEL  | R    | 0h    | SDCLK Frequency Select Value - High Speed mode<br>10-bit preset value to set SDCLK Frequency Select in the Clock Control<br>Register is described by a host system.                                                                                                                                                        |



### 5.15.2.33 MMC\_PVSDR25SDR50 Register

#### 1 MMC\_PVSDR25SDR50 Register (Offset = 268h) [reset = 0h]

Preset Value for SDR25 and SDR50 speed modes.

Return to [Summary Table](#)

**Table 5-2669. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCSD0        | 4830 0268h       |

**Figure 5-882. MMC\_PVSDR25SDR50 Name Register**

|                |           |    |    |    |                     |                |    |
|----------------|-----------|----|----|----|---------------------|----------------|----|
| 31             | 30        | 29 | 28 | 27 | 26                  | 25             | 24 |
| SDR50DS_SEL    | RESERVED1 |    |    |    | SDR50CLKGE<br>N_SEL | SDR50SDCLK_SEL |    |
| R              | R         |    |    |    | R                   | R              |    |
| 0h             | 0h        |    |    |    | 0h                  | 0h             |    |
| 23             | 22        | 21 | 20 | 19 | 18                  | 17             | 16 |
| SDR50SDCLK_SEL |           |    |    |    |                     |                |    |
| R              |           |    |    |    |                     |                |    |
| 0h             |           |    |    |    |                     |                |    |
| 15             | 14        | 13 | 12 | 11 | 10                  | 9              | 8  |
| SDR25DS_SEL    | RESERVED  |    |    |    | SDR25CLKGE<br>N_SEL | SDR25SDCLK_SEL |    |
| R              | R         |    |    |    | R                   | R              |    |
| 0h             | 0h        |    |    |    | 0h                  | 0h             |    |
| 7              | 6         | 5  | 4  | 3  | 2                   | 1              | 0  |
| SDR25SDCLK_SEL |           |    |    |    |                     |                |    |
| R              |           |    |    |    |                     |                |    |
| 0h             |           |    |    |    |                     |                |    |

**Table 5-2671. MMC\_PVSDR25SDR50 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                       |
|-------|-----------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | SDR50DS_SEL     | R    | 0h    | Driver Strength Select Value - SDR50 mode<br>Driver Strength is supported by 1.8V signaling bus speed modes.<br>This field is meaningless for 3.3V signaling.<br><br>0 Driver Type B is Selected.<br>1 Driver Type A is Selected.<br>2 Driver Type C is Selected.<br>3 Driver Type D is Selected. |
| 29:27 | RESERVED1       | R    | 0h    |                                                                                                                                                                                                                                                                                                   |
| 26    | SDR50CLKGEN_SEL | R    | 0h    | Clock Generator Select Value - SDR50 mode<br>This bit is effective when Host Controller supports programmable clock generator.<br><br>0 Host Controller Ver2.00 Compatible Clock Generator.<br>1 Programmable Clock Generator.                                                                    |
| 25:16 | SDR50SDCLK_SEL  | R    | 0h    | SDCLK Frequency Select Value - SDR50 mode<br>10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system.                                                                                                                                       |

**Table 5-2671. MMC\_PVSDR25SDR50 Register Field Descriptions (continued)**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                                           |
|-------|-----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | SDR25DS_SEL     | R    | 0h    | Driver Strength Select Value - SDR25 mode<br>Driver Strength is supported by 1.8V signaling bus speed modes.<br>This field is meaningless for 3.3V signaling.<br><br>0      Driver Type B is Selected.<br>1      Driver Type A is Selected.<br>2      Driver Type C is Selected.<br>3      Driver Type D is Selected. |
| 13:11 | RESERVED        | R    | 0h    |                                                                                                                                                                                                                                                                                                                       |
| 10    | SDR25CLKGEN_SEL | R    | 0h    | Clock Generator Select Value - SDR25 mode<br>This bit is effective when Host Controller supports programmable clock generator.<br><br>0      Host Controller ver2.00 Compatible Clock Generator.<br>1      Programmable Clock Generato.                                                                               |
| 9:0   | SDR25SDCLK_SEL  | R    | 0h    | SDCLK Frequency Select Value - SDR25 mode<br>10-bit preset value to set SDCLK Frequency Select in the Clock Control<br>Register is described by a host system.                                                                                                                                                        |

### 5.15.2.34 MMC\_PVSDR104DDR50 Register

#### 1 MMC\_PVSDR104DDR50 Register (Offset = 26Ch) [reset = 0h]

Preset Value for SDR104 and DDR50 speed modes.

Return to [Summary Table](#)

**Table 5-2672. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCSD0        | 4830 026Ch       |

**Figure 5-883. MMC\_PVSDR104DDR50 Name Register**

|                 |           |    |    |    |                   |                 |    |
|-----------------|-----------|----|----|----|-------------------|-----------------|----|
| 31              | 30        | 29 | 28 | 27 | 26                | 25              | 24 |
| DDR50DS_SEL     | RESERVED1 |    |    |    | DDR50CLKGE_N_SEL  | DDR50SDCLK_SEL  |    |
| R               | R         |    |    |    | R                 | R               |    |
| 0h              | 0h        |    |    |    | 0h                | 0h              |    |
| 23              | 22        | 21 | 20 | 19 | 18                | 17              | 16 |
| DDR50SDCLK_SEL  |           |    |    |    |                   |                 |    |
| R               |           |    |    |    |                   |                 |    |
| 0h              |           |    |    |    |                   |                 |    |
| 15              | 14        | 13 | 12 | 11 | 10                | 9               | 8  |
| SDR104DS_SEL    | RESERVED  |    |    |    | SDR104CLKGE_N_SEL | SDR104SDCLK_SEL |    |
| R               | R         |    |    |    | R                 | R               |    |
| 0h              | 0h        |    |    |    | 0h                | 0h              |    |
| 7               | 6         | 5  | 4  | 3  | 2                 | 1               | 0  |
| SDR104SDCLK_SEL |           |    |    |    |                   |                 |    |
| R               |           |    |    |    |                   |                 |    |
| 0h              |           |    |    |    |                   |                 |    |

**Table 5-2674. MMC\_PVSDR104DDR50 Register Field Descriptions**

| Bit   | Field           | Type | Reset | Description                                                                                                                                                                                                                                                                                    |
|-------|-----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | DDR50DS_SEL     | R    | 0h    | Driver Strength Select Value - DDR50 mode<br>Driver Strength is supported by 1.8V signaling bus speed modes. This field is meaningless for 3.3V signaling.<br><br>0 Driver Type B is Selected.<br>1 Driver Type A is Selected.<br>2 Driver Type C is Selected.<br>3 Driver Type D is Selected. |
| 29:27 | RESERVED1       | R    | 0h    |                                                                                                                                                                                                                                                                                                |
| 26    | DDR50CLKGEN_SEL | R    | 0h    | Clock Generator Select Value - DDR50 mode<br>This bit is effective when Host Controller supports programmable clock generator.<br><br>0 Host Controller Ver2.00 Compatible Clock Generator<br>1 Programmable Clock Generator                                                                   |
| 25:16 | DDR50SDCLK_SEL  | R    | 0h    | SDCLK Frequency Select Value - DDR50 mode<br>10-bit preset value to set SDCLK Frequency Select in the Clock Control Register is described by a host system.                                                                                                                                    |

**Table 5-2674. MMC\_PVSDR104DDR50 Register Field Descriptions (continued)**

| Bit   | Field            | Type | Reset | Description                                                                                                                                                                                                                                                                                                            |
|-------|------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | SDR104DS_SEL     | R    | 0h    | Driver Strength Select Value - SDR104 mode<br>Driver Strength is supported by 1.8V signaling bus speed modes.<br>This field is meaningless for 3.3V signaling.<br><br>0      Driver Type B is Selected.<br>1      Driver Type A is Selected.<br>2      Driver Type C is Selected.<br>3      Driver Type D is Selected. |
| 13:11 | RESERVED         | R    | 0h    |                                                                                                                                                                                                                                                                                                                        |
| 10    | SDR104CLKGEN_SEL | R    | 0h    | Clock Generator Select Value - SDR104 mode<br>This bit is effective when Host Controller supports programmable clock generator.<br><br>0      Host Controller ver2.00 Compatible Clock Generator.<br>1      Programmable Clock Generator.                                                                              |
| 9:0   | SDR104SDCLK_SEL  | R    | 0h    | SDCLK Frequency Select Value - SDR104 mode<br>10-bit preset value to set SDCLK Frequency Select in the Clock Control<br>Register is described by a host system.                                                                                                                                                        |

### 5.15.2.35 MMC\_REV Register

#### 1 MMC\_REV Register (Offset = 2FCh) [reset = 31010000h]

##### Versions Register

This register contains the hard coded RTL vendor revision number, the version number of SD specification compliancy and a slot status bit.

MMCHS\_REV[31:16] = Host controller version

MMCHS\_REV[15:0] = Slot Interrupt Status.

Return to [Summary Table](#)

**Table 5-2675. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MMCS0         | 4830 02FCh       |

**Figure 5-884. MMC\_REV Name Register**

|          |    |    |    |    |    |    |     |
|----------|----|----|----|----|----|----|-----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24  |
| VREV     |    |    |    |    |    |    |     |
| R        |    |    |    |    |    |    |     |
| 31h      |    |    |    |    |    |    |     |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16  |
| SREV     |    |    |    |    |    |    |     |
| R        |    |    |    |    |    |    |     |
| 1h       |    |    |    |    |    |    |     |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8   |
| RESERVED |    |    |    |    |    |    |     |
| R        |    |    |    |    |    |    |     |
| 0h       |    |    |    |    |    |    |     |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0   |
| RESERVED |    |    |    |    |    |    | SIS |
| R        |    |    |    |    |    |    | R   |
| 0h       |    |    |    |    |    |    | 0h  |

**Table 5-2677. MMC\_REV Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                  |
|-------|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | VREV     | R    | 31h   | Vendor Version Number: IP revision<br>[7:4] Major revision<br>[3:0] Minor revision<br>Examples:<br>0x10 for 1.0<br>0x21 for 2.1                                                                                                                                                                                                              |
| 23:16 | SREV     | R    | 1h    | Specification Version Number<br>This status indicates the Host Controller Spec. Version. The upper and lower 4-bits indicate the version.<br><br>0 SD Host Specification Version 1.00.<br>1 SD Host Specification Version 2.00 - Including the feature of the ADMA and Test Register.<br>2 SD Host Specification Version 3.00.<br>3 Reserved |
| 15:1  | RESERVED | R    | 0h    |                                                                                                                                                                                                                                                                                                                                              |

**Table 5-2677. MMC\_REV Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                       |
|-----|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | SIS   | R    | 0h    | <p>Slot Interrupt Status</p> <p>This status bit indicates the inverted state of interrupt signal for the module.</p> <p>By a power on reset or by setting a software reset for all [MMCSD_HCTL[SRA]], the interrupt signal shall be de-asserted and this status shall read 0.</p> |

## 5.16 MPU\_8

### MPU\_8

#### 5.16.1 MPU\_8 Summaries

#### MPU\_8 Summaries

**Table 5-2678. MPU\_8 Registers, Base Address=4024 0000h, Length=1024**

| Offset | Length | Register Name                            | MPU_HSM Physical Address | MPU_HSM_DTHE Physical Address | MPU_L2OCRAM_BANK0 Physical Address |
|--------|--------|------------------------------------------|--------------------------|-------------------------------|------------------------------------|
| 0h     | 32     | MPU_8_REVISION                           | 4024 0000h               | 4012 0000h                    | 4002 0000h                         |
| 10h    | 32     | MPU_8_INTERRUPT_RAW_STAT<br>US_SET       | 4024 0010h               | 4012 0010h                    | 4002 0010h                         |
| 14h    | 32     | MPU_8_INTERRUPT_ENABLED_<br>STATUS_CLEAR | 4024 0014h               | 4012 0014h                    | 4002 0014h                         |
| 18h    | 32     | MPU_8_INTERRUPT_ENABLE                   | 4024 0018h               | 4012 0018h                    | 4002 0018h                         |
| 1Ch    | 32     | MPU_8_INTERRUPT_ENABLE_C<br>LEAR         | 4024 001Ch               | 4012 001Ch                    | 4002 001Ch                         |
| 200h   | 32     | MPU_8_PROGRAMMABLE_1_ST<br>ART_ADDRESS   | 4024 0200h               | 4012 0200h                    | 4002 0200h                         |
| 204h   | 32     | MPU_8_PROGRAMMABLE_1_EN<br>D_ADDRESS     | 4024 0204h               | 4012 0204h                    | 4002 0204h                         |
| 208h   | 32     | MPU_8_PROGRAMMABLE_1_MP<br>PA            | 4024 0208h               | 4012 0208h                    | 4002 0208h                         |
| 210h   | 32     | MPU_8_PROGRAMMABLE_2_ST<br>ART_ADDRESS   | 4024 0210h               | 4012 0210h                    | 4002 0210h                         |
| 214h   | 32     | MPU_8_PROGRAMMABLE_2_EN<br>D_ADDRESS     | 4024 0214h               | 4012 0214h                    | 4002 0214h                         |
| 218h   | 32     | MPU_8_PROGRAMMABLE_2_MP<br>PA            | 4024 0218h               | 4012 0218h                    | 4002 0218h                         |
| 220h   | 32     | MPU_8_PROGRAMMABLE_3_ST<br>ART_ADDRESS   | 4024 0220h               | 4012 0220h                    | 4002 0220h                         |
| 224h   | 32     | MPU_8_PROGRAMMABLE_3_EN<br>D_ADDRESS     | 4024 0224h               | 4012 0224h                    | 4002 0224h                         |
| 228h   | 32     | MPU_8_PROGRAMMABLE_3_MP<br>PA            | 4024 0228h               | 4012 0228h                    | 4002 0228h                         |
| 230h   | 32     | MPU_8_PROGRAMMABLE_4_ST<br>ART_ADDRESS   | 4024 0230h               | 4012 0230h                    | 4002 0230h                         |
| 234h   | 32     | MPU_8_PROGRAMMABLE_4_EN<br>D_ADDRESS     | 4024 0234h               | 4012 0234h                    | 4002 0234h                         |
| 238h   | 32     | MPU_8_PROGRAMMABLE_4_MP<br>PA            | 4024 0238h               | 4012 0238h                    | 4002 0238h                         |
| 240h   | 32     | MPU_8_PROGRAMMABLE_5_ST<br>ART_ADDRESS   | 4024 0240h               | 4012 0240h                    | 4002 0240h                         |
| 244h   | 32     | MPU_8_PROGRAMMABLE_5_EN<br>D_ADDRESS     | 4024 0244h               | 4012 0244h                    | 4002 0244h                         |
| 248h   | 32     | MPU_8_PROGRAMMABLE_5_MP<br>PA            | 4024 0248h               | 4012 0248h                    | 4002 0248h                         |
| 250h   | 32     | MPU_8_PROGRAMMABLE_6_ST<br>ART_ADDRESS   | 4024 0250h               | 4012 0250h                    | 4002 0250h                         |
| 254h   | 32     | MPU_8_PROGRAMMABLE_6_EN<br>D_ADDRESS     | 4024 0254h               | 4012 0254h                    | 4002 0254h                         |
| 258h   | 32     | MPU_8_PROGRAMMABLE_6_MP<br>PA            | 4024 0258h               | 4012 0258h                    | 4002 0258h                         |

**Table 5-2678. MPU\_8 Registers, Base Address=4024 0000h, Length=1024 (continued)**

| Offset | Length | Register Name                          | MPU_HSM Physical Address | MPU_HSM_DTHE Physical Address | MPU_L2OCRAM_BANK0 Physical Address |
|--------|--------|----------------------------------------|--------------------------|-------------------------------|------------------------------------|
| 260h   | 32     | MPU_8_PROGRAMMABLE_7_ST<br>ART_ADDRESS | 4024 0260h               | 4012 0260h                    | 4002 0260h                         |
| 264h   | 32     | MPU_8_PROGRAMMABLE_7_EN<br>D_ADDRESS   | 4024 0264h               | 4012 0264h                    | 4002 0264h                         |
| 268h   | 32     | MPU_8_PROGRAMMABLE_7_MP<br>PA          | 4024 0268h               | 4012 0268h                    | 4002 0268h                         |
| 270h   | 32     | MPU_8_PROGRAMMABLE_8_ST<br>ART_ADDRESS | 4024 0270h               | 4012 0270h                    | 4002 0270h                         |
| 274h   | 32     | MPU_8_PROGRAMMABLE_8_EN<br>D_ADDRESS   | 4024 0274h               | 4012 0274h                    | 4002 0274h                         |
| 278h   | 32     | MPU_8_PROGRAMMABLE_8_MP<br>PA          | 4024 0278h               | 4012 0278h                    | 4002 0278h                         |
| 300h   | 32     | MPU_8_FAULT_ADDRESS                    | 4024 0300h               | 4012 0300h                    | 4002 0300h                         |
| 304h   | 32     | MPU_8_FAULT_STATUS                     | 4024 0304h               | 4012 0304h                    | 4002 0304h                         |
| 308h   | 32     | MPU_8_FAULT_CLEAR                      | 4024 0308h               | 4012 0308h                    | 4002 0308h                         |

**Table 5-2679. MPU\_8 Registers, Base Address=4024 0000h, Length=1024**

| Offset | Length | Register Name                            | MPU_L2OCRAM_BANK1 Physical Address | MPU_L2OCRAM_BANK2 Physical Address | MPU_L2OCRAM_BANK3 Physical Address |
|--------|--------|------------------------------------------|------------------------------------|------------------------------------|------------------------------------|
| 0h     | 32     | MPU_8_REVISION                           | 4004 0000h                         | 4006 0000h                         | 4008 0000h                         |
| 10h    | 32     | MPU_8_INTERRUPT_RAW_STAT<br>US_SET       | 4004 0010h                         | 4006 0010h                         | 4008 0010h                         |
| 14h    | 32     | MPU_8_INTERRUPT_ENABLED_<br>STATUS_CLEAR | 4004 0014h                         | 4006 0014h                         | 4008 0014h                         |
| 18h    | 32     | MPU_8_INTERRUPT_ENABLE                   | 4004 0018h                         | 4006 0018h                         | 4008 0018h                         |
| 1Ch    | 32     | MPU_8_INTERRUPT_ENABLE_C<br>LEAR         | 4004 001Ch                         | 4006 001Ch                         | 4008 001Ch                         |
| 200h   | 32     | MPU_8_PROGRAMMABLE_1_ST<br>ART_ADDRESS   | 4004 0200h                         | 4006 0200h                         | 4008 0200h                         |
| 204h   | 32     | MPU_8_PROGRAMMABLE_1_EN<br>D_ADDRESS     | 4004 0204h                         | 4006 0204h                         | 4008 0204h                         |
| 208h   | 32     | MPU_8_PROGRAMMABLE_1_MP<br>PA            | 4004 0208h                         | 4006 0208h                         | 4008 0208h                         |
| 210h   | 32     | MPU_8_PROGRAMMABLE_2_ST<br>ART_ADDRESS   | 4004 0210h                         | 4006 0210h                         | 4008 0210h                         |
| 214h   | 32     | MPU_8_PROGRAMMABLE_2_EN<br>D_ADDRESS     | 4004 0214h                         | 4006 0214h                         | 4008 0214h                         |
| 218h   | 32     | MPU_8_PROGRAMMABLE_2_MP<br>PA            | 4004 0218h                         | 4006 0218h                         | 4008 0218h                         |
| 220h   | 32     | MPU_8_PROGRAMMABLE_3_ST<br>ART_ADDRESS   | 4004 0220h                         | 4006 0220h                         | 4008 0220h                         |
| 224h   | 32     | MPU_8_PROGRAMMABLE_3_EN<br>D_ADDRESS     | 4004 0224h                         | 4006 0224h                         | 4008 0224h                         |
| 228h   | 32     | MPU_8_PROGRAMMABLE_3_MP<br>PA            | 4004 0228h                         | 4006 0228h                         | 4008 0228h                         |
| 230h   | 32     | MPU_8_PROGRAMMABLE_4_ST<br>ART_ADDRESS   | 4004 0230h                         | 4006 0230h                         | 4008 0230h                         |
| 234h   | 32     | MPU_8_PROGRAMMABLE_4_EN<br>D_ADDRESS     | 4004 0234h                         | 4006 0234h                         | 4008 0234h                         |
| 238h   | 32     | MPU_8_PROGRAMMABLE_4_MP<br>PA            | 4004 0238h                         | 4006 0238h                         | 4008 0238h                         |



**Table 5-2679. MPU\_8 Registers, Base Address=4024 0000h, Length=1024 (continued)**

| Offset | Length | Register Name                          | MPU_L2OCRAM_BANK1<br>Physical Address | MPU_L2OCRAM_BANK2<br>Physical Address | MPU_L2OCRAM_BANK3<br>Physical Address |
|--------|--------|----------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|
| 240h   | 32     | MPU_8_PROGRAMMABLE_5_ST<br>ART_ADDRESS | 4004 0240h                            | 4006 0240h                            | 4008 0240h                            |
| 244h   | 32     | MPU_8_PROGRAMMABLE_5_EN<br>D_ADDRESS   | 4004 0244h                            | 4006 0244h                            | 4008 0244h                            |
| 248h   | 32     | MPU_8_PROGRAMMABLE_5_MP<br>PA          | 4004 0248h                            | 4006 0248h                            | 4008 0248h                            |
| 250h   | 32     | MPU_8_PROGRAMMABLE_6_ST<br>ART_ADDRESS | 4004 0250h                            | 4006 0250h                            | 4008 0250h                            |
| 254h   | 32     | MPU_8_PROGRAMMABLE_6_EN<br>D_ADDRESS   | 4004 0254h                            | 4006 0254h                            | 4008 0254h                            |
| 258h   | 32     | MPU_8_PROGRAMMABLE_6_MP<br>PA          | 4004 0258h                            | 4006 0258h                            | 4008 0258h                            |
| 260h   | 32     | MPU_8_PROGRAMMABLE_7_ST<br>ART_ADDRESS | 4004 0260h                            | 4006 0260h                            | 4008 0260h                            |
| 264h   | 32     | MPU_8_PROGRAMMABLE_7_EN<br>D_ADDRESS   | 4004 0264h                            | 4006 0264h                            | 4008 0264h                            |
| 268h   | 32     | MPU_8_PROGRAMMABLE_7_MP<br>PA          | 4004 0268h                            | 4006 0268h                            | 4008 0268h                            |
| 270h   | 32     | MPU_8_PROGRAMMABLE_8_ST<br>ART_ADDRESS | 4004 0270h                            | 4006 0270h                            | 4008 0270h                            |
| 274h   | 32     | MPU_8_PROGRAMMABLE_8_EN<br>D_ADDRESS   | 4004 0274h                            | 4006 0274h                            | 4008 0274h                            |
| 278h   | 32     | MPU_8_PROGRAMMABLE_8_MP<br>PA          | 4004 0278h                            | 4006 0278h                            | 4008 0278h                            |
| 300h   | 32     | MPU_8_FAULT_ADDRESS                    | 4004 0300h                            | 4006 0300h                            | 4008 0300h                            |
| 304h   | 32     | MPU_8_FAULT_STATUS                     | 4004 0304h                            | 4006 0304h                            | 4008 0304h                            |
| 308h   | 32     | MPU_8_FAULT_CLEAR                      | 4004 0308h                            | 4006 0308h                            | 4008 0308h                            |

**Table 5-2680. MPU\_8 Registers, Base Address=4024 0000h, Length=1024**

| Offset | Length | Register Name                            | MPU_MBOX_SRAM<br>Physical Address | MPU_QSPI0 Physical<br>Address | MPU_R5SS0_CORE0_A<br>XIS Physical Address |
|--------|--------|------------------------------------------|-----------------------------------|-------------------------------|-------------------------------------------|
| 0h     | 32     | MPU_8_REVISION                           | 4014 0000h                        | 4016 0000h                    | 400A 0000h                                |
| 10h    | 32     | MPU_8_INTERRUPT_RAW_STAT<br>US_SET       | 4014 0010h                        | 4016 0010h                    | 400A 0010h                                |
| 14h    | 32     | MPU_8_INTERRUPT_ENABLED_<br>STATUS_CLEAR | 4014 0014h                        | 4016 0014h                    | 400A 0014h                                |
| 18h    | 32     | MPU_8_INTERRUPT_ENABLE                   | 4014 0018h                        | 4016 0018h                    | 400A 0018h                                |
| 1Ch    | 32     | MPU_8_INTERRUPT_ENABLE_C<br>LEAR         | 4014 001Ch                        | 4016 001Ch                    | 400A 001Ch                                |
| 200h   | 32     | MPU_8_PROGRAMMABLE_1_ST<br>ART_ADDRESS   | 4014 0200h                        | 4016 0200h                    | 400A 0200h                                |
| 204h   | 32     | MPU_8_PROGRAMMABLE_1_EN<br>D_ADDRESS     | 4014 0204h                        | 4016 0204h                    | 400A 0204h                                |
| 208h   | 32     | MPU_8_PROGRAMMABLE_1_MP<br>PA            | 4014 0208h                        | 4016 0208h                    | 400A 0208h                                |
| 210h   | 32     | MPU_8_PROGRAMMABLE_2_ST<br>ART_ADDRESS   | 4014 0210h                        | 4016 0210h                    | 400A 0210h                                |
| 214h   | 32     | MPU_8_PROGRAMMABLE_2_EN<br>D_ADDRESS     | 4014 0214h                        | 4016 0214h                    | 400A 0214h                                |
| 218h   | 32     | MPU_8_PROGRAMMABLE_2_MP<br>PA            | 4014 0218h                        | 4016 0218h                    | 400A 0218h                                |

**Table 5-2680. MPU\_8 Registers, Base Address=4024 0000h, Length=1024 (continued)**

| Offset | Length | Register Name                                           | MPU_MBOX_SRAM<br>Physical Address | MPU_QSPI0 Physical<br>Address | MPU_R5SS0_CORE0_A<br>XIS Physical Address |
|--------|--------|---------------------------------------------------------|-----------------------------------|-------------------------------|-------------------------------------------|
| 220h   | 32     | <a href="#">MPU_8_PROGRAMMABLE_3_ST<br/>ART_ADDRESS</a> | 4014 0220h                        | 4016 0220h                    | 400A 0220h                                |
| 224h   | 32     | <a href="#">MPU_8_PROGRAMMABLE_3_EN<br/>D_ADDRESS</a>   | 4014 0224h                        | 4016 0224h                    | 400A 0224h                                |
| 228h   | 32     | <a href="#">MPU_8_PROGRAMMABLE_3_MP<br/>PA</a>          | 4014 0228h                        | 4016 0228h                    | 400A 0228h                                |
| 230h   | 32     | <a href="#">MPU_8_PROGRAMMABLE_4_ST<br/>ART_ADDRESS</a> | 4014 0230h                        | 4016 0230h                    | 400A 0230h                                |
| 234h   | 32     | <a href="#">MPU_8_PROGRAMMABLE_4_EN<br/>D_ADDRESS</a>   | 4014 0234h                        | 4016 0234h                    | 400A 0234h                                |
| 238h   | 32     | <a href="#">MPU_8_PROGRAMMABLE_4_MP<br/>PA</a>          | 4014 0238h                        | 4016 0238h                    | 400A 0238h                                |
| 240h   | 32     | <a href="#">MPU_8_PROGRAMMABLE_5_ST<br/>ART_ADDRESS</a> | 4014 0240h                        | 4016 0240h                    | 400A 0240h                                |
| 244h   | 32     | <a href="#">MPU_8_PROGRAMMABLE_5_EN<br/>D_ADDRESS</a>   | 4014 0244h                        | 4016 0244h                    | 400A 0244h                                |
| 248h   | 32     | <a href="#">MPU_8_PROGRAMMABLE_5_MP<br/>PA</a>          | 4014 0248h                        | 4016 0248h                    | 400A 0248h                                |
| 250h   | 32     | <a href="#">MPU_8_PROGRAMMABLE_6_ST<br/>ART_ADDRESS</a> | 4014 0250h                        | 4016 0250h                    | 400A 0250h                                |
| 254h   | 32     | <a href="#">MPU_8_PROGRAMMABLE_6_EN<br/>D_ADDRESS</a>   | 4014 0254h                        | 4016 0254h                    | 400A 0254h                                |
| 258h   | 32     | <a href="#">MPU_8_PROGRAMMABLE_6_MP<br/>PA</a>          | 4014 0258h                        | 4016 0258h                    | 400A 0258h                                |
| 260h   | 32     | <a href="#">MPU_8_PROGRAMMABLE_7_ST<br/>ART_ADDRESS</a> | 4014 0260h                        | 4016 0260h                    | 400A 0260h                                |
| 264h   | 32     | <a href="#">MPU_8_PROGRAMMABLE_7_EN<br/>D_ADDRESS</a>   | 4014 0264h                        | 4016 0264h                    | 400A 0264h                                |
| 268h   | 32     | <a href="#">MPU_8_PROGRAMMABLE_7_MP<br/>PA</a>          | 4014 0268h                        | 4016 0268h                    | 400A 0268h                                |
| 270h   | 32     | <a href="#">MPU_8_PROGRAMMABLE_8_ST<br/>ART_ADDRESS</a> | 4014 0270h                        | 4016 0270h                    | 400A 0270h                                |
| 274h   | 32     | <a href="#">MPU_8_PROGRAMMABLE_8_EN<br/>D_ADDRESS</a>   | 4014 0274h                        | 4016 0274h                    | 400A 0274h                                |
| 278h   | 32     | <a href="#">MPU_8_PROGRAMMABLE_8_MP<br/>PA</a>          | 4014 0278h                        | 4016 0278h                    | 400A 0278h                                |
| 300h   | 32     | <a href="#">MPU_8_FAULT_ADDRESS</a>                     | 4014 0300h                        | 4016 0300h                    | 400A 0300h                                |
| 304h   | 32     | <a href="#">MPU_8_FAULT_STATUS</a>                      | 4014 0304h                        | 4016 0304h                    | 400A 0304h                                |
| 308h   | 32     | <a href="#">MPU_8_FAULT_CLEAR</a>                       | 4014 0308h                        | 4016 0308h                    | 400A 0308h                                |

**Table 5-2681. MPU\_8 Registers, Base Address=4024 0000h, Length=1024**

| Offset | Length | Register Name                                             | MPU_R5SS0_CORE1_A<br>XIS Physical Address | MPU_R5SS1_CORE0_A<br>XIS Physical Address | MPU_R5SS1_CORE1_A<br>XIS Physical Address |
|--------|--------|-----------------------------------------------------------|-------------------------------------------|-------------------------------------------|-------------------------------------------|
| 0h     | 32     | <a href="#">MPU_8_REVISION</a>                            | 400C 0000h                                | 400E 0000h                                | 4010 0000h                                |
| 10h    | 32     | <a href="#">MPU_8_INTERRUPT_RAW_STAT<br/>US_SET</a>       | 400C 0010h                                | 400E 0010h                                | 4010 0010h                                |
| 14h    | 32     | <a href="#">MPU_8_INTERRUPT_ENABLED_<br/>STATUS_CLEAR</a> | 400C 0014h                                | 400E 0014h                                | 4010 0014h                                |
| 18h    | 32     | <a href="#">MPU_8_INTERRUPT_ENABLE</a>                    | 400C 0018h                                | 400E 0018h                                | 4010 0018h                                |
| 1Ch    | 32     | <a href="#">MPU_8_INTERRUPT_ENABLE_C<br/>LEAR</a>         | 400C 001Ch                                | 400E 001Ch                                | 4010 001Ch                                |

**Table 5-2681. MPU\_8 Registers, Base Address=4024 0000h, Length=1024 (continued)**

| Offset | Length | Register Name                          | MPU_R5SS0_CORE1_A<br>XIS Physical Address | MPU_R5SS1_CORE0_A<br>XIS Physical Address | MPU_R5SS1_CORE1_A<br>XIS Physical Address |
|--------|--------|----------------------------------------|-------------------------------------------|-------------------------------------------|-------------------------------------------|
| 200h   | 32     | MPU_8_PROGRAMMABLE_1_ST<br>ART_ADDRESS | 400C 0200h                                | 400E 0200h                                | 4010 0200h                                |
| 204h   | 32     | MPU_8_PROGRAMMABLE_1_EN<br>D_ADDRESS   | 400C 0204h                                | 400E 0204h                                | 4010 0204h                                |
| 208h   | 32     | MPU_8_PROGRAMMABLE_1_MP<br>PA          | 400C 0208h                                | 400E 0208h                                | 4010 0208h                                |
| 210h   | 32     | MPU_8_PROGRAMMABLE_2_ST<br>ART_ADDRESS | 400C 0210h                                | 400E 0210h                                | 4010 0210h                                |
| 214h   | 32     | MPU_8_PROGRAMMABLE_2_EN<br>D_ADDRESS   | 400C 0214h                                | 400E 0214h                                | 4010 0214h                                |
| 218h   | 32     | MPU_8_PROGRAMMABLE_2_MP<br>PA          | 400C 0218h                                | 400E 0218h                                | 4010 0218h                                |
| 220h   | 32     | MPU_8_PROGRAMMABLE_3_ST<br>ART_ADDRESS | 400C 0220h                                | 400E 0220h                                | 4010 0220h                                |
| 224h   | 32     | MPU_8_PROGRAMMABLE_3_EN<br>D_ADDRESS   | 400C 0224h                                | 400E 0224h                                | 4010 0224h                                |
| 228h   | 32     | MPU_8_PROGRAMMABLE_3_MP<br>PA          | 400C 0228h                                | 400E 0228h                                | 4010 0228h                                |
| 230h   | 32     | MPU_8_PROGRAMMABLE_4_ST<br>ART_ADDRESS | 400C 0230h                                | 400E 0230h                                | 4010 0230h                                |
| 234h   | 32     | MPU_8_PROGRAMMABLE_4_EN<br>D_ADDRESS   | 400C 0234h                                | 400E 0234h                                | 4010 0234h                                |
| 238h   | 32     | MPU_8_PROGRAMMABLE_4_MP<br>PA          | 400C 0238h                                | 400E 0238h                                | 4010 0238h                                |
| 240h   | 32     | MPU_8_PROGRAMMABLE_5_ST<br>ART_ADDRESS | 400C 0240h                                | 400E 0240h                                | 4010 0240h                                |
| 244h   | 32     | MPU_8_PROGRAMMABLE_5_EN<br>D_ADDRESS   | 400C 0244h                                | 400E 0244h                                | 4010 0244h                                |
| 248h   | 32     | MPU_8_PROGRAMMABLE_5_MP<br>PA          | 400C 0248h                                | 400E 0248h                                | 4010 0248h                                |
| 250h   | 32     | MPU_8_PROGRAMMABLE_6_ST<br>ART_ADDRESS | 400C 0250h                                | 400E 0250h                                | 4010 0250h                                |
| 254h   | 32     | MPU_8_PROGRAMMABLE_6_EN<br>D_ADDRESS   | 400C 0254h                                | 400E 0254h                                | 4010 0254h                                |
| 258h   | 32     | MPU_8_PROGRAMMABLE_6_MP<br>PA          | 400C 0258h                                | 400E 0258h                                | 4010 0258h                                |
| 260h   | 32     | MPU_8_PROGRAMMABLE_7_ST<br>ART_ADDRESS | 400C 0260h                                | 400E 0260h                                | 4010 0260h                                |
| 264h   | 32     | MPU_8_PROGRAMMABLE_7_EN<br>D_ADDRESS   | 400C 0264h                                | 400E 0264h                                | 4010 0264h                                |
| 268h   | 32     | MPU_8_PROGRAMMABLE_7_MP<br>PA          | 400C 0268h                                | 400E 0268h                                | 4010 0268h                                |
| 270h   | 32     | MPU_8_PROGRAMMABLE_8_ST<br>ART_ADDRESS | 400C 0270h                                | 400E 0270h                                | 4010 0270h                                |
| 274h   | 32     | MPU_8_PROGRAMMABLE_8_EN<br>D_ADDRESS   | 400C 0274h                                | 400E 0274h                                | 4010 0274h                                |
| 278h   | 32     | MPU_8_PROGRAMMABLE_8_MP<br>PA          | 400C 0278h                                | 400E 0278h                                | 4010 0278h                                |
| 300h   | 32     | MPU_8_FAULT_ADDRESS                    | 400C 0300h                                | 400E 0300h                                | 4010 0300h                                |
| 304h   | 32     | MPU_8_FAULT_STATUS                     | 400C 0304h                                | 400E 0304h                                | 4010 0304h                                |
| 308h   | 32     | MPU_8_FAULT_CLEAR                      | 400C 0308h                                | 400E 0308h                                | 4010 0308h                                |

## **5.16.2 MPU\_8 Registers**

### **MPU\_8 Registers**

### 5.16.2.1 MPU\_8\_REVISION Register

#### 1 MPU\_8\_REVISION Register (Offset = 0h) [reset = 4E815101h]

Revision.

Return to [Summary Table](#)

**Table 5-2682. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0000h       |
| MPU_HSM_DTHE         | 4012 0000h       |
| MPU_L2OCRAM_BANK0    | 4002 0000h       |
| MPU_L2OCRAM_BANK1    | 4004 0000h       |
| MPU_L2OCRAM_BANK2    | 4006 0000h       |
| MPU_L2OCRAM_BANK3    | 4008 0000h       |
| MPU_MBOX_SRAM        | 4014 0000h       |
| MPU_QSPI0            | 4016 0000h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0000h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0000h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0000h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0000h       |

**Figure 5-885. MPU\_8\_REVISION Name Register**

| 31        | 30 | 29       | 28 | 27     | 26 | 25 | 24 |
|-----------|----|----------|----|--------|----|----|----|
| SCHEME    |    | RESERVED |    | MODID  |    |    |    |
| R         |    | R        |    | R      |    |    |    |
| 1h        |    | 0h       |    | E81h   |    |    |    |
| 23        | 22 | 21       | 20 | 19     | 18 | 17 | 16 |
| MODID     |    |          |    |        |    |    |    |
| R         |    |          |    |        |    |    |    |
| E81h      |    |          |    |        |    |    |    |
| 15        | 14 | 13       | 12 | 11     | 10 | 9  | 8  |
| REVRTL    |    |          |    | REVMAJ |    |    |    |
| R         |    |          |    | R      |    |    |    |
| Ah        |    |          |    | 1h     |    |    |    |
| 7         | 6  | 5        | 4  | 3      | 2  | 1  | 0  |
| REVCUSTOM |    | REVMIN   |    |        |    |    |    |
| R         |    | R        |    |        |    |    |    |
| 0h        |    | 1h       |    |        |    |    |    |

**Table 5-2684. MPU\_8\_REVISION Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                  |
|-------|-----------|------|-------|----------------------------------------------|
| 31:30 | SCHEME    | R    | 1h    | Scheme.                                      |
| 29:28 | RESERVED  | R    | 0h    | Always read a s0. Writes have no affect.     |
| 27:16 | MODID     | R    | E81h  | Module ID field.                             |
| 15:11 | REVRTL    | R    | Ah    | RTL revision.Will vary depending on release. |
| 10:8  | REVMAJ    | R    | 1h    | Major revision.                              |
| 7:6   | REVCUSTOM | R    | 0h    | Custom revision.                             |

**Table 5-2684. MPU\_8\_REVISION Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description     |
|-----|--------|------|-------|-----------------|
| 5:0 | REVMIN | R    | 1h    | Minor revision. |

### 5.16.2.2 MPU\_8\_INTERRUPT\_RAW\_STATUS\_SET Register

#### 1 MPU\_8\_INTERRUPT\_RAW\_STATUS\_SET Register (Offset = 10h) [reset = 0h]

Interrupt\_Raw\_Status\_Set.

Return to [Summary Table](#)

**Table 5-2685. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0010h       |
| MPU_HSM_DTHE         | 4012 0010h       |
| MPU_L2OCRAM_BANK0    | 4002 0010h       |
| MPU_L2OCRAM_BANK1    | 4004 0010h       |
| MPU_L2OCRAM_BANK2    | 4006 0010h       |
| MPU_L2OCRAM_BANK3    | 4008 0010h       |
| MPU_MBOX_SRAM        | 4014 0010h       |
| MPU_QSPI0            | 4016 0010h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0010h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0010h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0010h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0010h       |

**Figure 5-886. MPU\_8\_INTERRUPT\_RAW\_STATUS\_SET Name Register**

|          |    |    |    |    |    |          |          |
|----------|----|----|----|----|----|----------|----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25       | 24       |
| RESERVED |    |    |    |    |    |          |          |
| R        |    |    |    |    |    |          |          |
| 0h       |    |    |    |    |    |          |          |
| 23       | 22 | 21 | 20 | 19 | 18 | 17       | 16       |
| RESERVED |    |    |    |    |    |          |          |
| R        |    |    |    |    |    |          |          |
| 0h       |    |    |    |    |    |          |          |
| 15       | 14 | 13 | 12 | 11 | 10 | 9        | 8        |
| RESERVED |    |    |    |    |    |          |          |
| R        |    |    |    |    |    |          |          |
| 0h       |    |    |    |    |    |          |          |
| 7        | 6  | 5  | 4  | 3  | 2  | 1        | 0        |
| RESERVED |    |    |    |    |    | ADDR_ERR | PROT_ERR |
| R        |    |    |    |    |    | R/W1TS   | R/W1TS   |
| 0h       |    |    |    |    |    | 0h       | 0h       |

**Table 5-2687. MPU\_8\_INTERRUPT\_RAW\_STATUS\_SET Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description                                                                                             |
|------|----------|--------|-------|---------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED | R      | 0h    | Always read as 0.                                                                                       |
| 1    | ADDR_ERR | R/W1TS | 0h    | Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. |
| 0    | PROT_ERR | R/W1TS | 0h    | Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. |

### 5.16.2.3 MPU\_8\_INTERRUPT\_ENABLED\_STATUS\_CLEAR Register

#### 1 MPU\_8\_INTERRUPT\_ENABLED\_STATUS\_CLEAR Register (Offset = 14h) [reset = 0h]

Interrupt\_Enabled\_Status\_Clear.

Return to [Summary Table](#)

**Table 5-2688. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0014h       |
| MPU_HSM_DTHE         | 4012 0014h       |
| MPU_L2OCRAM_BANK0    | 4002 0014h       |
| MPU_L2OCRAM_BANK1    | 4004 0014h       |
| MPU_L2OCRAM_BANK2    | 4006 0014h       |
| MPU_L2OCRAM_BANK3    | 4008 0014h       |
| MPU_MBOX_SRAM        | 4014 0014h       |
| MPU_QSPI0            | 4016 0014h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0014h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0014h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0014h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0014h       |

**Figure 5-887. MPU\_8\_INTERRUPT\_ENABLED\_STATUS\_CLEAR Name Register**

|          |    |    |    |    |    |                      |                      |
|----------|----|----|----|----|----|----------------------|----------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25                   | 24                   |
| RESERVED |    |    |    |    |    |                      |                      |
| R        |    |    |    |    |    |                      |                      |
| 0h       |    |    |    |    |    |                      |                      |
| 23       | 22 | 21 | 20 | 19 | 18 | 17                   | 16                   |
| RESERVED |    |    |    |    |    |                      |                      |
| R        |    |    |    |    |    |                      |                      |
| 0h       |    |    |    |    |    |                      |                      |
| 15       | 14 | 13 | 12 | 11 | 10 | 9                    | 8                    |
| RESERVED |    |    |    |    |    |                      |                      |
| R        |    |    |    |    |    |                      |                      |
| 0h       |    |    |    |    |    |                      |                      |
| 7        | 6  | 5  | 4  | 3  | 2  | 1                    | 0                    |
| RESERVED |    |    |    |    |    | ENABLED_AD<br>DR_ERR | ENABLED_PR<br>OT_ERR |
| R        |    |    |    |    |    | R/W0TC               | R/W0TC               |
| 0h       |    |    |    |    |    | 0h                   | 0h                   |

**Table 5-2690. MPU\_8\_INTERRUPT\_ENABLED\_STATUS\_CLEAR Register Field Descriptions**

| Bit  | Field            | Type   | Reset | Description                                                                                                   |
|------|------------------|--------|-------|---------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED         | R      | 0h    | Always read as 0.                                                                                             |
| 1    | ENABLED_ADDR_ERR | R/W0TC | 0h    | Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. |
| 0    | ENABLED_PROT_ERR | R/W0TC | 0h    | Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. |



### 5.16.2.4 MPU\_8\_INTERRUPT\_ENABLE Register

#### 1 MPU\_8\_INTERRUPT\_ENABLE Register (Offset = 18h) [reset = 0h]

Interrupt\_Enable.

Return to [Summary Table](#)

**Table 5-2691. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0018h       |
| MPU_HSM_DTHE         | 4012 0018h       |
| MPU_L2OCRAM_BANK0    | 4002 0018h       |
| MPU_L2OCRAM_BANK1    | 4004 0018h       |
| MPU_L2OCRAM_BANK2    | 4006 0018h       |
| MPU_L2OCRAM_BANK3    | 4008 0018h       |
| MPU_MBOX_SRAM        | 4014 0018h       |
| MPU_QSPI0            | 4016 0018h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0018h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0018h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0018h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0018h       |

**Figure 5-888. MPU\_8\_INTERRUPT\_ENABLE Name Register**

|          |    |    |    |    |    |             |             |
|----------|----|----|----|----|----|-------------|-------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25          | 24          |
| RESERVED |    |    |    |    |    |             |             |
| R        |    |    |    |    |    |             |             |
| 0h       |    |    |    |    |    |             |             |
| 23       | 22 | 21 | 20 | 19 | 18 | 17          | 16          |
| RESERVED |    |    |    |    |    |             |             |
| R        |    |    |    |    |    |             |             |
| 0h       |    |    |    |    |    |             |             |
| 15       | 14 | 13 | 12 | 11 | 10 | 9           | 8           |
| RESERVED |    |    |    |    |    |             |             |
| R        |    |    |    |    |    |             |             |
| 0h       |    |    |    |    |    |             |             |
| 7        | 6  | 5  | 4  | 3  | 2  | 1           | 0           |
| RESERVED |    |    |    |    |    | ADDR_ERR_EN | PROT_ERR_EN |
| R        |    |    |    |    |    | R/W1TS      | R/W1TS      |
| 0h       |    |    |    |    |    | 0h          | 0h          |

**Table 5-2693. MPU\_8\_INTERRUPT\_ENABLE Register Field Descriptions**

| Bit  | Field       | Type   | Reset | Description                                                                                |
|------|-------------|--------|-------|--------------------------------------------------------------------------------------------|
| 31:2 | RESERVED    | R      | 0h    | Always read as 0.                                                                          |
| 1    | ADDR_ERR_EN | R/W1TS | 0h    | Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. |
| 0    | PROT_ERR_EN | R/W1TS | 0h    | Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. |

### 5.16.2.5 MPU\_8\_INTERRUPT\_ENABLE\_CLEAR Register

#### 1 MPU\_8\_INTERRUPT\_ENABLE\_CLEAR Register (Offset = 1Ch) [reset = 0h]

Interrupt\_Enable\_Clear.

Return to [Summary Table](#)

**Table 5-2694. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 001Ch       |
| MPU_HSM_DTHE         | 4012 001Ch       |
| MPU_L2OCRAM_BANK0    | 4002 001Ch       |
| MPU_L2OCRAM_BANK1    | 4004 001Ch       |
| MPU_L2OCRAM_BANK2    | 4006 001Ch       |
| MPU_L2OCRAM_BANK3    | 4008 001Ch       |
| MPU_MBOX_SRAM        | 4014 001Ch       |
| MPU_QSPI0            | 4016 001Ch       |
| MPU_R5SS0_CORE0_AXIS | 400A 001Ch       |
| MPU_R5SS0_CORE1_AXIS | 400C 001Ch       |
| MPU_R5SS1_CORE0_AXIS | 400E 001Ch       |
| MPU_R5SS1_CORE1_AXIS | 4010 001Ch       |

**Figure 5-889. MPU\_8\_INTERRUPT\_ENABLE\_CLEAR Name Register**

|          |    |    |    |    |    |                 |                 |
|----------|----|----|----|----|----|-----------------|-----------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25              | 24              |
| RESERVED |    |    |    |    |    |                 |                 |
| R        |    |    |    |    |    |                 |                 |
| 0h       |    |    |    |    |    |                 |                 |
| 23       | 22 | 21 | 20 | 19 | 18 | 17              | 16              |
| RESERVED |    |    |    |    |    |                 |                 |
| R        |    |    |    |    |    |                 |                 |
| 0h       |    |    |    |    |    |                 |                 |
| 15       | 14 | 13 | 12 | 11 | 10 | 9               | 8               |
| RESERVED |    |    |    |    |    |                 |                 |
| R        |    |    |    |    |    |                 |                 |
| 0h       |    |    |    |    |    |                 |                 |
| 7        | 6  | 5  | 4  | 3  | 2  | 1               | 0               |
| RESERVED |    |    |    |    |    | ADDR_ERR_EN_CLR | PROT_ERR_EN_CLR |
| R        |    |    |    |    |    | R/W0TC          | R/W0TC          |
| 0h       |    |    |    |    |    | 0h              | 0h              |

**Table 5-2696. MPU\_8\_INTERRUPT\_ENABLE\_CLEAR Register Field Descriptions**

| Bit  | Field           | Type   | Reset | Description                                                                                  |
|------|-----------------|--------|-------|----------------------------------------------------------------------------------------------|
| 31:2 | RESERVED        | R      | 0h    | Always read as 0.                                                                            |
| 1    | ADDR_ERR_EN_CLR | R/W0TC | 0h    | Addressing violation error enable. Write a 1 to clear the enable. Writing a 0 has no effect. |
| 0    | PROT_ERR_EN_CLR | R/W0TC | 0h    | Protection violation error enable. Write a 1 to clear the enable. Writing a 0 has no effect. |

### 5.16.2.6 MPU\_8\_PROGRAMMABLE\_1\_START\_ADDRESS Register

#### 1 MPU\_8\_PROGRAMMABLE\_1\_START\_ADDRESS Register (Offset = 200h) [reset = 0h]

Programmable\_1\_Start\_Address.

Return to [Summary Table](#)

**Table 5-2697. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0200h       |
| MPU_HSM_DTHE         | 4012 0200h       |
| MPU_L2OCRAM_BANK0    | 4002 0200h       |
| MPU_L2OCRAM_BANK1    | 4004 0200h       |
| MPU_L2OCRAM_BANK2    | 4006 0200h       |
| MPU_L2OCRAM_BANK3    | 4008 0200h       |
| MPU_MBOX_SRAM        | 4014 0200h       |
| MPU_QSPI0            | 4016 0200h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0200h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0200h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0200h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0200h       |

**Figure 5-890. MPU\_8\_PROGRAMMABLE\_1\_START\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2699. MPU\_8\_PROGRAMMABLE\_1\_START\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                |
|------|------------|------|-------|------------------------------------------------------------|
| 31:0 | START_ADDR | R/W  | 0h    | Start address for range N. Defaults to input signal value. |

### 5.16.2.7 MPU\_8\_PROGRAMMABLE\_1\_END\_ADDRESS Register

#### 1 MPU\_8\_PROGRAMMABLE\_1\_END\_ADDRESS Register (Offset = 204h) [reset = 0h]

Programmable\_1\_End\_Address.

Return to [Summary Table](#)

**Table 5-2700. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0204h       |
| MPU_HSM_DTHE         | 4012 0204h       |
| MPU_L2OCRAM_BANK0    | 4002 0204h       |
| MPU_L2OCRAM_BANK1    | 4004 0204h       |
| MPU_L2OCRAM_BANK2    | 4006 0204h       |
| MPU_L2OCRAM_BANK3    | 4008 0204h       |
| MPU_MBOX_SRAM        | 4014 0204h       |
| MPU_QSPI0            | 4016 0204h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0204h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0204h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0204h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0204h       |

**Figure 5-891. MPU\_8\_PROGRAMMABLE\_1\_END\_ADDRESS Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2702. MPU\_8\_PROGRAMMABLE\_1\_END\_ADDRESS Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                              |
|------|----------|------|-------|----------------------------------------------------------|
| 31:0 | END_ADDR | R/W  | 0h    | End address for range N. Defaults to input signal value. |

### 5.16.2.8 MPU\_8\_PROGRAMMABLE\_1\_MPPA Register

#### 1 MPU\_8\_PROGRAMMABLE\_1\_MPPA Register (Offset = 208h) [reset = 0h]

Programmable\_1\_MPPA.

Return to [Summary Table](#)

**Table 5-2703. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0208h       |
| MPU_HSM_DTHE         | 4012 0208h       |
| MPU_L2OCRAM_BANK0    | 4002 0208h       |
| MPU_L2OCRAM_BANK1    | 4004 0208h       |
| MPU_L2OCRAM_BANK2    | 4006 0208h       |
| MPU_L2OCRAM_BANK3    | 4008 0208h       |
| MPU_MBOX_SRAM        | 4014 0208h       |
| MPU_QSPI0            | 4016 0208h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0208h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0208h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0208h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0208h       |

**Figure 5-892. MPU\_8\_PROGRAMMABLE\_1\_MPPA Name Register**

|           |     |     |      |           |     |         |           |
|-----------|-----|-----|------|-----------|-----|---------|-----------|
| 31        | 30  | 29  | 28   | 27        | 26  | 25      | 24        |
| RESERVED3 |     |     | LOCK | RESERVED2 |     | AID15_0 |           |
| R         |     |     | R/W  | R         |     | R/W     |           |
| 0h        |     |     | 0h   | 0h        |     | 0h      |           |
| 23        | 22  | 21  | 20   | 19        | 18  | 17      | 16        |
| AID15_0   |     |     |      |           |     |         |           |
| R/W       |     |     |      |           |     |         |           |
| 0h        |     |     |      |           |     |         |           |
| 15        | 14  | 13  | 12   | 11        | 10  | 9       | 8         |
| AID15_0   |     |     |      |           |     | AIDX    | RESERVED1 |
| R/W       |     |     |      |           |     | R/W     | R         |
| 0h        |     |     |      |           |     | 0h      | 0h        |
| 7         | 6   | 5   | 4    | 3         | 2   | 1       | 0         |
| NS        | EMU | SR  | SW   | SX        | UR  | UW      | UX        |
| R/W       | R/W | R/W | R/W  | R/W       | R/W | R/W     | R/W       |
| 0h        | 0h  | 0h  | 0h   | 0h        | 0h  | 0h      | 0h        |

**Table 5-2705. MPU\_8\_PROGRAMMABLE\_1\_MPPA Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED3 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                     |
| 28    | LOCK      | R/W  | 0h    | this field is used for locking the corresponding MPU region configurations.<br>Write 1 to lock the configurations along with the lock bit.<br>Writing 1 is allowed once per boot.<br>Lock bit will clear on reset only.<br>Once locked SW can not modify the MPU configurations along with lock bit. |
| 27:26 | RESERVED2 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |

**Table 5-2705. MPU\_8\_PROGRAMMABLE\_1\_MPPA Register Field Descriptions (continued)**

| Bit   | Field     | Type | Reset | Description                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 25:10 | AID15_0   | R/W  | 0h    | AIDs checked for this region. Defaults to input value.<br>0 = AID is not checked for these permissions.<br>1 = AID is checked for these permissions. |
| 9     | AIDX      | R/W  | 0h    | Additional AIDs checked. Defaults to input value.                                                                                                    |
| 8     | RESERVED1 | R    | 0h    | Always read as 0.                                                                                                                                    |
| 7     | NS        | R/W  | 0h    | Non-secure permission. Defaults to input value.                                                                                                      |
| 6     | EMU       | R/W  | 0h    | Debug permission. Defaults to input value.                                                                                                           |
| 5     | SR        | R/W  | 0h    | Supervisor read permission. Defaults to input value.                                                                                                 |
| 4     | SW        | R/W  | 0h    | Supervisor write permission. Defaults to input value.                                                                                                |
| 3     | SX        | R/W  | 0h    | Supervisor executable permission. Defaults to input value.                                                                                           |
| 2     | UR        | R/W  | 0h    | User read permission. Defaults to input value.                                                                                                       |
| 1     | UW        | R/W  | 0h    | User write permission. Defaults to input value.                                                                                                      |
| 0     | UX        | R/W  | 0h    | User executable permission. Defaults to input value.                                                                                                 |

### 5.16.2.9 MPU\_8\_PROGRAMMABLE\_2\_START\_ADDRESS Register

#### 1 MPU\_8\_PROGRAMMABLE\_2\_START\_ADDRESS Register (Offset = 210h) [reset = 0h]

Programmable\_2\_Start\_Address.

Return to [Summary Table](#)

**Table 5-2706. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0210h       |
| MPU_HSM_DTHE         | 4012 0210h       |
| MPU_L2OCRAM_BANK0    | 4002 0210h       |
| MPU_L2OCRAM_BANK1    | 4004 0210h       |
| MPU_L2OCRAM_BANK2    | 4006 0210h       |
| MPU_L2OCRAM_BANK3    | 4008 0210h       |
| MPU_MBOX_SRAM        | 4014 0210h       |
| MPU_QSPI0            | 4016 0210h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0210h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0210h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0210h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0210h       |

**Figure 5-893. MPU\_8\_PROGRAMMABLE\_2\_START\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2708. MPU\_8\_PROGRAMMABLE\_2\_START\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                |
|------|------------|------|-------|------------------------------------------------------------|
| 31:0 | START_ADDR | R/W  | 0h    | Start address for range N. Defaults to input signal value. |

### 5.16.2.10 MPU\_8\_PROGRAMMABLE\_2\_END\_ADDRESS Register

#### 1 MPU\_8\_PROGRAMMABLE\_2\_END\_ADDRESS Register (Offset = 214h) [reset = 0h]

Programmable\_2\_End\_Address.

Return to [Summary Table](#)

**Table 5-2709. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0214h       |
| MPU_HSM_DTHE         | 4012 0214h       |
| MPU_L2OCRAM_BANK0    | 4002 0214h       |
| MPU_L2OCRAM_BANK1    | 4004 0214h       |
| MPU_L2OCRAM_BANK2    | 4006 0214h       |
| MPU_L2OCRAM_BANK3    | 4008 0214h       |
| MPU_MBOX_SRAM        | 4014 0214h       |
| MPU_QSPI0            | 4016 0214h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0214h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0214h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0214h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0214h       |

**Figure 5-894. MPU\_8\_PROGRAMMABLE\_2\_END\_ADDRESS Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2711. MPU\_8\_PROGRAMMABLE\_2\_END\_ADDRESS Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                              |
|------|----------|------|-------|----------------------------------------------------------|
| 31:0 | END_ADDR | R/W  | 0h    | End address for range N. Defaults to input signal value. |



### 5.16.2.11 MPU\_8\_PROGRAMMABLE\_2\_MPPA Register

#### 1 MPU\_8\_PROGRAMMABLE\_2\_MPPA Register (Offset = 218h) [reset = 0h]

Programmable\_2\_MPPA.

Return to [Summary Table](#)

**Table 5-2712. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0218h       |
| MPU_HSM_DTHE         | 4012 0218h       |
| MPU_L2OCRAM_BANK0    | 4002 0218h       |
| MPU_L2OCRAM_BANK1    | 4004 0218h       |
| MPU_L2OCRAM_BANK2    | 4006 0218h       |
| MPU_L2OCRAM_BANK3    | 4008 0218h       |
| MPU_MBOX_SRAM        | 4014 0218h       |
| MPU_QSPI0            | 4016 0218h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0218h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0218h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0218h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0218h       |

**Figure 5-895. MPU\_8\_PROGRAMMABLE\_2\_MPPA Name Register**

|           |     |     |      |           |     |         |           |
|-----------|-----|-----|------|-----------|-----|---------|-----------|
| 31        | 30  | 29  | 28   | 27        | 26  | 25      | 24        |
| RESERVED3 |     |     | LOCK | RESERVED2 |     | AID15_0 |           |
| R         |     |     | R/W  | R         |     | R/W     |           |
| 0h        |     |     | 0h   | 0h        |     | 0h      |           |
| 23        | 22  | 21  | 20   | 19        | 18  | 17      | 16        |
| AID15_0   |     |     |      |           |     |         |           |
| R/W       |     |     |      |           |     |         |           |
| 0h        |     |     |      |           |     |         |           |
| 15        | 14  | 13  | 12   | 11        | 10  | 9       | 8         |
| AID15_0   |     |     |      |           |     | AIDX    | RESERVED1 |
| R/W       |     |     |      |           |     | R/W     | R         |
| 0h        |     |     |      |           |     | 0h      | 0h        |
| 7         | 6   | 5   | 4    | 3         | 2   | 1       | 0         |
| NS        | EMU | SR  | SW   | SX        | UR  | UW      | UX        |
| R/W       | R/W | R/W | R/W  | R/W       | R/W | R/W     | R/W       |
| 0h        | 0h  | 0h  | 0h   | 0h        | 0h  | 0h      | 0h        |

**Table 5-2714. MPU\_8\_PROGRAMMABLE\_2\_MPPA Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED3 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                     |
| 28    | LOCK      | R/W  | 0h    | this field is used for locking the corresponding MPU region configurations.<br>Write 1 to lock the configurations along with the lock bit.<br>Writing 1 is allowed once per boot.<br>Lock bit will clear on reset only.<br>Once locked SW can not modify the MPU configurations along with lock bit. |
| 27:26 | RESERVED2 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |

**Table 5-2714. MPU\_8\_PROGRAMMABLE\_2\_MPPA Register Field Descriptions (continued)**

| Bit   | Field     | Type | Reset | Description                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 25:10 | AID15_0   | R/W  | 0h    | AIDs checked for this region. Defaults to input value.<br>0 = AID is not checked for these permissions.<br>1 = AID is checked for these permissions. |
| 9     | AIDX      | R/W  | 0h    | Additional AIDs checked. Defaults to input value.                                                                                                    |
| 8     | RESERVED1 | R    | 0h    | Always read as 0.                                                                                                                                    |
| 7     | NS        | R/W  | 0h    | Non-secure permission. Defaults to input value.                                                                                                      |
| 6     | EMU       | R/W  | 0h    | Debug permission. Defaults to input value.                                                                                                           |
| 5     | SR        | R/W  | 0h    | Supervisor read permission. Defaults to input value.                                                                                                 |
| 4     | SW        | R/W  | 0h    | Supervisor write permission. Defaults to input value.                                                                                                |
| 3     | SX        | R/W  | 0h    | Supervisor executable permission. Defaults to input value.                                                                                           |
| 2     | UR        | R/W  | 0h    | User read permission. Defaults to input value.                                                                                                       |
| 1     | UW        | R/W  | 0h    | User write permission. Defaults to input value.                                                                                                      |
| 0     | UX        | R/W  | 0h    | User executable permission. Defaults to input value.                                                                                                 |

### 5.16.2.12 MPU\_8\_PROGRAMMABLE\_3\_START\_ADDRESS Register

#### 1 MPU\_8\_PROGRAMMABLE\_3\_START\_ADDRESS Register (Offset = 220h) [reset = 0h]

Programmable\_3\_Start\_Address.

Return to [Summary Table](#)

**Table 5-2715. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0220h       |
| MPU_HSM_DTHE         | 4012 0220h       |
| MPU_L2OCRAM_BANK0    | 4002 0220h       |
| MPU_L2OCRAM_BANK1    | 4004 0220h       |
| MPU_L2OCRAM_BANK2    | 4006 0220h       |
| MPU_L2OCRAM_BANK3    | 4008 0220h       |
| MPU_MBOX_SRAM        | 4014 0220h       |
| MPU_QSPI0            | 4016 0220h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0220h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0220h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0220h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0220h       |

**Figure 5-896. MPU\_8\_PROGRAMMABLE\_3\_START\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2717. MPU\_8\_PROGRAMMABLE\_3\_START\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                |
|------|------------|------|-------|------------------------------------------------------------|
| 31:0 | START_ADDR | R/W  | 0h    | Start address for range N. Defaults to input signal value. |

### 5.16.2.13 MPU\_8\_PROGRAMMABLE\_3\_END\_ADDRESS Register

#### 1 MPU\_8\_PROGRAMMABLE\_3\_END\_ADDRESS Register (Offset = 224h) [reset = 0h]

Programmable\_3\_End\_Address.

Return to [Summary Table](#)

**Table 5-2718. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0224h       |
| MPU_HSM_DTHE         | 4012 0224h       |
| MPU_L2OCRAM_BANK0    | 4002 0224h       |
| MPU_L2OCRAM_BANK1    | 4004 0224h       |
| MPU_L2OCRAM_BANK2    | 4006 0224h       |
| MPU_L2OCRAM_BANK3    | 4008 0224h       |
| MPU_MBOX_SRAM        | 4014 0224h       |
| MPU_QSPI0            | 4016 0224h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0224h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0224h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0224h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0224h       |

**Figure 5-897. MPU\_8\_PROGRAMMABLE\_3\_END\_ADDRESS Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2720. MPU\_8\_PROGRAMMABLE\_3\_END\_ADDRESS Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                              |
|------|----------|------|-------|----------------------------------------------------------|
| 31:0 | END_ADDR | R/W  | 0h    | End address for range N. Defaults to input signal value. |

#### 5.16.2.14 MPU\_8\_PROGRAMMABLE\_3\_MPPA Register

##### 1 MPU\_8\_PROGRAMMABLE\_3\_MPPA Register (Offset = 228h) [reset = 0h]

Programmable\_3\_MPPA.

Return to [Summary Table](#)

**Table 5-2721. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0228h       |
| MPU_HSM_DTHE         | 4012 0228h       |
| MPU_L2OCRAM_BANK0    | 4002 0228h       |
| MPU_L2OCRAM_BANK1    | 4004 0228h       |
| MPU_L2OCRAM_BANK2    | 4006 0228h       |
| MPU_L2OCRAM_BANK3    | 4008 0228h       |
| MPU_MBOX_SRAM        | 4014 0228h       |
| MPU_QSPI0            | 4016 0228h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0228h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0228h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0228h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0228h       |

**Figure 5-898. MPU\_8\_PROGRAMMABLE\_3\_MPPA Name Register**

|           |     |     |      |           |     |         |           |
|-----------|-----|-----|------|-----------|-----|---------|-----------|
| 31        | 30  | 29  | 28   | 27        | 26  | 25      | 24        |
| RESERVED3 |     |     | LOCK | RESERVED2 |     | AID15_0 |           |
| R         |     |     | R/W  | R         |     | R/W     |           |
| 0h        |     |     | 0h   | 0h        |     | 0h      |           |
| 23        | 22  | 21  | 20   | 19        | 18  | 17      | 16        |
| AID15_0   |     |     |      |           |     |         |           |
| R/W       |     |     |      |           |     |         |           |
| 0h        |     |     |      |           |     |         |           |
| 15        | 14  | 13  | 12   | 11        | 10  | 9       | 8         |
| AID15_0   |     |     |      |           |     | AIDX    | RESERVED1 |
| R/W       |     |     |      |           |     | R/W     | R         |
| 0h        |     |     |      |           |     | 0h      | 0h        |
| 7         | 6   | 5   | 4    | 3         | 2   | 1       | 0         |
| NS        | EMU | SR  | SW   | SX        | UR  | UW      | UX        |
| R/W       | R/W | R/W | R/W  | R/W       | R/W | R/W     | R/W       |
| 0h        | 0h  | 0h  | 0h   | 0h        | 0h  | 0h      | 0h        |

**Table 5-2723. MPU\_8\_PROGRAMMABLE\_3\_MPPA Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED3 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                     |
| 28    | LOCK      | R/W  | 0h    | this field is used for locking the corresponding MPU region configurations.<br>Write 1 to lock the configurations along with the lock bit.<br>Writing 1 is allowed once per boot.<br>Lock bit will clear on reset only.<br>Once locked SW can not modify the MPU configurations along with lock bit. |
| 27:26 | RESERVED2 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |

**Table 5-2723. MPU\_8\_PROGRAMMABLE\_3\_MPPA Register Field Descriptions (continued)**

| Bit   | Field     | Type | Reset | Description                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 25:10 | AID15_0   | R/W  | 0h    | AIDs checked for this region. Defaults to input value.<br>0 = AID is not checked for these permissions.<br>1 = AID is checked for these permissions. |
| 9     | AIDX      | R/W  | 0h    | Additional AIDs checked. Defaults to input value.                                                                                                    |
| 8     | RESERVED1 | R    | 0h    | Always read as 0.                                                                                                                                    |
| 7     | NS        | R/W  | 0h    | Non-secure permission. Defaults to input value.                                                                                                      |
| 6     | EMU       | R/W  | 0h    | Debug permission. Defaults to input value.                                                                                                           |
| 5     | SR        | R/W  | 0h    | Supervisor read permission. Defaults to input value.                                                                                                 |
| 4     | SW        | R/W  | 0h    | Supervisor write permission. Defaults to input value.                                                                                                |
| 3     | SX        | R/W  | 0h    | Supervisor executable permission. Defaults to input value.                                                                                           |
| 2     | UR        | R/W  | 0h    | User read permission. Defaults to input value.                                                                                                       |
| 1     | UW        | R/W  | 0h    | User write permission. Defaults to input value.                                                                                                      |
| 0     | UX        | R/W  | 0h    | User executable permission. Defaults to input value.                                                                                                 |

### 5.16.2.15 MPU\_8\_PROGRAMMABLE\_4\_START\_ADDRESS Register

#### 1 MPU\_8\_PROGRAMMABLE\_4\_START\_ADDRESS Register (Offset = 230h) [reset = 0h]

Programmable\_4\_Start\_Address.

Return to [Summary Table](#)

**Table 5-2724. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0230h       |
| MPU_HSM_DTHE         | 4012 0230h       |
| MPU_L2OCRAM_BANK0    | 4002 0230h       |
| MPU_L2OCRAM_BANK1    | 4004 0230h       |
| MPU_L2OCRAM_BANK2    | 4006 0230h       |
| MPU_L2OCRAM_BANK3    | 4008 0230h       |
| MPU_MBOX_SRAM        | 4014 0230h       |
| MPU_QSPI0            | 4016 0230h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0230h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0230h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0230h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0230h       |

**Figure 5-899. MPU\_8\_PROGRAMMABLE\_4\_START\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2726. MPU\_8\_PROGRAMMABLE\_4\_START\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                |
|------|------------|------|-------|------------------------------------------------------------|
| 31:0 | START_ADDR | R/W  | 0h    | Start address for range N. Defaults to input signal value. |

### 5.16.2.16 MPU\_8\_PROGRAMMABLE\_4\_END\_ADDRESS Register

#### 1 MPU\_8\_PROGRAMMABLE\_4\_END\_ADDRESS Register (Offset = 234h) [reset = 0h]

Programmable\_4\_End\_Address.

Return to [Summary Table](#)

**Table 5-2727. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0234h       |
| MPU_HSM_DTHE         | 4012 0234h       |
| MPU_L2OCRAM_BANK0    | 4002 0234h       |
| MPU_L2OCRAM_BANK1    | 4004 0234h       |
| MPU_L2OCRAM_BANK2    | 4006 0234h       |
| MPU_L2OCRAM_BANK3    | 4008 0234h       |
| MPU_MBOX_SRAM        | 4014 0234h       |
| MPU_QSPI0            | 4016 0234h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0234h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0234h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0234h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0234h       |

**Figure 5-900. MPU\_8\_PROGRAMMABLE\_4\_END\_ADDRESS Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2729. MPU\_8\_PROGRAMMABLE\_4\_END\_ADDRESS Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                              |
|------|----------|------|-------|----------------------------------------------------------|
| 31:0 | END_ADDR | R/W  | 0h    | End address for range N. Defaults to input signal value. |



### 5.16.2.17 MPU\_8\_PROGRAMMABLE\_4\_MPPA Register

#### 1 MPU\_8\_PROGRAMMABLE\_4\_MPPA Register (Offset = 238h) [reset = 0h]

Programmable\_4\_MPPA.

Return to [Summary Table](#)

**Table 5-2730. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0238h       |
| MPU_HSM_DTHE         | 4012 0238h       |
| MPU_L2OCRAM_BANK0    | 4002 0238h       |
| MPU_L2OCRAM_BANK1    | 4004 0238h       |
| MPU_L2OCRAM_BANK2    | 4006 0238h       |
| MPU_L2OCRAM_BANK3    | 4008 0238h       |
| MPU_MBOX_SRAM        | 4014 0238h       |
| MPU_QSPI0            | 4016 0238h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0238h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0238h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0238h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0238h       |

**Figure 5-901. MPU\_8\_PROGRAMMABLE\_4\_MPPA Name Register**

|           |     |     |      |           |     |         |           |
|-----------|-----|-----|------|-----------|-----|---------|-----------|
| 31        | 30  | 29  | 28   | 27        | 26  | 25      | 24        |
| RESERVED3 |     |     | LOCK | RESERVED2 |     | AID15_0 |           |
| R         |     |     | R/W  | R         |     | R/W     |           |
| 0h        |     |     | 0h   | 0h        |     | 0h      |           |
| 23        | 22  | 21  | 20   | 19        | 18  | 17      | 16        |
| AID15_0   |     |     |      |           |     |         |           |
| R/W       |     |     |      |           |     |         |           |
| 0h        |     |     |      |           |     |         |           |
| 15        | 14  | 13  | 12   | 11        | 10  | 9       | 8         |
| AID15_0   |     |     |      |           |     | AIDX    | RESERVED1 |
| R/W       |     |     |      |           |     | R/W     | R         |
| 0h        |     |     |      |           |     | 0h      | 0h        |
| 7         | 6   | 5   | 4    | 3         | 2   | 1       | 0         |
| NS        | EMU | SR  | SW   | SX        | UR  | UW      | UX        |
| R/W       | R/W | R/W | R/W  | R/W       | R/W | R/W     | R/W       |
| 0h        | 0h  | 0h  | 0h   | 0h        | 0h  | 0h      | 0h        |

**Table 5-2732. MPU\_8\_PROGRAMMABLE\_4\_MPPA Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED3 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                           |
| 28    | LOCK      | R/W  | 0h    | this field is used for locking the corresponding MPU region configurations.<br>Write 1 to lock the configurations along with the lock bit.<br>Writing 1 is allowed once per boot.<br>Lock bit will reset clear on reset only.<br>Once locked SW can not modify the MPU configurations along with lock bit. |
| 27:26 | RESERVED2 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                          |

**Table 5-2732. MPU\_8\_PROGRAMMABLE\_4\_MPPA Register Field Descriptions (continued)**

| Bit   | Field     | Type | Reset | Description                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 25:10 | AID15_0   | R/W  | 0h    | AIDs checked for this region. Defaults to input value.<br>0 = AID is not checked for these permissions.<br>1 = AID is checked for these permissions. |
| 9     | AIDX      | R/W  | 0h    | Additional AIDs checked. Defaults to input value.                                                                                                    |
| 8     | RESERVED1 | R    | 0h    | Always read as 0.                                                                                                                                    |
| 7     | NS        | R/W  | 0h    | Non-secure permission. Defaults to input value.                                                                                                      |
| 6     | EMU       | R/W  | 0h    | Debug permission. Defaults to input value.                                                                                                           |
| 5     | SR        | R/W  | 0h    | Supervisor read permission. Defaults to input value.                                                                                                 |
| 4     | SW        | R/W  | 0h    | Supervisor write permission. Defaults to input value.                                                                                                |
| 3     | SX        | R/W  | 0h    | Supervisor executable permission. Defaults to input value.                                                                                           |
| 2     | UR        | R/W  | 0h    | User read permission. Defaults to input value.                                                                                                       |
| 1     | UW        | R/W  | 0h    | User write permission. Defaults to input value.                                                                                                      |
| 0     | UX        | R/W  | 0h    | User executable permission. Defaults to input value.                                                                                                 |

### 5.16.2.18 MPU\_8\_PROGRAMMABLE\_5\_START\_ADDRESS Register

#### 1 MPU\_8\_PROGRAMMABLE\_5\_START\_ADDRESS Register (Offset = 240h) [reset = 0h]

Programmable\_5\_Start\_Address.

Return to [Summary Table](#)

**Table 5-2733. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0240h       |
| MPU_HSM_DTHE         | 4012 0240h       |
| MPU_L2OCRAM_BANK0    | 4002 0240h       |
| MPU_L2OCRAM_BANK1    | 4004 0240h       |
| MPU_L2OCRAM_BANK2    | 4006 0240h       |
| MPU_L2OCRAM_BANK3    | 4008 0240h       |
| MPU_MBOX_SRAM        | 4014 0240h       |
| MPU_QSPI0            | 4016 0240h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0240h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0240h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0240h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0240h       |

**Figure 5-902. MPU\_8\_PROGRAMMABLE\_5\_START\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2735. MPU\_8\_PROGRAMMABLE\_5\_START\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                |
|------|------------|------|-------|------------------------------------------------------------|
| 31:0 | START_ADDR | R/W  | 0h    | Start address for range N. Defaults to input signal value. |

### 5.16.2.19 MPU\_8\_PROGRAMMABLE\_5\_END\_ADDRESS Register

#### 1 MPU\_8\_PROGRAMMABLE\_5\_END\_ADDRESS Register (Offset = 244h) [reset = 0h]

Programmable\_5\_End\_Address.

Return to [Summary Table](#)

**Table 5-2736. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0244h       |
| MPU_HSM_DTHE         | 4012 0244h       |
| MPU_L2OCRAM_BANK0    | 4002 0244h       |
| MPU_L2OCRAM_BANK1    | 4004 0244h       |
| MPU_L2OCRAM_BANK2    | 4006 0244h       |
| MPU_L2OCRAM_BANK3    | 4008 0244h       |
| MPU_MBOX_SRAM        | 4014 0244h       |
| MPU_QSPI0            | 4016 0244h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0244h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0244h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0244h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0244h       |

**Figure 5-903. MPU\_8\_PROGRAMMABLE\_5\_END\_ADDRESS Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2738. MPU\_8\_PROGRAMMABLE\_5\_END\_ADDRESS Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                              |
|------|----------|------|-------|----------------------------------------------------------|
| 31:0 | END_ADDR | R/W  | 0h    | End address for range N. Defaults to input signal value. |

### 5.16.2.20 MPU\_8\_PROGRAMMABLE\_5\_MPPA Register

#### 1 MPU\_8\_PROGRAMMABLE\_5\_MPPA Register (Offset = 248h) [reset = 0h]

Programmable\_5\_MPPA.

Return to [Summary Table](#)

**Table 5-2739. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0248h       |
| MPU_HSM_DTHE         | 4012 0248h       |
| MPU_L2OCRAM_BANK0    | 4002 0248h       |
| MPU_L2OCRAM_BANK1    | 4004 0248h       |
| MPU_L2OCRAM_BANK2    | 4006 0248h       |
| MPU_L2OCRAM_BANK3    | 4008 0248h       |
| MPU_MBOX_SRAM        | 4014 0248h       |
| MPU_QSPI0            | 4016 0248h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0248h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0248h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0248h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0248h       |

**Figure 5-904. MPU\_8\_PROGRAMMABLE\_5\_MPPA Name Register**

|           |     |     |      |           |     |         |           |
|-----------|-----|-----|------|-----------|-----|---------|-----------|
| 31        | 30  | 29  | 28   | 27        | 26  | 25      | 24        |
| RESERVED3 |     |     | LOCK | RESERVED2 |     | AID15_0 |           |
| R         |     |     | R/W  | R         |     | R/W     |           |
| 0h        |     |     | 0h   | 0h        |     | 0h      |           |
| 23        | 22  | 21  | 20   | 19        | 18  | 17      | 16        |
| AID15_0   |     |     |      |           |     |         |           |
| R/W       |     |     |      |           |     |         |           |
| 0h        |     |     |      |           |     |         |           |
| 15        | 14  | 13  | 12   | 11        | 10  | 9       | 8         |
| AID15_0   |     |     |      |           |     | AIDX    | RESERVED1 |
| R/W       |     |     |      |           |     | R/W     | R         |
| 0h        |     |     |      |           |     | 0h      | 0h        |
| 7         | 6   | 5   | 4    | 3         | 2   | 1       | 0         |
| NS        | EMU | SR  | SW   | SX        | UR  | UW      | UX        |
| R/W       | R/W | R/W | R/W  | R/W       | R/W | R/W     | R/W       |
| 0h        | 0h  | 0h  | 0h   | 0h        | 0h  | 0h      | 0h        |

**Table 5-2741. MPU\_8\_PROGRAMMABLE\_5\_MPPA Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED3 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                     |
| 28    | LOCK      | R/W  | 0h    | this field is used for locking the corresponding MPU region configurations.<br>Write 1 to lock the configurations along with the lock bit.<br>Writing 1 is allowed once per boot.<br>Lock bit will clear on reset only.<br>Once locked SW can not modify the MPU configurations along with lock bit. |
| 27:26 | RESERVED2 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |

**Table 5-2741. MPU\_8\_PROGRAMMABLE\_5\_MPPA Register Field Descriptions (continued)**

| Bit   | Field     | Type | Reset | Description                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 25:10 | AID15_0   | R/W  | 0h    | AIDs checked for this region. Defaults to input value.<br>0 = AID is not checked for these permissions.<br>1 = AID is checked for these permissions. |
| 9     | AIDX      | R/W  | 0h    | Additional AIDs checked. Defaults to input value.                                                                                                    |
| 8     | RESERVED1 | R    | 0h    | Always read as 0.                                                                                                                                    |
| 7     | NS        | R/W  | 0h    | Non-secure permission. Defaults to input value.                                                                                                      |
| 6     | EMU       | R/W  | 0h    | Debug permission. Defaults to input value.                                                                                                           |
| 5     | SR        | R/W  | 0h    | Supervisor read permission. Defaults to input value.                                                                                                 |
| 4     | SW        | R/W  | 0h    | Supervisor write permission. Defaults to input value.                                                                                                |
| 3     | SX        | R/W  | 0h    | Supervisor executable permission. Defaults to input value.                                                                                           |
| 2     | UR        | R/W  | 0h    | User read permission. Defaults to input value.                                                                                                       |
| 1     | UW        | R/W  | 0h    | User write permission. Defaults to input value.                                                                                                      |
| 0     | UX        | R/W  | 0h    | User executable permission. Defaults to input value.                                                                                                 |

### 5.16.2.21 MPU\_8\_PROGRAMMABLE\_6\_START\_ADDRESS Register

#### 1 MPU\_8\_PROGRAMMABLE\_6\_START\_ADDRESS Register (Offset = 250h) [reset = 0h]

Programmable\_6\_Start\_Address.

Return to [Summary Table](#)

**Table 5-2742. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0250h       |
| MPU_HSM_DTHE         | 4012 0250h       |
| MPU_L2OCRAM_BANK0    | 4002 0250h       |
| MPU_L2OCRAM_BANK1    | 4004 0250h       |
| MPU_L2OCRAM_BANK2    | 4006 0250h       |
| MPU_L2OCRAM_BANK3    | 4008 0250h       |
| MPU_MBOX_SRAM        | 4014 0250h       |
| MPU_QSPI0            | 4016 0250h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0250h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0250h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0250h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0250h       |

**Figure 5-905. MPU\_8\_PROGRAMMABLE\_6\_START\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2744. MPU\_8\_PROGRAMMABLE\_6\_START\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                |
|------|------------|------|-------|------------------------------------------------------------|
| 31:0 | START_ADDR | R/W  | 0h    | Start address for range N. Defaults to input signal value. |

### 5.16.2.22 MPU\_8\_PROGRAMMABLE\_6\_END\_ADDRESS Register

#### 1 MPU\_8\_PROGRAMMABLE\_6\_END\_ADDRESS Register (Offset = 254h) [reset = 0h]

Programmable\_6\_End\_Address.

Return to [Summary Table](#)

**Table 5-2745. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0254h       |
| MPU_HSM_DTHE         | 4012 0254h       |
| MPU_L2OCRAM_BANK0    | 4002 0254h       |
| MPU_L2OCRAM_BANK1    | 4004 0254h       |
| MPU_L2OCRAM_BANK2    | 4006 0254h       |
| MPU_L2OCRAM_BANK3    | 4008 0254h       |
| MPU_MBOX_SRAM        | 4014 0254h       |
| MPU_QSPI0            | 4016 0254h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0254h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0254h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0254h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0254h       |

**Figure 5-906. MPU\_8\_PROGRAMMABLE\_6\_END\_ADDRESS Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2747. MPU\_8\_PROGRAMMABLE\_6\_END\_ADDRESS Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                              |
|------|----------|------|-------|----------------------------------------------------------|
| 31:0 | END_ADDR | R/W  | 0h    | End address for range N. Defaults to input signal value. |



### 5.16.2.23 MPU\_8\_PROGRAMMABLE\_6\_MPPA Register

#### 1 MPU\_8\_PROGRAMMABLE\_6\_MPPA Register (Offset = 258h) [reset = 0h]

Programmable\_6\_MPPA.

Return to [Summary Table](#)

**Table 5-2748. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0258h       |
| MPU_HSM_DTHER        | 4012 0258h       |
| MPU_L2OCRAM_BANK0    | 4002 0258h       |
| MPU_L2OCRAM_BANK1    | 4004 0258h       |
| MPU_L2OCRAM_BANK2    | 4006 0258h       |
| MPU_L2OCRAM_BANK3    | 4008 0258h       |
| MPU_MBOX_SRAM        | 4014 0258h       |
| MPU_QSPI0            | 4016 0258h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0258h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0258h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0258h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0258h       |

**Figure 5-907. MPU\_8\_PROGRAMMABLE\_6\_MPPA Name Register**

|           |     |     |      |           |     |         |           |
|-----------|-----|-----|------|-----------|-----|---------|-----------|
| 31        | 30  | 29  | 28   | 27        | 26  | 25      | 24        |
| RESERVED3 |     |     | LOCK | RESERVED2 |     | AID15_0 |           |
| R         |     |     | R/W  | R         |     | R/W     |           |
| 0h        |     |     | 0h   | 0h        |     | 0h      |           |
| 23        | 22  | 21  | 20   | 19        | 18  | 17      | 16        |
| AID15_0   |     |     |      |           |     |         |           |
| R/W       |     |     |      |           |     |         |           |
| 0h        |     |     |      |           |     |         |           |
| 15        | 14  | 13  | 12   | 11        | 10  | 9       | 8         |
| AID15_0   |     |     |      |           |     | AIDX    | RESERVED1 |
| R/W       |     |     |      |           |     | R/W     | R         |
| 0h        |     |     |      |           |     | 0h      | 0h        |
| 7         | 6   | 5   | 4    | 3         | 2   | 1       | 0         |
| NS        | EMU | SR  | SW   | SX        | UR  | UW      | UX        |
| R/W       | R/W | R/W | R/W  | R/W       | R/W | R/W     | R/W       |
| 0h        | 0h  | 0h  | 0h   | 0h        | 0h  | 0h      | 0h        |

**Table 5-2750. MPU\_8\_PROGRAMMABLE\_6\_MPPA Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED3 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                     |
| 28    | LOCK      | R/W  | 0h    | this field is used for locking the corresponding MPU region configurations.<br>Write 1 to lock the configurations along with the lock bit.<br>Writing 1 is allowed once per boot.<br>Lock bit will clear on reset only.<br>Once locked SW can not modify the MPU configurations along with lock bit. |
| 27:26 | RESERVED2 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |

**Table 5-2750. MPU\_8\_PROGRAMMABLE\_6\_MPPA Register Field Descriptions (continued)**

| Bit   | Field     | Type | Reset | Description                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 25:10 | AID15_0   | R/W  | 0h    | AIDs checked for this region. Defaults to input value.<br>0 = AID is not checked for these permissions.<br>1 = AID is checked for these permissions. |
| 9     | AIDX      | R/W  | 0h    | Additional AIDs checked. Defaults to input value.                                                                                                    |
| 8     | RESERVED1 | R    | 0h    | Always read as 0.                                                                                                                                    |
| 7     | NS        | R/W  | 0h    | Non-secure permission. Defaults to input value.                                                                                                      |
| 6     | EMU       | R/W  | 0h    | Debug permission. Defaults to input value.                                                                                                           |
| 5     | SR        | R/W  | 0h    | Supervisor read permission. Defaults to input value.                                                                                                 |
| 4     | SW        | R/W  | 0h    | Supervisor write permission. Defaults to input value.                                                                                                |
| 3     | SX        | R/W  | 0h    | Supervisor executable permission. Defaults to input value.                                                                                           |
| 2     | UR        | R/W  | 0h    | User read permission. Defaults to input value.                                                                                                       |
| 1     | UW        | R/W  | 0h    | User write permission. Defaults to input value.                                                                                                      |
| 0     | UX        | R/W  | 0h    | User executable permission. Defaults to input value.                                                                                                 |

#### 5.16.2.24 MPU\_8\_PROGRAMMABLE\_7\_START\_ADDRESS Register

##### 1 MPU\_8\_PROGRAMMABLE\_7\_START\_ADDRESS Register (Offset = 260h) [reset = 0h]

Programmable\_7\_Start\_Address.

Return to [Summary Table](#)

**Table 5-2751. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0260h       |
| MPU_HSM_DTHE         | 4012 0260h       |
| MPU_L2OCRAM_BANK0    | 4002 0260h       |
| MPU_L2OCRAM_BANK1    | 4004 0260h       |
| MPU_L2OCRAM_BANK2    | 4006 0260h       |
| MPU_L2OCRAM_BANK3    | 4008 0260h       |
| MPU_MBOX_SRAM        | 4014 0260h       |
| MPU_QSPI0            | 4016 0260h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0260h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0260h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0260h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0260h       |

**Figure 5-908. MPU\_8\_PROGRAMMABLE\_7\_START\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2753. MPU\_8\_PROGRAMMABLE\_7\_START\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                |
|------|------------|------|-------|------------------------------------------------------------|
| 31:0 | START_ADDR | R/W  | 0h    | Start address for range N. Defaults to input signal value. |

### 5.16.2.25 MPU\_8\_PROGRAMMABLE\_7\_END\_ADDRESS Register

#### 1 MPU\_8\_PROGRAMMABLE\_7\_END\_ADDRESS Register (Offset = 264h) [reset = 0h]

Programmable\_7\_End\_Address.

Return to [Summary Table](#)

**Table 5-2754. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0264h       |
| MPU_HSM_DTHE         | 4012 0264h       |
| MPU_L2OCRAM_BANK0    | 4002 0264h       |
| MPU_L2OCRAM_BANK1    | 4004 0264h       |
| MPU_L2OCRAM_BANK2    | 4006 0264h       |
| MPU_L2OCRAM_BANK3    | 4008 0264h       |
| MPU_MBOX_SRAM        | 4014 0264h       |
| MPU_QSPI0            | 4016 0264h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0264h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0264h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0264h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0264h       |

**Figure 5-909. MPU\_8\_PROGRAMMABLE\_7\_END\_ADDRESS Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2756. MPU\_8\_PROGRAMMABLE\_7\_END\_ADDRESS Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                              |
|------|----------|------|-------|----------------------------------------------------------|
| 31:0 | END_ADDR | R/W  | 0h    | End address for range N. Defaults to input signal value. |

### 5.16.2.26 MPU\_8\_PROGRAMMABLE\_7\_MPPA Register

#### 1 MPU\_8\_PROGRAMMABLE\_7\_MPPA Register (Offset = 268h) [reset = 0h]

Programmable\_7\_MPPA.

Return to [Summary Table](#)

**Table 5-2757. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0268h       |
| MPU_HSM_DTHE         | 4012 0268h       |
| MPU_L2OCRAM_BANK0    | 4002 0268h       |
| MPU_L2OCRAM_BANK1    | 4004 0268h       |
| MPU_L2OCRAM_BANK2    | 4006 0268h       |
| MPU_L2OCRAM_BANK3    | 4008 0268h       |
| MPU_MBOX_SRAM        | 4014 0268h       |
| MPU_QSPI0            | 4016 0268h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0268h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0268h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0268h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0268h       |

**Figure 5-910. MPU\_8\_PROGRAMMABLE\_7\_MPPA Name Register**

|           |     |     |      |           |     |         |           |
|-----------|-----|-----|------|-----------|-----|---------|-----------|
| 31        | 30  | 29  | 28   | 27        | 26  | 25      | 24        |
| RESERVED3 |     |     | LOCK | RESERVED2 |     | AID15_0 |           |
| R         |     |     | R/W  | R         |     | R/W     |           |
| 0h        |     |     | 0h   | 0h        |     | 0h      |           |
| 23        | 22  | 21  | 20   | 19        | 18  | 17      | 16        |
| AID15_0   |     |     |      |           |     |         |           |
| R/W       |     |     |      |           |     |         |           |
| 0h        |     |     |      |           |     |         |           |
| 15        | 14  | 13  | 12   | 11        | 10  | 9       | 8         |
| AID15_0   |     |     |      |           |     | AIDX    | RESERVED1 |
| R/W       |     |     |      |           |     | R/W     | R         |
| 0h        |     |     |      |           |     | 0h      | 0h        |
| 7         | 6   | 5   | 4    | 3         | 2   | 1       | 0         |
| NS        | EMU | SR  | SW   | SX        | UR  | UW      | UX        |
| R/W       | R/W | R/W | R/W  | R/W       | R/W | R/W     | R/W       |
| 0h        | 0h  | 0h  | 0h   | 0h        | 0h  | 0h      | 0h        |

**Table 5-2759. MPU\_8\_PROGRAMMABLE\_7\_MPPA Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED3 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                     |
| 28    | LOCK      | R/W  | 0h    | this field is used for locking the corresponding MPU region configurations.<br>Write 1 to lock the configurations along with the lock bit.<br>Writing 1 is allowed once per boot.<br>Lock bit will clear on reset only.<br>Once locked SW can not modify the MPU configurations along with lock bit. |
| 27:26 | RESERVED2 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |

**Table 5-2759. MPU\_8\_PROGRAMMABLE\_7\_MPPA Register Field Descriptions (continued)**

| Bit   | Field     | Type | Reset | Description                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 25:10 | AID15_0   | R/W  | 0h    | AIDs checked for this region. Defaults to input value.<br>0 = AID is not checked for these permissions.<br>1 = AID is checked for these permissions. |
| 9     | AIDX      | R/W  | 0h    | Additional AIDs checked. Defaults to input value.                                                                                                    |
| 8     | RESERVED1 | R    | 0h    | Always read as 0.                                                                                                                                    |
| 7     | NS        | R/W  | 0h    | Non-secure permission. Defaults to input value.                                                                                                      |
| 6     | EMU       | R/W  | 0h    | Debug permission. Defaults to input value.                                                                                                           |
| 5     | SR        | R/W  | 0h    | Supervisor read permission. Defaults to input value.                                                                                                 |
| 4     | SW        | R/W  | 0h    | Supervisor write permission. Defaults to input value.                                                                                                |
| 3     | SX        | R/W  | 0h    | Supervisor executable permission. Defaults to input value.                                                                                           |
| 2     | UR        | R/W  | 0h    | User read permission. Defaults to input value.                                                                                                       |
| 1     | UW        | R/W  | 0h    | User write permission. Defaults to input value.                                                                                                      |
| 0     | UX        | R/W  | 0h    | User executable permission. Defaults to input value.                                                                                                 |

### 5.16.2.27 MPU\_8\_PROGRAMMABLE\_8\_START\_ADDRESS Register

#### 1 MPU\_8\_PROGRAMMABLE\_8\_START\_ADDRESS Register (Offset = 270h) [reset = 0h]

Programmable\_8\_Start\_Address.

Return to [Summary Table](#)

**Table 5-2760. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0270h       |
| MPU_HSM_DTHE         | 4012 0270h       |
| MPU_L2OCRAM_BANK0    | 4002 0270h       |
| MPU_L2OCRAM_BANK1    | 4004 0270h       |
| MPU_L2OCRAM_BANK2    | 4006 0270h       |
| MPU_L2OCRAM_BANK3    | 4008 0270h       |
| MPU_MBOX_SRAM        | 4014 0270h       |
| MPU_QSPI0            | 4016 0270h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0270h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0270h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0270h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0270h       |

**Figure 5-911. MPU\_8\_PROGRAMMABLE\_8\_START\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2762. MPU\_8\_PROGRAMMABLE\_8\_START\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                |
|------|------------|------|-------|------------------------------------------------------------|
| 31:0 | START_ADDR | R/W  | 0h    | Start address for range N. Defaults to input signal value. |

### 5.16.2.28 MPU\_8\_PROGRAMMABLE\_8\_END\_ADDRESS Register

#### 1 MPU\_8\_PROGRAMMABLE\_8\_END\_ADDRESS Register (Offset = 274h) [reset = 0h]

Programmable\_8\_End\_Address.

Return to [Summary Table](#)

**Table 5-2763. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0274h       |
| MPU_HSM_DTHE         | 4012 0274h       |
| MPU_L2OCRAM_BANK0    | 4002 0274h       |
| MPU_L2OCRAM_BANK1    | 4004 0274h       |
| MPU_L2OCRAM_BANK2    | 4006 0274h       |
| MPU_L2OCRAM_BANK3    | 4008 0274h       |
| MPU_MBOX_SRAM        | 4014 0274h       |
| MPU_QSPI0            | 4016 0274h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0274h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0274h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0274h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0274h       |

**Figure 5-912. MPU\_8\_PROGRAMMABLE\_8\_END\_ADDRESS Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2765. MPU\_8\_PROGRAMMABLE\_8\_END\_ADDRESS Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                              |
|------|----------|------|-------|----------------------------------------------------------|
| 31:0 | END_ADDR | R/W  | 0h    | End address for range N. Defaults to input signal value. |



### 5.16.2.29 MPU\_8\_PROGRAMMABLE\_8\_MPPA Register

#### 1 MPU\_8\_PROGRAMMABLE\_8\_MPPA Register (Offset = 278h) [reset = 0h]

Programmable\_8\_MPPA.

Return to [Summary Table](#)

**Table 5-2766. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0278h       |
| MPU_HSM_DTHE         | 4012 0278h       |
| MPU_L2OCRAM_BANK0    | 4002 0278h       |
| MPU_L2OCRAM_BANK1    | 4004 0278h       |
| MPU_L2OCRAM_BANK2    | 4006 0278h       |
| MPU_L2OCRAM_BANK3    | 4008 0278h       |
| MPU_MBOX_SRAM        | 4014 0278h       |
| MPU_QSPI0            | 4016 0278h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0278h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0278h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0278h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0278h       |

**Figure 5-913. MPU\_8\_PROGRAMMABLE\_8\_MPPA Name Register**

| 31        | 30  | 29  | 28   | 27        | 26  | 25      | 24        |
|-----------|-----|-----|------|-----------|-----|---------|-----------|
| RESERVED3 |     |     | LOCK | RESERVED2 |     | AID15_0 |           |
| R         |     |     | R/W  | R         |     | R/W     |           |
| 0h        |     |     | 0h   | 0h        |     | 0h      |           |
| 23        | 22  | 21  | 20   | 19        | 18  | 17      | 16        |
| AID15_0   |     |     |      |           |     |         |           |
| R/W       |     |     |      |           |     |         |           |
| 0h        |     |     |      |           |     |         |           |
| 15        | 14  | 13  | 12   | 11        | 10  | 9       | 8         |
| AID15_0   |     |     |      |           |     | AIDX    | RESERVED1 |
| R/W       |     |     |      |           |     | R/W     | R         |
| 0h        |     |     |      |           |     | 0h      | 0h        |
| 7         | 6   | 5   | 4    | 3         | 2   | 1       | 0         |
| NS        | EMU | SR  | SW   | SX        | UR  | UW      | UX        |
| R/W       | R/W | R/W | R/W  | R/W       | R/W | R/W     | R/W       |
| 0h        | 0h  | 0h  | 0h   | 0h        | 0h  | 0h      | 0h        |

**Table 5-2768. MPU\_8\_PROGRAMMABLE\_8\_MPPA Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED3 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                     |
| 28    | LOCK      | R/W  | 0h    | this field is used for locking the corresponding MPU region configurations.<br>Write 1 to lock the configurations along with the lock bit.<br>Writing 1 is allowed once per boot.<br>Lock bit will clear on reset only.<br>Once locked SW can not modify the MPU configurations along with lock bit. |
| 27:26 | RESERVED2 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |

**Table 5-2768. MPU\_8\_PROGRAMMABLE\_8\_MPPA Register Field Descriptions (continued)**

| Bit   | Field     | Type | Reset | Description                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 25:10 | AID15_0   | R/W  | 0h    | AIDs checked for this region. Defaults to input value.<br>0 = AID is not checked for these permissions.<br>1 = AID is checked for these permissions. |
| 9     | AIDX      | R/W  | 0h    | Additional AIDs checked. Defaults to input value.                                                                                                    |
| 8     | RESERVED1 | R    | 0h    | Always read as 0.                                                                                                                                    |
| 7     | NS        | R/W  | 0h    | Non-secure permission. Defaults to input value.                                                                                                      |
| 6     | EMU       | R/W  | 0h    | Debug permission. Defaults to input value.                                                                                                           |
| 5     | SR        | R/W  | 0h    | Supervisor read permission. Defaults to input value.                                                                                                 |
| 4     | SW        | R/W  | 0h    | Supervisor write permission. Defaults to input value.                                                                                                |
| 3     | SX        | R/W  | 0h    | Supervisor executable permission. Defaults to input value.                                                                                           |
| 2     | UR        | R/W  | 0h    | User read permission. Defaults to input value.                                                                                                       |
| 1     | UW        | R/W  | 0h    | User write permission. Defaults to input value.                                                                                                      |
| 0     | UX        | R/W  | 0h    | User executable permission. Defaults to input value.                                                                                                 |

### 5.16.2.30 MPU\_8\_FAULT\_ADDRESS Register

#### 1 MPU\_8\_FAULT\_ADDRESS Register (Offset = 300h) [reset = 0h]

Fault\_Address.

Return to [Summary Table](#)

**Table 5-2769. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0300h       |
| MPU_HSM_DTHE         | 4012 0300h       |
| MPU_L2OCRAM_BANK0    | 4002 0300h       |
| MPU_L2OCRAM_BANK1    | 4004 0300h       |
| MPU_L2OCRAM_BANK2    | 4006 0300h       |
| MPU_L2OCRAM_BANK3    | 4008 0300h       |
| MPU_MBOX_SRAM        | 4014 0300h       |
| MPU_QSPI0            | 4016 0300h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0300h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0300h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0300h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0300h       |

**Figure 5-914. MPU\_8\_FAULT\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2771. MPU\_8\_FAULT\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description    |
|------|------------|------|-------|----------------|
| 31:0 | FAULT_ADDR | R    | 0h    | Fault_address. |

### 5.16.2.31 MPU\_8\_FAULT\_STATUS Register

#### 1 MPU\_8\_FAULT\_STATUS Register (Offset = 304h) [reset = 0h]

Fault\_Status.

Return to [Summary Table](#)

**Table 5-2772. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0304h       |
| MPU_HSM_DTHE         | 4012 0304h       |
| MPU_L2OCRAM_BANK0    | 4002 0304h       |
| MPU_L2OCRAM_BANK1    | 4004 0304h       |
| MPU_L2OCRAM_BANK2    | 4006 0304h       |
| MPU_L2OCRAM_BANK3    | 4008 0304h       |
| MPU_MBOX_SRAM        | 4014 0304h       |
| MPU_QSPI0            | 4016 0304h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0304h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0304h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0304h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0304h       |

**Figure 5-915. MPU\_8\_FAULT\_STATUS Name Register**

|          |           |            |    |        |    |    |           |
|----------|-----------|------------|----|--------|----|----|-----------|
| 31       | 30        | 29         | 28 | 27     | 26 | 25 | 24        |
| ID       |           |            |    |        |    |    |           |
| R        |           |            |    |        |    |    |           |
| 0h       |           |            |    |        |    |    |           |
| 23       | 22        | 21         | 20 | 19     | 18 | 17 | 16        |
| MSTID    |           |            |    |        |    |    |           |
| R        |           |            |    |        |    |    |           |
| 0h       |           |            |    |        |    |    |           |
| 15       | 14        | 13         | 12 | 11     | 10 | 9  | 8         |
| RESERVED |           |            |    | PRIVID |    |    | RESERVED1 |
| R        |           |            |    | R      |    |    | R         |
| 0h       |           |            |    | 0h     |    |    | 0h        |
| 7        | 6         | 5          | 4  | 3      | 2  | 1  | 0         |
| NS       | RESERVED2 | FAULT_TYPE |    |        |    |    |           |
| R        | R         | R          |    |        |    |    |           |
| 0h       | 0h        | 0h         |    |        |    |    |           |

**Table 5-2774. MPU\_8\_FAULT\_STATUS Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description        |
|-------|-----------|------|-------|--------------------|
| 31:24 | ID        | R    | 0h    | Transfer ID        |
| 23:16 | MSTID     | R    | 0h    | Master ID.         |
| 15:13 | RESERVED  | R    | 0h    | Always read as 0.  |
| 12:9  | PRIVID    | R    | 0h    | Privilege ID.      |
| 8     | RESERVED1 | R    | 0h    | Always read as 0.  |
| 7     | NS        | R    | 0h    | Non-secure access. |
| 6     | RESERVED2 | R    | 0h    | Always read as 0.  |

**Table 5-2774. MPU\_8\_FAULT\_STATUS Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                           |
|-----|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5:0 | FAULT_TYPE | R    | 0h    | Fault_type.<br>100000 = supervisor read fault<br>010000 = supervisor write fault<br>001000 = supervisor execute fault<br>000100 = user read fault<br>000010 = user write fault<br>000001 = user execute fault<br>111111 = relaxed cache linefill fault<br>010010 = relaxed cache writeback fault<br>000000 = no fault |

### 5.16.2.32 MPU\_8\_FAULT\_CLEAR Register

#### 1 MPU\_8\_FAULT\_CLEAR Register (Offset = 308h) [reset = 0h]

Fault\_Clear.

Return to [Summary Table](#)

**Table 5-2775. Instance Table**

| Instance Name        | Physical Address |
|----------------------|------------------|
| MPU_HSM              | 4024 0308h       |
| MPU_HSM_DTHE         | 4012 0308h       |
| MPU_L2OCRAM_BANK0    | 4002 0308h       |
| MPU_L2OCRAM_BANK1    | 4004 0308h       |
| MPU_L2OCRAM_BANK2    | 4006 0308h       |
| MPU_L2OCRAM_BANK3    | 4008 0308h       |
| MPU_MBOX_SRAM        | 4014 0308h       |
| MPU_QSPI0            | 4016 0308h       |
| MPU_R5SS0_CORE0_AXIS | 400A 0308h       |
| MPU_R5SS0_CORE1_AXIS | 400C 0308h       |
| MPU_R5SS1_CORE0_AXIS | 400E 0308h       |
| MPU_R5SS1_CORE1_AXIS | 4010 0308h       |

**Figure 5-916. MPU\_8\_FAULT\_CLEAR Name Register**

|          |    |    |    |    |    |    |           |
|----------|----|----|----|----|----|----|-----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24        |
| RESERVED |    |    |    |    |    |    |           |
| R        |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16        |
| RESERVED |    |    |    |    |    |    |           |
| R        |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8         |
| RESERVED |    |    |    |    |    |    |           |
| R        |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0         |
| RESERVED |    |    |    |    |    |    | FAULT_CLR |
| R        |    |    |    |    |    |    | W         |
| 0h       |    |    |    |    |    |    | 0h        |

**Table 5-2777. MPU\_8\_FAULT\_CLEAR Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                   |
|------|-----------|------|-------|-------------------------------------------------------------------------------|
| 31:1 | RESERVED  | R    | 0h    | Always read as 0.                                                             |
| 0    | FAULT_CLR | W    | 0h    | Fault_clear. Writing a 1 clears the current fault. Writing a 0 has no effect. |

## 5.17 MPU\_16

### MPU\_16

#### 5.17.1 MPU\_16 Summaries

#### MPU\_16 Summaries

**Table 5-2778. MPU\_16 Registers, Base Address=401E 0000h, Length=1024**

| Offset | Length | Register Name                                         | MPU_R5SS0_CORE1_AHB Physical Address |
|--------|--------|-------------------------------------------------------|--------------------------------------|
| 0h     | 32     | <a href="#">MPU_16_REVISION</a>                       | 401E 0000h                           |
| 10h    | 32     | <a href="#">MPU_16_INTERRUPT_RAW_STATUS_SET</a>       | 401E 0010h                           |
| 14h    | 32     | <a href="#">MPU_16_INTERRUPT_ENABLED_STATUS_CLEAR</a> | 401E 0014h                           |
| 18h    | 32     | <a href="#">MPU_16_INTERRUPT_ENABLE</a>               | 401E 0018h                           |
| 1Ch    | 32     | <a href="#">MPU_16_INTERRUPT_ENABLE_CLEAR</a>         | 401E 001Ch                           |
| 200h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_1_START_ADDRESS</a>   | 401E 0200h                           |
| 204h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_1_END_ADDRESS</a>     | 401E 0204h                           |
| 208h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_1_MPPA</a>            | 401E 0208h                           |
| 210h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_2_START_ADDRESS</a>   | 401E 0210h                           |
| 214h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_2_END_ADDRESS</a>     | 401E 0214h                           |
| 218h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_2_MPPA</a>            | 401E 0218h                           |
| 220h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_3_START_ADDRESS</a>   | 401E 0220h                           |
| 224h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_3_END_ADDRESS</a>     | 401E 0224h                           |
| 228h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_3_MPPA</a>            | 401E 0228h                           |
| 230h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_4_START_ADDRESS</a>   | 401E 0230h                           |
| 234h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_4_END_ADDRESS</a>     | 401E 0234h                           |
| 238h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_4_MPPA</a>            | 401E 0238h                           |
| 240h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_5_START_ADDRESS</a>   | 401E 0240h                           |
| 244h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_5_END_ADDRESS</a>     | 401E 0244h                           |
| 248h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_5_MPPA</a>            | 401E 0248h                           |
| 250h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_6_START_ADDRESS</a>   | 401E 0250h                           |
| 254h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_6_END_ADDRESS</a>     | 401E 0254h                           |
| 258h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_6_MPPA</a>            | 401E 0258h                           |
| 260h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_7_START_ADDRESS</a>   | 401E 0260h                           |
| 264h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_7_END_ADDRESS</a>     | 401E 0264h                           |
| 268h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_7_MPPA</a>            | 401E 0268h                           |
| 270h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_8_START_ADDRESS</a>   | 401E 0270h                           |
| 274h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_8_END_ADDRESS</a>     | 401E 0274h                           |
| 278h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_8_MPPA</a>            | 401E 0278h                           |
| 280h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_9_START_ADDRESS</a>   | 401E 0280h                           |
| 284h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_9_END_ADDRESS</a>     | 401E 0284h                           |
| 288h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_9_MPPA</a>            | 401E 0288h                           |
| 290h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_10_START_ADDRESS</a>  | 401E 0290h                           |
| 294h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_10_END_ADDRESS</a>    | 401E 0294h                           |
| 298h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_10_MPPA</a>           | 401E 0298h                           |
| 2A0h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_11_START_ADDRESS</a>  | 401E 02A0h                           |
| 2A4h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_11_END_ADDRESS</a>    | 401E 02A4h                           |

**Table 5-2778. MPU\_16 Registers, Base Address=401E 0000h, Length=1024 (continued)**

| Offset | Length | Register Name                                        | MPU_R5SS0_CORE1_AHB Physical Address |
|--------|--------|------------------------------------------------------|--------------------------------------|
| 2A8h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_11_MPPA</a>          | 401E 02A8h                           |
| 2B0h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_12_START_ADDRESS</a> | 401E 02B0h                           |
| 2B4h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_12_END_ADDRESS</a>   | 401E 02B4h                           |
| 2B8h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_12_MPPA</a>          | 401E 02B8h                           |
| 2C0h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_13_START_ADDRESS</a> | 401E 02C0h                           |
| 2C4h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_13_END_ADDRESS</a>   | 401E 02C4h                           |
| 2C8h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_13_MPPA</a>          | 401E 02C8h                           |
| 2D0h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_14_START_ADDRESS</a> | 401E 02D0h                           |
| 2D4h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_14_END_ADDRESS</a>   | 401E 02D4h                           |
| 2D8h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_14_MPPA</a>          | 401E 02D8h                           |
| 2E0h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_15_START_ADDRESS</a> | 401E 02E0h                           |
| 2E4h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_15_END_ADDRESS</a>   | 401E 02E4h                           |
| 2E8h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_15_MPPA</a>          | 401E 02E8h                           |
| 2F0h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_16_START_ADDRESS</a> | 401E 02F0h                           |
| 2F4h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_16_END_ADDRESS</a>   | 401E 02F4h                           |
| 2F8h   | 32     | <a href="#">MPU_16_PROGRAMMABLE_16_MPPA</a>          | 401E 02F8h                           |
| 300h   | 32     | <a href="#">MPU_16_FAULT_ADDRESS</a>                 | 401E 0300h                           |
| 304h   | 32     | <a href="#">MPU_16_FAULT_STATUS</a>                  | 401E 0304h                           |
| 308h   | 32     | <a href="#">MPU_16_FAULT_CLEAR</a>                   | 401E 0308h                           |

### 5.17.2 MPU\_16 Registers

#### MPU\_16 Registers



### 5.17.2.1 MPU\_16\_REVISION Register

#### 1 MPU\_16\_REVISION Register (Offset = 0h) [reset = 4E815101h]

Revision.

Return to [Summary Table](#)

**Table 5-2779. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0000h       |

**Figure 5-917. MPU\_16\_REVISION Name Register**

|           |    |          |    |       |        |    |    |
|-----------|----|----------|----|-------|--------|----|----|
| 31        | 30 | 29       | 28 | 27    | 26     | 25 | 24 |
| SCHEME    |    | RESERVED |    | MODID |        |    |    |
| R         |    | R        |    | R     |        |    |    |
| 1h        |    | 0h       |    | E81h  |        |    |    |
| 23        | 22 | 21       | 20 | 19    | 18     | 17 | 16 |
| MODID     |    |          |    |       |        |    |    |
| R         |    |          |    |       |        |    |    |
| E81h      |    |          |    |       |        |    |    |
| 15        | 14 | 13       | 12 | 11    | 10     | 9  | 8  |
| REVRTL    |    |          |    |       | REVMAJ |    |    |
| R         |    |          |    |       | R      |    |    |
| Ah        |    |          |    |       | 1h     |    |    |
| 7         | 6  | 5        | 4  | 3     | 2      | 1  | 0  |
| REVCUSTOM |    | REVMIN   |    |       |        |    |    |
| R         |    | R        |    |       |        |    |    |
| 0h        |    | 1h       |    |       |        |    |    |

**Table 5-2781. MPU\_16\_REVISION Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                   |
|-------|-----------|------|-------|-----------------------------------------------|
| 31:30 | SCHEME    | R    | 1h    | Scheme.                                       |
| 29:28 | RESERVED  | R    | 0h    | Always read a s0. Writes have no affect.      |
| 27:16 | MODID     | R    | E81h  | Module ID field.                              |
| 15:11 | REVRTL    | R    | Ah    | RTL revision. Will vary depending on release. |
| 10:8  | REVMAJ    | R    | 1h    | Major revision.                               |
| 7:6   | REVCUSTOM | R    | 0h    | Custom revision.                              |
| 5:0   | REVMIN    | R    | 1h    | Minor revision.                               |

### 5.17.2.2 MPU\_16\_INTERRUPT\_RAW\_STATUS\_SET Register

#### 1 MPU\_16\_INTERRUPT\_RAW\_STATUS\_SET Register (Offset = 10h) [reset = 0h]

Interrupt\_Raw\_Status\_Set.

Return to [Summary Table](#)

**Table 5-2782. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0010h       |

**Figure 5-918. MPU\_16\_INTERRUPT\_RAW\_STATUS\_SET Name Register**

|          |    |    |    |    |    |          |          |
|----------|----|----|----|----|----|----------|----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25       | 24       |
| RESERVED |    |    |    |    |    |          |          |
| R        |    |    |    |    |    |          |          |
| 0h       |    |    |    |    |    |          |          |
| 23       | 22 | 21 | 20 | 19 | 18 | 17       | 16       |
| RESERVED |    |    |    |    |    |          |          |
| R        |    |    |    |    |    |          |          |
| 0h       |    |    |    |    |    |          |          |
| 15       | 14 | 13 | 12 | 11 | 10 | 9        | 8        |
| RESERVED |    |    |    |    |    |          |          |
| R        |    |    |    |    |    |          |          |
| 0h       |    |    |    |    |    |          |          |
| 7        | 6  | 5  | 4  | 3  | 2  | 1        | 0        |
| RESERVED |    |    |    |    |    | ADDR_ERR | PROT_ERR |
| R        |    |    |    |    |    | R/W1TS   | R/W1TS   |
| 0h       |    |    |    |    |    | 0h       | 0h       |

**Table 5-2784. MPU\_16\_INTERRUPT\_RAW\_STATUS\_SET Register Field Descriptions**

| Bit  | Field    | Type   | Reset | Description                                                                                             |
|------|----------|--------|-------|---------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED | R      | 0h    | Always read as 0.                                                                                       |
| 1    | ADDR_ERR | R/W1TS | 0h    | Addressing violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. |
| 0    | PROT_ERR | R/W1TS | 0h    | Protection violation error. Raw status is read. Write a 1 to set the status. Writing a 0 has no effect. |

### 5.17.2.3 MPU\_16\_INTERRUPT\_ENABLED\_STATUS\_CLEAR Register

#### 1 MPU\_16\_INTERRUPT\_ENABLED\_STATUS\_CLEAR Register (Offset = 14h) [reset = 0h]

Interrupt\_Enabled\_Status\_Clear.

Return to [Summary Table](#)

**Table 5-2785. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0014h       |

**Figure 5-919. MPU\_16\_INTERRUPT\_ENABLED\_STATUS\_CLEAR Name Register**

|          |    |    |    |    |    |                  |                  |
|----------|----|----|----|----|----|------------------|------------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25               | 24               |
| RESERVED |    |    |    |    |    |                  |                  |
| R        |    |    |    |    |    |                  |                  |
| 0h       |    |    |    |    |    |                  |                  |
| 23       | 22 | 21 | 20 | 19 | 18 | 17               | 16               |
| RESERVED |    |    |    |    |    |                  |                  |
| R        |    |    |    |    |    |                  |                  |
| 0h       |    |    |    |    |    |                  |                  |
| 15       | 14 | 13 | 12 | 11 | 10 | 9                | 8                |
| RESERVED |    |    |    |    |    |                  |                  |
| R        |    |    |    |    |    |                  |                  |
| 0h       |    |    |    |    |    |                  |                  |
| 7        | 6  | 5  | 4  | 3  | 2  | 1                | 0                |
| RESERVED |    |    |    |    |    | ENABLED_ADDR_ERR | ENABLED_PROT_ERR |
| R        |    |    |    |    |    | R/W0TC           | R/W0TC           |
| 0h       |    |    |    |    |    | 0h               | 0h               |

**Table 5-2787. MPU\_16\_INTERRUPT\_ENABLED\_STATUS\_CLEAR Register Field Descriptions**

| Bit  | Field            | Type   | Reset | Description                                                                                                   |
|------|------------------|--------|-------|---------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED         | R      | 0h    | Always read as 0.                                                                                             |
| 1    | ENABLED_ADDR_ERR | R/W0TC | 0h    | Addressing violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. |
| 0    | ENABLED_PROT_ERR | R/W0TC | 0h    | Protection violation error. Enabled status is read. Write a 1 to clear the status. Writing a 0 has no effect. |

#### 5.17.2.4 MPU\_16\_INTERRUPT\_ENABLE Register

##### 1 MPU\_16\_INTERRUPT\_ENABLE Register (Offset = 18h) [reset = 0h]

Interrupt\_Enable.

Return to [Summary Table](#)

**Table 5-2788. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0018h       |

**Figure 5-920. MPU\_16\_INTERRUPT\_ENABLE Name Register**

|          |    |    |    |    |    |             |             |
|----------|----|----|----|----|----|-------------|-------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25          | 24          |
| RESERVED |    |    |    |    |    |             |             |
| R        |    |    |    |    |    |             |             |
| 0h       |    |    |    |    |    |             |             |
| 23       | 22 | 21 | 20 | 19 | 18 | 17          | 16          |
| RESERVED |    |    |    |    |    |             |             |
| R        |    |    |    |    |    |             |             |
| 0h       |    |    |    |    |    |             |             |
| 15       | 14 | 13 | 12 | 11 | 10 | 9           | 8           |
| RESERVED |    |    |    |    |    |             |             |
| R        |    |    |    |    |    |             |             |
| 0h       |    |    |    |    |    |             |             |
| 7        | 6  | 5  | 4  | 3  | 2  | 1           | 0           |
| RESERVED |    |    |    |    |    | ADDR_ERR_EN | PROT_ERR_EN |
| R        |    |    |    |    |    | R/W1TS      | R/W1TS      |
| 0h       |    |    |    |    |    | 0h          | 0h          |

**Table 5-2790. MPU\_16\_INTERRUPT\_ENABLE Register Field Descriptions**

| Bit  | Field       | Type   | Reset | Description                                                                                |
|------|-------------|--------|-------|--------------------------------------------------------------------------------------------|
| 31:2 | RESERVED    | R      | 0h    | Always read as 0.                                                                          |
| 1    | ADDR_ERR_EN | R/W1TS | 0h    | Addressing violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. |
| 0    | PROT_ERR_EN | R/W1TS | 0h    | Protection violation error enable. Write a 1 to set the enable. Writing a 0 has no effect. |

### 5.17.2.5 MPU\_16\_INTERRUPT\_ENABLE\_CLEAR Register

#### 1 MPU\_16\_INTERRUPT\_ENABLE\_CLEAR Register (Offset = 1Ch) [reset = 0h]

Interrupt\_Enable\_Clear.

Return to [Summary Table](#)

**Table 5-2791. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 001Ch       |

**Figure 5-921. MPU\_16\_INTERRUPT\_ENABLE\_CLEAR Name Register**

|          |    |    |    |    |    |                 |                 |
|----------|----|----|----|----|----|-----------------|-----------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25              | 24              |
| RESERVED |    |    |    |    |    |                 |                 |
| R        |    |    |    |    |    |                 |                 |
| 0h       |    |    |    |    |    |                 |                 |
| 23       | 22 | 21 | 20 | 19 | 18 | 17              | 16              |
| RESERVED |    |    |    |    |    |                 |                 |
| R        |    |    |    |    |    |                 |                 |
| 0h       |    |    |    |    |    |                 |                 |
| 15       | 14 | 13 | 12 | 11 | 10 | 9               | 8               |
| RESERVED |    |    |    |    |    |                 |                 |
| R        |    |    |    |    |    |                 |                 |
| 0h       |    |    |    |    |    |                 |                 |
| 7        | 6  | 5  | 4  | 3  | 2  | 1               | 0               |
| RESERVED |    |    |    |    |    | ADDR_ERR_EN_CLR | PROT_ERR_EN_CLR |
| R        |    |    |    |    |    | R/W0TC          | R/W0TC          |
| 0h       |    |    |    |    |    | 0h              | 0h              |

**Table 5-2793. MPU\_16\_INTERRUPT\_ENABLE\_CLEAR Register Field Descriptions**

| Bit  | Field           | Type   | Reset | Description                                                                                  |
|------|-----------------|--------|-------|----------------------------------------------------------------------------------------------|
| 31:2 | RESERVED        | R      | 0h    | Always read as 0.                                                                            |
| 1    | ADDR_ERR_EN_CLR | R/W0TC | 0h    | Addressing violation error enable. Write a 1 to clear the enable. Writing a 0 has no effect. |
| 0    | PROT_ERR_EN_CLR | R/W0TC | 0h    | Protection violation error enable. Write a 1 to clear the enable. Writing a 0 has no effect. |

### 5.17.2.6 MPU\_16\_PROGRAMMABLE\_1\_START\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_1\_START\_ADDRESS Register (Offset = 200h) [reset = 0h]

Programmable\_1\_Start\_Address.

Return to [Summary Table](#)

**Table 5-2794. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0200h       |

**Figure 5-922. MPU\_16\_PROGRAMMABLE\_1\_START\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2796. MPU\_16\_PROGRAMMABLE\_1\_START\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                |
|------|------------|------|-------|------------------------------------------------------------|
| 31:0 | START_ADDR | R/W  | 0h    | Start address for range N. Defaults to input signal value. |

### 5.17.2.7 MPU\_16\_PROGRAMMABLE\_1\_END\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_1\_END\_ADDRESS Register (Offset = 204h) [reset = 0h]

Programmable\_1\_End\_Address.

Return to [Summary Table](#)

**Table 5-2797. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0204h       |

**Figure 5-923. MPU\_16\_PROGRAMMABLE\_1\_END\_ADDRESS Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2799. MPU\_16\_PROGRAMMABLE\_1\_END\_ADDRESS Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                              |
|------|----------|------|-------|----------------------------------------------------------|
| 31:0 | END_ADDR | R/W  | 0h    | End address for range N. Defaults to input signal value. |

### 5.17.2.8 MPU\_16\_PROGRAMMABLE\_1\_MPPA Register

#### 1 MPU\_16\_PROGRAMMABLE\_1\_MPPA Register (Offset = 208h) [reset = 0h]

Programmable\_1\_MPPA.

Return to [Summary Table](#)

**Table 5-2800. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0208h       |

**Figure 5-924. MPU\_16\_PROGRAMMABLE\_1\_MPPA Name Register**

| 31        | 30  | 29  | 28   | 27        | 26  | 25      | 24        |
|-----------|-----|-----|------|-----------|-----|---------|-----------|
| RESERVED3 |     |     | LOCK | RESERVED2 |     | AID15_0 |           |
| R         |     |     | R/W  | R         |     | R/W     |           |
| 0h        |     |     | 0h   | 0h        |     | 0h      |           |
| 23        | 22  | 21  | 20   | 19        | 18  | 17      | 16        |
| AID15_0   |     |     |      |           |     |         |           |
| R/W       |     |     |      |           |     |         |           |
| 0h        |     |     |      |           |     |         |           |
| 15        | 14  | 13  | 12   | 11        | 10  | 9       | 8         |
| AID15_0   |     |     |      |           |     | AIDX    | RESERVED1 |
| R/W       |     |     |      |           |     | R/W     | R         |
| 0h        |     |     |      |           |     | 0h      | 0h        |
| 7         | 6   | 5   | 4    | 3         | 2   | 1       | 0         |
| NS        | EMU | SR  | SW   | SX        | UR  | UW      | UX        |
| R/W       | R/W | R/W | R/W  | R/W       | R/W | R/W     | R/W       |
| 0h        | 0h  | 0h  | 0h   | 0h        | 0h  | 0h      | 0h        |

**Table 5-2802. MPU\_16\_PROGRAMMABLE\_1\_MPPA Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED3 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                     |
| 28    | LOCK      | R/W  | 0h    | this field is used for locking the corresponding MPU region configurations.<br>Write 1 to lock the configurations along with the lock bit.<br>Writing 1 is allowed once per boot.<br>Lock bit will clear on reset only.<br>Once locked SW can not modify the MPU configurations along with lock bit. |
| 27:26 | RESERVED2 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 25:10 | AID15_0   | R/W  | 0h    | AIDs checked for this region. Defaults to input value.<br>0 = AID is not checked for these permissions.<br>1 = AID is checked for these permissions.                                                                                                                                                 |
| 9     | AIDX      | R/W  | 0h    | Additional AIDs checked. Defaults to input value.                                                                                                                                                                                                                                                    |
| 8     | RESERVED1 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 7     | NS        | R/W  | 0h    | Non-secure permission. Defaults to input value.                                                                                                                                                                                                                                                      |
| 6     | EMU       | R/W  | 0h    | Debug permission. Defaults to input value.                                                                                                                                                                                                                                                           |
| 5     | SR        | R/W  | 0h    | Supervisor read permission. Defaults to input value.                                                                                                                                                                                                                                                 |
| 4     | SW        | R/W  | 0h    | Supervisor write permission. Defaults to input value.                                                                                                                                                                                                                                                |
| 3     | SX        | R/W  | 0h    | Supervisor executable permission. Defaults to input value.                                                                                                                                                                                                                                           |
| 2     | UR        | R/W  | 0h    | User read permission. Defaults to input value.                                                                                                                                                                                                                                                       |



**Table 5-2802. MPU\_16\_PROGRAMMABLE\_1\_MPPA Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                          |
|-----|-------|------|-------|------------------------------------------------------|
| 1   | UW    | R/W  | 0h    | User write permission. Defaults to input value.      |
| 0   | UX    | R/W  | 0h    | User executable permission. Defaults to input value. |

### 5.17.2.9 MPU\_16\_PROGRAMMABLE\_2\_START\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_2\_START\_ADDRESS Register (Offset = 210h) [reset = 0h]

Programmable\_2\_Start\_Address.

Return to [Summary Table](#)

**Table 5-2803. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0210h       |

**Figure 5-925. MPU\_16\_PROGRAMMABLE\_2\_START\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2805. MPU\_16\_PROGRAMMABLE\_2\_START\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                |
|------|------------|------|-------|------------------------------------------------------------|
| 31:0 | START_ADDR | R/W  | 0h    | Start address for range N. Defaults to input signal value. |

### 5.17.2.10 MPU\_16\_PROGRAMMABLE\_2\_END\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_2\_END\_ADDRESS Register (Offset = 214h) [reset = 0h]

Programmable\_2\_End\_Address.

Return to [Summary Table](#)

**Table 5-2806. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0214h       |

**Figure 5-926. MPU\_16\_PROGRAMMABLE\_2\_END\_ADDRESS Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2808. MPU\_16\_PROGRAMMABLE\_2\_END\_ADDRESS Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                              |
|------|----------|------|-------|----------------------------------------------------------|
| 31:0 | END_ADDR | R/W  | 0h    | End address for range N. Defaults to input signal value. |

### 5.17.2.11 MPU\_16\_PROGRAMMABLE\_2\_MPPA Register

#### 1 MPU\_16\_PROGRAMMABLE\_2\_MPPA Register (Offset = 218h) [reset = 0h]

Programmable\_2\_MPPA.

Return to [Summary Table](#)

**Table 5-2809. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0218h       |

**Figure 5-927. MPU\_16\_PROGRAMMABLE\_2\_MPPA Name Register**

| 31        | 30  | 29  | 28   | 27        | 26  | 25      | 24        |
|-----------|-----|-----|------|-----------|-----|---------|-----------|
| RESERVED3 |     |     | LOCK | RESERVED2 |     | AID15_0 |           |
| R         |     |     | R/W  | R         |     | R/W     |           |
| 0h        |     |     | 0h   | 0h        |     | 0h      |           |
| 23        | 22  | 21  | 20   | 19        | 18  | 17      | 16        |
| AID15_0   |     |     |      |           |     |         |           |
| R/W       |     |     |      |           |     |         |           |
| 0h        |     |     |      |           |     |         |           |
| 15        | 14  | 13  | 12   | 11        | 10  | 9       | 8         |
| AID15_0   |     |     |      |           |     | AIDX    | RESERVED1 |
| R/W       |     |     |      |           |     | R/W     | R         |
| 0h        |     |     |      |           |     | 0h      | 0h        |
| 7         | 6   | 5   | 4    | 3         | 2   | 1       | 0         |
| NS        | EMU | SR  | SW   | SX        | UR  | UW      | UX        |
| R/W       | R/W | R/W | R/W  | R/W       | R/W | R/W     | R/W       |
| 0h        | 0h  | 0h  | 0h   | 0h        | 0h  | 0h      | 0h        |

**Table 5-2811. MPU\_16\_PROGRAMMABLE\_2\_MPPA Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED3 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                     |
| 28    | LOCK      | R/W  | 0h    | this field is used for locking the corresponding MPU region configurations.<br>Write 1 to lock the configurations along with the lock bit.<br>Writing 1 is allowed once per boot.<br>Lock bit will clear on reset only.<br>Once locked SW can not modify the MPU configurations along with lock bit. |
| 27:26 | RESERVED2 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 25:10 | AID15_0   | R/W  | 0h    | AIDs checked for this region. Defaults to input value.<br>0 = AID is not checked for these permissions.<br>1 = AID is checked for these permissions.                                                                                                                                                 |
| 9     | AIDX      | R/W  | 0h    | Additional AIDs checked. Defaults to input value.                                                                                                                                                                                                                                                    |
| 8     | RESERVED1 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 7     | NS        | R/W  | 0h    | Non-secure permission. Defaults to input value.                                                                                                                                                                                                                                                      |
| 6     | EMU       | R/W  | 0h    | Debug permission. Defaults to input value.                                                                                                                                                                                                                                                           |
| 5     | SR        | R/W  | 0h    | Supervisor read permission. Defaults to input value.                                                                                                                                                                                                                                                 |
| 4     | SW        | R/W  | 0h    | Supervisor write permission. Defaults to input value.                                                                                                                                                                                                                                                |
| 3     | SX        | R/W  | 0h    | Supervisor executable permission. Defaults to input value.                                                                                                                                                                                                                                           |
| 2     | UR        | R/W  | 0h    | User read permission. Defaults to input value.                                                                                                                                                                                                                                                       |

**Table 5-2811. MPU\_16\_PROGRAMMABLE\_2\_MPPA Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                          |
|-----|-------|------|-------|------------------------------------------------------|
| 1   | UW    | R/W  | 0h    | User write permission. Defaults to input value.      |
| 0   | UX    | R/W  | 0h    | User executable permission. Defaults to input value. |

### 5.17.2.12 MPU\_16\_PROGRAMMABLE\_3\_START\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_3\_START\_ADDRESS Register (Offset = 220h) [reset = 0h]

Programmable\_3\_Start\_Address.

Return to [Summary Table](#)

**Table 5-2812. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0220h       |

**Figure 5-928. MPU\_16\_PROGRAMMABLE\_3\_START\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2814. MPU\_16\_PROGRAMMABLE\_3\_START\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                |
|------|------------|------|-------|------------------------------------------------------------|
| 31:0 | START_ADDR | R/W  | 0h    | Start address for range N. Defaults to input signal value. |

### 5.17.2.13 MPU\_16\_PROGRAMMABLE\_3\_END\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_3\_END\_ADDRESS Register (Offset = 224h) [reset = 0h]

Programmable\_3\_End\_Address.

Return to [Summary Table](#)

**Table 5-2815. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0224h       |

**Figure 5-929. MPU\_16\_PROGRAMMABLE\_3\_END\_ADDRESS Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2817. MPU\_16\_PROGRAMMABLE\_3\_END\_ADDRESS Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                              |
|------|----------|------|-------|----------------------------------------------------------|
| 31:0 | END_ADDR | R/W  | 0h    | End address for range N. Defaults to input signal value. |

#### 5.17.2.14 MPU\_16\_PROGRAMMABLE\_3\_MPPA Register

##### 1 MPU\_16\_PROGRAMMABLE\_3\_MPPA Register (Offset = 228h) [reset = 0h]

Programmable\_3\_MPPA.

Return to [Summary Table](#)

**Table 5-2818. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0228h       |

**Figure 5-930. MPU\_16\_PROGRAMMABLE\_3\_MPPA Name Register**

| 31        | 30  | 29  | 28   | 27        | 26  | 25      | 24        |
|-----------|-----|-----|------|-----------|-----|---------|-----------|
| RESERVED3 |     |     | LOCK | RESERVED2 |     | AID15_0 |           |
| R         |     |     | R/W  | R         |     | R/W     |           |
| 0h        |     |     | 0h   | 0h        |     | 0h      |           |
| 23        | 22  | 21  | 20   | 19        | 18  | 17      | 16        |
| AID15_0   |     |     |      |           |     |         |           |
| R/W       |     |     |      |           |     |         |           |
| 0h        |     |     |      |           |     |         |           |
| 15        | 14  | 13  | 12   | 11        | 10  | 9       | 8         |
| AID15_0   |     |     |      |           |     | AIDX    | RESERVED1 |
| R/W       |     |     |      |           |     | R/W     | R         |
| 0h        |     |     |      |           |     | 0h      | 0h        |
| 7         | 6   | 5   | 4    | 3         | 2   | 1       | 0         |
| NS        | EMU | SR  | SW   | SX        | UR  | UW      | UX        |
| R/W       | R/W | R/W | R/W  | R/W       | R/W | R/W     | R/W       |
| 0h        | 0h  | 0h  | 0h   | 0h        | 0h  | 0h      | 0h        |

**Table 5-2820. MPU\_16\_PROGRAMMABLE\_3\_MPPA Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED3 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                     |
| 28    | LOCK      | R/W  | 0h    | this field is used for locking the corresponding MPU region configurations.<br>Write 1 to lock the configurations along with the lock bit.<br>Writing 1 is allowed once per boot.<br>Lock bit will clear on reset only.<br>Once locked SW can not modify the MPU configurations along with lock bit. |
| 27:26 | RESERVED2 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 25:10 | AID15_0   | R/W  | 0h    | AIDs checked for this region. Defaults to input value.<br>0 = AID is not checked for these permissions.<br>1 = AID is checked for these permissions.                                                                                                                                                 |
| 9     | AIDX      | R/W  | 0h    | Additional AIDs checked. Defaults to input value.                                                                                                                                                                                                                                                    |
| 8     | RESERVED1 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 7     | NS        | R/W  | 0h    | Non-secure permission. Defaults to input value.                                                                                                                                                                                                                                                      |
| 6     | EMU       | R/W  | 0h    | Debug permission. Defaults to input value.                                                                                                                                                                                                                                                           |
| 5     | SR        | R/W  | 0h    | Supervisor read permission. Defaults to input value.                                                                                                                                                                                                                                                 |
| 4     | SW        | R/W  | 0h    | Supervisor write permission. Defaults to input value.                                                                                                                                                                                                                                                |
| 3     | SX        | R/W  | 0h    | Supervisor executable permission. Defaults to input value.                                                                                                                                                                                                                                           |
| 2     | UR        | R/W  | 0h    | User read permission. Defaults to input value.                                                                                                                                                                                                                                                       |



**Table 5-2820. MPU\_16\_PROGRAMMABLE\_3\_MPPA Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                          |
|-----|-------|------|-------|------------------------------------------------------|
| 1   | UW    | R/W  | 0h    | User write permission. Defaults to input value.      |
| 0   | UX    | R/W  | 0h    | User executable permission. Defaults to input value. |

### 5.17.2.15 MPU\_16\_PROGRAMMABLE\_4\_START\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_4\_START\_ADDRESS Register (Offset = 230h) [reset = 0h]

Programmable\_4\_Start\_Address.

Return to [Summary Table](#)

**Table 5-2821. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0230h       |

**Figure 5-931. MPU\_16\_PROGRAMMABLE\_4\_START\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2823. MPU\_16\_PROGRAMMABLE\_4\_START\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                |
|------|------------|------|-------|------------------------------------------------------------|
| 31:0 | START_ADDR | R/W  | 0h    | Start address for range N. Defaults to input signal value. |

### 5.17.2.16 MPU\_16\_PROGRAMMABLE\_4\_END\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_4\_END\_ADDRESS Register (Offset = 234h) [reset = 0h]

Programmable\_4\_End\_Address.

Return to [Summary Table](#)

**Table 5-2824. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0234h       |

**Figure 5-932. MPU\_16\_PROGRAMMABLE\_4\_END\_ADDRESS Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2826. MPU\_16\_PROGRAMMABLE\_4\_END\_ADDRESS Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                              |
|------|----------|------|-------|----------------------------------------------------------|
| 31:0 | END_ADDR | R/W  | 0h    | End address for range N. Defaults to input signal value. |

### 5.17.2.17 MPU\_16\_PROGRAMMABLE\_4\_MPPA Register

#### 1 MPU\_16\_PROGRAMMABLE\_4\_MPPA Register (Offset = 238h) [reset = 0h]

Programmable\_4\_MPPA.

Return to [Summary Table](#)

**Table 5-2827. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0238h       |

**Figure 5-933. MPU\_16\_PROGRAMMABLE\_4\_MPPA Name Register**

| 31        | 30  | 29  | 28   | 27        | 26  | 25      | 24        |
|-----------|-----|-----|------|-----------|-----|---------|-----------|
| RESERVED3 |     |     | LOCK | RESERVED2 |     | AID15_0 |           |
| R         |     |     | R/W  | R         |     | R/W     |           |
| 0h        |     |     | 0h   | 0h        |     | 0h      |           |
| 23        | 22  | 21  | 20   | 19        | 18  | 17      | 16        |
| AID15_0   |     |     |      |           |     |         |           |
| R/W       |     |     |      |           |     |         |           |
| 0h        |     |     |      |           |     |         |           |
| 15        | 14  | 13  | 12   | 11        | 10  | 9       | 8         |
| AID15_0   |     |     |      |           |     | AIDX    | RESERVED1 |
| R/W       |     |     |      |           |     | R/W     | R         |
| 0h        |     |     |      |           |     | 0h      | 0h        |
| 7         | 6   | 5   | 4    | 3         | 2   | 1       | 0         |
| NS        | EMU | SR  | SW   | SX        | UR  | UW      | UX        |
| R/W       | R/W | R/W | R/W  | R/W       | R/W | R/W     | R/W       |
| 0h        | 0h  | 0h  | 0h   | 0h        | 0h  | 0h      | 0h        |

**Table 5-2829. MPU\_16\_PROGRAMMABLE\_4\_MPPA Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED3 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                     |
| 28    | LOCK      | R/W  | 0h    | this field is used for locking the corresponding MPU region configurations.<br>Write 1 to lock the configurations along with the lock bit.<br>Writing 1 is allowed once per boot.<br>Lock bit will clear on reset only.<br>Once locked SW can not modify the MPU configurations along with lock bit. |
| 27:26 | RESERVED2 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 25:10 | AID15_0   | R/W  | 0h    | AIDs checked for this region. Defaults to input value.<br>0 = AID is not checked for these permissions.<br>1 = AID is checked for these permissions.                                                                                                                                                 |
| 9     | AIDX      | R/W  | 0h    | Additional AIDs checked. Defaults to input value.                                                                                                                                                                                                                                                    |
| 8     | RESERVED1 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 7     | NS        | R/W  | 0h    | Non-secure permission. Defaults to input value.                                                                                                                                                                                                                                                      |
| 6     | EMU       | R/W  | 0h    | Debug permission. Defaults to input value.                                                                                                                                                                                                                                                           |
| 5     | SR        | R/W  | 0h    | Supervisor read permission. Defaults to input value.                                                                                                                                                                                                                                                 |
| 4     | SW        | R/W  | 0h    | Supervisor write permission. Defaults to input value.                                                                                                                                                                                                                                                |
| 3     | SX        | R/W  | 0h    | Supervisor executable permission. Defaults to input value.                                                                                                                                                                                                                                           |
| 2     | UR        | R/W  | 0h    | User read permission. Defaults to input value.                                                                                                                                                                                                                                                       |

**Table 5-2829. MPU\_16\_PROGRAMMABLE\_4\_MPPA Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                          |
|-----|-------|------|-------|------------------------------------------------------|
| 1   | UW    | R/W  | 0h    | User write permission. Defaults to input value.      |
| 0   | UX    | R/W  | 0h    | User executable permission. Defaults to input value. |

### 5.17.2.18 MPU\_16\_PROGRAMMABLE\_5\_START\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_5\_START\_ADDRESS Register (Offset = 240h) [reset = 0h]

Programmable\_5\_Start\_Address.

Return to [Summary Table](#)

**Table 5-2830. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0240h       |

**Figure 5-934. MPU\_16\_PROGRAMMABLE\_5\_START\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2832. MPU\_16\_PROGRAMMABLE\_5\_START\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                |
|------|------------|------|-------|------------------------------------------------------------|
| 31:0 | START_ADDR | R/W  | 0h    | Start address for range N. Defaults to input signal value. |

### 5.17.2.19 MPU\_16\_PROGRAMMABLE\_5\_END\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_5\_END\_ADDRESS Register (Offset = 244h) [reset = 0h]

Programmable\_5\_End\_Address.

Return to [Summary Table](#)

**Table 5-2833. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0244h       |

**Figure 5-935. MPU\_16\_PROGRAMMABLE\_5\_END\_ADDRESS Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2835. MPU\_16\_PROGRAMMABLE\_5\_END\_ADDRESS Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                              |
|------|----------|------|-------|----------------------------------------------------------|
| 31:0 | END_ADDR | R/W  | 0h    | End address for range N. Defaults to input signal value. |

### 5.17.2.20 MPU\_16\_PROGRAMMABLE\_5\_MPPA Register

#### 1 MPU\_16\_PROGRAMMABLE\_5\_MPPA Register (Offset = 248h) [reset = 0h]

Programmable\_5\_MPPA.

Return to [Summary Table](#)

**Table 5-2836. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0248h       |

**Figure 5-936. MPU\_16\_PROGRAMMABLE\_5\_MPPA Name Register**

| 31        | 30  | 29  | 28   | 27        | 26  | 25      | 24        |
|-----------|-----|-----|------|-----------|-----|---------|-----------|
| RESERVED3 |     |     | LOCK | RESERVED2 |     | AID15_0 |           |
| R         |     |     | R/W  | R         |     | R/W     |           |
| 0h        |     |     | 0h   | 0h        |     | 0h      |           |
| 23        | 22  | 21  | 20   | 19        | 18  | 17      | 16        |
| AID15_0   |     |     |      |           |     |         |           |
| R/W       |     |     |      |           |     |         |           |
| 0h        |     |     |      |           |     |         |           |
| 15        | 14  | 13  | 12   | 11        | 10  | 9       | 8         |
| AID15_0   |     |     |      |           |     | AIDX    | RESERVED1 |
| R/W       |     |     |      |           |     | R/W     | R         |
| 0h        |     |     |      |           |     | 0h      | 0h        |
| 7         | 6   | 5   | 4    | 3         | 2   | 1       | 0         |
| NS        | EMU | SR  | SW   | SX        | UR  | UW      | UX        |
| R/W       | R/W | R/W | R/W  | R/W       | R/W | R/W     | R/W       |
| 0h        | 0h  | 0h  | 0h   | 0h        | 0h  | 0h      | 0h        |

**Table 5-2838. MPU\_16\_PROGRAMMABLE\_5\_MPPA Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED3 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                     |
| 28    | LOCK      | R/W  | 0h    | this field is used for locking the corresponding MPU region configurations.<br>Write 1 to lock the configurations along with the lock bit.<br>Writing 1 is allowed once per boot.<br>Lock bit will clear on reset only.<br>Once locked SW can not modify the MPU configurations along with lock bit. |
| 27:26 | RESERVED2 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 25:10 | AID15_0   | R/W  | 0h    | AIDs checked for this region. Defaults to input value.<br>0 = AID is not checked for these permissions.<br>1 = AID is checked for these permissions.                                                                                                                                                 |
| 9     | AIDX      | R/W  | 0h    | Additional AIDs checked. Defaults to input value.                                                                                                                                                                                                                                                    |
| 8     | RESERVED1 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 7     | NS        | R/W  | 0h    | Non-secure permission. Defaults to input value.                                                                                                                                                                                                                                                      |
| 6     | EMU       | R/W  | 0h    | Debug permission. Defaults to input value.                                                                                                                                                                                                                                                           |
| 5     | SR        | R/W  | 0h    | Supervisor read permission. Defaults to input value.                                                                                                                                                                                                                                                 |
| 4     | SW        | R/W  | 0h    | Supervisor write permission. Defaults to input value.                                                                                                                                                                                                                                                |
| 3     | SX        | R/W  | 0h    | Supervisor executable permission. Defaults to input value.                                                                                                                                                                                                                                           |
| 2     | UR        | R/W  | 0h    | User read permission. Defaults to input value.                                                                                                                                                                                                                                                       |



**Table 5-2838. MPU\_16\_PROGRAMMABLE\_5\_MPPA Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                          |
|-----|-------|------|-------|------------------------------------------------------|
| 1   | UW    | R/W  | 0h    | User write permission. Defaults to input value.      |
| 0   | UX    | R/W  | 0h    | User executable permission. Defaults to input value. |

### 5.17.2.21 MPU\_16\_PROGRAMMABLE\_6\_START\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_6\_START\_ADDRESS Register (Offset = 250h) [reset = 0h]

Programmable\_6\_Start\_Address.

Return to [Summary Table](#)

**Table 5-2839. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0250h       |

**Figure 5-937. MPU\_16\_PROGRAMMABLE\_6\_START\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2841. MPU\_16\_PROGRAMMABLE\_6\_START\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                |
|------|------------|------|-------|------------------------------------------------------------|
| 31:0 | START_ADDR | R/W  | 0h    | Start address for range N. Defaults to input signal value. |

### 5.17.2.22 MPU\_16\_PROGRAMMABLE\_6\_END\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_6\_END\_ADDRESS Register (Offset = 254h) [reset = 0h]

Programmable\_6\_End\_Address.

Return to [Summary Table](#)

**Table 5-2842. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0254h       |

**Figure 5-938. MPU\_16\_PROGRAMMABLE\_6\_END\_ADDRESS Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2844. MPU\_16\_PROGRAMMABLE\_6\_END\_ADDRESS Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                              |
|------|----------|------|-------|----------------------------------------------------------|
| 31:0 | END_ADDR | R/W  | 0h    | End address for range N. Defaults to input signal value. |

### 5.17.2.23 MPU\_16\_PROGRAMMABLE\_6\_MPPA Register

#### 1 MPU\_16\_PROGRAMMABLE\_6\_MPPA Register (Offset = 258h) [reset = 0h]

Programmable\_6\_MPPA.

Return to [Summary Table](#)

**Table 5-2845. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0258h       |

**Figure 5-939. MPU\_16\_PROGRAMMABLE\_6\_MPPA Name Register**

| 31        | 30  | 29  | 28   | 27        | 26  | 25      | 24        |
|-----------|-----|-----|------|-----------|-----|---------|-----------|
| RESERVED3 |     |     | LOCK | RESERVED2 |     | AID15_0 |           |
| R         |     |     | R/W  | R         |     | R/W     |           |
| 0h        |     |     | 0h   | 0h        |     | 0h      |           |
| 23        | 22  | 21  | 20   | 19        | 18  | 17      | 16        |
| AID15_0   |     |     |      |           |     |         |           |
| R/W       |     |     |      |           |     |         |           |
| 0h        |     |     |      |           |     |         |           |
| 15        | 14  | 13  | 12   | 11        | 10  | 9       | 8         |
| AID15_0   |     |     |      |           |     | AIDX    | RESERVED1 |
| R/W       |     |     |      |           |     | R/W     | R         |
| 0h        |     |     |      |           |     | 0h      | 0h        |
| 7         | 6   | 5   | 4    | 3         | 2   | 1       | 0         |
| NS        | EMU | SR  | SW   | SX        | UR  | UW      | UX        |
| R/W       | R/W | R/W | R/W  | R/W       | R/W | R/W     | R/W       |
| 0h        | 0h  | 0h  | 0h   | 0h        | 0h  | 0h      | 0h        |

**Table 5-2847. MPU\_16\_PROGRAMMABLE\_6\_MPPA Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED3 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                     |
| 28    | LOCK      | R/W  | 0h    | this field is used for locking the corresponding MPU region configurations.<br>Write 1 to lock the configurations along with the lock bit.<br>Writing 1 is allowed once per boot.<br>Lock bit will clear on reset only.<br>Once locked SW can not modify the MPU configurations along with lock bit. |
| 27:26 | RESERVED2 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 25:10 | AID15_0   | R/W  | 0h    | AIDs checked for this region. Defaults to input value.<br>0 = AID is not checked for these permissions.<br>1 = AID is checked for these permissions.                                                                                                                                                 |
| 9     | AIDX      | R/W  | 0h    | Additional AIDs checked. Defaults to input value.                                                                                                                                                                                                                                                    |
| 8     | RESERVED1 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 7     | NS        | R/W  | 0h    | Non-secure permission. Defaults to input value.                                                                                                                                                                                                                                                      |
| 6     | EMU       | R/W  | 0h    | Debug permission. Defaults to input value.                                                                                                                                                                                                                                                           |
| 5     | SR        | R/W  | 0h    | Supervisor read permission. Defaults to input value.                                                                                                                                                                                                                                                 |
| 4     | SW        | R/W  | 0h    | Supervisor write permission. Defaults to input value.                                                                                                                                                                                                                                                |
| 3     | SX        | R/W  | 0h    | Supervisor executable permission. Defaults to input value.                                                                                                                                                                                                                                           |
| 2     | UR        | R/W  | 0h    | User read permission. Defaults to input value.                                                                                                                                                                                                                                                       |

**Table 5-2847. MPU\_16\_PROGRAMMABLE\_6\_MPPA Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                          |
|-----|-------|------|-------|------------------------------------------------------|
| 1   | UW    | R/W  | 0h    | User write permission. Defaults to input value.      |
| 0   | UX    | R/W  | 0h    | User executable permission. Defaults to input value. |

#### 5.17.2.24 MPU\_16\_PROGRAMMABLE\_7\_START\_ADDRESS Register

##### 1 MPU\_16\_PROGRAMMABLE\_7\_START\_ADDRESS Register (Offset = 260h) [reset = 0h]

Programmable\_7\_Start\_Address.

Return to [Summary Table](#)

**Table 5-2848. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0260h       |

**Figure 5-940. MPU\_16\_PROGRAMMABLE\_7\_START\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2850. MPU\_16\_PROGRAMMABLE\_7\_START\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                |
|------|------------|------|-------|------------------------------------------------------------|
| 31:0 | START_ADDR | R/W  | 0h    | Start address for range N. Defaults to input signal value. |

### 5.17.2.25 MPU\_16\_PROGRAMMABLE\_7\_END\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_7\_END\_ADDRESS Register (Offset = 264h) [reset = 0h]

Programmable\_7\_End\_Address.

Return to [Summary Table](#)

**Table 5-2851. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0264h       |

**Figure 5-941. MPU\_16\_PROGRAMMABLE\_7\_END\_ADDRESS Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2853. MPU\_16\_PROGRAMMABLE\_7\_END\_ADDRESS Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                              |
|------|----------|------|-------|----------------------------------------------------------|
| 31:0 | END_ADDR | R/W  | 0h    | End address for range N. Defaults to input signal value. |

### 5.17.2.26 MPU\_16\_PROGRAMMABLE\_7\_MPPA Register

#### 1 MPU\_16\_PROGRAMMABLE\_7\_MPPA Register (Offset = 268h) [reset = 0h]

Programmable\_7\_MPPA.

Return to [Summary Table](#)

**Table 5-2854. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0268h       |

**Figure 5-942. MPU\_16\_PROGRAMMABLE\_7\_MPPA Name Register**

| 31        | 30  | 29  | 28   | 27        | 26  | 25      | 24        |
|-----------|-----|-----|------|-----------|-----|---------|-----------|
| RESERVED3 |     |     | LOCK | RESERVED2 |     | AID15_0 |           |
| R         |     |     | R/W  | R         |     | R/W     |           |
| 0h        |     |     | 0h   | 0h        |     | 0h      |           |
| 23        | 22  | 21  | 20   | 19        | 18  | 17      | 16        |
| AID15_0   |     |     |      |           |     |         |           |
| R/W       |     |     |      |           |     |         |           |
| 0h        |     |     |      |           |     |         |           |
| 15        | 14  | 13  | 12   | 11        | 10  | 9       | 8         |
| AID15_0   |     |     |      |           |     | AIDX    | RESERVED1 |
| R/W       |     |     |      |           |     | R/W     | R         |
| 0h        |     |     |      |           |     | 0h      | 0h        |
| 7         | 6   | 5   | 4    | 3         | 2   | 1       | 0         |
| NS        | EMU | SR  | SW   | SX        | UR  | UW      | UX        |
| R/W       | R/W | R/W | R/W  | R/W       | R/W | R/W     | R/W       |
| 0h        | 0h  | 0h  | 0h   | 0h        | 0h  | 0h      | 0h        |

**Table 5-2856. MPU\_16\_PROGRAMMABLE\_7\_MPPA Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED3 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                     |
| 28    | LOCK      | R/W  | 0h    | this field is used for locking the corresponding MPU region configurations.<br>Write 1 to lock the configurations along with the lock bit.<br>Writing 1 is allowed once per boot.<br>Lock bit will clear on reset only.<br>Once locked SW can not modify the MPU configurations along with lock bit. |
| 27:26 | RESERVED2 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 25:10 | AID15_0   | R/W  | 0h    | AIDs checked for this region. Defaults to input value.<br>0 = AID is not checked for these permissions.<br>1 = AID is checked for these permissions.                                                                                                                                                 |
| 9     | AIDX      | R/W  | 0h    | Additional AIDs checked. Defaults to input value.                                                                                                                                                                                                                                                    |
| 8     | RESERVED1 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 7     | NS        | R/W  | 0h    | Non-secure permission. Defaults to input value.                                                                                                                                                                                                                                                      |
| 6     | EMU       | R/W  | 0h    | Debug permission. Defaults to input value.                                                                                                                                                                                                                                                           |
| 5     | SR        | R/W  | 0h    | Supervisor read permission. Defaults to input value.                                                                                                                                                                                                                                                 |
| 4     | SW        | R/W  | 0h    | Supervisor write permission. Defaults to input value.                                                                                                                                                                                                                                                |
| 3     | SX        | R/W  | 0h    | Supervisor executable permission. Defaults to input value.                                                                                                                                                                                                                                           |
| 2     | UR        | R/W  | 0h    | User read permission. Defaults to input value.                                                                                                                                                                                                                                                       |



**Table 5-2856. MPU\_16\_PROGRAMMABLE\_7\_MPPA Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                          |
|-----|-------|------|-------|------------------------------------------------------|
| 1   | UW    | R/W  | 0h    | User write permission. Defaults to input value.      |
| 0   | UX    | R/W  | 0h    | User executable permission. Defaults to input value. |

### 5.17.2.27 MPU\_16\_PROGRAMMABLE\_8\_START\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_8\_START\_ADDRESS Register (Offset = 270h) [reset = 0h]

Programmable\_8\_Start\_Address.

Return to [Summary Table](#)

**Table 5-2857. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0270h       |

**Figure 5-943. MPU\_16\_PROGRAMMABLE\_8\_START\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2859. MPU\_16\_PROGRAMMABLE\_8\_START\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                |
|------|------------|------|-------|------------------------------------------------------------|
| 31:0 | START_ADDR | R/W  | 0h    | Start address for range N. Defaults to input signal value. |

### 5.17.2.28 MPU\_16\_PROGRAMMABLE\_8\_END\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_8\_END\_ADDRESS Register (Offset = 274h) [reset = 0h]

Programmable\_8\_End\_Address.

Return to [Summary Table](#)

**Table 5-2860. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0274h       |

**Figure 5-944. MPU\_16\_PROGRAMMABLE\_8\_END\_ADDRESS Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2862. MPU\_16\_PROGRAMMABLE\_8\_END\_ADDRESS Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                              |
|------|----------|------|-------|----------------------------------------------------------|
| 31:0 | END_ADDR | R/W  | 0h    | End address for range N. Defaults to input signal value. |

### 5.17.2.29 MPU\_16\_PROGRAMMABLE\_8\_MPPA Register

#### 1 MPU\_16\_PROGRAMMABLE\_8\_MPPA Register (Offset = 278h) [reset = 0h]

Programmable\_8\_MPPA.

Return to [Summary Table](#)

**Table 5-2863. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0278h       |

**Figure 5-945. MPU\_16\_PROGRAMMABLE\_8\_MPPA Name Register**

| 31        | 30  | 29  | 28   | 27        | 26  | 25      | 24        |
|-----------|-----|-----|------|-----------|-----|---------|-----------|
| RESERVED3 |     |     | LOCK | RESERVED2 |     | AID15_0 |           |
| R         |     |     | R/W  | R         |     | R/W     |           |
| 0h        |     |     | 0h   | 0h        |     | 0h      |           |
| 23        | 22  | 21  | 20   | 19        | 18  | 17      | 16        |
| AID15_0   |     |     |      |           |     |         |           |
| R/W       |     |     |      |           |     |         |           |
| 0h        |     |     |      |           |     |         |           |
| 15        | 14  | 13  | 12   | 11        | 10  | 9       | 8         |
| AID15_0   |     |     |      |           |     | AIDX    | RESERVED1 |
| R/W       |     |     |      |           |     | R/W     | R         |
| 0h        |     |     |      |           |     | 0h      | 0h        |
| 7         | 6   | 5   | 4    | 3         | 2   | 1       | 0         |
| NS        | EMU | SR  | SW   | SX        | UR  | UW      | UX        |
| R/W       | R/W | R/W | R/W  | R/W       | R/W | R/W     | R/W       |
| 0h        | 0h  | 0h  | 0h   | 0h        | 0h  | 0h      | 0h        |

**Table 5-2865. MPU\_16\_PROGRAMMABLE\_8\_MPPA Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED3 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                     |
| 28    | LOCK      | R/W  | 0h    | this field is used for locking the corresponding MPU region configurations.<br>Write 1 to lock the configurations along with the lock bit.<br>Writing 1 is allowed once per boot.<br>Lock bit will clear on reset only.<br>Once locked SW can not modify the MPU configurations along with lock bit. |
| 27:26 | RESERVED2 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 25:10 | AID15_0   | R/W  | 0h    | AIDs checked for this region. Defaults to input value.<br>0 = AID is not checked for these permissions.<br>1 = AID is checked for these permissions.                                                                                                                                                 |
| 9     | AIDX      | R/W  | 0h    | Additional AIDs checked. Defaults to input value.                                                                                                                                                                                                                                                    |
| 8     | RESERVED1 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 7     | NS        | R/W  | 0h    | Non-secure permission. Defaults to input value.                                                                                                                                                                                                                                                      |
| 6     | EMU       | R/W  | 0h    | Debug permission. Defaults to input value.                                                                                                                                                                                                                                                           |
| 5     | SR        | R/W  | 0h    | Supervisor read permission. Defaults to input value.                                                                                                                                                                                                                                                 |
| 4     | SW        | R/W  | 0h    | Supervisor write permission. Defaults to input value.                                                                                                                                                                                                                                                |
| 3     | SX        | R/W  | 0h    | Supervisor executable permission. Defaults to input value.                                                                                                                                                                                                                                           |
| 2     | UR        | R/W  | 0h    | User read permission. Defaults to input value.                                                                                                                                                                                                                                                       |

**Table 5-2865. MPU\_16\_PROGRAMMABLE\_8\_MPPA Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                          |
|-----|-------|------|-------|------------------------------------------------------|
| 1   | UW    | R/W  | 0h    | User write permission. Defaults to input value.      |
| 0   | UX    | R/W  | 0h    | User executable permission. Defaults to input value. |

### 5.17.2.30 MPU\_16\_PROGRAMMABLE\_9\_START\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_9\_START\_ADDRESS Register (Offset = 280h) [reset = 0h]

Programmable\_9\_Start\_Address.

Return to [Summary Table](#)

**Table 5-2866. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0280h       |

**Figure 5-946. MPU\_16\_PROGRAMMABLE\_9\_START\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2868. MPU\_16\_PROGRAMMABLE\_9\_START\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                |
|------|------------|------|-------|------------------------------------------------------------|
| 31:0 | START_ADDR | R/W  | 0h    | Start address for range N. Defaults to input signal value. |

### 5.17.2.31 MPU\_16\_PROGRAMMABLE\_9\_END\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_9\_END\_ADDRESS Register (Offset = 284h) [reset = 0h]

Programmable\_9\_End\_Address.

Return to [Summary Table](#)

**Table 5-2869. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0284h       |

**Figure 5-947. MPU\_16\_PROGRAMMABLE\_9\_END\_ADDRESS Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2871. MPU\_16\_PROGRAMMABLE\_9\_END\_ADDRESS Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                              |
|------|----------|------|-------|----------------------------------------------------------|
| 31:0 | END_ADDR | R/W  | 0h    | End address for range N. Defaults to input signal value. |

### 5.17.2.32 MPU\_16\_PROGRAMMABLE\_9\_MPPA Register

#### 1 MPU\_16\_PROGRAMMABLE\_9\_MPPA Register (Offset = 288h) [reset = 0h]

Programmable\_9\_MPPA.

Return to [Summary Table](#)

**Table 5-2872. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0288h       |

**Figure 5-948. MPU\_16\_PROGRAMMABLE\_9\_MPPA Name Register**

| 31        | 30  | 29  | 28   | 27        | 26  | 25      | 24        |
|-----------|-----|-----|------|-----------|-----|---------|-----------|
| RESERVED3 |     |     | LOCK | RESERVED2 |     | AID15_0 |           |
| R         |     |     | R/W  | R         |     | R/W     |           |
| 0h        |     |     | 0h   | 0h        |     | 0h      |           |
| 23        | 22  | 21  | 20   | 19        | 18  | 17      | 16        |
| AID15_0   |     |     |      |           |     |         |           |
| R/W       |     |     |      |           |     |         |           |
| 0h        |     |     |      |           |     |         |           |
| 15        | 14  | 13  | 12   | 11        | 10  | 9       | 8         |
| AID15_0   |     |     |      |           |     | AIDX    | RESERVED1 |
| R/W       |     |     |      |           |     | R/W     | R         |
| 0h        |     |     |      |           |     | 0h      | 0h        |
| 7         | 6   | 5   | 4    | 3         | 2   | 1       | 0         |
| NS        | EMU | SR  | SW   | SX        | UR  | UW      | UX        |
| R/W       | R/W | R/W | R/W  | R/W       | R/W | R/W     | R/W       |
| 0h        | 0h  | 0h  | 0h   | 0h        | 0h  | 0h      | 0h        |

**Table 5-2874. MPU\_16\_PROGRAMMABLE\_9\_MPPA Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED3 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                     |
| 28    | LOCK      | R/W  | 0h    | this field is used for locking the corresponding MPU region configurations.<br>Write 1 to lock the configurations along with the lock bit.<br>Writing 1 is allowed once per boot.<br>Lock bit will clear on reset only.<br>Once locked SW can not modify the MPU configurations along with lock bit. |
| 27:26 | RESERVED2 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 25:10 | AID15_0   | R/W  | 0h    | AIDs checked for this region. Defaults to input value.<br>0 = AID is not checked for these permissions.<br>1 = AID is checked for these permissions.                                                                                                                                                 |
| 9     | AIDX      | R/W  | 0h    | Additional AIDs checked. Defaults to input value.                                                                                                                                                                                                                                                    |
| 8     | RESERVED1 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 7     | NS        | R/W  | 0h    | Non-secure permission. Defaults to input value.                                                                                                                                                                                                                                                      |
| 6     | EMU       | R/W  | 0h    | Debug permission. Defaults to input value.                                                                                                                                                                                                                                                           |
| 5     | SR        | R/W  | 0h    | Supervisor read permission. Defaults to input value.                                                                                                                                                                                                                                                 |
| 4     | SW        | R/W  | 0h    | Supervisor write permission. Defaults to input value.                                                                                                                                                                                                                                                |
| 3     | SX        | R/W  | 0h    | Supervisor executable permission. Defaults to input value.                                                                                                                                                                                                                                           |
| 2     | UR        | R/W  | 0h    | User read permission. Defaults to input value.                                                                                                                                                                                                                                                       |



**Table 5-2874. MPU\_16\_PROGRAMMABLE\_9\_MPPA Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                          |
|-----|-------|------|-------|------------------------------------------------------|
| 1   | UW    | R/W  | 0h    | User write permission. Defaults to input value.      |
| 0   | UX    | R/W  | 0h    | User executable permission. Defaults to input value. |

### 5.17.2.33 MPU\_16\_PROGRAMMABLE\_10\_START\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_10\_START\_ADDRESS Register (Offset = 290h) [reset = 0h]

Programmable\_10\_Start\_Address.

Return to [Summary Table](#)

**Table 5-2875. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0290h       |

**Figure 5-949. MPU\_16\_PROGRAMMABLE\_10\_START\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2877. MPU\_16\_PROGRAMMABLE\_10\_START\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                |
|------|------------|------|-------|------------------------------------------------------------|
| 31:0 | START_ADDR | R/W  | 0h    | Start address for range N. Defaults to input signal value. |

### 5.17.2.34 MPU\_16\_PROGRAMMABLE\_10\_END\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_10\_END\_ADDRESS Register (Offset = 294h) [reset = 0h]

Programmable\_10\_End\_Address.

Return to [Summary Table](#)

**Table 5-2878. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0294h       |

**Figure 5-950. MPU\_16\_PROGRAMMABLE\_10\_END\_ADDRESS Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2880. MPU\_16\_PROGRAMMABLE\_10\_END\_ADDRESS Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                              |
|------|----------|------|-------|----------------------------------------------------------|
| 31:0 | END_ADDR | R/W  | 0h    | End address for range N. Defaults to input signal value. |

### 5.17.2.35 MPU\_16\_PROGRAMMABLE\_10\_MPPA Register

#### 1 MPU\_16\_PROGRAMMABLE\_10\_MPPA Register (Offset = 298h) [reset = 0h]

Programmable\_10\_MPPA.

Return to [Summary Table](#)

**Table 5-2881. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0298h       |

**Figure 5-951. MPU\_16\_PROGRAMMABLE\_10\_MPPA Name Register**

| 31        | 30  | 29  | 28   | 27        | 26  | 25      | 24        |
|-----------|-----|-----|------|-----------|-----|---------|-----------|
| RESERVED3 |     |     | LOCK | RESERVED2 |     | AID15_0 |           |
| R         |     |     | R/W  | R         |     | R/W     |           |
| 0h        |     |     | 0h   | 0h        |     | 0h      |           |
| 23        | 22  | 21  | 20   | 19        | 18  | 17      | 16        |
| AID15_0   |     |     |      |           |     |         |           |
| R/W       |     |     |      |           |     |         |           |
| 0h        |     |     |      |           |     |         |           |
| 15        | 14  | 13  | 12   | 11        | 10  | 9       | 8         |
| AID15_0   |     |     |      |           |     | AIDX    | RESERVED1 |
| R/W       |     |     |      |           |     | R/W     | R         |
| 0h        |     |     |      |           |     | 0h      | 0h        |
| 7         | 6   | 5   | 4    | 3         | 2   | 1       | 0         |
| NS        | EMU | SR  | SW   | SX        | UR  | UW      | UX        |
| R/W       | R/W | R/W | R/W  | R/W       | R/W | R/W     | R/W       |
| 0h        | 0h  | 0h  | 0h   | 0h        | 0h  | 0h      | 0h        |

**Table 5-2883. MPU\_16\_PROGRAMMABLE\_10\_MPPA Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED3 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                     |
| 28    | LOCK      | R/W  | 0h    | this field is used for locking the corresponding MPU region configurations.<br>Write 1 to lock the configurations along with the lock bit.<br>Writing 1 is allowed once per boot.<br>Lock bit will clear on reset only.<br>Once locked SW can not modify the MPU configurations along with lock bit. |
| 27:26 | RESERVED2 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 25:10 | AID15_0   | R/W  | 0h    | AIDs checked for this region. Defaults to input value.<br>0 = AID is not checked for these permissions.<br>1 = AID is checked for these permissions.                                                                                                                                                 |
| 9     | AIDX      | R/W  | 0h    | Additional AIDs checked. Defaults to input value.                                                                                                                                                                                                                                                    |
| 8     | RESERVED1 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 7     | NS        | R/W  | 0h    | Non-secure permission. Defaults to input value.                                                                                                                                                                                                                                                      |
| 6     | EMU       | R/W  | 0h    | Debug permission. Defaults to input value.                                                                                                                                                                                                                                                           |
| 5     | SR        | R/W  | 0h    | Supervisor read permission. Defaults to input value.                                                                                                                                                                                                                                                 |
| 4     | SW        | R/W  | 0h    | Supervisor write permission. Defaults to input value.                                                                                                                                                                                                                                                |
| 3     | SX        | R/W  | 0h    | Supervisor executable permission. Defaults to input value.                                                                                                                                                                                                                                           |
| 2     | UR        | R/W  | 0h    | User read permission. Defaults to input value.                                                                                                                                                                                                                                                       |

**Table 5-2883. MPU\_16\_PROGRAMMABLE\_10\_MPPA Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                          |
|-----|-------|------|-------|------------------------------------------------------|
| 1   | UW    | R/W  | 0h    | User write permission. Defaults to input value.      |
| 0   | UX    | R/W  | 0h    | User executable permission. Defaults to input value. |

### 5.17.2.36 MPU\_16\_PROGRAMMABLE\_11\_START\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_11\_START\_ADDRESS Register (Offset = 2A0h) [reset = 0h]

Programmable\_11\_Start\_Address.

Return to [Summary Table](#)

**Table 5-2884. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 02A0h       |

**Figure 5-952. MPU\_16\_PROGRAMMABLE\_11\_START\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2886. MPU\_16\_PROGRAMMABLE\_11\_START\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                |
|------|------------|------|-------|------------------------------------------------------------|
| 31:0 | START_ADDR | R/W  | 0h    | Start address for range N. Defaults to input signal value. |

### 5.17.2.37 MPU\_16\_PROGRAMMABLE\_11\_END\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_11\_END\_ADDRESS Register (Offset = 2A4h) [reset = 0h]

Programmable\_11\_End\_Address.

Return to [Summary Table](#)

**Table 5-2887. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 02A4h       |

**Figure 5-953. MPU\_16\_PROGRAMMABLE\_11\_END\_ADDRESS Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2889. MPU\_16\_PROGRAMMABLE\_11\_END\_ADDRESS Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                              |
|------|----------|------|-------|----------------------------------------------------------|
| 31:0 | END_ADDR | R/W  | 0h    | End address for range N. Defaults to input signal value. |

### 5.17.2.38 MPU\_16\_PROGRAMMABLE\_11\_MPPA Register

#### 1 MPU\_16\_PROGRAMMABLE\_11\_MPPA Register (Offset = 2A8h) [reset = 0h]

Programmable\_11\_MPPA.

Return to [Summary Table](#)

**Table 5-2890. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 02A8h       |

**Figure 5-954. MPU\_16\_PROGRAMMABLE\_11\_MPPA Name Register**

| 31        | 30  | 29  | 28   | 27        | 26  | 25      | 24        |
|-----------|-----|-----|------|-----------|-----|---------|-----------|
| RESERVED3 |     |     | LOCK | RESERVED2 |     | AID15_0 |           |
| R         |     |     | R/W  | R         |     | R/W     |           |
| 0h        |     |     | 0h   | 0h        |     | 0h      |           |
| 23        | 22  | 21  | 20   | 19        | 18  | 17      | 16        |
| AID15_0   |     |     |      |           |     |         |           |
| R/W       |     |     |      |           |     |         |           |
| 0h        |     |     |      |           |     |         |           |
| 15        | 14  | 13  | 12   | 11        | 10  | 9       | 8         |
| AID15_0   |     |     |      |           |     | AIDX    | RESERVED1 |
| R/W       |     |     |      |           |     | R/W     | R         |
| 0h        |     |     |      |           |     | 0h      | 0h        |
| 7         | 6   | 5   | 4    | 3         | 2   | 1       | 0         |
| NS        | EMU | SR  | SW   | SX        | UR  | UW      | UX        |
| R/W       | R/W | R/W | R/W  | R/W       | R/W | R/W     | R/W       |
| 0h        | 0h  | 0h  | 0h   | 0h        | 0h  | 0h      | 0h        |

**Table 5-2892. MPU\_16\_PROGRAMMABLE\_11\_MPPA Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED3 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                     |
| 28    | LOCK      | R/W  | 0h    | this field is used for locking the corresponding MPU region configurations.<br>Write 1 to lock the configurations along with the lock bit.<br>Writing 1 is allowed once per boot.<br>Lock bit will clear on reset only.<br>Once locked SW can not modify the MPU configurations along with lock bit. |
| 27:26 | RESERVED2 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 25:10 | AID15_0   | R/W  | 0h    | AIDs checked for this region. Defaults to input value.<br>0 = AID is not checked for these permissions.<br>1 = AID is checked for these permissions.                                                                                                                                                 |
| 9     | AIDX      | R/W  | 0h    | Additional AIDs checked. Defaults to input value.                                                                                                                                                                                                                                                    |
| 8     | RESERVED1 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 7     | NS        | R/W  | 0h    | Non-secure permission. Defaults to input value.                                                                                                                                                                                                                                                      |
| 6     | EMU       | R/W  | 0h    | Debug permission. Defaults to input value.                                                                                                                                                                                                                                                           |
| 5     | SR        | R/W  | 0h    | Supervisor read permission. Defaults to input value.                                                                                                                                                                                                                                                 |
| 4     | SW        | R/W  | 0h    | Supervisor write permission. Defaults to input value.                                                                                                                                                                                                                                                |
| 3     | SX        | R/W  | 0h    | Supervisor executable permission. Defaults to input value.                                                                                                                                                                                                                                           |
| 2     | UR        | R/W  | 0h    | User read permission. Defaults to input value.                                                                                                                                                                                                                                                       |



**Table 5-2892. MPU\_16\_PROGRAMMABLE\_11\_MPPA Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                          |
|-----|-------|------|-------|------------------------------------------------------|
| 1   | UW    | R/W  | 0h    | User write permission. Defaults to input value.      |
| 0   | UX    | R/W  | 0h    | User executable permission. Defaults to input value. |

### 5.17.2.39 MPU\_16\_PROGRAMMABLE\_12\_START\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_12\_START\_ADDRESS Register (Offset = 2B0h) [reset = 0h]

Programmable\_12\_Start\_Address.

Return to [Summary Table](#)

**Table 5-2893. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 02B0h       |

**Figure 5-955. MPU\_16\_PROGRAMMABLE\_12\_START\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2895. MPU\_16\_PROGRAMMABLE\_12\_START\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                |
|------|------------|------|-------|------------------------------------------------------------|
| 31:0 | START_ADDR | R/W  | 0h    | Start address for range N. Defaults to input signal value. |

#### 5.17.2.40 MPU\_16\_PROGRAMMABLE\_12\_END\_ADDRESS Register

##### 1 MPU\_16\_PROGRAMMABLE\_12\_END\_ADDRESS Register (Offset = 2B4h) [reset = 0h]

Programmable\_12\_End\_Address.

Return to [Summary Table](#)

**Table 5-2896. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 02B4h       |

**Figure 5-956. MPU\_16\_PROGRAMMABLE\_12\_END\_ADDRESS Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2898. MPU\_16\_PROGRAMMABLE\_12\_END\_ADDRESS Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                              |
|------|----------|------|-------|----------------------------------------------------------|
| 31:0 | END_ADDR | R/W  | 0h    | End address for range N. Defaults to input signal value. |

### 5.17.2.41 MPU\_16\_PROGRAMMABLE\_12\_MPPA Register

#### 1 MPU\_16\_PROGRAMMABLE\_12\_MPPA Register (Offset = 2B8h) [reset = 0h]

Programmable\_12\_MPPA.

Return to [Summary Table](#)

**Table 5-2899. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 02B8h       |

**Figure 5-957. MPU\_16\_PROGRAMMABLE\_12\_MPPA Name Register**

| 31        | 30  | 29  | 28   | 27        | 26  | 25      | 24        |
|-----------|-----|-----|------|-----------|-----|---------|-----------|
| RESERVED3 |     |     | LOCK | RESERVED2 |     | AID15_0 |           |
| R         |     |     | R/W  | R         |     | R/W     |           |
| 0h        |     |     | 0h   | 0h        |     | 0h      |           |
| 23        | 22  | 21  | 20   | 19        | 18  | 17      | 16        |
| AID15_0   |     |     |      |           |     |         |           |
| R/W       |     |     |      |           |     |         |           |
| 0h        |     |     |      |           |     |         |           |
| 15        | 14  | 13  | 12   | 11        | 10  | 9       | 8         |
| AID15_0   |     |     |      |           |     | AIDX    | RESERVED1 |
| R/W       |     |     |      |           |     | R/W     | R         |
| 0h        |     |     |      |           |     | 0h      | 0h        |
| 7         | 6   | 5   | 4    | 3         | 2   | 1       | 0         |
| NS        | EMU | SR  | SW   | SX        | UR  | UW      | UX        |
| R/W       | R/W | R/W | R/W  | R/W       | R/W | R/W     | R/W       |
| 0h        | 0h  | 0h  | 0h   | 0h        | 0h  | 0h      | 0h        |

**Table 5-2901. MPU\_16\_PROGRAMMABLE\_12\_MPPA Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED3 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                     |
| 28    | LOCK      | R/W  | 0h    | this field is used for locking the corresponding MPU region configurations.<br>Write 1 to lock the configurations along with the lock bit.<br>Writing 1 is allowed once per boot.<br>Lock bit will clear on reset only.<br>Once locked SW can not modify the MPU configurations along with lock bit. |
| 27:26 | RESERVED2 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 25:10 | AID15_0   | R/W  | 0h    | AIDs checked for this region. Defaults to input value.<br>0 = AID is not checked for these permissions.<br>1 = AID is checked for these permissions.                                                                                                                                                 |
| 9     | AIDX      | R/W  | 0h    | Additional AIDs checked. Defaults to input value.                                                                                                                                                                                                                                                    |
| 8     | RESERVED1 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 7     | NS        | R/W  | 0h    | Non-secure permission. Defaults to input value.                                                                                                                                                                                                                                                      |
| 6     | EMU       | R/W  | 0h    | Debug permission. Defaults to input value.                                                                                                                                                                                                                                                           |
| 5     | SR        | R/W  | 0h    | Supervisor read permission. Defaults to input value.                                                                                                                                                                                                                                                 |
| 4     | SW        | R/W  | 0h    | Supervisor write permission. Defaults to input value.                                                                                                                                                                                                                                                |
| 3     | SX        | R/W  | 0h    | Supervisor executable permission. Defaults to input value.                                                                                                                                                                                                                                           |
| 2     | UR        | R/W  | 0h    | User read permission. Defaults to input value.                                                                                                                                                                                                                                                       |

**Table 5-2901. MPU\_16\_PROGRAMMABLE\_12\_MPPA Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                          |
|-----|-------|------|-------|------------------------------------------------------|
| 1   | UW    | R/W  | 0h    | User write permission. Defaults to input value.      |
| 0   | UX    | R/W  | 0h    | User executable permission. Defaults to input value. |

### 5.17.2.42 MPU\_16\_PROGRAMMABLE\_13\_START\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_13\_START\_ADDRESS Register (Offset = 2C0h) [reset = 0h]

Programmable\_13\_Start\_Address.

Return to [Summary Table](#)

**Table 5-2902. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 02C0h       |

**Figure 5-958. MPU\_16\_PROGRAMMABLE\_13\_START\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2904. MPU\_16\_PROGRAMMABLE\_13\_START\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                |
|------|------------|------|-------|------------------------------------------------------------|
| 31:0 | START_ADDR | R/W  | 0h    | Start address for range N. Defaults to input signal value. |

### 5.17.2.43 MPU\_16\_PROGRAMMABLE\_13\_END\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_13\_END\_ADDRESS Register (Offset = 2C4h) [reset = 0h]

Programmable\_13\_End\_Address.

Return to [Summary Table](#)

**Table 5-2905. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 02C4h       |

**Figure 5-959. MPU\_16\_PROGRAMMABLE\_13\_END\_ADDRESS Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2907. MPU\_16\_PROGRAMMABLE\_13\_END\_ADDRESS Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                              |
|------|----------|------|-------|----------------------------------------------------------|
| 31:0 | END_ADDR | R/W  | 0h    | End address for range N. Defaults to input signal value. |

#### 5.17.2.44 MPU\_16\_PROGRAMMABLE\_13\_MPPA Register

##### 1 MPU\_16\_PROGRAMMABLE\_13\_MPPA Register (Offset = 2C8h) [reset = 0h]

Programmable\_13\_MPPA.

Return to [Summary Table](#)

**Table 5-2908. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 02C8h       |

**Figure 5-960. MPU\_16\_PROGRAMMABLE\_13\_MPPA Name Register**

| 31        | 30  | 29  | 28   | 27        | 26  | 25      | 24        |
|-----------|-----|-----|------|-----------|-----|---------|-----------|
| RESERVED3 |     |     | LOCK | RESERVED2 |     | AID15_0 |           |
| R         |     |     | R/W  | R         |     | R/W     |           |
| 0h        |     |     | 0h   | 0h        |     | 0h      |           |
| 23        | 22  | 21  | 20   | 19        | 18  | 17      | 16        |
| AID15_0   |     |     |      |           |     |         |           |
| R/W       |     |     |      |           |     |         |           |
| 0h        |     |     |      |           |     |         |           |
| 15        | 14  | 13  | 12   | 11        | 10  | 9       | 8         |
| AID15_0   |     |     |      |           |     | AIDX    | RESERVED1 |
| R/W       |     |     |      |           |     | R/W     | R         |
| 0h        |     |     |      |           |     | 0h      | 0h        |
| 7         | 6   | 5   | 4    | 3         | 2   | 1       | 0         |
| NS        | EMU | SR  | SW   | SX        | UR  | UW      | UX        |
| R/W       | R/W | R/W | R/W  | R/W       | R/W | R/W     | R/W       |
| 0h        | 0h  | 0h  | 0h   | 0h        | 0h  | 0h      | 0h        |

**Table 5-2910. MPU\_16\_PROGRAMMABLE\_13\_MPPA Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED3 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                     |
| 28    | LOCK      | R/W  | 0h    | this field is used for locking the corresponding MPU region configurations.<br>Write 1 to lock the configurations along with the lock bit.<br>Writing 1 is allowed once per boot.<br>Lock bit will clear on reset only.<br>Once locked SW can not modify the MPU configurations along with lock bit. |
| 27:26 | RESERVED2 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 25:10 | AID15_0   | R/W  | 0h    | AIDs checked for this region. Defaults to input value.<br>0 = AID is not checked for these permissions.<br>1 = AID is checked for these permissions.                                                                                                                                                 |
| 9     | AIDX      | R/W  | 0h    | Additional AIDs checked. Defaults to input value.                                                                                                                                                                                                                                                    |
| 8     | RESERVED1 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 7     | NS        | R/W  | 0h    | Non-secure permission. Defaults to input value.                                                                                                                                                                                                                                                      |
| 6     | EMU       | R/W  | 0h    | Debug permission. Defaults to input value.                                                                                                                                                                                                                                                           |
| 5     | SR        | R/W  | 0h    | Supervisor read permission. Defaults to input value.                                                                                                                                                                                                                                                 |
| 4     | SW        | R/W  | 0h    | Supervisor write permission. Defaults to input value.                                                                                                                                                                                                                                                |
| 3     | SX        | R/W  | 0h    | Supervisor executable permission. Defaults to input value.                                                                                                                                                                                                                                           |
| 2     | UR        | R/W  | 0h    | User read permission. Defaults to input value.                                                                                                                                                                                                                                                       |



**Table 5-2910. MPU\_16\_PROGRAMMABLE\_13\_MPPA Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                          |
|-----|-------|------|-------|------------------------------------------------------|
| 1   | UW    | R/W  | 0h    | User write permission. Defaults to input value.      |
| 0   | UX    | R/W  | 0h    | User executable permission. Defaults to input value. |

### 5.17.2.45 MPU\_16\_PROGRAMMABLE\_14\_START\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_14\_START\_ADDRESS Register (Offset = 2D0h) [reset = 0h]

Programmable\_14\_Start\_Address.

Return to [Summary Table](#)

**Table 5-2911. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 02D0h       |

**Figure 5-961. MPU\_16\_PROGRAMMABLE\_14\_START\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2913. MPU\_16\_PROGRAMMABLE\_14\_START\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                |
|------|------------|------|-------|------------------------------------------------------------|
| 31:0 | START_ADDR | R/W  | 0h    | Start address for range N. Defaults to input signal value. |

### 5.17.2.46 MPU\_16\_PROGRAMMABLE\_14\_END\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_14\_END\_ADDRESS Register (Offset = 2D4h) [reset = 0h]

Programmable\_14\_End\_Address.

Return to [Summary Table](#)

**Table 5-2914. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 02D4h       |

**Figure 5-962. MPU\_16\_PROGRAMMABLE\_14\_END\_ADDRESS Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2916. MPU\_16\_PROGRAMMABLE\_14\_END\_ADDRESS Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                              |
|------|----------|------|-------|----------------------------------------------------------|
| 31:0 | END_ADDR | R/W  | 0h    | End address for range N. Defaults to input signal value. |

### 5.17.2.47 MPU\_16\_PROGRAMMABLE\_14\_MPPA Register

#### 1 MPU\_16\_PROGRAMMABLE\_14\_MPPA Register (Offset = 2D8h) [reset = 0h]

Programmable\_14\_MPPA.

Return to [Summary Table](#)

**Table 5-2917. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 02D8h       |

**Figure 5-963. MPU\_16\_PROGRAMMABLE\_14\_MPPA Name Register**

| 31        | 30  | 29  | 28   | 27        | 26  | 25      | 24        |
|-----------|-----|-----|------|-----------|-----|---------|-----------|
| RESERVED3 |     |     | LOCK | RESERVED2 |     | AID15_0 |           |
| R         |     |     | R/W  | R         |     | R/W     |           |
| 0h        |     |     | 0h   | 0h        |     | 0h      |           |
| 23        | 22  | 21  | 20   | 19        | 18  | 17      | 16        |
| AID15_0   |     |     |      |           |     |         |           |
| R/W       |     |     |      |           |     |         |           |
| 0h        |     |     |      |           |     |         |           |
| 15        | 14  | 13  | 12   | 11        | 10  | 9       | 8         |
| AID15_0   |     |     |      |           |     | AIDX    | RESERVED1 |
| R/W       |     |     |      |           |     | R/W     | R         |
| 0h        |     |     |      |           |     | 0h      | 0h        |
| 7         | 6   | 5   | 4    | 3         | 2   | 1       | 0         |
| NS        | EMU | SR  | SW   | SX        | UR  | UW      | UX        |
| R/W       | R/W | R/W | R/W  | R/W       | R/W | R/W     | R/W       |
| 0h        | 0h  | 0h  | 0h   | 0h        | 0h  | 0h      | 0h        |

**Table 5-2919. MPU\_16\_PROGRAMMABLE\_14\_MPPA Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED3 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                     |
| 28    | LOCK      | R/W  | 0h    | this field is used for locking the corresponding MPU region configurations.<br>Write 1 to lock the configurations along with the lock bit.<br>Writing 1 is allowed once per boot.<br>Lock bit will clear on reset only.<br>Once locked SW can not modify the MPU configurations along with lock bit. |
| 27:26 | RESERVED2 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 25:10 | AID15_0   | R/W  | 0h    | AIDs checked for this region. Defaults to input value.<br>0 = AID is not checked for these permissions.<br>1 = AID is checked for these permissions.                                                                                                                                                 |
| 9     | AIDX      | R/W  | 0h    | Additional AIDs checked. Defaults to input value.                                                                                                                                                                                                                                                    |
| 8     | RESERVED1 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 7     | NS        | R/W  | 0h    | Non-secure permission. Defaults to input value.                                                                                                                                                                                                                                                      |
| 6     | EMU       | R/W  | 0h    | Debug permission. Defaults to input value.                                                                                                                                                                                                                                                           |
| 5     | SR        | R/W  | 0h    | Supervisor read permission. Defaults to input value.                                                                                                                                                                                                                                                 |
| 4     | SW        | R/W  | 0h    | Supervisor write permission. Defaults to input value.                                                                                                                                                                                                                                                |
| 3     | SX        | R/W  | 0h    | Supervisor executable permission. Defaults to input value.                                                                                                                                                                                                                                           |
| 2     | UR        | R/W  | 0h    | User read permission. Defaults to input value.                                                                                                                                                                                                                                                       |

**Table 5-2919. MPU\_16\_PROGRAMMABLE\_14\_MPPA Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                          |
|-----|-------|------|-------|------------------------------------------------------|
| 1   | UW    | R/W  | 0h    | User write permission. Defaults to input value.      |
| 0   | UX    | R/W  | 0h    | User executable permission. Defaults to input value. |

#### 5.17.2.48 MPU\_16\_PROGRAMMABLE\_15\_START\_ADDRESS Register

##### 1 MPU\_16\_PROGRAMMABLE\_15\_START\_ADDRESS Register (Offset = 2E0h) [reset = 0h]

Programmable\_15\_Start\_Address.

Return to [Summary Table](#)

**Table 5-2920. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 02E0h       |

**Figure 5-964. MPU\_16\_PROGRAMMABLE\_15\_START\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2922. MPU\_16\_PROGRAMMABLE\_15\_START\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                |
|------|------------|------|-------|------------------------------------------------------------|
| 31:0 | START_ADDR | R/W  | 0h    | Start address for range N. Defaults to input signal value. |

### 5.17.2.49 MPU\_16\_PROGRAMMABLE\_15\_END\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_15\_END\_ADDRESS Register (Offset = 2E4h) [reset = 0h]

Programmable\_15\_End\_Address.

Return to [Summary Table](#)

**Table 5-2923. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 02E4h       |

**Figure 5-965. MPU\_16\_PROGRAMMABLE\_15\_END\_ADDRESS Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2925. MPU\_16\_PROGRAMMABLE\_15\_END\_ADDRESS Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                              |
|------|----------|------|-------|----------------------------------------------------------|
| 31:0 | END_ADDR | R/W  | 0h    | End address for range N. Defaults to input signal value. |

### 5.17.2.50 MPU\_16\_PROGRAMMABLE\_15\_MPPA Register

#### 1 MPU\_16\_PROGRAMMABLE\_15\_MPPA Register (Offset = 2E8h) [reset = 0h]

Programmable\_15\_MPPA.

Return to [Summary Table](#)

**Table 5-2926. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 02E8h       |

**Figure 5-966. MPU\_16\_PROGRAMMABLE\_15\_MPPA Name Register**

| 31        | 30  | 29  | 28   | 27        | 26  | 25      | 24        |
|-----------|-----|-----|------|-----------|-----|---------|-----------|
| RESERVED3 |     |     | LOCK | RESERVED2 |     | AID15_0 |           |
| R         |     |     | R/W  | R         |     | R/W     |           |
| 0h        |     |     | 0h   | 0h        |     | 0h      |           |
| 23        | 22  | 21  | 20   | 19        | 18  | 17      | 16        |
| AID15_0   |     |     |      |           |     |         |           |
| R/W       |     |     |      |           |     |         |           |
| 0h        |     |     |      |           |     |         |           |
| 15        | 14  | 13  | 12   | 11        | 10  | 9       | 8         |
| AID15_0   |     |     |      |           |     | AIDX    | RESERVED1 |
| R/W       |     |     |      |           |     | R/W     | R         |
| 0h        |     |     |      |           |     | 0h      | 0h        |
| 7         | 6   | 5   | 4    | 3         | 2   | 1       | 0         |
| NS        | EMU | SR  | SW   | SX        | UR  | UW      | UX        |
| R/W       | R/W | R/W | R/W  | R/W       | R/W | R/W     | R/W       |
| 0h        | 0h  | 0h  | 0h   | 0h        | 0h  | 0h      | 0h        |

**Table 5-2928. MPU\_16\_PROGRAMMABLE\_15\_MPPA Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED3 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                     |
| 28    | LOCK      | R/W  | 0h    | this field is used for locking the corresponding MPU region configurations.<br>Write 1 to lock the configurations along with the lock bit.<br>Writing 1 is allowed once per boot.<br>Lock bit will clear on reset only.<br>Once locked SW can not modify the MPU configurations along with lock bit. |
| 27:26 | RESERVED2 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 25:10 | AID15_0   | R/W  | 0h    | AIDs checked for this region. Defaults to input value.<br>0 = AID is not checked for these permissions.<br>1 = AID is checked for these permissions.                                                                                                                                                 |
| 9     | AIDX      | R/W  | 0h    | Additional AIDs checked. Defaults to input value.                                                                                                                                                                                                                                                    |
| 8     | RESERVED1 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 7     | NS        | R/W  | 0h    | Non-secure permission. Defaults to input value.                                                                                                                                                                                                                                                      |
| 6     | EMU       | R/W  | 0h    | Debug permission. Defaults to input value.                                                                                                                                                                                                                                                           |
| 5     | SR        | R/W  | 0h    | Supervisor read permission. Defaults to input value.                                                                                                                                                                                                                                                 |
| 4     | SW        | R/W  | 0h    | Supervisor write permission. Defaults to input value.                                                                                                                                                                                                                                                |
| 3     | SX        | R/W  | 0h    | Supervisor executable permission. Defaults to input value.                                                                                                                                                                                                                                           |
| 2     | UR        | R/W  | 0h    | User read permission. Defaults to input value.                                                                                                                                                                                                                                                       |



**Table 5-2928. MPU\_16\_PROGRAMMABLE\_15\_MPPA Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                          |
|-----|-------|------|-------|------------------------------------------------------|
| 1   | UW    | R/W  | 0h    | User write permission. Defaults to input value.      |
| 0   | UX    | R/W  | 0h    | User executable permission. Defaults to input value. |

### 5.17.2.51 MPU\_16\_PROGRAMMABLE\_16\_START\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_16\_START\_ADDRESS Register (Offset = 2F0h) [reset = 0h]

Programmable\_16\_Start\_Address.

Return to [Summary Table](#)

**Table 5-2929. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 02F0h       |

**Figure 5-967. MPU\_16\_PROGRAMMABLE\_16\_START\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START_ADDR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2931. MPU\_16\_PROGRAMMABLE\_16\_START\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                |
|------|------------|------|-------|------------------------------------------------------------|
| 31:0 | START_ADDR | R/W  | 0h    | Start address for range N. Defaults to input signal value. |

### 5.17.2.52 MPU\_16\_PROGRAMMABLE\_16\_END\_ADDRESS Register

#### 1 MPU\_16\_PROGRAMMABLE\_16\_END\_ADDRESS Register (Offset = 2F4h) [reset = 0h]

Programmable\_16\_End\_Address.

Return to [Summary Table](#)

**Table 5-2932. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 02F4h       |

**Figure 5-968. MPU\_16\_PROGRAMMABLE\_16\_END\_ADDRESS Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END_ADDR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-2934. MPU\_16\_PROGRAMMABLE\_16\_END\_ADDRESS Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                              |
|------|----------|------|-------|----------------------------------------------------------|
| 31:0 | END_ADDR | R/W  | 0h    | End address for range N. Defaults to input signal value. |

### 5.17.2.53 MPU\_16\_PROGRAMMABLE\_16\_MPPA Register

#### 1 MPU\_16\_PROGRAMMABLE\_16\_MPPA Register (Offset = 2F8h) [reset = 0h]

Programmable\_16\_MPPA.

Return to [Summary Table](#)

**Table 5-2935. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 02F8h       |

**Figure 5-969. MPU\_16\_PROGRAMMABLE\_16\_MPPA Name Register**

| 31        | 30  | 29  | 28   | 27        | 26  | 25      | 24        |
|-----------|-----|-----|------|-----------|-----|---------|-----------|
| RESERVED3 |     |     | LOCK | RESERVED2 |     | AID15_0 |           |
| R         |     |     | R/W  | R         |     | R/W     |           |
| 0h        |     |     | 0h   | 0h        |     | 0h      |           |
| 23        | 22  | 21  | 20   | 19        | 18  | 17      | 16        |
| AID15_0   |     |     |      |           |     |         |           |
| R/W       |     |     |      |           |     |         |           |
| 0h        |     |     |      |           |     |         |           |
| 15        | 14  | 13  | 12   | 11        | 10  | 9       | 8         |
| AID15_0   |     |     |      |           |     | AIDX    | RESERVED1 |
| R/W       |     |     |      |           |     | R/W     | R         |
| 0h        |     |     |      |           |     | 0h      | 0h        |
| 7         | 6   | 5   | 4    | 3         | 2   | 1       | 0         |
| NS        | EMU | SR  | SW   | SX        | UR  | UW      | UX        |
| R/W       | R/W | R/W | R/W  | R/W       | R/W | R/W     | R/W       |
| 0h        | 0h  | 0h  | 0h   | 0h        | 0h  | 0h      | 0h        |

**Table 5-2937. MPU\_16\_PROGRAMMABLE\_16\_MPPA Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                          |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED3 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                     |
| 28    | LOCK      | R/W  | 0h    | this field is used for locking the corresponding MPU region configurations.<br>Write 1 to lock the configurations along with the lock bit.<br>Writing 1 is allowed once per boot.<br>Lock bit will clear on reset only.<br>Once locked SW can not modify the MPU configurations along with lock bit. |
| 27:26 | RESERVED2 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 25:10 | AID15_0   | R/W  | 0h    | AIDs checked for this region. Defaults to input value.<br>0 = AID is not checked for these permissions.<br>1 = AID is checked for these permissions.                                                                                                                                                 |
| 9     | AIDX      | R/W  | 0h    | Additional AIDs checked. Defaults to input value.                                                                                                                                                                                                                                                    |
| 8     | RESERVED1 | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                    |
| 7     | NS        | R/W  | 0h    | Non-secure permission. Defaults to input value.                                                                                                                                                                                                                                                      |
| 6     | EMU       | R/W  | 0h    | Debug permission. Defaults to input value.                                                                                                                                                                                                                                                           |
| 5     | SR        | R/W  | 0h    | Supervisor read permission. Defaults to input value.                                                                                                                                                                                                                                                 |
| 4     | SW        | R/W  | 0h    | Supervisor write permission. Defaults to input value.                                                                                                                                                                                                                                                |
| 3     | SX        | R/W  | 0h    | Supervisor executable permission. Defaults to input value.                                                                                                                                                                                                                                           |
| 2     | UR        | R/W  | 0h    | User read permission. Defaults to input value.                                                                                                                                                                                                                                                       |

**Table 5-2937. MPU\_16\_PROGRAMMABLE\_16\_MPPA Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                          |
|-----|-------|------|-------|------------------------------------------------------|
| 1   | UW    | R/W  | 0h    | User write permission. Defaults to input value.      |
| 0   | UX    | R/W  | 0h    | User executable permission. Defaults to input value. |

### 5.17.2.54 MPU\_16\_FAULT\_ADDRESS Register

#### 1 MPU\_16\_FAULT\_ADDRESS Register (Offset = 300h) [reset = 0h]

Fault\_Address.

Return to [Summary Table](#)

**Table 5-2938. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0300h       |

**Figure 5-970. MPU\_16\_FAULT\_ADDRESS Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FAULT_ADDR |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-2940. MPU\_16\_FAULT\_ADDRESS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description    |
|------|------------|------|-------|----------------|
| 31:0 | FAULT_ADDR | R    | 0h    | Fault_address. |

### 5.17.2.55 MPU\_16\_FAULT\_STATUS Register

#### 1 MPU\_16\_FAULT\_STATUS Register (Offset = 304h) [reset = 0h]

Fault\_Status.

Return to [Summary Table](#)

**Table 5-2941. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0304h       |

**Figure 5-971. MPU\_16\_FAULT\_STATUS Name Register**

|          |           |            |    |        |    |    |           |
|----------|-----------|------------|----|--------|----|----|-----------|
| 31       | 30        | 29         | 28 | 27     | 26 | 25 | 24        |
| ID       |           |            |    |        |    |    |           |
| R        |           |            |    |        |    |    |           |
| 0h       |           |            |    |        |    |    |           |
| 23       | 22        | 21         | 20 | 19     | 18 | 17 | 16        |
| MSTID    |           |            |    |        |    |    |           |
| R        |           |            |    |        |    |    |           |
| 0h       |           |            |    |        |    |    |           |
| 15       | 14        | 13         | 12 | 11     | 10 | 9  | 8         |
| RESERVED |           |            |    | PRIVID |    |    | RESERVED1 |
| R        |           |            |    | R      |    |    | R         |
| 0h       |           |            |    | 0h     |    |    | 0h        |
| 7        | 6         | 5          | 4  | 3      | 2  | 1  | 0         |
| NS       | RESERVED2 | FAULT_TYPE |    |        |    |    |           |
| R        | R         | R          |    |        |    |    |           |
| 0h       | 0h        | 0h         |    |        |    |    |           |

**Table 5-2943. MPU\_16\_FAULT\_STATUS Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                           |
|-------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | ID         | R    | 0h    | Transfer ID                                                                                                                                                                                                                                                                                                           |
| 23:16 | MSTID      | R    | 0h    | Master ID.                                                                                                                                                                                                                                                                                                            |
| 15:13 | RESERVED   | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                                     |
| 12:9  | PRIVID     | R    | 0h    | Privilege ID.                                                                                                                                                                                                                                                                                                         |
| 8     | RESERVED1  | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                                     |
| 7     | NS         | R    | 0h    | Non-secure access.                                                                                                                                                                                                                                                                                                    |
| 6     | RESERVED2  | R    | 0h    | Always read as 0.                                                                                                                                                                                                                                                                                                     |
| 5:0   | FAULT_TYPE | R    | 0h    | Fault_type.<br>100000 = supervisor read fault<br>010000 = supervisor write fault<br>001000 = supervisor execute fault<br>000100 = user read fault<br>000010 = user write fault<br>000001 = user execute fault<br>111111 = relaxed cache linefill fault<br>010010 = relaxed cache writeback fault<br>000000 = no fault |

### 5.17.2.56 MPU\_16\_FAULT\_CLEAR Register

#### 1 MPU\_16\_FAULT\_CLEAR Register (Offset = 308h) [reset = 0h]

Fault\_Clear.

Return to [Summary Table](#)

**Table 5-2944. Instance Table**

| Instance Name       | Physical Address |
|---------------------|------------------|
| MPU_R5SS0_CORE1_AHB | 401E 0308h       |

**Figure 5-972. MPU\_16\_FAULT\_CLEAR Name Register**

|          |    |    |    |    |    |    |           |
|----------|----|----|----|----|----|----|-----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24        |
| RESERVED |    |    |    |    |    |    |           |
| R        |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16        |
| RESERVED |    |    |    |    |    |    |           |
| R        |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8         |
| RESERVED |    |    |    |    |    |    |           |
| R        |    |    |    |    |    |    |           |
| 0h       |    |    |    |    |    |    |           |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0         |
| RESERVED |    |    |    |    |    |    | FAULT_CLR |
| R        |    |    |    |    |    |    | W         |
| 0h       |    |    |    |    |    |    | 0h        |

**Table 5-2946. MPU\_16\_FAULT\_CLEAR Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                   |
|------|-----------|------|-------|-------------------------------------------------------------------------------|
| 31:1 | RESERVED  | R    | 0h    | Always read as 0.                                                             |
| 0    | FAULT_CLR | W    | 0h    | Fault_clear. Writing a 1 clears the current fault. Writing a 0 has no effect. |



## 5.18 MSRAM

### MSRAM

#### 5.18.1 MSRAM Summaries

##### MSRAM Summaries

**Table 5-2947. MSRAM Registers, Base Address=7000 0000h, Length=524288**

| Offset     | Length | Register Name               | MSRAM_BANK0<br>Physical Address | MSRAM_BANK1<br>Physical Address | MSRAM_BANK2<br>Physical Address |
|------------|--------|-----------------------------|---------------------------------|---------------------------------|---------------------------------|
| 0h         | 32     | <a href="#">MSRAM_START</a> | 7000 0000h                      | 7008 0000h                      | 7010 0000h                      |
| 7FFFC<br>h | 32     | <a href="#">MSRAM_END</a>   | 7007 FFFCh                      | 700F FFFCh                      | 7017 FFFCh                      |

**Table 5-2948. MSRAM Registers, Base Address=7000 0000h, Length=524288**

| Offset     | Length | Register Name               | MSRAM_BANK3 Physical Address |
|------------|--------|-----------------------------|------------------------------|
| 0h         | 32     | <a href="#">MSRAM_START</a> | 7018 0000h                   |
| 7FFFC<br>h | 32     | <a href="#">MSRAM_END</a>   | 701F FFFCh                   |

#### 5.18.2 MSRAM Registers

##### MSRAM Registers

### 5.18.2.1 MSRAM\_START Register

#### 1 MSRAM\_START Register (Offset = 0h) [reset = 0h]

Return to [Summary Table](#)

**Table 5-2949. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSRAM_BANK0   | 7000 0000h       |
| MSRAM_BANK1   | 7008 0000h       |
| MSRAM_BANK2   | 7010 0000h       |
| MSRAM_BANK3   | 7018 0000h       |

**Figure 5-973. MSRAM\_START Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-2951. MSRAM\_START Register Field Descriptions**

| Bit  | Field | Type | Reset | Description             |
|------|-------|------|-------|-------------------------|
| 31:0 | START | R/W  | 0h    | L2 Memory start address |

### 5.18.2.2 MSRAM\_END Register

#### 1 MSRAM\_END Register (Offset = 7FFFCh) [reset = 0h]

Return to [Summary Table](#)

**Table 5-2952. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSRAM_BANK0   | 7007 FFFCh       |
| MSRAM_BANK1   | 700F FFFCh       |
| MSRAM_BANK2   | 7017 FFFCh       |
| MSRAM_BANK3   | 701F FFFCh       |

**Figure 5-974. MSRAM\_END Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 5-2954. MSRAM\_END Register Field Descriptions**

| Bit  | Field | Type | Reset | Description           |
|------|-------|------|-------|-----------------------|
| 31:0 | END   | R/W  | 0h    | L2 Memory end address |

## 5.19 MSS\_MBOX

### MSS\_MBOX

#### 5.19.1 MSS\_MBOX Summaries

#### MSS\_MBOX Summaries

**Table 5-2955. MSS\_MBOX Registers, Base Address=7200 0000h, Length=16384**

| Offset | Length | Register Name                  | MSS_MBOX0 Physical Address |
|--------|--------|--------------------------------|----------------------------|
| 0h     | 32     | <a href="#">MSS_MBOX_START</a> | 7200 0000h                 |
| 3FFCh  | 32     | <a href="#">MSS_MBOX_END</a>   | 7200 3FFCh                 |

#### 5.19.2 MSS\_MBOX Registers

#### MSS\_MBOX Registers

### 5.19.2.1 MSS\_MBOX\_START Register

#### 1 MSS\_MBOX\_START Register (Offset = 0h) [reset = 0h]

Return to [Summary Table](#)

**Table 5-2956. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_MBOX0     | 7200 0000h       |

**Figure 5-975. MSS\_MBOX\_START Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| START |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-2958. MSS\_MBOX\_START Register Field Descriptions**

| Bit  | Field | Type | Reset | Description          |
|------|-------|------|-------|----------------------|
| 31:0 | START | R/W  | 0h    | Memory start address |

### 5.19.2.2 MSS\_MBOX\_END Register

#### 1 MSS\_MBOX\_END Register (Offset = 3FFCh) [reset = 0h]

Return to [Summary Table](#)

**Table 5-2959. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| MSS_MBOX0     | 7200 3FFCh       |

**Figure 5-976. MSS\_MBOX\_END Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| END |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 5-2961. MSS\_MBOX\_END Register Field Descriptions**

| Bit  | Field | Type | Reset | Description           |
|------|-------|------|-------|-----------------------|
| 31:0 | END   | R/W  | 0h    | L2 Memory end address |

## 5.20 PBIST

### PBIST

#### 5.20.1 PBIST Summaries

#### PBIST Summaries

**Table 5-2962. PBIST Registers, Base Address=5330 0000h, Length=512**

| Offset | Length | Register Name                | PBIST0 Physical Address |
|--------|--------|------------------------------|-------------------------|
| 164h   | 16     | <a href="#">PBIST_DLR</a>    | 5330 0164h              |
| 180h   | 8      | <a href="#">PBIST_PACT</a>   | 5330 0180h              |
| 184h   | 8      | <a href="#">PBIST_ID</a>     | 5330 0184h              |
| 190h   | 8      | <a href="#">PBIST_FSFR0</a>  | 5330 0190h              |
| 194h   | 8      | <a href="#">PBIST_FSFR1</a>  | 5330 0194h              |
| 198h   | 8      | <a href="#">PBIST_FSRCR0</a> | 5330 0198h              |
| 19Ch   | 8      | <a href="#">PBIST_FSRCR1</a> | 5330 019Ch              |
| 1C0h   | 8      | <a href="#">PBIST_ROM</a>    | 5330 01C0h              |
| 1C4h   | 32     | <a href="#">PBIST_ALGO</a>   | 5330 01C4h              |
| 1C8h   | 32     | <a href="#">PBIST_RINFOL</a> | 5330 01C8h              |
| 1CCh   | 32     | <a href="#">PBIST_RINFOU</a> | 5330 01CCh              |

#### 5.20.2 PBIST Registers

#### PBIST Registers

### 5.20.2.1 PBIST\_DLR Register

#### 1 PBIST\_DLR Register (Offset = 164h) [reset = 208h]

Datalogger 0 .

Return to [Summary Table](#)

**Table 5-2963. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| PBIST0        | 5330 0164h       |

**Figure 5-977. PBIST\_DLR Name Register**

|      |    |    |    |    |    |   |   |
|------|----|----|----|----|----|---|---|
| 15   | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DLR1 |    |    |    |    |    |   |   |
| R/W  |    |    |    |    |    |   |   |
| 2h   |    |    |    |    |    |   |   |
| 7    | 6  | 5  | 4  | 3  | 2  | 1 | 0 |
| DLR0 |    |    |    |    |    |   |   |
| R/W  |    |    |    |    |    |   |   |
| 8h   |    |    |    |    |    |   |   |

**Table 5-2965. PBIST\_DLR Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                 |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:8 | DLR1  | R/W  | 2h    | Datalogger Register<br>[8] : Reserevd<br>[9] : Default Testing Mode. When in this mode, ROM-based testing is kicked off. If the intention is to perform go/no-go testing via config, write to both this bit and bit [2] of the Datalogger Register simultaneously<br>[15:10] : Reserevd                                                                                                     |
| 7:0  | DLR0  | R/W  | 8h    | Datalogger Register<br>[1:0] : Reserved<br>[2] : ROM-based testing mode. Setting this bit to 1 enables the PBIST controller to execute test algorithms that are stored in the PBIST ROM<br>[3] : Do not change this bit from its default value of 1<br>[4] : Config access mode. Setting this bit allows the host processor to configure the PBIST controller registers<br>[7:5] : Reserved |



### 5.20.2.2 PBIST\_PACT Register

#### 1 PBIST\_PACT Register (Offset = 180h) [reset = 0h]

Pbist Active.

Return to [Summary Table](#)

**Table 5-2966. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| PBIST0        | 5330 0180h       |

**Figure 5-978. PBIST\_PACT Name Register**

|          |    |    |    |    |    |   |            |
|----------|----|----|----|----|----|---|------------|
| 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8          |
| 7        | 6  | 5  | 4  | 3  | 2  | 1 | 0          |
| RESERVED |    |    |    |    |    |   | PBIST_PACT |
| NONE     |    |    |    |    |    |   | R/W        |
| 0h       |    |    |    |    |    |   | 0h         |

**Table 5-2968. PBIST\_PACT Register Field Descriptions**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:1 | RESERVED   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                             |
| 0   | PBIST_PACT | R/W  | 0h    | Pbist Active/ROM Clock Enable Register<br>[0]: This bit must be set to turn on internal PBIST clocks. Setting this bit asserts an internal signal that is used as the clock gate enable. As long as this bit is 0, any access to PBIST will not go through, and PBIST will remain in an almost zero-power mode.<br>Value 0 = Disable internal PBIST clocks<br>Value 1 = Enable internal PBIST clocks |

### 5.20.2.3 PBIST\_ID Register

#### 1 PBIST\_ID Register (Offset = 184h) [reset = 1h]

PBIST ID.

Return to [Summary Table](#)

**Table 5-2969. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| PBIST0        | 5330 0184h       |

**Figure 5-979. PBIST\_ID Name Register**

|          |    |    |    |          |    |   |   |
|----------|----|----|----|----------|----|---|---|
| 15       | 14 | 13 | 12 | 11       | 10 | 9 | 8 |
| 7        | 6  | 5  | 4  | 3        | 2  | 1 | 0 |
| RESERVED |    |    |    | PBIST_ID |    |   |   |
| NONE     |    |    |    | R/W      |    |   |   |
| 0h       |    |    |    | 1h       |    |   |   |

**Table 5-2971. PBIST\_ID Register Field Descriptions**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                        |
|-----|----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                           |
| 4:0 | PBIST_ID | R/W  | 1h    | PBIST ID.<br>This is a unique ID assigned to each PBIST controller in a device with multiple PBIST controllers. The value of this register does not effect the functionality of the CPU interface. |

### 5.20.2.4 PBIST\_FSFR0 Register

#### 1 PBIST\_FSFR0 Register (Offset = 190h) [reset = 0h]

Fail status fail - port 0 .

Return to [Summary Table](#)

**Table 5-2972. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| PBIST0        | 5330 0190h       |

**Figure 5-980. PBIST\_FSFR0 Name Register**

|          |    |    |    |    |    |   |             |
|----------|----|----|----|----|----|---|-------------|
| 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8           |
| 7        | 6  | 5  | 4  | 3  | 2  | 1 | 0           |
| RESERVED |    |    |    |    |    |   | PBIST_FSFR0 |
| NONE     |    |    |    |    |    |   | R           |
| 0h       |    |    |    |    |    |   | 0h          |

**Table 5-2974. PBIST\_FSFR0 Register Field Descriptions**

| Bit | Field       | Type | Reset | Description                                                                                                                                                                     |
|-----|-------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:1 | RESERVED    | NONE | 0h    | Reserved                                                                                                                                                                        |
| 0   | PBIST_FSFR0 | R    | 0h    | Fail Status Fail Register- Port 0<br>This register indicates if a failure occurred during a memory self-test.<br>Value 0 = No failure occurred<br>Value 1 = Indicates a failure |

### 5.20.2.5 PBIST\_FSFR1 Register

#### 1 PBIST\_FSFR1 Register (Offset = 194h) [reset = 0h]

Fail status fail - port 1

Return to [Summary Table](#)

**Table 5-2975. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| PBIST0        | 5330 0194h       |

**Figure 5-981. PBIST\_FSFR1 Name Register**

|          |    |    |    |    |    |   |             |
|----------|----|----|----|----|----|---|-------------|
| 15       | 14 | 13 | 12 | 11 | 10 | 9 | 8           |
| 7        | 6  | 5  | 4  | 3  | 2  | 1 | 0           |
| RESERVED |    |    |    |    |    |   | PBIST_FSFR1 |
| NONE     |    |    |    |    |    |   | R           |
| 0h       |    |    |    |    |    |   | 0h          |

**Table 5-2977. PBIST\_FSFR1 Register Field Descriptions**

| Bit | Field       | Type | Reset | Description                                                                                                                                                                     |
|-----|-------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:1 | RESERVED    | NONE | 0h    | Reserved                                                                                                                                                                        |
| 0   | PBIST_FSFR1 | R    | 0h    | Fail Status Fail Register- Port 1<br>This register indicates if a failure occurred during a memory self-test.<br>Value 0 = No failure occurred<br>Value 1 = Indicates a failure |

### 5.20.2.6 PBIST\_FSR0 Register

#### 1 PBIST\_FSR0 Register (Offset = 198h) [reset = 0h]

Fail Count fail - port 0 .

Return to [Summary Table](#)

**Table 5-2978. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| PBIST0        | 5330 0198h       |

**Figure 5-982. PBIST\_FSR0 Name Register**

|          |    |    |    |            |    |   |   |
|----------|----|----|----|------------|----|---|---|
| 15       | 14 | 13 | 12 | 11         | 10 | 9 | 8 |
| 7        | 6  | 5  | 4  | 3          | 2  | 1 | 0 |
| RESERVED |    |    |    | PBIST_FSR0 |    |   |   |
| NONE     |    |    |    | R          |    |   |   |
| 0h       |    |    |    | 0h         |    |   |   |

**Table 5-2980. PBIST\_FSR0 Register Field Descriptions**

| Bit | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | RESERVED   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                           |
| 3:0 | PBIST_FSR0 | R    | 0h    | Fail Status Count - Port 0<br>These registers keep count of the number of failures observed during the memory self-test. The PBIST controller stops executing the memory self-test whenever a failure occurs in any memory instance for any of the test algorithms. The value in gets incremented by one whenever a failure occurs |

### 5.20.2.7 PBIST\_FSR1CR1 Register

#### 1 PBIST\_FSR1CR1 Register (Offset = 19Ch) [reset = 0h]

Fail Count fail - port 1

Return to [Summary Table](#)

**Table 5-2981. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| PBIST0        | 5330 019Ch       |

**Figure 5-983. PBIST\_FSR1CR1 Name Register**

|          |    |    |    |               |    |   |   |
|----------|----|----|----|---------------|----|---|---|
| 15       | 14 | 13 | 12 | 11            | 10 | 9 | 8 |
| 7        | 6  | 5  | 4  | 3             | 2  | 1 | 0 |
| RESERVED |    |    |    | PBIST_FSR1CR1 |    |   |   |
| NONE     |    |    |    | R             |    |   |   |
| 0h       |    |    |    | 0h            |    |   |   |

**Table 5-2983. PBIST\_FSR1CR1 Register Field Descriptions**

| Bit | Field         | Type | Reset | Description                                                                                                                                                                                                                                                                                                                        |
|-----|---------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | RESERVED      | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                           |
| 3:0 | PBIST_FSR1CR1 | R    | 0h    | Fail Status Count - Port 1<br>These registers keep count of the number of failures observed during the memory self-test. The PBIST controller stops executing the memory self-test whenever a failure occurs in any memory instance for any of the test algorithms. The value in gets incremented by one whenever a failure occurs |

### 5.20.2.8 PBIST\_ROM Register

#### 1 PBIST\_ROM Register (Offset = 1C0h) [reset = 3h]

Rom Mask .

Return to [Summary Table](#)

**Table 5-2984. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| PBIST0        | 5330 01C0h       |

**Figure 5-984. PBIST\_ROM Name Register**

|          |    |    |    |    |    |           |   |
|----------|----|----|----|----|----|-----------|---|
| 15       | 14 | 13 | 12 | 11 | 10 | 9         | 8 |
| 7        | 6  | 5  | 4  | 3  | 2  | 1         | 0 |
| RESERVED |    |    |    |    |    | PBIST_ROM |   |
| NONE     |    |    |    |    |    | R/W       |   |
| 0h       |    |    |    |    |    | 3h        |   |

**Table 5-2986. PBIST\_ROM Register Field Descriptions**

| Bit | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                               |
|-----|-----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:2 | RESERVED  | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 1:0 | PBIST_ROM | R/W  | 3h    | <p>Rom Mask .</p> <p>This two-bit register sets appropriate ROM access modes for the PBIST controller.</p> <p>Value</p> <p>0h= No information is used from ROM</p> <p>Value</p> <p>1h= Only RAM Group information from ROM</p> <p>Value</p> <p>2h= Only Algorithm information from ROM</p> <p>Value</p> <p>3h= Both Algorithm and RAM information from ROM. This option should be selected for application self-test.</p> |

### 5.20.2.9 PBIST\_ALGO Register

#### 1 PBIST\_ALGO Register (Offset = 1C4h) [reset = FFFFFFFFh]

ROM Algorithm Mask 0

Return to [Summary Table](#)

**Table 5-2987. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| PBIST0        | 5330 01C4h       |

**Figure 5-985. PBIST\_ALGO Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| ALGO3 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFh   |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| ALGO2 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFh   |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| ALGO1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFh   |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ALGO0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| FFh   |    |    |    |    |    |    |    |

**Table 5-2989. PBIST\_ALGO Register Field Descriptions**

| Bit   | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                      |
|-------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | ALGO3 | R/W  | FFh   | This register is used to indicate the algorithm[s] to be used for the memory self-test routine. Each bit corresponds to a specific algorithm.<br>Writing a value 1 to the particular bit, enables the corresponding algorithm.<br>Writing a value 0 to the particular bit, disables the corresponding algorithm. |
| 23:16 | ALGO2 | R/W  | FFh   | This register is used to indicate the algorithm[s] to be used for the memory self-test routine. Each bit corresponds to a specific algorithm.<br>Writing a value 1 to the particular bit, enables the corresponding algorithm.<br>Writing a value 0 to the particular bit, disables the corresponding algorithm. |
| 15:8  | ALGO1 | R/W  | FFh   | This register is used to indicate the algorithm[s] to be used for the memory self-test routine. Each bit corresponds to a specific algorithm.<br>Writing a value 1 to the particular bit, enables the corresponding algorithm.<br>Writing a value 0 to the particular bit, disables the corresponding algorithm. |



**Table 5-2989. PBIST\_ALGO Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                     |
|-----|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | ALGO0 | R/W  | FFh   | <p>This register is used to indicate the algorithm[s] to be used for the memory self-test routine. Each bit corresponds to a specific algorithm.</p> <p>Writing a value 1 to the particular bit, enables the corresponding algorithm.</p> <p>Writing a value 0 to the particular bit, disables the corresponding algorithm.</p> |

### 5.20.2.10 PBIST\_RINFOL Register

#### 1 PBIST\_RINFOL Register (Offset = 1C8h) [reset = FFFFFFFFh]

RAM Info Mask Lower 0

Return to [Summary Table](#)
**Table 5-2990. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| PBIST0        | 5330 01C8h       |

**Figure 5-986. PBIST\_RINFOL Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RINFOL3 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| FFh     |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RINFOL2 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| FFh     |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RINFOL1 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| FFh     |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RINFOL0 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| FFh     |    |    |    |    |    |    |    |

**Table 5-2992. PBIST\_RINFOL Register Field Descriptions**

| Bit   | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|---------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RINFOL3 | R/W  | FFh   | This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithm to be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group. |
| 23:16 | RINFOL2 | R/W  | FFh   | This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithm to be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group. |
| 15:8  | RINFOL1 | R/W  | FFh   | This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithm to be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group. |
| 7:0   | RINFOL0 | R/W  | FFh   | This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithm to be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group. |

### 5.20.2.11 PBIST\_RINFOU Register

#### 1 PBIST\_RINFOU Register (Offset = 1CCh) [reset = FFFFFFFFh]

RAM Info Mask Upper 0

Return to [Summary Table](#)
**Table 5-2993. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| PBIST0        | 5330 01CCh       |

**Figure 5-987. PBIST\_RINFOU Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RINFOU3 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| FFh     |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RINFOU2 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| FFh     |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RINFOU1 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| FFh     |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RINFOU0 |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| FFh     |    |    |    |    |    |    |    |

**Table 5-2995. PBIST\_RINFOU Register Field Descriptions**

| Bit   | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|---------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | RINFOU3 | R/W  | FFh   | This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithm to be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group. |
| 23:16 | RINFOU2 | R/W  | FFh   | This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithm to be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group. |
| 15:8  | RINFOU1 | R/W  | FFh   | This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithm to be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group. |
| 7:0   | RINFOU0 | R/W  | FFh   | This register is to select memory groups to run the algorithms selected in the PBIST_ALGO register. For an algorithm to be executed on a particular memory group, the corresponding bit in this register must be set to 1. The default value of this register is all 1s, which means all the memory groups are selected. Writing a value 0 to the particular bit, disables the corresponding memory group. |

## 5.21 QSPI

### QSPI

#### 5.21.1 QSPI Summaries

#### QSPI Summaries

**Table 5-2996. QSPI Registers, Base Address=4820 0000h, Length=256**

| Offset | Length | Register Name                                  | QSPI0 Physical Address |
|--------|--------|------------------------------------------------|------------------------|
| 0h     | 32     | <a href="#">QSPI_PID</a>                       | 4820 0000h             |
| 4h     | 32     | <a href="#">QSPI_MSS_QSPI_RESERVED1</a>        | 4820 0004h             |
| 8h     | 32     | <a href="#">QSPI_MSS_QSPI_RESERVED2</a>        | 4820 0008h             |
| Ch     | 32     | <a href="#">QSPI_MSS_QSPI_RESERVED3</a>        | 4820 000Ch             |
| 14h    | 32     | <a href="#">QSPI_MSS_QSPI_RESERVED4</a>        | 4820 0014h             |
| 18h    | 32     | <a href="#">QSPI_MSS_QSPI_RESERVED5</a>        | 4820 0018h             |
| 1Ch    | 32     | <a href="#">QSPI_MSS_QSPI_RESERVED6</a>        | 4820 001Ch             |
| 20h    | 32     | <a href="#">QSPI_INTR_STATUS_RAW_SET</a>       | 4820 0020h             |
| 24h    | 32     | <a href="#">QSPI_INTR_STATUS_ENABLED_CLEAR</a> | 4820 0024h             |
| 28h    | 32     | <a href="#">QSPI_INTR_ENABLE_SET</a>           | 4820 0028h             |
| 2Ch    | 32     | <a href="#">QSPI_INTR_ENABLE_CLEAR</a>         | 4820 002Ch             |
| 30h    | 32     | <a href="#">QSPI_INTC_EOI</a>                  | 4820 0030h             |
| 34h    | 32     | <a href="#">QSPI_MSS_QSPI_RESERVED7</a>        | 4820 0034h             |
| 38h    | 32     | <a href="#">QSPI_MSS_QSPI_RESERVED8</a>        | 4820 0038h             |
| 3Ch    | 32     | <a href="#">QSPI_MSS_QSPI_RESERVED9</a>        | 4820 003Ch             |
| 40h    | 32     | <a href="#">QSPI_SPI_CLOCK_CNTRL</a>           | 4820 0040h             |
| 44h    | 32     | <a href="#">QSPI_SPI_DC</a>                    | 4820 0044h             |
| 48h    | 32     | <a href="#">QSPI_SPI_CMD</a>                   | 4820 0048h             |
| 4Ch    | 32     | <a href="#">QSPI_SPI_STATUS</a>                | 4820 004Ch             |
| 50h    | 32     | <a href="#">QSPI_SPI_DATA</a>                  | 4820 0050h             |
| 54h    | 32     | <a href="#">QSPI_SPI_SETUP0</a>                | 4820 0054h             |
| 58h    | 32     | <a href="#">QSPI_SPI_SETUP1</a>                | 4820 0058h             |
| 5Ch    | 32     | <a href="#">QSPI_SPI_SETUP2</a>                | 4820 005Ch             |
| 60h    | 32     | <a href="#">QSPI_SPI_SETUP3</a>                | 4820 0060h             |
| 64h    | 32     | <a href="#">QSPI_SPI_SWITCH</a>                | 4820 0064h             |
| 68h    | 32     | <a href="#">QSPI_SPI_DATA1</a>                 | 4820 0068h             |
| 6Ch    | 32     | <a href="#">QSPI_SPI_DATA2</a>                 | 4820 006Ch             |
| 70h    | 32     | <a href="#">QSPI_SPI_DATA3</a>                 | 4820 0070h             |

#### 5.21.2 QSPI Registers

#### QSPI Registers

### 5.21.2.1 QSPI\_PID Register

#### 1 QSPI\_PID Register (Offset = 0h) [reset = 4F400000h]

PID.

Return to [Summary Table](#)

**Table 5-2997. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 0000h       |

**Figure 5-988. QSPI\_PID Name Register**

|        |    |          |    |       |    |    |    |
|--------|----|----------|----|-------|----|----|----|
| 31     | 30 | 29       | 28 | 27    | 26 | 25 | 24 |
| SCHEME |    | RESERVED |    | FUNC  |    |    |    |
| R      |    | R        |    | R     |    |    |    |
| 1h     |    | 0h       |    | F40h  |    |    |    |
| 23     | 22 | 21       | 20 | 19    | 18 | 17 | 16 |
| FUNC   |    |          |    |       |    |    |    |
| R      |    |          |    |       |    |    |    |
| F40h   |    |          |    |       |    |    |    |
| 15     | 14 | 13       | 12 | 11    | 10 | 9  | 8  |
| RTL    |    |          |    | MAJOR |    |    |    |
| R      |    |          |    | R     |    |    |    |
| 0h     |    |          |    | 0h    |    |    |    |
| 7      | 6  | 5        | 4  | 3     | 2  | 1  | 0  |
| CUSTOM |    | MINOR    |    |       |    |    |    |
| R      |    | R        |    |       |    |    |    |
| 0h     |    | 0h       |    |       |    |    |    |

**Table 5-2999. QSPI\_PID Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                       |
|-------|----------|------|-------|-------------------------------------------------------------------|
| 31:30 | SCHEME   | R    | 1h    | The scheme of the register used. This indicates the PDR3.5 Method |
| 29:28 | RESERVED | R    | 0h    | Always read as 0                                                  |
| 27:16 | FUNC     | R    | F40h  | The function of the module being used                             |
| 15:11 | RTL      | R    | 0h    | RTL Release Version The PDR release number of this IP             |
| 10:8  | MAJOR    | R    | 0h    | Major Release Number                                              |
| 7:6   | CUSTOM   | R    | 0h    | Custom IP                                                         |
| 5:0   | MINOR    | R    | 0h    | Minor Release Number                                              |

### 5.21.2.2 QSPI\_MSS\_QSPI\_RESERVED1 Register

#### 1 QSPI\_MSS\_QSPI\_RESERVED1 Register (Offset = 4h) [reset = 0h]

Reserved.

Return to [Summary Table](#)

**Table 5-3000. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 0004h       |

**Figure 5-989. QSPI\_MSS\_QSPI\_RESERVED1 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_1 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_1 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_1 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED_1 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-3002. QSPI\_MSS\_QSPI\_RESERVED1 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description |
|------|------------|------|-------|-------------|
| 31:0 | RESERVED_1 | R    | 0h    | Reserved    |

### 5.21.2.3 QSPI\_MSS\_QSPI\_RESERVED2 Register

#### 1 QSPI\_MSS\_QSPI\_RESERVED2 Register (Offset = 8h) [reset = 0h]

Reserved.

Return to [Summary Table](#)

**Table 5-3003. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 0008h       |

**Figure 5-990. QSPI\_MSS\_QSPI\_RESERVED2 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_2 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_2 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_2 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED_2 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-3005. QSPI\_MSS\_QSPI\_RESERVED2 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description |
|------|------------|------|-------|-------------|
| 31:0 | RESERVED_2 | R    | 0h    | Reserved    |

### 5.21.2.4 QSPI\_MSS\_QSPI\_RESERVED3 Register

#### 1 QSPI\_MSS\_QSPI\_RESERVED3 Register (Offset = Ch) [reset = 0h]

Reserved.

Return to [Summary Table](#)

**Table 5-3006. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 000Ch       |

**Figure 5-991. QSPI\_MSS\_QSPI\_RESERVED3 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_3 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_3 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_3 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED_3 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-3008. QSPI\_MSS\_QSPI\_RESERVED3 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description |
|------|------------|------|-------|-------------|
| 31:0 | RESERVED_3 | R    | 0h    | Reserved    |



### 5.21.2.5 QSPI\_MSS\_QSPI\_RESERVED4 Register

#### 1 QSPI\_MSS\_QSPI\_RESERVED4 Register (Offset = 14h) [reset = 0h]

Reserved.

Return to [Summary Table](#)

**Table 5-3009. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 0014h       |

**Figure 5-992. QSPI\_MSS\_QSPI\_RESERVED4 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_4 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_4 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_4 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED_4 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-3011. QSPI\_MSS\_QSPI\_RESERVED4 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description |
|------|------------|------|-------|-------------|
| 31:0 | RESERVED_4 | R    | 0h    | Reserved    |

### 5.21.2.6 QSPI\_MSS\_QSPI\_RESERVED5 Register

#### 1 QSPI\_MSS\_QSPI\_RESERVED5 Register (Offset = 18h) [reset = 0h]

Reserved.

Return to [Summary Table](#)

**Table 5-3012. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 0018h       |

**Figure 5-993. QSPI\_MSS\_QSPI\_RESERVED5 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_5 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_5 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_5 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED_5 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-3014. QSPI\_MSS\_QSPI\_RESERVED5 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description |
|------|------------|------|-------|-------------|
| 31:0 | RESERVED_5 | R    | 0h    | Reserved    |

### 5.21.2.7 QSPI\_MSS\_QSPI\_RESERVED6 Register

#### 1 QSPI\_MSS\_QSPI\_RESERVED6 Register (Offset = 1Ch) [reset = 0h]

Reserved.

Return to [Summary Table](#)

**Table 5-3015. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 001Ch       |

**Figure 5-994. QSPI\_MSS\_QSPI\_RESERVED6 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_6 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_6 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_6 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED_6 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-3017. QSPI\_MSS\_QSPI\_RESERVED6 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description |
|------|------------|------|-------|-------------|
| 31:0 | RESERVED_6 | R    | 0h    | Reserved    |

### 5.21.2.8 QSPI\_INTR\_STATUS\_RAW\_SET Register

#### 1 QSPI\_INTR\_STATUS\_RAW\_SET Register (Offset = 20h) [reset = 0h]

INTR Interrupt Status Raw/Set Register.

Return to [Summary Table](#)

**Table 5-3018. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 0020h       |

**Figure 5-995. QSPI\_INTR\_STATUS\_RAW\_SET Name Register**

|          |    |    |    |    |    |          |          |
|----------|----|----|----|----|----|----------|----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25       | 24       |
| RESERVED |    |    |    |    |    |          |          |
| R        |    |    |    |    |    |          |          |
| 0h       |    |    |    |    |    |          |          |
| 23       | 22 | 21 | 20 | 19 | 18 | 17       | 16       |
| RESERVED |    |    |    |    |    |          |          |
| R        |    |    |    |    |    |          |          |
| 0h       |    |    |    |    |    |          |          |
| 15       | 14 | 13 | 12 | 11 | 10 | 9        | 8        |
| RESERVED |    |    |    |    |    |          |          |
| R        |    |    |    |    |    |          |          |
| 0h       |    |    |    |    |    |          |          |
| 7        | 6  | 5  | 4  | 3  | 2  | 1        | 0        |
| RESERVED |    |    |    |    |    | WIRQ_RAW | FIRQ_RAW |
| R        |    |    |    |    |    | R/W      | R/W      |
| 0h       |    |    |    |    |    | 0h       | 0h       |

**Table 5-3020. QSPI\_INTR\_STATUS\_RAW\_SET Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                               |
|------|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED | R    | 0h    | Always read as 0                                                                                                                          |
| 1    | WIRQ_RAW | R/W  | 0h    | Word Interrupt Status<br>Read indicates raw status<br>0 = inactive<br>1 = active<br>Writing 1 will set status<br>Writing 0 has no effect  |
| 0    | FIRQ_RAW | R/W  | 0h    | Frame Interrupt Status<br>Read indicates raw status<br>0 = inactive<br>1 = active<br>Writing 1 will set status<br>Writing 0 has no effect |

### 5.21.2.9 QSPI\_INTR\_STATUS\_ENABLED\_CLEAR Register

#### 1 QSPI\_INTR\_STATUS\_ENABLED\_CLEAR Register (Offset = 24h) [reset = 0h]

INTR Interrupt Status Enabled/Clear Register.

Return to [Summary Table](#)

**Table 5-3021. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 0024h       |

**Figure 5-996. QSPI\_INTR\_STATUS\_ENABLED\_CLEAR Name Register**

|          |    |    |    |    |    |          |          |
|----------|----|----|----|----|----|----------|----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25       | 24       |
| RESERVED |    |    |    |    |    |          |          |
| R        |    |    |    |    |    |          |          |
| 0h       |    |    |    |    |    |          |          |
| 23       | 22 | 21 | 20 | 19 | 18 | 17       | 16       |
| RESERVED |    |    |    |    |    |          |          |
| R        |    |    |    |    |    |          |          |
| 0h       |    |    |    |    |    |          |          |
| 15       | 14 | 13 | 12 | 11 | 10 | 9        | 8        |
| RESERVED |    |    |    |    |    |          |          |
| R        |    |    |    |    |    |          |          |
| 0h       |    |    |    |    |    |          |          |
| 7        | 6  | 5  | 4  | 3  | 2  | 1        | 0        |
| RESERVED |    |    |    |    |    | WIRQ_ENA | FIRQ_ENA |
| R        |    |    |    |    |    | R/W      | R/W      |
| 0h       |    |    |    |    |    | 0h       | 0h       |

**Table 5-3023. QSPI\_INTR\_STATUS\_ENABLED\_CLEAR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                |
|------|----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED | R    | 0h    | Always read as 0                                                                                                                                           |
| 1    | WIRQ_ENA | R/W  | 0h    | Word Interrupt Enabled Status<br>Read indicates enabled status<br>0 = inactive<br>1 = active<br>Writing 1 will clear interrupt<br>Writing 0 has no effect  |
| 0    | FIRQ_ENA | R/W  | 0h    | Frame Interrupt Enabled Status<br>Read indicates enabled status<br>0 = inactive<br>1 = active<br>Writing 1 will clear interrupt<br>Writing 0 has no effect |

### 5.21.2.10 QSPI\_INTR\_ENABLE\_SET Register

#### 1 QSPI\_INTR\_ENABLE\_SET Register (Offset = 28h) [reset = 0h]

INTR Interrupt Enable/Set Register.

Return to [Summary Table](#)

**Table 5-3024. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 0028h       |

**Figure 5-997. QSPI\_INTR\_ENABLE\_SET Name Register**

|          |    |    |    |    |    |              |              |
|----------|----|----|----|----|----|--------------|--------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25           | 24           |
| RESERVED |    |    |    |    |    |              |              |
| R        |    |    |    |    |    |              |              |
| 0h       |    |    |    |    |    |              |              |
| 23       | 22 | 21 | 20 | 19 | 18 | 17           | 16           |
| RESERVED |    |    |    |    |    |              |              |
| R        |    |    |    |    |    |              |              |
| 0h       |    |    |    |    |    |              |              |
| 15       | 14 | 13 | 12 | 11 | 10 | 9            | 8            |
| RESERVED |    |    |    |    |    |              |              |
| R        |    |    |    |    |    |              |              |
| 0h       |    |    |    |    |    |              |              |
| 7        | 6  | 5  | 4  | 3  | 2  | 1            | 0            |
| RESERVED |    |    |    |    |    | WIRQ_ENA_SET | FIRQ_ENA_SET |
| R        |    |    |    |    |    | R/W          | R/W          |
| 0h       |    |    |    |    |    | 0h           | 0h           |

**Table 5-3026. QSPI\_INTR\_ENABLE\_SET Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                                                                                     |
|------|--------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED     | R    | 0h    | Always read as 0                                                                                                                                                |
| 1    | WIRQ_ENA_SET | R/W  | 0h    | Word Interrupt Enable/Set<br>Read indicates interrupt enable<br>0 = disabled<br>1 = enabled<br>Writing 1 will set interrupt enabled<br>Writing 0 has no effect  |
| 0    | FIRQ_ENA_SET | R/W  | 0h    | Frame Interrupt Enable/Set<br>Read indicates interrupt enable<br>0 = disabled<br>1 = enabled<br>Writing 1 will set interrupt enabled<br>Writing 0 has no effect |

### 5.21.2.11 QSPI\_INTR\_ENABLE\_CLEAR Register

#### 1 QSPI\_INTR\_ENABLE\_CLEAR Register (Offset = 2Ch) [reset = 0h]

INTR Interrupt Enable/Clear Register.

Return to [Summary Table](#)

**Table 5-3027. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 002Ch       |

**Figure 5-998. QSPI\_INTR\_ENABLE\_CLEAR Name Register**

|          |    |    |    |    |    |              |              |
|----------|----|----|----|----|----|--------------|--------------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25           | 24           |
| RESERVED |    |    |    |    |    |              |              |
| R        |    |    |    |    |    |              |              |
| 0h       |    |    |    |    |    |              |              |
| 23       | 22 | 21 | 20 | 19 | 18 | 17           | 16           |
| RESERVED |    |    |    |    |    |              |              |
| R        |    |    |    |    |    |              |              |
| 0h       |    |    |    |    |    |              |              |
| 15       | 14 | 13 | 12 | 11 | 10 | 9            | 8            |
| RESERVED |    |    |    |    |    |              |              |
| R        |    |    |    |    |    |              |              |
| 0h       |    |    |    |    |    |              |              |
| 7        | 6  | 5  | 4  | 3  | 2  | 1            | 0            |
| RESERVED |    |    |    |    |    | WIRQ_ENA_CLR | FIRQ_ENA_CLR |
| R        |    |    |    |    |    | R/W          | R/W          |
| 0h       |    |    |    |    |    | 0h           | 0h           |

**Table 5-3029. QSPI\_INTR\_ENABLE\_CLEAR Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                                                                                         |
|------|--------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED     | R    | 0h    | Always read as 0                                                                                                                                                    |
| 1    | WIRQ_ENA_CLR | R/W  | 0h    | Word Interrupt Enable/Clear<br>Read indicates interrupt enable<br>0 = disabled<br>1 = enabled<br>Writing 1 will clear interrupt enabled<br>Writing 0 has no effect  |
| 0    | FIRQ_ENA_CLR | R/W  | 0h    | Frame Interrupt Enable/Clear<br>Read indicates interrupt enable<br>0 = disabled<br>1 = enabled<br>Writing 1 will clear interrupt enabled<br>Writing 0 has no effect |

### 5.21.2.12 QSPI\_INTC\_EOI Register

#### 1 QSPI\_INTC\_EOI Register (Offset = 30h) [reset = 0h]

EOI Register.

Return to [Summary Table](#)

**Table 5-3030. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 0030h       |

**Figure 5-999. QSPI\_INTC\_EOI Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| EOI_VECTOR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| EOI_VECTOR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| EOI_VECTOR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| EOI_VECTOR |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-3032. QSPI\_INTC\_EOI Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                         |
|------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | EOI_VECTOR | R/W  | 0h    | Number associated with the ipgenericirq for intr output. There are 1 interrupt outputs<br>Write 0x0 : Write to intr IP Generic<br>Any other write value is ignored. |



### 5.21.2.13 QSPI\_MSS\_QSPI\_RESERVED7 Register

#### 1 QSPI\_MSS\_QSPI\_RESERVED7 Register (Offset = 34h) [reset = 0h]

Reserved.

Return to [Summary Table](#)

**Table 5-3033. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 0034h       |

**Figure 5-1000. QSPI\_MSS\_QSPI\_RESERVED7 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_7 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_7 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_7 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED_7 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-3035. QSPI\_MSS\_QSPI\_RESERVED7 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description |
|------|------------|------|-------|-------------|
| 31:0 | RESERVED_7 | R    | 0h    | Reserved    |

### 5.21.2.14 QSPI\_MSS\_QSPI\_RESERVED8 Register

#### 1 QSPI\_MSS\_QSPI\_RESERVED8 Register (Offset = 38h) [reset = 0h]

Reserved.

Return to [Summary Table](#)

**Table 5-3036. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 0038h       |

**Figure 5-1001. QSPI\_MSS\_QSPI\_RESERVED8 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_8 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_8 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_8 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED_8 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-3038. QSPI\_MSS\_QSPI\_RESERVED8 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description |
|------|------------|------|-------|-------------|
| 31:0 | RESERVED_8 | R    | 0h    | Reserved    |

### 5.21.2.15 QSPI\_MSS\_QSPI\_RESERVED9 Register

#### 1 QSPI\_MSS\_QSPI\_RESERVED9 Register (Offset = 3Ch) [reset = 0h]

Reserved.

Return to [Summary Table](#)

**Table 5-3039. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 003Ch       |

**Figure 5-1002. QSPI\_MSS\_QSPI\_RESERVED9 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_9 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_9 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_9 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED_9 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-3041. QSPI\_MSS\_QSPI\_RESERVED9 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description |
|------|------------|------|-------|-------------|
| 31:0 | RESERVED_9 | R    | 0h    | Reserved    |

### 5.21.2.16 QSPI\_SPI\_CLOCK\_CNTRL Register

#### 1 QSPI\_SPI\_CLOCK\_CNTRL Register (Offset = 40h) [reset = 0h]

SPI Clock Control Register (SPICC).

Return to [Summary Table](#)

**Table 5-3042. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 0040h       |

**Figure 5-1003. QSPI\_SPI\_CLOCK\_CNTRL Name Register**

|          |          |    |    |    |    |    |    |
|----------|----------|----|----|----|----|----|----|
| 31       | 30       | 29 | 28 | 27 | 26 | 25 | 24 |
| CLKEN    | RESERVED |    |    |    |    |    |    |
| R/W      | R        |    |    |    |    |    |    |
| 0h       | 0h       |    |    |    |    |    |    |
| 23       | 22       | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |          |    |    |    |    |    |    |
| R        |          |    |    |    |    |    |    |
| 0h       |          |    |    |    |    |    |    |
| 15       | 14       | 13 | 12 | 11 | 10 | 9  | 8  |
| DCLK_DIV |          |    |    |    |    |    |    |
| R/W      |          |    |    |    |    |    |    |
| 0h       |          |    |    |    |    |    |    |
| 7        | 6        | 5  | 4  | 3  | 2  | 1  | 0  |
| DCLK_DIV |          |    |    |    |    |    |    |
| R/W      |          |    |    |    |    |    |    |
| 0h       |          |    |    |    |    |    |    |

**Table 5-3044. QSPI\_SPI\_CLOCK\_CNTRL Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                                                              |
|-------|----------|------|-------|--------------------------------------------------------------------------|
| 31    | CLKEN    | R/W  | 0h    | Clock Enable.<br>0- Data clock is turned off<br>1- Data clock is enabled |
| 30:16 | RESERVED | R    | 0h    | Always read as 0                                                         |
| 15:0  | DCLK_DIV | R/W  | 0h    | Serial data clock divide by ratio                                        |

### 5.21.2.17 QSPI\_SPI\_DC Register

#### 1 QSPI\_SPI\_DC Register (Offset = 44h) [reset = 0h]

SPI Data Control Register (SPIDC).

Return to [Summary Table](#)

**Table 5-3045. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 0044h       |

**Figure 5-1004. QSPI\_SPI\_DC Name Register**

| 31        | 30 | 29 | 28  | 27 | 26    | 25   | 24   |
|-----------|----|----|-----|----|-------|------|------|
| RESERVED4 |    |    | DD3 |    | CKPH3 | CSP3 | CKP3 |
| R         |    |    | R/W |    | R/W   | R/W  | R/W  |
| 0h        |    |    | 0h  |    | 0h    | 0h   | 0h   |
| 23        | 22 | 21 | 20  | 19 | 18    | 17   | 16   |
| RESERVED3 |    |    | DD2 |    | CKPH2 | CSP2 | CKP2 |
| R         |    |    | R/W |    | R/W   | R/W  | R/W  |
| 0h        |    |    | 0h  |    | 0h    | 0h   | 0h   |
| 15        | 14 | 13 | 12  | 11 | 10    | 9    | 8    |
| RESERVED2 |    |    | DD1 |    | CKPH1 | CSP1 | CKP1 |
| R         |    |    | R/W |    | R/W   | R/W  | R/W  |
| 0h        |    |    | 0h  |    | 0h    | 0h   | 0h   |
| 7         | 6  | 5  | 4   | 3  | 2     | 1    | 0    |
| RESERVED1 |    |    | DD0 |    | CKPH0 | CSP0 | CKP0 |
| R         |    |    | R/W |    | R/W   | R/W  | R/W  |
| 0h        |    |    | 0h  |    | 0h    | 0h   | 0h   |

**Table 5-3047. QSPI\_SPI\_DC Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                     |
|-------|-----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED4 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                                |
| 28:27 | DD3       | R/W  | 0h    | Data delay for chip select 3<br>00- Data is output on the same cycle as the CS_N goes active<br>01- Data is output 1 DCLK cycle after the CS_N goes active<br>10- Data is output 2 DCLK cycles after the CS_N goes active<br>11- Data is output 3 DCLK cycles after the CS_N goes active                        |
| 26    | CKPH3     | R/W  | 0h    | Clock phase for chip select 3<br>If CKP0 = 0<br>0- Data shifted out on falling edge; input on rising edge<br>1- Data shifted out on rising edge; input on falling edge<br>If CKP0 = 1<br>1- Data shifted out on falling edge; input on rising edge<br>0- Data shifted out on rising edge; input on falling edge |
| 25    | CSP3      | R/W  | 0h    | Chip select polarity for chip select 3<br>0- Active low<br>1- Active high                                                                                                                                                                                                                                       |
| 24    | CKP3      | R/W  | 0h    | Clock polarity for chip select 3<br>0- When data is not being transferred, SCK = 0<br>1- When data is not being transferred, SCK = 1                                                                                                                                                                            |
| 23:21 | RESERVED3 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                                |

**Table 5-3047. QSPI\_SPI\_DC Register Field Descriptions (continued)**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                      |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 20:19 | DD2       | R/W  | 0h    | Data delay for chip select 2<br>00- Data is output on the same cycle as the CS_N goes active<br>01- Data is output 1 DCLK cycle after the CS_N goes active<br>10- Data is output 2 DCLK cycles after the CS_N goes active<br>11- Data is output 3 DCLK cycles after the CS_N goes active                         |
| 18    | CKPH2     | R/W  | 0h    | Clock phase for chip select 2.<br>If CKP0 = 0<br>0- Data shifted out on falling edge; input on rising edge<br>1- Data shifted out on rising edge; input on falling edge<br>If CKP0 = 1<br>1- Data shifted out on falling edge; input on rising edge<br>0- Data shifted out on rising edge; input on falling edge |
| 17    | CSP2      | R/W  | 0h    | Chip select polarity for chip select 2<br>0- Active low<br>1- Active high                                                                                                                                                                                                                                        |
| 16    | CKP2      | R/W  | 0h    | Clock polarity for chip select 2<br>0- When data is not being transferred, SCK = 0<br>1- When data is not being transferred, SCK = 1                                                                                                                                                                             |
| 15:13 | RESERVED2 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                                 |
| 12:11 | DD1       | R/W  | 0h    | Data delay for chip select 1<br>00- Data is output on the same cycle as the CS_N goes active<br>01- Data is output 1 DCLK cycle after the CS_N goes active<br>10- Data is output 2 DCLK cycles after the CS_N goes active<br>11- Data is output 3 DCLK cycles after the CS_N goes active                         |
| 10    | CKPH1     | R/W  | 0h    | Clock phase for chip select 1.<br>If CKP0 = 0<br>0- Data shifted out on falling edge; input on rising edge<br>1- Data shifted out on rising edge; input on falling edge<br>If CKP0 = 1<br>1- Data shifted out on falling edge; input on rising edge<br>0- Data shifted out on rising edge; input on falling edge |
| 9     | CSP1      | R/W  | 0h    | Chip select polarity for chip select 1<br>0- Active low<br>1- Active high                                                                                                                                                                                                                                        |
| 8     | CKP1      | R/W  | 0h    | Clock polarity for chip select 1<br>0- When data is not being transferred, SCK = 0<br>1- When data is not being transferred, SCK = 1                                                                                                                                                                             |
| 7:5   | RESERVED1 | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                                                                 |
| 4:3   | DD0       | R/W  | 0h    | Data delay for chip select 0<br>00- Data is output on the same cycle as the CS_N goes active<br>01- Data is output 1 DCLK cycle after the CS_N goes active<br>10- Data is output 2 DCLK cycles after the CS_N goes active<br>11- Data is output 3 DCLK cycles after the CS_N goes active                         |
| 2     | CKPH0     | R/W  | 0h    | Clock phase for chip select 0.<br>If CKP0 = 0<br>0- Data shifted out on falling edge; input on rising edge<br>1- Data shifted out on rising edge; input on falling edge<br>If CKP0 = 1<br>1- Data shifted out on falling edge; input on rising edge<br>0- Data shifted out on rising edge; input on falling edge |
| 1     | CSP0      | R/W  | 0h    | Chip select polarity for chip select 0<br>0- Active low<br>1- Active high                                                                                                                                                                                                                                        |
| 0     | CKP0      | R/W  | 0h    | Clock polarity for chip select 0<br>0- When data is not being transferred, SCK = 0<br>1- When data is not being transferred, SCK = 1                                                                                                                                                                             |

### 5.21.2.18 QSPI\_SPI\_CMD Register

#### 1 QSPI\_SPI\_CMD Register (Offset = 48h) [reset = 0h]

SPI Command Register (SPICR).

Return to [Summary Table](#)

**Table 5-3048. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 0048h       |

**Figure 5-1005. QSPI\_SPI\_CMD Name Register**

| 31        | 30   | 29        | 28 | 27        | 26 | 25   | 24 |
|-----------|------|-----------|----|-----------|----|------|----|
| RESERVED3 |      | CSNUM     |    | RESERVED2 |    | WLEN |    |
| R         |      | R/W       |    | R         |    | R/W  |    |
| 0h        |      | 0h        |    | 0h        |    | 0h   |    |
| 23        | 22   | 21        | 20 | 19        | 18 | 17   | 16 |
| WLEN      |      |           |    | CMD       |    |      |    |
| R/W       |      |           |    | R/W       |    |      |    |
| 0h        |      |           |    | 0h        |    |      |    |
| 15        | 14   | 13        | 12 | 11        | 10 | 9    | 8  |
| FIRQ      | WIRQ | RESERVED1 |    | FLEN      |    |      |    |
| R/W       | R/W  | R         |    | R/W       |    |      |    |
| 0h        | 0h   | 0h        |    | 0h        |    |      |    |
| 7         | 6    | 5         | 4  | 3         | 2  | 1    | 0  |
| FLEN      |      |           |    |           |    |      |    |
| R/W       |      |           |    |           |    |      |    |
| 0h        |      |           |    |           |    |      |    |

**Table 5-3050. QSPI\_SPI\_CMD Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                              |
|-------|-----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:30 | RESERVED3 | R    | 0h    | Always read as 0                                                                                                                                                                                         |
| 29:28 | CSNUM     | R/W  | 0h    | Device select. Sets the active chip select for the transfer<br>00- Chip Select 0 active<br>01- Chip Select 1 active<br>10- Chip Select 2 active<br>11- Chip Select 3 active                              |
| 27:26 | RESERVED2 | R    | 0h    | Always read as 0                                                                                                                                                                                         |
| 25:19 | WLEN      | R/W  | 0h    | Word length. Sets the size of the individual transfers from 1 128 bits<br>0- 1 bit<br>1- 2 bits<br>127 128 bits                                                                                          |
| 18:16 | CMD       | R/W  | 0h    | Transfer command<br>000- Reserved<br>001- 4 pin Read Single<br>010- 4 pin Write Single<br>011- 4 pin Read Dual<br>100 Reserved<br>101 3 pin Read Single<br>110 3 pin Write Single<br>111 6 pin Read Quad |
| 15    | FIRQ      | R/W  | 0h    | Frame count interrupt enable                                                                                                                                                                             |
| 14    | WIRQ      | R/W  | 0h    | Word count interrupt enable                                                                                                                                                                              |
| 13:12 | RESERVED1 | R    | 0h    | Always read as 0                                                                                                                                                                                         |

**Table 5-3050. QSPI\_SPI\_CMD Register Field Descriptions (continued)**

| Bit  | Field | Type | Reset | Description                                                  |
|------|-------|------|-------|--------------------------------------------------------------|
| 11:0 | FLEN  | R/W  | 0h    | Frame Length<br>0- 1 word<br>1- 2 words<br>4095<br>4096words |



### 5.21.2.19 QSPI\_SPI\_STATUS Register

#### 1 QSPI\_SPI\_STATUS Register (Offset = 4Ch) [reset = 0h]

SPI Status Register (SPISR).

Return to [Summary Table](#)

**Table 5-3051. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 004Ch       |

**Figure 5-1006. QSPI\_SPI\_STATUS Name Register**

|           |    |    |    |       |    |    |      |
|-----------|----|----|----|-------|----|----|------|
| 31        | 30 | 29 | 28 | 27    | 26 | 25 | 24   |
| RESERVED2 |    |    |    | WDCNT |    |    |      |
| R         |    |    |    | R     |    |    |      |
| 0h        |    |    |    | 0h    |    |    |      |
| 23        | 22 | 21 | 20 | 19    | 18 | 17 | 16   |
| WDCNT     |    |    |    |       |    |    |      |
| R         |    |    |    |       |    |    |      |
| 0h        |    |    |    |       |    |    |      |
| 15        | 14 | 13 | 12 | 11    | 10 | 9  | 8    |
| RESERVED1 |    |    |    |       |    |    |      |
| R         |    |    |    |       |    |    |      |
| 0h        |    |    |    |       |    |    |      |
| 7         | 6  | 5  | 4  | 3     | 2  | 1  | 0    |
| RESERVED1 |    |    |    |       | FC | WC | BUSY |
| R         |    |    |    |       | R  | R  | R    |
| 0h        |    |    |    |       | 0h | 0h | 0h   |

**Table 5-3053. QSPI\_SPI\_STATUS Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                   |
|-------|-----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28 | RESERVED2 | R    | 0h    | Always read as 0                                                                                                                                                                                              |
| 27:16 | WDCNT     | R    | 0h    | Word count. This field will reflect the 14096 words transferred                                                                                                                                               |
| 15:3  | RESERVED1 | R    | 0h    | Always read as 0                                                                                                                                                                                              |
| 2     | FC        | R    | 0h    | Frame complete. This bit is set after all of the requested words have been transmitted.<br>0- Transfer is not complete<br>1- Transfer is complete<br>This bit is reset when the SPI Status Register is read   |
| 1     | WC        | R    | 0h    | Word complete. This bit is set after each word transfer is completed.<br>0- Word transfer is not complete<br>1- Word transfer is complete<br>This bit is reset when the SPI Status Register is read           |
| 0     | BUSY      | R    | 0h    | Busy bit. Active transfer in progress. This bit is only set during an active word transfer. Between words, the bit will clear to signal that it is ok to read/write the data registers.<br>0- Idle<br>1- Busy |

### 5.21.2.20 QSPI\_SPI\_DATA Register

#### 1 QSPI\_SPI\_DATA Register (Offset = 50h) [reset = 0h]

SPI Data Register (SPIDR).

Return to [Summary Table](#)

**Table 5-3054. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 0050h       |

**Figure 5-1007. QSPI\_SPI\_DATA Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-3056. QSPI\_SPI\_DATA Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                 |
|------|-------|------|-------|---------------------------------------------|
| 31:0 | DATA  | R/W  | 0h    | Data register for read and write operations |

### 5.21.2.21 QSPI\_SPI\_SETUP0 Register

#### 1 QSPI\_SPI\_SETUP0 Register (Offset = 54h) [reset = 20203h]

Memory Mapped SPI Setup0 Register.

Return to [Summary Table](#)

**Table 5-3057. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 0054h       |

**Figure 5-1008. QSPI\_SPI\_SETUP0 Name Register**

|           |    |           |    |             |    |             |    |
|-----------|----|-----------|----|-------------|----|-------------|----|
| 31        | 30 | 29        | 28 | 27          | 26 | 25          | 24 |
| RESERVED2 |    |           |    | NUM_D_BITS  |    |             |    |
| R         |    |           |    | R/W         |    |             |    |
| 0h        |    |           |    | 0h          |    |             |    |
| 23        | 22 | 21        | 20 | 19          | 18 | 17          | 16 |
| WCMD      |    |           |    |             |    |             |    |
| R/W       |    |           |    |             |    |             |    |
| 2h        |    |           |    |             |    |             |    |
| 15        | 14 | 13        | 12 | 11          | 10 | 9           | 8  |
| RESERVED1 |    | READ_TYPE |    | NUM_D_BYTES |    | NUM_A_BYTES |    |
| R         |    | R/W       |    | R/W         |    | R/W         |    |
| 0h        |    | 0h        |    | 0h          |    | 2h          |    |
| 7         | 6  | 5         | 4  | 3           | 2  | 1           | 0  |
| RCMD      |    |           |    |             |    |             |    |
| R/W       |    |           |    |             |    |             |    |
| 3h        |    |           |    |             |    |             |    |

**Table 5-3059. QSPI\_SPI\_SETUP0 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                                              |
|-------|-------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED2   | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                         |
| 28:24 | NUM_D_BITS  | R/W  | 0h    | Number of dummy bits to use if NUM_D_BYTES = 0                                                                                                                                                                                                                           |
| 23:16 | WCMD        | R/W  | 2h    | Write Command                                                                                                                                                                                                                                                            |
| 15:14 | RESERVED1   | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                         |
| 13:12 | READ_TYPE   | R/W  | 0h    | Determines if the read command is a single, dual or quad read mode command<br>00 Normal read [all data input on spi_din]<br>01 Dual read [odd bytes input on spi_din; even on spi_dout]<br>10 Normal read [all data input on spi_din]<br>11 Quad read [uses spi_qdin0/1] |
| 11:10 | NUM_D_BYTES | R/W  | 0h    | Number of dummy bytes to be used for fast read.<br>0 = use the value in NUM_D_BITS<br>1 = use 8 bits; 2 = use 16 bits; 3 = use 24 bits                                                                                                                                   |
| 9:8   | NUM_A_BYTES | R/W  | 2h    | Number of address bytes to be sent. 0 = 1 byte; 1 = 2 bytes; 2 = 3 bytes; 3 = 4 bytes                                                                                                                                                                                    |
| 7:0   | RCMD        | R/W  | 3h    | Read Command                                                                                                                                                                                                                                                             |

### 5.21.2.22 QSPI\_SPI\_SETUP1 Register

#### 1 QSPI\_SPI\_SETUP1 Register (Offset = 58h) [reset = 20203h]

Memory Mapped SPI Setup1 Register.

Return to [Summary Table](#)

**Table 5-3060. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 0058h       |

**Figure 5-1009. QSPI\_SPI\_SETUP1 Name Register**

|           |    |           |    |             |    |             |    |
|-----------|----|-----------|----|-------------|----|-------------|----|
| 31        | 30 | 29        | 28 | 27          | 26 | 25          | 24 |
| RESERVED2 |    |           |    | NUM_D_BITS  |    |             |    |
| R         |    |           |    | R/W         |    |             |    |
| 0h        |    |           |    | 0h          |    |             |    |
| 23        | 22 | 21        | 20 | 19          | 18 | 17          | 16 |
| WCMD      |    |           |    |             |    |             |    |
| R/W       |    |           |    |             |    |             |    |
| 2h        |    |           |    |             |    |             |    |
| 15        | 14 | 13        | 12 | 11          | 10 | 9           | 8  |
| RESERVED1 |    | READ_TYPE |    | NUM_D_BYTES |    | NUM_A_BYTES |    |
| R         |    | R/W       |    | R/W         |    | R/W         |    |
| 0h        |    | 0h        |    | 0h          |    | 2h          |    |
| 7         | 6  | 5         | 4  | 3           | 2  | 1           | 0  |
| RCMD      |    |           |    |             |    |             |    |
| R/W       |    |           |    |             |    |             |    |
| 3h        |    |           |    |             |    |             |    |

**Table 5-3062. QSPI\_SPI\_SETUP1 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                                              |
|-------|-------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED2   | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                         |
| 28:24 | NUM_D_BITS  | R/W  | 0h    | Number of dummy bits to use if NUM_D_BYTES = 0                                                                                                                                                                                                                           |
| 23:16 | WCMD        | R/W  | 2h    | Write Command                                                                                                                                                                                                                                                            |
| 15:14 | RESERVED1   | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                         |
| 13:12 | READ_TYPE   | R/W  | 0h    | Determines if the read command is a single, dual or quad read mode command<br>00 Normal read [all data input on spi_din]<br>01 Dual read [odd bytes input on spi_din; even on spi_dout]<br>10 Normal read [all data input on spi_din]<br>11 Quad read [uses spi_qdin0/1] |
| 11:10 | NUM_D_BYTES | R/W  | 0h    | Number of dummy bytes to be used for fast read.<br>0 = use the value in NUM_D_BITS<br>1 = use 8 bits; 2 = use 16 bits; 3 = use 24 bits                                                                                                                                   |
| 9:8   | NUM_A_BYTES | R/W  | 2h    | Number of address bytes to be sent. 0 = 1 byte; 1 = 2 bytes; 2 = 3 bytes; 3 = 4 bytes                                                                                                                                                                                    |
| 7:0   | RCMD        | R/W  | 3h    | Read Command                                                                                                                                                                                                                                                             |

### 5.21.2.23 QSPI\_SPI\_SETUP2 Register

#### 1 QSPI\_SPI\_SETUP2 Register (Offset = 5Ch) [reset = 20203h]

Memory Mapped SPI Setup2 Register.

Return to [Summary Table](#)

**Table 5-3063. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 005Ch       |

**Figure 5-1010. QSPI\_SPI\_SETUP2 Name Register**

|           |    |           |    |             |    |             |    |
|-----------|----|-----------|----|-------------|----|-------------|----|
| 31        | 30 | 29        | 28 | 27          | 26 | 25          | 24 |
| RESERVED2 |    |           |    | NUM_D_BITS  |    |             |    |
| R         |    |           |    | R/W         |    |             |    |
| 0h        |    |           |    | 0h          |    |             |    |
| 23        | 22 | 21        | 20 | 19          | 18 | 17          | 16 |
| WCMD      |    |           |    |             |    |             |    |
| R/W       |    |           |    |             |    |             |    |
| 2h        |    |           |    |             |    |             |    |
| 15        | 14 | 13        | 12 | 11          | 10 | 9           | 8  |
| RESERVED1 |    | READ_TYPE |    | NUM_D_BYTES |    | NUM_A_BYTES |    |
| R         |    | R/W       |    | R/W         |    | R/W         |    |
| 0h        |    | 0h        |    | 0h          |    | 2h          |    |
| 7         | 6  | 5         | 4  | 3           | 2  | 1           | 0  |
| RCMD      |    |           |    |             |    |             |    |
| R/W       |    |           |    |             |    |             |    |
| 3h        |    |           |    |             |    |             |    |

**Table 5-3065. QSPI\_SPI\_SETUP2 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                                              |
|-------|-------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED2   | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                         |
| 28:24 | NUM_D_BITS  | R/W  | 0h    | Number of dummy bits to use if NUM_D_BYTES = 0                                                                                                                                                                                                                           |
| 23:16 | WCMD        | R/W  | 2h    | Write Command                                                                                                                                                                                                                                                            |
| 15:14 | RESERVED1   | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                         |
| 13:12 | READ_TYPE   | R/W  | 0h    | Determines if the read command is a single, dual or quad read mode command<br>00 Normal read [all data input on spi_din]<br>01 Dual read [odd bytes input on spi_din; even on spi_dout]<br>10 Normal read [all data input on spi_din]<br>11 Quad read [uses spi_qdin0/1] |
| 11:10 | NUM_D_BYTES | R/W  | 0h    | Number of dummy bytes to be used for fast read.<br>0 = use the value in NUM_D_BITS<br>1 = use 8 bits; 2 = use 16 bits; 3 = use 24 bits                                                                                                                                   |
| 9:8   | NUM_A_BYTES | R/W  | 2h    | Number of address bytes to be sent. 0 = 1 byte; 1 = 2 bytes; 2 = 3 bytes; 3 = 4 bytes                                                                                                                                                                                    |
| 7:0   | RCMD        | R/W  | 3h    | Read Command                                                                                                                                                                                                                                                             |

### 5.21.2.24 QSPI\_SPI\_SETUP3 Register

#### 1 QSPI\_SPI\_SETUP3 Register (Offset = 60h) [reset = 20203h]

Memory Mapped SPI Setup3 Register.

Return to [Summary Table](#)

**Table 5-3066. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 0060h       |

**Figure 5-1011. QSPI\_SPI\_SETUP3 Name Register**

|           |    |           |    |             |    |             |    |
|-----------|----|-----------|----|-------------|----|-------------|----|
| 31        | 30 | 29        | 28 | 27          | 26 | 25          | 24 |
| RESERVED2 |    |           |    | NUM_D_BITS  |    |             |    |
| R         |    |           |    | R/W         |    |             |    |
| 0h        |    |           |    | 0h          |    |             |    |
| 23        | 22 | 21        | 20 | 19          | 18 | 17          | 16 |
| WCMD      |    |           |    |             |    |             |    |
| R/W       |    |           |    |             |    |             |    |
| 2h        |    |           |    |             |    |             |    |
| 15        | 14 | 13        | 12 | 11          | 10 | 9           | 8  |
| RESERVED1 |    | READ_TYPE |    | NUM_D_BYTES |    | NUM_A_BYTES |    |
| R         |    | R/W       |    | R/W         |    | R/W         |    |
| 0h        |    | 0h        |    | 0h          |    | 2h          |    |
| 7         | 6  | 5         | 4  | 3           | 2  | 1           | 0  |
| RCMD      |    |           |    |             |    |             |    |
| R/W       |    |           |    |             |    |             |    |
| 3h        |    |           |    |             |    |             |    |

**Table 5-3068. QSPI\_SPI\_SETUP3 Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                                                                                                                                                                                                                                                              |
|-------|-------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:29 | RESERVED2   | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                         |
| 28:24 | NUM_D_BITS  | R/W  | 0h    | Number of dummy bits to use if NUM_D_BYTES = 0                                                                                                                                                                                                                           |
| 23:16 | WCMD        | R/W  | 2h    | Write Command                                                                                                                                                                                                                                                            |
| 15:14 | RESERVED1   | R    | 0h    | Always read as 0                                                                                                                                                                                                                                                         |
| 13:12 | READ_TYPE   | R/W  | 0h    | Determines if the read command is a single, dual or quad read mode command<br>00 Normal read [all data input on spi_din]<br>01 Dual read [odd bytes input on spi_din; even on spi_dout]<br>10 Normal read [all data input on spi_din]<br>11 Quad read [uses spi_qdin0/1] |
| 11:10 | NUM_D_BYTES | R/W  | 0h    | Number of dummy bytes to be used for fast read.<br>0 = use the value in NUM_D_BITS<br>1 = use 8 bits; 2 = use 16 bits; 3 = use 24 bits                                                                                                                                   |
| 9:8   | NUM_A_BYTES | R/W  | 2h    | Number of address bytes to be sent. 0 = 1 byte; 1 = 2 bytes; 2 = 3 bytes; 3 = 4 bytes                                                                                                                                                                                    |
| 7:0   | RCMD        | R/W  | 3h    | Read Command                                                                                                                                                                                                                                                             |

### 5.21.2.25 QSPI\_SPI\_SWITCH Register

#### 1 QSPI\_SPI\_SWITCH Register (Offset = 64h) [reset = 0h]

Memory Mapped SPI Switch Register.

Return to [Summary Table](#)

**Table 5-3069. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 0064h       |

**Figure 5-1012. QSPI\_SPI\_SWITCH Name Register**

|          |    |    |    |    |    |           |        |
|----------|----|----|----|----|----|-----------|--------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25        | 24     |
| RESERVED |    |    |    |    |    |           |        |
| R        |    |    |    |    |    |           |        |
| 0h       |    |    |    |    |    |           |        |
| 23       | 22 | 21 | 20 | 19 | 18 | 17        | 16     |
| RESERVED |    |    |    |    |    |           |        |
| R        |    |    |    |    |    |           |        |
| 0h       |    |    |    |    |    |           |        |
| 15       | 14 | 13 | 12 | 11 | 10 | 9         | 8      |
| RESERVED |    |    |    |    |    |           |        |
| R        |    |    |    |    |    |           |        |
| 0h       |    |    |    |    |    |           |        |
| 7        | 6  | 5  | 4  | 3  | 2  | 1         | 0      |
| RESERVED |    |    |    |    |    | MM_INT_EN | MMPT_S |
| R        |    |    |    |    |    | R/W       | R/W    |
| 0h       |    |    |    |    |    | 0h        | 0h     |

**Table 5-3071. QSPI\_SPI\_SWITCH Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                  |
|------|-----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED  | R    | 0h    | Always read as 0                                                                                                                                                                             |
| 1    | MM_INT_EN | R/W  | 0h    | Memory Mapped mode interrupt enable.<br>0 Interrupts are disabled during memory mapped operations<br>1 Word Count interrupt is enabled for memory mapped operations                          |
| 0    | MMPT_S    | R/W  | 0h    | MMPT select. If 0 [default] config port has is selected to control config of core SPI module. If 1, Memory Mapped Protocol Translator is selected to control config port of core SPI module. |

### 5.21.2.26 QSPI\_SPI\_DATA1 Register

#### 1 QSPI\_SPI\_DATA1 Register (Offset = 68h) [reset = 0h]

SPI Data Register (SPIDR1).

Return to [Summary Table](#)

**Table 5-3072. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 0068h       |

**Figure 5-1013. QSPI\_SPI\_DATA1 Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-3074. QSPI\_SPI\_DATA1 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                 |
|------|-------|------|-------|---------------------------------------------|
| 31:0 | DATA  | R/W  | 0h    | Data register for read and write operations |



### 5.21.2.27 QSPI\_SPI\_DATA2 Register

#### 1 QSPI\_SPI\_DATA2 Register (Offset = 6Ch) [reset = 0h]

SPI Data Register (SPIDR2).

Return to [Summary Table](#)

**Table 5-3075. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 006Ch       |

**Figure 5-1014. QSPI\_SPI\_DATA2 Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-3077. QSPI\_SPI\_DATA2 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                 |
|------|-------|------|-------|---------------------------------------------|
| 31:0 | DATA  | R/W  | 0h    | Data register for read and write operations |

### 5.21.2.28 QSPI\_SPI\_DATA3 Register

#### 1 QSPI\_SPI\_DATA3 Register (Offset = 70h) [reset = 0h]

SPI Data Register (SPIDR3).

Return to [Summary Table](#)

**Table 5-3078. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| QSPI0         | 4820 0070h       |

**Figure 5-1015. QSPI\_SPI\_DATA3 Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DATA |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-3080. QSPI\_SPI\_DATA3 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                 |
|------|-------|------|-------|---------------------------------------------|
| 31:0 | DATA  | R/W  | 0h    | Data register for read and write operations |

## 5.22 RTI

### RTI

#### 5.22.1 RTI Summaries

#### RTI Summaries

**Table 5-3081. RTI Registers, Base Address=5218 0000h, Length=256**

| Offset | Length | Register Name                       | RTI0 Physical Address | RTI1 Physical Address | RTI2 Physical Address |
|--------|--------|-------------------------------------|-----------------------|-----------------------|-----------------------|
| 0h     | 32     | <a href="#">RTI_RTIGCTRL</a>        | 5218 0000h            | 5218 1000h            | 5218 2000h            |
| 4h     | 32     | <a href="#">RTI_RTITBCTRL</a>       | 5218 0004h            | 5218 1004h            | 5218 2004h            |
| 8h     | 32     | <a href="#">RTI_RTICAPCTRL</a>      | 5218 0008h            | 5218 1008h            | 5218 2008h            |
| Ch     | 32     | <a href="#">RTI_RTICOMPCTRL</a>     | 5218 000Ch            | 5218 100Ch            | 5218 200Ch            |
| 10h    | 32     | <a href="#">RTI_RTIFRC0</a>         | 5218 0010h            | 5218 1010h            | 5218 2010h            |
| 14h    | 32     | <a href="#">RTI_RTIUC0</a>          | 5218 0014h            | 5218 1014h            | 5218 2014h            |
| 18h    | 32     | <a href="#">RTI_RTICPUC0</a>        | 5218 0018h            | 5218 1018h            | 5218 2018h            |
| 20h    | 32     | <a href="#">RTI_RTICAFRC0</a>       | 5218 0020h            | 5218 1020h            | 5218 2020h            |
| 24h    | 32     | <a href="#">RTI_RTICAUC0</a>        | 5218 0024h            | 5218 1024h            | 5218 2024h            |
| 30h    | 32     | <a href="#">RTI_RTIFRC1</a>         | 5218 0030h            | 5218 1030h            | 5218 2030h            |
| 34h    | 32     | <a href="#">RTI_RTIUC1</a>          | 5218 0034h            | 5218 1034h            | 5218 2034h            |
| 38h    | 32     | <a href="#">RTI_RTICPUC1</a>        | 5218 0038h            | 5218 1038h            | 5218 2038h            |
| 40h    | 32     | <a href="#">RTI_RTICAFRC1</a>       | 5218 0040h            | 5218 1040h            | 5218 2040h            |
| 44h    | 32     | <a href="#">RTI_RTICAUC1</a>        | 5218 0044h            | 5218 1044h            | 5218 2044h            |
| 50h    | 32     | <a href="#">RTI_RTICOMP0</a>        | 5218 0050h            | 5218 1050h            | 5218 2050h            |
| 54h    | 32     | <a href="#">RTI_RTIUDCP0</a>        | 5218 0054h            | 5218 1054h            | 5218 2054h            |
| 58h    | 32     | <a href="#">RTI_RTICOMP1</a>        | 5218 0058h            | 5218 1058h            | 5218 2058h            |
| 5Ch    | 32     | <a href="#">RTI_RTIUDCP1</a>        | 5218 005Ch            | 5218 105Ch            | 5218 205Ch            |
| 60h    | 32     | <a href="#">RTI_RTICOMP2</a>        | 5218 0060h            | 5218 1060h            | 5218 2060h            |
| 64h    | 32     | <a href="#">RTI_RTIUDCP2</a>        | 5218 0064h            | 5218 1064h            | 5218 2064h            |
| 68h    | 32     | <a href="#">RTI_RTICOMP3</a>        | 5218 0068h            | 5218 1068h            | 5218 2068h            |
| 6Ch    | 32     | <a href="#">RTI_RTIUDCP3</a>        | 5218 006Ch            | 5218 106Ch            | 5218 206Ch            |
| 70h    | 32     | <a href="#">RTI_RTITBLCOMP</a>      | 5218 0070h            | 5218 1070h            | 5218 2070h            |
| 74h    | 32     | <a href="#">RTI_RTITBHCMP</a>       | 5218 0074h            | 5218 1074h            | 5218 2074h            |
| 80h    | 32     | <a href="#">RTI_RTISETINT</a>       | 5218 0080h            | 5218 1080h            | 5218 2080h            |
| 84h    | 32     | <a href="#">RTI_RTICLEARINT</a>     | 5218 0084h            | 5218 1084h            | 5218 2084h            |
| 88h    | 32     | <a href="#">RTI_RTIINTFLAG</a>      | 5218 0088h            | 5218 1088h            | 5218 2088h            |
| 90h    | 32     | <a href="#">RTI_RTIDWDCTRL</a>      | 5218 0090h            | 5218 1090h            | 5218 2090h            |
| 94h    | 32     | <a href="#">RTI_RTIDWDPRLD</a>      | 5218 0094h            | 5218 1094h            | 5218 2094h            |
| 98h    | 32     | <a href="#">RTI_RTIWDSTATUS</a>     | 5218 0098h            | 5218 1098h            | 5218 2098h            |
| 9Ch    | 32     | <a href="#">RTI_RTIWDKEY</a>        | 5218 009Ch            | 5218 109Ch            | 5218 209Ch            |
| A0h    | 32     | <a href="#">RTI_RTIDWDCNTR</a>      | 5218 00A0h            | 5218 10A0h            | 5218 20A0h            |
| A4h    | 32     | <a href="#">RTI_RTIWDRXNCTRL</a>    | 5218 00A4h            | 5218 10A4h            | 5218 20A4h            |
| A8h    | 32     | <a href="#">RTI_RTIWWDSECTRL</a>    | 5218 00A8h            | 5218 10A8h            | 5218 20A8h            |
| ACh    | 32     | <a href="#">RTI_RTIINTCLRENABLE</a> | 5218 00ACh            | 5218 10ACh            | 5218 20ACh            |
| B0h    | 32     | <a href="#">RTI_RTICOMP0CLR</a>     | 5218 00B0h            | 5218 10B0h            | 5218 20B0h            |
| B4h    | 32     | <a href="#">RTI_RTICOMP1CLR</a>     | 5218 00B4h            | 5218 10B4h            | 5218 20B4h            |
| B8h    | 32     | <a href="#">RTI_RTICOMP2CLR</a>     | 5218 00B8h            | 5218 10B8h            | 5218 20B8h            |

**Table 5-3081. RTI Registers, Base Address=5218 0000h, Length=256 (continued)**

| Offset | Length | Register Name                   | RTI0 Physical Address | RTI1 Physical Address | RTI2 Physical Address |
|--------|--------|---------------------------------|-----------------------|-----------------------|-----------------------|
| BCh    | 32     | <a href="#">RTI_RTICOMP3CLR</a> | 5218 00BCh            | 5218 10BCh            | 5218 20BCh            |

**Table 5-3082. RTI Registers, Base Address=5218 0000h, Length=256**

| Offset | Length | Register Name                      | RTI3 Physical Address |
|--------|--------|------------------------------------|-----------------------|
| 0h     | 32     | <a href="#">RTI_RTIGCTRL</a>       | 5218 3000h            |
| 4h     | 32     | <a href="#">RTI_RTITBCTRL</a>      | 5218 3004h            |
| 8h     | 32     | <a href="#">RTI_RTICAPCTRL</a>     | 5218 3008h            |
| Ch     | 32     | <a href="#">RTI_RTICOMPCTRL</a>    | 5218 300Ch            |
| 10h    | 32     | <a href="#">RTI_RTIFRC0</a>        | 5218 3010h            |
| 14h    | 32     | <a href="#">RTI_RTIUC0</a>         | 5218 3014h            |
| 18h    | 32     | <a href="#">RTI_RTICPUC0</a>       | 5218 3018h            |
| 20h    | 32     | <a href="#">RTI_RTICAFRC0</a>      | 5218 3020h            |
| 24h    | 32     | <a href="#">RTI_RTICAUC0</a>       | 5218 3024h            |
| 30h    | 32     | <a href="#">RTI_RTIFRC1</a>        | 5218 3030h            |
| 34h    | 32     | <a href="#">RTI_RTIUC1</a>         | 5218 3034h            |
| 38h    | 32     | <a href="#">RTI_RTICPUC1</a>       | 5218 3038h            |
| 40h    | 32     | <a href="#">RTI_RTICAFRC1</a>      | 5218 3040h            |
| 44h    | 32     | <a href="#">RTI_RTICAUC1</a>       | 5218 3044h            |
| 50h    | 32     | <a href="#">RTI_RTICOMP0</a>       | 5218 3050h            |
| 54h    | 32     | <a href="#">RTI_RTIUDCP0</a>       | 5218 3054h            |
| 58h    | 32     | <a href="#">RTI_RTICOMP1</a>       | 5218 3058h            |
| 5Ch    | 32     | <a href="#">RTI_RTIUDCP1</a>       | 5218 305Ch            |
| 60h    | 32     | <a href="#">RTI_RTICOMP2</a>       | 5218 3060h            |
| 64h    | 32     | <a href="#">RTI_RTIUDCP2</a>       | 5218 3064h            |
| 68h    | 32     | <a href="#">RTI_RTICOMP3</a>       | 5218 3068h            |
| 6Ch    | 32     | <a href="#">RTI_RTIUDCP3</a>       | 5218 306Ch            |
| 70h    | 32     | <a href="#">RTI_RTITBLCOMP</a>     | 5218 3070h            |
| 74h    | 32     | <a href="#">RTI_RTITBHCOMP</a>     | 5218 3074h            |
| 80h    | 32     | <a href="#">RTI_RTISSETINT</a>     | 5218 3080h            |
| 84h    | 32     | <a href="#">RTI_RTICLEARINT</a>    | 5218 3084h            |
| 88h    | 32     | <a href="#">RTI_RTIINTFLAG</a>     | 5218 3088h            |
| 90h    | 32     | <a href="#">RTI_RTIDWDCTRL</a>     | 5218 3090h            |
| 94h    | 32     | <a href="#">RTI_RTIDWDPRLD</a>     | 5218 3094h            |
| 98h    | 32     | <a href="#">RTI_RTIWDSTATUS</a>    | 5218 3098h            |
| 9Ch    | 32     | <a href="#">RTI_RTIWDKEY</a>       | 5218 309Ch            |
| A0h    | 32     | <a href="#">RTI_RTIDWDCNTR</a>     | 5218 30A0h            |
| A4h    | 32     | <a href="#">RTI_RTIWWDRXNCTRL</a>  | 5218 30A4h            |
| A8h    | 32     | <a href="#">RTI_RTIWWDSIZECTRL</a> | 5218 30A8h            |
| ACH    | 32     | <a href="#">RTI_RTIINTCLREABLE</a> | 5218 30ACH            |
| B0h    | 32     | <a href="#">RTI_RTICOMP0CLR</a>    | 5218 30B0h            |
| B4h    | 32     | <a href="#">RTI_RTICOMP1CLR</a>    | 5218 30B4h            |
| B8h    | 32     | <a href="#">RTI_RTICOMP2CLR</a>    | 5218 30B8h            |
| BCh    | 32     | <a href="#">RTI_RTICOMP3CLR</a>    | 5218 30BCh            |

### **5.22.2 RTI Registers**

#### **RTI Registers**

### 5.22.2.1 RTI\_RTIGCTRL Register

#### 1 RTI\_RTIGCTRL Register (Offset = 0h) [reset = 0h]

Global Control Register starts / stops the counters .

Return to [Summary Table](#)

**Table 5-3083. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 0000h       |
| RTI1          | 5218 1000h       |
| RTI2          | 5218 2000h       |
| RTI3          | 5218 3000h       |

**Figure 5-1016. RTI\_RTIGCTRL Name Register**

|           |           |    |    |        |    |        |        |
|-----------|-----------|----|----|--------|----|--------|--------|
| 31        | 30        | 29 | 28 | 27     | 26 | 25     | 24     |
| RESERVED2 |           |    |    |        |    |        |        |
| R/W       |           |    |    |        |    |        |        |
| 0h        |           |    |    |        |    |        |        |
| 23        | 22        | 21 | 20 | 19     | 18 | 17     | 16     |
| RESERVED2 |           |    |    | NTUSEL |    |        |        |
| R/W       |           |    |    | R/W    |    |        |        |
| 0h        |           |    |    | 0h     |    |        |        |
| 15        | 14        | 13 | 12 | 11     | 10 | 9      | 8      |
| COS       | RESERVED1 |    |    |        |    |        |        |
| R/W       | R/W       |    |    |        |    |        |        |
| 0h        | 0h        |    |    |        |    |        |        |
| 7         | 6         | 5  | 4  | 3      | 2  | 1      | 0      |
| RESERVED1 |           |    |    |        |    | CNT1EN | CNT0EN |
| R/W       |           |    |    |        |    | R/W    | R/W    |
| 0h        |           |    |    |        |    | 0h     | 0h     |

**Table 5-3085. RTI\_RTIGCTRL Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED2 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 19:16 | NTUSEL    | R/W  | 0h    | NTUSEL: Select NTU signal.<br>These bits determine which NTU input signal is used as external timebase. There are up to four inputs supported with four valid selection combinations. Any invalid selection value written to the NTUSEL bit-field will result in a TIED LOW being used as the NTU signal. The NTU signal will also be TIED LOW in case of a single-bit flip as it will result in an invalid combination of NTUSEL.<br>User and privilege mode [read]:<br>0000= NTU0<br>0101= NTU1<br>1010= NTU2<br>1111= NTU3<br>other = tied to 0<br>Privilege mode [write]:<br>0000= NTU0<br>0101= NTU1<br>1010= NTU2<br>1111= NTU3<br>other = tied to 0 |

**Table 5-3085. RTI\_RTIGCTRL Register Field Descriptions (continued)**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                              |
|------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | COS       | R/W  | 0h    | COS: Continue On Suspend.<br>This bit determines if both counters are stopped when the device goes into debug mode or if they continue counting.<br>User and privilege mode [read]:<br>0 = counters are stopped while in debug mode<br>1 = counters are running while in debug mode<br>Privilege mode [write]:<br>0 = stop counters in debug mode<br>1 = continue counting in debug mode |
| 14:2 | RESERVED1 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                                                    |
| 1    | CNT1EN    | R/W  | 0h    | CNT1EN: Counter 1 Enable. The CNT1EN bit starts and stops the operation of counter block 1 [UC1 and FRC1].<br>User and privilege mode [read]:<br>0 = counters are stopped<br>1 = counters are running<br>Privilege mode [write]:<br>0 = stop counters<br>1 = start counters<br>Gives the absolute 32 bit destination address [physical].                                                 |
| 0    | CNT0EN    | R/W  | 0h    | CNT0EN: Counter 0 Enable. The CNT0EN bit starts and stops the operation of counter block 0 [UC0 and FRC0].<br>User and privilege mode [read]:<br>0 = counters are stopped<br>1 = counters are running<br>Privilege mode [write]:<br>0 = stop counters<br>1 = start counters<br>Gives the absolute 32 bits source address [physical].                                                     |

### 5.22.2.2 RTI\_RTITBCTRL Register

#### 1 RTI\_RTITBCTRL Register (Offset = 4h) [reset = 0h]

Timebase Control selection which source triggers free running counter 0 .

Return to [Summary Table](#)

**Table 5-3086. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 0004h       |
| RTI1          | 5218 1004h       |
| RTI2          | 5218 2004h       |
| RTI3          | 5218 3004h       |

**Figure 5-1017. RTI\_RTITBCTRL Name Register**

|           |    |    |    |    |    |     |       |
|-----------|----|----|----|----|----|-----|-------|
| 31        | 30 | 29 | 28 | 27 | 26 | 25  | 24    |
| RESERVED3 |    |    |    |    |    |     |       |
| R/W       |    |    |    |    |    |     |       |
| 0h        |    |    |    |    |    |     |       |
| 23        | 22 | 21 | 20 | 19 | 18 | 17  | 16    |
| RESERVED3 |    |    |    |    |    |     |       |
| R/W       |    |    |    |    |    |     |       |
| 0h        |    |    |    |    |    |     |       |
| 15        | 14 | 13 | 12 | 11 | 10 | 9   | 8     |
| RESERVED3 |    |    |    |    |    |     |       |
| R/W       |    |    |    |    |    |     |       |
| 0h        |    |    |    |    |    |     |       |
| 7         | 6  | 5  | 4  | 3  | 2  | 1   | 0     |
| RESERVED3 |    |    |    |    |    | INC | TBEXT |
| R/W       |    |    |    |    |    | R/W | R/W   |
| 0h        |    |    |    |    |    | 0h  | 0h    |

**Table 5-3088. RTI\_RTITBCTRL Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED3 | R/W  | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 1    | INC       | R/W  | 0h    | <p>INC: Increment Free Running Counter 0.</p> <p>This bit determines whether the Free Running Counter 0 is automatically incremented if a failing clock on the NTUx signal is detected.</p> <p>User and privilege mode [read]:</p> <p>0 = FRC0 will not be incremented</p> <p>1 = FRC0 will be incremented</p> <p>Privilege mode [write]:</p> <p>0 = Do not increment FRC0 on failing external clock</p> <p>1 = Increment FRC0 on failing external clock</p> |



**Table 5-3088. RTI\_RTITBCTRL Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | TBEXT | R/W  | 0h    | <p>TBEXT: Timebase External.</p> <p>The Timebase External bit selects whether the Free Running Counter 0 is clocked by the internal Up Counter 0 or from the external signal NTUx. Since setting the TBEXT bit to 1 resets Up Counter 0, Free Running Counter 0 will not be incremented in this occurrence. The only source which is able to increment Free Running Counter 0 is NTUx.</p> <p>When the Timebase Supervisor circuit detects a missing clockedge, then the TBEXT bit is reset.</p> <p>The selection if the external signal should be used, can only be done by software.</p> <p>User and privilege mode [read]:</p> <p>0 = UC0 clocks FRC0</p> <p>1 = NTUx clocks FRC0</p> <p>Privilege mode [write]:</p> <p>0 = MUX is switched to internal UC0 clocking scheme</p> <p>1 = MUX is switched to external NTUx clocking scheme</p> |

### 5.22.2.3 RTI\_RTICAPCTRL Register

#### 1 RTI\_RTICAPCTRL Register (Offset = 8h) [reset = 0h]

Capture Control controls the capture source for the counters.

Return to [Summary Table](#)

**Table 5-3089. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 0008h       |
| RTI1          | 5218 1008h       |
| RTI2          | 5218 2008h       |
| RTI3          | 5218 3008h       |

**Figure 5-1018. RTI\_RTICAPCTRL Name Register**

|           |    |    |    |    |    |          |          |
|-----------|----|----|----|----|----|----------|----------|
| 31        | 30 | 29 | 28 | 27 | 26 | 25       | 24       |
| RESERVED4 |    |    |    |    |    |          |          |
| R/W       |    |    |    |    |    |          |          |
| 0h        |    |    |    |    |    |          |          |
| 23        | 22 | 21 | 20 | 19 | 18 | 17       | 16       |
| RESERVED4 |    |    |    |    |    |          |          |
| R/W       |    |    |    |    |    |          |          |
| 0h        |    |    |    |    |    |          |          |
| 15        | 14 | 13 | 12 | 11 | 10 | 9        | 8        |
| RESERVED4 |    |    |    |    |    |          |          |
| R/W       |    |    |    |    |    |          |          |
| 0h        |    |    |    |    |    |          |          |
| 7         | 6  | 5  | 4  | 3  | 2  | 1        | 0        |
| RESERVED4 |    |    |    |    |    | CAPCNTR1 | CAPCNTR0 |
| R/W       |    |    |    |    |    | R/W      | R/W      |
| 0h        |    |    |    |    |    | 0h       | 0h       |

**Table 5-3091. RTI\_RTICAPCTRL Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------|-----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED4 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                                                                                                                     |
| 1    | CAPCNTR1  | R/W  | 0h    | CAPCNTR1: Capture Counter 1.<br>This bit determines, which external interrupt source triggers a capture event of both UC1 and FRC1.<br>User and privilege mode [read]:<br>0 = capture event is triggered by Capture Event Source 0<br>1 = capture event is triggered by Capture Event Source 1<br>Privilege mode [write]:<br>0 = enable capture event triggered by Capture Event Source 0<br>1 = enable capture event triggered by Capture Event Source 1 |

**Table 5-3091. RTI\_RTICAPCTRL Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-----|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | CAPCNTR0 | R/W  | 0h    | <p>CAPCNTR0: Capture Counter 0.</p> <p>This bit determines, which external interrupt source triggers a capture event of both UC0 and FRC0.</p> <p>User and privilege mode [read]:</p> <p>0 = capture event is triggered by Capture Event Source 0</p> <p>1 = capture event is triggered by Capture Event Source 1</p> <p>Privilege mode [write]:</p> <p>0 = enable capture event triggered by Capture Event Source 0</p> <p>1 = enable capture event triggered by Capture Event Source 1</p> <p>11 indexed</p> <p>10 reserved</p> <p>01 post-increment</p> <p>00 constant</p> |

### 5.22.2.4 RTI\_RTICOMPCTRL Register

#### 1 RTI\_RTICOMPCTRL Register (Offset = Ch) [reset = 0h]

Compare Control controls the source for the compare registers.

Return to [Summary Table](#)

**Table 5-3092. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 000Ch       |
| RTI1          | 5218 100Ch       |
| RTI2          | 5218 200Ch       |
| RTI3          | 5218 300Ch       |

**Figure 5-1019. RTI\_RTICOMPCTRL Name Register**

|           |    |    |          |           |    |    |          |
|-----------|----|----|----------|-----------|----|----|----------|
| 31        | 30 | 29 | 28       | 27        | 26 | 25 | 24       |
| RESERVED8 |    |    |          |           |    |    |          |
| R/W       |    |    |          |           |    |    |          |
| 0h        |    |    |          |           |    |    |          |
| 23        | 22 | 21 | 20       | 19        | 18 | 17 | 16       |
| RESERVED8 |    |    |          |           |    |    |          |
| R/W       |    |    |          |           |    |    |          |
| 0h        |    |    |          |           |    |    |          |
| 15        | 14 | 13 | 12       | 11        | 10 | 9  | 8        |
| RESERVED8 |    |    | COMP3SEL | RESERVED7 |    |    | COMP2SEL |
| R/W       |    |    | R/W      | R/W       |    |    | R/W      |
| 0h        |    |    | 0h       | 0h        |    |    | 0h       |
| 7         | 6  | 5  | 4        | 3         | 2  | 1  | 0        |
| RESERVED6 |    |    | COMP1SEL | RESERVED5 |    |    | COMP0SEL |
| R/W       |    |    | R/W      | R/W       |    |    | R/W      |
| 0h        |    |    | 0h       | 0h        |    |    | 0h       |

**Table 5-3094. RTI\_RTICOMPCTRL Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                           |
|-------|-----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:13 | RESERVED8 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                 |
| 12    | COMP3SEL  | R/W  | 0h    | COMPSEL3: Compare Select 3.<br>This bit determines the counter with which the compare value hold in compare register 3 is compared.<br>User and privilege mode [read]:<br>0 = value will be compared with FRC 0<br>1 = value will be compared with FRC 1<br>Privilege mode [write]:<br>0 = enable compare with FRC 0<br>1 = enable compare with FRC 1 |
| 11:9  | RESERVED7 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                 |

**Table 5-3094. RTI\_RTICOMPCTRL Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                           |
|-----|-----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8   | COMP2SEL  | R/W  | 0h    | COMPSEL2: Compare Select 2.<br>This bit determines the counter with which the compare value hold in compare register 2 is compared.<br>User and privilege mode [read]:<br>0 = value will be compared with FRC 0<br>1 = value will be compared with FRC 1<br>Privilege mode [write]:<br>0 = enable compare with FRC 0<br>1 = enable compare with FRC 1 |
| 7:5 | RESERVED6 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                 |
| 4   | COMP1SEL  | R/W  | 0h    | COMPSEL1: Compare Select 1.<br>This bit determines the counter with which the compare value hold in compare register 1 is compared. User and privilege mode [read]:<br>0 = value will be compared with FRC 0<br>1 = value will be compared with FRC 1<br>Privilege mode [write]:<br>0 = enable compare with FRC 0<br>1 = enable compare with FRC 1    |
| 3:1 | RESERVED5 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                 |
| 0   | COMP0SEL  | R/W  | 0h    | COMPSEL0: Compare Select 0.<br>This bit determines the counter with which the compare value hold in compare register 0 is compared.<br>User and privilege mode [read]:<br>0 = value will be compared with FRC 0<br>1 = value will be compared with FRC 1<br>Privilege mode [write]:<br>0 = enable compare with FRC 0<br>1 = enable compare with FRC 1 |

### 5.22.2.5 RTI\_RTIFRC0 Register

#### 1 RTI\_RTIFRC0 Register (Offset = 10h) [reset = 0h]

Free Running Counter 0 current value of free running counter 0

Return to [Summary Table](#)

**Table 5-3095. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 0010h       |
| RTI1          | 5218 1010h       |
| RTI2          | 5218 2010h       |
| RTI3          | 5218 3010h       |

**Figure 5-1020. RTI\_RTIFRC0 Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FRC0 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FRC0 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FRC0 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FRC0 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-3097. RTI\_RTIFRC0 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | FRC0  | R/W  | 0h    | <p>FRC0: Free Running Counter 0.</p> <p>This registers holds the current value of the Free Running Counter 0 and will be updated continuously.</p> <p>User and privilege mode [read]:<br/>current value of the counter</p> <p>Privilege mode [write]:<br/>The counter can be preset by Writing to this register. The counter increments then from this written value upwards.</p> <p>Note: Presetting counters<br/>If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0.</p> |

### 5.22.2.6 RTI\_RTIUC0 Register

#### 1 RTI\_RTIUC0 Register (Offset = 14h) [reset = 0h]

Up Counter 0 current value of prescale counter 0

Return to [Summary Table](#)

**Table 5-3098. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 0014h       |
| RTI1          | 5218 1014h       |
| RTI2          | 5218 2014h       |
| RTI3          | 5218 3014h       |

**Figure 5-1021. RTI\_RTIUC0 Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UC0 |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UC0 |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| UC0 |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| UC0 |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 5-3100. RTI\_RTIUC0 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | UC0   | R/W  | 0h    | <p>UC0: Up Counter 0.</p> <p>This registers holds the current value of the Up Counter 0 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 0. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up Counter 0 and Free Running Counter 0.</p> <p>User and privilege mode [read]:<br/>value of the counter when the Free Running Counter 0 was read</p> <p>Privilege mode [write]:<br/>the counter can be preset by Writing to this register. The counter increments then from this written value upwards.</p> <p>Note: Presetting counters<br/>If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0.</p> <p>Note: Preset value concern<br/>If the preset value is bigger than the compare value stored in register RTICPUC0 then it can take a long time until a compare matches, since RTIUC0 has to count up until it overflows.</p> |

### 5.22.2.7 RTI\_RTICPUC0 Register

#### 1 RTI\_RTICPUC0 Register (Offset = 18h) [reset = 0h]

Compare Up Counter 0 compare value compared with prescale counter 0

Return to [Summary Table](#)

**Table 5-3101. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 0018h       |
| RTI1          | 5218 1018h       |
| RTI2          | 5218 2018h       |
| RTI3          | 5218 3018h       |

**Figure 5-1022. RTI\_RTICPUC0 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CPUC0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CPUC0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CPUC0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CPUC0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3103. RTI\_RTICPUC0 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CPUC0 | R/W  | 0h    | <p>This registers holds the compare value, which is compared with the Up Counter 0. When the compare matches, Free Running counter 0 is incremented. The Up Counter is set to zero when the counter value matches the CPUC0 value. The value set in this prescales the RTI clock.</p> <p>If CPUC0 =<br/> 0:then, frequency = RTICLK/ [2^32]<br/> If CPUC0<br/> 0:then , frequency = RTICLK/[CPUC0 + 1]</p> <p>User and privilege mode [read]:<br/> current compare value<br/> Privilege mode [write when TBEXT = 0]:<br/> the compare value is updated<br/> Privilege mode [write when TBEXT = 1]:<br/> the compare value is not changed</p> |



### 5.22.2.8 RTI\_RTICAFRC0 Register

#### 1 RTI\_RTICAFRC0 Register (Offset = 20h) [reset = 0h]

Capture Free Running Counter 0 current value of free running counter 0 on external event.

Return to [Summary Table](#)

**Table 5-3104. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 0020h       |
| RTI1          | 5218 1020h       |
| RTI2          | 5218 2020h       |
| RTI3          | 5218 3020h       |

**Figure 5-1023. RTI\_RTICAFRC0 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAFR0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAFR0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAFR0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAFR0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3106. RTI\_RTICAFRC0 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                       |
|------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CAFR0 | R/W  | 0h    | CAFR0: Capture Free Running Counter 0.<br>This registers captures the current value of the Free Running Counter 0 when a event occurs, controlled by the external capture control block.<br>User and privilege mode [read]:<br>value of Free Running Counter 0 on a capture event |

### 5.22.2.9 RTI\_RTICAUC0 Register

#### 1 RTI\_RTICAUC0 Register (Offset = 24h) [reset = 0h]

Capture Up Counter 0 current value of prescale counter 0 on external event.

Return to [Summary Table](#)

**Table 5-3107. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 0024h       |
| RTI1          | 5218 1024h       |
| RTI2          | 5218 2024h       |
| RTI3          | 5218 3024h       |

**Figure 5-1024. RTI\_RTICAUC0 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAUC0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAUC0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAUC0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAUC0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3109. RTI\_RTICAUC0 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CAUC0 | R/W  | 0h    | CAUC0: Capture Up Counter 0.<br>This registers captures the current value of the Up Counter 0 when a event occurs, controlled by the external capture control block. The read sequence has to be the same as with Up Counter 0 and Free Running Counter 0. So the RTICAFRC0 register has to be read first, before the RTICAUC0 register is read. This sequence ensures that the value of the RTICAUC0 register is the corresponding value to the RTICAFRC0 register, even if another capture event happens in between the two reads.<br>User and privilege mode [read]:<br>value of Up Counter 0 on a capture event |

### 5.22.2.10 RTI\_RTIFRC1 Register

#### 1 RTI\_RTIFRC1 Register (Offset = 30h) [reset = 0h]

Free Running Counter 1 current value of free running counter 1

Return to [Summary Table](#)

**Table 5-3110. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 0030h       |
| RTI1          | 5218 1030h       |
| RTI2          | 5218 2030h       |
| RTI3          | 5218 3030h       |

**Figure 5-1025. RTI\_RTIFRC1 Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FRC1 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FRC1 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FRC1 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FRC1 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-3112. RTI\_RTIFRC1 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | FRC1  | R/W  | 0h    | <p>FRC1: Free Running Counter 1.</p> <p>This registers holds the current value of the Free Running Counter 1 and will be updated continuously.</p> <p>User and privilege mode [read]:<br/>current value of the counter</p> <p>Privilege mode [write]:<br/>The counter can be preset by Writing to this register. The counter increments then from this written value upwards.</p> <p>Note: Presetting counters<br/>If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC1 and RTIFRC1.</p> |

### 5.22.2.11 RTI\_RTIUC1 Register

#### 1 RTI\_RTIUC1 Register (Offset = 34h) [reset = 0h]

Up Counter 1 current value of prescale counter 1

Return to [Summary Table](#)

**Table 5-3113. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 0034h       |
| RTI1          | 5218 1034h       |
| RTI2          | 5218 2034h       |
| RTI3          | 5218 3034h       |

**Figure 5-1026. RTI\_RTIUC1 Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UC1 |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UC1 |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| UC1 |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| UC1 |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 5-3115. RTI\_RTIUC1 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | UC1   | R/W  | 0h    | <p>UC1: Up Counter 1.</p> <p>This registers holds the current value of the Up Counter 1 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 1. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up Counter 1 and Free Running Counter 1.</p> <p>User and privilege mode [read]:<br/>value of the counter when the Free Running Counter 1 was read</p> <p>Privilege mode [write]:<br/>the counter can be preset by Writing to this register. The counter increments then from this written value upwards.</p> <p>Note: Presetting counters<br/>If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC1 and RTIFRC1.</p> <p>Note: Preset value concern<br/>If the preset value is bigger than the compare value stored in register RTICPUC1 then it can take a long time until a compare matches, since RTIUC1 has to count up until it overflows.</p> |

### 5.22.2.12 RTI\_RTICPUC1 Register

#### 1 RTI\_RTICPUC1 Register (Offset = 38h) [reset = 0h]

Compare Up Counter 1 compare value compared with prescale counter 1

Return to [Summary Table](#)

**Table 5-3116. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 0038h       |
| RTI1          | 5218 1038h       |
| RTI2          | 5218 2038h       |
| RTI3          | 5218 3038h       |

**Figure 5-1027. RTI\_RTICPUC1 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CPUC1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CPUC1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CPUC1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CPUC1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3118. RTI\_RTICPUC1 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CPUC1 | R/W  | 0h    | <p>This registers holds the compare value, which is compared with the Up Counter 1. When the compare matches, Free Running Counter 1 is incremented. The Up Counter is set to zero when the counter value matches the CPUC1 value. The value set in this prescales the RTI clock.</p> <p>If CPUC1 =</p> <p>0:then, frequency = RTICLK/ [2^32]</p> <p>If CPUC1</p> <p>0:then , frequency = RTICLK/[CPUC1 + 1]</p> <p>User and privilege mode [read]:</p> <p>current compare value</p> <p>Privilege mode [write when TBEXT = 0]:</p> <p>the compare value is updated</p> <p>Privilege mode [write when TBEXT = 1]:</p> <p>the compare value is not changed</p> |

### 5.22.2.13 RTI\_RTICAFRC1 Register

#### 1 RTI\_RTICAFRC1 Register (Offset = 40h) [reset = 0h]

Capture Free Running Counter 1 current value of free running counter 1 on external event.

Return to [Summary Table](#)

**Table 5-3119. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 0040h       |
| RTI1          | 5218 1040h       |
| RTI2          | 5218 2040h       |
| RTI3          | 5218 3040h       |

**Figure 5-1028. RTI\_RTICAFRC1 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAFR1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAFR1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAFR1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAFR1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3121. RTI\_RTICAFRC1 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                       |
|------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CAFR1 | R/W  | 0h    | CAFR1: Capture Free Running Counter 1.<br>This registers captures the current value of the Free Running Counter 1 when a event occurs, controlled by the external capture control block.<br>User and privilege mode [read]:<br>value of Free Running Counter 1 on a capture event |

### 5.22.2.14 RTI\_RTICAUC1 Register

#### 1 RTI\_RTICAUC1 Register (Offset = 44h) [reset = 0h]

Capture Up Counter 1 current value of prescale counter 1 on external event.

Return to [Summary Table](#)

**Table 5-3122. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 0044h       |
| RTI1          | 5218 1044h       |
| RTI2          | 5218 2044h       |
| RTI3          | 5218 3044h       |

**Figure 5-1029. RTI\_RTICAUC1 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAUC1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAUC1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAUC1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAUC1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3124. RTI\_RTICAUC1 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CAUC1 | R/W  | 0h    | CAUC1: Capture Up Counter 1.<br>This registers captures the current value of the Up Counter 1 when a event occurs, controlled by the external capture control block. The read sequence has to be the same as with Up Counter 1 and Free Running Counter 1. So the RTICAFRC1 register has to be read first, before the RTICAUC1 register is read. This sequence ensures that the value of the RTICAUC1 register is the corresponding value to the RTICAFRC1 register, even if another capture event happens in between the two reads.<br>User and privilege mode [read]:<br>value of Up Counter 1 on a capture event |

### 5.22.2.15 RTI\_RTICOMP0 Register

#### 1 RTI\_RTICOMP0 Register (Offset = 50h) [reset = 0h]

Compare 0 compare value to be compared with the counters.

Return to [Summary Table](#)

**Table 5-3125. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 0050h       |
| RTI1          | 5218 1050h       |
| RTI2          | 5218 2050h       |
| RTI3          | 5218 3050h       |

**Figure 5-1030. RTI\_RTICOMP0 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COMP0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COMP0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COMP0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COMP0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3127. RTI\_RTICOMP0 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | COMP0 | R/W  | 0h    | <p>COMP0: Compare 0.</p> <p>This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request.</p> <p>User and privilege mode [read]:<br/>current compare value</p> <p>Privilege mode [write]:<br/>update of the compare register with a new compare value</p> <p>Note: Reset behavior<br/>A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.</p> |



### 5.22.2.16 RTI\_RTIUDCP0 Register

#### 1 RTI\_RTIUDCP0 Register (Offset = 54h) [reset = 0h]

Update Compare 0 value to be added to the compare register 0 value on compare match.

Return to [Summary Table](#)

**Table 5-3128. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 0054h       |
| RTI1          | 5218 1054h       |
| RTI2          | 5218 2054h       |
| RTI3          | 5218 3054h       |

**Figure 5-1031. RTI\_RTIUDCP0 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UDCP0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UDCP0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| UDCP0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| UDCP0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3130. RTI\_RTIUDCP0 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                |
|------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | UDCP0 | R/W  | 0h    | UDCP0: Update Compare 0 Register.<br>This registers holds a value, which is added to the value in the compare 0 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.<br>User and privilege mode [read]:<br>value to be added to the compare 0 register on the next compare match<br>Privilege mode [write]:<br>new update value |

### 5.22.2.17 RTI\_RTICOMP1 Register

#### 1 RTI\_RTICOMP1 Register (Offset = 58h) [reset = 0h]

Compare 1 compare value to be compared with the counters.

Return to [Summary Table](#)

**Table 5-3131. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 0058h       |
| RTI1          | 5218 1058h       |
| RTI2          | 5218 2058h       |
| RTI3          | 5218 3058h       |

**Figure 5-1032. RTI\_RTICOMP1 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COMP1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COMP1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COMP1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COMP1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3133. RTI\_RTICOMP1 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | COMP1 | R/W  | 0h    | <p>COMP1: compare1.</p> <p>This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request.</p> <p>User and privilege mode [read]:</p> <p>current compare value</p> <p>Privilege mode [write]:</p> <p>update of the compare register with a new compare value</p> <p>Note: Reset behavior</p> <p>A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.</p> |

### 5.22.2.18 RTI\_RTIUDCP1 Register

#### 1 RTI\_RTIUDCP1 Register (Offset = 5Ch) [reset = 0h]

Update Compare 1 value to be added to the compare register 1 value on compare match.

Return to [Summary Table](#)

**Table 5-3134. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 005Ch       |
| RTI1          | 5218 105Ch       |
| RTI2          | 5218 205Ch       |
| RTI3          | 5218 305Ch       |

**Figure 5-1033. RTI\_RTIUDCP1 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UDCP1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UDCP1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| UDCP1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| UDCP1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3136. RTI\_RTIUDCP1 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                             |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | UDCP1 | R/W  | 0h    | UDCP1: Update compare1 Register.<br>This registers holds a value, which is added to the value in the compare1 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.<br>User and privilege mode [read]:<br>value to be added to the compare1 register on the next compare match<br>Privilege mode [write]:<br>new update value |

### 5.22.2.19 RTI\_RTICOMP2 Register

#### 1 RTI\_RTICOMP2 Register (Offset = 60h) [reset = 0h]

Compare 2 compare value to be compared with the counters.

Return to [Summary Table](#)

**Table 5-3137. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 0060h       |
| RTI1          | 5218 1060h       |
| RTI2          | 5218 2060h       |
| RTI3          | 5218 3060h       |

**Figure 5-1034. RTI\_RTICOMP2 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COMP2 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COMP2 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COMP2 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COMP2 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3139. RTI\_RTICOMP2 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | COMP2 | R/W  | 0h    | <p>COMP2: compare 2.</p> <p>This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request.</p> <p>User and privilege mode [read]:</p> <p>current compare value</p> <p>Privilege mode [write]:</p> <p>update of the compare register with a new compare value</p> <p>Note: Reset behavior</p> <p>A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.</p> |

### 5.22.2.20 RTI\_RTIUDCP2 Register

#### 1 RTI\_RTIUDCP2 Register (Offset = 64h) [reset = 0h]

Update Compare 2 value to be added to the compare register 2 value on compare match.

Return to [Summary Table](#)

**Table 5-3140. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 0064h       |
| RTI1          | 5218 1064h       |
| RTI2          | 5218 2064h       |
| RTI3          | 5218 3064h       |

**Figure 5-1035. RTI\_RTIUDCP2 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UDCP2 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UDCP2 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| UDCP2 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| UDCP2 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3142. RTI\_RTIUDCP2 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                |
|------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | UDCP2 | R/W  | 0h    | UDCP2: Update compare 2 Register.<br>This registers holds a value, which is added to the value in the compare 2 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.<br>User and privilege mode [read]:<br>value to be added to the compare 2 register on the next compare match<br>Privilege mode [write]:<br>new update value |

### 5.22.2.21 RTI\_RTICOMP3 Register

#### 1 RTI\_RTICOMP3 Register (Offset = 68h) [reset = 0h]

Compare 3 compare value to be compared with the counters.

Return to [Summary Table](#)

**Table 5-3143. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 0068h       |
| RTI1          | 5218 1068h       |
| RTI2          | 5218 2068h       |
| RTI3          | 5218 3068h       |

**Figure 5-1036. RTI\_RTICOMP3 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COMP3 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COMP3 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COMP3 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COMP3 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3145. RTI\_RTICOMP3 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | COMP3 | R/W  | 0h    | <p>COMP3: compare 3.</p> <p>This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request.</p> <p>User and privilege mode [read]:</p> <p>current compare value</p> <p>Privilege mode [write]:</p> <p>update of the compare register with a new compare value</p> <p>Note: Reset behavior</p> <p>A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.</p> |

### 5.22.2.22 RTI\_RTIUDCP3 Register

#### 1 RTI\_RTIUDCP3 Register (Offset = 6Ch) [reset = 0h]

Update Compare 3 value to be added to the compare register 3 value on compare match.

Return to [Summary Table](#)

**Table 5-3146. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 006Ch       |
| RTI1          | 5218 106Ch       |
| RTI2          | 5218 206Ch       |
| RTI3          | 5218 306Ch       |

**Figure 5-1037. RTI\_RTIUDCP3 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UDCP3 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UDCP3 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| UDCP3 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| UDCP3 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3148. RTI\_RTIUDCP3 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                |
|------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | UDCP3 | R/W  | 0h    | UDCP3: Update compare 3 Register.<br>This registers holds a value, which is added to the value in the compare 3 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.<br>User and privilege mode [read]:<br>value to be added to the compare 3 register on the next compare match<br>Privilege mode [write]:<br>new update value |

### 5.22.2.23 RTI\_RTITBLCOMP Register

#### 1 RTI\_RTITBLCOMP Register (Offset = 70h) [reset = 0h]

Timebase Low Compare compare value to activate edge detection circuit.

Return to [Summary Table](#)

**Table 5-3149. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 0070h       |
| RTI1          | 5218 1070h       |
| RTI2          | 5218 2070h       |
| RTI3          | 5218 3070h       |

**Figure 5-1038. RTI\_RTITBLCOMP Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TBLCOMP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TBLCOMP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TBLCOMP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TBLCOMP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-3151. RTI\_RTITBLCOMP Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|---------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | TBLCOMP | R/W  | 0h    | <p>TBLCOMP: Timebase Low Compare Value.</p> <p>This value determines when the edge detection circuit starts monitoring the NTUx signal. It will be compared with Up Counter 0.</p> <p>User and privilege mode [read]:</p> <p>current compare value</p> <p>Privilege mode [write when TBEXT = 0]:</p> <p>the compare value is updated</p> <p>Privilege mode [write when TBEXT = 1]:</p> <p>the compare value is not changed</p> <p>Note: Reset behavior</p> <p>A reset does not generate a compare match.</p> |



### 5.22.2.24 RTI\_RTITBHCOMP Register

#### 1 RTI\_RTITBHCOMP Register (Offset = 74h) [reset = 0h]

Timebase High Compare compare value to deactivate edge detection circuit.

Return to [Summary Table](#)

**Table 5-3152. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 0074h       |
| RTI1          | 5218 1074h       |
| RTI2          | 5218 2074h       |
| RTI3          | 5218 3074h       |

**Figure 5-1039. RTI\_RTITBHCOMP Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TBHCOMP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TBHCOMP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TBHCOMP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TBHCOMP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-3154. RTI\_RTITBHCOMP Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|---------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | TBHCOMP | R/W  | 0h    | <p>TBHCOMP: Timebase High Compare Value.</p> <p>This value determines when the edge detection circuit will stop monitoring the NTUx signal. It will be compared with Up Counter 0.</p> <p>RTITBHCOMP has to be less than RTICPUC0, since RTIUC0 will be reset when RTICPUC0 is reached.</p> <p>Example:</p> <p>The NTUx edge detection circuit should be active +/- 10 RTICLK cycles around RTICPUC0.</p> <p>RTICPUC0 = 0x00000050</p> <p>RTITBLCOMP = 0x000046</p> <p>RTITBHCOMP = 0x00000009</p> <p>User and privilege mode [read]:</p> <p>current compare value</p> <p>Privilege mode [write when TBEXT = 0]:</p> <p>the compare value is updated</p> <p>Privilege mode [write when TBEXT = 1]:</p> <p>the compare value is not changed</p> <p>Note: Reset behavior</p> <p>A reset does not generate a compare match.</p> |

### 5.22.2.25 RTI\_RTISSETINT Register

#### 1 RTI\_RTISSETINT Register (Offset = 80h) [reset = 0h]

Set Interrupt Enable sets interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation.

Return to [Summary Table](#)

**Table 5-3155. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 0080h       |
| RTI1          | 5218 1080h       |
| RTI2          | 5218 2080h       |
| RTI3          | 5218 3080h       |

**Figure 5-1040. RTI\_RTISSETINT Name Register**

|            |    |    |    |         |            |            |          |
|------------|----|----|----|---------|------------|------------|----------|
| 31         | 30 | 29 | 28 | 27      | 26         | 25         | 24       |
| RESERVED11 |    |    |    |         |            |            |          |
| R/W        |    |    |    |         |            |            |          |
| 0h         |    |    |    |         |            |            |          |
| 23         | 22 | 21 | 20 | 19      | 18         | 17         | 16       |
| RESERVED11 |    |    |    |         | SETOVL1INT | SETOVL0INT | SETTBINT |
| R/W        |    |    |    |         | R/W        | R/W        | R/W      |
| 0h         |    |    |    |         | 0h         | 0h         | 0h       |
| 15         | 14 | 13 | 12 | 11      | 10         | 9          | 8        |
| RESERVED10 |    |    |    | SETDMA3 | SETDMA2    | SETDMA1    | SETDMA0  |
| R/W        |    |    |    | R/W     | R/W        | R/W        | R/W      |
| 0h         |    |    |    | 0h      | 0h         | 0h         | 0h       |
| 7          | 6  | 5  | 4  | 3       | 2          | 1          | 0        |
| RESERVED9  |    |    |    | SETINT3 | SETINT2    | SETINT1    | SETINT0  |
| R/W        |    |    |    | R/W     | R/W        | R/W        | R/W      |
| 0h         |    |    |    | 0h      | 0h         | 0h         | 0h       |

**Table 5-3157. RTI\_RTISSETINT Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                             |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:19 | RESERVED11 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                   |
| 18    | SETOVL1INT | R/W  | 0h    | SETOVL1INT: Set Free Running Counter 1 Overflow Interrupt.<br>User and privilege mode [read]:<br>0 = interrupt is disabled<br>1 = interrupt is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = enable interrupt |
| 17    | SETOVL0INT | R/W  | 0h    | SETOVL0INT: Set Free Running Counter 0 Overflow Interrupt.<br>User and privilege mode [read]:<br>0 = interrupt is disabled<br>1 = interrupt is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = enable interrupt |

**Table 5-3157. RTI\_RTISSETINT Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                            |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 16    | SETTBINT   | R/W  | 0h    | SETTBINT: Set Timebase Interrupt.<br>User and privilege mode [read]:<br>0 = interrupt is disabled<br>1 = interrupt is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = enable interrupt         |
| 15:12 | RESERVED10 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                  |
| 11    | SETDMA3    | R/W  | 0h    | SETDMA3: Set Compare DMA Request 3.<br>User and privilege mode [read]:<br>0 = DMA request is disabled<br>1 = DMA request is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = enable DMA request |
| 10    | SETDMA2    | R/W  | 0h    | SETDMA2: Set Compare DMA Request 2.<br>User and privilege mode [read]:<br>0 = DMA request is disabled<br>1 = DMA request is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = enable DMA request |
| 9     | SETDMA1    | R/W  | 0h    | SETDMA1: Set Compare DMA Request 1.<br>User and privilege mode [read]:<br>0 = DMA request is disabled<br>1 = DMA request is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = enable DMA request |
| 8     | SETDMA0    | R/W  | 0h    | SETDMA0: Set Compare DMA Request 0.<br>User and privilege mode [read]:<br>0 = DMA request is disabled<br>1 = DMA request is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = enable DMA request |
| 7:4   | RESERVED9  | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                  |
| 3     | SETINT3    | R/W  | 0h    | SETINT3: Set Compare Interrupt 3.<br>User and privilege mode [read]:<br>0 = interrupt is disabled<br>1 = interrupt is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged                                 |
| 2     | SETINT2    | R/W  | 0h    | SETINT2: Set Compare Interrupt 2.<br>User and privilege mode [read]:<br>0 = interrupt is disabled<br>1 = interrupt is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = enable interrupt         |
| 1     | SETINT1    | R/W  | 0h    | SETINT1: Set Compare Interrupt 1.<br>User and privilege mode [read]:<br>0 = interrupt is disabled<br>1 = interrupt is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = enable interrupt         |

**Table 5-3157. RTI\_RTISSETINT Register Field Descriptions (continued)**

| Bit | Field   | Type | Reset | Description                                                                                                                                                                                                                    |
|-----|---------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | SETINT0 | R/W  | 0h    | SETINT0: Set Compare Interrupt 0.<br>User and privilege mode [read]:<br>0 = interrupt is disabled<br>1 = interrupt is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = enable interrupt |

### 5.22.2.26 RTI\_RTICLEARINT Register

#### 1 RTI\_RTICLEARINT Register (Offset = 84h) [reset = 0h]

Clear Interrupt Enable clears interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation.

Return to [Summary Table](#)

**Table 5-3158. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 0084h       |
| RTI1          | 5218 1084h       |
| RTI2          | 5218 2084h       |
| RTI3          | 5218 3084h       |

**Figure 5-1041. RTI\_RTICLEARINT Name Register**

|            |    |    |    |           |              |              |           |
|------------|----|----|----|-----------|--------------|--------------|-----------|
| 31         | 30 | 29 | 28 | 27        | 26           | 25           | 24        |
| RESERVED14 |    |    |    |           |              |              |           |
| R/W        |    |    |    |           |              |              |           |
| 0h         |    |    |    |           |              |              |           |
| 23         | 22 | 21 | 20 | 19        | 18           | 17           | 16        |
| RESERVED14 |    |    |    |           | CLEAROVL1INT | CLEAROVL0INT | CLEARINT  |
| R/W        |    |    |    |           | R/W          | R/W          | R/W       |
| 0h         |    |    |    |           | 0h           | 0h           | 0h        |
| 15         | 14 | 13 | 12 | 11        | 10           | 9            | 8         |
| RESERVED13 |    |    |    | CLEARDMA3 | CLEARDMA2    | CLEARDMA1    | CLEARDMA0 |
| R/W        |    |    |    | R/W       | R/W          | R/W          | R/W       |
| 0h         |    |    |    | 0h        | 0h           | 0h           | 0h        |
| 7          | 6  | 5  | 4  | 3         | 2            | 1            | 0         |
| RESERVED12 |    |    |    | CLEARINT3 | CLEARINT2    | CLEARINT1    | CLEARINT0 |
| R/W        |    |    |    | R/W       | R/W          | R/W          | R/W       |
| 0h         |    |    |    | 0h        | 0h           | 0h           | 0h        |

**Table 5-3160. RTI\_RTICLEARINT Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                                                                                                                                                                  |
|-------|--------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:19 | RESERVED14   | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                        |
| 18    | CLEAROVL1INT | R/W  | 0h    | CLEAROVL1INT: CLEAR Free Running Counter 1 Overflow Interrupt.<br>User and privilege mode [read]:<br>0 = interrupt is disabled<br>1 = interrupt is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = disable interrupt |
| 17    | CLEAROVL0INT | R/W  | 0h    | CLEAROVL0INT: CLEAR Free Running Counter 0 Overflow Interrupt.<br>User and privilege mode [read]:<br>0 = interrupt is disabled<br>1 = interrupt is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = disable interrupt |

**Table 5-3160. RTI\_RTICLEARINT Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                 |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 16    | CLEARTBINT | R/W  | 0h    | CLEARTBINT: CLEAR Timebase Interrupt.<br>User and privilege mode [read]:<br>0 = interrupt is disabled<br>1 = interrupt is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = disable interrupt         |
| 15:12 | RESERVED13 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                       |
| 11    | CLEARDMA3  | R/W  | 0h    | CLEARDMA3: CLEAR Compare DMA Request 3.<br>User and privilege mode [read]:<br>0 = DMA request is disabled<br>1 = DMA request is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = disable DMA request |
| 10    | CLEARDMA2  | R/W  | 0h    | CLEARDMA2: CLEAR Compare DMA Request 2.<br>User and privilege mode [read]:<br>0 = DMA request is disabled<br>1 = DMA request is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = disable DMA request |
| 9     | CLEARDMA1  | R/W  | 0h    | CLEARDMA1: CLEAR Compare DMA Request 1.<br>User and privilege mode [read]:<br>0 = DMA request is disabled<br>1 = DMA request is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = disable DMA request |
| 8     | CLEARDMA0  | R/W  | 0h    | CLEARDMA0: CLEAR Compare DMA Request 0.<br>User and privilege mode [read]:<br>0 = DMA request is disabled<br>1 = DMA request is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = disable DMA request |
| 7:4   | RESERVED12 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                       |
| 3     | CLEARINT3  | R/W  | 0h    | CLEARINT3: CLEAR Compare Interrupt 3.<br>User and privilege mode [read]:<br>0 = interrupt is disabled<br>1 = interrupt is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = disable interrupt         |
| 2     | CLEARINT2  | R/W  | 0h    | CLEARINT2: CLEAR Compare Interrupt 2.<br>User and privilege mode [read]:<br>0 = interrupt is disabled<br>1 = interrupt is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = disable interrupt         |
| 1     | CLEARINT1  | R/W  | 0h    | CLEARINT1: CLEAR Compare Interrupt 1.<br>User and privilege mode [read]:<br>0 = interrupt is disabled<br>1 = interrupt is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = disable interrupt         |

**Table 5-3160. RTI\_RTICLEARINT Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description                                                                                                                                                                                                                                                        |
|-----|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | CLEARINT0 | R/W  | 0h    | <p>CLEARINT0: CLEAR Compare Interrupt 0.</p> <p>User and privilege mode [read]:</p> <p>0 = interrupt is disabled</p> <p>1 = interrupt is enabled</p> <p>Privilege mode [write]:</p> <p>0 = leaves the corresponding bit unchanged</p> <p>1 = disable interrupt</p> |

### 5.22.2.27 RTI\_RTIINTFLAG Register

#### 1 RTI\_RTIINTFLAG Register (Offset = 88h) [reset = 0h]

Interrupt Flags interrupt pending bits.

Return to [Summary Table](#)

**Table 5-3161. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 0088h       |
| RTI1          | 5218 1088h       |
| RTI2          | 5218 2088h       |
| RTI3          | 5218 3088h       |

**Figure 5-1042. RTI\_RTIINTFLAG Name Register**

|            |    |    |    |      |         |         |       |
|------------|----|----|----|------|---------|---------|-------|
| 31         | 30 | 29 | 28 | 27   | 26      | 25      | 24    |
| RESERVED16 |    |    |    |      |         |         |       |
| R/W        |    |    |    |      |         |         |       |
| 0h         |    |    |    |      |         |         |       |
| 23         | 22 | 21 | 20 | 19   | 18      | 17      | 16    |
| RESERVED16 |    |    |    |      | OVL1INT | OVL0INT | TBINT |
| R/W        |    |    |    |      | R/W     | R/W     | R/W   |
| 0h         |    |    |    |      | 0h      | 0h      | 0h    |
| 15         | 14 | 13 | 12 | 11   | 10      | 9       | 8     |
| RESERVED15 |    |    |    |      |         |         |       |
| R/W        |    |    |    |      |         |         |       |
| 0h         |    |    |    |      |         |         |       |
| 7          | 6  | 5  | 4  | 3    | 2       | 1       | 0     |
| RESERVED15 |    |    |    | INT3 | INT2    | INT1    | INT0  |
| R/W        |    |    |    | R/W  | R/W     | R/W     | R/W   |
| 0h         |    |    |    | 0h   | 0h      | 0h      | 0h    |

**Table 5-3163. RTI\_RTIINTFLAG Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                  |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:19 | RESERVED16 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                        |
| 18    | OVL1INT    | R/W  | 0h    | OVL1INT: Free Running Counter 1 Overflow Interrupt Flag.<br>User and privilege mode [read]:<br>determines if an interrupt is pending<br>0 = no interrupt pending<br>1 = interrupt pending<br>Privilege mode [write]:<br>0 = leaves the bit unchanged<br>1 = set the bit to 0 |
| 17    | OVL0INT    | R/W  | 0h    | OVL0INT: Free Running Counter 0 Overflow Interrupt Flag.<br>User and privilege mode [read]:<br>determines if an interrupt is pending<br>0 = no interrupt pending<br>1 = interrupt pending<br>Privilege mode [write]:<br>0 = leaves the bit unchanged<br>1 = set the bit to 0 |



**Table 5-3163. RTI\_RTINTFLAG Register Field Descriptions (continued)**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                        |
|------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 16   | TBINT      | R/W  | 0h    | User and privilege mode [read]:<br>this flag is set when the TBEXT bit is cleared by detection of a missing external clockedge. It will not be set by clearing TBEXT by software.<br>determines if an interrupt is pending<br>0 = no interrupt pending<br>1 = interrupt pending<br>Privilege mode [write]:<br>0 = leaves the bit unchanged<br>1 = set the bit to 0 |
| 15:4 | RESERVED15 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                              |
| 3    | INT3       | R/W  | 0h    | INT3: Interrupt Flag 3.<br>User and privilege mode [read]:<br>determines if a interrupt is pending<br>0 = no interrupt pending<br>1 = interrupt pending<br>Privilege mode [write]:<br>0 = leaves the bit unchanged<br>1 = set the bit to 0                                                                                                                         |
| 2    | INT2       | R/W  | 0h    | INT2: Interrupt Flag 2.<br>User and privilege mode [read]:<br>determines if a interrupt is pending<br>0 = no interrupt pending<br>1 = interrupt pending<br>Privilege mode [write]:<br>0 = leaves the bit unchanged<br>1 = set the bit to 0                                                                                                                         |
| 1    | INT1       | R/W  | 0h    | INT1: Interrupt Flag 1.<br>User and privilege mode [read]:<br>determines if a interrupt is pending<br>0 = no interrupt pending<br>1 = interrupt pending<br>Privilege mode [write]:<br>0 = leaves the bit unchanged<br>1 = set the bit to 0                                                                                                                         |
| 0    | INT0       | R/W  | 0h    | INT0: Interrupt Flag 0.<br>User and privilege mode [read]:<br>determines if a interrupt is pending<br>0 = no interrupt pending<br>1 = interrupt pending<br>Privilege mode [write]:<br>0 = leaves the bit unchanged<br>1 = set the bit to 0                                                                                                                         |

### 5.22.2.28 RTI\_RTIDWDCTRL Register

#### 1 RTI\_RTIDWDCTRL Register (Offset = 90h) [reset = 0h]

Digital Watchdog Control Enables the Digital Watchdog.

Return to [Summary Table](#)

**Table 5-3164. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 0090h       |
| RTI1          | 5218 1090h       |
| RTI2          | 5218 2090h       |
| RTI3          | 5218 3090h       |

**Figure 5-1043. RTI\_RTIDWDCTRL Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DWDCTRL |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DWDCTRL |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DWDCTRL |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DWDCTRL |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-3166. RTI\_RTIDWDCTRL Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|------|---------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | DWDCTRL | R/W  | 0h    | <p>DWDCTRL: Digital Watchdog Control.</p> <p>User and privilege mode [read]:</p> <p>0x5312ACED = DWD counter is disabled. This is the default value.</p> <p>0xA98559DA = DWD counter is enabled</p> <p>Any other value = DWD counter state is unchanged [enabled or disabled]</p> <p>Privilege mode [write]:</p> <p>0xA98559DA = DWD counter is enabled</p> <p>Any other value = State of DWD counter is unchanged [stays enabled or disabled]</p> <p>Note: One-Write Functionality of DWDCTRL Register</p> <p>The RTIDWDCTRL register implements a one-write functionality, such that the application cannot write to this register more than once. Writing the default value will not enable the watchdog as described above. Writing the enable value will start the watchdog counters. A write to RTIDWDCTRL will only be enabled after a system reset again.</p> |

### 5.22.2.29 RTI\_RTIDWDPRLD Register

#### 1 RTI\_RTIDWDPRLD Register (Offset = 94h) [reset = 0h]

Digital Watchdog Preload sets the expiration time of the Digital Watchdog.

Return to [Summary Table](#)

**Table 5-3167. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 0094h       |
| RTI1          | 5218 1094h       |
| RTI2          | 5218 2094h       |
| RTI3          | 5218 3094h       |

**Figure 5-1044. RTI\_RTIDWDPRLD Name Register**

|            |    |    |    |         |    |    |    |
|------------|----|----|----|---------|----|----|----|
| 31         | 30 | 29 | 28 | 27      | 26 | 25 | 24 |
| RESERVED17 |    |    |    |         |    |    |    |
| R/W        |    |    |    |         |    |    |    |
| 0h         |    |    |    |         |    |    |    |
| 23         | 22 | 21 | 20 | 19      | 18 | 17 | 16 |
| RESERVED17 |    |    |    |         |    |    |    |
| R/W        |    |    |    |         |    |    |    |
| 0h         |    |    |    |         |    |    |    |
| 15         | 14 | 13 | 12 | 11      | 10 | 9  | 8  |
| RESERVED17 |    |    |    | DWDPRLD |    |    |    |
| R/W        |    |    |    | R/W     |    |    |    |
| 0h         |    |    |    | 0h      |    |    |    |
| 7          | 6  | 5  | 4  | 3       | 2  | 1  | 0  |
| DWDPRLD    |    |    |    |         |    |    |    |
| R/W        |    |    |    |         |    |    |    |
| 0h         |    |    |    |         |    |    |    |

**Table 5-3169. RTI\_RTIDWDPRLD Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED17 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 11:0  | DWDPRLD    | R/W  | 0h    | DWDPRLD: Digital Watchdog Preload Value.<br>User and privileged mode [read]:<br>A read from this register in any CPU mode returns the current preload value.<br>Privileged mode [write]:<br>The DWD preload register can be configured only when the DWD is disabled. Therefore, the application can only configure the DWD preload register before it enables the DWD down counter.<br>The expiration time of the DWD Down Counter can be determined with following equation:<br>$t_{exp} = [RTIDWDPRLD+1] \times 2^{13} / RTICK1$<br>where: RTIDWDPRLD = 0...4095 |

### 5.22.2.30 RTI\_RTIWDSTATUS Register

#### 1 RTI\_RTIWDSTATUS Register (Offset = 98h) [reset = 0h]

Watchdog Status reflects the status of Analog and Digital Watchdog.

Return to [Summary Table](#)

**Table 5-3170. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 0098h       |
| RTI1          | 5218 1098h       |
| RTI2          | 5218 2098h       |
| RTI3          | 5218 3098h       |

**Figure 5-1045. RTI\_RTIWDSTATUS Name Register**

|            |    |         |             |               |       |       |       |
|------------|----|---------|-------------|---------------|-------|-------|-------|
| 31         | 30 | 29      | 28          | 27            | 26    | 25    | 24    |
| RESERVED18 |    |         |             |               |       |       |       |
| R/W        |    |         |             |               |       |       |       |
| 0h         |    |         |             |               |       |       |       |
| 23         | 22 | 21      | 20          | 19            | 18    | 17    | 16    |
| RESERVED18 |    |         |             |               |       |       |       |
| R/W        |    |         |             |               |       |       |       |
| 0h         |    |         |             |               |       |       |       |
| 15         | 14 | 13      | 12          | 11            | 10    | 9     | 8     |
| RESERVED18 |    |         |             |               |       |       |       |
| R/W        |    |         |             |               |       |       |       |
| 0h         |    |         |             |               |       |       |       |
| 7          | 6  | 5       | 4           | 3             | 2     | 1     | 0     |
| RESERVED18 |    | DWWD_ST | ENDTIMEVIOL | STARTTIMEVIOL | KEYST | DWDST | AWDST |
| R/W        |    | R/W     | R/W         | R/W           | R/W   | R/W   | R/W   |
| 0h         |    | 0h      | 0h          | 0h            | 0h    | 0h    | 0h    |

**Table 5-3172. RTI\_RTIWDSTATUS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:6 | RESERVED18 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 5    | DWWD_ST    | R/W  | 0h    | DWWD ST: Windowed Watchdog Status.<br>This bit denotes whether the time-window defined by the windowed watchdog configuration has been violated, or if a wrong key or key sequence was written to service the watchdog.<br>User and privilege mode [read]:<br>0 = no time-window violation has occurred.<br>1 = a time-window violation has occurred. The watchdog will generate either a system reset or a non-maskable interrupt to the CPU in this case.<br>Privilege mode [write]:<br>0 = leaves the current value unchanged.<br>1 = clears the bit to 0. This will also clear all other status flags in the RTIWDSTATUS register except for the AWD ST flag. Clearing of the status flags will deassert the non-maskable interrupt generated due to violation of the DWWD. |

**Table 5-3172. RTI\_RTIVDSTATUS Register Field Descriptions (continued)**

| Bit | Field         | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-----|---------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | ENDTIMEVIOL   | R/W  | 0h    | <p>END TIME VIOL: Windowed Watchdog End Time Violation Status. This bit denotes whether the end-time defined by the windowed watchdog configuration has been violated. This bit is effectively a copy of the DWD ST status flag.</p> <p>User and privilege mode [read]:</p> <p>0 = no end-time window violation has occurred.</p> <p>1 = the end-time defined by the windowed watchdog configuration has been violated.</p> <p>Privilege mode [write]:</p> <p>0 = leaves the current value unchanged.</p> <p>1 = clears the bit to 0.</p>                                |
| 3   | STARTTIMEVIOL | R/W  | 0h    | <p>START TIME VIOL: Windowed Watchdog Start Time Violation Status. This bit denotes whether the start-time defined by the windowed watchdog configuration has been violated. This indicates that the WWD was serviced before the service window was opened.</p> <p>User and privilege mode [read]:</p> <p>0 = no start-time window violation has occurred.</p> <p>1 = the start-time defined by the windowed watchdog configuration has been violated.</p> <p>Privilege mode [write]:</p> <p>0 = leaves the current value unchanged.</p> <p>1 = clears the bit to 0.</p> |
| 2   | KEYST         | R/W  | 0h    | <p>KEYST: Watchdog KeyStatus. This bit denotes a reset generated by a wrong key or a wrong key-sequence written to the RTIWDKEY register.</p> <p>User and privilege mode [read]:</p> <p>0 = no wrong key or key-sequence written</p> <p>1 = wrong key or key-sequence written to RTIWDKEY register</p> <p>Privilege mode [write]:</p> <p>0 = leaves the current value unchanged</p> <p>1 = clears the bit to 0</p>                                                                                                                                                       |
| 1   | DWDST         | R/W  | 0h    | <p>DWDST: Digital Watchdog Status. This bit is effectively a copy of the END TIME VIOL status flag and is maintained for compatibility reasons.</p> <p>User and privilege mode [read]:</p> <p>0 = DWD timeout period not expired</p> <p>1 = DWD timeout period has expired</p> <p>Privilege mode [write]:</p> <p>0 = leaves the current value unchanged</p> <p>1 = clears the bit to 0</p>                                                                                                                                                                               |
| 0   | AWDST         | R/W  | 0h    | <p>AWDST: Analog Watchdog Status. User and privilege mode [read]:</p> <p>0 = AWD pin 0 &gt; 1 threshold not exceeded</p> <p>1 = AWD pin 0 &gt; 1 threshold exceeded</p> <p>Privilege mode [write]:</p> <p>0 = leaves the current value unchanged</p> <p>1 = clears the bit to 0</p>                                                                                                                                                                                                                                                                                      |

### 5.22.2.31 RTI\_RTIWDKEY Register

#### 1 RTI\_RTIWDKEY Register (Offset = 9Ch) [reset = 0h]

Watchdog Key correct written key values discharge the external capacitor.

Return to [Summary Table](#)

**Table 5-3173. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 009Ch       |
| RTI1          | 5218 109Ch       |
| RTI2          | 5218 209Ch       |
| RTI3          | 5218 309Ch       |

**Figure 5-1046. RTI\_RTIWDKEY Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED19 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED19 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| WDKEY      |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| WDKEY      |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-3175. RTI\_RTIWDKEY Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED19 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 15:0  | WDKEY      | R/W  | 0h    | WDKEY: Watchdog Key.<br>User and privilege mode reads are indeterminate.<br>Privilege mode [write]:<br>A write of 0xE51A followed by 0xA35C in two separate write operations defines the Key Sequence and discharges the watchdog capacitor. This also causes the upper 12 bits of the DWD down counter to be reloaded with the contents of the DWD preload register and the lower 13 bits to become all 1s. Writing any other value causes a digital watchdog reset, as shown in Table 1-3.<br>Note: Register write access time precaution<br>The user has to take into account that the write to the register takes 3 VCLK cycle. This needs to be considered for the AWD/DWD expiration calculation. |

### 5.22.2.32 RTI\_RTIDWDCNTR Register

#### 1 RTI\_RTIDWDCNTR Register (Offset = A0h) [reset = 0h]

Digital Watchdog Down Counter current value of DWD down counter.

Return to [Summary Table](#)

**Table 5-3176. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 00A0h       |
| RTI1          | 5218 10A0h       |
| RTI2          | 5218 20A0h       |
| RTI3          | 5218 30A0h       |

**Figure 5-1047. RTI\_RTIDWDCNTR Name Register**

|            |    |    |    |    |    |    |         |
|------------|----|----|----|----|----|----|---------|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24      |
| RESERVED20 |    |    |    |    |    |    | DWDCNTR |
| R/W        |    |    |    |    |    |    | R/W     |
| 0h         |    |    |    |    |    |    | 0h      |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16      |
| DWDCNTR    |    |    |    |    |    |    |         |
| R/W        |    |    |    |    |    |    |         |
| 0h         |    |    |    |    |    |    |         |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8       |
| DWDCNTR    |    |    |    |    |    |    |         |
| R/W        |    |    |    |    |    |    |         |
| 0h         |    |    |    |    |    |    |         |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0       |
| DWDCNTR    |    |    |    |    |    |    |         |
| R/W        |    |    |    |    |    |    |         |
| 0h         |    |    |    |    |    |    |         |

**Table 5-3178. RTI\_RTIDWDCNTR Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:25 | RESERVED20 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                                                                                   |
| 24:0  | DWDCNTR    | R/W  | 0h    | DWDCNTR: Digital Watchdog Down Counter.<br>The value of the DWDCNTR after a system reset is 0x002D_FFFF.<br>When the DWD is enabled and the DWD counter starts counting down from this value with an RTICLK1 time base of 3MHz, a watchdog reset will be generated in 1 second.<br>User and privilege mode [read]:<br>Reads return the current counter value.<br>Privilege mode [write]:<br>Writes dont have an effect. |

### 5.22.2.33 RTI\_RTIWWDRXNCTRL Register

#### 1 RTI\_RTIWWDRXNCTRL Register (Offset = A4h) [reset = 0h]

Windowed Watchdog Reaction Control configures the windowed watchdog to either generate a non-maskable interrupt to the CPU or to generate a system reset.

Return to [Summary Table](#)

**Table 5-3179. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 00A4h       |
| RTI1          | 5218 10A4h       |
| RTI2          | 5218 20A4h       |
| RTI3          | 5218 30A4h       |

**Figure 5-1048. RTI\_RTIWWDRXNCTRL Name Register**

|            |    |    |    |        |    |    |    |
|------------|----|----|----|--------|----|----|----|
| 31         | 30 | 29 | 28 | 27     | 26 | 25 | 24 |
| RESERVED21 |    |    |    |        |    |    |    |
| R/W        |    |    |    |        |    |    |    |
| 0h         |    |    |    |        |    |    |    |
| 23         | 22 | 21 | 20 | 19     | 18 | 17 | 16 |
| RESERVED21 |    |    |    |        |    |    |    |
| R/W        |    |    |    |        |    |    |    |
| 0h         |    |    |    |        |    |    |    |
| 15         | 14 | 13 | 12 | 11     | 10 | 9  | 8  |
| RESERVED21 |    |    |    |        |    |    |    |
| R/W        |    |    |    |        |    |    |    |
| 0h         |    |    |    |        |    |    |    |
| 7          | 6  | 5  | 4  | 3      | 2  | 1  | 0  |
| RESERVED21 |    |    |    | WWDRXN |    |    |    |
| R/W        |    |    |    | R/W    |    |    |    |
| 0h         |    |    |    | 0h     |    |    |    |

**Table 5-3181. RTI\_RTIWWDRXNCTRL Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                           |
|------|------------|------|-------|-------------------------------------------------------|
| 31:4 | RESERVED21 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect |



**Table 5-3181. RTI\_RTIIWDRXNCTRL Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|--------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0 | WWDRXN | R/W  | 0h    | <p>WWDRXN: Digital Windowed Watchdog Reaction.</p> <p>User and privilege mode [read], privileged mode [write]:</p> <p>0x5 = This is the default value. The windowed watchdog will cause a reset if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all.</p> <p>0xA = The windowed watchdog will generate a non-maskable interrupt to the CPU if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all.</p> <p>Writing any other value will cause a system reset if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all.</p> <p>Note: Configuration of DWWD Reaction</p> <p>The DWWD reaction can be selected by the application even when the DWWD counter is already enabled.</p> <p>If a change to the WWDRXN is made before the watchdog service window is opened, then the change in the configuration takes effect immediately.</p> <p>If a change to the WWDRXN is made when the watchdog service window is already open, then the change in configuration takes effect only after the watchdog is serviced.</p> |

### 5.22.2.34 RTI\_RTIWWDSizeCTRL Register

#### 1 RTI\_RTIWWDSizeCTRL Register (Offset = A8h) [reset = 0h]

Windowed Watchdog Size Control configures the size of the window for the digital windowed watchdog.

Return to [Summary Table](#)

**Table 5-3182. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 00A8h       |
| RTI1          | 5218 10A8h       |
| RTI2          | 5218 20A8h       |
| RTI3          | 5218 30A8h       |

**Figure 5-1049. RTI\_RTIWWDSizeCTRL Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| WWDSIZE |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| WWDSIZE |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| WWDSIZE |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| WWDSIZE |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-3184. RTI\_RTIIWWDSizeCTRL Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------|---------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | WWDSIZE | R/W  | 0h    | <p>WWDSIZE: Digital Windowed Watchdog Window Size. User and privilege mode [read], privileged mode [write]: Value written to WWDSIZE Window Size</p> <p>0x00000005 100% [Functionality same as the time-out digital watchdog.]</p> <p>0x00000050 50%</p> <p>0x00000500 25%</p> <p>0x00005000 12.5%</p> <p>0x00050000 6.25%</p> <p>0x00500000 3.125%</p> <p>Any other value 3.125%</p> <p>Note: Incorrect value being written to watchdog window size control register</p> <p>If an incorrect value is written to the WWDSIZE field, or if a system disturbance causes the WWDSIZE field to have a value other than 0x5, 0x50, 0x500, 0x5000, 0x50000, or 0x500000, then the window size will be configured to be 3.125%. This increases the chances of getting a reset due to the windowed watchdog, which enables the system to handle the cause for the incorrect configuration.</p> <p>Note: Configuration of DWWD Window Size</p> <p>The DWWD window size can be selected by the application even when the DWWD counter is already enabled.</p> <p>If a change to the WWDSIZE is made before the watchdog service window is opened, then the change in the configuration takes effect immediately.</p> <p>If a change to the WWDSIZE is made when the watchdog service window is already open, then the change in configuration takes effect only after the watchdog is serviced.</p> |

### 5.22.2.35 RTI\_RTIINTCLRENABLE Register

#### 1 RTI\_RTIINTCLRENABLE Register (Offset = ACh) [reset = 0h]

RTI Compare Interrupt Clear Enable enable the auto clear functionality for each of the compare interrupts.

Return to [Summary Table](#)

**Table 5-3185. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 00ACh       |
| RTI1          | 5218 10ACh       |
| RTI2          | 5218 20ACh       |
| RTI3          | 5218 30ACh       |

**Figure 5-1050. RTI\_RTIINTCLRENABLE Name Register**

|            |    |    |    |               |    |    |    |
|------------|----|----|----|---------------|----|----|----|
| 31         | 30 | 29 | 28 | 27            | 26 | 25 | 24 |
| RESERVED25 |    |    |    | INTCLRENABLE3 |    |    |    |
| R/W        |    |    |    | R/W           |    |    |    |
| 0h         |    |    |    | 0h            |    |    |    |
| 23         | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
| RESERVED24 |    |    |    | INTCLRENABLE2 |    |    |    |
| R/W        |    |    |    | R/W           |    |    |    |
| 0h         |    |    |    | 0h            |    |    |    |
| 15         | 14 | 13 | 12 | 11            | 10 | 9  | 8  |
| RESERVED23 |    |    |    | INTCLRENABLE1 |    |    |    |
| R/W        |    |    |    | R/W           |    |    |    |
| 0h         |    |    |    | 0h            |    |    |    |
| 7          | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| RESERVED22 |    |    |    | INTCLRENABLE0 |    |    |    |
| R/W        |    |    |    | R/W           |    |    |    |
| 0h         |    |    |    | 0h            |    |    |    |

**Table 5-3187. RTI\_RTIINTCLRENABLE Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|---------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28 | RESERVED25    | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                                                                                                            |
| 27:24 | INTCLRENABLE3 | R/W  | 0h    | INTCLRENABLE3.<br>Enables the auto-clear functionality on the compare 3 interrupt.<br>User and Privileged mode [read]:<br>0x5 = Auto-clear for compare 3 interrupt is disabled.<br>Any other value = Auto-clear for compare 3 interrupt is enabled.<br>Privileged mode [write]:<br>0x5 = Disables the auto-clear functionality on the compare 3 interrupt.<br>Any other value = Enables the auto-clear functionality on the compare 3 interrupt. |
| 23:20 | RESERVED24    | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                                                                                                            |

**Table 5-3187. RTI\_RTINTCLRENABLE Register Field Descriptions (continued)**

| Bit   | Field         | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|---------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19:16 | INTCLRENABLE2 | R/W  | 0h    | INTCLRENABLE2.<br>Enables the auto-clear functionality on the compare 2 interrupt.<br>User and Privileged mode [read]:<br>0x5 = Auto-clear for compare 2 interrupt is disabled.<br>Any other value = Auto-clear for compare 2 interrupt is enabled.<br>Privileged mode [write]:<br>0x5 = Disables the auto-clear functionality on the compare 2 interrupt.<br>Any other value = Enables the auto-clear functionality on the compare 2 interrupt. |
| 15:12 | RESERVED23    | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                                                                                                            |
| 11:8  | INTCLRENABLE1 | R/W  | 0h    | INTCLRENABLE1.<br>Enables the auto-clear functionality on the compare 1 interrupt.<br>User and Privileged mode [read]:<br>0x5 = Auto-clear for compare 1 interrupt is disabled.<br>Any other value = Auto-clear for compare 1 interrupt is enabled.<br>Privileged mode [write]:<br>0x5 = Disables the auto-clear functionality on the compare 1 interrupt.<br>Any other value = Enables the auto-clear functionality on the compare 1 interrupt. |
| 7:4   | RESERVED22    | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                                                                                                            |
| 3:0   | INTCLRENABLE0 | R/W  | 0h    | INTCLRENABLE0.<br>Enables the auto-clear functionality on the compare 0 interrupt.<br>User and Privileged mode [read]:<br>0x5 = Auto-clear for compare 0 interrupt is disabled.<br>Any other value = Auto-clear for compare 0 interrupt is enabled.<br>Privileged mode [write]:<br>0x5 = Disables the auto-clear functionality on the compare 0 interrupt.<br>Any other value = Enables the auto-clear functionality on the compare 0 interrupt. |

### 5.22.2.36 RTI\_RTICOMP0CLR Register

#### 1 RTI\_RTICOMP0CLR Register (Offset = B0h) [reset = 0h]

Compare 0 Clear compare value to be compared with the counter to clear the compare0 interrupt line.

Return to [Summary Table](#)

**Table 5-3188. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 00B0h       |
| RTI1          | 5218 10B0h       |
| RTI2          | 5218 20B0h       |
| RTI3          | 5218 30B0h       |

**Figure 5-1051. RTI\_RTICOMP0CLR Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COMP0CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COMP0CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COMP0CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COMP0CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-3190. RTI\_RTICOMP0CLR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | COMP0CLR | R/W  | 0h    | <p>COMP0CLR: Compare 0 Clear.</p> <p>This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the compare 0 interrupt or DMA request line is cleared.</p> <p>User and privilege mode [read]:<br/>current compare value</p> <p>Privilege mode [write]:<br/>update of the compare register with a new compare value</p> <p>Note: Reset behavior<br/>A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.</p> |

### 5.22.2.37 RTI\_RTICOMP1CLR Register

#### 1 RTI\_RTICOMP1CLR Register (Offset = B4h) [reset = 0h]

Compare 1 Clear compare value to be compared with the counter to clear the compare1 interrupt line.

Return to [Summary Table](#)

**Table 5-3191. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 00B4h       |
| RTI1          | 5218 10B4h       |
| RTI2          | 5218 20B4h       |
| RTI3          | 5218 30B4h       |

**Figure 5-1052. RTI\_RTICOMP1CLR Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COMP1CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COMP1CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COMP1CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COMP1CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-3193. RTI\_RTICOMP1CLR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | COMP1CLR | R/W  | 0h    | <p>COMP1CLR: Compare 1 Clear.</p> <p>This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the Compare 1 interrupt or DMA request line is cleared.</p> <p>User and privilege mode [read]:<br/>current compare value</p> <p>Privilege mode [write]:<br/>update of the compare register with a new compare value</p> <p>Note: Reset behavior<br/>A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.</p> |

### 5.22.2.38 RTI\_RTICOMP2CLR Register

#### 1 RTI\_RTICOMP2CLR Register (Offset = B8h) [reset = 0h]

Compare 2 Clear compare value to be compared with the counter to clear the compare2 interrupt line.

Return to [Summary Table](#)

**Table 5-3194. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 00B8h       |
| RTI1          | 5218 10B8h       |
| RTI2          | 5218 20B8h       |
| RTI3          | 5218 30B8h       |

**Figure 5-1053. RTI\_RTICOMP2CLR Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COMP2CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COMP2CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COMP2CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COMP2CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-3196. RTI\_RTICOMP2CLR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | COMP2CLR | R/W  | 0h    | <p>COMP2CLR: Compare 2 Clear.</p> <p>This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the Compare 2 interrupt or DMA request line is cleared.</p> <p>User and privilege mode [read]:<br/>current compare value</p> <p>Privilege mode [write]:<br/>update of the compare register with a new compare value</p> <p>Note: Reset behavior<br/>A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.</p> |



### 5.22.2.39 RTI\_RTICOMP3CLR Register

#### 1 RTI\_RTICOMP3CLR Register (Offset = BCh) [reset = 0h]

Compare 3 Clear compare value to be compared with the counter to clear the compare3 interrupt line.

Return to [Summary Table](#)

**Table 5-3197. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| RTI0          | 5218 00BCh       |
| RTI1          | 5218 10BCh       |
| RTI2          | 5218 20BCh       |
| RTI3          | 5218 30BCh       |

**Figure 5-1054. RTI\_RTICOMP3CLR Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COMP3CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COMP3CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COMP3CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COMP3CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-3199. RTI\_RTICOMP3CLR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | COMP3CLR | R/W  | 0h    | <p>COMP3CLR: Compare 3 Clear.</p> <p>This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the Compare 3 interrupt or DMA request line is cleared.</p> <p>User and privilege mode [read]:<br/>current compare value</p> <p>Privilege mode [write]:<br/>update of the compare register with a new compare value</p> <p>Note: Reset behavior<br/>A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.</p> |

## 5.23 SPINLOCK

### SPINLOCK

#### 5.23.1 SPINLOCK Summaries

#### SPINLOCK Summaries

**Table 5-3200. SPINLOCK Registers, Base Address=50E0 0000h, Length=32768**

| Offset | Length | Register Name                       | SPINLOCK0 Physical Address |
|--------|--------|-------------------------------------|----------------------------|
| 0h     | 32     | <a href="#">SPINLOCK_REVISION</a>   | 50E0 0000h                 |
| 10h    | 32     | <a href="#">SPINLOCK_SYSCONFIG</a>  | 50E0 0010h                 |
| 14h    | 32     | <a href="#">SPINLOCK_SYSTATUS</a>   | 50E0 0014h                 |
| 800h   | 32     | <a href="#">SPINLOCK_LOCK_REG_J</a> | 50E0 0800h + formula       |

#### 5.23.2 SPINLOCK Registers

#### SPINLOCK Registers

### 5.23.2.1 SPINLOCK\_REVISION Register

#### 1 SPINLOCK\_REVISION Register (Offset = 0h) [reset = 66FA6900h]

This is the standard TI peripheral ID register that exists at address 0 in the peripheral space.

Return to [Summary Table](#)

**Table 5-3201. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SPINLOCK0     | 50E0 0000h       |

**Figure 5-1055. SPINLOCK\_REVISION Name Register**

|          |    |           |    |          |           |    |    |
|----------|----|-----------|----|----------|-----------|----|----|
| 31       | 30 | 29        | 28 | 27       | 26        | 25 | 24 |
| SCHEME   |    | BU        |    | FUNCTION |           |    |    |
| R        |    | R         |    | R        |           |    |    |
| 1h       |    | 2h        |    | 6FAh     |           |    |    |
| 23       | 22 | 21        | 20 | 19       | 18        | 17 | 16 |
| FUNCTION |    |           |    |          |           |    |    |
| R        |    |           |    |          |           |    |    |
| 6FAh     |    |           |    |          |           |    |    |
| 15       | 14 | 13        | 12 | 11       | 10        | 9  | 8  |
| RTL_VER  |    |           |    |          | MAJOR_REV |    |    |
| R        |    |           |    |          | R         |    |    |
| Dh       |    |           |    |          | 1h        |    |    |
| 7        | 6  | 5         | 4  | 3        | 2         | 1  | 0  |
| CUSTOM   |    | MINOR_REV |    |          |           |    |    |
| R        |    | R         |    |          |           |    |    |
| 0h       |    | 0h        |    |          |           |    |    |

**Table 5-3203. SPINLOCK\_REVISION Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                            |
|-------|-----------|------|-------|--------------------------------------------------------|
| 31:30 | SCHEME    | R    | 1h    | Used to distinguish which ID numbering scheme is used. |
| 29:28 | BU        | R    | 2h    | BU identifier                                          |
| 27:16 | FUNCTION  | R    | 6FAh  | Module family.                                         |
| 15:11 | RTL_VER   | R    | Dh    | RTL version. R of X.Y.R.Z                              |
| 10:8  | MAJOR_REV | R    | 1h    | Major revision. X of X.Y.R.Z                           |
| 7:6   | CUSTOM    | R    | 0h    | Special version number                                 |
| 5:0   | MINOR_REV | R    | 0h    | Minor revision. Y of X.Y.R.Z                           |

### 5.23.2.2 SPINLOCK\_SYSCONFIG Register

#### 1 SPINLOCK\_SYSCONFIG Register (Offset = 10h) [reset = 0h]

Provides the SOFTRESET register for backwards compatibility with OMAP Spinlock.

Return to [Summary Table](#)

**Table 5-3204. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SPINLOCK0     | 50E0 0010h       |

**Figure 5-1056. SPINLOCK\_SYSCONFIG Name Register**

|          |    |    |    |    |    |            |          |
|----------|----|----|----|----|----|------------|----------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25         | 24       |
| RESERVED |    |    |    |    |    |            |          |
| NONE     |    |    |    |    |    |            |          |
| 0h       |    |    |    |    |    |            |          |
| 23       | 22 | 21 | 20 | 19 | 18 | 17         | 16       |
| RESERVED |    |    |    |    |    |            |          |
| NONE     |    |    |    |    |    |            |          |
| 0h       |    |    |    |    |    |            |          |
| 15       | 14 | 13 | 12 | 11 | 10 | 9          | 8        |
| RESERVED |    |    |    |    |    |            |          |
| NONE     |    |    |    |    |    |            |          |
| 0h       |    |    |    |    |    |            |          |
| 7        | 6  | 5  | 4  | 3  | 2  | 1          | 0        |
| RESERVED |    |    |    |    |    | SOFT_RESET | RESERVED |
| NONE     |    |    |    |    |    | R/W        | NONE     |
| 0h       |    |    |    |    |    | 0h         | 0h       |

**Table 5-3206. SPINLOCK\_SYSCONFIG Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                     |
|------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                        |
| 1    | SOFT_RESET | R/W  | 0h    | Module Software Reset<br>The bit is automatically reset by the hardware. During reads, it always returns 0<br>It has the same effect as the hardware reset<br>Writing a 0 has no effect. Writing a 1 will start a soft reset sequence and free all of the locks |
| 0    | RESERVED   | NONE | 0h    | Reserved                                                                                                                                                                                                                                                        |

### 5.23.2.3 SPINLOCK\_SYSTATUS Register

#### 1 SPINLOCK\_SYSTATUS Register (Offset = 14h) [reset = 8000000h]

Provides information about the Spinlock module.

Return to [Summary Table](#)

**Table 5-3207. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| SPINLOCK0     | 50E0 0014h       |

**Figure 5-1057. SPINLOCK\_SYSTATUS Name Register**

|           |         |         |         |         |         |         |         |
|-----------|---------|---------|---------|---------|---------|---------|---------|
| 31        | 30      | 29      | 28      | 27      | 26      | 25      | 24      |
| NUM_LOCKS |         |         |         |         |         |         |         |
| R         |         |         |         |         |         |         |         |
| 8h        |         |         |         |         |         |         |         |
| 23        | 22      | 21      | 20      | 19      | 18      | 17      | 16      |
| RESERVED  |         |         |         |         |         |         |         |
| NONE      |         |         |         |         |         |         |         |
| 0h        |         |         |         |         |         |         |         |
| 15        | 14      | 13      | 12      | 11      | 10      | 9       | 8       |
| RESERVED  |         |         |         |         |         |         |         |
| NONE      |         |         |         |         |         |         |         |
| 0h        |         |         |         |         |         |         |         |
| 7         | 6       | 5       | 4       | 3       | 2       | 1       | 0       |
| IN_USE7   | IN_USE6 | IN_USE5 | IN_USE4 | IN_USE3 | IN_USE2 | IN_USE1 | IN_USE0 |
| R         | R       | R       | R       | R       | R       | R       | R       |
| 0h        | 0h      | 0h      | 0h      | 0h      | 0h      | 0h      | 0h      |

**Table 5-3209. SPINLOCK\_SYSTATUS Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                        |
|-------|-----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:24 | NUM_LOCKS | R    | 8h    | Module configuration parameter n, the total number of spinlocks divided by 32.<br>e.g. For 256 spin locks, this will return the number 0x08                                                                                                                                                        |
| 23:8  | RESERVED  | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                           |
| 7     | IN_USE7   | R    | 0h    | In-Use flag 7 covering lock registers 224 - 255.<br>If no lock registers are implemented in this range, then this flag always reads as 0<br>Read<br>0 : All lock registers 224 - 255 are in the Not Taken state<br>Read<br>1 : At least one of the lock registers 224 - 255 are in the Taken state |
| 6     | IN_USE6   | R    | 0h    | In-Use flag 6 covering lock registers 192 - 223.<br>If no lock registers are implemented in this range, then this flag always reads as 0<br>Read<br>0 : All lock registers 192 - 223 are in the Not Taken state<br>Read<br>1 : At least one of the lock registers 192 - 223 are in the Taken state |

**Table 5-3209. SPINLOCK\_SYSTATUS Register Field Descriptions (continued)**

| Bit | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                        |
|-----|---------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | IN_USE5 | R    | 0h    | In-Use flag 5 covering lock registers 160 - 191.<br>If no lock registers are implemented in this range, then this flag always reads as 0<br>Read<br>0 : All lock registers 160 - 191 are in the Not Taken state<br>Read<br>1 : At least one of the lock registers 160 - 191 are in the Taken state |
| 4   | IN_USE4 | R    | 0h    | In-Use flag 4 covering lock registers 128 - 159.<br>If no lock registers are implemented in this range, then this flag always reads as 0<br>Read<br>0 : All lock registers 128 - 159 are in the Not Taken state<br>Read<br>1 : At least one of the lock registers 128 - 159 are in the Taken state |
| 3   | IN_USE3 | R    | 0h    | In-Use flag 3 covering lock registers 96 - 127.<br>If no lock registers are implemented in this range, then this flag always reads as 0<br>Read<br>0 : All lock registers 96 - 127 are in the Not Taken state<br>Read<br>1 : At least one of the lock registers 96 - 127 are in the Taken state    |
| 2   | IN_USE2 | R    | 0h    | In-Use flag 2 covering lock registers 64 - 95.<br>If no lock registers are implemented in this range, then this flag always reads as 0<br>Read<br>0 : All lock registers 64 - 95 are in the Not Taken state<br>Read<br>1 : At least one of the lock registers 64 - 95 are in the Taken state       |
| 1   | IN_USE1 | R    | 0h    | In-Use flag 1 covering lock registers 32 - 63.<br>If no lock registers are implemented in this range, then this flag always reads as 0<br>Read<br>0 : All lock registers 32 - 63 are in the Not Taken state<br>Read<br>1 : At least one of the lock registers 32 - 63 are in the Taken state       |
| 0   | IN_USE0 | R    | 0h    | In-Use flag 0 covering lock registers 0 - 31.<br>If no lock registers are implemented in this range, then this flag always reads as 0<br>Read<br>0 : All lock registers 0 - 31 are in the Not Taken state<br>Read<br>1 : At least one of the lock registers 0 - 31 are in the Taken state          |

### 5.23.2.4 SPINLOCK\_LOCK\_REG\_j Register

#### 1 SPINLOCK\_LOCK\_REG\_j Register (Offset = 800h + formula) [reset = 0h]

The Lock[a] register is read and written to perform lock and unlock operations on lock 'a'.

Return to [Summary Table](#)

Offset = (j \* 4h); where j = 0 to 255d

**Table 5-3210. Instance Table**

| Instance Name | Physical Address     |
|---------------|----------------------|
| SPINLOCK0     | 50E0 0800h + formula |

**Figure 5-1058. SPINLOCK\_LOCK\_REG\_j Name Register**

|          |    |    |    |    |    |    |       |
|----------|----|----|----|----|----|----|-------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24    |
| RESERVED |    |    |    |    |    |    |       |
| NONE     |    |    |    |    |    |    |       |
| 0h       |    |    |    |    |    |    |       |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16    |
| RESERVED |    |    |    |    |    |    |       |
| NONE     |    |    |    |    |    |    |       |
| 0h       |    |    |    |    |    |    |       |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8     |
| RESERVED |    |    |    |    |    |    |       |
| NONE     |    |    |    |    |    |    |       |
| 0h       |    |    |    |    |    |    |       |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0     |
| RESERVED |    |    |    |    |    |    | TAKEN |
| NONE     |    |    |    |    |    |    | R/W   |
| 0h       |    |    |    |    |    |    | 0h    |

**Table 5-3212. SPINLOCK\_LOCK\_REG\_j Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                         |
|------|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:1 | RESERVED | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                            |
| 0    | TAKEN    | R/W  | 0h    | Lock Status<br>Read<br>0 : Lock was previously free. The reader now has been granted the lock.<br>Read<br>1 : Lock was previously taken. The reader has not been granted the lock and must retry.<br>Write<br>0 : Free the lock by setting TAKEN to zero.<br>Write<br>1 : No effect |

## 5.24 UART

### UART

#### 5.24.1 UART Summaries

#### UART Summaries

**Table 5-3213. UART Registers, Base Address=5230 0000h, Length=512**

| Offset | Length | Register Name                   | UART0 Physical Address | UART1 Physical Address | UART2 Physical Address |
|--------|--------|---------------------------------|------------------------|------------------------|------------------------|
| 0h     | 32     | <a href="#">UART_DLL</a>        | 5230 0000h             | 5230 1000h             | 5230 2000h             |
| 0h     | 32     | <a href="#">UART_RHR</a>        | 5230 0000h             | 5230 1000h             | 5230 2000h             |
| 0h     | 32     | <a href="#">UART_THR</a>        | 5230 0000h             | 5230 1000h             | 5230 2000h             |
| 4h     | 32     | <a href="#">UART_DLH</a>        | 5230 0004h             | 5230 1004h             | 5230 2004h             |
| 4h     | 32     | <a href="#">UART_IER_CIR</a>    | 5230 0004h             | 5230 1004h             | 5230 2004h             |
| 4h     | 32     | <a href="#">UART_IER_IRDA</a>   | 5230 0004h             | 5230 1004h             | 5230 2004h             |
| 4h     | 32     | <a href="#">UART_IER_UART</a>   | 5230 0004h             | 5230 1004h             | 5230 2004h             |
| 8h     | 32     | <a href="#">UART_EFR</a>        | 5230 0008h             | 5230 1008h             | 5230 2008h             |
| 8h     | 32     | <a href="#">UART_FCR</a>        | 5230 0008h             | 5230 1008h             | 5230 2008h             |
| 8h     | 32     | <a href="#">UART_IIR_CIR</a>    | 5230 0008h             | 5230 1008h             | 5230 2008h             |
| 8h     | 32     | <a href="#">UART_IIR_IRDA</a>   | 5230 0008h             | 5230 1008h             | 5230 2008h             |
| 8h     | 32     | <a href="#">UART_IIR_UART</a>   | 5230 0008h             | 5230 1008h             | 5230 2008h             |
| Ch     | 32     | <a href="#">UART_LCR</a>        | 5230 000Ch             | 5230 100Ch             | 5230 200Ch             |
| 10h    | 32     | <a href="#">UART_MCR</a>        | 5230 0010h             | 5230 1010h             | 5230 2010h             |
| 10h    | 32     | <a href="#">UART_XON1_ADDR1</a> | 5230 0010h             | 5230 1010h             | 5230 2010h             |
| 14h    | 32     | <a href="#">UART_LSR_CIR</a>    | 5230 0014h             | 5230 1014h             | 5230 2014h             |
| 14h    | 32     | <a href="#">UART_LSR_IRDA</a>   | 5230 0014h             | 5230 1014h             | 5230 2014h             |
| 14h    | 32     | <a href="#">UART_LSR_UART</a>   | 5230 0014h             | 5230 1014h             | 5230 2014h             |
| 14h    | 32     | <a href="#">UART_XON2_ADDR2</a> | 5230 0014h             | 5230 1014h             | 5230 2014h             |
| 18h    | 32     | <a href="#">UART_MSR</a>        | 5230 0018h             | 5230 1018h             | 5230 2018h             |
| 18h    | 32     | <a href="#">UART_TCR</a>        | 5230 0018h             | 5230 1018h             | 5230 2018h             |
| 18h    | 32     | <a href="#">UART_XOFF1</a>      | 5230 0018h             | 5230 1018h             | 5230 2018h             |
| 1Ch    | 32     | <a href="#">UART_SPR</a>        | 5230 001Ch             | 5230 101Ch             | 5230 201Ch             |
| 1Ch    | 32     | <a href="#">UART_TLR</a>        | 5230 001Ch             | 5230 101Ch             | 5230 201Ch             |
| 1Ch    | 32     | <a href="#">UART_XOFF2</a>      | 5230 001Ch             | 5230 101Ch             | 5230 201Ch             |
| 20h    | 32     | <a href="#">UART_MDR1</a>       | 5230 0020h             | 5230 1020h             | 5230 2020h             |
| 24h    | 32     | <a href="#">UART_MDR2</a>       | 5230 0024h             | 5230 1024h             | 5230 2024h             |
| 28h    | 32     | <a href="#">UART_SFLSR</a>      | 5230 0028h             | 5230 1028h             | 5230 2028h             |
| 28h    | 32     | <a href="#">UART_TXFLL</a>      | 5230 0028h             | 5230 1028h             | 5230 2028h             |
| 2Ch    | 32     | <a href="#">UART_RESUME</a>     | 5230 002Ch             | 5230 102Ch             | 5230 202Ch             |
| 2Ch    | 32     | <a href="#">UART_TXFLH</a>      | 5230 002Ch             | 5230 102Ch             | 5230 202Ch             |
| 30h    | 32     | <a href="#">UART_RXFLL</a>      | 5230 0030h             | 5230 1030h             | 5230 2030h             |
| 30h    | 32     | <a href="#">UART_SFREGL</a>     | 5230 0030h             | 5230 1030h             | 5230 2030h             |
| 34h    | 32     | <a href="#">UART_RXFLH</a>      | 5230 0034h             | 5230 1034h             | 5230 2034h             |
| 34h    | 32     | <a href="#">UART_SFREGH</a>     | 5230 0034h             | 5230 1034h             | 5230 2034h             |
| 38h    | 32     | <a href="#">UART_BLR</a>        | 5230 0038h             | 5230 1038h             | 5230 2038h             |
| 38h    | 32     | <a href="#">UART_UASR</a>       | 5230 0038h             | 5230 1038h             | 5230 2038h             |



**Table 5-3213. UART Registers, Base Address=5230 0000h, Length=512 (continued)**

| Offset | Length | Register Name                         | UART0 Physical Address | UART1 Physical Address | UART2 Physical Address |
|--------|--------|---------------------------------------|------------------------|------------------------|------------------------|
| 3Ch    | 32     | <a href="#">UART_ACREG</a>            | 5230 003Ch             | 5230 103Ch             | 5230 203Ch             |
| 40h    | 32     | <a href="#">UART_SCR</a>              | 5230 0040h             | 5230 1040h             | 5230 2040h             |
| 44h    | 32     | <a href="#">UART_SSR</a>              | 5230 0044h             | 5230 1044h             | 5230 2044h             |
| 48h    | 32     | <a href="#">UART_EBLR</a>             | 5230 0048h             | 5230 1048h             | 5230 2048h             |
| 50h    | 32     | <a href="#">UART_MVR</a>              | 5230 0050h             | 5230 1050h             | 5230 2050h             |
| 58h    | 32     | <a href="#">UART_SYSS</a>             | 5230 0058h             | 5230 1058h             | 5230 2058h             |
| 5Ch    | 32     | <a href="#">UART_WER</a>              | 5230 005Ch             | 5230 105Ch             | 5230 205Ch             |
| 60h    | 32     | <a href="#">UART_CFPS</a>             | 5230 0060h             | 5230 1060h             | 5230 2060h             |
| 64h    | 32     | <a href="#">UART_RXFIFO_LVL</a>       | 5230 0064h             | 5230 1064h             | 5230 2064h             |
| 68h    | 32     | <a href="#">UART_TXFIFO_LVL</a>       | 5230 0068h             | 5230 1068h             | 5230 2068h             |
| 6Ch    | 32     | <a href="#">UART_IER2</a>             | 5230 006Ch             | 5230 106Ch             | 5230 206Ch             |
| 70h    | 32     | <a href="#">UART_ISR2</a>             | 5230 0070h             | 5230 1070h             | 5230 2070h             |
| 74h    | 32     | <a href="#">UART_FREQ_SEL</a>         | 5230 0074h             | 5230 1074h             | 5230 2074h             |
| 78h    | 32     | <a href="#">UART_ABAUD_1ST_CHAR</a>   | 5230 0078h             | 5230 1078h             | 5230 2078h             |
| 7Ch    | 32     | <a href="#">UART_BAUD_2ND_CHAR</a>    | 5230 007Ch             | 5230 107Ch             | 5230 207Ch             |
| 80h    | 32     | <a href="#">UART_MDR3</a>             | 5230 0080h             | 5230 1080h             | 5230 2080h             |
| 84h    | 32     | <a href="#">UART_TX_DMA_THRESHOLD</a> | 5230 0084h             | 5230 1084h             | 5230 2084h             |
| 88h    | 32     | <a href="#">UART_MDR4</a>             | 5230 0088h             | 5230 1088h             | 5230 2088h             |
| 8Ch    | 32     | <a href="#">UART_EFR2</a>             | 5230 008Ch             | 5230 108Ch             | 5230 208Ch             |
| 90h    | 32     | <a href="#">UART_ECR</a>              | 5230 0090h             | 5230 1090h             | 5230 2090h             |
| 94h    | 32     | <a href="#">UART_TIMEGUARD</a>        | 5230 0094h             | 5230 1094h             | 5230 2094h             |
| 98h    | 32     | <a href="#">UART_TIMEOUTL</a>         | 5230 0098h             | 5230 1098h             | 5230 2098h             |
| 9Ch    | 32     | <a href="#">UART_TIMEOUTH</a>         | 5230 009Ch             | 5230 109Ch             | 5230 209Ch             |
| A0h    | 32     | <a href="#">UART_SCCR</a>             | 5230 00A0h             | 5230 10A0h             | 5230 20A0h             |
| A4h    | 32     | <a href="#">UART_ERHR</a>             | 5230 00A4h             | 5230 10A4h             | 5230 20A4h             |
| A4h    | 32     | <a href="#">UART_ETHR</a>             | 5230 00A4h             | 5230 10A4h             | 5230 20A4h             |
| A8h    | 32     | <a href="#">UART_MAR</a>              | 5230 00A8h             | 5230 10A8h             | 5230 20A8h             |
| ACh    | 32     | <a href="#">UART_MMR</a>              | 5230 00ACh             | 5230 10ACh             | 5230 20ACh             |
| B0h    | 32     | <a href="#">UART_MBR</a>              | 5230 00B0h             | 5230 10B0h             | 5230 20B0h             |

**Table 5-3214. UART Registers, Base Address=5230 0000h, Length=512**

| Offset | Length | Register Name                 | UART3 Physical Address | UART4 Physical Address | UART5 Physical Address |
|--------|--------|-------------------------------|------------------------|------------------------|------------------------|
| 0h     | 32     | <a href="#">UART_DLL</a>      | 5230 3000h             | 5230 4000h             | 5230 5000h             |
| 0h     | 32     | <a href="#">UART_RHR</a>      | 5230 3000h             | 5230 4000h             | 5230 5000h             |
| 0h     | 32     | <a href="#">UART_THR</a>      | 5230 3000h             | 5230 4000h             | 5230 5000h             |
| 4h     | 32     | <a href="#">UART_DLH</a>      | 5230 3004h             | 5230 4004h             | 5230 5004h             |
| 4h     | 32     | <a href="#">UART_IER_CIR</a>  | 5230 3004h             | 5230 4004h             | 5230 5004h             |
| 4h     | 32     | <a href="#">UART_IER_IRDA</a> | 5230 3004h             | 5230 4004h             | 5230 5004h             |
| 4h     | 32     | <a href="#">UART_IER_UART</a> | 5230 3004h             | 5230 4004h             | 5230 5004h             |
| 8h     | 32     | <a href="#">UART_EFR</a>      | 5230 3008h             | 5230 4008h             | 5230 5008h             |
| 8h     | 32     | <a href="#">UART_FCR</a>      | 5230 3008h             | 5230 4008h             | 5230 5008h             |
| 8h     | 32     | <a href="#">UART_IIR_CIR</a>  | 5230 3008h             | 5230 4008h             | 5230 5008h             |
| 8h     | 32     | <a href="#">UART_IIR_IRDA</a> | 5230 3008h             | 5230 4008h             | 5230 5008h             |

**Table 5-3214. UART Registers, Base Address=5230 0000h, Length=512 (continued)**

| Offset | Length | Register Name                         | UART3 Physical Address | UART4 Physical Address | UART5 Physical Address |
|--------|--------|---------------------------------------|------------------------|------------------------|------------------------|
| 8h     | 32     | <a href="#">UART_IIR_UART</a>         | 5230 3008h             | 5230 4008h             | 5230 5008h             |
| Ch     | 32     | <a href="#">UART_LCR</a>              | 5230 300Ch             | 5230 400Ch             | 5230 500Ch             |
| 10h    | 32     | <a href="#">UART_MCR</a>              | 5230 3010h             | 5230 4010h             | 5230 5010h             |
| 10h    | 32     | <a href="#">UART_XON1_ADDR1</a>       | 5230 3010h             | 5230 4010h             | 5230 5010h             |
| 14h    | 32     | <a href="#">UART_LSR_CIR</a>          | 5230 3014h             | 5230 4014h             | 5230 5014h             |
| 14h    | 32     | <a href="#">UART_LSR_IRDA</a>         | 5230 3014h             | 5230 4014h             | 5230 5014h             |
| 14h    | 32     | <a href="#">UART_LSR_UART</a>         | 5230 3014h             | 5230 4014h             | 5230 5014h             |
| 14h    | 32     | <a href="#">UART_XON2_ADDR2</a>       | 5230 3014h             | 5230 4014h             | 5230 5014h             |
| 18h    | 32     | <a href="#">UART_MSR</a>              | 5230 3018h             | 5230 4018h             | 5230 5018h             |
| 18h    | 32     | <a href="#">UART_TCR</a>              | 5230 3018h             | 5230 4018h             | 5230 5018h             |
| 18h    | 32     | <a href="#">UART_XOFF1</a>            | 5230 3018h             | 5230 4018h             | 5230 5018h             |
| 1Ch    | 32     | <a href="#">UART_SPR</a>              | 5230 301Ch             | 5230 401Ch             | 5230 501Ch             |
| 1Ch    | 32     | <a href="#">UART_TLR</a>              | 5230 301Ch             | 5230 401Ch             | 5230 501Ch             |
| 1Ch    | 32     | <a href="#">UART_XOFF2</a>            | 5230 301Ch             | 5230 401Ch             | 5230 501Ch             |
| 20h    | 32     | <a href="#">UART_MDR1</a>             | 5230 3020h             | 5230 4020h             | 5230 5020h             |
| 24h    | 32     | <a href="#">UART_MDR2</a>             | 5230 3024h             | 5230 4024h             | 5230 5024h             |
| 28h    | 32     | <a href="#">UART_SFLSR</a>            | 5230 3028h             | 5230 4028h             | 5230 5028h             |
| 28h    | 32     | <a href="#">UART_TXFLL</a>            | 5230 3028h             | 5230 4028h             | 5230 5028h             |
| 2Ch    | 32     | <a href="#">UART_RESUME</a>           | 5230 302Ch             | 5230 402Ch             | 5230 502Ch             |
| 2Ch    | 32     | <a href="#">UART_TXFLH</a>            | 5230 302Ch             | 5230 402Ch             | 5230 502Ch             |
| 30h    | 32     | <a href="#">UART_RXFLL</a>            | 5230 3030h             | 5230 4030h             | 5230 5030h             |
| 30h    | 32     | <a href="#">UART_SFREGL</a>           | 5230 3030h             | 5230 4030h             | 5230 5030h             |
| 34h    | 32     | <a href="#">UART_RXFLH</a>            | 5230 3034h             | 5230 4034h             | 5230 5034h             |
| 34h    | 32     | <a href="#">UART_SFREGH</a>           | 5230 3034h             | 5230 4034h             | 5230 5034h             |
| 38h    | 32     | <a href="#">UART_BLR</a>              | 5230 3038h             | 5230 4038h             | 5230 5038h             |
| 38h    | 32     | <a href="#">UART_UASR</a>             | 5230 3038h             | 5230 4038h             | 5230 5038h             |
| 3Ch    | 32     | <a href="#">UART_ACREG</a>            | 5230 303Ch             | 5230 403Ch             | 5230 503Ch             |
| 40h    | 32     | <a href="#">UART_SCR</a>              | 5230 3040h             | 5230 4040h             | 5230 5040h             |
| 44h    | 32     | <a href="#">UART_SSR</a>              | 5230 3044h             | 5230 4044h             | 5230 5044h             |
| 48h    | 32     | <a href="#">UART_EBLR</a>             | 5230 3048h             | 5230 4048h             | 5230 5048h             |
| 50h    | 32     | <a href="#">UART_MVR</a>              | 5230 3050h             | 5230 4050h             | 5230 5050h             |
| 58h    | 32     | <a href="#">UART_SYSS</a>             | 5230 3058h             | 5230 4058h             | 5230 5058h             |
| 5Ch    | 32     | <a href="#">UART_WER</a>              | 5230 305Ch             | 5230 405Ch             | 5230 505Ch             |
| 60h    | 32     | <a href="#">UART_CFPS</a>             | 5230 3060h             | 5230 4060h             | 5230 5060h             |
| 64h    | 32     | <a href="#">UART_RXFIFO_LVL</a>       | 5230 3064h             | 5230 4064h             | 5230 5064h             |
| 68h    | 32     | <a href="#">UART_TXFIFO_LVL</a>       | 5230 3068h             | 5230 4068h             | 5230 5068h             |
| 6Ch    | 32     | <a href="#">UART_IER2</a>             | 5230 306Ch             | 5230 406Ch             | 5230 506Ch             |
| 70h    | 32     | <a href="#">UART_ISR2</a>             | 5230 3070h             | 5230 4070h             | 5230 5070h             |
| 74h    | 32     | <a href="#">UART_FREQ_SEL</a>         | 5230 3074h             | 5230 4074h             | 5230 5074h             |
| 78h    | 32     | <a href="#">UART_ABAUD_1ST_CHAR</a>   | 5230 3078h             | 5230 4078h             | 5230 5078h             |
| 7Ch    | 32     | <a href="#">UART_BAUD_2ND_CHAR</a>    | 5230 307Ch             | 5230 407Ch             | 5230 507Ch             |
| 80h    | 32     | <a href="#">UART_MDR3</a>             | 5230 3080h             | 5230 4080h             | 5230 5080h             |
| 84h    | 32     | <a href="#">UART_TX_DMA_THRESHOLD</a> | 5230 3084h             | 5230 4084h             | 5230 5084h             |
| 88h    | 32     | <a href="#">UART_MDR4</a>             | 5230 3088h             | 5230 4088h             | 5230 5088h             |

**Table 5-3214. UART Registers, Base Address=5230 0000h, Length=512 (continued)**

| Offset | Length | Register Name                  | UART3 Physical Address | UART4 Physical Address | UART5 Physical Address |
|--------|--------|--------------------------------|------------------------|------------------------|------------------------|
| 8Ch    | 32     | <a href="#">UART_EFR2</a>      | 5230 308Ch             | 5230 408Ch             | 5230 508Ch             |
| 90h    | 32     | <a href="#">UART_ECR</a>       | 5230 3090h             | 5230 4090h             | 5230 5090h             |
| 94h    | 32     | <a href="#">UART_TIMEGUARD</a> | 5230 3094h             | 5230 4094h             | 5230 5094h             |
| 98h    | 32     | <a href="#">UART_TIMEOUTL</a>  | 5230 3098h             | 5230 4098h             | 5230 5098h             |
| 9Ch    | 32     | <a href="#">UART_TIMEOUTH</a>  | 5230 309Ch             | 5230 409Ch             | 5230 509Ch             |
| A0h    | 32     | <a href="#">UART_SCCR</a>      | 5230 30A0h             | 5230 40A0h             | 5230 50A0h             |
| A4h    | 32     | <a href="#">UART_ERHR</a>      | 5230 30A4h             | 5230 40A4h             | 5230 50A4h             |
| A4h    | 32     | <a href="#">UART_ETHR</a>      | 5230 30A4h             | 5230 40A4h             | 5230 50A4h             |
| A8h    | 32     | <a href="#">UART_MAR</a>       | 5230 30A8h             | 5230 40A8h             | 5230 50A8h             |
| ACh    | 32     | <a href="#">UART_MMR</a>       | 5230 30ACh             | 5230 40ACh             | 5230 50ACh             |
| B0h    | 32     | <a href="#">UART_MBR</a>       | 5230 30B0h             | 5230 40B0h             | 5230 50B0h             |

### 5.24.2 UART Registers

#### UART Registers

### 5.24.2.1 UART\_DLL Register

#### 1 UART\_DLL Register (Offset = 0h) [reset = 0h]

Divisor Latches Low Register.

Return to [Summary Table](#)

**Table 5-3215. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0000h       |
| UART1         | 5230 1000h       |
| UART2         | 5230 2000h       |
| UART3         | 5230 3000h       |
| UART4         | 5230 4000h       |
| UART5         | 5230 5000h       |

**Figure 5-1059. UART\_DLL Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED  |    |    |    |    |    |    |    |
| NONE      |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED  |    |    |    |    |    |    |    |
| NONE      |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED  |    |    |    |    |    |    |    |
| NONE      |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CLOCK_LSB |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 5-3217. UART\_DLL Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                               |
|------|-----------|------|-------|-------------------------------------------|
| 31:8 | RESERVED  | NONE | 0h    | Reserved                                  |
| 7:0  | CLOCK_LSB | R/W  | 0h    | Used to store the 8-bit LSB divisor value |

### 5.24.2.2 UART\_RHR Register

#### 1 UART\_RHR Register (Offset = 0h) [reset = 0h]

The receiver section consists of the receiver holding register (RHR) and the receiver shift register. The RHR is actually a 64-byte FIFO. The receiver shift register receives serial data from RX input. The data is converted to parallel data and moved to the RHR. If the FIFO is disabled location zero of the FIFO is used to store the single data character.

Note: If an overflow occurs the data in the RHR is not overwritten.

Return to [Summary Table](#)

**Table 5-3218. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0000h       |
| UART1         | 5230 1000h       |
| UART2         | 5230 2000h       |
| UART3         | 5230 3000h       |
| UART4         | 5230 4000h       |
| UART5         | 5230 5000h       |

**Figure 5-1060. UART\_RHR Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_24 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_24 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_24 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RHR         |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-3220. UART\_RHR Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description              |
|------|-------------|------|-------|--------------------------|
| 31:8 | RESERVED_24 | R    | 0h    | Reserved                 |
| 7:0  | RHR         | R    | 0h    | Receive holding register |

### 5.24.2.3 UART\_THR Register

#### 1 UART\_THR Register (Offset = 0h) [reset = 0h]

The transmitter section consists of the transmit holding register (THR) and the transmit shift register. The transmit holding register is actually a 64-byte FIFO. The LH writes data to the THR. The data is placed into the transmit shift register where it is shifted out serially on the TX output. If the FIFO is disabled location zero of the FIFO is used to store the data.

Return to [Summary Table](#)

**Table 5-3221. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0000h       |
| UART1         | 5230 1000h       |
| UART2         | 5230 2000h       |
| UART3         | 5230 3000h       |
| UART4         | 5230 4000h       |
| UART5         | 5230 5000h       |

**Figure 5-1061. UART\_THR Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_24 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_24 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_24 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| THR         |    |    |    |    |    |    |    |
| W           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-3223. UART\_THR Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description               |
|------|-------------|------|-------|---------------------------|
| 31:8 | RESERVED_24 | R    | 0h    | Reserved                  |
| 7:0  | THR         | W    | 0h    | TRANSMIT HOLDING REGISTER |

### 5.24.2.4 UART\_DLH Register

#### 1 UART\_DLH Register (Offset = 4h) [reset = 0h]

Divisor Latches High Register.

Return to [Summary Table](#)

**Table 5-3224. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0004h       |
| UART1         | 5230 1004h       |
| UART2         | 5230 2004h       |
| UART3         | 5230 3004h       |
| UART4         | 5230 4004h       |
| UART5         | 5230 5004h       |

**Figure 5-1062. UART\_DLH Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED  |    |    |    |    |    |    |    |
| NONE      |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED  |    |    |    |    |    |    |    |
| NONE      |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED  |    |    |    |    |    |    |    |
| NONE      |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CLOCK_MSB |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 5-3226. UART\_DLH Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                               |
|------|-----------|------|-------|-------------------------------------------|
| 31:8 | RESERVED  | NONE | 0h    | Reserved                                  |
| 7:0  | CLOCK_MSB | R/W  | 0h    | Used to store the 8-bit MSB divisor value |

### 5.24.2.5 UART\_IER\_CIR Register

#### 1 UART\_IER\_CIR Register (Offset = 4h) [reset = 0h]

The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 6 types of interrupt in these modes, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually.

Return to [Summary Table](#)

**Table 5-3227. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0004h       |
| UART1         | 5230 1004h       |
| UART2         | 5230 2004h       |
| UART3         | 5230 3004h       |
| UART4         | 5230 4004h       |
| UART5         | 5230 5004h       |

**Figure 5-1063. UART\_IER\_CIR Name Register**

|           |              |           |               |            |        |        |     |
|-----------|--------------|-----------|---------------|------------|--------|--------|-----|
| 31        | 30           | 29        | 28            | 27         | 26     | 25     | 24  |
| RESERVED  |              |           |               |            |        |        |     |
| NONE      |              |           |               |            |        |        |     |
| 0h        |              |           |               |            |        |        |     |
| 23        | 22           | 21        | 20            | 19         | 18     | 17     | 16  |
| RESERVED  |              |           |               |            |        |        |     |
| NONE      |              |           |               |            |        |        |     |
| 0h        |              |           |               |            |        |        |     |
| 15        | 14           | 13        | 12            | 11         | 10     | 9      | 8   |
| RESERVED  |              |           |               |            |        |        |     |
| NONE      |              |           |               |            |        |        |     |
| 0h        |              |           |               |            |        |        |     |
| 7         | 6            | 5         | 4             | 3          | 2      | 1      | 0   |
| NOT_USED2 | TX_STATUS_IT | NOT_USED1 | RX_OVERRUN_IT | RX_STOP_IT | THR_IT | RHR_IT |     |
| R/W       | R/W          | R/W       | R/W           | R/W        | R/W    | R/W    | R/W |
| 0h        | 0h           | 0h        | 0h            | 0h         | 0h     | 0h     | 0h  |

**Table 5-3229. UART\_IER\_CIR Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                                                     |
|------|---------------|------|-------|---------------------------------------------------------------------------------|
| 31:8 | RESERVED      | NONE | 0h    | Reserved                                                                        |
| 7:6  | NOT_USED2     | R/W  | 0h    |                                                                                 |
| 5    | TX_STATUS_IT  | R/W  | 0h    | 0 Disables the TX status interrupt.<br>1 Enables the TX status interrupt.       |
| 4    | NOT_USED1     | R/W  | 0h    |                                                                                 |
| 3    | RX_OVERRUN_IT | R/W  | 0h    | 0 Disables the RX overrun interrupt.<br>1 Enables the RX overrun interrupt.     |
| 2    | RX_STOP_IT    | R/W  | 0h    | 0 Disables the receive stop interrupt.<br>1 Enables the receive stop interrupt. |



**Table 5-3229. UART\_IER\_CIR Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                   |
|-----|--------|------|-------|---------------------------------------------------------------|
| 1   | THR_IT | R/W  | 0h    | 0 Disables the THR interrupt.<br>1 Enables the THR interrupt. |
| 0   | RHR_IT | R/W  | 0h    | 0 Disables the RHR interrupt.<br>1 Enables the RHR interrupt. |

### 5.24.2.6 UART\_IER\_IRDA Register

#### 1 UART\_IER\_IRDA Register (Offset = 4h) [reset = 0h]

The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are 8 types of interrupt in these modes, received EOF, LSR interrupt, TX status, status FIFO interrupt, RX overrun, last byte in RX FIFO, THR interrupt and RHR interrupt and they can be enabled/disabled individually.

Return to [Summary Table](#)

**Table 5-3230. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0004h       |
| UART1         | 5230 1004h       |
| UART2         | 5230 2004h       |
| UART3         | 5230 3004h       |
| UART4         | 5230 4004h       |
| UART5         | 5230 5004h       |

**Figure 5-1064. UART\_IER\_IRDA Name Register**

|          |             |              |                      |                   |                     |        |        |
|----------|-------------|--------------|----------------------|-------------------|---------------------|--------|--------|
| 31       | 30          | 29           | 28                   | 27                | 26                  | 25     | 24     |
| RESERVED |             |              |                      |                   |                     |        |        |
| NONE     |             |              |                      |                   |                     |        |        |
| 0h       |             |              |                      |                   |                     |        |        |
| 23       | 22          | 21           | 20                   | 19                | 18                  | 17     | 16     |
| RESERVED |             |              |                      |                   |                     |        |        |
| NONE     |             |              |                      |                   |                     |        |        |
| 0h       |             |              |                      |                   |                     |        |        |
| 15       | 14          | 13           | 12                   | 11                | 10                  | 9      | 8      |
| RESERVED |             |              |                      |                   |                     |        |        |
| NONE     |             |              |                      |                   |                     |        |        |
| 0h       |             |              |                      |                   |                     |        |        |
| 7        | 6           | 5            | 4                    | 3                 | 2                   | 1      | 0      |
| EOF_IT   | LINE_STS_IT | TX_STATUS_IT | STS_FIFO_TRI<br>G_IT | RX_OVERRUN<br>_IT | LAST_RX_BYT<br>E_IT | THR_IT | RHR_IT |
| R/W      | R/W         | R/W          | R/W                  | R/W               | R/W                 | R/W    | R/W    |
| 0h       | 0h          | 0h           | 0h                   | 0h                | 0h                  | 0h     | 0h     |

**Table 5-3232. UART\_IER\_IRDA Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                     |
|------|--------------|------|-------|-------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED     | NONE | 0h    | Reserved                                                                                        |
| 7    | EOF_IT       | R/W  | 0h    | 0 Disables the received EOF interrupt.<br>1 Enables the received EOF interrupt.                 |
| 6    | LINE_STS_IT  | R/W  | 0h    | 0 Disables the receiver line status interrupt.<br>1 Enables the receiver line status interrupt. |
| 5    | TX_STATUS_IT | R/W  | 0h    | 0 Disables the TX status interrupt.<br>1 Enables the TX status interrupt.                       |

**Table 5-3232. UART\_IER\_IRDA Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description                                                                                                       |
|-----|------------------|------|-------|-------------------------------------------------------------------------------------------------------------------|
| 4   | STS_FIFO_TRIG_IT | R/W  | 0h    | 0 Disables the status FIFO trigger level interrupt.<br>1 Enables the status FIFO trigger level interrupt.         |
| 3   | RX_OVERRUN_IT    | R/W  | 0h    | 0 Disables the RX overrun interrupt.<br>1 Enables the RX overrun interrupt.                                       |
| 2   | LAST_RX_BYTE_IT  | R/W  | 0h    | 0 Disables the last byte of frame in RX FIFO interrupt.<br>1 Enables the last byte of frame in RX FIFO interrupt. |
| 1   | THR_IT           | R/W  | 0h    | 0 Disables the THR interrupt.<br>1 Enables the THR interrupt.                                                     |
| 0   | RHR_IT           | R/W  | 0h    | 0 Disables the RHR interrupt.<br>1 Enables the RHR interrupt.                                                     |

### 5.24.2.7 UART\_IER\_UART Register

#### 1 UART\_IER\_UART Register (Offset = 4h) [reset = 0h]

The interrupt enable register (IER) can be programmed to enable/disable any interrupt. There are seven types of interrupt in this mode: receiver error, RHR interrupt, THR interrupt, XOFF received and CTS\*/RTS\* change of state from low to high. Each interrupt can be enabled/disabled individually. There is also a sleep mode enable bit.

Return to [Summary Table](#)

**Table 5-3233. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0004h       |
| UART1         | 5230 1004h       |
| UART2         | 5230 2004h       |
| UART3         | 5230 3004h       |
| UART4         | 5230 4004h       |
| UART5         | 5230 5004h       |

**Figure 5-1065. UART\_IER\_UART Name Register**

|          |        |         |            |                  |             |        |        |
|----------|--------|---------|------------|------------------|-------------|--------|--------|
| 31       | 30     | 29      | 28         | 27               | 26          | 25     | 24     |
| RESERVED |        |         |            |                  |             |        |        |
| R        |        |         |            |                  |             |        |        |
| 0h       |        |         |            |                  |             |        |        |
| 23       | 22     | 21      | 20         | 19               | 18          | 17     | 16     |
| RESERVED |        |         |            |                  |             |        |        |
| R        |        |         |            |                  |             |        |        |
| 0h       |        |         |            |                  |             |        |        |
| 15       | 14     | 13      | 12         | 11               | 10          | 9      | 8      |
| RESERVED |        |         |            |                  |             |        |        |
| R        |        |         |            |                  |             |        |        |
| 0h       |        |         |            |                  |             |        |        |
| 7        | 6      | 5       | 4          | 3                | 2           | 1      | 0      |
| CTS_IT   | RTS_IT | XOFF_IT | SLEEP_MODE | MODEM_STS_I<br>T | LINE_STS_IT | THR_IT | RHR_IT |
| R/W      | R/W    | R/W     | R/W        | R/W              | R/W         | R/W    | R/W    |
| 0h       | 0h     | 0h      | 0h         | 0h               | 0h          | 0h     | 0h     |

**Table 5-3235. UART\_IER\_UART Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                      |
|------|------------|------|-------|--------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED   | R    | 0h    |                                                                                                  |
| 7    | CTS_IT     | R/W  | 0h    | 0 Disables the CTS* interrupt<br>1 Enables the CTS* interrupt                                    |
| 6    | RTS_IT     | R/W  | 0h    | 0 Disables the RTS* interrupt<br>1 Enables the RTS* interrupt                                    |
| 5    | XOFF_IT    | R/W  | 0h    | 0 Disables the XOFF interrupt<br>1 Enables the XOFF interrupt                                    |
| 4    | SLEEP_MODE | R/W  | 0h    | 0 Disables sleep mode<br>1 Enables sleep mode (stop baud rate clock when the module is inactive) |

**Table 5-3235. UART\_IER\_UART Register Field Descriptions (continued)**

| Bit | Field        | Type | Reset | Description                                                                                                 |
|-----|--------------|------|-------|-------------------------------------------------------------------------------------------------------------|
| 3   | MODEM_STS_IT | R/W  | 0h    | 0 Disables the modem status register interrupt<br>1 Enables the modem status register interrupt             |
| 2   | LINE_STS_IT  | R/W  | 0h    | 0 Disables the receiver line status interrupt<br>1 Enables the receiver line status interrupt               |
| 1   | THR_IT       | R/W  | 0h    | 0 Disables the THR interrupt<br>1 Enables the THR interrupt                                                 |
| 0   | RHR_IT       | R/W  | 0h    | 0 Disables the RHR interrupt and time out interrupt.<br>1 Enables the RHR interrupt and time out interrupt. |

### 5.24.2.8 UART\_EFR Register

#### 1 UART\_EFR Register (Offset = 8h) [reset = 0h]

Enhanced Feature Register.

Return to [Summary Table](#)

**Table 5-3236. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0008h       |
| UART1         | 5230 1008h       |
| UART2         | 5230 2008h       |
| UART3         | 5230 3008h       |
| UART4         | 5230 4008h       |
| UART5         | 5230 5008h       |

**Figure 5-1066. UART\_EFR Name Register**

|             |             |                          |             |                 |    |    |    |
|-------------|-------------|--------------------------|-------------|-----------------|----|----|----|
| 31          | 30          | 29                       | 28          | 27              | 26 | 25 | 24 |
| RESERVED    |             |                          |             |                 |    |    |    |
| NONE        |             |                          |             |                 |    |    |    |
| 0h          |             |                          |             |                 |    |    |    |
| 23          | 22          | 21                       | 20          | 19              | 18 | 17 | 16 |
| RESERVED    |             |                          |             |                 |    |    |    |
| NONE        |             |                          |             |                 |    |    |    |
| 0h          |             |                          |             |                 |    |    |    |
| 15          | 14          | 13                       | 12          | 11              | 10 | 9  | 8  |
| RESERVED    |             |                          |             |                 |    |    |    |
| NONE        |             |                          |             |                 |    |    |    |
| 0h          |             |                          |             |                 |    |    |    |
| 7           | 6           | 5                        | 4           | 3               | 2  | 1  | 0  |
| AUTO_CTS_EN | AUTO_RTS_EN | SPECIAL_CHARACTER_DETECT | ENHANCED_EN | SW_FLOW_CONTROL |    |    |    |
| R/W         | R/W         | R/W                      | R/W         | R/W             |    |    |    |
| 0h          | 0h          | 0h                       | 0h          | 0h              |    |    |    |

**Table 5-3238. UART\_EFR Register Field Descriptions**

| Bit  | Field                    | Type | Reset | Description                                                                                                                                                                                                                                                                        |
|------|--------------------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED                 | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                           |
| 7    | AUTO_CTS_EN              | R/W  | 0h    | Auto-CTS enable bit.<br>0:Normal operation.<br>1:Auto-CTS flow control is enabled i.e. transmission is halted when the CTS* pin is high (inactive).                                                                                                                                |
| 6    | AUTO_RTS_EN              | R/W  | 0h    | Auto-RTS enable bit.<br>0:Normal operation.<br>1:Auto- RTS flow control is enabled i.e. RTS* pin goes high (inactive) when the receiver FIFO HALT trigger level, TCR[3:0], is reached, and goes low (active) when the receiver FIFO RESTORE transmission trigger level is reached. |
| 5    | SPECIAL_CHARACTER_DETECT | R/W  | 0h    | 0: Normal operation.<br>1:Special character detect enable. Received data is compared with XOFF2 data. If a match occurs the received data is transferred to RX FIFO and IIR bit 4 is set to 1 to indicate a special character has been detected.                                   |

**Table 5-3238. UART\_EFR Register Field Descriptions (continued)**

| Bit | Field           | Type | Reset | Description                                                                                                                                                                       |
|-----|-----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | ENHANCED_EN     | R/W  | 0h    | Enhanced functions write enable bit.<br>0:Disables Writing to IER bits 4-7, FCR bits 4-5, and MCR bits 5-7.<br>1:Enables Writing to IER bits 4-7, FCR bits 4-5, and MCR bits 5-7. |
| 3:0 | SW_FLOW_CONTROL | R/W  | 0h    | Combinations of Software flow control can be selected by programming bit 3 - bit 0. See Software Flow Control Options                                                             |

### 5.24.2.9 UART\_FCR Register

#### 1 UART\_FCR Register (Offset = 8h) [reset = 0h]

Notes:

Bits 4 and 5 can only be written to when EFR[4] = 1

Bits 0 to 3 can be changed only when the baud clock is not running (DLL and DLH set to 0)

See Table 31 for FCR[5:4] setting restriction when SCR[6]=1

See Table 32 for FCR[7:6] setting restriction when SCR[7]=1

Return to [Summary Table](#)

**Table 5-3239. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0008h       |
| UART1         | 5230 1008h       |
| UART2         | 5230 2008h       |
| UART3         | 5230 3008h       |
| UART4         | 5230 4008h       |
| UART5         | 5230 5008h       |

**Figure 5-1067. UART\_FCR Name Register**

|              |              |    |          |                   |                   |         |    |
|--------------|--------------|----|----------|-------------------|-------------------|---------|----|
| 31           | 30           | 29 | 28       | 27                | 26                | 25      | 24 |
| RESERVED_24  |              |    |          |                   |                   |         |    |
| R            |              |    |          |                   |                   |         |    |
| 0h           |              |    |          |                   |                   |         |    |
| 23           | 22           | 21 | 20       | 19                | 18                | 17      | 16 |
| RESERVED_24  |              |    |          |                   |                   |         |    |
| R            |              |    |          |                   |                   |         |    |
| 0h           |              |    |          |                   |                   |         |    |
| 15           | 14           | 13 | 12       | 11                | 10                | 9       | 8  |
| RESERVED_24  |              |    |          |                   |                   |         |    |
| R            |              |    |          |                   |                   |         |    |
| 0h           |              |    |          |                   |                   |         |    |
| 7            | 6            | 5  | 4        | 3                 | 2                 | 1       | 0  |
| RX_FIFO_TRIG | TX_FIFO_TRIG |    | DMA_MODE | TX_FIFO_CLE<br>AR | RX_FIFO_CLE<br>AR | FIFO_EN |    |
| W            | W            |    | W        | W                 | W                 | W       |    |
| 0h           | 0h           |    | 0h       | 0h                | 0h                | 0h      |    |

**Table 5-3241. UART\_FCR Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                           |
|------|--------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED_24  | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                              |
| 7:6  | RX_FIFO_TRIG | W    | 0h    | Sets the trigger level for the RX FIFO:<br>If SCR[7] = 0 and TLR[7:4] = 0000<br>br#00: 8 characters<br>br#01: 16 characters<br>br#10: 56 characters<br>br#11: 60 characters<br>If SCR[7] = 0 and TLR[7:4] != 0000 RX_FIFO_TRIG is not considered.<br>If SCR[7]=1, RX_FIFO_TRIG is 2 LSB of the trigger level [1-63 on 6 bits] with the granularity 1. |



**Table 5-3241. UART\_FCR Register Field Descriptions (continued)**

| Bit | Field         | Type | Reset | Description                                                                                                                                                                                                                                                                                                                          |
|-----|---------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5:4 | TX_FIFO_TRIG  | W    | 0h    | Sets the trigger level for the TX FIFO:<br>If SCR[6] = 0 and TLR[3:0] = 0000<br>br#00: 8 spaces<br>br#01: 16 spaces<br>br#10: 32 spaces<br>br#11: 56 spaces<br>If SCR[6] = 0 and TLR[3:0] != 0000 TX_FIFO_TRIG is not considered.<br>If SCR[6]=1, TX_FIFO_TRIG is 2 LSB of the trigger level [1-63 on 6 bits] with the granularity 1 |
| 3   | DMA_MODE      | W    | 0h    | This register is considered if SCR[0] = 0.<br>0 DMA_MODE 0 (No DMA)<br>1 DMA_MODE 1 (UART_nDMA_REQ[0] in TX, UART_nDMA_REQ[1] in RX)                                                                                                                                                                                                 |
| 2   | TX_FIFO_CLEAR | W    | 0h    | 0 No change<br>1 Clears the transmit FIFO and resets its counter logic to zero. Returns to zero after clearing FIFO.                                                                                                                                                                                                                 |
| 1   | RX_FIFO_CLEAR | W    | 0h    | 0 No change<br>1 Clears the receive FIFO and resets its counter logic to zero. Returns to zero after clearing FIFO.                                                                                                                                                                                                                  |
| 0   | FIFO_EN       | W    | 0h    | 0 Disables the transmit and receive FIFOs. The transmit and receive holding registers are one byte FIFOs.<br>1 : Enables the transmit and receive FIFOs. The transmit and receive holding registers are 64-bytes FIFOs.                                                                                                              |

### 5.24.2.10 UART\_IIR\_CIR Register

#### 1 UART\_IIR\_CIR Register (Offset = 8h) [reset = 0h]

The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.

Return to [Summary Table](#)

**Table 5-3242. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0008h       |
| UART1         | 5230 1008h       |
| UART2         | 5230 2008h       |
| UART3         | 5230 3008h       |
| UART4         | 5230 4008h       |
| UART5         | 5230 5008h       |

**Figure 5-1068. UART\_IIR\_CIR Name Register**

|          |              |          |          |            |        |        |    |
|----------|--------------|----------|----------|------------|--------|--------|----|
| 31       | 30           | 29       | 28       | 27         | 26     | 25     | 24 |
| RESERVED |              |          |          |            |        |        |    |
| NONE     |              |          |          |            |        |        |    |
| 0h       |              |          |          |            |        |        |    |
| 23       | 22           | 21       | 20       | 19         | 18     | 17     | 16 |
| RESERVED |              |          |          |            |        |        |    |
| NONE     |              |          |          |            |        |        |    |
| 0h       |              |          |          |            |        |        |    |
| 15       | 14           | 13       | 12       | 11         | 10     | 9      | 8  |
| RESERVED |              |          |          |            |        |        |    |
| NONE     |              |          |          |            |        |        |    |
| 0h       |              |          |          |            |        |        |    |
| 7        | 6            | 5        | 4        | 3          | 2      | 1      | 0  |
| RESERVED | TX_STATUS_IT | RESERVED | RX_OE_IT | RX_STOP_IT | THR_IT | RHR_IT |    |
| NONE     | R            | NONE     | R        | R          | R      | R      |    |
| 0h       | 0h           | 0h       | 0h       | 0h         | 0h     | 0h     |    |

**Table 5-3244. UART\_IIR\_CIR Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                          |
|------|--------------|------|-------|----------------------------------------------------------------------|
| 31:6 | RESERVED     | NONE | 0h    | Reserved                                                             |
| 5    | TX_STATUS_IT | R    | 0h    | 0 TX status interrupt inactive<br>1 TX status interrupt active       |
| 4    | RESERVED     | NONE | 0h    | Reserved                                                             |
| 3    | RX_OE_IT     | R    | 0h    | 0 RX overrun interrupt inactive<br>1 RX overrun interrupt active     |
| 2    | RX_STOP_IT   | R    | 0h    | 0 Receive stop interrupt inactive<br>1 Receive stop interrupt active |
| 1    | THR_IT       | R    | 0h    | 0 THR interrupt inactive<br>1 THR interrupt active                   |
| 0    | RHR_IT       | R    | 0h    | 0 RHR interrupt inactive<br>1 RHR interrupt active                   |

### 5.24.2.11 UART\_IIR\_IRDA Register

#### 1 UART\_IIR\_IRDA Register (Offset = 8h) [reset = 0h]

The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.

Return to [Summary Table](#)

**Table 5-3245. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0008h       |
| UART1         | 5230 1008h       |
| UART2         | 5230 2008h       |
| UART3         | 5230 3008h       |
| UART4         | 5230 4008h       |
| UART5         | 5230 5008h       |

**Figure 5-1069. UART\_IIR\_IRDA Name Register**

|          |             |              |             |          |                          |        |        |
|----------|-------------|--------------|-------------|----------|--------------------------|--------|--------|
| 31       | 30          | 29           | 28          | 27       | 26                       | 25     | 24     |
| RESERVED |             |              |             |          |                          |        |        |
| NONE     |             |              |             |          |                          |        |        |
| 0h       |             |              |             |          |                          |        |        |
| 23       | 22          | 21           | 20          | 19       | 18                       | 17     | 16     |
| RESERVED |             |              |             |          |                          |        |        |
| NONE     |             |              |             |          |                          |        |        |
| 0h       |             |              |             |          |                          |        |        |
| 15       | 14          | 13           | 12          | 11       | 10                       | 9      | 8      |
| RESERVED |             |              |             |          |                          |        |        |
| NONE     |             |              |             |          |                          |        |        |
| 0h       |             |              |             |          |                          |        |        |
| 7        | 6           | 5            | 4           | 3        | 2                        | 1      | 0      |
| EOF_IT   | LINE_STS_IT | TX_STATUS_IT | STS_FIFO_IT | RX_OE_IT | RX_FIFO_LAS<br>T_BYTE_IT | THR_IT | RHR_IT |
| R        | R           | R            | R           | R        | R                        | R      | R      |
| 0h       | 0h          | 0h           | 0h          | 0h       | 0h                       | 0h     | 0h     |

**Table 5-3247. UART\_IIR\_IRDA Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                    |
|------|--------------|------|-------|------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED     | NONE | 0h    | Reserved                                                                                       |
| 7    | EOF_IT       | R    | 0h    | 0 Received EOF interrupt inactive<br>1 Received EOF interrupt active                           |
| 6    | LINE_STS_IT  | R    | 0h    | 0 Receiver line status interrupt inactive<br>1 Receiver line status interrupt active           |
| 5    | TX_STATUS_IT | R    | 0h    | 0 TX status interrupt inactive<br>1 TX status interrupt active                                 |
| 4    | STS_FIFO_IT  | R    | 0h    | 0 Status FIFO trigger level interrupt inactive<br>1 Status FIFO trigger level interrupt active |
| 3    | RX_OE_IT     | R    | 0h    | 0 RX overrun interrupt inactive<br>1 RX overrun interrupt active                               |

**Table 5-3247. UART\_IIR\_IRDA Register Field Descriptions (continued)**

| Bit | Field                | Type | Reset | Description                                                                                                               |
|-----|----------------------|------|-------|---------------------------------------------------------------------------------------------------------------------------|
| 2   | RX_FIFO_LAST_BYTE_IT | R    | 0h    | <div>0 Last byte of frame in RX FIFO interrupt inactive</div> <div>1 Last byte of frame in RX FIFO interrupt active</div> |
| 1   | THR_IT               | R    | 0h    | <div>0 THR interrupt inactive</div> <div>1 THR interrupt active</div>                                                     |
| 0   | RHR_IT               | R    | 0h    | <div>0 RHR interrupt inactive</div> <div>1 RHR interrupt active</div>                                                     |

### 5.24.2.12 UART\_IIR\_UART Register

#### 1 UART\_IIR\_UART Register (Offset = 8h) [reset = 1h]

The IIR is a read-only register, which provides the source of the interrupt in a prioritized manner.

Return to [Summary Table](#)

**Table 5-3248. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0008h       |
| UART1         | 5230 1008h       |
| UART2         | 5230 2008h       |
| UART3         | 5230 3008h       |
| UART4         | 5230 4008h       |
| UART5         | 5230 5008h       |

**Figure 5-1070. UART\_IIR\_UART Name Register**

|             |    |         |    |    |    |    |            |
|-------------|----|---------|----|----|----|----|------------|
| 31          | 30 | 29      | 28 | 27 | 26 | 25 | 24         |
| RESERVED_24 |    |         |    |    |    |    |            |
| R           |    |         |    |    |    |    |            |
| 0h          |    |         |    |    |    |    |            |
| 23          | 22 | 21      | 20 | 19 | 18 | 17 | 16         |
| RESERVED_24 |    |         |    |    |    |    |            |
| R           |    |         |    |    |    |    |            |
| 0h          |    |         |    |    |    |    |            |
| 15          | 14 | 13      | 12 | 11 | 10 | 9  | 8          |
| RESERVED_24 |    |         |    |    |    |    |            |
| R           |    |         |    |    |    |    |            |
| 0h          |    |         |    |    |    |    |            |
| 7           | 6  | 5       | 4  | 3  | 2  | 1  | 0          |
| FCR_MIRROR  |    | IT_TYPE |    |    |    |    | IT_PENDING |
| R           |    | R       |    |    |    |    | R          |
| 0h          |    | 0h      |    |    |    |    | 1h         |

**Table 5-3250. UART\_IIR\_UART Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                                   |
|------|-------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED_24 | R    | 0h    | Reserved                                                                                                                                                                                                                                                                                      |
| 7:6  | FCR_MIRROR  | R    | 0h    | Mirror the contents of FCR[0] on both bits.                                                                                                                                                                                                                                                   |
| 5:1  | IT_TYPE     | R    | 0h    | 0 Modem Interrupt. Priority=4<br>1 THR interrupt. Priority=3<br>2 RHR interrupt. Priority=2<br>3 Receiver line status error. Priority=3<br>6 Rx timeout. Priority=2<br>8 Xoff/Special character. Priority=5<br>16 CTS, RTS, DSR change state from active (low) to inactive (high). Priority=6 |
| 0    | IT_PENDING  | R    | 1h    | 0 An interrupt is pending<br>1 No interrupt is pending                                                                                                                                                                                                                                        |

### 5.24.2.13 UART\_LCR Register

#### 1 UART\_LCR Register (Offset = Ch) [reset = 0h]

LCR[6:0] define parameters of the transmission and reception.

Note: As soon as LCR[6] is set to 1, the TX line is forced to 0 and remains in this state as long as LCR[6] = 1.

Return to [Summary Table](#)

**Table 5-3251. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 000Ch       |
| UART1         | 5230 100Ch       |
| UART2         | 5230 200Ch       |
| UART3         | 5230 300Ch       |
| UART4         | 5230 400Ch       |
| UART5         | 5230 500Ch       |

**Figure 5-1071. UART\_LCR Name Register**

|             |          |                  |                  |           |         |             |    |
|-------------|----------|------------------|------------------|-----------|---------|-------------|----|
| 31          | 30       | 29               | 28               | 27        | 26      | 25          | 24 |
| RESERVED_24 |          |                  |                  |           |         |             |    |
| R           |          |                  |                  |           |         |             |    |
| 0h          |          |                  |                  |           |         |             |    |
| 23          | 22       | 21               | 20               | 19        | 18      | 17          | 16 |
| RESERVED_24 |          |                  |                  |           |         |             |    |
| R           |          |                  |                  |           |         |             |    |
| 0h          |          |                  |                  |           |         |             |    |
| 15          | 14       | 13               | 12               | 11        | 10      | 9           | 8  |
| RESERVED_24 |          |                  |                  |           |         |             |    |
| R           |          |                  |                  |           |         |             |    |
| 0h          |          |                  |                  |           |         |             |    |
| 7           | 6        | 5                | 4                | 3         | 2       | 1           | 0  |
| DIV_EN      | BREAK_EN | PARITY_TYPE<br>2 | PARITY_TYPE<br>1 | PARITY_EN | NB_STOP | CHAR_LENGTH |    |
| R/W         | R/W      | R/W              | R/W              | R/W       | R/W     | R/W         |    |
| 0h          | 0h       | 0h               | 0h               | 0h        | 0h      | 0h          |    |

**Table 5-3253. UART\_LCR Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                                                                                                                                                                           |
|------|--------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED_24  | R    | 0h    | Reserved                                                                                                                                                                                                                                              |
| 7    | DIV_EN       | R/W  | 0h    | 0 Normal operating condition<br>1 Divisor latch enable. Allows to access to DLL, DLH and other registers (refer to the registers mapping)                                                                                                             |
| 6    | BREAK_EN     | R/W  | 0h    | Break control bit.<br>0 Normal operating condition.<br>1 Forces the transmitter output to go low to alert the communication terminal                                                                                                                  |
| 5    | PARITY_TYPE2 | R/W  | 0h    | Selects the forced parity format [if LCR[3] = 1]. If LCR[5] = 1 and LCR[4] = 0, the parity bit is forced to 1 in the transmitted and received data. If LCR[5] = 1 and LCR[4] = 1, the parity bit is forced to 0 in the transmitted and received data. |

**Table 5-3253. UART\_LCR Register Field Descriptions (continued)**

| Bit | Field        | Type | Reset | Description                                                                                                                                                                    |
|-----|--------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | PARITY_TYPE1 | R/W  | 0h    | 0     Odd parity is generated (if LCR[3] = 1)<br>1     Even parity is generated (if LCR[3] = 1)                                                                                |
| 3   | PARITY_EN    | R/W  | 0h    | 0     No parity<br>1     A parity bit is generated during transmission and the receiver checks for received parity.                                                            |
| 2   | NB_STOP      | R/W  | 0h    | Specifies the number of stop bits:<br>0     1 stop bits (word length = 5, 6, 7, 8)<br>1     1.5 stop bits (word length = 5) in USART mode. 2 stop bits (word length = 6, 7, 8) |
| 1:0 | CHAR_LENGTH  | R/W  | 0h    | Specifies the word length to be transmitted or received.<br>0     5 bits<br>1     6 bits<br>2     7 bits<br>3     8 bits                                                       |

#### 5.24.2.14 UART\_MCR Register

##### 1 UART\_MCR Register (Offset = 10h) [reset = 0h]

MCR[3:0] controls the interface with the modem, data set or peripheral device that is emulating the modem.

Return to [Summary Table](#)

**Table 5-3254. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0010h       |
| UART1         | 5230 1010h       |
| UART2         | 5230 2010h       |
| UART3         | 5230 3010h       |
| UART4         | 5230 4010h       |
| UART5         | 5230 5010h       |

**Figure 5-1072. UART\_MCR Name Register**

|             |         |        |             |           |           |     |     |
|-------------|---------|--------|-------------|-----------|-----------|-----|-----|
| 31          | 30      | 29     | 28          | 27        | 26        | 25  | 24  |
| RESERVED_24 |         |        |             |           |           |     |     |
| R           |         |        |             |           |           |     |     |
| 0h          |         |        |             |           |           |     |     |
| 23          | 22      | 21     | 20          | 19        | 18        | 17  | 16  |
| RESERVED_24 |         |        |             |           |           |     |     |
| R           |         |        |             |           |           |     |     |
| 0h          |         |        |             |           |           |     |     |
| 15          | 14      | 13     | 12          | 11        | 10        | 9   | 8   |
| RESERVED_24 |         |        |             |           |           |     |     |
| R           |         |        |             |           |           |     |     |
| 0h          |         |        |             |           |           |     |     |
| 7           | 6       | 5      | 4           | 3         | 2         | 1   | 0   |
| RESERVED    | TCR_TLR | XON_EN | LOOPBACK_EN | CD_STS_CH | RI_STS_CH | RTS | DTR |
| R           | R/W     | R/W    | R/W         | R/W       | R/W       | R/W | R/W |
| 0h          | 0h      | 0h     | 0h          | 0h        | 0h        | 0h  | 0h  |

**Table 5-3256. UART\_MCR Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                                                             |
|------|-------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED_24 | R    | 0h    | Reserved                                                                                                                                                                                                |
| 7    | RESERVED    | R    | 0h    |                                                                                                                                                                                                         |
| 6    | TCR_TLR     | R/W  | 0h    | 0 No action<br>1 Enables access to the TCR and TLR registers.                                                                                                                                           |
| 5    | XON_EN      | R/W  | 0h    | 0 Disable 'XON any' function<br>1 Enable 'XON any' function                                                                                                                                             |
| 4    | LOOPBACK_EN | R/W  | 0h    | 0 Normal operating mode<br>1 Enable local loopback mode (internal). In this mode the MCR[3:0] signals are looped back into MSR[7:4]. The transmit output is looped back to the receive input internally |



**Table 5-3256. UART\_MCR Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description                                                                                                                                                                                        |
|-----|-----------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3   | CD_STS_CH | R/W  | 0h    | 0 In loopback forces DCD* input high and IRQ outputs to inactive state.<br>1 In loopback forces DCD* input low and IRQ outputs to inactive state.                                                  |
| 2   | RI_STS_CH | R/W  | 0h    | 0 In loopback forces RI* input high.<br>1 In loopback forces RI* input low.                                                                                                                        |
| 1   | RTS       | R/W  | 0h    | In loop back controls MSR[4].<br>If auto-RTS is enabled the RTS* output is controlled by hardware flow control.<br>0 Force RTS* output to inactive (high).<br>1 Force RTS* output to active (low). |
| 0   | DTR       | R/W  | 0h    | 0 Force DTR* output to inactive (high).<br>1 Force DTR* output to active (low).                                                                                                                    |

### 5.24.2.15 UART\_XON1\_ADDR1 Register

#### 1 UART\_XON1\_ADDR1 Register (Offset = 10h) [reset = 0h]

XON1/ADDR1 Register.

Return to [Summary Table](#)

**Table 5-3257. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0010h       |
| UART1         | 5230 1010h       |
| UART2         | 5230 2010h       |
| UART3         | 5230 3010h       |
| UART4         | 5230 4010h       |
| UART5         | 5230 5010h       |

**Figure 5-1073. UART\_XON1\_ADDR1 Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED  |    |    |    |    |    |    |    |
| NONE      |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED  |    |    |    |    |    |    |    |
| NONE      |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED  |    |    |    |    |    |    |    |
| NONE      |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XON_WORD1 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 5-3259. UART\_XON1\_ADDR1 Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                              |
|------|-----------|------|-------|------------------------------------------------------------------------------------------|
| 31:8 | RESERVED  | NONE | 0h    | Reserved                                                                                 |
| 7:0  | XON_WORD1 | R/W  | 0h    | Used to store the 8-bit XON1 character in UART modes and ADDR1 address 1 for IrDA modes. |

### 5.24.2.16 UART\_LSR\_CIR Register

#### 1 UART\_LSR\_CIR Register (Offset = 14h) [reset = 81h]

IR CIR mode line status register.

Return to [Summary Table](#)

**Table 5-3260. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0014h       |
| UART1         | 5230 1014h       |
| UART2         | 5230 2014h       |
| UART3         | 5230 3014h       |
| UART4         | 5230 4014h       |
| UART5         | 5230 5014h       |

**Figure 5-1074. UART\_LSR\_CIR Name Register**

|           |          |         |          |    |    |           |    |
|-----------|----------|---------|----------|----|----|-----------|----|
| 31        | 30       | 29      | 28       | 27 | 26 | 25        | 24 |
| RESERVED  |          |         |          |    |    |           |    |
| NONE      |          |         |          |    |    |           |    |
| 0h        |          |         |          |    |    |           |    |
| 23        | 22       | 21      | 20       | 19 | 18 | 17        | 16 |
| RESERVED  |          |         |          |    |    |           |    |
| NONE      |          |         |          |    |    |           |    |
| 0h        |          |         |          |    |    |           |    |
| 15        | 14       | 13      | 12       | 11 | 10 | 9         | 8  |
| RESERVED  |          |         |          |    |    |           |    |
| NONE      |          |         |          |    |    |           |    |
| 0h        |          |         |          |    |    |           |    |
| 7         | 6        | 5       | 4        | 3  | 2  | 1         | 0  |
| THR_EMPTY | RESERVED | RX_STOP | RESERVED |    |    | RX_FIFO_E |    |
| R         | R        | R       | NONE     |    |    | R         |    |
| 1h        | 0h       | 0h      | 0h       |    |    | 1h        |    |

**Table 5-3262. UART\_LSR\_CIR Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                             |
|------|-----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED  | NONE | 0h    | Reserved                                                                                                                                                                                                                |
| 7    | THR_EMPTY | R    | 1h    | 0 Transmit holding register (TX FIFO) is not empty<br>1 Transmit hold register (TX FIFO) is empty. The transmission is not necessarily completed                                                                        |
| 6    | RESERVED  | R    | 0h    |                                                                                                                                                                                                                         |
| 5    | RX_STOP   | R    | 0h    | The RX_STOP is generated based on the value set in the BOF Length register (EBLR). It is cleared on a single read of the LSR register<br>0 Reception is on going or waiting for a new frame<br>1 Reception is completed |
| 4:1  | RESERVED  | NONE | 0h    | Reserved                                                                                                                                                                                                                |

**Table 5-3262. UART\_LSR\_CIR Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description                                                                                                            |
|-----|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------|
| 0   | RX_FIFO_E | R    | 1h    | <div>0</div> <div>1</div> <div>No data in the receive FIFO</div> <div>At least one data character in the RX FIFO</div> |

### 5.24.2.17 UART\_LSR\_IRDA Register

#### 1 UART\_LSR\_IRDA Register (Offset = 14h) [reset = 83h]

IR-IRDA mode line status register.

Return to [Summary Table](#)

**Table 5-3263. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0014h       |
| UART1         | 5230 1014h       |
| UART2         | 5230 2014h       |
| UART3         | 5230 3014h       |
| UART4         | 5230 4014h       |
| UART5         | 5230 5014h       |

**Figure 5-1075. UART\_LSR\_IRDA Name Register**

|           |               |              |                |       |     |            |           |
|-----------|---------------|--------------|----------------|-------|-----|------------|-----------|
| 31        | 30            | 29           | 28             | 27    | 26  | 25         | 24        |
| RESERVED  |               |              |                |       |     |            |           |
| NONE      |               |              |                |       |     |            |           |
| 0h        |               |              |                |       |     |            |           |
| 23        | 22            | 21           | 20             | 19    | 18  | 17         | 16        |
| RESERVED  |               |              |                |       |     |            |           |
| NONE      |               |              |                |       |     |            |           |
| 0h        |               |              |                |       |     |            |           |
| 15        | 14            | 13           | 12             | 11    | 10  | 9          | 8         |
| RESERVED  |               |              |                |       |     |            |           |
| NONE      |               |              |                |       |     |            |           |
| 0h        |               |              |                |       |     |            |           |
| 7         | 6             | 5            | 4              | 3     | 2   | 1          | 0         |
| THR_EMPTY | STS_FIFO_FULL | RX_LAST_BYTE | FRAME_TOO_LONG | ABORT | CRC | STS_FIFO_E | RX_FIFO_E |
| R         | R             | R            | R              | R     | R   | R          | R         |
| 1h        | 0h            | 0h           | 0h             | 0h    | 0h  | 1h         | 1h        |

**Table 5-3265. UART\_LSR\_IRDA Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                                                                                                                                                                                                                                                                                                  |
|------|---------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED      | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                                                                     |
| 7    | THR_EMPTY     | R    | 1h    | 0 Transmit holding register (TX FIFO) is not empty<br>1 Transmit hold register (TX FIFO) is empty. The transmission is not necessarily completed                                                                                                                                                                             |
| 6    | STS_FIFO_FULL | R    | 0h    | 0 Status FIFO not full<br>1 Status FIFO full                                                                                                                                                                                                                                                                                 |
| 5    | RX_LAST_BYTE  | R    | 0h    | 0 The RX FIFO (RHR) does not contain the last byte of the frame to be read<br>1 The RX FIFO (RHR) contains the last byte of the frame to be read. This bit is only set when the last byte of a frame is available to be read. It is used to determine the frame boundary. It is cleared on a single read of the LSR register |

**Table 5-3265. UART\_LSR\_IRDA Register Field Descriptions (continued)**

| Bit | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                     |
|-----|----------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | FRAME_TOO_LONG | R    | 0h    | <div>0</div> <div>1</div> No frame-too-long error in frame<br>Frame-too-long error in the frame at the top of the STATUS FIFO, [next character to be read]. This bit is set to 1 when a frame exceeding the maximum length (set by RXFLH and RXFLL registers) has been received. When this error is detected, current frame reception is terminated. Reception is stopped until the next START flag is detected |
| 3   | ABORT          | R    | 0h    | <div>0</div> <div>1</div> No abort pattern error in frame<br>Abort pattern is received. SIR & MIR: Abort pattern. FIR: Illegal symbol                                                                                                                                                                                                                                                                           |
| 2   | CRC            | R    | 0h    | <div>0</div> <div>1</div> No CRC error in frame<br>CRC error in the frame at the top of the STATUS FIFO (next character to be read)                                                                                                                                                                                                                                                                             |
| 1   | STS_FIFO_E     | R    | 1h    | <div>0</div> <div>1</div> Status FIFO not empty<br>Status FIFO empty                                                                                                                                                                                                                                                                                                                                            |
| 0   | RX_FIFO_E      | R    | 1h    | <div>0</div> <div>1</div> No data in the receive FIFO<br>At least one data character in the RX FIFO                                                                                                                                                                                                                                                                                                             |

### 5.24.2.18 UART\_LSR\_UART Register

#### 1 UART\_LSR\_UART Register (Offset = 14h) [reset = 60h]

Return to [Summary Table](#)

**Table 5-3266. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0014h       |
| UART1         | 5230 1014h       |
| UART2         | 5230 2014h       |
| UART3         | 5230 3014h       |
| UART4         | 5230 4014h       |
| UART5         | 5230 5014h       |

**Figure 5-1076. UART\_LSR\_UART Name Register**

|             |         |           |       |       |       |       |           |
|-------------|---------|-----------|-------|-------|-------|-------|-----------|
| 31          | 30      | 29        | 28    | 27    | 26    | 25    | 24        |
| RESERVED_24 |         |           |       |       |       |       |           |
| R           |         |           |       |       |       |       |           |
| 0h          |         |           |       |       |       |       |           |
| 23          | 22      | 21        | 20    | 19    | 18    | 17    | 16        |
| RESERVED_24 |         |           |       |       |       |       |           |
| R           |         |           |       |       |       |       |           |
| 0h          |         |           |       |       |       |       |           |
| 15          | 14      | 13        | 12    | 11    | 10    | 9     | 8         |
| RESERVED_24 |         |           |       |       |       |       |           |
| R           |         |           |       |       |       |       |           |
| 0h          |         |           |       |       |       |       |           |
| 7           | 6       | 5         | 4     | 3     | 2     | 1     | 0         |
| RX_FIFO_STS | TX_SR_E | TX_FIFO_E | RX_BI | RX_FE | RX_PE | RX_OE | RX_FIFO_E |
| R           | R       | R         | R     | R     | R     | R     | R         |
| 0h          | 1h      | 1h        | 0h    | 0h    | 0h    | 0h    | 0h        |

**Table 5-3268. UART\_LSR\_UART Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                           |
|------|-------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED_24 | R    | 0h    | Reserved                                                                                                                                                              |
| 7    | RX_FIFO_STS | R    | 0h    | 0 Normal operation<br>1 At least one parity error, framing error or break indication in the RX FIFO. Bit 7 is cleared when no more errors are present in the RX FIFO. |
| 6    | TX_SR_E     | R    | 1h    | 0 Transmitter hold (TX FIFO) and shift registers are not empty.<br>1 Transmitter hold (TX FIFO) and shift registers are empty                                         |
| 5    | TX_FIFO_E   | R    | 1h    | 0 Transmit hold register (TX FIFO) is not empty<br>1 Transmit hold register (TX FIFO) is empty. The transmission is not necessarily completed.                        |

**Table 5-3268. UART\_LSR\_UART Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description                                                                                                                                                                                          |
|-----|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | RX_BI     | R    | 0h    | 0 No break condition<br>1 A break was detected while the data being read from the RX FIFO was being received. (i.e. RX input was low for one character + 1 bit time frame).                          |
| 3   | RX_FE     | R    | 0h    | 0 No framing error in data being read from RX FIFO.<br>1 Framing error occurred in data being read from RX FIFO. (received data did not have a valid stop bit)                                       |
| 2   | RX_PE     | R    | 0h    | 0 No parity error in data being read from RX FIFO.<br>1 Parity error in data being read from RX FIFO                                                                                                 |
| 1   | RX_OE     | R    | 0h    | 0 No overrun error<br>1 Overrun error has occurred. Set when the character held in the receive shift register is not transferred to the RX FIFO. This case can occur only when receive FIFO is full. |
| 0   | RX_FIFO_E | R    | 0h    | Line Status Register<br>0 No data in the receive FIFO<br>1 At least one data character in the RX FIFO                                                                                                |



### 5.24.2.19 UART\_XON2\_ADDR2 Register

#### 1 UART\_XON2\_ADDR2 Register (Offset = 14h) [reset = 0h]

XON2/ADDR2 Register.

Return to [Summary Table](#)

**Table 5-3269. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0014h       |
| UART1         | 5230 1014h       |
| UART2         | 5230 2014h       |
| UART3         | 5230 3014h       |
| UART4         | 5230 4014h       |
| UART5         | 5230 5014h       |

**Figure 5-1077. UART\_XON2\_ADDR2 Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED  |    |    |    |    |    |    |    |
| NONE      |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED  |    |    |    |    |    |    |    |
| NONE      |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED  |    |    |    |    |    |    |    |
| NONE      |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XON_WORD2 |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 5-3271. UART\_XON2\_ADDR2 Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                              |
|------|-----------|------|-------|------------------------------------------------------------------------------------------|
| 31:8 | RESERVED  | NONE | 0h    | Reserved                                                                                 |
| 7:0  | XON_WORD2 | R/W  | 0h    | Used to store the 8-bit XON2 character in UART modes and ADDR2 address 2 for IrDA modes. |

### 5.24.2.20 UART\_MSR Register

#### 1 UART\_MSR Register (Offset = 18h) [reset = 0h]

This register provides information about the current state of the control lines from the modem, data set or peripheral device to the LH. It also indicates when a control input from the modem changes state.

Return to [Summary Table](#)

**Table 5-3272. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0018h       |
| UART1         | 5230 1018h       |
| UART2         | 5230 2018h       |
| UART3         | 5230 3018h       |
| UART4         | 5230 4018h       |
| UART5         | 5230 5018h       |

**Figure 5-1078. UART\_MSR Name Register**

|             |         |          |          |         |        |         |         |
|-------------|---------|----------|----------|---------|--------|---------|---------|
| 31          | 30      | 29       | 28       | 27      | 26     | 25      | 24      |
| RESERVED_24 |         |          |          |         |        |         |         |
| R           |         |          |          |         |        |         |         |
| 0h          |         |          |          |         |        |         |         |
| 23          | 22      | 21       | 20       | 19      | 18     | 17      | 16      |
| RESERVED_24 |         |          |          |         |        |         |         |
| R           |         |          |          |         |        |         |         |
| 0h          |         |          |          |         |        |         |         |
| 15          | 14      | 13       | 12       | 11      | 10     | 9       | 8       |
| RESERVED_24 |         |          |          |         |        |         |         |
| R           |         |          |          |         |        |         |         |
| 0h          |         |          |          |         |        |         |         |
| 7           | 6       | 5        | 4        | 3       | 2      | 1       | 0       |
| NCD_STS     | NRI_STS | NDSR_STS | NCTS_STS | DCD_STS | RI_STS | DSR_STS | CTS_STS |
| R           | R       | R        | R        | R       | R      | R       | R       |
| 0h          | 0h      | 0h       | 0h       | 0h      | 0h     | 0h      | 0h      |

**Table 5-3274. UART\_MSR Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                              |
|------|-------------|------|-------|----------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED_24 | R    | 0h    | Reserved                                                                                                 |
| 7    | NCD_STS     | R    | 0h    | This bit is the complement of the DCD* input. In loop-back mode it is equivalent to MCR[3]               |
| 6    | NRI_STS     | R    | 0h    | This bit is the complement of the RI* input. In loop-back mode it is equivalent to MCR[2]                |
| 5    | NDSR_STS    | R    | 0h    | This bit is the complement of the DSR* input. In loop-back mode, it is equivalent to MCR[0]              |
| 4    | NCTS_STS    | R    | 0h    | This bit is the complement of the CTS* input. In loop-back mode it is equivalent to MCR[1]               |
| 3    | DCD_STS     | R    | 0h    | Indicates that DCD* input [or MCR[3] in loop back] has changed. Cleared on a read.                       |
| 2    | RI_STS      | R    | 0h    | Indicates that RI* input [or MCR[2] in loop back] has changed state from low to high. Cleared on a read. |

**Table 5-3274. UART\_MSR Register Field Descriptions (continued)**

| Bit | Field   | Type | Reset | Description                                                                                |
|-----|---------|------|-------|--------------------------------------------------------------------------------------------|
| 1   | DSR_STS | R    | 0h    | 1 Indicates that DSR* input (or MCR[0] in loop back) has changed state. Cleared on a read  |
| 0   | CTS_STS | R    | 0h    | 1 Indicates that CTS* input (or MCR[1] in loop back) has changed state. Cleared on a read. |

### 5.24.2.21 UART\_TCR Register

#### 1 UART\_TCR Register (Offset = 18h) [reset = Fh]

Transmission Control Register.

Return to [Summary Table](#)

**Table 5-3275. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0018h       |
| UART1         | 5230 1018h       |
| UART2         | 5230 2018h       |
| UART3         | 5230 3018h       |
| UART4         | 5230 4018h       |
| UART5         | 5230 5018h       |

**Figure 5-1079. UART\_TCR Name Register**

|                    |    |    |    |                   |    |    |    |
|--------------------|----|----|----|-------------------|----|----|----|
| 31                 | 30 | 29 | 28 | 27                | 26 | 25 | 24 |
| RESERVED           |    |    |    |                   |    |    |    |
| NONE               |    |    |    |                   |    |    |    |
| 0h                 |    |    |    |                   |    |    |    |
| 23                 | 22 | 21 | 20 | 19                | 18 | 17 | 16 |
| RESERVED           |    |    |    |                   |    |    |    |
| NONE               |    |    |    |                   |    |    |    |
| 0h                 |    |    |    |                   |    |    |    |
| 15                 | 14 | 13 | 12 | 11                | 10 | 9  | 8  |
| RESERVED           |    |    |    |                   |    |    |    |
| NONE               |    |    |    |                   |    |    |    |
| 0h                 |    |    |    |                   |    |    |    |
| 7                  | 6  | 5  | 4  | 3                 | 2  | 1  | 0  |
| RX_FIFO_TRIG_START |    |    |    | RX_FIFO_TRIG_HALT |    |    |    |
| R/W                |    |    |    | R/W               |    |    |    |
| 0h                 |    |    |    | Fh                |    |    |    |

**Table 5-3277. UART\_TCR Register Field Descriptions**

| Bit  | Field              | Type | Reset | Description                                            |
|------|--------------------|------|-------|--------------------------------------------------------|
| 31:8 | RESERVED           | NONE | 0h    | Reserved                                               |
| 7:4  | RX_FIFO_TRIG_START | R/W  | 0h    | RX FIFO trigger level to RESTORE transmission (0 - 60) |
| 3:0  | RX_FIFO_TRIG_HALT  | R/W  | Fh    | RX FIFO trigger level to HALT transmission (0 - 60)    |

### 5.24.2.22 UART\_XOFF1 Register

#### 1 UART\_XOFF1 Register (Offset = 18h) [reset = 0h]

XOFF1 Register.

Return to [Summary Table](#)

**Table 5-3278. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0018h       |
| UART1         | 5230 1018h       |
| UART2         | 5230 2018h       |
| UART3         | 5230 3018h       |
| UART4         | 5230 4018h       |
| UART5         | 5230 5018h       |

**Figure 5-1080. UART\_XOFF1 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XOFF_WORD1 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-3280. UART\_XOFF1 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                    |
|------|------------|------|-------|----------------------------------------------------------------|
| 31:8 | RESERVED   | NONE | 0h    | Reserved                                                       |
| 7:0  | XOFF_WORD1 | R/W  | 0h    | Used to store the 8-bit XOFF1 character in used in UART modes. |

### 5.24.2.23 UART\_SPR Register

#### 1 UART\_SPR Register (Offset = 1Ch) [reset = 0h]

This read/write register does not control the module in anyway. It is intended as a scratchpad register to be used by the programmer to hold temporary data.

Return to [Summary Table](#)

**Table 5-3281. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 001Ch       |
| UART1         | 5230 101Ch       |
| UART2         | 5230 201Ch       |
| UART3         | 5230 301Ch       |
| UART4         | 5230 401Ch       |
| UART5         | 5230 501Ch       |

**Figure 5-1081. UART\_SPR Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_24 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_24 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_24 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SPR_WORD    |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-3283. UART\_SPR Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description         |
|------|-------------|------|-------|---------------------|
| 31:8 | RESERVED_24 | R    | 0h    | Reserved            |
| 7:0  | SPR_WORD    | R/W  | 0h    | Scratchpad register |

### 5.24.2.24 UART\_TLR Register

#### 1 UART\_TLR Register (Offset = 1Ch) [reset = 0h]

Trigger Level Register.

Return to [Summary Table](#)

**Table 5-3284. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 001Ch       |
| UART1         | 5230 101Ch       |
| UART2         | 5230 201Ch       |
| UART3         | 5230 301Ch       |
| UART4         | 5230 401Ch       |
| UART5         | 5230 501Ch       |

**Figure 5-1082. UART\_TLR Name Register**

|                  |    |    |    |                  |    |    |    |
|------------------|----|----|----|------------------|----|----|----|
| 31               | 30 | 29 | 28 | 27               | 26 | 25 | 24 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 23               | 22 | 21 | 20 | 19               | 18 | 17 | 16 |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 15               | 14 | 13 | 12 | 11               | 10 | 9  | 8  |
| RESERVED         |    |    |    |                  |    |    |    |
| NONE             |    |    |    |                  |    |    |    |
| 0h               |    |    |    |                  |    |    |    |
| 7                | 6  | 5  | 4  | 3                | 2  | 1  | 0  |
| RX_FIFO_TRIG_DMA |    |    |    | TX_FIFO_TRIG_DMA |    |    |    |
| R/W              |    |    |    | R/W              |    |    |    |
| 0h               |    |    |    | 0h               |    |    |    |

**Table 5-3286. UART\_TLR Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                 |
|------|------------------|------|-------|-----------------------------|
| 31:8 | RESERVED         | NONE | 0h    | Reserved                    |
| 7:4  | RX_FIFO_TRIG_DMA | R/W  | 0h    | Receive FIFO trigger level  |
| 3:0  | TX_FIFO_TRIG_DMA | R/W  | 0h    | Transmit FIFO trigger level |

### 5.24.2.25 UART\_XOFF2 Register

#### 1 UART\_XOFF2 Register (Offset = 1Ch) [reset = 0h]

XOFF2 Register.

Return to [Summary Table](#)

**Table 5-3287. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 001Ch       |
| UART1         | 5230 101Ch       |
| UART2         | 5230 201Ch       |
| UART3         | 5230 301Ch       |
| UART4         | 5230 401Ch       |
| UART5         | 5230 501Ch       |

**Figure 5-1083. UART\_XOFF2 Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED   |    |    |    |    |    |    |    |
| NONE       |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| XOFF_WORD2 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-3289. UART\_XOFF2 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                    |
|------|------------|------|-------|----------------------------------------------------------------|
| 31:8 | RESERVED   | NONE | 0h    | Reserved                                                       |
| 7:0  | XOFF_WORD2 | R/W  | 0h    | Used to store the 8-bit XOFF2 character in used in UART modes. |



### 5.24.2.26 UART\_MDR1 Register

#### 1 UART\_MDR1 Register (Offset = 20h) [reset = 7h]

The mode of operation can be programmed by writing to MDR1[2:0] and therefore the MDR1 must be programmed on start-up after configuration of the configuration registers (DLL, DLH, LCR). The value of MDR1[2:0] must not be changed again during normal operation.

Note: If the module is disabled by setting the MODE\_SELECT field to.

Return to [Summary Table](#)

**Table 5-3290. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0020h       |
| UART1         | 5230 1020h       |
| UART2         | 5230 2020h       |
| UART3         | 5230 3020h       |
| UART4         | 5230 4020h       |
| UART5         | 5230 5020h       |

**Figure 5-1084. UART\_MDR1 Name Register**

|                |          |     |          |          |             |    |    |
|----------------|----------|-----|----------|----------|-------------|----|----|
| 31             | 30       | 29  | 28       | 27       | 26          | 25 | 24 |
| RESERVED_24    |          |     |          |          |             |    |    |
| R              |          |     |          |          |             |    |    |
| 0h             |          |     |          |          |             |    |    |
| 23             | 22       | 21  | 20       | 19       | 18          | 17 | 16 |
| RESERVED_24    |          |     |          |          |             |    |    |
| R              |          |     |          |          |             |    |    |
| 0h             |          |     |          |          |             |    |    |
| 15             | 14       | 13  | 12       | 11       | 10          | 9  | 8  |
| RESERVED_24    |          |     |          |          |             |    |    |
| R              |          |     |          |          |             |    |    |
| 0h             |          |     |          |          |             |    |    |
| 7              | 6        | 5   | 4        | 3        | 2           | 1  | 0  |
| FRAME_END_MODE | SIP_MODE | SCT | SET_TXIR | IR_SLEEP | MODE_SELECT |    |    |
| R/W            | R/W      | R/W | R/W      | R/W      | R/W         |    |    |
| 0h             | 0h       | 0h  | 0h       | 0h       | 7h          |    |    |

**Table 5-3292. UART\_MDR1 Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                                                                                |
|------|----------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED_24    | R    | 0h    | Reserved                                                                                                                                                   |
| 7    | FRAME_END_MODE | R/W  | 0h    | IrDA mode only.<br>0 Frame-length method<br>1 Set EOT bit method                                                                                           |
| 6    | SIP_MODE       | R/W  | 0h    | MIR/FIR modes only.<br>0 Manual SIP mode: SIP is generated with the control of ACREG[3]<br>1 Automatic SIP mode: SIP is generated after each transmission. |

**Table 5-3292. UART\_MDR1 Register Field Descriptions (continued)**

| Bit | Field       | Type | Reset | Description                                                                                                                                                                                                                                                    |
|-----|-------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5   | SCT         | R/W  | 0h    | Store and control the transmission<br>0 Starts the Infrared transmission as soon as a value is written to THR<br>1 Starts the Infrared transmission with the control of ACREG[2]. Note: before starting any transmission, there must be no reception on going. |
| 4   | SET_TXIR    | R/W  | 0h    | Used to configure the infrared transceiver.<br>0 No action if MDR2[7]=0. TXIR pin output is forced low if MDR2[7]=1<br>1 TXIR pin output is forced high (not dependant of MDR2[7] value).                                                                      |
| 3   | IR_SLEEP    | R/W  | 0h    | 0 IrDA/CIR sleep mode disabled<br>1 IrDA/CIR sleep mode enabled                                                                                                                                                                                                |
| 2:0 | MODE_SELECT | R/W  | 7h    | 0 UART 16x mode<br>1 SIR mode<br>2 UART 16x auto-baud<br>3 UART 13x mode<br>4 MIR mode<br>5 FIR mode<br>6 CIR mode<br>7 Disable (default state)                                                                                                                |

### 5.24.2.27 UART\_MDR2 Register

#### 1 UART\_MDR2 Register (Offset = 24h) [reset = 0h]

IR-IrDA and IR-CIR modes only.

MDR2[0] describes the status of the interrupt in IIR[5]. The IRTX\_UNDERRUN bit should be read after an IIR[5] TX\_STATUS\_IT interrupt has occurred. The bits [2:1] of this register sets the trigger level for the frame status FIFO (8 entries) and must be programmed before the mode is programmed in MDR1[2:0].

Note: The MDR2[6] gives the flexibility to invert the RX pin inside the UART module to ensure that the protocol at the input of the transceiver module has the same polarity at module level. By default, the RX pin is inverted because most of transceiver invert the IR receive pin.

Return to [Summary Table](#)

**Table 5-3293. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0024h       |
| UART1         | 5230 1024h       |
| UART2         | 5230 2024h       |
| UART3         | 5230 3024h       |
| UART4         | 5230 4024h       |
| UART5         | 5230 5024h       |

**Figure 5-1085. UART\_MDR2 Name Register**

|              |            |                |    |            |               |    |                |
|--------------|------------|----------------|----|------------|---------------|----|----------------|
| 31           | 30         | 29             | 28 | 27         | 26            | 25 | 24             |
| RESERVED_24  |            |                |    |            |               |    |                |
| R            |            |                |    |            |               |    |                |
| 0h           |            |                |    |            |               |    |                |
| 23           | 22         | 21             | 20 | 19         | 18            | 17 | 16             |
| RESERVED_24  |            |                |    |            |               |    |                |
| R            |            |                |    |            |               |    |                |
| 0h           |            |                |    |            |               |    |                |
| 15           | 14         | 13             | 12 | 11         | 10            | 9  | 8              |
| RESERVED_24  |            |                |    |            |               |    |                |
| R            |            |                |    |            |               |    |                |
| 0h           |            |                |    |            |               |    |                |
| 7            | 6          | 5              | 4  | 3          | 2             | 1  | 0              |
| SET_TXIR_ALT | IRRXINVERT | CIR_PULSE_MODE |    | UART_PULSE | STS_FIFO_TRIG |    | IRTX_UNDEERRUN |
| R/W          | R/W        | R/W            |    | R/W        | R/W           |    | R              |
| 0h           | 0h         | 0h             |    | 0h         | 0h            |    | 0h             |

**Table 5-3295. UART\_MDR2 Register Field Descriptions**

| Bit  | Field        | Type | Reset | Description                                                                                              |
|------|--------------|------|-------|----------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED_24  | R    | 0h    | Reserved                                                                                                 |
| 7    | SET_TXIR_ALT | R/W  | 0h    | Provide alternate functionality for MDR1[4] [SET_TXIR]<br>0 Normal mode<br>1 Alternate mode for SET_TXIR |

**Table 5-3295. UART\_MDR2 Register Field Descriptions (continued)**

| Bit | Field          | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                      |
|-----|----------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6   | IRRXINVERT     | R/W  | 0h    | Only for IR mode [IRDA & CIR]Invert RX pin inside the module before the voting or sampling system logic of the infra red block. This will not effect the RX path in UART Modem modes.<br><br>0      inversion is performed<br>1      No inversion is performed                                                                                                                   |
| 5:4 | CIR_PULSE_MODE | R/W  | 0h    | CIR Pulse modulation definition. It defines high level of the pulse width associated with a digit:<br><br>0      Pulse width of 3 from 12 cycles<br>1      Pulse width of 4 from 12 cycles<br>2      Pulse width of 5 from 12 cycles<br>3      Pulse width of 6 from 12 cycles                                                                                                   |
| 3   | UART_PULSE     | R/W  | 0h    | UART mode only. Used to allow pulse shaping in UART mode.<br><br>0      normal UART mode<br>1      UART mode with a pulse shaping                                                                                                                                                                                                                                                |
| 2:1 | STS_FIFO_TRIG  | R/W  | 0h    | Only for IR-IRDA mode.<br>Frame Status FIFO Threshold select:<br><br>0      1 entry<br>1      4 entries<br>2      7 entries<br>3      8 entries                                                                                                                                                                                                                                  |
| 0   | IRTX_UNDERRUN  | R    | 0h    | IRDA Transmission status interrupt.When the IIR[5] interrupt occurs, the meaning of the interrupt is :<br><br>0      the last bit of the frame has been transmitted successfully without error.<br>1      an underrun has occurred. The last bit of the frame has been transmitted but with an underrun error present. The bit is reset to '0' when the RESUME register is read. |

### 5.24.2.28 UART\_SFLSR Register

#### 1 UART\_SFLSR Register (Offset = 28h) [reset = 0h]

IrDA modes only.

Reading this register effectively reads frame status information from the status FIFO (this register doesn't physically exist). Reading this register will increment the status FIFO read pointer (SFREGL and SFREGH must be read first).

Return to [Summary Table](#)

**Table 5-3296. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0028h       |
| UART1         | 5230 1028h       |
| UART2         | 5230 2028h       |
| UART3         | 5230 3028h       |
| UART4         | 5230 4028h       |
| UART5         | 5230 5028h       |

**Figure 5-1086. UART\_SFLSR Name Register**

|             |    |    |          |                      |              |           |           |
|-------------|----|----|----------|----------------------|--------------|-----------|-----------|
| 31          | 30 | 29 | 28       | 27                   | 26           | 25        | 24        |
| RESERVED_24 |    |    |          |                      |              |           |           |
| R           |    |    |          |                      |              |           |           |
| 0h          |    |    |          |                      |              |           |           |
| 23          | 22 | 21 | 20       | 19                   | 18           | 17        | 16        |
| RESERVED_24 |    |    |          |                      |              |           |           |
| R           |    |    |          |                      |              |           |           |
| 0h          |    |    |          |                      |              |           |           |
| 15          | 14 | 13 | 12       | 11                   | 10           | 9         | 8         |
| RESERVED_24 |    |    |          |                      |              |           |           |
| R           |    |    |          |                      |              |           |           |
| 0h          |    |    |          |                      |              |           |           |
| 7           | 6  | 5  | 4        | 3                    | 2            | 1         | 0         |
| RESERVED5   |    |    | OE_ERROR | FRAME_TOO_LONG_ERROR | ABORT_DETECT | CRC_ERROR | RESERVED0 |
| R           |    |    | R        | R                    | R            | R         | R         |
| 0h          |    |    | 0h       | 0h                   | 0h           | 0h        | 0h        |

**Table 5-3298. UART\_SFLSR Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                           |
|------|----------------------|------|-------|-----------------------------------------------------------------------|
| 31:8 | RESERVED_24          | R    | 0h    | Reserved                                                              |
| 7:5  | RESERVED5            | R    | 0h    |                                                                       |
| 4    | OE_ERROR             | R    | 0h    | 1 Overrun error in RX FIFO when frame at top of RX FIFO was received. |
| 3    | FRAME_TOO_LONG_ERROR | R    | 0h    | 1 Frame-length too long error in frame at top of RX FIFO.             |
| 2    | ABORT_DETECT         | R    | 0h    | 1 Abort pattern detected in frame at top of RX FIFO                   |

**Table 5-3298. UART\_SFLSR Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description                                                                                 |
|-----|-----------|------|-------|---------------------------------------------------------------------------------------------|
| 1   | CRC_ERROR | R    | 0h    | 1 CRC error in frame at top of RX FIFO. top of RX FIFO = Next frame to be read from RX FIFO |
| 0   | RESERVED0 | R    | 0h    |                                                                                             |

### 5.24.2.29 UART\_TXFLL Register

#### 1 UART\_TXFLL Register (Offset = 28h) [reset = 0h]

IrDA modes only.

The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.

Return to [Summary Table](#)

**Table 5-3299. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0028h       |
| UART1         | 5230 1028h       |
| UART2         | 5230 2028h       |
| UART3         | 5230 3028h       |
| UART4         | 5230 4028h       |
| UART5         | 5230 5028h       |

**Figure 5-1087. UART\_TXFLL Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_24 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_24 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_24 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TXFLL       |    |    |    |    |    |    |    |
| W           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-3301. UART\_TXFLL Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                   |
|------|-------------|------|-------|-----------------------------------------------|
| 31:8 | RESERVED_24 | R    | 0h    | Reserved                                      |
| 7:0  | TXFLL       | W    | 0h    | LSB register used to specify the frame length |

### 5.24.2.30 UART\_RESUME Register

#### 1 UART\_RESUME Register (Offset = 2Ch) [reset = 0h]

IR-IrDA and IR-CIR modes only.

This register is used to clear internal flags, which halt transmission/reception when an underrun/overflow error occurs. Reading this register resumes the halted operation. This register does not physically exist and reads always as 0x00.

Return to [Summary Table](#)

**Table 5-3302. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 002Ch       |
| UART1         | 5230 102Ch       |
| UART2         | 5230 202Ch       |
| UART3         | 5230 302Ch       |
| UART4         | 5230 402Ch       |
| UART5         | 5230 502Ch       |

**Figure 5-1088. UART\_RESUME Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_24 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_24 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_24 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESUME      |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-3304. UART\_RESUME Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                        |
|------|-------------|------|-------|------------------------------------|
| 31:8 | RESERVED_24 | R    | 0h    | Reserved                           |
| 7:0  | RESUME      | R    | 0h    | Dummy read to restart the TX or RX |



### 5.24.2.31 UART\_TXFLH Register

#### 1 UART\_TXFLH Register (Offset = 2Ch) [reset = 0h]

IrDA modes only.

The registers TXFLL and TXFLH hold the 13-bit transmit frame length (expressed in bytes). TXFLL holds the least significant bits and TXFLH holds the most significant bits. The frame length value is used if the frame length method of frame closing is used.

Return to [Summary Table](#)

**Table 5-3305. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 002Ch       |
| UART1         | 5230 102Ch       |
| UART2         | 5230 202Ch       |
| UART3         | 5230 302Ch       |
| UART4         | 5230 402Ch       |
| UART5         | 5230 502Ch       |

**Figure 5-1089. UART\_TXFLH Name Register**

|             |    |    |    |       |    |    |    |
|-------------|----|----|----|-------|----|----|----|
| 31          | 30 | 29 | 28 | 27    | 26 | 25 | 24 |
| RESERVED_24 |    |    |    |       |    |    |    |
| R           |    |    |    |       |    |    |    |
| 0h          |    |    |    |       |    |    |    |
| 23          | 22 | 21 | 20 | 19    | 18 | 17 | 16 |
| RESERVED_24 |    |    |    |       |    |    |    |
| R           |    |    |    |       |    |    |    |
| 0h          |    |    |    |       |    |    |    |
| 15          | 14 | 13 | 12 | 11    | 10 | 9  | 8  |
| RESERVED_24 |    |    |    |       |    |    |    |
| R           |    |    |    |       |    |    |    |
| 0h          |    |    |    |       |    |    |    |
| 7           | 6  | 5  | 4  | 3     | 2  | 1  | 0  |
| RESERVED    |    |    |    | TXFLH |    |    |    |
| R           |    |    |    | W     |    |    |    |
| 0h          |    |    |    | 0h    |    |    |    |

**Table 5-3307. UART\_TXFLH Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                   |
|------|-------------|------|-------|-----------------------------------------------|
| 31:8 | RESERVED_24 | R    | 0h    | Reserved                                      |
| 7:5  | RESERVED    | R    | 0h    |                                               |
| 4:0  | TXFLH       | W    | 0h    | MSB register used to specify the frame length |

### 5.24.2.32 UART\_RXFLL Register

#### 1 UART\_RXFLL Register (Offset = 30h) [reset = 0h]

IrDA modes only.

The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is  $n$  bytes, then program RXFLL and RXFLH to be  $n + 3$  in SIR or MIR modes and  $n + 6$  in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).

Return to [Summary Table](#)

**Table 5-3308. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0030h       |
| UART1         | 5230 1030h       |
| UART2         | 5230 2030h       |
| UART3         | 5230 3030h       |
| UART4         | 5230 4030h       |
| UART5         | 5230 5030h       |

**Figure 5-1090. UART\_RXFLL Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_24 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_24 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_24 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RXFLL       |    |    |    |    |    |    |    |
| W           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-3310. UART\_RXFLL Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                |
|------|-------------|------|-------|------------------------------------------------------------|
| 31:8 | RESERVED_24 | R    | 0h    | Reserved                                                   |
| 7:0  | RXFLL       | W    | 0h    | LSB register used to specify the frame length in reception |

### 5.24.2.33 UART\_SFREGL Register

#### 1 UART\_SFREGL Register (Offset = 30h) [reset = 0h]

IrDA modes only.

The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.

Return to [Summary Table](#)

**Table 5-3311. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0030h       |
| UART1         | 5230 1030h       |
| UART2         | 5230 2030h       |
| UART3         | 5230 3030h       |
| UART4         | 5230 4030h       |
| UART5         | 5230 5030h       |

**Figure 5-1091. UART\_SFREGL Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_24 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_24 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_24 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| SFREGL      |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-3313. UART\_SFREGL Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                  |
|------|-------------|------|-------|------------------------------|
| 31:8 | RESERVED_24 | R    | 0h    | Reserved                     |
| 7:0  | SFREGL      | R    | 0h    | LSB part of the frame length |

### 5.24.2.34 UART\_RXFLH Register

#### 1 UART\_RXFLH Register (Offset = 34h) [reset = 0h]

IrDA modes only.

The registers RXFLL and RXFLH hold the 12-bit receive maximum frame length. RXFLL holds the least significant bits and RXFLH holds the most significant bits. If the intended maximum receive frame length is  $n$  bytes, then program RXFLL and RXFLH to be  $n + 3$  in SIR or MIR modes and  $n + 6$  in FIR mode (+3 and +6 are due to frame format with CRC and stop flag; there are two bytes associated with the FIR stop flag).

Return to [Summary Table](#)

**Table 5-3314. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0034h       |
| UART1         | 5230 1034h       |
| UART2         | 5230 2034h       |
| UART3         | 5230 3034h       |
| UART4         | 5230 4034h       |
| UART5         | 5230 5034h       |

**Figure 5-1092. UART\_RXFLH Name Register**

|             |    |    |    |       |    |    |    |
|-------------|----|----|----|-------|----|----|----|
| 31          | 30 | 29 | 28 | 27    | 26 | 25 | 24 |
| RESERVED_24 |    |    |    |       |    |    |    |
| R           |    |    |    |       |    |    |    |
| 0h          |    |    |    |       |    |    |    |
| 23          | 22 | 21 | 20 | 19    | 18 | 17 | 16 |
| RESERVED_24 |    |    |    |       |    |    |    |
| R           |    |    |    |       |    |    |    |
| 0h          |    |    |    |       |    |    |    |
| 15          | 14 | 13 | 12 | 11    | 10 | 9  | 8  |
| RESERVED_24 |    |    |    |       |    |    |    |
| R           |    |    |    |       |    |    |    |
| 0h          |    |    |    |       |    |    |    |
| 7           | 6  | 5  | 4  | 3     | 2  | 1  | 0  |
| RESERVED    |    |    |    | RXFLH |    |    |    |
| R           |    |    |    | W     |    |    |    |
| 0h          |    |    |    | 0h    |    |    |    |

**Table 5-3316. UART\_RXFLH Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                |
|------|-------------|------|-------|------------------------------------------------------------|
| 31:8 | RESERVED_24 | R    | 0h    | Reserved                                                   |
| 7:4  | RESERVED    | R    | 0h    |                                                            |
| 3:0  | RXFLH       | W    | 0h    | MSB register used to specify the frame length in reception |

### 5.24.2.35 UART\_SFREGH Register

#### 1 UART\_SFREGH Register (Offset = 34h) [reset = 0h]

IrDA modes only.

The frame lengths of received frames are written into the status FIFO. This information can be read by reading the SFREGL and SFREGH registers (i.e. these registers do not physically exist). The least significant bits are read from SFREGL and the most significant bits are read from SFREGH. Reading these registers does not alter the status FIFO read pointer. These registers should be read before the pointer is incremented by reading the SFLSR.

Return to [Summary Table](#)

**Table 5-3317. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0034h       |
| UART1         | 5230 1034h       |
| UART2         | 5230 2034h       |
| UART3         | 5230 3034h       |
| UART4         | 5230 4034h       |
| UART5         | 5230 5034h       |

**Figure 5-1093. UART\_SFREGH Name Register**

|             |    |    |    |        |    |    |    |
|-------------|----|----|----|--------|----|----|----|
| 31          | 30 | 29 | 28 | 27     | 26 | 25 | 24 |
| RESERVED_24 |    |    |    |        |    |    |    |
| R           |    |    |    |        |    |    |    |
| 0h          |    |    |    |        |    |    |    |
| 23          | 22 | 21 | 20 | 19     | 18 | 17 | 16 |
| RESERVED_24 |    |    |    |        |    |    |    |
| R           |    |    |    |        |    |    |    |
| 0h          |    |    |    |        |    |    |    |
| 15          | 14 | 13 | 12 | 11     | 10 | 9  | 8  |
| RESERVED_24 |    |    |    |        |    |    |    |
| R           |    |    |    |        |    |    |    |
| 0h          |    |    |    |        |    |    |    |
| 7           | 6  | 5  | 4  | 3      | 2  | 1  | 0  |
| RESERVED    |    |    |    | SFREGH |    |    |    |
| R           |    |    |    | R      |    |    |    |
| 0h          |    |    |    | 0h     |    |    |    |

**Table 5-3319. UART\_SFREGH Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                  |
|------|-------------|------|-------|------------------------------|
| 31:8 | RESERVED_24 | R    | 0h    | Reserved                     |
| 7:4  | RESERVED    | R    | 0h    |                              |
| 3:0  | SFREGH      | R    | 0h    | MSB part of the frame length |

### 5.24.2.36 UART\_BLR Register

#### 1 UART\_BLR Register (Offset = 38h) [reset = 40h]

IrDA modes only.

Note that BLR[6] is used to select whether 0xC0 or 0xFF start patterns are to be used, when multiple start flags are required in SIR Mode. If only one start flag is required, this will always be 0xC0. If n start flags are required, then either (n-1) 0xC0 or (n-1) 0xFF flags are sent, followed by a single 0xC0 flag (immediately preceding the first data byte).

Return to [Summary Table](#)

**Table 5-3320. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0038h       |
| UART1         | 5230 1038h       |
| UART2         | 5230 2038h       |
| UART3         | 5230 3038h       |
| UART4         | 5230 4038h       |
| UART5         | 5230 5038h       |

**Figure 5-1094. UART\_BLR Name Register**

|                    |           |          |    |    |    |    |    |
|--------------------|-----------|----------|----|----|----|----|----|
| 31                 | 30        | 29       | 28 | 27 | 26 | 25 | 24 |
| RESERVED_24        |           |          |    |    |    |    |    |
| R                  |           |          |    |    |    |    |    |
| 0h                 |           |          |    |    |    |    |    |
| 23                 | 22        | 21       | 20 | 19 | 18 | 17 | 16 |
| RESERVED_24        |           |          |    |    |    |    |    |
| R                  |           |          |    |    |    |    |    |
| 0h                 |           |          |    |    |    |    |    |
| 15                 | 14        | 13       | 12 | 11 | 10 | 9  | 8  |
| RESERVED_24        |           |          |    |    |    |    |    |
| R                  |           |          |    |    |    |    |    |
| 0h                 |           |          |    |    |    |    |    |
| 7                  | 6         | 5        | 4  | 3  | 2  | 1  | 0  |
| STS_FIFO_RE<br>SET | XBOF_TYPE | RESERVED |    |    |    |    |    |
| R/W1TS             | R/W       | R        |    |    |    |    |    |
| 0h                 | 1h        | 0h       |    |    |    |    |    |

**Table 5-3322. UART\_BLR Register Field Descriptions**

| Bit  | Field          | Type   | Reset | Description                                  |
|------|----------------|--------|-------|----------------------------------------------|
| 31:8 | RESERVED_24    | R      | 0h    | Reserved                                     |
| 7    | STS_FIFO_RESET | R/W1TS | 0h    | Status FIFO reset. This bit is self-clearing |
| 6    | XBOF_TYPE      | R/W    | 1h    | SIR xBOF select.<br>0 0xFF<br>1 0xC0         |
| 5:0  | RESERVED       | R      | 0h    |                                              |

### 5.24.2.37 UART\_UASR Register

#### 1 UART\_UASR Register (Offset = 38h) [reset = 0h]

UART Autobauding Status Register.

Return to [Summary Table](#)

**Table 5-3323. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0038h       |
| UART1         | 5230 1038h       |
| UART2         | 5230 2038h       |
| UART3         | 5230 3038h       |
| UART4         | 5230 4038h       |
| UART5         | 5230 5038h       |

**Figure 5-1095. UART\_UASR Name Register**

|             |    |             |    |       |    |    |    |
|-------------|----|-------------|----|-------|----|----|----|
| 31          | 30 | 29          | 28 | 27    | 26 | 25 | 24 |
| RESERVED    |    |             |    |       |    |    |    |
| NONE        |    |             |    |       |    |    |    |
| 0h          |    |             |    |       |    |    |    |
| 23          | 22 | 21          | 20 | 19    | 18 | 17 | 16 |
| RESERVED    |    |             |    |       |    |    |    |
| NONE        |    |             |    |       |    |    |    |
| 0h          |    |             |    |       |    |    |    |
| 15          | 14 | 13          | 12 | 11    | 10 | 9  | 8  |
| RESERVED    |    |             |    |       |    |    |    |
| NONE        |    |             |    |       |    |    |    |
| 0h          |    |             |    |       |    |    |    |
| 7           | 6  | 5           | 4  | 3     | 2  | 1  | 0  |
| PARITY_TYPE |    | BIT_BY_CHAR |    | SPEED |    |    |    |
| R           |    | R           |    | R     |    |    |    |
| 0h          |    | 0h          |    | 0h    |    |    |    |

**Table 5-3325. UART\_UASR Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                                                                                                                                            |
|------|-------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED    | NONE | 0h    | Reserved                                                                                                                                                                                                                                                                               |
| 7:6  | PARITY_TYPE | R    | 0h    | 00 => No Parity identified. 01 => Parity space. 10 => Even Parity. 11 => Odd Parity                                                                                                                                                                                                    |
| 5    | BIT_BY_CHAR | R    | 0h    | 0 => 7 bits character identified. 1 => 8 bits character identified                                                                                                                                                                                                                     |
| 4:0  | SPEED       | R    | 0h    | Used to report the speed identified. 00000 => No speed identified. 00001 => 115200 bauds. 00010 => 57600 bauds. 00011 => 38400 bauds. 00100 => 28800 bauds. 00101 => 19200 bauds. 00110 => 14400 bauds. 00111 => 9600bauds. 01000 => 4800bauds. 01001 => 2400bauds. 01010 => 1200bauds |

### 5.24.2.38 UART\_ACREG Register

#### 1 UART\_ACREG Register (Offset = 3Ch) [reset = 0h]

IR-IrDA and IR-CIR modes only.

Return to [Summary Table](#)

**Table 5-3326. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 003Ch       |
| UART1         | 5230 103Ch       |
| UART2         | 5230 203Ch       |
| UART3         | 5230 303Ch       |
| UART4         | 5230 403Ch       |
| UART5         | 5230 503Ch       |

**Figure 5-1096. UART\_ACREG Name Register**

|             |        |           |                     |          |         |          |        |
|-------------|--------|-----------|---------------------|----------|---------|----------|--------|
| 31          | 30     | 29        | 28                  | 27       | 26      | 25       | 24     |
| RESERVED_24 |        |           |                     |          |         |          |        |
| R           |        |           |                     |          |         |          |        |
| 0h          |        |           |                     |          |         |          |        |
| 23          | 22     | 21        | 20                  | 19       | 18      | 17       | 16     |
| RESERVED_24 |        |           |                     |          |         |          |        |
| R           |        |           |                     |          |         |          |        |
| 0h          |        |           |                     |          |         |          |        |
| 15          | 14     | 13        | 12                  | 11       | 10      | 9        | 8      |
| RESERVED_24 |        |           |                     |          |         |          |        |
| R           |        |           |                     |          |         |          |        |
| 0h          |        |           |                     |          |         |          |        |
| 7           | 6      | 5         | 4                   | 3        | 2       | 1        | 0      |
| PULSE_TYPE  | SD_MOD | DIS_IR_RX | DIS_TX_UNDE<br>RRUN | SEND_SIP | SCTX_EN | ABORT_EN | EOT_EN |
| R/W         | R/W    | R/W       | R/W                 | R/W1TS   | R/W1TS  | R/W      | R/W1TS |
| 0h          | 0h     | 0h        | 0h                  | 0h       | 0h      | 0h       | 0h     |

**Table 5-3328. UART\_ACREG Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                                                                                                  |
|------|-------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED_24 | R    | 0h    | Reserved                                                                                                                                                                                     |
| 7    | PULSE_TYPE  | R/W  | 0h    | SIR pulse width select:<br>0 3/16 of baud-rate pulse width<br>1 1.6us                                                                                                                        |
| 6    | SD_MOD      | R/W  | 0h    | Primary output used to configure transceivers. Connected to the SD/<br>MODE input pin of IrDA transceivers.<br>0 SD pin is set to high<br>1 SD pin is set to low                             |
| 5    | DIS_IR_RX   | R/W  | 0h    | 0 Normal operation (RX input automatically<br>disabled during transmit but enabled<br>outside of transmit operation).<br>1 Disables RX input (permanent state -<br>independent of transmit). |



**Table 5-3328. UART\_ACREG Register Field Descriptions (continued)**

| Bit | Field           | Type   | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                     |
|-----|-----------------|--------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | DIS_TX_UNDERRUN | R/W    | 0h    | <p>It is recommended to disable TX FIFO underrun capability by masking corresponding underrun interrupt. When disabling underrun by setting ACREG[4]=1, garbage data is sent over TX line.</p> <p>0 Long stop bits cannot be transmitted, TX underrun is enabled</p> <p>1 Long stop bits can be transmitted, TX underrun is disabled</p>                                                        |
| 3   | SEND_SIP        | R/W1TS | 0h    | <p>MIR/FIR Modes only. Send Serial Infrared Interaction Pulse [SIP] If this bit is set during a MIR/FIR transmission, the SIP will be send at the end of it. This bit automatically gets cleared at the end of the SIP transmission.</p> <p>0 No action</p> <p>1 Send SIP pulse.</p>                                                                                                            |
| 2   | SCTX_EN         | R/W1TS | 0h    | <p>Store and controlled TX start. When MDR1[5] = 1 and the LH writes 1 to this bit the TX state machine starts frame transmission. This bit is self-clearing.</p>                                                                                                                                                                                                                               |
| 1   | ABORT_EN        | R/W    | 0h    | <p>Frame Abort. The LH can intentionally abort transmission of a frame by Writing 1 to this bit. Neither the end flag nor the CRC bits are appended to the frame.</p> <p>If transmit FIFO is not empty and MDR1[5]=1, UART IrDA will start a new transfer with data of previous frame as soon as abort frame has been sent. Therefore, TX FIFO must be reset before sending an abort frame.</p> |
| 0   | EOT_EN          | R/W1TS | 0h    | <p>EOT [end of transmission] bit. The LH writes 1 to this bit just before it writes the last byte to the TX FIFO in set-EOT bit frame closing method. This bit automatically gets cleared when the LH writes to the THR [TX FIFO].</p>                                                                                                                                                          |

### 5.24.2.39 UART\_SCR Register

#### 1 UART\_SCR Register (Offset = 40h) [reset = 0h]

Note: Bit 4 enables the wake-up interrupt, but this interrupt is not mapped into the IIR register. Therefore, when an interrupt occurs and there is no interrupt pending in the IIR register, the SSR[1] bit must be checked. To clear the wake-up interrupt, bit SCR[4] must be reset to 0.

Return to [Summary Table](#)

**Table 5-3329. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0040h       |
| UART1         | 5230 1040h       |
| UART2         | 5230 2040h       |
| UART3         | 5230 3040h       |
| UART4         | 5230 4040h       |
| UART5         | 5230 5040h       |

**Figure 5-1097. UART\_SCR Name Register**

|                    |                    |        |                                   |                     |            |    |                  |
|--------------------|--------------------|--------|-----------------------------------|---------------------|------------|----|------------------|
| 31                 | 30                 | 29     | 28                                | 27                  | 26         | 25 | 24               |
| RESERVED_24        |                    |        |                                   |                     |            |    |                  |
| R                  |                    |        |                                   |                     |            |    |                  |
| 0h                 |                    |        |                                   |                     |            |    |                  |
| 23                 | 22                 | 21     | 20                                | 19                  | 18         | 17 | 16               |
| RESERVED_24        |                    |        |                                   |                     |            |    |                  |
| R                  |                    |        |                                   |                     |            |    |                  |
| 0h                 |                    |        |                                   |                     |            |    |                  |
| 15                 | 14                 | 13     | 12                                | 11                  | 10         | 9  | 8                |
| RESERVED_24        |                    |        |                                   |                     |            |    |                  |
| R                  |                    |        |                                   |                     |            |    |                  |
| 0h                 |                    |        |                                   |                     |            |    |                  |
| 7                  | 6                  | 5      | 4                                 | 3                   | 2          | 1  | 0                |
| RX_TRIG_GRA<br>NU1 | TX_TRIG_GRA<br>NU1 | DSR_IT | RX_CTS_DSR_<br>WAKE_UP_EN<br>ABLE | TX_EMPTY_CT<br>L_IT | DMA_MODE_2 |    | DMA_MODE_C<br>TL |
| R/W                | R/W                | R/W    | R/W                               | R/W                 | R/W        |    | R/W              |
| 0h                 | 0h                 | 0h     | 0h                                | 0h                  | 0h         |    | 0h               |

**Table 5-3331. UART\_SCR Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                                   |
|------|----------------|------|-------|---------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED_24    | R    | 0h    | Reserved                                                                                                      |
| 7    | RX_TRIG_GRANU1 | R/W  | 0h    | 0 DISABLES THE GRANULARITY OF 1 FOR TRIGGER RX LEVEL.<br>1 ENABLES THE GRANULARITY OF 1 FOR TRIGGER RX LEVEL. |
| 6    | TX_TRIG_GRANU1 | R/W  | 0h    | 0 DISABLES THE GRANULARITY OF 1 FOR TRIGGER TX LEVEL.<br>1 Enables the granularity of 1 for trigger TX level. |
| 5    | DSR_IT         | R/W  | 0h    | 0 DISABLES DSR* INTERRUPT.<br>1 ENABLES DSR* INTERRUPT.                                                       |

**Table 5-3331. UART\_SCR Register Field Descriptions (continued)**

| Bit | Field                     | Type | Reset | Description                                                                                                                                                                                                                                      |
|-----|---------------------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | RX_CTS_DSR_WAKE_UP_ENABLE | R/W  | 0h    | 0      DISABLES THE WAKE UP INTERRUPT AND CLEARS SSR[1].<br>1      waits for a falling edge of pins RX, CTS* or DSR* to generate an interrupt                                                                                                    |
| 3   | TX_EMPTY_CTL_IT           | R/W  | 0h    | 0      Normal mode for THR interrupt (See UART mode interrupts table).<br>1      THE THR INTERRUPT IS GENERATED WHEN TX FIFO AND TX SHIFT REGISTER ARE EMPTY.                                                                                    |
| 2:1 | DMA_MODE_2                | R/W  | 0h    | Used to specify the DMA mode valid if SCR[0] = 1<br>0      DMA mode 0 (no DMA)<br>1      DMA mode 1 (UART_nDMA_REQ[0] in TX, UART_nDMA_REQ[1] in RX)<br>2      DMA mode 2 (UART_nDMA_REQ[0] in RX)<br>3      DMA mode 3 (UART_nDMA_REQ[0] in TX) |
| 0   | DMA_MODE_CTL              | R/W  | 0h    | 0      The DMA_MODE is set with FCR[3]<br>1      The DMA_MODE is set with SCR[2:1]                                                                                                                                                               |

#### 5.24.2.40 UART\_SSR Register

##### 1 UART\_SSR Register (Offset = 44h) [reset = 4h]

Note: Bit 1 is reset only when SCR[4] is reset to 0.

Return to [Summary Table](#)

**Table 5-3332. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0044h       |
| UART1         | 5230 1044h       |
| UART2         | 5230 2044h       |
| UART3         | 5230 3044h       |
| UART4         | 5230 4044h       |
| UART5         | 5230 5044h       |

**Figure 5-1098. UART\_SSR Name Register**

|             |    |    |    |    |                    |                                |              |
|-------------|----|----|----|----|--------------------|--------------------------------|--------------|
| 31          | 30 | 29 | 28 | 27 | 26                 | 25                             | 24           |
| RESERVED_24 |    |    |    |    |                    |                                |              |
| R           |    |    |    |    |                    |                                |              |
| 0h          |    |    |    |    |                    |                                |              |
| 23          | 22 | 21 | 20 | 19 | 18                 | 17                             | 16           |
| RESERVED_24 |    |    |    |    |                    |                                |              |
| R           |    |    |    |    |                    |                                |              |
| 0h          |    |    |    |    |                    |                                |              |
| 15          | 14 | 13 | 12 | 11 | 10                 | 9                              | 8            |
| RESERVED_24 |    |    |    |    |                    |                                |              |
| R           |    |    |    |    |                    |                                |              |
| 0h          |    |    |    |    |                    |                                |              |
| 7           | 6  | 5  | 4  | 3  | 2                  | 1                              | 0            |
| RESERVED    |    |    |    |    | DMA_COUNT<br>R_RST | RX_CTS_DSR_<br>WAKE_UP_ST<br>S | TX_FIFO_FULL |
| R           |    |    |    |    | R/W                | R                              | R            |
| 0h          |    |    |    |    | 1h                 | 0h                             | 0h           |

**Table 5-3334. UART\_SSR Register Field Descriptions**

| Bit  | Field                      | Type | Reset | Description                                                                                                                                                                            |
|------|----------------------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED_24                | R    | 0h    | Reserved                                                                                                                                                                               |
| 7:3  | RESERVED                   | R    | 0h    |                                                                                                                                                                                        |
| 2    | DMA_COUNTER_RST            | R/W  | 1h    | 0 The DMA counter will not be reset if the corresponding FIFO is reset (via FCR[1] or FCR[2])<br>1 The DMA counter will be reset if corresponding FIFO is reset (via FCR[1] or FCR[2]) |
| 1    | RX_CTS_DSR_WAKE_U<br>P_STS | R    | 0h    | 0 No falling edge event on RX, CTS* and DSR*<br>1 A falling edge occurred on RX, CTS* or DSR*                                                                                          |
| 0    | TX_FIFO_FULL               | R    | 0h    | 0 TX FIFO is not full<br>1 TX FIFO is full.                                                                                                                                            |

### 5.24.2.41 UART\_EBLR Register

#### 1 UART\_EBLR Register (Offset = 48h) [reset = 0h]

IR-IrDA and IR-CIR modes only.

In IR-IrDA SIR operation, this register specifies the number of BOF + xBOFs to transmit. Value set into this register must take into account the BOF character, therefore to only sent one BOF with no XBOF this register must be set to 1. To send one BOF with N XBOF this register must be set to N+1. Furthermore, the value 0 will send 1 BOF plus 255 XBOF.

In IR-IrDA MIR mode, this register specifies the number of additional start flags (MIR protocol mandates a minimum of 2 start flags).

In IR-CIR mode, this register specifies the number of consecutive zeros to be received before generating the RX\_STOP interrupt (IIR[2]). All the received zeros are stored in the RX FIFO. When the register is set to 0, this feature is de-activated and always in reception state which can be disabled by setting the ACREG[5] to.

Return to [Summary Table](#)

**Table 5-3335. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0048h       |
| UART1         | 5230 1048h       |
| UART2         | 5230 2048h       |
| UART3         | 5230 3048h       |
| UART4         | 5230 4048h       |
| UART5         | 5230 5048h       |

**Figure 5-1099. UART\_EBLR Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_24 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_24 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_24 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| EBLR        |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |

**Table 5-3337. UART\_EBLR Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description |
|------|-------------|------|-------|-------------|
| 31:8 | RESERVED_24 | R    | 0h    | Reserved    |

**Table 5-3337. UART\_EBLR Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | EBLR  | R/W  | 0h    | <p>IR-IRDA mode: This register allows to define up to 176 xBOFs, the maximum required by IrDA specification.</p> <p>IR-CIR mode: This register specifies the number of consecutive zeros to be received before generating the RX_STOP interrupt [IIR[2]].</p> <p>0x00: feature disabled.</p> <p>0x01: generate RX_STOP interrupt after receiving one zero bit.</p> <p>...</p> <p>0xFF: generate RX_STOP interrupt after receiving 255 zero bits.</p> |

#### 5.24.2.42 UART\_MVR Register

##### 1 UART\_MVR Register (Offset = 50h) [reset = 47424E03h]

The reset value is fixed by hardware and corresponds to the RTL revision of this module. A reset has no effect on the value returned

Notes:

UART / IRDA SIR only module is revision 1.x (WMU\_012\_1 specification).

UART / IRDA with SIR, MIR and FIR support is revision 2.x (WMU\_012\_2 specification).

UART / IRDA with SIR, MIR and FIR / CIR support is revision 3.x (this specification).

For example: MVR = 0x30 => Version 3.0 MVR = 0x38 => Version 3.8

Return to [Summary Table](#)

**Table 5-3338. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0050h       |
| UART1         | 5230 1050h       |
| UART2         | 5230 2050h       |
| UART3         | 5230 3050h       |
| UART4         | 5230 4050h       |
| UART5         | 5230 5050h       |

**Figure 5-1100. UART\_MVR Name Register**

|        |    |          |    |       |    |    |    |
|--------|----|----------|----|-------|----|----|----|
| 31     | 30 | 29       | 28 | 27    | 26 | 25 | 24 |
| SCHEME |    | RESERVED |    | FUNC  |    |    |    |
| R      |    | R        |    | R     |    |    |    |
| 1h     |    | 0h       |    | 742h  |    |    |    |
| 23     | 22 | 21       | 20 | 19    | 18 | 17 | 16 |
| FUNC   |    |          |    |       |    |    |    |
| R      |    |          |    |       |    |    |    |
| 742h   |    |          |    |       |    |    |    |
| 15     | 14 | 13       | 12 | 11    | 10 | 9  | 8  |
| RTL    |    |          |    | MAJOR |    |    |    |
| R      |    |          |    | R     |    |    |    |
| 9h     |    |          |    | 6h    |    |    |    |
| 7      | 6  | 5        | 4  | 3     | 2  | 1  | 0  |
| CUSTOM |    | MINOR    |    |       |    |    |    |
| R      |    | R        |    |       |    |    |    |
| 0h     |    | 3h       |    |       |    |    |    |

**Table 5-3340. UART\_MVR Register Field Descriptions**

| Bit   | Field    | Type | Reset | Description                           |
|-------|----------|------|-------|---------------------------------------|
| 31:30 | SCHEME   | R    | 1h    | Scheme revision number of module      |
| 29:28 | RESERVED | R    | 0h    | Reserved                              |
| 27:16 | FUNC     | R    | 742h  | Function revision number of module    |
| 15:11 | RTL      | R    | 9h    | Rtl revision number of module         |
| 10:8  | MAJOR    | R    | 6h    | Major revision number of the module.  |
| 7:6   | CUSTOM   | R    | 0h    | Custom revision number of the module. |
| 5:0   | MINOR    | R    | 3h    | Minor revision number of the module.  |

### 5.24.2.43 UART\_SYSS Register

#### 1 UART\_SYSS Register (Offset = 58h) [reset = 0h]

Return to [Summary Table](#)

**Table 5-3341. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0058h       |
| UART1         | 5230 1058h       |
| UART2         | 5230 2058h       |
| UART3         | 5230 3058h       |
| UART4         | 5230 4058h       |
| UART5         | 5230 5058h       |

**Figure 5-1101. UART\_SYSS Name Register**

|             |    |    |    |    |    |    |           |
|-------------|----|----|----|----|----|----|-----------|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24        |
| RESERVED_24 |    |    |    |    |    |    |           |
| R           |    |    |    |    |    |    |           |
| 0h          |    |    |    |    |    |    |           |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16        |
| RESERVED_24 |    |    |    |    |    |    |           |
| R           |    |    |    |    |    |    |           |
| 0h          |    |    |    |    |    |    |           |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8         |
| RESERVED_24 |    |    |    |    |    |    |           |
| R           |    |    |    |    |    |    |           |
| 0h          |    |    |    |    |    |    |           |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0         |
| RESERVED    |    |    |    |    |    |    | RESETDONE |
| R           |    |    |    |    |    |    | R         |
| 0h          |    |    |    |    |    |    | 0h        |

**Table 5-3343. UART\_SYSS Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                          |
|------|-------------|------|-------|--------------------------------------------------------------------------------------|
| 31:8 | RESERVED_24 | R    | 0h    | Reserved                                                                             |
| 7:1  | RESERVED    | R    | 0h    |                                                                                      |
| 0    | RESETDONE   | R    | 0h    | Internal Reset Monitoring<br>0 Internal Module Reset is ongoing<br>1 Reset completed |



#### 5.24.2.44 UART\_WER Register

##### 1 UART\_WER Register (Offset = 5Ch) [reset = FFh]

The UART wakeup enable register is used to mask and unmask a UART event that would subsequently notify the system. The events are any activity in the logic that could cause an interrupt and/ or an activity that would require the system to wakeup. It should be noted that even if the wakeup is disabled for certain events, if these events are also an interrupt to the UART, then the UART will still register the interrupt as such.

Return to [Summary Table](#)

**Table 5-3344. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 005Ch       |
| UART1         | 5230 105Ch       |
| UART2         | 5230 205Ch       |
| UART3         | 5230 305Ch       |
| UART4         | 5230 405Ch       |
| UART5         | 5230 505Ch       |

**Figure 5-1102. UART\_WER Name Register**

|                      |                                        |                       |                     |                         |                    |                      |                      |
|----------------------|----------------------------------------|-----------------------|---------------------|-------------------------|--------------------|----------------------|----------------------|
| 31                   | 30                                     | 29                    | 28                  | 27                      | 26                 | 25                   | 24                   |
| RESERVED_24          |                                        |                       |                     |                         |                    |                      |                      |
| R                    |                                        |                       |                     |                         |                    |                      |                      |
| 0h                   |                                        |                       |                     |                         |                    |                      |                      |
| 23                   | 22                                     | 21                    | 20                  | 19                      | 18                 | 17                   | 16                   |
| RESERVED_24          |                                        |                       |                     |                         |                    |                      |                      |
| R                    |                                        |                       |                     |                         |                    |                      |                      |
| 0h                   |                                        |                       |                     |                         |                    |                      |                      |
| 15                   | 14                                     | 13                    | 12                  | 11                      | 10                 | 9                    | 8                    |
| RESERVED_24          |                                        |                       |                     |                         |                    |                      |                      |
| R                    |                                        |                       |                     |                         |                    |                      |                      |
| 0h                   |                                        |                       |                     |                         |                    |                      |                      |
| 7                    | 6                                      | 5                     | 4                   | 3                       | 2                  | 1                    | 0                    |
| EVENT_7_TX_WAKEUP_EN | EVENT_6_RECEIVER_LINE_STATUS_INTERRUPT | EVENT_5_RHR_INTERRUPT | EVENT_4_RX_ACTIVITY | EVENT_3_DCD_CD_ACTIVITY | EVENT_2_RIACTIVITY | EVENT_1_DSR_ACTIVITY | EVENT_0_CTS_ACTIVITY |
| R/W                  | R/W                                    | R/W                   | R/W                 | R/W                     | R/W                | R/W                  | R/W                  |
| 1h                   | 1h                                     | 1h                    | 1h                  | 1h                      | 1h                 | 1h                   | 1h                   |

**Table 5-3346. UART\_WER Register Field Descriptions**

| Bit  | Field                                  | Type | Reset | Description                                                                                                                               |
|------|----------------------------------------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED_24                            | R    | 0h    | Reserved                                                                                                                                  |
| 7    | EVENT_7_TX_WAKEUP_EN                   | R/W  | 1h    | 0 Event is not allowed to wake up the system<br>1 EVENT CAN WAKE UP THE SYSTEM: Event can be: THR_IT or TX_DMA request and/or TX_SATUS_IT |
| 6    | EVENT_6_RECEIVER_LINE_STATUS_INTERRUPT | R/W  | 1h    | 0 Event is not allowed to wake up the system<br>1 Event can wake up the system                                                            |
| 5    | EVENT_5_RHR_INTERRUPT                  | R/W  | 1h    | 0 Event is not allowed to wake up the system<br>1 Event can wake up the system                                                            |

**Table 5-3346. UART\_WER Register Field Descriptions (continued)**

| Bit | Field                   | Type | Reset | Description                                                                    |
|-----|-------------------------|------|-------|--------------------------------------------------------------------------------|
| 4   | EVENT_4_RX_ACTIVITY     | R/W  | 1h    | 0 Event is not allowed to wake up the system<br>1 Event can wake up the system |
| 3   | EVENT_3_DCD_CD_ACTIVITY | R/W  | 1h    | 0 Event is not allowed to wake up the system<br>1 Event can wake up the system |
| 2   | EVENT_2_RI_ACTIVITY     | R/W  | 1h    | 0 Event is not allowed to wake up the system<br>1 Event can wake up the system |
| 1   | EVENT_1_DSR_ACTIVITY    | R/W  | 1h    | 0 Event is not allowed to wake up the system<br>1 Event can wake up the system |
| 0   | EVENT_0_CTS_ACTIVITY    | R/W  | 1h    | 0 Event is not allowed to wake up the system<br>1 Event can wake up the system |

### 5.24.2.45 UART\_CFPS Register

#### 1 UART\_CFPS Register (Offset = 60h) [reset = 69h]

Since the Consumer IR works at modulation rates of 30 56.8 KHz, the 48 MHz clock must be pre scaled before the clock can drive the IR logic. This register sets the divisor rate to give a range to accommodate the remote control requirements in BAUD multiples of 12x. The value of the CFPS at reset is 0105 decimal which equates to a 38.1 KHz output from starting conditions. The 48 MHz carrier is prescaled by the CFPS which is then divided by the 12x BAUD multiple.

Return to [Summary Table](#)

**Table 5-3347. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0060h       |
| UART1         | 5230 1060h       |
| UART2         | 5230 2060h       |
| UART3         | 5230 3060h       |
| UART4         | 5230 4060h       |
| UART5         | 5230 5060h       |

**Figure 5-1103. UART\_CFPS Name Register**

|             |    |    |    |    |    |    |    |
|-------------|----|----|----|----|----|----|----|
| 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED_24 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 23          | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED_24 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 15          | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED_24 |    |    |    |    |    |    |    |
| R           |    |    |    |    |    |    |    |
| 0h          |    |    |    |    |    |    |    |
| 7           | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CFPS        |    |    |    |    |    |    |    |
| R/W         |    |    |    |    |    |    |    |
| 69h         |    |    |    |    |    |    |    |

**Table 5-3349. UART\_CFPS Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description |
|------|-------------|------|-------|-------------|
| 31:8 | RESERVED_24 | R    | 0h    | Reserved    |

**Table 5-3349. UART\_CFPS Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                  |
|-----|-------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | CFPS  | R/W  | 69h   | <p>System clock frequency prescaler at [12x multiple]. Examples for CFPS values are given in the table below.</p> <p>Target Freq [KHz] CFPS [decimal] Actual Freq[KHz]</p> <p>30 133 30.08</p> <p>32.75 122 32.79</p> <p>36 111 36.04</p> <p>36.7 109 36.69</p> <p>38* 105 38.1</p> <p>40 100 40</p> <p>56.8 70 57.14</p> <p>* configured at reset to this value</p> <p>Note: CFPS = 0 is not supported.</p> |

### 5.24.2.46 UART\_RXFIFO\_LVL Register

#### 1 UART\_RXFIFO\_LVL Register (Offset = 64h) [reset = 0h]

Level of the RX FIFO.

Return to [Summary Table](#)

**Table 5-3350. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0064h       |
| UART1         | 5230 1064h       |
| UART2         | 5230 2064h       |
| UART3         | 5230 3064h       |
| UART4         | 5230 4064h       |
| UART5         | 5230 5064h       |

**Figure 5-1104. UART\_RXFIFO\_LVL Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED24 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED24 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED24 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RXFIFO_LVL |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-3352. UART\_RXFIFO\_LVL Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description |
|------|------------|------|-------|-------------|
| 31:8 | RESERVED24 | R    | 0h    | Reserved    |
| 7:0  | RXFIFO_LVL | R    | 0h    |             |

### 5.24.2.47 UART\_TXFIFO\_LVL Register

#### 1 UART\_TXFIFO\_LVL Register (Offset = 68h) [reset = 0h]

Level of the TX FIFO.

Return to [Summary Table](#)

**Table 5-3353. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0068h       |
| UART1         | 5230 1068h       |
| UART2         | 5230 2068h       |
| UART3         | 5230 3068h       |
| UART4         | 5230 4068h       |
| UART5         | 5230 5068h       |

**Figure 5-1105. UART\_TXFIFO\_LVL Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED24 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED24 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED24 |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TXFIFO_LVL |    |    |    |    |    |    |    |
| R          |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-3355. UART\_TXFIFO\_LVL Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description |
|------|------------|------|-------|-------------|
| 31:8 | RESERVED24 | R    | 0h    | Reserved    |
| 7:0  | TXFIFO_LVL | R    | 0h    |             |

### 5.24.2.48 UART\_IER2 Register

#### 1 UART\_IER2 Register (Offset = 6Ch) [reset = 0h]

Enables RX/TX FIFOs empty corresponding interrupts.

Return to [Summary Table](#)

**Table 5-3356. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 006Ch       |
| UART1         | 5230 106Ch       |
| UART2         | 5230 206Ch       |
| UART3         | 5230 306Ch       |
| UART4         | 5230 406Ch       |
| UART5         | 5230 506Ch       |

**Figure 5-1106. UART\_IER2 Name Register**

|           |    |    |    |    |            |                 |                 |
|-----------|----|----|----|----|------------|-----------------|-----------------|
| 31        | 30 | 29 | 28 | 27 | 26         | 25              | 24              |
| RESERVED1 |    |    |    |    |            |                 |                 |
| R         |    |    |    |    |            |                 |                 |
| 0h        |    |    |    |    |            |                 |                 |
| 23        | 22 | 21 | 20 | 19 | 18         | 17              | 16              |
| RESERVED1 |    |    |    |    |            |                 |                 |
| R         |    |    |    |    |            |                 |                 |
| 0h        |    |    |    |    |            |                 |                 |
| 15        | 14 | 13 | 12 | 11 | 10         | 9               | 8               |
| RESERVED1 |    |    |    |    |            |                 |                 |
| R         |    |    |    |    |            |                 |                 |
| 0h        |    |    |    |    |            |                 |                 |
| 7         | 6  | 5  | 4  | 3  | 2          | 1               | 0               |
| RESERVED  |    |    |    |    | RHR_IT_DIS | EN_TXFIFO_EMPTY | EN_RXFIFO_EMPTY |
| R         |    |    |    |    | R/W        | R/W             | R/W             |
| 0h        |    |    |    |    | 0h         | 0h              | 0h              |

**Table 5-3358. UART\_IER2 Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description                                                   |
|------|-----------------|------|-------|---------------------------------------------------------------|
| 31:8 | RESERVED1       | R    | 0h    |                                                               |
| 7:3  | RESERVED        | R    | 0h    |                                                               |
| 2    | RHR_IT_DIS      | R/W  | 0h    | 0 Enables the RHR interrupt.<br>1 Disables the RHR interrupt. |
| 1    | EN_TXFIFO_EMPTY | R/W  | 0h    | Enables[1]/DISABLES[0] EN_TXFIFO_EMPTY interrupt.             |
| 0    | EN_RXFIFO_EMPTY | R/W  | 0h    | Enables[1]/disables[0] EN_RXFIFO_EMPTY interrupt.             |

### 5.24.2.49 UART\_ISR2 Register

#### 1 UART\_ISR2 Register (Offset = 70h) [reset = 3h]

Status of RX/TX FIFOs empty corresponding interrupts.

Return to [Summary Table](#)

**Table 5-3359. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0070h       |
| UART1         | 5230 1070h       |
| UART2         | 5230 2070h       |
| UART3         | 5230 3070h       |
| UART4         | 5230 4070h       |
| UART5         | 5230 5070h       |

**Figure 5-1107. UART\_ISR2 Name Register**

|           |    |    |    |    |    |                  |                  |
|-----------|----|----|----|----|----|------------------|------------------|
| 31        | 30 | 29 | 28 | 27 | 26 | 25               | 24               |
| RESERVED1 |    |    |    |    |    |                  |                  |
| R         |    |    |    |    |    |                  |                  |
| 0h        |    |    |    |    |    |                  |                  |
| 23        | 22 | 21 | 20 | 19 | 18 | 17               | 16               |
| RESERVED1 |    |    |    |    |    |                  |                  |
| R         |    |    |    |    |    |                  |                  |
| 0h        |    |    |    |    |    |                  |                  |
| 15        | 14 | 13 | 12 | 11 | 10 | 9                | 8                |
| RESERVED1 |    |    |    |    |    |                  |                  |
| R         |    |    |    |    |    |                  |                  |
| 0h        |    |    |    |    |    |                  |                  |
| 7         | 6  | 5  | 4  | 3  | 2  | 1                | 0                |
| RESERVED  |    |    |    |    |    | TXFIFO_EMPTY_STS | RXFIFO_EMPTY_STS |
| R         |    |    |    |    |    | R/W1TC           | R/W1TC           |
| 0h        |    |    |    |    |    | 1h               | 1h               |

**Table 5-3361. UART\_ISR2 Register Field Descriptions**

| Bit  | Field            | Type   | Reset | Description                                                                                            |
|------|------------------|--------|-------|--------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED1        | R      | 0h    | Reserved                                                                                               |
| 7:2  | RESERVED         | R      | 0h    | Reserved                                                                                               |
| 1    | TXFIFO_EMPTY_STS | R/W1TC | 1h    | TXFIFO interrupt pending<br>0 TXFIFO_EMPTY interrupt not pending.<br>1 TXFIFO_EMPTY interrupt pending. |
| 0    | RXFIFO_EMPTY_STS | R/W1TC | 1h    | RXFIFO interrupt pending<br>0 RXFIFO_EMPTY interrupt not pending.<br>1 RXFIFO_EMPTY interrupt pending. |



### 5.24.2.50 UART\_FREQ\_SEL Register

#### 1 UART\_FREQ\_SEL Register (Offset = 74h) [reset = 1Ah]

Sample per bit value selector.

Return to [Summary Table](#)

**Table 5-3362. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0074h       |
| UART1         | 5230 1074h       |
| UART2         | 5230 2074h       |
| UART3         | 5230 3074h       |
| UART4         | 5230 4074h       |
| UART5         | 5230 5074h       |

**Figure 5-1108. UART\_FREQ\_SEL Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED2 |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED2 |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED2 |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FREQ_SEL  |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 1Ah       |    |    |    |    |    |    |    |

**Table 5-3364. UART\_FREQ\_SEL Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                 |
|------|-----------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED2 | R    | 0h    | RESERVED                                                                                                                                    |
| 7:0  | FREQ_SEL  | R/W  | 1Ah   | Sets the sample per bit if non default frequency is used. MDR3[1] must be set to 1 after this value is set. Must be equal or higher then 6. |

### 5.24.2.51 UART\_ABAUD\_1ST\_CHAR Register

#### 1 UART\_ABAUD\_1ST\_CHAR Register (Offset = 78h) [reset = 0h]

Unused.

Return to [Summary Table](#)

**Table 5-3365. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0078h       |
| UART1         | 5230 1078h       |
| UART2         | 5230 2078h       |
| UART3         | 5230 3078h       |
| UART4         | 5230 4078h       |
| UART5         | 5230 5078h       |

**Figure 5-1109. UART\_ABAUD\_1ST\_CHAR Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-3367. UART\_ABAUD\_1ST\_CHAR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | R    | 0h    |             |

### 5.24.2.52 UART\_BAUD\_2ND\_CHAR Register

#### 1 UART\_BAUD\_2ND\_CHAR Register (Offset = 7Ch) [reset = 0h]

Unused.

Return to [Summary Table](#)

**Table 5-3368. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 007Ch       |
| UART1         | 5230 107Ch       |
| UART2         | 5230 207Ch       |
| UART3         | 5230 307Ch       |
| UART4         | 5230 407Ch       |
| UART5         | 5230 507Ch       |

**Figure 5-1110. UART\_BAUD\_2ND\_CHAR Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RESERVED |    |    |    |    |    |    |    |
| R        |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-3370. UART\_BAUD\_2ND\_CHAR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description |
|------|----------|------|-------|-------------|
| 31:0 | RESERVED | R    | 0h    |             |

### 5.24.2.53 UART\_MDR3 Register

#### 1 UART\_MDR3 Register (Offset = 80h) [reset = 0h]

Mode definition register 3.

Return to [Summary Table](#)

**Table 5-3371. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0080h       |
| UART1         | 5230 1080h       |
| UART2         | 5230 2080h       |
| UART3         | 5230 3080h       |
| UART4         | 5230 4080h       |
| UART5         | 5230 5080h       |

**Figure 5-1111. UART\_MDR3 Name Register**

|           |    |    |        |         |                      |                 |                      |
|-----------|----|----|--------|---------|----------------------|-----------------|----------------------|
| 31        | 30 | 29 | 28     | 27      | 26                   | 25              | 24                   |
| RESERVED2 |    |    |        |         |                      |                 |                      |
| R         |    |    |        |         |                      |                 |                      |
| 0h        |    |    |        |         |                      |                 |                      |
| 23        | 22 | 21 | 20     | 19      | 18                   | 17              | 16                   |
| RESERVED2 |    |    |        |         |                      |                 |                      |
| R         |    |    |        |         |                      |                 |                      |
| 0h        |    |    |        |         |                      |                 |                      |
| 15        | 14 | 13 | 12     | 11      | 10                   | 9               | 8                    |
| RESERVED2 |    |    |        |         |                      |                 |                      |
| R         |    |    |        |         |                      |                 |                      |
| 0h        |    |    |        |         |                      |                 |                      |
| 7         | 6  | 5  | 4      | 3       | 2                    | 1               | 0                    |
| RESERVED1 |    |    | DIR_EN | DIR_POL | SET_DMA_TX_THRESHOLD | NONDEFAULT_FREQ | DISABLE_CIR_RX_DEMOD |
| R         |    |    | R/W    | R/W     | R/W                  | R/W             | R/W                  |
| 0h        |    |    | 0h     | 0h      | 0h                   | 0h              | 0h                   |

**Table 5-3373. UART\_MDR3 Register Field Descriptions**

| Bit  | Field                | Type | Reset | Description                                                                                                   |
|------|----------------------|------|-------|---------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED2            | R    | 0h    | Reserved                                                                                                      |
| 7:5  | RESERVED1            | R    | 0h    | Reserved                                                                                                      |
| 4    | DIR_EN               | R/W  | 0h    | RS-485 External Transceiver Direction Enable                                                                  |
| 3    | DIR_POL              | R/W  | 0h    | RS-485 External Transceiver Direction Polarity. 0 => TX: RTS=0, RX: RTS=1. 1 => TX: RTS=1, RX: RTS=0          |
| 2    | SET_DMA_TX_THRESHOLD | R/W  | 0h    | Enable to set different TX DMA threshold then 64-trigger [usage of new register TX_DNA_THRESHOLD]             |
| 1    | NONDEFAULT_FREQ      | R/W  | 0h    | Enables[1]/Disables[0] using NONDEFAULT fclk frequencies                                                      |
| 0    | DISABLE_CIR_RX_DEMOD | R/W  | 0h    | Disables[1]/Enables[0] CIR RX demodulation<br>0 Enables CIR RX demodulation<br>1 Disables CIR RX demodulation |

#### 5.24.2.54 UART\_TX\_DMA\_THRESHOLD Register

##### 1 UART\_TX\_DMA\_THRESHOLD Register (Offset = 84h) [reset = 0h]

Use to manually set the TX DMA threshold level.

MDR3[2] SET\_TX\_DMA\_THRESHOLD must be one and must be value + tx\_trigger\_level <= 64 (TX FIFO size).

If not, 64-tx\_trigger\_level will be used w/o modifying the value of this register.

Return to [Summary Table](#)

**Table 5-3374. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0084h       |
| UART1         | 5230 1084h       |
| UART2         | 5230 2084h       |
| UART3         | 5230 3084h       |
| UART4         | 5230 4084h       |
| UART5         | 5230 5084h       |

**Figure 5-1112. UART\_TX\_DMA\_THRESHOLD Name Register**

|           |    |                  |    |    |    |    |    |
|-----------|----|------------------|----|----|----|----|----|
| 31        | 30 | 29               | 28 | 27 | 26 | 25 | 24 |
| RESERVED1 |    |                  |    |    |    |    |    |
| R         |    |                  |    |    |    |    |    |
| 0h        |    |                  |    |    |    |    |    |
| 23        | 22 | 21               | 20 | 19 | 18 | 17 | 16 |
| RESERVED1 |    |                  |    |    |    |    |    |
| R         |    |                  |    |    |    |    |    |
| 0h        |    |                  |    |    |    |    |    |
| 15        | 14 | 13               | 12 | 11 | 10 | 9  | 8  |
| RESERVED1 |    |                  |    |    |    |    |    |
| R         |    |                  |    |    |    |    |    |
| 0h        |    |                  |    |    |    |    |    |
| 7         | 6  | 5                | 4  | 3  | 2  | 1  | 0  |
| RESERVED  |    | TX_DMA_THRESHOLD |    |    |    |    |    |
| R         |    | R/W              |    |    |    |    |    |
| 0h        |    | 0h               |    |    |    |    |    |

**Table 5-3376. UART\_TX\_DMA\_THRESHOLD Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description                                     |
|------|------------------|------|-------|-------------------------------------------------|
| 31:8 | RESERVED1        | R    | 0h    | RESERVED                                        |
| 7:6  | RESERVED         | R    | 0h    | Reserved                                        |
| 5:0  | TX_DMA_THRESHOLD | R/W  | 0h    | Use to manually set the TX DMA threshold level. |

### 5.24.2.55 UART\_MDR4 Register

#### 1 UART\_MDR4 Register (Offset = 88h) [reset = 0h]

Mode definition register 4

Return to [Summary Table](#)

**Table 5-3377. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0088h       |
| UART1         | 5230 1088h       |
| UART2         | 5230 2088h       |
| UART3         | 5230 3088h       |
| UART4         | 5230 4088h       |
| UART5         | 5230 5088h       |

**Figure 5-1113. UART\_MDR4 Name Register**

|           |       |            |    |    |      |    |    |
|-----------|-------|------------|----|----|------|----|----|
| 31        | 30    | 29         | 28 | 27 | 26   | 25 | 24 |
| RESERVED1 |       |            |    |    |      |    |    |
| R         |       |            |    |    |      |    |    |
| 0h        |       |            |    |    |      |    |    |
| 23        | 22    | 21         | 20 | 19 | 18   | 17 | 16 |
| RESERVED1 |       |            |    |    |      |    |    |
| R         |       |            |    |    |      |    |    |
| 0h        |       |            |    |    |      |    |    |
| 15        | 14    | 13         | 12 | 11 | 10   | 9  | 8  |
| RESERVED1 |       |            |    |    |      |    |    |
| R         |       |            |    |    |      |    |    |
| 0h        |       |            |    |    |      |    |    |
| 7         | 6     | 5          | 4  | 3  | 2    | 1  | 0  |
| RESERVED  | MODE9 | FREQ_SEL_H |    |    | MODE |    |    |
| R         | R/W   | R/W        |    |    | R/W  |    |    |
| 0h        | 0h    | 0h         |    |    | 0h   |    |    |

**Table 5-3379. UART\_MDR4 Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                         |
|------|------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED1  | R    | 0h    |                                                                                                                                                                                                                                                     |
| 7    | RESERVED   | R    | 0h    |                                                                                                                                                                                                                                                     |
| 6    | MODE9      | R/W  | 0h    | 9-bit character length. When '1', overrides character length setting in LCR                                                                                                                                                                         |
| 5:3  | FREQ_SEL_H | R/W  | 0h    | Upper 3 bits of FREQ_SEL register for higher division values, as required for example for FI/Di in ISO7816 mode                                                                                                                                     |
| 2:0  | MODE       | R/W  | 0h    | New modes [when set, overrides MDR1 modes]<br>0 disabled (no override)<br>1 reserved<br>2 Synchronous mode with external clock<br>3 Synchronous mode with generated clock<br>4 ISO 7816 mode T=0<br>5 ISO 7816 mode T=1<br>6 reserved<br>7 reserved |

### 5.24.2.56 UART\_EFR2 Register

#### 1 UART\_EFR2 Register (Offset = 8Ch) [reset = 0h]

Enhanced Features Register 2

Return to [Summary Table](#)
**Table 5-3380. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 008Ch       |
| UART1         | 5230 108Ch       |
| UART2         | 5230 208Ch       |
| UART3         | 5230 308Ch       |
| UART4         | 5230 408Ch       |
| UART5         | 5230 508Ch       |

**Figure 5-1114. UART\_EFR2 Name Register**

|           |                    |     |     |     |           |                 |        |
|-----------|--------------------|-----|-----|-----|-----------|-----------------|--------|
| 31        | 30                 | 29  | 28  | 27  | 26        | 25              | 24     |
| RESERVED1 |                    |     |     |     |           |                 |        |
| R         |                    |     |     |     |           |                 |        |
| 0h        |                    |     |     |     |           |                 |        |
| 23        | 22                 | 21  | 20  | 19  | 18        | 17              | 16     |
| RESERVED1 |                    |     |     |     |           |                 |        |
| R         |                    |     |     |     |           |                 |        |
| 0h        |                    |     |     |     |           |                 |        |
| 15        | 14                 | 13  | 12  | 11  | 10        | 9               | 8      |
| RESERVED1 |                    |     |     |     |           |                 |        |
| R         |                    |     |     |     |           |                 |        |
| 0h        |                    |     |     |     |           |                 |        |
| 7         | 6                  | 5   | 4   | 3   | 2         | 1               | 0      |
| BROADCAST | TIMEOUT_BEH<br>AVE | C8  | C4  | C2  | MULTIDROP | RHR_OVERRU<br>N | ENDIAN |
| R/W       | R/W                | R/W | R/W | R/W | R/W       | R/W             | R/W    |
| 0h        | 0h                 | 0h  | 0h  | 0h  | 0h        | 0h              | 0h     |

**Table 5-3382. UART\_EFR2 Register Field Descriptions**

| Bit  | Field          | Type | Reset | Description                                                                                                                                                  |
|------|----------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED1      | R    | 0h    |                                                                                                                                                              |
| 7    | BROADCAST      | R/W  | 0h    | Enables broadcast address matching in multi-drop address match mode                                                                                          |
| 6    | TIMEOUT_BEHAVE | R/W  | 0h    | Specifies how timeout is measured<br>0 timeout after at least one character has been received<br>1 periodic timeout even when no character has been received |
| 5    | C8             | R/W  | 0h    | Value for ISO 7816C8 pin for software control                                                                                                                |
| 4    | C4             | R/W  | 0h    | Value for ISO 7816C4 pin for software control                                                                                                                |
| 3    | C2             | R/W  | 0h    | Value for ISO 7816reset pin [software controllable]                                                                                                          |
| 2    | MULTIDROP      | R/W  | 0h    | Enables parity Multi-drop mode [overrides LCR[5..3]] when '1'                                                                                                |

**Table 5-3382. UART\_EFR2 Register Field Descriptions (continued)**

| Bit | Field       | Type | Reset | Description                                                                                                                                                |
|-----|-------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | RHR_OVERRUN | R/W  | 0h    | RHR Overrun behaviour when buffer full<br>0 data in RHR is not overwritten (standard)<br>1 data in RHR is overwritten when buffer full (and FIFO disabled) |
| 0   | ENDIAN      | R/W  | 0h    | Endianness<br>0 Little Endian (LSB First)<br>1 Big Endian (MSB First)                                                                                      |



### 5.24.2.57 UART\_ECR Register

#### 1 UART\_ECR Register (Offset = 90h) [reset = 18h]

Enhanced Control register.

Return to [Summary Table](#)

**Table 5-3383. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0090h       |
| UART1         | 5230 1090h       |
| UART2         | 5230 2090h       |
| UART3         | 5230 3090h       |
| UART4         | 5230 4090h       |
| UART5         | 5230 5090h       |

**Figure 5-1115. UART\_ECR Name Register**

|           |             |       |       |        |        |             |    |
|-----------|-------------|-------|-------|--------|--------|-------------|----|
| 31        | 30          | 29    | 28    | 27     | 26     | 25          | 24 |
| RESERVED1 |             |       |       |        |        |             |    |
| R         |             |       |       |        |        |             |    |
| 0h        |             |       |       |        |        |             |    |
| 23        | 22          | 21    | 20    | 19     | 18     | 17          | 16 |
| RESERVED1 |             |       |       |        |        |             |    |
| R         |             |       |       |        |        |             |    |
| 0h        |             |       |       |        |        |             |    |
| 15        | 14          | 13    | 12    | 11     | 10     | 9           | 8  |
| RESERVED1 |             |       |       |        |        |             |    |
| R         |             |       |       |        |        |             |    |
| 0h        |             |       |       |        |        |             |    |
| 7         | 6           | 5     | 4     | 3      | 2      | 1           | 0  |
| RESERVED  | CLEAR_TX_PE | TX_EN | RX_EN | TX_RST | RX_RST | A_MULTIDROP |    |
| R         | W           | R/W   | R/W   | W      | W      | W           |    |
| 0h        | 0h          | 1h    | 1h    | 0h     | 0h     | 0h          |    |

**Table 5-3385. UART\_ECR Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                                                                                                            |
|------|-------------|------|-------|------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED1   | R    | 0h    |                                                                                                                        |
| 7:6  | RESERVED    | R    | 0h    |                                                                                                                        |
| 5    | CLEAR_TX_PE | W    | 0h    | Write 1 to clear parity error from the Transmitter to allow it to continue to try sending data [ISO7816 transmit only] |
| 4    | TX_EN       | R/W  | 1h    | Enables/Disables the transmitter<br>0 Transmitter is shut down<br>1 Transmitter is working                             |
| 3    | RX_EN       | R/W  | 1h    | Enables/Disables the receiver<br>0 Receiver is shut down<br>1 Receiver is operating                                    |
| 2    | TX_RST      | W    | 0h    | Writing '1' resets the transmitter                                                                                     |
| 1    | RX_RST      | W    | 0h    | Writing '1' resets the receiver                                                                                        |

**Table 5-3385. UART\_ECR Register Field Descriptions (continued)**

| Bit | Field       | Type | Reset | Description                                                                                                                                               |
|-----|-------------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | A_MULTIDROP | W    | 0h    | In multi-drop mode, when written with the value '1' causes the next byte written into THR to be transmitted with the parity bit set, signaling an address |

### 5.24.2.58 UART\_TIMEGUARD Register

#### 1 UART\_TIMEGUARD Register (Offset = 94h) [reset = 0h]

Timeguard.

Return to [Summary Table](#)

**Table 5-3386. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0094h       |
| UART1         | 5230 1094h       |
| UART2         | 5230 2094h       |
| UART3         | 5230 3094h       |
| UART4         | 5230 4094h       |
| UART5         | 5230 5094h       |

**Figure 5-1116. UART\_TIMEGUARD Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED  |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED  |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED  |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TIMEGUARD |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 5-3388. UART\_TIMEGUARD Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                          |
|------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED  | R    | 0h    |                                                                                                                                                      |
| 7:0  | TIMEGUARD | R/W  | 0h    | Specifies the amount of idle baud clocks [transmitter bit period] to insert between transmitted bytes, useful when communicating with slower devices |

### 5.24.2.59 UART\_TIMEOUTL Register

#### 1 UART\_TIMEOUTL Register (Offset = 98h) [reset = 0h]

Timeout lower byte.

Return to [Summary Table](#)

**Table 5-3389. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 0098h       |
| UART1         | 5230 1098h       |
| UART2         | 5230 2098h       |
| UART3         | 5230 3098h       |
| UART4         | 5230 4098h       |
| UART5         | 5230 5098h       |

**Figure 5-1117. UART\_TIMEOUTL Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED  |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED  |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED  |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TIMEOUT_L |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 5-3391. UART\_TIMEOUTL Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                   |
|------|-----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED  | R    | 0h    |                                                                                                                               |
| 7:0  | TIMEOUT_L | R/W  | 0h    | Custom timeout period in baud clocks, to override the internal value, when different from 0. [Lower byte of the 16 bit value] |

### 5.24.2.60 UART\_TIMEOUT Register

#### 1 UART\_TIMEOUT Register (Offset = 9Ch) [reset = 0h]

Timeout higher byte.

Return to [Summary Table](#)

**Table 5-3392. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 009Ch       |
| UART1         | 5230 109Ch       |
| UART2         | 5230 209Ch       |
| UART3         | 5230 309Ch       |
| UART4         | 5230 409Ch       |
| UART5         | 5230 509Ch       |

**Figure 5-1118. UART\_TIMEOUT Name Register**

|           |    |    |    |    |    |    |    |
|-----------|----|----|----|----|----|----|----|
| 31        | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED  |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 23        | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED  |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 15        | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED  |    |    |    |    |    |    |    |
| R         |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |
| 7         | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TIMEOUT_H |    |    |    |    |    |    |    |
| R/W       |    |    |    |    |    |    |    |
| 0h        |    |    |    |    |    |    |    |

**Table 5-3394. UART\_TIMEOUT Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                    |
|------|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED  | R    | 0h    |                                                                                                                                |
| 7:0  | TIMEOUT_H | R/W  | 0h    | Custom timeout period in baud clocks, to override the internal value, when different from 0. [Higher byte of the 16 bit value] |

### 5.24.2.61 UART\_SCCR Register

#### 1 UART\_SCCR Register (Offset = A0h) [reset = 7h]

Smartcard (ISO7816) mode Control Register.

Return to [Summary Table](#)

**Table 5-3395. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 00A0h       |
| UART1         | 5230 10A0h       |
| UART2         | 5230 20A0h       |
| UART3         | 5230 30A0h       |
| UART4         | 5230 40A0h       |
| UART5         | 5230 50A0h       |

**Figure 5-1119. UART\_SCCR Name Register**

|           |       |          |    |    |               |    |    |
|-----------|-------|----------|----|----|---------------|----|----|
| 31        | 30    | 29       | 28 | 27 | 26            | 25 | 24 |
| RESERVED1 |       |          |    |    |               |    |    |
| R         |       |          |    |    |               |    |    |
| 0h        |       |          |    |    |               |    |    |
| 23        | 22    | 21       | 20 | 19 | 18            | 17 | 16 |
| RESERVED1 |       |          |    |    |               |    |    |
| R         |       |          |    |    |               |    |    |
| 0h        |       |          |    |    |               |    |    |
| 15        | 14    | 13       | 12 | 11 | 10            | 9  | 8  |
| RESERVED1 |       |          |    |    |               |    |    |
| R         |       |          |    |    |               |    |    |
| 0h        |       |          |    |    |               |    |    |
| 7         | 6     | 5        | 4  | 3  | 2             | 1  | 0  |
| DSNACK    | INACK | RESERVED |    |    | MAX_ITERATION |    |    |
| R/W       | R/W   | R        |    |    | R/W           |    |    |
| 0h        | 0h    | 0h       |    |    | 7h            |    |    |

**Table 5-3397. UART\_SCCR Register Field Descriptions**

| Bit  | Field         | Type | Reset | Description                                                                                                                                                                                                                           |
|------|---------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED1     | R    | 0h    |                                                                                                                                                                                                                                       |
| 7    | DSNACK        | R/W  | 0h    | Applies Max_Iteration to receiver aswell - when maximum number of NACKs have been returned, the receiver will accept the data regardless of error. The data will be loaded into the receiver FIFO and PE will be set when Reading it. |
| 6    | INACK         | R/W  | 0h    | Inhibit NACK when receiving, even if an error is received. The data will be loaded into the receiver FIFO and PE will be set when Reading it.                                                                                         |
| 5:3  | RESERVED      | R    | 0h    |                                                                                                                                                                                                                                       |
| 2:0  | MAX_ITERATION | R/W  | 7h    | Number of times to repeat transmitted character, if the receiver did not acknowledge. If not acknowledged after the max value is reached, the UART transmitter will set parity error, stop and not continue until it is cleared.      |

### 5.24.2.62 UART\_ERHR Register

#### 1 UART\_ERHR Register (Offset = A4h) [reset = 0h]

Extended Receive Holding Register.

Return to [Summary Table](#)

**Table 5-3398. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 00A4h       |
| UART1         | 5230 10A4h       |
| UART2         | 5230 20A4h       |
| UART3         | 5230 30A4h       |
| UART4         | 5230 40A4h       |
| UART5         | 5230 50A4h       |

**Figure 5-1120. UART\_ERHR Name Register**

|          |    |    |    |    |    |    |      |
|----------|----|----|----|----|----|----|------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24   |
| RESERVED |    |    |    |    |    |    |      |
| R        |    |    |    |    |    |    |      |
| 0h       |    |    |    |    |    |    |      |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16   |
| RESERVED |    |    |    |    |    |    |      |
| R        |    |    |    |    |    |    |      |
| 0h       |    |    |    |    |    |    |      |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8    |
| RESERVED |    |    |    |    |    |    | ERHR |
| R        |    |    |    |    |    |    | R    |
| 0h       |    |    |    |    |    |    | 0h   |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0    |
| ERHR     |    |    |    |    |    |    |      |
| R        |    |    |    |    |    |    |      |
| 0h       |    |    |    |    |    |    |      |

**Table 5-3400. UART\_ERHR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                            |
|------|----------|------|-------|------------------------------------------------------------------------|
| 31:9 | RESERVED | R    | 0h    |                                                                        |
| 8:0  | ERHR     | R    | 0h    | Extended Receive Holding Register - allows accessing the full 9bit RHR |

### 5.24.2.63 UART\_ETHR Register

#### 1 UART\_ETHR Register (Offset = A4h) [reset = 0h]

Extended Transmit Holding Register.

Return to [Summary Table](#)

**Table 5-3401. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 00A4h       |
| UART1         | 5230 10A4h       |
| UART2         | 5230 20A4h       |
| UART3         | 5230 30A4h       |
| UART4         | 5230 40A4h       |
| UART5         | 5230 50A4h       |

**Figure 5-1121. UART\_ETHR Name Register**

|          |    |    |    |    |    |    |      |
|----------|----|----|----|----|----|----|------|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24   |
| RESERVED |    |    |    |    |    |    |      |
| R        |    |    |    |    |    |    |      |
| 0h       |    |    |    |    |    |    |      |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16   |
| RESERVED |    |    |    |    |    |    |      |
| R        |    |    |    |    |    |    |      |
| 0h       |    |    |    |    |    |    |      |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8    |
| RESERVED |    |    |    |    |    |    | ETHR |
| R        |    |    |    |    |    |    | W    |
| 0h       |    |    |    |    |    |    | 0h   |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0    |
| ETHR     |    |    |    |    |    |    |      |
| W        |    |    |    |    |    |    |      |
| 0h       |    |    |    |    |    |    |      |

**Table 5-3403. UART\_ETHR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                           |
|------|----------|------|-------|-----------------------------------------------------------------------|
| 31:9 | RESERVED | R    | 0h    |                                                                       |
| 8:0  | ETHR     | W    | 0h    | Extended Transmit Holding Register - allows Writing the full 9bit RHR |



### 5.24.2.64 UART\_MAR Register

#### 1 UART\_MAR Register (Offset = A8h) [reset = 0h]

Multidrop Address Register.

Return to [Summary Table](#)

**Table 5-3404. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 00A8h       |
| UART1         | 5230 10A8h       |
| UART2         | 5230 20A8h       |
| UART3         | 5230 30A8h       |
| UART4         | 5230 40A8h       |
| UART5         | 5230 50A8h       |

**Figure 5-1122. UART\_MAR Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| ADDRESS  |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-3406. UART\_MAR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                   |
|------|----------|------|-------|-------------------------------|
| 31:8 | RESERVED | NONE | 0h    | Reserved                      |
| 7:0  | ADDRESS  | R/W  | 0h    | Multidrop match address value |

### 5.24.2.65 UART\_MMR Register

#### 1 UART\_MMR Register (Offset = ACh) [reset = 0h]

Multidrop Mask Register.

Return to [Summary Table](#)

**Table 5-3407. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 00ACh       |
| UART1         | 5230 10ACh       |
| UART2         | 5230 20ACh       |
| UART3         | 5230 30ACh       |
| UART4         | 5230 40ACh       |
| UART5         | 5230 50ACh       |

**Figure 5-1123. UART\_MMR Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED |    |    |    |    |    |    |    |
| NONE     |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| MASK     |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-3409. UART\_MMR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                             |
|------|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------|
| 31:8 | RESERVED | NONE | 0h    | Reserved                                                                                                                |
| 7:0  | MASK     | R/W  | 0h    | Address match masking value ? Writing a 0 to a bit means that the corresponding address bit will be ignored in matching |

### 5.24.2.66 UART\_MBR Register

#### 1 UART\_MBR Register (Offset = B0h) [reset = 0h]

Multidrop Broadcast Address Register.

Return to [Summary Table](#)

**Table 5-3410. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| UART0         | 5230 00B0h       |
| UART1         | 5230 10B0h       |
| UART2         | 5230 20B0h       |
| UART3         | 5230 30B0h       |
| UART4         | 5230 40B0h       |
| UART5         | 5230 50B0h       |

**Figure 5-1124. UART\_MBR Name Register**

|                   |    |    |    |    |    |    |    |
|-------------------|----|----|----|----|----|----|----|
| 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 23                | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 15                | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| RESERVED          |    |    |    |    |    |    |    |
| NONE              |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |
| 7                 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| BROADCAST_ADDRESS |    |    |    |    |    |    |    |
| R/W               |    |    |    |    |    |    |    |
| 0h                |    |    |    |    |    |    |    |

**Table 5-3412. UART\_MBR Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description                            |
|------|-------------------|------|-------|----------------------------------------|
| 31:8 | RESERVED          | NONE | 0h    | Reserved                               |
| 7:0  | BROADCAST_ADDRESS | R/W  | 0h    | Broadcast address for address matching |

## 5.25 WDT

### WDT

#### 5.25.1 WDT Summaries

#### WDT Summaries

**Table 5-3413. WDT Registers, Base Address=5210 0000h, Length=256**

| Offset | Length | Register Name                       | WDT0 Physical Address | WDT1 Physical Address | WDT2 Physical Address |
|--------|--------|-------------------------------------|-----------------------|-----------------------|-----------------------|
| 0h     | 32     | <a href="#">WDT_RTIGCTRL</a>        | 5210 0000h            | 5210 1000h            | 5210 2000h            |
| 4h     | 32     | <a href="#">WDT_RTITBCTRL</a>       | 5210 0004h            | 5210 1004h            | 5210 2004h            |
| 8h     | 32     | <a href="#">WDT_RTICAPCTRL</a>      | 5210 0008h            | 5210 1008h            | 5210 2008h            |
| Ch     | 32     | <a href="#">WDT_RTICOMPCTRL</a>     | 5210 000Ch            | 5210 100Ch            | 5210 200Ch            |
| 10h    | 32     | <a href="#">WDT_RTIFRC0</a>         | 5210 0010h            | 5210 1010h            | 5210 2010h            |
| 14h    | 32     | <a href="#">WDT_RTIUC0</a>          | 5210 0014h            | 5210 1014h            | 5210 2014h            |
| 18h    | 32     | <a href="#">WDT_RTICPUC0</a>        | 5210 0018h            | 5210 1018h            | 5210 2018h            |
| 20h    | 32     | <a href="#">WDT_RTICAFRC0</a>       | 5210 0020h            | 5210 1020h            | 5210 2020h            |
| 24h    | 32     | <a href="#">WDT_RTICAUC0</a>        | 5210 0024h            | 5210 1024h            | 5210 2024h            |
| 30h    | 32     | <a href="#">WDT_RTIFRC1</a>         | 5210 0030h            | 5210 1030h            | 5210 2030h            |
| 34h    | 32     | <a href="#">WDT_RTIUC1</a>          | 5210 0034h            | 5210 1034h            | 5210 2034h            |
| 38h    | 32     | <a href="#">WDT_RTICPUC1</a>        | 5210 0038h            | 5210 1038h            | 5210 2038h            |
| 40h    | 32     | <a href="#">WDT_RTICAFRC1</a>       | 5210 0040h            | 5210 1040h            | 5210 2040h            |
| 44h    | 32     | <a href="#">WDT_RTICAUC1</a>        | 5210 0044h            | 5210 1044h            | 5210 2044h            |
| 50h    | 32     | <a href="#">WDT_RTICOMP0</a>        | 5210 0050h            | 5210 1050h            | 5210 2050h            |
| 54h    | 32     | <a href="#">WDT_RTIUDCP0</a>        | 5210 0054h            | 5210 1054h            | 5210 2054h            |
| 58h    | 32     | <a href="#">WDT_RTICOMP1</a>        | 5210 0058h            | 5210 1058h            | 5210 2058h            |
| 5Ch    | 32     | <a href="#">WDT_RTIUDCP1</a>        | 5210 005Ch            | 5210 105Ch            | 5210 205Ch            |
| 60h    | 32     | <a href="#">WDT_RTICOMP2</a>        | 5210 0060h            | 5210 1060h            | 5210 2060h            |
| 64h    | 32     | <a href="#">WDT_RTIUDCP2</a>        | 5210 0064h            | 5210 1064h            | 5210 2064h            |
| 68h    | 32     | <a href="#">WDT_RTICOMP3</a>        | 5210 0068h            | 5210 1068h            | 5210 2068h            |
| 6Ch    | 32     | <a href="#">WDT_RTIUDCP3</a>        | 5210 006Ch            | 5210 106Ch            | 5210 206Ch            |
| 70h    | 32     | <a href="#">WDT_RTITBLCOMP</a>      | 5210 0070h            | 5210 1070h            | 5210 2070h            |
| 74h    | 32     | <a href="#">WDT_RTITBHCOMP</a>      | 5210 0074h            | 5210 1074h            | 5210 2074h            |
| 80h    | 32     | <a href="#">WDT_RTISSETINT</a>      | 5210 0080h            | 5210 1080h            | 5210 2080h            |
| 84h    | 32     | <a href="#">WDT_RTICLEARINT</a>     | 5210 0084h            | 5210 1084h            | 5210 2084h            |
| 88h    | 32     | <a href="#">WDT_RTIINTFLAG</a>      | 5210 0088h            | 5210 1088h            | 5210 2088h            |
| 90h    | 32     | <a href="#">WDT_RTIDWDCTRL</a>      | 5210 0090h            | 5210 1090h            | 5210 2090h            |
| 94h    | 32     | <a href="#">WDT_RTIDWDPRLD</a>      | 5210 0094h            | 5210 1094h            | 5210 2094h            |
| 98h    | 32     | <a href="#">WDT_RTIWDSTATUS</a>     | 5210 0098h            | 5210 1098h            | 5210 2098h            |
| 9Ch    | 32     | <a href="#">WDT_RTIWDKEY</a>        | 5210 009Ch            | 5210 109Ch            | 5210 209Ch            |
| A0h    | 32     | <a href="#">WDT_RTIDWDCNTR</a>      | 5210 00A0h            | 5210 10A0h            | 5210 20A0h            |
| A4h    | 32     | <a href="#">WDT_RTIWWDRXNCTRL</a>   | 5210 00A4h            | 5210 10A4h            | 5210 20A4h            |
| A8h    | 32     | <a href="#">WDT_RTIWWDSIZECTRL</a>  | 5210 00A8h            | 5210 10A8h            | 5210 20A8h            |
| ACh    | 32     | <a href="#">WDT_RTIINTCLRENABLE</a> | 5210 00ACh            | 5210 10ACh            | 5210 20ACh            |
| B0h    | 32     | <a href="#">WDT_RTICOMP0CLR</a>     | 5210 00B0h            | 5210 10B0h            | 5210 20B0h            |
| B4h    | 32     | <a href="#">WDT_RTICOMP1CLR</a>     | 5210 00B4h            | 5210 10B4h            | 5210 20B4h            |
| B8h    | 32     | <a href="#">WDT_RTICOMP2CLR</a>     | 5210 00B8h            | 5210 10B8h            | 5210 20B8h            |

**Table 5-3413. WDT Registers, Base Address=5210 0000h, Length=256 (continued)**

| Offset | Length | Register Name                   | WDT0 Physical Address | WDT1 Physical Address | WDT2 Physical Address |
|--------|--------|---------------------------------|-----------------------|-----------------------|-----------------------|
| BCh    | 32     | <a href="#">WDT_RTICOMP3CLR</a> | 5210 00BCh            | 5210 10BCh            | 5210 20BCh            |

**Table 5-3414. WDT Registers, Base Address=5210 0000h, Length=256**

| Offset | Length | Register Name                       | WDT3 Physical Address |
|--------|--------|-------------------------------------|-----------------------|
| 0h     | 32     | <a href="#">WDT_RTIGCTRL</a>        | 5210 3000h            |
| 4h     | 32     | <a href="#">WDT_RTITBCTRL</a>       | 5210 3004h            |
| 8h     | 32     | <a href="#">WDT_RTICAPCTRL</a>      | 5210 3008h            |
| Ch     | 32     | <a href="#">WDT_RTICOMPCTRL</a>     | 5210 300Ch            |
| 10h    | 32     | <a href="#">WDT_RTIFRC0</a>         | 5210 3010h            |
| 14h    | 32     | <a href="#">WDT_RTIUC0</a>          | 5210 3014h            |
| 18h    | 32     | <a href="#">WDT_RTICPUC0</a>        | 5210 3018h            |
| 20h    | 32     | <a href="#">WDT_RTICAFRC0</a>       | 5210 3020h            |
| 24h    | 32     | <a href="#">WDT_RTICAUC0</a>        | 5210 3024h            |
| 30h    | 32     | <a href="#">WDT_RTIFRC1</a>         | 5210 3030h            |
| 34h    | 32     | <a href="#">WDT_RTIUC1</a>          | 5210 3034h            |
| 38h    | 32     | <a href="#">WDT_RTICPUC1</a>        | 5210 3038h            |
| 40h    | 32     | <a href="#">WDT_RTICAFRC1</a>       | 5210 3040h            |
| 44h    | 32     | <a href="#">WDT_RTICAUC1</a>        | 5210 3044h            |
| 50h    | 32     | <a href="#">WDT_RTICOMP0</a>        | 5210 3050h            |
| 54h    | 32     | <a href="#">WDT_RTIUDCP0</a>        | 5210 3054h            |
| 58h    | 32     | <a href="#">WDT_RTICOMP1</a>        | 5210 3058h            |
| 5Ch    | 32     | <a href="#">WDT_RTIUDCP1</a>        | 5210 305Ch            |
| 60h    | 32     | <a href="#">WDT_RTICOMP2</a>        | 5210 3060h            |
| 64h    | 32     | <a href="#">WDT_RTIUDCP2</a>        | 5210 3064h            |
| 68h    | 32     | <a href="#">WDT_RTICOMP3</a>        | 5210 3068h            |
| 6Ch    | 32     | <a href="#">WDT_RTIUDCP3</a>        | 5210 306Ch            |
| 70h    | 32     | <a href="#">WDT_RTITBLCOMP</a>      | 5210 3070h            |
| 74h    | 32     | <a href="#">WDT_RTITBHCOMP</a>      | 5210 3074h            |
| 80h    | 32     | <a href="#">WDT_RTISSETINT</a>      | 5210 3080h            |
| 84h    | 32     | <a href="#">WDT_RTICLEARINT</a>     | 5210 3084h            |
| 88h    | 32     | <a href="#">WDT_RTIINTFLAG</a>      | 5210 3088h            |
| 90h    | 32     | <a href="#">WDT_RTIDWDCTRL</a>      | 5210 3090h            |
| 94h    | 32     | <a href="#">WDT_RTIDWDPRLD</a>      | 5210 3094h            |
| 98h    | 32     | <a href="#">WDT_RTIWDSTATUS</a>     | 5210 3098h            |
| 9Ch    | 32     | <a href="#">WDT_RTIWDKEY</a>        | 5210 309Ch            |
| A0h    | 32     | <a href="#">WDT_RTIDWDCNTR</a>      | 5210 30A0h            |
| A4h    | 32     | <a href="#">WDT_RTIWWDRXNCTRL</a>   | 5210 30A4h            |
| A8h    | 32     | <a href="#">WDT_RTIWWDSIZECTRL</a>  | 5210 30A8h            |
| ACH    | 32     | <a href="#">WDT_RTIINTCLRENABLE</a> | 5210 30ACH            |
| B0h    | 32     | <a href="#">WDT_RTICOMP0CLR</a>     | 5210 30B0h            |
| B4h    | 32     | <a href="#">WDT_RTICOMP1CLR</a>     | 5210 30B4h            |
| B8h    | 32     | <a href="#">WDT_RTICOMP2CLR</a>     | 5210 30B8h            |
| BCh    | 32     | <a href="#">WDT_RTICOMP3CLR</a>     | 5210 30BCh            |

### **5.25.2 WDT Registers**

#### **WDT Registers**

### 5.25.2.1 WDT\_RTIGCTRL Register

#### 1 WDT\_RTIGCTRL Register (Offset = 0h) [reset = 0h]

Global Control Register starts / stops the counters .

Return to [Summary Table](#)

**Table 5-3415. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 0000h       |
| WDT1          | 5210 1000h       |
| WDT2          | 5210 2000h       |
| WDT3          | 5210 3000h       |

**Figure 5-1125. WDT\_RTIGCTRL Name Register**

|           |           |    |    |        |    |        |        |
|-----------|-----------|----|----|--------|----|--------|--------|
| 31        | 30        | 29 | 28 | 27     | 26 | 25     | 24     |
| RESERVED2 |           |    |    |        |    |        |        |
| R/W       |           |    |    |        |    |        |        |
| 0h        |           |    |    |        |    |        |        |
| 23        | 22        | 21 | 20 | 19     | 18 | 17     | 16     |
| RESERVED2 |           |    |    | NTUSEL |    |        |        |
| R/W       |           |    |    | R/W    |    |        |        |
| 0h        |           |    |    | 0h     |    |        |        |
| 15        | 14        | 13 | 12 | 11     | 10 | 9      | 8      |
| COS       | RESERVED1 |    |    |        |    |        |        |
| R/W       | R/W       |    |    |        |    |        |        |
| 0h        | 0h        |    |    |        |    |        |        |
| 7         | 6         | 5  | 4  | 3      | 2  | 1      | 0      |
| RESERVED1 |           |    |    |        |    | CNT1EN | CNT0EN |
| R/W       |           |    |    |        |    | R/W    | R/W    |
| 0h        |           |    |    |        |    | 0h     | 0h     |

**Table 5-3417. WDT\_RTIGCTRL Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:20 | RESERVED2 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 19:16 | NTUSEL    | R/W  | 0h    | NTUSEL: Select NTU signal.<br>These bits determine which NTU input signal is used as external timebase. There are up to four inputs supported with four valid selection combinations. Any invalid selection value written to the NTUSEL bit-field will result in a TIED LOW being used as the NTU signal. The NTU signal will also be TIED LOW in case of a single-bit flip as it will result in an invalid combination of NTUSEL.<br>User and privilege mode [read]:<br>0000= NTU0<br>0101= NTU1<br>1010= NTU2<br>1111= NTU3<br>other = tied to 0<br>Privilege mode [write]:<br>0000= NTU0<br>0101= NTU1<br>1010= NTU2<br>1111= NTU3<br>other = tied to 0 |

**Table 5-3417. WDT\_RTIGCTRL Register Field Descriptions (continued)**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                              |
|------|-----------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15   | COS       | R/W  | 0h    | COS: Continue On Suspend.<br>This bit determines if both counters are stopped when the device goes into debug mode or if they continue counting.<br>User and privilege mode [read]:<br>0 = counters are stopped while in debug mode<br>1 = counters are running while in debug mode<br>Privilege mode [write]:<br>0 = stop counters in debug mode<br>1 = continue counting in debug mode |
| 14:2 | RESERVED1 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                                                    |
| 1    | CNT1EN    | R/W  | 0h    | CNT1EN: Counter 1 Enable. The CNT1EN bit starts and stops the operation of counter block 1 [UC1 and FRC1].<br>User and privilege mode [read]:<br>0 = counters are stopped<br>1 = counters are running<br>Privilege mode [write]:<br>0 = stop counters<br>1 = start counters<br>Gives the absolute 32 bit destination address [physical].                                                 |
| 0    | CNT0EN    | R/W  | 0h    | CNT0EN: Counter 0 Enable. The CNT0EN bit starts and stops the operation of counter block 0 [UC0 and FRC0].<br>User and privilege mode [read]:<br>0 = counters are stopped<br>1 = counters are running<br>Privilege mode [write]:<br>0 = stop counters<br>1 = start counters<br>Gives the absolute 32 bits source address [physical].                                                     |



### 5.25.2.2 WDT\_RTITBCTRL Register

#### 1 WDT\_RTITBCTRL Register (Offset = 4h) [reset = 0h]

Timebase Control selection which source triggers free running counter 0 .

Return to [Summary Table](#)

**Table 5-3418. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 0004h       |
| WDT1          | 5210 1004h       |
| WDT2          | 5210 2004h       |
| WDT3          | 5210 3004h       |

**Figure 5-1126. WDT\_RTITBCTRL Name Register**

|           |    |    |    |    |    |     |       |
|-----------|----|----|----|----|----|-----|-------|
| 31        | 30 | 29 | 28 | 27 | 26 | 25  | 24    |
| RESERVED3 |    |    |    |    |    |     |       |
| R/W       |    |    |    |    |    |     |       |
| 0h        |    |    |    |    |    |     |       |
| 23        | 22 | 21 | 20 | 19 | 18 | 17  | 16    |
| RESERVED3 |    |    |    |    |    |     |       |
| R/W       |    |    |    |    |    |     |       |
| 0h        |    |    |    |    |    |     |       |
| 15        | 14 | 13 | 12 | 11 | 10 | 9   | 8     |
| RESERVED3 |    |    |    |    |    |     |       |
| R/W       |    |    |    |    |    |     |       |
| 0h        |    |    |    |    |    |     |       |
| 7         | 6  | 5  | 4  | 3  | 2  | 1   | 0     |
| RESERVED3 |    |    |    |    |    | INC | TBEXT |
| R/W       |    |    |    |    |    | R/W | R/W   |
| 0h        |    |    |    |    |    | 0h  | 0h    |

**Table 5-3420. WDT\_RTITBCTRL Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED3 | R/W  | 0h    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 1    | INC       | R/W  | 0h    | <p>INC: Increment Free Running Counter 0.</p> <p>This bit determines whether the Free Running Counter 0 is automatically incremented if a failing clock on the NTUx signal is detected.</p> <p>User and privilege mode [read]:</p> <p>0 = FRC0 will not be incremented</p> <p>1 = FRC0 will be incremented</p> <p>Privilege mode [write]:</p> <p>0 = Do not increment FRC0 on failing external clock</p> <p>1 = Increment FRC0 on failing external clock</p> |

**Table 5-3420. WDT\_RTITBCTRL Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | TBEXT | R/W  | 0h    | <p>TBEXT: Timebase External.</p> <p>The Timebase External bit selects whether the Free Running Counter 0 is clocked by the internal Up Counter 0 or from the external signal NTUx. Since setting the TBEXT bit to 1 resets Up Counter 0, Free Running Counter 0 will not be incremented in this occurrence. The only source which is able to increment Free Running Counter 0 is NTUx.</p> <p>When the Timebase Supervisor circuit detects a missing clockedge, then the TBEXT bit is reset.</p> <p>The selection if the external signal should be used, can only be done by software.</p> <p>User and privilege mode [read]:</p> <p>0 = UC0 clocks FRC0</p> <p>1 = NTUx clocks FRC0</p> <p>Privilege mode [write]:</p> <p>0 = MUX is switched to internal UC0 clocking scheme</p> <p>1 = MUX is switched to external NTUx clocking scheme</p> |

### 5.25.2.3 WDT\_RTICAPCTRL Register

#### 1 WDT\_RTICAPCTRL Register (Offset = 8h) [reset = 0h]

Capture Control controls the capture source for the counters.

Return to [Summary Table](#)

**Table 5-3421. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 0008h       |
| WDT1          | 5210 1008h       |
| WDT2          | 5210 2008h       |
| WDT3          | 5210 3008h       |

**Figure 5-1127. WDT\_RTICAPCTRL Name Register**

|           |    |    |    |    |    |          |          |
|-----------|----|----|----|----|----|----------|----------|
| 31        | 30 | 29 | 28 | 27 | 26 | 25       | 24       |
| RESERVED4 |    |    |    |    |    |          |          |
| R/W       |    |    |    |    |    |          |          |
| 0h        |    |    |    |    |    |          |          |
| 23        | 22 | 21 | 20 | 19 | 18 | 17       | 16       |
| RESERVED4 |    |    |    |    |    |          |          |
| R/W       |    |    |    |    |    |          |          |
| 0h        |    |    |    |    |    |          |          |
| 15        | 14 | 13 | 12 | 11 | 10 | 9        | 8        |
| RESERVED4 |    |    |    |    |    |          |          |
| R/W       |    |    |    |    |    |          |          |
| 0h        |    |    |    |    |    |          |          |
| 7         | 6  | 5  | 4  | 3  | 2  | 1        | 0        |
| RESERVED4 |    |    |    |    |    | CAPCNTR1 | CAPCNTR0 |
| R/W       |    |    |    |    |    | R/W      | R/W      |
| 0h        |    |    |    |    |    | 0h       | 0h       |

**Table 5-3423. WDT\_RTICAPCTRL Register Field Descriptions**

| Bit  | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------|-----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:2 | RESERVED4 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                                                                                                                     |
| 1    | CAPCNTR1  | R/W  | 0h    | CAPCNTR1: Capture Counter 1.<br>This bit determines, which external interrupt source triggers a capture event of both UC1 and FRC1.<br>User and privilege mode [read]:<br>0 = capture event is triggered by Capture Event Source 0<br>1 = capture event is triggered by Capture Event Source 1<br>Privilege mode [write]:<br>0 = enable capture event triggered by Capture Event Source 0<br>1 = enable capture event triggered by Capture Event Source 1 |

**Table 5-3423. WDT\_RTICAPCTRL Register Field Descriptions (continued)**

| Bit | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-----|----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | CAPCNTR0 | R/W  | 0h    | <p>CAPCNTR0: Capture Counter 0.</p> <p>This bit determines, which external interrupt source triggers a capture event of both UC0 and FRC0.</p> <p>User and privilege mode [read]:</p> <p>0 = capture event is triggered by Capture Event Source 0</p> <p>1 = capture event is triggered by Capture Event Source 1</p> <p>Privilege mode [write]:</p> <p>0 = enable capture event triggered by Capture Event Source 0</p> <p>1 = enable capture event triggered by Capture Event Source 1</p> <p>11 indexed</p> <p>10 reserved</p> <p>01 post-increment</p> <p>00 constant</p> |

### 5.25.2.4 WDT\_RTICOMPCTRL Register

#### 1 WDT\_RTICOMPCTRL Register (Offset = Ch) [reset = 0h]

Compare Control controls the source for the compare registers.

Return to [Summary Table](#)

**Table 5-3424. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 000Ch       |
| WDT1          | 5210 100Ch       |
| WDT2          | 5210 200Ch       |
| WDT3          | 5210 300Ch       |

**Figure 5-1128. WDT\_RTICOMPCTRL Name Register**

|           |    |    |          |           |    |    |          |
|-----------|----|----|----------|-----------|----|----|----------|
| 31        | 30 | 29 | 28       | 27        | 26 | 25 | 24       |
| RESERVED8 |    |    |          |           |    |    |          |
| R/W       |    |    |          |           |    |    |          |
| 0h        |    |    |          |           |    |    |          |
| 23        | 22 | 21 | 20       | 19        | 18 | 17 | 16       |
| RESERVED8 |    |    |          |           |    |    |          |
| R/W       |    |    |          |           |    |    |          |
| 0h        |    |    |          |           |    |    |          |
| 15        | 14 | 13 | 12       | 11        | 10 | 9  | 8        |
| RESERVED8 |    |    | COMP3SEL | RESERVED7 |    |    | COMP2SEL |
| R/W       |    |    | R/W      | R/W       |    |    | R/W      |
| 0h        |    |    | 0h       | 0h        |    |    | 0h       |
| 7         | 6  | 5  | 4        | 3         | 2  | 1  | 0        |
| RESERVED6 |    |    | COMP1SEL | RESERVED5 |    |    | COMP0SEL |
| R/W       |    |    | R/W      | R/W       |    |    | R/W      |
| 0h        |    |    | 0h       | 0h        |    |    | 0h       |

**Table 5-3426. WDT\_RTICOMPCTRL Register Field Descriptions**

| Bit   | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                           |
|-------|-----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:13 | RESERVED8 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                 |
| 12    | COMP3SEL  | R/W  | 0h    | COMPSEL3: Compare Select 3.<br>This bit determines the counter with which the compare value hold in compare register 3 is compared.<br>User and privilege mode [read]:<br>0 = value will be compared with FRC 0<br>1 = value will be compared with FRC 1<br>Privilege mode [write]:<br>0 = enable compare with FRC 0<br>1 = enable compare with FRC 1 |
| 11:9  | RESERVED7 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                 |

**Table 5-3426. WDT\_RTICOMPCTRL Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                           |
|-----|-----------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8   | COMP2SEL  | R/W  | 0h    | COMPSEL2: Compare Select 2.<br>This bit determines the counter with which the compare value hold in compare register 2 is compared.<br>User and privilege mode [read]:<br>0 = value will be compared with FRC 0<br>1 = value will be compared with FRC 1<br>Privilege mode [write]:<br>0 = enable compare with FRC 0<br>1 = enable compare with FRC 1 |
| 7:5 | RESERVED6 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                 |
| 4   | COMP1SEL  | R/W  | 0h    | COMPSEL1: Compare Select 1.<br>This bit determines the counter with which the compare value hold in compare register 1 is compared. User and privilege mode [read]:<br>0 = value will be compared with FRC 0<br>1 = value will be compared with FRC 1<br>Privilege mode [write]:<br>0 = enable compare with FRC 0<br>1 = enable compare with FRC 1    |
| 3:1 | RESERVED5 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                 |
| 0   | COMP0SEL  | R/W  | 0h    | COMPSEL0: Compare Select 0.<br>This bit determines the counter with which the compare value hold in compare register 0 is compared.<br>User and privilege mode [read]:<br>0 = value will be compared with FRC 0<br>1 = value will be compared with FRC 1<br>Privilege mode [write]:<br>0 = enable compare with FRC 0<br>1 = enable compare with FRC 1 |

### 5.25.2.5 WDT\_RTIFRC0 Register

#### 1 WDT\_RTIFRC0 Register (Offset = 10h) [reset = 0h]

Free Running Counter 0 current value of free running counter 0

Return to [Summary Table](#)

**Table 5-3427. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 0010h       |
| WDT1          | 5210 1010h       |
| WDT2          | 5210 2010h       |
| WDT3          | 5210 3010h       |

**Figure 5-1129. WDT\_RTIFRC0 Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FRC0 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FRC0 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FRC0 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FRC0 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-3429. WDT\_RTIFRC0 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | FRC0  | R/W  | 0h    | <p>FRC0: Free Running Counter 0.</p> <p>This registers holds the current value of the Free Running Counter 0 and will be updated continuously.</p> <p>User and privilege mode [read]:<br/>current value of the counter</p> <p>Privilege mode [write]:<br/>The counter can be preset by Writing to this register. The counter increments then from this written value upwards.</p> <p>Note: Presetting counters<br/>If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0.</p> |

### 5.25.2.6 WDT\_RTIUC0 Register

#### 1 WDT\_RTIUC0 Register (Offset = 14h) [reset = 0h]

Up Counter 0 current value of prescale counter 0

Return to [Summary Table](#)

**Table 5-3430. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 0014h       |
| WDT1          | 5210 1014h       |
| WDT2          | 5210 2014h       |
| WDT3          | 5210 3014h       |

**Figure 5-1130. WDT\_RTIUC0 Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UC0 |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UC0 |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| UC0 |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| UC0 |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 5-3432. WDT\_RTIUC0 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | UC0   | R/W  | 0h    | <p>UC0: Up Counter 0.</p> <p>This registers holds the current value of the Up Counter 0 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 0. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up Counter 0 and Free Running Counter 0.</p> <p>User and privilege mode [read]:<br/>value of the counter when the Free Running Counter 0 was read</p> <p>Privilege mode [write]:<br/>the counter can be preset by Writing to this register. The counter increments then from this written value upwards.</p> <p>Note: Presetting counters<br/>If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC0 and RTIFRC0.</p> <p>Note: Preset value concern<br/>If the preset value is bigger than the compare value stored in register RTICPUC0 then it can take a long time until a compare matches, since RTIUC0 has to count up until it overflows.</p> |



### 5.25.2.7 WDT\_RTICPUC0 Register

#### 1 WDT\_RTICPUC0 Register (Offset = 18h) [reset = 0h]

Compare Up Counter 0 compare value compared with prescale counter 0

Return to [Summary Table](#)

**Table 5-3433. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 0018h       |
| WDT1          | 5210 1018h       |
| WDT2          | 5210 2018h       |
| WDT3          | 5210 3018h       |

**Figure 5-1131. WDT\_RTICPUC0 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CPUC0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CPUC0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CPUC0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CPUC0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3435. WDT\_RTICPUC0 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CPUC0 | R/W  | 0h    | <p>This registers holds the compare value, which is compared with the Up Counter 0. When the compare matches, Free Running counter 0 is incremented. The Up Counter is set to zero when the counter value matches the CPUC0 value. The value set in this prescales the RTI clock.</p> <p>If CPUC0 =<br/> 0:then, frequency = RTICLK/ [2^32]<br/> If CPUC0<br/> 0:then , frequency = RTICLK/[CPUC0 + 1]</p> <p>User and privilege mode [read]:<br/> current compare value<br/> Privilege mode [write when TBEXT = 0]:<br/> the compare value is updated<br/> Privilege mode [write when TBEXT = 1]:<br/> the compare value is not changed</p> |

### 5.25.2.8 WDT\_RTICAFRC0 Register

#### 1 WDT\_RTICAFRC0 Register (Offset = 20h) [reset = 0h]

Capture Free Running Counter 0 current value of free running counter 0 on external event.

Return to [Summary Table](#)

**Table 5-3436. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 0020h       |
| WDT1          | 5210 1020h       |
| WDT2          | 5210 2020h       |
| WDT3          | 5210 3020h       |

**Figure 5-1132. WDT\_RTICAFRC0 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAFR0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAFR0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAFR0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAFR0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3438. WDT\_RTICAFRC0 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                       |
|------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CAFR0 | R/W  | 0h    | CAFR0: Capture Free Running Counter 0.<br>This registers captures the current value of the Free Running Counter 0 when a event occurs, controlled by the external capture control block.<br>User and privilege mode [read]:<br>value of Free Running Counter 0 on a capture event |

### 5.25.2.9 WDT\_RTICAUC0 Register

#### 1 WDT\_RTICAUC0 Register (Offset = 24h) [reset = 0h]

Capture Up Counter 0 current value of prescale counter 0 on external event.

Return to [Summary Table](#)

**Table 5-3439. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 0024h       |
| WDT1          | 5210 1024h       |
| WDT2          | 5210 2024h       |
| WDT3          | 5210 3024h       |

**Figure 5-1133. WDT\_RTICAUC0 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAUC0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAUC0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAUC0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAUC0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3441. WDT\_RTICAUC0 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CAUC0 | R/W  | 0h    | CAUC0: Capture Up Counter 0.<br>This registers captures the current value of the Up Counter 0 when a event occurs, controlled by the external capture control block. The read sequence has to be the same as with Up Counter 0 and Free Running Counter 0. So the RTICAFRC0 register has to be read first, before the RTICAUC0 register is read. This sequence ensures that the value of the RTICAUC0 register is the corresponding value to the RTICAFRC0 register, even if another capture event happens in between the two reads.<br>User and privilege mode [read]:<br>value of Up Counter 0 on a capture event |

### 5.25.2.10 WDT\_RTIFRC1 Register

#### 1 WDT\_RTIFRC1 Register (Offset = 30h) [reset = 0h]

Free Running Counter 1 current value of free running counter 1

Return to [Summary Table](#)

**Table 5-3442. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 0030h       |
| WDT1          | 5210 1030h       |
| WDT2          | 5210 2030h       |
| WDT3          | 5210 3030h       |

**Figure 5-1134. WDT\_RTIFRC1 Name Register**

|      |    |    |    |    |    |    |    |
|------|----|----|----|----|----|----|----|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| FRC1 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FRC1 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 15   | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| FRC1 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |
| 7    | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FRC1 |    |    |    |    |    |    |    |
| R/W  |    |    |    |    |    |    |    |
| 0h   |    |    |    |    |    |    |    |

**Table 5-3444. WDT\_RTIFRC1 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | FRC1  | R/W  | 0h    | <p>FRC1: Free Running Counter 1.</p> <p>This registers holds the current value of the Free Running Counter 1 and will be updated continuously.</p> <p>User and privilege mode [read]:<br/>current value of the counter</p> <p>Privilege mode [write]:<br/>The counter can be preset by Writing to this register. The counter increments then from this written value upwards.</p> <p>Note: Presetting counters<br/>If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC1 and RTIFRC1.</p> |

### 5.25.2.11 WDT\_RTIUC1 Register

#### 1 WDT\_RTIUC1 Register (Offset = 34h) [reset = 0h]

Up Counter 1 current value of prescale counter 1

Return to [Summary Table](#)

**Table 5-3445. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 0034h       |
| WDT1          | 5210 1034h       |
| WDT2          | 5210 2034h       |
| WDT3          | 5210 3034h       |

**Figure 5-1135. WDT\_RTIUC1 Name Register**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UC1 |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 23  | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UC1 |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 15  | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| UC1 |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |
| 7   | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| UC1 |    |    |    |    |    |    |    |
| R/W |    |    |    |    |    |    |    |
| 0h  |    |    |    |    |    |    |    |

**Table 5-3447. WDT\_RTIUC1 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | UC1   | R/W  | 0h    | <p>UC1: Up Counter 1.</p> <p>This registers holds the current value of the Up Counter 1 and prescales the RTI clock. It will be only updated by a previous read of Free Running Counter 1. This gives effectively a 64 bit read of both counters, without having the problem of a counter being updated between two consecutive reads on Up Counter 1 and Free Running Counter 1.</p> <p>User and privilege mode [read]:<br/>value of the counter when the Free Running Counter 1 was read</p> <p>Privilege mode [write]:<br/>the counter can be preset by Writing to this register. The counter increments then from this written value upwards.</p> <p>Note: Presetting counters<br/>If counters have to be preset, they have to be stopped from counting in the RTIGCTRL register in order to ensure consistency between RTIUC1 and RTIFRC1.</p> <p>Note: Preset value concern<br/>If the preset value is bigger than the compare value stored in register RTICPUC1 then it can take a long time until a compare matches, since RTIUC1 has to count up until it overflows.</p> |

### 5.25.2.12 WDT\_RTICPUC1 Register

#### 1 WDT\_RTICPUC1 Register (Offset = 38h) [reset = 0h]

Compare Up Counter 1 compare value compared with prescale counter 1

Return to [Summary Table](#)

**Table 5-3448. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 0038h       |
| WDT1          | 5210 1038h       |
| WDT2          | 5210 2038h       |
| WDT3          | 5210 3038h       |

**Figure 5-1136. WDT\_RTICPUC1 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CPUC1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CPUC1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CPUC1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CPUC1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3450. WDT\_RTICPUC1 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CPUC1 | R/W  | 0h    | <p>This registers holds the compare value, which is compared with the Up Counter 1. When the compare matches, Free Running Counter 1 is incremented. The Up Counter is set to zero when the counter value matches the CPUC1 value. The value set in this prescales the RTI clock.</p> <p>If CPUC1 =</p> <p>0:then, frequency = RTICLK/ [2<sup>32</sup>]</p> <p>If CPUC1</p> <p>0:then , frequency = RTICLK/[CPUC1 + 1]</p> <p>User and privilege mode [read]:</p> <p>current compare value</p> <p>Privilege mode [write when TBEXT = 0]:</p> <p>the compare value is updated</p> <p>Privilege mode [write when TBEXT = 1]:</p> <p>the compare value is not changed</p> |

### 5.25.2.13 WDT\_RTICAFRC1 Register

#### 1 WDT\_RTICAFRC1 Register (Offset = 40h) [reset = 0h]

Capture Free Running Counter 1 current value of free running counter 1 on external event.

Return to [Summary Table](#)

**Table 5-3451. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 0040h       |
| WDT1          | 5210 1040h       |
| WDT2          | 5210 2040h       |
| WDT3          | 5210 3040h       |

**Figure 5-1137. WDT\_RTICAFRC1 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAFR1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAFR1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAFR1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAFR1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3453. WDT\_RTICAFRC1 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                       |
|------|-------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CAFR1 | R/W  | 0h    | CAFR1: Capture Free Running Counter 1.<br>This registers captures the current value of the Free Running Counter 1 when a event occurs, controlled by the external capture control block.<br>User and privilege mode [read]:<br>value of Free Running Counter 1 on a capture event |

### 5.25.2.14 WDT\_RTICAUC1 Register

#### 1 WDT\_RTICAUC1 Register (Offset = 44h) [reset = 0h]

Capture Up Counter 1 current value of prescale counter 1 on external event.

Return to [Summary Table](#)

**Table 5-3454. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 0044h       |
| WDT1          | 5210 1044h       |
| WDT2          | 5210 2044h       |
| WDT3          | 5210 3044h       |

**Figure 5-1138. WDT\_RTICAUC1 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| CAUC1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| CAUC1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| CAUC1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| CAUC1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3456. WDT\_RTICAUC1 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | CAUC1 | R/W  | 0h    | CAUC1: Capture Up Counter 1.<br>This registers captures the current value of the Up Counter 1 when a event occurs, controlled by the external capture control block. The read sequence has to be the same as with Up Counter 1 and Free Running Counter 1. So the RTICAFRC1 register has to be read first, before the RTICAUC1 register is read. This sequence ensures that the value of the RTICAUC1 register is the corresponding value to the RTICAFRC1 register, even if another capture event happens in between the two reads.<br>User and privilege mode [read]:<br>value of Up Counter 1 on a capture event |



### 5.25.2.15 WDT\_RTICOMP0 Register

#### 1 WDT\_RTICOMP0 Register (Offset = 50h) [reset = 0h]

Compare 0 compare value to be compared with the counters.

Return to [Summary Table](#)

**Table 5-3457. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 0050h       |
| WDT1          | 5210 1050h       |
| WDT2          | 5210 2050h       |
| WDT3          | 5210 3050h       |

**Figure 5-1139. WDT\_RTICOMP0 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COMP0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COMP0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COMP0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COMP0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3459. WDT\_RTICOMP0 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | COMP0 | R/W  | 0h    | <p>COMP0: Compare 0.</p> <p>This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request.</p> <p>User and privilege mode [read]:</p> <p>current compare value</p> <p>Privilege mode [write]:</p> <p>update of the compare register with a new compare value</p> <p>Note: Reset behavior</p> <p>A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.</p> |

### 5.25.2.16 WDT\_RTIUDCP0 Register

#### 1 WDT\_RTIUDCP0 Register (Offset = 54h) [reset = 0h]

Update Compare 0 value to be added to the compare register 0 value on compare match.

Return to [Summary Table](#)

**Table 5-3460. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 0054h       |
| WDT1          | 5210 1054h       |
| WDT2          | 5210 2054h       |
| WDT3          | 5210 3054h       |

**Figure 5-1140. WDT\_RTIUDCP0 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UDCP0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UDCP0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| UDCP0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| UDCP0 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3462. WDT\_RTIUDCP0 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                |
|------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | UDCP0 | R/W  | 0h    | UDCP0: Update Compare 0 Register.<br>This registers holds a value, which is added to the value in the compare 0 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.<br>User and privilege mode [read]:<br>value to be added to the compare 0 register on the next compare match<br>Privilege mode [write]:<br>new update value |

### 5.25.2.17 WDT\_RTICOMP1 Register

#### 1 WDT\_RTICOMP1 Register (Offset = 58h) [reset = 0h]

Compare 1 compare value to be compared with the counters.

Return to [Summary Table](#)

**Table 5-3463. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 0058h       |
| WDT1          | 5210 1058h       |
| WDT2          | 5210 2058h       |
| WDT3          | 5210 3058h       |

**Figure 5-1141. WDT\_RTICOMP1 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COMP1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COMP1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COMP1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COMP1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3465. WDT\_RTICOMP1 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | COMP1 | R/W  | 0h    | <p>COMP1: compare1.</p> <p>This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request.</p> <p>User and privilege mode [read]:</p> <p>current compare value</p> <p>Privilege mode [write]:</p> <p>update of the compare register with a new compare value</p> <p>Note: Reset behavior</p> <p>A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.</p> |

### 5.25.2.18 WDT\_RTIUDCP1 Register

#### 1 WDT\_RTIUDCP1 Register (Offset = 5Ch) [reset = 0h]

Update Compare 1 value to be added to the compare register 1 value on compare match.

Return to [Summary Table](#)

**Table 5-3466. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 005Ch       |
| WDT1          | 5210 105Ch       |
| WDT2          | 5210 205Ch       |
| WDT3          | 5210 305Ch       |

**Figure 5-1142. WDT\_RTIUDCP1 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UDCP1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UDCP1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| UDCP1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| UDCP1 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3468. WDT\_RTIUDCP1 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                             |
|------|-------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | UDCP1 | R/W  | 0h    | UDCP1: Update compare1 Register.<br>This registers holds a value, which is added to the value in the compare1 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.<br>User and privilege mode [read]:<br>value to be added to the compare1 register on the next compare match<br>Privilege mode [write]:<br>new update value |

### 5.25.2.19 WDT\_RTICOMP2 Register

#### 1 WDT\_RTICOMP2 Register (Offset = 60h) [reset = 0h]

Compare 2 compare value to be compared with the counters.

Return to [Summary Table](#)

**Table 5-3469. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 0060h       |
| WDT1          | 5210 1060h       |
| WDT2          | 5210 2060h       |
| WDT3          | 5210 3060h       |

**Figure 5-1143. WDT\_RTICOMP2 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COMP2 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COMP2 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COMP2 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COMP2 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3471. WDT\_RTICOMP2 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|-------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | COMP2 | R/W  | 0h    | <p>COMP2: compare 2.</p> <p>This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request.</p> <p>User and privilege mode [read]:</p> <p>current compare value</p> <p>Privilege mode [write]:</p> <p>update of the compare register with a new compare value</p> <p>Note: Reset behavior</p> <p>A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.</p> |

### 5.25.2.20 WDT\_RTIUDCP2 Register

#### 1 WDT\_RTIUDCP2 Register (Offset = 64h) [reset = 0h]

Update Compare 2 value to be added to the compare register 2 value on compare match.

Return to [Summary Table](#)

**Table 5-3472. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 0064h       |
| WDT1          | 5210 1064h       |
| WDT2          | 5210 2064h       |
| WDT3          | 5210 3064h       |

**Figure 5-1144. WDT\_RTIUDCP2 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UDCP2 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UDCP2 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| UDCP2 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| UDCP2 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3474. WDT\_RTIUDCP2 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                |
|------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | UDCP2 | R/W  | 0h    | UDCP2: Update compare 2 Register.<br>This registers holds a value, which is added to the value in the compare 2 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.<br>User and privilege mode [read]:<br>value to be added to the compare 2 register on the next compare match<br>Privilege mode [write]:<br>new update value |

### 5.25.2.21 WDT\_RTICOMP3 Register

#### 1 WDT\_RTICOMP3 Register (Offset = 68h) [reset = 0h]

Compare 3 compare value to be compared with the counters.

Return to [Summary Table](#)

**Table 5-3475. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 0068h       |
| WDT1          | 5210 1068h       |
| WDT2          | 5210 2068h       |
| WDT3          | 5210 3068h       |

**Figure 5-1145. WDT\_RTICOMP3 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COMP3 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COMP3 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COMP3 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COMP3 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3477. WDT\_RTICOMP3 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------|-------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | COMP3 | R/W  | 0h    | <p>COMP3: compare 3.</p> <p>This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, an interrupt is flagged. With this register it is also possible to initiate a DMA request.</p> <p>User and privilege mode [read]:<br/>current compare value</p> <p>Privilege mode [write]:<br/>update of the compare register with a new compare value</p> <p>Note: Reset behavior<br/>A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.</p> |

### 5.25.2.22 WDT\_RTIUDCP3 Register

#### 1 WDT\_RTIUDCP3 Register (Offset = 6Ch) [reset = 0h]

Update Compare 3 value to be added to the compare register 3 value on compare match.

Return to [Summary Table](#)

**Table 5-3478. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 006Ch       |
| WDT1          | 5210 106Ch       |
| WDT2          | 5210 206Ch       |
| WDT3          | 5210 306Ch       |

**Figure 5-1146. WDT\_RTIUDCP3 Name Register**

|       |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| UDCP3 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 23    | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| UDCP3 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 15    | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| UDCP3 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |
| 7     | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| UDCP3 |    |    |    |    |    |    |    |
| R/W   |    |    |    |    |    |    |    |
| 0h    |    |    |    |    |    |    |    |

**Table 5-3480. WDT\_RTIUDCP3 Register Field Descriptions**

| Bit  | Field | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                |
|------|-------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | UDCP3 | R/W  | 0h    | UDCP3: Update compare 3 Register.<br>This registers holds a value, which is added to the value in the compare 3 register each time a compare matches. This gives the possibility to generate periodic interrupts without software intervention.<br>User and privilege mode [read]:<br>value to be added to the compare 3 register on the next compare match<br>Privilege mode [write]:<br>new update value |



### 5.25.2.23 WDT\_RTITBLCOMP Register

#### 1 WDT\_RTITBLCOMP Register (Offset = 70h) [reset = 0h]

Timebase Low Compare compare value to activate edge detection circuit.

Return to [Summary Table](#)

**Table 5-3481. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 0070h       |
| WDT1          | 5210 1070h       |
| WDT2          | 5210 2070h       |
| WDT3          | 5210 3070h       |

**Figure 5-1147. WDT\_RTITBLCOMP Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TBLCOMP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TBLCOMP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TBLCOMP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TBLCOMP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-3483. WDT\_RTITBLCOMP Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|---------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | TBLCOMP | R/W  | 0h    | <p>TBLCOMP: Timebase Low Compare Value.</p> <p>This value determines when the edge detection circuit starts monitoring the NTUx signal. It will be compared with Up Counter 0.</p> <p>User and privilege mode [read]:</p> <p>current compare value</p> <p>Privilege mode [write when TBEXT = 0]:</p> <p>the compare value is updated</p> <p>Privilege mode [write when TBEXT = 1]:</p> <p>the compare value is not changed</p> <p>Note: Reset behavior</p> <p>A reset does not generate a compare match.</p> |

### 5.25.2.24 WDT\_RTITBHCOMP Register

#### 1 WDT\_RTITBHCOMP Register (Offset = 74h) [reset = 0h]

Timebase High Compare compare value to deactivate edge detection circuit.

Return to [Summary Table](#)

**Table 5-3484. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 0074h       |
| WDT1          | 5210 1074h       |
| WDT2          | 5210 2074h       |
| WDT3          | 5210 3074h       |

**Figure 5-1148. WDT\_RTITBHCOMP Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| TBHCOMP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| TBHCOMP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| TBHCOMP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TBHCOMP |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-3486. WDT\_RTITBHCOMP Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|------|---------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | TBHCOMP | R/W  | 0h    | <p>TBHCOMP: Timebase High Compare Value.</p> <p>This value determines when the edge detection circuit will stop monitoring the NTUx signal. It will be compared with Up Counter 0.</p> <p>RTITBHCOMP has to be less than RTICPUC0, since RTIUC0 will be reset when RTICPUC0 is reached.</p> <p>Example:</p> <p>The NTUx edge detection circuit should be active +/- 10 RTICLK cycles around RTICPUC0.</p> <p>RTICPUC0 = 0x00000050</p> <p>RTITBLCOMP = 0x000046</p> <p>RTITBHCOMP = 0x00000009</p> <p>User and privilege mode [read]:</p> <p>current compare value</p> <p>Privilege mode [write when TBEXT = 0]:</p> <p>the compare value is updated</p> <p>Privilege mode [write when TBEXT = 1]:</p> <p>the compare value is not changed</p> <p>Note: Reset behavior</p> <p>A reset does not generate a compare match.</p> |

### 5.25.2.25 WDT\_RTISSETINT Register

#### 1 WDT\_RTISSETINT Register (Offset = 80h) [reset = 0h]

Set Interrupt Enable sets interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation.

Return to [Summary Table](#)

**Table 5-3487. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 0080h       |
| WDT1          | 5210 1080h       |
| WDT2          | 5210 2080h       |
| WDT3          | 5210 3080h       |

**Figure 5-1149. WDT\_RTISSETINT Name Register**

|            |    |    |    |         |            |            |          |
|------------|----|----|----|---------|------------|------------|----------|
| 31         | 30 | 29 | 28 | 27      | 26         | 25         | 24       |
| RESERVED11 |    |    |    |         |            |            |          |
| R/W        |    |    |    |         |            |            |          |
| 0h         |    |    |    |         |            |            |          |
| 23         | 22 | 21 | 20 | 19      | 18         | 17         | 16       |
| RESERVED11 |    |    |    |         | SETOVL1INT | SETOVL0INT | SETTBINT |
| R/W        |    |    |    |         | R/W        | R/W        | R/W      |
| 0h         |    |    |    |         | 0h         | 0h         | 0h       |
| 15         | 14 | 13 | 12 | 11      | 10         | 9          | 8        |
| RESERVED10 |    |    |    | SETDMA3 | SETDMA2    | SETDMA1    | SETDMA0  |
| R/W        |    |    |    | R/W     | R/W        | R/W        | R/W      |
| 0h         |    |    |    | 0h      | 0h         | 0h         | 0h       |
| 7          | 6  | 5  | 4  | 3       | 2          | 1          | 0        |
| RESERVED9  |    |    |    | SETINT3 | SETINT2    | SETINT1    | SETINT0  |
| R/W        |    |    |    | R/W     | R/W        | R/W        | R/W      |
| 0h         |    |    |    | 0h      | 0h         | 0h         | 0h       |

**Table 5-3489. WDT\_RTISSETINT Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                             |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:19 | RESERVED11 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                   |
| 18    | SETOVL1INT | R/W  | 0h    | SETOVL1INT: Set Free Running Counter 1 Overflow Interrupt.<br>User and privilege mode [read]:<br>0 = interrupt is disabled<br>1 = interrupt is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = enable interrupt |
| 17    | SETOVL0INT | R/W  | 0h    | SETOVL0INT: Set Free Running Counter 0 Overflow Interrupt.<br>User and privilege mode [read]:<br>0 = interrupt is disabled<br>1 = interrupt is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = enable interrupt |

**Table 5-3489. WDT\_RTISSETINT Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                            |
|-------|------------|------|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 16    | SETTBINT   | R/W  | 0h    | SETTBINT: Set Timebase Interrupt.<br>User and privilege mode [read]:<br>0 = interrupt is disabled<br>1 = interrupt is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = enable interrupt         |
| 15:12 | RESERVED10 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                  |
| 11    | SETDMA3    | R/W  | 0h    | SETDMA3: Set Compare DMA Request 3.<br>User and privilege mode [read]:<br>0 = DMA request is disabled<br>1 = DMA request is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = enable DMA request |
| 10    | SETDMA2    | R/W  | 0h    | SETDMA2: Set Compare DMA Request 2.<br>User and privilege mode [read]:<br>0 = DMA request is disabled<br>1 = DMA request is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = enable DMA request |
| 9     | SETDMA1    | R/W  | 0h    | SETDMA1: Set Compare DMA Request 1.<br>User and privilege mode [read]:<br>0 = DMA request is disabled<br>1 = DMA request is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = enable DMA request |
| 8     | SETDMA0    | R/W  | 0h    | SETDMA0: Set Compare DMA Request 0.<br>User and privilege mode [read]:<br>0 = DMA request is disabled<br>1 = DMA request is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = enable DMA request |
| 7:4   | RESERVED9  | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                  |
| 3     | SETINT3    | R/W  | 0h    | SETINT3: Set Compare Interrupt 3.<br>User and privilege mode [read]:<br>0 = interrupt is disabled<br>1 = interrupt is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged                                 |
| 2     | SETINT2    | R/W  | 0h    | SETINT2: Set Compare Interrupt 2.<br>User and privilege mode [read]:<br>0 = interrupt is disabled<br>1 = interrupt is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = enable interrupt         |
| 1     | SETINT1    | R/W  | 0h    | SETINT1: Set Compare Interrupt 1.<br>User and privilege mode [read]:<br>0 = interrupt is disabled<br>1 = interrupt is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = enable interrupt         |

**Table 5-3489. WDT\_RTISSETINT Register Field Descriptions (continued)**

| Bit | Field   | Type | Reset | Description                                                                                                                                                                                                                    |
|-----|---------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | SETINT0 | R/W  | 0h    | SETINT0: Set Compare Interrupt 0.<br>User and privilege mode [read]:<br>0 = interrupt is disabled<br>1 = interrupt is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = enable interrupt |

### 5.25.2.26 WDT\_RTICLEARINT Register

#### 1 WDT\_RTICLEARINT Register (Offset = 84h) [reset = 0h]

Clear Interrupt Enable clears interrupt enable bits int RTIINTCTRL without having to do a read-modify-write operation.

Return to [Summary Table](#)

**Table 5-3490. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 0084h       |
| WDT1          | 5210 1084h       |
| WDT2          | 5210 2084h       |
| WDT3          | 5210 3084h       |

**Figure 5-1150. WDT\_RTICLEARINT Name Register**

|            |    |    |    |           |              |              |           |
|------------|----|----|----|-----------|--------------|--------------|-----------|
| 31         | 30 | 29 | 28 | 27        | 26           | 25           | 24        |
| RESERVED14 |    |    |    |           |              |              |           |
| R/W        |    |    |    |           |              |              |           |
| 0h         |    |    |    |           |              |              |           |
| 23         | 22 | 21 | 20 | 19        | 18           | 17           | 16        |
| RESERVED14 |    |    |    |           | CLEAROVL1INT | CLEAROVL0INT | CLEARINT  |
| R/W        |    |    |    |           | R/W          | R/W          | R/W       |
| 0h         |    |    |    |           | 0h           | 0h           | 0h        |
| 15         | 14 | 13 | 12 | 11        | 10           | 9            | 8         |
| RESERVED13 |    |    |    | CLEARDMA3 | CLEARDMA2    | CLEARDMA1    | CLEARDMA0 |
| R/W        |    |    |    | R/W       | R/W          | R/W          | R/W       |
| 0h         |    |    |    | 0h        | 0h           | 0h           | 0h        |
| 7          | 6  | 5  | 4  | 3         | 2            | 1            | 0         |
| RESERVED12 |    |    |    | CLEARINT3 | CLEARINT2    | CLEARINT1    | CLEARINT0 |
| R/W        |    |    |    | R/W       | R/W          | R/W          | R/W       |
| 0h         |    |    |    | 0h        | 0h           | 0h           | 0h        |

**Table 5-3492. WDT\_RTICLEARINT Register Field Descriptions**

| Bit   | Field        | Type | Reset | Description                                                                                                                                                                                                                                                  |
|-------|--------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:19 | RESERVED14   | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                        |
| 18    | CLEAROVL1INT | R/W  | 0h    | CLEAROVL1INT: CLEAR Free Running Counter 1 Overflow Interrupt.<br>User and privilege mode [read]:<br>0 = interrupt is disabled<br>1 = interrupt is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = disable interrupt |
| 17    | CLEAROVL0INT | R/W  | 0h    | CLEAROVL0INT: CLEAR Free Running Counter 0 Overflow Interrupt.<br>User and privilege mode [read]:<br>0 = interrupt is disabled<br>1 = interrupt is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = disable interrupt |

**Table 5-3492. WDT\_RTICLEARINT Register Field Descriptions (continued)**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                 |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 16    | CLEARTBINT | R/W  | 0h    | CLEARTBINT: CLEAR Timebase Interrupt.<br>User and privilege mode [read]:<br>0 = interrupt is disabled<br>1 = interrupt is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = disable interrupt         |
| 15:12 | RESERVED13 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                       |
| 11    | CLEARDMA3  | R/W  | 0h    | CLEARDMA3: CLEAR Compare DMA Request 3.<br>User and privilege mode [read]:<br>0 = DMA request is disabled<br>1 = DMA request is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = disable DMA request |
| 10    | CLEARDMA2  | R/W  | 0h    | CLEARDMA2: CLEAR Compare DMA Request 2.<br>User and privilege mode [read]:<br>0 = DMA request is disabled<br>1 = DMA request is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = disable DMA request |
| 9     | CLEARDMA1  | R/W  | 0h    | CLEARDMA1: CLEAR Compare DMA Request 1.<br>User and privilege mode [read]:<br>0 = DMA request is disabled<br>1 = DMA request is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = disable DMA request |
| 8     | CLEARDMA0  | R/W  | 0h    | CLEARDMA0: CLEAR Compare DMA Request 0.<br>User and privilege mode [read]:<br>0 = DMA request is disabled<br>1 = DMA request is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = disable DMA request |
| 7:4   | RESERVED12 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                       |
| 3     | CLEARINT3  | R/W  | 0h    | CLEARINT3: CLEAR Compare Interrupt 3.<br>User and privilege mode [read]:<br>0 = interrupt is disabled<br>1 = interrupt is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = disable interrupt         |
| 2     | CLEARINT2  | R/W  | 0h    | CLEARINT2: CLEAR Compare Interrupt 2.<br>User and privilege mode [read]:<br>0 = interrupt is disabled<br>1 = interrupt is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = disable interrupt         |
| 1     | CLEARINT1  | R/W  | 0h    | CLEARINT1: CLEAR Compare Interrupt 1.<br>User and privilege mode [read]:<br>0 = interrupt is disabled<br>1 = interrupt is enabled<br>Privilege mode [write]:<br>0 = leaves the corresponding bit unchanged<br>1 = disable interrupt         |

**Table 5-3492. WDT\_RTICLEARINT Register Field Descriptions (continued)**

| Bit | Field     | Type | Reset | Description                                                                                                                                                                                                                                                        |
|-----|-----------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0   | CLEARINT0 | R/W  | 0h    | <p>CLEARINT0: CLEAR Compare Interrupt 0.</p> <p>User and privilege mode [read]:</p> <p>0 = interrupt is disabled</p> <p>1 = interrupt is enabled</p> <p>Privilege mode [write]:</p> <p>0 = leaves the corresponding bit unchanged</p> <p>1 = disable interrupt</p> |



### 5.25.2.27 WDT\_RTIINTFLAG Register

#### 1 WDT\_RTIINTFLAG Register (Offset = 88h) [reset = 0h]

Interrupt Flags interrupt pending bits.

Return to [Summary Table](#)

**Table 5-3493. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 0088h       |
| WDT1          | 5210 1088h       |
| WDT2          | 5210 2088h       |
| WDT3          | 5210 3088h       |

**Figure 5-1151. WDT\_RTIINTFLAG Name Register**

|            |    |    |    |         |      |         |       |
|------------|----|----|----|---------|------|---------|-------|
| 31         | 30 | 29 | 28 | 27      | 26   | 25      | 24    |
| RESERVED16 |    |    |    |         |      |         |       |
| R/W        |    |    |    |         |      |         |       |
| 0h         |    |    |    |         |      |         |       |
| 23         | 22 | 21 | 20 | 19      | 18   | 17      | 16    |
| RESERVED16 |    |    |    | OVL1INT |      | OVL0INT | TBINT |
| R/W        |    |    |    | R/W     |      | R/W     | R/W   |
| 0h         |    |    |    | 0h      |      | 0h      | 0h    |
| 15         | 14 | 13 | 12 | 11      | 10   | 9       | 8     |
| RESERVED15 |    |    |    |         |      |         |       |
| R/W        |    |    |    |         |      |         |       |
| 0h         |    |    |    |         |      |         |       |
| 7          | 6  | 5  | 4  | 3       | 2    | 1       | 0     |
| RESERVED15 |    |    |    | INT3    | INT2 | INT1    | INT0  |
| R/W        |    |    |    | R/W     | R/W  | R/W     | R/W   |
| 0h         |    |    |    | 0h      | 0h   | 0h      | 0h    |

**Table 5-3495. WDT\_RTIINTFLAG Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                  |
|-------|------------|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:19 | RESERVED16 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                        |
| 18    | OVL1INT    | R/W  | 0h    | OVL1INT: Free Running Counter 1 Overflow Interrupt Flag.<br>User and privilege mode [read]:<br>determines if an interrupt is pending<br>0 = no interrupt pending<br>1 = interrupt pending<br>Privilege mode [write]:<br>0 = leaves the bit unchanged<br>1 = set the bit to 0 |
| 17    | OVL0INT    | R/W  | 0h    | OVL0INT: Free Running Counter 0 Overflow Interrupt Flag.<br>User and privilege mode [read]:<br>determines if an interrupt is pending<br>0 = no interrupt pending<br>1 = interrupt pending<br>Privilege mode [write]:<br>0 = leaves the bit unchanged<br>1 = set the bit to 0 |

**Table 5-3495. WDT\_RTINTFLAG Register Field Descriptions (continued)**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                        |
|------|------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 16   | TBINT      | R/W  | 0h    | User and privilege mode [read]:<br>this flag is set when the TBEXT bit is cleared by detection of a missing external clockedge. It will not be set by clearing TBEXT by software.<br>determines if an interrupt is pending<br>0 = no interrupt pending<br>1 = interrupt pending<br>Privilege mode [write]:<br>0 = leaves the bit unchanged<br>1 = set the bit to 0 |
| 15:4 | RESERVED15 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                              |
| 3    | INT3       | R/W  | 0h    | INT3: Interrupt Flag 3.<br>User and privilege mode [read]:<br>determines if a interrupt is pending<br>0 = no interrupt pending<br>1 = interrupt pending<br>Privilege mode [write]:<br>0 = leaves the bit unchanged<br>1 = set the bit to 0                                                                                                                         |
| 2    | INT2       | R/W  | 0h    | INT2: Interrupt Flag 2.<br>User and privilege mode [read]:<br>determines if a interrupt is pending<br>0 = no interrupt pending<br>1 = interrupt pending<br>Privilege mode [write]:<br>0 = leaves the bit unchanged<br>1 = set the bit to 0                                                                                                                         |
| 1    | INT1       | R/W  | 0h    | INT1: Interrupt Flag 1.<br>User and privilege mode [read]:<br>determines if a interrupt is pending<br>0 = no interrupt pending<br>1 = interrupt pending<br>Privilege mode [write]:<br>0 = leaves the bit unchanged<br>1 = set the bit to 0                                                                                                                         |
| 0    | INT0       | R/W  | 0h    | INT0: Interrupt Flag 0.<br>User and privilege mode [read]:<br>determines if a interrupt is pending<br>0 = no interrupt pending<br>1 = interrupt pending<br>Privilege mode [write]:<br>0 = leaves the bit unchanged<br>1 = set the bit to 0                                                                                                                         |

### 5.25.2.28 WDT\_RTIDWDCTRL Register

#### 1 WDT\_RTIDWDCTRL Register (Offset = 90h) [reset = 0h]

Digital Watchdog Control Enables the Digital Watchdog.

Return to [Summary Table](#)

**Table 5-3496. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 0090h       |
| WDT1          | 5210 1090h       |
| WDT2          | 5210 2090h       |
| WDT3          | 5210 3090h       |

**Figure 5-1152. WDT\_RTIDWDCTRL Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| DWDCTRL |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| DWDCTRL |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| DWDCTRL |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| DWDCTRL |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-3498. WDT\_RTIDWDCTRL Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|------|---------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | DWDCTRL | R/W  | 0h    | <p>DWDCTRL: Digital Watchdog Control.</p> <p>User and privilege mode [read]:</p> <p>0x5312ACED = DWD counter is disabled. This is the default value.</p> <p>0xA98559DA = DWD counter is enabled</p> <p>Any other value = DWD counter state is unchanged [enabled or disabled]</p> <p>Privilege mode [write]:</p> <p>0xA98559DA = DWD counter is enabled</p> <p>Any other value = State of DWD counter is unchanged [stays enabled or disabled]</p> <p>Note: One-Write Functionality of DWDCTRL Register</p> <p>The RTIDWDCTRL register implements a one-write functionality, such that the application cannot write to this register more than once. Writing the default value will not enable the watchdog as described above. Writing the enable value will start the watchdog counters. A write to RTIDWDCTRL will only be enabled after a system reset again.</p> |

### 5.25.2.29 WDT\_RTIDWDPRLD Register

#### 1 WDT\_RTIDWDPRLD Register (Offset = 94h) [reset = 0h]

Digital Watchdog Preload sets the expiration time of the Digital Watchdog.

Return to [Summary Table](#)

**Table 5-3499. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 0094h       |
| WDT1          | 5210 1094h       |
| WDT2          | 5210 2094h       |
| WDT3          | 5210 3094h       |

**Figure 5-1153. WDT\_RTIDWDPRLD Name Register**

|            |    |    |    |         |    |    |    |
|------------|----|----|----|---------|----|----|----|
| 31         | 30 | 29 | 28 | 27      | 26 | 25 | 24 |
| RESERVED17 |    |    |    |         |    |    |    |
| R/W        |    |    |    |         |    |    |    |
| 0h         |    |    |    |         |    |    |    |
| 23         | 22 | 21 | 20 | 19      | 18 | 17 | 16 |
| RESERVED17 |    |    |    |         |    |    |    |
| R/W        |    |    |    |         |    |    |    |
| 0h         |    |    |    |         |    |    |    |
| 15         | 14 | 13 | 12 | 11      | 10 | 9  | 8  |
| RESERVED17 |    |    |    | DWDPRLD |    |    |    |
| R/W        |    |    |    | R/W     |    |    |    |
| 0h         |    |    |    | 0h      |    |    |    |
| 7          | 6  | 5  | 4  | 3       | 2  | 1  | 0  |
| DWDPRLD    |    |    |    |         |    |    |    |
| R/W        |    |    |    |         |    |    |    |
| 0h         |    |    |    |         |    |    |    |

**Table 5-3501. WDT\_RTIDWDPRLD Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:12 | RESERVED17 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 11:0  | DWDPRLD    | R/W  | 0h    | DWDPRLD: Digital Watchdog Preload Value.<br>User and privileged mode [read]:<br>A read from this register in any CPU mode returns the current preload value.<br>Privileged mode [write]:<br>The DWD preload register can be configured only when the DWD is disabled. Therefore, the application can only configure the DWD preload register before it enables the DWD down counter.<br>The expiration time of the DWD Down Counter can be determined with following equation:<br>$t_{exp} = [RTIDWDPRLD+1] \times 2^{13} / RTICK1$<br>where: RTIDWDPRLD = 0...4095 |

### 5.25.2.30 WDT\_RTIWDSTATUS Register

#### 1 WDT\_RTIWDSTATUS Register (Offset = 98h) [reset = 0h]

Watchdog Status reflects the status of Analog and Digital Watchdog.

Return to [Summary Table](#)

**Table 5-3502. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 0098h       |
| WDT1          | 5210 1098h       |
| WDT2          | 5210 2098h       |
| WDT3          | 5210 3098h       |

**Figure 5-1154. WDT\_RTIWDSTATUS Name Register**

|            |         |             |               |       |       |       |     |
|------------|---------|-------------|---------------|-------|-------|-------|-----|
| 31         | 30      | 29          | 28            | 27    | 26    | 25    | 24  |
| RESERVED18 |         |             |               |       |       |       |     |
| R/W        |         |             |               |       |       |       |     |
| 0h         |         |             |               |       |       |       |     |
| 23         | 22      | 21          | 20            | 19    | 18    | 17    | 16  |
| RESERVED18 |         |             |               |       |       |       |     |
| R/W        |         |             |               |       |       |       |     |
| 0h         |         |             |               |       |       |       |     |
| 15         | 14      | 13          | 12            | 11    | 10    | 9     | 8   |
| RESERVED18 |         |             |               |       |       |       |     |
| R/W        |         |             |               |       |       |       |     |
| 0h         |         |             |               |       |       |       |     |
| 7          | 6       | 5           | 4             | 3     | 2     | 1     | 0   |
| RESERVED18 | DWWD_ST | ENDTIMEVIOL | STARTTIMEVIOL | KEYST | DWDST | AWDST |     |
| R/W        | R/W     | R/W         | R/W           | R/W   | R/W   | R/W   | R/W |
| 0h         | 0h      | 0h          | 0h            | 0h    | 0h    | 0h    | 0h  |

**Table 5-3504. WDT\_RTIWDSTATUS Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:6 | RESERVED18 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 5    | DWWD_ST    | R/W  | 0h    | DWWD ST: Windowed Watchdog Status.<br>This bit denotes whether the time-window defined by the windowed watchdog configuration has been violated, or if a wrong key or key sequence was written to service the watchdog.<br>User and privilege mode [read]:<br>0 = no time-window violation has occurred.<br>1 = a time-window violation has occurred. The watchdog will generate either a system reset or a non-maskable interrupt to the CPU in this case.<br>Privilege mode [write]:<br>0 = leaves the current value unchanged.<br>1 = clears the bit to 0. This will also clear all other status flags in the RTIWDSTATUS register except for the AWD ST flag. Clearing of the status flags will deassert the non-maskable interrupt generated due to violation of the DWWD. |

**Table 5-3504. WDT\_RTIWDSTATUS Register Field Descriptions (continued)**

| Bit | Field         | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-----|---------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4   | ENDTIMEVIOL   | R/W  | 0h    | <p>END TIME VIOL: Windowed Watchdog End Time Violation Status. This bit denotes whether the end-time defined by the windowed watchdog configuration has been violated. This bit is effectively a copy of the DWD ST status flag.</p> <p>User and privilege mode [read]:</p> <p>0 = no end-time window violation has occurred.</p> <p>1 = the end-time defined by the windowed watchdog configuration has been violated.</p> <p>Privilege mode [write]:</p> <p>0 = leaves the current value unchanged.</p> <p>1 = clears the bit to 0.</p>                                |
| 3   | STARTTIMEVIOL | R/W  | 0h    | <p>START TIME VIOL: Windowed Watchdog Start Time Violation Status. This bit denotes whether the start-time defined by the windowed watchdog configuration has been violated. This indicates that the WWD was serviced before the service window was opened.</p> <p>User and privilege mode [read]:</p> <p>0 = no start-time window violation has occurred.</p> <p>1 = the start-time defined by the windowed watchdog configuration has been violated.</p> <p>Privilege mode [write]:</p> <p>0 = leaves the current value unchanged.</p> <p>1 = clears the bit to 0.</p> |
| 2   | KEYST         | R/W  | 0h    | <p>KEYST: Watchdog KeyStatus. This bit denotes a reset generated by a wrong key or a wrong key-sequence written to the RTIWDKEY register.</p> <p>User and privilege mode [read]:</p> <p>0 = no wrong key or key-sequence written</p> <p>1 = wrong key or key-sequence written to RTIWDKEY register</p> <p>Privilege mode [write]:</p> <p>0 = leaves the current value unchanged</p> <p>1 = clears the bit to 0</p>                                                                                                                                                       |
| 1   | DWDST         | R/W  | 0h    | <p>DWDST: Digital Watchdog Status. This bit is effectively a copy of the END TIME VIOL status flag and is maintained for compatibility reasons.</p> <p>User and privilege mode [read]:</p> <p>0 = DWD timeout period not expired</p> <p>1 = DWD timeout period has expired</p> <p>Privilege mode [write]:</p> <p>0 = leaves the current value unchanged</p> <p>1 = clears the bit to 0</p>                                                                                                                                                                               |
| 0   | AWDST         | R/W  | 0h    | <p>AWDST: Analog Watchdog Status. User and privilege mode [read]:</p> <p>0 = AWD pin 0 &gt; 1 threshold not exceeded</p> <p>1 = AWD pin 0 &gt; 1 threshold exceeded</p> <p>Privilege mode [write]:</p> <p>0 = leaves the current value unchanged</p> <p>1 = clears the bit to 0</p>                                                                                                                                                                                                                                                                                      |

### 5.25.2.31 WDT\_RTIWDKEY Register

#### 1 WDT\_RTIWDKEY Register (Offset = 9Ch) [reset = 0h]

Watchdog Key correct written key values discharge the external capacitor.

Return to [Summary Table](#)

**Table 5-3505. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 009Ch       |
| WDT1          | 5210 109Ch       |
| WDT2          | 5210 209Ch       |
| WDT3          | 5210 309Ch       |

**Figure 5-1155. WDT\_RTIWDKEY Name Register**

|            |    |    |    |    |    |    |    |
|------------|----|----|----|----|----|----|----|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| RESERVED19 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| RESERVED19 |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| WDKEY      |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| WDKEY      |    |    |    |    |    |    |    |
| R/W        |    |    |    |    |    |    |    |
| 0h         |    |    |    |    |    |    |    |

**Table 5-3507. WDT\_RTIWDKEY Register Field Descriptions**

| Bit   | Field      | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|-------|------------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:16 | RESERVED19 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 15:0  | WDKEY      | R/W  | 0h    | WDKEY: Watchdog Key.<br>User and privilege mode reads are indeterminate.<br>Privilege mode [write]:<br>A write of 0xE51A followed by 0xA35C in two separate write operations defines the Key Sequence and discharges the watchdog capacitor. This also causes the upper 12 bits of the DWD down counter to be reloaded with the contents of the DWD preload register and the lower 13 bits to become all 1s. Writing any other value causes a digital watchdog reset, as shown in Table 1-3.<br>Note: Register write access time precaution<br>The user has to take into account that the write to the register takes 3 VCLK cycle. This needs to be considered for the AWD/DWD expiration calculation. |

### 5.25.2.32 WDT\_RTIDWDCNTR Register

#### 1 WDT\_RTIDWDCNTR Register (Offset = A0h) [reset = 1FFFFFFh]

Digital Watchdog Down Counter current value of DWD down counter.

Return to [Summary Table](#)

**Table 5-3508. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 00A0h       |
| WDT1          | 5210 10A0h       |
| WDT2          | 5210 20A0h       |
| WDT3          | 5210 30A0h       |

**Figure 5-1156. WDT\_RTIDWDCNTR Name Register**

|            |    |    |    |    |    |    |          |
|------------|----|----|----|----|----|----|----------|
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24       |
| RESERVED20 |    |    |    |    |    |    | DWDCNTR  |
| R/W        |    |    |    |    |    |    | R/W      |
| 0h         |    |    |    |    |    |    | 1FFFFFFh |
| 23         | 22 | 21 | 20 | 19 | 18 | 17 | 16       |
| DWDCNTR    |    |    |    |    |    |    |          |
| R/W        |    |    |    |    |    |    |          |
| 1FFFFFFh   |    |    |    |    |    |    |          |
| 15         | 14 | 13 | 12 | 11 | 10 | 9  | 8        |
| DWDCNTR    |    |    |    |    |    |    |          |
| R/W        |    |    |    |    |    |    |          |
| 1FFFFFFh   |    |    |    |    |    |    |          |
| 7          | 6  | 5  | 4  | 3  | 2  | 1  | 0        |
| DWDCNTR    |    |    |    |    |    |    |          |
| R/W        |    |    |    |    |    |    |          |
| 1FFFFFFh   |    |    |    |    |    |    |          |

**Table 5-3510. WDT\_RTIDWDCNTR Register Field Descriptions**

| Bit   | Field      | Type | Reset    | Description                                                                                                                                                                                                                                                                                                                                                                                                            |
|-------|------------|------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:25 | RESERVED20 | R/W  | 0h       | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                                                                                  |
| 24:0  | DWDCNTR    | R/W  | 1FFFFFFh | DWDCNTR: Digital Watchdog Down Counter.<br>The value of the DWDCNTR after a system reset is 0x01FF_FFFF.<br>When the DWD is enabled and the DWD counter starts counting down from this value with an RTICK1 time base of 3MHz, a watchdog reset will be generated in 1 second.<br>User and privilege mode [read]:<br>Reads return the current counter value.<br>Privilege mode [write]:<br>Writes dont have an effect. |



### 5.25.2.33 WDT\_RTIWWDRXNCTRL Register

#### 1 WDT\_RTIWWDRXNCTRL Register (Offset = A4h) [reset = 0h]

Windowed Watchdog Reaction Control configures the windowed watchdog to either generate a non-maskable interrupt to the CPU or to generate a system reset.

Return to [Summary Table](#)

**Table 5-3511. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 00A4h       |
| WDT1          | 5210 10A4h       |
| WDT2          | 5210 20A4h       |
| WDT3          | 5210 30A4h       |

**Figure 5-1157. WDT\_RTIWWDRXNCTRL Name Register**

|            |    |    |    |        |    |    |    |
|------------|----|----|----|--------|----|----|----|
| 31         | 30 | 29 | 28 | 27     | 26 | 25 | 24 |
| RESERVED21 |    |    |    |        |    |    |    |
| R/W        |    |    |    |        |    |    |    |
| 0h         |    |    |    |        |    |    |    |
| 23         | 22 | 21 | 20 | 19     | 18 | 17 | 16 |
| RESERVED21 |    |    |    |        |    |    |    |
| R/W        |    |    |    |        |    |    |    |
| 0h         |    |    |    |        |    |    |    |
| 15         | 14 | 13 | 12 | 11     | 10 | 9  | 8  |
| RESERVED21 |    |    |    |        |    |    |    |
| R/W        |    |    |    |        |    |    |    |
| 0h         |    |    |    |        |    |    |    |
| 7          | 6  | 5  | 4  | 3      | 2  | 1  | 0  |
| RESERVED21 |    |    |    | WWDRXN |    |    |    |
| R/W        |    |    |    | R/W    |    |    |    |
| 0h         |    |    |    | 0h     |    |    |    |

**Table 5-3513. WDT\_RTIWWDRXNCTRL Register Field Descriptions**

| Bit  | Field      | Type | Reset | Description                                           |
|------|------------|------|-------|-------------------------------------------------------|
| 31:4 | RESERVED21 | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect |

**Table 5-3513. WDT\_RTIWWDRXNCTRL Register Field Descriptions (continued)**

| Bit | Field  | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-----|--------|------|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3:0 | WWDRXN | R/W  | 0h    | <p>WWDRXN: Digital Windowed Watchdog Reaction.</p> <p>User and privilege mode [read], privileged mode [write]:</p> <p>0x5 = This is the default value. The windowed watchdog will cause a reset if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all.</p> <p>0xA = The windowed watchdog will generate a non-maskable interrupt to the CPU if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all.</p> <p>Writing any other value will cause a system reset if the watchdog is serviced outside the time window defined by the configuration, or if the watchdog is not serviced at all.</p> <p>Note: Configuration of DWWD Reaction</p> <p>The DWWD reaction can be selected by the application even when the DWWD counter is already enabled.</p> <p>If a change to the WWDRXN is made before the watchdog service window is opened, then the change in the configuration takes effect immediately.</p> <p>If a change to the WWDRXN is made when the watchdog service window is already open, then the change in configuration takes effect only after the watchdog is serviced.</p> |

### 5.25.2.34 WDT\_RTIWWDSIZECTRL Register

#### 1 WDT\_RTIWWDSIZECTRL Register (Offset = A8h) [reset = 0h]

Windowed Watchdog Size Control configures the size of the window for the digital windowed watchdog.

Return to [Summary Table](#)

**Table 5-3514. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 00A8h       |
| WDT1          | 5210 10A8h       |
| WDT2          | 5210 20A8h       |
| WDT3          | 5210 30A8h       |

**Figure 5-1158. WDT\_RTIWWDSIZECTRL Name Register**

|         |    |    |    |    |    |    |    |
|---------|----|----|----|----|----|----|----|
| 31      | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| WWDSIZE |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 23      | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| WWDSIZE |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 15      | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| WWDSIZE |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |
| 7       | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| WWDSIZE |    |    |    |    |    |    |    |
| R/W     |    |    |    |    |    |    |    |
| 0h      |    |    |    |    |    |    |    |

**Table 5-3516. WDT\_RTIWWDSIZECTRL Register Field Descriptions**

| Bit  | Field   | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|------|---------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | WWDSIZE | R/W  | 0h    | <p>WWDSIZE: Digital Windowed Watchdog Window Size. User and privilege mode [read], privileged mode [write]:</p> <p>Value written to WWDSIZE Window Size</p> <p>0x00000005 100% [Functionality same as the time-out digital watchdog.]</p> <p>0x00000050 50%</p> <p>0x00000500 25%</p> <p>0x00005000 12.5%</p> <p>0x00050000 6.25%</p> <p>0x00500000 3.125%</p> <p>Any other value 3.125%</p> <p>Note: Incorrect value being written to watchdog window size control register</p> <p>If an incorrect value is written to the WWDSIZE field, or if a system disturbance causes the WWDSIZE field to have a value other than 0x5, 0x50, 0x500, 0x5000, 0x50000, or 0x500000, then the window size will be configured to be 3.125%. This increases the chances of getting a reset due to the windowed watchdog, which enables the system to handle the cause for the incorrect configuration.</p> <p>Note: Configuration of DWWD Window Size</p> <p>The DWWD window size can be selected by the application even when the DWWD counter is already enabled.</p> <p>If a change to the WWDSIZE is made before the watchdog service window is opened, then the change in the configuration takes effect immediately.</p> <p>If a change to the WWDSIZE is made when the watchdog service window is already open, then</p> |

### 5.25.2.35 WDT\_RTIINTCLRENABLE Register

#### 1 WDT\_RTIINTCLRENABLE Register (Offset = ACh) [reset = 0h]

RTI Compare Interrupt Clear Enable enable the auto clear functionality for each of the compare interrupts.

Return to [Summary Table](#)

**Table 5-3517. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 00ACh       |
| WDT1          | 5210 10ACh       |
| WDT2          | 5210 20ACh       |
| WDT3          | 5210 30ACh       |

**Figure 5-1159. WDT\_RTIINTCLRENABLE Name Register**

|            |    |    |    |               |    |    |    |
|------------|----|----|----|---------------|----|----|----|
| 31         | 30 | 29 | 28 | 27            | 26 | 25 | 24 |
| RESERVED25 |    |    |    | INTCLRENABLE3 |    |    |    |
| R/W        |    |    |    | R/W           |    |    |    |
| 0h         |    |    |    | 0h            |    |    |    |
| 23         | 22 | 21 | 20 | 19            | 18 | 17 | 16 |
| RESERVED24 |    |    |    | INTCLRENABLE2 |    |    |    |
| R/W        |    |    |    | R/W           |    |    |    |
| 0h         |    |    |    | 0h            |    |    |    |
| 15         | 14 | 13 | 12 | 11            | 10 | 9  | 8  |
| RESERVED23 |    |    |    | INTCLRENABLE1 |    |    |    |
| R/W        |    |    |    | R/W           |    |    |    |
| 0h         |    |    |    | 0h            |    |    |    |
| 7          | 6  | 5  | 4  | 3             | 2  | 1  | 0  |
| RESERVED22 |    |    |    | INTCLRENABLE0 |    |    |    |
| R/W        |    |    |    | R/W           |    |    |    |
| 0h         |    |    |    | 0h            |    |    |    |

**Table 5-3519. WDT\_RTIINTCLRENABLE Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|---------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:28 | RESERVED25    | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                                                                                                            |
| 27:24 | INTCLRENABLE3 | R/W  | 0h    | INTCLRENABLE3.<br>Enables the auto-clear functionality on the compare 3 interrupt.<br>User and Privileged mode [read]:<br>0x5 = Auto-clear for compare 3 interrupt is disabled.<br>Any other value = Auto-clear for compare 3 interrupt is enabled.<br>Privileged mode [write]:<br>0x5 = Disables the auto-clear functionality on the compare 3 interrupt.<br>Any other value = Enables the auto-clear functionality on the compare 3 interrupt. |
| 23:20 | RESERVED24    | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                                                                                                            |

**Table 5-3519. WDT\_RTINTCLRENABLE Register Field Descriptions (continued)**

| Bit   | Field         | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|---------------|------|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 19:16 | INTCLRENABLE2 | R/W  | 0h    | INTCLRENABLE2.<br>Enables the auto-clear functionality on the compare 2 interrupt.<br>User and Privileged mode [read]:<br>0x5 = Auto-clear for compare 2 interrupt is disabled.<br>Any other value = Auto-clear for compare 2 interrupt is enabled.<br>Privileged mode [write]:<br>0x5 = Disables the auto-clear functionality on the compare 2 interrupt.<br>Any other value = Enables the auto-clear functionality on the compare 2 interrupt. |
| 15:12 | RESERVED23    | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                                                                                                            |
| 11:8  | INTCLRENABLE1 | R/W  | 0h    | INTCLRENABLE1.<br>Enables the auto-clear functionality on the compare 1 interrupt.<br>User and Privileged mode [read]:<br>0x5 = Auto-clear for compare 1 interrupt is disabled.<br>Any other value = Auto-clear for compare 1 interrupt is enabled.<br>Privileged mode [write]:<br>0x5 = Disables the auto-clear functionality on the compare 1 interrupt.<br>Any other value = Enables the auto-clear functionality on the compare 1 interrupt. |
| 7:4   | RESERVED22    | R/W  | 0h    | Reserved.<br>Reads return 0 and writes have no effect                                                                                                                                                                                                                                                                                                                                                                                            |
| 3:0   | INTCLRENABLE0 | R/W  | 0h    | INTCLRENABLE0.<br>Enables the auto-clear functionality on the compare 0 interrupt.<br>User and Privileged mode [read]:<br>0x5 = Auto-clear for compare 0 interrupt is disabled.<br>Any other value = Auto-clear for compare 0 interrupt is enabled.<br>Privileged mode [write]:<br>0x5 = Disables the auto-clear functionality on the compare 0 interrupt.<br>Any other value = Enables the auto-clear functionality on the compare 0 interrupt. |

### 5.25.2.36 WDT\_RTICOMP0CLR Register

#### 1 WDT\_RTICOMP0CLR Register (Offset = B0h) [reset = 0h]

Compare 0 Clear compare value to be compared with the counter to clear the compare0 interrupt line.

Return to [Summary Table](#)

**Table 5-3520. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 00B0h       |
| WDT1          | 5210 10B0h       |
| WDT2          | 5210 20B0h       |
| WDT3          | 5210 30B0h       |

**Figure 5-1160. WDT\_RTICOMP0CLR Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COMP0CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COMP0CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COMP0CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COMP0CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-3522. WDT\_RTICOMP0CLR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | COMP0CLR | R/W  | 0h    | <p>COMP0CLR: Compare 0 Clear.</p> <p>This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the compare 0 interrupt or DMA request line is cleared.</p> <p>User and privilege mode [read]:<br/>current compare value</p> <p>Privilege mode [write]:<br/>update of the compare register with a new compare value</p> <p>Note: Reset behavior<br/>A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.</p> |

### 5.25.2.37 WDT\_RTICOMP1CLR Register

#### 1 WDT\_RTICOMP1CLR Register (Offset = B4h) [reset = 0h]

Compare 1 Clear compare value to be compared with the counter to clear the compare1 interrupt line.

Return to [Summary Table](#)

**Table 5-3523. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 00B4h       |
| WDT1          | 5210 10B4h       |
| WDT2          | 5210 20B4h       |
| WDT3          | 5210 30B4h       |

**Figure 5-1161. WDT\_RTICOMP1CLR Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COMP1CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COMP1CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COMP1CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COMP1CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-3525. WDT\_RTICOMP1CLR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | COMP1CLR | R/W  | 0h    | <p>COMP1CLR: Compare 1 Clear.</p> <p>This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the Compare 1 interrupt or DMA request line is cleared.</p> <p>User and privilege mode [read]:<br/>current compare value</p> <p>Privilege mode [write]:<br/>update of the compare register with a new compare value</p> <p>Note: Reset behavior<br/>A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.</p> |



### 5.25.2.38 WDT\_RTICOMP2CLR Register

#### 1 WDT\_RTICOMP2CLR Register (Offset = B8h) [reset = 0h]

Compare 2 Clear compare value to be compared with the counter to clear the compare2 interrupt line.

Return to [Summary Table](#)

**Table 5-3526. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 00B8h       |
| WDT1          | 5210 10B8h       |
| WDT2          | 5210 20B8h       |
| WDT3          | 5210 30B8h       |

**Figure 5-1162. WDT\_RTICOMP2CLR Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COMP2CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COMP2CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COMP2CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COMP2CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-3528. WDT\_RTICOMP2CLR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | COMP2CLR | R/W  | 0h    | <p>COMP2CLR: Compare 2 Clear.</p> <p>This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the Compare 2 interrupt or DMA request line is cleared.</p> <p>User and privilege mode [read]:<br/>current compare value</p> <p>Privilege mode [write]:<br/>update of the compare register with a new compare value</p> <p>Note: Reset behavior<br/>A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.</p> |

### 5.25.2.39 WDT\_RTICOMP3CLR Register

#### 1 WDT\_RTICOMP3CLR Register (Offset = BCh) [reset = 0h]

Compare 3 Clear compare value to be compared with the counter to clear the compare3 interrupt line.

Return to [Summary Table](#)

**Table 5-3529. Instance Table**

| Instance Name | Physical Address |
|---------------|------------------|
| WDT0          | 5210 00BCh       |
| WDT1          | 5210 10BCh       |
| WDT2          | 5210 20BCh       |
| WDT3          | 5210 30BCh       |

**Figure 5-1163. WDT\_RTICOMP3CLR Name Register**

|          |    |    |    |    |    |    |    |
|----------|----|----|----|----|----|----|----|
| 31       | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| COMP3CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 23       | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| COMP3CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 15       | 14 | 13 | 12 | 11 | 10 | 9  | 8  |
| COMP3CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |
| 7        | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| COMP3CLR |    |    |    |    |    |    |    |
| R/W      |    |    |    |    |    |    |    |
| 0h       |    |    |    |    |    |    |    |

**Table 5-3531. WDT\_RTICOMP3CLR Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------|----------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 31:0 | COMP3CLR | R/W  | 0h    | <p>COMP3CLR: Compare 3 Clear.</p> <p>This registers holds a compare value, which is compared with the counter selected in the compare control logic. If the Free Running Counter matches the compare value, the Compare 3 interrupt or DMA request line is cleared.</p> <p>User and privilege mode [read]:<br/>current compare value</p> <p>Privilege mode [write]:<br/>update of the compare register with a new compare value</p> <p>Note: Reset behavior<br/>A reset does not generate a compare match, since the compare logic will only be active, when the associated counter block is enabled.</p> |

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025